

MEETING OR CONTACT REPORT

Date of Report: December 1, 1958

Organization & Location: Military Products Division, Kingston	Date: November 25, 1958
	Reported By: G. A. Blaauw
Project: (11) 7000X Committee Investigation of SAC-SAGE Computer	Department: 539
	Follow-up Date:

PERSONNEL PARTICIPATING:
(Place asterisk next to those on
distribution list. Other distribu-
tion show at end of report)

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I. Subject:

The subject of the meeting was the computer which is at present being developed at IBM Kingston for the SAC and SAGE II contracts.

II. Application:

The SAC-SAGE computer is being designed with the objective of meeting the requirements of the SAC contract and the SAGE II proposal. The computer would be available for other applications as a standard production item.

III. Machine Description:

The computer has a performance range of about two to three times the 7090 performance and about six to seven times the FSQ7 performance. The word length would be 48 bits a word consists of 8 bytes of 6 bits each. Any group of bytes within one word may be addressed in one operation. The floating point format consists of one sign bit, eleven exponent bits and thirty-six fraction bits. The instruction address is 18 bits. Memory consists of independent modules of 16,000 words each.

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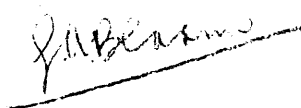
Input-output makes use of DSU channels. Control words are used to specify the memory areas which are used in the data transmission. Main memory is used for control word storage. Data are assembled in a word register and transmitted one word at a time. For the low speed units data are transmitted a byte at a time and assembled in main memory. A high speed drum with a data rate of 2.5 usec. per word and a capacity of 139,000 words is available. In addition ITT is developing another drum for the SAC message center memory. The computer does not have interrupt facilities but periodically scans the input areas. Programmable breakpoint is provided.

A total of 15 index registers is available. One of these is an accumulator register. Index registers are 18 bit transistor registers. The SAC-SAGE computer would have four index registers. Multi-level indexing is possible.

The computer has various SAGE features. One of the most prominent of these features is the ability to split the 48 bit accumulator into two 24 bit accumulators.

IV. Current Status:

The instruction set, suitable for both the SAC and the SAGE contracts, is semi frozen. Delivery of the first SAC computer should be made in spring 1960, which is 16 months after contract date. A manual of instructions will be sent within a few weeks.



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