SAVE

Jan 16, '58

Meeting on 0.5 μsec Mem. & whether to keep in System
S. Dunwell, Presiding.

1. Simulation brings to light for probs done.
   - 2 μs mem. can replace 0.5 μs provided separate from data mem. Consequence of ½ ind logic.

2. 3 areas:
   (1) basic : not imp.
   (2) Sigma : probably not?
   (3) Harvest: significant here

3. Review of Sim. Studys.

1.	"Standard" Case	100 Speed
2.	No FM, 4MM, 16XM	82.
3.	No FM 4MM, NoXM	41.
4.	2MM, 4MM, 16XM	98.
5.	No FM 6MM, 16XM	85.

→ results 10 days on Monte Carlo prob. from simulator (~~24th~~ Jan)
Feb 1 date : on budget.

Cost of 0.5 μs 1025 Mem ≈ 2.0 μs 16K Mem.

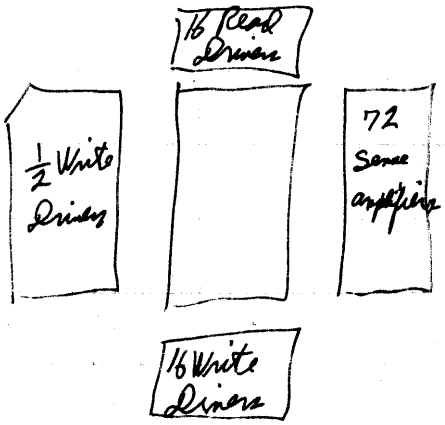
Registers : 0.1 is too fast as is.

→ Question sort out Intermediate results — put in FM.

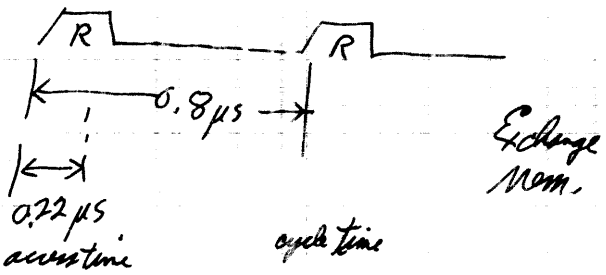
2 Bus system:

→ 2 Mems for Instr., 4 Mems for data. but some bus.

4. High speed cores for Indexing;
   1. Intermediate Data
   2. Index quantities,
   3. Inner loops.
   4. Internal Registers in cores.

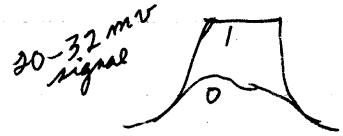


XSTR Count	Wd size
824	16
929	32



another system same transistor count.

NDRO core Times →
- Non-destructive Read Cycle : 0.3 μs. (actually should be 0.1 μs)
- Clear & Write : 0.6 to 0.75 μs (Same as 0.5 μ mem)



Propose: a separate mem. of this high speed for X reg.

How important is Non-destructive Read out vs. regular read-write - (Dura & Bade will do)
exchange memory.

Harvest: Someone -

→ use {0.7 for 0.5 μ mem. cycle