Title: Asynchronous Add-Subtract Circuit
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The diagram below shows one order, or the "i-th" order, of an asynchronous add-subtract circuit. The rectangles A, B and T represent bistable elements or flip-flops for one order of registers A, B and T. The circuit has the ability to combine an augend in register A and an addend in register B to produce a sum in register T and to concurrently subtract the addend from the sum to produce a difference which, if correct, is equal to the augend. Comparing means produce a signal when carries are complete and this signal also indicates that the answer is correct. In the case of 48 digit binary numbers, the longest carry may range over as many as 48 digits but the average longest carry will be only over 6 digits. The present circuit makes possible an average add speed appropriate to the 6 digit carry whereas a conventional adder must necessarily always allow time for the 48 digit carry.

The circuit also has the ability to perform subtraction. In this case a subtrahend is subtracted from a minuend to produce a difference. At the same time, the subtrahend is added to the difference to produce a sum which should be equal to the subtrahend. The comparing circuits operate to check the subtraction and to signal the end of carry propagation.

A six bit model was built using current mode transistor switching circuits, as shown in Docket 5474, and operated satisfactorily at a ten megacycle rate.