Memory locations:

		op	addr	index	decr.	
top of memory: (TC) A_1	A_1	HTR	OPCODE,	0,	$-A_2$	
	C_1	HTR	0,	0,	0	
	T_1	HTR	0,	0,	0	
	O_1	HTR	0,	0,	0	
	I_{11}	HTR	$-A_{j1}$			
	⋮	⋮				
	I_{1n}	HTR	$-A_{jn}$			
	⋮	⋮				
1010 A_i	A_i	HTR	OPCODE,	0,	$-A_{i+1}$	
1009	C_i	HTR	0,	0,	0	complement value
1008	T_i	HTR	0,	0,	0	True value
1007	O_i	HTR	0,	0,	0	output from A_i
	I_{i1}	HTR	$-A_{j1}$ +1 for comp, +2 for True			inputs to A_i
	⋮	⋮				
	I_{im}	HTR	$-A_{jm}$			
A_{i+1}	A_{i+1}	HTR	OPCODE,	0,	$-A_{i+1}$	
	C_{i+1}	HTR	0			
	T_{i+1}	HTR	0			
	O_{i+1}	HTR	0			
	$I_{i+1\,1}$	HTR	$-A_j$			
	⋮	⋮				
	$I_{i+1\,m}$					
	⋮					

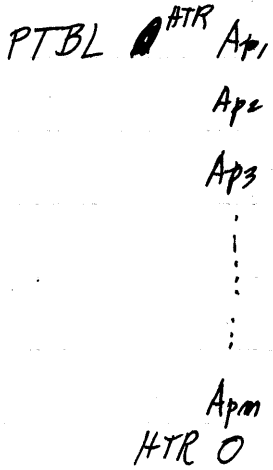
A Delay has only 1 no inputs

AD1 has $-A_1$ in decr.

no ... no of inputs

address: $A_i = A_{i+1} + 4 + m$

Print table:



Data Input:

A1	Logical Element	PTEL Printable	Source Table
A2			B1
			BN
AN			
			B52
ADV			

Note: B's must be located below 4 in memory