August 15, 1957

MEMO TO: Mr. S. W. Dunwell Dr. W. Buchholz SUBJECT: Stretch Evaluation

Product Planning has been examining the 3-in-1 report and contrasting it with our previous position i. e., an integrated, parallel Sigma system with the highest possible performance and a Harvest system with a possible commercial derivative.

There seems to be one main argument for and one main argument against the 3-in-1 concept.

- A. Opinions and statements were made that one integrated program (3-in-1) offered substantial savings in development, manufacturing, and maintenance.
  - B. Opinions and statements were made that the portion of the 3-in-1 system which corresponded to Sigma is more costly in hardware and offers less in performance.

Product Planning is trying to find the answers to these questions, and I am requesting your help.

I am working with the following assumptions, the I/O units, the exchange, the bus, and the memories are common to the 3-in-1 and the two machine concept. The main frames of the 3-in-1 consist of the elements B, H, and S as described. Within the two machine concept the Harvest main frame consists of a B and an H while the Sigma main frame is similar to the parallel S device but contains most, if not all of the functions of B + S.

Operating with this set of assumptions, could you give some statements as to the total costs and estimated savings of the two machine approach and the 3-in-1 approach.

To assist in the determination of any possible performance penalty, I would appreciate the following times:

1. How long is the arithmetic unit interlocked in B (in S) for the operations Load, Add, Multiply, Divide, Store, for both variable field length and floating point?

#### Stretch Evaluation

- 2. What full cycle times are to be assumed for the 512, 1024, 8192, and 16, 384 word units?
- 3. What intermediate time point is to be used during the memory cycle to show the start of data transmission to or from the memory register to other parts of the calculator?
- 4. What are bus transmission times?
- 5. When B and S are attached, does B still operate with only a single instruction overlapped with execution or can it take advantage of the S look-ahead for all operations?
- 6. What are the times involved in the instruction and indexing mechanism for S or Sigma? The following steps seems to be relevant:

a. Advance instruction counter

- b. Instruction address to memory
- c. Memory to instruction register
- d. Decode for possible indexing
- e. Index address to memory
- f. Memory to index register

g. Index instruction register

h. Data address to memory

- i. Instruction to look-ahead register
- 7. What are the similar times for B, including the release of (h.) above in relation to the execution of the previous instruction in the arithmetic unit.

Stretch Evaluation

Obviously, we intend to use these times to compare programs operating on B + S against the same times for programs on Sigma. Our investigation will be on problems similar to the SNG code where computing is the main interest and I/O and editing are secondary. We would like the assistance of Dr. John Cocke since using his program for simulation will shorten the investigation time. Could you release him for this effort?

D. W. Sweeney

DWS:jcv cc: Mr. W. W. Simmons Mr. D. W. Pendery Mr. B. L. Sarahan Mr. J. Cocke Mr. E. F. Codd Mr. J. E. Griffith Mr. J. C. Gibson

& Cocke

### PROJECT STRETCH

# REPORT OF THE 3-IN-1 COMMITTEE

1. Introduction

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Goals Assumptions Approach Problem Characteristics

2. Proposed Solution

Allocation of Functions Interconnection of Units B B + S B + H

3. Consequences of Integration

Advantages Problems Disadvantages

4. Conclusions

Poughkeepsie, N.Y. June 1, 1957

#### REPORT OF THE 3-IN-1 COMMITTEE

#### 1. Introduction

1.1 Goals

The 3-In-1 Committee was formed on May 6, 1957 to study the various proposals for several advanced solid-state computers to see if a compromise solution could be achieved, such that IBM could develop three machine systems with a single integrated engineering program. The committee understood these to be the three systems required about 1960:

- System I This system should satisfy the requirements of those customers who will need a machine for commercial and intermediate technical problems. This machine should be larger and faster than the present 700 Series. It is presumed that System I would serve as the next advance beyond the 705 and 709 systems, and its cost would be within a factor of two or three times the cost of those systems.
- System II This system should satisfy the requirements of a contract which presently exists between IBM and the U. S. Atomic Energy Commission. This system should also serve as a large ultra-high speed general purpose computer for scientific and engineering applications. It is expected that this system would be sold to those customers whose need is for the largest and fastest system obtainable.
- System III This system should satisfy the requirements of a contract which is proposed as a future undertaking between IBM and the Bureau of Ships.

Systems I and II are intended to become production systems for release to the field. System III is intended to be applied to the specialized problems of a single large customer. The majority of the committee had no direct knowledge of these problems beyond the problem characteristics listed elsewhere in this report.

It had been proposed that the three systems have much in common, and that one engineering effort could produce all three systems if certain compromises were allowed. It was the primary goal of the committee to define by June 1, 1957, a machine system consisting of four units, B, R, S, and H, such that:

1. The basic unit, B, preferably operate alone as a respectable computing machine.

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- 2. B + R constitute a high- performance system suited for advanced commercial data processing and intermediate technical computing.
- 3. B + S constitute a system satisfying the requirements of the Los Alamos contract.
- 4. B + H constitute a system essentially the same as that set forth in the Harvest Preliminary Manual.

A secondary goal was to minimize the equipment and complexity of units S, H, and especially R, subject to the constraints of reasonably high performance levels for each system.

From the above statement, it can be seen that:

B + R = System I (Commercial and Intermediate Technical)
B + S = System II (Technical)
B + H = System III (BuShips)

### 1.2 Assumptions

The committee agreed at the outset on a set of basic assumptions which would underlie the considerations:

- 1. That there will be a common bus system interconnecting the various component units of a computing system.
- 2. That all units shall operate asynchronously with respect to the bus system.
- That the principle of the Exchange and I/O equipment as postulated in the Harvest Manual and elsewhere is desirable. (This assumption refers only to the principle of the Exchange and I/O equipment, and does not imply acceptance or rejection of any postulated Exchange or I/O equipment).
- 4. That memories of 2.0 usec, 0, 5 usec and 0.1 usec cycles will be available at 64 bits per word. The counting, or-ing, and clearing in the memories are to be features unique to the B + H System.

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5. That in each system configuration proposed, there will be a unique source of instruction control.

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6. That any combination of the B, B + R, B + S, and B + H central processing units shall have the ability to work concurrently when attached to the bus system. This implies that the systems shall have, at least the ability to be coupled through a common memory.

# 1.3 Approach

In line with the assumptions stated above, the committee elected to restrict its considerations to the central processing unit of the three proposed systems. This means that memories, bus systems, and I/O equipment were taken to be of secondary importance in determining the compromise reached. It was assumed, in addition, that all equipment external to the CPU would be common to all systems.

The committee recognized the relevance of the Sigma, Delta, 750, and Harvest Manuals. The committee further recognized that the Harvest system was defined more precisely at this time than any other Stretch system, and that Chapter 5 of the Harvest Manual represented the latest engineering thinking on most of the topics treated in the Delta Manual. Therefore, the committee agreed that the starting point for a compromise configuration would be the Harvest system. In particular, the concept of machine organization illustrated by Fig. 4.1 of the Harvest Manual was used as a starting point. Report of The 3-In-1 Committee

### 1.4 Problem Characteristics

In order to guide the details of the compromise, the committee listed characteristics of three problem categories:

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### 1.4.1 Commercial

- a. Data is highly structured in hierarchies.
  - (1) Basic unit is the byte, a collection of bits representing a character, digit, or control datum.
  - (2) Fields are composed of variable numbers of bytes, all of one size.
  - (3) Records are groups of fields.
  - (4) A file is a collection of all records of a given type.
- b. Arithmetic is performed on fields of integers, often unsigned, and the ratio of multiplications to additions is comparatively low.
- c. On the average, few arithmetic operations are performed per item brought into memory.
- d. Non-arithmetic operations of importance include editing for input-output formats, code conversion, tabular transformations, and decision operations.
- e. Taken together, the non-arithmetic operations outnumber arithmetic operations in frequency of execution.
- f. The amount of information processed at a time, including programs and frequently consulted tables, currently ranges from ten to five hundred thousand bytes.
- g. The amount of information which must be available for consultation within short periods ranges from a few hundred thousand to several million bytes.
- h. Indexing is important primarily for relative addressing rather than array scanning.
- i. No universal and well-defined symbolism exists for describing problems, and few useful macro-operations are known.

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- j. Most machine time is used on a few different programs. These are usually run many times with frequent minor changes. These usually are changes in the problem and not in its method of solution.
- k. Most programmers are full-time but relatively unsophisticated.
- 1. Sorting and file maintenance are generally performed upon long records with short key fields.
- m. File consultation is not well-ordered; therefore sequentially arranged files have low activity rates. This low activity applies both to records within the file and to fields within the record.
- n. Satisfaction of random inquiries is necessary; problems may be viewed as slow-scale real-time.
- o. Problems are usually ill-defined enough so that the intervention of human judgement at some point is necessary.

### 1.4.2 Technical

- a. The basic data units are signed numbers which may vary over a wide range in precision and a very wide range in magnitude. For problem control, fields of varying size consisting of integers and logical operands are usually introduced.
- b. Arithmetic is usually performed on signed floating-point words, and the ratio of multiplications to additions is comparatively high.
- c. On the average, many arithmetic operations are performed per item brought into memory.
- d. The non-arithmetic operations listed in 1.4.1, d., are present but to a lesser degree. Logical operations facilitate complex program control.
- e. The arithmetic operations outnumber the non-arithmetic operations in frequency of execution.
- f. The amount of information processed at a time currently ranges from four to two hundred thousand words.

g. Large amounts of information are commonly held in readiness for sequential consultation.

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- h. Indexing is important for both array-scanning and relative addressing, especially subroutine control.
- i. Usually there exists a universal and well-defined symbolism for describing problems, and many useful macro-operations are known.
- j. Much machine time is used on short runs of many different problems. These are usually run only a few times between changes which arise as experiments in the method of solving a problem.
- k. Most programmers are part-time users of the machine as a tool for their investigations. However, these programmers are usually sophisticated and competent.
- 1. Sorting and maintenance of long-term files is of secondary importance.
- m. File consultation is well-ordered and activity rates are high (usually 100%).
- n. Random inquiry during a calculation is rare.
- o. Problems are presently so specified that human intervention is performed between machine runs. More sophisticated operation in the future will probably involve more intervention.

### 1.4.3 BuShips

- a. The basic data unit is the byte; integer counts represent a second unit. Bytes are presented for operation in well-defined hierarchical patterns.
- b. Arithmetic is performed on counts; modular arithmetic and logical operations are performed on individual bytes in long sequences.
- c. On the average, many operations are performed per item brought into memory.
- d. Besides editing and code conversion for input-output, particularly facile tabular transformations are required.

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- e. Byte-wise operations considerably outnumber arithmetic operations upon fields.
- f. The amount of information processed at a time is of the same order as in commercial problems.
- g. Large information capacity is needed for sequential consultation.
- h. Indexing is important for relative addressing and especially for array scanning.
- i. Few useful macro-operations are known.
- j. Long and short, frequently and infrequently changing problems all occur.
- k. Programmers are fairly sophisticated.
- 1. Sorting is generally performed on short records with long keys.
- m. File activity rates are high.
- n. Satisfaction of random inquiries during calculation is rare.
- o. Intervention of human judgement usually occurs between machine runs.
- p. Special conditions must be able to interrupt byte-wise operations.
- q. Simulation of counter banks is necessary.
- r. The accumulation of sums and counts in parallel with byte-wise operations is very desirable.

The next section of this report describes the proposed configuration for the three systems to solve the problems characterized above.

FIG. J. CPU CONFIGURATIONS



TECHNICAL SYSTEM B S REAISTER BANK

BUSHIPS SYSTEM B REGISTER BANK H

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#### 2. Proposed Solution

The three central processing units are constructed in tinkertoy fashion from the following units:

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- a, A control unit B common to all systems.
- b. A control unit S required for the Technical System only.
- c. A control unit H required for the BuShips System only.
- d. A bank of high-speed registers, all of uniform construction but supplied in different quantities for the different systems.

With register banks of suitable size, B forms the CPU of the Commercial and Intermediate Technical System, B + S the CPU of the Technical System, and B + H the CPU of the BuShips System (See Fig. 1). It will be noted that the unit R (which was originally postulated for the Commercial System only) has been eliminated.

Underlying the proposed solution is an important principle, that of separating arithmetic and control registers from their controlling circuits. Adoption of this principle enables a register to behave differently as different control boxes are connected, and consequently reduces the degree of duplication of registers in the various systems. A further consequence of adopting this principle is that the control boxes and register bank must be very intimately related, at least as intimately as the three sections of a Type 738 Magnetic Core Storage Unit.

### 2.1 Allocation of Functions in B, S, H

In arriving at the distribution described below, the Committee was guided by certain principles. The more important of these were:

- a. That those functions common to the BuShips and senior Technical Systems be incorporated in the Commercial and Intermediate Technical System together with a minimum of additional functions required to insure a sufficient degree of speed and flexibility to be properly balanced with respect to the memories, exchange, input and output.
- b. That the arithmetic and logic speeds (particularly floating point arithmetic) required by the Technical System should not be prejudiced or compromised in any way.
- c. That those operations desired by BuShips whose general applica tion is too infrequent to justify incorporation in B would be relegated to H.

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One result of applying these principles is that the control units B, S, and H have increasing size and complexity in that order. Another result is that the number of . 1 us registers in the CPU register bank is successively higher in the Commercial, Technical and BuShiga Systems. Figure 1 is intended to convey these relationships, but is not intended to indicate accurately the ratios of size or complexity.

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For all three systems, ultimate control of all processes is centered in a single instruction register and a single instruction counter. These items are accordingly allotted to the control unit B.

Some of the principal properties common to all three systems are as follows:

- a. Word length is 64 bits.
- b. Addressing is binary.
- c. Addresses are assigned to all locations in memory and also to all registers in the register bank (including these used as part of the logical units of B, S, and H). To address a full word location, 20 bits are normally required (for cestain purposes 12 will do). An extra 6 bits are required to specify a bit pesition within a word together with 6 bits to indicate a field length. There will be no gap in the addressing of 2.0 µs and .5 µs memory.
- d. The operand address specified in an instruction may be direct, indirect or immediate. Whichever it is, it may be indexed immediately prior to execution of the instruction by the contents of one or more memory locations.
- e. A break-in system is postulated with essentially the same characteristics as that described in the Harvest Manual.
- f. Operations for which either variable length or full word operands may be used include: binary and decimal (fixed point) arithmetic and a variety of logical operations. In general, full word treatment is a special case of variable field length.
- g. Provision is made for transmitting blocks of data consisting of an integral number of full words between memory locations.

- h. Operations are provided to facilitate editing and card image conversion. These include a somewhat more general table look-up than that provided in the 709 together with a scattered bit load and store for transposing binary arrays.
- i. Any memory location in the .5 us or .1 us memories can be used as an index register for single or multi-level indexing. Certain restrictions exist on the use of 2.0 usec memory for indexing.

Since these properties or functions are common to all three systems, they are incorporated in the control unit B.

It was clear that parallel binary floating point operations properly belonged in S because of the senior Technical requirements. A less powerful serial floating point system was incorporated in B. The serial floating point also uses a binary radix and produces results identical with those produced by the parallel. In this way, a high degree of program compatibility is achieved between the B and B + S systems. When S is attached to B, the serial floating point in B is suppressed in favor of the parallel version in S.

A look-ahead device capable of more than single overlap is considered desirable for efficient operation of the B + S system and is therefore incorporated in S.

The streaming operations as described in the Harvest Manual were allotted to H because it was felt they were insufficiently applicable and too costly to be included in either the B or B + S systems.

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# 2.2 Interconnection of Units

The scheme of organization of B,  $S_{0}$  H, and the high-speed registers is shown in Fig. 2. The B system uses nine similar registers for data and control. Although any register could in theory be used for any purpose, those registers that have the same function in all system configurations are only provided with the switching for that function. Thus, one register is permanently wired as an instruction register; another serves as the accumulator for all system configurations; and so on.

In single-address instructions that require two operands, one is explicitly addressed while the other is implied by the operation code. While some of the high-speed registers can be addressed by implication, they are assigned direct addresses as well. A B, B+S, or B + H system need include only those high-speed registers that are implied by operations for that system, but it may also include others that are used for highspeed memory.

In the B system, registers A, B, C, and C' can be connected to the switch matrices for parallel to serial conversion. Operands pass bytewise through the B logical unit and to the outgoing switch matrix, which can assemble parallel words in C or C'.

When a B + H system is in use, additional controls and centrol registers are needed. Also registers A' and B' are added to alternate with A and B during streaming and thus permit greater simultaneity of memory accesses. Arithmetic operations are performed just as in B alone. Streaming operations have their own controls that govern the connection of A, A', B and B' to the incoming switch matrices and of C and C' to the outgoing matrix. Further, the operands, after being transfermed to serial bytes, pass through the H serial logical unit (including byte masks, table look-up apparatus, etc.) subject to H's controls.

When a B + S system is in use, extra registers are required for instruction look-ahead, as well as additional controls. Logical and variable field length operations are performed just as in B alone. Floating point operations cause the S controls to switch the operands from A and B registers into the S floating point arithmetic unit instead of the parallel-serial switch matrices. The serial floating point mechanism of B is not used in the B + S system.

The very intimate connections of the registers and basic controls to all parts of the several systems present timing and packaging problems that can be very severe. Several of these are treated later, but they all appear solvable.



3-1 HIGH SPEED REGISTER ORGANIZATION

fig. 2

#### 2.3 The B Processing Unit

## 2.3.1 Functions

The B Processing Unit will perform arithmetic operations on variable length fields of up to 64 bits. The arithmetic operations which can be performed are:

ADD
ADD TO MEMORY
COMPARE
DIMINISH
DIMINISH TO MEMORY
DIVIDE
LOAD
MULTIPLY
ROUND
STORE
STORE B

These operations can be performed in binary upon fields of any length up to 64 bits. They may be performed in decimal on fields of up to 64 bits which are multiples of the character size. Character sizes of 1, 4, 6, or 8 bits are permitted for decimal arithmetic. Any field may be signed or unsigned. If it is signed binary, the sign character may be 1, 4, 6, or 8 bits. If it is signed decimal, the sign character is of the same size as the other decimal characters.

A sign modifier is associated with each operation. It causes the sign of the stated operand (implied, in case of ADD TO MEMORY, STORE, and DIMINISH TO MEMORY) to be taken as is, inverted, taken as plus, or taken as minus. An internal 7-bit plus sign shift register may define the positioning of the addressed operand with respect to the accumulater contents.

Indicators signal exception conditions, logical properties of results, and errors.

Arithmetic operations may also be performed on 64 bit binary signed floating point words.

COMPARE is modified in action when floating point is specified.

Additional operations are provided which only apply to floating point numbers. They are:

> ADD SINGLE TO DOUBLE ADD EXPONENT ADD MANTISSA

Special indicators signal outsize or ill-defined results and almost-outsize results, as well as the conditions mentioned above.

The B Processing Unit will form the 16 bit-wise logical connectives of fields of lengths up to 64 bits. The instructions are:

# CONNECT CONNECT TO MEMORY

and operation code modifiers designate which connective is to be formed. Four other operations perform logical counts of binary ones or zeros in the specified operand. The counts appear in the accumulator. The operations are:

> COUNT LEFT ZEROS COUNT LEFT ONES COUNT ALL ZEROS COUNT ALL ONES .

Condition monitoring and testing, branching, and program interruption are performed in a flexible manner. Conditional branching may depend upon any bit in the Accumulator (A) or the Indicator Register. Logical functions of bits in memory are formed in A, while conditions arising during computation are held and monitored in the Indicator Register. This generalized conditional branching includes testing of indexing as a special case. Furthermore, special instructions are provided for counting, testing, and branching.

Unconditional branching may store the contents of the instruction Counter in any location in the memory whose addresses lie below  $2^{12}$ . (This will hereafter be referred to as "12-bit memory".

Facilities are provided so that the programmer may choose which of the 64 conditions signalled in the Indicator Register are to be monitored. The occurrence of any of these conditions causes the program to be interrupted and an alternate program suitable for the signalled condition to be initiated.

Operations associated with branching and program interruptions are:

BRANCH IF A OFF BRANCH IF A ON BRANCH (and) ENABLE(interrupt mechanism) BRANCH IF I OFF BRANCH IF I ON BRANCH COUNT AND BRANCH IF NOT EQUAL COUNT AND BRANCH IF EQUAL IDLE LOAD MASK AND ENABLE NO OPERATION RESET INTERRUPT Report of The 3-In-1 Committee -14-

A fairly sophisticated operand addressing and indexing system is provided in B. Arithmetic and logical instructions provide for addressing a single operand by a 26 bit address, of which 20 designate the memory word and 6 specify the bit within the word which begins the variable length field. Six more bits specify the number of bits in variable length fields. Instructions whose operations can be applied only to full words use the bit address and field length positions to specify a 12-bit second address. The operand address may be immediate, in which case the address itself is used as the operand. It may be direct, so that the effective address after indexing designates the operand. It may be indirect, in which case the effective address after indexing specifies another operand address, which may in turn be immediate, direct, or indirect and may be indexed. Any word in 12-bit memory may be used directly as an index quantity. Any word may be used for indexing by an oblique method.

The index address may be indirect, specifying a multiple index address word. This may in turn specify another. On each level of direct or indirect addressing, any number of index quantities may be algebraically added to the base address to form the effective address. Indexing is uniformly applied to both the word and bit address portions of an operand address.

Each index word contains an index value and a limit. Each time the value is incremented, it is compared with the limit, and indicators are set. Signed increments of up to 26 bits may be used. The operations for manipulation of index quantities are:

> COUNT AND BRANCH IF NOT ZERO COUNT AND BRANCH IF ZERO INCREMENT INCREMENT AND CONDITIONALLY RESET REPLACE L(imit) BY L(imit) REPLACE L BY V(alue) REPLACE V BY L REPLACE V BY V

All of the index manipulative operations use the second address to specify the index register operated upon and the operand address (which may be indexed) to specify the operand such as the increment, branch address, or replacing quantity.

Special operations are provided for transmitting blocks of whole words between locations in memory (including central registers). The operations, one the inverse of the other, are:

### RECEIVE TRANSMIT

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The number of words to be moved are specified by the contents of the designated index word which is counted up until its limit is reached.

Similar operations are provided for moving single bits. In these, however, the bits are received in or transmitted from the accumulator. The full bit address specifies the first operand in memory and a pre-set first level increment (byte size 1-256) designates the distance between bit locations affected in memory. The operations are:

# RECEIVE BITS TRANSMIT BITS

The field length specified applies to the field in the accumulator and, therefore, gives the number of bits to be transmitted.

Input-output operations are controlled by sending the exchange, the address of a control word, the address of an input-output unit, and an operation such as read or write. The operations are:

> CONTROL DISCONNECT LOCATE READ WRITE

A system is proposed in B for performing tabular transformations. The wisdom of providing the extra hardware for this function appears to be an independent question from that of integrating the several systems, and the committee neither recommends nor rejects this feature.

The Table Transform instructions specify binary addition, decimal addition in 1, 4, 6, and 8 bit byte sizes, or one of the 16 Connect operations. It specifies in its word address and index address fields the indexed base address of the table used for the initial transformation. The argument is assumed to be in the accumulator, and the bit address gives the location of the first argument byte, whose byte size is also specified. The field length specifies the number of single byte transformations to be performed.



EXAMPLES OF V.F.L. NUMERIC FORMATS





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and the second

INDIRECT ADDRESS WORD



FORMATS DERIVED FROM INSTRUCTION WORD

*fig.5* 

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The argument byte is added to the base address and the complete word addressed is fetched. This word contains 27 bits of data, 6 bits and sign that give the increment to be used in finding the next argument byte, 7 bits and sign that give the increment to the last data bit address to determine where the data enters the output register, a 20 bit base address for the table look-up of the next argument byte, a bit to stop the look-up process, and a programmer's tag bit. The stop bit sets an indicator as well as stopping the operation. The whole 27 bits of data are used in the operation upon the contents of the output register.

Because of its generality, the system performs code translation, editing for printing, and many other specialized functions.

The operations are:

# TABLE TRANSFORM ADD TABLE TRANSFORM CONNECT

### 2.3.2 Formats

- a. Variable length data fields consist of a number of bits of binary data or a number of 1, 4, 6, or 8 bit decimal bytes. A field may be signed or unsigned. Signed binary fields may have 1, 4, 6, or 8 bits devoted to non-numeric information. Signed decimal fields have a sign byte of the same size as the numerical characters. The sign byte is on the right end of the field, and the assignments of bits within it are shown in the examples of Fig. 3. No field may exceed 64 bits.
- b. Variable field length connect operations are commonly performed on unsigned binary fields.
- c. The format for floating point words is shown in Fig. 4. The tag bits of operands are or-ed to give the tag bits of results. Tag bits and some high-order exponent bits control individual indicators.
- d. The instruction formats common to all systems are shown in Fig. 4. The B + H system also executes streaming instructions whose format is specified below. The discrepancy between the 7-bit operation code in the B instruction format and the 6-bit operation code in the streaming instruction format requires that two 7-bit codes be reserved for each streaming operation.

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The B instruction format designates all B and B + S instructions. The variations within the format are the use of the second address as a unit, slightly different interpretations of bit address and field length in table transformations and bit transmissions, and the different interpretation of the sign and format modifiers for the CONNECT instruction. The bit address and field length of floating point instructions are ignored.

- e. The indirect address word format and that of the multiple index address word are derived from the instruction format and are shown in Fig. 5.
- f. The index word format is closely associated with the exchange control word format, which the committee did not consider. The information content of the index word format of Fig. 4 appears satisfactory.

# 2.4 The B + S Processing Unit

The B + S Processing Unit performs very few operations not performed by B. It is distinguished by the fact that all fleating point operations are performed by a special arithmetic unit and a special look-ahead mechanism which permits necessary delays to be overlapped with other functions, so that the system achieves much more simultaneous operation of its memories, indexing system, instruction access system, and arithmetic system.

a. The floating point operations are done in parallel at a faster speed:

.6 usec for full-word addition, 1.2 usec for full-word multiplication.

- b. Additional indicator and mask bits may be provided for the interrupt system, if needed.
- c. Floating point operations are provided in S to perform a few functions that demand a sub-routine in B. These operations are:

BORROW DIVIDE DOUBLE BY SINGLE SQUARE ROOT

d. Any program written for B will run on B + S (and get the same answers). If the operations specified in c., above, were provided in B, the converse would also be true. It is proposed, however, that these operations actuate in B a separate indicator whenever they are decoded. This instructionunique-to-S indicator is actuated whether B is operating alone or as part of B + S.

# 2.5 The B + H Processing Unit

### 2.5.1 Functions

In spite of the considerable difference in the construction of the Processing Unit contemplated in this report and that contemplated in the Harvest Manual, there are very few changes in function. Since this is so, the functions and formats of the B + H combination will be explained in terms of the differences between these functions and formats as now postulated and those set forth in the Harvest Manual.

- a. Variable field length arithmetic and logic is performed in B. Since single-length registers are postulated for the operands instead of full double-length registers, the organisation and flow of data are somewhat different and some operation times are longer. In particular, the Accumulator (A) must be loaded by a serial rather than a parallel operation, and operands that overlap word boundaries may require slightly more time for operation.
- b. The functions of LENGTHEN and SHORTEN are not provided explicitly. Instead, a seven-bit and sign shift register can be used on any operation to identify the amount by which the specified operand is offset from the right end of the Accumulator. For example, if the Accumulator's contents (in 4-bit decimal) are 653214 and the shift register specifies a shift of + 8 binary positions, an Add order with operand of 1, and using the shift, will form

653214
100
653314

and a subsequent STORE order with shift would deliver 6533.

Blind positions furnish zeros, and signs are properly handled.

The use of this register facilitates many operations, including those upon the exponents of floating point numbers.

The ROUND operation does not perform a shortening, but sets the shift register to the value specified by the effective address and rounds the number according to the next lower digit:

Accumulator Contents:	653264
ROUND 8 (Dec)	
New contents	653364

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- c. Decimal data bytes and sign bytes of binary data may be only 1, 4, 6, or 8 bits long. Binary fields may be of any length up to 64 and bytes for streaming may be arbitrary subsets of 8 contiguous bits.
- d. The serial floating point system and its special operations are a part of B and are therefore a part of B + H.
- e. The INCREMENT AND CONDITIONALLY RESET operation is added. If the value of an index word after incrementation is equal to the limit for that word, the value is automatically reset to zero.
- f. The general indexing system uses a limit for index values instead of a length. The limit remains unchanged in the incrementing process.
- g. The new eperation RECEIVE BITS and TRANSMIT BITS are provided in B and hence in B + H.
- h. The new operations CONNECT TO MEMORY and DIMINISH TO MEMORY are provided.
- i. The new operations TABLE TRANSFORM ADD and TABLE TRANSFORM CONNECT are provided.
- j. Bits in the Indicator Register have some new assignments so that the floating point conditions, greater in number than the four provided, can be properly indicated.
- k. The RESTORE operation is not provided, since the use of limit instead of length makes it unnecessary.
- 1. The eight MERGE instructions are assigned one 7-bit operation code and distinguished by use of the connective modifier.
- m. There is in B a separate indicator which is actuated whenever an instruction unique to H is decoded.

### 2.5.2 Formats

- a. The bit immediately to the right of the sign bit is not necessarily a zero bit. It may be best to make this another programmer's tag bit.
- b. The floating point data format is new.
- c. The Table Word format, a modification of the Index Word format, is new.

d. The Instruction format is modified by reducing the byte size from 3 to 2 bits:

Code	Byte Size
00	8
01	1
10	4
11	6

- e. The Instruction format is modified by increasing the operation code from 6 to 7 bits.
- f. The Stream Instruction format is modified by moving the Logical Unit Signal Invert bit from bit position 62 to position 54, while the fields from 54-61 are moved to 55-62. The operation code still occupies 6 bits, 48-53.
- g. The Stream operations

STREAM INSERT BYTE STREAM LOGIC-ODD PARITY STREAM LOGIC-NON ZERO STREAM MODULAR ADD-CARRY STREAM MODULAR REVERSE SUBTRACT STREAM MODULAR SUBTRACT STREAM MODULAR ADD-ZERO STREAM SELECT

are assigned distinct 6-bit operation codes.

- h. All other operations are assigned seven bit operation codes whose first six bits are distinct from any of the codes assigned the stream operations.
- i. The Threshold value in the Statistical Accumulator is a fixed limit rather than a changing length, so that the Statistical Accumulator is still constructed like the general indexing system.

### 3. Consequences of Integration

The system organisation which has been described results in advantages and disadvantages for each system. In addition, several problems arise which would not accompany a more conventional approach to computer organization. Report of The 3-In-1 Committee -21-

# 3.1 Advantages

The 3-In-I approach has several distinct advantages. Since programming compatibility has been postulated and reasonably well insured, the customer has the option to grow from B to B + S. A growth from B to B + H is likewise possible, but less likely. The B machine will be produced in larger quantities since it occurs not only as a single machine but also as a part of each B + H and B + Sinstallation. Finally, the use of a common B machine has the advantages which were the aim of the original 3-In-1 proposal: reduction in engineering, education, maintenance and manufacturing effort.

It should be observed that a common STRETCH program already would result in engineering savings due to common components and building blocks such as adders, registers and counters. The use of a common B machine greatly expands the area in which reduction of effort is achieved.

### 3.2 Problems

The close integration of the several separate components implied by the proposed system organization generates technical problems. Some of those readily recognized are:

- a. The number and variety of connections between separate units are greatly increased.
- b. The physical separation of closely associated apparatus into different units may cause timing problems due to transmission delays.
- c. When S is added to B, the B decoder must be modified in the process of connection so that floating point instructions are identified as belonging to S.
- d. The same switch matrices are subject to detailed control from two separate units in B + H, and the controlling unit may change from instruction to instruction.

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### 3.3 Disadvantages

The disadvantages of satisfying the BuShips and senior Technical requirements by combining B and H or B and S can be determined by comparing these machines in equipment and function with a Harvest or Sigma machine of independent design. Furthermore, the penalties imposed upon B in order to be able to connect H or S should be noted.

The penalties in equipment can be divided into two groups:

a. Duplication of equipment.

b. Interconnection of control and data paths.

The first group represents a permanent investment in hardware. It concerns B + H and B + S, not B alone. The second group represents an initial investment in design effort and will, in many cases, also represent a permanent hardware investment. It affects B in particular. The problem of interconnection is considerable in machines of the size and speed of B, H, and S. In the proposed machine configurations, an effort has been made to reduce the number of interconnections at the expense of duplicating equipment. Nevertheless, the interconnection problem is very serious. If a closer examination leads to a change, this change is likely to be in the direction of more duplication and less interconnections.

The penalties in function are changes in specifications resulting from the combination of B with S and H.

In the following sections the specific consequences for B, B + H, and B + S will be listed. The discussion concerns itself with instruction centrol, decoding, operation execution, and data flow.

### 3.3.1 B Machine

The B machine, taken alone, contains the equipment which is generally believed to be necessary to perform the functions of an advanced independent data processing machine. An effort has been made to avoid the inclusion of unnecessary equipment and functions in B. The system, as presented, represents a preliminary solution. By no means should the description of the B machine presented be mistaken for a final set of specifications. A considerable effort is still required to arrive at a set of specifications for a B machine. This effort, however, should not greatly influence the conclusions of this report. The instruction counter, instruction register, index register, and associated adder of B will be used in all possible machine configurations. This equipment is not duplicated in H er S. Since there will be a single instruction overlap in B, there must be an effective instruction register. The indexed instructions stay in this register during execution, while the next instruction is being brought from memory and indexed. This register again can be shared by the H and S machines. The requirements for B + H are such that a full register is necessary. In the case of B and B + S, some of the register positions may turn out to be unused.

It has been postulated that any instructions which occur in more than one of the possible machine configurations have identical operation codes and operational results. It furthermore has been postulated that an instruction which belongs to one computer exclusively will have an operation code which is distinct from any other operation code. The operation codes are classified by B in five groups: those pertaining to B, to B or S, to H, to S and the unused codes. The B codes are at all times performed by B only. The codes pertaining to B or S are the floating point codes. They are executed by B when S is not attached; they are always executed by S in the B + 5 system. The H, the S and the unused codes always give an automatic interrupt. These interrupts refer to three distinct indicator bits. Each indication is subject to a mask bit. With the mask allowing an interrupt, the breakin occurs independent of the presence of H or S. H and S do not perform the corresponding operation. When the mask does not allow a break-in, the operation is performed by H or S, if attached, otherwise the instruction is ignored. The unused codes are always ignored when break-in is disallowed. H and S each have a decoder which is able to distinguish the operations performed by the machine itself. After completion of an operation performed by H or S, a back signal is supplied to B so that the instruction counter and indexing system can proceed.

B also contains a preliminary decoder associated with the instruction register which determines if any indexing operations should be performed.

The dataflow paths of B are not affected by attaching S to the system. The ability to connect H, however, introduces considerable complications because of the desire to share the parallel-serial switch matrices. The serial entries and exits to these matrices and the entries to the bit address decoders must be available to H. Report of The 3-In-1 Committee -24-

The indicator system of B should be able to accept overflow-, zero-, and other signals which result from the operations in H or S, as well as signals from the exchange.

### 3.3.2 B + H System

None of the operations performed by H is duplicated in B. Connecting H to B does not affect the operation of B. Both systems have the same degree of look-ahead.

Several of the highly specialized functions desired for B + H are performed in a quite rudimentary manner in B. It seems best to provide separate mechanisms for performing these functions in B and H. This procedure has been followed for the logical unit, the byte masks, and for bit indexing and addressing. A large part of the H machine has no corresponding equipment in B. The equipment required for Table Address Assembly, Table Extract Unit, Statistical Accumulator, Statistical Threshold, Statistical Counter, Match Recognition, and Numbering Counter is in this category. The parallel to serial and the serial to parallel switch matrices represent an in-between case. The equipment is virtually identical for the B and B + H requirements. B requires two s-p and one p-s matrices. H requires three s-p and one p-s matrices. Duplicating the switch matrices in B and H involves extra hardware for the B + H system. It presents a very clean solution to the interconnection problem. Connecting H to B follows the same procedure as connecting S to B. The alternative to this selution is to share the switch matrices of B. with H. H would require one additional p-s matrix. B should permit the 8-bit output of the p-s matrices and the 8-bit input to the s-p matrix to be connected and gated to H. Also the inputs to the bit address decoders should be switched between B and H. This solution is proposed until further facts are known about the magnitude of the interconnection problem which it poses.

### 3. 3. 3 B + S System

The senior Technical requirements appear to imply a look-ahead which goes beyond the simple overlap of instruction decode and execute as available in the B and B + H systems. These look-ahead requirements are satisfied by the equipment in S. This equipment makes use of several registers in the high-speed register bank to store a series of effective instructions. It is proposed that instruction access, index access, and instruction modification proceed for B + S in the same manner as for B or B + H. A careful timing study will have to verify whether this Report of The 3-In-1 Committee -25-

assumption is valid. Once an instruction is modified, it is moved to one of the "effective instruction" registers. The controls in S keep track of the effective instructions as they are being executed in the proper order by B or S. Every time an instruction is executed a signal is supplied to B indicating that a new instruction may be obtained from memory. Several instruction types require different treatment. Among these are branch and block, transfer instructions. They are recognized by a preliminary decoding in the B machine. The special recognition of these instructions is also required for B operating as a single machine, and consequently does not form an added complication or equipment duplication.

It may be concluded, for the look-ahead requirements for S, that:

a. They represent a considerable amount of equipment in S.

- b. they influence only to a minor degree the equipment in B.
- c. the instruction control of B should be designed simultaneously with the look-ahead control of S, and an appreciable amount of ingenuity will'be required to have both function in harmony.

Attachment of the S machine to the B machine requires that decoding of floating point codes in B be disabled. Floating point sperations are no longer performed in B. The floating point switching circuits in B are idle and form duplicate equipment in the B + S system.

The S machine communicates directly with the data registers which are part of the high-speed register bank. All controls for floating point operation are contained in S. There is no need for direct interconnection between the S and B machine as far as data paths are concerned.

The S machine may equally well be connected to a B + H machine as to a B machine.

In the proposed solution, all variable field length logic and arithmetic operations are performed in B. S performs only the fleating point instructions in parallel and at high speed. An investigation has shown that performing the variable field length instruction in parallel in B would give only a small speed advantage at a considerable cost to the B system. The speed advantage of the parallel system was obtained for fields larger than 20 bits. For smaller fields, the serial system is faster. For both systems, the actual speed of execution was strongly influenced by the memory access time. Report on The 3-In-1 Committee -26-

Another approach would be to provide S with a parallel variable field length unit. In this case, the useful equipment in B would be reduced to the instruction modification equipment and the equipment required by a few remaining instruction types, such as, Branch and Receive-Transmit. It was concluded that with a parallel variable field length unit in S:

a. the amount of equipment duplicated in B and S is considerable,

- b. the amount of equipment in B which is being used in B + S is small,
- c. the problem of interconnecting B and S is equally complex, and as a result,

d. the idea of combining B and S might as well be abandoned.

It follows from the above-mentioned alternatives that a B + S system would require parallel floating point arithmetic in S and serial variable field length operations in B. This system in turn must be compared with a senior Technical machine of independent design. For such a machine, an integrated parallel arithmetic and legical unit would probably be desirable. A detailed engineering study would have to be made of such a machine before any definite conclusions about such a machine could be made. However, it is likely that arithmetic speeds could be maintained in spite of the use of the parallel adder for logical functions. A preliminary investigation indicates that the independent technical computer would involve somewhat less equipment than the B + S combination.

In addition, a speed advantage would be obtained for variable field operations on fields larger than 20 bits. The option would exist to improve this speed advantage at the expense of further equipment. This option does not exist in the B + S system. On the other hand, the B + S system has a small advantage in instruction flexibility in addition to the advantages of the integrated approach mentioned above. In particular, bit transmission and changes in byte size are handled more conveniently in the B + Smachine.

As far as engineering effort is concerned, the B + S approach has the initial disadvantage of the problems connected with integrating two machines. The detailed design work is reduced considerably by a common B unit. The independent technical machine has less problems in the development stage but requires a design effort which largely duplicates the design effort on B.

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The relative size of B, H, and S machines and the degree of duplication in the B + H and B + S systems will be listed for the convenience of the reader. The estimates upon which these figures are based have not been made by the 3-In-1 Committee, but have been derived indepently hy Stretch Systems Engineering. They represent a first approximation based upon preliminary layouts for each machine. The figures for S are based on extrapolation rather than estimation. The figures for H and S do not include the general purpose high-speed registers.

With the B machine of the order of 65,000 transistors taken as 100%, the percentages for H and S are 170% and 100%. Compared to the basic machine, the B + H machine is 270%, the B + S machine 200% and the B + S + H machine 360%. The last figure is not 370% since H and S use a few data registers in common. The duplication in the B + H machine is 4.5% of the total B + H equipment. When it is decided to duplicate the switch matrices of B in H, the total amount of duplication becomes 8.5% of the total B + H equipment. The duplication in the B + S machine is estimated at 1% of the total B + S equipment. The B + S combination is estimated to be 7% larger than the central processing unit of a technical machine of independent design.

#### Conclusions

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All of the following conclusions were reached unanimously:

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- 1. It is possible to set forth a workable 3-In-1 system meeting our goals, with the possible exception of price.
- 2. We believe that the system described herein is such a solution.
- 3. The B Machine has a more sophisticated logical design than previous machines, and even if it were built with the same components, it would be more powerful and flexible than 700 series machines.
- 4. While the B machine is small in the 3-In-1 context, it is a large and powerful machine in its own right and is intended for advanced applications.
- 5. The B + H system suffers little in performance because of integration into the 3-In-1 system, and duplication of equipment is on the order of 5% of the total B + H central processing unit.
- 6. The Harvest system is readily separable into a specialized unit H and a general purpose unit B. If the system is to be built, this separation should be preserved.
- 7. Integration into the 3-In-1 system has caused no compromise in the floating point arithmetic speeds of the Sigma system.
- Integration into the 3-In-1 system limits the logical and variable field arithmetic speeds obtainable for the Sigma system. If faster speeds for these operations are needed, the 3-In-1 approach must be abandoned.
- 9. An independent senior technical computer could perform most of the functions of B + S, and offer the possibility of adding equipment to increase logical and variable field length operation speed. Preliminary investigation indicates that such an independent machine could be built with slightly less hardware than B + S. Further engineering study would be necessary to establish equipment comparison more precisely.

The conclusions are intended to summarize the facts disclosed by the committee's study. They do not represent a recommendation of any course of action.

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