HARVEST REPORT #6

Subject: Arithmetic and Logical Unit

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The following specifications define the requirements of the Arithmetic and Logical Unit (ALU) in general terms.

Input

The input to the ALU will be one or more streams of bytes from Continuous Stream Registers #1 and #2. The ALU will process the operand from one stream, or the operands from both streams in parallel, at the basic 0.2 microsecond pulse rate of the machine.

Logic

The ALU will be capable of performing the operations AND, OR and EXCLUSIVE OR upon pairs of bytes (in parallel upon pairs of bits within bytes) whose size may be up to the maximum that can be emitted from the Continuous Stream Registers. In addition, it will be possible to negate (invert) the output of Continuous Stream Register #1 and/or the output of the logical unit in lieu of providing additional logical connectives.

Arithmetic

It will be possible to perform modular addition and subtraction on bytes of any size up to the maximum that can be emitted from the Continuous Stream Registers. It is taken for granted that the ALU will be capable of performing decimal and binary arithmetic on numbers in fixed point notation with words of variable size.

Compare

It will be possible to compare two bytes and sense a high, low or equal condition, and to sense the presence or absence of one or more special characters. Moreover, it will be possible to sense a change from a previous condition to the next condition. The point of termination of a stream of comparisons may be designated by a special character in either operand or by a count as indicated in the compare instruction itself.

Output

The output of the ALU will be a stream of characters which can be entered into Continuous Stream Register #3, into the Bit Assembly device or the Accumulator Counter. (It is tentatively assumed that the input and the output from the ALU will not come from and go to the same machine functional unit. A final decision as to the validity of this assumption will be made only after further problem study.) The output stream may consist of sense signals generated in the ALU. Thus a stream of bytes may be effectively mapped into a stream of bits.

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