HARVEST REPORT #5

Subject: Bit Assembly Mechanism

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Machine Specification Report #2 has discussed the general theory of the system by which bits will be assembled as addresses and as re-ordered data. The following are rough specifications for the mechanism necessary to accomplish this function.

Input

The input to the bit assembly mechanism will arise from either or both of two continuous stream registers. These registers will carry within themselves an indication of the number of bits which represent a character of output. This number of lines will be active between the continuous stream register and the bit assembly device.

Prefix-Suffix Register

A 26 bit prefix-suffix register in association with the bit assembly device will provide bits in addition to those which arise out of the continuous stream register mechanisms. It is possible that the capacity of this register will be increased beyond 26 bits. A decision to do so would depend upon the discovery of important problems requiring additional capacity.

Output

The output of the bit assembly device will be a word of not more than 26 bits which can be connected to the memory address mechanism.

Range of Switching

The several bits which represent a character of output from a continuous stream register can be connected in a block to any series of positions of the output stream starting with zero as a minimum up to 15 as a maximum.

Counter

Further examination of problems may reveal the need for a counter whose output would be assembled together with the outputs of the continuous stream registers as a part of each output word from the bit assembly device.

Special Character Storage

A single character storage device will be associated with the bit assembly mechanism to hold a character which the bit assembly mechanism is to recognize as special. Controls will be provided to allow this character to be compared against the characters from either or both of the continuous stream registers. When recognized, the character can cause the output word to be omitted. Alternatively, it may cause special action as yet unspecified.

Control of the Bit Assembly Device

Two words or subwords of data are required to set up the bit assembly device. The first of these is 26 bits of information which are to be read into the prefix-suffix register. We will assume that one will always introduce 26 bits and that any unused portion of the prefix-suffix register will receive zeros. In addition, it is necessary to provide a control word which will indicate the following:

1.	The connection of continuous stream register #1	4 bits
2.	The connection of continuous stream register #2	4 bits
3.	The special character to be recognized	6 to 8 bits
4.	Whether special character is to be checked against one or both stream of information	2 bits
5.	The action to be taken when a special character is recognized	1 bit

Sequential Assembly

The mechanism as visualized takes one or two input bytes in parallel and forms them into an output address together with the prefix-suffix information. It may be necessary to accept up to four bytes in time sequence from one input stream for each address formation. If needed, this requirement would not appreciably alter the basic mechanism but rather appears as primarily a control problem. It will be elaborated in future reports dealing with control.

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