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HARVEST REPORT #1

Subject: Continuous Stream Register

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It is commonly necessary for streams of information to flow continuously for extended periods between memory and the logical mechanism. In many cases two or more streams will be flowing into the logical unit and a single stream out of the logical unit simultaneously.

Each stream will provide a character (byte) at a time, with the numbers of bits in a character (byte) being defined individually for each stream, and being any number of bits from 1 to 6. The character rate should be 0.2 microseconds or less per character for each stream.

While in the simplest case, the stream of information will be a simple succession of characters, there must be provision for generating streams of a more complex nature. For example, it may be desired to read out characters 12345, followed by characters 23456, followed by characters 34567, etc. Alternatively, it may be desired to select only particular characters within a memory word under control of another stream serving as a mask. Whenever the sequence is not a simple succession, it is to be assumed that a special instruction mechanism will have been included in the machine to specify and control the nature of the sequence.

Each stream of information will be controlled by an instruction which defines the starting and ending points of that particular stream. The nature of the instruction is discussed below.

In order to provide a continuous stream of characters from a memory which must be addressed a word at a time, it is necessary to provide in association with each stream a pair of single word registers together with an appropriate control mechanism. While one register of a pair is in communication with the logical unit on a character by character basis, the alternate register is

free to communicate with the memory a word at a time. The registers reverse their function as each succeeding word is completed.

Information Required to Command the Register

The control mechanism associated with each stream of information will be set up by an instruction providing the following information.

1. The starting word in memory.
2. The starting character within the word.
3. The number of bits in a character.
4. The number of characters in a group, if groups of characters are to be treated in some special way.
5. An indication of whether the stream of information is to flow from memory to the logical unit or from the logical unit to memory. This presupposes that a single kind of register mechanism can be used to control the flow of information in either direction.
6. An indication of which logical unit and which part of the logical unit the register is to communicate with. Alternatively, this information may be included in a subsequent instruction commanding the operation to be performed by the logical unit.
7. An indication of whether the operation is to terminate or to repeat.
8. An indication of whether or not the data is to spiral, as when reading out 12345, 23456, 34567. When spiraling, it is necessary to indicate by a control of type 1 or 2 when and where to return. It is also necessary to indicate by method 4 or 5 when to terminate. It is further necessary to indicate how many bits or characters to advance on each loop of the spiral.

The termination of the stream of information may be determined in any of several ways, which must in some manner be indicated by the instruction.

1. It may be terminated when the stream has reached a particular point in memory in terms of a memory word and character within word.

2. It may be terminated when a specified number of words or characters has been generated.
3. It may be terminated by one or several of the bit combinations serving as end-of-record marks.
4. It may be terminated by a termination signal from another stream, the signal in this other stream having been generated in any of the above manners. For example, a record mark character in one of the incoming streams would typically cut off the flow of information on all other input and output streams.
5. It may be terminated by a signal from the logical unit.

When two or more streams of information are to flow simultaneously, an instruction word must be given each stream to provide the above information. A subsequent instruction will define the operation to be performed by the logical unit and command the flow of information to start. Once started, it will continue to flow until the designated termination condition has been satisfied.

The size of each of the words which provide the above data and the manner in which they will be assembled to form an instruction can be decided only when the information requirements are known for all classes of instructions.

Looping

Provision should be made for looping or repeating a stream of data of any length without interrupting or terminating the flow of data to the logical unit.

Interruptions to Information Flow

It must be possible to interrupt the flow of information momentarily prior to its termination. The interruption can be in any of the following forms.

1. If any register pair is unable to continue to provide information to the logical unit or to accept information from it because of a momentary inability to communicate with memory, all streams of information should be interrupted until the memory reference can be made.
2. Any one or several streams of information should be

capable of stopping at the end of any character on a command from the logical unit.

3. In some instances one of the streams of information will serve as a mask to control character by character the flow of information from another.

Masking

When one of the streams of information serves as a mask, it can control the processing of the other streams of information in any of many ways. As already noted, it may interrupt the flow of another stream. Similarly, it may cause the injection of additional characters at arbitrary points, or the duplication of characters. On the other hand, it may modify the logical control in any of many ways. The mask may have the same or a different number of bits in each character as the stream which it controls. It may consist of a long stream of information, or of a short stream which repeats itself automatically without interrupting the flow of information from other registers.

This report is concerned only with the data flow aspects of masking. The logical control aspects will be treated in a separate report as one of the classes of logical control.

Form of the Register

In view of the fact that it will be necessary to provide streams of information which are not a simple succession of the characters stored in memory, it will be necessary to arrange the register to switch from any one character of from one to six bits to any character in the same or an adjacent word within a single character time. This precludes the use of stepping registers and similar revolving mechanisms.

Backing Up

When the streams of information are interrupted under control of the logical unit, it will often happen that the signal to interrupt will occur several character cycles after the characters which generated the signal appeared in the stream of input information. In this instance, it may be necessary to back up one or more characters for further special processing before proceeding. The register may have proceeded on to obtain the next word from memory, in

this process destroying the character to which the machine later finds it wishes to return.

There appear to be three basic methods for taking care of the above:

1. Delay memory references until it is certain that the previous word in the register is no longer required.

2. Arrange the addressing system so that it can retrieve an earlier word when further work upon it is found to be necessary.

3. Add a third register to the system.

Both methods 1 and 2 should be provided under program control. Method 1 will be employed when spiraling, at which time a word register will not be released for its memory reference until a spiral both begins and ends within the other register of the pair. This effectively limits the length of a spiral to approximately the size of a single register. When required, longer spirals would be handled by conventional programming. Since spiralling involves the reuse of the data several times, there will be a relatively long period between memory references, such that the delay in the release of the register will not ordinarily affect the operating speed of the machine.

Method 2 will be used to bring the continuous stream register back to an earlier position when a delayed control signal is received from the logical unit. We will have to consider whether it can always be brought back precisely to the desired position, or whether it should be brought back to an arbitrary point known to be sufficiently far and then walked slowly forward to the point in question.

Method 3 is considered to be too extravagant to be used.

The control instruction must include an indication that method 1 or 2 is to be employed. No other instructional data is required.

Speed of Operation

The applications which have been reviewed to date require that the

stream of information proceed at a rate not greater than 0.2 microseconds per character because of limitations imposed by other parts of the system. The present design standards call for a 0.1 microsecond rate, on the assumption that application analysis will later reveal needs for it.

Design

It is proposed to design a single continuous stream register mechanism which is capable of working both to and from memory. The computer would be arranged to accept several, possibly as many as five of these units. The number of continuous stream systems contained in any given computer might depend on the area of application for which it is primarily intended.

IBM is at the present time giving special consideration to the development of a special form of ferrite switching device capable of operating at the required speed of 0.1 microsecond per character. If it should be found that this cannot be developed, the register system would be executed in transistors. In any case, the register control mechanism would be made up primarily of transistors.

While the above presupposes that the continuous stream registers will be individually provided with a complete complement of control mechanism, counters, etc., it may prove more economical to use a single high speed central control unit with a small section of very high speed memory to serve them all. A later Machine Specification Report will cover this subject.

The above will for the time being be accepted as the design standards for the continuous stream mechanism.

Revision: The above is a revision of the original report #1 of July 9, 1956 prepared as a result of the joint conference of July 13, 1956.

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