FILE MEMORANDUM November 20, 1956

SUBJECT: A Machine Organization

During the study of a practical interpretation of the "Look Ahead" features of Stretch, it was shown that a faster version of this feature was possible. The principle timesaving described in previous "Look Ahead" schemes was provided by the elimination of memory reference time from the over-all calculate time for a specific program. The feature of a control arithmetic unit is, for this discussion, not considered one of "Look Ahead."

An analysis of instruction sets indicates that orders are associated with others to make up total thoughts. Many total thoughts are associated in a sequential manner to produce total programs. Almost all of the single thoughts could consist of six or less orders. Within a thought, it is generally not logical to form a summation or difference of more than three factors before performing a store operation.

It was felt that it should be possible to operate on an instruction set by thoughts rather than by single serial instructions and in fact produce a design which would operate on a thought in approximately the propagate time of a single parallel adder.

In order to attain this manner of operation the following ideas were proposed:

1. That instruction registers be divided into three groups of six and that as instructions come from memory that they be defined as families. Each group of instruction registers will be loaded during the time the other group is executing its operations. Each register will have a complete associated decoder.

2. In order that sums and differences can be produced in a minimum time two standard parallel adders would be multiplexed. Three factors could be introduced to the adder and carries propogated in only slightly more time than is required for two factors.

3. In order that store time would not be added to the computing time, two registers would be available for adder sums. One register would be stored while the other was being used for a new sum. The store address would be associated with the accumulator register when the sum is placed in it.

4. Shifting would be done by matrix and could be performed at the time that the adder is gated into the accumulator register.

5. A set of six instructions could be placed in one set of registers and operated upon in a repetitive manner without references to memory for instructions but for new data only.

The mode of design described would produce a multiple address machine with all the advantages of such operation but with the flexibility of a single address machine. By simultaneous decoding of a thought group of orders, the time consumed for non-adder operations would be trivial. As in other "Look Ahead" schemes, memory reference time would be eliminated from the over-all calculate time.

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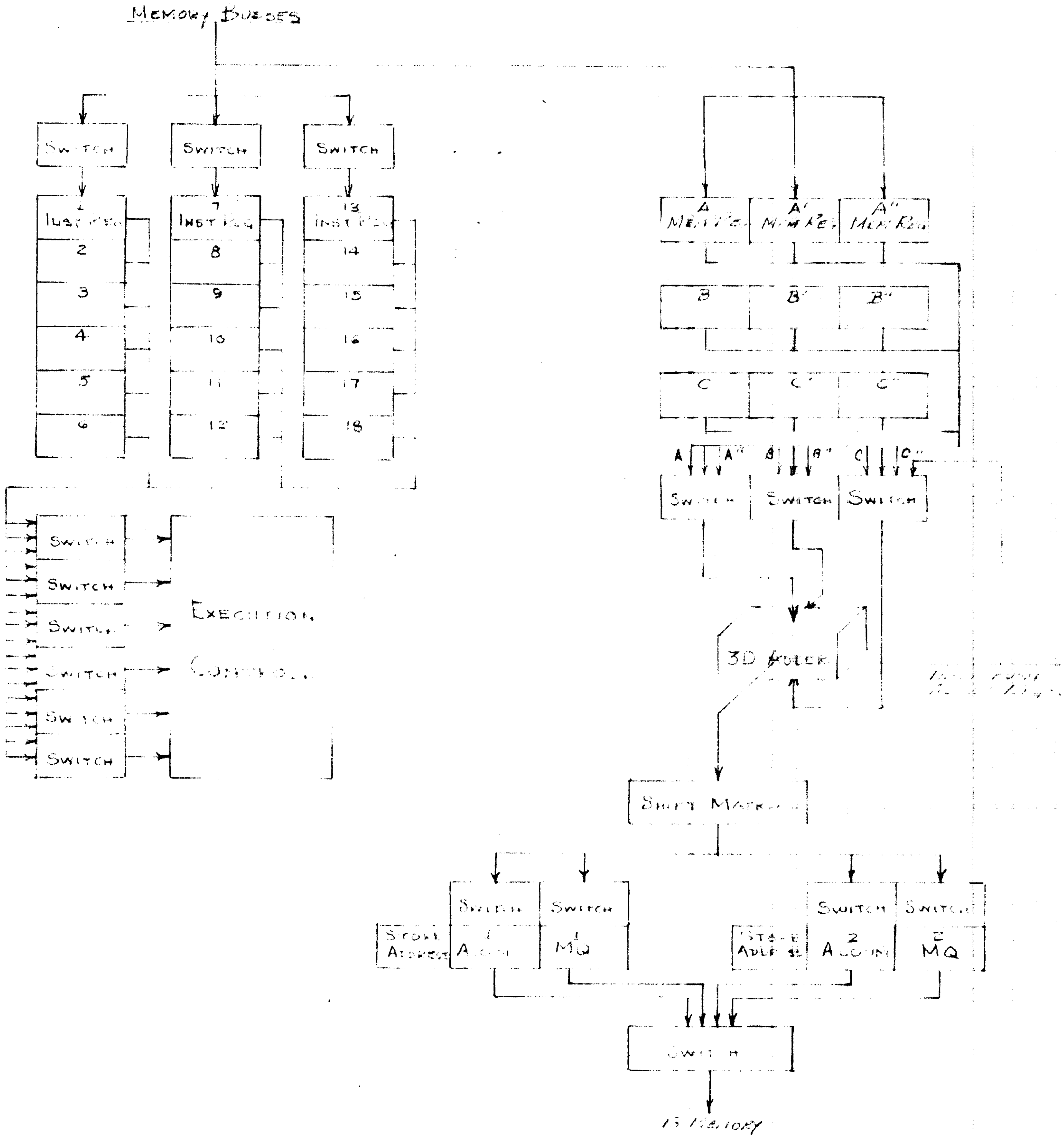
BLOCK DESCRIPTION OF ARITHMETIC SECTION

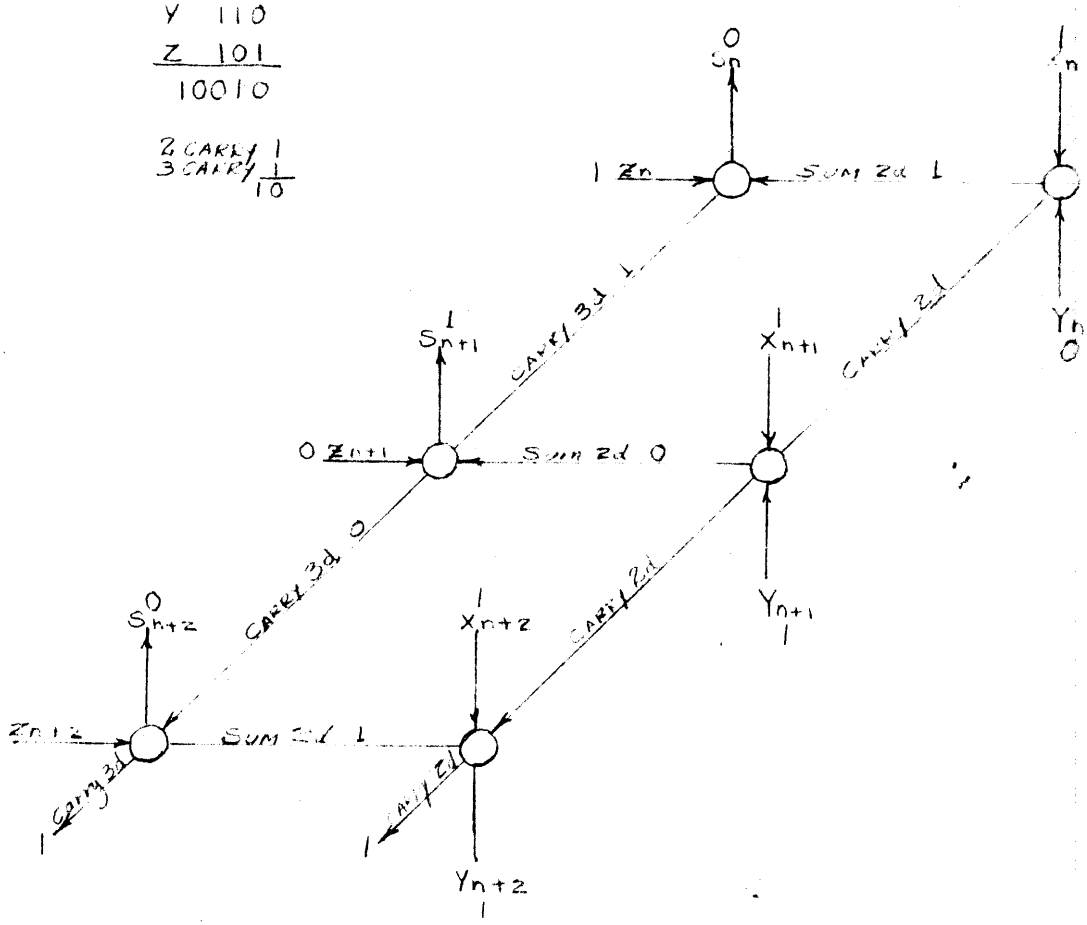


11-20-56

THREE FACTOR ADDER

X 111
Y 110
Z 101
10010

2 CARRY 1
3 CARRY 1
10



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