List of Important Registers in the 7030

I-Box

1Y (64 bits + check bits) Instruction buffer (even-addressed full words)

2Y (64 bits + check bits) Instruction buffer (odd-addressed full words)
(Both 1Y and 2Y may be used as I-box operand buffer)

Z (64 bits + check bits) Instruction ~~decoding~~ Preparation and execution register.

XS (17 words, each with 64 bits + check bits). Index storage (contains locations 1.0, 16.0-31.0)

X (64 bits + check bits) Index data register (buffer register for XS)

X-adder (32 + check bits). Index adder (capable of 24-bit additions)

W (18 bits + check bit) Work register serving misc functions in I-box
(LVS address decoding; second operand address in VFL; refill and interruption address; count for T and swap; LVS "address" decoding)

IC (19 bits + check bits). Instruction counter.

GLAR A left zeros counter for LVS instruction execution ("geometric load address register").

Originals of $XF, $XVLZ, $XVZ, $XVGZ, $XCZ, $XL, $XE, $XH.

I-Checker (shared between I-box and Lookahead)

Lookahead (LA)

LA0, LA1, LA2, LA3 } Lookahead buffer levels, each has
- Op code field (10 bits + check)
- Operand field (64 bits + checks)
- Indicator bit field (15 bits)
- Instruction counter field (19 bits + checks)

plus these bits:

NØØP	no-op bit
WBC	word boundary crossover bit
LAØP	LA op code bit
IC	Instruction counter bit
INT	Internal fetch bit
LC	Level checked bit
LF	Level filled bit
FF	"Forward form" bit
DISC	Disconnect bit

LAAR Lookahead address register (18 + check)

"LAAR Busy" bit

"Store executed" bit

"Forward cycle required" bit

IC buffer (19 + checks)

Counters (each 2 bits):
- IAUC (Instruction-arithmetic unit counter) For LA loading from I-box
- ØCC (Operand check counter). For check of opnd arrived from MBCU.
- TBC (Transfer bus counter). For loading of E-box.
- ABC (Arithmetic bus counter). For interrupt system updating, internal opnd fetch.
- SCC (Store check counter). For storing into main memory.

T.C.C. Oct 1960

Important Registers (cont'd)

Interruption system
- $IND. Indicator register.
- $MASK. Mask register.
- $CPUS. Other CPU.
- $CA. Channel address register.
- Left zeros counter to handle interrupts.

E-box
- $L, $R. Accumulator.
- $SB. Sign byte register.
- C, D. Operand buffer register (each 64 + check bits).
- $LZC. Left zeros counter.
- $AØC. All ones counter.
- SAU. Serial arithmetic unit
  - SAU decoder
  - SAU arithmetic-logical unit
- PAU. Parallel arithmetic unit
  - PAU decoder
  - PAU arithmetic-logical unit:
    - PAU adder
    - PAU multiplier
    - (PAU) F-register

Exchange
- Exchange storage (EM)
- EMAR. Exchange ~~store~~ memory address register. (7 bits + check)
- Word register (communicates with EM) (76 bits)
- MMAR. Main memory address register (18 + check bits) for dealing with MBCU
- Buffer register (72 bits) to handle traffic with MBCU
- Interrupt address register (7+check) to contain address of interrupting channel
- Interrupt triggers for 5 exchange interrupt conditions.
- Interrupt wait bit.
- Multiplexer for dealing with individual channels.
- ECC generator and comparing circuits.

T.C.C. Oct 1960