



DATE January 13, 1960

SUBJECT Complementing Checkerboard
Program
TO PDP Distribution List

FROM John C. Conley

This is a utility program for checking the performance and reliability of the magnetic core memory. It works the memory in the roughest way possible and is self-checking for easy location of faulty or weak cores.

The memory is loaded in a fixed order from the test word, using both the test word and its complement.

The content of each register is then checked, and if correct the content is complemented and stored. The program after initial loading is in a continuous loop of checking, complementing, storing and then checking again, complementing and storing. This will continue indefinitely until the machine is stopped manually or on the location of an error during checking.

The memory plane is loaded in the following order, assuming that the test word is all l's and that the skip instruction in register 1717 is skip on AC positive. This instruction is set by the program and may be a skip on either positive or negative. If negative the loading will be the complement of that shown. Any combination of l's and o's may be used in the test word.

MEMORY PLANE

| | | | | | | | | | | - | | - | | - | | | | | | |
|------------------------|---|---|---|------------|-----|-----|----|----|----|----|-----|----|-----|-----|----|----|----|-------|----|----|
| Register | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 20 | 35 | 36 | 37 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 40 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 100 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | |
| : | | | | The second | | | | | | | | | | | | | | | | |
| 1640 1700) 1740) | 0 | 1 | | Pr | og: | rar | n: | is | in | th | ese | re | gis | ter | 3 | , | | | | |

OPERATING INSTRUCTIONS

- 1. Set Test Word to configuration of 1's and 0's you want to use.
- 2. Set Test Address to 1700.
- 3. Push start switch on console.
- 4. The machine will halt at 1745 (PC = 1746) if an error is detected. The AC will show the address of the register containing the error.
- 5. To locate faulty core, set Test Address to address shown in AC. Push examine switch and locate, core which is incorrect. For example, if 1's and 0's have been loaded, faulty core will have a 1 while the rest of the register shows 0's or just the reverse of this.
- 6. To determine what should be in any register examine program registers 1717 and 1737. If they are the same memory should contain what was loaded initially, if they are different the program is in the complement cycle and the complement of what was loaded should be in memory.
 - NOTE: If this examination is made after a halt at 1745, all registers before the address shown in the AC will have been complemented and so be the reverse of the statement above. Those registers after the address in the AC will be as explained above.

| еу | Address | Instruction | Code | Comments |
|-----|--|--|--|---|
| | 1700 1701 1702 | LAC L DAC D DAC G | 20-1767) 24-1737) 24-1717) | Sets skip instruction for initial lead and check of memory registers 0-157? |
| | 1703 1704 | LAC T DAC F | 20 - 1777) 24 - 1716) | Puts in dummy instruction for initial loading of memory |
| E | 1705 1706 | LAC Z DAC Q | 20 - 1772) 24 - 1775) | Designates first register to be loaded or checked |
| A | 1707 1710 1711 1712 1713 1714 1715 | LAC Q RAR 5 XOR Q DAC M RAR 1 XOR M RAR 1 | 20-1775) 67-1037) 06-1775) 24-1770) 67-1001) 06-1770) 67-1001) | Determines what should be in each memory register |
| F | 1716 | (Dummy JMP D | 76-000 60-1737 | |
| C B | 1717 1720 1721 1722 1723 1724 1725 | (SPA SNA JMP C LAT JMP B LAT & CMA DAC* Q IDX Q | 64) 60-1723) 76-2200) 60-1724) 76-3200) 25-1775) 44-1775) | Loads memory initially |
| | 1726 | SAS V | 52-1771 | Checks for last register |
| | 1727 | JMP A | 60-1707 | |
| | 1730 | LAC R | 20-1774 | |
| | 1731 | DAC F | 24-1716 | |
| | 1732 1733 1734 1735 | LAT DAC W CMA DAC P | 76-2200) 24-1776) 76-1000) 24-1773) | Sets constants from TW for checking |
| | 1736 | JMP E | 60-1705 | Start checking |
| D | 1737 | (SPA (SNA | 64-0200 64-0400 | |

| l | Complementing | Checkerboard | cont'd. |
|---|---------------|--------------|---------|
| | | | |

| roy. | Address | Instruction | Code | Comments |
|--------|--|---|--|--|
| N H | 1740 1741 1742 1743 1744 1745 1746 1747 1750 1751 1752 | JMP H LAC *Q SAD W JMP J LAC Q Halt LAC *Q SAS P JMP N CMA DAC *Q | 60-1746) 21-1775) 50-1776) 60-1751) 20-1775) 76-0400) 21-1775) 52-1773) 60-1744) 76-1000) 25-1775) | Checks memory register and reloads complement. If error is detected halts at 1745 with address of incorrect register in AC |
| | 1753 1754 | IDX Q SAS V | 44-1775) 52 -1771) | Checks for last register |
| Page A | 1755 | JMP A | 60-1707 | |
| | 1 1756 | LAC K | 20-1766) | |
| | 1757 1760 | DAC D DAC M | 24-1737) 24-1770) | Changes skip instruction after each |
| | 1761 1762 | LAC L DAC K | 20-1767) | complete run through of memory for next check and complement cycle |
| | 1763 1764 | LAC M DAC L | 20-1770) | nox oncor and comprenent cycle |
| J. C. | | | | |
| 31 | 1765 | JMP E | 60-1705 | |
| K | 1766 | SPA | 64-0200 | |
| L | 1767 | SNA | 611-01100 | |
| M | 1770 | , | | |
| Л | 1771 | | 001700 | |
| Z | 1772 | | 000000 | |
| P | 1773 | | | |
| R | 1774 | | 60-1737 | |
| Q | 1775 | | | |
| W | 1776 | | | |
| T | 1777 | | 76-0000 | |
| | Design Control | | | |