

IMPROVED PACKET RADIO (IPR) USERS GUIDE

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T/R SIGNAL

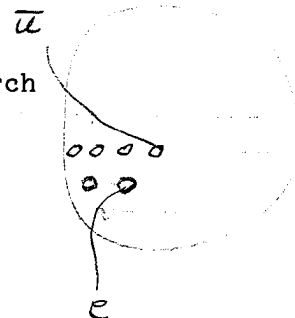
"Tx enable-delayed"

monitor connector (J2)

PIN 2  
GND - 1

WATCH OUT FOR  
LOADING

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the United States Government.

+4V = TX  
0V = RX

SRI International

## CONTENTS

LIST OF ILLUSTRATIONS . . . . .	vi
1 INTRODUCTION . . . . .	1
2 PHYSICAL CONFIGURATION . . . . .	4
2.1 Environmental . . . . .	10
2.2 Power Requirements . . . . .	10
2.3 Fuses . . . . .	13
2.4 Cables . . . . .	18
3 DESCRIPTION OF MODULES . . . . .	21
3.1 Functional Description of the Radio Unit . . . . .	21
3.2 Radio Module Functions . . . . .	25
3.2.1 Frequency Synthesizer . . . . .	25
3.2.2 Encoder/Modulator . . . . .	25
3.2.3 Noncoherent AGC . . . . .	25
3.2.4 SAWD . . . . .	25
3.2.5 Bit Syncs - 100 Kbps and 400 Kbps . . . . .	26
3.2.6 Preamble and Data Detector . . . . .	26
3.2.7 Radio/Digital Interface . . . . .	26
3.2.8 Transceiver . . . . .	27
3.3 Functional Description of the Digital Unit . . . . .	27
3.4 Digital Module Functions . . . . .	29
3.4.1 Memory . . . . .	29
3.4.2 Address Decode . . . . .	29
3.4.3 Central Processing Unit (CPU) . . . . .	29
3.4.4 Master Bus Interface . . . . .	30
3.4.5 Slave Bus Interface . . . . .	30
3.4.6 DMA Channel . . . . .	31
3.4.7 Radio/Station Transmit Interface . . . . .	31
3.4.8 Radio/Station Receive Interface . . . . .	32
3.4.9 Console I/O Channel . . . . .	32

3.4.10	Configuration/Display Interface . . . . .	32
3.4.11	Radio/Digital Interface . . . . .	33
3.4.12	RX Channel Select/TX Carrier Sense Control . . . . .	33
3.4.13	Address Mapping . . . . .	33
3.5	Antenna . . . . .	37
3.6	Ranging Considerations . . . . .	39
4	PERIPHERALS AND INTERFACE DESCRIPTION . . . . .	41
4.1	1822 Interface . . . . .	41
4.2	Console I/O Channel . . . . .	44
4.3	Elapsed Time Clock and Interval Timer . . . . .	46
4.4	Manual Control and Display . . . . .	47
4.5	Radio/Digital Interface . . . . .	49
4.6	Bus Coupler Interface . . . . .	49
4.7	Maintenance Monitor Interface . . . . .	49
4.8	Radio Transmit Interface . . . . .	49
4.9	Radio Receive Interface . . . . .	52
4.10	Hardware Strapping Options . . . . .	53
4.10.1	PR ID . . . . .	53
4.10.2	Auto-restart Enable . . . . .	53
4.10.3	Down-Line Load Enable . . . . .	53
4.10.4	Default RF Frequency . . . . .	53
4.10.5	Initialization Control . . . . .	54
4.11	Power On . . . . .	55
5	OPERATING PROCEDURES . . . . .	56
5.1	Operation/Hardware Strap Options . . . . .	56
5.1.1	Normal Unattended Operation . . . . .	56
5.1.2	Normal Attended Operation . . . . .	57
5.1.3	Maintenance/Test Operations . . . . .	58
5.1.4	Operator Action Following a Fault . . . . .	59
5.1.4.1	LED Fault Display . . . . .	59
5.1.4.2	Console display . . . . .	60
5.2	Initialization . . . . .	61
5.2.1	Causes . . . . .	61

5.2.2	Displays . . . . .	61
5.2.2.1	LED display . . . . .	61
5.2.2.2	Console messages . . . . .	62
5.2.2.3	Error Information Stored in Memory . . . . .	65
5.2.3	Special Test Modes and Procedures . . . . .	65
5.2.3.1	Test Mode Switches . . . . .	65
5.2.3.2	Bootstrap Load and Go . . . . .	66
5.3	Operator Interface for Console I/O . . . . .	68
5.4	Operator Control/Monitor (DEBUG) Commands . . . . .	69
5.4.1	Operation . . . . .	69
5.4.2	Operator Command Input . . . . .	70
5.4.3	Restart Initialization (RS) Command . . . . .	71
5.4.4	Power-Up Initialization (IN) Command . . . . .	71
5.4.5	Halt Jobs (HJ) Command . . . . .	71
5.4.6	Terminate Jobs (TJ) Command . . . . .	72
5.4.7	Execute Jobs (XJ) Command . . . . .	72
5.4.8	Display Jobs (DJ) Command . . . . .	72
5.4.9	Display Memory or Peripheral I/O (DM) Command . . . . .	74
5.4.10	Alter Memory or Peripheral I/O (AM) Command . . . . .	75
5.4.11	Display Job Registers (DR) Command . . . . .	76
5.4.12	Alter Job Registers (AR) Command . . . . .	76
5.4.13	Set Trace Breakpoint (ST) Command . . . . .	77
5.4.14	Clear Trace Breakpoint (CT) Command . . . . .	79
5.4.15	Execute Operator Routine (GO) Command . . . . .	79
5.4.16	Console Load (LD)/Load Verify (LV) Commands . . . . .	80
5.4.17	Down-Line Load (DL)/Load Verify (DV) Commands . . . . .	82
6	CHANNEL ACCESS PROTOCOL . . . . .	83
6.1	Packet Header Format . . . . .	83
6.2	User Definition of Packet Header . . . . .	87
7	MAINTENANCE . . . . .	90

7.1	Hardware Maintenance . . . . .	90
7.2	Diagnostic Software . . . . .	90
7.2.1	CPUDG1 (CPU diagnostic) . . . . .	91
7.2.2	RAMD (RAM memory diagnostic) . . . . .	91
7.2.3	HSRSD1 (Straps/restart diagnostic) . . . . .	91
7.2.4	DMADG2 (DMA I/O diagnostic) . . . . .	91
7.2.5	LNKTS4 (Link test support program) . . . . .	91
7.2.6	MSCD (Miscellaneous function diagnostic) . . . . .	92

APPENDIX:

PERFORMANCE SUMMARY . . . . .	94
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## ILLUSTRATIONS

1	IMPROVED PACKET RADIO UNIT . . . . .	5
2	SEPARATION OF IPR RADIO AND DIGITAL UNITS . . . . .	6
3	IPR DIMENSIONS - FRONT VIEW . . . . .	7
4	IPR DIMENSIONS - SIDE VIEW . . . . .	8
5	IPR DIMENSIONS - TOP VIEW . . . . .	9
6	AC/DC VOLTAGE CONVERTER . . . . .	11
7	FRONT OF THE IPR WITH DOORS OPEN . . . . .	14
8	BACK OF THE IPR DIGITAL SECTION WITH DOORS OPEN . . . . .	15
9	BACK OF THE IPR RADIO UNIT WITH THE DOOR OPEN . . . . .	16
10	BACK OF THE IPR DIGITAL UNIT WITH THE DOOR CLOSED . . . . .	17
11	SIDE VIEW OF THE IPR RADIO SECTION . . . . .	19
12	IPR RADIO UNIT CIRCUIT BOARDS . . . . .	22
13	IPR DIGITAL UNIT CIRCUIT BOARDS . . . . .	23
14	FUNCTIONAL DIAGRAM OF THE IPR RADIO UNIT . . . . .	24
15	FUNCTIONAL DIAGRAM OF THE IPR DIGITAL UNIT . . . . .	28
16	ADDRESS MAPPING WITH CPU BIAS AND LIMIT REGISTERS . . . . .	35
17	CPU ADDRESS MAPPING INTO BUS ADDRESS SPACE . . . . .	36
18	IPR ANTENNA FOR MOUNTING ON A HELICOPTER . . . . .	38
19	1822 INTERFACE CABLE SPECIFICATION . . . . .	42
20	I/O CABLE PIN DEFINITIONS . . . . .	45
21	IPR DIGITAL UNIT STATUS LIGHTS . . . . .	48
22	IPR RADIO/DIGITAL INTERFACE CABLE - TRANSMIT PORTION . . . . .	50
23	IPR RADIO/DIGITAL INTERFACE CABLE - RECEIVE PORTION . . . . .	51
24	DEFINITION OF INITIALIZATION SECTION IDS . . . . .	63
25	DEFINITION OF INITIALIZATION ERROR CODES . . . . .	64
26	PACKET HEADER FORMAT . . . . .	84

## 1 INTRODUCTION

The Packet Radio Network (PRN) provides a capability for geographically separated fixed and mobile digital terminals to reliably communicate with each other. Protection against jamming is provided by spread spectrum signalling. The system has the potential for RF coexistence such that, in general, it may be deployed in a frequency band assigned to other systems without significant interference. The PRN is designed to accommodate a wide variety of computer communication traffic requirements with essentially error-free performance.

A typical Packet Radio Network contains three primary functional elements: host computers, stations, and Packet Radio (PR) repeaters. Any or all of these elements may be mobile. The users access the network via terminating computers which support devices such as keyboard terminals, displays, or sensors. The stations have the responsibility for overall management of the network including initialization, routing, traffic control, and directory functions. Some host computers may serve as gateways to other networks, and some may act as concentrators for sensor systems, e.g., radar tracking and acoustic sensors. Depending on the terrain, repeaters may be necessary to extend the geographic range of the network and provide adequate connectivity for mobile units.

Each host computer (or station or gateway) is "connected" into the network through a local Packet Radio (PR). The network communications traffic is formed into discrete digital segments, called packets, and transferred between the PRs via a common RF channel at either 100 kilobits/sec or 400 kilobits/sec. During a typical operation, a user device passes a message to its PR. This message is then radio transmitted from PR to PR through the network until it finally arrives at the destination PR, which in turn passes it along to the destination device.

The Packet Radio project was begun in 1973 when an Experimental Packet Radio (EPR) was designed and 29 prototypes built. The EPR, containing a single CMOS microprocessor, was successfully deployed in several testbed networks around the United States. In 1977, an Improved Packet Radio (IPR) was designed to take advantage of the latest advances in digital hardware. The 27 IPRs that have been built utilize the same radio unit as the EPR, but the IPR digital unit contains two fast I<sup>2</sup>L microprocessors. EPRs and IPRs can coexist in the same network and perform the same functional tasks.

This document contains the specifications for the installation of an IPR and its interconnection to a station or host computer. Sufficient information is provided to enable a user to install and operate the PR as an active element in the PRN. However, should questions or problems arise, inquiries should be addressed to:

Rockwell International  
Collins Communications  
Systems Division  
P.O. Box 10462  
MS 401-137  
Dallas, Texas 75207  
(214)996-6980  
Attn: Dr. S. Gronemeyer

The other components of a typical Packet Radio network include the station(s) and internet gateways and terminal interface units (TIUs) which support user access to PRN and internet resources. Questions about station and gateway operation should be addressed to:

Bolt Beranek and Newman, Inc  
Computer Science Division  
10 Moulton St.  
Cambridge, MA 02138  
(617)491-1850  
Attn: Dr. J. Burchfiel

Questions about TIU operation should be addressed to:



SRI International  
Telecommunications Research Group  
333 Ravenswood Ave.  
Menlo Park, CA 94025  
(415)326-6200  
Attn: Dr. D. Nielson

The Packet Radio technology has been developed under the support and direction of the Defense Advanced Research Projects Agency. Questions about the Packet Radio research and development program should be addressed to:

DARPA/IPTO  
1400 Wilson Blvd.  
Arlington, VA 22209  
(202)694-3049  
Attn: Dr. V. Cerf

## 2 PHYSICAL CONFIGURATION

The physical design of the Improved Packet Radio (IPR) corresponds to the major division of the internal electronics. The IPR is divided into two boxes, one mounted above the other. The top box is the radio unit and contains the RF head, antenna, RF conversion stages and the signal processing electronics. The radio section transforms digital data into a radiated RF signal and inversely transforms received RF signals into digital data and timing pulses. The bottom box is roughly 50% wider than the top box and contains the digital unit. The lower box contains memory, interface circuits, and two microprocessors. The digital section of the IPR controls the transmission, reception, and processing of packets.

The IPR may be separated into two boxes by unscrewing the eight phillips screws located in the bracket separating the radio and digital units. While the units are frequently separated in the service depot, there is rarely a need for separation at a field site. Figure 1 shows the IPR as a single unit, while Figure 2 shows the separate radio and digital units.

Dimensional drawings of the IPR are shown in Figure 3 and Figure 4. All dimensions in the figures are expressed in inches to the nearest hundredth. The flanges shown attached to the IPR allow mounting in standard EIA 19" racks. The flanges may be removed for special installations. The antenna may also be remotely located for special applications. Figure 5 shows the clearance required to open the IPR doors.

All doors on the IPR are opened by unlocking the camlocks on the doors. Using a regular flat-blade screwdriver, the camlocks are pushed in, turned counter-clockwise 1/4 turn, and then released. A bracket is

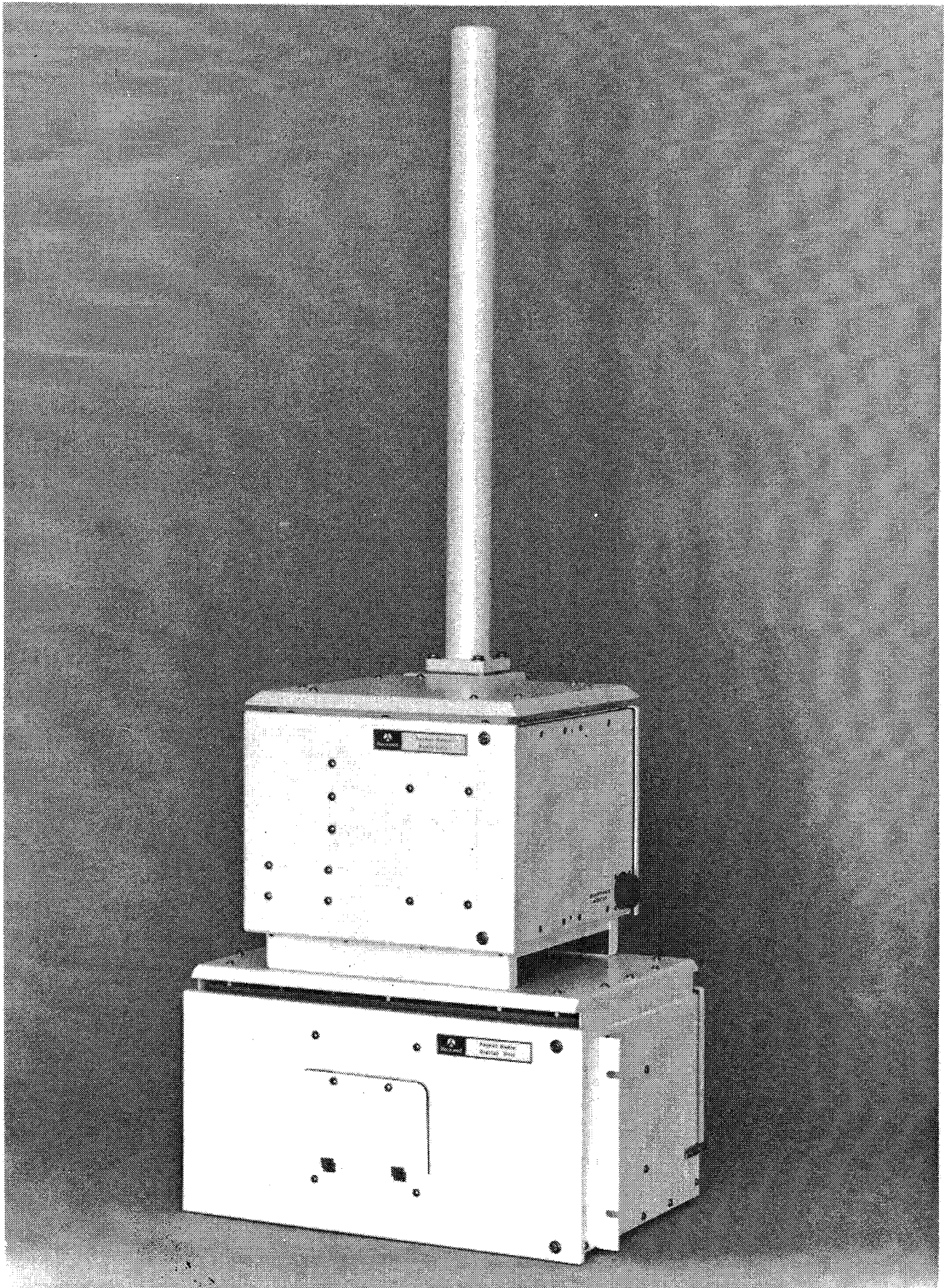


FIGURE 1  
IMPROVED PACKET RADIO UNIT

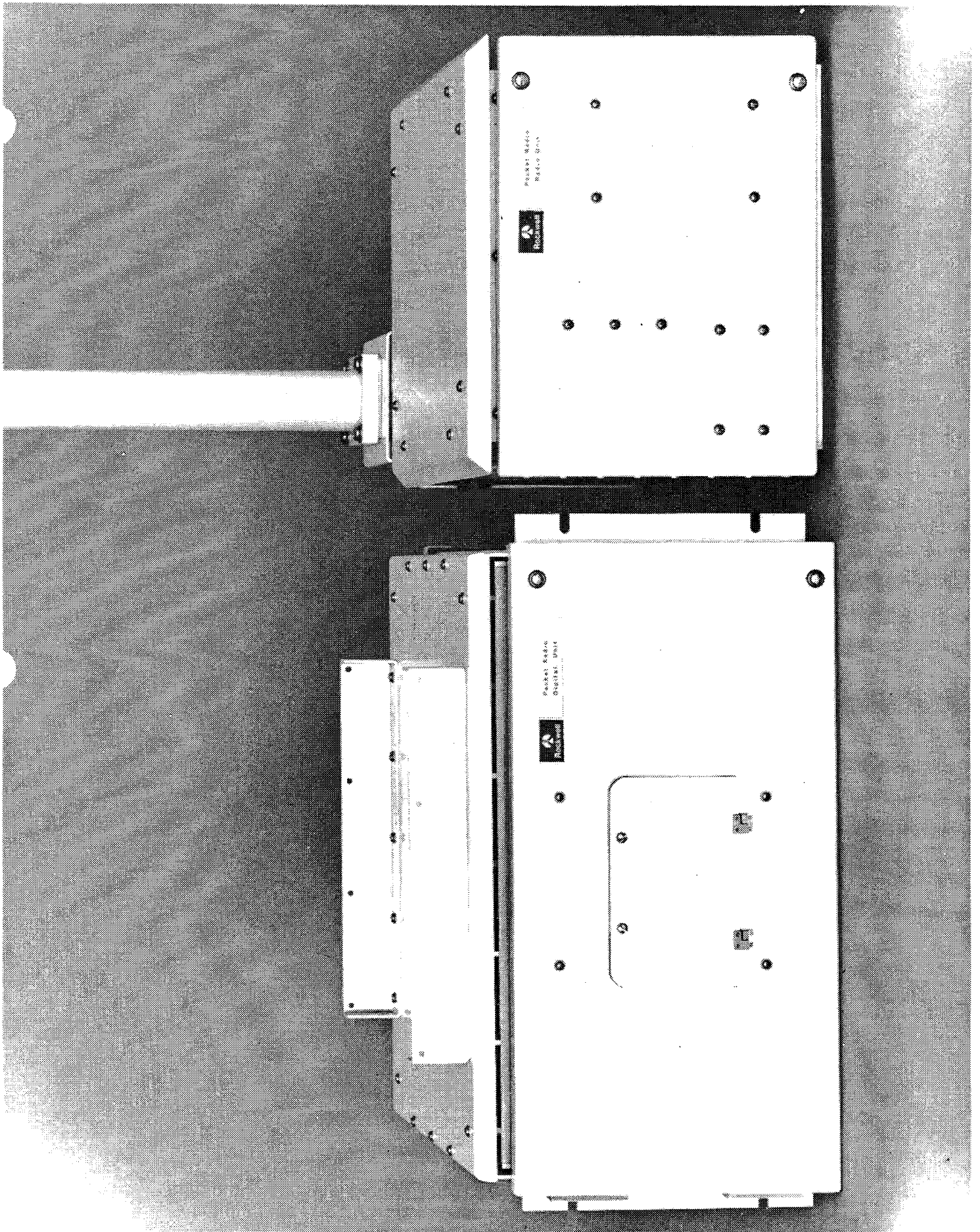


FIGURE 2  
SEPARATION OF IPR RADIO AND DIGITAL UNITS

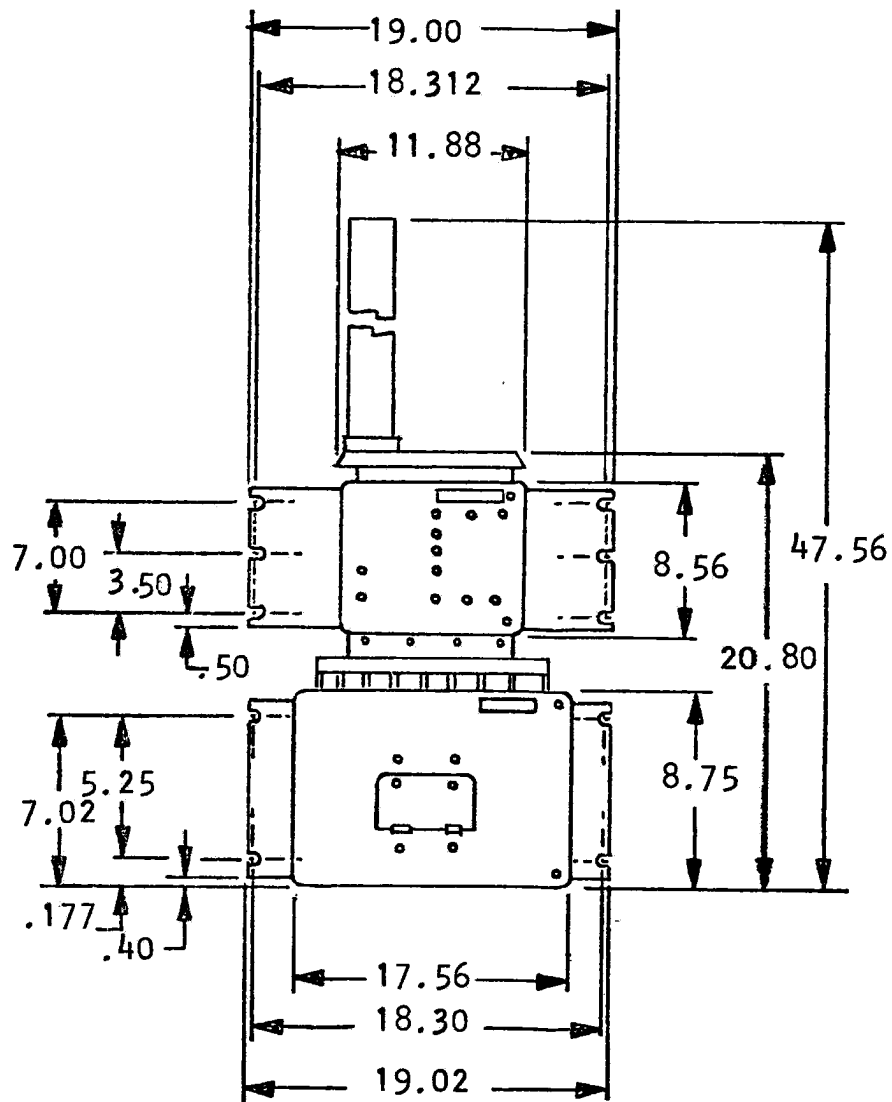


FIGURE 3  
IPR DIMENSIONS - FRONT VIEW

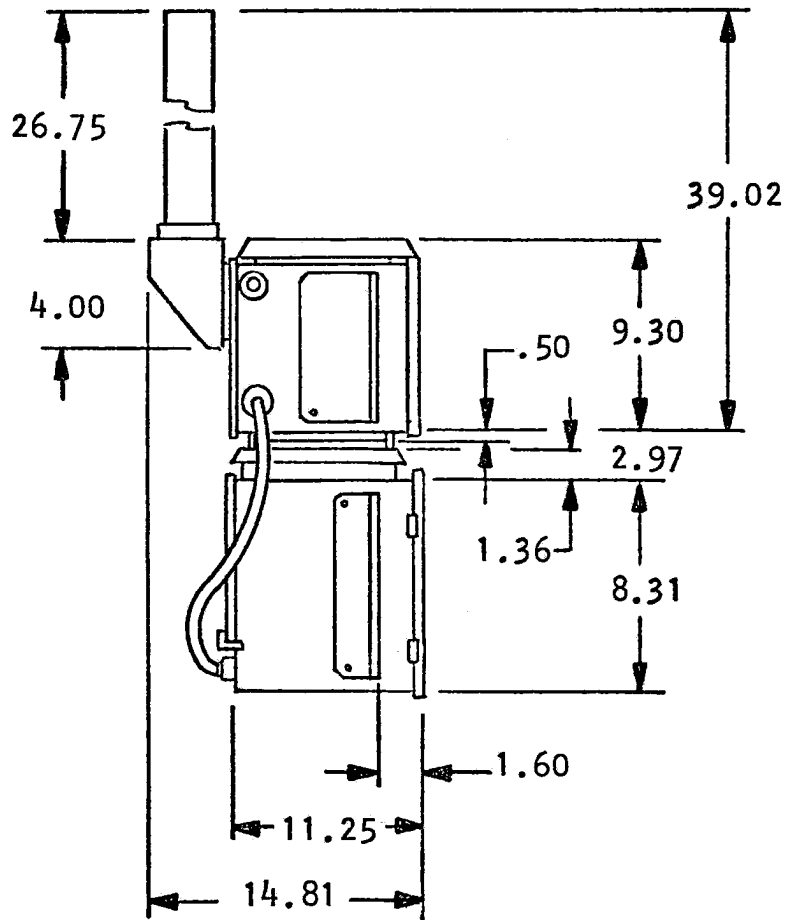


FIGURE 4  
 IPR DIMENSIONS - SIDE VIEW

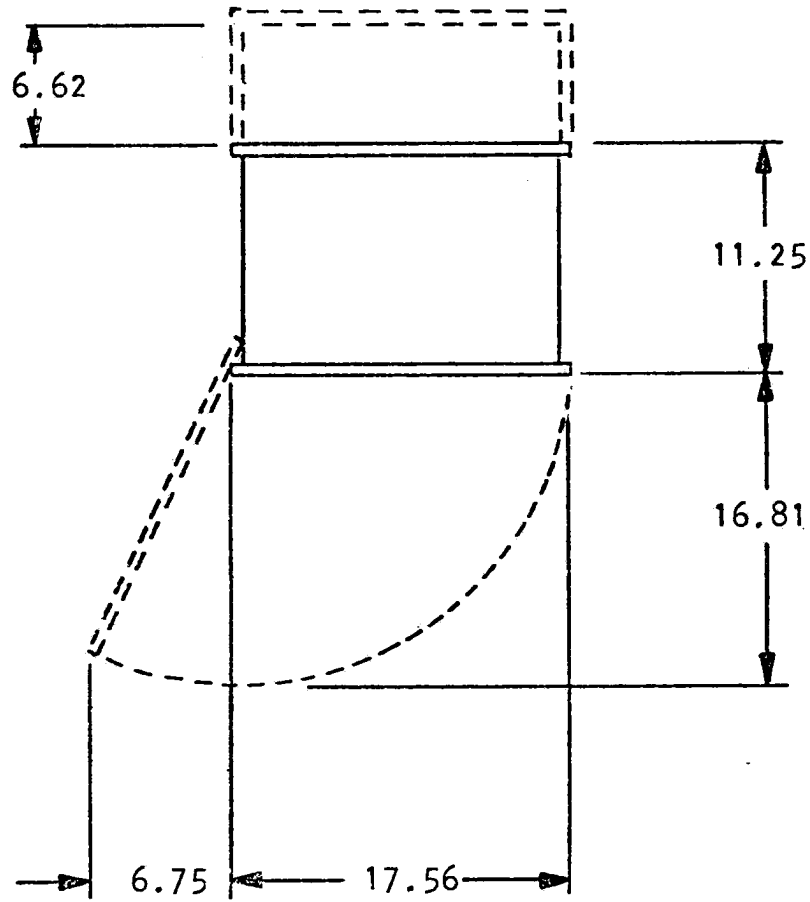
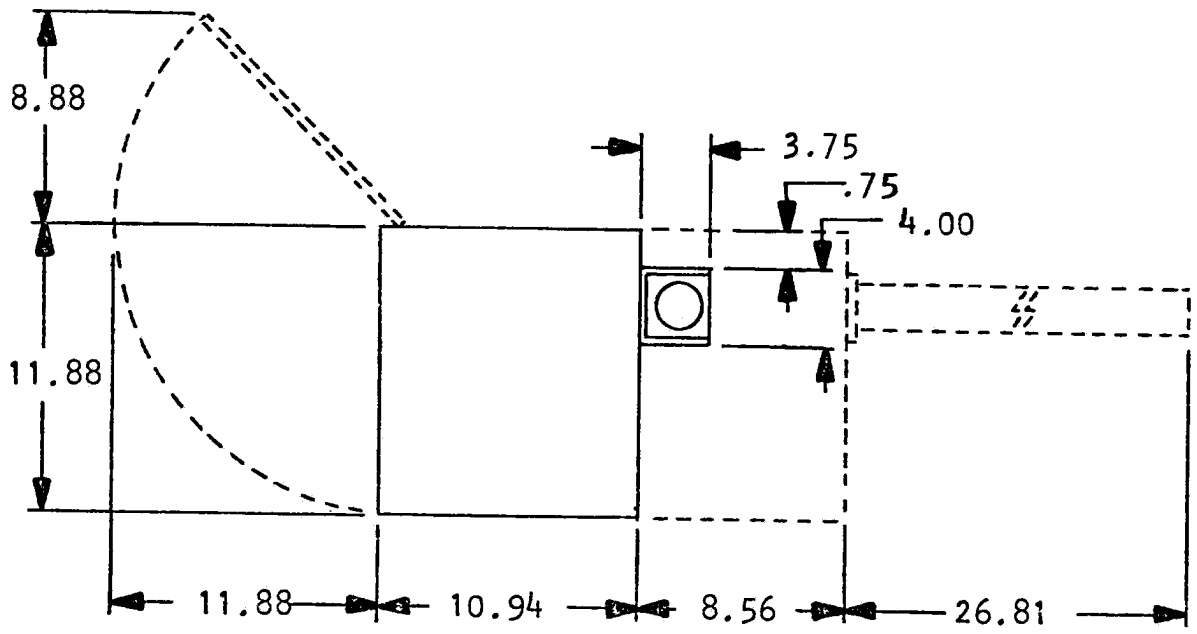


FIGURE 5  
IPR DIMENSIONS - TOP VIEW

provided on the back door of the radio section on which the user may mount the antenna.

## 2.1 Environmental

The Improved Packet Radio meets specifications to satisfy normal environmental conditions. All packet radios will operate in an ambient environment from 0 to 50 degrees centigrade. The units are rain-resistant and will withstand rain being blown at a 45 degree angle to the vertical. The doors are sealed by foam rubber tape to make them watertight. External cable connectors are sealed by watertight rubber gaskets. The units are commercial grade equipment and are not designed for operation in the harsh environments usually encountered by military equipment.

Due to its low power dissipation, the IPR does not require blowers or ducts for cooling. Because all heat dissipation is done by convection, the area beneath the IPR should be kept clear for convection air flow. The front door of the radio unit and the back door of the digital unit act as heat sinks for the DC/DC voltage converters. The rear door of the radio unit serves as a heat sink for the transceiver module.

## 2.2 Power Requirements

The IPR requires a nominal power supply input of 24 VDC, which may be generated by either batteries or an AC/DC converter. Many IPRs are supplied with the AC/DC converter shown in Figure 6. However, any AC/DC converter that satisfies the following power requirements may be used.

Because the radio transmitter consumes a large amount of power, the IPR's power requirements are a function of the transmitter duty cycle. The IPR will use significantly less power in a normal protocol network environment (estimated to be less than 20% duty cycle) than it would in a diagnostic mode with continuous radio transmission. The AC/DC converter supplied with the IPR has two power output plugs and will



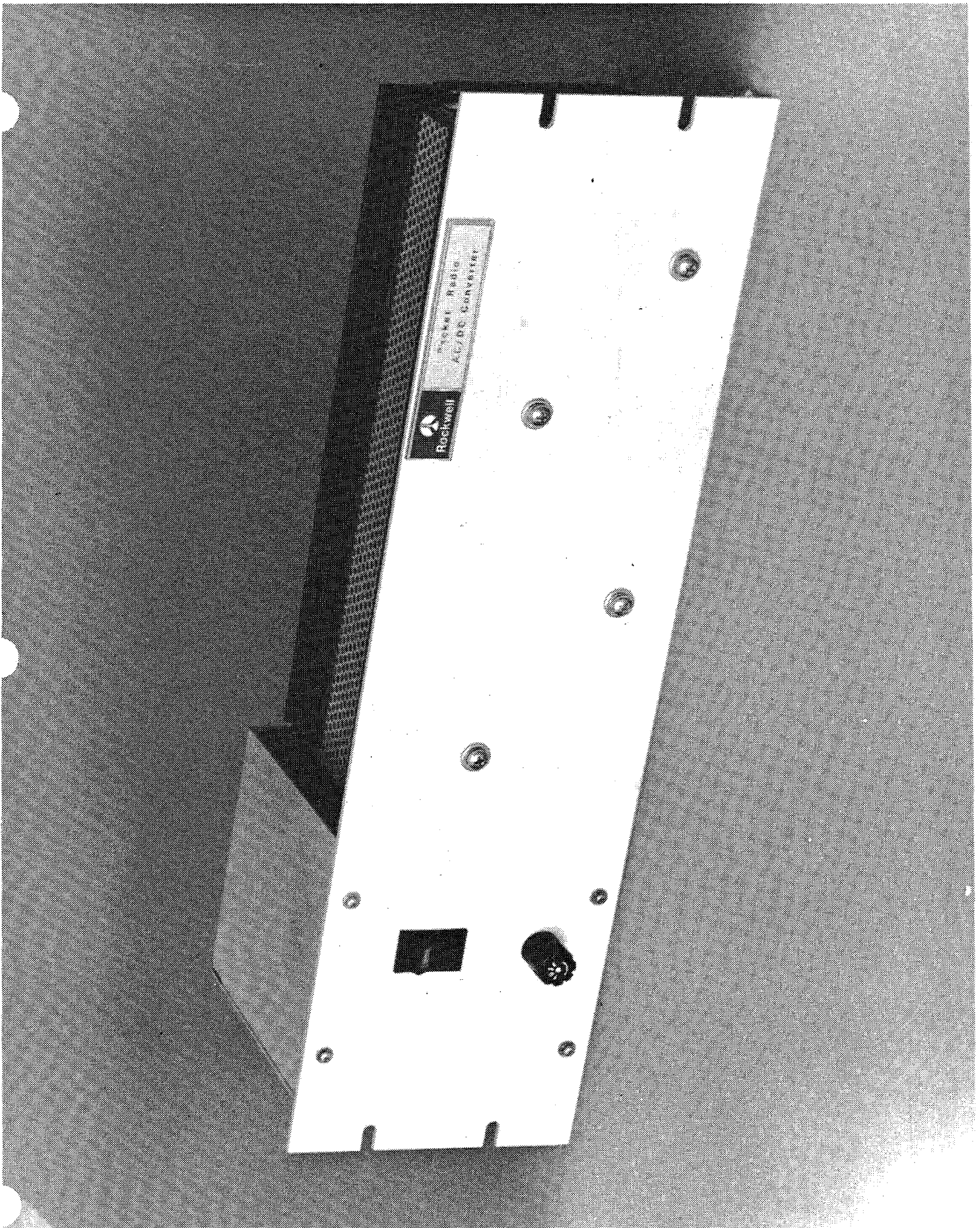


FIGURE 6  
AC/DC VOLTAGE CONVERTER  
- 11 -

provide sufficient current to two IPRs running in a protocol environment. The single converter cannot, however, power two radios in the continuous transmit mode.

While the IPR requires a nominal input voltage of 24 VDC, it will operate with input voltages from 21 VDC to 28 VDC. A power failure sensing circuit board in the IPR activates when the input voltage drops below 21 VDC. When the power failure board is activated, NiCd batteries on the board provide power to the RAM memory boards, but remove power from all other boards in the IPR. Fully charged NiCd batteries will maintain the contents of the RAM memory for at least 10 hours. The power failure circuit board will remain activated until the input voltage rises above 22 VDC. The power failure board and NiCd batteries can be seen in Figure 8.

The user should exercise caution when using an external battery supply. Many batteries that are rated at 24 volts may store an initial charge of more than 28 volts. Input voltages in excess of the specified 28 volts may cause permanent damage to the DC/DC converters in the IPR.

The voltages and currents listed below are average values measured at the IPR power connectors, not at the output of the AC/DC converter. With the power cable provided with the IPR, as much as a volt may be dropped in the cable. For this reason the AC/DC converter output is typically adjusted to approximately 25 VDC. Due to the variability in the hybrid radio components, the power consumption of the IPR may vary as much as 10% between radios.

The IPR uses four DC/DC converters and a 24 VDC series-pass limiting regulator. When the input voltage is greater than, or equal to, 24.2 VDC, the limiting regulator outputs 24.0 VDC. When the input voltage is less than 24.2, the limiter simply outputs the input minus .2 VDC. The limiting regulator and two of the converters are mounted on the front door of the radio unit (Figure 7). The remaining two converters are mounted on the back door of the digital unit (Figure 8). The radio unit converter "A" outputs voltages of +15, +5, and -15

VDC, while the converter "B" outputs -5 VDC. The digital converter "C" outputs +5 volts, while converter "D" outputs +12 and -12 volts.

The following table provides the current requirements for the IPR radio unit at various duty cycles and input voltages. Also provided are the current requirements of the digital section. As mentioned earlier, voltages less than 24 VDC are not regulated through the series pass limiting regulator. The RF transmit power amplifier requires a nominal 24 VDC supply. Since this regulator output drives the power amplifier, any voltage less than 24 VDC results in reduced output power from the power amplifier. This explains the lower current values for the 21 VDC inputs in the following table.

CURRENT (AMPS) PER INPUT VOLTAGE AND DUTY CYCLE

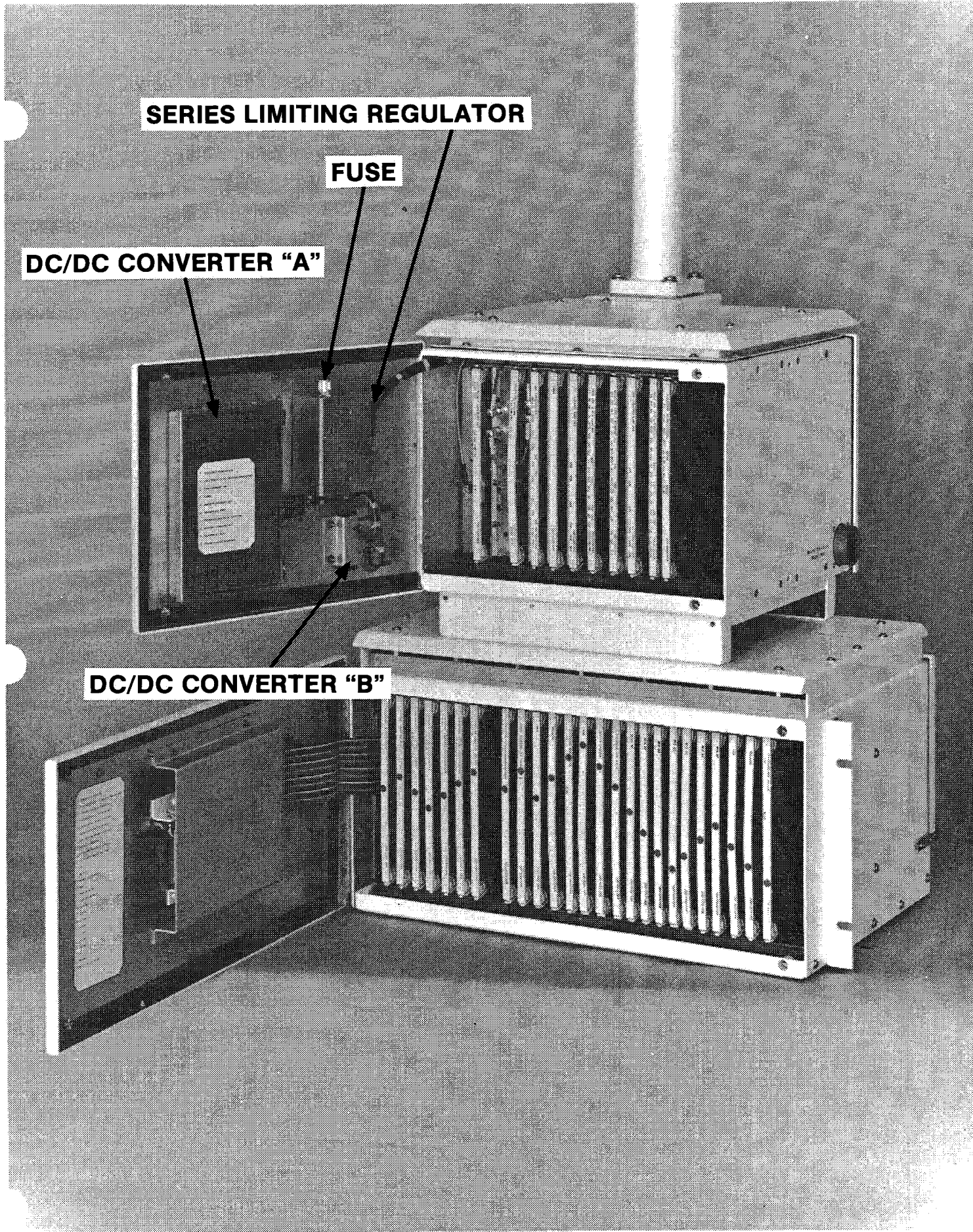
UNIT	DUTY CYCLE	21 VDC	24 VDC	28 VDC
Radio	100%	2.6	3.0	2.8
Radio	50%	1.9	2.0	2.0
Radio	20%	1.6	1.4	1.2
Digital	N/A	3.3	2.9	2.6

*2.140 WATTS*

### 2.3 Fuses

The IPR radio unit has a 5.0 amp fuse that is found inside the back door as shown in Figure 9. The radio unit also has a 2.0 amp fuse in the 24 VDC regulator shown in Figure 7. The IPR digital unit has a 5.0 amp fuse that is accessible from the back of the digital unit as shown in Figure 10.

The two radio fuses are subminiature normal-blow (type GMW), while the digital fuse is a fast-blow cartridge.



**SERIES LIMITING REGULATOR**

**FUUSE**

**DC/DC CONVERTER "A"**

**DC/DC CONVERTER "B"**

FIGURE 7  
FRONT OF THE IPR WITH DOORS OPEN

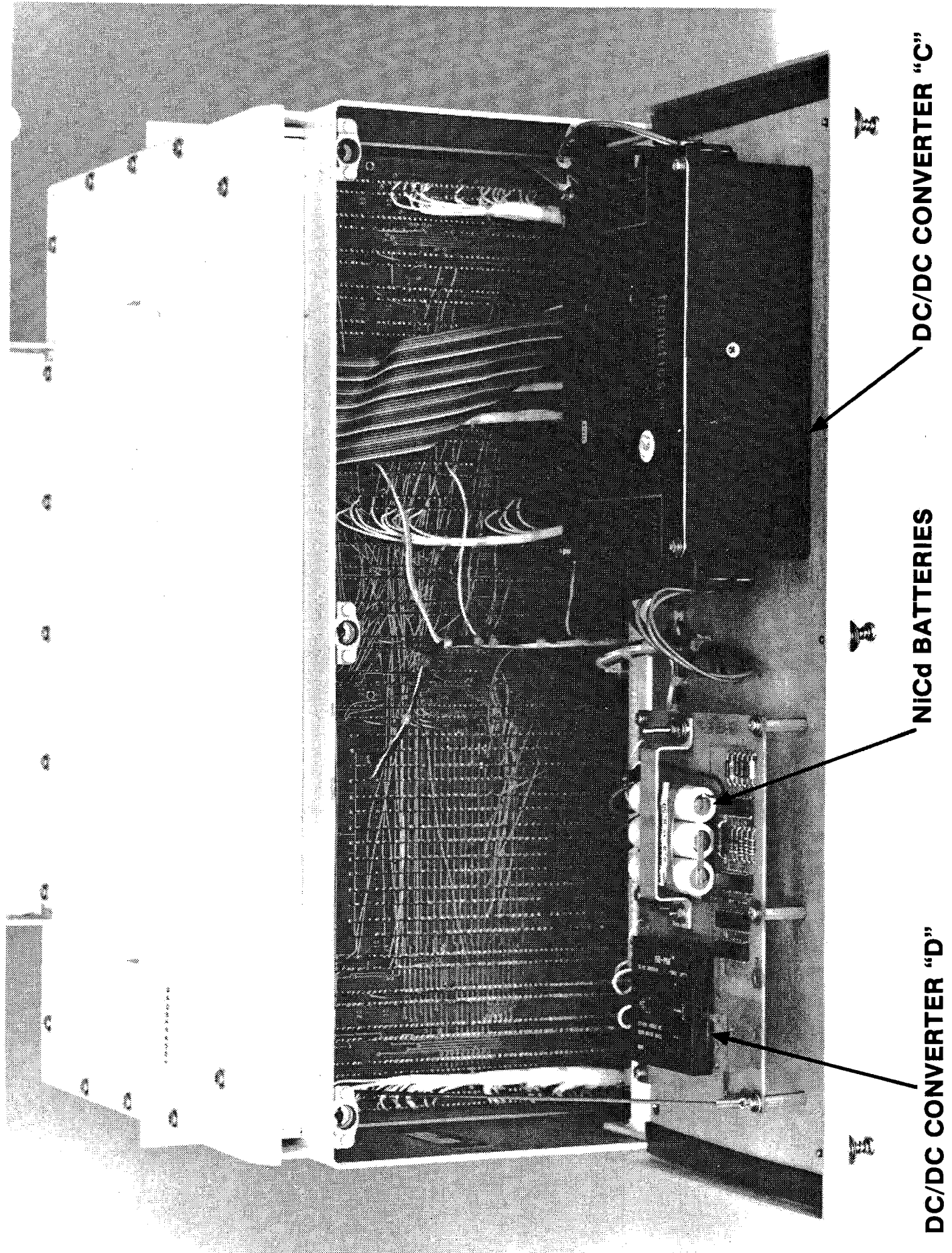


FIGURE 8  
BACK OF THE IPR DIGITAL SECTION WITH DOORS OPEN  
- 15 -

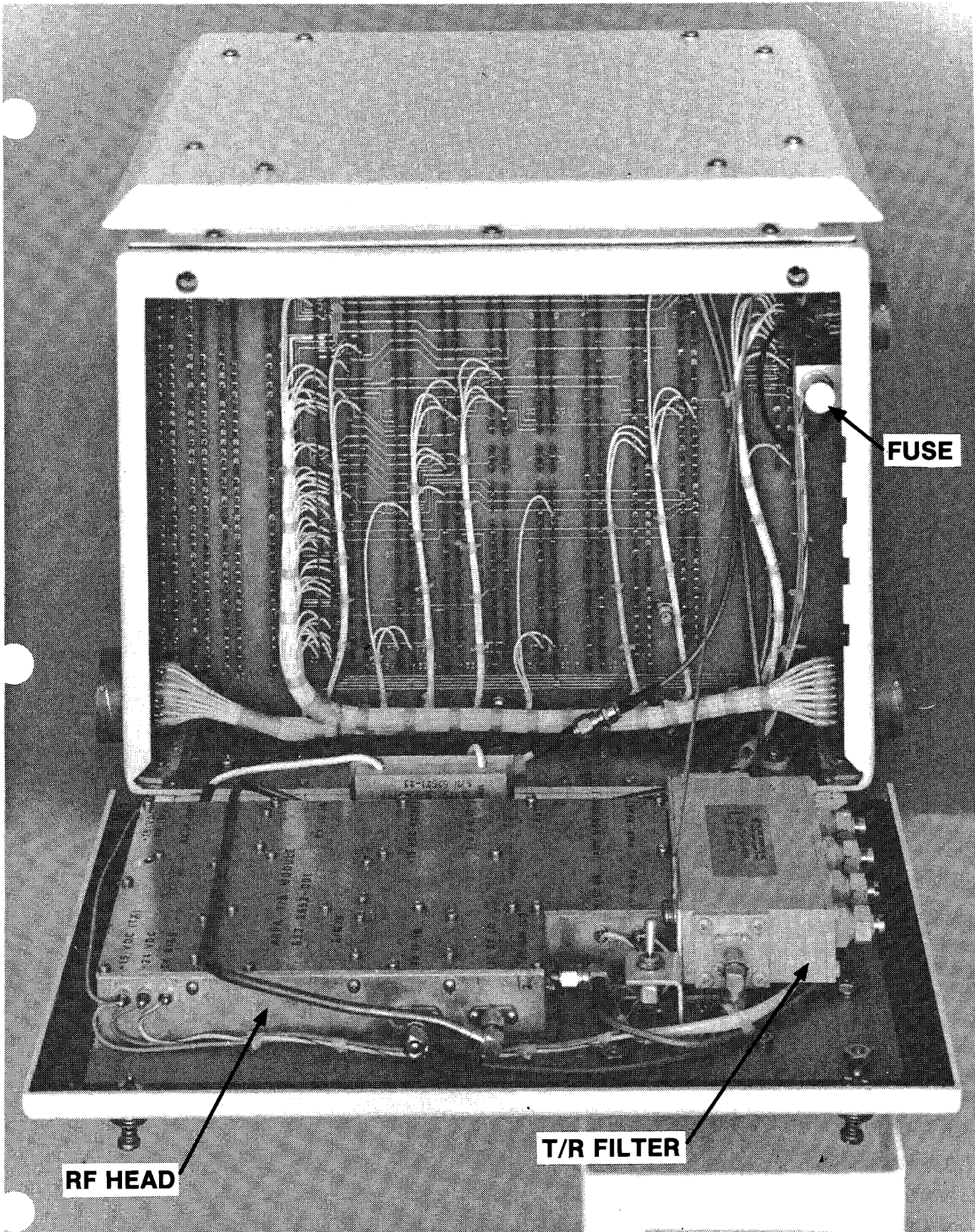


FIGURE 9  
BACK OF THE IPR RADIO UNIT WITH THE DOOR OPEN

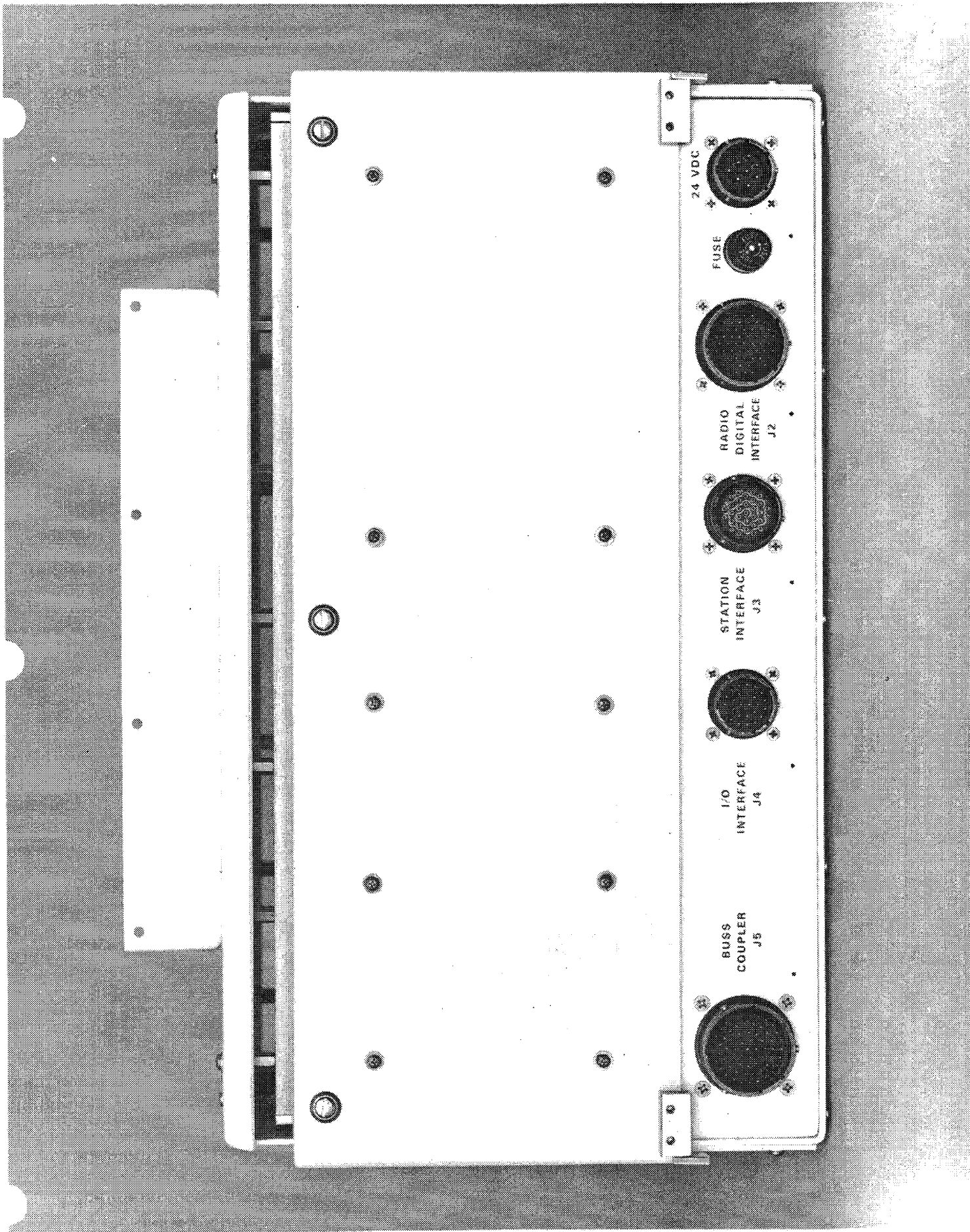


FIGURE 10  
BACK OF IPR DIGITAL UNIT WITH THE DOOR CLOSED

## 2.4 Cables

The Improved Packet Radio is supplied with the following four cables:

- (1) Power input
- (2) Radio/digital interface
- (3) RS-232 interface (I/O)
- (4) 1822 interface (station)

The connectors on all the cables are of the "quick disconnect" type. To attach the cable, twist the connector to find the alignment key, push the connector in and turn it clockwise to the locking position.

Because the IPR can be separated into two units, each unit must have a power input cable. The IPR is supplied with a 25 foot power cable. One end of the cable has a connector to plug into the AC/DC converter. The other end splits in two with connectors to plug into both the radio and digital units. The power cable consists of just two wires, i.e., a black wire for ground and a red wire for +24 VDC. The power cable plugs into the side of the radio unit, as shown in Figure 11, and into the back of the digital unit, as shown in Figure 10.

Each IPR is supplied with a 25 foot console I/O cable. The console I/O cable connects to the back of the digital unit (see Figure 10) and is terminated by a standard RS-232 connector. The cable will also support current loop devices. Section 4.2 defines the pins used in the cable.

The radio/digital interface cable is used to connect the radio and digital units. This cable runs from the side of the radio unit (see Figure 11) to the back of the digital unit (see Figure 10). The IPR is supplied with a short cable that is just long enough to connect the units when they are attached together. If the user wishes to separate the units, a longer cable must be made according to the pin specification in Section 4.5. For extremely long cable lengths (up to a maximum length of 1000 feet), the user should contact Collins



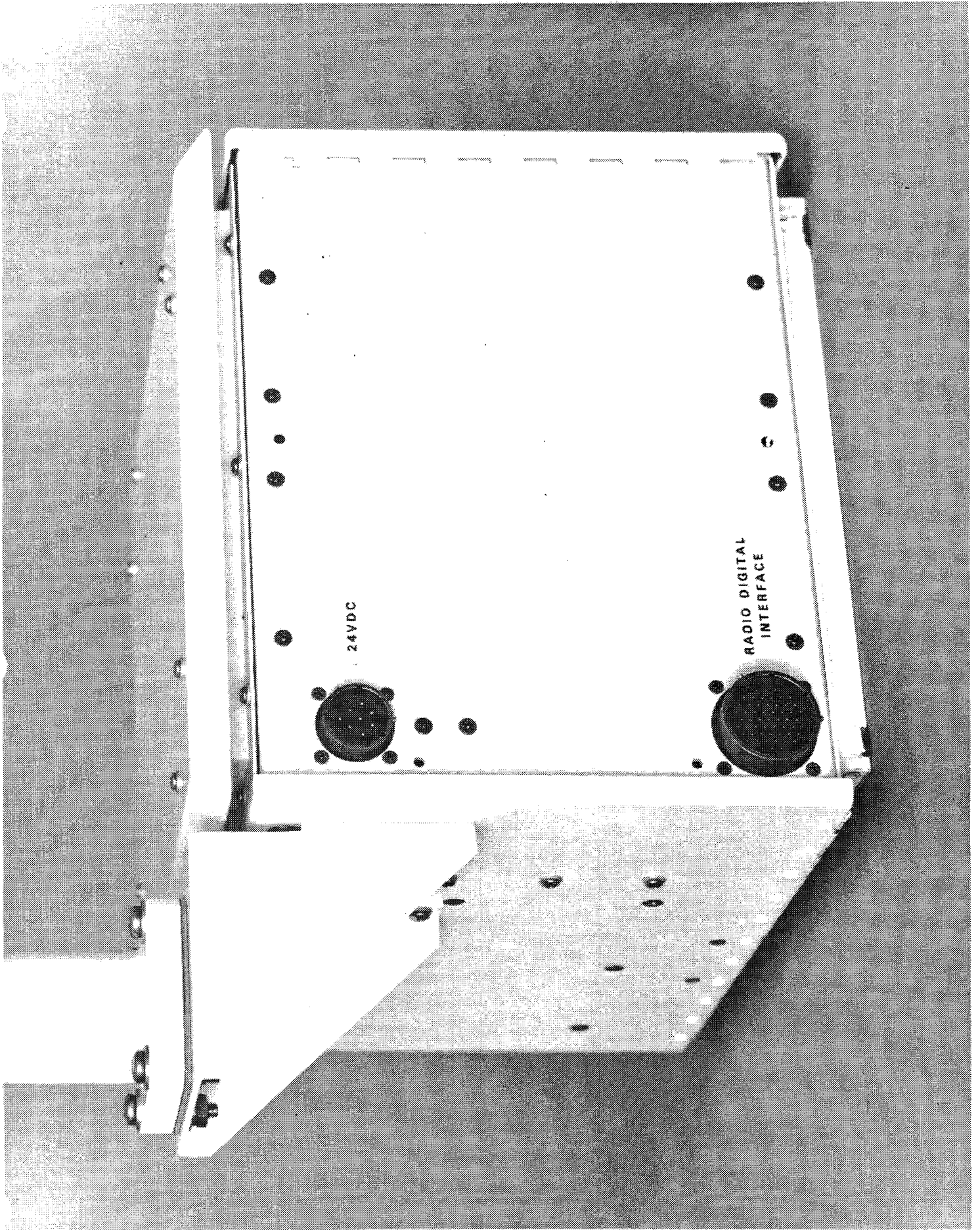


FIGURE 11  
SIDE VIEW OF THE IPR RADIO SECTION  
- 19 -

for a specification for the cable. The radio/digital cable is symmetrically defined and either end of the cable may be connected to either unit.

The 1822 interface cable allows the IPR to be connected to the user's host computer. The 1822 cable connects to the back of the digital unit as shown in Figure 10. The cable supplied with the IPR is 25 feet long and has two male connectors. Section 4.1 defines the pins in this cable. The 1822 cable is symmetrically defined and either end of the cable may be connected to the IPR.

### 3 DESCRIPTION OF MODULES

The Improved Packet Radio is organized and constructed as a set of functional modules to facilitate module interchangeability and future upgraded modules to be retrofitted into existing packet radio card cages.

Modularity in the IPR is illustrated in Figure 12 and Figure 13. As can be seen, many of the radio modules have RF shielding in the form of a metal "can" built over the circuit board. Each of the modules plug into a common backplane having the appropriate edge-on and coax connectors, as shown in Figure 9. Figure 13 shows the digital unit modules plugging in from the front to a common PC wire-wrap type backplane in the back (Figure 8).

#### 3.1 Functional Description of the Radio Unit

A functional block diagram of the IPR radio unit is shown in Figure 14. When in the transmit mode, packets in serial digital form flow from the transmit DMA to the encoder/modulator. The encoder chip encodes each data bit by expanding each bit into a number of "chips" and presents the chips to the Minimum Shift Keying (MSK) modulator. The MSK modulator output is up-converted to RF, where it is amplified to a minimum of 8 watts. The transmitter output is coupled to the antenna through the Transmit/Receive (T/R) switch. The T/R switch also isolates the transmitter from the receiver.

In the receive mode, the T/R switch directs the RF signals from the antenna to the down-converter section. The down-converter output is processed and demodulated for serial transmission to the receive DMA.

The system allows operation at data rates of 100 KBPS and 400 KBPS. The RF and IF portions of the receiver are common for the two data rates

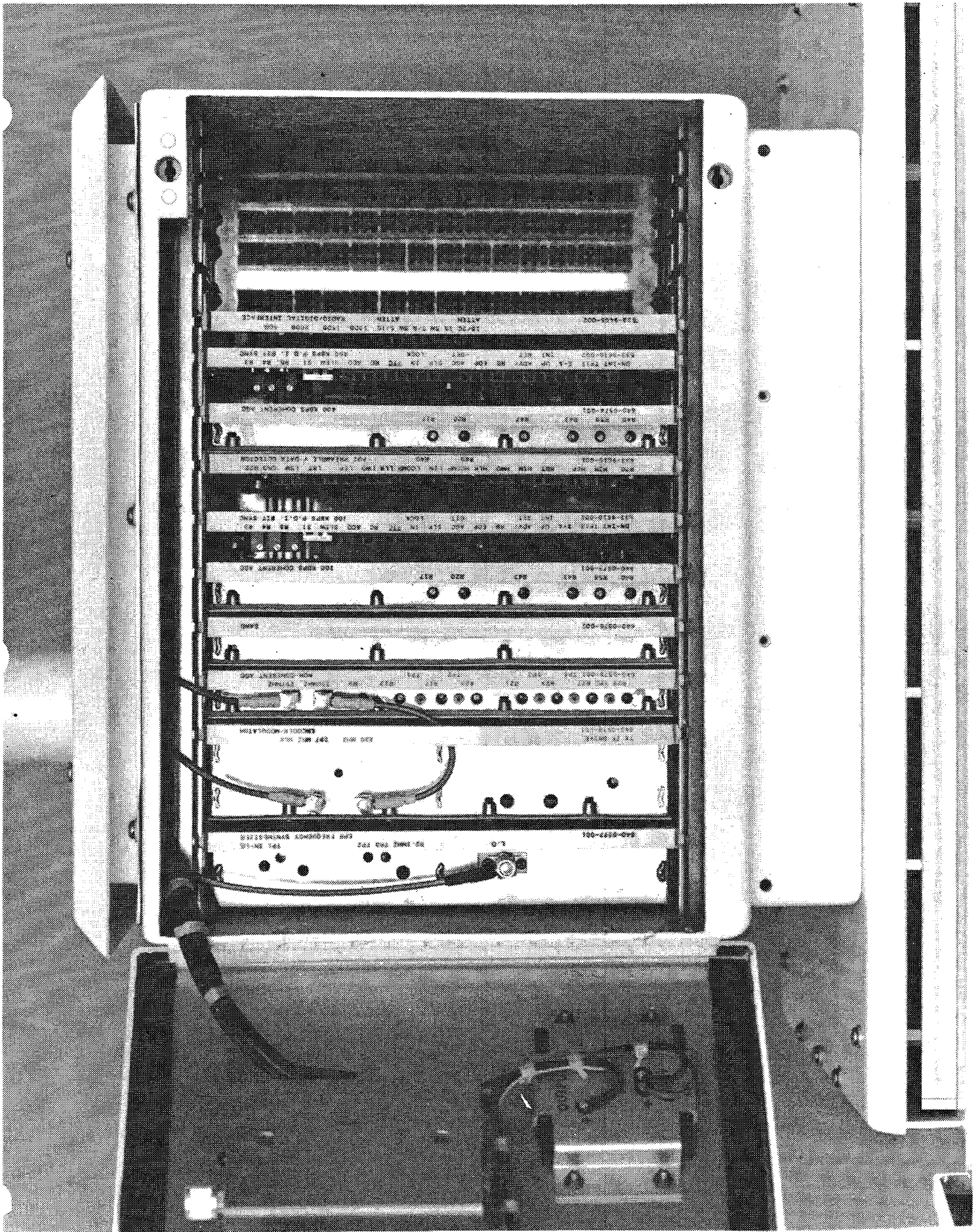


FIGURE 12  
IPR RADIO UNIT CIRCUIT BOARDS  
- 22 -

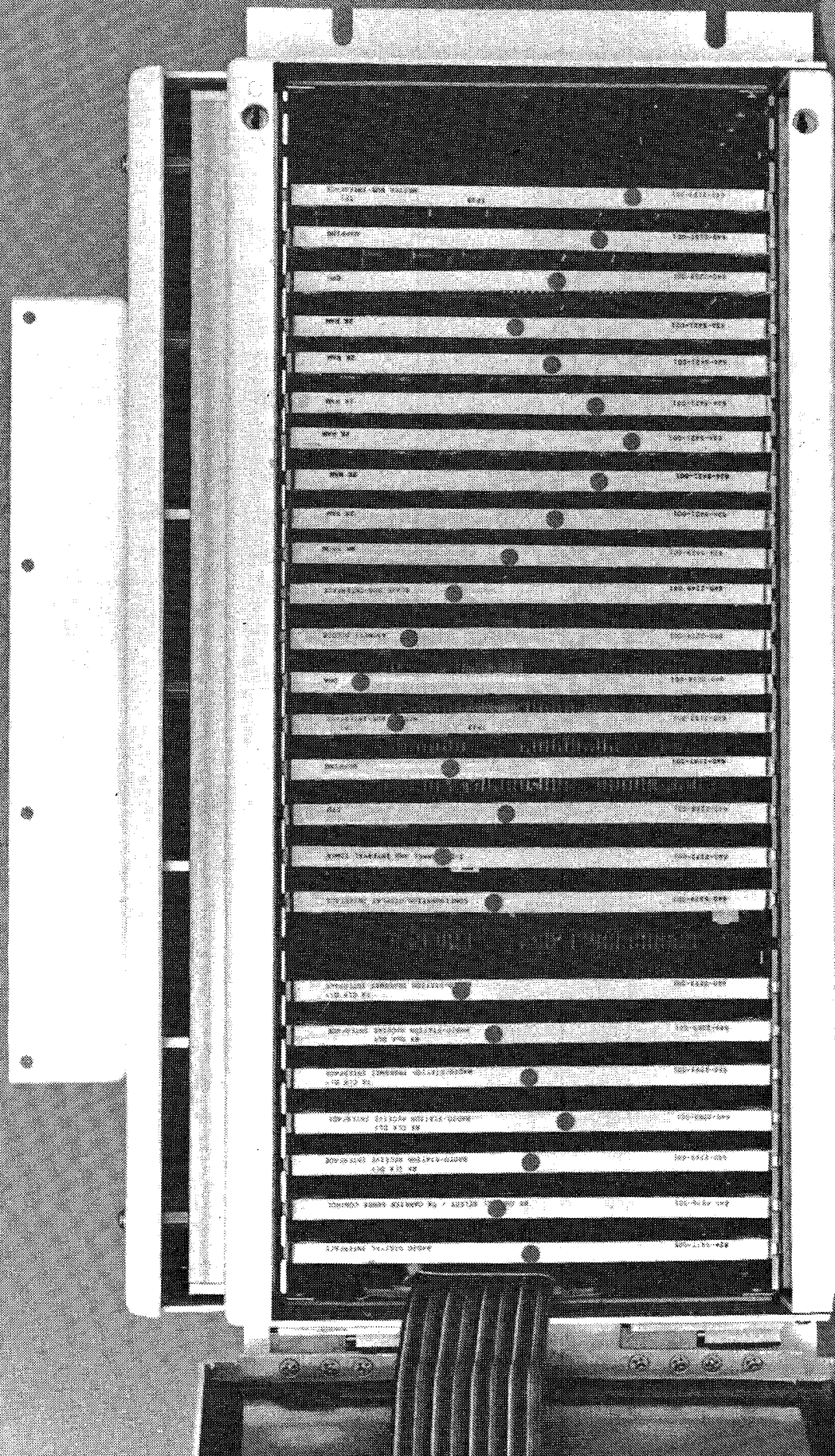


FIGURE 13  
IPR DIGITAL UNIT CIRCUIT BOARDS

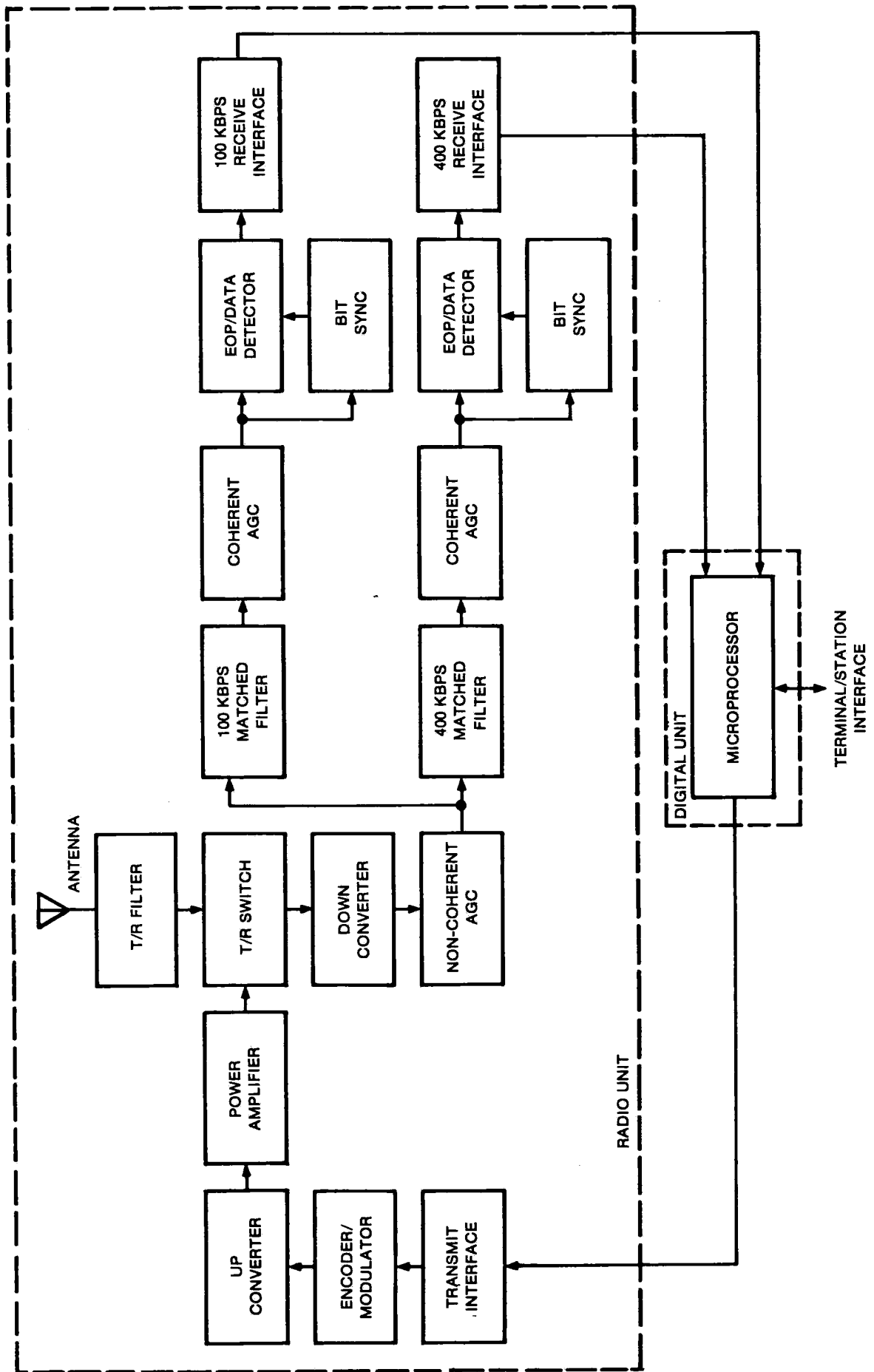


FIGURE 14  
FUNCTIONAL DIAGRAM OF THE IPR RADIO UNIT

up to the non-coherent AGC output. The AGC signal is split and serves as the input to two independent circuits, one per data rate.

### 3.2 Radio Module Functions

#### 3.2.1 Frequency Synthesizer

The frequency synthesizer provides 20 frequencies in 6.400000 MHz steps from 1420.800000 to 1542.400000 MHz. With an IF frequency of 297.915456 MHz, this produces an RF center frequency range of 1718.715456 to 1840.315456 MHz in 6.400000 MHz steps. The local oscillator (L.O.) frequency is software controlled by six control lines from the radio transmit DMA interface.

#### 3.2.2 Encoder/Modulator

The encoder accepts a digital packet of information from the radio transmit DMA interface, and "chip encodes" the packet for spread spectrum transmission. The spread factors are 128 chips/bit at 100.106 KBPS and 32 chips/bit at 400.424 KBPS. MSK modulation is achieved by impulsing a transmit SAWD matched filter with the code. This SAWD output (67.271232 MHz MSK) is then up-converted with 230.644224 MHz to give the radio IF of 297.915456 MHz MSK.

#### 3.2.3 Noncoherent AGC

The noncoherent AGC amplifier is located before a SAWD matched filter and provides the SAWD with a constant level input signal. This constant level signal is the result of down converting the received 297.915456 MHz MSK signal with the 230.644224 MHz L.O. giving 67.271232 MHz MSK to the SAWDS.

#### 3.2.4 SAWD

There are two receive SAWD filters matched to the encoder/modulator's transmit SAWD. One is for a 100.106 KBPS data rate and the other is for a 400.424 KBPS data rate. The receive SAWD input is a wideband spread spectrum IF signal (67.271232 MHz) normalized to a

constant level by the noncoherent AGC circuits. The output of the SAWD is the autocorrelation of the input code spread signal with the tap coded SAWDS. The output autocorrelation pulses are compared to the correlation pulse from the previous bit and coherently combined in a hybrid.

### 3.2.5 Bit Syncs - 100 Kbps and 400 Kbps

The purpose of the bit sync is to align the data sampling pulses with the received bits. The bit sync is required continuously throughout the detection of an incoming packet.

The incoming data pulses go through an advance/retard circuit which centers the data pulses in a sample window within a specified time. When this occurs, bit sync in-lock is acquired.

To enhance mobile operation, the bit sync integrates the incoming data pulses plus multipath over a given period of time. This reduces the overall effects of multipath fading.

### 3.2.6 Preamble and Data Detector

Post detection integration of DPSK demodulation is implemented to enhance performance in a mobile, highly urban environment. Data detection occurs after the end of preamble (EOP) at either of the two data rates (100 KBPS or 400 KBPS).

The preamble and data detector functions to determine the occurrence and timing of the end of the preamble of a received packet. This alerts the processor to the start of data.

### 3.2.7 Radio/Digital Interface

The radio/digital interface card contains the appropriate line drivers and receivers to allow remote location of the PR radio unit. All signals to and from the digital unit pass through this card. Separation of the radio unit from the digital unit can be up to 1000 ft.



### 3.2.8 Transceiver

The RF head (transceiver) is mounted on the back door of the radio unit. The T/R filter can be seen in Figure 9 mounted to the right of the RF head when looking from the rear of the radio. The RF head is a hybridized unit, performing the RF up-conversion and power amplification in the transmit mode, and the IF down-conversion and amplification in the receive mode. The minimum output power is 8 watts in the 1710 to 1850 MHz (L-band) frequency range. The output power can be controlled from full power to -20 dB range in 5 dB steps. The T/R filter has a frequency passband of 50 MHz, mechanically tunable to any center frequency in the 1710 to 1850 MHz band. The antenna is a 9 dBi gain omnidirectional antenna (in the azimuth plane) consisting of sleeved dipoles stacked colinearly for maximum bandwidth.

### 3.3 Functional Description of the Digital Unit

A functional block diagram of the IPR is illustrated in Figure 15. It consists of two microprocessors, memory (both PROM and RAM), DMA I/O interfaces to the radio and 1822 interfaces, a hexadecimal display and an RS-232 interface to a console. All devices are connected to a common bus consisting of 20 address lines, 16 data lines, and appropriate control signals.

The digital section of the IPR controls the transmission and reception of packets, and buffers and processes the packets according to the channel access protocol program.

A bus coupler may be implemented to expand the system to a dual bus structure. The device connected to the bus coupler may contain additional CPUs, memory, and peripheral devices.

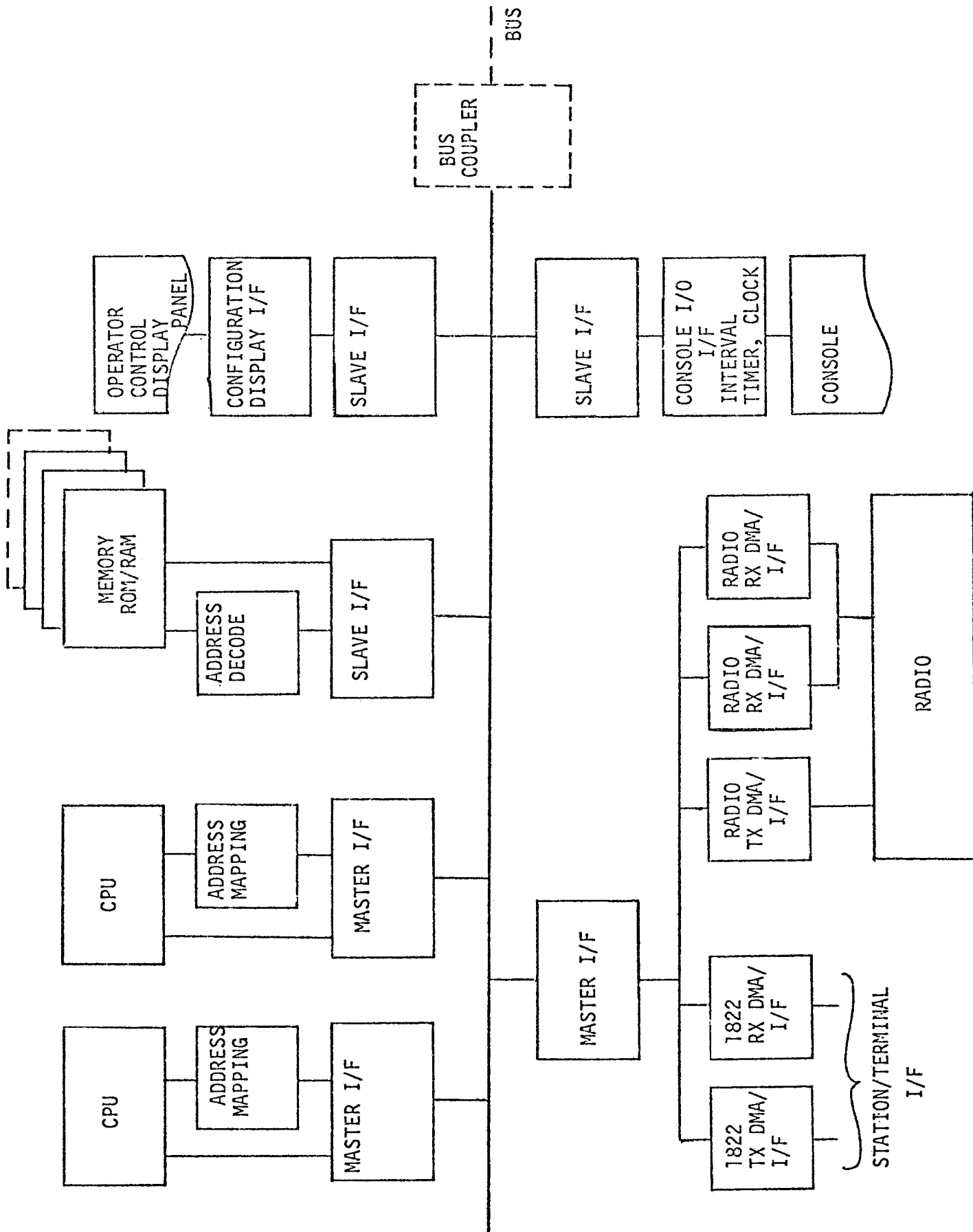


FIGURE 15  
 FUNCTIONAL DIAGRAM OF THE IPR DIGITAL UNIT

### 3.4 Digital Module Functions

#### 3.4.1 Memory

The IPR contains both RAM and PROM memory. Every 16-bit word of memory has associated with it a single odd parity bit for error detection. The IPR contains six RAM boards, where each board holds 2K words plus the associated parity bits. The IPR also contains a single PROM board holding 4K words plus parity.

#### 3.4.2 Address Decode

All of the zone 3 and 4 memory decode (chip enable) signals and the I/O address tags are decoded on this board. Zones 1 and 2 are decoded on the Slave board. The 20-bit address bus is not exhaustively decoded, but sufficient decoding is provided for 23K words of RAM, 4K words of PROM, and 144 address tags for I/O devices.

#### 3.4.3 Central Processing Unit (CPU)

Each of the CPUs in the IPR is a Texas Instruments SBP 9900 microprocessor using  $I^2L$  technology. The 9900 is a 16-bit CPU that implements 69 different instructions (including fixed point multiply and divide) using seven addressing modes. When the 9900 is operated with a 3 MHz clock, instruction execution times (excluding multiply and divide) vary from 2.7 us to 20.0 us with an average of about 7 us. Instructions are one, two, or three 16 bit words in length.

The 9900 provides 16 vectored prioritized hardware interrupts. Instead of a stack architecture, the CPU performs "context switching" of the processor work space, program counter, and status registers. A "work space" is the CPU's 16 general purpose registers which are resident in the system's main memory (rather than on the CPU chip itself). When a system call, subroutine call, or interrupt occurs, a context switch is executed by saving a pointer to the old work space, program counter, and status in a new work space used by the called process.

The 9900 contains a special serial I/O interface called the CRU (Communications Register Unit) that is utilized in the IPR to interface with the limit and bias registers. More details about the CPU may be obtained from the TMS 9900 Microprocessor Data Manual.

In addition to the CPU chip, the following major functions are included on this board: 16-level interrupt priority encoder, external hardware decode of the ABS instruction (for contention resolution in a multi-CPU environment), watchdog timer (to detect infinite program loops), and hardware decode of illegal op-codes.

#### 3.4.4 Master Bus Interface

This board resolves bus contention between the different bus masters, i.e., CPUs and DMAs, and provides bus access logic. The DMA master has priority over either of the CPUs, and CPU1 has priority over CPU2. The DMA is only allowed to hold the bus for a single cycle, but a CPU can hold the bus for two cycles while doing an ABS instruction. This board also contains a system clock for its corresponding master. Each Master board contains a DMA master and a CPU master. By including two Master boards in the IPR, two CPUs and a DMA may exist on a single bus (with one DMA master going unused).

#### 3.4.5 Slave Bus Interface

In order to accommodate different speed peripherals, the IPR is asynchronous in nature. That is, after a bus master gains access to the system bus, the master presents an address on the bus and asserts the ABGO (Asynchronous Bus GO) signal. After the ABGO signal is asserted, address decoding circuits on the slave board determine whether the address corresponds to RAM memory, PROM memory, or an I/O device. Once the address has been decoded to one of these three types, the slave board delays a certain amount of time before asserting the ABTM (Asynchronous Bus Terminate) signal indicating the bus transfer has been completed. Because the PROM memory is the fastest peripheral, the slave board inserts the smallest delay when PROM is referenced. The RAM

memory has an intermediate speed, and the I/O devices are slowest and require the largest delay.

The slave board also contains the circuitry to generate, and check, the one parity bit associated with each word of memory. In addition, the slave board provides address decoding for zones 1 and 2.

#### 3.4.6 DMA Channel

The DMA channel board provides the circuits for transferring data to and from memory without CPU intervention. A single DMA board is capable of handling sixteen different DMA channels, but only five channels are necessary for operation of the IPR, i.e., radio transmit, two radio receive, 1822 transmit, and 1822 receive. For each channel, the board contains an address register, word counter, status/control register, and sufficient logic to handle the bus request/grant protocol. If two or more channels simultaneously request a bus access, the DMA board implements a priority scheme to order the bus grants. The radio receive channel #1 has the highest priority, followed by the second radio receive channel, the radio transmitter, the 1822 receiver, and the 1822 transmitter (in that order).

#### 3.4.7 Radio/Station Transmit Interface

The IPR contains two transmit interfaces. One interface passes data to the radio section for RF transmission, while the other interface implements the 1822 protocol to pass data to an attached host computer. Each interface is implemented on a separate board, but the two boards are identical except for the backplane slot. The transmit interface board contains a parallel-to-serial converter, a cyclic redundancy checksum generator, status and command registers, and assorted logic to perform the 1822 protocol. The interface board also contains sufficient circuitry to perform loop-back tests without a radio or 1822 host.

### 3.4.8 Radio/Station Receive Interface

The IPR contains three receive interfaces. Two interfaces are devoted to receiving data from the radio section, while the third interface implements the 1822 protocol to receive data from an attached host computer. Each interface is implemented on a separate board, but the three boards are identical except for the backplane slot. The receive interface board contains a serial-to-parallel converter, a cyclic redundancy checksum checker, a status and command register, and assorted logic to perform the 1822 protocol. The interface board also contains sufficient circuitry to perform loop-back tests without a radio or 1822 host.

### 3.4.9 Console I/O Channel

The console I/O channel provides the circuits to allow connection of a terminal console device to the IPR. It is used for program loading, memory alteration and inspection, definition of operating parameters in diagnostic programs and other maintenance functions. Both RS-232 and current loop (20 ma) options are provided on this board. The console I/O board contains a 10 position rotary switch for defining the baud rate. The baud rates available are listed in Section 4.2.

The console I/O board contains an interval timer and an elapsed timer. These timers are described in more detail in Section 4.3.

### 3.4.10 Configuration/Display Interface

The configuration board contains 32 DIP switches that are read by the Operating System firmware. The purpose of those switches is described in Section 4.10. The board also contains latches and circuitry to display data on the front door display board.

### 3.4.11 Radio/Digital Interface

The radio/digital interface card contains the appropriate line drivers and receivers for separation of the radio and digital units. All signals to and from the radio unit pass through this card. The radio and digital units may be separated by as much as 1000 feet.

### 3.4.12 RX Channel Select/TX Carrier Sense Control

This board has two distinct functions. This first function is channel selection on a packet reception. The IPR has two DMA channels allocated for radio reception and a received packet of either data rate may be transferred through either DMA channel. When a packet reception begins, the channel select logic chooses an available channel and routes the data accordingly.

The second function of this board is to perform transmit randomization while sensing the radio carrier. This circuitry delays a random amount of time before checking the carrier sense signal from the radio. If carrier is sensed, another random delay is performed. If the carrier is not sensed at the end of the delay, the packet transmission is allowed to begin. The number of delay increments, as well as the length of the increments, is under software control.

### 3.4.13 Address Mapping

The IPR digital unit contains two mapping boards (one per CPU) to convert, or "map", the 15-bit CPU address into a 20-bit address on the system bus. The TI9900 CPU is able to address  $2^{16}$  unique bytes of memory or peripherals. However, the CPU only outputs a 15 bit address bus and all memory/peripheral operations are performed on words. (The least significant address bit is used internally by the CPU for byte addressing.) All 15-bit addresses output by the CPU are modified by the IPR mapping hardware to provide a 20-bit bus address. This is accomplished by summing the CPU address with one of several bias registers as shown in Figure 16. The particular bias register used in the summing process is determined by the contents of the limit

registers. Figure 17 shows how the CPU address is mapped into the bus address space after initialization has completed loading of the limit and bias registers.

Associated with each CPU in the IPR are three software variable bias registers, one fixed bias (hardware strapped) register and three software variable limit registers. These registers are set and read under software control via the CPU's CRU interface. The three limit registers, each 7 bits in length, may be used to partition the 32K address space of the CPU into four zones. The 7-bit limit registers are compared with the most significant 7 bits of address output by the CPU. If the CPU address is equal to, or greater than, limit register 3, then zone 4 is defined and the CPU address is summed with fixed bias 4. If the CPU address is not in zone 4 and is equal to, or greater than, limit register 2, then zone 3 is defined and the CPU address is summed with variable bias 3. If the CPU address is not in zone 4 or zone 3 and is equal to, or greater than, limit register 1, then zone 2 is defined and the CPU address is summed with variable bias 2. If the CPU address is not in zones 2, 3, or 4, then zone 1 is defined and the CPU address is summed with variable bias 1. The length of each zone is determined by the content of the limit registers.

When power is first applied to the CPU, and before the CPU has had time to define the limit and bias registers, a special mechanism must be employed to enable a default form of mapping to occur. In the normal mapping mode, the CPU address is simultaneously compared to all three limit registers and the zone decision (based upon the rules stated above) is presented to the bias registers in the form of two signal lines. The four possible states of these two lines determine which of the four bias registers will be added to the CPU address. However, when power is first applied to the system, a flip-flop is set on the mapping board which bypasses the limit registers and forces the default mapping to occur. When the flip-flop is set, the two signal lines to the bias registers are set high forcing the zone 4 bias register to be used for all CPU addresses. While the bias registers for zones 1, 2, and 3 are



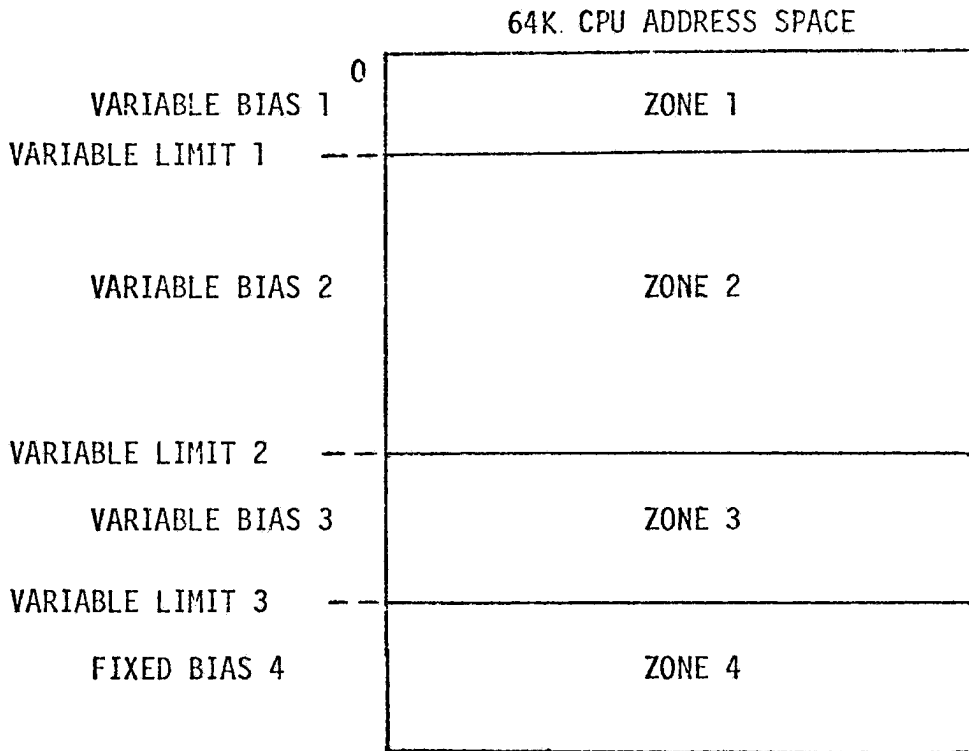
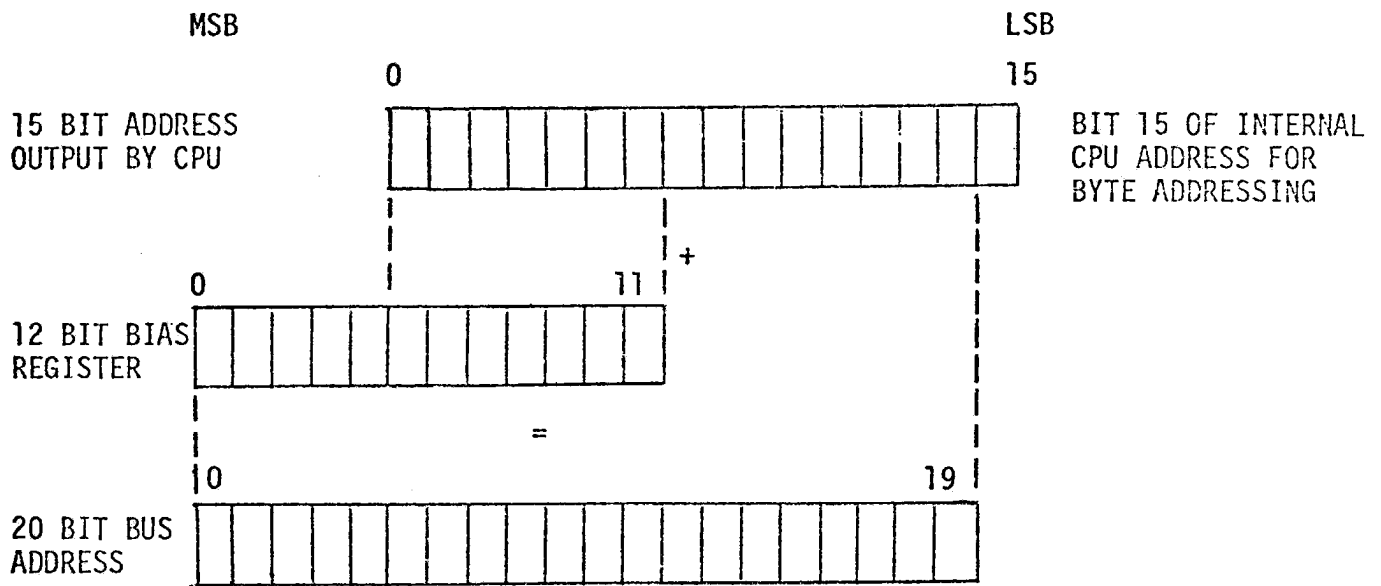


FIGURE 16  
ADDRESS MAPPING WITH CPU BIAS AND LIMIT REGISTERS

CPU ADDRESS SPACE

BUS ADDRESS SPACE

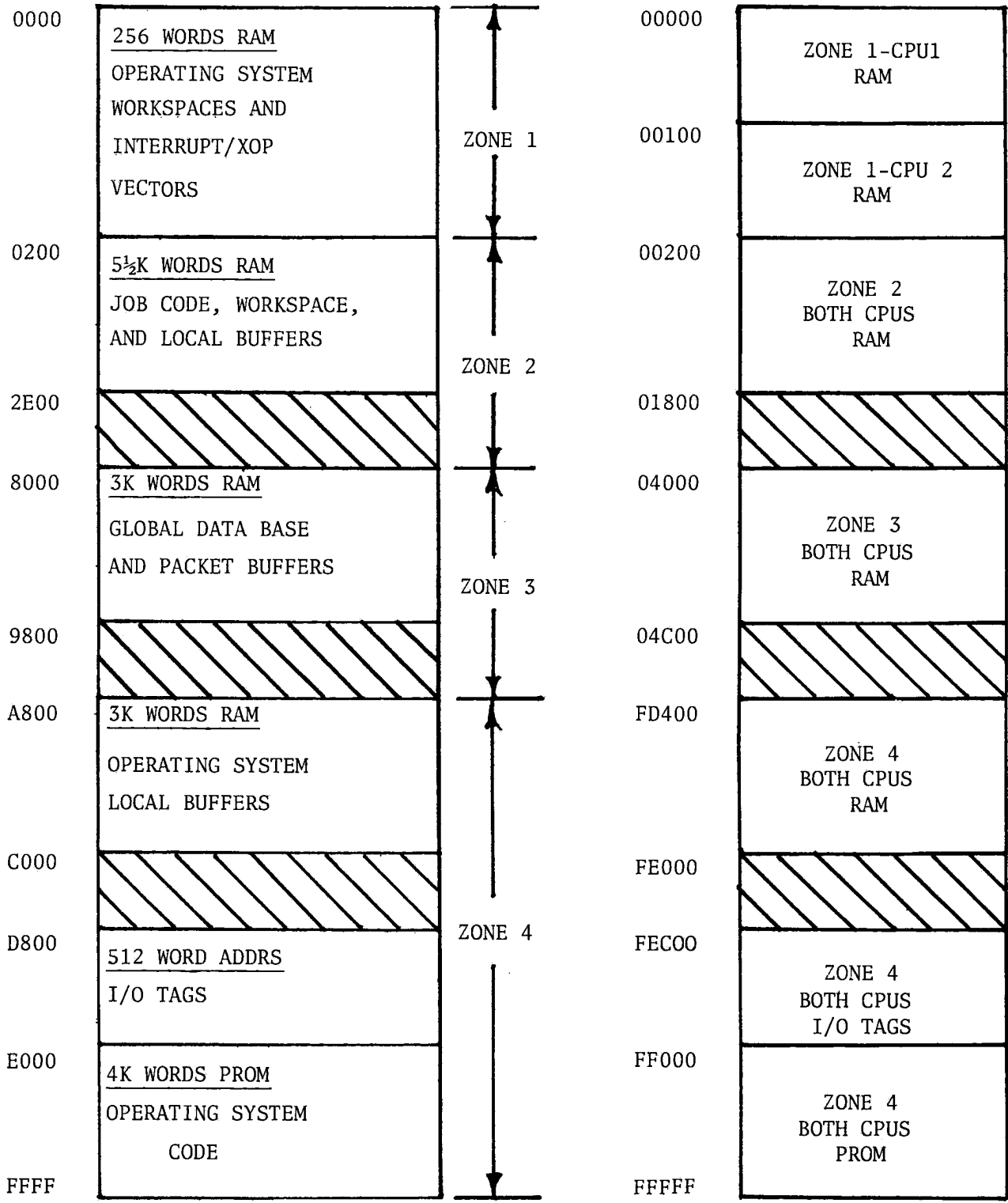


FIGURE 17  
CPU ADDRESS MAPPING INTO BUS ADDRESS SPACE

software controllable, the zone 4 bias register is strapped in hardware to be  $111110000000_2$ . In this way the default flip-flop and hardware strapped bias 4 allows the system to begin executing instructions at a known location in the 1024K system address space. The default flip-flop, and thus the default mapping, stays set until the CPU writes to limit register 3.

Addresses generated by the DMA interface do not pass through the mapping board. Rather, the DMA addresses are always mapped by a hardware strapped bias value. Because the DMA operations are always to the packet buffers in zone 3, the DMA's bias register is strapped to be the same value as the software settable bias register 3.

The comparison of a CPU address with a limit value is effectively done by subtracting the limit value from the address and testing for a borrow out of the most significant bit. Because the mapping board was designed to perform additions, rather than subtractions, the limit register must be loaded with the two's complement of the intended limit value. The comparison of the CPU address with the limit value is then performed by adding the CPU address to the limit register and testing for a carry out.

### 3.5 Antenna

The vertically polarized antenna supplied with each packet radio is a colinear sleeved dipole array providing a +9 dBi gain with omnidirectional coverage in the azimuthal plane. Vertical beam width is approximately 14 degrees centered at 0 degrees (horizon). The normal antenna mounting is on the antenna bracket located on the radio unit's back door.

Many installations, due to poor radio connectivity, require mounting the antenna on a mast or rooftop while the IPR itself is more conveniently located in a building or shelter. When such an installation is required, the antenna should be mounted with a low loss coaxial cable connecting the antenna to the antenna connector on the

*FIRST BUILD  
@ 12 30 83*

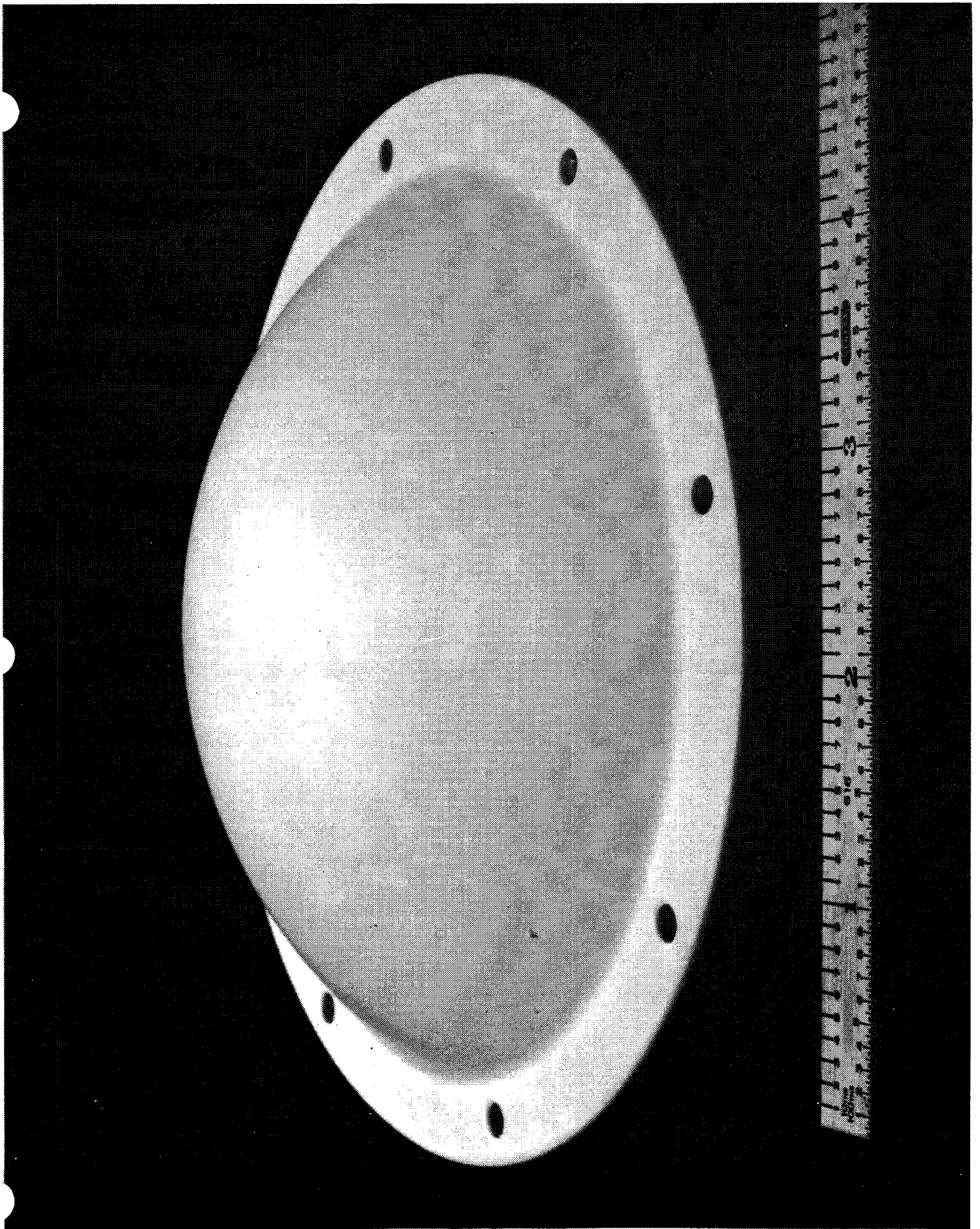


FIGURE 18  
IPR ANTENNA FOR MOUNTING ON A HELICOPTER

back door of the radio unit. If necessary, the antenna mounting bracket on the back door may be removed. All IPR radios and antennae are provided with type N connectors.

In general, coaxial cable lengths longer than 100 feet should be avoided, unless special ranging and sensitivity analysis is performed. The insertion loss of the cable versus cable length must be considered when remotely siting the antenna. Listed below are several suitable coaxial cable transmission lines and their insertion loss characteristics.

TRANSMISSION LINE	TYPE	INSERTION LOSS (1800 MHZ)
7/8" Air Dielectric	Heliac	2 dB per 100 feet
1/4" Semi-Rigid		9 dB per 100 feet
0.4" Coax	RG/U-214	14 dB per 100 feet
0.2" Coax	RG/U-58	28 dB per 100 feet

Selection of cable type consonant with expense and performance should be considered in conjunction with ranging and sensitivity analysis. A rule of thumb is that each 6 dB of excess coaxial cable insertion loss at either end of a radio link results in a 50% reduction of achievable link range.

For special airborne users, a low profile antenna providing hemispherical coverage is available from Rockwell/Collins. This antenna is shown in Figure 18.

### 3.6 Ranging Considerations

The range at which a particular IPR can communicate with another is a strong function of antenna heights, environment and siting. The Packet Radios are designed to be either fixed or mobile in all environments from flat rural links to highly urban links with associated man-made noise influences. A set of rough guidelines follow to aid in selecting IPR locations in a particular network.

The 100 KBPS performance is always 6 dB better than 400 KBPS. All performance parameters discussed herein are assumed to be 100 KBPS unless otherwise stated. Certain conditions may prevail, such as extreme multipath characteristics in urban environments, that preclude 400 KBPS operation. The protocol software dynamically selects the data rate for a given link on a packet by packet basis.

*MULTIPATH 7.25 MS*

If both antennae on a given link are within line-of-sight (LOS) of each other, the link can be several hundred miles long. With LOS conditions and normal antenna heights of 6 feet, IPRs can communicate to the radio horizon (32 miles).

For non-LOS conditions, antenna elevation strongly influences range. For one antenna at a height of 6 feet and the other antenna at a height of 150 feet, the average range over all possible environments is approximately 22 miles in a rural environment to 2 miles in a dense urban environment. Raising antenna height at either end of the link doubles the range for every doubling of antenna height. Also, increased attenuation such as transmission coaxial line loss, amplifier power control, path blockages, etc., shorten the urban range by half for every additional 9 dB of attenuation.

*10:1 Reduction IN URBAN ENVIRONMENT*

*why 9 dB?*

#### 4 PERIPHERALS AND INTERFACE DESCRIPTION

This section describes the hardware requirements for connection of the IPR to external devices, e.g., host computer, station/terminal, or local console, as well as the interconnection of the radio and digital sections of the PR. Cable connections and pin positions are defined for each PR interface connection.

##### 4.1 1822 Interface

The processor-processor interface used by the IPR is the same as that used on the ARPANET. A user wishing to connect a computer to the IPR would use this interface and must provide the host side of the interface hardware. The 1822 interface protocol is described in Bolt Beranek and Newman (BBN) Report No. 1822.

The data transfer rate over the 1822 interface is a function of the associated host CPU interface and delays in the IPR's handshaking. Under optimal conditions, the 1822 interface can transfer data at rates up to 400 kbit/sec. The data transfer is full duplex and asynchronous with a four-way handshake on each bit.

Differential line drivers and receivers are provided for twisted pair transmission lines. The line impedance is a nominal 120 ohms.

The following is a summary of the signals in the 1822 interface. The interface connector pin information is given in Figure 19. The 1822 interface cable was designed to be symmetrical. That is, either end of the cable may be attached to the IPR. The cable must have a Cannon connector #48-16R18-31P on either end. The panel mounted connector on the IPR is a Cannon connector #48-10R18-31S.

PR READY TEST

The test signal sent to the PR to interrogate its ready status through the PR's relay contacts. No more than 100 ma should flow in this wire and the PR MASTER READY wire.

<u>BACKPLANE</u>	<u>PR CONNECTOR</u>	<u>HOST CONNECTOR</u>	<u>DEFINITION</u>
6-67	11	13	HOST READY TEST
6-11	12	14	HOST MASTER READY
6-8	20	6	THERE'S YOUR HOST BIT -
6-10	19	5	THERE'S YOUR HOST BIT +
7-10	8	18	RDY FOR NEXT HOST BIT -
7-9	7	17	RDY FOR NEXT HOST BIT +
6-7	22	2	LAST HOST BIT -
6-6	21	1	LAST HOST BIT +
7-11	13	11	PR RDY TEST
7-14	14	12	PR MASTER RDY
6-14	24	4	HOST TO PR DATA -
6-12	23	3	HOST TO PR DATA +
7-7	2	22	LAST PR BIT -
7-8	1	21	LAST PR BIT +
7-16	18	8	RDY FOR NEXT PR BIT -
7-42	17	7	RDY FOR NEXT PR BIT +
7-15	6	20	THERE'S YOUR PR BIT -
7-12	5	19	THERE'S YOUR PR BIT +
7-27	4	24	PR TO HOST DATA -
7-31	3	23	PR TO HOST DATA +
7-23	31	31	GROUND

FIGURE 19 1822 INTERFACE CABLE SPECIFICATION



PR MASTER READY	The return for the PR READY TEST signal through the PR's relay contacts.
HOST READY TEST	The ground signal sent to the host computer to interrogate its ready status through the host CPU's relay contacts. No more than 100 ma should flow in this wire and the HOST MASTER READY wire.
HOST MASTER READY	The return for the HOST READY TEST signal through the host computer relay contact.
HOST-TO-PR DATA LINE	The data from the host computer should remain stable until after the PR READY FOR NEXT HOST BIT signal goes off indicating that the previous bit has been accepted.
THERE'S YOUR HOST BIT	This signal should be presented to the PR by the host computer as soon as the host computer has a bit available to transmit and the PR is indicating that it is ready for next host bit. When the READY FOR NEXT HOST BIT signal is removed, the THERE'S YOUR HOST BIT signal should be removed.
READY FOR NEXT HOST BIT	This signal will be presented to the host computer whenever the PR is waiting for a transmission from the host computer. Each time that the host CPU gives the PR a bit (via THERE'S YOUR HOST BIT), the READY FOR NEXT HOST BIT will go off after the bit has been taken in. It will go back on after THERE'S YOUR HOST BIT goes off.
LAST HOST BIT	When the host computer transmits the last bit of a message, the LAST HOST BIT signal should be sent to the PR in conjunction with the THERE'S YOUR HOST BIT. The LAST HOST BIT signal should remain on at least until READY FOR NEXT HOST BIT goes off.
PR-TO-HOST DATA LINE	The data for the host computer will remain stable until after the host's READY FOR NEXT PR BIT signal goes off, indicating that the previous bit has been accepted.
THERE'S YOUR PR BIT	This signal will be presented to the host by the PR as soon as the PR has a bit available to transmit and the host computer presents the READY FOR NEXT PR BIT signal. When the READY FOR NEXT PR BIT goes off, the THERE'S YOUR PR BIT signal will be removed. It will not be renewed until a new READY FOR NEXT PR BIT signal arrives. There will be a minimum of 500

nsec delay in THERE'S YOUR PR BIT going on following the PR TO HOST DATA LINE becoming true for deskewing purposes.

READY FOR NEXT PR BIT This signal should be presented to the PR whenever the host computer is ready to receive a new bit. Each time that the PR gives the host a bit (via the THERE'S YOUR PR BIT line), the READY FOR NEXT PR BIT signal should go off after the bit has been taken in. This notifies the PR that the bit has been taken and that a new bit can be placed on the PR TO HOST DATA LINE. READY FOR NEXT PR BIT should be off at least until THERE'S YOUR PR BIT goes off.

LAST PR BIT When the PR transmits the last bit of the second CRC checksum word, the LAST PR BIT signal will be sent to the host computer in conjunction with the THERE'S YOUR PR BIT signal. Specifically, the LAST PR BIT signal will come on no later than the THERE'S YOUR PR BIT signal, and will remain on until the host computer turns off READY FOR NEXT PR BIT.

#### 4.2 Console I/O Channel

The I/O channel provides a character (8-bit) serial interface to a standard terminal. Both RS-232 and current loop options are provided. The I/O channel is used for program loading and other operator functions. Figure 20 defines the wires in the I/O cable. The I/O cable has a standard RS-232 connector (DBM 255) on one end, while the other end of the cable has a Cannon connector #PT06ASR16-26S. The panel-mounted connector on the IPR is a Cannon connector #PT02A16-26P.

The console I/O channel operates on an interrupt basis. When data is received from the terminal device, an interrupt is generated to both CPUs to cause the channel to be serviced. Similarly, as data is being transmitted to the terminal, an interrupt is generated to inform the processor that another character can be transmitted.

Data moves to and from the processor via the data bus on an 8-bit character basis. Circuits are provided to enable and disable either TX or RX interrupts and to select binary or ASCII modes. The IPR transmits

<u>BACKPLANE</u>	<u>PR CONNECTOR</u>	<u>TERMINAL CONNECTOR</u>	<u>DEFINITION</u>
10-74	E	6	DATA SET READY
10-72	G	8	DATA CARRIER DETECT
10-77	D	5	CLEAR TO SEND
10-16	B	3	TX DATA
10-23	F	7	SIGNAL GROUND
10-79	C	4	REQUEST TO SEND
10-32	P	20	DATA TERM READY
10-28	A	2	RX DATA
10-42	K	14	TX CURRENT LOOP +
10-38	L	15	TX CURRENT LOOP -
10-14	M	16	RX CURRENT LOOP +
10-17	N	17	RX CURRENT LOOP -

FIGURE 20 I/O CABLE PIN DEFINITIONS

characters with even parity, but ignores parity on input. A ten position rotary switch on the I/O board selects any of the following baud rates:

switch	baud	switch	baud
0	110	5	1800
1	150	6	4800
2	300	7	9600
3	2400	8	2400
4	1200	9	600

While the IPR's UART is able to transmit and receive at 9600 baud, the CPU is not fast enough to handle a continuous stream of input characters above 4800 baud. That is, a user can communicate with the IPR at 9600 baud if the input is from a keyboard, but software can not be loaded at 9600 baud.

4800 baud  
max

In order to provide delay for the mechanical carriage return of the TI Silent 700 terminal, the software driver routines implement a 260-390 msec delay after transmission of any carriage return character. The TI terminal will transmit and receive characters at baud rates up to 1200, but mechanical reasons prevent the terminal from printing more than 30 characters per second. A switch on the edge of the console I/O board (down for TI) provides the additional delay needed. When the TI switch is down and the baud rate is over 300, a 25 msec delay is inserted between the UART's "TX ready" signal and the generation of an interrupt.

down  
TI

#### 4.3 Elapsed Time Clock and Interval Timer

The IPR implements a single 32 bit elapsed time clock. The least and most significant words of the clock may be read by IPR software processes for the determination of elapsed time. The least significant clock word has a tick rate of 6.51 usec, and the most significant clock word has a tick rate of 427 msec.

The IPR also implements a 16 bit interval timer. The timer may be loaded with any 16 bit binary count. The count is decremented at a rate of 1.667 msec and a CPU interrupt is generated when the count reaches

zero. The interval timer is reserved for use by the operating system software.

#### 4.4 Manual Control and Display

The control/display panel is illustrated in Figure 21. This panel is located on the front of the IPR digital unit under a hinged door.

The code and data hexadecimal (0-9, A-F) display may be set, blanked (turned off), or blinked by the PR software. It is utilized to display status and define failure during initialization and normal operation of the IPR.

The initialization (INIT) pushbutton switch is depressed to invoke power-up initialization of the PR. The restart (RSET) pushbutton switch is used to invoke restart initialization of the PR. The RSET pushbutton operation is functionally identical to the RSET instruction.

The remaining LED displays are directly driven by the hardware and are not under direct control of the PR software. The run indicators, when illuminated, indicate that the defined CPU is fetching instructions, and that it is not idled (IDLE instruction) or failed.

The fault indicator (FLT) is illuminated for approximately 2 seconds whenever a bus response timeout, invalid op-code, memory parity error, or elapsed watch dog timer error occurs.

The radio transmit indicator (TX) is lit for the duration of a packet transmission. The radio receive 100 Kbit (RX1), or 400 Kbit (RX4) receive indicators are lit for the duration of the packet reception.

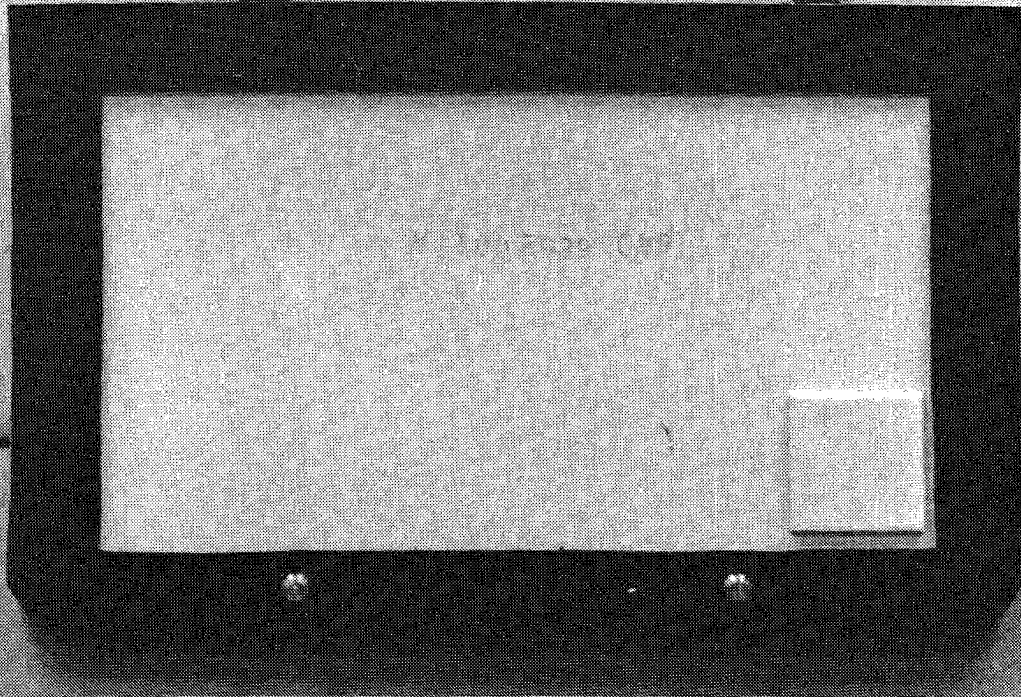
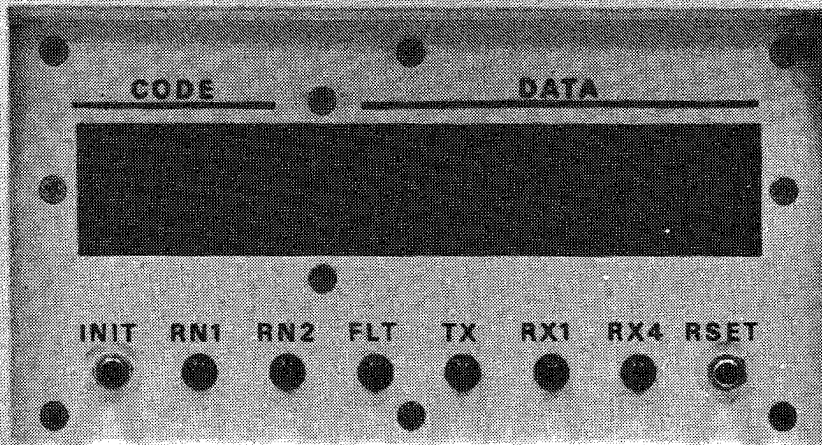
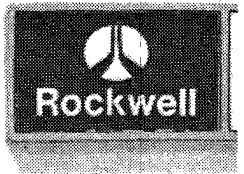


FIGURE 21

IPR DIGITAL UNIT STATUS LIGHTS

#### 4.5 Radio/Digital Interface

The PR is provided with line driver/line terminator circuit cards to allow separation of the radio and digital units. If twisted pair cables are used, the units may be separated by as much as 1000 feet. The cable requires two 55 pin connectors (Cannon KPT06B22-55S) with rubber gaskets (Bendix 113822-55). Figure 22 and Figure 23 define the connections required to build the cable.

#### 4.6 Bus Coupler Interface

In the lower left corner of Figure 10, a connector can be seen that is labeled "buss coupler". A bus coupler may be used to expand the system to a dual bus structure. The device connected to the bus coupler may contain additional CPUs, memory, and peripheral devices. Currently there are no bus coupler circuit boards and no devices designed the attach to the bus coupler. Consequently, the external bus coupler connector can be ignored.

#### 4.7 Maintenance Monitor Interface

In Figure 1 and Figure 7, the back right-hand corner of the radio unit can be seen to have a connector. This connector is labeled "Maintenance Monitor" and is attached to numerous test points within the radio unit. This interface is strictly for use at Rockwell/Collins during the repair and test of radio units.

#### 4.8 Radio Transmit Interface

When a packet is to be radio transmitted, the processor initializes the radio transmit DMA channel by loading the starting address of the packet buffer, the packet length in words, and a control word into registers in the DMA channel board.

The packet data, including the preamble, is sent from memory via the DMA channel to the parallel/serial shift register in the transmit interface. As the TX data is shifted out, a 32 bit CRC checksum is calculated and appended to the end of the packet. When the packet transmission is complete, an interrupt is generated to the CPUs.

<u>DIGITAL BACKPLANE</u>	<u>CONNECTOR</u>	<u>RADIO BACKPLANE</u>	<u>DEFINITION</u>
1-42	z	10-78	TX RATE SELECT -
1-70	y	10-79	TX RATE SELECT +
1-123	BB	10-37	TX REF BIT CLK -
1-121	AA	10-33	TX REF BIT CLK +
1-82	DD	10-70	TX CLK -
1-83	CC	10-72	TX CLK +
1-78	FF	10-74	TX DATA -
1-79	EE	10-75	TX DATA +
1-85	HH	10-83	TX ENABLE -
1-86	GG	10-84	TX ENABLE +
1-57	r	10-119	FREQ CNTL 1 -
1-73	q	10-117	FREQ CNTL 1 +
1-71	p	10-112	FREQ CNTL 2 -
1-69	n	10-109	FREQ CNTL 2 +
1-35	m	10-106	FREQ CNTL 4 -
1-75	k	10-108	FREQ CNTL 4 +
1-67	j	10-97	FREQ CNTL 8 -
1-65	i	10-99	FREQ CNTL 8 +
1-46	h	10-113	FREQ CNTL 10 -
1-58	g	10-120	FREQ CNTL 10 +
1-74	f	10-116	FREQ CNTL 20 -
1-76	e	10-114	FREQ CNTL 20 +
1-44	x	10-98	PWR CNTL A -
1-43	w	10-96	PWR CNTL A +
1-68	v	10-95	PWR CNTL B -
1-66	u	10-86	PWR CNTL B +
1-40	t	10-91	PWR CNTL C -
1-39	s	10-89	PWR CNTL C +

FIGURE 22 IPR RADIO/DIGITAL INTERFACE CABLE - TRANSMIT PORTION



<u>DIGITAL BACKPLANE</u>	<u>CONNECTOR</u>	<u>RADIO BACKPLANE</u>	<u>DEFINITION</u>
1-45	b	10-31	RX ENABLE 100 -
1-33	a	10-71	RX ENABLE 100 +
1-96	Z	10-64	RX DATA 100 -
1-94	Y	10-62	RX DATA 100 +
1-102	X	10-40	RX CLK 100 -
1-100	W	10-39	RX CLK 100 +
1-116	V	10-53	RX EOP 100 -
1-113	U	10-69	RX EOP 100 +
1-41	T	10-81	RX ENABLE 400 -
1-37	S	10-82	RX ENABLE 400 +
1-95	R	10-63	RX DATA 400 -
1-93	P	10-61	RX DATA 400 +
1-99	N	10-42	RX CLK 400 -
1-90	M	10-54	RX CLK 400 +
1-101	L	10-67	RX EOP 400 -
1-103	K	10-65	RX EOP 400 +
1-120	d	10-38	CARRIER SENSE -
1-118	c	10-66	CARRIER SENSE +

FIGURE 23 IPR RADIO/DIGITAL INTERFACE CABLE - RECEIVE PORTION

The CRC shift register is filled with zeros before arrival of the first data bit. The CRC checksum is subsequently calculated on a serial bit stream in the following manner: 1) Shift the 32 bit checksum left one bit, placing a zero in the least significant bit. 2) Exclusive-or the input bit with the most significant bit shifted out of the checksum. 3) If the result of the exclusive-or operation is a 1, exclusive-or the number  $00400007_{16}$  into the checksum.

An "error burst of length N" is defined as the number of bits between the first bit in error in the packet and the last bit in error. The number of bits in error between the first and last is irrelevant to this calculation. A 32 bit CRC checksum has the property of detecting all error bursts of length 32 or less. The probability of a length 33 error burst going undetected is less than  $2^{-32}$ . The probability of an error burst of length greater 32 bits going undetected is less than  $2^{-31}$ .

#### 4.9 Radio Receive Interface

The IPR is able to receive data at either the 100 kbit or 400 kbit rates. Functional operation of the PR is the same for both data rates. In order to receive a packet, the processor initializes the DMA channel by loading a packet buffer address and control word into registers in the DMA board.

When a packet is being received, the data is asynchronously written into memory a word at a time without intervention from the CPUs. As the data is being received, the receive DMA channel automatically calculates a 32 bit CRC checksum and compares it with the checksum appended to the end of the packet. If an error is detected, an error bit is set in the DMA channel's status register.

#### 4.10 Hardware Strapping Options

The IPR hardware utilizes several hardware straps (DIP switches) that are located on the "Configuration/Display Interface" circuit board. Four DIP switch packages are located on the top left corner of this board when viewed with the backplane connector facing to the right. Each package contains eight switches. When the top portion of the rocker switch is depressed, the system software reads a binary zero.

DIP SWITCHES  
DOWN TOWARD  
BOARD CENTER  
Equals "1"

##### 4.10.1 PR ID

The two left-most switch packages define the PR's ID. The most significant bit of the 16-bit PR ID is the left-most switch of the two ID packages.

"9036"

##### 4.10.2 Auto-restart Enable

The left-most switch of the third switch package enables (1) or disables (0) auto-restart in the event of failure of the IPR.

"1"

##### 4.10.3 Down-Line Load Enable

The second switch of the third switch package enables (1) or inhibits (0) the request for a down-line load by the IPR software during the IPR initialization.

"1"

##### 4.10.4 Default RF Frequency

The right-most six switches of the third switch package define the default radio RF frequency utilized for down-line loading of the IPR. The binary value in the switches and the corresponding RF frequency are shown below.

Because the radio unit has a mechanically tunable 50 MHz bandpass filter, the default frequency must be within the frequency range defined by the filter. Definition of a frequency outside the range of the bandpass filter may damage the RF head.

"100100"  
1508.3 MHz

Freq selection  
MUST be within  
50 MHz BANDPASS

SWITCHES	RF FREQ (MHZ)
111001	1712.3
111000	1718.7
110111	1725.1
110110	1731.5
110101	1737.9
110100	1744.3
110011	1750.7
110010	1757.1
110001	1763.5
110000	1769.9
101001	1776.3
101000	1782.7
100111	1789.1
100110	1795.5
100101	1801.9
100100	1808.3
100011	1814.7
100010	1821.1
100001	1827.5
100000	1833.9
011001	1840.3

NO Jumper = 1  
Jumper = 0

Field NET →  
LAB NET →  
20 -

1782.7 officially OK @ JAC  
3/82 @ JAC per  
SALMON NOTE 4/23/82

ok Freqs  
w/0 Returnng  
T/R FILTER Toned Here  
-3dB @ 1796.1  
1846.1  
For GS-82

The six frequency switches are used to control a 6-bit BCD divide chain. The allowable switch values shown above represent BCD numbers ranging from 19<sub>10</sub> to 39<sub>10</sub>. If a BCD number less than 19 is used, the frequency generated will be too high and will be filtered out in the T/R filter. There are no BCD numbers higher than the legal 39. If the switches are set to a value that is not a valid BCD number, the frequency generated is indeterminate.

4.10.5 Initialization Control

The left-most five switches of the right-most switch package are unused and undefined. The remaining three switches are used for special maintenance and test options during initialization. All switches in this package are normally set to binary zero.

- Switch 6      Loop on Error
- Switch 7      Write Memory in Loop on Error
- Switch 8      Do mini-initialization

#### 4.11 Power On

After installing the PR in a new location, the plug-in circuit cards and modules should be checked to ensure none were jarred loose during installation. The handles should be pushed all the way in under the retaining lip of the card cage. Fuses, located in the back of each unit, should always be checked before power on. Should the PR fail to operate properly, the operator should contact Rockwell/Collins.

In order to turn on an IPR radio unit, connect the radio/digital interface cable and the +24 VDC power cable. The toggle switch on the back door of the radio unit should be in the "ON" position. This switch is a troubleshooting service switch which disables the IPR's RF head when in the "OFF" position. This switch should only be used by authorized service personnel.

The hardware straps on the configuration board must be set to the proper positions. If a terminal is to be used, ensure the rotary baud rate switch is properly set.

## 5 OPERATING PROCEDURES

The following paragraphs describe operator actions and display visible to the operator during operation of the PR.

### 5.1 Operation/Hardware Strap Options

The hardware straps which effect PR operation are described in Section 4.10. The terminal type and terminal baud rate switches must be set for the console connected to the PR I/O channel. The PR ID switches are set to uniquely define the PR. The auto-restart and down-line load switches are set to define the appropriate operational configuration as described below. The radio RF frequency switches are set to define the value used for down-line loading of the PR. User jobs may use this value or other values. The initialization mode switches are normally zero except when initialization faults need to be debugged.

For changed values of the auto-restart, down-line load, and/or radio RF frequency switches to take effect, power-up initialization must be (re)executed, i.e., the INIT pushbutton must be pushed or the IN console command must be executed.

#### 5.1.1 Normal Unattended Operation

For normal PR operation, unattended by an operator, auto-restart and down-line load are enabled via the hardware switches. The PR I/O channel console need not be implemented except for use as a monitor display. After initial initialization invoked by the operator, down-line loading of the remaining portion of the operating system and the user jobs and initiation of job execution is done automatically. The PR will auto-restart and if necessary reload software in the event of failure.

Operational sequence

Operator action	Depress and release front panel initiate (INIT) pushbutton.
Display	Console bell, then LED display of sequential execution of initialization sections 1-6 (01-06 in code LEDs) by each CPU (N000 in data LEDs, where N is the CPU number). Blinking display if errors. See Section 5.2.
Display	LED display of initialization section 7 by one CPU plus console message for down-line load of operating system:  DOWN-LINE LOAD-END  Blinking LEDs and console messages if error. See Section 5.2 and Section 5.4.17.
Display	LED display of initialization section 8 by each CPU (08 in code LEDs, N000 in data LEDs). Blinking display if errors. See Section 5.2.
Display	LED display (09 N000) and console messages for initialization and job loading:  DOWN-LINE LOAD-END  Blinking LEDs and console messages if error. See Section 5.2 and Section 5.4.17.
Display	Final LED display for successful initialization is 0F 0000. Console message for Debug job initiation:  JOB DEBUG
Display	Console message for initiation of job execution:  AUTO-XJ  LED display is blanked (turned off).

5.1.2 Normal Attended Operation

For normal PR operation, attended by an operator, auto-restart is enabled and down-line load is disabled via hardware switches. The remaining portion of the operating system and the user jobs are loaded by the operator via the PR I/O channel console. Job execution is

initiated via the operator XJ console command. The PR will auto-restart in the event of failure. Additional operator action is required only if reloading of software is necessary.

### Operational Sequences

Operator Action	Depress and release front panel initiate (INIT) pushbutton.
Display	Console bell, then LED display of sequential execution of initialization sections 1-6 (01-06 in code LEDs) by each CPU (N000 in data LEDs, where N is the CPU number). Blinking display if errors. See Section 5.2.
Display	LED display of initialization section 7 by one CPU plus console message for loading of operating system:  TURN TAPE ON-TURN TAPE OFF-END  Blinking LEDs and console messages if error. See Section 5.2 and Section 5.4.17 for tape cassette load procedure.
Display	LED display of initialization section 8 by each CPU (08 N000 in code/data LEDs). Blinking display if errors. See Section 5.2.
Display	Final LED display for successful initialization - OF 0000. Console message for Debug job initiation:  JOB DEBUG  Debug job is executing in PR halted (stand-alone) mode. Operator is required to load jobs and initiate job execution. See Section 5.4 for console commands.

### 5.1.3 Maintenance/Test Operations

For diagnostic testing and maintenance of the IPR, auto-restart and down-line load are normally disabled via the hardware switches. A local I/O channel console with software load capability is implemented. Alternatively a simpler local console (keyboard/printer) may be used if down-line load (switch) is enabled to remotely load the operating system and off-line diagnostic software.



For special maintenance situations, the initialization mode switches may be set (See Section 5.2.3.1), the load-and-go capability (see Section 5.2.3.2) may be used, or the operator GO (see Section 5.4.15) command may be used.

The operational sequence is the same as shown in Section 5.1.2. The operating system is down-line loaded or loaded locally by the operator depending upon the down-line load switch. The final LED display is 0F 0000 or blinking 0F nnnn to define the number (nnnn) of initialization errors. Also if errors, the console message below is printed:

#### INIT/RSET FAULT

#### 5.1.4 Operator Action Following a Fault

If the PR is configured for auto-restart, initialization is automatically invoked as part of the fault service. If not, the operator must manually restart the system following a fault. This may be done either by executing the restart (RS) command or by depressing the RSET pushbutton. The execute jobs (XJ) command should not be executed following any fault except "TRACE FAULT". Other operator control/monitor console commands may be entered before restarting the system.

#### 5.1.4.1 LED Fault Display

During steady-state operation, hardware faults are displayed in the front panel LEDs in the following format:

Code digit 1:	CPU number
Code digit 2:	Type
Data digits 1-4:	PC, for type > 0
	ST, for type = 0
Type bit 0 on:	Watch dog timer
Type bit 1 on:	Bus response time-out
Type bit 2 on:	Invalid op-code
Type bit 3 on:	Memory parity error
Type = 0:	Unused interrupt

For the hardware faults which cause a failure interrupt, the program counter (PC) when the fault interrupt occurred is displayed. A failure interrupt is not presented to the CPU until the instruction after the one which caused the failure, and by the time it is recognized by the CPU, the program counter (PC) will have been incremented once again, i.e., the PC displayed points to the instruction which is two instructions beyond the instruction which actually caused the hardware failure.

For unused interrupts, the status (ST) after the trap has taken is displayed. The CPU sets the interrupt mask - the least four significant bits of the ST - to a value one less than the interrupt level. For example, a ST = 0001 would indicate that a level 2 interrupt had occurred. Levels 2, 5, 10, 13, 14, and 15 are unused.

Because of the often repetitive nature of hardware faults, the fault service includes a safeguard that only one fault per CPU can occur without restarting the system. If a second one does occur, the CPU takes one of three actions, depending on the switch settings: if auto-restart and down-line load are enabled, power-up initialization is invoked; if auto-restart is enabled but down-line load is not enabled, restart initialization is invoked; if neither auto-restart nor down-line load is enabled, the CPU idles.

#### 5.1.4.2 Console display

All faults, hardware and software, are printed on the console in the format of the message display for the display job (DJ) command shown in Section 5.4.8.

## 5.2 Initialization

### 5.2.1 Causes

When power is first applied to the PR, power-up initialization occurs. If power is lost and then re-applied before initialization has completed, the section currently being executed is begun again. After initialization has been completed, a loss and re-application of power causes restart initialization to begin again.

Pushing the INIT pushbutton at any time causes power-up initialization. Pushing the RSET pushbutton causes the initialization section being executed to be begun again. After initialization has been completed, pushing the RSET pushbutton causes restart initialization to begin again.

After initialization has completed, the operator may enter console commands. The IN command is functionally equivalent to the INIT pushbutton; executing it causes power-up initialization. The RS command is functionally equivalent to the RSET pushbutton; executing it causes restart initialization.

In order to re-initialize the system after initialization has completed, push RSET or execute the RS command if you don't need any of the sections of power-up (RAM tests, mapping register tests, or bootstrap load) to be done. Otherwise push INIT or execute the IN command. Do not select INIT or IN if the contents of any of the RAM, e.g., loaded jobs, need to be preserved.

### 5.2.2 Displays

#### 5.2.2.1 LED display

The format of the front panel LED display during initialization is as follows:

Code Digit 1:	0
Code Digit 2:	Section ID

Data Digit 1: CPU number

Data Digits 2-4: Error code (if blinking)

As each CPU starts execution of each section, the section ID and CPU number are displayed. The section IDs are listed in Figure 24.

When an error is detected during initialization, its code is superimposed on the LED display as the last 3 digits of the data LEDs, and the display is blinked for at least 2 seconds. The error codes are listed in Figure 25.

An "F" is displayed in the second digit of the code LEDs and the total number of initialization errors is displayed in all 4 digits of the data LEDs in the last section. If the number of errors is non-zero, the display is blinked.

#### 5.2.2.2 Console messages

The beginning of power-up initialization is announced by the console bell.

Section 7 includes the bootstrap load of the operating system. The console messages and operator actions are described in Section 5.4.16 or Section 5.4.17. Section 9 may include a job down-line load with the accompanying console message:

DOWN-LINE LOAD-END

After initialization has completed, if there were any errors, the following console message is printed:

INIT/RSET FAULT

In any case, the message announcing the beginning of the execution of Debug is then printed:

JOB DEBUG

	SECTION ID	SECTION NAME
	-----	-----
Power-Up	1	PROM checksum test
	2	RAM test with incrementing test values
	3	RAM test with decrementing test values
	4	Mapping register read back test
	5	Mapping register address memory test
	6	RAM test/initialization with zero
	7 <sup>[1]</sup>	Bootstrap load and checksum generation
Restart	8	OS initialization and OS checksum tests
	9	OS initialization and jobs' load and checksum tests
	A <sup>[2]</sup>	Error summary

[1] Section ID 7 is displayed only by the first CPU to execute it.

[2] When the number of errors is displayed, the section ID character changes to an F.

FIGURE 24 DEFINITION OF INITIALIZATION SECTION IDS

ERROR CODE	SECTION ID	ERROR DESCRIPTION
100-108	7,9	Load error - see Section 5.4.16 (LED error 10N corresponds to printed error N)
901	4	Bias register 1 did not read back correctly
902	4	Limit register 1 did not read back correctly
903	4	Bias register 2 did not read back correctly
904	4	Limit register 2 did not read back correctly
905	4	Bias register 3 did not read back correctly
906	4	Limit register 3 did not read back correctly
AOX <sup>[1]</sup>	6,8	Checksum for zone 4 address space X incorrect
AYY <sup>[2]</sup>	9	Checksum for job YY incorrect
BOX <sup>[1]</sup>	6,8	Parity or bus time-out error in zone 4 address space X
BYY <sup>[2]</sup>	9	Parity or bus time-out error in job YY
COO	8,9	Parity error in zone 4 RAM (CPU addresses A810-BFFE, bus addresses FD408-FDFFF)
ZZZ <sup>[3]</sup>	2,3,6	RAM test error between bus addresses ZZZ00 and ZZZFF
ZZZ <sup>[3]</sup>	5	Mapping register address memory test error at bus address ZZZ00

[1] The zone 4 address spaces are:

X	CPU Addresses	Bus Addresses
1	F000-FFFE	FF800-FFFFFF
2	E000-EFFE	FF000-FF7FF
3	AD42-AE2E	FD6A1-FD717
4	B124-B7D2	FD892-FDBE9

[2] Jobs are numbered  $05_{16} \leq YY \leq 28_{16}$

[3] The possible values of ZZZ depend on where RAM is actually installed. Currently,  $000 \leq ZZZ < 018$ ,  $040 \leq ZZZ < 04C$ , or  $FD4 \leq ZZZ < FE0$ .

FIGURE 25 DEFINITION OF INITIALIZATION ERROR CODES

### 5.2.2.3 Error Information Stored in Memory

Information about initialization errors is stored in memory. The total number of errors is stored at the location labeled "WSINER". The first error's section ID, CPU number, and error code (i.e., 2 words which are the contents of the front panel LEDs), the CPU's status, program counter, and workspace pointer, and the contents of the 16 workspace registers are stored at the location labeled "ERBFR". The number of times the PR has restarted, without going back to power-up initialization, is stored at the location labeled "WSINRC".

## 5.2.3 Special Test Modes and Procedures

### 5.2.3.1 Test Mode Switches

Three switches on the Configuration Board control special initialization test modes to aid in debugging:

Bit 13: Loop on error

Bit 14: Write in loop in error

Bit 15: Mini-initialization

The "loop in error" switches (bits 13 and 14) have effect only when an initialization error has been detected. Once an error has been detected, the CPU will loop indefinitely on the set of instructions which caused/detected the error. Errors are displayed only momentarily, rather than for 2 seconds, and the display returns to normal for the loops in which the error is not detected. Each loop is fast enough to allow oscilloscope and/or logic analyzer investigation.

The "write in loop in error" mode (bit 14) is identical to the "loop on error" (bit 13) mode except for the addition of the appropriate write instruction in the loop. For example, the RAM test would add the write instruction:

```
MOV  R0,*R2
```

to the loop containing the read and test instructions:

```
MOV  *R2,R1
C    R1,R0
```

The mini-initialization mode (bit 15) is used when the only desire is to complete initialization in order to use Debug commands like AM, DM, and LD. The mini-initialization mode skips sections 1 through 5. It also displays errors only momentarily (although the total number of errors, if any, is still displayed at the very end).

The following rules apply to the interaction of the enabled switches:

- . Bit 13 (loop on error) overrides Bit 0 (auto-restart)
- . Bit 14 (write in loop on error) overrides Bits 0 and 13
- . Bit 15 (mini-initialization) overrides Bits 0, 13, and 14

#### 5.2.3.2 Bootstrap Load and Go

Instead of loading the O.S. cassette tape, you can load other absolute, i.e, not relocatable, programs for immediate execution. Such a load and go program is identified by adding the entry point address as the operand of the END statement. This produces a "1" tag followed by the address in the object code. The loader, having read this "1" tag and the address, branches to the address after finishing the load.

You should be aware of the environment in which a load and go program will execute. The CPU that does the load (CPU A) is the one that will execute the program. The workspace in which execution will begin is "WSTRMS", currently at address AACC<sub>16</sub>. If you desire a different workspace, do a LWPI instruction. Interrupts will be masked off; doing a LIMI instruction will change that.

You should also be aware of the other CPU (CPU B) the one that didn't do the load. It will stay in the ABS loop at "IN3000" until the CPU executing the load and go program (CPU A) does a RSET



instruction or changes workspace "WSIN" register R7 to a negative value. After CPU B is released from the ABS loop, it will display section 1 and its CPU number in the LEDs and then branch to the contents of workspace "WSIN" register R10 (B \*R10). This means that the load and go program should set WSIN's R10 to the entry address appropriate to CPU B before setting WSIN's R7 negative.

You can write a source load and go program, assemble it, and dump the object file on cassette, or you can just create the machine code on cassette directly. The cassette should be formatted according to the instructions in the following paragraphs.

Every record should start with a line feed and an asterisk (\*), except the first record, which should start with a less-than sign (<). Every record should end with an "F" and a carriage return, except the last record, which doesn't need the "F".

The first record should have a "<", followed by five zeros and the 8 character name of the program, ended by an "F" and a carriage return.

All other records, except the next-to-last and last, after the line feed and "\*", should have a "9" and a four-hex-digit absolute address at which to start loading consecutive data, followed by up to 12 groups of "B" and a four-hex-digit datum to load, ended by an "F" and a carriage return. For example, the record

```
*9AD40B02E0BA880F
```

would cause the data  $02E0_{16}$  and  $A880_{16}$  (LWPI >A880) to be loaded at locations  $AD40_{16}$  and  $AD42_{16}$ , respectively.

The next-to-last record, after the line feed and "\*", should have "1" and the absolute entry address of the program, ended by a carriage return.

The last record should have a line feed, "\*", colon ":", and carriage return.

### 5.3 Operator Interface for Console I/O

The console I/O routines implement job requested output to the local (RS-232 interface) console and allow an operator to address input to different jobs. The single console is time-shared between the multiple jobs of the IPR.

If several jobs were allowed to interleave their outputs without any delimiting character or phrase, the resulting display could be very confusing to the operator. For this reason, the console I/O routines will insert the phrase "JOB XYZ" before job XYZ's output is printed. If job XYZ makes several output requests before another job requests an output, the phrase "JOB XYZ" is only printed before the first output.

The console I/O routines allow an operator to type an arbitrary character string and indicate which job is to receive the input. To designate an input for a particular job, the operator must type "@" followed by the job name, a space, and the desired input string terminated by a control-E (ETX) or a carriage return (CR). For example, in order to give the input string "PQR" to job "XYZ", the operator would type

```
@XYZ PQR (ETX or CR)
```

The job name may be abbreviated to any number of characters. If the abbreviated name is not unique, the console I/O routines will give the input to the first job requesting input that matches the abbreviated name. For example, suppose the list of jobs requesting input contained the following jobs in this order: XYZ, ABC, ACB. The job XYZ could then be referenced in any of these ways:

```
@X PQR (ETX or CR)
```

```
@XY PQR (ETX or CR)
```

```
@XYZ PQR (ETX or CR)
```

The job ACB could be referenced in two ways:

@AC PQR (ETX or CR)

@ACB PQR (ETX or CR)

If the name ACB were abbreviated to simply A, the input would be given to job ABC.

The specific job to receive input need not be explicitly stated for every input. If the first character the operator types is not "@", then everything typed is given to the last job that was explicitly specified. On initialization or when the PR is halted, the job Debug is assumed to have received the last input.

While inputting characters, the operator has limited editing capability. The rub-out (DEL) character deletes the last character input by the operator and is echoed by "\". Several characters can be deleted by repeatedly hitting DEL. To delete all characters previously entered and exit the input mode, the operator should type ESC, which is echoed by "\$", carriage , and line feed.

If the operator attempts to input a character and is echoed by "\$", carriage return, and line feed, then all three input buffers are busy, i.e., the buffers have not yet been released by jobs that previously received input.

If an operator attempts to input a line of text and "?" is printed, then either the job name entered is not in the system job list or the job specified will not accept input.

#### 5.4 Operator Control/Monitor (DEBUG) Commands

The following paragraphs describe the operator console commands used to control and monitor PR operation, to support PR software development, and to support PR hardware testing and maintenance.

##### 5.4.1 Operation

The Debug job may be executed in normal PR operation or PR halted (stand-alone) operation. In normal operation, Debug is executed

like any other job. It may be called by the operator or by another job. It shares the I/O channel console with other jobs.

When the PR is halted, Debug is executed in a single CPU independent of the normal scheduler. Console and radio/1822 DMA I/O are executed in a polling non-interrupt driven mode. The console is dedicated to the Debug job. No other jobs are executed.

The PR halted mode is invoked by hardware or software failure, upon completion of PR initialization, upon execution of a software trace breakpoint, or by operator or another jobs HJ, TJ, IN, or RS console command. Normal execution is invoked by the operator XJ command or by automatic XJ if auto-restart is enabled and jobs are resident. If the PR is halted by the operator HJ command or by an operator specified breakpoint then the operator must input the XJ command to resume normal operation.

All operator commands are valid when the PR is halted. Some commands are invalid in normal operation.

#### 5.4.2 Operator Command Input

The operator in normal PR operation must direct Debug command input to the Debug job by typing

@DEBUG

prior to the command. This is done once and need not be repeated until the operator wishes to input to another job. A truncated job name may be used as long as it is unique.

The input "@DEBUG" is not required when the PR is halted (stand-alone) and will if input be interpreted as a command error. All console input is given to Debug when the PR is halted.

An operator begins with a two character command code, sometimes followed by one or more operands, and terminated by the single character Control-C (ETX) or carriage return. Debug provides for command chaining. The ";" separates individual commands. ETX or

carriage return terminates the single or set of chained commands. One or more ASCII space characters are used to separate command codes and operands in command strings. Input may be edited, as described in Section 5.3, until input of ETX or carriage return. Operator input for a single command or set of chained commands is limited to a single console line.

Debug interprets and executes the command. Upon completion of command processing a carriage return, line feed, line feed is output. If a command input syntax error is detected, the message "CMD?" is printed.

All numeric operator input and numeric display is in hexadecimal 0-9, A-F.

#### 5.4.3 Restart Initialization (RS) Command

The RS command is equivalent in operation to depression of the front panel restart (RSET) pushbutton. A RSET instruction is executed to invoke restart initialization. Command chaining after RS is permitted. The RS command is always valid.

#### 5.4.4 Power-Up Initialization (IN) Command

The IN command is equivalent to depression of the front panel initiate (INIT) pushbutton. Commands chained beyond IN are lost. The IN command is always valid.

#### 5.4.5 Halt Jobs (HJ) Command

The HJ command is used to halt execution of all PR jobs. Any job currently executing (busy) is checkpointed. Normal operation is suspended and the PR enters the PR halted (stand-alone) mode of operation. The HJ command is always valid.

#### 5.4.6 Terminate Jobs (TJ) Command

The TJ command discards all jobs by clearing the system job index and system job list of all entries. Restart initialization is invoked by execution of the RSET instruction. The TJ command is always valid.

#### 5.4.7 Execute Jobs (XJ) Command

The XJ command initiates normal PR operation. All idle or halted jobs are called. The XJ command is valid only when the PR is halted. Automatic execution of this command is indicated by a console message saying "AUTO-XJ".

#### 5.4.8 Display Jobs (DJ) Command

The DJ command is used to display the state of an operator selected job (or CPU), or all jobs. It is used automatically to describe a job or CPU halt due to failure or trace breakpoint. Further, the job specified by the operator or halted job defines the job (or CPU) referenced in other commands. The commands which relate to a specific job are DM, AM, DR, AR, and ST.

The three operator command input options are shown below. These commands are always valid.

DJ

DJ jobname

DJ ALL

If the job name is omitted, the currently selected job is displayed. The one to five character name specifies the desired job. "ALL" requests the display of all resident jobs in sequential order. Additionally the ALL option displays the PR ID and current operational mode as shown below:

PR I.D. XXXX HALTED

PR I.D. XXXX

The job or halted CPU state is displayed as shown below:

JOB jobname

state reason CPU n ST: XXXX PC: XXXX WP: XXXX

The "jobname" defines the job or CPU. The CPU name (CPU 1, CPU 2, etc.) is printed instead of a job name for PR halts which may not be associated with a system job.

The "state" describes the job's current execution state, as follows:

BUSY	Job busy executing
HALTED	Job halted due to hardware failure, job detected failure or software trace breakpoint
SPNDED	Job execution suspended
CKPTED	Job execution checkpointed
IDLE	Job has never executed or has been re-initialized

The "reason" describes why a job is halted, as follows:

TIMER FAULT	Watch dog timer elapsed
BUS TIMEOUT FAULT	Bus response timeout
INV OPC FAULT	Invalid instruction operation code
PARITY FAULT	RAM or PROM memory parity error
TRACE FAULT	Software trace breakpoint trap
FAULT	Job detected fault invoked by "XOP @XHALT,JBCTRL" instruction
INTR FAULT	Invalid (unused) interrupt fault

CPU n, where n equals 1, 2, 3, etc., identifies the CPU which is executing or has last executed the job.

XXXX respectively describes the current contents of the non-busy job's CPU status (ST), program counter (PC), and workspace pointer (WP) registers. The PC defines the address of the next instruction to be executed.

XXXX is an absolute 16-bit CPU address or status register value. A job's zone 2 address for the PC and WP register content is displayed as XXXXR. R following the address indicates that the relocation constant has been subtracted from the absolute address before display. XXXXR defines the job address as it appears in the source/object program listing (see use of XXXXR address specification in AM/DM commands).

#### 5.4.9 Display Memory or Peripheral I/O (DM) Command

This command is used to display the contents of selected RAM, PROM, or peripheral device registers. The operator may display single locations or a series of locations between specific address limits. The operator may specify the addresses of locations to be displayed as a 20-bit absolute CPU address, as a 16-bit absolute CPU address, or as a 16-bit CPU byte address relocated to a specific job's zone 2 address space. Example of the operator input options and resulting display are shown below. These commands are always valid. Operator input is underlined.

```
DM F000
F000 AAAA
```

```
DM E124 E128
E124 0431 0006 072C
```

```
DM 400R
0410 0000
```

```
DM OW 8W
00000 0100 B67E 0100 B686 0100 B67E 0080 B6EC
```

The first example illustrates the display of a single absolute 16-bit CPU byte address  $F000_{16}$ . The second example illustrates the display of a series of locations  $E124_{16}$  to  $E128_{16}$ . The third example illustrates use of the absolute 16-bit CPU byte address relocated in zone 2. The character "R" immediately following the address specifies this option. This option allows the operator to input an address from the job source/object listing and have it relocated to its absolute value in zone 2. The last example illustrates use of the absolute 20-bit address option.



Leading zeros in all addresses may be omitted. Mixed address formats in a single command are not permitted. The 16-bit CPU addresses are incremented by 2, while 20-bit absolute address are incremented by 1 for each consecutive location.

#### 5.4.10 Alter Memory or Peripheral I/O (AM) Command

This command is used to alter (modify) the contents of selected RAM memory or peripheral device interface registers. The operator may modify single locations or a series of locations beginning at a selected address. Locations in a series may be selectively skipped. As in the DM commands, the selected address may be an absolute or relocated 16-bit CPU byte address, or an absolute 20-bit bus address. The operator input options are illustrated below. These commands are always valid.

AM F000 123

AM F000 1234 S 4567

AM 300R 460 310R

AM F0001W ABCD

Line 1 modifies absolute 16-bit CPU address  $F000_{16}$  to contain  $0123_{16}$ . All data input is right justified in one 16-bit word. Line 2 modifies locations  $F000_{16}$  and  $F004_{16}$  to contain  $1234_{16}$  and  $4567_{16}$ , respectively. The character "S" causes, in this case, location  $F004_{16}$  to be skipped.

Line 3 modifies two locations,  $300_{16}$  and  $302_{16}$ , relocated to the selected job's zone 2 address space. The data  $0310_{16}$  will be modified by the value of the job's zone 2 relocation displacement. Line 4 modifies absolute bus location  $F0001_{16}$  to contain  $ABCD_{16}$ .

Data operands or skip location characters are delimited by one or more space characters. Input is limited to a single console line. Leading zeros in address or data operands may be omitted. Consecutive data operands modify consecutive locations from the selected start

address. A 16-bit CPU byte address increments by 2, a 20-bit bus address increments by 1 to address the next consecutive location.

#### 5.4.11 Display Job Registers (DR) Command

This command is used to display the contents of a selected job's registers: status (ST), program counter (PC), workspace pointer (WP), or workspace registers (R0-RF) defined by the workspace pointer. A specific job is selected by the Display Job (DJ) command. The operator input options are shown below. These commands are always valid.

DR ST

DR PC

DR WP

DR Rn<sub>1</sub>

DR Rn<sub>1</sub> Rn<sub>2</sub>

The numbers n<sub>1</sub> and n<sub>2</sub> are hexadecimal numbers, i.e., 0-9 or A-F.

Lines 1, 2, and 3 illustrate the operator input to display respectively the selected non-busy job's ST, PC, and WP registers. The display via printed messages is identical to the Display Memory (DM) command display where the first column displays the address and the second column the contents of the selected register.

Lines 4 and 5 illustrate respectively the operator input to display the contents of a single workspace register or a consecutive series of registers Rn<sub>1</sub> through Rn<sub>2</sub>. As above, the display via printed messages is identical to the Display Memory (DM) command display.

#### 5.4.12 Alter Job Registers (AR) Command

This command is used to alter (modify) the current the current contents of a selected job's registers: status (ST), program counter (PC), workspace pointer (WP), or workspace registers. A specific job is

selected by the Display Job (DJ) command. The operator input options are shown below. These commands are valid only when the PR is halted.

AR ST F

AR PC 300R

AR WP 0200

AR Rn F123

AR Rn 1234 5678

The number n is a hexadecimal digit, i.e., 0-9 or A-F.

Lines 1, 2, and 3 illustrate the operator input to modify respectively the contents of the ST, PC, and WP registers to contain  $000F_{16}$ ,  $0300_{16}$  plus job relocation displacement, and  $0200_{16}$ . A single register may be modified per operator command. Line 4 illustrates the operator input to modify a single workspace register. Line 5 illustrates the operator input to modify a series of consecutive workspace registers, beginning at the specified register. Data input formats are identical to data input for the Alter Memory (AM) command.

#### 5.4.13 Set Trace Breakpoint (ST) Command

This command is used to select one to six software instruction trace breakpoints. The operator input is shown below. These commands are valid only when the PR is halted.

ST E100

ST 300R 310R 314R 500R 504R 506R

ST S 320R 0

Line 1 illustrates the operator input to define the first trace breakpoint at location  $E100_{16}$ . A previously defined first trace breakpoint is discarded. The remaining five breakpoints are unchanged. Line 2 illustrates selection of all six trace breakpoints. All breakpoints, in this case, are relocated to the selected job's zone 2

address space. the job is selected by the Display Job (DJ) command. Line 3 illustrates the operator input which skips the first breakpoint (breakpoint remains as previously defined), defines the second breakpoint, and clears the third breakpoint. All breakpoints may be cleared by use of the Clear Trace (CT) command. Guidelines for selection of trace breakpoints are listed below:

1. Trace breakpoints for more than one job may be concurrently defined. Previously selected breakpoints may be cleared or redefined regardless of previous job selection.
2. Trace breakpoint word aligned addresses must define the first word of multiword length instructions. They must define an instruction (not data) address.
3. Multiple trace breakpoints must not define the same address.
4. Trace breakpoints may be selected in reiterative program sequences as long as continuation address is included. Trace continuation is described below.
5. The 20-bit bus address (W) form may not be used to define trace breakpoints.

The SET Trace (ST) command inserts breakpoints. The instruction at the selected address is saved and replaced by an "XOP R0,TBPT" (2C80<sub>16</sub>) instruction. Job execution is initiated with the XJ command. Execution continues normally until a trace breakpoint is encountered.

Upon execution of the breakpoint instruction, the operating system captures the machine state of the trace halted job, halts execution of all other jobs, and calls the Operator Control/Monitor (Debug) job which displays the state of the trace halted job as shown in Section 5.4.8. Other debug job commands may be used to further investigate the state of the PR at the trace breakpoint.

Software execution may be continued from the trace breakpoint location by use of the Execute Jobs (XJ) command. When the job initiate address (current PC) equals a selected breakpoint, a continuation breakpoint is created at the next instruction location from the breakpoint if this location is not also a selected breakpoint. The breakpoint location is restored. The operating system regains control via the continuation breakpoint, restores the continuation location, and inserts the breakpoint instruction at the original breakpoint. Execution is then continued normally from the continuation breakpoint location.

#### 5.4.14 Clear Trace Breakpoint (CT) Command

The CT command is used to clear all previously selected trace breakpoints. The original instructions at the trace breakpoints are restored. The CT command is only valid when the PR is halted.

#### 5.4.15 Execute Operator Routine (GO) Command

The GO command specifies an entry address and transfers control to an operator specified routine. The GO command is always valid. A sample of an operator's input is shown below.

```
GO 440R
```

Only absolute or relocated 16-bit byte address entry addresses are permitted. The operator routine, typically defined by an AM command, is entered at the specified address. The routine executes as part of the Debug job.

Only registers R0-R8 may be used if a new workspace is not defined by the routine. To resume normal Debug execution, the routine should be exited with a "B \*R13" (045D<sub>16</sub>) instruction.

The GO command is intended for use in special test/maintenance situations.

#### 5.4.16 Console Load (LD)/Load Verify (LV) Commands

These commands are used to load (LD) object software into the PR, or to verify the correctness of previously loaded software (LV). The LD and LV commands are only valid when the PR is halted.

Object code is typically contained on cassettes for the TI Silent 700 terminal. The object code is input from the terminal connected to the RS-232 channel. After operator input of the LD or LV command, the operator is instructed to start data input by the message below.

TURN TAPE ON

To input data from the tape cassette:

1. Insert tape cassette in terminal.
2. Set Record/Playback switch to playback.
3. Set Playback switch to LINE.
4. Set Tape Format switch to LINE.
5. Depress Rewind followed by LOAD/FF to rewind tape and set tape to load point.
6. Depress Playback Control CONT START.

If an error is detected during the load the error message illustrated below is printed.

-ERROR n jobname aaaa

The error number "n" describes the failure as shown below.

Error 0 - A load verification of a relocatable job was requested, but the job did not exist in the system job list.

Error 1 - A relocatable job load was requested, but there were no empty entries in the system job list.

- Error 2 - The checksum at the end of an object code record does not match the checksum calculated while inputting the record.
- Error 3 - While loading a program, no characters were received for 150 character periods.
- Error 4 - An object code tag not supported by the loader was encountered.
- Error 5 - A job checksum error was detected in a job, or a bus time-out or memory parity error was detected while generating and testing the checksum of the load.
- Error 6 - Load verification error. The data word from tape did not equal the resident word.
- Error 7 - A memory parity error failure was detected.
- Error 8 - A bus time-out failure was detected.

The job name is printed for errors detected during loading of the job. The hexadecimal number "aaaa" is a 16-bit CPU address. For errors 6, 7, and 8, "aaaa" defines the memory address in error or address accessed when the error occurred.

Upon completion of the load (with or without errors), the message below is printed.

-TURN TAPE OFF

The operator should stop data input by depressing the STOP switch opposite the CONT START position. After data input has ceased, the message below is printed.

-END

The message resulting from an error free load or load verify is shown below.

-TURN TAPE ON-TURN TAPE OFF-END

5.4.17 Down-Line Load (DL)/Load Verify (DV) Commands

These commands are used to down-line load (DL), or down-line verify (DV) object data via the PR radio or 1822 interface. The commands may be used regardless of the value of the down-line load enable hardware switch. The commands are only valid when the PR is halted. The operator may specify the name of the load data file. Operator input is shown below.

DL jobname

DV jobname

The one to seven character jobname if specified is inserted in the load request ROP packet. If omitted any load object file will be accepted (file name in load request ROP is ETX only). After the command input, the message below is printed on the I/O channel console to indicate initiation of the load.

DOWN-LINE LOAD

Errors detected during loading are identified via console message shown below as described in Section 5.4.17.

-ERROR n jobname aaaa

Completion or termination due to error of the down-line load or load verify is indicated by the console message below.

-END

The console message for an error free load or load verify is shown below.

DOWN-LINE LOAD-END



## 6 CHANNEL ACCESS PROTOCOL

The following section will define the format of the current packet header. In addition, a list is made of those items in the header for which the user is responsible. The channel access protocol and its associated header are quite volatile and a user should contact Rockwell-Collins or BBN before actually writing software to interface to a Packet Radio.

### 6.1 Packet Header Format

The packet header implemented and utilized by the PR's is shown in Figure 26. The design goal is that this header contain only those elements necessary to support packet transport protocol within the PRN and not include elements of other protocols. These elements may exist in packet text and will be transparent to the PR's and packet transport protocol.

Figure 26 illustrates the packet header as it appears in PR memory. In word #6, bits 11-15 are currently undefined and not used. The remaining fields of the packet header are defined below.

HOP COUNT	A four bit field (bits 12-15 of word 1) indicating progress along a route. The hop count is incremented (modulo 16) whenever the packet is forwarded over the radio. The hop count is used in hop acknowledge recognition.
HEADER LENGTH	Four bit field (bits 8-11 of word 1) to define the packet header length in 16 bit words.
PACKET LENGTH	Eight bit field (bits 0-7 of word 1) to define the packet length in 16 bit words. The length includes the header plus the text but excludes the 3 word preamble and 2 word checksum. Packets ransmitted or received by the PR's radio may be a maximum of 127 words in length excluding preamble and checksum.

- (1) Hop Count, Header Length, Packet Length
  - Bits 12-15 => Hop Count
  - Bits 8-11 => Header Length
  - Bits 0-7 => Packet Length
- (2) Source ID
- (3) Destination ID
- (4) Sequence Number, SPP TX Count
  - Bits 3-15 => Sequence Number
  - Bits 0-2 => SPP TX Count
- (5) Flags
  - Bits 13-15 => TYPE field
  - Bit 12 => ACK bit
  - Bit 11 => INV bit
  - Bits 8-10 => FUNCTION field
  - Bit 7 => ART bit
  - Bit 6 => ARQ bit
  - Bit 5 => ARP bit
  - Bit 4 => ACT bit
  - Bit 0-3 => Hop Pointer
- (6) RSUP, TXCNT2, TXCNT1
  - Bits 11-15 => Unused
  - Bit 10 => RSUP bit
  - Bits 5-9 => TXCNT2 field
  - Bits 0-4 => TXCNT1 field
- (7) - (14) Route ID words  
[Bit 15 is the most significant bit in the word.]

FIGURE 26 PACKET HEADER FORMAT

**SOURCE ID** Sixteen bit field to define the originator of the packet. The ID may define a PR or a process in an attached device. The source ID may define the destination of an end-to-end acknowledgement packet.

**DESTINATION ID** Sixteen bit field to define the final destination of a packet. The ID may define a PR or a process in an attached device. End-to-end acknowledgement packets are forwarded from the destination ID to the source ID of a packet. The ID number assigned to a device is defined by the device's function in the network.

0000	ID not defined
0001 to 0FFF	PRN Stations
1000 to 7FFF	PRN Terminals
8000 to AFFF	PRN Packet Radios
B000 to FFFF	Invalid ID

**PACKET SEQUENCE NO.** Thirteen bit field (bits 3-15 of word 4) utilized to sequence packets in the network. The sequence number is defined by the device originating the packet and is used to uniquely identify packets in a stream of packets from the same source/destination pair.

**SPP TRANSMIT COUNT** Three-bit field (bits 0-2 of word 4) utilized to uniquely identify SPP retransmissions of a packet. This field represents the number of SPP transmissions of a packet.

**TYPE** Three-bit (bits 13-15) field used to define the packet type as follows:

000	- Local Repeater on Packet
001	- Label Packet
010	- Undefined
011	- Information Packet
100	- Command Data Packet
101	- Command Packet

	110 - Performance Data Packet
	111 - Undefined
ACK	One-bit flag (bit 12 of word 5) indicating the packet is an end-to-end acknowledgement of a previous packet.
ROUTE INVERT	One bit flag (bit 11 of word 5) indicating whether the order of route IDs in the packet header should be reversed. When this bit is zero, the route is inverted. When this bit is one, the route is not changed.
FUNCTION	Three-bit field (bits 8-10) used to define the packet SPP protocol function as:  000-011 - Undefined  100 - Normal Connection  101 - Open Connection  110 - Close Connection  111 - Open/Close Connection
ART	One-bit (bit 7 of word 5) flag set to one by a PR to indicate the departure of a packet from the route originally contained in the packet header.
ARQ	One-bit flag (bit 6 of word 5) set by device originating the packet to request an end-to-end acknowledgement from the destination device.
ARP	One-bit flag (bit 5 of word 5) set to indicate the packet is being alternately routed. When set, any PR hearing the packet will decide whether it can help the packet along its route. ARP is cleared by any PR receiving the packet.
ACT	One-bit flag (bit 4 of word 5) set to indicate the packet is an active acknowledge.
HOP POINTER	Four-bit field (bits 0-3 of word 5) that defines to which ID in the route the packet is addressed. For example, if the hop pointer equal 3, the packet is addressed to the PR whose ID is third in the route:
TXCNT1, TXCNT2	Two five bit fields (bits 0-4 and 5-9 of word 6) used by the Cum Stats routines. TXCNT1 contains the total number of times the packet has been transmitted by CAP. Upon reception, TXCNT1 is

	shifted left five bits to fill the TXCNT2 field and TXCNT1 is zeroed.
RSUP	One-bit flag (bit 10 of word 6) to indicate to the station whether the normal PTP route assignment action should be suppressed. If a packet is forwarded via the station and the RSUP bit is not set, the station will forward the packet to the destination and then attempt to assign a PTP route to the originating PR. If, however, the RSUP bit is set, the station will forward the packet and take no further action.
PACKET ROUTE	Five 16-bit words which contain the IDs utilized in packet routing. One ID is required to define each PR along the route. The end of the route is delimited by exhaustion of the five ID positions or inclusion of an end-of-route (FFFF) ID.

## 6.2 User Definition of Packet Header

A user desiring to inject a packet into the Packet Radio network via a PR 1822 interface must specify the following packet header fields:

- . Header length
- . Packet length
- . Source ID
- . Destination ID
- . Sequence Number
- . SPP TX count (optional)
- . TYPE field
- . ACK bit
- . FUNCTION field

The sequence number is necessary for duplicate filtering in the network to function properly. If an end-to-end protocol is used with retransmissions, the SPP TX count field should contain the retransmission count.

A user may define all fields of the packet route or request the PR to specify the packet route. If the first route ID is non-zero, the

route and the route suppression bit (RSUP) are assumed to have been defined by the user. A simple test for the route validity is made by verifying that the route ID indicated by the hop pointer equals the PR's ID. If the route is not valid, the route table is searched for the source/destination ID pair.

If the user receives a packet from the PR and wishes to return the packet along the same route, the user need only clear the route inversion bit (INV). This will cause the PR to reverse the order of the IDs in the packet and set the hop pointer to one.

If the first route ID equals zero, the PR will insert a route in accordance with the second packet header route word. If the second route ID is all binary ones ( $FFFF_{16}$ ), the route to the station is inserted into the packet. The route suppression bit (RSUP) is assumed to have been defined by the user.

If the second route ID is other than FFFF, the route table is searched for the packet's source/destination ID pair and the route suppression bit in the header is cleared. If the ID pair is found and the route is defined, the route is inserted into the packet. If the ID pair is found but the route is not defined, the packet is routed to the station. If no route table entry is found with the packet's ID pair, the packet's source/destination IDs are written into an empty table entry (if one exists), the entry route is marked as "undefined", and the packet is routed to the station. If no empty entries are found, the table is searched for an entry which has not been used in 30 seconds. If an old entry is found, the entry is reused for the new ID pair, the entry's route is marked as "undefined", and the packet is sent to the station. If no old entry is found, the route suppression bit is set in the packet header and the packet is sent to the station.

If the PR receives a packet from the user with a ROP packet type (000) and the source undefined, the PR will insert the station ID in the packet's destination ID, the PR's ID in the packet's source ID, and route the packet to the station.

Whenever the PR inserts a route into a packet, the INV bit is set and the hop pointer set to one.

## 7 MAINTENANCE

### 7.1 Hardware Maintenance

Described below are the recommended maintenance procedures for user personnel. Repair service by the user should not be attempted under any circumstances not approved in advance by Rockwell/Collins. If the user should discover any problems or faults in the operation of the PR, he should contact Rockwell/Collins at the address given in Section 1.

Maintenance of the IPR by the user should be limited to checking power supply voltages, fuses, and the hardware straps.

The module on the extreme left in Figure 12 is the frequency synthesizer. The abbreviation OOL can be seen on the handle. These letters stand for the synthesizer being "out of lock". This refers to the LED indicator located just left of the OOL and visible through the module shield. Each time the microprocessor is loaded, the synthesizer OOL light should be out or very dim. If it is a bright red, the synthesizer is out of lock and the program should be reloaded.

### 7.2 Diagnostic Software

The IPR is supplied with a set of five diagnostics programs. These programs are designed to reveal hardware faults in the IPR. The names and functions of these diagnostics are listed below. For more details about these programs, the user should reference the documentation for each individual program.

Complete analysis of the error messages provided by these diagnostic programs should not be attempted by the user. However, all of the programs provide very unambiguous messages when no errors are found. Rockwell/Collins should be notified if any of these diagnostic programs indicate anything less than perfect operation.



### 7.2.1 CPUDG1 (CPU diagnostic)

The CPU diagnostics program exercises each of the IPR's two TI9900 CPUs to verify the performance of all CPU hardware functions. The diagnostic runs in one operator-selected CPU at a time and performs 56 distinct tests on the CPU chip.

### 7.2.2 RAMD (RAM memory diagnostic)

The RAM diagnostic performs a comprehensive test of the IPR's RAM. The RAM diagnostic can test a single block of contiguous RAM memory or all of the RAM memory implemented in a single CPU IPR. Because some of the system memory is only accessible by a single CPU, the RAM diagnostic should be executed in both CPUs to assure all memory in the system has been tested.

### 7.2.3 HSRSD1 (Straps/restart diagnostic)

The IPR straps/restart diagnostic is used for the off-line testing of the IPR hardware straps (auto-restart, down-line load, default frequency, IPR ID) and testing of IPR auto-restart due to software trap, watchdog timer, and power failure.

### 7.2.4 DMADG2 (DMA I/O diagnostic)

The DMA diagnostic provides the diagnostic testing of the IPR's DMA channels and interfaces. It is designed for testing in various turnaround modes in a single IPR and for testing between IPR's or other systems for specific test configurations. The DMA diagnostic also contains a subprogram which causes and verifies errors in the DMA's hardware status registers.

### 7.2.5 LNKTS4 (Link test support program)

The link test program implements packet transfer between selected IPR DMA channel interfaces to support testing of the IPR in various test configurations. While this program is normally used in conjunction with the DMA I/O diagnostic in another IPR, the link test

program can be used in a network monitoring mode in which packets received over the radio interface are automatically passed to a recording device over the 1822 interface.

#### 7.2.6 MSCD (Miscellaneous function diagnostic)

The MSCD diagnostic provides the diagnostic testing of the IPR digital units's miscellaneous functions. These functions include the watchdog timer, bus time-out recognition, illegal op-code recognition, CPU-directed interrupts, interval timer, and the elapsed timer.

Appendix  
PERFORMANCE SUMMARY

Appendix  
PERFORMANCE SUMMARY

Frequency Band	50-MHz bandwidth, tunable in 1710 to 1850 MHz band
Frequency Channel Spacing	20 steps of 6.4 MHz, 1712.3 to 1840.3 MHz
Transmitter Power Output	Minimum of 8 watts at antenna, software control of power down to -20 dB in four steps of 5 dB each
Transmitter Spurious Output	More than 50 dB below desired output in a 20 MHz bandwidth, not including modulation sidebands.
Antenna	Colinear array with 9 dBi gain
Modulation	Code (pseudonoise) spread spectrum
Chip Modulation	MSK (minimum shift keying)
Occupied Bandwidth	20 MHz for 99.5% of transmitter energy
Bit Modulation	Differentially coherent
Chip Rate	12.8 megachip per second (Mcps)
Bit Rates (Dual)	100 Kbps at 128 chip spread factor 400 Kbps at 32 chip spread factor
Receiver Processing Gain	+21 dB at 100 Kbps +15 dB at 400 Kbps
Receiver Signal Level	-99 dBm to -20 dBm at 100 Kbps -93 dBm to -20 dBm at 400 Kbps
Noise Figure	< 8 dB
Receiver Noise Bandwidth	20 MHz determined by IF filter
Interference Levels	In-band interferers (+10 MHz of carrier): < 10 dB above signal provided that level is in linear range of receiver
Transmit/Receive filter	4 pole Chebyshev filter, BW = 50 MHz, mechanically tunable over 1710 to 1850 MHz band
Image rejection	> 80 dB
Doppler sensitivity	Negligible effect up to platform speeds of Mach 1

Range at 100 KBPS	2 miles for 50% packet detection in a dense urban environment with a 6' and a 50' antenna. 22 miles for rural environment. 32 miles for LOS radio horizon. 600 miles for LOS airborne.
BER Performance	$\leq 10^{-5}$
Preamble	Total length = 48 bits. A 9-bit inverted Barker code followed by two 13-bit inverted Barker codes and one non-inverted 13-bit Barker code.
Preamble Detection	Probability of Detection = 0.999 Probability of false alarm = $10^{-6}$
Microprocessor	TI 9900 with 3 Mhz clock
RAM	12K 16-bit words with 1 parity bit per word
PROM	4K 16-bit words with 1 parity bit per word