SEP 15 1982

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INTEROFFICE MEMO

To: Gordon Bell

CC: Bill Demmer

Date: 9 September 1982
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 247-2990
Loc/Mail Stop: TWO/B02

Subject: IMPROVING THE SCORPIO SYSTEMS PERFORMANCE

With Nautilus moving to a much higher performance (and cost) class machine, the Scorpio systems will need to cover a much bigger hole between the low-end VAX systems and (through the mid-range performance space) the high-end VAX systems. Bob Willard, our Scorpio systems architect, has prepared a proposal with a number of systems implementation alternatives which (via multiprocessing and some other hardware techniques) could cover the performance space.

I thought you might like to review our current thinking along these lines. If you have any comments, please respond to me or Bob directly. We would like to have your opinion.

DL:clc

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MAIL #238

From: OBLIO::WILLARD 10-AUG-1982 23:07
To: OBLIO::LIGNOS
Subj: Stretched Scorpio Systems

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* D I G I T A L * INTEROFFICE MEMORANDUM

To: Demetrios Lignos, Mike Titelbaum

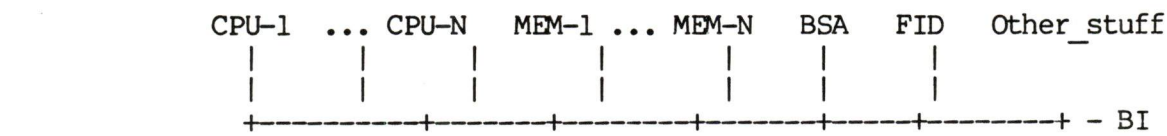
cc: Dileep Bhandarkar, Frank Bomba, Bob Chen, Brian Hannon, Ann Katan, Ken Mamayek, Ernie Preisig, Tom Sherman, Jim Stegeman, Bill Strecker

Date: 82-Aug-10

From: Bob Willard, SCORPIO Engineering, 247-2823, TWO/B02, OBLIO::WILLARD

Subj: Stretched Scorpio Systems

It has been pointed out that the throughput of the BI is finite. Recently, a small company in a semi-foreign country (Texas, I think it was), expressed their desire for some increased capacity. To pick that situation, since it is typical of what we will hear from other bandwidth freaks, they have the following:



The CPUs are all KDZs running VMSmp or SEAmp, and the MEMs are Scorpio memories. The BSA is an interface to high-end disks; it might be a few BUA-UDA pairs at FRS. The FID is a Fast Interface Device, such as a DR32. The Other_stuff represents the usual collection of sync/async comm.gear, which is assumed to be low bandwidth.

The problem occurs when a long burst of data arrives from the FID, which must be swallowed intact (that's what they are paying for). Assuming 2 MB/sec for 15 seconds, a Scorpio cannot bear enough memory to simply buffer the burst. The BI bandwidth needed is 2 MB/sec for FID-to-MEM, plus 2 MB/sec for MEM-to-BSA to dispose of the FID-sourced data, plus 2 MB/sec per CPU to keep VMS/SEA running, plus a minor contribution from the Other_stuff and some additional disk traffic stirred up by VMS/SEA.

With optimal (octaword) transfers only, and with no re-tries, and ignoring the effects of Other_stuff/NI/VMS disk_traffic, BI will nearly saturate with 3 CPUs. When second-order effects are considered, including longword writes from the CPU and interrupt traffic, we are pinched.

It is tempting to believe that using Hi/Lo BI priorities, instead of the preferred round-robin scheme, will solve this problem. This is a dangerous fallacy. Presumably, one would make the FID and the BSA run at Hi-pri, and make the CPUs run at Lo-pri (I am ignoring the Other_stuff). Hi/Lo priority schemes help for short bursts (where large memory buffers totally solve the problem), but for long bursts the CPU(s) must be involved to manage the FID-MEM and MEM-BSA transfers (something must do the QIOs). Round-robin is required to make it work, although the Other_stuff and the attached CPUs could be given Lo-pri in this particular application.

Possible solutions to this problem:

1. El Cheapo: when the system senses that a burst is happening, turn off the unnecessary stuff for a while. Sensing is usually not difficult: in most cases, these data acquisition bursts are pre-scheduled or initiated by a program; in other cases, the FID may give a "warning shot" to announce that data is coming (in droves); finally, the first QIO completion interrupt from the FID is sufficient warning that a burst has just started. Turning off the Other stuff is easy: don't issue any more QIOs for a while; the more radical step, of cancelling outstanding QIOs, will usually not be needed but could be done. More important, the primary processor can tell the attached processors to pause (execute a null process) for a while: running a null process, on a cached CPU, drops its memory access rate from 2 MB/sec to zero; a rather dramatic difference.

The El Cheapo solution sounds a bit hokey. However, it is simple to implement in many common applications, and it does not require any new hardware.

2. El Expensivo: call it the KDZ-11/23B or something. Subsequent to the KDZ, it will be possible to build a KDZ which has at least as much power as the KDZ, and uses less BI bandwidth. Although this is all futures, let me count the ways:

a. Bigger and better cache: going from 8 KB to 16 or 32 KB will do little, based on 780 measurements. Replacing the current direct mapped structure with a set-associative architecture would probably do more. The 780 is two-way set-associative; four-way would do more. The biggest step in reducing the BI bandwidth would be a write-back cache, as in Nautilus.

b. Bigger TB: the 780 TB (2x64) causes threshing in VMS, and Scorpio (2x32) is even smaller. While the story with Seaboard is unknown, going to a 2x256 TB would clearly help VMS run faster which, indirectly, means less BI bandwidth needed for the same function.

c. WCS: currently, Scorpio has no Writeable Control Store option. Since we have on-board II (for the NI), we have a home for WCS. While WCS is not a panacea, it can be of great help for special applications, such as some of the bandwidth freaks desire.

d. On-board ROM: like WCS, but intended as a home for macro- instead of micro-code.

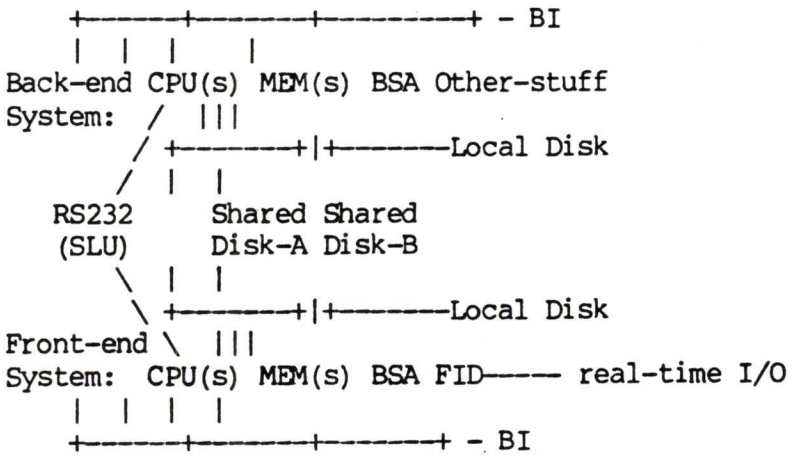
There are several other things that could be done to augment the KDZ's successor, but none of these are really relevant to the current time frame.

Having disposed of the available solution (1), and the unattainable (for now) solution (2), let us consider what can be done with a little more hardware.

All of these solutions are based on loosely-coupled multi-processor structures, since the tightly-coupled solutions (all CPUs and all memory of the same BI) will all leave BI as the bottleneck, albeit a rather wide bottleneck.

All of these solutions will be discussed in terms of a front-end data acquisition system, coupled to a back-end data crunching system. In some cases, this could be generalized to N front-ends coupled to M back-ends using (more of) the same hardware; however, the most prevalent case will be a single front-end and a single back-end.

3. Shared disks: VMS supports, and Seaboard may support, shared disk structures, such as:



The reason for two shared disks is to permit the front-end system to manage FID-to-disk on one disk, while the back-end system does data reduction on the other shared disk (typically based on the data received by the front-end system during the last burst). Depending on the FID traffic (burst-length and inter-burst time), one shared disk may suffice.

The reason for the RS232 link between the front-end and the back-end is to synchronize disk-sharing between the two coupled systems. This could also be done via the NI ports.

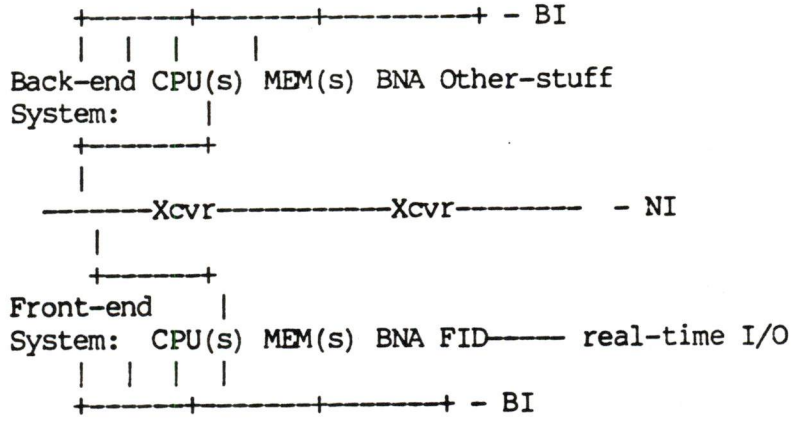
This is a common structure for on-line applications (such as airline reservation systems), but not for real-time systems. Disadvantages of this structure in real-time systems include:

a. The high cost of BSA-class disks, and the high space-cost of the footprint.

b. The environmental restrictions of disks -- temperature, humidity, dirt and chemicals, and vibration. Winchester technology helps, but does not entirely solve the problem.

c. Time lag in the data stream, as seen by the back-end system. This can be solved in some cases (under VMS, at least), by letting the back-end read the shared disk while the front-end is writing to it, but synchronization problems are tough. The time to swap disks (0.1-1.0 seconds) will eliminate this approach for some applications.

4. NI/DECnet: VMS supports, and Seaboard will also support:



The KDZ's on-board NI port could be used in some cases, but in cases where heavy traffic is anticipated between the front-end and the back-end, the BNA is a better match.

The NI/DECnet approach has a number of advantages, including:

a. The capability to connect N front-ends to M back-ends.

b. Reasonably large area coverage.

c. Low-cost, low-throughput alternative: the on-board NI port.

d. Easy support and debug for Seaboard.

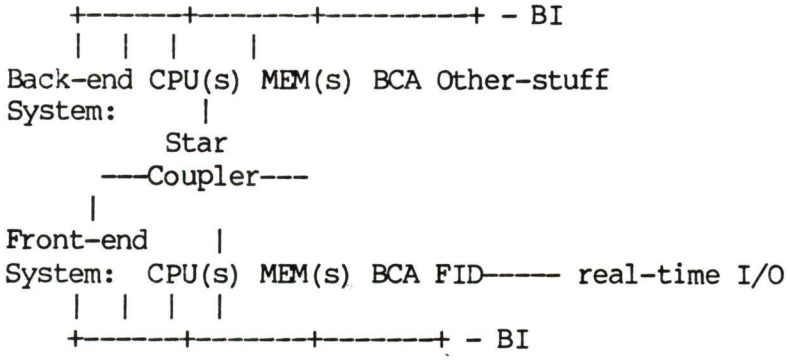
Since the hardware and the software will exist, this structure is appealing until the real-time parameters are included:

a. To a user who feels constrained by the 10+ MB/sec BI, adding a 100 KB/sec link between the front-end and the back-end will not be perceived as credible. NI/DECnet throughput is a severe bottleneck in these cases.

b. The message transit times for NI are large and, of importance to real-time folks, non-deterministic.

NI is terrific in its own space, but as a high-capacity link between a front-end and a back-end, it will rarely suffice. Not the answer for high-end systems which exceed the bandwidth of a single BI.

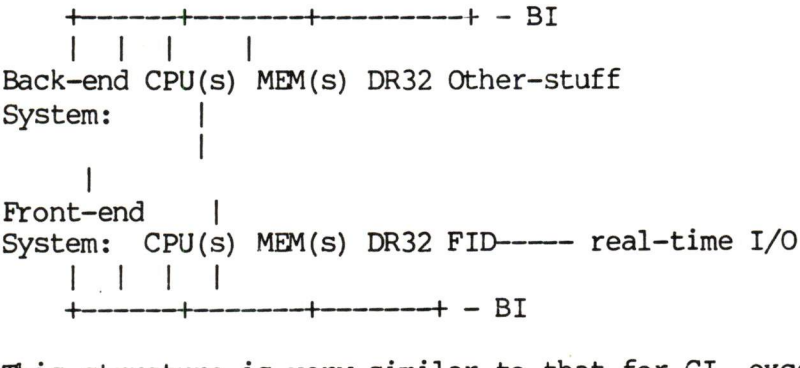
5. VAX clusters: VMS supports, and Seaboard may support:



This structure is very similar to that for NI/DECnet, except that the throughput offered at the port driver level is roughly 2 MB/sec, instead of the 100 KB/sec offered by NI/DECnet. A mono-CPU (or, perhaps, a 2-CPU) front-end could swallow 2 MB/sec from the FID, copy the FID-data to local BSA-disk, and copy the FID-data stream to the back-end over CI without swamping the BI.

As long as the user will accept a message-oriented interface between the front-end and the back-end, CI is a strong contender. Further, it (like NI) supports multiple front-ends connected to multiple back-ends. Since HSCs may be connected to CI, high-end disk needs may also be satisfied via the BCAs. CI is redundant and, therefore, rather reliable: a genuine plus.

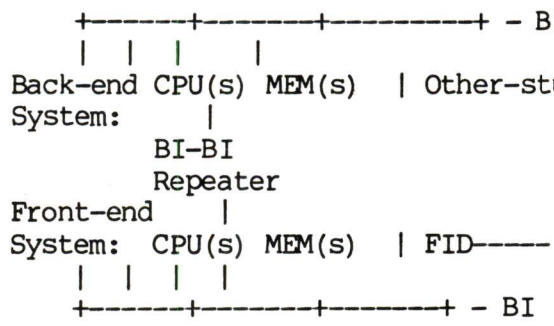
6. DR32: VMS supports, and Seaboard may support:



This structure is very similar to that for CI, except that the DR32 is point-to-point and non-redundant. The DR32 interconnect is slightly faster than CI.

The DR32 is very appealing in cases where the FID is, itself, a DR32: it is far easier to manage and program two identical devices, than to cope with two different devices.

7. The BI-BI repeater:

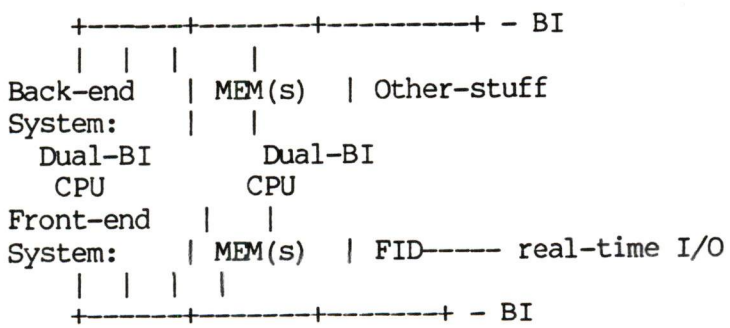


The repeater must understand, via something akin to mapping registers, the configuration of both BIs. When a transaction is addressed to the repeater, it must be remapped into a transaction onto the other BI.

Physically, this could be a single double-height card, which is connected to a top BI and a bottom BI, or it could be a pair of cards with an interconnecting cable.

Since the BI node address field is not extensible, I suspect that any such repeater will be a kludge, offering only long debug time and long access times. Yuck. Sorry I mentioned it.

8. A CPU with two BIs:



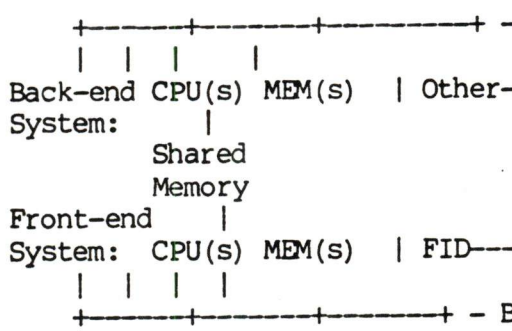
The CPUs must understand, via something akin to mapping registers, the configuration of both BIs. When a read/write is directed to physical memory or to I/O space, the CPU (in its port controller or equivalent) must steer the read/write to the correct BI.

Physically, this could be a single double-height card, which is connected to a top BI and a bottom BI, or it could be a pair of cards with an interconnecting cable.

Functionally, this can be done. Minor surgery may be necessary to the BI architectural documents, but there is no apparent impact on existing designs to allow two BIs on a CPU.

This effort goes wildly beyond the current scope of the present Scorpio project; however, I can't think of anything we are doing today which precludes a dual-BI CPU, and I don't think there is anything we should be doing differently to retain this possibility for the future.

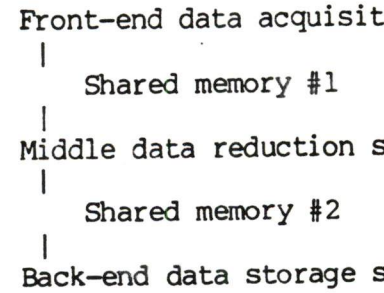
9. Shared multi-port memory: on the 780, VMS supports:



VMS support for shared memory includes: common event flags (an inter-process interrupt mechanism), mailboxes (an inter-process message delivery mechanism), and global sections (an inter-process shared database).

Shared memory is clearly the fastest interconnect between a front-end and a back-end system, both in throughput (10+ MB/sec) and transit time (pleasantly close to zero).

Shared memory may also be used recursively, such as:



In addition to memory, any shared memory system must support inter-system interrupt and inter-system cache invalidates.

Shared memory must also respond rationally when one system is running, and another system executes self-test.

For high-end real-time Scorpio applications, when the bandwidth of a single BI system is exceeded, shared multi-port memory is the fastest and most flexible interconnect between a front-end and a back-end.

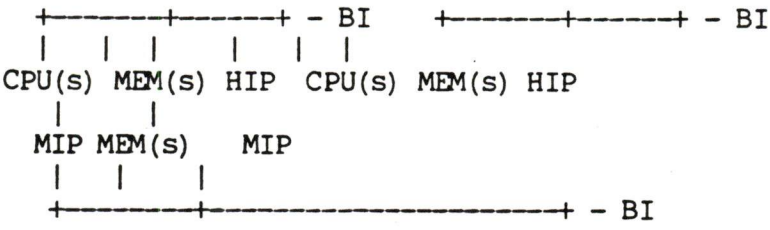
Shared multi-port memory could be implemented as:

a. A double-height Eurocard, which is connected to a top BI and a bottom BI. This does restrict the multi-port memory to two ports; however, of the >100 MA780s shipped, only three customers have used more than two ports.

Based on 256 Kb chips, a 2 MB memory should easily fit on a double-height Eurocard, including all the additional control logic for port contention, inter-system cache invalidates, and inter-system interrupt.

This is the minimum cost approach.

b. For each system, one Host Interface Port (HIP) and one Memory Interface Port (MIP) gives access to up to 28 MB of shared memory:



The MEMs which constitute shared memory are identical to the MEMs which are local memory. One of the lessons learned (one hopes) from the MA780 is that memory technology advances in local memory should be easily translated into equivalent upgrades to shared memory.

It should be easy to fit either HIP or MIP onto a Eurocard, and the I/O pinning is generous (perhaps a MIP could connect to two HIPs). The MIP must be capable of generating the BI clock (optional), and the usual self-test issues must be addressed.

This arrangement allows up to a dozen systems to share the same memory.

This is not a low-cost configuration, but in the high-end Scorpio business, the capability is far more important than the cost.

Given current budget/manpower/etc. constraints, the addition of new Scorpio sub-projects is irrational. However, we should ensure that none of the techniques for stretching Scorpio systems listed above is precluded by our current focus on the low end of the business. There is a need for high-end capabilities in the Scorpio space, and most of the structures defined in this memo will be requested/demanded in the future.

To summarize what must be done in the present to make the future possible, structure-by-structure:

1. El Cheapo (a/k/a program around it) is the current strategy. This requires nothing new from the Scorpio team, and it is up to the product line folks to point out this approach to customers.

2. El Expensivo (super-KDZ) is compatible with our current direction. If and when the super-KDZ exists, it replaces the standard KDZ. We should, perhaps, re-examine the BI architecture to ensure that the hooks are there for write-back caches; all else is fine.

3. Shared disks should not represent anything new for Scorpio. As long as VMS supports them through the BSA, we have no new work. If the product lines also want Seaboard to support shared disks, it is just one more Seaboard enhancement.

4. NI/DECnet support for the on-board NI is in the works, and Nautilus is planning for the BNA. No new work for us.

5. VAX clusters are supported under VMS. All we need is the BCA, which takes time and money. No architectural impact, however, aside from the BCA-unique effort. There is a need to get support (documentation) for the port-driver interface, to achieve high throughput. It would be nice if the Nautilus troops would do a BCA, instead of a NCA, to avoid redundant engineering effort.

6. DR32 does offer a potential opportunity: if the parallel I/O port on the multi-function module could become DR32 compatible, this module could solve three problems for the price of one design: the TVG fast parallel port to foreign devices, the LDP DR32 port, and the Primitive Interconnect. In any event, the DR32 does not require any new architectural issues at the system level.

7. The BI-BI repeater is felt to be a kludge, and I hope that nobody suggests it seriously. Any arguments?

8. A CPU with two BIs does not seem to be in conflict with the BI architecture. The one architectural problem, of steering CPU transactions to the right BI, would seem to be an isolated problem in the architecture of that dual-BI CPU. Not trivial, but solvable.

9. Shared multi-port memory does present some architectural issues, which should be addressed now. It appears that the issues are the same for either of the two proposed structures: inter-system interrupt, inter-system cache invalidates, contention, test/self-test, and booting/sizing memory.

Since the detailed memory architecture for Scorpio is not complete, this is the opporture time to architect shared memory as well.

What are the consequences to the program?

Summary (think of it as a reward for reading the rest of this memo):

1. Scorpio is, in many applications, THE high-end VAX. With all due respect to Venus and Nautilus, and the 780, remember that:

   a. Scorpio is the high-end VAX in Class C environements without disk.

   b. Scorpio is the high-end VAX in Class B environments with disk.

   c. Scorpio is the high-end Seaboard VAX.

2. There are many possible ways to stretch the performance limits of Scorpio, most of which will be desired in the future.

3. We seem to be on track for all of these future extensions, except for shared multi-port memory.

4. We should exert the effort now to facilitate shared memory in our architecture.

Cheers, Bob

MAIL>

OT4.9

digital

INTEROFFICE MEMO

To: SSPO Members

CC: SSPO Alternates
Distribution

Date: 3 November 1982
From: Omur Tasar
Dept: Low End VAX Systems Dev
Ext.: 229-6119
Loc/Mail Stop: LTN1-2/F15

Subject: SSPO MINUTES--27 OCTOBER 1982

Attendees: Demetrios Lignos, Doug Hanzlik, Kevin Reilly, Duane Dickhut, Mike Titelbaum, Bill Schmidt, Tom Sherman, Herb Jacobs, Ken Meissner, Dave Hurlbut, Omur Tasar, Bill Johnson, Kaj Larsen, Bob Willard

Absent: Carl Blatchley

A. ADMINISTRATIVE ISSUES

The next SSPO meeting will be on 10 November 1982 from 3:00 to 5:00 p.m. in the Engineering Conference Room in Salem (SV). The meeting has been moved from 2:00 to 3:00 because of a conflict Ken Meissner has.

B. AGENDA

1. Preparations for the Program Review (Omur Tasar)

The next major program review has been scheduled for 30 November 1982. Omur distributed a tentative agenda for comments. She said that the review is intended to show our readiness for exiting Phase 1. The phase exit review meeting will be separately conducted by Tom Sherman.

It was decided that the dry run for the program review will happen on 24 November 1982 at the regularly scheduled SSPO meeting but the meeting will start at 1:00 instead of 2:00. Only Herb Jacobs will be on vacation that day and will send his overheads to Omur before the meeting.

2. VMS Schedule Alternatives for Scorpio (Herb Jacobs)

Herb reported that they generated four alternatives for VMS to support Scorpio. Briefly:

1. VMS support as desired by V3B schedule requires the Scorpio CPU to boot at the end of January 84. At this time, the console load device, processor and system disk should work; MP, BI adatpers, decimal and floating point functionalities are not necessary. In this scenario, Scorpio would need to be announced in April 84 along with 3B release.

Although this is the no risk alternative to VMS, it is very unlikely to happen because Scorpio in the January 84 timeframe will be debugging second pass V11 chips and they probably will not have enough functionality working to boot VMS.

2. VMS 3B latent support is the second alternative. This alternative requires that Scorpio boots before VMS is released to SDC, that is, before March 84 timeframe. If the "boot software" needs to change after 3B is released, Scorpio has to wait for the next release.

   For this alternative or the first alternative to work, the Scorpio system configuration has to be frozen by January 83. These are major system configuration definitions such as LESI being on Unibus or BI or console load device being RX50 or TU58. VMS will have dedicated resources on Scorpio in May 83 timeframe.

   There was an extensive discussion on VMS support for peripheral devices. Herb explained that NI, BSA for example can be supported as drivers in latent support but for booting off of one of these devices they had to be in a major release. Herb was skeptical of NI being in the 3B release as a boot device.

   This alternative would allow Scorpio FRS in February 85 with V3B support.

3. Remaster VMS for Scorpio was the third alternative to meet the February 85 schedule. But this is an undesireable solution since earlier versions of 3B would potentially not run Scorpio. For this, Scorpio has to boot before 1 July 1984. It was agreed that we would fall back to this alternative only if Alternative 2 was not achieved.

4. Alternative 4 was Scorpio being supported by the next release of VMS which is Version 4. But from the VMS standpoint, it is unrealistic to schedule another release in less than 18 months. This brings V4 release to October 85 which is too late for the current Scorpio schedule.

It was agreed unanimously to go with Alternative 2, but give Alternative 1 a chance just in case the V11 first pass chips come out with enough functionality. Engineering agreed to freeze system configuration by the end of January 83. This involves making or not making a commitment for native BI adapters to be available at system FRS time.

A suggestion was made to look into debugging some of the critical VMS boot code on the CPU microcode simulator. Herb will work with Dick Sites to understand if reasonable work can be accomplished on the simulator prior to having hardware available.

C. MAJOR PROGRAM HIGHLIGHTS

1. System Hardware Development (Mike Titelbaum)

A handshake agreement has been reached with Motorola for the development of the BI clock driver. The specifications have been agreed to and Motorola started the design. Tentative date for the contract to be signed with Motorola is the end of November.

The BIIC spec has been updated and distributed for review. The chip logic design is 99% complete. The circuit design is 75% complete, the layout is 55% complete. BI spec has been updated; it will be available for review on 8 Novemeber 1982.

The BUA breadboard plan is being accelerated 3 months from 7/83 to 4/83 to be used with the test system debug.

Mike has a need for at least one microcode and one system hardware design engineer.

2. CPU Development (Bill Johnson)

Bill said they closed on the toy clock getting out of the M-Chip. The toy clock functionality will be realized on the module. The module real estate is getting scarce. The DC-to-DC converter may have to go.

The DC412 which is one of the TAT020's on the CPU module is being designed. It is mostly entered into SUDS, some DECSIM modeling has started.

Microcode development has achieved a significant milestone. The first compatability mode instruction has worked.

The chip development team worked on debugging CHAS last week. In the next two weeks, they are expecting the bugs to be fixed. They are working on detailed plans for Q2. Weekly milestones are being set.

Work has started on the engineering tester. Mike suggested that tester functionality and CPU debug and verification plans be reviewed with Ann Katan and Dave Wells to understand the overlap if there is any between the CPU engineering tester and the system tester.

Discussion of NI and booting of off NI revealed that there is a potential resource issue of getting the NI boot code and macro code developed for Scorpio. Mike said Bob is working the technical issues to get agreement between the HL, VMS, Distributed Systems, and Seaboard teams. Once a technical solution is bought into, the implementation issues will be worked.

Bill said much closer work is underway with Manufacturing and that this interface is going smoothly.

The F-Chip resources are being searched for. Lackey and Walker are on the F-Chip. The plan is still to get the F-Chip out by Q4 FY85.

3. Memory Development (Dave Hurlbut)

The memory functional spec has been updated. The updated project plan is out for review and approval. The memory funding issue for FY'83 has been resolved by the Scorpio program's $200K contribution.

Memory is still planning for on-board self test, it will be implemented on one of the gate arrays. Bill and Mike suggested that if self test implementation becomes a gate count or schedule issue, it could be dropped later on since some self test can be accomplished from the CPU.

4. Power and Packaging Development (Bill Schmidt)

Bill announced that Scorpio macro-packaging will be managed by John Edfors. Charlie Barker who was responsible for that task has moved to work on the LCN program.

5. Manufacturing Status (Ken Meissner)

Ken is working on the plan for the dedicated resources in Manufacturing for the Scorpio program. When such resource needs are defined, they will go to Metzger and Thorpe to see if these resources can be found from Metzger's organization. The manufacturing plan is being worked on; it will be out on 15 November 1982. The plan will have first pass estimates of transfer costs. Ken will present the manufacturing plan at the next SSPO meeting.

6. TAT020 Status (Omur Tasar)

A very productive meeting took place in Houston between TI and DEC on the CAD process and how it could be optimized for our needs. We defined a flow with TI that will allow for submitting placement information to TI partially or totally. TI has been requested to give DEC access to their layout tools over Remote Job Entry (RJE) terminals. This request will be discussed at the high level management meeting between TI and DEC on 28 October 1982. Nevertheless, work is in progress to set up the RJE facility in LTN. TI reported very encouraging news on upgrading the TAT020 performance.

The 10K material resulted in 30% performance improvement over the current samples. TI decided to standardize the 10K material. All our chips including the test case (WOMBAT) will be done in 10K.

Development contract negotiations are in progress. The goal is to have a contract signed by the end of the calender year.

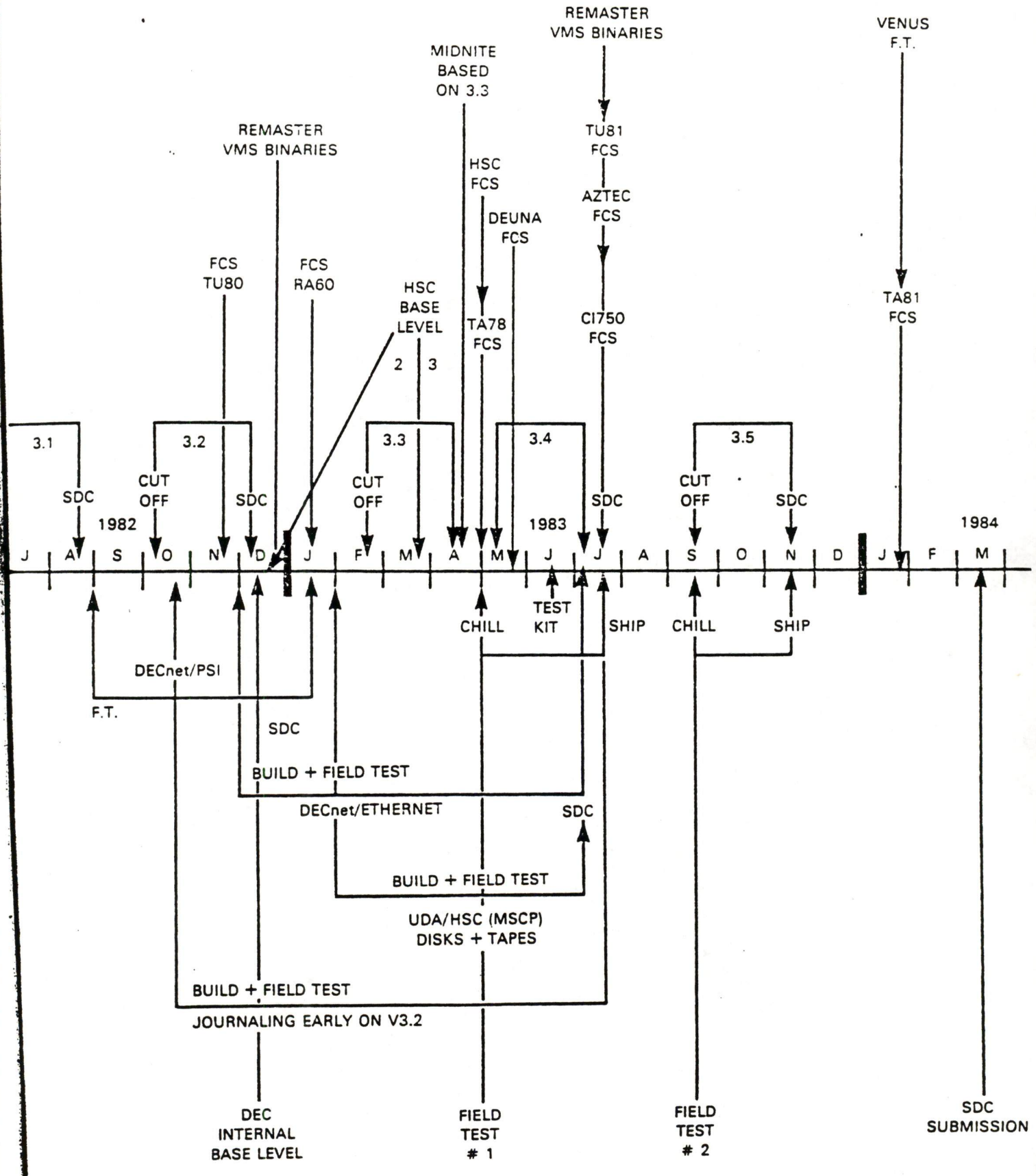
D. AGENDA FOR THE NEXT SSPO MEETING

- Review of the Manufacturing Plan (Ken Meissner)

See you on 10 November 1982 in the Engineering Conference Room, Salem (SV).

OT:clc
Attachment

VMS V3.0B SCHEDULE



10/82

SSPO MEMBERS

Carl Blatchley	MLO1-3/U6	223-3764	CACHE::BLATCHLEY
Duane Dickhut	HLO1-1/S11	225-4941	CHIPS::DICKHUT
Ron Given	MLO21-2/E64	223-6139	
Doug Hanzlik	TWO/A02	247-2515	SUPER::HANZLIK
Herb Jacobs	ZKO1-1/D42	264-8451	STAR::JACOBS
Kaj Larsen	HLO2-1/E10	225-5409	OBLIO::LARSEN
Demetrios Lignos	LTN1-2/F15	229-6116	OBLIO::LIGNOS
Ken Meissner	SVO	261-3215	OBLIO::MEISSNER
Kevin Reilly	LTN1-2/F15	229-6072	OBLIO::REILLY
Bill Schmidt	LTN1-2/F15	229-6118	OBLIO::SCHMIDT
Tom Sherman	LTN1-2/F15	229-6117	OBLIO::SHERMAN
Omur Tasar	LTN1-2/F15	229-6119	OBLIO::TASAR
Mike Titelbaum	LTN1-2/F15	229-6120	OBLIO::TITELBAUM
Bob Willard	LTN1-2/F15	229-6139	OBLIO::WILLARD

Alternates

Clark D'Elia	ZKO1-1/D42	264-8615	DELPHI::DELIA
John Forde	MLO3-6/E94	223-3516	CACHE::FORDE
Ted Gent	TWO/A02	247-2531	SUPER::GENT
Dave Hurlbut	MLO21-4/E10	223-5349	ZEUS::HURLBUT
Bill Johnson	HLO1-1/S11	225-4961	CHIPS::JOHNSON
Jim McWilliams	SVO	261-3239	OBLIO::MCWILLIAMS
Nelson Velez	LTN1-2/F15	229-6137	OBLIO::VELEZ

For Information Only

Peter Barck	LTN1-2/F15
Gordon Bell	MLO12-1/A51
Joel Berman	TWO/A02
Dileep Bhandarkar	LTN1-2/H07
Corinne Chumsae	LTN1-2/F15
Larry Coppenrath	ZSO
Bill Demmer	LTN1-2/G09
Bud Dill	SVO
Ian Evans	HLO2-1/A10
Dan Haley	MLO21-2/E64
Brian Hannon	LTN1-2/F15
Marv Horovitz	SVO
Peter Jessel	LTN1-2/H04
Ann Katan	LTN1-2/F15
Bob Kugler	SVO
George Plowman	SVO
Ernie Preisig	LTN1-2/F20
Sharon Sambursky	SVO
Linda Sarles	HLO2-1/C10
Chris Shatara	LJO
Bill Strecker	LTN1-2/H07
Lou Tancredi	APO-2/C4
Steve Teicher	HLO2-2/N07

Please contact Cindy Cue, Ext. 229-6115, for changes to this list.

WPS USERS - Enter HP mode and then type <CR>

****
* d i g i t a l *
****

TO: see "TO" DISTRIBUTION

DATE: FRI 15 JAN 1982 2:12 PM EST
FROM: BILL DEMMER
DEPT: 32 BIT SYSTEMS
EXT: 247-2112
LOC/MAIL STOP: TW/D19

SUBJECT: THE LOW-END VAX STRATEGY AND THE BI

There still appears to be considerable confusion surrounding the direction of the Low-end 32 Bit Strategy and the BI Bus. Therefore, I will try to reconstruct the thinking behind the changes we are postulating.

The top half of Figure I shows the Scorpio configuration based upon the BI as defined during the past year, as well as indicating the set of new technologies being employed. This design had the attribute of meeting the original Scorpio design goal of being utilized in both Board and System applications.

However, the risks associated with the new technologies coupled with the high development cost of all new adapters suggested a re-examination of the design approach. Given this importance of the Systems market we decided to focus on it first and found that we could structure a systems design that meets almost all of our goals as can be seen in the bottom half of Figure I. The V11 chip set is the only new technology required to support this approach. Having the BI available will also help the Tech OEM interface need, but is not required to have an acceptable System product. Since the BI is no longer planned to be used as a memory bus we are investigating the possibility of simplifying its design and increasing its bandwidth. I am hopeful that we can then use the BI for the Board Market in a manner that gives Digital a leadership bus product. It will also serve as the interface bus on the Nautilus yielding a common interface for these two systems for customer I/O and obviating the need for further DR type products. The BI can also be used within system structures as the need for its bandwidth or other functionality attributes arises.

To address the Board Market with a competitive product where all the functionality provided by the full VAX instruction set is not required, it is believed that a relative high performing single chip coupled with microcode and software can be obtained from an outside supplier in a reasonable timeframe (2 years?). However, to get a top semiconductor supplier interested we anticipate they will insist on being able to market the chip on the open market. This opens up a new set of opportunities and a new set of problems. The latter has several forms, but the one I fear the most is the emergence of plug compatible systems hardware which might erode our total Systems business by a significant amount (20%?). However, this can possibly be offset by the opportunity of getting the world's 32 Bit Microprocessor standard around this VAX subset, which in turn could broaden the entire market for VAX

products, more than off setting our loss to PCMs (particularly if we raise the software prices!) We are assuming that this fundamental business question will be worked in parallel with the technical program to define such Micro-VAX chip.

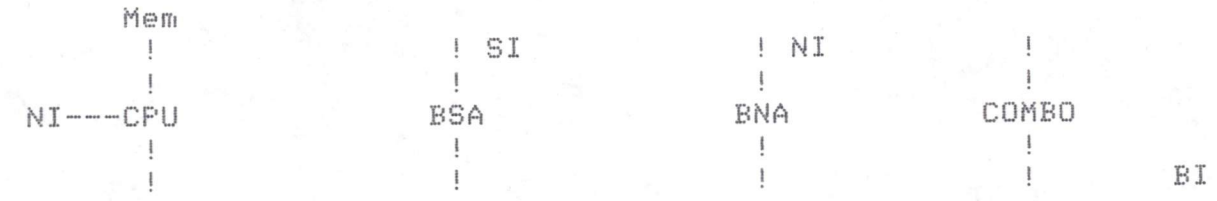
With the initial focus of Scorpio at the systems level, I would expect to initially focus the Micro-VAX product at the board level, where given the constraint of a single chip the priority is on performance over functionality. (See Figure 2). Over time I expect the applications of Scorpio and Micro-VAX to begin to overlap with Micro-VAX moving into in-house controllers and Scorpio into those Workstations where the functionality is required. It is also possible that Scorpio could serve the High End Board market with the BI bus.

Some of the specifics of the above are still evolving, particularly setting agreement with Micros on the Board Strategy. As I will be away next week, questions on Scorpio can be addressed to Demetrios Lismos and those on Micro-VAX to Brian Croxon who should be able to directly clarify things or identify the person who can.

/VJT
3.27

THE BI

SCORPIO - 1981



V11 CHIP SET	NEW MODULE	PLUS POTENTIALLY:
TAT 20 GATE ARRAY	NEW CONNECTOR	UNIBUS ADAPTER
BI CHIP	NEW PWR/PKG	CI ADAPTER

SCORPIO - 1982

V11 CHIP SET

EXISTING OR ORION PKG.

BI GOALS	BI APPLICATIONS
I/O BUS (NOT A MEMORY BUS)	TECH OEM INTERFACE
HIGHER BANDWIDTH	BOARD PRODUCT BUS
SIMPLER DESIGN	FUTURE SYSTEMS BUS

FIGURE I

LOW-END 32 BIT FOCUS

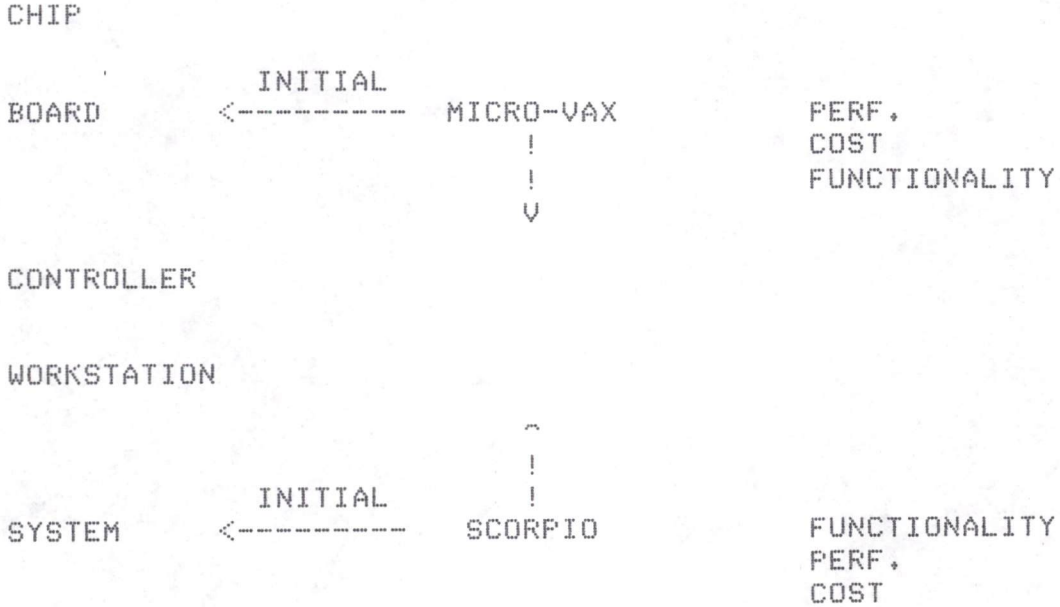


FIGURE 2

"TO" DISTRIBUTION:

JIM CUDMORE	LLOYD FUGATE	SAM FULLER
GVPC:	JEFF KALB	JACK MACKEEN
ROY MOFFA	PEG:	STEVE TEICHER
THIRTY TWO BIT PT:	LARRY WADE	

****
* d i g i t a l *
****

TO: see "TO" DISTRIBUTION

DATE: MON 11 JAN 1982 3:05 PM EST
FROM: DEMETRIOS LIGNOS
DEPT: LOW END VAX SYS DEV
EXT: 247-2990
LOC/MAIL STOP: TW/B02

SUBJECT: DECISION TO DECOUPLE THE BI BUS FROM THE FIRST

Subject: Decision to Decouple the BI Bus From the First Scorpio System FCS

We have decided to modify our I/O bus plans for the Low-End 32-Bit Scorpio VAX System. Our new strategy calls for a Unibus based Scorpio system to be our first entry into the market place. The BI effort, as currently defined, will continue but not with the original intent of using the BIIC chip in our first product. Furthermore, we will look at opportunities to improve its functionality and performance while at the same time try to simplify the design and lower the cost. In addition to the BIIC planning modifications, the associated new BI interconnect micro-packaging (i.e., Euro-module, new connector, backpanel, etc.) will not be required at FCS. It would be desirable, however, to find a way to continue the new packaging project as an advanced development effort.

The basic reasons for making the BI delay decision at this time, are as follows:

1. Reduce the FY'83 development cost impact on the Engineering development budget.

2. Minimize the technical risks associated with the BIIC and the new micro-packaging from impacting our FRS dates (time-to-market issue).

3. Better understanding of the "new bus" performance and functional needs for the late 80's and 90's. The present thinking is the BI, as presently defined, may not be the right bus architecture for our next generation products.

The Scorpio System Development Group is proceeding with our development plan modifications to incorporate this strategic change. Please modify your plans to reflect the changes as well. Over the next two to three months (end of March time frame), we will publish a new BI (or modified BI) plan with revised availability dates for chip development activities.

I will be happy to answer any questions you might have on the BI issues (my extension is 247-2990).

263-870

DL:clc
DL3.19

"TO" DISTRIBUTION:

PHIL ARNOLD
DILEEP BHANDARKAR
TOM BURNIECE
BILL DEMMER
JOHN FORDE
DOUG HANZLIK
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BILL JOHNSON
BERNIE LACROUTE
MARK MENEZES
OMUR TASAR @TWSK
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TOM SHERMAN
MIKE TITELBAUM
WAYNE PARKER @HPLT

*GORDON BELL
CARL BLATCHLEY
CLARK D'ELIA @ZKXX
DUANE DICKHUT
FRANK BOMBA @TWSK
FRANK HASSETT
JIM MCWILLIAMS @SVXX
GEORGE KATRONGE
ART LIM
NELSON VELEZ @TWSK
NAT PARKE
GRANT SAVIERS
STEVE TEICHER
JIM WADE
WILLIAM JOHNSON @HPLT

JOEL BERMAN
BRIAN HANNON @TWSK
JIM CUDMORE
BUD DILL
TED GENT
BILL HEFFNER
JOE CHENAIL @BQIX
KEVIN REILLY @TWSK
DON MCINNIS
JOHN O'KEEFE
GEORGE PLOWMAN
TED SEMPLE
THIRTY TWO BIT PT:
LARRY WADE

****
* d i g i t a l *
****

TO: WARD MACKENZIE

cc: see "CC" DISTRIBUTION

DATE: WED 16 DEC 1981 10:59 EDT
FROM: LARRY WADE
DEPT: TECH. OEM MARKETING
EXT: 223-3689
LOC/MAIL STOP: PK3-1/M12

SUBJECT: SCORPIO AND BI

I do not believe that a UNIBUS version of SCORPIO is a viable product for TOEM. I strongly believe that our original concepts and goals for the BI were correct and that we must figure out how to implement the original goals as quickly as possible. I don't think we should bother coming out with a UNIBUS SCORPIO.

COMMENTS ON THE BI

1. SPEED - I have heard that some in Engineering believe that the BI performance is overkill. It is not overkill for our markets and competition. I believe that SEL is doing a VLSI version on their machine and I believe they will do a 26MB/SEC implementation. The INTEL Packetbus is rumored to have a 12mb/sec rate. LOTs of our OEMs ask us for access to the backplane bus of the 750 and the 780, because they have devices which require high speed. If the BI is delayed and re-specified to a slower speed, I believe we are making a strategic error for TVG.

2. STANDARDS

There are lots of companies pushing their busses. The beauty of the BI in this domain was that it brought order out of chaos in the internal DEC world. As far as I can tell the last three years of interconnects strategy seems to have slipped into a bad mess. I perceive that the NI strategy is losing momentum, CI is still ridiculously expensive (and not totally funded) and we are still inventing new interconnects (II, LESI, LNI). I believe that companies which can provide leadership and stability are going to walk away with a lot of the business.

3. MULTIPROCESSOR SUPPORT

I have a concern that DEC is lapsing into such a rigid model that we can no longer keep up with technology. When projects run into trouble we always fall back to our 1970 mono-processor model, while the world advances into more sophisticated multi-computer architectures. I believe that the goal of making the BI conceptually replace the Q and UBUS as "standards" is the right goal, and for the replacement to be viable over the next 10-15 years, we must have multiprocessor support.

4. HIGH END VS LOW END

I assume that there are multiple problems causing Bill and Gordon to propose dropping the BI, or delaying and redefining

it. I also assume that the VENUS problems are one significant factor. I see the tubing of the BI as a way to get more money into VENUS. I propose cancelling VENUS and keeping up with our low end developments. The company has to decide which businesses it is going to be in. I see us continually compromising the low end for the high end. Gordon stated the corporate strategy a few years back to excel in systems below $250K. To me we are pouring so much money into big systems (VENUS, HSC50, CI), that the strategy statement should be amended to reflect the reality that we are going after systems in the 250-1000K range as well.

I urge you to extend the dialog on the BI strategy and not change it overnight. We are making a major change to our complete strategy and I believe the issues should have extensive dialog.

16-DEC-81 11:06:40 S 4121 MLDP

"CC" DISTRIBUTION:

*GORDON BELL	BILL DEMMER	LLOYD FUGATE
JACK MACKEEN	JOHN O'KEEFE	LINDA SARLES

[redacted],

cc Bill Avery, Mike Gutman } Please drive this

DEC 3 1981

digital

INTEROFFICE MEMORANDUM

TO: Gordon Bell
Larry Portner
Jack Smith

cc: DATE: 30 NOV 1981
FROM: Patrick Buffet
DEPT: Technical External Resources
EXT: 223-2453
LOC: ML1-5/M83

CC: Pete Connell
Mitch Federman
Don Feinberg
Lloyd Fugate
Sam Fuller
Don Gaubatz
Mike Gutman
Paul Kotch
Jack MacKeen
Don Metzger
Dave Schanin
Herb Shanzer
Joe Tiano
George Tranos
Mike Weinstein
Pat White
Maurice Wilkes

SUBJ: ii BUS RELEASE: PUBLICITY AND STANDARDS. UPDATE.
REF: My memo of 8.11.81

The ii is still important to our ability to use industry chips, this is why I'm writing this memo. Since the referred memo, Dave has received feedback from the vendors and accordingly changed slightly his spec.

The new version 2.1 of the spec will be reviewed internally to DEC in December; Dave drives that.

Dave will also reconfirm the agreement in principle, he had obtained within DEC to release the spec to the vendors as being "final".

At this point, it seems to be our consensus that on IEEE standards group looking into the ii could have a negative effect. It could lead toward an only incrementally better version which is not the one we want.

Obtaining a de facto industry standard is a matter of publicity, then commitment to the principle. Pete Connell in our Public Relations Department is investigating a "P.R." package that would include exposure in the trade press. As Dave and I discuss with more people, we will update you within 2 months.

By the way, does anyone volunteer to:

1) Drive the ii P.R. effort?
2) Fund the ii P.R. effort?

So far the ii is a monument built to the "bootleg" engineering process. Are we keeping the tradition?

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DIGITAL
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INTEROFFICE MEMORANDUM

TO: GORDON BELL

DATE: 11 AUG 81
FROM: PATRICK BUFFET PB
DEPT: TECHNICAL EXTERNAL RESOURCES
EXT: 3-2453
LOC/MAIL STOP: ML3-2/E41

CC: MITCH FEDERMAN
DON FEINBERG
LLOYD FUGATE
SAM FULLER
MIKE GUTMAN
PAUL KOTCH
JACK MACKEEN
DON METZGER
LARRY PORTNER
DAVE SCHNIN
HERB SHANZER
JOE TIANO
GEORGE TRANOS
MIKE WEINSTEIN
PAT WHITE
MAURICE WILKES

SUBJECT: RELEASE OF THE ii SPECIFICATION, YOUR NOTE ON HERB'S MEMO OF 7.22.81

You want to improve the mileage we get out of the release of the ii specification, by obtaining publicity and driving the industry with a standard.

Publicity:

Mitch Federman in LSI Purchasing will be the person releasing the specification externally. Mitch works with our public relations to get visibility in the trade press. The form he suggests is a first page article in Electronic News with picture and interview. The rest of the press would be given a statement. This will announce the ii to a broad audience, at no cost to us, but with little depth unless we follow up in a technical article elsewhere.

The iEEE/ACM publications have a lead time to press of 6 to 18 months, which we do not control. They also require a fully written document, ready for print. We do not seem to have volunteers to write a lengthy article yet. This can be alleviated somehow by granting an exclusive interview to an editor of a commercial magazine (Electronics...). He will write an article in his trade magazine under his name. The more material we supply the more we control the actual rendition. I'll be glad to orchestrate this approach if we go for it.

If we are ready to invest in a presentation, conferences will give us exposure. The one I know well (ISSCC) is really about chips for which silicon exists, it is premature for the ii - WESCON will be with us in a few weeks, we already missed it. Lloyd can you do something? (CompCom, NCC, Electro ?)

Standards

We have a person on the iEEE "Microprocessor Standards Committee" (Don Feinberg). The ii fits to a tee the concept of the "micro bus" which was debated a few years ago by group P 596. The group was then disbanded because there was no reality to their discussions! Now when the ii is giving credence to the approach we could ask for the regrouping of P 596. Pat White notes that there is a risk to do so immediately: the iEEE group could modify our proposal if someone else has an equivalent approach that we do not suspect yet. (a la F.P.A.). By understanding the reactions of the vendors to the ii release we will be able to know the kind of support we have and strategize. I made a note to discuss the standardization issue in a meeting in early November.

CTi

The CTi is basically a superset of the ii. We could possibly have it in mind when dealing with the publicity and the standardization for the ii. Mike Weinstein what do you think?

attachment

Sam. We are proposing a very powerful standard here vis a vis the Semiconductor industry. I'd like us to do it with much more flair & via the industry Stds. process in parallel. Also could we do it with publicity?

Gordon

Pat

group VP C.

MacKeen Fugate Wilkes

Fdh

JUL 23 1981

+----------------+
| d i g i t a l |
+----------------+

INTEROFFICE MEMO

TO: GORDON BELL
LARRY PORTNER
MIKE GUTMAN

DATE: 22-JUL-81
FROM: HERB SHANZER
DEPT: 16 BIT PROGRAM OFFICE
EXT: 223-5159
MAIL STOP: MLI-2/E60

SUBJECT: RELEASE OF THE II SPECIFICATION

As you may know, David Schanin in the 16 Bit Advanced Development Group has been working on the II Specification. The II Specification is being created to give Digital a common LSI interconnect for the design of custom LSI, as well as to optimize the utilization of commodity LSI in our systems. For this reason, it is important to acquire the commodity LSI vendors' inputs to the II. Prior to releasing the final version internally, he is planning to ask the commodity LSI vendors to review the II Specification for their inputs relative to interfacing their LSI to the II. The legal people (Les Grodberg), LSI purchasing (Mitch Federman), and myself have no objections to releasing the specification for review, and Dave will be rechecking with the uCPG Product Line (LLoyd Fugate and Jack MacKeen) who have had no objections in the past. Since the II was used as the interface on the Ethernet chip RFP, there is already precedent for releasing the spec.

I know that Dave has already discussed this issue with you, Gordon, so unless someone raises additional objections by the end of July, Dave will be relesing the II Specification for vendor review.

This is fine ... but let's maximize the situation!

Gordon Bell

ML12-1/A51

00 BURT DECGRAM ACCEPTED S 11958 O 49 06-DEC-81 20:54:12

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* d i g i t a l *
****

TO: BILL DEMMER

cc: see "CC" DISTRIBUTION

DATE: SUN 6 DEC 1981 8:51 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

SUBJECT: BI AND NAUTILUS: REVIEW AT THE OPERATIONS COMMITTEE

It is gratifying to hear that there is an alternative to the BI. This sure agrees with my gut feel, given it has taken so long. I hope the consensus is use Unibus until we can be compatible with an international standard. Motorola's VME seems to meet every constraint: cost, bandwidth, chip availability and Euroformfactor. When can we make this decision and save our money?

We seem to be getting nowhere on looking at a trade-off of processor product cost versus earlier time to market with Nautilus. In order that we not lose a critical month (I'm gone from 12/20 to 1/10), I would like to get this issue scheduled with Ken and the Operations Committee for early Jan. Ken would like to meet with you, Don, Steve, Bob and I on this. Would you please arrange the meeting and presentation?

Both of these items are too big to be made by the current processes which go nowhere near the Group Vice Presidents or Operations Committee. They are big, $50 to $100 million dollar engineering expense, items and far more when you look at the revenue and other cost impacts. We must insist that others review the wisdom of our direction and recommendations.

"CC" DISTRIBUTION:

SAM FULLER
KEN OLSEN

GVPC:
JACK SMITH

DON MCINNIS
BILL STRECKER

****
* d i g i t a l *
****

TO: BILL DEMMER

cc: *GORDON BELL
EDWARD A. SCHWARTZ

DATE: TUE 8 DEC 1981 2:14 PM EST
FROM: KEN OLSEN
DEPT: ADMINISTRATION
EXT: 223-2301
LOC/MAIL STOP: ML10-2/A50

SUBJECT: NEW BI BUS FOR FUTURE VAX PRODUCTS

I understand the new BI BUS for future VAX machines requires a significant investment measured in tens of millions of dollars and will require additional processes, as well as delaying the time to market of our machines.

We have a policy that investments in product or equipment that come to several million dollars have to be reviewed by the Board of Directors.

Before the decision is made on our new BUS structure, will you let me know the cost implications of it and the product cost, savings, and other benefits. We will plan to bring it to the Board of Directors in January.

KHO:ml
KO1:S7.82

SCORPIO SYSTEM

HARDWARE IMPLEMENTATION ALTERNATIVES

D. LIGNOS
30 JULY 82
DL6.13

SYSTEM I (CURRENT DESIGN CENTER)	SYSTEM II (SINGLE AZTEC)	SYSTEM III 5 1/4" STORAGE)
BI AND UNIBUS	BI ONLY	BI ONLY
AZTEC DISK (SINGLE AND DUAL)	SINGLE AZTEC DRIVE	5 1/4" DISK FIXED
RX50 CONSOLE LOAD DEV	RX50 CONSOLE LOAD DEV	5 1/4" TAPE STREAMER
2 MB MEMORY (MIN)	2 MB MEMORY (MIN)	RX50 CONSOLE LOAD DEV
PEDESTAL PACKAGING	PEDESTAL PACKAGING	2MB MEMORY (MIN)
NO OF USERS: 2	NO OF USERS: 2	PEDESTAL PACKAGING
CENTRAL SUPPLY	CENTRAL SUPPLY	NO OF USERS: 2
LA200 TERM	LA200 TERMINAL	CENTRAL SUPPLY
VMS COMPATIBLE	VMS COMPATIBLE	LA200 TERMINAL
		VMS COMPATIBLE

IN ADDITION: OUR PLANS INCLUDE THE DEVELOPMENT OF AN OEM BOX COMPRISED OF THE FOLLOWING COMPONENTS:

SCORPIO CPU MODULE	POWER SUPPLY
MEMORY (2MB)	RX50
UNIBUS (9 SLOT)	RACK MOUNT
BI (6 SLOT)	

D. LIGNOS
30 JULY 82
DL6.13

	SYSTEM 1	SYSTEM II	SYSTEM III	OEM BOX
ELECTRONICS	3,665	3,150	3,300	3,475
PACKAGING	430	360	360	350
POWER	1,200	900	630	950
AZTEC I	2,000	2,000	---	---
5 1/4" DISK (FIXED)	---	---	1,400	---
5 1/4" STREAMER	---	---	442	---
RX50	250	250	250	250
TERMINAL	800	800	800	---
MFG ASSY & TEST	400	275	275	275
TOTAL COST	$8,745	$7,735	$7,457	$5,300

COMMENTS:

- ALL SYSTEMS EXCLUDE COMM OPTIONS:

DMF32	$1,028	
BI COMM	800	INCLUDES DISTRIBUTION PANEL
BI MFA	650	

- SYSTEM A COST IS FOR A SINGLE AZTEC OPTION.

D. LIGNOS
30 JULY 82
DL6.13

PROJECTED DEVELOPMENT COSTS (FY'83) AND SCHEDULE

	SYSTEM I	SYSTEM II	SYSTEM III
DEVELOPMENT SCHEDULE	Q3 FY'85	Q3 FY'85	Q3 FY'85
DEVELOPMENT COST	$8.2M	$8.2M+	$8.2M+

COMMENTS:

- THE DEVELOPMENT SCHEDULE FOR ALL THREE ALTERNATIVES DOES NOT ALTER, SINCE THE CRITICAL PATH IS STILL THE V-11 CHIPS AND CPU MODULE AVAILABILITY IN Q1 FY'85.

- THE CONTINUATION OF THE BUA DEVELOPMENT (EVEN ON BI ONLY SYSTEMS) IS NEEDED FOR THE OEM BOX CONFIGURATIONS.

- A BI ONLY SYSTEM APPROACH, PUTS EMPHASIS ON THE DEVELOPMENT OF BI OPTIONS (PRESENTLY NOT FULLY FUNDED AND NOT ON CRITICAL PATH).

- NON-AZTEC SYSTEMS PRESENT ADDITIONAL RISKS TO THE SCORPIO PROGRAM DUE TO VENDOR DEPENDENCY. AND NEW SOFTWARE DEVELOPMENT REQUIREMENTS (VMS SUPPORT FOR 5 1/4" PRODUCTS).

D. LIGNOS
30 JULY 82
DL6.13

SYSTEMS ISSUES ASSOCIATED WITH THE ALTERNATIVES

SYSTEM I: CURRENT DESIGN CENTER

ADVANTAGES:

- PROVIDES FOR BOTH SINGLE AND DUAL AZTEC CONFIGURATIONS (84 MBs MAXIMUM STORAGE).

- ALLOWS FOR EXPANDABILITY TO AZTEC II CAPACITY AND PERFORMANCE (300 MBs MAXIMUM STORAGE).

- PEDESTAL SYSTEM INCLUDES BOTH BI AND UB BACKPANELS. ALLOWS FOR USE OF UNIBUS OPTIONS.

- THE SYSTEM CAN ACCOMMODATE UP TO 18 USERS (16 USERS WITH BI COMM OR DMF32 AND TWO SERIAL LINES).

- DESK-HIGH (28") BY 20" WIDE AND 24" DEEP PORTABLE ENCLOSURE (FOR OFFICE COMPATABILITY). (FITS UNDER SOME U.S. DESKS BUT MEETS THE DESK HEIGHT IN EUROPE.)

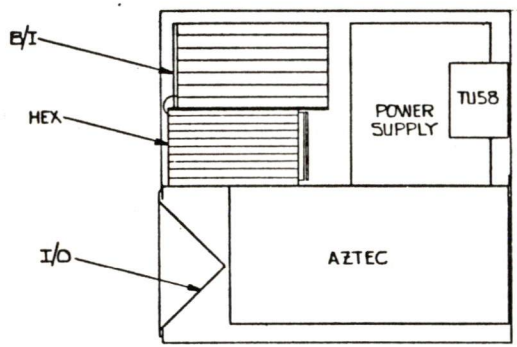
DISADVANTAGES:

- HIGH TRANSFER COST (AS PRESENTLY CONFIGURED AND DEFINED).

- LARGEST OFFICE COMPATIBLE PHYSICAL SIZE SYSTEM PACKAGE (AMONG THE THREE ALTERNATIVES).

- 20 AMP LINE CARD REQUIRING DEDICATED OUTLET AND POWER LINE.

D. LIGNOS
30 JULY 82
DL6.13



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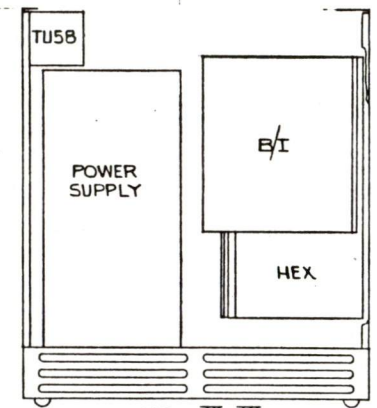
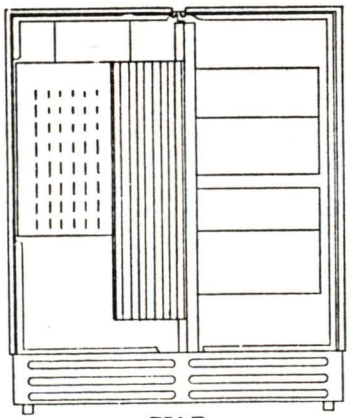
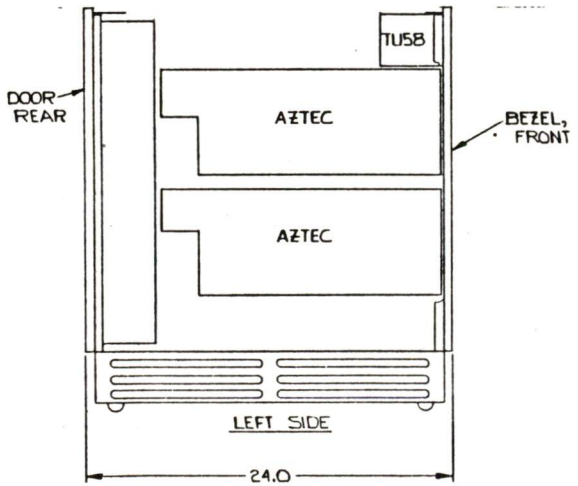


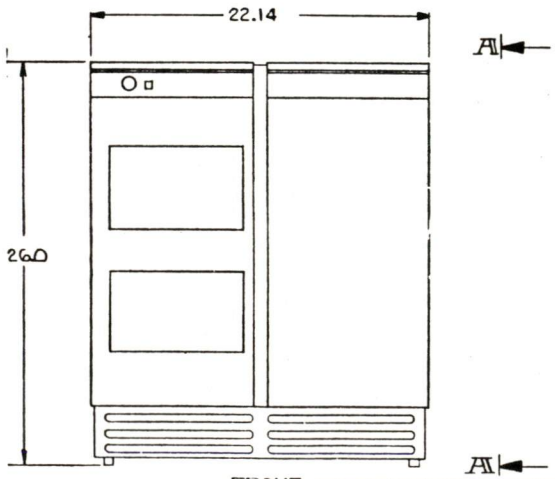
VIEW A-A
RIGHT SIDE



REAR
W/O I/O



LEFT SIDE



FRONT

SYSTEM I : SINGLE OR DUAL AZTEC, BI AND UB CONFIGURATION

DESCRIPTION	DWG PART NO	ITEM NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE MILLIMETER					
		OVER 1 TO 5	OVER 5 TO 30	OVER 30 TO 100	OVER 100 TO 300	OVER 300 TO 1000	OVER 1000 TO 2000
SURFACE QUALITY IN MICROINCHES	MEDIUM ☐	±0.1	±0.2	±0.3	±0.4	±0.6	±1.0
	PREFERRED ☐	±0.3	±0.4	±0.6	±1.0	±1.6	±2.5

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL

DRN
CHK'D
ENG
PROJ ENG
PROD
NEXT HIGHER ASSY

FIRST USED ON

digital

TITLE

SCORPIO, SYSTEM I

SIZE | CODE | NUMBER | REV

REV | NUMBER | SIZE | CODE

SYSTEM II: SINGLE AZTEC BI ONLY SYSTEM

ADVANTAGES:

- LOWER TRANSFER COST THAN SYSTEM I.

- SMALL PACKAGE: 24" (HIGH) X 14" (WIDE) X 24" (DEEP)

DISADVANTAGES:

- BASIC SYSTEM EXPANDABILITY IS LIMITED. NO UNIBUS EXPANSION FOR ENTRY LEVEL SYSTEM.

- IF UNIBUS EXPANSION IS DESIRED, THEN TWO ALTERNATIVES EXIST:

    A. DESIGN ANOTHER SMALL CABINET WITH UNIBUS SLOTS INSTEAD OF BI (PHYSICALLY BOLTED AGAINST THE SYSTEM CABINET).

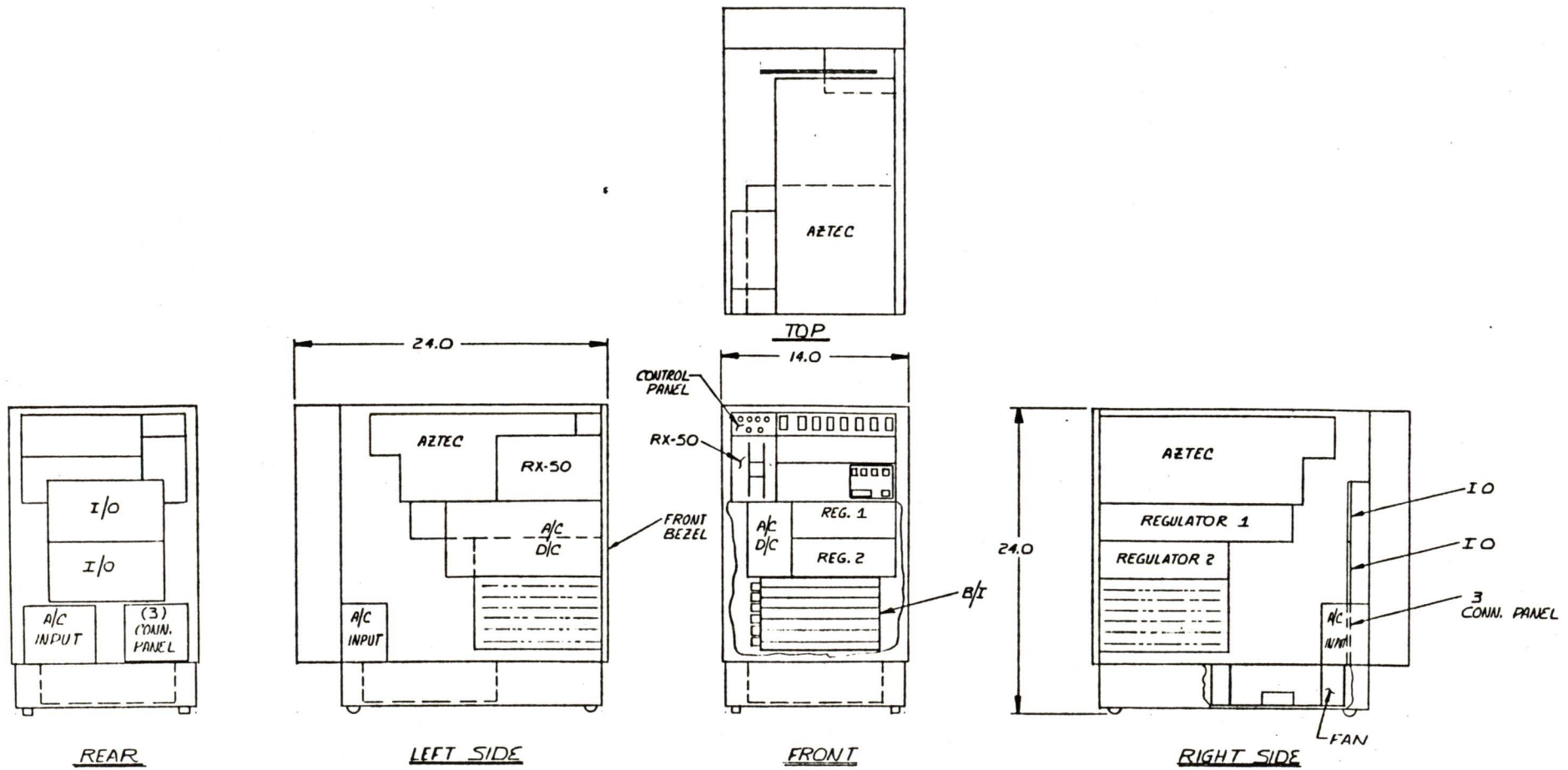
    B. USING THE OEM BOX, PROVIDE FOR UNIBUS OPTIONS.

- STORAGE EXPANSION IS LIMITED TO THE AZTEC II. IF ADDITIONAL STORAGE IS DESIRED, THE ABOVE ALTERNATIVES ARE VALID IN THIS CASE ALSO.

- DIGITAL DOES NOT KNOW HOW TO MARKET A SYSTEM WITH A SINGLE SPINDLE (F+R) DISK. THE MAJORITY OF OUR CUSTOMERS (ESTIMATED AT 80%) WILL REQUIRE A SECOND AZTEC (FOR MULTI-USER APPLICATIONS).

- REQUIRES FIRM COMMITMENTS AND DELIVERY SCHEDULES FOR ADDITONAL BI OPTIONS.

D. LIGNOS
30 JULY 82
DL6.13



System II : Single Aztec, BI only configuration

DESCRIPTION	DWG./PART NO.	ITEM

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE MILLIMETERS				
		OVER 1 TO 6	OVER 6 TO 30	OVER 30 TO 100	OVER 100 TO 300	OVER 300 TO 1000
SURFACE QUALITY IN MICROINCHES	ISOMIN ☐	±0.1	±0.2	±0.3	±0.4	±0.6
	PREFERRED ☐	±0.3	±0.4	±0.8	±1.0	±1.5

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL

DRN

CHK'D

ENG.

PROJ. ENG.

PROD

NEXT HIGHER ASSY.

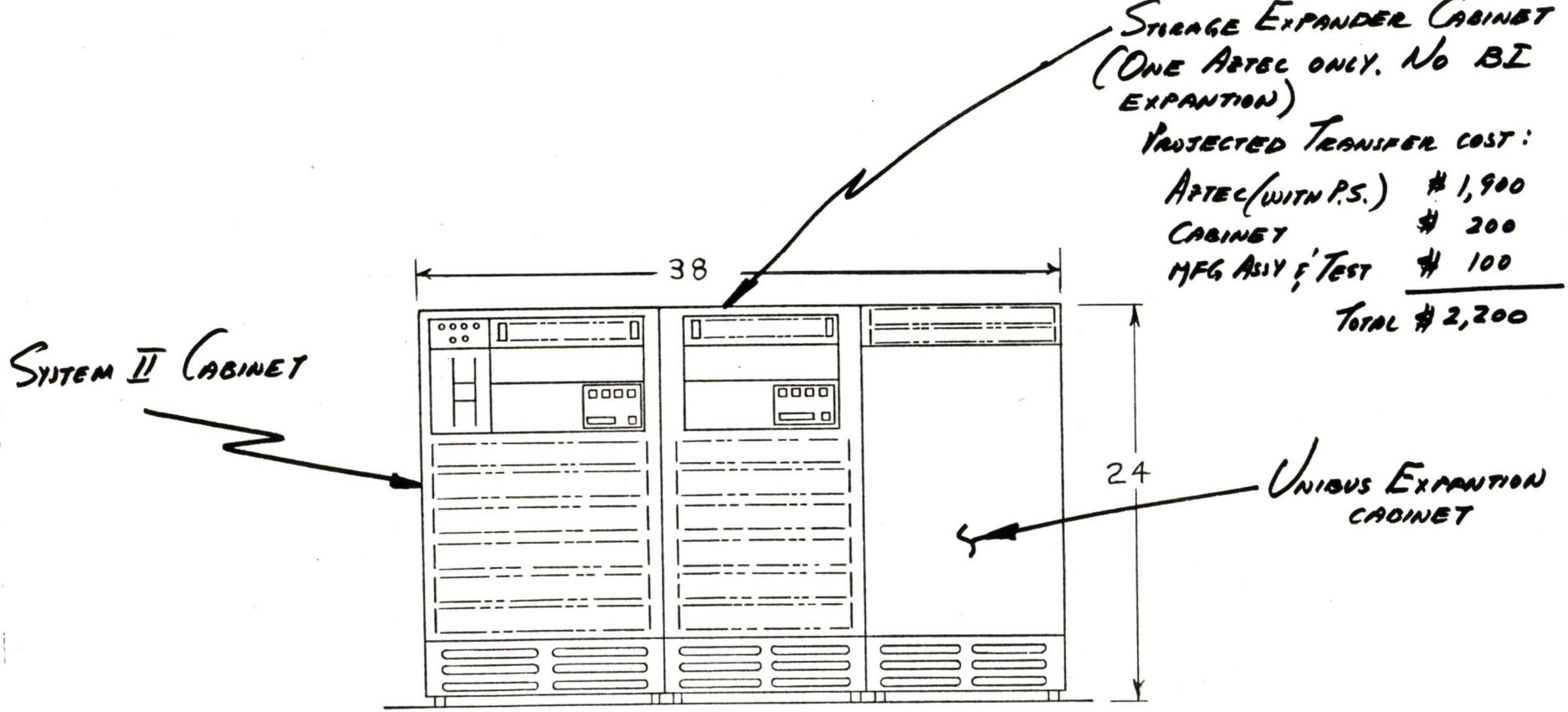
FIRST USED ON

digital

TITLE SCORPIO, SYSTEM ID

SIZE | CODE | NUMBER

REVISIONS | REV | CHANGE NO.

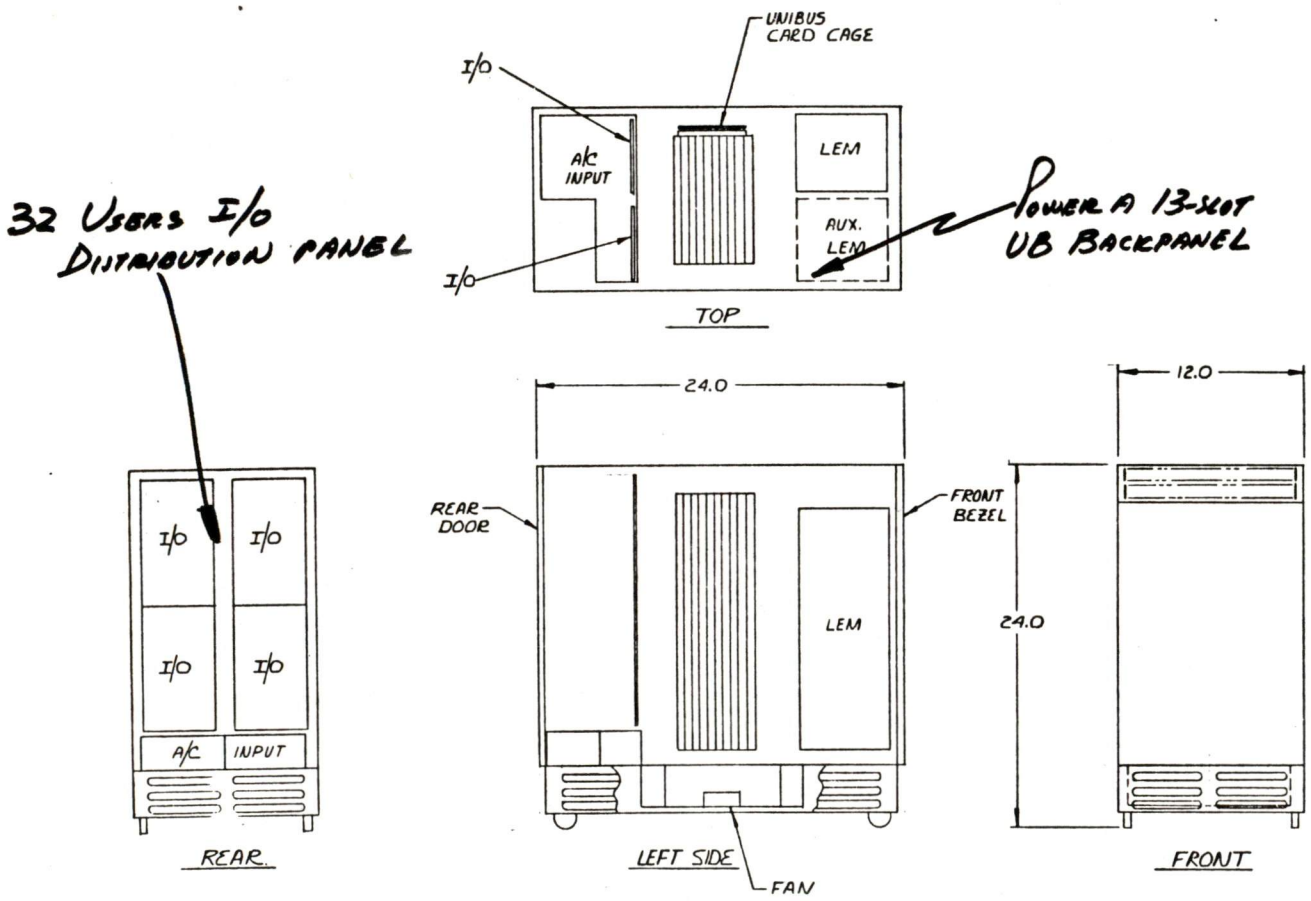


EXPANDED SYSTEM II

MULTI-CAB PEDESTAL CONFIGURATION FOR EXPANTION

PROJECTED TRANSFER COST:

BUA	$600
CABINET	$250
BLOWER	$ 50
UB BACKPLANE (9-SLOT)	$225
POWER SUPPLY (REUTO)	$150
MFG. ASSY AND TEST	$125
TOTAL	$1,700



UNIBUS EXPANTION PEDESTAL CABINET

DESCRIPTION						DWG./PART NO.					ITEM NO
UNLESS OTHERWISE SPEC. ED DIMENSIONS ARE IN MILLIMETERS											
ANGLES 10' 30'	CLASS OF ACCURACY (CHECK ONE)		NOMINAL DIMENSION RANGE MILLIMETER								
			OVER 1 TO 3	OVER 3 TO 30	OVER 30 TO 100	OVER 100 TO 300	OVER 300 TO 1000	OVER 1000 TO 2000			
SURFACE QUALITY IN MICROINCHES	MEDIUM ☐		101	102	103	104	105	110			
	PREFERRED ☐		103	104	106	110	116	125			
QUANTITY & VARIATION											
THIRD ANGLE PROJECTION	DRN. CC Brown		FIRST USED ON								
	CH'K'D		digital								
	ENG.		TITLE								
REMOVE BURRS AND BREAK SHARP CORNERS	PROJ. ENG.		UNIBUS EXPANSION PEDESTAL								
DO NOT SCALE DWG.	PROD.										
MATERIAL	NEXT HIGHER ASSY.		SIZE	CODE	NUMBER						REV.

REVISIONS: REV. / CHANGE NO.

SYSTEM III: 5 1/4" DISK AND STREAMER, BI ONLY SYSTEM

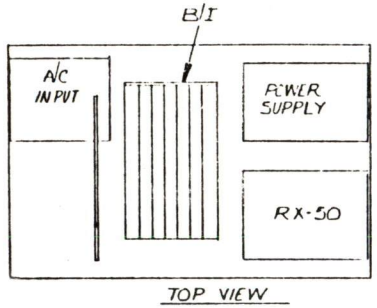
ADVANTAGES:

- LOWEST TRANSFER COST (OF THE THREE ALTERNATIVES).
- SMALLEST AND QUIETEST PACKAGE: 24" (HIGH) X 13" (WIDE) X 24" (DEEP)
- ALLOWS FOR STORAGE EXPANSION VIA THE EVOLUTION OF 5 1/4" STORAGE PRODUCT TECHNOLOGY.
- DUE TO SEPARATE SPINDLES, MULTI-USER ENVIRONMENT IS NOT IMPACTED (AS WITH SYSTEM II).
- ANY 5 1/4" FORM FACTOR DEVICE CAN FIT IN THE SPACES PROVIDED.
- 15 AMP STANDARD LINE CORD SYSTEM.

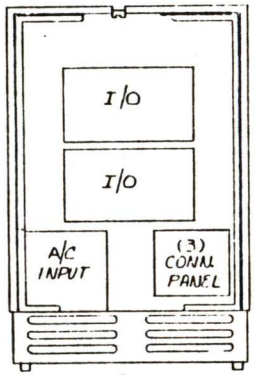
DISADVANTAGES:

- LIMITED ALTERNATIVES FOR UNIBUS EXPANSION (SAME AS FOR SYSTEM B).
- MAJOR RISK TO THE PROGRAM, THE BUYOUT EFFORT OF TWO 5 1/4" PRODUCTS. DIGITAL HAS NOT BOUGHT A STREAMER BEFORE.
- NEW VMS SOFTWARE DRIVERS NEED TO BE DEVELOPED TO SUPPORT THE 5 1/4" SOTRAGE PRODUCTS.
- THERE ARE NO COST DIFFERENCES BETWEEN A SINGLE AZTEC (F+R) SUBSYSTEM AND A 5 1/4" DISK AND STREAMER SUBSYSTEM.
- REQUIRES FIRM COMMITMENTS AND DELIVERY SCHEDULES FOR ADDITIONAL BI OPTIONS.

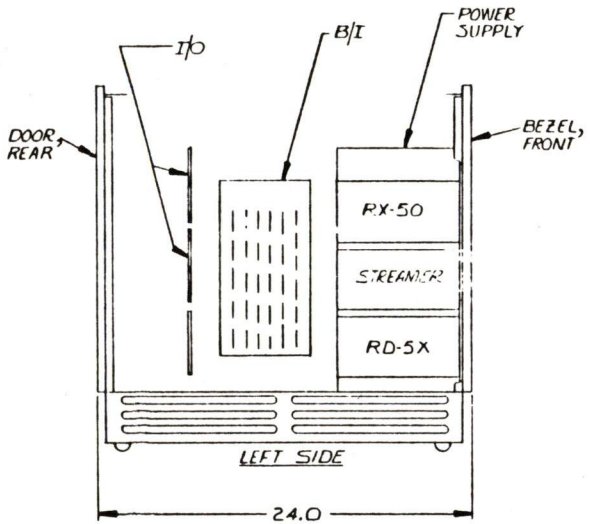
D. LIGNOS
30 JULY 82
DL6.13



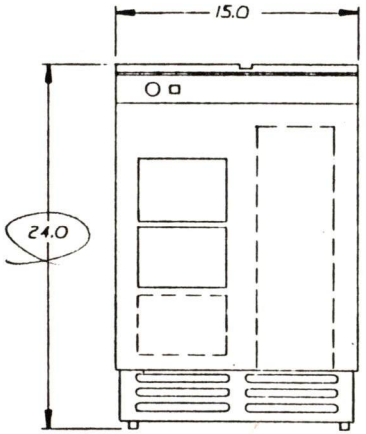
TOP VIEW



REAR W/O DOOR



LEFT SIDE



FRONT

DESCRIPTION	DWG PART NO	ITEM NO
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS		

ANGLES ± 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL SIZE RANGE MILLIMETERS					
SURFACE QUALITY IN MICROINCHES	MEDIUM						
QUANTITY & VARIATION	PREFERRED						

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL

FINISH

DRN	
CHK'D	
ENG	
PROJ ENG	
PROD	
NEXT HIGHER ASSY	
SCALE	

FIRST USED ON

digital

TITLE

STORFIO, SYSTEM C

SIZE	CODE	NUMBER	REV
1			

REVISIONS		
REV	CHANGE NO.	

SYSTEM III : 5 1/4" DISK AND STREAMER, BI ONLY CONFIGURATION

SCORPIO SYSTEMS BUILT CONFIGURED WITH OEM BOX

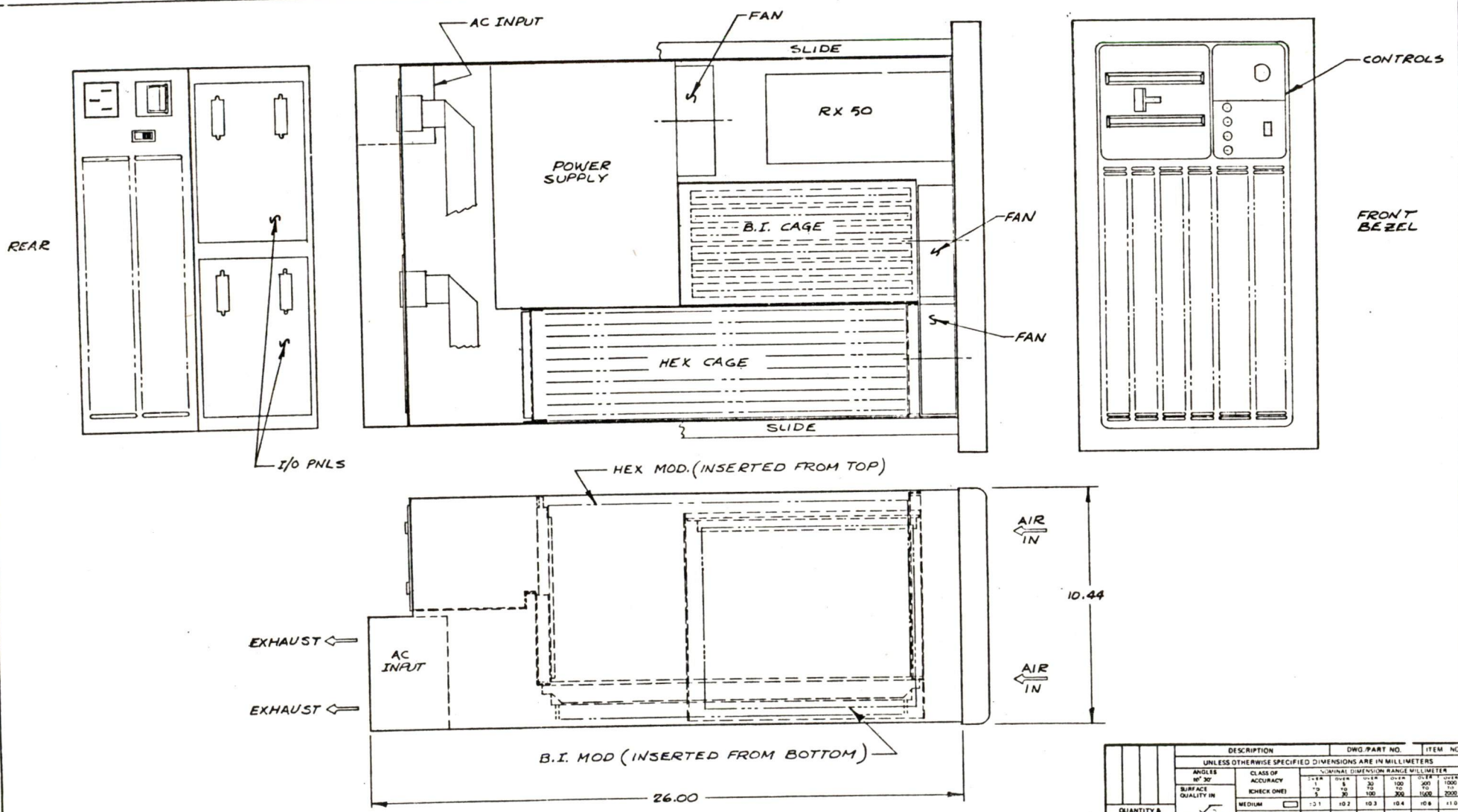
ADVANTAGES:

- ALLOWS MAXIMUM EXPANDABILITY BOTH IN AN OFFICE ENVIRONMENT (ACOUSTICAL CAB) OR IN THE COMPUTER ROOM ENVIRONMENT (STANDARD CAB).
- MAXIMUM FLEXIBILITY FOR BI AND UNIBUS OPTIONS.
- RACK-MOUNT ELECTRONICS PACKAGING (STANDARD RACK).
- AT LEAST 32 USERS.

DISADVANTAGES:

- LARGE CABINET (FOOTPRINT AND HEIGHT) FOR OFFICE ENVIRONMENT.
- LACK OF PORTABILITY.
- REQUIRES ADJACENT CABINETS FOR LARGE STORAGE CAPACITY AND HIGH PERFORMANCE PRODUCTS.

D. LIGNOS
30 JULY 82
DL6.13



Scorpio OEM Box

DESCRIPTION	DWG./PART NO.	ITEM NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE MILLIMETER					
SURFACE QUALITY IN MICROINCHES		OVER 1 TO 5	OVER 5 TO 30	OVER 30 TO 100	OVER 100 TO 300	OVER 300 TO 1500	OVER 1000 TO 2000
	MEDIUM ☐	±0.1	±0.2	±0.3	±0.4	±0.6	±1.0
✓	PREFERRED ☐	±0.3	±0.4	±0.6	±1.0	±1.6	±2.5

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

DRN. [illegible] 10/28/

CHK'D

ENG.

PROJ. ENG.

PROD.

NEXT HIGHER ASSY

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG.

MATERIAL

FINISH

FIRST USED ON

digital

TITLE SCORPIO CEM BOX VERSION 4

SIZE 1 | CODE | NUMBER | REV.

SCALE 1/1

SHEET 1 OF 1

REVISIONS: REV. | CHANGE NO. | BY

Transfer Cost Info (Estimated)

- **Basic Scorpio OEM Box and Cabinet:**

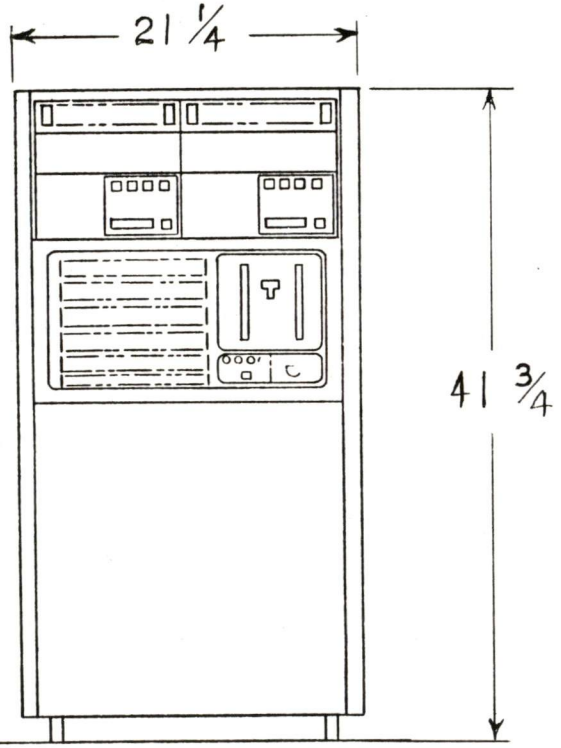
Scorpio OEM Box:	# 5,300
Cabinet	# 500
Power Control Box	# 150
MFG Assy and Test	# 200
Total	# 6,150

- **Single Aztec Configuration:**

OEM Box with Cab:	# 6,150
Aztec Subsystem (includes P.S.)	# 2,600
Terminal (LA200)	# 800
MFG Assy and Test	# 200
Total	# 9,750

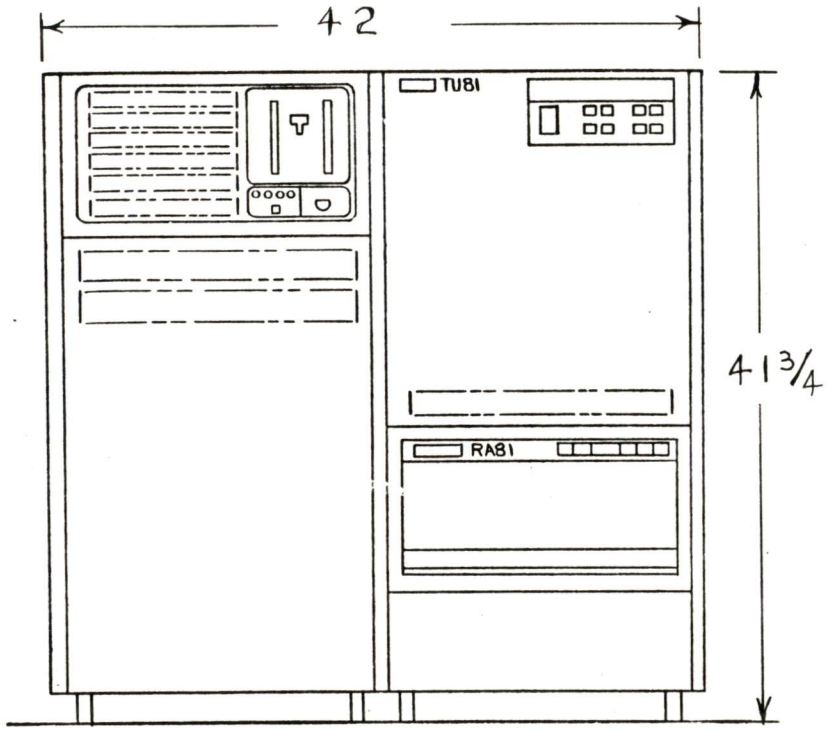
- **Dual Aztec Configuration:**

Single Aztec System:	# 9,750
Second Aztec (slave):	# 1,885
	# 11,750



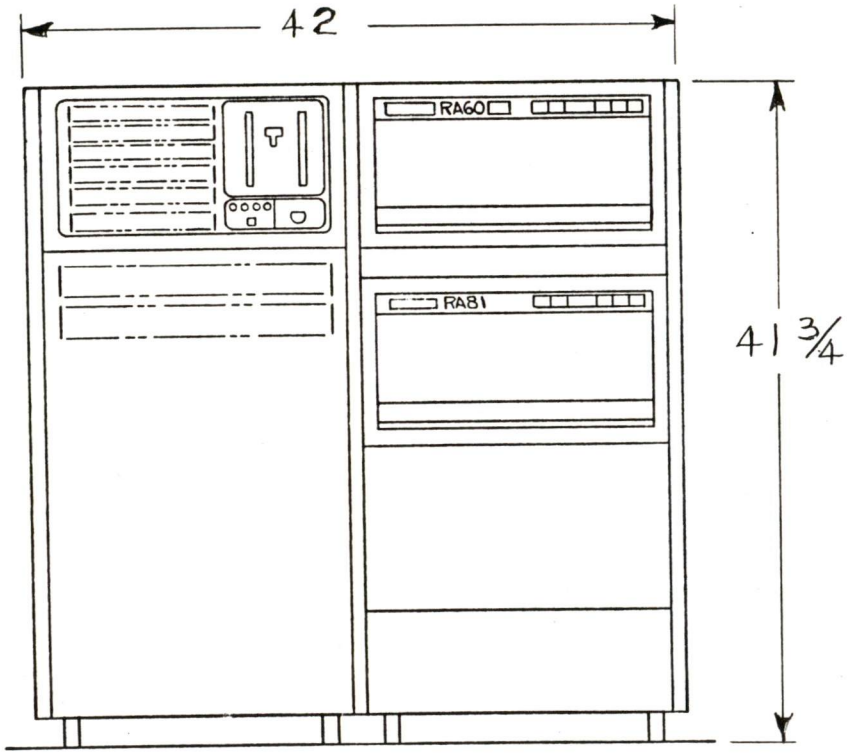
DUAL AZTEC SYSTEM

Note: For an Accoustical cab., add # 200.00.
(Accoustical cab is 40" deep)



RA81/TU81 SYSTEM

Scorpio OEM BOX WITH RA81/TU81 STORAGE PERIPHERALS



RA60 / RA81 SYSTEM

SCORPIO OEM BOX WITH RA60/RA81 STORAGE PERIPHERALS

SUMMARY/CONCLUSIONS

- HOW THE MARKET WILL RESPOND TO BI ONLY SYSTEMS, WITHOUT EASY UNIBUS OPTIONS EXPANDABILITY.

- THE ALLEGED COST ADVANTAGE OF THE 5 1/4" PRODUCTS AGAINST THE AZTEC IS NOT REAL.

- PACKAGING OUR SMALL BI ONLY SYSTEMS FOR UNIBUS EXPANDABILITY IS EXPENSIVE.

- CONCENTRATING ON BI ONLY SYSTEMS WILL INCREASE THE DEVELOPMENT COSTS FOR FY'83 SINCE THE BI OPTIONS ARE NOT FUNDED OR COMMITTED PRODUCTS AT THIS TIME.

- MARKETING A SINGLE SPINDLE SYSTEM IS A FIRST FOR DIGITAL. NOT SURE AT THIS TIME HOW OUR CUSTOMERS WILL RECEIVE SUCH A PRODUCT (SYSTEM II).

D. LIGNOS
30 JULY 82
DL6.13

SUMMARY TRANSFER COSTS

	BASE COST	ADD SECOND AZTEC	BI ONLY (SINGLE AZTEC)	UNIBUS EXPANSION	ACOUSTICAL CAB	STANDARD CAB
SYSTEM I	8,745	10,245	8,100			
SYSTEM II	7,735	9,935 (NO BI EXPANSION)		9,435 (NO DISK EXPANSION)		
SYSTEM III	7,457			9,157 (NO DISK EXPANSION)		
OEM BOX	5,300				6,350 (NO PERI-PHERALS)	6,150 (NO PERI-PHERALS)

NOTES:

- OEM BOX CABINET INCLUDES POWER CONTROL BOX, I/O DISTRIBUTION PANEL AND MANUFACTURING ASSEMBLY AND TEST COSTS.

- NO COMMUNICATION MULTIPLEXERS INCLUDED IN THE ABOVE NUMBERS.

D. Lignos
30 July 82
DL6.13

LEGEND/NOTES

⊠ = INITIAL OFFERING

⊗ = FOLLOW-ON OFFERING (NEW DISKS, NATIVE BI, ETC.)

ALL SYSTEMS 2 MB MEMORY EXCEPT DUAL RAXY AND RAXX/TA81 WHICH ARE 4 MB.

$ = TRANSFER COST

40" CABS

DUAL RAXY OR RAXX/TA81: ⊗ 600 + MB (4MB) $15.9/20.2K —(+3 BI COMM)→ ⊗ 600 + MB (4MB)

DUAL RA60 OR RA81/TU81: ⊠ 400 + MB $16.9/21.0K —(+3 DMF32)→ ⊠ 400 + MB

PEDESTAL

SYSTEM I DUAL AZTEC II: ⊗ 75/MB —(+ BI COMM)→ ⊗ 150MB/150MB $10.4K

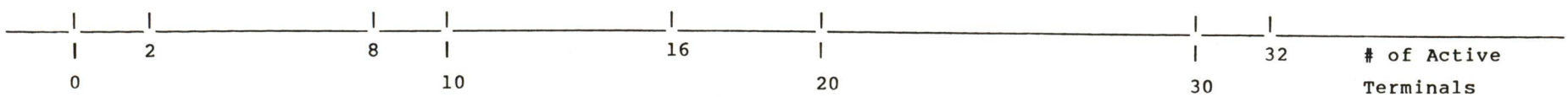
SYSTEM I SINGLE AZTEC II: ⊗ 75MB/75MB $8.0K —(+ BI COMM)→ ⊗ $8.8K —(+ AZTEC II + BI COMM)→ ⊗ 150MB/150MB $10.4K

SYSTEM I DUAL AZTEC: ⊠ 21MB/21MB $9.8K —(+ DMF32)→ ⊠ 42MB/42MB $11.3K

SYSTEM I SINGLE AZTEC: ⊠ 21MB/21MB $8.7K —(+ DMF32)→ ⊠ $9.8K —(+ AZTEC + DMF32)→ ⊠ 42MB/42MB $11.3K

NOTE:

THIS SPACE CAN BE CONVERED WITH A DUAL AZTEC OEM PACKAGE CONFIGURATION. SUCH A SYSTEM CONFIGURATION THEN ALLOWS FOR MORE STORAGE AND MORE USERS (COMM DISTRIBUTION).



RECOMMENDATIONS

- STAY WITH THE CURRENT SINGLE AND DUAL AZTEC SYSTEM CONFIGURATION, BI AND UNIBUS SYSTEM IMPLEMENTATION.

- DEVELOP THE SYSTEM HARDWARE COMPONENTS SUCH THAT:

    - SHIP TO SYSTEM WITH ONE AZTEC ONLY (PROJECTED TRANSFER COST: $8,745).

    - SHIP THE SYSTEM WITH BI ONLY (PROJECTED TRANSFER COST: $8,100).

    - DESIGN THE CAPABILITY FOR CUSTOMER INSTALLABLE SECOND AZTEC IN THE FIELD (GOAL).

    - ALLOW THE ABILITY TO INSTALL A SECOND 6 SLOT BI BACKPLANE INSTEAD OF A UNIBUS BACKPLANE (FOR 12 BI SLOTS).

- WE RECOMMEND THAT SUB VMS PRODUCTS (MINI AND MICRO-VMS) SHOULD USE 5 1/4" STORAGE DEVICES.

D. LIGNOS
30 JULY 82
DL6.13

APR 26 1983

d i g i t a l

INTEROFFICE MEMO

TO: GORDON BELL

CC: DEMETRIOS LIGNOS
BILL JOHNSON

DATE: 22 APRIL 83
FROM: BILL DEMMER Bill Demmer
DEPT: 32 BIT SYSTEMS
EXT: 229-6065
LOC/MAIL STOP: LTN01-2/H09
ENG. NETWORK NODE: PHENIX

SUBJECT: YOUR MEMO ON THE BI PACKAGE OF APRIL 6, 1983

Gordon, we believe we have stabilized the BI package and know of no specific problems with it. Attached is Demetrios's detailed evaluation of the strawhorse you presented and the rationale behind why we are where we are with the BI packaging effort.

My own macrolevel summary of the rationale behind the current BI package would be as follows:

1. To achieve the band width and the number of nodes that we've specified for the BI, the electrical characteristics require a denser connection to the backplane then we now have with the green block.

2. While the basic module size is somewhat arbitrary, the design is geared towards a multi module system that allows, in general, individual options to be housed on a single module. This suggests a module of the ball park size we are planning.

3. There appears to be an emerging standard OEM rack configuration that our planned BI module size of 9.2 inches seems to fit that our standard 10.4 inch quad module would not fit. Given the change in connector and module thickness we can find no penalty that Digital is paying to go with the planned BI module. i.e The upside potential may be significant with little or no downside risk associated with size alone.

Because of my own concern over the wisdom of introducing a new connector there has been a lot of pressure in the system for the past several months to make sure the approach we are taking is technically sound and production viable. We have instituted a review process across the range of Digital expertise to maximize our probability of success in the implementation effort.

If you would like, upon your return, we could have an informal round table discussion about the BI package. Meanwhile, if you see any fatal flaws with our plan please have Ken or Jack communicate with us so that we may take the appropriate corrective action.

DL9.47

d i g i t a l

INTEROFFICE MEMO

To: Gordon Bell

CC: Bill Demmer
Bill Johnson

Date: 21 April 1983
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::LIGNOS

Subject: BI Physical Interconnect Strategy Definition

Ref: Your memo "A Reaffirmation of the BI Package," dated 6 April 1983

I would like to try to address the issues that you and Ken have raised on our present BI Physical Interconnect strategy. We are now in the process of finalizing the BI physical interconnect strategy and I have attached, for your information (Attachment #1), the three step process that I am using to publicize our decision throughout the corporation at all levels before it is cast in concrete. The position we are now at, in terms of the BI packaging design, has been evolving over two years of advance development and product development activities. So far, our impression (as a result of numerous presentations to a number of connector experts in Engineering and Manufacturing) has been that our approach is the right one from all aspects, based on what we are trying to do with out next generation systems.

Before I proceed with the qualification of the above statements, I would like to emphasize that the BI physical interconnect recommendation is not and was never intended to be a "Green Block" replacement across the board. I should also state, that the design we have, does not preclude usage of the BI physical interconnect components for other applications throughout our new product development organizations.

A. Original Objectives of the BI Packaging Design

In general, our original BI system's development goals were as follows:

1. The ability to easily configure and reconfigure systems for a large variety of applications (i.e., applications such as Office Environment , Workstation, etc.).

2. Customer installability and maintainability.

3. Maximize the system performance, while at the same time, minimize the physical size of the system box.

4. Develop cost competitive products.

To meet the above goals, we provided the following development solutions:

1. We decided that one major function per module is the simplest way of creating a functional building block concept for our systems. Thus far the KDZ11 CPU, Memory, BUA, BI LESI, BI MFA and others are single module options. A couple of newer options (i.e., BSA, BCA) may be dual module options in their initial implementations.

2. For ease of field installation, repairability and customer maintainability, we decided that no cables should come off the BI modules. The problems with cables in the field have been occasionally disastrous for us and we felt that the technologies of the future that we have available to us would support our decision to eliminate them completely. Such a decision makes things easy for Manufacturing, Field Service and customer handling of our next generation products.

3. To facilitate ease in customer (and the field) insertion and removal of a module, we decided on a ZIF connector. We believe that a zero force insertion and removal of the module from the back panel, will be significant for the product's quality and a major contribution to a lengthy MTBF in the field.

4. Although current and future custom LSI and VLSI technologies support the choice of small modules for the next generation products, the small modules also contribute to the overall reliability, cost and ease of handling of our products. A small module is easier to stock, carry, ship and cheaper to buy than a large one. Because of the high component density requirement of the technologies, the customer may be paying for unused real estate for a function that requires a lot less physical space than the large size module provides.

   I want to emphasize here that the major force behind our decision to go with small modules, was purely technical. The modern high density and performance components require high density pin concentration in order to meet the very stringent electrical characteristics (i.e., lead lengths between components) that are required to meet the performance specs (signal integrity) of the BI bus).

5. Another advantage of a small module is the general requirement of lesser volume of air to cool it. The lesser power and smaller air volume both contribute significantly to the use of the BI in the office environment application of Scorpio and Microvax based products.

6. Further advantage of the smaller modules, with lots of components and interconnect, is our ability to lay them out using automated tools. After a certain component density,

our present CAD tools break down. We already know that we are O.K., as a result of a successfully completed experimental case (VLS will solve these problems when it does become available).

7. We have designed the BI physical packaging components with the BI specs in mind. The present hardware is tuned perfectly to the BI performance specs (more on that, later on).

8. So far the cost associated with the BI physical parts is very much in line with our original cost goals. We have written quotes from vendors that we have based our cost estimates on. Although it is hard to do an "apples to apples" comparison, a rough cost comparison between the "Green Block" and the BI packaging implementations, is as follows:

BI Physical Interconnect:	Cost/pin = 5 cents
Green Block:	Cost/pin = 2.5 cents

B. Highlights of our Current BI Physical Interconnect Strategy

There is a tremendous amount of paperwork and energy that has gone into the BI I/O connector scheme. I will try to spare you a lot of the details (available upon request) in order to give you the highlights of our decision to use the Burndy design of a 300 pin ZIF single piece connector, with 50 mil pin spacing but using 100 mil PWB technology.

1. Why can't we use the existing connector schemes?

I will try to explain that our decision to bring in a new connector was not made capriciously. All the viable existing connector schemes were investigated and for a number of valid reasons they were not acceptable.

a. Electrical Characteristics: In order for the BI bus to meet its performance specs, it is essential that the I/O connector meets stringent RCL characteristics. Any other existing solution (including some Burndy 300 pin connector competitors) did not meet these requirements. For this determination, we looked at the electrical performance requirements that the next generation technology electrical components will impose on the BI physical hardware. (I have attached the comparative technical data between the Burndy and Amp connector for your information; Attachment #2.)

b. Pin Density (300 Pins vs. a Lesser Amount):

At first, not understanding the pin requirements, we used Rent's rule to come up with an I/O pin density, which would satisfy the number of gates that we estimated the BI module would hold. Today, however, the 300 pin arrange-

ment appears to still be valid and may even be on the low side.

Even though the BI bus occupies 120 individual pins (2 60-pin segments on the connector) the rest of the pins are about enough (with a few spares) to:

- Connect the Unibus on the BUA module. (240 pins)
- Connect the LESI interface on the BI LESI module.
- Provide intercommunication (via the back panel) between multi-module BI options (one of the two BSA modules requires 297 I/O pins).
- Etc.

c. Customer Installability:

If a customer can handle the module correctly, then Manufacturing and the Field should have no problems at all. The ZIF concept allows for easy, error free (connector is keyed) insertion and removal of the module in the field. The 2-piece versions (Amp, Terradyne, etc.) require a 50 lb. force to install. I should point out here, that a longer or even larger size module could bend under such force (especially applied by untrained hands), thereby causing a possible intermittent problem due to a hairline crack on the etch.

2. BI Connector Review Results and Recommendations

Following a detailed design review of the chosen BI connector (conducted on February 17th), the recommendation was that the connector design looked good and we should proceed. The responsible design team acknowledged that an extensive test and evaluation program would now be needed to thoroughly test the new connector over the next year to 18 months. Such a test plan is now being prepared and will be available over the next month, for review and comments. (I have attached a copy of the technical review results for your information; Attachment #3.)

Following the completion of the detailed financial analysis (driven by John Hittel from the Nautilus Manufacturing group), we set up a senior technical management review of the BI physical interconnect strategy, but with emphasis on the new BI connector justification. The review actually took place on April 7th. The review team was comprised of:

Don Metzger
Camille Sahely
Dave Thorpe
Walt Hanstein

Dick Best
Bill Demmer
Bill Mooney (Kanata Mfg.)

Dick Gonzales and Dick Clayton had been invited to attend but were unable to make it. In any case, Bill Schmidt talked to Dick Gonzales on the phone on Thursday morning (prior to the meeting) and Dick indicated that he was supportive of the connector design and our decision. From Dick's group, Bruce Weaver (the CT mechanical engineer) is now very familiar with the BI connector design. As a matter of fact, I understand he is considering using a variation of that connector on the next CT set of products.

The review committee unanimously approved our design approach. They listened to the reasons and rationale of our new connector design approach versus the Green Blocks and other connector systems. Based on the technical reasons presented (associated with the BI bus specs), the review committee agreed that the new connector is necessary, as opposed to any of the existing "standard" approaches.

Some of their comments/questions at the review were as follows:

a. Have we looked at 50 ohm impedance for next generation applications? (Present design at 75 ohms.)

b. What is involved if we had to change board thickness? (Board thickness is now spec'ed at .093 ± 10% mils.)

c. What is the longest board size before we can expect contact reliability problems?

d. How do we ECO the backplane? (Several approaches exist, but need to be documented.)

e. Have we looked at the EMI/RFI analysis of the back panel (Multiple cables of various frequencies)?

In general, all the comments were favorable. The review team encouraged us to proceed with the design and bring it into Digital as soon as possible. Their main advice was that "we cannot be too careful, when it comes to the extensive testing and evaluation that is necessary to assure the reliability of the connector."

(Detailed minutes of the above review will be available shortly.)

3. Why Can't we use the Existing "Standard" Module Form Factors? (Dual, Quad, Hex)?

a. Use of Today's "Standard" Modules

My first comment to your "Standard Quad" term, is that it implies the usage of a Quad as we know it today (i.e., present physical size and "Green Block" connector scheme). The same comment, by the way, is true in the case of the other "standard" form factors.

I have already explained, I believe, the reasons why we cannot use the "Green Block" connector system with BI bus systems. Given that, the I/O connector must be different for BI systems, the argument of using the existing module form factors is reduced to mean only in terms of physical dimensions (footprint). A quad size module (or any other physical size module, for that matter) with a new ZIF connector, is indeed a new module type and bears no resemblance to the existing "standard" modules, other than from the general physical dimensions point of view. The BI board itself is a thicker board (.093"), due to the many layers required to handle the larger BI power needs.

Our entire packaging scheme is based on the BI module form factor that we have selected. Because the new connector is modular (multiple 60-pin segments), another connector size can be constructed with more than the five such segments required for the BI modules (300 pins) to fit a larger size module. Nautilus is using a 480 pin connector (eight segments) for the extended hex form factors that they have chosen (NMI interface and intermodule communications). But I want to emphasize that the Nautilus module form factor is not a "standard" extended hex. As a result of the new I/O connector usage, Nautilus will be introducing a new type module.

b. Possibility of Using the Current Quad Module Footprint

The question that comes to mind, in this case, is: "Is there any benefit to using a Quad Std module (8.0"x10.4") versus the BI module size (8.0"x9.2")?" Back, about 18 months ago, when we picked the BI module size (8.0"x9.2") over the Quad module size (8.0"x10.4"), we did it for the following reasons:

- Minimum scrap off the standard size stock panel (board fabrication).

- We were influenced by the Micros Group, who convinced us via a business analysis, that a 9.2" dimension would give us substantial flexibility to compete in the international OEM markets with our BI based board products.

That Micros claim may not be of significance any longer, but we do understand that recently the trend of module dimensions in this country, is being influenced by the 9.2" European standard. A number of companies (such as

Motorola, Intel and others) appear to be moving in that direction for their board products.

The significance of the BI module dimensions (8.0"x9.2") to our program, however, is in the OEM system box design area. The 9.2" dimension is instrumental in our ability to contain the height of the Scorpio OEM box to 10.5 inches. Due to the heavy congestion of system components in the OEM box (i.e., Power Supply, a 9-slot Unibus and a 6-slot BI Logic Cage, etc.), an increase of 9.2" dimension to 10.4" (to meet the present Quad footprint), would require a total redesign of the OEM box package.

At this point, I see no real advantage of considering the 10.4" demension over the 9.2". We will, however, look a little closer (with Manufacturing's help) to make sure that we have not overlooked any one advantage that would be significant enough to cause us to rethink the BI module 9.2" dimension at a later time.

Summary

Gordon, in my opinion the BI physical interconnect strategy is already in place, complete with prototype hardware to fit all cases for present and future BI systems. In addition to Scorpio systems, both Microvax and Nautilus have agreed to use the BI module for all their BI systems. Furthermore, all the engineering groups working on BI options will use the BI module as well.

Using the current BI physical interconnect strategy, we have built full scale metal engineering models, complete with working power supplies (built for Scorpio). We have established the physical dimensions of the pedestal and OEM box configurations and we are now in the process of cabling up the engineering models in preparation for temperature, acoustics and FCC tests.

From the electrical standpoint, we have already sized the major functions and have determined that most of them fit on a single BI module. Those that do not fit on a single module, would probably not fit on a single hex size module either. Our engineers have disciplined themselves to design only what is necessary to incorporate the function under design and, so far, they have succeeded. We now know that the Microvax CPU fits on one BI module also. The BCA and BSA required two modules with today's technology but will fit into one when Hitachi's 20,000 gate array technology becomes available in a few years.

The BI physical interconnect strategy has been accepted by all those who are designing systems and options for the BI. At our April 7 review meeting, the Corporation's senior technical experts (and before them, their senior technical people) saw the need and endorsed the new connector design. The actual physical size of the BI module was not discussed at length at the April 7th meeting, but I believe there was

a general agreement that the future technology trends support our choice of small size modules for our next generation BI systems.

bjc

Attachments 3

(Attachment #1).

DL9.17

| d | i | g | i | t | a | l |

INTEROFFICE MEMO

To: Distribution

Date: 24 January 1983
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::LIGNOS

Subject: BI BUS CONNECTOR SELECTION PROCESS

According to our Scorpio Systems Program Plan, during the month of January we are to make a very significant hardware implementation decision related to the BI bus connector type. Because of the major significance of this decision to our next generation 32-bit systems products, we have devised a process which will, hopefully, help us cover all the potential application situations, before our decision is actually "cast in concrete".

The connector decision process we have decided to follow is actually comprised of three steps:

Step 1: Using an independent team of experienced volume Manufacturing people, do a thorough cost analysis of the acceptable connector alternatives. The independent team was named by Dave Thorpe (Advanced Manufacturing Group) and is comprised of John Hittel (Team Leader), Bill Mooney and Dick Dunlap. Assisting the independent team are Bill Schmidt, Jim Mars and Kevin Reilly from the Scorpio group.

The timeframe for the cost estimating team to meet and perform the cost analysis is about two weeks from now (first week in February). Dave Thorpe will call the meeting and organize the team.

Step 2: Bill Schmidt will organize a thorough technical design review of the connector alternatives. Participating in the review, in addition to the Scorpio personnel, will be technical representatives of other engineering groups that are planning to use the BI bus, technical personnel from the Advanced Manufacturing Group and others who are considered knowledgeable in the micro-packaging technology area. The objective of the review team will be to evaluate the technical data associated with the connector alternatives and help the BI physical interconnect team pick the best alternative.

This meeting should take place around the middle of February after the cost information becomes available. The detailed technical information will be distributed to the review participant a few days ahead of the meeting.

Step 3: Dave Thorpe has recommended a list of names as senior technical managers (the actual names to be announced after the managers have been contacted and their participation assured) to review the connector decision. This review team's objectives are as follows:

a. Review the connector decision process. The reasons why a new type connector is needed for the BI based systems.

b. Review the logical steps that caused the particular connector to be selected.

c. Ask the appropriate questions to assure that something significant has not been overlooked during the decision process.

d. Review the business impact of a new physical interconnect implementation to Digital.

The purpose of this review team is not to review the detailed technical reasons that led us to the selection of a particular connector type. This team can assume that the technical details have been examined during the previous technical review (Step 2).

The expected outcome of this review is the final endorsement of this connector as the BI connector of the future. The timeframe of this review will be about the last week of February. Advanced technical information on the connector will be distributed a few days ahead of this review.

I realize that the actual endorsement of the BI connector decision moves to February instead of the planned January time. Once again the significance of that decision is such that a thorough review process must take place before the corporation is committed to a particular implementation.

Specific dates for the above outlined process steps will be announced in the near future.

DL:clc

(ATTACHMENT #2)

COMPARATIVE BI INTERCONNECT DATA

FUNCTIONALITY	AMP LIF	BURNDY ZIF
BI SIGNAL PINS	89	94
POWER CONNECTIONS	31 SIGNAL PINS 2 SIGNAL PINS	8 POWER P NS AND
I/O SECTION	180 PINS	180 PINS
MODULE INSERTION	TOP ENTRY ONLY	TOP/SIDE ENTRY
MEASURED ELECTRICAL DATA		
MEASURED PIN INDUCTANCE	SHORT PIN 6.5 NH LONG PIN 16 NH	5 NH 6 NH
MEASURED PIN-TO-PIN CAPACITANCE	1.0 PF	0.8 PF
MEASURED IMPEDANCE (SIGNAL AND RETURN)	90 OHM	75 OHM
MEASURED PIN RESISTANCE--SIGNAL --POWER	20 MILLI OHMS 20 MILLI OHMS	10 MILLI OHMS 3 MILLI OHMS
INTERCONNECT MEANS		
BACKPLANE	PRESSPIN ON .100 GRID	SURFACE MOUNT ON .050 CENTERS
MODULE	REFLOW SOLDER 300 PINS	GOLD ON GOLD CONTACT

B. SCHMIDT
7 APR 83
BS1.36

(Attachment #3)

BS1.25

| d | i | g | i | t | a | l |

INTEROFFICE MEMO

To: Distribution

Date: 23 February 1983
From: Bill Schmidt
Dept: Low-End VAX Systems Dev
Ext.: 229-6118
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::SCHMIDT

Subject: BI INTERCONNECT DESIGN REVIEW MINUTES--17 FEBRUARY 1983

Attendees: D. Lignos, B. Schmidt, F. O'Brien, B. Forgione, J. Mars, O. Tasar, N. Commo, P. Wade, D. Staffiere, J. Grady, B. Stewart, D. McInnis, J. Drew, D. Lick, K. Reilly, P. Chen, M. Titelbaum, T. Gent, D. Hurlbut, B. Mooney, D. Dunlap, B. Pedersen, A. Kantargis, B. Allison, R. Boudreau, R. Olson, N. Velez, E. Classon, R. Hanneman, J. Wardell, B. Mathrani, B. Weaver.

On 17 February 1983, a technical design review of the recommended BI interconnect hardware was held in Littleton. The meeting opened with some brief remarks by Bill Schmidt and then the floor was given to George Kitzman to present the developmental history of the BI connector and the preferred solution selected as satisfying the BI requirements both electrically and mechanically. Copies of his slides presented are attached.

The development effort headed by George as an A/D effort in Andover brought to ardware the response to a design objectives document authored by eorge Kitzman. The only respondant to this document with a connector atisfying all the objectives was Burndy Corporation with a zero inse on force (ZIF) connector. This connector has been developed and tested and is the proposed connector for BI. Burndy has also had a meeting with Winchester to exchange mutual intent in Winchester second sourcing the connector in production.

Bill Schmidt then presented slides (also attached) showing the connector and BI logic cage implementation for both top and side access. Data taken to date on electrical performance of the connector as well as test data accumulated in accelerated life testing was shown. It was pointed out that this life testing will continue to 1000 hours which is felt to simulate 10 years of extreme service.

During the presentation of this data, several comments and concerns were expressed. In summary:

- Demetrios Lignos asked about quality of tests run to date. Response was that the testing is only partially complete to the extent that is they will continue to 1000 hours and in scope. Ed Classon feels that nothing in testing done to date would prohibit endorsement by him from the Components Engineering perspective. Some spurious data needs further understanding and analysis but the bulk of the data is good and suggests a basically sound design.

- Questions were raised around the GTH contact as a reliable prodution interconnect. George Kitzman responded that he has had some six years experience with a previous employer using a GTH stacking connector. He has never seen a failure related to GTH contacts.

- Mike Titelbaum asked if there was a visual indication of connector position open or closed. Bill Schmidt responded that the actuator in the top entry implementation provided that but there was no such indication for side entry. This will be looked at.

- What other connectors looked at? AMP offered a system with the requisite number of pins but did not meet system electrical performance objectives and did not allow both side and top entry. As a backup strategy a complete logic cage design using this connector has been implemented and a true fall back could be made without significant (less than 1 month) schedule impact until near FCS.

- Bruce Weaver offered that for connector development, Burndy or Winchester is the best company to do such a task.

- Concern was raised over backplane and module thickness tolerance. Jim Mars responded that both quotes and verbal contact with outside board shops and with Greenville have not reflected concern on their part. Additionally, it was pointed out that the thickness tolerance on the backplane is required for impedance control and not connector related. The module tolerance and thickness is also a routing and impedance requirement.

- Ted Gent expressed concern that connector actuation testing should be done without a module in place to test a real situation and amplity stress related failures in this high stress condition. The point was well taken and such testing will be done.

- A suggestion was made to do accelerated life testing of unmated GTH contacts such as connector to I/O header interface. This is incorporated as an action item.

- It was pointed out that 1000 hours of accelerated life testing will be completed by 25 February. This is felt to be equivalent to 10 years of industrial service.

- Dick Dunlap recommends obtaining written quotations from DEC-Greenville for module manufacturing of MSL boards with gold pads.

- A strong recommendation from the floor was to have a viable backup strategy in place. This is done and is described above.

- One concern expressed on the accelerated life testing is the relationship of the testing to DEC experience. A simple way to solve this is to use a "standard" connector, such as a green block, as a reference and control in tests.

- Dick Dunlap suggested that a possible way to alleviate the fear of incorporating a new connector in a high volume product is to incorporate it into a low volume product early on to gain field experience. This is being considered.

Conclusions and Action Items

- Proceed with ZIF connector implementation as primary strategy.

- Maintain 2-piece (AMP) connector as backup strategy.

- Prepare comprehensive test plan and circulate for comments and suggestions from those with prior connector experience. Try to develop and understand MTBF model.

- Proceed with caution (lots of testing and evaluation).

BS:clc

Attachments

digital

Interoffice Memo

TO: BILL DEMMER

cc: *GORDON BELL
DEMETRIOS LIGNOS
JACK SMITH

DATE: TUE 19 APR 1983 1:20 PM EST
FROM: BILL JOHNSON
DEPT: SYS. AND COMM.
EXT: 223-3982
LOC/MAIL STOP: ML012-1/U29

MESSAGE ID: 5197337451

SUBJECT: BI PACKAGE

Should Demetrios drive this?

BJ

ATTACHED: MEMO;63

digital

Interoffice Memo

TO: see "TO" DISTRIBUTION

cc: see "CC" DISTRIBUTION

DATE: WED 6 APR 1983 5:33 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

MESSAGE ID: 5196017222

SUBJECT: A REAFFIRMATION OF THE BI PACKAGE

Ken has been especially unhappy with the BI in terms of schedule, package, and the fact that we have appeared to make decisions which overally favor the OEM (especially the European OEM) versus end user. I (and Ken) are delighted with BI's performance, RAMP, multiprocessor, large address and user features!

Given the TAI020 demise, now is the time to look at BI and reaffirm or change the direction vis a vis the packaging. In this note I don't want to get into the decision on it being a standard, or whether we license National to use the bus, or even whether we focus on being an end user versus OEM company, but only the technical questions:

1 Do we have the right sized module? Why not use a standard quad?
2 Why are we using such an expensive connector with so many conductors when BI was made to be so narrow? What module needs so many conductors? Why not use unique slots and connect the i/o there, or use a connector on the backpanel?
3 Why don't we use cables that come off the side or back of the module ala the old days? or why not extend the module so that i/o can plug directly into the back ala Pluto line cards or IBM's PC? These both look much more elegant and relevant to our use.

Basically, as a strawhorse, let me propose an alternative package which is quad form factor, uses both rear connection (ala the IBM PC), and allows front or direct cable connection ala our traditional (old) Unibus and Qbus... even though I don't expect we'll use this. Can we compare the strawhorse and the current BI in terms of:

. cost (at module and set of modules level),
. time to market impact,
. ability to make system of small, medium and large size,
. OEM desirability and market size impact,
. compatibility with existing box package sizes (eg. Qbus) and module manufacturing, NOTE WE ARE SURE TO HAVE A Q TO BI CONVERTER, GIVEN THE PLETHORA OF QBUS MODULES WE ARE BUILDING!)
. RAMP
. Ease of customer installability of module and cables.

We just have to bring this BI package to a close. Can we do it soon?

"TO" DISTRIBUTION:

BILL DEMMER BILL JOHNSON DEMETRIOS LIGNOS

"CC" DISTRIBUTION:

WARD MACKENZIE ROY MOFFA KEN OLSEN
JACK SMITH

%%

00[illegible] CORE DECGRAM ACCEPTED S 006190 O 660 06-APR-83 23:47:55

digital Interoffice Memo

TO: see "TO" DISTRIBUTION

cc: see "CC" DISTRIBUTION

DATE: WED 6 APR 1983 5:33 PM EST
FROM: GORDON BELL
DEPT: ENG STAFF
EXT: 223-2236
LOC/MAIL STOP: ML12-1/A51

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. RAMP
. Ease of customer installability of module and cables.

We just have to bring this BI package to a close. Can we do it soon?

"TO" DISTRIBUTION:

BILL DEMMER BILL JOHNSON DEMETRIOS LIGNOS

"CC" DISTRIBUTION:

WARD MACKENZIE ROY MOFFA KEN OLSEN
JACK SMITH

DL9.22

d i g i t a l

INTEROFFICE MEMO

To: George Champine

CC: Gordon Bell
Brian Croxon
Bill Demmer
Jesse Lipcon
Bob Magers
Roy Moffa
Pauline Nist
Mahendra Patel
Bill Strecker

Date: 2 February 1983
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::LIGNOS

Subject: COMMENTS ON THE BI MODULE PHYSICAL SIZE

Reference: Your memo, "Board Size", dated 28 January 1983.

George, I appreciate your comments and your concern over the BI module dimensions. Let me restate the results of our extensive studies that we believe justifies our decision to select the BI option module dimensions (9.187" x 8.00"):

1. First, I have attached for your information (Attachment A) a copy of a page from an earlier report that states the available Euro card dimensions (see Paragraph 4.4). Both dimensions (HB and DB) are variable. We have picked one of these dimensions (HB = 9.187") to be constant and upon it we have based the BI physical hardware interconnect (BI connector and backpanel). The other dimension (DB) is variable. As you know, we have picked 8" for cost control purposes in manufacturing volume production, but you can select another dimension up to 11.024" provided you design a new card cage. The Scorpio BI modules should fit in the new card cage because they are shorter.

2. The basic reasons, however, for picking a small size module as opposed to a large one are listed below. I want to emphasize that our first decision was whether a large or a small size module should be selected. Once we understood the first part of the question, then we compromised on the actual physical dimensions (the Euro size).

    a. Assuming that the packing density of the electronics remains constant with the longer board, the CAD tools (as we have discovered experimentally) will keep assigning additional layers per module as the complexity of the logic and control signals increases. If you restrict the number of layers, the CAD tools will "break" and the board cannot be laid out.

The larger the number of layers the more difficult the module fabrication becomes and the higher the cost (see Attachment B).

b. A very dense module with high power dissipation components requires adequate cooling. Since we are building the Scorpio pedestal system for the office environment, we have restricted the maximum cooling requirements per module at 50 watts. A longer module with the same density would require more cooling, that implies larger and noisier cooling fans (not conducive to the office environment).

c. The intent of Scorpio and MicroVAX based products (most of the BI options) are to be used in the board market. The cost of ownership for a small size module is less than a large module assuming high packing density of electronics. I don't really believe that anyone can argue that the functionality will remain constant on a larger size module. It is the nature of the hardware development groups that given a larger module they will find more things to put on so that they will constantly be running out of space. So the packing density of the electronics will remain high and so will the cost of ownership.

d. Our Field Service philosophy is to replace the damaged FRU as opposed to fault isolation and repair at the component level. The field repair float cost (according to Field Service) is definitely less expensive with smaller size modules. The MicroVAX based BI systems will be sensitive to such costs as they will impact customer service costs.

e. Electrically, there are clear advantages to the smaller module. The accidental flexing of a large module can cause hair line cracks or breaks on the etch (reliability issue). The smaller the module, the less the potential of such intermittent problems. Furthermore, the high density semiconductor technology we are now using as well as the technology of the future (even higher concentration of gates on a chip and lower level signals) will require the hardware designer to keep the device interconnect paths as short as possible (less capacitive) so that the interconnect delay is at a minimum to keep the transmission line behavior under control and minimize the cross talk. Consequently, the technology trend indicates increasingly higher physical packing density of components and interconnects per square inch. This trend in turn, points to small size modules for the future, in order to keep the technical difficulties (design and fabrication) as well as the cost per module down.

I personally feel that the way we are going with the chosen BI module dimensions, is the correct way. I am convinced that small module sizes are the way to go. The decision to use the Euro dimensions was indeed influenced by the board market but I believe the Euro

dimensions issue is a secondary one. Once we convinced ourselves that small size is the one to go with, we compromised with TVG since the difference between the standard quad size board and the Euro size that we picked is rather small. We could argue whether we should go back to the quad module in order to gain another inch in the width of the module. I don't believe, however, that going to a hex size module or larger will be a good technical decision for the next generation technology products.

I hope that my memo will cause you to rethink the factors that you listed favoring the present BI board size. I do think you are suggesting (indirectly) a change in the BI board format but I really don't believe that it would be a good idea at this point. Further, my suggestion is that you do not discard Rent's rule just yet. We have all been optimisitc at one time or another on pin and packing density requirements only to declare a "gross underestimation" of the complexities at a later time.

DL:clc

Attachments

Attachment (A)

4.3 What is our Competitor doing?

All our competitors, Intel, Motorola, and National are offering products based on the Eurocard form factor. The offering is done either direct or by cooperation with big companies, like Siemens in Germany. Next is a list of products offered today on Eurocard:

Intel/Seimens	8085
	8086
Motorola	6800
	68000
T.I.	990
Zilog	280
	28000

Even the microprocessors mentioned as 16 bit all our competitors have announced that their 32-bit products will use the same form factor either implemented by themselves or by an OEM, like Seimens.

In the past two months the new bus architecture VME, developed by Motorola, has got enormous publicity and is looked at as one of the standards for the future, and again VME is based on Eurocard.

4.4 What Part of the Eurocard standard is key to DEC?

The following list will show the key components of the standard DEC will have to implement to be compatible.

Board size:

	HB		DB	
DB	mm	inch	mm	inch
	55.55	2.187	100.0	3.937
	100.0	13.937	160.0	6.300
	144.45	5.687	220.0	8.651
	188.9	7.437	280.0	11.024
	233.35	9.187		

DEC has selected HB: 9.187" (233.35mm) and DB: 8.00". The reason for DB equal 8.00" and not 8.651 is related to cost saving in cutting raw material.

The European standard committee has approved our measurement 9.187" x 8.00" as long as our card cage is constructed to accept the European standard 9.182" x 8.651.

ATTACHMENT (B)

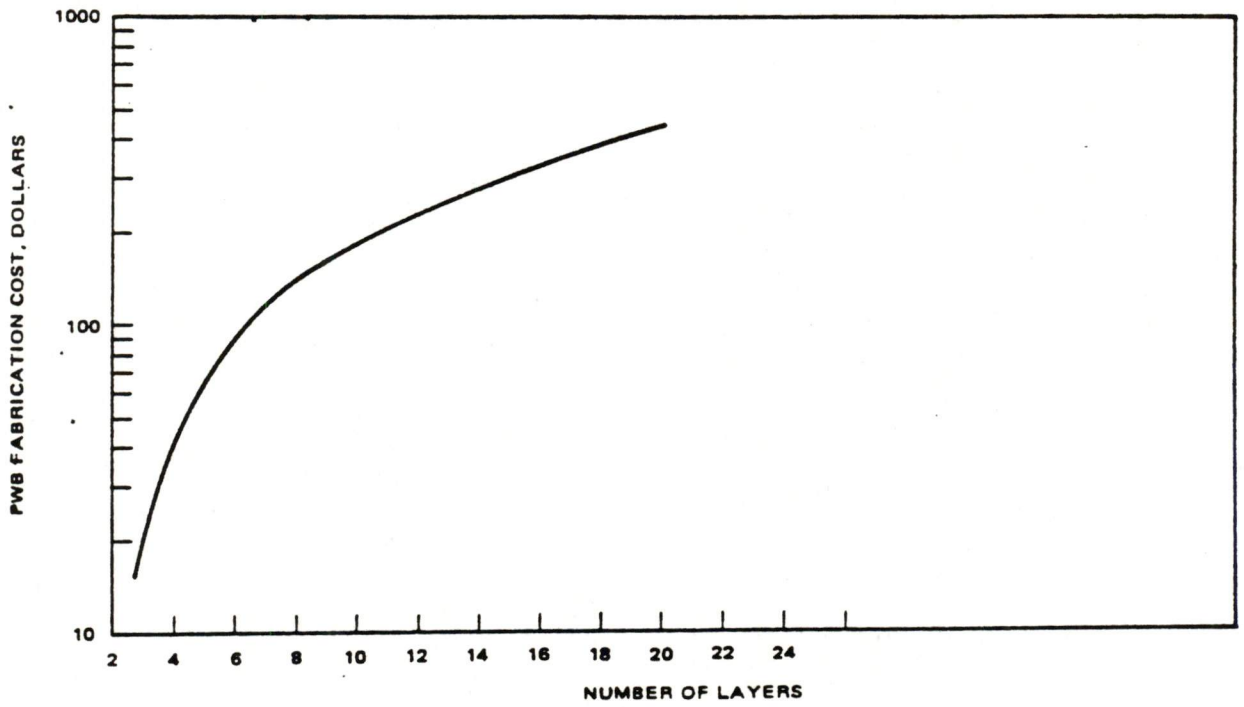

Figure 2-7. Printed wiring board (PWB) fabrication cost as a function of the number of board layers.

SOURCE: CONTRACT #NAS8-32607
WORKED PERFORMED BY:
INDUSTRIAL ELECTRONICS GROUP
HUGHES AIRCRAFT (FOR NASA)
15 OCTOBER 1979

OT4.35

| d | i | g | i | t | a | l |

INTEROFFICE MEMO

To: SSPO Members

CC: SSPO Alternates
Distribution

Date: 28 January 1983
From: Omur Tasar
Dept: Low End VAX Systems Dev
Ext.: 229-6119
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::TASAR

Subject: SSPO MEETING MINUTES --19 JANUARY 1983

Attendees: Demetrios Lignos, Kevin Reilly, Bill Laprade, Mike Titelbaum, Ken Meissner, Omur Tasar, Bob Willard, Tom Sherman, Doug Hanzlik, Paul Chen, Carl Blatchley, Herb Jacobs, Kaj Larsen

A. ADMINISTRATIVE ISSUES

The next SSPO meeting will be on 2 February 1983 in the Engineering Conference Room in Salem (SV).

B. AGENDA

1. PDP-11 Compatability Mode (Demetrios Lignos)

Demetrios said the issue of PDP-11 compatibility was once again on the table. Steve Teicher wrote a memo suggesting we take compatability mode out of Scorpio because it will cause several months of delay to the chip set availability and the I/E chip size increases beyond limits of achieving accepable yields.

Six months ago HL requested an ECO to the VAX architecture. The purpose at that time was to reduce the microcode development effort. The request was rejected at that time. Now that the impact is better understood on the I/E chip, the consequences of trying to include compatability mode are more severe.

Avram Miller supported Teicher's position, whereas Mike Gutman requested to understand the business impact. Tom Sherman has an action item to collect data from the product lines.

Herb Jacobs said one alternative could be to take compatability mode out of the hardware, but put it in software later. Software emulation can be made available after FRS time. It was added that both Seahorse and Microvax do not support compatability mode. Herb also said that one other alternative could be the addition of 2 microcode instructions to speed software emulation. Herb will discuss this with HL.

Bob Willard said that compatability mode is not a strong need for Scorpio. He said at this point he would rather use the microcode space for the NI boot solution.

Demetrios suggested we, as SSPO, recommend a position which supports the compability mode to be taken out because of a significant schedule hit and take the software emulator solution. Omur added that with the constraints on the I/E chip it may not even be doable even if we took the schedule hit. Mike supported the position with the provision that it was implemented in software. He said it could be decoupled from FRS.

Based on the above discussion, a SSPO position statement has already been published by Demetrios.

C. STATUS

1. Overall Program Status (Demetrios Lignos)

Demetrios made a presentation to Lou Gaviglia last Monday. So far, attempts to bring Salem up and ready for Scorpio manaufacturing support in a timely fashion have not been very effective. George Plowman supported Demetrios' position that additional resources and a dedicated organization were required to meet Scorpio's start up needs. All acknowledged that it takes 6 months to bring new people to a productive state. Demetrios believed that after 1 January 1983 for every month Manufacturing is delayed the program will be delayed. Salem has now permission to hire from outside. Also, Bud Dill acknowledges that the plant will be organized to support new products. Next Thursday Bud, George and Demetrios will meet. There are planned reviews with Lou Gaviglia every two weeks until the issue is resolved.

Demetrios said this month we will make a major decision on the BI physical interconnect. High level management including Ken Olsen has shown interest in the new style physical interconnect.

With BI packaging, we are defining the next 20 years physical interconnect. A process has been defined for the review and selection of the BI connector. A task force led by John Hittel will review the cost analysis. Another task force including senior level managers will review the rationale behind the decisions made. Dave Thorpe will function as the coordinator of the BI connector selection process.

2. AZTEC Status (Carl Blatchley)

Carl reported that the AZTEC deliveries to NEBULA, VMS and DMT labs have slipped because of the production problem still due to erasure. The engineering team is evaluating some design changes. They will need 6 weeks or so to implement the changes on the production units, which will make in-house availability of AZTEC's worse. The duration of the erasure problem caused the schedule to be reassessed. The FCS date may have to move out.

Demetrios asked whether we should continue to depend on AZTEC. Carl responded that his answer representing the Storage Group is "yes". Storage is not looking at alternatives. Mike asked whether this is affecting the AZTEC 2 schedule. Carl said that potentially it will not be affected.

3. System Hardware Development (M. Titelbaum)

Mike had reported problems with the byte aligner chip at the last SSPO meeting. The delay in the submission of this chip caused the accelerated schedule of BUA not to be viable, but we believe we can maintain the original schedule of BUA. Test bed will now be debugged with BIPASS and other tools in the absence of the BUA.

A meeting was held with the CAD group to understand how the design process effectiveness can be improved with the existing tools.

BIIC is moving along per the revised schedule. Layout is 90% done. Problems exist in the design verification process. Bob Willard added that DECSIM could use the checkpoint facility in VMS. This facility will be out by 15 February 1983 and it is not a piece of verified software. Nevertheless, if it can be used, it could provide substantial savings in turning around DECSIM BIIC simulation results. Mike will suggest Tony Hutchings to get together with Clark D'Elia. First PG for BIIC is still planned for 5 March 1983; first silicon in 20 May 1983 assuming design verification problems can be resolved. In 4 to 6 weeks, we will have more accurate data on schedule.

The BI clock driver and receiver design is progressing at Motorola per the schedule.

Mike had a meeting with Mike Powell from TW on how he can be helpful in the DVT and DMT process. Ken asked Ellery to be involved.

The System Development Group interviewed a technician. They are still looking for a designer and a microcoder.

4. Hudson Status (Bill Laprade)

At the AFL quarterly it was announced that the I/E chip took a 3 week slip and the M chip a 5 week slip from the original schedule. It is not clear, however, as to how the backend of the schedule is affected. In the next 4 to 6 weeks, the team will understand if there are any areas where the complexity has been underestimated and how reliable the rest of the schedule is.

Microcode development and module development had 2 weeks slip. Bill is still planning to submit his first gate array on 20 January 1983.

5. TAT020 Status (O. Tasar)

Omur explained that there were several meetings with TI. The regular technical meeting was held in Colorado, where a set of specific action items were generated for TI.

On 14 Janaury, we met the new management team of the Customized Components Division. Logic Arrays are now under a brand new division in the R & D group. The new management is a mature team who have sincere intentions to support DEC in all its needs. They assured us that all delinquencies to DEC will be taken care of. One such issue was a need for a dedicated DEC program manager at TI. They assigned Gary Westbrook solely to support DEC. The second issue has been getting good silicon in WOMBAT. So far they ran 4 lots on WOMBAT; 2 with 15K material and 2 with 10K material. TI will prepare a tecnical report on the problems they had with WOMBAT. TI has named the second source to DEC program office. We are planning to visit the second source at the end of February.

We are cautiously optimistic about the responsiveness of the new group and we feel our needs will be addressed in a timely fashion.

6. Manufacturing Status (K. Meissner)

The Scorpio pert will be ready at the end of January. This is a very detailed pert.

Ken found additional memory for the Scorpio machines in LTN. He said they will be shipped from Salem this week.

The resource planning that was generated bottom up in Salem shows that Scorpio will need 45 people at the end of FY83. Ken said they will scrutinize the numbers.

Jerry Jeansonne determined what needs to be done for L200 test process, but he does not have the actual resources to do the tasks. Marv and Ken are evaluating an alternate test strategy to L200. The decision to pursue an alternative will be made by the end of February.

7. VMS Status (Herb Jacobs)

Version 3.2 is now shipping.

As far as VMS is concerned the NI boot issue is closed. Bob Willard added that there is still the issue of microcode space and resources to implement the code are nonexistent.

Herb said the BSA/BDA issue was still open. Based on the latest information from Colorado, we told Herb that BDA support should be made available at Scorpio FRS time. BSA is still an open issue because what is needed (4MB throughput) and when (Q3 FY85) are in conflict.

We also reminded Herb that SSPO's formal position was to ask VMS support on the BI LESI and Unibus LESI at FRS time. Herb will check if they need to support MFA module.

8. CSEE Status (Doug Hanzlik)

Doug explained that there is a problem with the customer installability of the VMS products. Basically, the problem is a definitional one, of what constituted customer installability of software. VMS tended to think that once the system was built and booted, that was enough. CSSE wanted to go one step further and do some "coarse tuning" for the customer and insure that the applications packages (layered products) could also be installed. Herb asked for a list of requirements describing and defining what was needed. Doug reported that he will get this information. However, the group responsible to provide the list would like to wait until they have field test results with the 730 system in April.

Two SSPO members were not present at the meeting, but provided their status information:

1. Power/Packaging Status (Bill Schmidt)

We have received the AMP connectors. Burndy is delivering their parts today. Testing and evaluation of the connectors started at an outside lab. The review date and process will be announced next week.

The Macro-packaging Group has started to build parts for the sheet metal engineering model. The height issue is being resolved. Mark Kopeke is understanding the USA and European compatability of the pedestal height.

2. Memory Status (Dave Hurlbut)

On the data path gate array, SUDS type errors are being cleaned up. The design is near completion. It should be just about complete at the end of this week. Dave will set a design review for the data path gate array within a week.

A meeting was held between Memory Manufacturing and Salem Manufacturing and Memory Engineering to review the overall status. The dialog was good and no major problems were identified. The preliminary test flow for the memory module was one of the items reviewed. Quality goals were also reviewed. Jim McWilliams, Ellery Willett and Rubin Soto attended the meeting.

D. AGENDA FOR THE NEXT SSPO MEETING

- Status

OT:clc

SSPO MEMBERS

Carl Blatchley	MLO1-3/U6	223-3764	CACHE::BLATCHLEY
Paul Chen	LTN1-2/F15	229-6378	OBLIO::PCHEN
Duane Dickhut	HLO1-1/S11	225-4941	CHIPS::DICKHUT
Doug Hanzlik	LTN1-2/D07	229-6160	PHENIX::HANZLIK
Dave Hurlbut	MLO21-4/E10	223-5349	ZEUS::HURLBUT
Herb Jacobs	ZKO1-1/D42	264-8451	STAR::JACOBS
Kaj Larsen	HLO2-1/O05	225-5409	OBLIO::LARSEN
Demetrios Lignos	LTN1-2/F15	229-6116	OBLIO::LIGNOS
Ken Meissner	SVO	261-3215	OBLIO::MEISSNER
Kevin Reilly	LTN1-2/F15	229-6072	OBLIO::REILLY
Bill Schmidt	LTN1-2/F15	229-6118	OBLIO::SCHMIDT
Tom Sherman	LTN1-2/F15	229-6117	OBLIO::SHERMAN
Omur Tasar	LTN1-2/F15	229-6119	OBLIO::TASAR
Mike Titelbaum	LTN1-2/F15	229-6120	OBLIO::TITELBAUM
Bob Willard	LTN1-2/F15	229-6139	OBLIO::WILLARD

Alternates

Clark D'Elia	ZKO1-1/D42	264-8615	DELPHI::DELIA
John Forde	MLO1-3/U7	223-3516	CACHE::FORDE
Ted Gent	LTN1-2/D07	247-2531	OBLIO::GENT
Bill Johnson	HLO1-1/S11	225-4961	CHIPS::JOHNSON
Jim McWilliams	SVO	261-3239	OBLIO::MCWILLIAMS
Nelson Velez	LTN1-2/F15	229-6137	OBLIO::VELEZ

For Information Only

Peter Barck	LTN1-2/F15
Gordon Bell	MLO12-1/A51
Joel Berman	VWO1-1/C11
Dileep Bhandarkar	LTN1-2/H07
Corinne Chumsae	LTN1-2/F15
Larry Coppenrath	ZSO
Bill Demmer	LTN1-2/G09
Bud Dill	SVO
Ian Evans	HLO2-1/O05
Dan Haley	MLO21-2/E64
Brian Hannon	LTN1-2/F15
Marv Horovitz	SVO
Peter Jessel	LTN1-2/H04
Ann Katan	LTN1-2/F15
Bob Kugler	SVO
Pauline Nist	LTN1-2/D03
George Plowman	SVO
Barry Poland	LTN1-2/F20
Ernie Preisig	LTN1-2/F20
Sharon Sambursky	SVO
Linda Sarles	HLO2-1/C10
Chris Shatara	LJO
Bill Strecker	LTN1-2/H07
Lou Tancredi	APO-2/C4
Steve Teicher	HLO2-2/N07
Ellery Willett	NIO/N9

Please contact Cindy Cue, Ext. 229-6115, for changes to this list.

Date: January 1983

BI OPTION STATUS MONTHLY REPORT
(Prepared By: D. Lignos)

BI Option	PEG Mgr	Eng Mgr	Req'd FCS	Planned FCS	Comments
1) KDZ11 (Scorpio CPU Module)	S. Teicher	D. Dickhut	FY85	FY85	In development.
2) BI Memory	G. Saviers	P. VanRoekens	FY85	FY85	In development.
3) BUA	B. Demmer	D. Lignos	FY85	FY85	In development.
4) BI LESI	B. Demmer	D. Lignos	FY85	Not Committed	In development (not funded in FY84)
5) BI MFA	B. Demmer	D. Lignos	FY85	Not Committed	In development (not funded in FY84).
6) B5A	B. Demmer	B. Strecker	FY85	Not Committed	BI option for MicroVAX primarily. (Storage/Comm interface module.) Development has not begun. Not funded.
7) BI COMM	B. Lacroute(?)	Not Assigned	FY85	Not Committed	Development has not begun. (Preliminary spec exists.)
8) BNA	B. Lacroute	D. Rodgers	Not Clear	Not Committed	Development has not begun. Option required by Nautilus.
9) BCA	B. Demmer	G. Hoff	FY85	Not Committed	Development to start soon (not funded in FY84).
10) BDA	G. Saviers	T. Burniece	Not Clear	FY85	Development has begun (UDA functionality).
11) BSA	G. Saviers	T. Burniece	FY85	Not Committed	Delayed due to funds and resource limitations. Option required in FY85 by Nautilus.
12) BI Microvax CPU	Not Clear	Not Clear	FY85	Not Committed	Development has not begun

DL8.14

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INTEROFFICE MEMO

To: Distribution

Date: 23 November 1982
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15

Subject: BI OPTIONS DEVELOPMENT PLANS (REV 1)

This document is revised to reflect my misunderstanding concerning the status of the BSA. According to Grant Saviers, the BSA project is a funded and committed product. What is not clear at this time is its functionality and performance requirements.

Category 1: Funded and Committed

A. Scorpio CPU Module (KDZ11)

Scorpio (V-11 based) CPU module. This single module FCS is scheduled for Q1 FY'85. The responsible development engineering group is located in Hudson.

Responsible Engineering Manager: Bill Johnson

B. Scorpio Memory Module

An 0.5 megabyte (assuming 64K chips) or a two megabyte (assuming 256K chips) memory module being developed by Storage Engineering in Maynard for the Scorpio CPU. This single module FCS is scheduled for Q1 FY'85.

Responsible Engineering Manager: Ron Given

C. BI-to-Unibus Adapter (BUA)

This option is being developed in Littleton (32-Bit Systems Engineering). The function of this module will be to facilitate immediate utilization of existing Unibus options for BI systems and to provide a smooth migration from Unibus to BI only systems. This single module FCS is scheduled for Q3 FY'85 which is the Scorpio system FCS date.

Responsible Engineering Manager: Brian Hannon

D. BI-to-Ethernet Adapter (BNA)

The function of this option will be to interface the BI only systems to the NI (Ethernet) connection. This option is being developed in addition to the NI port (Lance chip) that will be available on the KDZ11 module itself.

The development of this module is expected to begin in Q3 FY'83 by Distributed Systems in Tewksbury. This single module FCS is scheduled for late FY'85.

Responsible Engineering Manager: Tom Ermolovich

E. BI-to-SI Adapter (BSA)

The function of this option will be to interface mid-range and high end storage devices (disk and tapes) to the BI. The development is in the functionality proposal stage. The developers are the Storage Engineering Group in Colorado. The present estimate is for a two module option in order to include the preferred functionality. The proposed FCS is for Q1 FY'86 but efforts are being made by Colorado Engineering to move the schedule back to FY'85.

Responsible Engineering Manager: Bill Mathrani

Note: In addition to the above list of BI option modules, the BI chip set (BIIC) will also be available in Q1 FY'85 for purchase. The BIIC will become public with full documentation in time for the Scorpio board and chip products FCS date.

Category 2: Unfunded and Uncommitted

A. BI-to-LESI Adapter (BI LESI)

The function of this module will be to interface Storage products (disks or tapes) that conform to the low-cost storage interface (LESI) protocol. Although officially unfunded in FY'83, the development of this option is progressing normally with a target FCS during first half of FY'85. We anticipate appropriate funding in FY'84. The module is being developed in Littleton.

Responsible Engineering Manager: Brian Hannon

B. BI-to-MFA Adapter (BI MFA)

The function of this module will be to provide low cost communications capability to BI based systems. The BI Multi-Function Adapter (MFA) is a programmable four line communications module and is being developed per the request of the Technical Volume Group (TVG) for the board market. Although officially unfunded in FY'83, the development of this option is progressing normally with a target FCS during first half of FY'85. We anticipate appropriate funding in FY'84. The module is being developed in Littleton.

Responsible Engineering Manager: Brian Hannon

C. BI Communications (BI COMM)

This module functionality is equivalent to the DMF32 module with a full complement of synchronous and asynchronous comm lines. The option is expected to be developed by Distributed Systems but the start of this development has not been planned as yet. Assuming that this module (project to be a single module option) is developed by Distributed Systems, the development will be done in Tewksbury by Dave Rodgers' group.

D. BI-to-CI Adapter (BCA)

The tentative development responsibility for this option is with the current VAX Group in Tewksbury. Due to other tasks within the group, no work has been started as yet on this option. Although I should mention that a CI chip set is currently being developed in Colorado and planned to be incorporated in the BCA single module option.

Responsible Engineering Manager: John Holtz

E. Additional BI Option Proposals

In addition to the above listed BI options, the following new options have been proposed. Due to the very recent surfacing of these proposals, however, the available information is very sketchy:

- BI DMZ (or BI-to-T1): DMF32 functionality on a BI board (DMZ to T1 to 24 line distribution panel).

- BI PBX: A BI version of the current CSS Unibus PBX interface.

- BI SYNCH MUX: A BI version of the current Unibus DH with modem control (looks like a DMF without the printer/DMA port).

- BI-to-IBM Ring Adapter: 4-8 lines with bit stuffing and IBM multi-drop capability.

- BI Encryption Adapter

The above information represents a "snap-shot" of the BI options development and planning status throughout the engineering groups involved in BI based systems. Please call me if you have any questions.

DL:clc

Gutmann, Jack Smith, Kalb, Strecker

NOV 19 1982

Note. This is NOT a winning plan for the BI (and VAX)!

DL8.9

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cc: This page Roy, BJ
Demmer, Ward, Ryan,

INTEROFFICE MEMO

To: Distribution

Date: 16 November 1982
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15

Subject: BI OPTIONS DEVELOPMENT PLANS

How can we get a good plan?
FU 12/3

In response to a general request for a brief summary of the BI options development plans, I have prepared this memo for your information. The BI options listed are divided into two distinct categories; those that are funded and committed and those that are not funded or fully funded to date and, therefore, not committed as deliverable products.

Category 1: Funded and Committed

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Responsible Engineering Manager: Brian Hannon

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Responsible Engineering Manager: Tom Ermolovich

Note: In addition to the above list of BI option modules, the BI chip set (BIIC) will also be available in Q1 FY'85 for purchase. The BIIC will become public with full documentation in time for the Scorpio board and chip products FCS date.

Category 2: Unfunded and Uncommitted

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Responsible Engineering Manager: Brian Hannon

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Responsible Engineering Manager: Bill Mathrani

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- BI Encryption Adapter

The above information represents a "snap-shot" of the BI options development and planning status throughout the engineering groups involved in BI based systems. Please call me if you have any questions.

DL:clc

JAN 24 1983

DIGITAL

TO: Scorpio Program Review Distribution

CC: Distribution

DATE: 18 January 83
FROM: Mike Titelbaum Mike
DEPT: LOW END VAX DEV
EXT: 229-6120
LOC/MS: LTN 1-2/F15
ENET: OBLIO::TITELBAUM

Subject: Scorpio Program Review Action Item Responses

The following is a response to the Action Items that were assigned to me at the November 30, 1982, Scorpio Program Review. Some of them will require further followup, and others should be considered closed by the clarifications stated below.

1. Issues on the 11/750 based BI testbed

The BI testbed provides a tool for developers of BI adapters and BI adapter diagnostics for partial debug of their designs prior to the availability of a BI CPU. The BI testbed is a VAX 11/750 with a custom designed interface between the CMI (COMET Memory Interconnect bus of the 11/750) and the BI. The CMI to BI Adapter (CBA) is soft microcoded to allow for timely correction of implementation errors or errors in the design of the BI or CBA. It will also allow for the generation of custom BI sequences including illegal commands or sequences for the unit under test. In addition, a BI backplane with associated power supplies is included for the unit under test.

The testbed will provide 3 software environments:

1. 11/750 console -- The console can be invoked to manipulate BI address space directly, manipulate registers or check primitive adapter functions.

2. 11/750 diagnostic supervisor with a CBA level 3 macrodiagnostic -- In addition to ensuring the CBA is operational and loading operational microcode, this environment provides a micro-routine utility for loading and running specific BI test sequences.

3. Modified 11/750 diagnostic supervisor -- makes the CBA transparent and allows level 3 diagnostic programs for these adapters writen for the SCORPIO environment to be run unchanged.

The BI testbed is NOT intended to provide hardware that emulates a SCORPIO BI CPU. Given current schedules for SCORPIO CPU availability, the BI testbed would not allow significantly shorter development time or significantly decrease the software development risk for CPU and BI specific VMS code. (See Dave Wells 9-Dec-1982 memo "Rationale for BI Testbed Implementation".) There is nothing in the current BI testbed design that precludes use of the BI testbed by VMS development. Therefore, in the event of significant schedule changes, the use of the BI testbed by VMS development can be re-evaluated. VMS development will be informed of any changes to the BI testbed as well as adapter and CPU changes so that they can accurately assess alternative strategies for the development of VMS support for SCORPIO systems.

We do intend to make at least two of these testbeds available in Littleton for use by the LTN and other BI adapter developers. We will have the system and its custom interface formally documented and maintained out of the systems engineering group.

2. VMS support of the BIMFA

VMS is not planning support of the BIMFA with any specific driver development. The BIMFA has an on-board programmable T-11 microprocessor which when programmed by the user will determine the precise device characteristics. There is some value in having a sample VMS driver available as was done for the DR780. Such a skeleton driver is not a gating item for BIMFA shipment.

It is far more important for Seaboard to have a skeleton driver, than it is for VMS, since the BIMFA is viewed as far more important to Seaboard users than VMS users. Seaboard is not currently committed to a skeleton driver, but some interest has been expressed, (awaiting hardware development commitment).

The skeleton driver should include: the sample driver, the sample T-11 code, at least
one sample load mechanism used by the driver to load the T-11 code into the MFA, and some sample DCL procedures to create the driver and the T-11 code. Supporting documentation and inclusion of the BIMFA in the debug tools would also be required.

We will pursue this with the Seaboard development team.

3. NO Scorpio MP FRS date

Our plans have always been that Scorpio MP configurations are upgrades to uniprocessor configurations and that in many cases we would expect that many of the Scorpio OEM customers would order an additional processor option and create the MP configuration themselves. As part of the Scorpio Systems DVT plans we expect to DVT both Single and Multiprocessor Scorpio configurations prior to uniprocessor System shipment with VMS and Seaboard. There will be a very tight schedule to do this prior to Scorpio Board and Uniprocessor system FRS. From the Scorpio/ BI hardware perspective though there still is curently no hardware differences between a single processor Scorpio CPU and a Scorpio CPU used in an MP configuration. (Primary and attached processor determininations are made when the systems package is assembled and EEPROM code is modified on the appropriate CPU board. Predefined backplane pins will enable or disable functions for the primary and attached processors.)

As part of the early FY84 planning process we have seperated out a Scorpio Systems MP project and will have identified an individual who will be the MP project engineer focused specifically on MP configurations. We have also planned shipments of Scorpio MP systems configured in MFG for Q4 FY85, one quarter after Scorpio Uniprocessor Pedestal and OEM box system shipments. This target will now be rolled up in the Software, Diagnostic, Mfg. and CSSE planning to verify Q4 FY85 for the DEC configured MP ship date.

4. Where does the TOY reside?
(The following is taken directly from the Scorpio Systems Spec)
"2.1.7 TOY (Time Of Year) Clock

Implementation of the TOY clock is split between the Scorpio processor module and the front panel sub-assembly. The M-chip of the processor module includes the 32-bit binary counter which is incremented every 10 milliseconds; this register is not incremented during power outages.

The clock module (part of the front panel subassembly) contains a crystal oscillator and a watch chip (HH:MM:SS etc., format) which is incremented every second and which has local battery (Ni-Cad) backup. This watch chip is connected to the primary processor via PCI (Port Control Interface), and is read/write accessible in I/O space. This module includes a detector for loss of battery power which is also available in I/O space.

It is the responsibility of the operating system, when the system is started or restarted, to read the clock module and back calculate a value for the 32 bit binary counter. Since the clock module is connected only to the primary processor, the TOY clocks in attached processors will be useless (unless the operating system initializes their TOY clocks as well).

Since the front panel, including the clock module, is included with every Scorpio system, all DEC-built Scorpio systems will have a battery backed up TOY clock. OEM-built systems may be created without this capability."

This implementation partitioning was arrived at as a VLSI M-chip design risk minimization as well as a KDZ Scorpio CPU board layout risk minimization. Originally the VLSI plan was to partition the M-chip such that the section of the chip containing the 32 bit TOY counter would be powered from a separate supply line (TOY battery or switched power) from the rest of the M-chip power lines. The oscillator circuitry outside of the M-chip would also have separated TOY supply line power. The circuit design risk of guaranteeing operation of the M-chip (this design has not been done previously) was reduced by moving the circuitry to be backed up off the M-chip and onto the KDZ board. The complete circuitry including oscillator, clock chips, battery low detection circuits and the battery would not fit in total on the KDZ board, and the decision was made to partition the circuitry between the KDZ and the system front panel.

The actual oscillator and clock design circuitry including timer/counters, the battery and voltage low detection circuits will be lifted from the CT design directly. We believe that this is the best engineering compromise to guarantee the VAX TOY clock for Scorpio as specified in the VAX SRM. (We may want to offer the front panel or subassembly of the front panel to module level customers who want the complete backed up TOY clock.)

5. Why support PDP-11 on Unibus? What are the implications?

The main reason for supporting PDP-11 on the Unibus side of the Scorpio BUA is to provide a standard software and hardware migration path for existing PDP-11 Unibus OEM customers who will not be able to immediately either move their software to Scorpio and retain their investment in their own as well as DEC's Unibus interfaces or immediately be able to develop equivalent BI adapters to replace or upgrade their existing Unibus I/O interfaces. (Neither VMS nor Seaboard is expected to support this capability, nor is any DEC software for PDP-11's expected to support this capability).

We have received inputs from Schlumberger, a large PDP-11 OEM, who wants to migrate their real time PDP-11 applications (hardware and software) to Scorpio/BI and the VAX family of processors. Schlumberger, like many other PDP-11 real time OEMS, wants Scorpio initially, as a backend real time data analysis and data reduction machine until they have have their new hardware and software developed.

Having a PDP-11 on the Unibus side of the Scorpio BUA gives them the opportunity to evolve their real time systems and use Scorpio/BI early rather than redesign both hardware and software (since most of their software is real time code optimized for their application and is not directly translatable into VAX compatibility mode). This capabiltiy is of substantial value to them. Their alternatives would be to use a Unibus Window adapter module set (most are technologically and physically obsolete), design their own window module and they have even considered buying BI and J-11 chips and building a J-11/BI system that would buy them time to fully utilize Scorpio/BI in their applications. Other links between the PDP-11 and Scorpio were considered (NI, Serial line, etc.) but were discarded due to slow response times for the real time applications.

Mike Gutman believes that the Schlumberger model is the case for many of our current PDP-11 OEMS and that if we don't provide systems migration hooks from PDP-11/Unibus to Scorpio/BI, then many OEM's may find the migration hurdle too large and look to alternate solutions (other than DEC) for their current or future applications.

The implication of this capability is that the Unibus arbitration logic on the BUA will become programmable, from the Scorpio/BI side, to either have the BUA arbitrate NPR's and BR's or have a PDP-11 processor arbitrate the Unibus BR's and NPR's (in this latter case the BUA will issue NPR's and wait for NPG's before initiating transfers). The programmable arbitration as well as minimal status information will take up much less than 5% of the logic on the BUA and will have only minimal self test and diagnostic implications. In all cases control bits will only be programmable through the Scorpio/BI side and the PDP-11 processor will not be able to modify the BUA map registers or other BUA status bits . We are developing this capability in conjuction with Jesse Lipcon and Don Gaubatz in the 16 Bit Program Office, and have reviewed it with Rick Casabona and others. They concur with our approach. We do not expect VMS or Seaboard support of this capability, only diagnostic verification.

The 11/780 as well as the 11/750 incorporated equivalent circuitry to what we are proposing for the Scorpio/BI BUA. In the case of the 780 the Arbitration Master decision was made by actually swapping a board in the DW780. In the 750 the logic was designed in but was never enabled. (See the paper by Browne, Cranier, Sherden, Weaver "A PDP-11 Front End for a VAX-11/780," on the use of this capability in a system where an 11/04 was used as a real time data acquisition front end to an 11/780.)

DISTRIBUTION

Meeting Attendees
SSPO

John Adams	TWO/B12
Phil Arnold	CXO1-1/P13
Paul Bauer	MLO1-3/T62
Tom Burniece	CXO/Q21
Paul Chen	TWO/C04
Lou Gaviglia	ICO/G01
George Hoff	TWO/C04
John Holz	TWO/C04
Bill Johnson	MLO12-3/A62
Bernie Lacroute	TWO/A08
Bruce Ryan	LTN1-2/D08
Dave Rodgers	TWO/A08
Grant Saviers	MLO3-6/E94

ATTENDEES

Gordon Bell	MLO12-1/A51	Bob Kirk	CXO1-2/Q12
Dileep Bhandarkar	LTN1-2/H07	George Kitzman	APO1/F2
Carl Blatchley	MLO1-3/U6	Kaj Larsen	HLO2-1/A10
Frank Bomba	LTN1-2/F15	Chi Lau	WOO/D97
Kirk Bonner	GSO/E6	Ken Mamayek	MLO21-4/E10
Randi Brenowitz	LTN1-1/H10	Jim Mars	LTN1-2/F15
Reid Brown	ZSO	Bill Mathrani	CXO1-1/P13
Bob Burley	LTN1-2/B17	Don McInnis	LTN1-2/B17
Elaine Burke	SVO	Ray Mercier	HLO1-1/S11
Michael Callander	HLO1-1/S11	Roy Moffa	HLO2-1/B11
Joe Chenail	SVO	Peter Murphy	SVO
Bill Demmer	LTN1-2/H09	Al Nichols	VWO/C02
Joe Dunne	GA	Bob Pedersen	LTN1-1/D05
Ian Evans	HLO2-1/A10	Ernie Preisig	LTN1-2/F20
Bob Fallon	APO1/E2	Franco Previd	SVO
Mitch Federman	LMO2/P41	Kevin Reilly	LTN1-2/F15
Ted Gent	LTN1-2/D07	Bill Schmidt	LTN1-2/F15
Brian Hannon	LTN1-2/F15	Tom Sherman	LTN1-2/F15
Doug Hanzlik	LTN1-2/D07	Jim Stegeman	MLO21-2/E64
Marv Horovitz	SVO	Omur Tasar	LTN1-2/F15
Dave Hurlbut	MLO21-4/E10	Mike Titelbaum	LTN1-2/F15
Bill Johnson	HLO1-1/S11	Nelson Velez	LTN1-2/F15
Bob Johnston	ICO/D25	Paul Wade	LTN1-2/F15
Jim Kane	MRO5/O6	Joe Welch	APO1/E2
Ann Katan	LTN1-2/F15	Bob Willard	LTN1-2/F15
Sid Kimber	APO1/C15	Steve Zabinski	OGO1-2/S07

JAN 12 1983

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I N T E R O F F I C E M E M O

TO: ROY MOFFA

CC: SEE DISTRIBUTION LIST

DATE: 10 JANUARY 83
FROM: BILL DEMMER
DEPT: 32 BIT SYSTEMS
EXT: 229-6065
LOC/MAIL STOP: LTN01-2/H09
ENG. NETWORK NODE: PHENIX

SUBJECT: THE BI MICROVAX PLAN

Attached is a copy of the latest project plan for the BI MicroVAX System. This plan is intended to be responsive to the need of extending BI based 32 Bit Systems below Scorpio multiuser systems into the sub $20K entry price area.

During at least the FY84 - FY86 time period it is expected that Q Bus based MicroVAX Systems will provide the lowest priced 32 Bit System in the Digital product line. Thus, the focus of the BI MicroVAX System will be primarily as a downward extension of our current and planned VAX family of systems.

We are actively seeking budget and manpower resources to move this program Advanced Development into Product Development. Your support for this effort and your suggestions for the program are welcomed.

"CC" Distribution (With Attachments)

Gordon Bell Mike Gutman Jeff Kalb
Jack Smith

"CC" (Without Attachements)

Bill Johnson Pauline Nist Bill Strecker

UVAX PROJECT PLAN

PRELIMINARY PROPOSAL

AUTHOR: Pauline Nist
32 BIT Architecture
and Adv. Dev
MAIL: LTN/H02
DTN: 229-6151
NODE: MIRACL

REVISION HISTORY:

VERSION 0.1	PRELIMINARY PROPOSAL	1 December 1982
VERSION 0.2	BUDGET AND TECHNICAL UPDATE	4 January 1983

APPROVALS:

Bill Strecker Group Manager

Bill Demmer 32-bit Systems

Roy Poffa uVAX Program Office

1.0 EXECUTIVE SUMMARY

This project plan describes the development effort necessary to produce a BI based UVAX system in a price performance band below that currently planned for BI based Scorpio systems. The principal engineering efforts involved in the project are:

1. Design of a UVAX CPU/MEMORY module. This module would be a Eurocard form factor and mount in the current standard BI backplane being planned for Scorpio systems. Memory would be done with 256K RAM and it appears that 1MB of local memory would fit on the module. Standard BI memory could be used for expansion memory. Ideally this module could also serve as a single board product for IVG.

2. Design of two new BI interface chips. These chips would be used along with the BIIC chip under development for Scorpio. While equivalent functionality could be provided with TAI20 gate arrays, the custom chips have been chosen in order to bring down the cost of the BI interface. One is of moderate difficulty, while the other is low-medium difficulty. These chips are not unique to this design and could be used by other projects desiring to interface to the BI.

3. Design of a BI based "COMBO" module that would provide a Winchester disk interface (using an industry standard disk interface) an NI port (using the planned DEC NI chip set) and parallel and serial lines. The major justification for this module is the goal of a low total system price, which is difficult if standard BI modules are used for this functionality. This module is also Eurocard form factor.

4. Either buyout of an appropriate power supply (for BI voltages) or design of a new supply based upon much of the hybrid work done for the Scorpio project. Because of time to market and cost the buyout is favored but securing a supply with all the BI voltages may be a problem.

5. Modification to some set of existing packages to produce both an office pedestal and an OEM package. Ideally the cooling for the 6.25" box could be improved adequately for our needs without becoming too noisy for the office environment, and would also work in the rack mount OEM market. Worst case a slightly larger pedestal (8-1/2" wide) would be done for the office and a separate OEM box would become products. Even in this case much of the

effort would lever off of the Scorpio and LCP work.

6. Acceleration of plans for a high density (greater than 25MB) 5 1/4" hard disk, either through buyout or internal effort.

7. MicroVMS and Seaboard as available operating systems.

8. The product will be customer installable with customer runnable diagnostics.

9. Diagnostics to utilize the BI tester in the manufacturing process will be provided.

1.1 PROJECT ABSTRACT

The UVAX fulfills the need for:

1. A VAX system in the price performance band below Scorpio Systems.

2. A base system on which more competitive workstation products can be built.

3. A UVAX board product for the OEM market.

4. A OEM box product.

5. A low cost real time system (with Seahorse software).

1.1.1 PROJECT DELIVERABLES

The products that will result from this project plan are:

1. A UVAX System product consisting of a standard 5 slot BI backplane, a 1MB CPU module and a BI "Combo" board along with a high density (greater than 25MB) 5 1/4" disk, and a 5 1/4" floppy disk. These pieces would be housed in a quiet ergonomic package (a 6.25" or larger pedestal). The system would allow for use of either a standard VT type terminal(future product) or use of a high resolution graphics station as the primary system

terminal.

2. A 5 or 6 slot BI based OEM box.

3. A single CPU module with 1MB of memory (256K RAM).

4. MicroVMS or Seahorse as software products with the system.

1.2 SUMMARY OF GOALS

The primary goal is a small, lower cost, BI based VAX system, competitive with the market place at the time. Time to market is critical in that the system should be available consistent with availibility of the uVAX chip from Hudson. MicroVMS and/or Seahorse support are essential for First Ship. Since price is viewed as a key issue, all decisions regarding pheripheral support.,etc. will be viewed from the perspective of product cost. Target MLP for entry level system is less than $15K, with graphics workstation systems extending upward into the $16-30K range.

NON GOALS

The product should not interfere with the SCORPIO product plans. It is not essential that uVAX be extensible into the middle of the SCORPIO price band. Rather it is a low end, bounded VAX entry system that is BI compatible. Product cost is held down by constraining power and packaging, along with bounding the system.

PHASE	DATE
PHASE 0	TBD
PHASE 1	TBD
PHASE 2	TBD
PHASE 3	TBD
PHASE 4	TBD
PHASE 5	TBD

NOTE: ALL SCHEDULES SUPPLIED ASSUME THAT STAFFING REQUIREMENTS OUTLINED IN THIS PROPOSAL ARE APPROVED, ALONG WITH ADVANCED DEVELOPMENT SCHEDULES FOR THE BI CHIPS.

1.3.1 POWER AND PACKAGING SCHEDULE

MILESTONE	DATE
START FEASIBILITY A.D.	1/1/83
SURVEY PWR VENDORS	1/1/83
DECISION ON BUYOUT VS INTERNAL PWR SUPPLY	4/1/83
DECISION ON PKG STRATEGY (ONE VS TWO PKGS)	4/1/83
PRELIMINARY PACKAGE DESIGN	7/1/83
MOCKUP PACKAGE PARTS	8/15/83
ASSEMBLE/DEBUG MOCKUP	9/15/83
EVALUATION OF MOCKUP	9/30/83
ORDER DVT AND PROTO PKG PARTS	10/30/83
PRELIMINARY PWR DESIGN	10/30/83
BREADBOARD PWR SUPPLY	1/1/84
DEBUG PWR SUPPLY	3/1/84
ORDER DVT AND PROTO PWR PARTS	3/1/84
DVT MATERIALS AVAILABLE	5/1/84
ASSEMBLE DVT MATERIALS	5/15/84
PWR PROTO BUILD	5/15/84
DVT TESTING COMPLETE INCL DEC 102 ETC	7/15/84
DRAWINGS COMPLETE BEGIN LP	7/15/84
PWR PKG UNITS AVAILABLE FOR DMT	10/15/84

1.3.2 CPU MEMORY MODULE SCHEDULE

MILESTONE	DATE
START DESIGN	3/1/83
PRELIMINARY DESIGN COMPLETE	8/1/83
START BACKPLANE EFFORT	8/1/83
START LAYOUT	9/1/83
PROTO BACKPLANE AVAILABLE	1/1/84
PROTO BOARDS AVAILABLE	1/1/84
FIRST PASS UVAX CHIPS	1/15/84
DEBUG WITH SCORPIO PWR SYSTEM	3/15/84
SECOND PASS UVAX CHIPS	5/15/84
FINALIZE BACKPLANE	6/15/84
SECOND PASS LAYOUT	7/15/84
SECOND PASS PROTO MODULES	10/15/84
BACKPLANE PROTOS AVAILABLE	10/15/84
MODULE DVT STARTS	10/15/84
DVT OF BOARD AND PKG STARTS	10/15/84
FINISH DVT	12/15/84
START LR TO MFG	1/1/85
COMPLETE LR TO MFG	2/1/85
DVT COMPLETE	4/15/85

1.3.4 BI "COMBO" MODULE SCHEDULE

MILESTONE	DATE
BEGIN DESIGN	7/1/83
PRELIMINARY DESIGN DONE	1/2/84
START LAYOUT	1/15/84
PROTO BOARDS AVAILABLE	4/5/84
START DISTRIBUTION PANEL	4/5/84
DEBUG ON SCORPIO SYSTEM	4/15/84
SECOND PASS LAYOUT STARTS	7/5/84
PROTOTYPE DISTRIBUTION PANELS	7/5/84
DEBUG WITH UVAX	7/15/84
BEGIN DVT	9/15/84
SECOND PASS BOARDS AVAILABLE	10/15/84
FINAL DISTRIBUTION PANEL	10/15/84
BEGIN DMT	10/15/84
FINISH DVT	10/30/84
BEGIN LR TO MFG	11/15/84
FINISH LR TO MFG	1/15/85
DMT COMPLETE	4/15/85

:

1.3.6 BI CHIP SCHEDULE

MILESTONE	DATE
BEGIN DESIGN BC3I IC (A.D.)	10/1/82
PG TAPES TO HUDSON BC3I	1/15/83
BEGIN DESIGN BI3 IC	1/15/83
PG TAPES TO HUDSON BI3	5/15/83
FIRST PASS WAFERS BC3I	5/15/83
FIRST PASS WAFER DEBUG COMP BC3I	8/15/83
SECOND PASS PG BC3I	8/30/83
SECOND PASS WAFERS BC3I	11/15/83
LIMITED RELEASE BC3I	1/5/84
FIRST PASS WAFERS BI3	9/15/83
FIRST PASS DEBUG COMP BI3	12/15/83
SECOND PASS PG BI PG	1/5/84
SECOND PASS WAFERS BI3	3/15/84
LIMITED RELEASE BI3	5/15/84
START QUALIFICATION BC3I	2/15/84
START QUALIFICATION BI3	7/15/84
QUALIFICATION COMPLETE BC3I	6/15/84
QUALIFICATION COMPLETE BI3	12/15/84

NOTE: This work has currently begun in 32-bit Advanced Development and their plan should be consulted for further details.

1.4 RELATED PROJECT DOCUMENTATION

1. MicroVAX CPU Chip Development Plan DC333 REV 2.0
2. SCORPIO SYS DEVELOPMENT ENG. PLAN REV 0.2
3. BI Interface Chip Spec. REV 1.2
4. A Low End BI uVAX System 1/4/82 Peter Jessel
5. SCORPIO PROGRAM REVIEW 30 NOV. 1982

2.0 PROJECT GOALS

The project goals for BI UVAX are:

1. Entry level system price (MLP) of $16K (without graphics terminal).

2. Time to market consistent with UVAX CHIP Schedule

3. BI interface cost that is competitive with other DEC buses.

4. Compatible with other BI systems offerings.

5. Complements rather than competes with SCORPIO system offerings.

6. Low cost interface to Ethernet.

7. Storage system is compatible with office ergonomics and tracks technology curve. Interface should be easily upgradable to newer storage devices.

8. Compatible with all reasonable (for this price band) BI options.

9. System is customer installable with customer runnable diagnostics.

10. CPU board is acceptable as volume board product.

11. Supports standard DEC terminals.

12. Configurations are bounded for cost control.

13. Ergonomic package.

14. Board set is packaged in OEM box.

15. Provides base system for integrated workstation.

2.0.1 PROJECT DEPENDANCIES

This project plan requires key efforts from other parts of the company. They are:

1. That Hudson provide first and second pass uVAX chips on the schedule published in the uVAX Chip Project Plan.

2. That VMS provide an operating system with appropriate device support.

3. That Seahorse provide support for the BI and necessary options.

4. That Storage Systems accelerate plans for a high density 5 1/4" hard disk. The preference is for an industry standard controller interface. Current input indicates that greater than 25MB disks should be available in volume from various vendors.

5. That Storage Systems qualifies 256K RAM vendors on an appropriate schedule.

6. That both Diagnostics and Power and Packaging resources are put in place in a time frame that supports the overall schedule.

7. That Distributed Systems in conjunction with AMD and MOSTEK provide the MI chip set on schedule.

8. That the 32-bit Advanced Development BI chip effort continues, and that some low risk process is put in place to evolve the effort into a full scale chip design project, with appropriate production support from Hudson.

9. That manufacturing provide support early on to permit qualification of both the board and system level products on an agressive schedule.

10. That VMS product management provide creative approaches to permit licensing of the microVMS software at costs competitive with other micro processor based operating systems.

11. That Workstations provide and integrated video module that is BI compatible.

2.4.2 RESPONSIBILITY CHARTS

TASK	DRI
Architecture	D. Bhandarkar
VMS	D. Huseyedt
Hardware Engineering	B. Strecker
BI Chips	P. Jessel
Packaging	D. Staffiere
Manufacturing Support	TBD
Diagnostics	D. Auenschel
SCAPOARD software	D. Cutler

UVAX CHIPS	B Supnik
UVAX PROGRAM	R. Moffa
Video Module	B. Croxon

2.0.3 OPEN ISSUES

Because this is a preliminary proposal there are still many issues that need investigation and direction. They include:

1. What is the product impact of using only 5 rather than 6 slots of the BI backplane, which could save both power and packaging dollars?

2. Should the NI interface be on the CPU module or the BI combo board?

3. Do we entirely understand the risks associated with two additional BI chips? What is the fallback?

4. What combinations of serial and parallel interfaces should be on the "Combo" module?

5. What is the possiblity of staffing critical positions in Q3 and Q4 of FY83? What is the impact to schedules if this is not done?

6. Is there any need or desire to ever offer the microvax CPU module in the Scorpio package? What effect does this have on product mix and markets?

7. Is the CPU/MODULE set acceptable to workstations?

8. Is the CPU module acceptable as a board product?

9. Is and industry standard interface to a high density winchester (5 1/4") the right approach?

10. How much (greater than 25-6) disk is really the right amount? (40-60Mb?).

11. Is floppy the preferred second perioherial? Is streaming tape more appropriate in this market or is the interchangability of floppies a plus?

12. What is the impact of a pedestal vesus desktop/pedestal package?

13. What is the schedule for the floating point co-processor chip?

14. What additional BI configurations, that require additional cabinetry (eg: BI-LESI to two AZTECS) will be permitted? What does the cabinet profile look like?

15. Is battery backup necessary in this market? at what price?

16. Should the product support the BI-CI adaptor(BCA) or will we push the Scorpio product in that market?

17. Is there a need for a low end system with only 256K of memory and a cheap (only 5-10MB) disks?

Note: Additional items and comments welcomed

2.1 DESIGN GOALS

1. BI compatible

2. Single Eurocard CPU module with 1 MB of 256K RAM memory

3. Single Eurocard BI comoo module with NI chip set,industry standard controller for floppy and hard 5 1/4" disk and misc serial/parallel lines.

4. Full implementation of BI support on BIIC chip plus two additional chips.

5. Ergonomically and acoustically acceptable package for the office environment(between 5.5-5.9 Bels).

6. Rack mountable OEM box.

7. Single CPU module should satisfy needs of board market.

2.2 TRANSFER COST ESTIMATES

TOTAL SYSTEM	FY85 COST
CPU w/1MB memory	1308.5
BOX + PWR	910.00

Patch Panel	100.00
RD (25+MB) w/ctl	1300.00
RX	225.00
MODULES:	
BI COMBO	827.50
MFG value added	200.00
TOTAL	4871.00

Note: Video module/s to be supplied at a later date.

CPU w/1MB memory

uVAX chip	214.00
BI3IC chip (BI to II)	85.00
BI clock + transciever	40.00
Hi density sockers	24.00
misc components	25.00
Misc hardware	10.00
P.C. Board	100.00
Misc Material	50.00
1MB Memory	648.00
Buffers	37.50
Memory ctl	75.00
TOTAL	1308.50

BI COMBO

NI protocol chip	30.00
NI driver chip	10.00
Winchester ctl chip	40.00
phase lock loop int	30.00
uVAX microprocessor	214.00
local memory	64.00
parallel interface	60.00
Multiprotocol serial line	7.50
misc support logic	75.00
P.C. board	100.00
BCI3 chip	50.00
BIIC	137.00
BI clock xcvr	10.00
TOTAL	827.50

POWER AND PACKAGE

Modified LCP/pedestal bo	360.00
Power 300-350W	350.00

Backplane and connectors (5 slot BI)	200.00
TOTAL	910.00

2.3 MAINTAINABILITY

The basic strategy for BI based uVAX systems is customer maintainebility. While field service contracts should be available for volume users, the goal will be for self test and customer runnable diagnostics everywhere. For spares a variety of solutions should be explored including mailers, over the counter service etc. All diagnostics should isolate faults to the module level.

2.4 RELIABILITY

Reliability targets will be published later in the project. Goals will be consistent with Scorpio BI systems and with other Digital Systems in this price band.

2.5 SERVICIBILITY

The field replacable unit will be the eurocard module. The goal is for all modules to have self test, along with customer runnable diagnostics that isolate faults to the board level in the field. Various methods of service must be explored in light of the product's low cost. (eg:mailers, over the counter etc).

3.0 DETAILED PRODUCT DESCRIPTION

This will be supplied once the advanced efforts in the packaging area are completed and once the uVAX program office has supplied further help in defining answers to the configuration and module partitioning outlined in the issues sections.

4.0 PRODUCT CONFIGURATIONS

To be supplied at a later date.

5.0 DETAILED IMPLEMENTATION PLAN

TO BE SUPPLIED PRIOR TO PHASE 0

5.0.1 ACCELERATED IMPLEMENTATION PLAN

Should the availability of the uVAX chip prior to the publisned schedule be deemed a reasonable possibility then the attached development plan can be accelerated, primarily by starting immediately (i.e., Q3 FY83 1/1/83). The key efforts required would be the reassignment or hiring of key people above and beyond that effort described in Section 5.1.

Additional people and funds beyond that outlined below would be required to accelerate the uVAX BI chip effort underway in Advanced Development. This would be on the order of approximately 2 people $60-100K. See Peter Jessel for additional information.

The accelerated hiring plan would be as follows: (and should be considered a replacement for section 5.1)

	Q3	Q4
Power System Design Engineer(1) (contract to Pwr. and Pkg., who may request additional manpower)	17K	17K
Packaging engineer (1) (contract to Pwr. and Pkg., who may request additional manpower)	17K	34K
CPU module engineers (2) (home cost ctr.)	34K	34K
COMBO Module engineers (2)	34K	34K
Diagnostics Engineers (2) (contract to diagnostics eng. who may request additional manpower)	34K	34K
PRODUCT MANAGER	20K	20K
SUB-TOTAL	156K	173K
CAPITAL (75x,730 systems and lab gear)	100K	250K
EXPENSE (terminals etc)	10K	20K
GRAND TOTAL	266K	443K

HEADCOUNT:		
Home cost Center	5	5
Diagnostics	2	2
Power Supply	1	1

Packaging	1	2

MILESTONES FOR Q3-Q4 FY83 ACCELERATED EFFORT

1. Resolution of packaging approach and start of packaging design.

2. Initiation of fan vendor selection.

3. Make vs buy decision on power supply. Appropriation action following decision.

4. Resolution of module content.

5. Resolution of login partitioning across modules.

6. Start of module specification for both modules.

7. Start of module design effort.

8. Acceleration of CPU module design and qualification effort understood and planned, in order to permit early availability of board product.

9. Work with Hudson to get functioning uVAX "ICE" systems (730's) in place to support module efforts.

10. Lab and office space in place.

11. Senior Diagnostics people in place.

12. Development of Systems Level Diagnostic strategy for uVAX systems.

13. Acceleration of Q1 recruiting effort.

14. Product Management Hired.

15. Acceleration of BI chip Advanced Development Effort is also essential and will require additional personnel and funding. See Peter Jessel's plan for details.

16. Put a VAX timesharing system in place.

5.1 STAFFING

In addition to budgets outlined in section 6.0 and the staffing summary listed below it is ABSOLUTELY ESSENTIAL that certain key advanced development efforts be started in Q3 and Q4 of FY83. This staff will work in those areas which lack definition because of lack of data. Delay of this early start will delay shipment of the product by two quarters. The key staff positions necessary in FY 83 are:

	Q3	Q4
POWER SYSTEM DESIGN ENG	17	34
PACKAGING ENGINEER	17	17
CPU MODULE DESIGN ENGINEER	17	17
COMBO MODULE DESIGN ENGINEER		17
	$51K	$85K
HEADCOUNT	3	5

HEADCOUNT TOTALS FOR FY84,85,86

	FY84				FY85	FY86
	Q1	Q2	Q3	Q4		
HOME COST CENTER						
CPU + SYS WC4	4	4	4	4	5	5
CPU + SYS WC2	3	3	4	5	6	6
COMBO WC4	2	2	2	2	2	2
COMBO WC2	1	1	1	1	1	1
TOTAL WC4	6	6	6	6	7	7
TOTAL WC2	4	4	5	6	7	7
TOTAL CC	10	10	11	12	14	14

HEADCOUNT FOR POWER AND PACKAGING

	FY84 Q1	Q2	Q3	Q4	FY85	FY86
PACKAGING	4	4	5	6	6	5
POWER	2.5	3.75	5.5	5.5	5.5	3

HEADCOUNT FOR DIAGNOSTICS

CPU + SYS	5	6	6	6	6	5
COMBO	1	2	3	3	2	.6
TOTAL DIAGNOSTICS	6	8	9	9	8	5.6

6.0 PROJECT BUDGET

All budget numbers are estimates. Power and packaging are based on input from those groups of costs for approximate work on other work underway for existing 32-bit projects.

CPU/SYS MODULE AND PROJECT MGMT

	FY84					FY	FY
	Q1	Q2	Q3	Q4	TOT	85	86
ENG (2)	36	36	36	36	144	156	170
TECH (1)	13.5	13.5	13.5	13.5	54	59	65
MATERIAL	5	10	20	20	55	200	20
MGR + SECY	38	38	38	38	152	154	165
CC DIRECT SUBTOTAL	92.5	97.5	107.5	107.5	405	569	420
CAD	10	20	20	20	70	80	30
LAYOUT		10	20	30	60	90	30
MODULE DIAG	34	51	51	51	187	228	168
SYS DIAG	51	51	51	51	204	228	255
F303			10	20	30	90	50
MODEL SHOP		10	10		20	30	
COMP ENG		5	10	20	35	75	
MECH ENG	5	5	10	5	25	50	20
TECH DOCS MOD			10	10	20	75	25
TECH DOCS SYS		10	30	50	90	300	150
SYS EVAL						50	25
DMT						150	
IND PKG SYS			10	10	20	50	
IND PKG MOD				10	10	30	
TIMESHARING	10	15	20	20	65	100	40
DRAFTING		5	10	10	25	30	
DEC 102/EMI			10	5	15	20	
PROTO BUILD				20	20	230	
MFG/NTL STARTUP						100	100
SUB TOTAL	110	182	272	332	896	2006	893
MODULE SUB TOTAL	202.5	279.5	379.5	439.5	1301	2575	1313

CPU/SYS MODULE AND PROJECT MGMT CONTINUED

PROJECT/CC							
GP MGR						132	144
PRODUCT MGR	25	25	25	25	100	112	124
SECY (1)	12.5	12.5	12.5	12.5	50	112	124
TECH AND MATL ADMINISTR			15	30	45	132	144
MISC (SCOPES, WPS, MAPPS,ETC.	12	20	20	20	72	176	100
SUBTOTAL	49.5	57.5	72.5	87.5	267	664	636
TOTAL CPU MODULE/SYS	252	337	452	527	1568	3239	1949
HEADCOUNT:							
HOME CC	7	7	8	9	11	11	11
DIAGNOSTICS	5	6	6	6	6	6	5

UVAX PACKAGING

	FY84					FY	FY
	Q1	Q2	Q3	Q4	TOT	85	86
ENG (3)	54	54	81	108	297	312	170
TECH (1)	13.5	13.5	13.5	13.5	54	118	65
MATERIAL	5	15	15	40	75	50	20
CONTINGENCY FOR TWO BOX DESIGN		40	48	21	109	500	200
CC SUB TOTAL	72.5	122.5	157.5	182.5	535	980	455
DRAFTING	10	20	30	30	90	50	30
NEW PROD PUCH	5	5	5		15	25	
INDUST DESIGN	5	5	5	5	20	10	
PROD SAFETY TEST						20	
DEC 102						15	
COMP ENG	5	5	5	5	20	5	
EMI TEST				5	5	15	
THERM ENG				10	10	10	
PROD ACCOUSTIC			5	5	10	10	
INDUST PKG			10	10	20	20	
P.C.CAD	5	10	10	10	35	60	
PROTOTYPES				20	20	75	
MFG STARTUP						100	
SUB TOTAL	35	45	70	100	250	415	30
TOTAL PKG	107.5	167.5	227.5	282.5	785	1395	485
HEADCOUNT PACKAGING	4	4	5	6		6	3

UVAX POWER

	FY84					FY	FY
	Q1	Q2	Q3	Q4	TOT	85	86
LABOR	42.5	71.0	92.0	92.0	297.5	335	240
MATERIAL	4	5	18	13.5	40.5	65	
DIRECT	46.5	76.0	110	105.5	338.0	400	240
DESIGN SVC		38	29	19	86	59	
COMP ENG		2	4	5	11		
CORP SAFETY				1	1	2	
MODEL SHOP				2	2		
TECH DOCS			12	12	24		
MECH ENG			4	4	8		
EMI/RFI				1	1	4	
DMT LAB						70	
TESTERS						30	
CONTINGENCY FOR PRELIM PLAN	10	10	15	15	50	100	25
PROTOTYPE BLD				20	20	100	
MFG STARTUP						50	20
SUBTOTAL	10	50	64	79	203	435	45
TOTAL POWER	56.5	126	174	184.5	541	835	285
HEADCOUNT	2.5	3.75	5.5	5.5		5.5	3.0

BI COMBO MODULE (WINCHESTER + NI + PARALLEL + SERIAL)

	Q1	Q2	Q3	Q4	TOT	85	86
ENG (2)	36	36	36	36	144	156	170
TECH (1)	13.5	13.5	13.5	13.5	54	59	65
MATERIALS		5	5	10	20	30	10
CC SUB-TOTAL	49.5	54.5	54.5	59.5	218	245	245
CAD	5	15	15	15	50	50	20
LAYOUT		5	20	30	55	60	20
DIAGNOSTICS	17	34	51	51	153	136	51
F333 TESTER				10	10	60	10
MODEL SHOP			10	10	20	30	
COMP ENG	5	10	10	10	35	40	
MECH ENG			5	10	15	20	
TECH DOCS			10	15	25	70	
SYS EVAL						20	10
DMT						50	20
INDUST PKG						10	
COMPUTING	10	10	10	15	45	50	20
DRAFTING				10	10	20	
DEC 102 + EMI						20	
PROTO BUILD						150	
MFG STARTUP						50	50
SUBTOTAL	37	74	131	176	418	816	201
TOTAL COMBO	86.5	128.5	185.5	235.5	636	1061	446

HEADCOUNT:

HOME CC	3	3	3	3	3	3	3
DIAGNOSTICS	1	2	3	3	3	2	.6

BUDGET AND HEADCOUNT TOTALS

	FY 84					FY	FY
	Q1	Q2	Q3	Q4	TOT	85	86
CPU + SYSTEM	252.?	337.0	452.?	527.0	1586	3239	1949
PACKAGING	107.5	167.5	227.5	282.5	785	1395	485
POWER	56.5	126.0	174.0	184.5	541	835	285
BI COMBO	86.5	128.5	185.5	235.5	636	961	446
	502.5	759	1039	1229.5	3530	6530	3165

HEADCOUNT TOTALS

HOME COST CIR:						
CPU + SYS	7	7	8	9	11	11
COMBO	3	3	3	3	3	3
DIAGNOSTICS:						
CPU + SYS	5	6	6	6	6	5
COMBO	1	2	3	3	2	.6
PACKAGING	4	4	5	6	6	3
POWER	2.5	3.75	5.5	5.5	5.5	3

NOTE: BI CHIP MANPOWER NOT INCLUDED HERE. SEE ADVANCED DEVELOPMENT PLAN

Return to me

JAN 18 1983

OT4.29

d i g i t a l

INTEROFFICE MEMO

To: SSPO Members

CC: SSPO Alternates
Distribution

Date: 17 January 1983
From: Omur Tasar
Dept: Low End VAX Systems Dev
Ext : 229-6119
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::TASAR

Subject: SSPO MEETING MINUTES--5 JANUARY 1983

Attendees: Demetrios Lignos, Kevin Reilly, Duane Dickhut, Mike Titelbaum, Bill Schmidt, Ken Meissner, Dave Hurlbut, Omur Tasar, Ted Gent, Bob Willard

A. ADMINISTRATIVE ISSUES

The next SSPO meeting will be on 19 January 1983 in the Cassiopeia Conference Room in Littleton.

B. AGENDA

1. Presentation on the BI Adapter Development (Mike Titelbaum)

Mike presented the goals of BI adapter development and the problems we have in prioritizing the needs of the various systems that will be using the BI bus. Currently Scorpio, Nautilus and potentially MicroVax systems are configured with the BI bus and for obvious reasons their priorities for the BI adapter development are different. From a Scorpio perspective, it is desireable to make BI adapters available concurrent with the board and system offerings and have software and other support available at the FRS time. The major problem in making this a realistic goal has been the lack of engineering resources in design, CAD, Diagnostics and Manufacturing as well as funding commitments for these adapters. Although the need for the timely development of such adapters have been recognized at all levels, the funding commitment and 32-bit program strategic commitment have been an outstanding issue. The BI adaptors that are being considered for initial availability are:

BI MFA : Multifunction Adapter; High Speed Programmable Parallel and COMM Interface
BI LESI : Dual Channel LESI for AZTEC and TU81
BI COMM : More than 8 line asynchronous MUX
BSA/BDA : RA81/RA60 (plus tape?)
BCA : BI-to-CI
BNA : BI-to-NI
B5A : Integrated 5 1/4" MiniWini, Comm, (NI?)
BUA : BI-to-Unibus Adapter

Mike presented two scenarios that could be used to prioritize the above list:

Scenario 1 - Support board customers with required BI adapter functionality at the time of Scorpio and MicroVax board products availability.

Scenario 2 - Optimize towards systems availability and do not provide broad support for board level products.

Mike added that Bill Strecker made a presentation to Demmer's staff and using the second scenario he came up with a list of priorities. Mike proposed a priority list taking the first scenario into account. The two priority lists are as follows:

SCENARIO 1	PROPOSED FRS	SCENARIO 2	PROPOSED FRS
BUA	Q1'85	BUA	Q1'85
BI MFA	Q1'85	B5A	Q3'85
BI LESI	Q2'85	BCA	Q3'85
BI COMM	Q3'85	BSA	Q3'85
B5A	Q3'85	BI COMM	Q3'85
BDA/BSA	Q1'85	BI LESI	Q3'85
BCA	Q4'85	BI MFA	Q4'85
BNA	Q4'85	BNA	Q4'85

The proposals assume that:

Scorpio board (CPU, Memory, BI) set FVS is Q1 FY85
Scorpio board set FRS is Q2 FY85
Scorpio systems FRS is Q3 FY85
Nautulis systems FRS is Q3-Q4 FY85
MicroVax BI boards FRS is Q3 FY85
MicroVax BI systems is Q3-Q4 FY85

Discussion around the two alternatives revealed that BI MFA was very crucial for the success of the Scorpio systems in the OEM market as well as the board market as a development tool. Whereas B5A would be used as a system integration building block. B5A would be critical for standalone systems. Bob Willard said that we are estimating for the majority of Scorpio systems to be distributed systems over the NI. Demetrios said that from his perspective the need for B5A early in FY85 can be met by the combination of BI MFA and BI LESI if we find a way to get 5 1/4" disk defined on LESI interface. This would be a two board solution instead of one, but still meet the requirements of MicroVax product. Bob added that BCA for Scorpio was not a priority need because we could get the same performance with HSC50 and build distributed systems over NI. Duane added that one other alternative for the MicroVax systems was to have an integrated controller right on the CPU module, which would make the board very attractive.

Mike then reviewed the people and dollar resources that will be necessary to get the BI adaptors developed. FY83 thru FY85 rough budgets required looked like this:

BUA:	$1.2M
BI MFA:	$1.5M
B5A:	$1.0M (guess)
BI LESI:	$1.0M
BI COMM:	$1.0M
BDA/BSA:	$8.0M
BCA:	$8.0M (guess)

As obvious from the budget required, it is necessary to establish a priority across all the BI adapters because at any given time we will be against limited people and dollar resources. Ken Meissner showed an estimate of people resource requirements for manufacturing. For simple boards one person was needed, for complex boards 4 to 5 persons were needed. We assumed that initially all BI modules would be complex. As an aside, Ken said that he was able to add one test person for Scorpio; also a technician was assigned to work with Mike's people in LTN.

Mike's recommendations were to keep the current implementation strategy in place and adopt Scenario 1 for BI adapter development. Further get committed funding for these programs and identify the dedicated resources for these efforts. SSPO endorsed Mike's proposal. Demetrios took the action item to negotiate this position at the 32-Bit Program Office.

Herb could not attend this meeting, but our request to the VMS group is to support BI adapters as presented in the timetable we have. VMS had requested the identification of BI adapters in the system at FRS time by the end of January. SSPO's recommendation to VMS is to assume that BUA, BI MFA, BI LESI, BI COMM and BSA will be available for Scorpio at FRS time. While the matter is strategized at various program offices, we would like this position to be taken as SSPO's formal position.

C. STATUS

1. Overall Program Status (D. Lignos)

Demetrios said that an action item was taken to review the module size based on a request by Ken Olsen. Ken generated a memo asking many questions about the size of the module and what priorites were used to arrive at the module size. Demetrios explained that we've revisited the rationale behind the present module size and it is still valid. The review revealed nothing new that would change our position.

Demetrios added that the next issue was the selection of the BI connector. Bill Schmidt will make a recommendation by the end of January. This Friday there will be a review with Bill Demmer to explain the merits of the ZIF connector. Bill Demmer would like to assure that all bases have been covered before making this crucial decision. There are still some issues remaining. One such issue is our present rack fitting into existing Euroracks. But this will have to be resolved. Demetrios said he has action item to talk to Ward McKenzie to make sure we have TVG's latest position on BI physical interconnect. It was suggested that another person to touch base with would be Jack McKeen, TVG Marketing Manager.

2. System Hardware Development (M. Titelbaum)

Mike reported that the Byte Aligner Chip will not be submitted until 2-3 weeks from now. He said that the team learned a lot from this first gate array design. Major reasons for the delay of the chip submission was the knowledge of SUDS and other CAD tools and getting to simulation stage. He said the impact on the BUA schedule will be reviewed next week.

There are some priority issues regarding the module layout of the foundation module. Jim Mars found out that our layout resource was going to be diverted to Superstar and the Scorpio task would be delayed 2 weeks. Demetrios took an action item to work this with Tays. BIIC circuit design is being reviewed today. The BIIC chip package has been submitted to Kyocera.

Bob Willard is making progress nailing down the system level architectural issues.

Mike generated a memo on his resource requirements. He needs 8 more people in the design group over the next 9 months. (Including the continuation of the development of BI Options and MP).

3. Hudson Status (D. Dickhut)

Duane said he needs a senior diagnostic engineer for the M chip. One of the microcoders is now helping with that task. Otherwise he has all the resources on board.

The F chip logic designer will be starting 17 January 1983. This person is an outside hire.

It is now closed that the V11 and MicroVax will use the same FPA kernel design. Resources are being leveraged off the J11 FPA design. The kernel design is the same, but the FPA chips for the V11 and MicroVax will be two separate die and package. The bus interfaces for the two chips are different. Larry Walker is the project manager for both development efforts.

BIIC PG date is now 5 March 1983. Schedule change notices reflected the slip on further milestones. Omur, Duane and Mike will meet mid February to understand if the second pass BIIC chip availability date can remain December 83. Many of the other development efforts are relying on this date and if it changes it will affect the program schedule.

The ROM/RAM chip PG date is end of January. Bill Johnson is the project manager for this task. This chip is pioneering the use of the back end CAD tools such as design verification and is resolving many problems.

The wirelister for QUICKDRAW is now working and getting ready to be a production tool.

New date for the first CPU TAT020 submission is 20 January 1983. New module specification is out by Bill Laprade. There are a lot of changes in this spec. Everybody should review this, especially Bob Willard.

Ken reported that Marv Horovitz requested the CPU group to include restart and loop back on errors detected by self test if it is doable. Duane said he will look into it. Duane added that Dick Sites who is leading both the Microcode and Diagnostic development is under extreme pressure and response to such requests may be slow.

Stan Lackey has decided to leave Digital by the end of January. Stan is the Chief Architect of the V11 and MicroVAX chips. His departure will be noticed.

4. Power and Packaging Status (B. Schmidt)

Bill said that they have released the BIIC package spec to Kyocera. The turn around time is 16 weeks.

Burndy will ship connectors today. AMP will ship theirs on Friday. Connectors will be evaluated in an outside lab because DEC resources were not readily available to do this. Ample data will be collected to make a sound decision. Bill has put together a matrix of criteria. The data along with a recommendation will be reviewed at the end of the month.

Pedestal drawings are being documented in detail. From these drawings we will be able to build the actual pedestal. Two pedestals are being planned for LTN. Colorado requested two more. In February, we will have the first sheet metal implementation of the pedestal with all the internal detail.

The fan appears to work in the LCN package. We are evaluating it for our accoustics and capacity specifications.

5. Memory Status (D. Hurlbut)

Dave said that he was making arrangements to work with the LTN group and do their simulations with HILO. They have a potential CAD person who will interview with P. Barck next week.

Memory TAT020 design is getting ready to be simulated. The submission date is February. Memory designers are now using Earl's latch. Omur said that she asked every group to bring their recommended latch to the TAT020 meeting on January 12th. On that date, there will be a decision as to which latch or latch types will be in the macro library.

Dave added that the DVT plan is being put together for the memory module.

6. System Architecture (B. Willard)

Bob said that the System Specification is out. There will be a review next Monday afternoon. This includes all the FRS deliverables including power and packaging. Schmidt, Sherman and Gent are involved.

NI boot issue was discussed this morning. A tentative agreement has been reached. This is a compromise solution which was described at the last SSPO meeting as "EEPROM interrupt pre-handler at IPL=31". This is an acceptable solution to VMS.

7. Manufacturing Status (K. Meissner)

Ken reported that a new person by the name of John Potucek is now on board for test issues of Scorpio. Jack Valentine will be diverted to Nebula for a while, but John will work with Jack. The pert for manufacturing milestones will be done by the end of January.

The module line schedule now says that the line will be up by the end of the month and Nebula modules will go thru it by mid February. The capital budget for the module line is in place. For things that are needed two years from now capital budget has not yet been approved.

Duane asked if Manufacturing would like to see APT hooks designed into the CPU module. Ken responded that they are now working on a system called SAVES which is a VAX based system and Salem is not planning to use APT. However, Scorpio modules can be built at other manufacturing sites such as Puerto Rico and Albuquerque who are planning to use APT. Salem should also keep APT system as a backup, because systems like SAVES or APT take years to mature. Ken will have an answer for Duane by the next meeting.

7. TAT020 Status (O. Tasar)

RJE link is up and being tested for actual file transfer. WOMBAT slices received from TI have been packaged and are being probed by the test group. This chip is the first silicon we have seen from TI and will be used as a mini qualification vehicle.

The contract is going thru the signature loop at TI. It is expected to be signed by mid January.

D. AGENDA FOR THE NEXT SSPO MEETING

- Status

See you on January 19th in Cassiopeia Conference Room in Littleton....

OT:clc

Attachment

SSPO MEMBERS

Carl Blatchley	MLO1-3/U6	223-3764	CACHE::BLATCHLEY
Paul Chen	LTN1-2/F15	229-6378	OBLIO::PCHEN
Duane Dickhut	HLO1-1/S11	225-4941	CHIPS::DICKHUT
Doug Hanzlik	LTN1-2/D07	247-2515	OBLIO::HANZLIK
Dave Hurlbut	MLO21-4/E10	223-5349	ZEUS::HURLBUT
Herb Jacobs	ZKO1-1/D42	264-8451	STAR::JACOBS
Kaj Larsen	HLO2-1/E10	225-5409	OBLIO::LARSEN
Demetrios Lignos	LTN1-2/F15	229-6116	OBLIO::LIGNOS
Ken Meissner	SVO	261-3215	OBLIO::MEISSNER
Kevin Reilly	LTN1-2/F15	229-6072	OBLIO::REILLY
Bill Schmidt	LTN1-2/F15	229-6118	OBLIO::SCHMIDT
Tom Sherman	LTN1-2/F15	229-6117	OBLIO::SHERMAN
Omur Tasar	LTN1-2/F15	229-6119	OBLIO::TASAR
Mike Titelbaum	LTN1-2/F15	229-6120	OBLIO::TITELBAUM
Bob Willard	LTN1-2/F15	229-6139	OBLIO::WILLARD

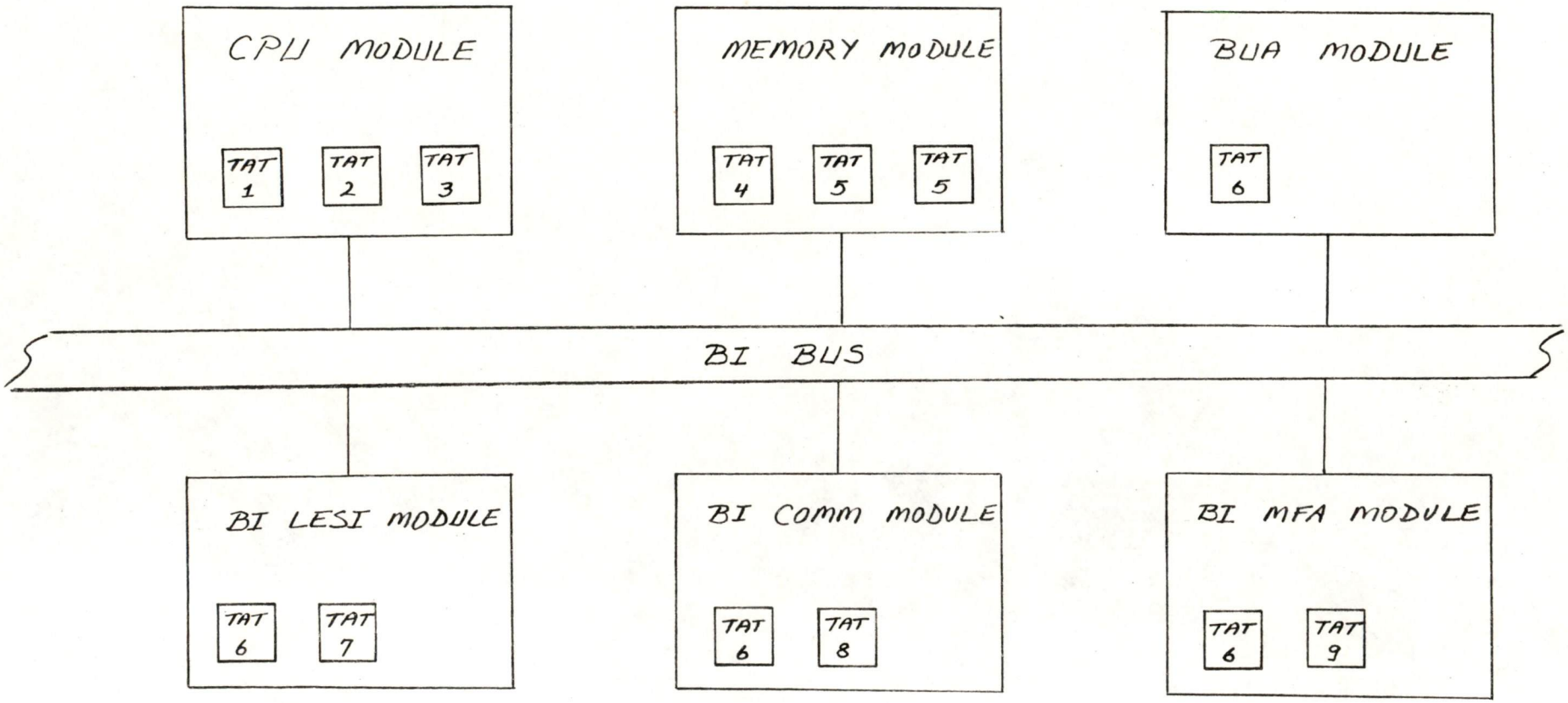
Alternates

Clark D'Elia	ZKO1-1/D42	264-8615	DELPHI::DELIA
John Forde	MLO3-6/E94	223-3516	CACHE::FORDE
Ted Gent	LTN1-2/D07	247-2531	OBLIO::GENT
Bill Johnson	HLO1-1/S11	225-4961	CHIPS::JOHNSON
Jim McWilliams	SVO	261-3239	OBLIO::MCWILLIAMS
Nelson Velez	LTN1-2/F15	229-6137	OBLIO::VELEZ

For Information Only

Peter Barck	LTN1-2/F15
Gordon Bell	MLO12-1/A51
Joel Berman	VWO1-1/C11
Dileep Bhandarkar	LTN1-2/H07
Corinne Chumsae	LTN1-2/F15
Larry Coppenrath	ZSO
Bill Demmer	LTN1-2/G09
Bud Dill	SVO
Ian Evans	HLO2-1/A10
Dan Haley	MLO21-2/E64
Brian Hannon	LTN1-2/F15
Marv Horovitz	SVO
Peter Jessel	LTN1-2/H04
Ann Katan	LTN1-2/F15
Bob Kugler	SVO
George Plowman	SVO
Barry Poland	LTN1-2/F20
Ernie Preisig	LTN1-2/F20
Sharon Sambursky	SVO
Linda Sarles	HLO2-1/C10
Chris Shatara	LJO
Bill Strecker	LTN1-2/H07
Lou Tancredi	APO-2/C4
Steve Teicher	HLO2-2/N07
Ellery Willett	NIO/N9

Please contact Cindy Cue, Ext. 229-6115, for changes to this list.



TAT020 USAGE ON THE DEFINED MODULES

O. TASAR
10. DEC 82

HERE IS A SUMMARY OF DECISIONS MADE IN THE CAD/DESIGN METHODOLOGY AREAS IN CRONOLOGICAL ORDER.

APR 82: CAD STRATEGY DEFINED; TOOLS TO SUPPORT THE STRATEGY IDENTIFIED DECSIM WAS SEEN AS INSUFFICIENT TO SUPPORT HIEARCHICAL DESIGN VERIFICATION OF BI ADAPTERS.

MAY 82: HILO IDENTIFIED AS A POSSIBLE TOOL TO SUPPLEMENT FUNCTIONAL DEFICIENCIES IN DECSIM.

JUN 82: INTERNAL CAD REVIEW WAS HELD. UPON KUSIK'S REQUEST AN ACTION ITEM WAS TAKEN TO CONSIDER VALID INSTEAD OF SUDS/AUTODLY FOR DRAWING AND TIMING VERIFICATION.

JULY 82: DECIDED TO STICK WITH SUDS TO BE ABLE TO SUPPORT THE THREE ORGANIZATIONS. VALID ALSO INTRODUCED A HIGH SCHEDULE RISK.

AUG 82: HELD A MAJOR CAD REVIEW. CAD TOOLS WERE ACCEPTED, HOWEVER, WE RECEIVED FEEDBACK TO STUDY THE DETAILED IMPLEMENTATIONS OF "TOP DOWN" DESIGN METHODOLOGY AND TIMING VERIFICATION.

SEP 82: TI ANNOUNCED THEIR FIRST SPEC OF THE TAT020. 15K MATERIAL PUT THE MEMORY AND CPU DESIGNS ON THE EDGE OF DESIGNING WITH TAT020s. NAUTILUS SWITCHED TO MCAs. AT THE FIRST TI/DEC MEETING WE UNDERSTOOD WE COULD LIVE WITH TAT020 WITH SOME PAIN.

OCT 82: TAT020 DESIGNS AND SUDS DRAWINGS STARTED. GATE LEVEL LIBRARIES FOR THE TATs WERE AVAILABLE AS AN UPGRADE FROM THE GEMINI TAT008 DESIGNS. INITIAL LIBRARY FOR THE TAT020 WAS RECEIVED FROM NAUTILUS. TI MADE A DECISION TO STANDARDIZE THEIR BETTER PERFORMANCE DEVICE (10K MATERIAL). IT WAS UNDERSTOOD THAT FOR AUTODLY TO BE APPLIED, MACRO'S HAVE TO BE IDENTIFIED WITH A SPECIAL NAMING CONVENTION AND TWO LEVELS OF DRAWINGS WHOULD BE DONE FOR EVERY TAT020. DESIGNERS RESPONDED UNFAVORABLY TO DRAWING TWO SEPARATE DRAWINGS, BECAUSE IT IS TIME CONSUMING AND ERROR PRONE.

NOV 82: WE LEARNED FROM TI THAT THEIR HDL TOOLS NOW SUPPORT TIMING VERIFICATION FOR MACRO LEVEL DESIGN SUBMISSIONS. FOR THE FIRST TIME DESIGNING WITH MACROS BECAME AN ALTERNATIVE FOR SCORPIO. THE BUA AND CPU TAT020s WERE 90% SUDS AT THIS POINT. THE DECISION WAS MADE TO SUBMIT THESE DESIGNS AT GATE LEVEL. SCHEDULE PRESSURES DID NOT ALLOW FOR MACRO LEVEL DESIGNS TO BE DRAWN ON SUDS.

O. TASAR
10 DEC 82
OT4.21

WHERE ARE WE TODAY

OUR STRENGTHS:

- ESTABLISHED AT TOP/DOWN DESIGN METHODOLOGY AND TOOLS TO COMPARE DESIGNS AT BEHAVIORAL AND GATE LEVEL.

- ESTABLISHED PROCESSES FOR THE DEVELOPMENT OF TEST AND DIAGNOSTICS CONCURRENT WITH DESIGN AND TOOLS FOR VERIFICATION OF TEST AND DIAGNOSTICS.

- CHOSE TO USE "EXISTING" TOOLS WHENEVER POSSIBLE NOT TO PUT CAD TOOL DEVELOPMENT ON THE CRITICAL PATH.

    - TAT020 TOOLS ARE DEVELOPED AND ARE BEING TESTED AT GATE LEVEL WITH THE EXCEPTION OF AUTODLY.

OUR WEAKNESSES:

- WE DID NOT FOCUS ON A STANDARD MACRO LIBRARY AND MACRO DESIGN.

- WE WERE NOT ABLE TO USE THE SAME TOOLS. FOR EXAMPLE: DECSIM/HILO FOR SOME VALID REASONS.

- WE DO NOT HAVE A COMMON/CONSISTENT SYSTEM SIMULATION STRATEGY, THAT IS, SIMULATION OF CPU WITH THE BI ADAPTERS.

O. TASAR
10 DEC 82
OT4.21

WHERE CAN WE GO FROM HERE

- PROCEED WITH SUBMISSIONS OF THE CURRENT TATO2O DESIGNS.
    - BUA TATO2O IN DECEMBER
    - CPU TATO2O IN JANUARY
    - MEMORY IN FEBRUARY
- CAREFULLY EVALUATE THE RISK OF NOT EXECUTING TIMING VERIFICATION ON THE ABOVE DESIGNS.
    - IF NEEDED START PARALLEL EFFORT TO REDESIGN THESE CHIPS AT MACRO LEVEL.
- ESTABLISH A STANDARD GATE AND MACRO LIBRARY AND A PROCESS FOR MACRO DESIGN.
    - PAUL WADE WORKING WITH BOB STEWART AND DESIGN ENGINEERS.
- AGREE TO DO LOGIC DESIGN REVIEWS PRIOR TO SUBMISSIONS.

O. TASAR
10 DEC 82
OT4.21

STEPS TO GO TO MACRO DESIGN

TIME REQUIRED

JANUARY 1. SELECT STANDARD MACROS

JANUARY 2. GENERATE LIBRARIES FOR MACROS

- SUDS
- HILO/DECSIM (INCLUDING ATG FOR HILO)
- AUTODLY
- HDL

JANUARY 3. UPGRADE EXISTING TAT020 TOOLS TO WORK WITH MACROS

✓ - MAPPS
MARCH - SUDS TO HDL
✓ - DECSIM AND HILO TO TDL
APRIL - PSTAT TO DECSIM, HILO, AND AUTODLY
FEBRUARY - SUDS TO HILO AND DECSIM

MARCH 4. VERIFY PROCESS

APRIL 5. VERIFY LINK TO/FROM TI

O. TASAR
10 DEC 82
OT4.21

DL8.24

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INTEROFFICE MEMO

To: Distribution

Date: 10 December 1982
From: Demetrios Lignos
Dept: Low-End VAX Systems Dev
Ext.: 229-6116
Loc/Mail Stop: LTN1-2/F15
ENET: OBLIO::LIGNOS

Subject: MINUTES FROM THE SCORPIO TECHNICAL PROGRAM REVIEW

GENERAL

On Tuesday, 30 November, the second Scorpio Program Technical Review took place in Marlboro (LM02). Attending the review were a large number of people (see the list of attendees) from Central Engineering, Manufacturing, and Field Service. The review format was very similar to the first such technical review held last May. The presentation content was actually an account of what transpired over the last seven months between reviews, a "snapshot" of where the program is today and where we are going. The review content (copies of all the slides in the order that they were presented) was distributed in a special binder to all the review participants at the review.

Basically, the committed pieces of the Scorpio program are in the implementation state. All the functional specs for those items have been completed and distributed. Paper designs are well on the way and we are actually about to submit the first TAT020 designs to TI. The Scorpio program (committed FCS products) is pretty much on schedule today, but we are very aware that the more difficult period of the project is yet to come.

There were a number of comments and action items that were generated during the review. We should point out that none of these items were considered major or of a "show stopper" nature for our program. A list of these comments and action items follows:

COMMENTS AND ACTION ITEMS LIST

- Are there any plans to deliver an 11/750 based BI tester to the VMS Group? There are no specific plans at this time but we need to investigate this.

  Action: Mike Titelbaum

- How are we going to support a line printer on Scorpio systems? Is the BI COMM going to have a parallel interface? At this time, our plans are for a serial interface only. The printer group needs to get involved to clarify the support process and approach.

  Action: Bob Willard

- Status of other important BI options:

  BI COMM: Not committed to a schedule. Moving at a very slow pace today.

  BSA: Would like to have it a year earlier than presently proposed (Q1 FY'86).

  BCA: Not a staffed group at this time.

  Gordon suggested that I publish a one page BI options status memo on a monthly basis.

  Action: Demetrios Lignos

- Our group in Littleton should function as the clearing house for all BI modules that are being done in the corporation. We should try to get as many BI options started as possible.

- It may turn out that the presently available 16 CI nodes on the star coupler are not enough for the Scorpio system. Is it possible to handle multiple CI clusters with VMS?

  Action: Bob Willard/VMS

- Can we use the same memory module that is being designed for 64K and 256K chips for 1M bit chips as well? According to Memory Engineering, the module will have to be redesigned to handle the 1M bit chips.

- We are planning to simulate the entire module (every module) before we build it. We will construct (using HILO) a behavioral simulator of the BI that all the modules are going to use for simulation.

- Very strong recommendation that the hardware logic designers should be constrained in their use of unlimited designs of state devices (flops and latches). The multiple gate level implementations for state devices will result in a very big job using AUTODLY and having to characterize manually each device.

  Action: All hardware design managers

- Gordon was concerned that we have to do timing verification at the chip level. We should know the timing margins in the design as a result of the worst case logic design approach that we are following.

- All the software tools listed in the Scorpio design methodology process are available today. The only hickup in our CAD total plan is the timing verification. We will be running a test case with our first TAT020 design to verify the methodology as outlined with the exception of timing verification.

- In order for HILO to be usable for module simulation, we need to model several complex devices. All are covered and will be available except the T11 modeling since Genrad is the parent company for Cirrus (the London based creator to HILO) can we get them to do the modeling of the T11 for us? Or can we farm it out anyway?

- Can we make the BI model available in the HILO library?

  Action: Omur Tasar/Demetrios Lignos

- Concerning the ability to restrict logic designers from using an unlimited number of state device designs, Don McInnis suggested that Bob Stewart give a tutorial to the designers on the subject. We will set it up.

  Action: Omur Tasar

- Gordon requested a detailed design review of the TAT020 designs in process at this time. We will set up such a review.

  Action: Demetrios Lignos

- If the OEM was just BI (no Unibus backpanel), would it be easier to implement? Even though it would be necessary to reconfigure the pieces inside, it would be much easier (and cheaper) to implement.

- Is there any problem of powering the second BI backplane if it was used instead of the Unibus backplane? What are the limiations?

  Action: Bill Schmidt

- How close are the mechanical piece parts design between LCN and Scorpio? Can the hard tooling be common between those two products? There is very little parts commonality due to the weight, size, etc. differences.

- In the manufacturing presentation list of outstanding issues, Franco Previd was asked to add the issue of assigning dedicated teams to the project. Franco has no problem of doing that.

  Action: Franco Previd

- Is VMS planning to support the BI MFA? There are no such plans today according to Herb Jacobs since VMS has no information on the BI MFA today.

  Action: Mike Titelbaum

- The system disk cannot be on the BSA unless the BSA is supported by Release 3B. At the present time, the BSA target schedule calls for VMS support in Release 4.

- Can we use a software model to simulate the BSA so that VMS software can be tested ahead of the hardware? It may be possible.

  Action: Bill Mathrani

- What are our plans for making the BIIC public? It should happen within six months or so from now.

  Action: BI Product Manager (Paul Chen)

- Concerned about process of exportation of BI related physical hardware technology to other DEC engineering groups such as Colorado. Need to establish such a process and put into affect.

  Action: Bill Schmidt

The action items below are from a list of "loose ends" presented by Bill Demmer at the conclusion of our review:

- No MP FRS date.

  Action: Mike Titelbaum

- Where does toy reside?

  Action: Mike Titelbaum/Bill Schmidt

- When will the F-Chip be available?

  Action: Bill Johnson

- Will BIIC chip simulation get done in two months?

  Action: Omur Tasar, et al

- Why support PDP-11 on Unibus? What are the implications?

  Action: Bob Willard, et al

- How do you attach line printers?

  Action: Bob Willard

- Do we need BNA? Or is Scorpio it? (BCA, BI COMM, BSA schedule)

  Action: Bob Willard

- Who will address > 16 node CI requirements?

  Action: Bob Willard

- What is the controlled library for logic designers? (Currently the CAD risk not completely under control.)

  Action: Hardware logic design managers

- How do we take advantage of the new module shrink capabilities?

  Action: Bill Schmidt/Jim Mars

- Scorpio pedestal height is 28 1/2". Is LCN 26" high?

  Action: Bill Schmidt

- The Salem Volume NPSU funnel (bottleneck?) dynamics of synchronizing with VMS.

  Action: Scorpio Program Office

It should be noted that our review went very well with all the attendees very positive in their comments. I would also like to point out that the apparent progress in our development is largely due to the stability in our development plans which we have been enjoying since our project was last redefined in January 1982. I am sure I am echoing everyone on the project in hoping that this stability continues.

I would like to request that each of the individuals whose name appears on the action items list respond by addressing the isse(s) in a timely fashion and before the next review. At this time, we are planning the next technical program review to occur around mid-April 1983. Certain very significant events will have occurred by then which will determine whether the Scorpio program will remain on the current schedule.

Please call me if you have any questions or comments.

DL:clc

DISTRIBUTION

Meeting Attendees
SSPO

John Adams	TWO/B12
Phil Arnold	CXO1-1/P13
Paul Bauer	MLO1-3/T62
Tom Burniece	CXO/Q21
Paul Chen	TWO/C04
Lou Gaviglia	ICO/G01
George Hoff	TWO/C04
John Holz	TWO/C04
Bill Johnson	MLO12-3/A62
Bernie Lacroute	TWO/A08
Bruce Ryan	LTN1-2/D08
Dave Rodgers	TWO/A08
Grant Saviers	MLO3-6/E94

ATTENDEES

Gordon Bell	MLO12-1/A51	Bob Kirk	CXO1-2/Q12
Dileep Bhandarkar	LTN1-2/H07	George Kitzman	APO1/F2
Carl Blatchley	MLO1-3/U6	Kaj Larsen	HLO2-1/A10
Frank Bomba	LTN1-2/F15	Chi Lau	WOO/D97
Kirk Bonner	GSO/E6	Ken Mamayek	MLO21-4/E10
Randi Brenowitz	LTN1-1/H10	Jim Mars	LTN1-2/F15
Reid Brown	ZSO	Bill Mathrani	CXO1-1/P13
Bob Burley	LTN1-2/B17	Don McInnis	LTN1-2/B17
Elaine Burke	SVO	Ray Mercier	HLO1-1/S11
Michael Callander	HLO1-1/S11	Roy Moffa	HLO2-1/B11
Joe Chenail	SVO	Peter Murphy	SVO
Bill Demmer	LTN1-2/H09	Al Nichols	VWO/C02
Joe Dunne	GA	Bob Pedersen	LTN1-1/D05
Ian Evans	HLO2-1/A10	Ernie Preisig	LTN1-2/F20
Bob Fallon	APO1/E2	Franco Previd	SVO
Mitch Federman	LMO2/P41	Kevin Reilly	LTN1-2/F15
Ted Gent	LTN1-2/D07	Bill Schmidt	LTN1-2/F15
Brian Hannon	LTN1-2/F15	Tom Sherman	LTN1-2/F15
Doug Hanzlik	LTN1-2/D07	Jim Stegeman	MLO21-2/E64
Marv Horovitz	SVO	Omur Tasar	LTN1-2/F15
Dave Hurlbut	MLO21-4/E10	Mike Titelbaum	LTN1-2/F15
Bill Johnson	HLO1-1/S11	Nelson Velez	LTN1-2/F15
Bob Johnston	ICO/D25	Paul Wade	LTN1-2/F15
Jim Kane	MRO5/06	Joe Welch	APO1/E2
Ann Katan	LTN1-2/F15	Bob Willard	LTN1-2/F15
Sid Kimber	APO1/C15	Steve Zabinski	OGO1-2/S07