JUN 18 1979

digital

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 14 June 1979
FROM: George Hoff
DEPT: LSG Engineering Operations
EXT: 231-6524
LOC/MAIL STOP: MR1-2/E78

SUBJ: VENUS TECHNOLOGY REVIEW - 06 JUNE 1979

Attached is a summary of the issues discussed, positions taken, and decisions made. I have also attached a copy of the slides presented and handouts prepared for the meeting. The minutes are highly condensed in order to get this information distributed in a timely manner. If anyone has corrections or additions please contact me.

GH/dmc
attachments

digital

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 14 June 1979
FROM: George Hoff
DEPT: LSG Engineering Operations
EXT: 231-6524
LOC/MAIL STOP: MR1-2/E78

SUBJ: SUMMARY OF DISCUSSION AND DATA REVIEWED AT VENUS TECHNOLOGY REVIEW 06 JUNE 1979

Attendees

O^2D:	Gordon Bell, Jim Cudmore, Ulf Fagerquist
LSG:	Sas Durvasula, George Hoff, Vic Ku, Jud Leonard, Pat Sullivan, Bill Walton, Sultan Zia
Microproducts:	Russ Doane
MSD:	Brian Croxon
Purchasing:	Dan Hamel, Steve Kavicchi
O^2T:	Alan Kotok

Goal for Meeting

Review tradeoffs between three technology alternatives for Venus: MCA (Motorola), Siemmens 100K ECL array and 100K MSI(Fairchild).

Tradeoff Review included:

1. Prime Vendor Status and second sources
2. Burdened Part Cost (Cost of each type of IC mounted on tested module)
3. Venus Cost Estimate with each technology
4. Schedule differences
5. Development Cost

Review of Positions

Decision on how to proceed

Review of Data (see slides attached)

The data presented indicated that with a average module cost estimated ($350 for 8 layers) the MCA approach yielded a pro-

cessor kernel cost of $9695 (5% above goal), versus $11592 (20% above goal) for 100K MSI. Siemmens was significantly more expensive than the MCA and provides less functionality (36 cells vs. 48 for the MCA) and was excluded.

The cost difference between 100K MSI and the MCA was noted as not highly significant in the cost of the total system. Pat Sullivan further projected the 100K MSI cost could be brought down to the MCA cost by reducing module cost to $120 and application of 24 pin dips in lieu of chip carriers. Pat was alone in believing that this could be accomplished. Another issue discussed was the value of chip replacement (instead of modules) which Field Service has estimated to be worth $20 million over the life of the product. The MCA with I^2L diagnostic logic and sockets maximizes our chances of reaching this goal.

A review of schedule differences between the 100K MSI approach and the MCA indicated only a slight advantage for 100K MSI (1 month). This was not generally accepted and the consensus appeared to be more like 3-6 months based on Comet experience.

The development cost for Venus with MCA was estimated at $14.3 million vs. $12.9 million for 100K MSI.

Position Summary

The vendor/second source situation is not optimum for any of the technologies. Motorola (MCA) looks better than Fairchild (100K MSI) primarily due to a potential 2nd U.S. source and a history of more stability as a volume vendor. The fact that we will not have a qualified part until October is a major concern. (Hamel) Gordon suggested we exploit this decision process to secure commitments from Motorola at the senior management levels.

The data we have been able to generate to date indicates only a moderate cost advantage (20%) for the MCA, however, to a designer the actual potential looks greater. As the designers learn to use the MCA the cost reduction yield relative to 100K MSI will increase. The MCA is the choice of the designers because it is the most competitive solution with the greatest potential and we have a running start in the CAD tools area. The MCA also reduces the level of module interconnect required which should enhance our chances of volume module build by Digital -- this is critical to Venus. (Durvasula, Hoff, Leonard, Kotok)

Pat Sullivan's position that 100K MSI was a better solution in terms of schedule, risk, and potential cost was not changed as a result of the discussion above. Pat suggested that a Hybrid approach of 100K MSI and Siemens arrays for control might be optimum. Gordon rejected this proposal on the grounds that it resulted in maximum risk; i.e. we would need to develop two volume technologies to get Venus to market.

The potential application of 100K MSI for the 2080 was also discussed. Since the 2080 is less cost sensitive, has lower volume and critical time to market requirement a different technology choice may be appropriate. The 2080 could possibly use multiwire for production relieving the requirement for a fine line multilayer 100K module. A multiwire 100K MSI approach for the 2080 would eliminate conflict for both chip layout and module layout resources between Venus and 2080 in Marlboro.

We need to build up our knowledge in complex design tools and processes. The oxide isolation process is a critical "next step" in our bi-polar process development. We must go forward into advanced technology and drive prices down. (Croxon, Cudmore, Doane)

The real tradeoff is between the short term and long term. All indications are that the future is gate array and beyond. We must stage this product to build the knowledge base for the next product. We can not skip a technology step and expect to make a double jump in the next generation machine. The Comet experience indicates we can expect incremental development cost and longer time to market (3-6 months), however, this is the risk we must take to meet the competition. The Venus schedule and budget must be tested versus what happened on Comet. (Bell, Fagerquist)

Decision

Gordon's position was to proceed with the design using the MCA. O^2D approval and Operations Committee approval must be attained before the decision is final. Gordon will recommend approval of the MCA technology for Venus. Gordon also recommended that we actively pursue putting the Bipolar RAMs also in the sockets as this would yield a substantial savings in the field service replacement costs.

digital

INTEROFFICE MEMORANDUM

TO: Ulf Fagerquist

CC: Distribution

DATE: June 11, 1979
FROM: Bill Green *Bill*
DEPT: LSI Mfg. & Eng.
EXT: 2220
LOC/MAIL STOP: ML1-4 B34

SUBJ: I.C. Technology for Venus

The long range technology objective of the LSI Group may be summarized in two statements:

1. To develop silicon processes that are close to those of the industry leaders. This requires continued improvements in device density, speed, and power.

2. To develop design processes and tools of a structured (CAD-able) nature that will allow low cost, quick turn around custom chip design.

In addition to supporting these objectives with PL97 and 98 funds, experience dictates that we explore actively opportunities to integrate these efforts with product programs. In such programs the reality of the market place more effectively refines our efforts than is possible elsewhere. This memo will relate the technology objectives above to the choices you are making with respect to Venus and to a lesser extent 20/80.

The alternatives you are examining for the Venus CPU are:

1. 100K MSI
2. Siemens gate array + MSI
3. Motorola gate array + MSI.

Alternative 1 does not in any way support the technology objectives stated above. Furthermore, it does not leave any residuals — insofar as we can judge — for future machines. We believe, in fact, that it merely delays an inevitable move to LSI and probably makes that step steeper when finally taken. If either alternative 2 or 3 produces an equivalent system, they are much more supportive of our objectives.

Both alternatives 2 and 3 support the LSI technology objectives. With regard to silicon processes, both the Motorola and Siemens processes represent a substantial advance over the Comet process. A detailed comparison from available sources shows the two to be literally <u>identical</u> step by step except for the resistivety of the starting material. Thus the work already expended on the Motorola process should contribute equally well to progress on the Siemens process. Until we know more details, it is not equally clear whether the equipment ordered for the oxide isolation step is also useful. Given the fact that both will take DEC to the same end point of performance, the maturity of the Siemens process recommends it.

To illustrate the advantages for future DEC products accruing from the acquisition of the process, a simple comparison is made below between the Comet array and a proposed Siemens TTL array.

	Comet	Siemens
Gates	480	700+
Pins	48	64
Power	1.6-2.0 W	1.5 W
Speed	3-7 ns.	1 ns.

Such an array might be useful for a next generation Comet.

With regard to CAD process technology, both gate arrays will lead to useful progress. The efforts already expended on the Motorola array have been substantial and are essentially complete. No such work has been done in DEC on CAD for the Siemens array. This will require additional effort to achieve an equivalent posture.

A table is attached to compare the technology for business arrangements possible with Siemens and Motorola. The Motorola agreement is known in detail. The Siemens proposal, while remarkably complete on short notice, is yet to be negotiated in detail. Note that though the Siemens agreement calls for a royalty while the Motorola one does not, there is some equivalent offset since we believe we experience some small price increase on guaranteed business. From a business point of view neither the cost nor obligations are sufficiently different to discriminate between the two.

Summary and Recommendation

The execution of Venus in 100K MSI does not enhance the DEC technology position in LSI nor leave any residuals toward future systems. Either gate array proposal supports both LSI silicon and design process objectives and builds residuals toward future systems. While both silicon processes are in principle identical, the Siemens process is substantially more mature and proven by a reasonable amount of production. As an offset, the CAD to support logic design is more advanced with Motorola. The business positions with both vendors are nearly equivalent with Motorola representing a broader potential as a partner. In summary, the LSI group finds little sharp distinction between the support for its programs between Motorola and Siemens and will support equally either choice.

WBG:cg
Attachment (1)
Distribution:

CC: Gordon Bell
Pat Buffet
Jim Cudmore
Dan Hamel
George Hoff ✓
Ruth Rawa
Rod Schmidt
Jack Schneider
Bobby Snow
Joe Zeh

Attachment 1.

	Motorola	Siemens
Provides gate array design	yes	yes
Provides ECL process	yes	yes
Provides technical consultation	yes	yes
Gate array business	FY81 70% FY82 50% FY83 50%	about 50%
Cash payment	$150,000	about $100,000
Royalty	no	about 3% on I.C.'s produced by DEC
Standard Device Business	$5M	no
Unibus license	yes	no
Other	preferential qualification on new standard device	unknown
Provides CAD programs	no	yes
ECL RAM business	40% FY81-83	not clear

TECHNOLOGY STATUS REVIEW

① **MCA**: TWO U.S. SOURCES
ⓐ MOTOROLA ⓑ NATIONAL SEMI

ⓐ MOTOROLA'S WORKING PARTS - SEPT 79
COMITTED TO VOLUME - SEPT 80
ⓑ NATIONAL SEMI — NO DATA YET

② **SIEMENS ARRAY**: TWO EUROPEAN SOURCES
a) SIEMENS
b) RTC

ⓐ SIEMENS PART IS HERE IN QUANTITES
ⓑ RTC IS ONE YEAR AWAY FROM DELIVERING OPTIONS TO SIEMENS.

③ **100K SSI, MSI**: TWO U.S. SOURCES
ONE EUROPEAN SOURCE

a) FAIRCHILD HAS 35 PART TYPES
b) NATIONAL WILL HAVE 17TYPES IN TWO YEARS
c) RTC WILL HAVE 27 TYPES IN TWO YEARS.

— x —

	MCA	SIEMENS 36 ARRAY	100K LOGIC A.S.P
DEVICE COST	\$ 33.00	\$ 42.00	2.05

ASSUMPTIONS IN THE COSTING OF THE MODULE

FOR MCA & GATE ARRAY:

1. 8 LAYER (4 SIGNAL) EXTENDED HEX.
2. 32 MCAs OR GATE ARRAYS / board
3. DEVICES SOCKETED
4. CHIP LEVEL ISOLATION
5. ASSOCIATED TERMINATORS & CAPACITORS

FOR 100K LOGIC FAMILY:

1. 8 LAYER (4 SIGNAL) EXTENDED HEX
2. 162 DEVICES IN CHIP CARRIERS
3. SURFACE MOUNTED COMPONANTS WITH REFLOW SOLDER PROCESS
4. BOARD LEVEL ISOLATION
5. ASSOCIATED TERMINATORS & CAPACITORS.

PRODUCT COST COMPARISON IS DONE BY

1) CALCULATING THE COST OF A FULLY POPULATED MODULE FOR EACH OF THE THREE TECHNOLOGIES.

2) CALCULATE THE COST OF A FULLY LOADED DEVICE BY DIVIDING THE COST OF THE MODULE BY THE NUMBER OF DEVICES

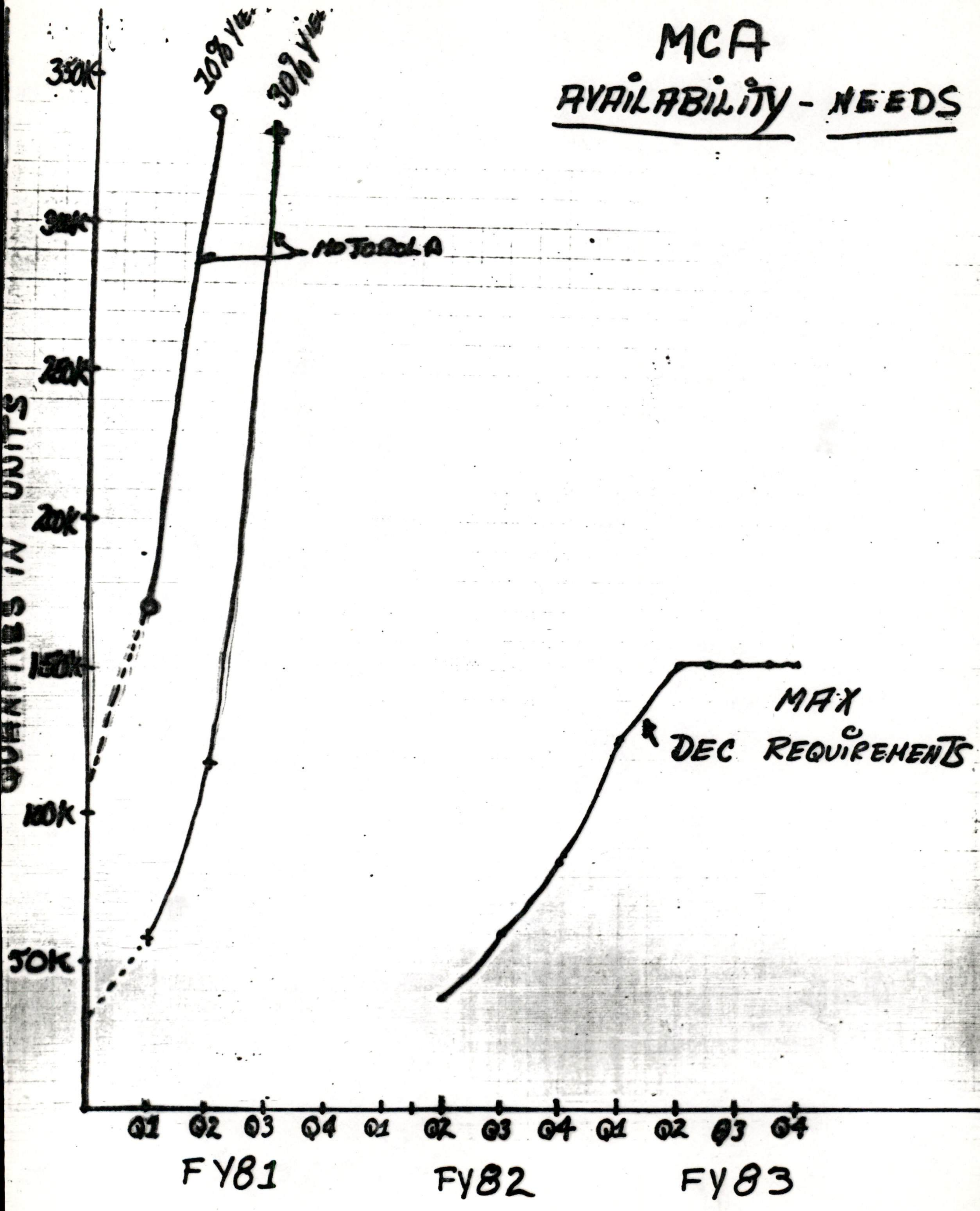
3) CALCULATE THE PRODUCT COST BY MULTIPLYING THE LOADED COST / DEVICE BY THE NUMBER OF DEVICES IN THE CPU.

LOADED COST / DEVICE ANALYSIS

	NOT	SIE-24	SIE-36	100K IN CHIP CARRIER	100K IN 24 PIN DIP*
P.C. BD. (8 LAYER)	350	350	350	350	120*
SOCKET	96	96	96	------	----
CAPS	25.7	25.7	25.7	32	32
RESISTORS	24	24	24	32	47
ASSEMBLY/TEST	70	82	82	160	97
DIAGNOSTIC LOGIC	------	176	176	75	{ 349
I.C.'s	1056	1088.	1344.	328	
INCOMMING INSPECTION	106	109	134	32.8	35
TOTAL	$ 1727.7	$1950.7	$2231.7	$ 1010.00	$ 680.00
COST/DEVICE	54.0	61.0	69.74	6.23	4.53
COST OF POWER/DEVICE	5.0	3.0	4.0	.80	.80
TOTAL COST/DEVICE	59.0	64.0	73.7	7.0	5.3

ASSUMPTIONS:

1. 32 MCAs PER EXTENDED HEX
2. 32 SIEMENS ARRAY PER EXTENDED HEX
3. 162 SSI, MSI PER EXTENDED HEX
4. 8 LAYER (4 SIGNAL LAYERS) P.C. BOARD.
5.* COST BASED ON POSSIBILITY OF MOUNTING 171 24 PIN DIPS ON 6 LAYER EXTENDED HEX.



MCA
AVAILABILITY - NEEDS
QUANTITIES IN UNITS
350K
300K
250K
200K
150K
100K
50K
10% Yie
30% Yie
MOTOROLA
MAX
DEC REQUIREMENTS
Q1
Q2
Q3
Q4
FY81
FY82
FY83

DATA PATH TRIAL DESIGNS

	MCA	SIEMENS	100K	RATIO MSI/GATE ARRAY MCA	SIEMENS
VENUS IBOX DATA PATH					
CHIP COUNT	16 (13)	20	130	8.1 (10)	12
DELAY (NS)	50 (57)	49	58	1.16(1.02)	1.18
VENUS EBOX DATA PATH					
CHIP COUNT	13		80	6.2	
DELAY	50		57	1.14	
VENUS MBOX DATA PATH					
CHIP COUNT	8	8	90	11.3	11.3
DELAY	30		29	.96	
DOLPHIN MBOX DATA PATH					
CHIP COUNT	17	26+7msi	505	29.7	18.7
DELAY	76	60			

CONTROL TRIAL DESIGNS

	MCA	SIEMENS	100K	RATIO MSI/GATE ARRAY MCA	SIEMENS
MULTI-MEM CONTROL					
CHIP COUNT	.4	.6	11	27	18
DELAY	24	22	25	1.04	1.14
KL10 MB CONTROL					
CHIP COUNT	.5	1.0	19	38	19
MICROSTACK CONTROL					
CHIP COUNT	.26		5.4	21	
IBOX VALID CONTROL					
CHIP COUNT	.5		16	32	
DOLPHIN BUS INTERFACE					
CHIP COUNT	1		17	17	

WEIGHTED MEAN FUNCTIONALITY RATIOS

DATA PATH: **1x MCA = 8.1x 100K MSI (excluding Dolphin MBOX)**
1x MCA = 1.3x SIEMENS

CONTROL: **1x MCA = 26x 100K MSI**
1x MCA = 1.8x SIEMENS

CPU DESIGNERS POLL

"WHAT PROPORTION OF CHIPS IN A TYPICAL CPU ARE USED FOR DATA PATH AS OPPOSED TO CONTROL?"

PAUL BINDER: 1/3 TO 1/2 IS CONTROL

JEFF MITCHELL: ABOUT HALF CONTROL

ALAN KOTOK: ABOUT 50 - 50

KL10 MODULES:	30% RAM
	37% CONTROL
	33% DATA PATH
780 MODULES:	22% RAM/PROM
	44% CONTROL
	33% DATA PATH

IN ORDER TO COMPARE COSTS, WE WANT THE OVERALL RATIO (R) OF MSI TO GATE ARRAY CHIPS TO IMPLEMENT EQUAL FUNCTION

LET F_c = FRACTION OF MSI CHIPS NEEDED FOR CONTROL

$F_d = 1 - F_c$ = FRACTION OF MSI CHIPS FOR DATA PATH

R_c = RATIO OF CONTROL MSI PER GATE ARRAY

R_d = RATIO OF DATA PATH MSI PER GATE ARRAY

THEN

$$\frac{F_c}{R_c} + \frac{1-F_d}{R_d} = \frac{1}{R}$$

$$R = \frac{R_c R_d}{R_d F_c + R_c(1-F_c)}$$

EXAMPLE: GIVEN A 1000-CHIP MSI CPU, HALF CONTROL AND HALF DATA PATH, HOW MANY MCA'S ARE REQUIRED TO REPLACE IT, AT A RATIO OF 8.1 FOR DATA PATH AND 26 FOR CONTROL?

DATA PATH MCA'S = 500 / 8.1 = 62

CONTROL MCA'S = 500 / 26 = 19

TOTAL MCA'S 81

OVERALL RATIO (R) = 1000 / 81 = 12.3

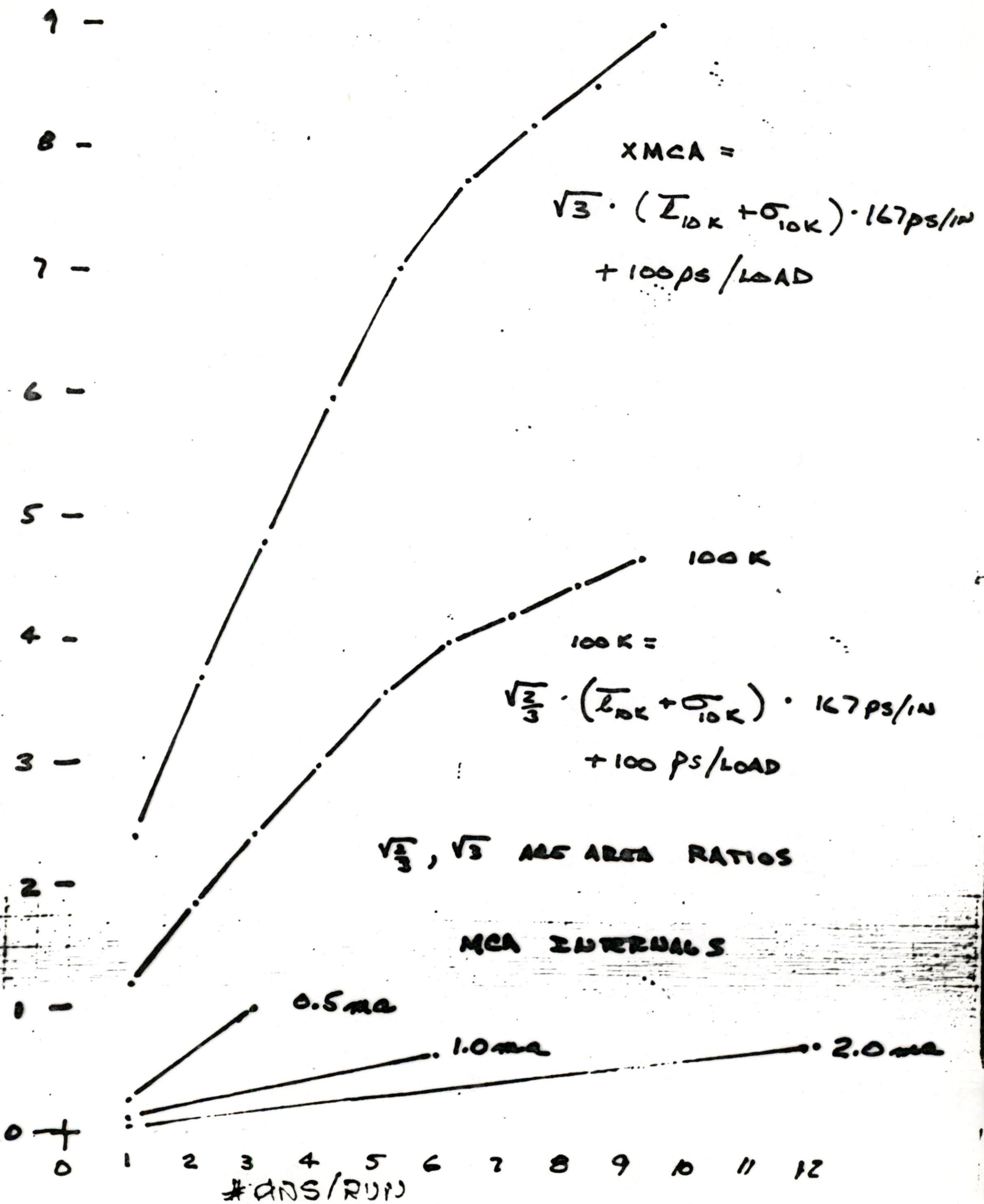
LOGIC COST COMPARISON: GOAL = $9200

MCA IMPLEMENTATION
USING MARCH 10 ESTIMATES

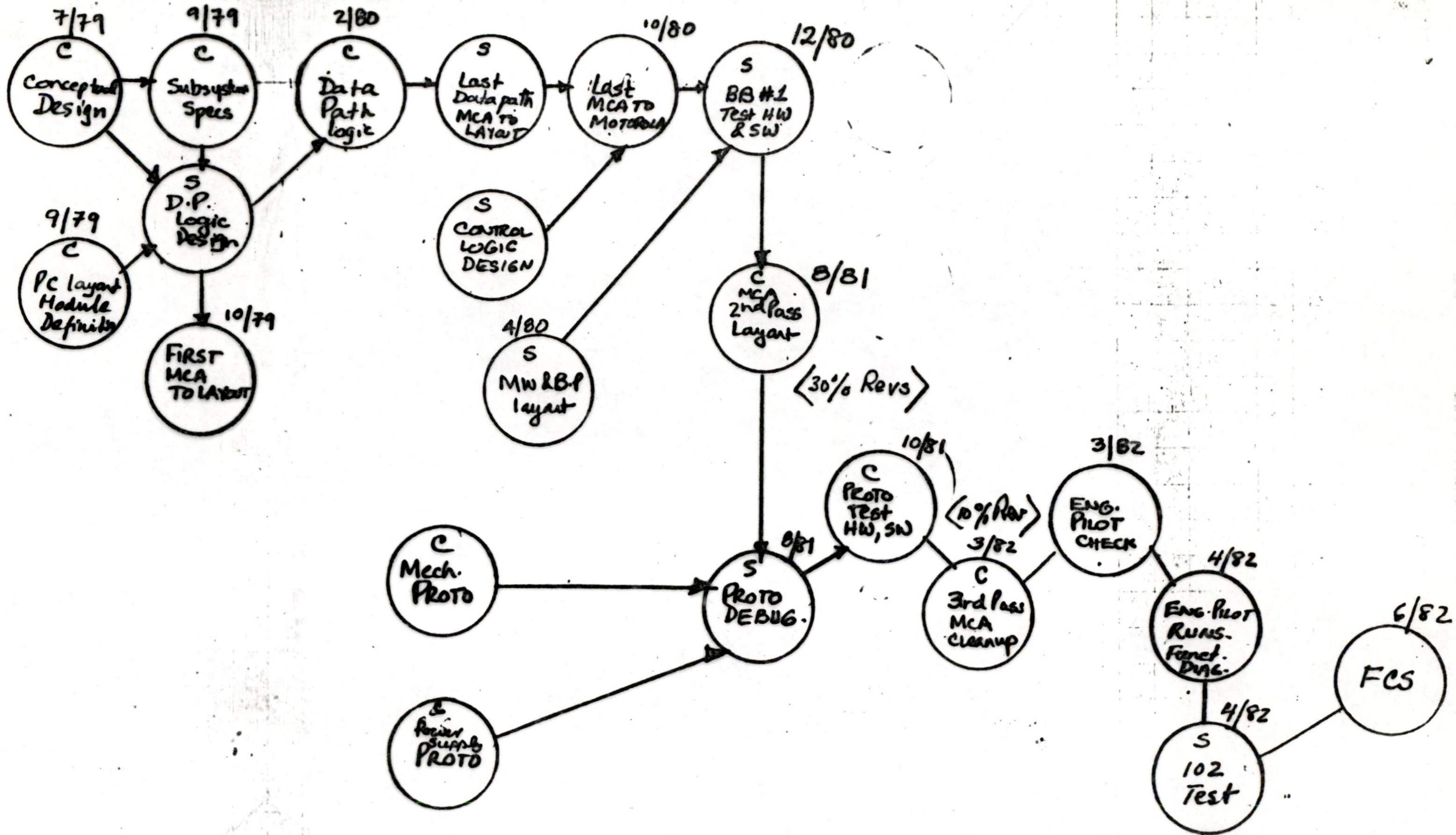
70 MCA @ $59	$ 4130		9 bds
235 4K RAM @ $19	4465	BURDENED	
100 1K RAM @ $11	1100	$5/CHIP	
	$ 9695		

100K EQUIVALENT IMPLEMENTATION
@ FUNCTIONALITY RATIO.= 12.3

861 MSI @ $7	$ 6027	11 bds
TOTAL RAMS	5565	
	$ 11592	



9
8
7
6
5
4
3
2
1
0
XMCA =
$\sqrt{3} \cdot (I_{10K} + \sigma_{10K}) \cdot 167ps/IN$
+ 100ps/LOAD
100K
100K =
$\sqrt{\frac{2}{3}} \cdot (I_{10K} + \sigma_{10K}) \cdot 167ps/IN$
+ 100 ps/LOAD
$\sqrt{\frac{2}{3}}$, $\sqrt{3}$ ARE AREA RATIOS
MCA INTERNALS
0.5ma
1.0ma
2.0ma
0 1 2 3 4 5 6 7 8 9 10 11 12
#ANS/RUN

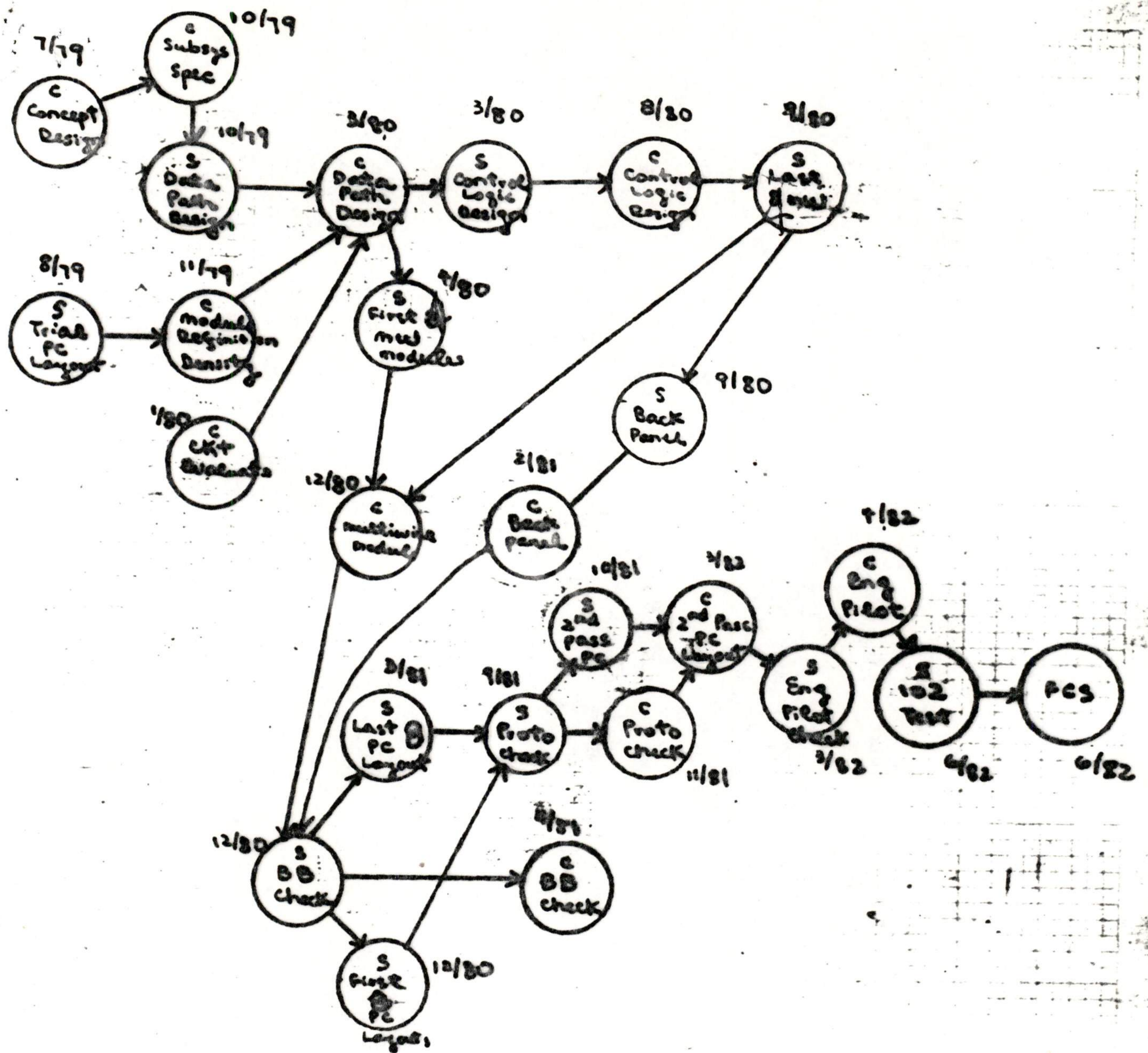


MCA BASED VENUS DEV. PERT TO FCS

MCA VENUS PERT

ASSUMPTIONS:

1. MCA, 10K Technology
2. Do all MCA design for breadboard with emulator backup for failing MCAs.
3. Maximum of 40 MCA types to do the design.
4. FY80, 81, 82 loading 10 Engineers and 7 Technicians for MCA design.
5. Start first MCA layout by 15 OCT, 4 pipes in layout.
6. 6 weeks layout time, 4 weeks for calma operation, 12 weeks in MOTOROLA for chips.
7. Breadboard is multiwire and proto is etch.
8. 3 passes to get MCAs right for FCS.
9. No schedule improvement in MOTOROLA during the first two years.
10. MCA development cost 80K/MCA.



Venus Pert using 100K

6/12/79

Assumptions = 1) 100K SSI and MSI chips

2) Total chip count = 11/780 = 2087 chips (excluding RAMS and ROMS)

3) 160 chips/module, 4 signal layer/module

4) Total CPU module count = 16

5) 20 weeks per layout, 6 IC designers

6) BBs are multiwire, Prototypes, Pilots, FCS Systems are etched

Vic Ku
6/12/79

VENUS PROJECT MAJOR MILESTONES

	with MCA	with 100K
Conceptual Design Done	7/79	7/79
Specifications Available	9/78	9/79
Complete Data Path Design	2/80	3/80
Complete Control Path Design	5/80	5/80
BB Power On	12/80	9/80
Complete BB Checkout	4/81	12/80
Proto Power On	8/81	6/81
Complete Proto Checkout	10/81	8/81
Eng. Pilot Power On	2/82	12/81
	3/82	1/82
DMT, 102 Complete	5/82	3/82
FCS (50%)	5/82	3/82 (1)
FCS (90%)	3/83	9/82
Volume FCS (50%)	11/82	9/82

(1) If PC layout time is 10 weeks instead of 20 weeks, this date will be one quarter sooner.

Vic Ku
6/12/79

VENUS HARDWARE DEVELOPMENT COST (K) - MCA

	FY80	FY81	FY82	FY83	Total (K)
CPU	1600	2600	2200	700	7100
Memory	327	600	300	70	1297
Technology	1016	1050	900	200	3166
MCA/tools	500	50	30	--	580
Release Eng.	46	58	200	100	404
IPA/HSC50	167	240	70	50	527
Hydra Comm/UR	40	72	50	50	212
SBI Adaptor	143	263	70	48	524
CAD	103	120	140	100	463
				Total	14.3M

Vic Ku
6/12/79

VENUS HARDWARE DEVELOPMENT COST (K) - 100 K

	FY80	FY81	FY82	FY83	Total (K)
CPU Design	1500	2100	1700	700	6000
Memory	327	600	300	70	1297
Technology	1200	1100	1000	200	3500
Release	46	58	200	100	404
IPA/HSC50	167	240	70	50	527
Hydra Comm/UR	40	72	50	50	212
SBI Adaptor	143	263	70	48	524
CAD	103	120	140	100	463
				Total	12.9M

Vic Ku
6/12/79

DECISION MATRIX

CRITERIA	MOTOROLA			SIEMENS			FSC/100K		
	SCORE	WEIGHTING	TOTAL SCORE	SCORE	WEIGHTING	TOTAL SCORE	SCORE	WEIGHTING	TOTAL SCORE
1. SYSTEM COST	10	2	20	6	2	12	9	2	16
2. A. DESIGN RISK ARRAY	7	3	21	10	3	30	10	3	30
B. SCHEDULE RISK DUE TO INTERNAL PROBLEMS	8	3	24	6	3	18	10	3	30
C. SCHEDULE RISK EXTERNAL	5	3	15	9	3	27	9	3	27
3. SECOND SOURCE	8	1	8	6	1	6	8	1	8
4. MANUFACTURABILITY									
A. YIELD	5	1	5	7	1	7	9	1	9
B. CAPACITY	8	1	8	8	1	8	9	1	9
5. SUPPORT CIRCUITS	3	1	3	10	1	10	10	1	10
6. EASE OF ENG. INTERACTION	9	1	9	5	1	5	5	1	5
7. DESIRE TO SELL	10	1	10	7	1	7	8	1	8
8. RELATIONSHIP W/DEC	10	1	10	5	1	5	4	1	4

DECISION MATRIX (CONT'D)

	CRITERIA	MOTOROLA			SIEMENS			FSC/100K		
		SCORE	WEIGHTING	TOTAL SCORE	SCORE	WEIGHTING	TOTAL SCORE	SCORE	WEIGHTING	TOTAL SCORE
9.	LONG TERM BUSINESS DIRECTION	10	1	10	10	1	10	5	1	5
10.	EASE OF FUTURE ECL DESIGN BUSINESS	10	1	10	7	1	7	0	0	0
11.	TECHNOLOGY TRANSFER	10	1	10	8	1	8	~~10~~ 0	1	~~10~~ 0 N/A
12.	DEC PENETRATION* (LOW IS GOOD)	8	1	8	5	1	5	6	1	6
13.	CONTRACTUAL EASE	10	1	10	6	1	6	6	1	6
	TOTAL SCORE			181			171			~~182~~ 172

*30% OF MOTOROLA G/A PRODUCTION
50% OF SIEMENS' G/A PRODUCTION
35% OF FSC'S 100K PRODUCTION
W/ 100K ONLY

DAN HAMEL
11 JUNE 79

```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

DATE: May 2, 1979
REV 1: JUNE 13, 1979
FROM: JOHN HACKENBERG J.H.
DEPT: I.C.E.G.
EXT: 6106
LOC: MR1-2/E47

TO: Distribution list

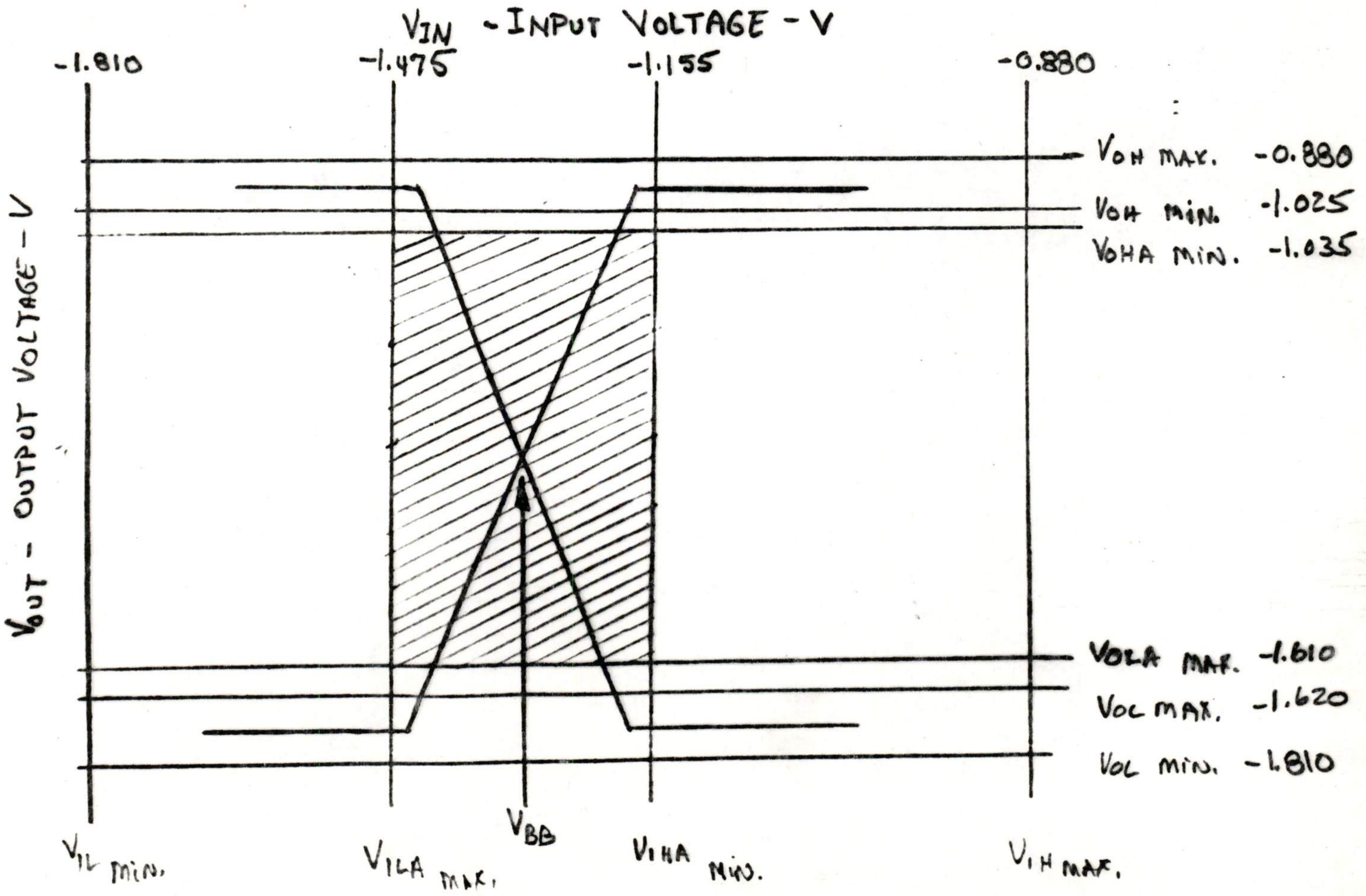
SUBJ: Noise Margin for 100K ECI

This memo shows the noise margin when using 100K and/or 10K ECI parts. This study takes into account voltage and temperature differentials that may exist in a ECI system.

The Siemens Gate Array will incorporate voltage compensation and temperature compensation.

The following noise margin study is based on the 100K ECI noise marging information supplied in the Fairchild ECI Data Bookpublished in 1977. This memo will follow the same outline as the memo of Nov. 2, 1978 on " System Noise Margin for the Dolphin ECI logic".

The following graph shows the points for determining noise margin for the 100K ECI gates:



Guaranteed noise margin (NM) is defined as follows:

(1) $NM_{high\ level} = V_{OHA\ min} - V_{IHA\ min}$

(2) $NM_{low\ level} = V_{ILA\ max} - V_{OLA\ max}$

The above equations do NOT take into account temperature and voltage varitions in a system. For 100k ECL parts, the tracking rates for the supply voltages are:

ΔV_{OHV} = 35 mV/V, ΔV_{BBV} =52 mV/V, and ΔV_{OLV} =70 mV/V

ΔV_{OHV} = The change in V_{OH} due to a change in V_{EE}.

ΔV_{OLV} = The change in V_{OL} due to a change in V_{EE}.

ΔV_{BBV} = The change in V_{BB} due to a change in V_{EE}.

Temperature:

The 100k series operates in both still or forced air systems where an ambient temperature of 0 °C to +85°C is maintained. The required cooling is determined solely by this ambient temperature requirement. There is no need to maintain a constant temperature throughout the system. The 100k devices are relatively insensitive to variations in junction temperature. No power warm-up or moving air cooling is required to assure the specified device characteristics.

The requied system voltage at Vee pins is -4.2 to -5.7 Volts. With a load on all outputs of 50 ohms to -2.0 V and a 0°C to a +85°C temperature range, the device dc parameter are guaranteed for a nominal Vee of -4.5 V.

For 100K ECL,

$$NM_H = 120 \text{ mV and } NM_L = 135 \text{ mV}$$

These numbers are over the temperature range 0°C to +85°C. If there are supply voltage differentials between packages, the above noise margin numbers change.

The magnitude of the output levels and the bias level is larger as the magnitude of the supply voltage increases. The effects of temperature changes are specified in the data sheets. As the temperature increases, the magnitude of the input and output levels get smaller. From these facts, equation (1) and (2) are modified as follows:

(3) $NM_H = /V_{IHA\ min}$ at smallest magnitude of V_{EE} and the highest temp/

$-/V_{OHA\ min}$ at largest magnitude of V_{EE} and the lowest temp/

(4) $NM_L = /V_{OLA\ max}$ at smallest magnitude of V_{EE} and the highest temp/

$-/V_{ILA\ max}$ at the largest mag. of V_{EE} and the lowest temp/

Equations (3) and (4) may be rewritten in terms of temperature and voltage.

(5) $NM_H = /V_{IHA\ min} / - [(\Delta V_{BBV})(\Delta V_L) + (\Delta V_{IHAT})(T_H - 25^\circ C)]$

$-/V_{OHA\ min} / - [(\Delta V_{OHV})(\Delta V_H) + (\Delta V_{OHT})(25^\circ C - T_L)]$

(6) $NM_L = /V_{OLA\ max} / - [(\Delta V_{OLV})(\Delta V_L) + (\Delta V_{OLT})(T_H - 25^\circ C)]$

$-/V_{ILA\ max} / - [(\Delta V_{BBV})(\Delta V_H) + (\Delta V_{ILAT})(25^\circ C - T_L)]$

T_L = Ambient temperature of incoming air to system

T_H = Temperature of air exiting system.

$T = T_H - T_L$ = max. temp differential between packages.

V_H = The largest magnitude of V_{EE}.

V_L = The smallest magnitude of V_{EE}.

$V_H = V_H$ -5.2 (or -4.5 V)

V_L = 5.2 (or -4.5 V) - V_L

NM_H = High voltage noise margin in mV.

NM_L = Low voltage noise margin in mV.

The tracking rates can be inserted into equations (5) and (6) to obtain noise margin equations for for 100K ECL. Neglect Temperature variations in 100K ECL logic.

1) 100K ECL driving 100K ECL

$$NM_H = 120 - 52(\Delta V_L) - 35(\Delta V_H)$$

$$NM_L = 135 - 70(\Delta V_L) - 52(\Delta V_H)$$

The following is a chart of Noise margin (in mV) for different supply voltages:

Voltage Tolerance		NM_H	NM_l
-4.5	+/- 7%	97.56mV	101.9mV
-4.5	+/- 5%	100.4	107.55
-4.5	+/- 3%	108.2	118.5
-5.2	+/- 7%	88.3	90.6
-5.2	+/- 5%	97.4	103.3
-5.2	+/- 3%	106.4	115.97

The following is a comparison between 10K ECL non-compensated, 10K ECL compensated, and 100K.

	10K ECI Non-Compensated	10K ECI Compensated	100K ECI
Logic levels			
Voh max.	-0.810 V	-0.810 V	-0.880 V
Voh min.	-0.960 V	-0.960 V	-1.025 V
Voha min.	-0.980 V	-0.960 V	-1.035 V
Vola max.	-1.630 V	-1.630 V	-1.610 V
Vol max.	-1.650 V	-1.650 V	-1.620 V
Vol min.	-1.850 V	-1.850 V	-1.810 V
Vih max.	-0.810 V	-0.810 V	-0.880 V
Viha min.	-1.105 V	-1.105 V	-1.155 V
Vila max.	-1.475 V	-1.475 V	-1.475 V
Vil min.	-1.850 V	-1.850 V	-1.810 V
Noise Margin			
NM h	125 mV	125 mV	120 mV
NM l	155 mV	155 mV	135 mV
NOTE: Voltage differentials and temperature tracking are NOT taken into consideration here.			
Noise Margin			
-4.5 V 7%			
NM h	-	-	92.56 mV
NM l	-	-	101.9 mV
-4.5 V 5%			
NM h	-	-	103.1
NM l	-	-	111.4
-4.5 V 3%			
NM h	-	-	108.2
NM l	-	-	118.5

CONTINUED FROM PAGE 5

	10K ECL Non-Compensated		10K ECL Compensated		100K ECL
-5.2 V 7%	Δ10°C	Δ20°C	Δ10°C	Δ20°C	
NM h	53.3 mV	-1.9 mV	-	-	88.3 mV
NM l	41.3	-13.9	-	-	90.59
-5.2V 5%					
NM h	70	58	101 mV	89 mV	97.4
NM l	46	40	127	121	103.3
-5.2V 3%					
NM h	87.4	75.4	105.8	93.8	106.4
NM l	87.1	81.3	135.2	129.3	115.97
-5.2V 2%					
NM h	96	84	107	95	-
NM l	108	102	138	132	-
Logic swing Voh max. - Vol min.	1040 mV		1040 mV		930 mV
Voh min. - Vol max.	690 mV		690 mV		595 mV
Rise Time 20% to 80%	1.1 NS		1.0 NS		0.5 NS
0% to 100%	1.84 NS		1.67 NS		0.84 NS

Summary of Noise margin study:

The following is the noise margin for each ECl type operated at it's nominal operating voltage +/- 3% for power distribution, power supply regulation and filtering on modules.

Nominal Operating Voltages	10K ECl Non-compensated	10K ECl Compensated	100K
+/- 3%	87.1 mV (Δ10°C)	105.8 mV (Δ10°C)	108.2 mV

DISTRIBUTION LIST:

GORDON BELL	ML12-1/A11
RON BINGHAM	MR1-2/E85
STEVE CAVICCHI	WB
DICK CLAYTON	ML12-2/E71
BRIAN CROXON	TW/C04
JIM CUDMORE	ML1-5/E30
BILL DEMMER	TW/D19
RUSS DOANE	ML1-4/E34
SAS DURVASALA	MR1-2/E47
ULF FAGERQUIST	MR1-2/E78
BILL GREEN	ML1-4/B34
DAN HAMEL	WB
GEORGE HOFF	MR1-2/E78
BILL JOHNSON	ML12-3/A62
ALAN KOTOK	ML3-5/H33
VIC KU	MR1-2/E47
JUD LEONARD	MR1-2/E47
JOHN MEYER	ML12-1/A11
LARRY PORTNER	ML12-1/T32
GRANT SAVIERS	MR3-6/E94
BILL WALTON	MR1-2/E47
SULTAN ZIA	MR1-2/E47

MAY 1 6 1979

VENUS PRODUCT REQUIREMENTS

MAY 1979

AUTHOR: Marilyn S. Ressler
TW/A08
247-2421

DIGITAL EQUIPMENT CORPORATION

C O M P A N Y   C O N F I D E N T I A L

TABLE OF CONTENTS PAGE

Acknowledgment 3

Preface 4

1.0 Overview 6

2.0 Digital's Corporate Strategy and Objectives 8

3.0 The Marketplace 9
- 3.1 Market Requirements 9
- 3.2 Market Segments 10
  - 3.2.1. Scientific Computation 12
  - 3.2.2. Real-time Computation 13
  - 3.2.3. Transaction Processing 14
  - 3.2.4. General Purpose Commercial EDP 15
  - 3.2.5. General Purpose Timesharing 16
- 3.3 Digital's Marketing Groups 17
  - 3.3.1. Technical Group 17
    - TOEM 17
    - LDP 17
    - MSG 18
    - ESG 18
    - ECS 19
    - GSG 20
  - 3.3.2. Commercial Group 21
    - COEM 21
    - CSI 21
    - MDC 22
    - T&UG 22

4.0 Product Strategy and Objectives 23

5.0 Product Requirements 25

6.0 Product Assessment 40
- 6.1 Market Fitness and Competitive Goodness 40
- 6.2 VAX Family Product Positioning 41
- 6.3 Compatibility with Digital Systems 43
- 6.4 Product Development Assumptions 44
- 6.5 Product Development Risks 44

APPENDIX A: VENUS Systems 46
APPENDIX B: Preliminary Product Forecasts and Assumptions 47
APPENDIX C: Comparison Prices and Costs for VAX-11/780 49
APPENDIX D: VAX Software Plans 50
APPENDIX E: Related Documentation 51

DIGITAL EQUIPMENT CORPORATION
COMPANY CONFIDENTIAL

ACKNOWLEDGMENT

This VENUS Product Requirements Document is based extensively on a November 1978 preliminary draft written by Peter Conklin and Bernie Lacroute. For this update of VENUS requirements, much-needed technical and marketing information and several good ideas were contributed by Peter Conklin, Bernie Lacroute, Dave Rodgers, Steve Jenkins, Ed Slaughter, Kathryn Norris, Ed McHugh, Al Avery, and Al Ryder.

Similar product requirements documents created in the Mid-range Systems Product Management group by Kathryn Norris (VAX/VMS R2.0) and Lou Philippon (NEBULA) were used as guides for the structure and content of this VENUS document.

The Product Line Marketing section of the VAX-11/780 Sales Guide was the source of details included here on coverage of the market segments.

The MSD Red Book for FY79 provided information on corporate and MSD strategy and on the VENUS product relative to other 32-bit products under development.

This entire document was prepared on a WS102 word processing system by Carol Hicks, Mid-range Systems Product Management.

PREFACE

This is a Product Requirements document for VENUS, the VAX-11/780 replacement product. Several other documents on the VENUS product will be published. Among these are:

1. Preliminary Product Summary (PPS)/Product Contract
2. Project Plans
3. System Plan
4. Product Description and Specification
5. Business Plan

The objectives of this Product Requirements document are:

1. to specify the attributes of the VENUS product;
2. to identify the marketplace for VENUS;
3. to describe how the VENUS product, its marketplace, and its product strategy are compatible with the corporate strategy and objectives;
4. to provide product and market information to every DIGITAL group involved in the VENUS development and marketing;
5. to establish a precedent for creation and subsequent use of this document and several other product-related documents that are necessary for short- and long-term review and control of VENUS product development and marketing.

Initially this document reiterates the DIGITAL strategy and objectives for developing and marketing computer products with a 32-bit architecture. Then the market need for a VENUS product is explained. As part of this, the principal market segments are identified along with their respective product requirements. Further breakdown of the market segments is presented relative to DIGITAL's current organization of the Product Lines. The main competitors of each Product Line are also noted.

Next the product strategy and objectives are given, that is, the plans for the VENUS product, what its principal characteristics are, how it fits in with other DIGITAL products. This is followed by a list of product requirements with development priorities specified.

Finally a product assessment denotes the product's market fit, its competitive goodness, and its positioning and compatibility with other DIGITAL products. Then the assumptions and risks of product development and marketing are given.

The last portion of this document, Appendices A through E, contain general information that is relevant to the VENUS development and marketing.

Note that this Product Requirements document is being published now to assist in the transfer of VENUS product development from Tewksbury to Marlborough. As such, the document is somewhat premature. Release of a fully updated requirements document (based on a preliminary draft authored by Peter Conklin and Bernie Lacroute in November, 1978) was anticipated following the completion of several key information gathering tasks being done in Mid-range Systems Product Management. This work has been suspended temporarily and, instead, all effort has been given to preparation of this interim document based on data available as of April 1979. The information gathering tasks will be resumed by LSG after transfer is complete.

1.0 OVERVIEW

The corporate strategy is to converge on a 32-bit architecture by FY85 with the center of business in systems having MLP less than $250,000. Focus will be given to development of systems for distributed processing and for high availability.

Between now and the mid-1980's the marketplace will demand computer system products that are cost- and performance-effective, easy to use, secure, highly reliable, and family oriented. The products must support distributed processing with interconnections to systems of many vendors and to packet switched networks. They must be laden with rich software (languages, data management, utilities, applications).

The market for VENUS-based systems meeting these product requirements is divided into five segments:

1. scientific computation
2. real-time computation
3. transaction processing
4. general purpose commercial EDP
5. general purpose timesharing

Digital's Product Line Groups are currently organizied to serve these segments as follows:

TECHNICAL GROUP --

- TOEM: scientific and real-time computation
- LDP : scientific and real-time computation
- MSG : real-time computation, general purpose commercial EDP
- ESG : general purpose timesharing, scientific computation
- ECS : general purpose timesharing
- GSG : all segments

COMMERCIAL GROUP --

- COEM: general purpose commercial EDP
- CSI : general purpose commercial EDP, transaction processing, general purpose timesharing
- MDC : general purpose timesharing, real-time computation
- T&UG: real-time computation, general purpose timesharing, general purpose commercial EDP

No analysis has been done for the Product Lines in the Computer Group and the Customer Services Group.

VENUS is a product at the high end of the VAX family pyramid during the FY82-85 timeframe. It will meet the market's requirements with product development priorities as follows:

- #1 - design center at $180K MLP with performance at 3.5 times VAX-11/780
- #2 - new I/O architecture based on ICCS, HSC50, and MERCURY
- #3 - SBI capability for -11/780 migration
- #4 - FCS in Q1FY82; volume in Q2FY82
- #5 - entry level system at $99K MLP
- #6 - significant RAMP improvements
- #7 - system options
- #8 - large system

The VENUS system product is an excellent offering to the traditional Digital markets --- scientific, real-time, timesharing. For transaction processing and for general purpose commercial EDP, VENUS will also be a strong product with the continued development of software products appropriate to those market segments.

The VENUS system product will be compatible with the VAX family architecture. It will use the single VAX family operating system, VAX/VMS. VAX-11/780 migration is supported, and PDP-11 compatibility mode is maintained.

2.0 DIGITAL'S CORPORATE STRATEGY AND OBJECTIVES

The corporate strategy is to develop and market computer products intended for distributed processing systems and for high availability systems. The center of the corporate business will be single-processor systems with a purchase price below $250,000. While current products are based on 8-, 16-, 32-, and 36-bit architectures, there will be convergence to a single 32-bit architecture by 1985. The products based on the latter architecture will be developed and marketed in a manner that provides maximum protection of our existing PDP-11, DECsystem-10, and DECSYSTEM-20 customer base.

3.0 THE MARKETPLACE

3.1 Market Requirements

In the FY82-FY85 time frame, the computer system manufacturers in the EDP industry must offer products that meet the following requirements:

- Cost-/performance-effective computing engines
- Distributed computing capability
- Systems with a high degree of data integrity, internal security and protection
- Effective system interconnection (DEC to DEC, DEC to IBM and other mainframes, X25 for packet switched networks)
- Non-stop computing capability, fault tolerant computing (HYDRA-like configurations)
- Highly reliable systems
- System packaging/operation suitable to an office environment
- System familiness whether or not the individual systems are physically tied into a network
- Highly approachable, easy-to-use systems whether dedicated to a single application or to several different modes of operation
- Training and documentation suited to a wide variety of end users
- Richness of software (languages, data management, utilities, applications)
- Availability of skilled services from the computer system vendor (maintenance, system design, applications programming help)

It will be necessary for vendors of these products to provide complete and accurate cost-of-ownership data to the prospective customers in each market segment. Since the distributed processing style of computing (with more computing on more data by more people) will be emphasized for these products, the amount of mass storage and the number of end user terminals to be purchased will greatly increase from present-day levels.

It will also be necessary to provide prospective customers with comprehensive system performance data that is specific to their particular use of the computer system product. As an example, for a transaction processing application this could be data on system throughput in terms of the number of transactions processed per hour based on such variables as 1) the number of characters in each transaction, 2) the number and speed of the communications lines, 3) the number of multi-drop terminals on each line, and 4) the number of disk accesses per transaction.

A major challenge will be to provide these highly cost-/performance-effective computing engines for systems which require neither a sizable staff of support specialists nor a special operational environment. This means that the systems must be easy to build (dock merge), easy to install (customer merge), easy to use, and easy to repair (self-diagnosis, some customer maintenance). Similarly, the desire of customers to utilize the computer system as a resource to do a specific job (rather than to learn how to be system programmers) and to increase worker productivity puts a great emphasis on 1) the availability of programming languages, data management facilties, utilities and applications software, 2) the reduction (and even elimination) of system and sub-system downtime, and 3) the familiness of systems to ensure that no learning is required when upgrading to a more powerful configuration or when adding another family member to a network.

3.2 Market Segments

VENUS-based systems will be capable of meeting the marketplace requirements outlined above. To provide focus for VENUS product development and marketing, several key market segments can be identified according to how the VENUS-based systems are used, what the characteristics are of computer system products utilized in these market segments, and who these users are.

From the perspective of system use, the market segments for the VENUS product are:

1. Scientific Computation
2. Real-time Computation
3. Transaction Processing
4. General Purpose Commercial EDP
5. General Purpose Timesharing

There are characteristics common to the computer systems utilized in all these segments. These include:

- o Easy-to-use, highly approachable, friendly systems for various levels of users
- o Easy-to-use program development tools
- o Documentation, commands, prompting, error messages in the language and style of the end user
- o System HELP facilities
- o Internal system security and protection
- o Large capacity, high-speed mass storage
- o Fast backup/restore between disks and tapes
- o Storage hierarchies
- o Data management, data integrity
- o Support (programming tools, file exchange utilities) for transfer from other current DIGITAL products, migration to future products; system familiness is critical
- o Ease of connection to other DEC (DECnet), IBM, CDC, other networks (X25)
- o Network transparency to applications programs and to terminal users
- o One general purpose operating system with sufficient extensibility/adaptability to serve the entire range of market segments
- o Systems configurable/tunable to effective use by a specific market segment (and its changing needs)
- o Ease of adding applications packages to the system
- o Variety of programming languages
- o ANSI-standard languages with validated compilers
- o Common for all programming -- call standards, data types, record management, exception handling, run-time library, symbolic debugger
- o High system reliability -- extensive H/W, S/W RAMP support; solid quality assurance testing

In addition to the above common characteristics, each market segment has very specific needs to be fulfilled by the VENUS product. By market segment these are:

3.2.1. Scientific Computation

- Multi-user systems
- Good interactive performance
- High-speed processing
- Accuracy
- Fast, mainframe FORTRAN, PL/1
- FORTRAN IV PLUS to match IBM Level H FORTRAN
- Global optimizer (optional during program development)
- APL with file system
- Vector processor with language support
- Large programs
- Sharable programs
- Reliable systems to run large programs to completion
- Mainframe off-loading (ANSI-standard high performance FORTRAN and PL/1, ANSI-standard mag tape, virtual address space)
- Multi-system, high-speed interconnects to other DEC; to IBM, CDC, and UNIVAC
- DECnet, X25
- Batch processing (especially when replacing outmoded IBM systems)
- Data management (for large data files)
- Software routines for graphics displays and plotters
- Applications packages (statistics, project management/control, math library)

3.2.2. Real-time Computation

- High-speed processing
- Rapid context switching
- Low scheduling overhead
- Fast interrupt handling (response to, service of interrupts)
- Fast I/O
- Accuracy
- DECnet (for distributed data acquistion systems)
- Microcoded math functions
- High availability through redundancy, ease/transparency of switchover
- File exchange utility for other DEC products (especially -11M systems)
- Fast, highly-optimized FORTRAN (optimizer optional during program development)
- PASCAL, PL/1, ADA, CORAL-66 (United Kingdom), PEARL (Germany)
- Fully-supported end-user tools for UCS and KMC-11 or equivalent
- Ease of interfacing and supporting special devices.
- Tools for performance measurement, system tuning

3.2.3. Transaction Processing

- Many (10-500) terminals on-line simultaneously in a network
- Terminal cluster controllers with down-line load, up-line dump, data entry/verify, interim storage for off-line data entry
- Intelligent communications subsystems (MERCURY)
- TP concurrent with program development
- Multi-drop terminals
- Intelligent terminals with down-line load
- Fast COBOL, PL/1
- Data management
- Distributed data base management, data base integrity
- Hierarchical data storage, archiving
- Message control
- Forms definition language (compiler, debugger)
- Batch
- Connect to DECnet, IBM, X25
- Fast, reliable communications
- Network transparency to user terminals, applications programs
- High availability (HYDRA-like configuration)
- Journalling
- Shadow recording
- Transaction roll forward/roll backward
- System-/network-wide data directory and dictionary
- Tools for network performance measurement, load balancing, tuning, reconfiguring
- Easy switchover of TP terminal to general purpose use (program development, data inquiry)
- Additional operators' consoles

DIGITAL EQUIPMENT CORPORATION
COMPANY CONFIDENTIAL

3.2.4. General Purpose Commercial EDP

Multi-user system (production EDP runs concurrent with interactive program development, word processing, on-line applications, RJE to mainframes)
Tools for computer-assisted program documentation
File design assists
Support for a family of terminals (dumb to intelligent)
Applications packages (broad range of capabilties; ease of installation, use, support)
Multi-volume disk files
Data management
Distributed data base management
Data integrity
Inquiry language, report writer
Forms definition language (compiler, debugger)
Limited transaction processing
Journalling
Shadow recording
Transaction roll forward/roll backward
Communication with other mainframes (IBM, CDC, UNIVAC); connect to DECnet, X25
Industry standard languages
Fast, mainframe COBOL, PL/1
Interactive BASIC
RPG II, BASIC, MUMPS, APL with file system
SORT with MERGE option
Tools for migration from IBM to DEC
IBM tape handling (including EBCDIC data)
ANSI-standard tapes (labels, formats)
Disk allocation controls and reporting
BATCH (scheduling, resource allocation, reporting)
Job class scheduling
System resource accounting
System-/network-wide data directory and dictionary

- Office automation (connect to remote word processors, backup storage for large documents, document interchange utility, electronic mail)
- Support of typeset terminals (SCRIBE editor)
- Hierarchical data storage, archiving
- System security and protection (e.g., terminals limited to running a single application)

3.2.5. General Purpose Timesharing

- Multi-user system (512 edu terminals active sumultaneously)
- Good interactive performance (especially for on-line applications; for edit, compile, link/task build, debug/test process)
- Large programs
- Sharable programs
- Interactive BASIC
- Multiple languages (FORTRAN, COBOL, PL/1, BASIC, PASCAL, ADA, RPG II, BLISS, APL, MUMPS, ALGOL)
- Fast compilers
- Fast syntax checkers for all languages
- Flexible BATCH, spooler queues
- File exchange utilities
- Data management
- Inquiry language
- Report writer
- Resource allocation, quotas, scheduling
- System resource accounting
- Dynamic working set size selection
- Applications packages (especially CAI, school administration, project management/control; broad range of capabilities; ease of installation, use, support)
- Tools for host development of small systems (DEC) software
- Software for graphics displays and plotters
- Connect to other mainframes (IBM, CDC, UNIVAC)
- DECnet, X25
- Scientific computation
- Office automation

3.3 DIGITAL'S Marketing Groups

If we now consider the current organization of DIGITAL'S Product Line Marketing Groups, it is possible to identify several of the users (customers) within each of these segments and to denote those customers with requirements spanning two or more market segments. Mainly the Technical and Commercial Groups have been studied because of the applicability of VENUS to their Product Lines. Further study should be done especially with the Word Processing, Computer Special Systems, and Graphic Arts Product Lines.

3.3.1. TECHNICAL GROUP

TOEM, Technical OEM.

Their users are involved with

a. flight training simulation -- real-time computation
b. power monitoring -- real-time computation (high-availability systems)
c. seismic exploration -- scientific computation
d. aerospace systems -- real-time and scientific computation (familiness is required)

Potential new users are those in industrial automation and in telephone and data communications (both real-time computation).

TOEM sees competition from SEL, Interdata, Harris (all in-flight simulation), Modcomp (power monitoring), and PRIME and the mainframe vendors (in seismic and aerospace).

LDP, Laboratory Products

Their users, primarily doing scientific and real-time computation, are involved with

a. U.S. and foreign government research
b. university research
c. energy research
d. industrial research
e. simulation (sensor-based and modeling)

Competition is mainly from SEL, Harris, and Interdata. CDC will remain strong competition since there are many systems (6400, 6600, 7600s especially in energy) to be off-loaded or even replaced by one or more VENUS systems.

MSG, Medical Systems

Their users are

a. medical OEMs -- real-time computation (high availability systems)
b. medical administration -- general purpose commercial EDP (patient billing, report generation, financial applications)

With medical OEM's the main competition comes from IBM, Data General and Honeywell. Hewlett-Packard is becoming very active in this area. In medical administration the strongest competitors are Hewlett-Packard, IBM, and NCR.

ESG, Engineering Systems

Their users specialize in

a. aerospace design
b. automotive design
c. chemical engineering
d. electronic/electrical design
e. engineering consulting
f. architectural and engineering design

A general purpose timesharing system is required with strength in the area of scientific computation.

Competition comes mainly from Data General, Hewlett-Packard, PRIME, CDC, and IBM. Sometimes Harris and Interdata are seen.

ECS, Education

Their users, always conscious of system price, prefer a general purpose timesharing system for large numbers of users with specialties as noted:

a. school district students -- BASIC programs (small-scale problem solving, little I/O); good text editors, fast compile, debuggers for program development; not production.

b. university students -- technically sophisticated; more FORTRAN than BASIC; heavy text editing; large, complex FORTRAN and COBOL programs.

c. university departments -- variety of languages; some large FORTRAN programs.

d. school administration -- RJE required to installed main frame; high performance COBOL, some data management; administrative usage is growing; on-line, interactive applications; need application packages.

e. private college administration and students -- good COBOL and data management plus applications packages for administration; students need BASIC, FORTRAN, COBOL.

The competitors of ECS are IBM, Harris, PRIME, Hewlett-Packard.

GSG, Government Systems

Their users are from every organization within Federal governments around the world. The needs of these users cover every market segment described above. In the United States, particular emphasis is given to users in

a. military intelligence -- scientific and real-time computation; extensive PDP-11 experience to migrate.

b. civilian agencies -- with competitive procurements and long systems lifetime (5-8 years), systems require wide range of capabilities and low life cycle cost; interface to other mainframes (IBM, CDC, UNIVAC).

Generally, the competitors of GSG are IBM, Univac and Honeywell. SEL also does considerable U.S. Government business. For governments in countries outside the U.S., competition is usually seen from any vendor native to the country.

3.3.2 COMMERCIAL GROUP

COEM, Commercial OEM

Their users acquire systems intended for operation with specialized applications packages, e.g., business office management (wages and payroll, accounts payable, general ledger), customer billing, order entry and inventory control, sales analysis. Many of these systems are sold to small manufacturing and distribution companies and to lawyers, accountants, physicians, and dentists.

Competition for COEM comes primarily from IBM, Wang, and Basic Four in addition to DG and HP oems.

CSI, Commercial Service Industries

Their users work in

a. banks, insurance companies, financial institutions
b. data services companies
c. transportation companies
d. state and local government
e. retail business
f. service business

Many of these users require general purpose commercial EDP systems. A low-cost subset of the general purpose system can be geared to users in the small business community. Transaction processing is becoming extremely important to these users as is real-time computation for communications and sensor-based applications. Data service companies are interested in general purpose timesharing.

Competition is very strong from IBM at the account level. Other competitors are Hewlett-Packard, Data General, Honeywell, Tandem, NCR, PRIME, Computer Automation, and Burroughs.

MDC, Manufacturing Distribution and Control

Their users are found in

a. manufacturing companies
b. process industries

Required is a general purpose timesharing system to be used mainly for host development of software for smaller -11 based production systems running RSX-11M or RSX-11S. This general purpose system must have a good FORTRAN with an easy-to-use file system plus COBOL for data processing activities such as inventory control and materials scheduling. Real-time computation is becoming a requirement for more of these users.

Competitors for MDC are IBM, Tandem, SEL, Perkin-Elmer (Interdata), and Harris. Hewlett-Packard is beginning to enter this market area.

T&UG, Telephone & Utilities

Their users are involved with

a. telephone equipment manufacturers -- real-time computation, general purpose timesharing for development of specialized applications (e.g., traffic monitoring, billing data collection, repair order administration)
b. operating telephone companies -- general purpose commercial EDP with emphasis on communications with IBM mainframes.

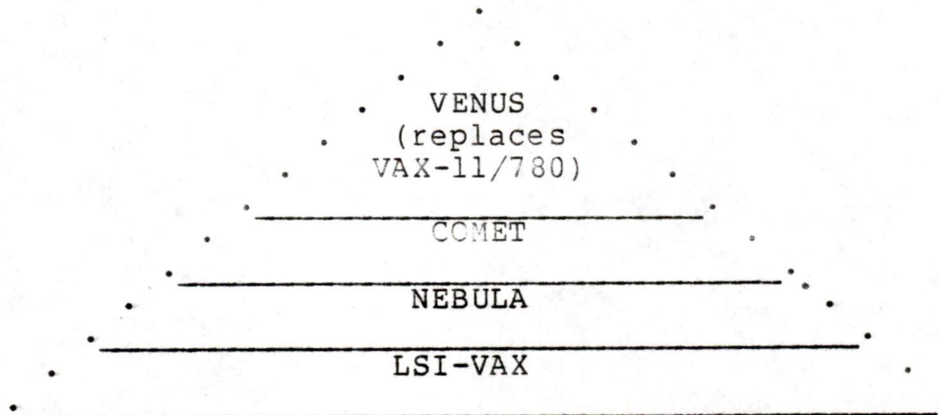
Competition comes from Interdata, especially at Bell Labs. IBM and Hewlett-Packard are competitors in the operating companies. Tandem is a potential competitor.

4.0 PRODUCT STRATEGY AND OBJECTIVES

VENUS is a high performance computer system product which implements the VAX-11 architecture and runs the VAX/VMS operating system with its associated layered software products. The MLP ($) design center of VENUS is the same as that of the VAX-11/780. Increased system performance is achieved by applying state-of-the-art technology (e.g., Mosaic ECL Array Technology) to the VAX-11 architecture.

In the FY82-FY85 timeframe VENUS is at the top of a pyramid of VAX family distributed data processing products in terms of

- o general purpose computing capability,
- o cost and performance
- o ease of interconnection to and strict compatibility with all other members of the pyramid.



VENUS will remain as a product offering until FY87 although a new, higher performance processor might be introduced in the FY85/86 timeframe.

As the VAX-11/780 replacement, the VENUS product is consistent with the corporate strategy which calls for a single 32-bit system architecture by 1985. Furthermore, VENUS will augment the VAX family of 32-bit products in a fashion which is consistent with the corporate goal calling for concentration on systems priced at $250,000 or less.

In a single processor configuration or in distributed processing configurations, VENUS provides the functional base for scientific and real-time computations, transaction processing, general purpose commercial EDP, and general purpose timesharing. VENUS can also be utilized in HYDRA multi-processor configurations (high availability, non-stop computing systems).

VENUS systems comply with the constraint of having VAX/VMS serve as the single operating system for the entire VAX family. A vast array of layered software products (such as COBOL, FORTRAN, DATA BASE MANAGEMENT), system options (such as TRANSACTION PROCESSING, HIGH AVAILABILITY modules), and applications will be offered. These will be VAX/VMS system add-ons in much the same fashion as, for example, disk and tape hardware sub-systems are field add-ons at an existing customer installation.

5.0 PRODUCT REQUIREMENTS

The VENUS system product will satisfy the market requirements outlined above. Priorities to guide the development of this product are given below (in descending order of importance):

- o Design center at $180K MLP with performance at 3.5 times VAX-11/780
- o New I/O architecture based on ICCS, HSC50, and MERCURY
- o SBI capability for -11/780 migration
- o FCS in Q1FY82; volume in Q2FY82
- o Entry level system at $99K MLP
- o Significant RAMP improvements
- o System options
- o Large system

The capabilities and functions to be developed for VENUS-based systems according to these priorities are illustrated by the following chart.

VENUS PRODUCT REQUIREMENTS

	ENTRY LEVEL SYSTEM *	DESIGN CENTER SYSTEM *	LARGE SYSTEM	MAX. CONFIG.
CPU with CIS warm floating point(includes G and H)	yes	yes	yes	yes
ECC MOS Memory	1MB	4MB	16MB	32MB
Vector Processor	none	none	1	1
Disks	2 x 40-50MB, removable	600MB, fixed or fixed/ removable	4 x 600MB, fixed or fixed/ removable	4 x 600MB, fixed or fixed/ removable
Mag tape	none	1600/6250 bpi, 125ips	2 x 6250 bpi, 200ips	4 x 6250 bpi, 200ips
Console with terminal plus dual load device	yes	yes	yes	yes
Asynch lines	8	8	128 (MERCURY)	512 (MERCURY)
Line Printer	none	none	1	1
Card Reader	none	none	1	1
SBI	none	none	none	2
ICCS	1	1	2	4
Remote diagnostics, console port	yes	yes	yes	yes
Cabinetry, power supplies	single cabinet w/exp.space	single cabinet w/exp.space	TBD	TBD
On-line diagnostics, UETP	yes	yes	yes	yes
VAX/VMS	yes	yes	yes	yes
Languages	1	any (not in $180K)	any	all
MLP	$99K	$180K	TBD	TBD

*Note expansion possibilities under discussion of Priority #1 and #5.

PRIORITY #1: Design center at $180K MLP with performance at 3.5 times VAX-11/780.

With an MLP of $180K, the system transfer cost is $40K (based on MU=4.5).

The basic components of this dock merge system product are:

- CPU with CIS and warm floating point (including G and H)
- 4MB ECC MOS memory
- 600MB disk mass storage; fixed or fixed/removable media
- 1600/6250 bpi, 125 ips magnetic tape subsystem
- Console, including terminal and dual load device for software patches, software distribution
- 8 asynchronous lines
- ICCS I/O bus
- Remote diagnostics with console port
- Cabinetry, power supplies
- On-line diagnostics, UETP
- VAX/VMS operating system (language licenses not included in the $180K)
- Expansion space in this single cabinet for
  - 4MB ECC MOS memory (additional)
  - 24 asynchronous lines (additional)
  - 1 line printer
  - 1 card reader
  - 6-8 synchronous lines
  - 1 accelerator (FORTRAN or COBOL)

Note that the $180K MLP covers the pre-wiring for these expansion components only and not the components themselves.

The configuration rules for this design center system and for all other VENUS-based systems must be easily stated and must be subject to easy verification by all sales people.

Performance at 3.5 times VAX-11/780

FORTRAN and COBOL --

The best FORTRAN and COBOL performance must be

FORTRAN = 3032 = 370/168

COBOL = 3032 = 370/168

This performance can be achieved via accelerators or any other engineering option.

When these high-performance capabilities are removed from the system, the performance is at the 3031 or 370/158 level.

FORTRAN is measured using the Whetstone and SP1111 benchmark programs. The performance for data types F, D=G, and H should each meet these goals compared to the corresponding IBM data types.

COBOL is measured using the U.S. Steel and Profile benchmark programs. The performance for display, binary, and index subscripts and for trailing overpunched and packed decimal data should each meet these goals compared to the corresponding IBM measures.

Real-time --

Times for context switching, CALL, and response to/service of interrupts must be at least 3 times faster than the speedier of COMET and VAX-11/780.

Throughput --

Memory bandwidth for VENUS must be at least 30MB/second with access times much faster than those of the -11/780. Further, a VENUS system configured with the new ICCS I/O bus must be capable of handling the equivalent of 4 UNIBUSes plus 8 MASSBUSes in addition to the maximum allowable number of intersystem connections. This assumes that the ICCS bus also supports (via MERCURY) line printer, card reader, asynchronous and synchronous communications lines, customer real-time devices, and slow-speed mass storage units. For availability reasons, it must be possible to configure a single VENUS system with at least two ICCS busses.

Delays in development --

Should the time to market goal not be met, it is required that all performance specifications given above will increase by 30% per year.

Availability of performance data --

An extensive set of performance measurements tasks must be done to provide data that is relevant to customers in the respective market segments. These performance analyses must be completed with results available by the time of VENUS product announcement. Such performance measurement projects must continue throughout the lifetime of VENUS in response to its changing environment (e.g., in terms of new DIGITAL products and competitors' new offerings).

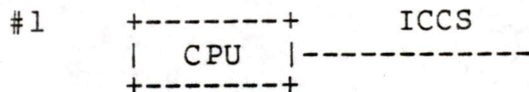
PRIORITY #2: New I/O architecture based on ICCS, HSC50, and MERCURY

VENUS will have the new I/O architecture based on the ICCS bus, the HSC50 mass storage controller for disk and tape, and the MERCURY intelligent communications subsystem for asynchronous and synchronous lines and for unit record equipment.

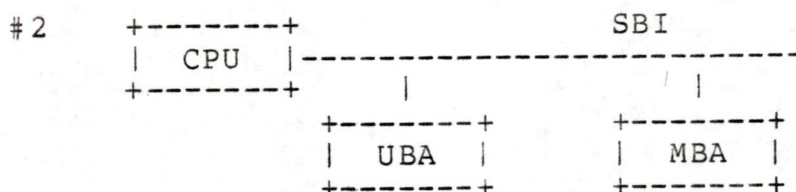
PRIORITY #3: SBI capability for -11/780 migration

To facilitate migration of the current VAX-11/780 customers to VENUS, ports for UNIBUS and MASSBUS devices must be provided via the SBI interface.

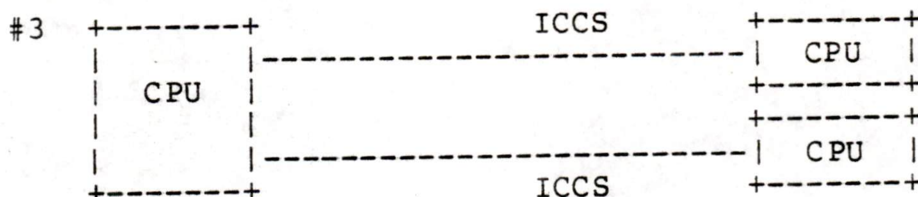
Under the above two priorities (ICCS and SBI capabilities), the various i/o configurations for VENUS systems and the priorities for their development are:



For the design center system and the entry level system. This must be available at FCS.

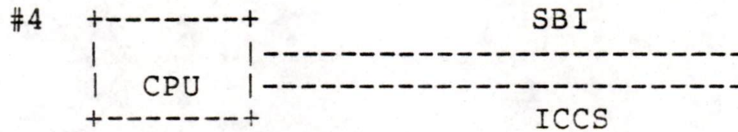


For -11/780 customers wanting an upgrade to a system with a more powerful central processor but with support for existing peripheral devices (via the UBA and/or MBA). This must be available at FCS.

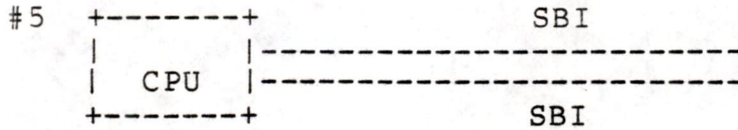


For customers with a distributed processing operation comprised of high-performance connections among intelligent subsystems. These high availability, high reliability systems will be suited for transaction processing, real-time computation, and general purpose timesharing off-loaded from a mainframe. This I/O configuration is part of the VENUS/HYDRA configuration and must be available at FCS.

DIGITAL EQUIPMENT CORPORATION
COMPANY CONFIDENTIAL



For customers (especially OEM) needing a system with a link to the past (via the SBI) and to newly-developed products (via the ICCS).



Again for -11/780 customers wanting a more powerful central processor but with increased i/o performance using existing peripheral devices.

DIGITAL EQUIPMENT CORPORATION
COMPANY CONFIDENTIAL

PRIORITY #4: FCS in Q1FY82; volume in Q2FY82

The VAX-11/780 product was announced in October, 1977 with FCS in December, 1977 (Q2FY78). Assuming the need for a replacement product every 3-4 years, the desired announcement date for the VENUS product is Q3 or Q4FY81. First customer shipments will follow in Q1FY82. Volume shipments will be reached by Q2FY82.

To summarize the key dates for VENUS:

Announcement of design center product	Q3/Q4FY81
First customer shipment (FCS)	Q1FY82
Volume availability	Q2FY82
Availability of	
Entry level system	FCS + 3 months
Vector processor	FCS + 6 months
Large system	FCS + 9 months

PRIORITY #5: Entry level system at $99K MLP

The entry level system is aimed at cost-sensitive applications. At a $99K MLP, this system permits a marketing campaign based on pure system cost. With an MLP of $99K, the system transfer cost is $22K (based on MU = 4.5).

The entry level system is bounded. Expansion is allowed but only at a price which does not disturb the product's design center business.

The basic components of this dock merge system are:

- CPU with CIS and warm floating point (including G and H)
- 1MB ECC MOS memory
- 2 x 40/50 MB ea. disk drives (removable media)
- Console, including terminal and dual load device for software patches, software distribution
- 8 asynchronous lines
- ICCS I/O bus
- Remote diagnostics with console port
- Cabinetry, power supplies
- On-line diagnostics, UETP
- VAX/VMS operating system with license for one language
- Expansion space in this single cabinet for
  - 1MB ECC MOS memory (additional)
  - 8 asynchronous lines (additional)
  - 1 line printer
  - 1 card reader
  - 6 x 40/50MB ea. disk drives (removable media)
  - 2 synchronous lines
  - 1 accelerator (FORTRAN or COBOL)

Note that the $99K MLP covers the pre-wiring for these expansion components only and not the components themselves.

PRIORITY #6: Significant RAMP improvements

VENUS development must expand on the RAMP designed and implemented for the VAX-11/780. The BMC of the resulting product must not exceed 1.5% of its transfer cost. RAMP plans should include software warranty and installation cost goals. RAMP must be considered according to the customer's perception of a total system, e.g., Are spares available when needed? Can troubleshooting be done without taking the entire system down? Is field software support responsive? Did the system product undergo enough quality assurance testing?

Improved RAMP is necessary for at least two reasons:

1. Customers are demanding highly reliable systems. They are becoming increasingly intolerant of computer system interruptions which wreak havoc throughout their organization.

2. With the growth of distributed data processing systems, customers will see growing maintenance costs for the many system processing units that are spread across a wide geographical area. Customers will not pay these high service costs. Furthermore, system vendors will be unable to provide a sufficient (and large) number of capable service personnel for such maintenance.

For VENUS, undetected failures must be minimized, and the total unrecovered system crash rate must be reduced. The latter includes all crashes attributed to environmental causes, operational procedures, software, hardware, and unexplained failures.

The MTBF must be increased significantly from that of the -11/780. Further, the total unproductive time per year must be reduced drastically. This includes, but is not limited to,

1. hardware preventive maintenance
2. software updates and maintenance
3. disk backup operations
4. emergency system maintenance
5. time spent waiting for parts
6. the ambiguous time during repetitive and undetected failures (especially for service calls which do not isolate the problem cause)

It is expected that reducing non-productive time will require significant changes in operational and service philosophies.

As part of the VENUS RAMP, consideration should be given to those features available from the HYDRA learning experience. Examples are redundant power supplies and fans plus devices with redundant access paths.

PRIORITY #7: System options

To meet the requirements of the marketplace, the VENUS system product will have several options as listed below. These options must be included in VENUS from the start of product design and development. Availability to the marketplace is noted here as "FCS+n" in months.

Hardware --

Availability	Category	Option
(FCS+9)	32MB max. ECC MOS memory (system total)	
(FCS+12)	I/O busses:	max. of 4 ICCS
(FCS+12)		max. of 2 SBI each with up to 2 UBAs plus 4 MBAs
(FCS)	disks:	600 MB, fixed media
(FCS+3)		40-80 MB, removable media; optional dual channel access for both
(FCS+9)	tapes:	6250 bpi, 200 ips, auto load, radial bus, dual channel access (optional)
(FCS)		1600/6250 bpi, 125 ips
(FCS)	unit record equipment:	line printer (IBM quality, VFU, DMA)
(FCS)		card reader (DMA)
(FCS)	processor options:	FORTRAN (accelerator)
(FCS)		COBOL (accelerator)
(FCS+6)		Vector processor
(FCS)		UCS, KMC (or equivalent)
(FCS)		MA780 (including COMET shared memory systems)
(FCS)		DR780
(FCS)	terminals:	multi-drop terminals for TP
(FCS)		VT100-based terminals
(FCS)		PDT terminals
(FCS)		GIGI terminal
(FCS)		Typeset terminals
(FCS)		terminal clusters

Communications --

Availability	Option
(FCS)	DECnet
(FCS)	X25
(FCS)	Interconnect to IBM, CDC, UNIVAC
(FCS)	MERCURY communications controller
(FCS)	DMA/buffered asynchronous and synchronous lines

Software (native mode) --

(FCS)	SORT/MERGE	(FCS)	Interactive BASIC-PLUS
(FCS)	APL with file system	(FCS)	BASIC-PLUS-2
(FCS)	PL/1	(?)	ADA
(FCS)	PASCAL	(FCS)	CORAL-66
(FCS)	BLISS-32	(?)	PEARL
(FCS)	RPG II	(FCS)	MUMPS
(?)	ALGOL	(?)	LISP

Note for all new languages: compliance with existing ANSI-standard language specifications; validated compilers.

(FCS) Symbolic debuggers for all languages
(FCS) Language support for vector processor
(FCS) DBMS-32
(FCS) DATATRIEVE-32 (inquiry language, report writer)
(FCS) TRAX-32
(FCS) Forms language compiler, debugger
(FCS) Message control with transaction roll forward/backward, journalling, shadow recording
(FCS) Multi-volume disk files
(FCS) ANSI-standard mag tape handling routines
(FCS) IBM mag tape handling
(FCS) Routines for graphics displays and plotters
(FCS) Math library
(FCS) Routines for performance measurement, network tuning, applications program tuning
(FCS) System resource accounting
(FCS) Resource allocation, quotas, scheduling (especially by JOB class); all in BATCH also
(FCS) Support routines for office automation (interface to remote word processors, backup storage for large documents, document interchange utility, electronic mail)
(FCS) Routines for RSTS migration (emulators, conversion utilities)
(FCS) Cross-system development for RSX-11M, -11S, RT-11, RT2.

General --

(FCS) Node in a HYDRA configuration
(FCS) 512 simultaneous educational users (BASIC-PLUS on a single-processor system)
(FCS) System-/network-wide data dictionary, data directory
(FCS) H/W, S/W support of all devices on -11/780, COMET, NEBULA, HYDRA, FONZ, SCS, PDT.
(FCS) Additional operator consoles

PRIORITY #8: Large system

The components of this system are:

- CPU with CIS and warm floating point (including G and H)
- 16MB ECC MOS memory
- 4 x 600 MB disk mass storage; fixed or fixed/removable media; dual channel access
- 2 x 6250 bpi, 200 ips magnetic tape; auto load; dual channel access
- Console, including terminal and dual load device for software patches, software distribution
- 128 asynchronous lines (MERCURY)
- 2 x ICCS I/O bus with two (2) ICCS ports connected to VENUS, COMET, or NEBULA processors
- 2 synchronous lines to IBM or CDC (MERCURY)
- 1 line printer (MERCURY)
- 1 card reader (MERCURY)
- Vector processor
- Remote diagnostics with console port
- Cabinetry, power supplies
- On-line diagnostics, UETP
- VAX/VMS operating system with FORTRAN, COBOL, PL/1, BASIC, DBMS, PASCAL

6.0 PRODUCT ASSESSMENT

6.1 Market Fitness and Competitive Goodness

The potential for success of the VENUS system product in its marketplace is summarized below:

MARKET SEGMENT	ASSESSMENT
Scientific Computation	Excellent
Real-time Computation	Excellent
Transaction Processing	Very Good
General Purpose Commercial EDP	Very Good
General Purpose Timesharing	Excellent

Against the competitive products either currently offered in the market or else known to be under development for release during VENUS' product life, VENUS should be a very strong performer for DIGITAL, especially in the traditional market segments (scientific, real-time, general purpose timesharing). The challenge will be to achieve the same level of excellence for transaction processing and for general purpose commercial EDP. By and large, success here depends upon our ability

1. to develop a considerable number of software products in time for the VENUS announcement and shipment;

2. to gain TP and commercial experience and to build a reputation as a viable vendor of high-end commercial-oriented products;

3. to understand how to win a sizable share of these two markets which are now dominated by extremely strong, well-entrenched competition.

Particular attention must be given here to the competitive challenge of IBM in all our market segments. With the coming H-series to complement their current 4300-series, the 8100, and the System/38, IBM will appear to have a comprehensive product offering aimed specifically at the distributed processing marketplace. The best resources of DIGITAL will be required to beat back this challenge with a rich array of products that can win wide customer acceptance.

6.2 VAX Family Product Positioning

As stated earlier, VENUS is at the top of a pyramid of VAX family distributed processing products. A brief description of each product is given below.

VENUS

- High end of the VAX family.
- VAX-11/780 replacement.
- Top of distributed computers hierarchy.
- General purpose capabilities for Scientific and Real-time Computation, Commercial Data Processing, Time Sharing, BATCH.
- Basic system optimized for $180K sale price.
- Configurable in high availability topologies (HYDRA).
- Attack product for new customers and PDP-11 customers in the $150K-$300K average systems range.
- Migrate top end of 11/74-MP business to VENUS.

Competition for VENUS is

IBM 303X, 370, 4300
CDC Cyber
Burroughs
NCR
Honeywell
SEL

COMET/HYDRA

Mid-range VAX family product at center of corporate business ($50K-$80K) for single processor applications.

Main product for distributed data processing host machine at the department/group level.

Tailored by application of VMS software options to Scientific Computation, Commercial Data Processing, Real-time Computation, Time-sharing, or Transaction Processing environment.

Attack product for new customers and PDP-11 customers in the $50K-$150K range.

Attack product for non-stop systems.

Migrate low end of 11/780 business, some of 11/74-MP business, and top end of 11/44.

Competition for COMET/HYDRA is:

IBM Low end 370, 4331
HP 3000
DG M600
S250
DG 32-bit
PRIME
Tandem
Interdata
SEL

NEBULA

Low end VAX family product.

Optimized for $25K systems range.

Tailored to specific application by packaging VMS options.

Attack product for new customers and PDP-11 customers in the $20K-$50K range.

Migrate bulk of 11/34, 11/44 business.

Competition for NEBULA is:

IBM Series 1, 8100
HP 3000, HP 1000
DG S250 + New Series
PRIME
Microdata

LSI/VAX

Very low end VAX family product.
Optimized for personal, lab, and office use.
$8-$10K system.
Bottom of the distributed data processing pyramid.
Tailored to a specific function by packaging of VMS (sysgen out functions).
Migration for 11/04, LSI-11 business; co-exist with PDP-11 bounded systems.

Competition for LSI/VAX is:

DG Micro Nova
HP desk top
Microdata
Intel
Wang

6.3 Compatibility with DIGITAL Systems

The key compatibility issues relative to VENUS product development are:

1. VAX family architecture is maintained.

2. The strategy of one operating system, VAX/VMS, is maintained.

3. VENUS supports SBI ports to allow connection (with no changes) to the MA780 and DR780.

4. UNIBUS and MASSBUS ports are provided to facilitate migration of the current -11/780 customer base.

5. The new ICCS I/O bus structure is implemented in a uniform fashion across all family members.

6. The PDP-11 compatibility mode is maintained as in the -11/780.

7. It is possible to use the library of VAX diagnostics unchanged for all existing devices.

8. RSX-11M compatibility is maintained in emulator mode.

9. There is a continued convergence on a single on-disk structure (ODS II), file access method (RMS), and command language (DCL).

10. Tools will be developed to support VENUS-based RT-11 development of software for PDT clusters and the FONZ and also SCS-11 host development.

6.4 Product Development Assumptions

The VENUS product development assumes that VAX/VMS is the one operating system maintained for the entire family. Further, the VAX family architecture is maintained, and all implementations are consistent throughout the family.

In this product development, emphasis is placed on languages, data management, communications, ease of use, and system availability. VENUS is suitable as a node in a HYDRA configuration. DECnet is an integral and critical part of the VENUS product. X25 and interconnects to IBM, CDC, UNIVAC are integrated into continued VAX/VMS development.

Tailoring of hardware products to the VENUS marketplace is achieved by adding layered software products and/or boot-time selecting VAX/VMS as appropriate.

6.5 Product Development Risks

A major risk involves timely development of several software products required especially by the commercial-oriented market segments. The significant challenge of this product development is being met today. Major software development projects are currently underway. Others are in the planning stages and require corporate funding and commitment of resources.

The design center and entry level systems depend on the availability of mass storage subsystems (disk and tape) that are significantly more cost-/performance-effective than our current product offerings.

VENUS is the first DIGITAL product scheduled to use the Mosaic ECL Array technology. Originally VENUS development plans had included the opportunity to learn from the DOLPHIN experience with the MCAs. Their extensive diagnostic capability will contribute heavily to achievement of VENUS' higher RAMP goals.

To achieve the higher RAMP goals, significant changes must be made in the philosophies governing hardware/software design and implementation and system support in the field.

APPENDIX A: VENUS Systems

Representative configurations of VENUS systems are:

1. 1MB memory
   ICCS bus
   2 x RL04 via UDA
   8 asynchronous lines
   VMS + one language
   $99K MLP (entry level system)

2. 2MB memory
   SBI
   RM/RA80 via MBA
   TU77
   8 lines
   VMS

3. 4MB memory
   ICCS bus
   RP08 via HSC
   TU78
   8 lines
   VMS (no languages)
   $180K MLP (design center)

4. 16MB Memory
   2 x ICCS bus
   4 x RP08 via HSC
   4 x TU78
   128 lines (MERCURY)
   VMS

5. 2 x System #2
   1 MA780 with 1MB memory (esp. for OEM)

6. 2 x System #4 with 256 lines total (this is VENUS/HYDRA)

APPENDIX B: Preliminary Product Forecasts and Assumptions

In late December 1978 Al Avery and Peter Conklin prepared a forecast of VENUS units covering FY82-FY85. The forecast amounts for all high-end mid-range systems (-11/70, -11/74, -11/780, and VENUS) were derived and appear here with the assumptions of the forecasting exercise.

FORECAST

	78	79	80	81	82	83	84	85
Corp. NOR ($G)	1.44	1.87	2.43	3.16	4.11	5.34	6.94	9.02
15% of NOR ($M)	216	280	365	475	615	800	1040	1350
Units:								
11/70 + 11/74	1400	1800	1800	1600	1000	500	100	0
11/780	35	550	1000	1500	1800	1500	900	400
VENUS	0	0	0	0	400	1800	3600	5900
TOTAL UNITS ---	1435	2350	2800	3100	3200	3800	4600	6300
Discount:								
11/70 + /74 (%)	15	----	----	----	----	----	----	----
11/780 + VENUS (%)	11	11	11	13	15	12	12	14
NOR:								
11/70 + /74 ($M)	180	260	260	230	145	70	15	0
/780 + VENUS ($M)	6	117	220	325	470	730	1025	1350
TOTAL NOR ($M)	186	377	480	555	615	800	1040	1350

APPENDIX B: (continued)

ASSUMPTIONS

1. High-end Packaged Systems = 15% of corporate NOR.

2. Corporate NOR grows at 30%/year compounded.

3. By the beginning of FY81, 11/780 has sufficient commercial functionality to pick up the high-end 11/70 commercial business.

4. DEC will have learned by the beginning of FY81 how to penetrate high-functionality commercial business.

5. No 16-bit products beyond 11/74 will be developed at the high end ($).

6. VENUS FCS = Q2/82; has all functionality: 3X performance @ +15% MLP. (NOTE: Requirements now are FCS = Q1FY82, Vol. = Q2FY82, 3.5 x -11/780 performance.)

7. VENUS is new market attack product; 11/780's continue to be built in whatever volumes are required to satisfy customer demands, namely, no great forced migration from /780's to VENUS.

8. OEM's and TELCO continue to buy high-end midi systems.

9. Discounts: 11/70 and 11/74 = 15% flat

10. Add-on business = 15% of average of previous two years NOR.

11. This forecast addresses the Mid-range Systems contribution to corporate NOR. Large Systems Group will be responsible for an updated forecast based on VENUS' replacement of current LSG products.

12. No analysis has been made here by the Product Lines to determine how the volume given above can be achieved.

APPENDIX C: Comparison Prices and Costs for VAX-11/780

Given here are the configuration, price, cost and BMC of VAX-11/780 packaged systems.

DESCRIPTION	FY80 MLP (M.U.)	FY80 Est. Transfer Cost	FY80 BMC (% XFER)
VAX-11/780 System, 512KB memory, 2 x RK07 (28 MB ea.), 8 asynch. comm. lines, and virtual memory operating system software.	$134,600 (x5.1)	$ 26,600	$748 (2.8%)
VAX-11/780 System, 512KB memory, RM03 disk pack (67MB), TE16 magnetic tape (1600/800 bpi, 45 ips), 8 asynch. comm. lines, and virtual memory operating system software	167,000 (x4.6)	36,100	783 (2.2%)
VAX-11/780 System, 512KB memory, RM03 disk pack (67MB), TU77 magnetic tape (1600/800 bpi, 125 ips), 8 asynch. comm. lines, and virtual memory operating system software.	177,000 (x4.3)	40,700	843 (2.1%)
VAX-11/780 System, 1MB memory, RP06 disk pack (176 MB), TE16 magnetic tape (1600/800 bpi, 45 ips), 8 asynch. comm. lines, and virtual memory operating system software.	207,000 (x4.8)	42,800	937 (2.2%)
VAX-11/780 System, 1MB memory, RP06 disk pack (176MB), TU77 magnetic tape (1600/800 bpi, 125 ips), 8 asynch. comm. lines, and virtual memory operating system software.	217,000 (x4.7)	46,500	997 (2.1%)
"UNIBUS" VAX-11/780 System, 256KB memory, 2 x RK07 (28 MB ea.), 8 asynch. comm. lines, and virtual memory operating system software. (system subject to corporate approval)	99,800 (x3.9)	25,300	698 (2.7%)

APPENDIX D: VAX Software Plans

This calendar was prepared by Peter F. Conklin

V A X   C A L E N D A R

HARDWARE

FY79	1979	FY80	1980	FY81	1981	FY82
		COMET: MA780, DR780		NEBULA: HYDRA-I (T), MERCURY (T)		VENUS (T), HYDRA-II (T)

OPER. SYSTEM

- Multi-User
- Real Time
- Interfacing
- Tunable
- Batch
- Operator
- Fast I/O
- Tapes
- Mount-Disks
- RMS
- English Messages
- M-V Disks
- Alloc. Ctrl.
- ISAM
- Resource Alloc.
- SMP Breadboard
- Disk Quotas
- MA780

LAYERED COMPONENTS

R1.0	R1.5	R2.0		R3.0 (T)		R4.0 (T)
COMPUTATION	COBOL-74	PASCAL	FORMS (T)	APLSF (T)		TRAX (?)
DECnet	SORT	BASIC +	3271 (T)	STEP (T)		
FORTRAN	BLISS	BASIC +2	FAST BACKUP (T)			
DATATRIVE	RPG-II	RSTS MIGR.I	NATIVE DATATR. (T)			
COMMON LANG.	GRAPHICS	DECnetIII	SNA (T)			
DEBUG	DX	MUX200	RSTS REPLACEMENT (T)			
DCL		APL	COBOL-79			
MCR		DECmail	PL/I (T)			
EDITORS		CORAL-66	TYPESET			
DIFFERENCES		KMC TOOLS	CATS (T)			
RUNOFF	2780/3780	MULTI-DROP	MERGE (T)		DIST.DATA MGMT (T)	
RSX MIGR.	WCS TOOLS			MUMPS (?)		
				PEARL (?)		
				X.25 (?)		
				LISP (?)		

```
+-------------------------------------------+
| (T)  =  Target, not yet phase 1 commit     |
| (?)  =  Possible; plans not firm           |
+-------------------------------------------+
```

APPENDIX E: Related Documentation

Existing documents that are useful for anyone working in VENUS product development and marketing are listed below:

1. VENUS Project Proposal (27 Dec. 1978)
   Contact Steve Jenkins, TW/C04, DTN #247-2395.

2. VENUS Product Description (20 Jan. 1979)
   Contact Steve Jenkins

3. VENUS Impact Statement (13 Feb. 1979)
   Contact Don Ames, TW/A02, DTN #247-2517.

4. VENUS Software Plans (10 Apr. 1979)
   Contact Peter Conklin, TW/A08, DTN #247-2119.

5. VAX/VMS R2.0 Requirements Document (Sept. 1978)
   Contact Kathryn Norris, TW/A08, DTN #247-2580.

6. System plan for VAX/VMS (10 Jan. 1979)
   Contact Joe Carchidi, TW/D08, DTN #247-2251.

7. VAX/VMS RELEASE TWO Project Plan (9 Feb. 1979)
   Contact Trevor Porter, TW/D08, DTN #247-2262

8. Commercial Market Product Requirements (March 1979)
   Contact Roger Cady, MK1-1/E25, DTN #264-5045.

9. NEBULA Product Requirements (Feb. 1979)
   Contact Lou Philippon, TW/A08, DTN #247-2860.

DIGITAL EQUIPMENT CORPORATION
C O M P A N Y C O N F I D E N T I A L

VENUS PRODUCT REQUIREMENTS - DISTRIBUTION LIST

Name	Location	Name	Location
Gordon Bell	ML12-1/A51	Robert Lane	MK1-2/B11
Ron Bingham	MR1-2/E85	John Leng	MR1-1/A65
Brian Croxon	TW/C04	Bill Long	ML10-2/A57
Art Campbell	PK3-1/M12	Si Lyle	MR1-1/M42
Roger Cady	MK1-2/E25	Ward MacKenzie	PK3-1/A60
Patrick Courtin	MK1-2/D29	Julius Marcus	MK1-2/C37
Dick Clayton	ML12-2/E71	Jim Marshall	TW/A03
Bill Demmer	TW/D19	Bob Nealon	MR2-4/F19
Raff Ellis	MR2-4/M79	Ken Olsen	ML10-2/A50
Ulf Fagerquist	MR1-2/E78	Stan Olsen	MK1-2/C36
Barbara Farquhar	MR2-4/M79	Stan Pearson	ML12-2/E71
Ed Fauvre	MK1-2/E06	George Plowman	ML5-5/E97
Jack Gilmore	MK1-1/J14	Larry Portner	ML12-3/A62
Rose-Ann Giordano	MR1-2/A65	Franco Previd	MR1-2/E18
Mike Gutman	ML3-6/E94	Dick Rislove	MK1-2/L35
Bill Heffner	TW/C10	Joel Schwartz	MR2-4/M51
Win Hindle	ML10-2/A53	John Shebell	MR1-1/S35
Per Hjerppe	MR1-2/E78	Jack Shields	PK3-2/A58
George Hoff	MR1-2/E47	Leo Shpiz	MK1-2/H32
John Holman	PK3-1/P84	Pete Smith	MR1-1
Irwin Jacobs	MK1-2/H32	Dick Snyder	MR1-2/E37
Bob Joseph	MR1-1/M42	Charlie Spector	ML5-2/A33
Paul Kelley	MR1-2/E18	Harvey Weiss	MR1-1/M85
John Kevill	ML3-6/E84	Jim Willis	MK1-2/H32
Bill Kiesewetter	MK1-1/M49	Jerry Witmore	PK3-1/M40
Bob Klein	MR1-1/M85		

MSD PRODUCT MANAGEMENT

Name	Location	Name	Location
Al Avery	TW/A08	Lou Philippon	TW/A08
Dave Best	TW/A08	Mike Powell	TW/A08
Walt Colby	TW/A08	Carol Reid	TW/A08
Peter Conklin	TW/A08	Marilyn Ressler	TW/A08
Marion Dancy	TW/A08	Tom Sherman	TW/A08
Bernie Lacroute	TW/A08	Ed Slaughter	TW/A08
Don McInnis	TW/A08	Mike Torla	TW/A08
Kathie Norris	TW/A08	Ed Wargo	TW/A08

MSD ENGINEERING

Name	Location	Name	Location
Don Ames	TW/A02	Ed McHugh	TW/E07
Joe Carchidi	TW/D08	Dave Potter	TW/C04
Dave Cutler	TW/D08	Wayne Rosing	TW/C03
Sas Durvasula	TW/C04	Steve Rothman	TW/D06
Tom Eggers	TW/C04	Dave Rodgers	TW/C04
John Gilbert	TW/E07	Bob Stewart	TW/C04
Al Helenius	TW/C04	Bill Strecker	TW/A08
Dick Hustvedt	TW/D08	Jim O'Loughlin	TW/E07
Steve Jenkins	TW/C04	Peter van Roekens	TW/E07
Jud Leonard	TW/C04	Linda Wright	TW/E07

digital

INTEROFFICE MEMORANDUM

TO: Design Review Attendees

DATE: March 12, 1980
FROM: Sultan M. Zia
DEPT: L.S.E.G.
EXT: 6277
LOC/MAIL STOP: MR1-2/E47

SUBJECT: MEETING REMINDER

This memo is to confirm the Venus Technology Design Review meeting scheduled for Wednesday, March 19, 1980, from 2:00 P.M. to 5:00 P.M., in the DEC10 Conference Room.

Attached is a copy of the agenda and some reading material on the Venus technology effort.

SZ/jrl
Attachment

VENUS TECHNOLOGY REVIEW - AGENDA

1.	OVERVIEW	SULTAN ZIA	2:00 - 2:15
2.	PACKAGING	JIM MCELROY	2:15 - 3:30
3.	POWER SYSTEM/ ENVIRONMENTAL CONTROL	CHUCK BUTALA DERRICK CHIN	3:30 - 4:15
4.	MCA	BILL WALTON	4:15 - 5:00
5.	FEED BACK & WRAP UP		5:00 - 5:30

MAR 13 1980

++++++++++++++++
!D I G I T A L!
++++++++++++++++

INTEROFFICE MEMORANDUM

TO: Gordon Bell

DATE: March 13, 1980
FROM: Sultan M. Zia
DEPT: L.S.E.G.
LOC: MR1-2/E47
EXT: 231-6277

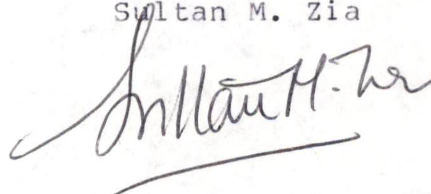
SUBJ: VENUS TECHNOLOGY CONCEPT REVIEW

Gordon,

I am holding this meeting on March 19, 1980, (it is in your calender) to review with key technical people in the corporation the basic design concepts that we are using in areas of packaging, power system and environmental controls. Also, we will be updating the reviewers on the status of the MCA.

We hope that you can make it to the meeting.

Sultan M. Zia



SZ/jrl
Attachment

C. MACRO PLACEMENT CONSIDERATIONS

The V_{CC} current is divided between the two V_{CC} pins. If an imaginary line is drawn between pin 43 and 9, the V_{CC} current to the top half of the array comes from pin 60 while the V_{CC} current to the bottom half of the array is connected to pin 26. When placing the macros in the array approximately half should be placed in upper or lower half. The bias network looks at the current in the lower half to determine proper bias voltages. In order to maintain the guaranteed noise margins, the power (due to V_{CC} current) in the upper half of the array should be within ±10% of the lower half.

follower. The library in Appendix A designates all macro inputs that go to an input follower with an *. The reason for the compensation network is to insure that the input will not oscillate due to negative input impedance. No compensation network is required on macro inputs that are not connected to a bonding pad.

There are 26 possible outputs from the array that must be connected to bonding pad pins 1 through 24 (not including pins 3, 9, 15, and 20) and pins 62 through 68 (not pin 66). If the array contains less than 26 outputs, then these pins can be used as inputs. The output emitter followers of the output cells are located next to these bonding pad pins. Pins 67, 68, 1, 2, 16, 17, 18, and 19 have two emitter followers at each pad. The driver of macro 016 or 017 (transceiver) can be routed from any output cell to one of the above pins in order to drive 50 or 25 ohm loads to -2 volts. All other macros can drive 50 ohms to -2 volts. Note that transistors Q6 and Q7 in Figure 9 are actually located near the bonding pad.

Figure 20 shows the location of the output emitter followers (OEF) from the output cell next to the bonding pads. Also shown is the location of the 100K ohm load resistors (L), and the compensation networks (RC).

B. EXTERNAL PIN USAGE

Figure 10 shows the pin configuration of the Macrocell Array. There are eight power pins and 60 logic pins. The ground, V_{CCO}, for the output followers of the Output cells is separated from the ground V_{CC}, for the rest of the logic. The current supplied to V_{CC} is rather constant while the current supplied to V_{CCO} changes when outputs are switching. The V_{CC} and V_{CCO} pins should be connected together to a good ground outside the package similar to normal MECL 10K grounding.

There is an input compensation network and a 100K ohm input pull down resistor located next to each of 36 bonding pads (pins 24 through 62, not including pin 26, 43, and 60). There is also a 100K ohm input pull down resistor located next to pins 4, 5, 6, 12, 13, 14, 21, 22, 23, 63, 64, and 65. There is a total of 48 100K ohm input pull down resistors with each located next to a bonding pad as indicated above. These resistors can be connected to their respective pad if it is used as an input so that an unconnected input pin will automatically be held in a logic low state. The input compensation network should be connected to its respective bonding pad pin if it is connected to an input

IV. MACROCELL ARRAY DESIGN CONSIDERATIONS

A. UNUSED INPUTS

Unused inputs in the array will automatically be forced to a low voltage (logic "0") by the CAD system (the input base is shorted to the emitter). There are no special provisions for providing a high voltage (logic "1") on an unused input. A logic "1" can be generated using a spare inverter from an interface on major cell.

The driver of the transceiver macros can drive 25 ohm or 50 ohm load resistors to -2 volts with a low voltage output, V_{OL}, in the cut-off mode, of -2 volts. The average power dissipation of the output transistor for the transceiver driver is 20mw for 25 ohm load or 10mw for 50 ohm load. The power dissipation of the receiver follower can be calculated by multiplying 5.2 volts times the output follower current.

The fan-in for the output macros is shown in parenthesis (in Appendix A). Normally, the fan-in is 3 for the upper tree input and 1 for the lower tree input. An exception is the inputs of the transceiver driver where the fan-in is 3. The upper tree input normally has to switch 3.5ma, while the input follower has to switch 1ma.

An output (Y1) is also available for driving internal loads. This output can be selected with an output follower current of 1 or 2ma.

Figure 9 shows a schematic of the transceiver macro 016. The current source for the driver is 8ma and the input follower current is 2ma. A diode is not placed in series with the input follower of the driver since it is not a series gated function and soft saturation cannot occur. The output transistors Q6 and Q7 are located near the bonding pad and not in the output cell. When the Y output of the cell is connected to the bonding pad via the CAD system, the collector of Q4 is actually routed to the bases of Q6 and Q7 with the emitters connected to the bonding pad. The load resistor, R4, is placed outside the package. For the receiver, the current source is 3.5ma. The output emitter follower current of the receiver can be selected for 0, 1, or 2ma.

The typical power dissipation, PD, specified in Appendix A does not include the output follower. Since the load resistor is placed outside the Macrocell Array package, only the power of the output transistor need be calculated. For 50 ohm terminations to -2 volts, the average power dissipation for the output transistor is 15mw.

C. OUTPUT CELL

The 26 output cells are located around the right half periphery of the array as shown in Figure 2. The output cell is used to interface to logic outside the chip by providing 50 ohm and 25 ohm drive capability. The output cell library (shown in Appendix A) provides macros with a similar logic capability as an interface cell (about ¼ the logic capability of the major cell).

Each output cell contains 15 transistors and 16 resistors as shown in Figure 8. These components are connected together on first layer metal to form logic functions with one full series gated structure. Two partial series gated structures can be formed in one cell for the transceiver macro functions.

The current source for output cell macros 0Ø1 through 015 is 3.5ma. The circuit configuration for a latch is similar to the interface configuration shown in Figure 7 except that only one output is available and resistor R1 is zero. The output emitter follower is located near the bonding pad. The input follower current is 1ma instead of .5ma (R8 and R9 in Figure 7). A diode, Q13, in Figure 7, is connected in series with the input follower on all lower level inputs (marked with *) of macros 0Ø1 through 015.

combinations. Very useful macros like IØ5, IØ6, IØ7, and I1Ø (where one input is inverted)are not available in standard logic families. Macros IØ6 and IØ7 together can be used to form a 1 of 4 decoder similar to M45 except an enable line is not present. Macros I13 and I14 together can be used to form a D flip flop similar to M31.

If both outputs are used an output follower current of .5 or 1ma may be selected in the CAD system. An output that is not used will not have a pulldown resistor. If only one output is used a 2ma current can be selected when driving a high number of fan-ins (>6) in order to minimize propagation delay degradation. A .5ma current can be used in non-critical delay paths. Note that the outputs are actually buffered through the output emitter followers (Q3 and Q4) and are not fed back directly as shown in the logic equivalent diagram.

The typical power dissipation, PD, specified in Appendix A does not include the output follower since different current values can be specified. The power dissipation of the output follower can be calculated by multiplying 5.2 volts times the output follower current.

The logic power of series gating can again be shown in Figure 7. The latch can be formed with only one series gated structure with a logic equivalent of four gates. Clamp transistors are not required in the interface macros since collector dotting occurs in only one series gated structure. All the inputs of the macros in the Interface cell library have a fan-in of 1. Dual gate functions are also available in the library in numerous

t_{pd}, from the D input to the Q or $\overline{Q}$ output is 1.3ns while the delay, t_{pd}*, from the E1 or E2 input to the Q or $\overline{Q}$ is 1.6ns. These values are for a 1ma output follower current (at R6 and R7) driving a fan-in of 3. The asterisk at the E1 and E2 input denote they are connected to an input follower which connects to the lower portion of the series gated current tree. The current source is 1ma which is formed by Q15 and R10. The bias voltages are the same as the major cells.

The input followers, Q11 and Q12, have an input follower current of .5ma. A diode, Q13, is placed in series with the input follower to insure that soft saturation cannot occur when interfacing to signals off the chip under worst case conditions. The diode increases the propagation delay by 100ps. Transistor Q14 is required to translate $V_{BB}1$ (due to the diode, Q13) with a current of .5ma through resistor R9.

For the latch, Q and $\overline{Q}$ are actually fed back to both sides of the differential amplifier, Q5 and Q6, in order to insure reliable operation. The logic equivalent shows only the Q output being fed back. Due to the feedback, a total of 1ma of current flows through R4 and R5.

B. INTERFACE CELL

The 32 interface cells are located around the left half periphery of the array as shown in Figure 2. In addition to input buffering, the interface cells provide about one-fourth the logic capability of the major cells. These cells can be utilized for input interfacing and to provide extra logic power within the array.

Interface cell macro outputs (as well as major cell macro outputs) can only be connected to internal macro inputs. These outputs do not have enough drive capability to drive signals off the chip. Only outputs from output cell macros can drive 50 ohm or 25 ohm loads.

Each interface cell contains 17 transistors and 13 resistors as shown in Figure 6. These components are connected together on first layer metal to form logic functions with one full series gated structure. Two partial series gated structures can be formed in one cell for dual gate macro functions. The Interface Cell Library in Appendix A lists the 14 macros and their characteristics.

Figure 7 illustrates the interconnection of the components to form a latch. The maximum propagation delay,

Emitter dotting of output transistors forms a wired-OR logic function. Emitter dotting of up to four outputs is allowed between cells in the array for a 2ma output follower current. Two outputs can be wired-ORed for a 1ma output follower current.

The fan-in for each input when greater than one is also specified in Appendix A. For the circuit shown in Figure 5, the fan-in of all inputs is 1 even though some inputs go to more than one base. When an input goes to two different bases at the top of one current tree, the fan-in (as far as propagation delay degradation is concerned) is considered to be 1. The reason is that the input driving the two bases has to switch a maximum of 1ma since only 1ma can flow into the current source Q17. If an input is connected to two different current trees (2 series gated structures) then the fan-in is specified as 2.

The value of series gating can be seen by the logic equation for the 4 input exclusive OR gate shown in Figure 5. To implement this function using gates would require eight 4-input AND gates plus one 8-input OR gate. Gates also might be required to form the true and complement of each input. About 40 connections would be required if gates were used as compared to five connections for the series gated macro.

The output drive capability to other macros on the chip is limited only by propagation delay degradation. Essentially, there is no limit due to DC conditions since the base current required per fan-in is only 20μ amps. Where performance is a premium a fan out of 12 should not be exceeded.

The typical power dissipation, PD, specified in Appendix A does not include the output follower current since different values can be specified. The power dissipation of the output follower can be calculated by multiplying 5.2 volts times the output follower current.

The logic power of series gating can be easily shown in Figure 5. Collector dotting in the top of the current tree (such as collectors Q3, Q5, Q8 and Q10) forms a wired AND logic function. Transistors Q1 and Q2 are used to clamp the voltage at the bases of Q19 and Q20 when more than 1ma must be supplied through resistors R2 and R3. When collectors of two different current trees are tied together, a clamp transistor is provided in order to maintain a proper "low" level at the output. Collector dotting is allowed only within the cell since any capacitance at the collectors will degrade propagation delays appreciably.

in Figure 2 while the master bias driver cell is shown at the bottom of the array. V_{CS} tracks with V_{EE} to maintain a constant current in the current source.

The input followers, Q11 and Q14, each have an emitter current of .5ma average for the input at B or D in the high or low state. The input follower current is about 10% higher when the input is in the high state and about 10% lower when the input is in the low state. If the input follower drives two current trees from one input follower (such as the clock lines of a D flip flop), the input follower current is normally 1ma.

The output follower current (through R8) can be selected by the designer for 0, .5, 1, or 2ma if two outputs or less are used per half cell. If four outputs per half cell are used the current can be selected for 0, .5, or 1ma. A 1ma current should be selected if the output is driving a fan-in of 3 or less in order to maintain the speed specified. A 2ma current should be selected for a higher number of fan-ins (>6) in order to minimize propagation delay degradation. Curves will be available in the design manual showing the degradation versus fan-out and output follower current. A .5ma current should be used, in order to save power, if the delay path is not critical.

A. MAJOR CELL DESCRIPTION

The major cells in the array comprise the internal area on the chip and are used for the majority of the logic capability. Each major cell contains 52 transistors and 48 resistors as shown in Figure 4. These components are connected together on first layer metal to form logic functions with four series gated structures operating on MECL 10K logic levels. Figure 5 illustrates the interconnection of the components to form a 4 input Exclusive OR gate (half cell of M11). The maximum propagation delay, t_{pd}, from the A or C input to the Y output is 1.5ns. This value is for a 1ma output follower current (R8) with the output driving a fan-out of 3. Similiarly, the maximum propagation delay, t_{pd}*, from the B or D input to the Y output is 1.8ns. The asterisk at the B and D input denotes that each input is connected to an input follower which connects to the lower level of the series gated current tree.

Outputs of the major cell macro can only drive inputs of other macros within the array. The current source for each current tree (in Figure 5) is 1ma which is formed by Q17 and R6 and Q18 and R7. The bias voltages are $V_{BB}1$= -2.1 volts, and V_{CS}= -4.0 volts. The 24 slave bias drivers are shown next to the major cells in three different columns

gates. If dual flip flops, M31, were used in all the major cells (a total of 96 flip flops at 7 gates per flip flop) instead of full adders, the array would contain 904 equivalent gates. The application example for 8 X 8 2's complement multiplier (see Application section) contains 888 equivalent gates with a 93% cell utilization.

Although the chip is large good yields are experienced since most of the chip is composed of metal for interconnecting the macros. The total emitter area of the active devices is the primary concern in determining the yield.

The macrocell array is voltage compensated so that V_{EE} can range from -5.2 volts ±10%. Thus, a system designed with the macrocell array can operate with a V_{EE} of -4.68 volts resulting in approximately 10% less power at the same performance.

The maximum operating junction temperature is specified at 165°C (the same as MECL 10K) with the package capable of dissipating 5 watts of power. A recommended heat sink and 1000 LFM of air flow result in a thermal resistance, θ_{JA}, of only 15°C/watt. The ambient temperature range is 0 to 70°C. More on the performance characteristics is discussed in Section E.

Material for Packaging Section of Venus Technology Review

A brief description of the material contained herein is provided to guide the reader to the areas of interest:

1. Two overview drawings are shown to depict the dual SBI and dual BI configurations. Of course the Unibus cabinet is also required for the SBI system.

2. C.G. Analysis of the enclosure.

3. Structual analysis of the power supply support frame.

4. A cross section through the CPU card cage shows the module/backpanel interface. Elements of the D.C. power distribution are also depicted.

5. Detailed view of dual SBI system backpanels.

6. Description of backpanel layup and construction.

7. Memo's describing ECL and TTL module density estimates.

8. Component placements for trial layout of FPA module.

9. Memo describing calculation for number of module ground pins.

10. Description of module layup and construction.

11. Description of MCA chip carrier & socket features.

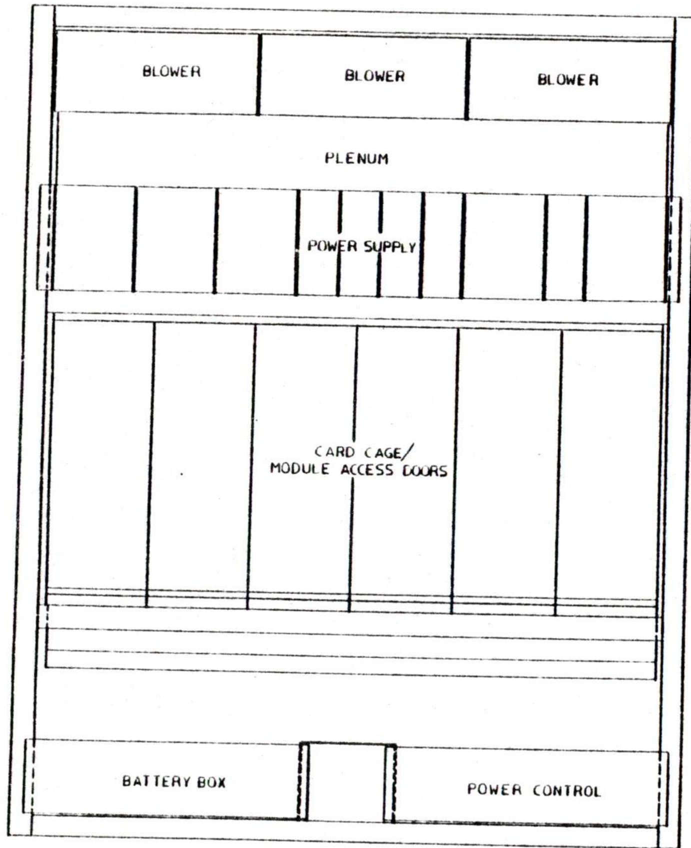
12. Report on MCA carrier/socket noise problem.

13. Report on thermal testing.

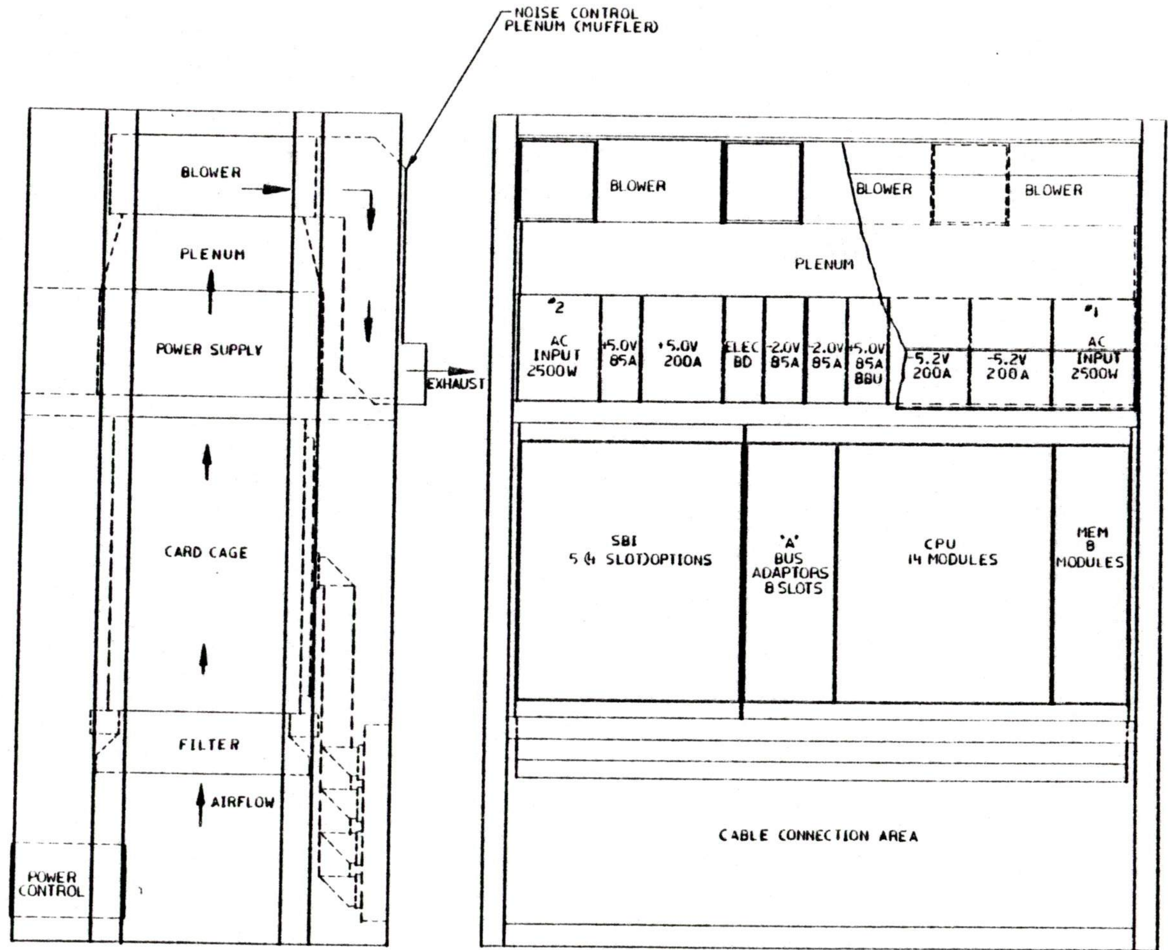
14. Report on accoustical testing.

NOTE:

FIRST PAGE OF EACH SECTION IS MARKED WITH CIRCLED NUMBERS CORRESPONDING TO ITEMS ABOVE.



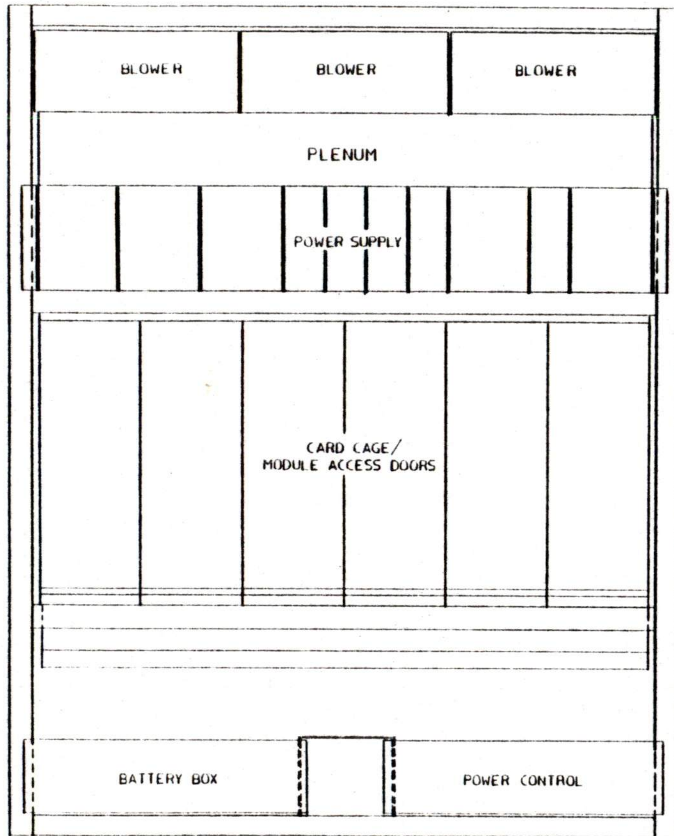
FRONT VIEW



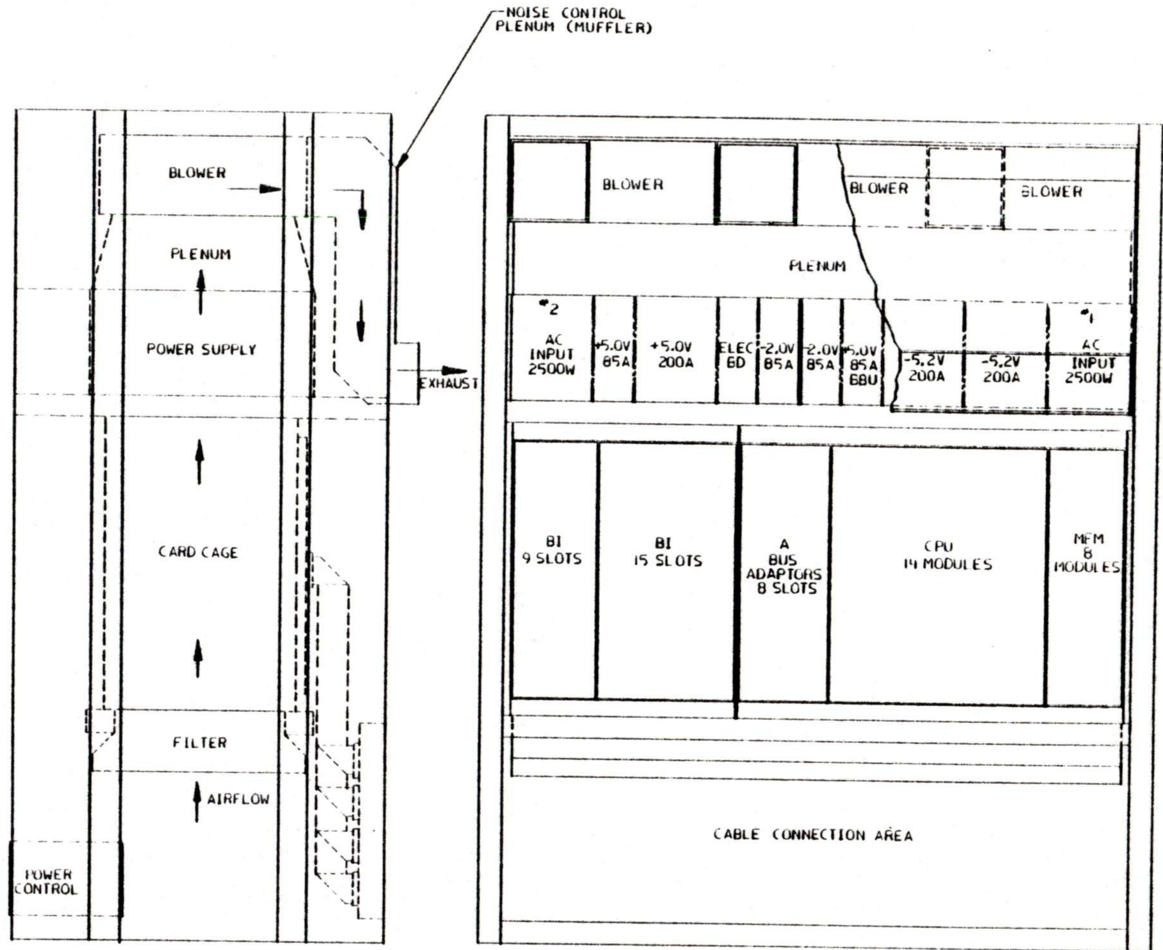
SIDE VIEW

REAR VIEW
BACKPLANE "PIN SIDE" SHOWN

VENUS EQUIPMENT CONFIGURATION 'C' SBI
SCALE: 1/4
26 FEB 80



FRONT VIEW



SIDE VIEW

REAR VIEW

BACKPLANE "PIN SIDE" SHOWN

VENUS EQUIPMENT CONFIGURATION "D" BI

SCALE: 1/4

27 FEB 80

Calculation of Venus CG

John M. Drake
10 March 80

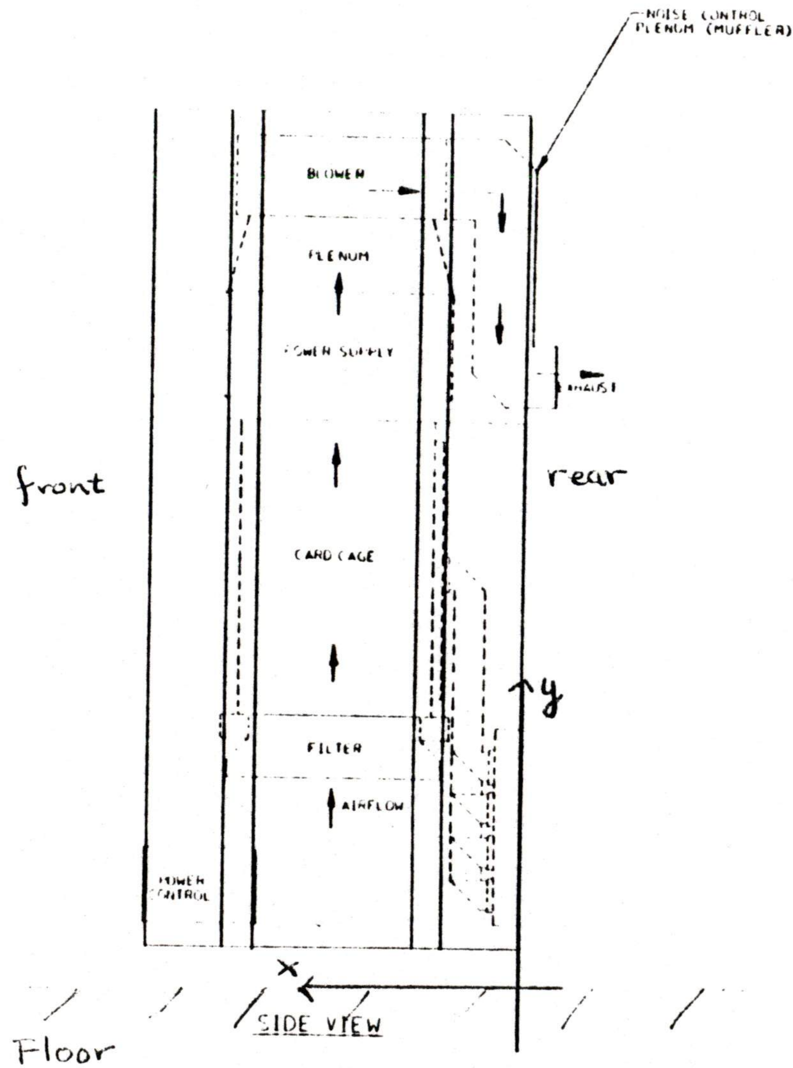
Estimated weights of Cabinet, components and their center of gravity positions relative to the origin (see figure on next page)

Component		Weight (lbs)	X_{cg} (in.)	Y_{cg} (in.)
Cabinet w/ covers	344 lbs			
crate	87 lbs			
total	431 lbs	431	12.5	32.0
Air movers 3 @ 25 lbs		75	12.4	57.2
Power supply		100	12.4	-3.2
Battery Box		21	21.4	6.5
Power Control		30	21.4	6.5
Card Cage (aluminum)	30 lbs			
Modules 14 @ 2.5 lbs	35 lbs			
36 @ 2.2 lbs	79 lbs			
Backplanes (w/ connectors)				
I/O	10 lbs			
CPU	10 lbs			
MEM	6 lbs			
Adaptor	5 lbs			
Backplane frame	15 lbs			
Module access doors*	10 lbs			
total	200 lbs	200	12.4	28.0
Plenum*		9	12.4	49.0
Exhaust Plenum*		25	1.5	[illegible]
Intake Plenum*		13	12.4	16.0
Steel tubing for mounts (6)		15	12.2	23.4
Cable connector panels		20	1.0	10.4

TOTAL	939 lbs	12.4 inches	32.6 inches

* Weight savings of 33 lbs total if aluminum is substituted for steel in these items.

Definition of Coordinate references



VENUS EQUIPMENT CONFIGURATION "D"
SCALE: 1/4

Calculations

$$\bar{x}_{cg} = \frac{\sum w_i x^i_{cg}}{\sum w_i}$$

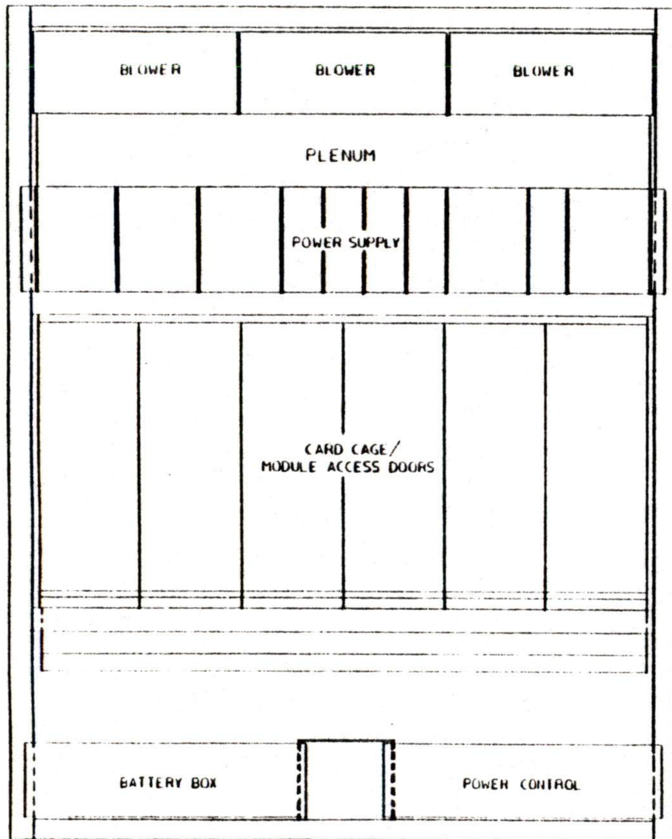
where w_i is the weight of the component located at x^i_{cg}.
Similarly,

$$\bar{y}_{cg} = \frac{\sum w_i y^i_{cg}}{\sum w_i} .$$

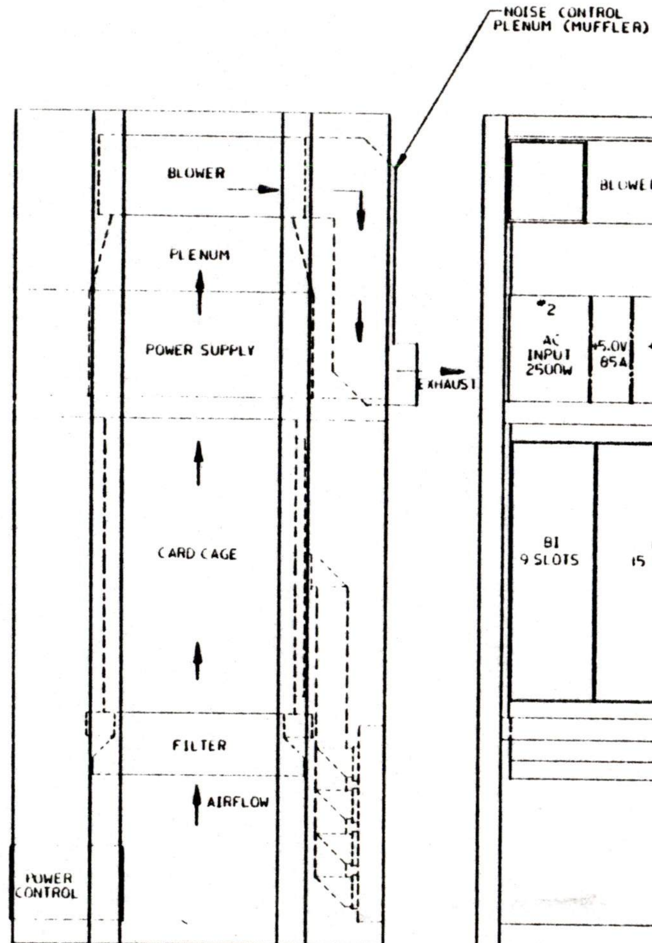
Using the weights and positions given in the table,

$$\bar{x}_{cg} = 12.4 \text{ inches}$$

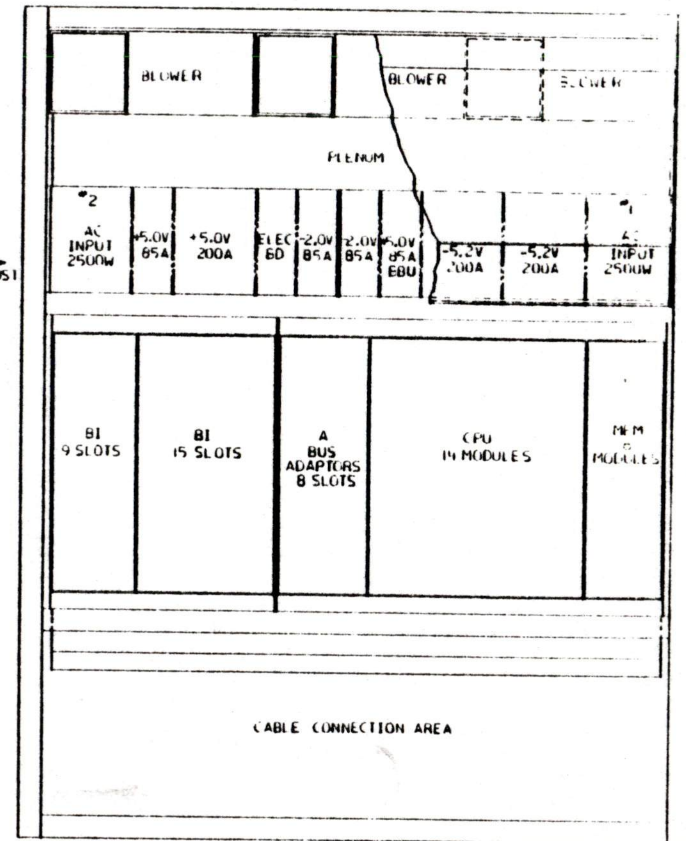
$$\bar{y}_{cg} = 32.6 \text{ inches}$$



FRONT VIEW



SIDE VIEW

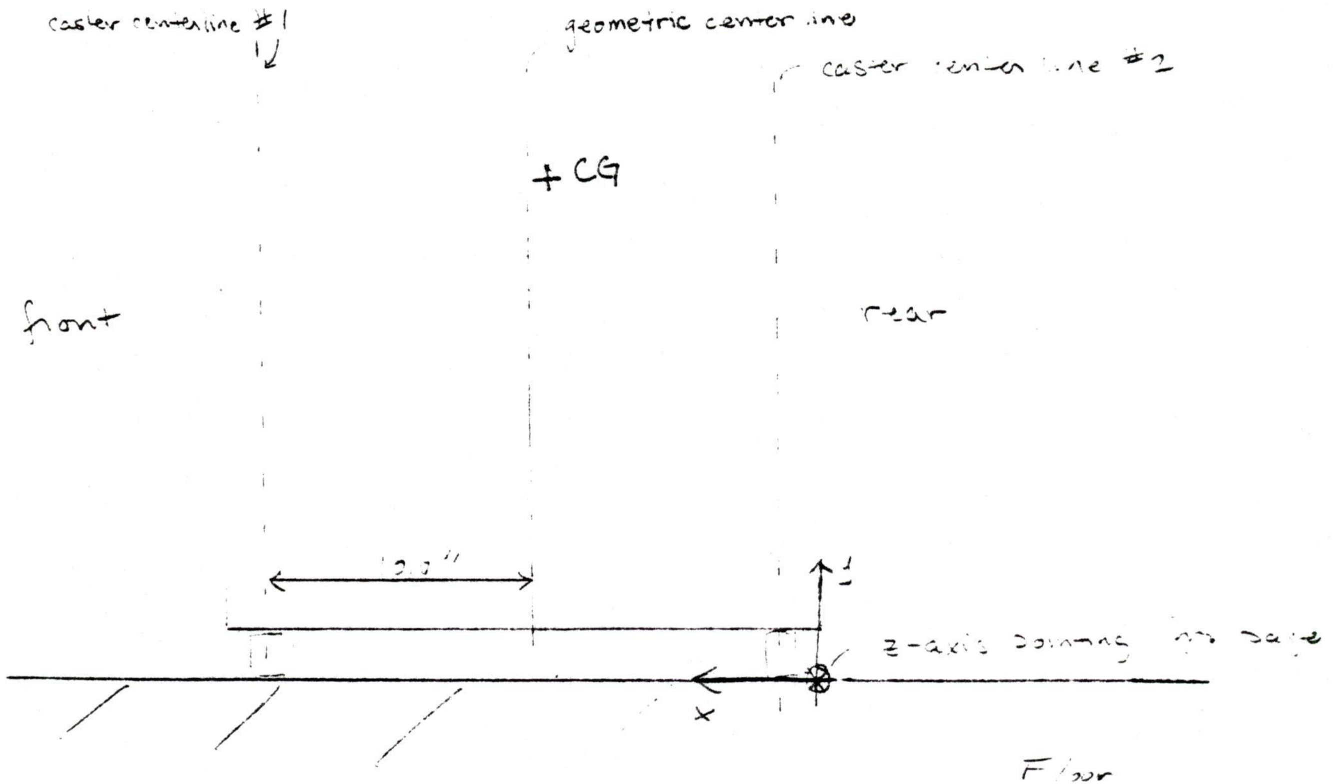


REAR VIEW
BACKPLANE "PIN SIDE" SHOWN

VENUS EQUIPMENT CONFIGURATION "D"
SCALE: 1/4
27 FEB 80

Calculations of Critical angles

Side View



Two critical angles will result from tipping around each of the casters.

$$\tan \theta = \frac{\text{distance between caster center line and cab CG}}{\text{distance from floor to cab CG}}$$

Case 1: Tipping about rear caster.

$$\tan \theta_1 = \frac{9.9 \text{ in}}{32.6 \text{ in}} = .303$$

$$\theta_1 = .295 \text{ radians} = 16.9^\circ$$

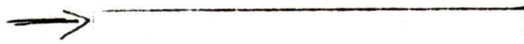
Case 2: Tipping about front caster.

$$\tan \theta_2 = \frac{10.1 \text{ in}}{32.6 \text{ in}} = .310$$

$$\theta_2 = .300 \text{ radians} = 17.2^\circ$$

Force required to tip stationary cabinet over.

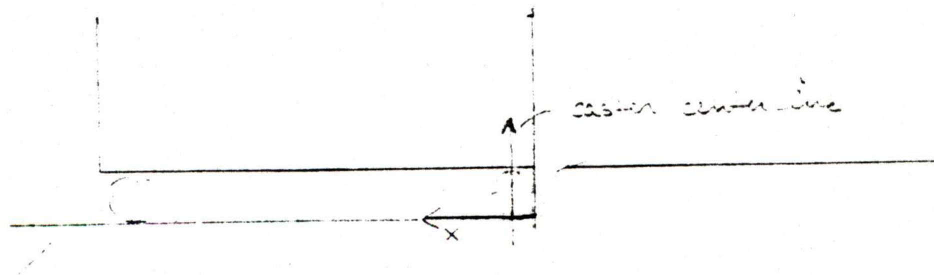
Side View



CG

Front

Rear



Force, F, applied at height of 60" with rear (front) caster locked. When the cab is just at the point of tipping

$$\Sigma M_o = 0 = (939 \text{ lbs}_f)(9.9 \text{ in}) - F(60 \text{ in})$$

or

$$F_1 = 155 \text{ lbs}_f$$

If front caster is locked,

$$\Sigma M_o = 0 = (939\ lbs_f)(10.[illegible]\ in) - F(60\ in)$$

$$F = 160\ lbs_f$$

The force required to stop the cabinet from rolling down an incline of 10° is

$$(939\ lbs_f)(\sin 10°) = 163\ lbs_f$$

Structual Analysis of Venus Power Supply Mounting Scheme, Using Computer Graphic Analysis Methods.

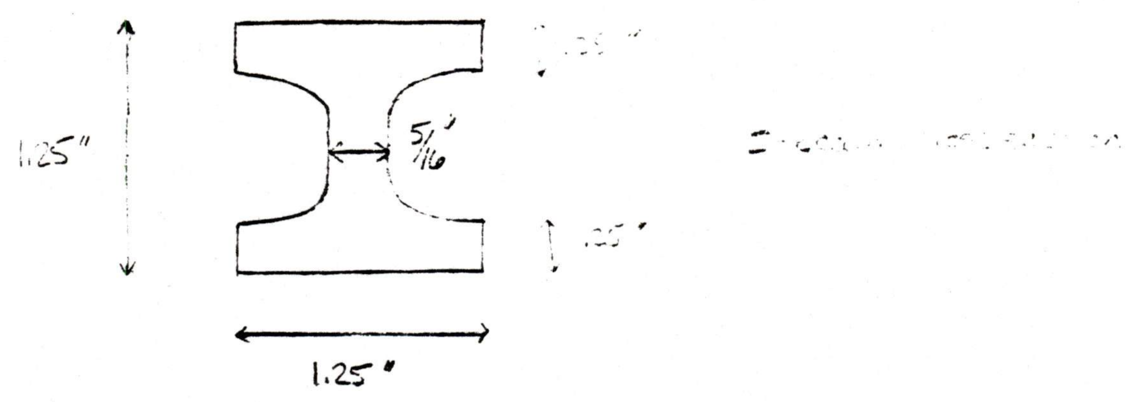
Intro

By the use of computer graphic methods, structual analysis can be accomplished accurately and swiftly compared to hand calculation methods. This report will give an example of a structual problem, how it was modeled and show the results obtained.

Structures Problem

The Venus Power Supply will weigh appromimately 100 pounds. During a typical drop test (DEC STD 102), accelerations of up to 20 g's are encountered. The mounting support for the power supply must, then, be able to withstand 2000 lbs-force.

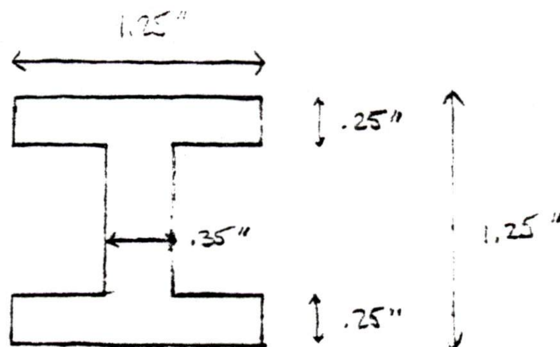
The mounting support (shown in figure 1) consists of four I-beams. In the front and in the back the I-beams will be connected together with steel strips. The I-beam cross section with dimensions is shown below.



The length of each I-beam is 42 inches and the axes of the beams are seperated from top to bottom by a distance of 7 inches. The centerline of the beams in the front are 14 3/4 inches from the centerlines of the beams in the back.

Modeling

To simplify the configuration, a model consisting of the front half of the power supply mounting bracket was constructed. Because of the limitations of the graphics input of the computer the cross section of the beam was squared off....



I-beam cross section of model

The length of the beams is 42 inches and they are seperated by 7 inches. A graphics display of the model constructed is shown in figure 2.

The model can be constructed by two graphic methods. The first consists of drawing the model from a top and side view, dividing it into several elements and inputing the nodes of the elements with an electronic digitizer.

In the second method, a series of bricks can be constructed by the computer (the dimensions of which are input by the user) and the bricks can be combined using interactive graphics, constructing the model.

In Figure 2 the beam supports are shown by up arrows and the loads are shown by down arrows. The locations of these supports and loads were graphically input and the magnitudes of the forces were typed in. These forces were one hundred pounds each, totalling 1000 pounds.

Results

The computer program uses a finite element method to calculate displacements and rotations for each node point and stresses for each brick element. Examples of the computer output are shown in Figures 3 and 4.

The results indicate that the highest stresses in the Aluminum I-beams is about 4000 psi. The highest stresses in the steel connecting bars is about 5000 psi. Both of these stresses occur close to the connecting areas between the steel connectors and the aluminum I-beams and the walls and aluminum I-beams.

The largest deflections occur at the center of the structure and have magnitudes less than .05 inches.

Conclusions

The tensile strength of the aluminum alloy used is about 40,000 psi. A conservative estimate of the yield strength would be about one-half of this, or 20,000 psi. Since the highest stress encountered in the aluminum I-beam was 4000 psi, the safety factor is 5.

For the steel connectors the tensile strength is about 75,000 psi, and the yield strength is estimated at 38,000 psi resulting is in safety factor of about 7.

These safety factors are quite high and we feel comfortable with the capabilities of the mounting support. The high safety factors indicate, also, that a reduction in the I-beam cross section is possible. Analyses similar to this one may be done quite easily to find the smallest cross section that will support the power supply.

John Druke

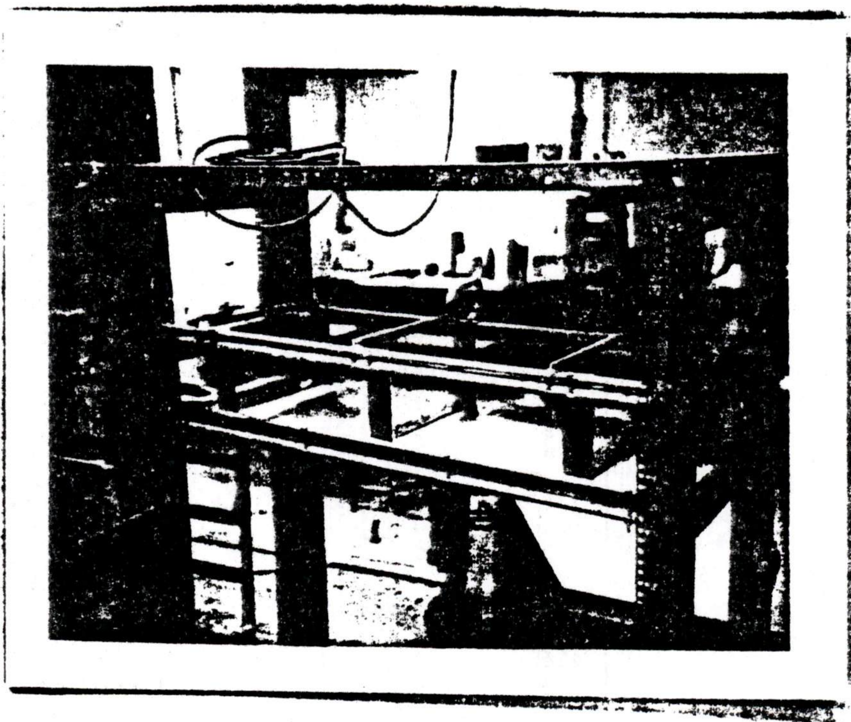


Fig. 1

Power Supply Supports.

(Metal plates at bottom simulate P/S weight.) Photo courtesy of P. Gildea's Bridgeworks, Inc. 1979

-1 - RETURN
0 - ORIG. SIZE
1 - ORIG. ORIENT.
2 - ROTATE
3 - ZOOM
4 - EXPAND
5 - BLINK/SING.EL.

NEXT>

TWO I-BEAMS SUPPORTED BY STEEL CONNECTORS

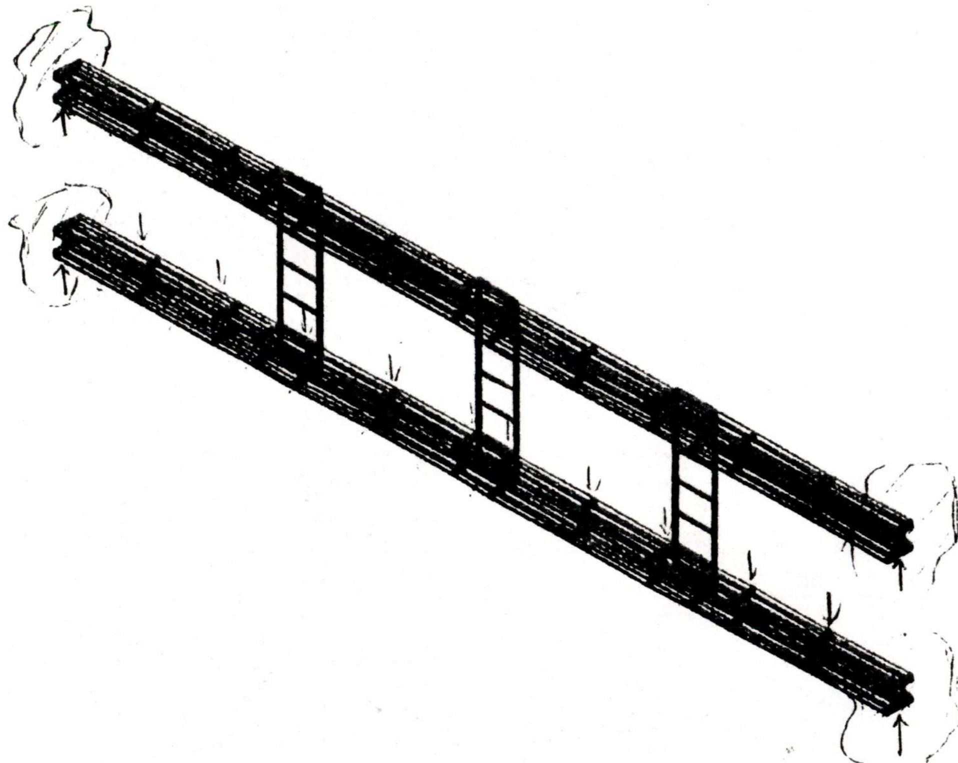


Fig. 2

DE DISPLACEMENTS/ROTATIONS

LOAD CASE 1

ODE BER	X- TRANSLATION	Y- TRANSLATION	Z- TRANSLATION	X- ROTATION	Y- ROTATION	Z- ROTATION
1	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
2	2.7090E-04	-1.3075E-05	2.0730E-05	0.0000E-01	0.0000E-01	0.0000E-01
3	2.2800E-04	-2.1895E-05	9.5625E-07	0.0000E-01	0.0000E-01	0.0000E-01
4	2.2358E-04	-2.1910E-05	-3.7832E-06	0.0000E-01	0.0000E-01	0.0000E-01
5	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
6	2.0353E-04	-1.3813E-05	-2.4489E-05	0.0000E-01	0.0000E-01	0.0000E-01
7	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
8	-1.7928E-04	2.7096E-05	2.5873E-05	0.0000E-01	0.0000E-01	0.0000E-01
9	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
10	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
11	-1.0834E-04	2.4102E-05	-9.9013E-07	0.0000E-01	0.0000E-01	0.0000E-01
12	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
13	-1.8605E-05	1.9464E-05	-7.7851E-06	0.0000E-01	0.0000E-01	0.0000E-01
14	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
15	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01	0.0000E-01
16	3.8924E-05	6.1171E-06	-1.7535E-05	0.0000E-01	0.0000E-01	0.0000E-01
17	6.7817E-04	-4.8847E-03	3.4506E-04	0.0000E-01	0.0000E-01	0.0000E-01
18	1.0307E-03	-4.8974E-03	-6.4539E-05	0.0000E-01	0.0000E-01	0.0000E-01
19	9.9939E-04	-4.1618E-03	-8.8806E-05	0.0000E-01	0.0000E-01	0.0000E-01
20	9.0964E-04	-3.5909E-03	-1.0424E-04	0.0000E-01	0.0000E-01	0.0000E-01
21	6.5141E-04	-2.8496E-03	2.8572E-04	0.0000E-01	0.0000E-01	0.0000E-01
22	8.3745E-04	-2.8552E-03	-1.2061E-04	0.0000E-01	0.0000E-01	0.0000E-01
23	7.0935E-04	-4.1510E-03	3.1733E-04	0.0000E-01	0.0000E-01	0.0000E-01
24	6.6548E-04	-3.5827E-03	3.0366E-04	0.0000E-01	0.0000E-01	0.0000E-01
25	-1.4575E-03	-2.8256E-03	1.9810E-03	0.0000E-01	0.0000E-01	0.0000E-01
26	-9.4548E-04	-2.8112E-03	1.5450E-03	0.0000E-01	0.0000E-01	0.0000E-01
27	-6.4298E-04	-3.5775E-03	1.5293E-03	0.0000E-01	0.0000E-01	0.0000E-01
28	-1.1684E-03	-3.5846E-03	1.9413E-03	0.0000E-01	0.0000E-01	0.0000E-01
29	-4.5186E-04	-4.1427E-03	1.5195E-03	0.0000E-01	0.0000E-01	0.0000E-01
30	-9.5317E-04	-4.1483E-03	1.9128E-03	0.0000E-01	0.0000E-01	0.0000E-01
31	-5.7978E-04	-4.8389E-03	1.8875E-03	0.0000E-01	0.0000E-01	0.0000E-01
32	-3.9997E-05	-4.8312E-03	1.5135E-03	0.0000E-01	0.0000E-01	0.0000E-01
33	7.9780E-04	-1.8762E-02	1.3411E-03	0.0000E-01	0.0000E-01	0.0000E-01
34	3.9600E-04	-1.8870E-02	-3.3304E-03	0.0000E-01	0.0000E-01	0.0000E-01
35	3.2209E-04	-1.9488E-02	-3.3395E-03	0.0000E-01	0.0000E-01	0.0000E-01
36	9.1664E-04	-1.3645E-02	1.6709E-03	0.0000E-01	0.0000E-01	0.0000E-01
37	1.6368E-03	-1.3644E-02	6.8229E-04	0.0000E-01	0.0000E-01	0.0000E-01
38	1.3708E-03	-1.1858E-02	6.8120E-04	0.0000E-01	0.0000E-01	0.0000E-01
39	1.1892E-03	-1.0454E-02	6.7829E-04	0.0000E-01	0.0000E-01	0.0000E-01
40	9.3995E-04	-8.6264E-03	6.8115E-04	0.0000E-01	0.0000E-01	0.0000E-01
41	4.0045E-04	-5.6310E-03	1.7011E-03	0.0000E-01	0.0000E-01	0.0000E-01

Fig. 3

.....8-NODE SOLID ELEMENT STRESSES

ELEMENT	LOAD NO.	FACE	SIG-XX	SIG-YY	SIG-ZZ	SIG-XY	SIG-YZ	SIG-ZX
1	1	0	-2.62E+03	-1.73E+02	-3.81E+02	-2.05E+02	1.00E+02	2.60E+02
2	1	0	-5.04E+02	1.28E+02	1.85E+02	2.36E+02	-2.15E+01	-1.87E+01
3	1	0	9.89E+01	-7.86E+01	-8.35E+01	-4.96E+01	9.35E+00	1.78E+02
4	1	0	7.77E+02	8.40E+01	7.20E+01	2.13E+02	1.09E+01	3.43E+00
5	1	0	6.48E+02	-3.87E+01	-4.61E+01	7.81E+00	-1.18E+01	-1.40E+01
6	1	0	1.27E+03	1.04E+01	1.21E+01	3.08E+01	3.93E+00	7.83E+01
7	1	0	-2.09E+03	-1.70E+02	-3.55E+02	-2.64E+02	-1.70E+01	2.99E+02
8	1	0	-7.50E+01	1.34E+02	1.65E+02	2.28E+01	-2.47E+01	2.54E+02
9	1	0	3.97E+02	-3.50E+01	-8.88E+01	-2.14E+02	-9.02E+01	4.03E+02
10	1	0	3.51E+02	3.69E+00	5.19E+00	9.46E+01	-7.59E+00	2.40E+02
11	1	0	1.47E+02	-6.97E+01	-8.36E+01	-4.83E+01	3.17E+01	7.76E+01
12	1	0	1.03E+03	6.67E+01	8.63E+01	-5.10E+01	-7.90E+00	1.29E+02
13	1	0	-1.36E+03	-8.23E+01	-2.06E+02	-2.41E+02	-7.33E+01	-1.52E+02
14	1	0	1.52E+01	-5.43E+01	-3.39E+00	2.83E+01	2.95E+01	1.60E+01
15	1	0	1.95E+03	6.26E+02	5.11E+02	-[illegible].85E+02	1.13E+02	-5.57E+02

Fig. 4

12.00 ±.03
CARD CAGE

POWER CONN HSG

POWER PAD

GROUND HSG CONTACTS

CASTING RIB

GROUND PAD

℄ CONTACT

PRESS PIN CONN HSG

BACKPLANE

POWER BUSS BARS (COPPER)

19.72 ±.02
CARD CAGE

15.688 +.015/−.020
MODULE

15.718 ±.015
CHASSIS

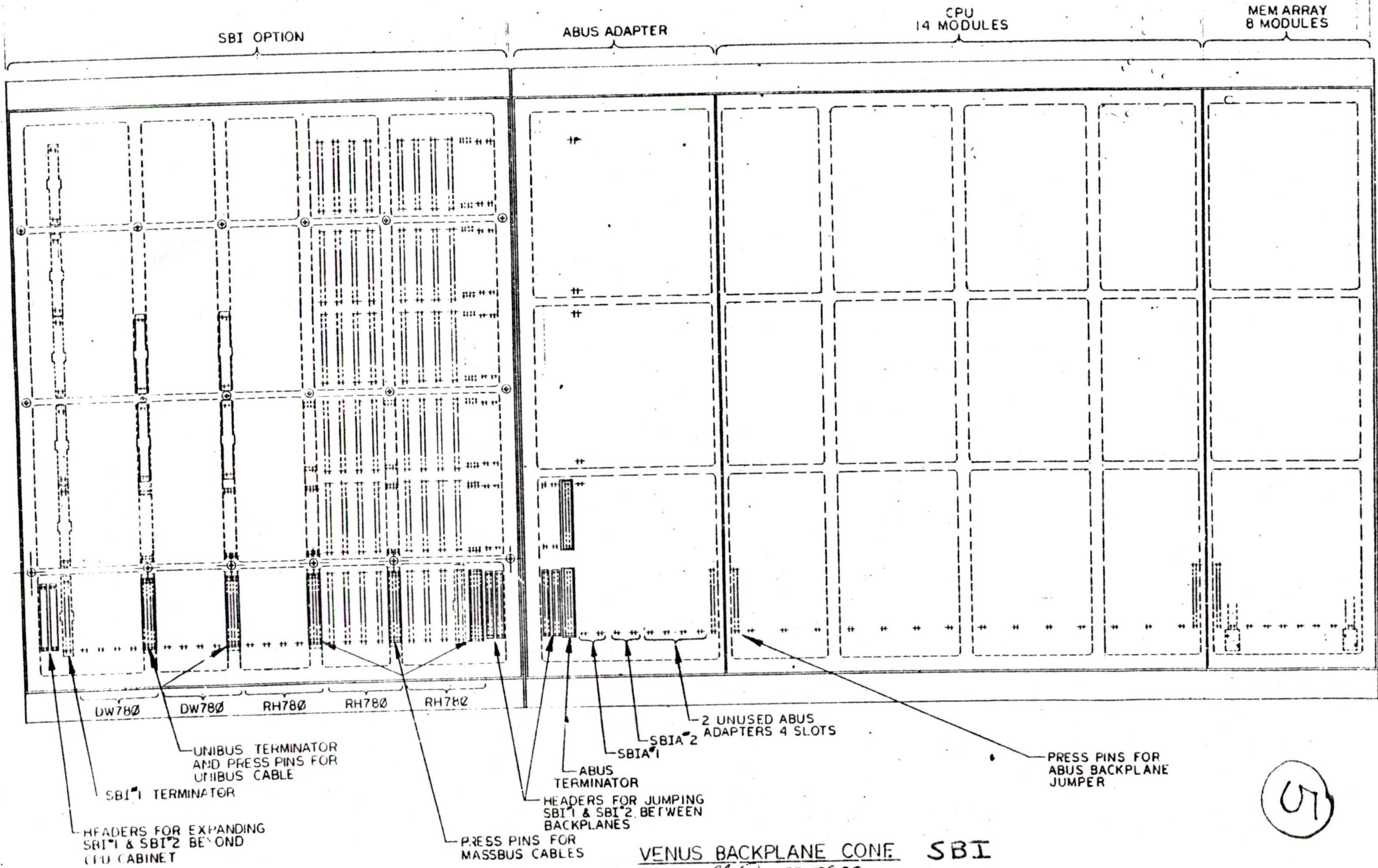
.015
REF

2.00

11.56 ±.02
EJECTOR HOLE

SECTION B-B
SCALE: 1/1

SIDE VIEW
VENUS CARD CAGE
SHT 3 OF 3



VENUS BACKPLANE CONE SBI

27 FEB 80

6

The following is a layup of a 2080 CPU Backpanel and a Venus CPU/~~MEM~~ backpanel:

```
L1 (signal)         ---------------      2 oz Cu
                    ///////////////      FR4 10 mils +/- 1.0
                    ///////////////
L2 (grd/pwr)        ---------------      2 oz Cu
                    ///////////////      FR4 6 mils +/- 2 mils
L3 (grd/pwr)        ---------------      2 oz Cu
                    ///////////////
                    ///////////////      FR4 16 mils +/- 2
L4 (signal)         - - - - - - - - -    1 oz Cu
                    ///////////////      FR4 3.5 mils +/- .5
L5 (signal)         - - - - - - - - -    1 oz Cu
                    ///////////////      FR4 16 mils +/- 2
                    ///////////////
L6 (grd/pwr)        ---------------      2 oz Cu
                    ///////////////      FR4 6 mils +/- 2 mils
L7 (grd/pwr)        ---------------      2 oz Cu
                    ///////////////
                    ///////////////      FR4 16 mils +/- 2
L8 (signal)         - - - - - - - - -    1 oz Cu
                    ///////////////      FR4 3.5 mils +/- .5
L9 (signal)         - - - - - - - - -    1 oz Cu
                    ///////////////
                    ///////////////      FR4 16 mils +/- 2 mils
L10 (grd/pwr)       ---------------      2 oz Cu
                    ///////////////      FR4 6 mils +/- 2 mils
L11 (grd/pwr)       ---------------      2 oz Cu
                    ///////////////
                    ///////////////      FR4 16 mils +/- 2
L12 (signal)        - - - - - - - - -    1 oz Cu
                    ///////////////      FR4 3.5 mils +/- .5
L13 (signal)        - - - - - - - - -    1 oz Cu
                    ///////////////      FR4 16 mils +/- 2 mils
                    ///////////////
L14 (grd/pwr)       ---------------      2 oz Cu
                    ///////////////      FR4 6 mils +/- 2 mils
L15 (grd/pwr)       ---------------      2 oz Cu
                    ///////////////
                    ///////////////      FR4 10 mils +/- 1
L16 (signal)        - - - - - - - - -    2 oz Cu
```

Board Impedance: All signal layers are to be 55 +/- 5 ohms. (ECL)

Board information:

Finished Board Size:

Venus: 17.8" x 16.3"
2080: 17.8" x 22.93"

Finished Board thickness: 186.9 +/- 23.5 mils

Plated-thru-hole size: 40 +3 mils, -4 mils,
A press-fit pin connector (AMP) will be used on this backplane.

Dielectric constant: I assumed a dielectric constant of
4.5 at 50 MHz for buried signal layers,
4.7 at 50 MHz for surface signal layers.

Etch line width: L1 and L16: 14 +/-1 mils
Buried signal layers: 10 +/-1 mils

Estimated number of pin to pin connections:
Venus: 2700
2080: 4140

Estimated number of connector pins on the backpanel:
Venus: 6120
2080: 8000

The following is a layup of the VENUS & 2080 Memory Backpanels:

```
L1 (signal)      ---------------     2 oz Cu
                 ///////////////     FR4 10 mils +/- 1.0
                 ///////////////
L2 (grd/pwr)     ---------------     2 oz Cu
                 ///////////////     FR4 100 mils
                 ///////////////
L3 (grd/pwr)     ---------------     2 oz Cu
                 ///////////////
                 ///////////////     FR4 10 mils +/- 1
L4 (signal)      - - - - - - - -     2 oz Cu
```

Board Impedance: All signal layers are to be 55 ohms +/- 5 ohms (ECL)

Board information:

Finished Board Size:

2080: 17.8" x 9.47"

Finished Board thickness: Minimum Board Thickness of 93 mils

Plated-thru-hole size: 40 mils + 3 mils, -4 mils
A press-fit pin connector is to be used on this backplane.

Dielectric constant: I assumed a dielectric constant of 4.7 at 50 MHz for surface signal layers.

Etch line width: 14 +/- 1 mils

The following is a layup of the 2080 and Venus I/O Backpanels:

```
L1 (signal)        ---------------        2 oz Cu
                   ////////////////       FR4 15 mils +/- 2.0
                   ////////////////
L2 (grd/pwr)       ---------------        2 oz Cu
                   ////////////////
                   ////////////////       FR4 20 mils +/- 2
L3 (signal)        - - - - - - - -        1 oz Cu
                   ////////////////       FR4 20 mils +/- 2
                   ////////////////
L4 (grd/pwr)       ---------------        2 oz Cu
                   ////////////////
                   ////////////////       FR4 10 mils +/- 2
L5 (grd/pwr)       ---------------        2 oz Cu
                   ////////////////
                   ////////////////       FR4 20 mils +/- 2
L6 (signal)        - - - - - - - -        1 oz Cu
                   ////////////////       FR4 20 mils +/- 2
                   ////////////////
L7 (grd/pwr)       ---------------        2 oz Cu
                   ////////////////
                   ////////////////       FR4 15 mils +/- 2
L8 (signal)        - - - - - - - -        2 oz Cu
```

Board Impedance: 80 ohms (TTL)

Board information:

Finished board Size:

Venus: 3.1" x 17.8"
2080: 9.5" x 20.5"

Finished Board thickness: 135.6 mils +/- 14 mils

Plated-thru-hole size: 40 mils +3 mils, -4 mils

Dielectric Constant: I assumed a dielectric constant of 4.7

Etch line width: 8 mils +/- 2 mils

(7)

```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

DATE: July 9, 1979
FROM: JOHN HACKENBERG
DEPT: L.C.E.G.
EXT: 6106
LOC: MR1-2/E47

TO: Distribution List

Subj: Number of MCA's per Extended Hex Board for Venus

The following method was used to determine the component count for an extended Hex module. This method is used by Andy Matthews to determine component count for any given type board, but I modified it to handle termination of ECL signals.

The method goes as follows:

A) Determine what components go into a cell. A cell in the case of the MCA consists of one MCA, two bypass capacitors for -5.2 volts, two ten resistor networks, and four bypass capacitiors for the resistor networks (for -2.0 volts). See figure 1.

B) Determine the number of channnels that are needed in the "X" and "Y" directions. The etch connection length between cells is one horizontal and one vertical channel.

1) For 50 mil etch spacing (center-to-center etch spacing), assume that 50% of available channels are usable when routing a PC board. Therefore, from the 50 mil spacing and 50% utilization of available channels, there is 1 channel per 0.1 inch for signal connections.

2) Determine the number of signal connections that must be routed between cells. First, sum up all components (IC's) pins, multiply by 80%, and multiply by 2/3 (equation (1)). This gives you the number of channels or signal connections between cells. For ECL logic which contains terminators, count the number of terminators per cell and divide by two (equation (2)). This converts terminator connections within a cell to equivalent cell to cell connections. Terminators on ECL boards have their source located within the cell. Sum up the IC signal connection count plus the equivalent terminator signal count (equation (3)). This is the number of channels needed in each "X" and "Y" direction.

(1) $$Pic * 0.8 * 0.666 = Cc$$

(2) $$Tr / 2 = Cr$$

(3) $$Cc + Cr = Ct$$

Pic = Total number of IC pins per cell
Cc = Channels per cell for ICs
Tr = Total number of terminators per cell
Cr = equivalent cell to cell channels for resistors
Ct = Total number of channels per cell

C) From the cell size, you know how many channels are available using a 50% utilization of all channels. Remember that you need the same number of channels in each direction, "X" and "Y".

D) For a given number of signal layers, the following is the process for determining how many components that can be placed on a given board.

1) Determine how many signal layers you have available for each routing direction. This is usally one-half the total number of signal layers for the board being used (equation (4)). Divide the number of layers in a given direction into the number of channels that are needed for routing in each direction (equation(5)). This gives you the number of channels per signal layer. Now figure out how much board real estate is needed (using 50% utilization of expanded cell size) for the new cell size. This procedure must be repeated for the other direction.

(4) Ct / 2 = Cl

(5) Ct / Cl = Cpl

Ct = Total number of channels per cell per routing direction
Cl = Number of signal layers per given routing direction
Cpl = Number of channels per layer for a given direction

2) An extended hex board has 168 square inches of routable real estate. Subtract from the routable area of the board the real estate required for a stiffener and storage capacitors. The remaining board real estate is the area in which components can be placed. Divide the cell size from paragraph D-1 into the remaining board real estate, this gives you the number of component that can be place on a given PC board.

(6) Ra / Ca = No. of components per board

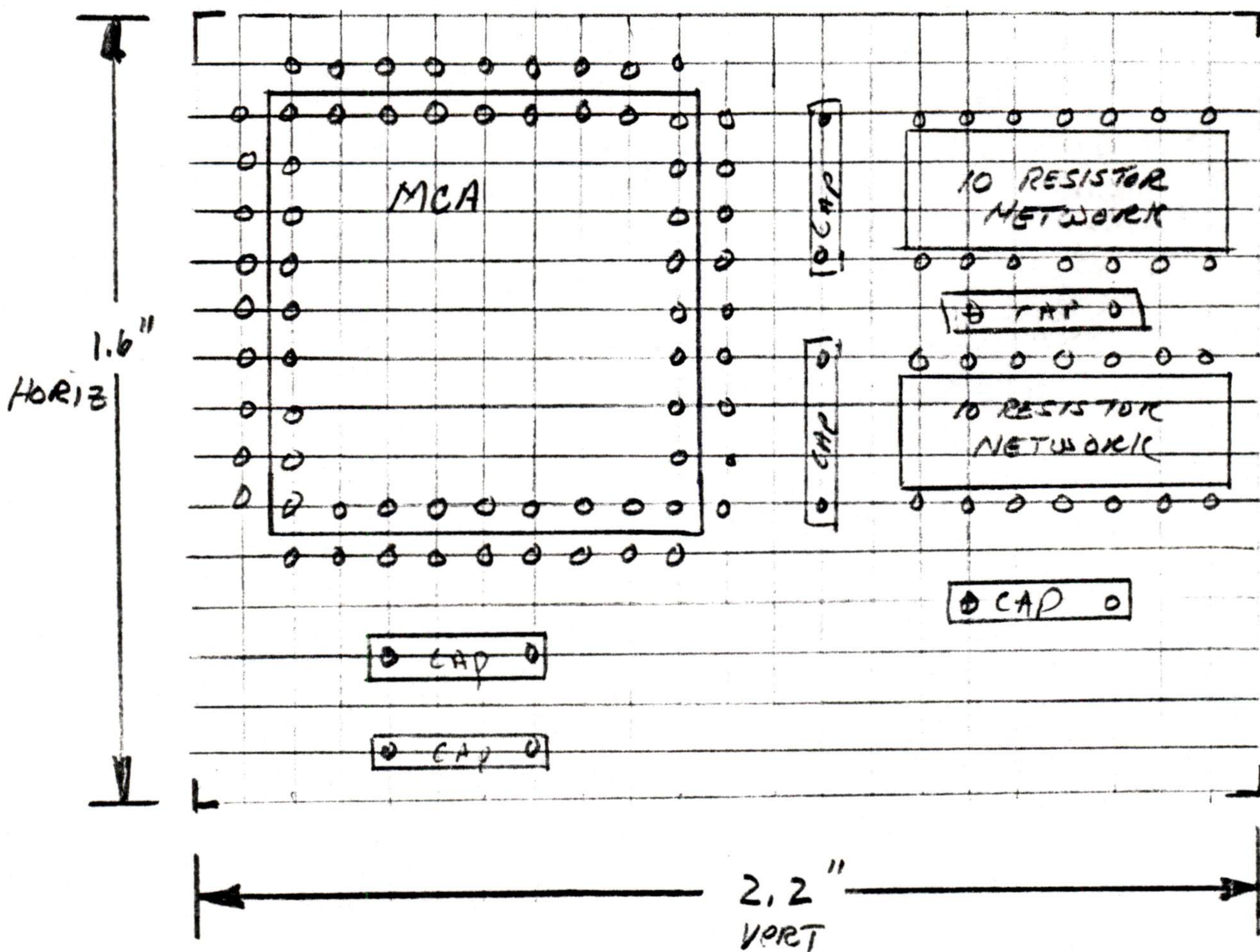
Ra = Routable area in square inches
Ca = Cell are in square inches

For an extended hex module having 4 signal layers, 30 MCAs can be

routed on the board. If the extended hex has 2 signal layers, then only 10 MCAs can be routed on the board.

MCA

FIGURE 1



Channels Available
Horiz = 32
VERT = 44

50 mil center-to-center spacing of etch.

50% UTILIZATION of channels
Horiz = 16
VERT = 22

Channels needed in Horiz & Vert. DIRECTIONS

(1) $P_{IC}\,(.8)\,(.666) = C_c$
$(64)(.8)(.666) = 36.3 = C_c$

(2) $T_R / 2 = C_r$

$C_r = \frac{20}{2} = 10$

(3) $C_c + C_R = C_T$
$36.3 + 10 = 46.3 = C_T$

For 4 layers – channels needed / Layer

$C_L = \frac{C_T}{2} = \frac{46.3}{2} = 23.15$

Four Signal Layers
8 Layer Bd

Need 23.15 channels per layer in order to route the MCAs & resistor networks.

∴ Using 50 utilization of all available channels, a cell size of 2.3" x 2.3" is needed per MCA.

For an extended hex module which contains 168 sq. inches of routable area.

$168 - 10 = 158$ sq inches
10 sq in for stiffener & storage capacitors

$$\frac{158 \text{ sq in.}}{2.3 \times 2.3} \doteq 30$$

30 MCAs / Ext. Hex module

Two Signal Layers

Here the cell size must be expanded because of less routing channels per Board.

(1) $C = 36.3$
(2) $T_R/4 = 14$ — modified equation since terminators can remain same distance from MCA as in four signal layer boards

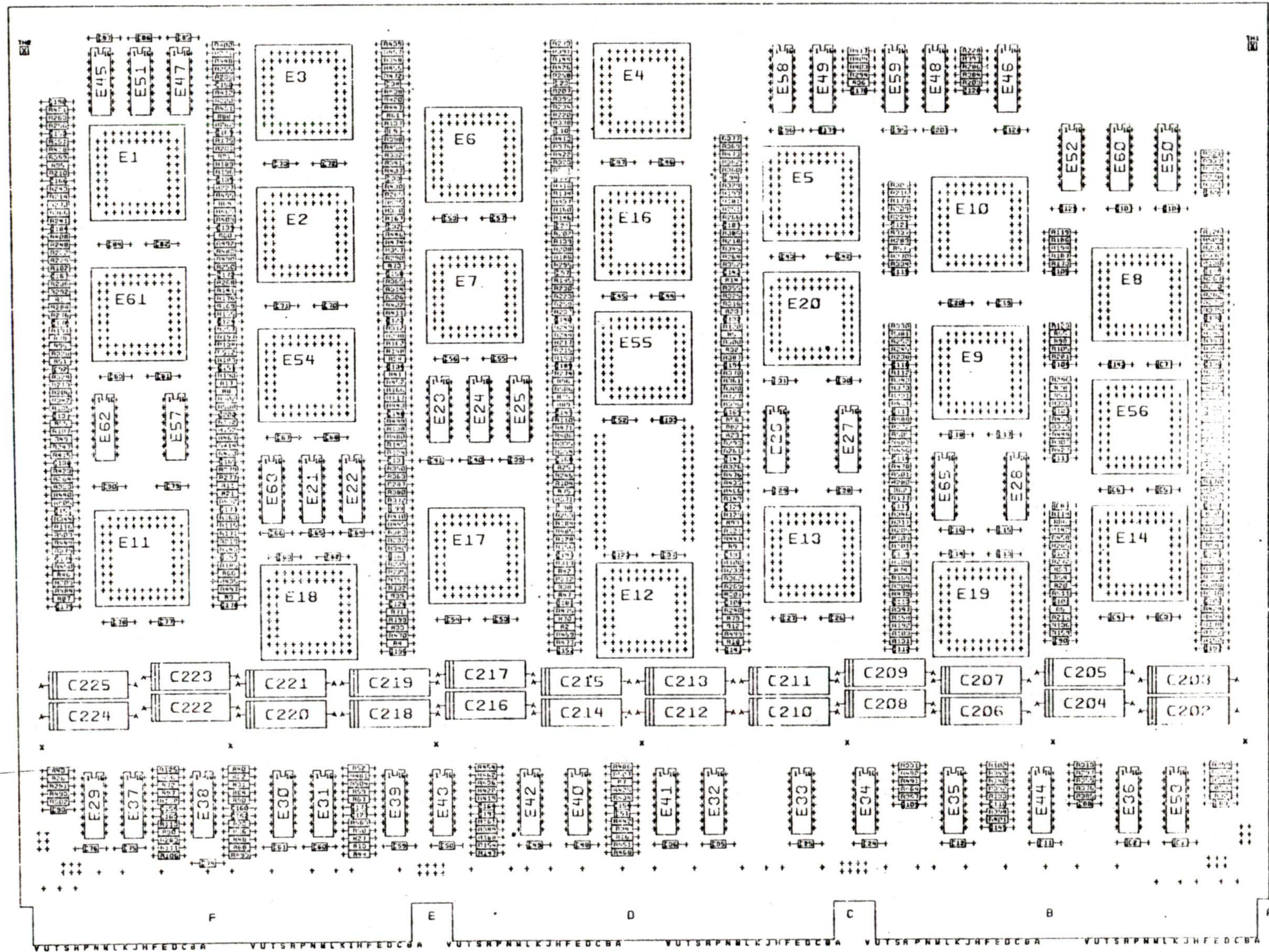
$\frac{20}{4} = 5$

(3) $C_T = 36.3 + 5$
$C_T = 41.3$

∴ Cell size $= 4.1" \times 4.1"$

$$\frac{158 \text{ sq in.}}{4.1" \times 4.1"} = 9.4 \text{ or } \cong$$ **10 MCA / Ext Hex Bd**

COMPONENT SIDE VIEW



COMPONENT PLACEMENT VENUS FPA BOARD - DISCRETE RESISTORS

(9)

```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

DATE: Feb. 3, 1980
FROM: JOHN HACKENBERG
DEPT: L.C.E.G.
EXT: 5106
LOC: MR1-2/E47

TO: VENUS Technical Distribution List

Subj: Number of Ground Pins Required Per Extended TRI Module for 10K ECL Logic as used in the VENUS System

Extended TRI board is the same physical dimension as the COMET board which has three finger paddles instead of six as does the extended hex. The extended TRI will be used in the Venus system.

To determine the number of ground pins needed for each individual board, use the following formulas:

$$0.25A + 0.5B = N$$

A = Number of 50 ohm finger pins which are switching in the same direction and within 3 ns of each other.

B = Number of 25 ohm finger pins which are switching in the same direction and within 3 ns of each other.

N = Total number of ground pins needed for 50 and 25 ohm finger pins which are switching in the same direction and within 3 ns of each other.

If N exceeds 50, then the number of ground pins needed is

$$N - 50 = Y$$

Y = the number of additional ground pins needed for a given module.

The additional ground pins must be evenly distributed across the finger pins.

For two signal layer pc boards which will contain only TTL logic, the following component density may be used:

Package size (WIDTH)	Component Density	(Component area)
14 PIN DIP (0.3")	189	(1.0" x 0.7")
16 PIN DIP (0.3")	171	(1.1" x 0.8")
20 PIN DIP (0.3")	105	(1.3" x 1.0")
24 PIN DIP (0.6")	80	(1.5" X 1.2")
28 PIN DIP (0.6")	55	(1.7" X 1.3")

A 30 mil grid is used for routing the board with eight mil wide lines.

If four signal layer boards are used, then the component density for TTL PC boards is as follows:

Package size (WIDTH)	Component Density	(Component area)
14 PIN DIP (0.3")	270	(1.0" x 0.5")
16 PIN DIP (0.3")	240	(1.1" x 0.5")
20 PIN DIP (0.3")	175	(1.3" x 0.6")
24 PIN DIP (0.6")	114	(1.5" X 0.8")
28 PIN DIP (0.6")	95	(1.7" X 0.8")

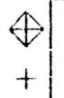
NOTE: A routing test should be done to verify the above component density for a four signal layer board. I have no plans of doing this routing test unless someone is going to use a four signal layer board for TTL.

To determine component density for a mix of different types of components, determine the amount of necessary real estate from the component area for each package size. The sum of the component real estate areas shall not exceed 150 square inches.

COMPONENT SIDE VIEW

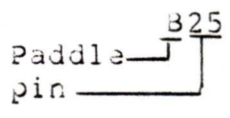
digital

JOB NAME: BCARD4, BASE REV: , ASMB REV: 0002



COMPONENT PLACEMENT VENUS FPA BOARD - SIP RESISTORS

For a single module, the slot number is eliminated.



Allocation of finger pins for VENUS modules:

1) 282 finger pins available

2) 12 pins reserved for +5.Ø Volts

   Standard +5.Ø Volt pins are

   AØ3 AØ4 A91 A92
   BØ3 BØ4 B91 B92
   CØ3 CØ4 C91 C92

3) 38 pins reserved for standard ground pins

   Standard ground pins are

   AØ1 AØ7 A13 A16 A23 A33 A43
   A51 A61 A72 A79 A82 A94

   BØ1 B13 B16 B23 B33 B43 B51
   B61 B72 B79 B82 B94

   CØ1 C13 C16 C23 C33 C43 C51
   C61 C72 C79 C82 C83 C94

4) One pin is reserved for +12 volts, AØ2.
   One pin is reserved for -12 volts, A93.

5) -5.2 V and -2.Ø V are distributed using AMPS power contacts.

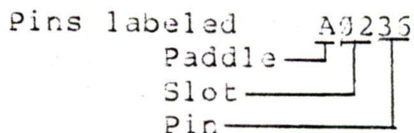
6) There are four large ground distribution contacts, equivalent to 12 ground pins. Therefore, each extended TRI board has an equivalent of 5Ø ground pins.

7) If no additional ground pins (finger pins) are needed on a given module, there are 23Ø finger pins available for signal I/O.

It should be noted that the module to be used in the VENUS has a different finger pin nomenclature then the extended hex module, i.e. use DECA instead of DEC in SUDS. The nomenclature is as follows:

There are three IDENTICAL "paddles" labeled "A", "B", and "C" each with 94 "finger pins" labeled 1 thru 94. Odd numbered pins are on side 1 and even numbered pins are on side 2 of module.

Pins labeled



```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

DATE: Dec. 17,1979
FROM: JOHN HACKENBERG
DEPT: L.C.E.G.
EXT: 6106
LOC: MR1-2/E47

TO: Venus Hardware Engineering

Subj: Component Density for Venus TTL PC Boards

Component density on a extended hex module with two signal layers, a four layer pc board, is as follows:

When a PC board contains both TTL and ECL logic, the IDEAS router will allow only one grid in auto routing. Therefore, a fifty mil grid is required for both TTL and ECL logic.

TTL Component density for a PC board with ECL on it:

Package size (WIDTH)	Component Density	(Component area)
14 PIN DIP (0.3")	171	(1.0" x 0.8")
16 PIN DIP (0.3")	153	(1.1" x 0.9")
20 PIN DIP (0.3")	91	(1.3" x 1.1")
24 PIN DIP (0.6")	66	(1.5" X 1.3")
28 PIN DIP (0.6")	50	(1.7" X 1.5")

Component density for ECL when using a two signal layer board.

Package size (WIDTH)	Component Density	(Component area)
16 PIN DIP (0.3")	135	(1.1" x 0.8")
28 PIN DIP (0.6")	40	(1.8" X 1.8")

Component density for ECL takes terminators and bypass capacitors into consideration. A 16 pin dip has three terminators per package and a 28 pin dip allows for for 6 terminators per package.

ECL and TTL logic must be isolated from each other by 0.15 inches when routing the PC board.

Example calculation for component density:

```
50 RAMS (24 PINS)        Cell size:      1.5" x .6" = 45 sq in.
Terminators for RAMS
Assume you need 5 terminator packages
                         Cell size:      1.2" x 0.5"=  3 sq in.
10 10K parts             Cell size:      1.2" x 1.5"=  9 sq in.
                                             -------------
                                                  57 sq in.

Available area remaining for MCAs
                         150 sq in.
                       -  57 sq in.
                         -----------
                         93 sq in.
```

Each MCA requires 5.29 sq inches.

Therefore, 93/5.29 = 17.6 MCAs

The 17 MCAs is reduced to 15 MCAs when the clock driver and etched delay line are added to the module.

Terminators:
10 per 16 pin DIP
Cell size: 1.2" x 0.5"

D) 10K ECL:
No MCAs or RAMs
160 ICs/module
16 pin DIPS plus bypass capacitor
Includes terminators
Cell size: 1.2" x 1.5"
Includes 2 16 pin IC (DIPS) plus
a 10 resistor terminator package

E) Partitioning of logic must allow for a maximum of 230 signal pins/module.

F) Assume that the CLOCK DRIVER and ETCHED DELAY LINE occupy the equivalent space of two MCAs.

Each MCA size equals 2.3" x 2.3".

G) Maximum power per extended hex module is limited to 170 watts.

No more than 35 watts in any one column as air blows across components.
Refer to Cliff Lupien memo on cooling of modules for placements of MCAs and other components on the modules.

MCA = 5 watts
RAMS = 1 watt
10K = 0.25 to 0.5 watts

Board Density:

Boards which have MCAs require the module next to it, on the component side, to be on 1.0 inch centers.

Boards which have DIPs require the module next to it, on the component side, to be on a minimum of 0.5 inch centers.

To determine component density for a mix of different types of components, determine the amount of necessary real estate from the cell size given above. The sum of the component real estate shall not exceed 150 square inches.

```
+----------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+----------------+
```

DATE: July 17, 1979
FROM: JOHN HACKENBERG
DEPT: L.C.E.G.
EXT: 6106
LOC: MR1-2/E47

TO: Distribution List

Subj: Component and Board Density for Venus (ECL)

Component density on a extended hex module with four signal layers, an eight layer board, is as follows:

Assume the the following:
Module size: Extended Hex
Number of signal layers: 4
Routeable area: 150 square inches

A) 30 MCAs per Board
No RAMs or jelly bean ICs

Includes bypass capacitors, and two
16 pin (DIP) terminator packages per MCA
Each terminator package has 10 resistors

DOES NOT INCLUDE THE CLOCK DRIVER AND ETCHED DELAY LINE

B) RAMS (1k by 4)
No MCAs or jelly bean ICs

RAMS:
24 pin (DIPs) plus bypass capacitors
168 RAMS/Module
No CLOCK DRIVER OR ETCHED DELAY LINE
NO Terminators included
Cell size: 1.5" x 0.6"

Terminators:
10 per 16 pin DIP
Cell size: 1.2" x 0.5"

C) RAMS (4k by 1)
No MCAs or jelly bean ICs

RAMS:
18 pin (DIPs) plus bypass capacitors
240 RAMS/Module
No CLOCK DRIVER OR ETCHED DELAY LINE
NO Terminators included
Cell size: 1.2" x 0.5"

10

```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

DATE: Jan. 16, 1980
FROM: JOHN HACKENBERG
DEPT: L.C.E.G.
EXT: 6106
LOC: MR1-2/E47

TO: John Belanger
G. Sankar

Subj: Preliminary PC and Backpanels Board Specifcations for Venus and 2080

This document specifies the preliminary requirements for multilayer boards for Venus and 2080 along with the backpanel specifcation for each system.

I want the Acton Board Technology to comment on the layups of each board type and return the comments to me as soon as possible.

Note: Acton must specify the correct dielectric constant of the core and 'B Stage' material for the backpanels so that more accurate layups can be defined to obtain the correct impedance for the backpanels.

The following layup is for Venus and 2080 PC Boards:

```
                                                3 oz Cu
L1 (pads)              ---------------          FR4 4 mils +/- 1.0
                       ///////////////          1 oz Cu
L2 (signal)            - - - - - - - -          FR4 3.5 mils +/- .5
                       ///////////////          1 oz Cu
L3 (signal)            - - - - - - - -          FR4 10 mils +/- 1.0
                       ///////////////
                       ///////////////          3 oz Cu
L4 (ground)            ---------------
                       ///////////////          FR4 6 mils +/- 2.0
                       ///////////////          3 oz Cu
L5 (power)             ---------------          FR4 10 mils +/- 1.0
                       ///////////////
                       ///////////////          1 oz Cu
L6 (signal)            - - - - - - - -          FR4 3.5 mils +/- .5
                       ///////////////          1 oz Cu
L7 (signal)            - - - - - - - -          FR4 4 mils +/- 1.0
                       ///////////////          3 oz Cu
L8 (pads)              ---------------
```

Material: Base material shall meet UL 94V2 or better requirements.

Special ground and power distribution pads are used on layers 1 and 8 which need to be gold and nickel plated.
Board Impedance: 55 +/- 5 ohms (ECL)

Board information:

Finished Board Size:

Venus: Extended Hex
2080: Extended Hex

Finished Board thickness: 54 to 70 mils

Plated-thru-hole size: Standard hole size will be 40 +/- 3 mils

Dielectric constant: 4.7 +/-0.4 at 50 MHZ

Etch line width: L2 and L7: 18 mils +/- 1 mil
L3 and L6: 12 mils +/- 1 mil

MCA PACKAGING FEATURES

CHIP CARRIER

- 68 I/O LEADLESS TYPE "A" (50 MIL ℄)
- DESIGNED FOR USE IN SOCKETS
- $\theta_{JC} \simeq 4^{o}C/$ WATT FOR MCA DIE SIZE
- GOLD OVER NICKEL OVER REFRACTORY METAL
- KEYED CORNER FEATURE
- 2 LAYER & 3 LAYER VERSION
- GLASS FRIT SEAL

SOCKET

- STANDARD GRID PINNOUT (.1" ℄)
- SOLDER TAIL
- TOPSIDE PROBING
- 100 GM CONTACT FORCE
- 15 LB. COVER CLOSING FORCE
- KEYED TO CARRIER AND P.C. BOARD
- .003 $F/10^6$ HRS. CONTACT FAILURE RATE FOR STRESS RELAXATION @ $T_C = 68^{o}C$

```
+---------------+
! d i g i t a l !   I N T E R O F F I C E   M E M O R A N D U M
+---------------+
```

TO: DISTRIBUTION

DATE: MARCH 7 1983
FROM: MOHAMMED TYABUDDIN
DEPT: LCEG
EXT: 5924 LOC: MR1-2

SUBJ: Noise Analysis Of MCA Packaging

This memorandum contains the noise analysis of the Macro Cell Array (MCA) socket and chip carrier.

When one of the outputs of the MCA is held high or low and the other outputs switching, the noise seen on the nonswitching output is about 195mv. This noise is coupled from the Vcco bus through the collector to base capacitance of the output emitter follower and thus appears on the output.

The noise generated on the Vcco bus is due to the inductance of the bonding wires, the chip carrier and the socket.

Clearly the noise magnitude of 195mv on the output is intolerable, so to reduce this coupling noise from the Vcco bus, the inductance of the chip carrier and the socket should be reduced, assuming not much could be done about the bonding wires.

The reason for this analysis is to determine actually how much noise is generated due to each of the above mentioned three items, and which is the major contributor, so that necessary steps could be taken to reduce the inductance.

The following pages shows the result of the analysis, which was simulated using Spice2 program, and also measured in any of the permissible conditions on the test chip.

At the end of the memorandum is the details of how the inductance of the bonding wire, chip carrier, and the socket pin was calculated or measured.

The spicemodel used in simulation is attached.

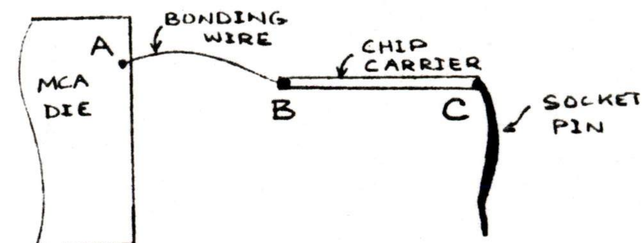
MCA WITH SOCKET

Vcco PIN 3

CONDITION	NOISE IN MILLIVOLTS					
	PIN 6		A	B	C	
	SIMULATED	MEASURED	SIMULATED	SIMULATED	SIMULATED	MEASURED
PIN 6 LOW SWITCHING PINS 1,2,4,5,7,8	105	190	710	680	420	
PIN 6 HIGH SWITCHING PINS 1,2,4,5,7,8	195	195	738	704	407	
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	X		115	99	60	
SWITCHING PINS 1,2,4,5,6,7,8	X		833	777	463	
PINS 1,2 SWITCHING PINS 4,5,6,7,8 HIGH	90		397	383	227	
PINS 1,2 SWITCHING PINS 4,5,7,8 HIGH, PIN 6 LOW	45		410	379	220	
PINS 1,2,6 HIGH PINS 4,5,7,8 SWITCHING	75		380	362	199	
PINS 1,2 HIGH, PIN 6 LOW PINS 4,5,7,8 SWITCHING	45		385	352	205	

MEASURED AND SIMULATED NOISE FOR PIN 6

SIMULATED NOISE AT POINTS A, B, C FOR Vcco PIN 3



DISTRIBUTION OF NOISE

Vcco PIN 3

CONDITION	BONDING WIRE A-B (MV)	%	CHIP CARRIER B-C (MV)	%	SOCKET PIN C (MV)	%
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	30	4.2	260	36.6	420	59.2
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	34	4.6	297	40.2	407	55.2
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	16	13.9	39	33.9	60	52.2
PINS 1,2,4,5,7,8 SWITCHING	56	6.7	314	37.7	463	55.6
PINS 1,2 SWITCHING PINS 4,5,6,7,8 HIGH	14	3.5	156	39.3	227	57.2
PINS 1,2 SWITCHING PINS 4,5,7,8 HIGH, PIN 6 LOW	31	7.5	159	38.7	220	53.8
PINS 1,2,6 HIGH PINS 4,5,7,8 SWITCHING	18	4.7	163	42.9	199	52.4
PINS 1,2 HIGH, PIN 6 LOW PINS 4,5,7,8 SWITCHING	33	8.5	147	38.3	205	53.2

NOISE IN MILLIVOLTS AND PERCENTAGES GENERATED BY BONDING WIRE, CHIP-CARRIER AND SOCKET, ON Vcco PIN 3

MCA WITH SOCKET

V_{cc} PIN 60

CONDITION	NOISE IN MILLIVOLTS			
	A	B	C	
	SIMULATED	SIMULATED	SIMULATED	MEASURED
PIN 6 LOW SWITCHING PINS 1,2,4,5,7,8	149	127	75	
PIN 6 HIGH SWITCHING PINS 1,2,4,5,7,8	281	224	145	
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	52	48	32	
SWITCHING PINS 1,2,4,5,6,7,8	327	272	170	
PINS 1,2 SWITCHING PINS 4,5,6,7,8 HIGH	147	119	79	
PINS 1,2 SWITCHING PINS 4,5,7,8 HIGH, PIN 6 LOW	146	119	79	
PINS 1,2,6 HIGH PINS 4,5,7,8 SWITCHING	194	155	86	
PINS 1,2 HIGH, PIN 6 LOW PINS 4,5,7,8 SWITCHING	194	155	103	

SIMULATED NOISE AT POINTS A, B, C FOR V_{cc} PIN 60

DISTRIBUTION OF NOISE

Vcc PIN 60

	BONDING WIRE		CHIP CARRIER		SOCKET PIN	
CONDITION	A-B (MV)	%	B-C (MV)	%	C (MV)	%
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	22	14.8	52	34.9	75	50.3
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	57	20.3	79	28.1	145	51.6
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	4	7.6	16	30.8	32	61.6
PINS 1,2,4,5,6,7,8 SWITCHING	55	16.8	102	31.2	170	60
PINS 1,2 SWITCHING PINS 4,5,6,7,8 HIGH	28	19	40	27.2	79	53.8
PINS 1,2 SWITCHING PINS 4,5,7,8 HIGH, PIN 6 LOW	27	18.5	40	27.4	79	54.1
PINS 1,2,6 HIGH PINS 4,5,7,8 SWITCHING	39	20.1	69	35.6	86	44.3
PINS 1,2 HIGH, PIN 6 LOW PINS 4,5,7,8 SWITCHING	39	20.1	52	26.8	103	53.1

NOISE IN MILLIVOLTS AND PERCENTAGES GENERATED BY BONDING WIRE, CHIP-CARRIER AND SOCKET, FOR Vcc PIN 60

MCA WITHOUT SOCKET

V_{cco} PIN 3

CONDITION	NOISE IN MILLIVOLTS				
	PIN 6		A	B	
	SIMULATED	MEASURED	SIMULATED	SIMULATED	MEASURED
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	75	150	534	479	
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	135	195	528	470	400

V_{cc} PIN 60

CONDITION	NOISE IN MILLIVOLTS		
	A	B	
	SIMULATED	SIMULATED	MEASURED
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	213	141	
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	214	141	85

SIMULATED AND MEASURED NOISE ON PIN 6

" " " " " V_{cco} PIN 3, V_{cc} PIN 60 AT POINTS A, B, C

SIMULATION FOR $-V_{cco}$ BUS SPLIT

V_{cco} PIN 3

	NOISE IN MILLIVOLTS			
CONDITION	PIN 6	A	B	C
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	105	746	740	440
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	210	768	727	437
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	X	120	90	45

V_{cc} PIN 60

	NOISE IN MILLIVOLTS			
CONDITION	PIN 6	A	B	C
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING	105	140	126	72
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING	210	264	241	152
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	X	47	47	30

MCA WITH SOCKET

Vcco PIN 3

CONDITION	SIMULATED NOISE IN MILLIVOLTS			
	PIN 6	A	B	C
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING 1 Mf CAP. BETWEEN Vcc → Vcco	150	253	215	133
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING 1 Mf CAP. BETWEEN Vcc → Vcco	165	290	258	139
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	150	254	233	134
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	165	287	255	149

CAPACITOR BETWEEN POINTS 28 AND 22 }
SHORT BETWEEN POINTS 28 AND 22 } SEE MCA SPICE MODEL ATTACHED

MCA WITH SOCKET

V_{CC} PIN 60

	SIMULATED NOISE IN MILLIVOLTS			
CONDITION	PIN 6	A	B	C
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING 1μf CAP BETWEEN $V_{CC} \to V_{CCO}$	150	232	228	166
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING 1μf CAP. BETWEEN $V_{CC} \to V_{CCO}$	165	260	260	161
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING SHORTED $V_{CC} \to V_{CCO}$	150	231	231	162
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING SHORTED $V_{CC} \to V_{CCO}$	165	261	245	154

CAPACITOR BETWEEN POINTS 28 AND 22 }
SHORT BETWEEN POINTS 28 AND 22 } SEE MCA SPICE MODEL ATTACHED

DISTRIBUTION OF NOISE

Vcco PIN 3

CONDITION	BONDING WIRE A-B (MV)	%	CHIP CARRIER B-C (MV)	%	SOCKET PIN C (MV)	%
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING 1 µf CAP. BETWEEN Vcc → Vcco	38	15	82	32	133	53
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING 1 µf CAP. BETWEEN Vcc → Vcco	32	11	119	41	139	48
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	21	8.3	99	40	134	52.7
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	32	11.1	106	36.9	149	51.9

Vcc PIN 60

CONDITION	BONDING WIRE A-B (MV)	%	CHIP CARRIER B-C (MV)	%	SOCKET PIN C (MV)	%
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING 1 µf CAP. BETWEEN Vcc → Vcco	4	1.7	62	26.7	166	71.6
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING 1 µf CAP. BETWEEN Vcc → Vcco	0	0	99	38	161	62
PIN 6 LOW PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	0	0	69	29.8	162	70.2
PIN 6 HIGH PINS 1,2,4,5,7,8 SWITCHING SHORTED Vcc → Vcco	16	6.1	91	34.9	154	59

CAPACITOR BETWEEN [illegible] AND [illegible]

[illegible]

SIMULATED PROPAGATION DELAYS OF OEF'S

LEADING-EDGE

	PROPAGATION DELAY TO OUTPUT PINS (NS)						
CONDITION	1	2	4	5	6	7	8
PIN 6 LOW SWITCHING PINS 1,2,4,5,7,8	4.3	4.3	3.4	3.4	X	3.4	3.4
PIN 6 HIGH SWITCHING PINS 1,2,4,5,7,8	4.3	4.3	3.4	3.4	X	3.4	3.4
PIN 6 SWITCHING PINS 1,2,4,5,7,8 HIGH	X	X	X	X	2.6	X	X
SWITCHING PINS 1,2,4,5,6,7,8	4.4	4.4	3.5	3.5	3.5	3.5	3.5
PINS 1,2 SWITCHING PINS 4,5,6,7,8 HIGH	3.9	3.9	X	X	X	X	X
PINS 1,2 SWITCHING PINS 4,5,7,8 HIGH, PIN 6 LOW	3.9	3.9	X	X	X	X	X
PINS 1,2,6 HIGH PINS 4,5,7,8 SWITCHING	X	X	2.7	2.7	X	2.7	2.7
PINS 1,2 HIGH, PIN 6 LOW PINS 4,5,7,8 SWITCHING	X	X	2.7	2.7	X	2.7	2.7

THE INDUCTANCE OF THE BONDING-WIRE WAS CALCULATED BY USING THE FORMULA :-

$$L = 0.00508\, l \left\{ \left(2.303 \log_{10} \frac{4l}{d} \right) - 0.75 \right\} 10^{-6} \text{ HENRY}$$

WHERE l = LENGTH IN INCHES
d = DIAMETER IN INCHES

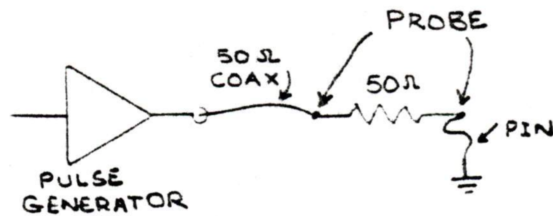
$l = 0.1''$
$d = .001''$

$$L = .00508(.1) \left\{ \left(2.303 \log_{10} \frac{4(.1)}{.001} \right) - 0.75 \right\} 10^{-6}$$

$$= .000508 \left\{ (2.303 \log_{10} 400) - 0.75 \right\} 10^{-6}$$

$$= .000508 \left\{ 5.99 - 0.75 \right\} 10^{-6}$$

$$= 2.66 \times 10^{-7} \text{ HENRY}$$



INDUCTANCE MEASUREMENT
FOR MCA SOCKET PIN :-

$$V = L \frac{di}{dt}$$

$$L = \frac{V dt}{di}$$

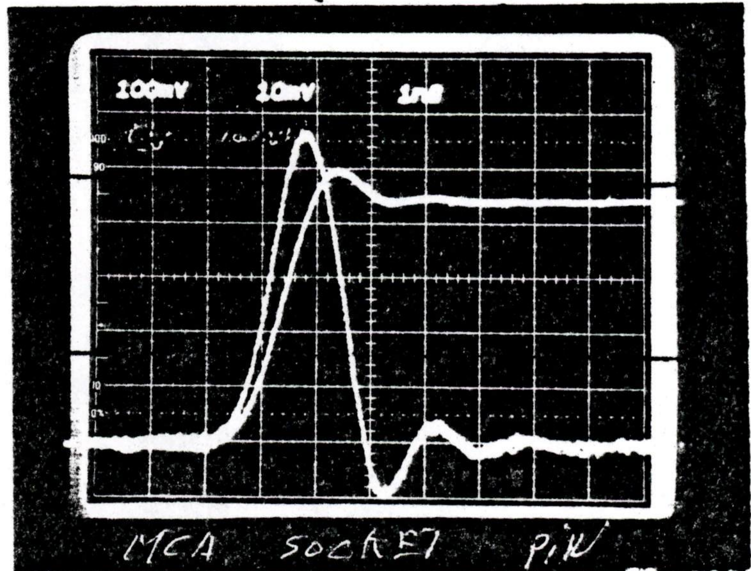
$$di = \frac{dV}{R}$$

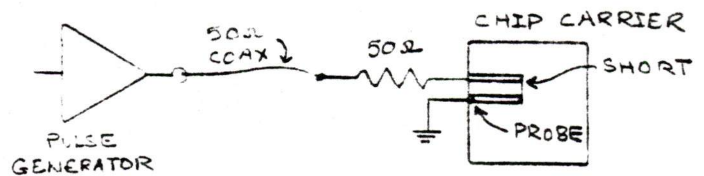
$$di = \frac{5V}{50\Omega} = 100MA$$

$$dt = 1.6 \times 10^{-9} \text{ sec.}$$

$$L = \frac{565 \times 10^{-3} \times 1.6 \times 10^{-9}}{100 \times 10^{-3}}$$

$$L = 9.04 \text{ NH}$$





INDUCTANCE MEASUREMENT
FOR MCA CHIP CARRIER :-

$$L = \frac{V dt}{di}$$

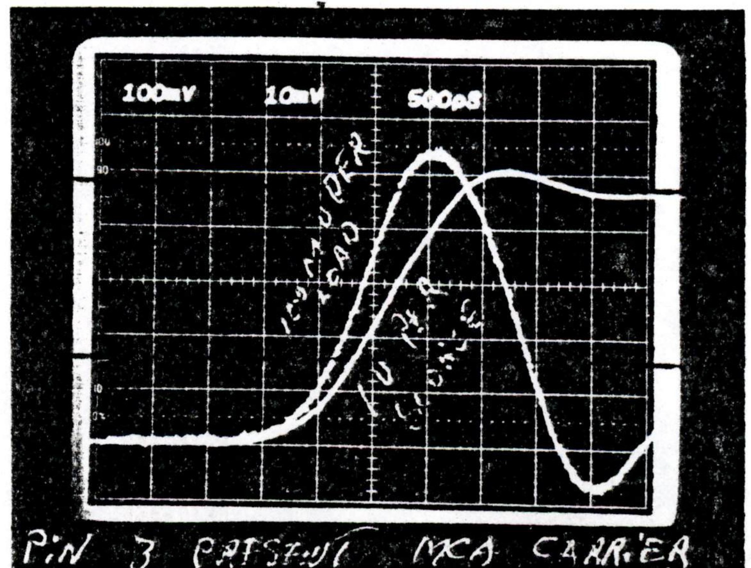
$$di = \frac{5.1}{50} = 102MA$$

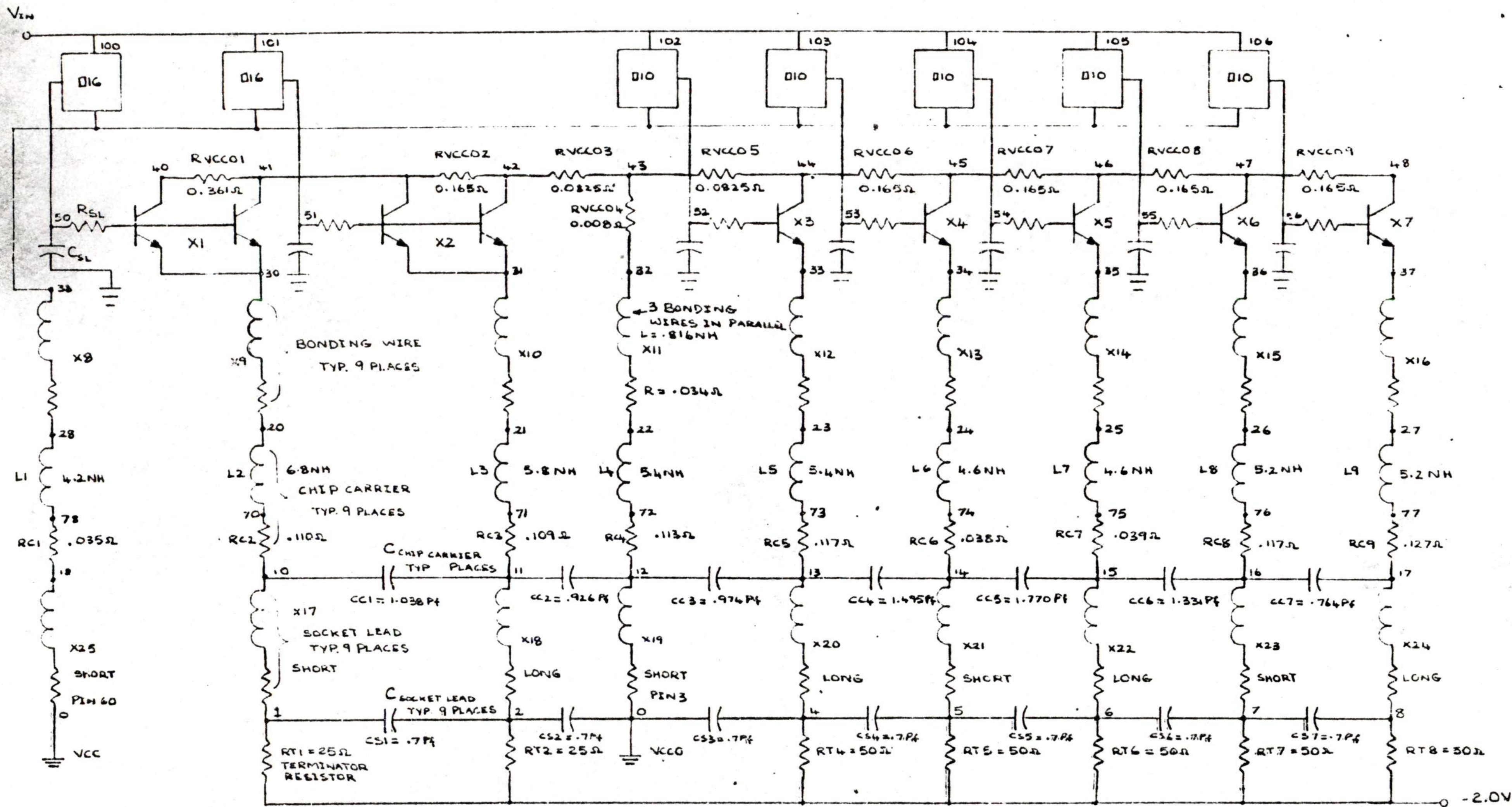
$$dt = 1.5 \times 10^{-9} \text{ sec.}$$

$$L = \frac{540 \times 10^{-3} \times 1.5 \times 10^{-9}}{102 \times 10^{-3}}$$

$$L = \frac{7.9 \text{ NH}}{2}$$

$\cong$ 4 NH FOR ONE PATH





RVCCO = RESISTANCE OF VCCO BUS

D16 = 25Ω MACRO

D10 = 50Ω MACRO

R_{SL} = 100 MILLS RESISTANCE SECOND LAYER

C_{SL} = 100 MILLS CAPACITANCE SECOND LAYER

MCA SPICE MODEL

(13)

INTEROFFICE MEMORANDUM

TO: Distribution

DATE: March 7, 1980
FROM: John Druke / Roger Scott
DEPT: L.S.E.G.
EXT: #4588 #5136
LOC/MAIL STOP: MR1-2/E47

SUBJECT: Study of the Effects of Various Cooling Parameters on Device Die Temperatures.

Introduction

The die temerature of a device and the difference between the die temperature of different devices on a module has significant impact on the performance of the Venus System. By effecting efficient thermal management of this system we will be able to adequately control the die temperatures and the differences between them.

This report expresses the experimental set-up that is being used to study the effects of various cooling parameters on the device die temperatures as well as some initial results used as an example of the data being recorded.

Die Temperature Measurement

To measure the temperature of a single device, a thermal die can be used. The thermal die is placed in the same package as the device being simulated. It has resistors that can be powered to dissipate the required amount of heat and diodes which, with the current passing through, have a temperature sensitive voltage drop and can be calibrated so that the die temperature can be measured.

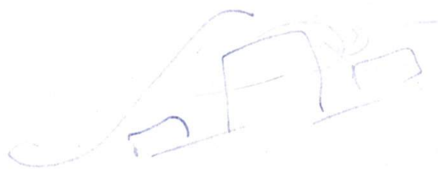
The schematic of a thermal die used to simulate an MCA chip is shown in Figure 1. The calibration of the diodes is accomplished by applying a 100 μamp current across the diode and immersing the device in an inert fluid bath. The temperature of the bath is varied and temperature vs. voltage drop data recorded (See Figure 2.). When the experiments are conducted, the voltage drop across the diode is measured and the temperature can be derived.

Die Placement at Module Level

Thermal dies simulating some different types of DIPs, RAMs, and MCAs will be used to study various configurations of device placement on an extended hex module for the Venus System.

The first set of tests use a module fully loaded with MCAs (Figure 3). From these initial tests, the time required for the system to reach thermal equilibrium was found and the slots in the CPU cage giving the worst thermal characteristics defined (These will be used to reduce the amount of future testing required.)

Future testing will include variations in the device arrangement. A board partially filled with MCA simulators will be tested to see when and what kind of baffles are needed. Then, DIP and RAM simulators will be added with the objective of defining rules for DIP and RAM placement as well as when heat sinks should be added.



Cabinet Mock-up

A mock-up of the Venus Cabinet was constructed to simulate what we expect the final configuration to be. Figures 4 and 5 show the cabinet with the components labeled.

Test Conditions

These tests were conducted in an ambient air temperature of 24°C.

The current supplied to the blowers was at 50 hz and 193 volts (Future tests will reveal the effects of having the current supplied at 60 hz and 230 volts.) 24.7 volts was supplied to each MCA simulator resulting in a nominal power dissipation of 4.5 watts each. Two modules were packed with resistors, powered to dissipate heat and placed on each side of the thermal board to simulate actual running conditions.

Initial Experimental Results

The first set of data was recorded to determine the length of time required for the system to reach thermal equilibrium. In subsequent experiments the system will be allowed to run this length at time before temperature measurements are recorded.

After the first fifteen minutes the thermal dies were at roughly 90-95% of the final readings. Over the next fifteen minutes, 21 of the thermal dies increased their temperature readings by 1°C. After fifteen more minutes 5 of the thermal dies increased their temperature readings by 1°C. The next fifteen minutes saw 4 of the devices increase by 1°C. Over the next hour, two devices increased their temperature by 1°C. (See Fig 6)

The conclusion drawn is that one hour is sufficient to allow thermal equilibrium to be reached.

The next set of data was recorded to find the worst slots in the CPU area. A sample of the data that was recorded is shown in Figures 7 and 8. The parameters used to determine which of the slots were the "worst" were, the average device temperature, the average air temperature rise across the board and the maximum die temperature difference. The results*are summarized in Table 1.

Slot No	Average Device Temp °C	2 Lowest Device Temp °C	2 Highest Device Temp °C	Max device °C Die temp diff.	Av. Air °C Temp diff.
1	100	85, 88	111, 112	27	11.3
2	101	85, 89	113, 114	29	11.5
3	104	88, 90	117, 117	29	12.3
4 ←	107	92, 94	120, 124	32	14.7
5	106	91, 94	118, 118	27	14.1
6	106	90, 93	120, 121	31	12.9
7 ←	107	90, 95	121, 122	32	12.9
8 ←	106	90, 94	121, 122	32	12.6
9	103	87, 93	115, 116	29	12.8
10	103	87, 92	115, 116	29	12.9
11	N O T U S E D				
12	102	87, 92	114, 117	30	11

TABLE 1

Arrows indicate worst slots.

* Data from device #26 was expelled on grounds of inconsistent performance.

As can be seen in Table 1, slots 4, 7, and 8 result in the greatest average device temperatures and temperature differences. These three slots will be used as further testing is conducted.

Conclusion

Besides setting us up to conduct future testing these initial data indicate some interesting results. First of all, the device die temperature and the rise in air temperature across the module are in the ball park of what we expected. The die to ambient thermal resistances of the MCA simulating devices are close to what had been predicted by the Thermal Engineering Group.

Secondly, for the first time, accurate measurements of the device die temperatures have been made. These temperatures give us an indication of the failure rate of a device. The die temperature difference between various devices can also be calculated. Previously, the average air temperature rise across the board was used to give an indication of the device die temperature difference. The data indicate that the device die temperature difference is actually quite higher, in fact, more than twice as great. This has some impact on the ability of devices to "communicate" with one another.

Future testing will include finding cooling methods for modules extended outside of the card cage being probed, for defects, verification of heat sink optimization, making breadboard preparations and testing various airflow arrangements.

/13 76L Test schematic 3/8/78 HG
68 LEAD LSI PACK

VEE POWER SUPPLY

IEE METER

VEE METER DVM

Pin	Element	Pins
30	R_1	29, 31
25	R_2	24, 26
20	R_3	13, 19
40	R_4	43, 46
	R_5	
11	R_6	6, 9
48	R_7	54, 55, 56
60	R_8	59, 61
5	R_9	63, 64, 65
28	D_1	32
23	D_2	27
14	D_3	22
42	D_4	41
	D_5	
10	D_6	12
57	D_7	47
62	D_8	58
3	D_9	4

V_{BE} (T_J, 100 ua)

DVM

100 ua

Heating Supply Must Be Floating Because Leakage in thermal Die causes errors in V_{BE} measurements.

Fig 1

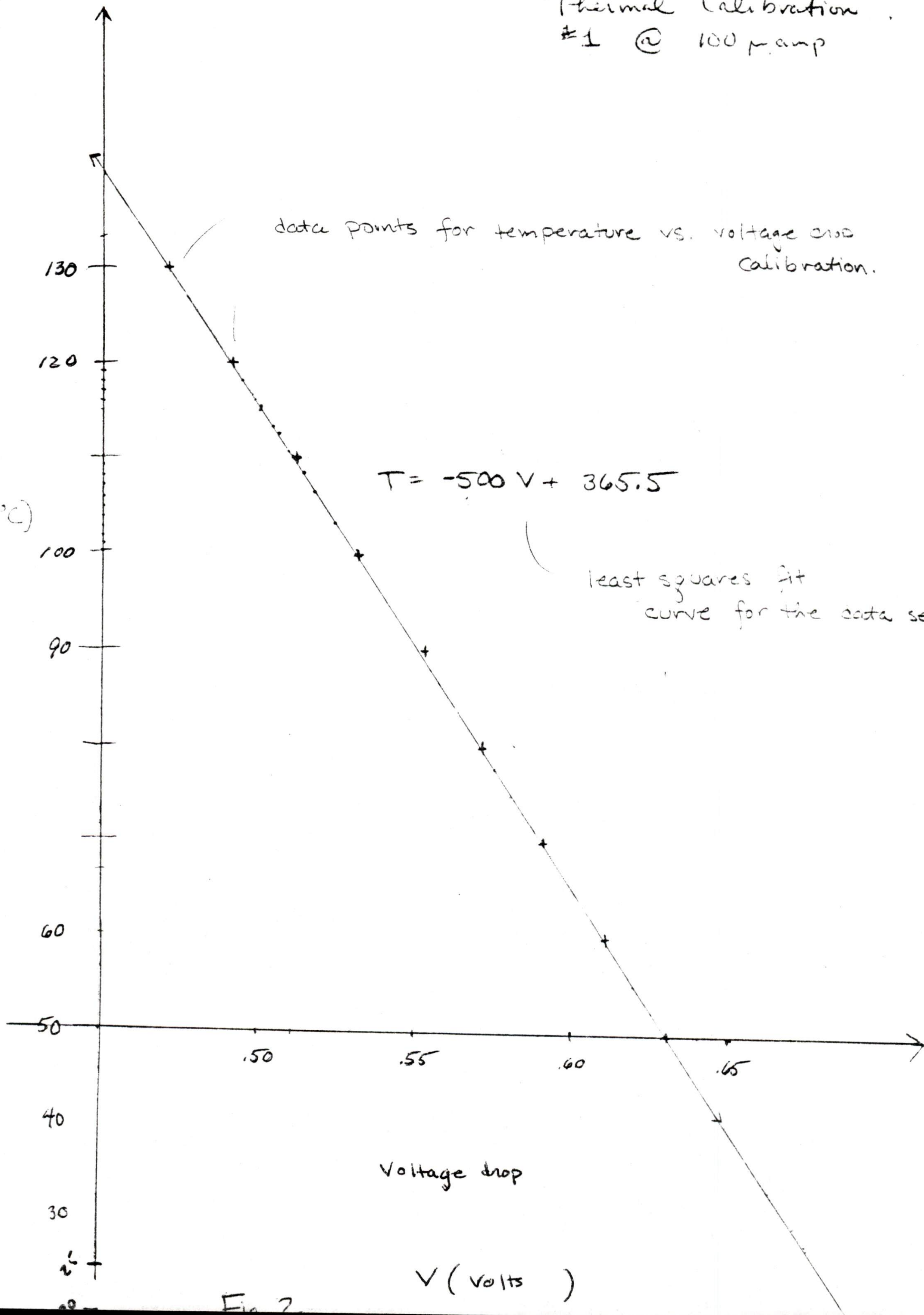


Fig. 2

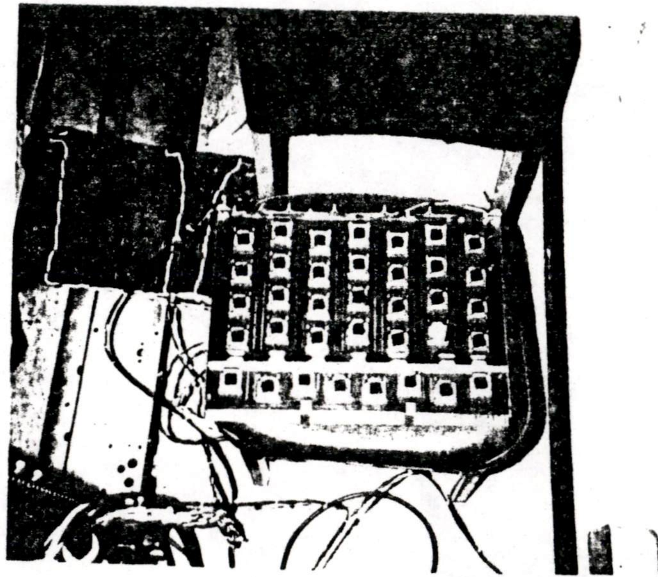


Fig 3. Extended hex loaded with MCA thermal dies.

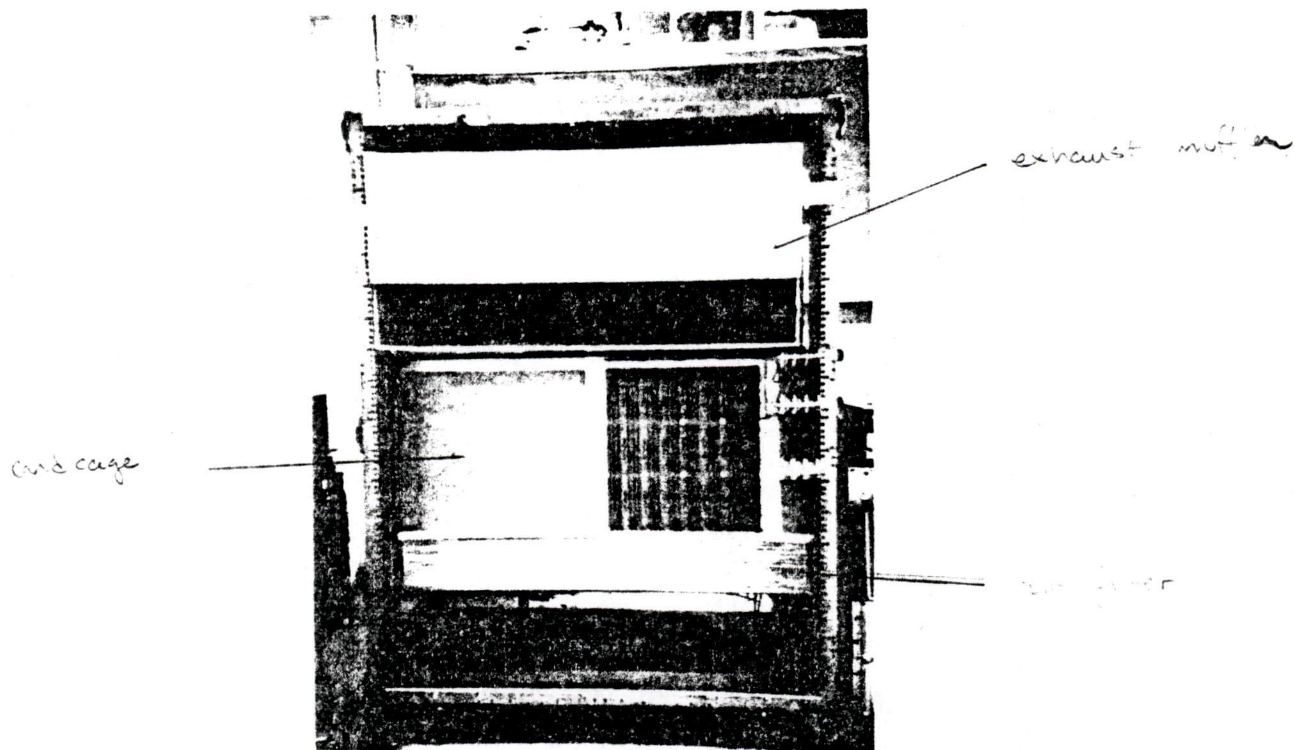


Fig 4 (front)

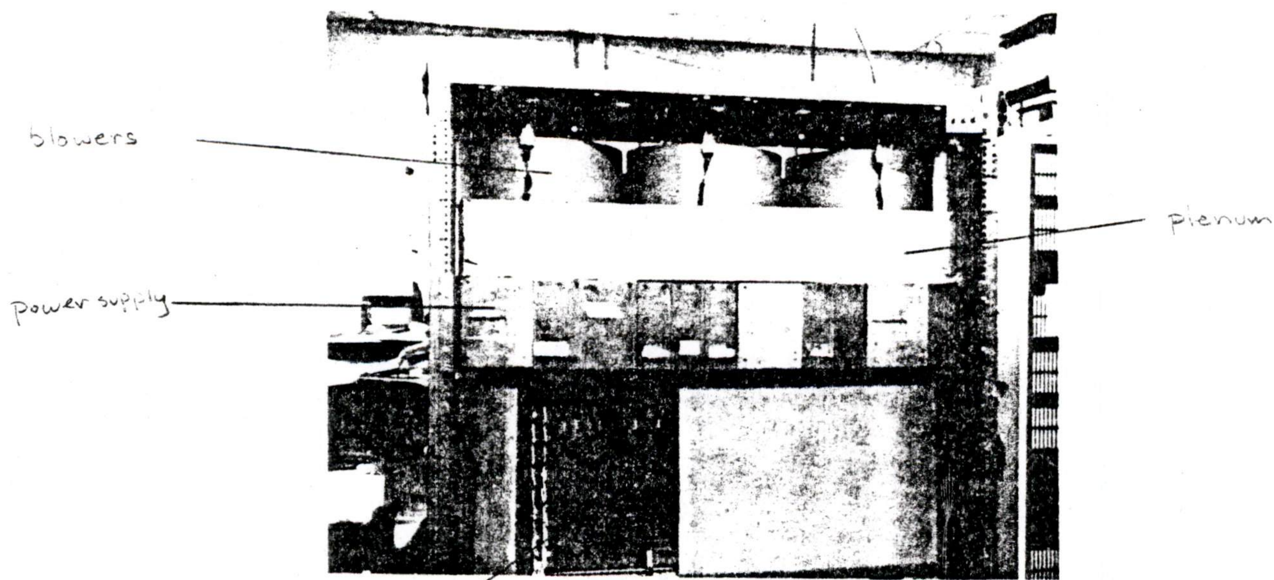


Fig 5 (back)

Graph of percent of dies reaching final temperature versus time. (Final temperatures refer to the temperatures recorded after 2 hours.)

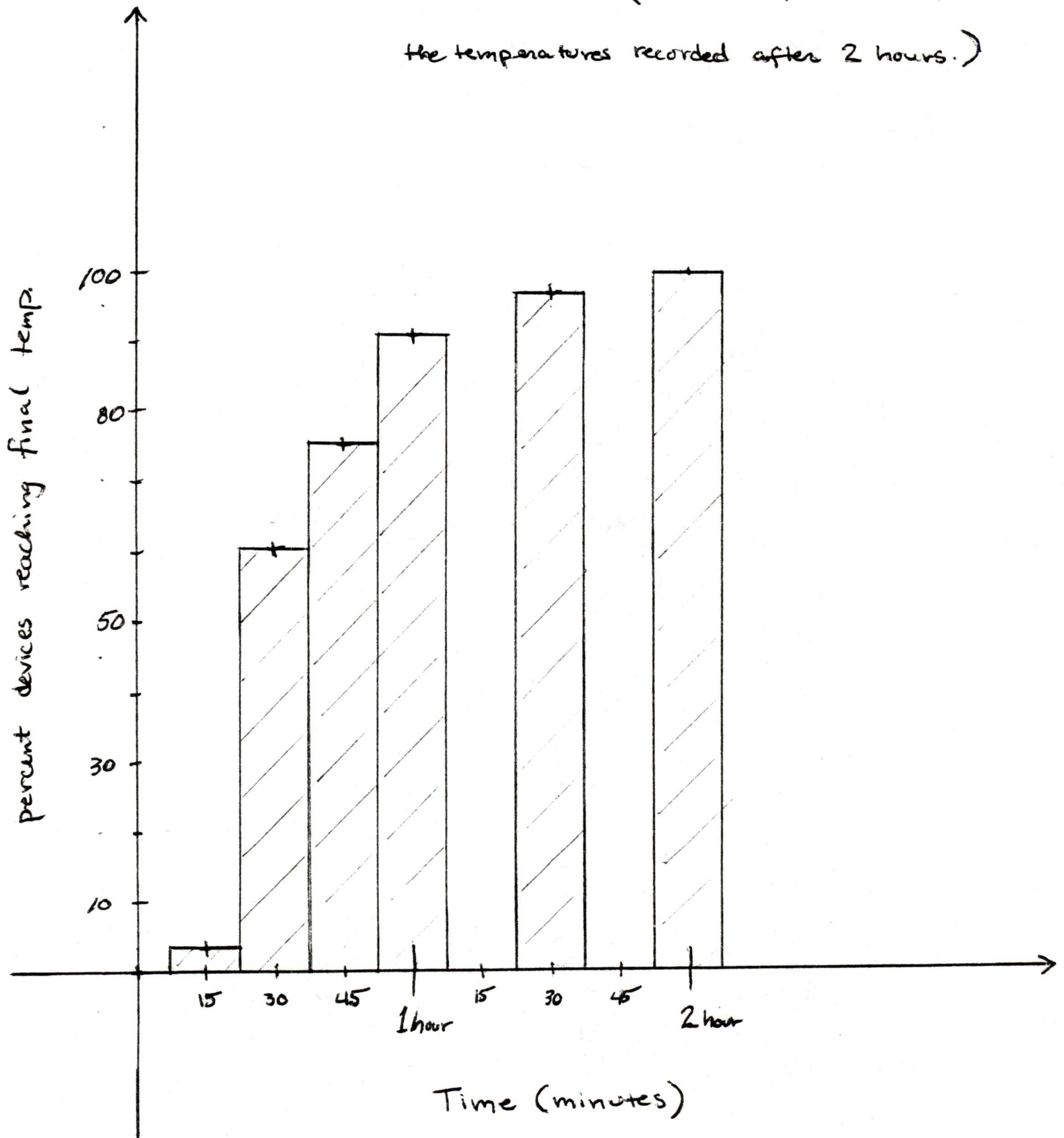


Fig. 6

AIRFLOW →

9:30 A.M. 3 MAR 80 SLOT 1

E36 546mv #3' 92°C	E31 545mv #28 95°C	E25 534mv #22 99°C	E20 532mv #17 102°C	E15 527mv #13 105°C	E10 513mv #8 111°C	E5 516mv #4 111°C	
E35 541mv #2' 97°C	E30 536mv #27 99°C	E24 543mv #21 97°C	E19 534mv #16 101°C	E14 533mv #12 102°C	E9 534mv #7 101°C	E4 521mv #3 106°C	
E34 561mv #31 88°C	E29 483mV #26 128°C	E23 536mv #20 99°C	E18 (X)	E13 534mv #11 103°C	E8 536mv #6 100°C	E3 527mv #2 104°C	
E33 565mv #30 85°C	E28 551mv #25 91°C	E22 547mv #19 94°C	E17 547mv #15 94°C	E12 540mv #10 98°C	E7 (X)	E2 539mv #1' NO CURVE	
E32 513mv #29 112°C	E27 538mv #24 99°C	E26 551mv #23 93°C	E21 535mv #18 99°C	E16 527mv #14 105°C	E11 517mv #9 110°C	E6 525mv #5 105°C	E1 517mv #1 106°C

FINGER SIDE

9:30AM 3MAR80 SLOT #1

Thermocouple temperature readings.

Thermocouple number	Location		Temperature (°C)
1	Module exhaust	Left	34
2	Module exhaust	↓	38
3	Module exhaust	↓	38
4	Module exhaust		37
5	Module exhaust	Right	32
6	Module inlet - left		25
7	Module inlet - right		24
8	Fan exhaust - left		23
9	Fan exhaust - mid		24
10	Fan exhaust - right		27
11	Ambient - Top cab left		23
12	Ambient - Top cab right		23
13	Ambient - removed (7 ft) high		23
14	Ambient - removed - low		23

Note: At module level, finger pins are on right.
At cab level, left, right references are facing backplane pins.
High ~ 6 ft
Low ~ 2 ft

Fig 8.

80-482 (14)

digital

INTEROFFICE MEMORANDUM

TO: [redacted]
Jim McElroy, MR1-2/E18

CC: Barbara Donohue, ML8-3/T13
Rob Hannemann, ML8-3/T13
Bob Lotz, ML8-3/T13

DATE: 18 FEB 80
FROM: N. Chris Paulhus NRP
DEPT: Product Acoustics
EXT: 223-6871
LOC/MAIL STOP: ML8-3/T13

SUBJECT: VENUS MUFFLER EVALUATION AND PRELIMINARY NOISE MEASUREMENTS

1. On February 12 and 13, 1980, Steve Weston and I conducted air flow and noise measurements on the VENUS mock-up. The first task was to evaluate the air flow effects of the different mufflers. Steve had cut an inspection hole in the scroll of the center blower and covered it with plastic plate. This allowed us to monitor the rpm of this blower with a stroboscope, which allowed us to go back to the Torin supplied fan curves and determine the operating point of the blower. Table 1 shows the different mufflers, the rpm of the center blower (taken with all three blowers on), and the derived cfm and static pressure conditions from the fan curves (the blower was also tested in our air flow chamber - the cfm and s.p. versus rpm relationship agrees with the Torin information within 5%).

TABLE 1: EFFECT OF VARIOUS MUFFLERS ON AIR FLOW

	Muffler	rpm	cfm	s.p.
1.	S curve muffler	1640 rpm	480 cfm	1.23 in. s.p.
2.	Regular radius with dividers	1645 rpm	470 cfm	1.27 in. s.p.
3.	Regular radius - no dividers	1625 rpm	505 cfm	1.15 in. s.p.
4.	Long muffler	1635 rpm	490 cfm	1.20 in. s.p.

2. We then measured the rear bystander position (1 m out, 1.5 m up from floor) noise levels of each muffler.

TABLE 2: VENUS NOISE LEVELS WITH VARIOUS MUFFLERS

	Muffler	Level
1.	S curve muffler	68.8 dBA
2.	Regular radius with dividers	67.8 dBA
3.	Regular radius - no dividers	67.5 dBA
4.	Long muffler	64.0 dBA

Due to the marked superiority of the long muffler, the preliminary noise measurements were made with this muffler installed.

3. I then made 1 m measurements of the untreated unit with the long muffler installed.

TABLE 3: VENUS MOCK-UP, UNTREATED, LONG MUFFLER

Position	Level
Rear	64.0 dBA
Side	60.2 dBA
Front	64.0 dBA

4. I then added absorption to the inside lower portion of the cabinet skins - around the air intake plenum, sealed off the midcabinet front louvers, and taped the door, side, and top gaps. The resulting sound level measurements are:

TABLE 4: VENUS MOCK-UP, TREATED, LONG MUFFLER

Rear - 61.5 dBA
Side - 57.0 dBA
Front - 59.2 dBA

These average out (four sides) to just below our goal level of 60 dBA. The treatments are crude approximations of what we expect to need in the final design. They do indicate that with the installed blowers and the long muffler, the 60 dBA goal level is attainable.

5. The long muffler is a severe interference with cable space. A shorter muffler would be 3 to 4 dB less effective. It appears that in order to go to the shorter muffler, we need blowers that are 3 to 4 dB quieter. Our tests and calculations of the installed blowers indicate that these units are 7 to 9 dB noisier than we expect them to be. We should easily be able to find replacements that are 5 or 6 dB quieter than the Torin units now installed in the mock-up.

   Our rough sound power measurements on the installed blowers indicate that we should be looking for a blower with a sound power output of somewhere between 75 and 80 dBA Lw at the operating point. We will be able to refine this figure this summer when our reverberation chamber is operating, allowing us to make precision sound power measurements on blowers.

mpe

Derrick Chin
Chuck Butala

VENUS POWER SYSTEM AND ENVIRONMENTAL MONITORING

POWER SUPPLIES

There is one power supply for the CPU bay and one power supply for the expansion memory bay. The power supplies are configured from various elements of the Modular Power System (MPS), presently under development by the Power Supply Engineering Group. The MPS consists of an AC to DC Input module from which several DC to DC output regulators are powered. The Input module rectifies three phase line voltages into a raw 300 VDC bus. Each output regulator then uses constant frequency pulse width modulation at 50/100 Khz to convert the 300 VDC to the desired output voltage.

MPS units used are:

2500 watt input module
5V 200A output regulator
5V 35A output regulator
2V 85A output regulator

Fig. 1 shows a block diagram of the power supplies. ECL voltages of -5.2V and -2.0V are directly tied in parallel where possible to minimize voltage differences between any two ECL gates and thus reduce ECL signal noise margin loss. The following DC power requirements were calculated for CPU, 3 memory boards and 5 I/O devices:

-5.2V @ 340A
-2.0V @ 110A
+5.0V @ 250A
+5.0V @ 42A (optionally battery backed up)
+12.0V @ 1A
-12.0V @ 1A

Optional battery back up will be available for backing up just the dynamic RAMS and refresh TTL logic of the main storage boards. A 48 volt battery with built in charger is converted up to 300 VDC to hold up the 300 VDC bus of the input module. All other regulators except the one being backed up, are turned off. Backup times range from 60 minutes for 1 storage board to 5 minutes for 3 storage boards. A separate 100 hour battery back up will be available for the time-of-year clock. The MPS can maintain proper output voltages for up to 12.5 milliseconds after line to neutral voltage drops below 90 VAC RMS.

The input modules are designed to run off three phase power in the U.S. and Canada. For other countries, an optional external transformer will be available to handle the numerous different line voltages. Mechanically, the input modules and output regulators are mounted side by side above the VENUS logic boards to be cooled by air exiting from the logic. Estimates of supply costs are MTBF are shown in Fig. 2.

FEATURES

Visual Aids

For the regulators
- module ok - Green LED
- overcurrent - Red LED
- overvoltage - Red LED

For the input module
in addition to the ones for the regulators
- AC OK - Green LED
- Overtemp - Mechanically latched colored disc

Logical Aids

Logic enable input - allows on/off control of regulator by console board through diagnostic. Monitoring of the module OK, signal then allows identification of defective regulator that is under console board control.

Margining

+5% margining - each regulator has logical inputs for margining the output voltage under console board control.

DC Power Sequencing

Regulators will be powered on in the following sequence:

first - all +5V units for storage boards, I/O devices and console TTL. These units are not under console board control but are enabled on by the auxiliary +12V output of the input modules.

second - all -5.2V units for ECL logic. These are under console control.

third - all -2.0V units for ECL terminators. These are under console control.

Power Modes

OFF no AC power at switched outlets of power controls. All fans off. Battery back up disconnected. Battery not being charged.

ON normal DC power sequenced on if console board is operational. All fans on. If installed, battery back up available.

STANDBY similar to ON except only RAMS and refresh TTL logic of storage boards are on. All other voltages are off. This allows servicing of all boards except storage boards and preserves memory data.

DC POWER DISTRIBUTION

The VENUS PC boards have three connection paddles of 94 pins each for a total of 292 pins per board. To maximize the number of pins available for signals in and out of the PC board, ground, -5.2V and -2.0V are brought into the board through new power connectors utilizing sections of the board that are presently unused. At the two inner notches, special power connectors mate to four pads on the board. These are ground connections. At both ends of the board, additional power connectors mate to four other pads on the board. These are for -5.2V and -2.0V. Forty of the finger pins are used for additional ground, +5.0V, +12.0V and -12.0V. This scheme results in 230 pins available for signals compared to about 168 for the hex board. Use of these special AMP power connectors require use of an aluminum frame through which logic ground current flows and a pair of horizontal bars at both the top and bottom edges of the logic back-panel for -5.2V and -2.0V distribution.

ENVIRONMENTAL MONITORING

In addition to the electronics for implementing the above features, DC output voltages, ambient temperature, logic board temperature rise and blower rotation will be monitored. Also, should a thermal switch in a regulator be activated, provision will be made for identifying the regulator even after the thermal switch has cooled off and re-opened. The electronics and electromechanical devices for all of the above, will be contained in a unit referred to as the monitor board. This will consist of a PC board plus a front panel on which LEDs and fuses will be mounted. The entire unit will plug into the power supply backpanel and will have dimensions similar to an 35 ampere regulator.

DC Voltages

There will be voltage detectors for sensing when a given output voltage is not within its normal operating range. Two means of implementing the detectors are being considered:

- Analog voltage comparators with fixed limits determined by a reference voltage and fixed resistors.

- A/D converter with 16 channel analog multi-plexers. Lookup tables for voltage limits and decision-making will be located in the CPU.

Temperature And Adequate Air Flow

Ambient temperature will be measured. Adequacy of air flow will be indirectly measured by measuring the rise in temperature of the air flowing through the logic assembly.

Ambient Temperature

A single linear thermistor network is mounted just below the logic assembly to measure incoming air temperature. When 32 degrees C is exceeded (yellow zone), a warning is put out on the teletype. When 42 degrees C is exceeded (red zone), a warning is put out on the teletype and a graceful power down sequence is initiated under diagnostic control. The yellow zone signal is also useful for warning that peripheral devices such as discs etc., may be operating beyond their recommended maximum temperatures.

Logic Temperature Differential

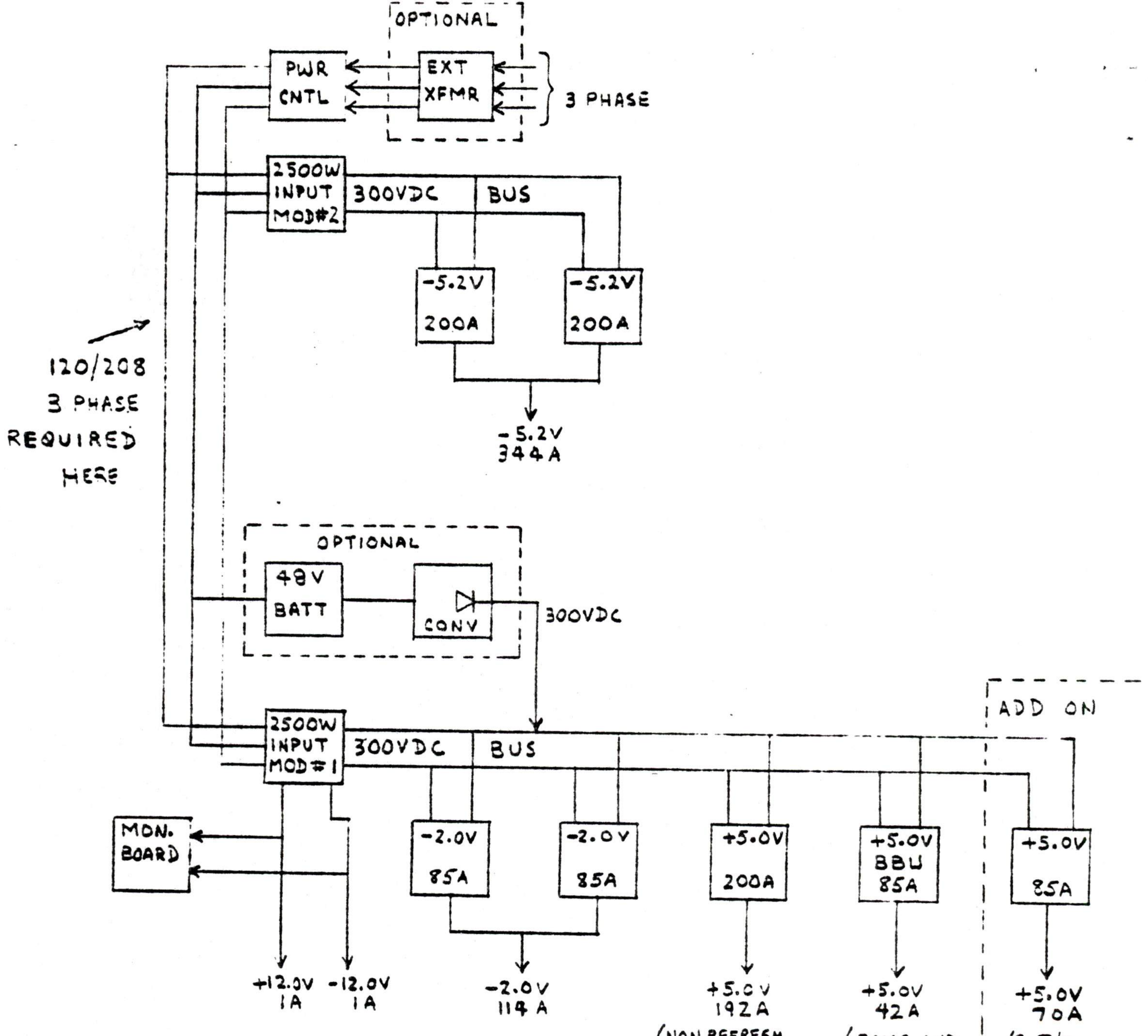
Three linear thermistor networks are mounted directly above the logic assembly, one network under each blower. They are used in conjunction with the ambient thermistor network to measure logic air temperature differentals greater than 10 degrees C such as caused by blower failure, air flow blockage or dirty air filters. When a 10 degrees C differential is exceeded, a warning is put out on the teletype.

Blower Rotation

Due to the wide variation of conditions under which the system must operate, e.g. low line to high line and sea level to 3000 feet altitude, it may be possible for a blower to fail without causing the logic air temperature differential to be exceeded. It is still desirable to identify the failed blower. Hall Effect switches are designed to be mounted inside the blower housing. A magnet is usually mounted on the rotating portion of the blower so that it passes close to the Hall Effect switch mounted on a stationary portion of the blower. Every time the magnet passes the switch, a pulse is emitted from the switch. Timing circuits will be provided on the monitor board to detect minimum blower rotational speed or stoppage.

Thermal Shutdown

A thermal switch is located in each output regulator. Its primary purpose is to close when the heat sink on which it is mounted exceeds a certain temperature due to a fault in the regulator. This temperature may also be exceeded if both yellow zone and red zone warnings do not result in preventive measures being taken. When a thermal switch is closed, a bicolored (black/yellow) magnetized disc flips from black to yellow and the power control is turned off through the DEC remote power bus. The disc will remain in the yellow position with power off and even with subsequent power on. A pushbutton is used to manually reset all the discs. There is one disc for each output regulator.

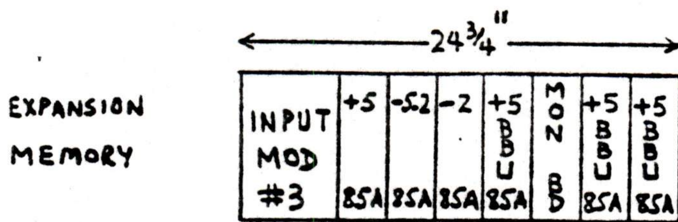


	P.S.#1	P.S.#2	
BACKPANEL DC POWER	1772	1789	watts
HARNESS POWER	78	61	watts
DC OUTPUT POWER	1850	1850	watts
EFFICIENCY	.74	.75	
INPUT DC PWR REQ'D	2500	2470	watts
POWER FACTOR	.6	.6	
INPUT AC PWR REQ'D	4170	4120	8290 volt amperes total

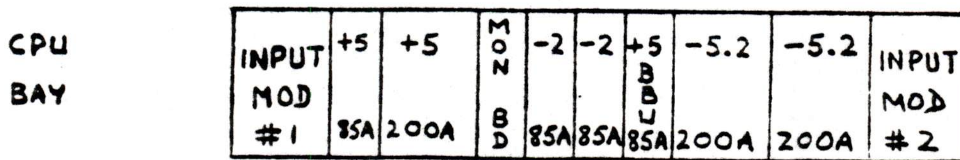
One power control can supply 8100 volt amperes.

FIG1A VENUS POWER SUPPLIES

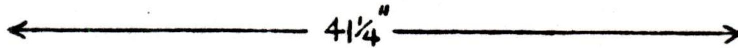
D. J. Ch[illegible]
2-24-[illegible]



WEIGHT, NOT INCLUDING RACK = 62 POUNDS



WEIGHT, NOT INCLUDING RACK = 100 POUNDS



AVAILABLE SPACE = 41.78" NOT INCLUDING P.S. RACK

ESTIMATED SUPPLY COSTS

CPU BAY

2 INPUT MODULES @ 280	560
3 200A UNITS @ 466	1398
4 85A UNITS @ 280	1120
BACKPANEL, FAB ETC	222
	3300
MONITOR BOARD	100
1 BATT PACK AND CONVERTER	300
	3700

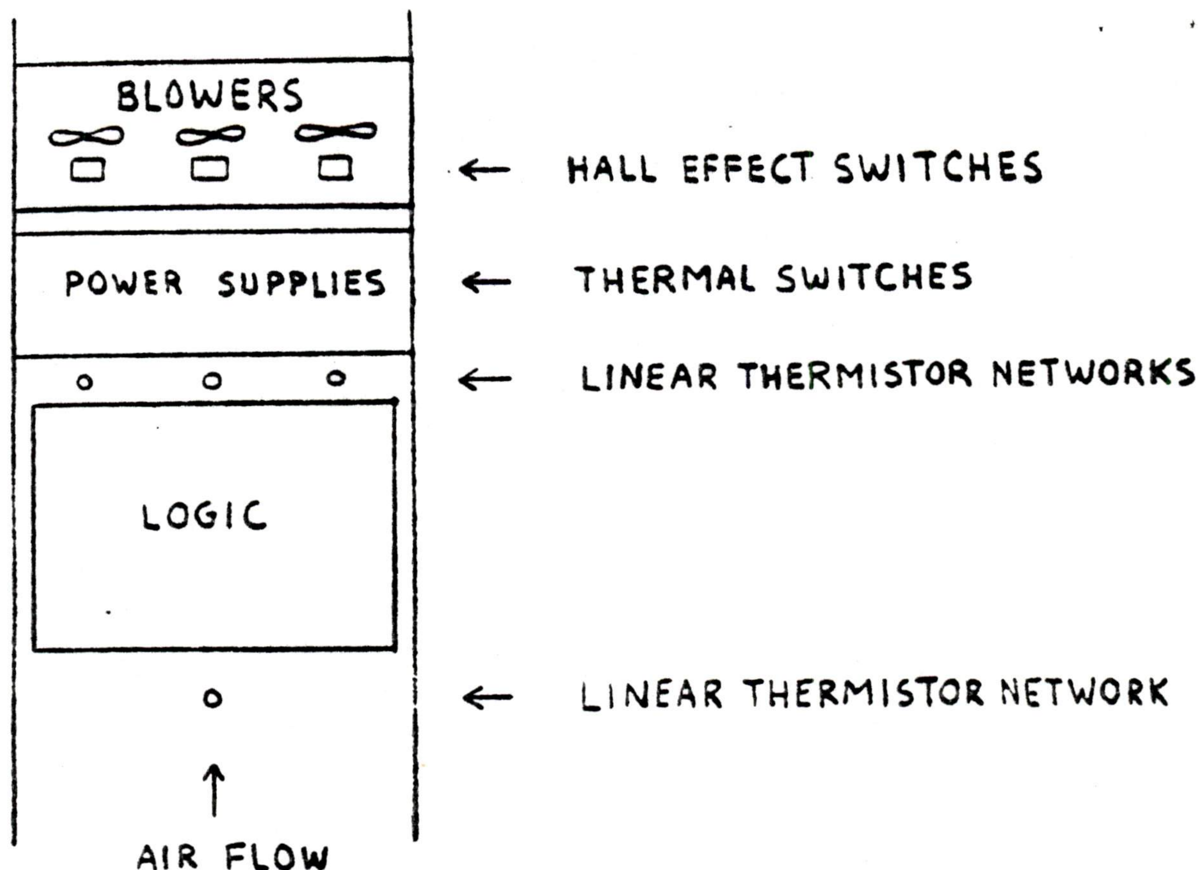
EXPANSION MEMORY

1 INPUT MODULE	280
6 85A UNITS @ 280	1680
BACKPANEL, FAB ETC.	240
	2200
MONITOR BOARD	100
3 BATT PACK AND CONVERTERS	900
	3200

MTBF

ESTIMATED FOR PWR CONTROL, INPUT MODULE, REGULATORS, MONITOR BOARD	WITHOUT BATTERY BACKUP		WITH BATTERY BACKUP		
	CPU BAY	EXPANSION MEMORY BAY	CPU BAY	EXPANSION MEMORY BAY	
BASED ON H217B CALCULATIONS (NOT INCLUDING CONNECTORS, FANS, ETC)					
221,000 HRS/UNIT GND BENIGN	20,000	25,000	18,000	18,000	HOURS
71,500 HRS/UNIT GND FIXED	6,500	7,900	6,000	6,000	HOURS
GUARANTEED BY PWR SUPPLY ENGINEERING 30,000 HRS/UNIT GND FIXED	2,700	3,300	2,500	2,500	HOURS

FIG 2



LINEAR THERMISTOR NETWORKS - SINGLE UNIT BELOW LOGIC IS USED TO DETECT INCOMING (AMBIENT) AIR TEMPERATURE GREATER THAN 32°C (YELLOW ZONE) AND 42°C (RED ZONE). THREE UNITS ABOVE LOGIC ARE USED WITH AMBIENT DETECTING UNIT TO DETECT LOGIC AIR TEMPERATURE RISE GREATER THAN 10°C.

HALL EFFECT SWITCHES - ONE INSIDE EACH BLOWER IS USED TO DETECT BLOWER ROTATION.

THERMAL SWITCHES - ONE IN EACH OUTPUT REGULATOR IS USED FOR FAIL SAFE SHUTDOWN OF AC POWER.

ENVIRONMENTAL MONITORS

TABLE OF CONTENTS

I. Introduction

II. Macrocell Array Concept

III. Macrocell Description

- A. Major Cell Description
- B. Interface Cell Description
- C. Output Cell Description

IV. Macrocell Array Design Considerations

- A. Unused Inputs
- B. External Pin Usage
- C. Macro Placement Considerations
- D. VIA Placement Restrictions
- E. Performance Characteristics
- F. Wire - ORing
- G. Voltage Levels
- H. Noise Margins
- I. Internal Voltage Levels

V. CAD Interface

VI. Packaging

VII. Applications

- A. Multiplier Design Example

APPENDIX

A. Macrocell Library

The MECL 10,000 Macrocell Array was developed for customers requiring complex high speed custom LSI circuits. A unique CAD interface provides an economical solution for custom circuits while providing fast turn-around time.

The material presented in this manual should enable the reader to determine whether the macrocell array will meet his system requirements. Also the reader will be able to partition his system into blocks using the Macrocell Library. An application example shows the logic implementation of an 8 X 8 2's complement multiplier and a worksheet shows the metal interconnect.

I. INTRODUCTION

The semiconductor industry has previously satisfied the customer's demand for LSI using three approaches:

1) Standard LSI circuits for volume production and lowest cost per function.
2) Custom circuits with high volume in order to lower development cost.
3) Gate arrays with medium volume requiring a metal interconnection mask.

The first approach, using standard LSI, such as the

M10800 family, is a very economical approach. However, many LSI functions that customers require are very complex, specialized, and in some cases proprietary.

The second approach provides the customer with custom circuits but the turn-around time can be 1 to 2 years. The custom approach also means the Semiconductor manufacturer must provide more design people to interface with the customer in developing custom chips requiring high development costs.

The third approach, using gate arrays, provides a quicker turn-around time since the basic array can be fabricated up to metalization. However, designing with gates requires the customer to interconnect simple gates into a common MSI and SSI functions normally used in logic design. This results in a longer MSI propagation delay compared to building the functions directly using ECL series gating techniques. Also, the interconnecting metal makes the chip larger than a custom designed circuit. Finally, there is the customer interface problem of handling and producing the metal masks and the testing of the packaged arrays.

II. MACROCELL ARRAY CONCEPT

The approach taken by Motorola is the development of the MECL 10K MACROCELL ARRAY with industry standard MECL 10K compatibility. The array is an extension of the gate array concept presently being used in mainframe computers. Instead of gates, each cell in the array contains unconnected transistors and resistors. There are standard logic elements such as a dual D flip flop, dual full adder, quad latch, and many other functions. These macros are interconnected using series gated ECL structures in order to optimize performance. Presently a library of 85 logic functions, called Macros, can be selected. Thus, the designer need only be concerned with interconnecting the logic functions contained in the library. There are a total of 106 cells on each Macrocell Array chip. A CAD (computer aided design) system containing the cell library speeds up the option development while simplifying the designer/Motorola interface. The CAD system is operated via standard time sharing terminals to design the interconnects, to check out the performance of the design, and to generate the custom metal patterns which complete the IC processing sequence.

A new process called MOSAIC I (see Figure 1) is used in the Macrocell Array in order to achieve the high performance requirements of .9ns (typical) for internal gate

delays. The process forms a non-walled emitter and a walled base. An oxide isolation between devices is accomplished with an isotropic etch. The peaking of the oxide is controlled and monitored to guarantee flatness during processing. The peaking of the oxide is maintained to less than 4000 Å thick. The first layer metal is 10,000 Å thick which covers the peaking of the oxide reliably. A nitride surface covers the oxide so that the metal system is over nitride which is normal in other MECL processes. The base and emitter diffusions are controlled by ion implantation to a junction depth used in other processes. Also, the oxide isolated process achieves a high packing density while achieving good yields.

The high packing density of the Macrocell Array lowers system component count, reduces power dissipation (by a factor of 5 over discrete logic), while increasing system speed and reliability. Up to 50 discrete IC logic packages can be replaced by one Macrocell Array. Parts can be developed in a short period of time for a new product. Interconnects remain proprietary to the customer.

Customer product development is speeded up with a 12 week turn-around from the time the customer gives the go ahead for generating the metal mask until he receives the finished parts.

In summary, the MECL 10K Macrocell Array achieves over discrete IC logic:

1) A reduction in part count of up to 50 to 1.
2) A reduction in power of 5 to 1.
3) Fast internal delays of .9ns typical.
4) An "equivalent" gate delay of .6ns for many macrocells.
5) A large selection of macros.
6) And proprietary custom parts at a relatively low cost.

III. MACROCELL ARRAY DESCRIPTION

There are a total of 106 cells organized on the Macrocell Array chip as shown in Figure 2. There are 48 major cells (M), 32 interface cells (I), and 26 output cells (O). All macrocell array chips are built from a standard semiconductor diffusion set up to metalization. Appendix A contains a cell library of 85 logic functions called macros. A macro (sometimes called macrocell) is a first layer metal intraconnection pattern that interconnects the components of a cell into a specific logic function. There are 54 macros for major cells, 14 macros for interface cells, and 17 macros for output cells. The CAD system contains the required first layer metalization pattern for each macro as well as the I/O ports.

Each major cell can be divided into two independent half cells, an upper half and a lower half. As an example, the upper half of a major cell could be designated a D flip flop (½ of M31 in Appendix A) and the lower half a full adder (½ of M52).

The power, ground, and bias supply lines are not shown in Figure 2. These interconnects are automatically accomplished by the CAD system. Figure 2 shows only the free channels that are used by the designer to interconnect the

cells in the array. The 100 channels in the vertical direction are accomplished on first layer metal while the 130 channels in the horizontal direction are accomplished on second layer metal. Note that the second layer metal can be placed over the cell without interferring with the macro in that cell since all macros are intraconnected on first layer metal. The second layer metal is separated from the first layer by an oxide isolation. Metal runs on the chip have little affect on delay times because of the oxide isolation between metal and active devices. Connections between 1st layer and 2nd layer metal are accomplished with VIA's. The interconnecting of cells on the array can be compared to routing signal lines on a two sided PC board.

The important features of the array are listed in Figure 3. The array could contain up to 1192 equivalent gates if all the major cells contain dual full adders, M52 (a total of 96 adders at 10 gates per adder) and the interface and output cells contain latches, I14 and O14 (a total of 58 latches at 4 gates per latch). The number of equivalent gates for each macro can be found by counting the number of gates given in the library (Appendix A). Note that a 2 input exclusive OR gate is counted as 3

D. VIA PLACEMENT RESTRICTIONS

In the routing alleys (see Figure 2) the only restriction on via's (connection between 1st and 2nd layer metal) is that adjacent horizontal via's are not allowed. This restriction has very little impact on laying our a circuit. Adjacent vertical and adjacent diagonal via's are allowed.

E. PERFORMANCE CHARACTERISTICS

The Macrocell Library in Appendix A contains the performance characteristics of each macro logic function. The worst case propagation delay is specified for V_{EE} = -5.2 volts ±10% and a T_J max = 130°C, the maximum operating junction termperature is 165°C. A 10% lower power dissipation can be obtained by operating the chip at the lower V_{EE} limit of -4.68 volts. If the array is operated above the 130°C junction temperature, a slight degradation of the propagation delay numbers in Appendix A will occur (approximately 15% when the junction temperature is 165°C).

In order to maintain a reasonable junction temperature (and adequate noise margins), the customer is required to connect a Motorola recommended heat sink to the package and operate the device with a recommended air flow of 1000 lfpm (linear feet per minute). This combination results in a θ_{JA} (thermal resistance from junction to ambient) of 15°C/watt. If the system designer maintains the ambient temperature at 55°C, then a 5 watt maximum chip dissipation would result in a junction temperature of 130°C (thus, there would not be any propagation delay degradation for the numbers given in

Appendix A). For high utilization of the chip (around 90%), the typical power dissipation will be around four watts.

The performance of the macros specified in Appendix A in regards to fanout and loading is as follows.

For the Major and Interface Cell macros, the maximum values given for propagation delay are for a 1 or 2 ma output follower current driving a fan-out of 3 or a .5 ma output follower current driving a fan-out of 1. For the output cell macros, the maximum propagation delay for the Y output is specified at 2.2 ns from the 50% point of the input to the 50% point of the output when driving a 50 ohm load (a 25 ohm load for 016 and 017 driver) to -2 volts.

The Output Cell macros can be used as interface cells by using the Y1 output. The maximum propagation delay for the Y1 output driving a fan-out of three is 1.5 ns when the Y output is not used. (2.2 ns when the Y output is used).

1. Metal Interconnect Length

The metal interconnect between the macros in the array represents a line capacitance (.005 pf/mil maximum for both first and second layer metal) to the driving gate. This line capacitance primarily effects the fall time at the gate output and causes a slight degradation in propagation delay. Figure 2 shows the dimensions of the chip so that the metal interconnect length can be closely approximated.

The propagation delay degradation (due to metal length) for the output switching from high to low (Δtpd-) for various output follower currents is as follows:

Δtpd- = .6 ps/mil	for 2ma output follower current
Δtpd- = 1.4 ps/mil	for 1ma output follower current
Δtpd- = 3.8 ps/mil	for .5ma output follower current

The propagation delay degradation (due to metal length) for the output switching from low to high (tpd+) for .5, 1, or 2ma output follower current is:

Δtpd+ = .6 ps/mil

For long lines, a 2ma output follower current should be used to minimize delay degradation and skew. A line that is 100 mils long will increase the propagation delay (tpd-) of the driving macro by 60 ps for 2ma follower current or 380 ps for a .5ma follower current. These are worst case numbers. The delay degradation due to metal length on the input to the chip and on the output of the chip is negligible and may be ignored. The reason for this is the low impedance drive of the driving gate (normally 50 ohms).

2. Fanout

The propagation delay degradation due to fan-out has been analyzed by computer simulation. The results show that the fan-out delay degradation (for the output going high or low) is Δtpd = 60 ps/fan-out for .5, 1, or 2ma output follower current.

This equation is good for a fan-out of up to 3 for .5ma output follower current, a fan-out of 6 for 1ma output follower current, and a fan-out 12 for 2ma output follower current.

The propagation delay of a macro given in Appendix A must be increased by 60 ps/fan-out for fan-outs of 4 or more with output follower currents of 1 or 2ma. For a .5ma output follower current the propagation delay must be increased by 60 ps/fan-out for fan-outs of 2 or more.

As an example of delay degradation due to fan-out and metal length, assume that a 4 - 1 MUX is driving a fan-out of 5 with a total interconnect lenght of 100 mils. From Appendix A the propagation delay from data input to output is 1.5ns (tpd). If a 1ma output follower is selected, then the increase in delay due to the fan-out is 120ps and 140ps for the metal length. Then, the total propagation delay is 1.76ns. If a 2ma ouput follower current is selected, then the total delay would be reduced slightly to 1.68ns. A .5ma output follower current is normally used in non-critical delay paths in order to save power.

3. Rise Time

When external inputs drive the array, the rise and fall times should be 1ns (20 to 80%) in order to meet the propagation delay specified in Appendix A. Slower

rise and fall times increase the propagation delay. When a MECL 10K gate with a 3.3 ns max rise and fall time drive the array, 400 ps delay should be added to the input macro delay time. For a 2ns edge, 175ps delay should be added.

For each nanosecond increase in rise or fall time, 175ps in delay should be added. The output rise and fall times of the output cell is 1ns min, 1.5ns typical. If the maximum output rise and fall time is 2.5ns then 265ps should be added to the input macro delay time when one macrocell array is driving another.

THESE SAME NUMBERS APPLY WHEN EXTERNAL INPUTS DRIVE INTERNAL CELLS (i.e. MAJOR CELLS) & OUTPUT CELLS

4. Input Follower

All the pins that are not used for power can be used as inputs to the array. Inputs from the bonding pad pins can be connected to inputs of major, interface, or output cell macros. However, if the input pin is connected to an input follower (denoted by asterisk, *) of a major cell macro, a maximum of 300ps should be added to the propagation delay due to possible soft

saturation under worst case conditions. UNTIL WE CAN GET MOTOROLA TO SPEC THIS WORST CASE DO NOT BRING INPUTS INTO MAJOR CELL LOWER INPUTS THAT IS THOSE MARKED WITH AN ASTERISK

In addition, the ECL outputs (outside the chip) driving an input follower of a major cell, should be loaded with 50 ohms to -2 volts in order to keep V_{OH} at specified limits (a 510 ohm load would result in a higher V_{OH}). The reason for this slight restriction can be seen by comparing the input follower circuit of a major cell macro (Figure 5) and an interface cell macro (Figure 7). The interface cell macro contains an extra diode in order to prevent soft saturation under worst case conditions. The diode and a couple of other components were not added to the major cell in order to reduce chip size. Also the diode adds an extra 100ps of delay. Since most connections to the input of major cell macros would be internal connections, components were reduced and propagation delay was optimized. No extra delay need be added when circuit inputs to the array are connected to the top portion of the current tree (inputs A and C in Figure 5) of a major cell. Also no extra delay need be added when any circuit input of a major cell macro is connected to the output of other interface or major cell macros in the array.

If the Y1 output of the Output Cell macro is driving the input follower of a Major Cell macro, 300ps should be added to the propagation delay if the Y output (of the same output macro) is unloaded. If the Y output is loaded externally with 50 ohms, then an additional 150ps should be added to the propagation delay. The reason is the same as given above for an external MECL signal driving an input follower of a Major Cell macro. The Y1 output has normal 10K voltage levels instead of the reduced 650mv internal levels. The internal voltage levels are more fully discussed in Section I.

F. Wire ORing

Outputs of interface and major cells can be tied together to form a wired OR function. The sum total output follower current allowed with wire ORed outputs is 2mA. Up to four outputs can be tied together for a total output follower current of 2mA. Up to two outputs can be tied together for a total output follower current of 1 to 2mA (.5mA not allowed). With wire ORing it is recommended that the output follower current be divided equally among the outputs. For instance, when four outputs are tied together each output should be selected for .5mA.

When outputs are tied together, current will flow from the output that is "high" to the load resistors located at other outputs. This current causes a small IR drop, which decreases the noise margin. The maximum IR drop allowed is 25mV. The resistance of first layer metal is .2 ohms/mil while the resistance for second layer metal is .062 ohms/mil. For instance, assume there is a metal run of 100 mils total between two outputs tied together where 50 mils is on first layer and 50 mils is on second layer. A 1mA output follower current at each output would

mean that 1mA of current would flow from the output that is "high" to the other output when in the "low" state. This could cause a voltage drop of 10mV on first layer and 3.1mV on second layer for a total drop of 13.1mV. The wired OR outputs should be physically as close as possible to reduce loss of noise margin.

Wire ORing of internal macro outputs will cause some degradation which should be added to the propagation delay specified in Appendix A. The propagation delay degradation for the output falling, $t_{pd}-$ is a maximum of

$$\Delta t_{pd}- = 20ps/wire\text{-}OR$$

This degradation is small since the delay is due to a very small capacitance associated with the additional output device on the line. The propagation delay for the output rising, $t_{pd}+$, is much larger as shown in the Table 1 below. When two macro outputs are wire ORed and both are in the "low" state, one output could be supplying more current to the load resistors than the other output (called current hogging). When the output that is supplying the

smallest amount of current switches to the "high" state, it must now supply all of the current resulting in the additional delay shown in Table 1. The Table also shows the allowable combination of the number of wire OR's versus the required total output follower current.

Table 1. Maximum Delay Degradation for Output Rising, $\Delta t_{pd}+$, Versus the Number of Wire OR's and Output Follower Current.

Total Output Follower Current (mA)	$\Delta t_{pd}+$ in ps		
	Wired OR of 2	Wired OR of 3	Wired OR of 4
1.0	150	—	—
1.5	225	275	—
2.0	300	350	400

Wire ORing of the output emitter followers of the output macros (Y output) is not allowed on the chip due to voltage drops on the chip. However, a wire OR of two Y output may be connected on the chip when using the bonding pads that have two emitter followers (pins 67, 68, 1, 2, 16, 17, 18, and 19). A wire OR

of two or more Y outputs can be performed outside the package but this reduces the number of bonding pads available for other input signals.

Eight of the 26 bonding pads have two output emitter followers for driving 25 ohms when the driver of the transceiver macros is connected. A ninth 25 ohm driver is possible by connecting the output of the transceiver macro to two adjacent bonding pads that have single emitter followers and connecting these pads outside the package (it is not allowed to connect these pads on the chip).

It should be noted that the delays shown in Table 1 are specified for wire ORing of interface and major cell macro outputs as well as the Y1 output of the output cell macros.

G. VOLTAGE LEVELS

All input and output levels (including input thresholds) of the Macrocell Array are specified exactly the same as the MECL 10,000, MECL 10800, and MECL III families over the temperature range. In addition, the Macrocell Array is voltage compensated so that it can be operated over a range of V_{EE} = -4.68 volts to -5.72 volts with little change in performance. The voltage tracking rates are:

1) ΔV_{OHV} = 10mv/volt
2) ΔV_{BBV} = 45mv/volt
3) ΔV_{OLV} = 60mv/volt

The output levels and input thresholds are the same for devices that have the same ambient temperature even though the junction temperature of the devices can be different. This is partly accomplished in the design of the bias driver. The bias driver is designed to automatically adjust the bias voltages according to the current being drawn through the V_{CC} pin. If part A uses one watt (the junction temperature will be 40°C at 25°C ambient) and part B uses five watts (the junction temperature will be 100°C at 25°C ambient) the following voltages would result:

	PART A	PART B
V_{BB}	-1.2806	1.2790
$V_{BB}1$	-2.0639	-1.9701
V_{CS}	-3.9812	-4.0468
V_{OH}	-0.9296	-0.9146
V_{OL}	-1.7343	-1.7466

As can be seen above the voltages remain fairly constant even though the difference in the junction temperature is large. These voltages also remain constant for two identical arrays from different lots. For instance, part B of lot 1 may dissipate 3.875 watts minimum and part B from lot 2 may draw 6.125 watts maximum. In conclusion, the junction temperature differentials due to variations in I_{EE} are taken care of as standard design practice in the design of every MECL device. The parametric voltage levels (such as V_{OHA}, V_{OLA}, V_{IHA}, and V_{ILA}) which specify noise margin are tested and specified over temperature and include variation of junction temperature due to variations in I_{EE}, θ_{JA}, and output power. These levels are guaranteed for the Macrocell Array when using the recommended heat sink and 1000 lfpm of air flow. Under these conditions, the θ_{JA} is 15 ± 2°C/watt.

H. NOISE MARGINS

The worst case noise margins (NM) for the Macrocell Array over temperature (0 to 70°C ambient) for a V_{EE} = -5.2 volts in NM_{High} = 125mv, NM_{Low} = 155mv. These values assume that the recommended heat sink and 1000 lfpm is used. The V_{EE} regulation and the ambient temperature differentials between packages will reduce these numbers slightly.

Figure 11 shows a tabulation of noise margins for a 10°C ambient temperature differential between packages combined with power supply regulation of ±2%, 0 to 5%, and ±5%. With a 1000 lfpm of air flow, a temperature differential of 10°C max is realistic.

When the Macrocell Array is used, power supply regulation has a negligible effect on noise margins. It is interesting to note that it is actually possible to gain noise margin when intermixing the voltage compensated Macrocell Array and MECL 10K.

I. INTERNAL VOLTAGE LEVELS

The output voltage levels of the Interface, and Major cell macros (and receivers of Output cell macros) are as follows for inputs at V_{IHA} min. and V_{ILA} max.

OUTPUT FOLLOWER Current (ma)	V_{OH} (volts)	V_{OL} (volts)
2	-1.0	-1.64
1	-.975	-1.62
.5	-.95	-1.6

Note that the internal output voltage swing is smaller than the external output voltage swing. The input threshold voltage is the same as specified for MECL 10K of V_{IHA} min = -1.105 volts and V_{ILA} max = -1.475. The reason for the smaller swing is to maintain high speed operation.

As discussed the previous section, noise margin between chips in a system is determined by the voltage regulation (line drops) and temperature differentials. However on the chip, the temperature is constant with essentially $0^{o}C$ temperature differential. Each of the macro functions on the chip have the same value of power supply voltage (due to common mode on the chip) regardless of the external power supply regulation. Therefore, the noise margin for the internal voltage swings is:

NM_H = 1105-1000 = 105mv

NM_L = 1600-1475 = 125mv

V_{EE} = -5.2v

The noise margins get larger for V_{EE} >5.2 volts. If V_{EE} = -5.2v $\pm$ 5% (V_{EE} will get as low as -4.96 volts), then the internal noise margins will be reduced slightly to NM_H = 96mv and NM_L = 121mv.

The short line length of interconnections internal to the chip eliminates the need for transmission lines. In general, internal noise immunity will be greater than the noise immunity between chips in a system.

The output voltage swing for the Y1 output of the Output Cell macros is larger than the internal voltage swings of the other macros. The reason is that the Y output of the output cell must be 10K voltage compatible so the voltage at the base of the output emitter follower has a larger swing. If the Y output is loaded with 50 ohms to -2 volts, the Y1 output levels are V_{OH} = -.90 volts and V_{OL} = -1.7 volts. If the Y output is unloaded, the Y1 output levels are V_{OH} = .83 volts and V_{OL} = -1.7 volts. The noise margin for the Y1 output is larger than the numbers indicated above due to the larger voltage swing.

VI. PACKAGING

A new LSI package is being used for the Macrocell Array as shown in Figure 13. The 68 pin leadless package has been developed in accordance with the "JEDEC LSI package standard". 3M and Kyocera are manufacturers of the package. In high speed systems, long lead frames are not suitable because of the large inductance of the leads. The leadless package improves system reliability by reducing the failure rate due to mechanical features of bending leads and replacement damage. The package has 17 connection terminals per side on .05" centers. The IC chip mounts to a ceramic base measuring .95 inches on a side. Gold plated metal on the base piece routes signals and power from the package edge to the IC chip. The Macrocell Array chip is die attached to the package using a preform which provides an excellent thermal interface between the die and the ceramic. The thermal resistance of the device from the junction to the case is less than 5°C/watt. Figure 10 shows the chip wire bonded to the package. A ceramic cover fits on top of package to provide a hermetic seal.

The package is mounted upside down from conventional IC practice with the base of the chip on the top side away from the PC board. A heat sink (such as the

Wakefield #4493) is attached (by the customer) to the package on the same ceramic piece as the IC chip for very efficient heat transfer. Figure 14 shows the heat sink attached to the package being mounted in a connector manufactured by AMP. This connector can be soldered to the PC board or held in place with a mounting bolt. The leadless package is held in the connector with a spring clip. There are 68 package pins in order to facilitate testing and trouble shooting. The input pin capacitance of the package going to the input on the chip has been measured to be around 2.5pf.

Another method of mounting the leadless package to the PC board is shown in Figure 15. The method consists of mounting stand-off pins or metal clips, manufactured by Berg Electronics, to the package. The metal clips come in strips that are connected to the leadless package by wave soldering. The package can now be connected to the PC board by also using reflow soldering techniques.

The thermal resistance from junction to ambient is $15^{o}C/W$ with heat sink attached to the package and 1000 lfpm of air flow. If the air flow is reduced to 500 lfpm, θ_{JA} increases to $19^{o}C$/watt. Without a heat sink and 1000 lfpm of air flow the θ_{JA} is $20^{o}C$/watt.

LIST OF FIGURES

1. Cross Section of MOSAIC I Process
2. MECL Macrocell Array Metal Interconnect Channels
3. Macrocell Array Features
4. Half Cell Schematic
5. Schematic of 4 Input Exclusive OR Gate
6. Interface Cell Schematic
7. Schematic of Interface Macro, I13 Latch
8. Output Cell Schematic
9. Schematic of Output Cell, 016 Translator
10. Macrocell Array Mounted in 68 Lead Chip Carrier
11. Worse Case Noise Margins
12. Macrocell Array Option Development Flow
13. 68 Pin Leadless Package
14. Leadless Package with Connector
15. Leadless Package with Stand-Off Pins
16. 8 Bit Binary/BCD ALU
17. 16 X 4 Multi-Port Register File
18. 8 X 8 Array Multiplier
19. 8 X 8 Multiplier Logic Drawing
20. Layout Worksheet
21. Power Calculations for 8 X 8 Multiplier
22. 8 X 8 Multiplier Channel Interconnect

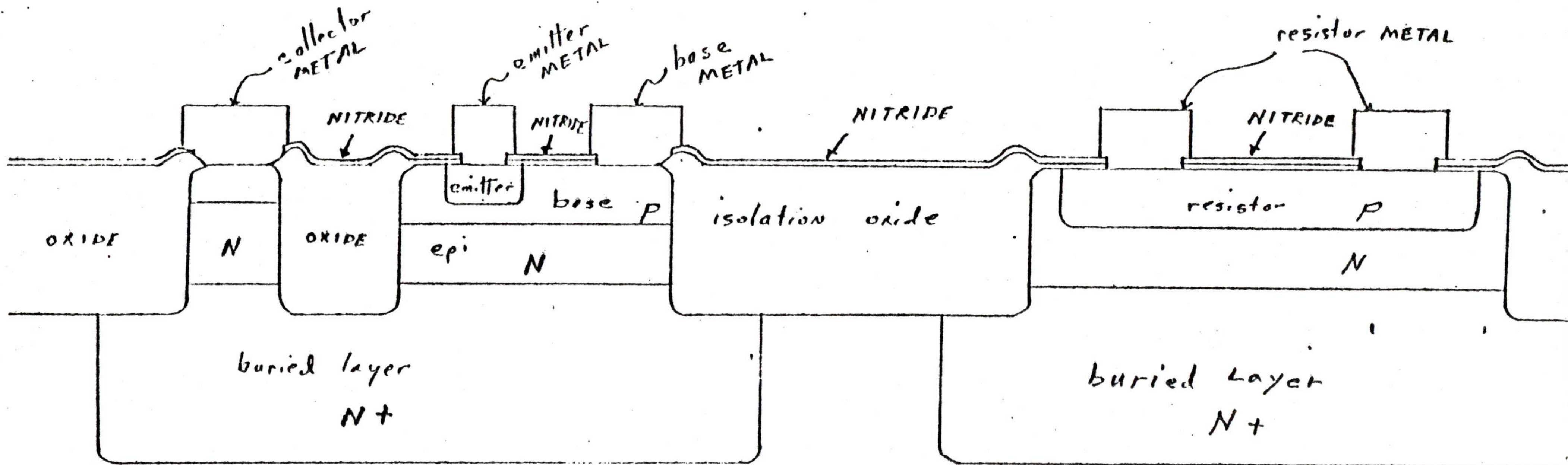
Figure 1. CROSS SECTION OF MOSAIC ? PROCESS

Emitter
$\rho_s = 12 \Omega/\square$
$x_j = 4000$ Å

Base
$\rho_s = 500 \Omega/\square$
$x_j = 6000$ Å

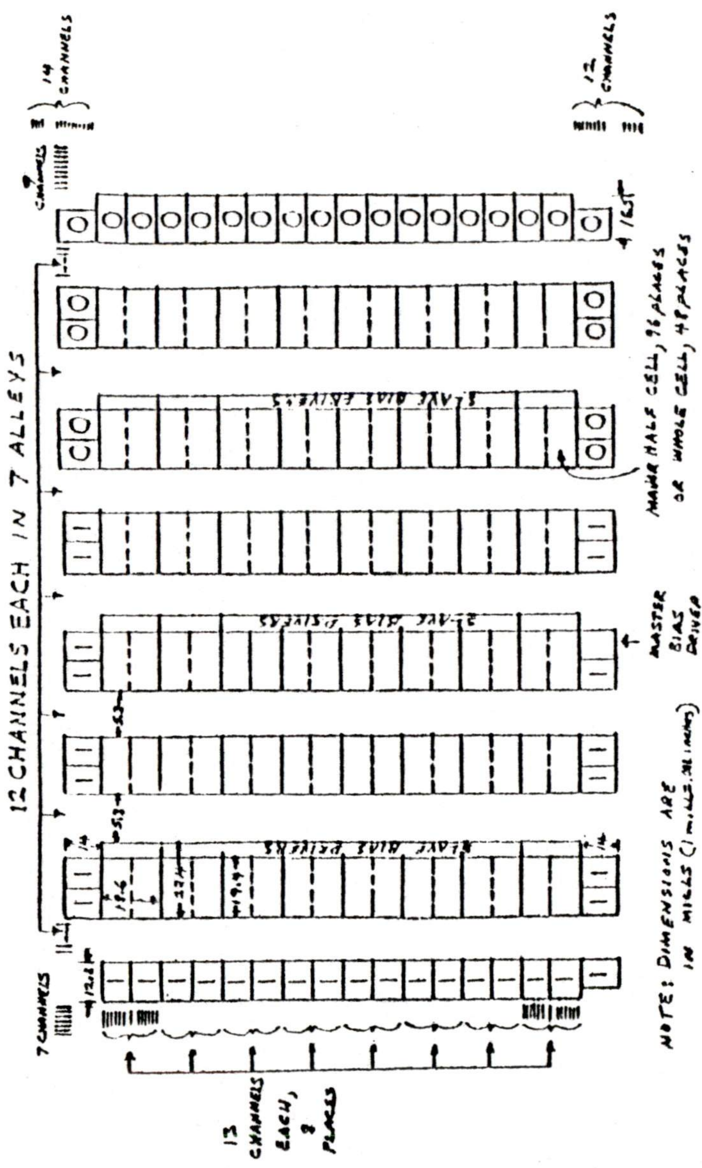
Resistor
$\rho_s = 100, 500$ (base), high value
$x_j = 5000 - 7000$ Å

Buried layer
$\rho_s = 25 \Omega/\square$
$x_j = 4-6$ µm



NOTE: MOSAIC IS THE APPREVIATION OF "MOTOROLA OXIDE SELF-ALIGNED IMPLANTED CIRCUIT".

FIGURE 2. MECL MACROCELL ARRAY – METAL INTERCONNECT CHANNELS



1. 106 total cells - 48 major, 32 interface, and 26 output cells.
2. Up to 1192 equivalent gates if Full adders and latches are used in all the cells.
3. Up to 904 equivalent gates if flip-flops and latches are used in all the cells.
4. Die size - 221 X 249 mils.
5. Power Dissipation - 4 watts typical
6. 4.4 mw per equivalent gate (for 904 gates and 4 watts)
7. Interface cell delay - .9ns typ (1.3ns max)
8. Major cell delay - .9 to 1.3ns typ (1.3 to 1.8ns max)
9. Output cell delay - 1.5ns typ (2.2ns max)
10. Any output cell (up to a total of 8) can drive a 25 ohm load.
11. All output cells can drive 50 ohm loads.
12. Edge speed - 1.5ns typ 20 to 80% (1ns min)
13. 85 Macros in Cell Library - 54 macros for major cells, 14 macros for interface cells, 17 macros for output cells.
14. Ambient temperature range with heat sink and 1000 lfm air flow = 0 to 70°C.
15. $\theta JA = 15^{0}C/w$ with heatsink and 1000 lfm air flow
16. Absolute Maximum Junction temperature, $T_J = 165^{0}C$
17. Voltage compensated, $V_{EE} = -5.2$ volts ±10%
18. MECL 10K compatible

FIGURE 3 - Important Macrocell Array Features

FIGURE 4. HALF CELL SCHEMATIC (1/2 OF MAJOR CELL)

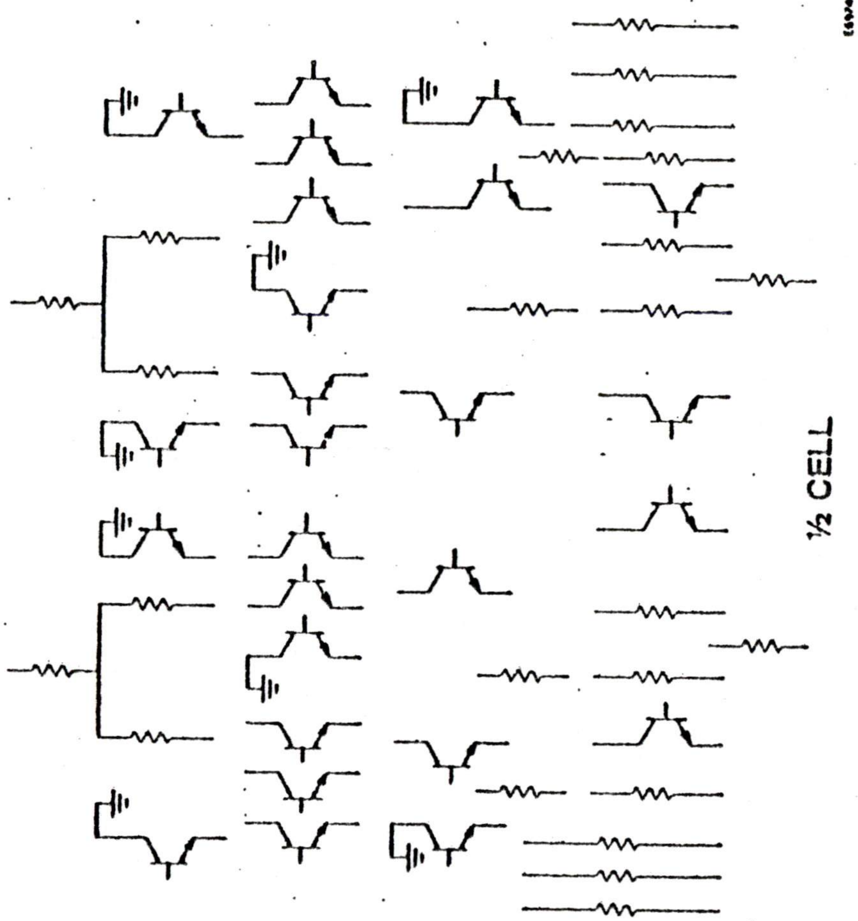
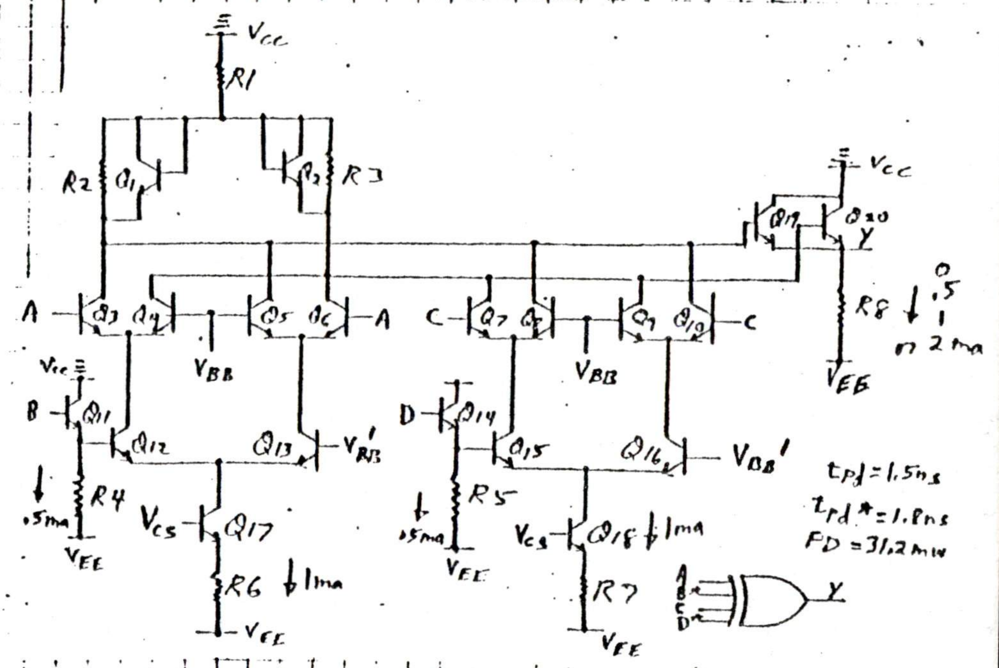


Figure 5. Schematic of 4 input Exclusive OR Gate (1/2 M11)



$$Y = A\bar{B}CD + \bar{A}BCD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}$$

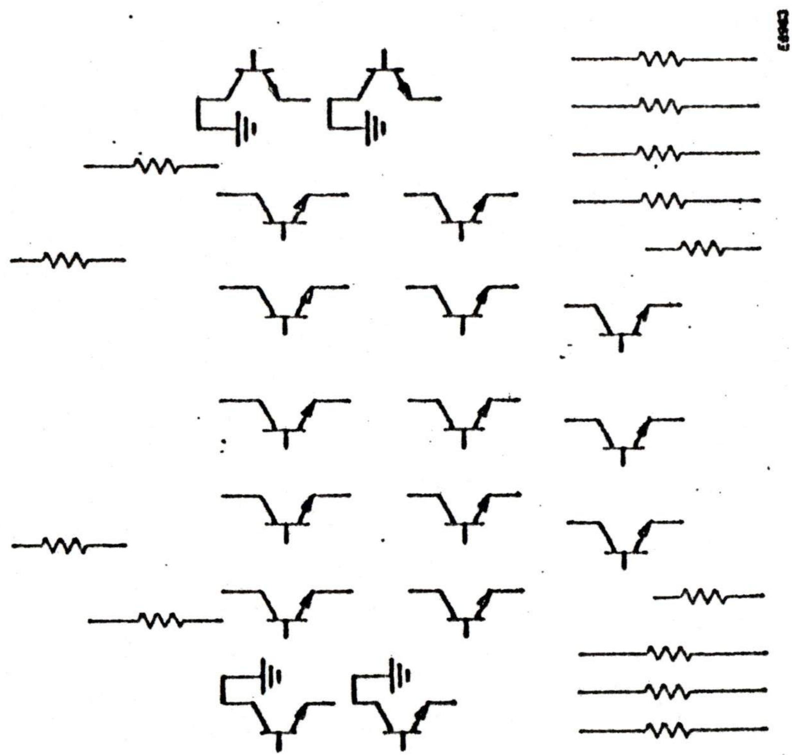
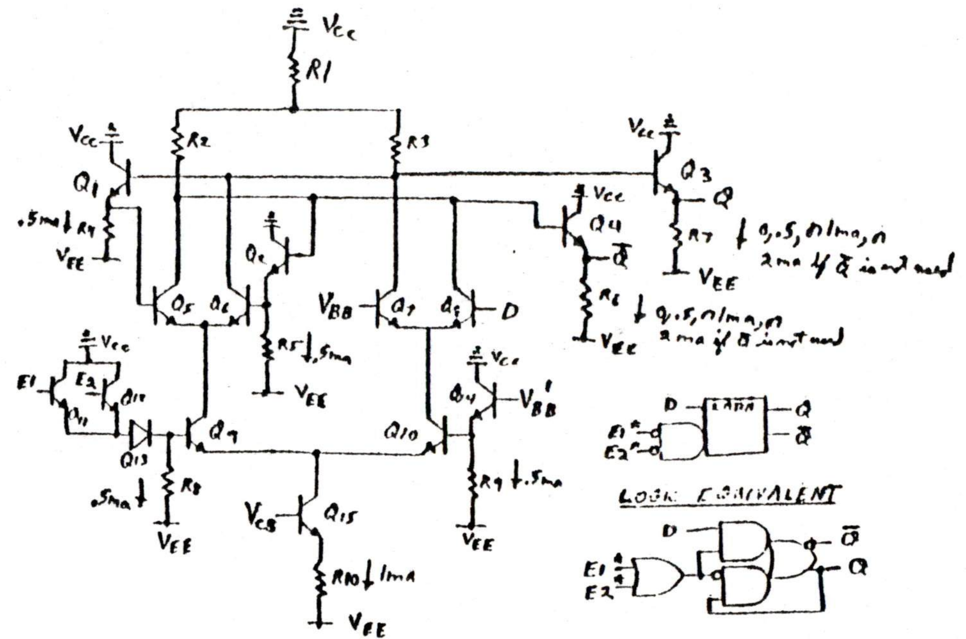


FIGURE 6. INTERFACE CELL SCHEMATIC

FIGURE 7, Schematic of Interface Macro, I 13 LATC



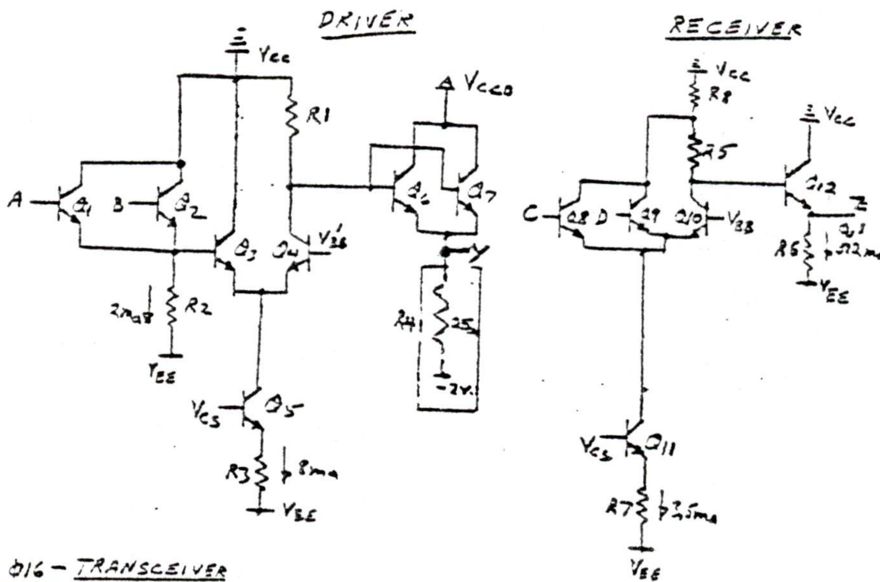
TRUTH TABLE

E1	E2	Q
L	L	D
X	H	—
H	X	—

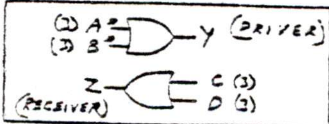
— = NO CHANGE
X = DON'T CARE
L = V_{OL} H = V_{OH}

$t_{pd} = 1.3 ns$
$t_{pd}^{*} = 1.6 ns$
PD = 15.6 mw

FIGURE 9. Schematic of Output Cell, O16 Transceiver



O16 – TRANSCEIVER



$Y = A + B \quad Z = C + D$

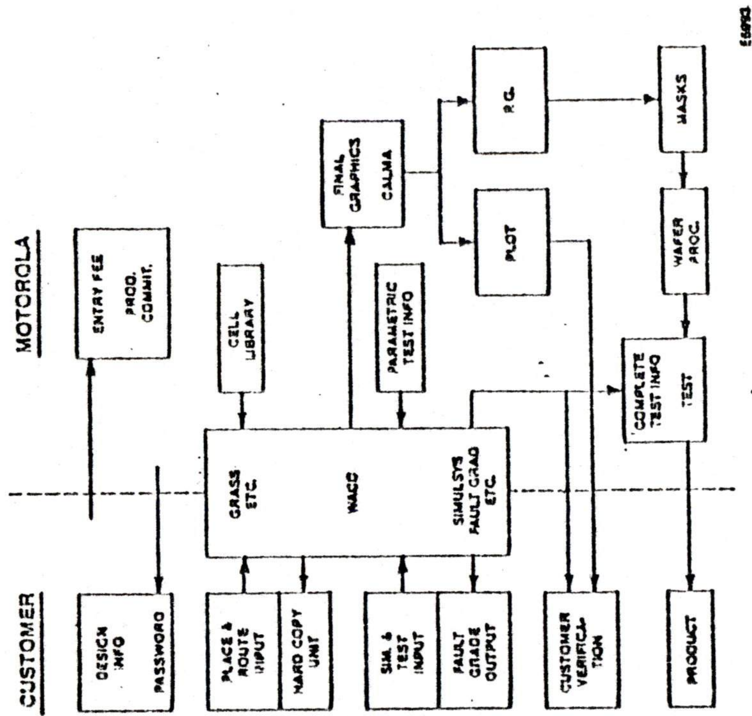
Y WILL DRIVE 25Ω OR 50Ω OUTPUT LOAD

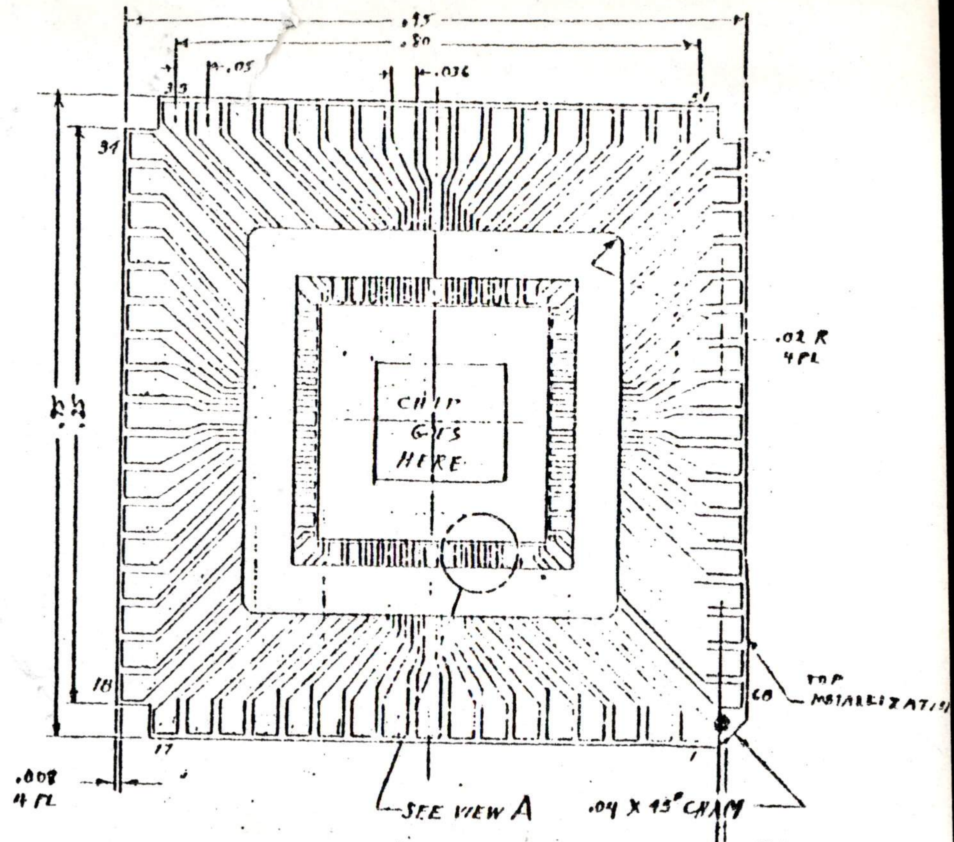
Z WILL DRIVE ONLY INTERNAL LOADS

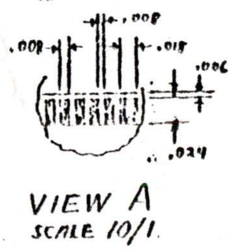
Tpd Y = 2.2ns   PD (Y) = 52 mw

Tpd Z = 1.5ns   PD (Z) = 18.2 mw

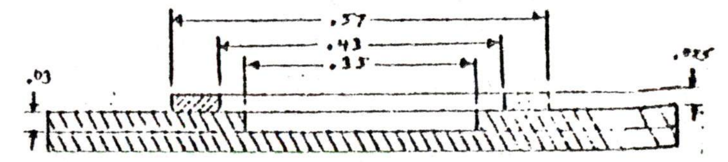
FIGURE 12. MACROCELL ARRAY OPTION DEVELOPMENT FLOW







VIEW A
SCALE 10/1



DIMENSIONS ARE IN INCHES

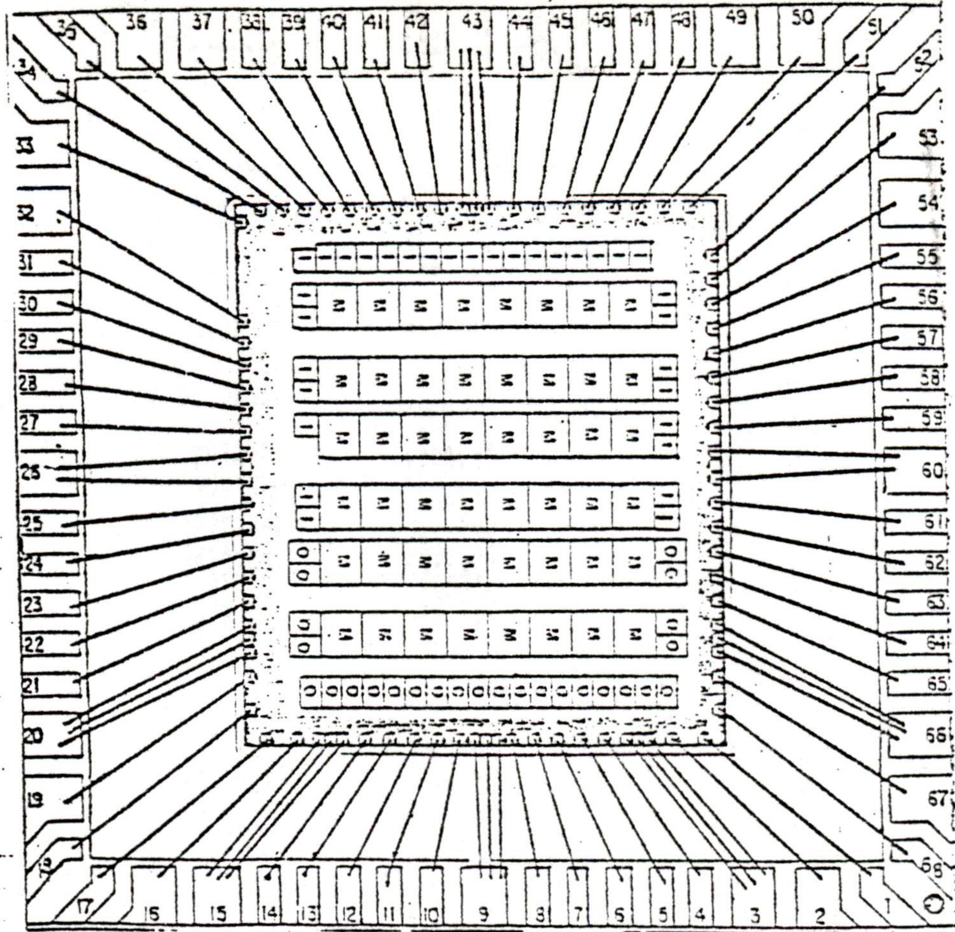


Figure 10. – Macrocell Array Mounted in 68 lead Chip Carrier

V_{CC} = PIN 26, PIN 60 V_{EE} = PIN 9, PIN 43

V_{CCO} = PIN 3, PIN 15, PIN 20, PIN 66

CONDITION		± 2% REGULATION $-5.304 \leq V_{EE} \leq -5.096V$	0 to +5% REGULATION $-5.46 \leq V_{EE} \leq -5.2V$	± 5% REGULATION $-5.46 \leq V_{EE} \leq -4.94V$
MECL 10K Driving MECL 10K	NM_H	96	109	70
	NM_L	108	111	46
MACROCELL ARRAY Driving MACROCELL ARRAY	NM_H	107	110	99
	NM_L	138	137	122
MECL 10K Driving MACROCELL ARRAY	NM_H	107	109	97
	NM_L	118	137	72
MACROCELL ARRAY Driving MECL 10K	NM_H	97	110	72
	NM_L	128	111	95

FIGURE 11. Worse case noise margins (in millivolts) for MECL 10K and the 10K MACROCELL ARRAY. For an ambient temperature differential of 10°C between packages. ($0°C \leq$ ambient temperature $\leq 85°C$)