dec INTEROFFICE MEMORANDUM

DATE: August 3, 1964

SUBJECT: PDP-5 Course Convening August 10, 1964

TO: K. Olsen
H. Anderson
S. Olsen
N. Mazzarese
R. Beckman
A. Hall
Receptionist Building 12
All Sales Personnel
District Offices

FROM: R. Bernier

The following individuals are scheduled to attend a one week PDP-5 Maintenance Course convening August 10, 1964.

1.	------	The Foxboro Company
2.	------	The Foxboro Company
3.	Dr. P. Coleman	University of Maryland
4.	P. Tittle	University of Maryland
5.	E. Cain	DEC, Maynard
6.	E. Steinberger	DEC, Maynard
7.	------	Carnegie Tech
8.	L. Taylor	Nortronics, Anaheim, Cal.
9.	D. Edwards	DEC, Maynard

mcs

H. Anderson

INTEROFFICE MEMORANDUM

DATE August 3, 1964

SUBJECT Programming for PDP-4/PDP-7

TO Computer Guidance Committee
D. Fellows
R. Belden
D. Cotton

FROM R. Wilson

All PDP-4 programs that now exist in the Program Library will be modified to be PDP-4/7 programs.

Method

a. All changes will be made so that the PDP-4 and PDP-7 will remain program compatible. The phasing is basically:

1. PDP-4 (FIO-DEC, Baudot)

2. PDP-4/7 (FIO-DEC, Baudot, with ASCII)

3. PDP-7/4 (ASCII with FIO-DEC, Baudot)

4. ~~PDP-7 (ASCII or Mecca)~~

b. The type 32 (28) and type 33 teletypes will use the same IOT numbers, however when the Type 33 is installed an IO Skip instruction will be wired in. The IOT instruction for it will be 703301_8. (Which is essentially a skip on flag instruction.)

c. All programs will be re-written with the I/O skip testing for the model 33 and a dispatch to a 32 (28) or 33 subroutine to make th two devices appear equal.

d. All new programs generated will be for the Type 33 teletype using the ASCII code.

e. Programs that accept tape as an input will be modified to accept both FIO-DEC and ASCII codes. There are basically three ways this might be implemented.

   1. Sensing a switch position on the console. However knowing a programmer's aversion to setting switches the two additional methods are also suggested.

2. Systems assembler written with parameters which can be redefined so that a programmer might select which code he will use at his installation or change to accept type of tape from the console switches.

3. The assumption can be made that all Baudot Codes will use FIO-DEC as the input medium, and all ASCII codes will use ASCII as the input medium. (The three methods above all require approximately the same time.)

f. All in-house PDP-4's should be wired now to accept both 32 (28) and (33) teletypes by a manual switch so that programming can go at maximum possible smoothness and speed.

g. Dave Fellows will start modifications to the existing PDP-4 Library on August 15, 1964. Rod Belden and Dave Cotton will assist as required.

The time estimation for this change will be approximately one week. This definitely will allow the programs to be delivered with the first computer. This method of change over will allow the maintenance of one (1) library during a possible phasing out of the PDP-4. If this ever comes to pass, a further change can take place and the subroutines can be removed for the Type 32 (28).

RW/ll

INTEROFFICE MEMORANDUM

DATE August 3, 1964

SUBJECT

TO Harlan Anderson
Win Hindle
Dick Best

FROM Kenneth H. Olsen

Our engineering programs in the immediate future are fairly well laid out and we are all enthusiastic about them but I think it's time now for us to look at those areas which we want to be strong in a year from now. The one area which I think is going to pay off well in that time will be automated design. We have given Chuck Stein some freedom in this area but I don't think that it will be enough to make it a key product for us. I think he will do a good job in designing logic and circuits and will sell several computers as a result but we should consider a program to do this more extensively.

One time we thought of hiring Dr. Larry Roberts from Lincoln Laboratory but he was not interested. Now that we have a PDP-6 with the possibility of a large amount of memory, we might be able to offer him an interesting opportunity to do automated design with a decent size computer.

Ken Olsen

KHO:ech

INTEROFFICE MEMORANDUM

DATE August 4, 1964

SUBJECT PDP-6 Prospect, NASA Huntsville

TO Harlan Anderson
Nick Mazzarese
Gordon Bell

FROM Ted Johnson

An RFQ will be released within the next few weeks for what might be called the DAMU System (Display and Monitor Unit).

Officially, the system will not be a computer system. It will have multiple-display capabilities, with keyboards. Graphic as well as language material will be displayed. It will have to handle 6 independent streams of 72KC telemetry data. The serial streams will be converted to 10 bit parallel samples before entry by external hardware.

General requirements will indicate at least 24 bit word, at least 32K core, 2 u/sec. memory. Assembly and compiling will be done on the computer.

The present 110A system cannot handle their load. The 110 will be run in parallel, handling non-critical data.

The requirements possibly call for 4 complete systems with 2 back-up computers. The most stringent boiler plate requirement will have to do with RFI.

The system will probably call for 6 tapes and a High Speed Printer.

The SDS DEE's (Digital Event Evaluators - 910s, 920s) are used only for information processing, with absolutely no control responsibility. They are, according to my source, liable to be excluded from this system bid because of the "commercial" nature of their equipment. I do not know if this is a result of performance or what is meant by commercial.

The ability of one producer to provide both displays and computer systems will be very important.

The delivery of the first system will be March or April of 1965.

We need to get on the bidders list and then make personal calls to establish our identity in Huntsville.

INTEROFFICE MEMORANDUM

DATE August 4, 1964

SUBJECT Delivery of Basic PDP-6 Central Processor to Checkout

TO E. Harwood
R. Beckman

FROM J. Smith

cc: H. Anderson
G. Bell

PDP-6-6	9/7/64
PDP-6-7	9/28/64
PDP-6-8	10/12/64
PDP-6-9	10/19/64
PDP-6-10	10/26/64
PDP-6-11	11/9/64
PDP-6-12	11/16/64
PDP-6-13	11/23/64
PDP-6-14	12/7/64
PDP-6-15	12/14/64
PDP-6-16	12/21/64

INTEROFFICE MEMORANDUM

DATE August 5, 1964

SUBJECT PDP-4/7 Software

TO
H Anderson
J Fadiman
T Johnson
L Hantman
H Morse
G Bell
R Beckman
J Shields

FROM R Wilson

All PDP-4 programs that now exist in the Program Library will be modified to PDP-4/7 programs.

Since it is not intended or desirable to offer the KSR32 Teletype with the PDP-7, all references will be made to the KSR28 or KSR33 Teletypes.

The KSR 33 Teletype using ASCII code will be the standard console typewriter delivered with the PDP-7 computer.

The KSR33 Teletype on the PDP-7 will use the same IOT instructions as the KSR28 Teletype on the PDP-4. However when the Type 33 is installed an IO Skip instruction will be wired in, which will be essentially a flag so that programs can test for the presence of the Type 33. The IOT instruction to test for the presence of a Type 33 is 703301_8 (tts - Teletype Test Skip).

All programs will be rewritten with the tts testing for the Model 33 and a dispatch to a 28 or 33 subroutine to make the two devices appear equal. Programs that accept tape as an input will be modified to accept both FIO-DEC or ASCII codes descending upon the condition of bit X of the Accumulator Switches. If accumulator switch bit X = Ø (down) the input tape is FIO-DEC. If the switch X=1 (up) the input tape is ASCII.

All in house PDP-4's will be modified so that either the 28 or 33 can be used. A manual switch will be provided for selection. Modifications will be made by Field Service.

With the two exceptions listed below this changeover will allow the maintenance of one library and complete program compatibility of both machines.

A. DDT - will exist in two versions -

1. As presently used
2. A modified version for ASCII

B. FORTRAN II - For 4K and 8K -

1. The 4K version of FORTRAN II will operate with only FIO-DEC

2. The 8K version of FORTRAN II will be compatible with FIO-DEC or ASCII.

RS:ASJ

INTEROFFICE MEMORANDUM

DATE August 5, 1964

SUBJECT Manufacturing Cost - PDP-6 Central Processor Construction

TO K. Olsen
H. Anderson ←
G. Bell

FROM J. Smith

cc: D. Packer

Labor Costs

	Hours
Mechanical Assembly of Panels	28 3/4
Gnd Loop Prep 1 and 2	12 3/4
Gnd Loop Wiring 1 and 2	37
1B-1C Logic	30
Buss Wire Prep	13 1/2
1D-1E-1F Logic	35 1/2
1H-1J-1K Logic	42 1/2
1L-1M-1N Logic	32 1/2
1 Bay Vert. Interwiring	87
1 Bay Cable Prep and Wiring	23
1 Bay Components	19 1/2
1 Bay Checkout	77 1/2
2B-2C Logic	28 3/4
2D-2E-2F Logic	39
2H-2J-2K Logic	20
2L-2M-2N Logic	37 1/4
2 Bay Vert. Interwiring	67 1/4
2 Bay Cable Prep and Wiring	62 1/4
2 Bay Components	20 1/2
2 Bay Checkout	55 1/4
1 Bay to 2 Bay Interwiring	48 1/2
1 Bay to 2 Bay Checking	17
Harness	7
2 Bay to 1 Bay Interwiring	39 1/2
2 Bay to 1 Bay Checking	19 3/4
Solder and Clean-up and Inspec.	31 1/2
Total Wiring Labor, Bay 1 and 2	933 Hours
Power Wiring and Final Construction	176 Hours

Please ask Jack to mark his copies

CONFIDENTIAL

Cabinet Assembly	20 Hours	
Quality Control Inspection	10 Hours	
Total Hours	1,139 Hours	

Total Direct Labor and Overhead 1,139 @ $6.50 — $ 7,403.50

<u>Material Costs</u>

Cabinets and Associated Trim	$1,010.00	
Control and Indicator Panels	1,371.00	
Main Frame Harness	250.00	
Mounting Panel Hardware	800.00	
Total		$ 3,431.00
Modules and Power Supplies		$19,214.00
Total Manufacturing Cost		$30,048.00

H. Anderson

INTEROFFICE MEMORANDUM

DATE August 7, 1964

SUBJECT Educational Discounts

TO Computer Guidance Committee FROM Nick Mazzarese

The following individuals have been given educational discounts of 20% for LINC Computers. The source of funding is NIH and the laboratories will have ownership of the equipment.

Dr. Koella - Worcester Foundation for Experimental Biology

Prof. George Gerstein - University of Pennsylvania
Dept. of Bio-physics

INTEROFFICE MEMORANDUM

DATE August 10, 1964

SUBJECT

TO Win Hindle
cc: Harlan Anderson

FROM Kenneth H. Olsen

At times we have had propositions from organizations to help us train our middle management. I think we should review these possibilities because I think that, as our organization is becoming more structured, it is becoming more and more important that our people understand what a manager is and what his responsibilities are. We have a number of managers who have certain general ideas of what it means to manage but have very definite gaps in their knowledge. I think some of those with the biggest gaps are those who have worked with me for many years or who have come from MIT where there's little appreciation for management.

If we're going to send Jon Fadiman to Europe in the immediate future, we should consider taking the time now to send him to some school where he would learn some of the skills and responsibilities of managing.

Ken Olsen

KHO:ech

HEA

INTEROFFICE MEMORANDUM

DATE August 10, 1964

SUBJECT ITT (Autodin)Discount Decision

TO Harlan Anderson
Kenneth Olsen
Gordon Bell

FROM Dave Packer

The final decision regarding discounts for the ITT (Autodin) proposal was made August 6, 1964 at a meeting attended by:

Harlan Anderson, Gordon Bell, Jim McKalip, Dick Best and Dave Packer.

This memo summarizes the decision process.

Background

DEC's initial proposal to ITT for the Autodin bid quoted a price of about $1,600,000 per duplex PDP-6 system. This price involved maximum discounts of 32-34% on processors and memories and discounts of 10 to 34% on other equipment.

Recently, ITT informed us that they believed their bid on the Autodin contract was higher than that of RCA for all sizes of systems and IBM for the smaller systems. ITT felt that to stand a good chance of being low bidder, their price should be reduced about $200,000 per duplex system. They requested that we evaluate whether our prices could be reduced, so that they could reduce their bid price.

Decision

Our decision was to reduce the price of a duplex system by about $58,600. The reduction was achieved by raising discounts on processors and memories to 35-40%. The result of the $58,600 reduction to a duplex system price of $1,600,000 is approximately 3.7%.

Procedure

The first step was to estimate manufacturing costs for each major system component. The Appendix gives the detailed estimates used for processors, memories, drums, and tapes.

The second step is depicted by Exhibit 1 below, which shows manufacturing cost, list price, price with the discounts previously offered (highest discount used), and cost of sales percentage for each component. It then gives the number of components per duplex system and the extended system price.

EXHIBIT 1

INITIAL DISCOUNT OFFER

(thousands of dollars)

Component	Mfg. Cost	List Price	Discounted Price	Cost of Sales %	Components/ System	System Price
Processor	38.3	161.1	106.4	36.0%	2	212.8
Memory	28.2	129.1	85.3	33.0%	5	426.5
Drum	36.5	81.0	71.7	51.0%	3	215.1
Tape	11.5	30.4	23.1	50.0%	13	300.3
Fast Memory	12.0	30.0	19.8	60.5%	2	39.6
					Total	1,194.3

Examination of Exhibit 1 data showed that only processors and memories had sufficiently low cost of sales percentages; i.e., high markups, to be considered for price reductions. On the other items, with markups already less than 2, it was decided to hold to previously quoted prices and discounts.

The next step was to try to cut $100,000 from each duplex system price by:

Reducing processor price $20,000 ($40,000/system)
and Reducing memory price $12,000 ($60,000/system).

Exhibit 2 shows the outcome of these reductions and calculates the discount percentage necessary to achieve the $100,000 cut.

EXHIBIT 2

$100,000 REDUCTION

(thousands of dollars)

Component	Mfg. Cost	List Price	New Discounted Price	Cost of Sales %	Discounted %
Processor	38.3	161.1	86.4	44.4%	46.5%
Memory	28.2	129.1	73.3	38.5%	43.2%

This alternative was rejected because it led to unacceptably high discount and cost of goods sold percentages.

The third step was to try a 40% discount, thought to be the maximum we should offer, on processors and memories. Exhibit 3 shows the effects of this decision.

EXHIBIT 3

40% DISCOUNT

(thousands of dollars)

Component	Mfg. Cost	List Price	New Discounted Price	Cost of Sales %	Components/ System	System Price
Processor	38.3	161.1	96.6	39.6%	2	193.2
Memory	28.2	129.1	77.5	36.4%	5	387.5

Exhibit 4 gives the total system price reduction achieved with the 40% discounts above. The reduction is $58,600.

EXHIBIT 4

SYSTEM PRICE REDUCTION

(thousands of dollars)

Original System Prices:	Processor	212.8	
	Memory	426.5	
	Total		639.3
40% Discount System Prices:	Processor	193.2	
	Memory	387.5	
	Total		580.7
Price Reduction			58.6

It was agreed to offer the 40% discount level on processors and memories.

Exhibit 5 shows the cost of goods sold percentage and markup for the entire system with the 40% discount on processors and memories.

EXHIBIT 5

40% DISCOUNT ON PROCESSORS AND MEMORIES

(thousands of dollars)

Component	Mfg. Cost	Components/ System	Mfg. Cost/ System	System Price
Processor	38.3	2	96.6	193.2
Memory	28.2	5	141.0	387.5
Drum	36.5	3	109.5	215.1
Tape	11.5	13	149.5	300.3
Fast Memory	12.0	2	12.0	39.6
		Totals	508.6	1,135.7

Cost of Goods Sold % $= \frac{508.6}{1,135.7} \times 100 = 44.7\%$

Markup = 1/44.7 = 2.24

It is believed that the 2.24 markup is adequate considering the size of the order. We should note the markup for the entire ITT order should be higher than 2.24 because each duplex system requires about $400,000 of modules not included in the above analysis.

D. Packer

DWP:ncs

APPENDIX

MANUFACTURING COST ESTIMATES

Arithmetic Processor

Total 36.8 (See Jack Smith's memo dated 5 August, 64).

Memory (Revised 8/6/64 by J. McKalip)

Stack	13.2
Mod.	8.2
Mem Sel.	.155
Mem Cont. & Pwr.	3.3
Power	.8
2 Cabinets	.5
10 Wired Panel	1.5
Checkout	.5
Cable	.240
Total	28.2K

Drum/Drum Sw

Physical Drum	30.0
Electronics (4 mounting panels)	3.6
8 Cables	.480
1 Cabinet	.500
Hardware	.400
Power	.500
Checkout	1.000
Total	36.5

Tape

Transport	8.312
Labor	.645
Catalog Items	2.284
Miscellaneous	.175
Total	11.462

INTEROFFICE MEMORANDUM

DATE August 10, 1964

SUBJECT Wall Charts, etc.

TO J. Atwood

FROM Gordon Bell

cc: S. Grover
N. Mazzarese
H. Anderson

The powers of 2 wall chart turned out to be quite an interesting idea in that junk collectors, etc who like to hang interesting-useful stuff on their walls want them, and this puts the name of DEC before the computer user-buying public (hopefully).

Let us extend the series to include:

1. Code conversion tables - ASCII, IBM, etc.

2. Interesting numbers and their octal and decimal equivalences eg II, e, etc.

3. A page of random numbers

4. Flow chart symbols (courtesy of ASA)

5. Fortran statement table usage

6. Algol statement table usage

7. Cobol statement table usage

8. PDP-6 op. code layout

9. Engineering numbers (possibly included in 2).

DIGITAL MAYN

RECEIVED
1964 AUG 11 AM 8:07
DIGITAL EQUIPMENT CORP.
SALES DEPARTMENT

DIGITAL EQPA

TO HARLAN ANDERSON ....FROM KEN LARSEN

MARVIN MINSKY TOLD NORMAN HARDY THAT PROJECT MAC WAS ORDERING A

GE 635 COMPUTER. NORM HARDY TALKED TO MINSKY ON FRIDAY 8/7/64

END.......

dec INTEROFFICE MEMORANDUM

Hold for Works Comm. Aug 18

DATE August 11, 1964

SUBJECT Manufacturing of DEC Compatible Cera-Circuits

TO Works Committee FROM J. Smith

Purpose:

The purpose of manufacturing a DEC package compatible to cera-circuits is outlined below.

1. To enable better control over the availability of cera-circuits presently being supplied by Sprague. In the past, there has been a great deal of difficulty in the procurement of these circuits.

2. To gain experience in the production problems that arise in this type of manufacturing construction. The experience gained should prove invaluable when we move into the area of Micro-Circuit construction. It is hoped that cera-circuit construction will serve as a stepping stone to our ultimate goal of micro-circuit construction.

3. A reduced module manufacturing cost, via savings in material, and direct labor should be realized with the use of micro-circuits over our present method. Preliminary figures denote a substantial impact on direct labor costs.

Attached you will find specifications of the chips we intend to manufacture.

Manufacturing Process:

Manufacturing process of cera-circuits involves the accomplishment of the below listed tasks:

1. Screen and fire conductor number 1

2. Screen and fire the glass dialectric

3. Screen and fire conductor number 2

4. Screen and fire the resistors

5. Trim resistors

6. Insert and bonding pins

7. Potting

Steps 1 through 3 are accomplished with similar equipment and operations. The only variables being time and temperatures of the various operations. It is, therefore, conceivable that all three steps could be accomplished on one conveyor system. All succeeding steps require specialized equipment that is unique to the particular operation.

Proposal:

At the present time all firing operations are in a constant state of flux, with the introduction of new materials and methods on almost a daily basis. It is for this reason, I do not feel it would be practical to forge ahead on a continuous highly automated system at this time. I suggest we start with a one screen, conveyor and oven arrangement. As the various operational techniques settle down and yield demand increases, we can add additional conveyor sections to increase the yield. Special handling of the chips is not required after each firing, and they could drop in a tray-type arrangement for storage. We would also be gaining valuable experience at a minimum capital outlay.

Yield:

Yield from the proposed single conveyor system would, of course, be at a minimum; but the yield realized on a single-shift basis would still be adequate to meet our present monthly usage of 10,000 cera-circuits currently being supplied by Sprague. All the equipment initially purchased would be useable in a more automated system with a larger yield.

Cost and Availability of Equipment:

Conveyor System - Construction would be accomplished by our in-house facilities in six weeks at a cost of	$ 500.00
Oven - Purchased item with a six to eight week delivery	$11,000.00
Resistor Trimmer - Construction would be accomplished in house in four weeks at a cost of	$ 5,000.00
Pin Inserter - Construction would be accomplished in house in six weeks at a cost of	$ 1,500.00
Potting Arrangement - It has not been determined whether to purchase or build this arrangement, an approximate cost of $500.00 is estimated	$ 500.00
Total Cost	$18,500.00

If construction should commence this week, we could be operational by October 1.

Personnel Requirements:

Mechanical Engineering:

Design of the specialized equipment required - One (1) man month

Machine Shop:

Construction of specialized equipment - Two (2) man weeks

Sheet Metal Shop:

Construction of specialized equipment - Four (4) man weeks

Drafting:

Presently all layouts are being accomplished by a technician working with Tom Stockebrand.

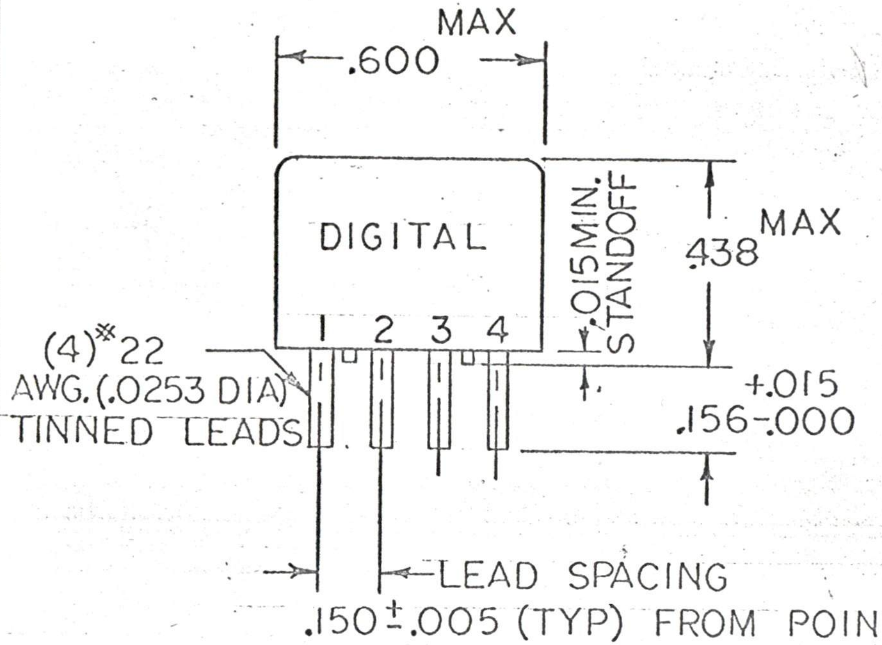
Operational Personnel:

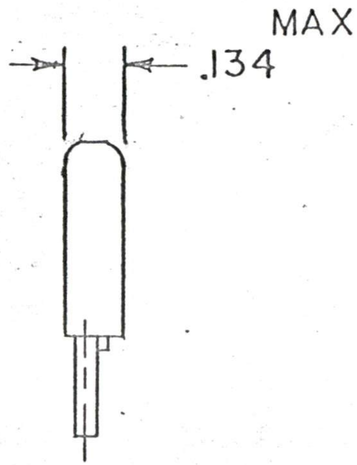
Two (2) girls

digital EQUIPMENT CORPORATION	PURCHASE SPECIFICATION

Number HY-0003	Rev
Date 4-17-64	
Revisions	
Change No.	
Eng	Eng
Drawn D.F.R.	QC
CHK: [illegible]	Purch

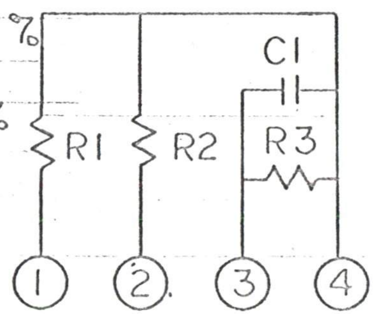
TITLE:





SCHEMATIC

C1 56MMF ± 10 %
R1 68K ± 5 %
R2 100K ± 5 %
R3 3K ± 5 %



APPROVED VENDOR:
SPRAGUE ELECTRIC
#SB01609-1-BR-56
C.T.S. Corp.,
Elkhart, Indiana

Unless other specified use:

Fractions	Decimals	Angles
± 1/64	± .005	±

Sheet 1 of 6	Scale 2 1/2 - 1
Number HY-0003	Rev

D.E.C. PART NO. 1719-

PH-2

2.1 Leads are number 22 AWG tinned copper wire.

2.2 Leads are spaced at multiples of .150 inches.

3.0 Resistor Characteristics:

3.1 Power Rating: The power rating of each resistor is as specified and is based on continuous operation up to 85° C.

3.2 Resistance: The resistance values shall be within the specified tolerances for each resistor. Measurements shall be made at 3 VDC and 25° C or else referred to measurements at that voltage and temperature.

Note: Resistor elements in series with other circuit elements may not be directly measurable. In such cases, impedance measurements may be necessary. Also some circuit configurations may include closed resistance loops which require extra calculations to determine individual resistant values.

3.3 Voltage Rating: The maximum voltage rating on any resistor shall be determined by the maximum power rating specified.

3.4 Short Time Overload: All resistors shall withstand for five (5) seconds a voltage equal to 2.5 times the rated continuous voltage without exhibiting a permanent change of more than ±1% of the resistance value.

3.5 Temperature Coefficient: The temperature coefficient of all resistors shall be within ±500 ppm/°C.

3.5.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

3.6 Humidity Resistance: After exposure for a period of 250 hours to an atmosphere of 95% relative humidity at a temperature of 65° C and one hour exposure of 40% maximum relative humidity at 25° C, the maximum resistance change shall be 1.0%.

3.6.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

3.7 Life Test: When these resistors are operated at rated wattage and 85 C for 1000 hours, the maximum change shall be less than ±2% for all resistance values.

3.7.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

3.8 Temperature Cycling: Resistors shall show no mechanical damage nor a change of resistance greater than ±1% when subject to 5 temperatures cycles from +25°C to -55°C to +85°C to +25°C.

3.8.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

4.0 Capacitor Characteristics:

4.1 Capacitance Measurement: The capacitance shall be within the specified tolerances when measured at a maximum of 5 VAC and 25°C with a standard frequency of measurement of 1 KC or else referred to measurements at that voltage, temperature and frequency.

4.2 Voltage Rating: The standard continuous DC voltage rating of the capacitor (s) are as specified for each capacitor for operation up to 85°C.

4.3 Dissipation Factor: Dissipation factor of the capacitor (s) shall not exceed 1.5% when measured under the conditions specified for measurement of capacitance in paragraph 4.1.

4.4 Insulation Resistance: The minimum value of insulation resistance at 25 C shall be 10,000 megohms. Measurement shall be made after a two minute charge at rated voltage.

4.5 Dielectric Testing: Capacitor (s) shall withstand without damage 250% of the DC rated voltage applied for not less than one second nor more than five seconds when charged by a current of not more than 20 ma.

4.5.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

4.6 Temperature Coeffecient: The maximum capacitance change shall be within ±4.7% between the temperature range of -55°C to +85°C.

4.7 Humidity Resistance: After exposure for a period of 250 hours to an atmosphere of 95% relative humidity at a temperature of 65 C and one hour exposure of 40% maximum relative humidity at 25 C the capacitor (s) shall have a minimum insulation resistance of 1000 megohms when measured as specified in the paragraph 4.4. The maximum dissipation factor shall be less than 1.5% when measured as specified in paragraph 4.3.

4.7.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

4.8 Life Test: When operated at 200% of rated VDC at 85 C for 1000 hours, the minimum insulation resistance shall be 1000 megohms, when measured as specified in paragraph 4.4. The dissipation factor shall be less than 2.0%, when measured as specified in paragraph 4.3.

4.8.1 No more than one (1) failure shall be permitted in twelve (12) units tested.

INTEROFFICE MEMORANDUM

DATE August 11, 1964

SUBJECT

TO
K. Olsen
H. Anderson
R. L. Best
G. Bell
J. Atwood
S. Grover
A. Stephens
R. Beckman
R. Tringale
A. Kotok
H. Morse
L. Hantman
J. Hastings

FROM Arthur Hall

On Monday, August 10th, DEC received a letter from the Foxboro Company requesting that DEC share $2500 in expenses incurred by Adams Associates in reworking some programs (done for Foxboro) which were incorrect because of omissions and errors in DEC programming notes.

As this falls under the heading of consequential damages we have no legal obligation to pay. Ethically the answer is moot. There was no intent to cause trouble or misrepresent the facts. Oversight or carelessness was the cause; nonetheless one of our good customers has been put to unnecessary expense and delay.

I can't help but think that this difficulty was at least partially preventable. The Type 18 Extended Arithmetic Element write-up caused part of the trouble, and the #24 Drum write-up caused the rest. Persons at DEC writing programs for these devices must have come up against the same troubles and found out what was wrong. Perhaps the Users Societies should receive pre-republication notes of manual mistakes discovered at DEC and elsewhere. (We obviously can't undertake to notify everyone in possession of a manual.)

Perhaps we should have in every publication a disclaimer to the effect; "While every effort has been made to insure the accuracy of this publication, DEC can not be responsible for inconvenience or expense caused by errors or oversights. Notification of errors or suggestions for improvements are welcome."

Whatever the solution we should give the matter some careful thought. It is quite conceivable that a firm could do months of programming in anticipation of the delivery of a computer and, if the literature be incorrect, have a good deal of the effort go down the drain. Under the circumstance, the legal niceties or not, they might be tempted to do something drastic like cancel the order or sue us (or both).

AHH/ll

H. Anderson

August 11, 1964

SUMMARY OF SOME RECENT SALES CALL REPORTS FROM GUENTER HUEWE

1. Speech Analysis Lab., Technical High School, Stockholm, report of 7/27/64. Definitely plan to order a PDP-5 for Speech Analysis work. Expect to settle details in September.

2. University of Stockholm, Physics Department, report of 7/28/64. Interested in HPD or PEPR system. Also interested in PDP-6 for on-line computation. Nothing definite.

3. Technical High School in Munich, report of 7/30/64. Interest in PDP-5 or possibly PDP-7 for on-line computations but nothing definite.

4. Julich Atomic Research Center in Julich Germany, report of 7/23/64. Not much interest because decided to order IBM 360 system.

5. AB Atom Energy in Stockholm, Sweden, report of 7/27/64. Interested in PDP-5 Pulse Height Analyzer, but nothing definite.

6. Statskontrole in Stockholm, report of 7/27/64. Contact with Mr. Svenonius who advises all universities in Sweden about computer equipment. Working hard here but at present Mr. Svenonius prejudiced toward IBM first, and CDC second. But nevertheless, interested in PDP-6.

7. Pharmacollege Institute for Medicine at University of Munich, report of 7/22/64. Interest in PDP-5 or PDP-8 for medical applications. No specific need at present, but perhaps at beginning of next year.

8. Computing Center for the Technical High School at Aachen, report of 7/22/64. Probably not much interest in PDP-6; require Algol.

dec INTEROFFICE MEMORANDUM

DATE August 12, 1964

SUBJECT Sales Newsletter

TO H. Anderson
S. Olsen
N. Mazzarese
B. Scudney
A. Stephens

FROM Ted. Johnson

I requested Martin Thomas to write up the results of discussion and thought about the Sales Newsletter.

Following our Monday sales staff meeting, the idea of editing and controlling the Newsletter was well received.

Whether or not a "Digital Newsletter" might emerge is of secondary importance right now.

I plan to trim the subscription list, using routings for non-sales departments. I'm sure I'll get a reaction from several sources.

Based on the outlined responsibilities on page 2, I intend to actively solicit "meaty" and timely entries by all people in sales, and will manage the editing job. Entries will still be sent to Alex Stephens as before.

PRELIMINARY PROPOSAL

Since its inception as a vehicle for detailed information for salesmen, the Sales Newsletter has been increasingly drawn into the role of a company wide bulletin. To restore the Sales function of the newsletter without abandoning the dissemination of general company news, it is proposed that three newsletters exist in the company with the following titles and functions.

THE ENGINEERING NEWS

The Engineering News will retain its present format. It will carry contributions of technical information and be circulated to people doing design and engineering work. Items of general interest carried in the Newsletter may be duplicated in the Digital Newsletter for a larger audience.

DIGITAL NEWSLETTER

The creation of the Digital Newsletter will fill the need for general company wide information on such topics as industry news, organizational and personnel information, and new products. This newsletter will be prepared by the advertising department and may be distributed in all areas of the company. Voluntary contributions from people in the company are of the greatest value in maintaining the timeliness and interest necessary for such a publication. Articles may appear in Digital Newsletter exclusively or may be borrowed from the special interest Engineering News or Sales Newsletter.

SALES NEWSLETTER

The Sales Newsletter will be rededicated to providing detailed information for people directly concerned with selling DEC products. This information originates in all departments of the company and should be channeled regularly to the Newsletter by the persons who originate the items. A preliminary list of items to be included in the Newsletter appears below along with the area of the company responsible for reporting such items. Informations related to these topics should be submitted as soon as possible to Alex Stephens, X391.

Responsibility	Topic
M	Sales policy and strategy (directives)
	Delivery and price information
	Promotion (space advertising, trade shows, publications, mailings)
M,E	New products, software, (status, technical description)
M,S	Current reviews of sales (kind of customer, location, product, application)
	Industry News -- government spending, contracts, etc. (marketting information)
M,S,E	Organizational information (personnel, responsibility, changes, new offices, etc.)
	Competition (review and comparisons)
	Sales arguments, approaches, "pitches" - Sales and Project leaders
S,E	Detailed applications where of direct help to salesmen (timely)

M = Management
S = Sales
E = Engineering

Ted Johnson will be in charge of preparing the new Sales Newsletter for distribution twice weekly as at present. Jim Hastings will assist in gathering items for the Newsletter from the meetings of company committees.

In relation to all three publications it should be stressed that the responsibility for making an item known lies with each individual concerned. It is far better to have an item reported twice than omitted because someone else should have reported it.

Martin V. Thomas

H Anderson

INTEROFFICE MEMORANDUM

DATE August 12, 1964

SUBJECT Jack Dennis' one day consulting visit regarding Multi-Programming, Multi-Processing, and BTL.

TO File

FROM Gordon Bell

cc: H.E. Anderson
A. Kotok
H. R. Morse
K. H. Olsen
R. L. Best
R. Lane
N. Mazzarese

We discussed segmentation including how various level procedures call others and pass the relocation information. The Burroughs D825 has a solution which solves some problems. Jack feels the new 360 line does not solve the problem, and the people designing the system do not understand that there is a problem. We need to think more about ways of naming subroutines, arrays, etc., in unique fashions. Solutions to some of our problems were discussed.

Protection and Relocation Page Scheme

Stop our present scheme for special customers and generalize the proposed MAC scheme by using main memory. Make a Relocation Table Base Register which is a Table Lookup Area of main memory which tells where an actual block is , if the block is in core, or is available. This register is set for each program to avoid referencing main memory for each page (a block) referenced, a 4 or 5 register associative memory would be used to hold the latest references. One of the 4 would be permanently reserved for the program, and the others would be used for data references. Kotok suggested a cyclic counter to point to the last register used and this would be advanced each time a new entry was needed in the memory, or something had to be re-written.

Inter-Processor Job Requests

Our scheme proposed to MAC seems good enough, except another set of registers should be used to specify communication in the opposite direction. Data would be placed in pre-determined cells. The meaning of the bits would be:

A to B request
A to B request acknowledge
B to A request
B to A request acknowledge

Schedule Operation for Multi-Processors

Requires processors to change and test memory in one instruction. We do have this instruction, and as such jobs can be picked from a common queue while informing the memory of the status change.

Duplex Switching of I/O

Generally attractive from reliability and asthetic considerations. Can be used to balance processor-I/O loadings and as such, must be dynamic. People may not want to pay the price ($) for switches. An AP for IO Processing can be sold though. (MAC is not getting two IO Controllers for example nor can GE yet duplex connect the I/O.)

One Microsecond Memory

Helps decrease processor times. Access time is almost as important as cycle time.

Method of Executing Instructions from Executive Mode in User's Areas

Very desirable for us now, as it is painful to fetch and store data in a user's program without testing it against parameters of a job.

BTL Real Time Channel

We should really cook up something great for them to show our feeling for their problems, lots of lights, a funny processor, patch panels, etc., and a special memory.

BTL People

Jack doesn't feel H. S. Mac Donald has much to do with the computer decision. The people are:

1. E. E. David (head man)
2. J. L. Kelly
3. Vassotsky
4. Doug Mc Elroy
5. Tom Crowley

J. L. Kelly was the only one present at our briefing.

General Status and Sales Attitude

BTL will be most interested in the above items. Although we are learning about the general problems our attitude should be somewhat bold in response to competition since no one has any real experience in the above. MAC is getting some solutions to the above problems from GE, through special design.

We must get:

GE-635	Programming Reference Manual	CPB-1004
GE 65	General Comprehensive Operating Manual	CPB-1002

We have finally made some points with Jack in regard to our design:

1. Regardless of the GE-Memory Based Interrupt System, the effect upon processors and programs in both systems is identical.

2. Regardless of the GE-Memory Based Interrupt System, the number of cables (a system design cleanliness criteria) is the same.

3. The trading of an IO Controller (GE) and associated programming for a general AP (DEC) to save a different kind of bus (IO Bus) is a marginal improvement. MAC must get a third kind of processor, one which does nothing more than pass drum data to and from memory, (the same problem and solution as DEC).

4. There can be cable and logic failures in both systems which can stop a processor and a memory temporarily. The GE system of radial signal distribution may be slightly better than our bus system, (assuming both are of good mechanical design).

5. Memory parity checking is important.

GB/mro

dec INTEROFFICE MEMORANDUM

DATE: August 13, 1964

SUBJECT: PDP-5 Maintenance Class

TO: H. Anderson
R. Beckman
K. Olsen
S. Olsen
All District Offices
All Sales Personnel

FROM: Ray Bernier

The following people will be attending the PDP-5 Maintenance Course convening August 17, 1964:

1. Mr. E. Chevrier - DEC
2. Mr. D. Edwards - DEC
3. Mr. P. Hammond - Woods Hole Oceanographic Institute
4. Mr. L. McGraw - Carnegie Technical Institute
5. Mr. R. Riley - DEC
6. Miss Ai Tsung Lu - DEC

MCS

dec INTEROFFICE MEMORANDUM

DATE August 13, 1964

SUBJECT Cost Accumulation Numbers for Computer System Manufacturing

TO Harlan Anderson
Stan Olsen
Nick Mazzarese
Bob Beckman
Frank Kalwell
Ed Harwood
Tom Whalen
Dick Best
Gordon Bell

cc: Data Processing Committee

FROM Data Processing Committee

Our present methods for using customer order numbers (EN 2000 series) has led to problems in cost collection. The central problem is that we now assign a specific computer to a specific customer at varying points in the manufacturing process. The Data Processing Committee has devised a job numbering system to be put into effect in the near future that should solve the problem. The system is described in this memo for your study to be sure that no loopholes exist. If you see any serious problems, please contact Win Hindle or Dave Packer.

There are three types of costs associated with computer system manufacturing:

1. Costs of manufacturing computer components.
2. Costs of manufacturing computer systems.
3. Costs resulting from activities necessary to fill computer orders for a specific customer.

The cost accumulation numbers for these three types of costs will be as follows:

1. Components (items currently having option numbers plus items such as the PDP-1 central processor that could have option numbers):

Charge labor and materials to:

M	0 6	1 6 6	1 5
	Product Line	Option #	Serial # of Option

and collect costs of manufacturing each option. The option number will be closed after the item has been checked out, when it is complete and ready for installation in a computer system.

2. Computer Systems: A computer system comes into existence whenever components are brought together. Sometimes this will be after an order has been received but often it occurs before an order comes, when we decide to build systems of the type we expect to be ordered. Systems will be assigned serial numbers, but the number of the system does not necessarily correspond to the serial numbers of any of the components. The system is a new entity with its own identification. It is built (by putting components together), checked out as a system, and shipped to a customer.

The components are requisitioned to the following number and all systems checkout is also charged to the same number:

M	0	6										2	1
	Product Line								System Serial #				

This is the hardware system number. This number is closed out at the moment the system is shipped from our plant to the customer and the costs are held until acceptance, then transferred to Cost of Goods Sold.

3. Specific Customer Order Activities: Often, if not always, we do things that are necessary only because of a specific order. We visit the customer's plant after the order is received, engineer and build special devices, apply special paint, etc.

The DEC Customer Order form and Construction Requisition form will be prepared so that the item numbers (for standard options and for non-standard units) are identical on both forms. In fact, we may want to combine these two forms in the future. The costs for each non-standard item will be collected under the following number:

C	0	6	I	T	M	0	4	0	7	7	4	2
	Product Line		Item # on DEC Customer Order Form					D.E.C. Order #				

Trips to the customer's plant or liaison work relating to the entire order would be charged to:

C	0	6	0	0	0	0	0	0	7	7	4	2

Installation of the system will still be listed as a separate item on the Customer Order form and the installation costs charged to that number. When the system is accepted by the customer, the customer number (or numbers) will be closed and the costs transferred to Cost of Goods Sold.

This system of cost accumulation clearly separates standard computer manufacturing costs from non-standard, customer-related costs. The scheduling of computers into production is not affected, nor is the assignment of specific machines to specific customers affected. In fact, this system allows considerable flexibility in shifting standard computers among customers, since the standard computer manufacturing costs are kept separate from specific customer costs. The number of cost accumulation numbers is reduced significantly which should result in easier and more accurate cost reporting.

Win Hindle

WRH:ech

INTEROFFICE MEMORANDUM

DATE August 13, 1964

SUBJECT Product Line Coordinators

TO

FROM

To promote continuity and control in each product line, the company has appointed a coordinator for each product line:

Product Line	Coordinator
PDP-1	Ed Harwood
PDP-4	Ed Harwood
PDP-5	Ed De Castro
PDP-6	Gordon Bell
PDP-7	Ron Wilson
LINC	Mort Ruderman
Memory Test Equipment	Pat Greene
Lab Modules	Burt Scudney
System Modules	Burt Scudney
Small Modules	Burt Scudney

General

These individuals must take an over-all view of the product line so as to co-ordinate all of the varied activities in the line. Their responsibility encompasses:

a. Coordinating planning for the product line.

b. Taking effective action toward both recognition and solution of problems in the product line.

No aspect of product line activity is too big or too small for the attention of the coordinator. Maintenance problems, sales difficulties, and potential new products should be brought to his attention. He must work through others to accomplish these tasks, since he will not have direct responsibility over those in other departments.

Product line planning should be done on an annual (fiscal year) basis. Plans should be evolved in conjunction with department managers. Summaries of detailed plans, giving forecast revenues and expenditures in each area of activity should be submitted to Works Committee for review and approval.

Coordinators must keep in close contact with product line efforts and results throughout the year to assure that actual performance corresponds with planned performance. Coordinators will receive monthly statements of product line sales and costs.

The Product Line Coordinator's Role

This section outlines specific functions of product line coordinators in several company activities. He must work with almost every department in carrying out his role as coordinator.

a. Engineering

Planning

1. Work with Engineering Department in laying out development plans:
   What improvements?
   What new projects?
   What manuals?

2. Coordinate schedules and assemble the costs for projects to be done during the year.

Control

1. Receive information about development projects; spot problems and take action.

2. Coordinate programming efforts; make sure programs and documentation are available.

3. Assure that manuals are consistent and adequate.

4. Evaluate special customer-request projects.

5. Recommend adoption of and discontinuance of projects.

b. Marketing

Planning

1. Work with Computer or Module Sales Manager in setting down basic marketing strategy:
   What kinds of customers?
   What kinds of markets?
   Sales approach?
   Sales training?

2. Help formulate and schedule advertising, mailings, etc.

3. Help develop sales forecast for the line.

Control

1. Keep current on sales activities.
2. Receive salesmen's critiques of products, software, etc., and take appropriate action.
3. Assure that the sales force is well-informed about product line developments.

c. Other Areas

Planning

1. Make annual product line plan.

Control

1. Assure that technical problems receive engineering attention.
2. Recommend schedule changes, when needed, and assure that all changes are properly coordinated among affected departments.

Supervision:

No organization changes are needed, as Product Line Coordinators will continue to work for their present supervisor. Harlan Anderson will assure that coordinators accomplish their task and will help when needed.

Product line performance is a major interest of the Works Committee which will review the over-all product line activities.

Project Support

All direct development expenditures must be supported by product lines or by the Works Committee (for projects in new areas that benefit no existing product line). Before an activity that benefits several product lines (such as development of a tape unit or a joint advertising campaign) is undertaken, its costs must be split along product lines. Should conditions change so that project support arrangements appear inequitable, they may be changed at the start of any fiscal quarter. Changes require approval of all product line coordinators involved. Coordinators are also free to withdraw support from efforts they believe will not benefit the product line.

Change in Plans

If new projects are proposed during the year, they may be added to a product line forecast with the approval of Computer or Module Guidance Committee (for small projects) or Works Committee (for large projects). Product line coordinators should take the initiative in promoting new activities they believe valuable. All major changes in product line plans should be taken before the appropriate committee for approval.

DP & WRH

INTEROFFICE MEMORANDUM

DATE August 14, 1964

SUBJECT PDP Production Rate

TO J. Smith FROM Ed Harwood

cc: K. Olsen
S. Olsen
H. Anderson
N. Mazzarese
D. Pinkney
R. Mangsen

The production rate to Checkout for the next 12 months will be:

PDP-1	None
PDP-4-33	August 17, 1964
PDP-4-34	September 1, 1964
PDP-5	Continue delivery four (4) per month through October, 1964.
PDP-6	One every 2½ weeks through January, 1965. Starting in February, 1965, deliver three (3) per month.

dec INTEROFFICE MEMORANDUM

DATE August 17, 1964

SUBJECT Proposed In-Plant Company-Sponsored Metal Fabricating Course

TO Works Committee

FROM L. Prentice
R. Richardson
R. Lassen

Up to now, our technical training efforts have been directed principally toward our electronic technicians. Our technical training classes combined with planned job progressions have been extremely effective in insuring that our most capable men continue to grow with the company. These efforts have not only prepared technicians for more complex job assignments, but have helped to motivate them to further their careers.

At the present time, our metal fabricating employees are trained on the job. To supplement this on the job training, we have for several months been attempting to locate qualified metal fabricating instructors to conduct an in-plant course in <u>shop math</u>, <u>blue print reading</u> and <u>practical metal fabricating functions</u> which would be tailored to our particular fabricating activities. After discussing this problem with representatives from Marlboro Vocational, Waltham Vocational and Lowell Trade, we have unanimously agreed that the Lowell Trade School faculty will provide an excellent course which will be adapted to our functions.

We, therefore, propose that the company sponsor such a course and submit the following information for your review:

<u>Principal Subjects</u>--Shop Math, Blue Print Reading and Metal Fabricating Functions related to DEC's fabricating activities.

<u>Length of Course</u>--20 weeks (2-hour classes held once a week)

<u>Time</u>--5:30 P.M. to 7:30 P.M. (one 10-minute break)

<u>Place</u>--DEC Plant.

<u>Attendance</u> (Voluntary) 30 people--preference will be given to employees in the Sheet Metal, Machine and Cabinet Assembly shops. A limited number of openings may be available for people in Drafting and Mechanical Inspection.

Since attendance is voluntary, the employee will not receive pay for attending the class.

Company Sponsored--Course will be taught by members of the faculty of Lowell Trade under the company's supervision. DEC will pay for the instructor's fees, text material and looseleaf notebooks. The company will also provide the classroom space.

Employee Progress--Examinations will be given and the employee's progress will be recorded. The employee will be advised of his progress and of his completion of the course as either "satisfactory" or "unsatisfactory." Attendance will be taken.

Cost to DEC:

Instructor's Fees	- $15 per class x 20	- $300.00
(Includes travel time)		
Text Material	- $2.38 x 30	- 71.40
Looseleaf notebooks	- $1.00 x 30	- 30.00
	Total Cost of Course	- $401.40

INTEROFFICE MEMORANDUM

DATE August 18, 1964

SUBJECT MIT Project on Computer-Generated Music

TO Ken Olsen
Harlan Anderson
Nick Mazzarese
Bob Lane

FROM Win Hindle

About a month ago Ercolino Ferretti visited DEC to propose a scheme whereby he could have a PDP-6 at MIT to use in his computer-generated music project. Ferretti is a musician who came to MIT ten years ago to learn engineering because he felt that something entirely new was needed in the composition of music. He wants to make it possible for a composer of the future to create any sound he wants using a computer, thereby freeing the composer from the restraints of today's instruments.

Mr. Ferretti has caught the keen interest of Prof. Klaus Liepmann, head of music at MIT. The two of them have worked out an idea for purchasing a PDP-6 (total configuration - $600K) with the Music Department paying one-third, the Institute paying one-third, and DEC giving one-third as a contribution. They have talked with Jerry Wiesner, now MIT's Dean of Science, and he indicated in a general way that MIT would help. The Music Department has no funds, so Liepmann would have to approach a foundation or private individual. Because the support could probably not be raised at once, they propose that the payments be spread over 5 years in 5 equal installments. Prof. Henry Zimmermann, Director of RLE, has agreed to furnish maintenance and space - probably the present TX-0 room.

Alan Kotok and I visited Ferretti and Liepmann several weeks ago and heard a Ferretti composition, which I found very appealing. It has taken forever to program the piece using the MIT Computation Center with its 24-hour turnaround, which is the reason that Ferretti wants his own machine. I explained that a part of DEC's interest in considering the proposal was to put a PDP-6 in the hands of students and faculty as we had done with PDP-1. Thus, Ferretti and his colleagues would use one shift only and the balance would be available for others. We left the conversation with the agreement that they would forward a written proposal to DEC so we could take some official action on a 33 1/3 educational discount.

I made a second visit on August 13 to talk with Prof. Zimmermann. He wants to help the project, as RLE has supported Ferretti on a "sub rosa" basis for ten years. He had just received a draft of the proposal that Liepmann and Ferretti prepared and noted that they had considered only purchase price and had forgotten to consider yearly operating expenses. He will talk with Jerry Wiesner and then work with Liepmann to get more practicality into the proposal before it is sent. The financing for this project is extremely shaky at this point.

WRH:ech

H. E. Anderson

INTEROFFICE MEMORANDUM

DATE August 19, 1964

SUBJECT Australian Liason at Perth

TO J. Fadimon
N. Mazzarese
H. E. Anderson
R. Frith
R. Beckman

FROM Gordon Bell

Please get Ron Smart's Programmer who will be at Perth to come immediately and stay until delivery of their machine. He will get into the system and be ready to teach, modify, etc., their software.

GB/mro

H. E. Anderson

dec INTEROFFICE MEMORANDUM

DATE August 20, 1964

SUBJECT S. Boillen

TO J. Fadiman
H. E. Anderson
N. Mazzarese

FROM G. Bell

Shelly Boillen of BBN has asked if we are interested in hiring him for a sales position in a foreign office.

Please bring up the subject somewhere, and I'll call Shelly.

GB/mro

INTEROFFICE MEMORANDUM

DATE August 20, 1964

SUBJECT Rand Corporation

TO H. Anderson

FROM T. Johnson

I notice from your call report that we are considering systems responsibility including the discs. We sent a TWX on August 18, in which we gave dollar figures for maintenance plans based on standard DEC equipment. I left the door open a bit but feel we should make a decision or talk this point over some more with Rand.

H. Anderson

dec INTEROFFICE MEMORANDUM

DATE August 20, 1964

SUBJECT Comparison of Drum and File Storage

TO Computer Guidance Committee

FROM Gordon Bell

ITEM	STORAGE HEIRARCHY CAPACITY	ACCESS/DATA RATE	APPROX. COST $22K-167 IOP $13K-236 CONT. } COMMON	PROBLEMS	PROS.	
DEC DRUM	2^4 WORDS/BLOCK 2^9 BLOCKS/TRACKS 2^7 TRACKS/DRUM 1 X 2^{20} WORDS 36 X 2^{20} BITS	4.2 US/WORD 34 US MAX	237 DRUM: DRUM 30KX ELECTRONICS(DEC) 5.5 CKO 3.0 SELL PRICE 75K	1. CUTS 2. DRUM DENSITY HIGH 3. NEW 4. HIGH COST/BIT	1. SIMPLEST WAY TO GET $1 X 10^6$ BITS. 2. VERY FAST	
BURROUGHS DISCFILE	2^7 WORDS/BLOCK 2^5 BLOCKS/TRACKS 2^1 SIDES/DISC 2^2 DISC/CABINET $2^{5.5}$ TRACKS/SIDE 1.5 X 2^{20} WORDS 59 X 2^{20} BITS	8 US/WORD 40 US/REVOL.	ADDIT. CONTROL 20KX ADDIT. ELEC. ADDIT. CKO DISC UNIT 31K	1. BURROUGHS 2. HIGH XFER RATE BUT REQUIRES TRICKY LOGIC 3. MUST BUY 29K COMPRESSOR, POWER SUPPLY 4. ONLY 5 IN FIELD 5. LONG DELIVERY 6. MAY NOT SELL TO DEC	1. VERY MODULAR 2. SUFFICIENT SWAP RATE TO NEGATE DRUM 3. GUARANTEE BY BURROUGHS	
FASTRAN	28 WORDS/BLOCK 2^6 BLOCK/TRACK 2^6 TRACK/POS. 2^6 POSIT/DRUM 2^1 DRUMS/UNIT 14 X 2^{20} WORDS 504 X 2^{20} BITS	40 US/WORD	UNIVAC CONTROL 35K UNIVAC DRUM 160K (OEM=140K)	1. CAN NOT MARK UP 2. NOT VERY FAST RATE	1. LOWEST $/1 BIT 2. R-R GUARANTEE	
DP DISCFILE	2^7 WORD/BLOCK 12 BLOCK/ TRACK PR 2^2 TRACK PR/POSIT. 2^6 POSIT/DISC 2^4 DISC/DISCFILE 6 X 2^{20} WORDS 216 X 2^{20} BITS	52 US/REVOL. 175 US AVG. ACCESS 7 BLOCKS @ 50 US/WORD 5 BLOCKS @ 80 US/WORD	DP DISCFILE, & DP LOGIC UNIT $75K	1. SMALL COMPANY 2. NOT VERY FAST RATE	1. LOW $/1 BIT 2. 120-150 DAY DELIVERY 3. USED BY GE, CDC 4. ABOUT 150 IN FIELD	

H. ANDERSON

INTEROFFICE MEMORANDUM

DATE August 25, 1964

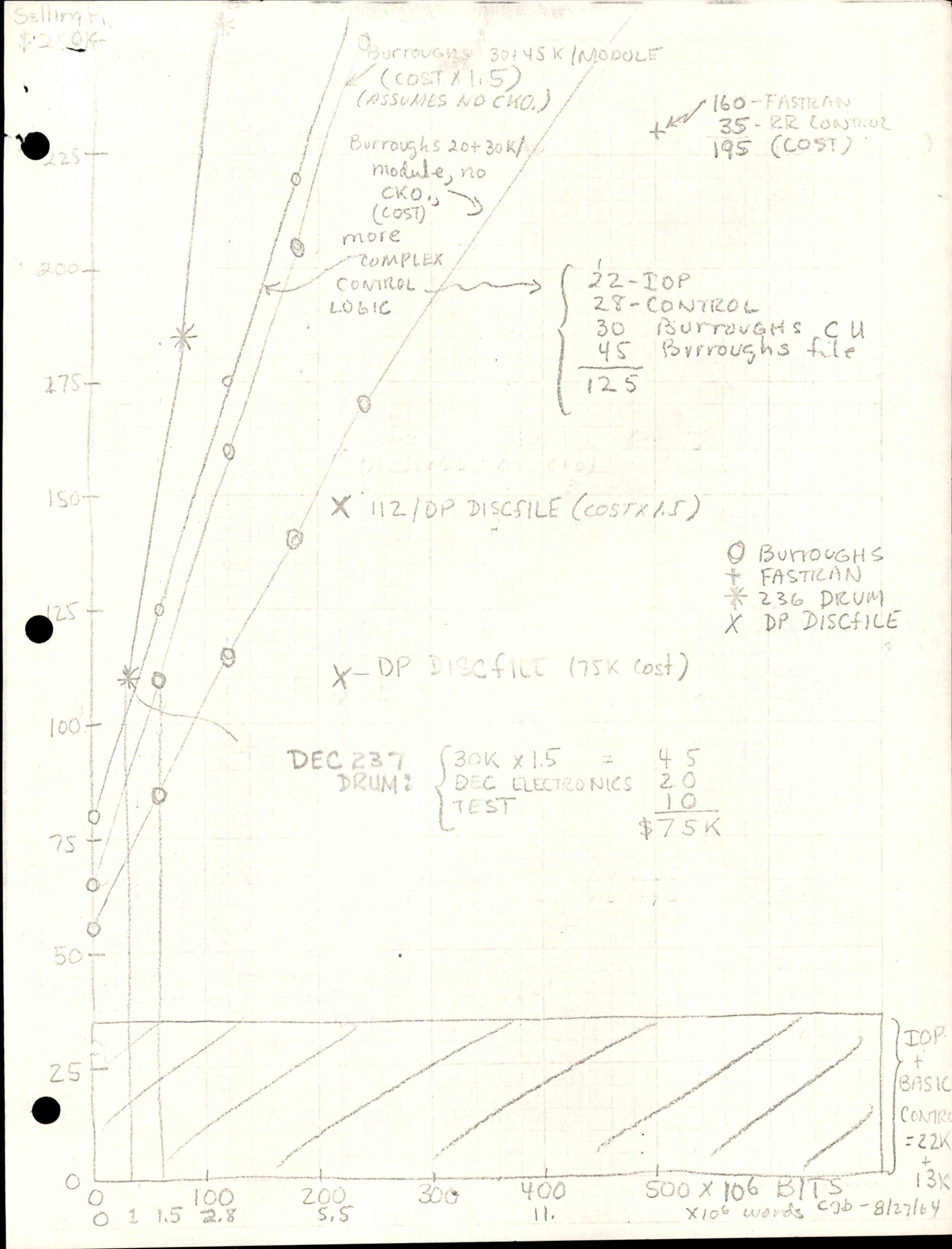
SUBJECT Bulk Storage Graph

TO Computer Guidance Committee

FROM Gordon Bell

The enclosed graph appends memo entitled Comparison of Drum and File Storage dated August 20, 1964 on DISC files.

GB/mro



Selling Pr.
$250K
Burroughs 30+45K/MODULE
(COST X 1.5)
(ASSUMES NO CKO.)
160 - FASTRAN
35 - RR CONTROL
195 (COST)
Burroughs 20+30K/module, no CKO., (COST)
more COMPLEX CONTROL LOGIC
22 - IOP
28 - CONTROL
30 Burroughs CU
45 Burroughs file
125
X 112/DP DISCFILE (COST X 1.5)
O BURROUGHS
+ FASTRAN
* 236 DRUM
X DP DISCFILE
X - DP DISCFILE (75K cost)
DEC 237 DRUM:
30K x 1.5 = 45
DEC ELECTRONICS 20
TEST 10
$75K
IOP + BASIC CONTROL = 22K + 13K
225
200
175
150
125
100
75
50
25
0
0 100 200 300 400 500 X 10^6 BITS
0 1 1.5 2.8 5.5 11. X10^6 words
CJb - 8/27/64

TECHNICAL MEMORANDUM - 700

To: Sales Staff

From: R. Belden

Note on the PDP-7 with Comments on the SDS 925

R. Belden
August 21, 1964

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Figure 1 I/O Buffer Comparison

Figure 2 Price Comparison

1.0 INTRODUCTION

Both machines in this comparison are faster and improved versions of earlier models. Announced at the Spring Joint Computer Conference April 1964, the PDP-7 first delivery date is September 1964. Announced in mid-1964, the SDS 925 first delivery date is expected in January 1965.

The SDS 925 is a single-address, binary, serial machine with a 24-bit word length (plus parity) and a 1.75 microsecond memory cycle time. The 925 is a faster version of the SDS 910 (8μs) and uses the 910's instruction set and internal organization. It appears as if no new features have been added to the 910 in designing the SDS 925. The 33ASR teleprinter may be offered with the basic computer in place of the 910 typewriter.

The PDP-7 is a single-address, fully parallel, binary computer with an 18-bit word length and a 1.75 microsecond memory cycle time. As a faster version of the PDP-4, the PDP-7 maintains full upward compatibility with the PDP-4 operation and programming. New features of the PDP-7 (explained later) include:

1. READ-IN Switch - reads in binary tape and executes the last instruction. Allows automatic loading of the PDP-4/7 manual loader (optional loader available for microtape).

2. Instruction Trap Mode - traps IOT instructions and prevents the program from halting or tying up the machine in an xct (itself). The Trap mode is intended to facilitate the addition of the many desired features in a time-shared system.

3. Paper tape punch is operated under program control. Both binary and alpha-numeric punching modes are standard equipment.

4. Model 33KSR teleprinter using ASCII code as standard equipment.

5. Dual Microtape System - provides a fixed-address magnetic tape facility for high-speed loading, readout, and program updating. (optional)

Unless otherwise noted, the discussion and comparison will be based on a Typical installation, as outlined on the Price Comparison Table. Typical is assumed to include a high speed paper tape reader and punch.

2.0 SPECIFICATIONS

2.1 Serial vs. Parallel - A quotation from the SDS 900 Series Input-Output Manual indicates the serial nature of the SDS 925 bit-transfer logic.

> ...The character register is connected serially to the word register and a 24-bit circular lift shift takes place through the word register. This transfers the contents of the character register into the least significant bits of the word register... (parity is checked but a parity error does not stop the computer)...As soon as the contents of the character register have been shifted into the word register, the contents of the number-of-characters-per-word counter are decremented by one. If the new content of this counter is still greater than zero, the buffer will wait for the next character. When the next character arrives, the character register and the word register repeat the shifting operation described above. The information which was in the 6 right hand positions of the word register will be shifted left 6 bits, and the new contents of the character register will be shifted into the 6 right hand positions of the word register. When the character counter reaches zero, it initiates an interrupt to the computer.
>
> (quoted from SDS 900 Series Input-Output Manual, page 2)

Advantages to the manufacturer of a serial machine are its cheap manufacturing cost. However cost is sacrificed at the loss of reliability and of I/O speed. Speed can be recovered with the addition of optional buffering or block-data-transfer hardware. Reliability, however, is not increased by the use of parity. Parity is used to detect errors, not prevent them. Because words on a serial line are transferred by 6-bit character parts and not in parallel by full words, it is frequently more difficult to diagnose trouble on a serial machine. Hence down time is longer.

2.2 Parity-check-sum - Because the PDP-7 uses parallel logic, a parity check is not generally provided as hardware. (Note that on most large general purpose computers parity is not used.) However to detect possible bit losses, binary tapes contain check sums which are recomputed by the loader as they are read into memory. The sums are compared with the block-sum included as the last word in the block. Should the sum not check, the loader error routine assumes control. In the alpha-numeric mode it is possible to compute parity under program control. However, this is rarely necessary.

3.0 INPUT/OUTPUT

3.1 Buffering - On the SDS 925 all input/output transmission is channeled serially through a single 5.5 character buffer, the W Register. The Y register, a second buffer, is optional equipment. With but a single buffer register, only one I/O device (Tape Reader or Teleprinter or Punch, etc.) can operate under computer control at a time.

The PDP-7 operates with separate buffering on each one of its I/O units (teleprinter, tape read, and tape punch). With buffering, all standard and optional I/O devices attached to the basic PDP-7 are capable of operating simultaneously at their maximum speed. Core memory is not required as a buffer. The central processor does no waiting for an I/O buffer to fill. The PDP-7 continues to compute and stops only long enough to service a buffer in response to a program interrupt. (See I/O Buffer Comparison, Figure 1) Character assembly is accomplished in each I/O buffer before word transfer.

3.2 Word Transfer - Words read from the SDS 925 W register are transferred directly to memory by a WIM instruction in 3 cycles plus a wait for the buffer to fill. It is not possible to load the accumulator (A register) directly with incoming data on the SDS 925. All characters go directly to memory. However, at the end of every I/O transmission it is necessary to sense an end-of-transmission code. (A carriage return or tab signifies this from a teleprinter, and a stop code from punched tape.) In real time applications, data just read in is immediately operated on. For manipulation, the data must be brought into the accumulator.

Instructions for transferring words between the SDS 925 assembler and memory are LDA (two cycles) and STA (three cycles). Words in any input buffer on the PDP-7 are transferred directly to the accumulator in a one cycle instruction. For each piece of data read and checked, the SDS 925 requires four additional cycles.

PDP-7 Instruction	Memory Cycles	
iot	1	reads input device buffer into accumulator
	X	perform validity check
dac	3	deposit contents of accumulator in next memory location, through auto-index register.
	4 memory cycles	

SDS 925		
1 WIM	3	deposit contents of W register in next memory location using index register
1 LDA	2	load A register from memory
	X	perform validity check
1 STA	3	store A register in memory
	8 memory cycles	

The time for data transfer exclusive of the data validity-check routine is twice as long on two SDS 925 as it is on the PDP-7.

3.3 Real Time Control - The Real-Time Control, furnished as standard equipment with PDP-7, provides communication between the Internal Processor and all I-O devices. Real Time Control gives the system the capability of operating efficiently over a wide range of information handling rates (from seconds per event to 570,000 words per second) with a large variety of input/output devices. The Real-Time Control consists of a Device Selector, an Information Collector, an Information Distributor, an Input-Output Skip facility, a Program Interrupt Control, a Data Interrupt Control, and a Clock/Timer.

3.4 Input/Output Skip - The Input/Output Skip facility of the PDP-7 enables the program to skip or branch according to various external device states. There are 21 standard inputs to the Skip facility. The iot pulses from the Device Selector strobe an input line and if a logic condition is present, the instruction following the iot is skipped. A similar function "Actuate and Test External Device" is described for the SDS 925 as requiring a routine of EOM and SKS instructions. Only six input signals can be tested.

3.5 Trap Mode - The Trap Mode is a new standard feature on the PDP-7 and has no equivalent on the SDS 925. The effect of the Trap is to insert a program break in place of the iot, xct, and hlt instructions. The break permits a simulation or substitution of an instruction in place of the trapped instruction. This is the basic hardware necessary for I/O device simulation.

A common type of simulation is simulating the paper tape punch or teleprinter while using microtape. This permits a rapid running of programs normally slowed by the punch (or other slow I/O devices) speed during a period of heavy use of the computer. Actual punching or listings from the microtape would be made at a later time. Similarly for input, the paper tape reader may be simulated by the keyboard. This removes the necessity for preparing test tapes when debugging. The application and flexibility inherent in the Trap Mode cannot be simulated on another machine without heavy programming restrictions.

3.6 Extend Mode - To make it possible for any program with a 13-bit memory address per instruction, to run in any memory bank of a 32,768 word (15 bits) PDP-7, it is necessary to supply the two high order bits of the instruction address. When in the Extend Mode, program control may be extended beyond the resident 8K memory bank.

When not in the Extend Mode, the high order two bits of an address are always supplied by the Program Counter. With these bits supplied, the memory bank of operation is immaterial to the program. In this way programs will run properly on any memory bank without the need for relocation. A priority interrupt is possible to any memory bank with a short subroutine.

The addition of the Trap and Extend Mode permits more than one user simultaneous access to bank portions of memory without fear of overlap. Now a real time control or lengthy program need not tie up long periods of machine time. The hardware for multi-user operation is included in the basic PDP-7 computers.

4.0 PROGRAMMING

4.1 Indexing - As a standard PDP-7 feature, Auto-Indexing provides eight separate index locations. When addressed, each location is incremented with no added machine time.

The SDS 925 has a single Index register which supplies address modification at no additional memory time. To reference the Index register, an instruction must contain a 1 in bit position 1. The index register is incremented by the combined instruction BRX - increment index and branch. If the index register contains a 1 in the high order address bit, there is no branch. In this way one index register is suitable for single loop control or for multi-loop control if all loops are incremented in parallel.

However when searching, sorting, or expanding data tables, the auto-index registers of the PDP-7 require but a small amount of initialization compared to that necessary to do the same program with one index register. In the following cases this is especially true. 1) When the program interrupt is being used for real time supervision of several programs, the eight auto-index registers of the PDP-7 eliminate the need for a subroutine to store and re-initialize a single index register in step with the current program. 2) When simultaneous input/output of data at different speeds requires more than one table pointer, it would be necessary to re-initialize a single index register (or use indirect addressing with a memory increment) each time the pointer is shifted between tables.

4.2 Program Interrupt - The basic SDS 925 includes two channels for priority interrupt. Each channel is limited to a unique memory location and is fixed in number priority. When used for I/O priority interrupting on the single-buffered SDS 925, the maximum speed of interrupt is governed by the speed of the I/O device connected at the time of interrupt. This is so because in the absence of separate I/O buffering the W register must remain connected to the peripheral device during the mechanical operation of the I/O device. (See Figure 1) If the paper tape punch is connected to the W register, an interrupt may be delayed 1/60 sec (16,667μs) while the current instruction cycle (a punch-character instruction) is completed.

Twelve channels on the basic PDP-7 are provided as standard equipment for use with program interrupt. Optionally this is expandable to any number of channels. When an interrupt occurs, the contents of the Program Counter and the Link are stored in memory location 0 and an interrupt program begins in memory location 1. Priority of a channel is determined by the program. Should an interrupt signal the computer after a lower priority routine has begun, the computer may either break immediately to the new routine (following an interrupt re-enable by the program) or completely service the present interrupt before responding to new one. All interrupt signals set flip-flops if they are not immediately acknowleged and are serviced in the order of their priority.

The speed of interrupt on the PDP-7 is not I/O limited because all I/O devices on the basic PDP-7 are equipped with separate word buffers. The accumulator is connected to an I/O buffer for the single memory cycle time of one iot instruction (1.75 microseconds). During this time, a word is transferred in parallel between the accumulator and the selected I/O buffer. After this memory cycle, the accumulator is free to load other I/O buffers in response to other program interrupts.

4.3 Register and Memory Examination/Modification

Program Counter Modification - To change the SDS 925 Program Counter, it is necessary to insert a BRU instruction and then execute it:

1. Switch REGISTER to select C
2. Push CLEAR
3. Key in the instruction BRU xxxxx (branch unconditionally to xxxxx)
4. Press STEP switch (single step, execute #3)
5. Press RUN

The equivalent branch is done on the PDP-7 in just two steps:

1. Set new address on ADDRESS switches
2. Press START (computer starts running at the address set in the ADDRESS switches)

Note: Should an error be made when keying in an instruction on the SDS 925, the complete register must be cleared and the instruction re-keyed. On the PDP-7 it is only necessary to reset the switch in error.

To change the contents of a memory location on the SDS 925 (equivalent to the PDP-7 DEPOSIT key)

1. Switch REGISTER to select C
2. Push CLEAR
3. Key in the instruction STA xxxxx (Store A register)
4. Switch REGISTER to select A
5. Key in new contents desired
6. Press STEP (executes STA)

To resume operations after a deposit or examine on the SDS 925, see Program Counter Modification (above).

To examine 5 (or any number) successive memory locations - Frequently when running or debugging a program it is necessary to examine the contents of memory locations without the aid of a debugging routine - to check data values or intermediate solutions. On the SDS 925 this is done by keying in and executing a branch instruction.

1. Switch REGISTER to select C
2. Push Clear
3. Key in the instruction BRU xxxx1
4. Push STEP switch

At this point the machine has executed the BRU and is now in IDLE mode. The contents of xxxx1 (the first location to be examined) are displayed in the C register. Pushing STEP again would not display xxxx2, it would execute the instruction contained in xxxx1. Therefore it is necessary to repeat the last three of the above steps manually four more times to examine the next four memory locations. Each time the address part of the BRU instruction would have to be incremented.

On the PDP-7, locations in memory can be examined at any time using the EXAMINE/EXAMINE NEXT key. For comparison, the two steps are

1. Set location to be examined in the ADDRESS switches.

2. Press EXAMINE.

The contents of xxxx1 are displayed in the memory buffer register. Pressing EXAMINE NEXT displays the contents of the next successive location xxxx2, and so on.

5.0 INSTRUCTIONS

5.1 Memory Increment - An instruction much boasted about on the SDS 925 is MIN (increments the contents of memory by 1). This instruction takes three memory cycles. The same increment to memory is provided by the PDP-7 isz instruction which adds 1 to memory in two memory cycles. In addition to counting, the isz instruction will increment and branch on zero if the count is predetermined.

MIN	COUNT	Add 1 to memory	3 cycles
isz	COUNT	Increment and skip if zero	2 cycles

5.2 Register Store - Because of its parallel logic, the PDP-7 is capable of storing the contents of the Accumulator in memory in less time than on the SDS 925. A dac (deposit accumulator in memory) instruction on the PDP-7 takes 2 cycle times; the corresponding STA instruction on the SDS 925 takes 3 cycle times.

5.3 Negate - Negate or complement is used regularly on the PDP-7 to minimize the number of load and store instructions needed in one's complement arithmetic. Complement the Accumulator cma is a one cycle instruction on the PDP-7.

The SDS 925 instruction set does not contain a similar complement function. A negate may be executed by using an EOR (exclusive or) with 111111. This takes two cycles and requires a memory location loaded with ones.

As a result of this, the three cycle STA instruction and other logical differences, times for programmed arithmetic on the two computers differ markedly.

6.0 SOFTWARE

6.1 PDP-7 FORTRAN - Derived from Fortran II and Fortran IV, the PDP-7 Fortran has already been field tested and proven on the PDP-4. The Assembler System operates with paper tape, mag/micro tape or punched cards. The alpha-numeric format on mag tape is IBM compatible. PDP-7 Fortran includes these added features:

1. The ability to mix symbolic codes with Fortran statements. Symbolic codes intermixed with Fortran statements permits the use of any peripheral devices (A/D Converters, CRT displays, etc.) during the execution of a Fortran program.

2. Variable precision floating point, a choice of mantissa (25 or 36 bits) and exponent (8 up to 99 bits)

3. Type declarations capable of overriding the Fortran naming conventions which differentiate fixed and floating variables.

4. Input/Output statements derived from Fortran IV.

   Tape control is an essential part of the Fortran language.

5. Built-in functions are indefinitely expandable.

6. Arrays of up to 4 dimensions, either fixed or floating, with the capability of expanding the Assembler for more.

7. Fortran language debugging with mag/micro tape.

8. Compiler includes diagnostic routine with an error analysis print out.

6.2 Program Library - A large program library for the PDP-7 is already available based on the field proven PDP-4 library. Where necessary, minor changes have been made in the I/O instructions to accomodate the 33KSR teleprinter.

Symbolic programs in the PDP-7 library focus on the concept of more efficient use of a computer installation through computer-aided programming. A typewriter rather than console switches is used for on-line debugging. On-line debugging with the PDP-7 gives the user close control over program execution, and prevents bugs from destroying other portions of his program. Symbolic editing relieves the programmer of the routine of reproducing, listing, and desk-checking his program.

Special-function programs now available for the PDP-7 include:

1. BUS PAK II - An assembler that provides a pseudo-language for business-oriented programming. Includes control of, but does not require, mag tape and card input/output equipment.

2. MAINDEC - Maintenance test routines for peripheral equipment and internal processor accuracy.

3. Diagnostic and demonstration routines for CRT display.

7.0 CONSOLE FUNCTIONS

(*Functions which are significantly different between the PDP-7 and SDS 925)

7.1 KEYS/SWITCHES

KEYS/SWITCHES	PDP-7	SDS 925
START	Clears major registers and starts computer running at the address set in the ADDRESS switches.	Initializes the control section of the computer.
*RIM (new feature)	Paper tape is read in binary mode into a memory block selected by the ADDRESS switches. Computer then automatically executes the last word in the block.	Equivalent is FILL. Computer reads one word into memory location 0002 and executes it. The X register is set to -6.
*REGISTER SELECT	Not necessary. All important registers (PC,MA,MB,AC,L) are simultaneously displayed.	Rotary switch to select any one of A,B,X, or C registers.
*REGISTER	15 ADDRESS switches establish the memory address for the start, examine, and deposit operations. 18 ACCUMULATOR switches set the word placed in memory by the DEPOSIT and DEPOSIT NEXT keys, or placed in the accumulator under program control.	24 switches permit loading a word into the register being displayed. The computer must be in Idle and the register cleared.
CLEAR	Not necessary. See DEPOSIT switches.	Clears contents of register selected.
STOP	Stops the processor at the completion of the memory cycle in progress at the time of key operation.	See IDLE.

KEYS/SWITCHES	PDP-7	SDS 925
*TRAP	Permits Trap mode to be enabled by the program.	Not available.
*EXTEND	Enables the Extend mode to be used with all memory reference console switches.	Not available.
SINGLE INSTRUCTION	Computer stops at the completion of each instruction. Repeated operation of CONTINUE while this switch is on will step the program one instruction at a time.	Instruction can not be observed one cycle at a time. A 3 position toggle RUN-IDLE-STEP switch selects normal run, idle, and step modes through instructions.
*SINGLE STEP	Computer stops at the completion of each memory cycle. Repeated operation of CONTINUE while this switch is on will step the program one cycle at a time.	Instructions can not be stepped or observed by memory cycles.
*EXAMINE EXAMINE NEXT	The contents of the memory cell specified by the ADDRESS switches are displayed in the accumulator and memory buffer register. A block of memory can be displayed in sequence by pushing the EXAMINE NEXT key. Each time this key is depressed, the program counter is incremented and the contents of the next location are displayed.	A branch instruction must be manually keyed into the C register and executed for each location examined. To examine successive locations, 3 steps must be repeated n times. See section 4.3.
*DEPOSIT DEPOSIT NEXT	Deposit places the contents of the accumulator switches in the memory location specified by the address switches. The program counter is set to the address of the next cell so that depressing the DEPOSIT NEXT key deposits the contents of the accumulator switches in subsequent memory locations. This feature facilitates keying in short test programs.	To change a memory location a store A instruction must be keyed into the C register and the new contents keyed into the A register. Because only 1 register is available at the console at a time this requires 6 manual steps. See section 4.3.

KEYS/SWITCHES	PDP-7	SDS 925
CONTINUE	Causes the computer to resume operation from the point at which it was stopped by the last previous operation of STOP or one of the EXAMINE or DEPOSIT keys.	A branch can be manually keyed in and executed to resume operation of the program. The Run key is also equivalent to the continue.
*REPEAT	Used with the SPEED controls, REPEAT makes it possible to step slowly through a program to find infinite loops or other errors.	Not available.
BREAKPOINT	The 18 accumulator switches can be read by the program.	4 switches can be tested by a program.
MARGIN TEST	A complete marginal test panel with variable voltage metering and control is standard equipment. All registers are displayed simultaneously.	A 3 position MARGIN TEST switch on console can be used while manually selecting registers with REGISTER SELECT switch.
MEMORY PARITY	Not offered on standard machines.	If set, switch causes computer to Idle for each parity error.
INTERRUPT ENABLED	Interrupt is controlled by computer program.	Locks interrupt mode on.
HOLD	See use of STOP and CONTINUE switches.	HOLD switch stops stepping of program counter.
POWER	On-off switch and indicator	On-off switch and indicator

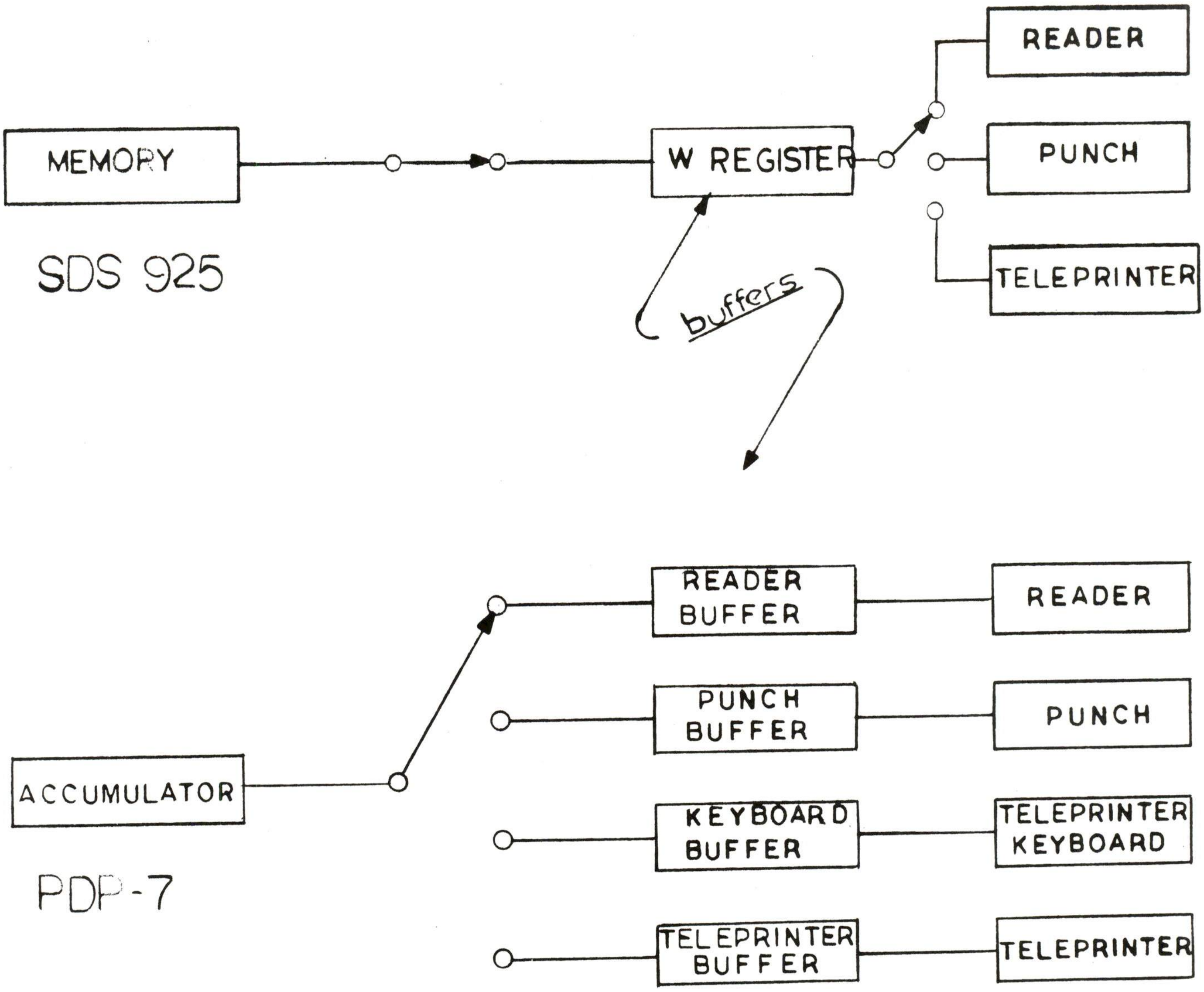
7.2 DISPLAYS

PROGRAM LOCATION	15 bit program counter continuously displayed.	14 bit program counter continuously displayed.

KEYS/SWITCHES	PDP-7	SDS 925
*REGISTER DISPLAY	18 bit accumulator continuously displayed. 18 bit memory buffer continuously displayed. 15 bit memory address register continuously displayed. 4 bit instruction register continuously displayed.	4 position rotary switch selects display of 24 bit C register <u>or</u> A register <u>or</u> B register <u>or</u> X register. Any <u>one</u> is continuously displayed.
OVERFLOW	Link bit indicator	Overflow indicator light
HALT	Run indicator on when program is running.	Indicator off when program is running.
*MEMORY PARITY	None	Indicator on when parity error has been made. Machine will not halt unless switch is set.
INTERRUPT	No indicator	Interrupt enables indicator
INPUT/ OUTPUT	No indicators necessary since each I/O device has its own buffer.	Lights showing which of the I/O devices is connected to the W register.
*CYCLE	Fetch indicator on when in fetch cycle. Defer indicator on when in defer cycle. Execute indicator on when in execute cycle. Break indicator on when in break cycle. Note: these indicators are especially useful when single-stepping through a program.	Machine control state is not displayed.

KEYS/SWITCHES	PDP-7	SDS 925
*DEBUGGING	SINGLE STEP and SINGLE INSTRUCTION indicators when in those modes. This is very useful when debugging programs. REPEAT indicator; see switch section.	Machine has no control state indicators.
POWER	POWER on indicator	Power on indicator

I/O BUFFER COMPARISON
SDS 925 & PDP-7



The SDS 925 W register serves as a single buffer register to all peripheral I/O devices. Because characters are fed from the W register directly to the peripheral device, the W register must remain connected to the peripheral device during the mechanical operation of the I/O device. (ex. 16,667μs. for a punch).

All I/O devices on the basic PDP-7 are equipped with separate word buffers. The accumulator is connected to an I/O buffer for a single memory cycle (1.75 microseconds). During this time a word is transferred in parallel between the accumulator and the selected I/O buffer. After this memory cycle, the accumulator is free to load other I/O buffers for simultaneous I/O operation.

Figure 1

PRICE COMPARISON

Figure 2

BASIC SYSTEM	PDP-7		SDS 925
Central Processor		Central Processor	
Operator Console		Operator Console	
4096 Word Memory		4096 Word Memory	
Console Teleprinter (10 cps)		Console Teleprinter (10 cps)	
Paper Tape Punch (63.3 cps)		Paper Tape Punch (cps)*	
Paper Tape Reader (300 cps)		Paper Tape Reader (cps)*	
		(*Note if low speed 33ASR, 10 cps Punch and Reader)	
Real Time Control with Program Interrupt (1 2 channels) Input/Output Test Input/Output Trap Real Time Clock Direct Data Interrupting			
	$72,000.		$80,000.

OPTIONS

Buffers for all I/O devices included in basic system		Second I/O Buffer (Y Register)	$7K-10K
Real Time Clock included in basic system		Real Time Clock	$1.5K
First Extra 4096 Word Core Memory Module	$16,000.	Extra 4096 Word Core Memory Module	$15K-20K
Dual Microtape System Two independent tape drives	$ 7,400.	MagPaK Unit (No MagPaKs yet delivered)	
Control for 4 Dual Microtapes	$ 9,400.	One dual control with tapes	$15,000.

PDP-7 SALES

Serial #	Customer	System Includes	Delivery
1	Prototype	4K	9/30/64
2	New York University	micro tape	10/16/64
3	Jet Propulsion Laboratory	12K	10/26/64
4	Bell Laboratories	8K	11/6/64
5	Stanford University	EAE	12/1/64
6			12/4/64
7	Technische Hogeschool Delft (Netherlands)	EAE	12/18/64

(Orders placed after September 1, 1964 may expect a 4-month delivery)

8/21/64

TO: Sales Newsletter FROM: Nick Mazzarese 4/29/64
Rev. 8/20/64

PDP-7 Competition

Machine	Word Length (bit)	Memory Cycle (microseconds)	Multiply (fixed)	Price Including Reader Punch & Typewriter	Index	First Installation	Orders Filled	Orders Unfilled
DEC PDP-7	18	1.75us	~~4.4~~ 6.1us	$72,000	8 auto	9/64	0	6
ASI-2100	21	2us	30us	87,800	3	12/63	5	2
SDS 925	24	1.75us	8us	92,000	1	1/65	0	0
CCC DDP-224	24	1.9us	6.47us	96,900	1	4/21/64	1	5
Honeywell 300	24	1.75us	7us	100,00?	1	7/65	0	4
PB 440	24	3us	23-38us	130,000	6	3/64	4	8

INTEROFFICE MEMORANDUM

TO: K. Olsen
H. Anderson
S. Olsen
N. Mazzarese
R. Beckman
T. Johnson
Receptionist Bldg. 12
All Sales Personnel
All District Offices

DATE: August 21, 1964

FROM: R. Bernier

SUBJECT: PDP-4 Course Convening August 24, 1964

The following individuals are scheduled to attend a two-week PDP-4 Maintenance and Familiarization Course convening August 24, 1964.

Name	Company
1. D. Agosti	Westinghouse Electric Corporation Pittsburgh, Pa.
2. -----	University of Pittsburgh Pittsburgh, Pa.
3. -----	University of Pittsburgh Pittsburgh, Pa.

INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT Data Processing Committee Progress Report

TO Works Committee

FROM Dave Packer

Since its inception in May, the major efforts of the Data Processing Committee have gone toward processing project and product line cost information and reporting to managers. Accomplishments to date include:

1. Design and implementation of a cost accumulation and charge numbering system that enables direct charging to projects, product lines, and cost centers. A revised charge number system was introduced June 29th and final numbering changes will be made September 28th.

2. Design of a PDP-4 processing system for taking in raw cost data and producing project, product line, and cost center reports.

Short term plans are:

1. To have individual project reports* for July and August available in September and to be producing reports on a routine, monthly basis thereafter. This lags our initial schedule by one month, due to programming problems.

2. To design and routinely distribute summary project and product line cost reports beginning in November.

3. To process and produce cost center reports starting in late November.

4. To evaluate desirability of extending system to include weekly labor runs, payroll, and other routine accounting functions currently handled by punched card equipment.

Longer range considerations:

1. The committee is currently beginning an evaluation of an inventory control-purchasing-accounts payable system as a possible next step for internal data processing.

* A sample of project report format is attached.

Other candidates for future work include the Orders-Shipments-Invoices-Accounts Receivable system and a prospect list for coordinating marketing efforts.

2. Programming resources now include one full time programmer and one in training. Future activity may necessitate more effort in this area.

3. Hardware is continually under study. The accounting PDP-4 will almost certainly be overloaded with the next year. Alternatives include a PDP-4 (7) reserved for internal data processing or use of the PDP-6 if a business compiler becomes available or on line operations are warranted.

Dave Packer

DWP:ncs
Attachment

PROJECT REPORT SEPTEMBER 1964

PROJECT NO. D,P 1394

Start Date	Project Manager	Complete Date
September 1964	______________	September 1966

Cost Center No.	Cost Center Name	Labor	Material	Overhead	Outside Contracts	Travel	Monthly Total (Act.)	Fiscal Year to Date Total (Act.)
14	Technical Publications	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
23	Drafting	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
24	Engineering	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
26	Model Shop	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
	Total Summary	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx

INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT News Releases

TO Jack Atwood

FROM Kenneth H. Olsen

We're now doing a lot of interesting things -- new modules, new computers, and computers being used in strange places and I think we ought to have a news release in the local newspapers every week. Will you have your news release man make out a schedule for the next few months listing what news release we will release each week.

Ken Olsen

KHO:ech

cc: Harlan Anderson

HEA

INTEROFFICE MEMORANDUM

SUBJECT: Announcement of Product Line Coordinator Appointments

DATE: August 24, 1964

TO: Works Committee

FROM: Win Hindle

For Engineering and Sales Newsletters

Product Line Coordinators

For each of the company's product lines, a product line coordinator has been appointed to take an overall view of the varied activities in the line. This responsibility encompasses coordination of planning, and control, in addition to taking effective action to recognize and solve problems in the product line. As DEC's product lines grow, it becomes more difficult to coordinate the efforts involved in planning, developing, and marketing the line. This new position has been developed to solve that problem.

The product line coordinator will be concerned with every phase of company activity. No aspect of the product line will be too large or too small for his attention. At the same time, he will work through others to accomplish these tasks, since he will have no direct control over those in other departments. No organization changes are required in establishing this position, as the coordinators will continue in their present assignments.

To illustrate the functions of a product line coordinator, he will do the following in his product line:

1. Work with Engineering in laying out development plans.
2. Coordinate Engineering schedules and assemble cost forecast for projects to be done.
3. Receive information about development projects, spot problems and take action.
4. Assure that programming, documentation and manuals are available, consistent and accurate.
5. Work with Computer Sales Manager on basic marketing strategy.
6. Help formulate and schedule advertising, mailings, etc.
7. Help in developing sales forecasts.
8. Receive salesmen's critiques on products.
9. Assure salesmen are well informed on product line.
10. Assure that technical problems get solved.

As the list indicates, the coordinator assures that no aspect of product line activity "falls between the cracks". He makes sure that all details are covered and all plans carried out. As time goes on, he will undoubtedly be the one who knows more about all aspects of an individual product line than anyone else in the company. He will need help from everyone and, in turn, he will be able to provide the information and stimulate the action that everyone needs.

Following are the coordinators for all company product lines:

Product Line	Coordinator
PDP-1	Ed Harwood
PDP-4	Ed Harwood
PDP-5	Ed DeCastro
PDP-6	Gordon Bell
PDP-7	Ron Wilson
LINC	Mort Ruderman
Memory Test Equipment	Pat Greene
Lab Modules	Burt Scudney
System Modules	"
Small Modules	"

WRHj:ncs

HEA

INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT Data Processing Committee Progress Report

TO Works Committee

FROM Dave Packer

Since its inception in May, the major efforts of the Data Processing Committee have gone toward processing project and product line cost information and reporting to managers. Accomplishments to date include:

1. Design and implementation of a cost accumulation and charge numbering system that enables direct charging to projects, product lines, and cost centers. A revised charge number system was introduced June 29th and final numbering changes will be made September 28th.

2. Design of a PDP-4 processing system for taking in raw cost data and producing project, product line, and cost center reports.

Short term plans are:

1. To have individual project reports* for July and August available in September and to be producing reports on a routine, monthly basis thereafter. This lags our initial schedule by one month, due to programming problems.

2. To design and routinely distribute summary project and product line cost reports beginning in November.

3. To process and produce cost center reports starting in late November.

4. To evaluate desirability of extending system to include weekly labor runs, payroll, and other routine accounting functions currently handled by punched card equipment.

Longer range considerations:

1. The committee is currently beginning an evaluation of an inventory control-purchasing-accounts payable system as a possible next step for internal data processing.

* A sample of project report format is attached.

Other candidates for future work include the Orders-Shipments-Invoices-Accounts Receivable system and a prospect list for coordinating marketing efforts.

2. Programming resources now include one full time programmer and one in training. Future activity may necessitate more effort in this area.

3. Hardware is continually under study. The accounting PDP-4 will almost certainly be overloaded with the next year. Alternatives include a PDP-4 (7) reserved for internal data processing or use of the PDP-6 if a business compiler becomes available or on line operations are warranted.

Dave Packer

DWP:ncs
Attachment

PROJECT REPORT SEPTEMBER 1964

PROJECT NO. D,P 1394

Start Date	Project Manager	Complete Date
September 1964	____________	September 1966

Cost Center No.	Cost Center Name	Labor	Material	Overhead	Outside Contracts	Travel	Monthly Total (Act.)	Fiscal Year to Date Total (Act.)
14	Technical Publications	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
23	Drafting	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
24	Engineering	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
26	Model Shop	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx
	Total Summary	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx	xxx,xxx.xx

INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT Installation of General Purpose Experimental Display System at Fort Meade

TO Computer Guidence Committee

FROM Tom Leonard

On Tuesday, August 12, 1964, the General Purpose Experimental Display System (PDP-4C-24 and 340-5) was shipped to Fort Meade, Maryland.

On Wednesday, August 13, 1964, I arrived at Fort Meade, accompanied by Joseph Kosiewski, to install the system and to assure that the on site acceptance tests were performed satisfactorily. The system did not arrive as scheduled on Wednesday due to difficulties encountered by the trucker.

The system finally arrived around 11:00 A.M. on Thursday, August 14. I inspected the system after it was unloaded from the van and found no visible signs of damage. However, as the resident millwrights were transporting the PDP-4 from the loading platform to the area in which it was to be installed, they damaged the manual intervention switches on the operator's console. The damage did not prevent the switches from operating, but did cause the bat handles to be broken. Also damaged to the point of uselessness were the speed switch and the speed potentiometer. It was possible to operate the system in spite of this damage.

By 2:00 P.M. on Thursday the system was plugged in, interconnecting cables connected and the basic central processor diagnostic tests were started. The central processor performed to the satisfaction of myself and the customer.

Friday, August 14 was spent in checking the operation of the special logic concerned with the shaft encoder knobs, track ball and lights and switches located on the special operators console of the 340 Display. All of these special devices performed satisfactorily. The 340 Display was also checked for the operation of the standard portions of this device and found to perform satisfactorily except that the raster was not square. This was noted as an exception on the acceptance sheet since I did not know the adjustment procedure necessary to square the raster and system operation was not adversely affected. Also noted was the fact that the first dot of a vector or increment was displaced from the rest of the vector by about one scope unit. This also was noted as an exception on the acceptance form.

After the basic 340 was shown to operate properly (except for a slightly distorted presentation caused by the two previously stated conditions(the subroutining capability of the display was checked for proper operation. Except for a couple of pulse terminating resistors that had been omitted, this portion of the display would also have been a success on the first try. This section of the 340 was given a more extensive test than was performed during checkout, so that the effect of the omission of these resistors was not readily apparent during checkout. One condition was encountered both on the checkout floor and on the customer's site which may result in a programming restriction if corrective logic cannot be disigned to correct the condition. The situation is that when a vector is drawn and the light pen picks up the very last dot on the vector and certain historical conditions in the 340 are true, the display will hang up, not in an unknown condition, but in an undesired one. I will examine the logic more extensively and try to find a solution to this problem. This is noted as the third exception on the acceptance sheet.

The entire system was now checked out as a closed or self contained entity. However, this system is to be considered as a piece of input/output equipment attached to the data channels of a CDC-1604A computer. It now remained to check the ability of the two computers (PDP-4 and 1604A) to successfully communicate with one another and the ability of the 1604 to transfer a program to the PDP-4 and then tell the PDP-4 to execute this program. The customer had provided a closed loop self checking test which allowed the PDP-4 to simulate, with its special lights and switches, the action of the 1604. The test was successfully run on August 15 and on August 16, Sunday, the PDP-4 was connected to the 1604 lines and the 1604 successfully transferred data to the PDP-4. The PDP-4 was not successfully transferring data to the 1604 due to the fact that one wire was missing. (The fact that this wire was missing was about the only condition that the simulated test could not detect.) The following test was then performed: 1) A program was read into the PDP-4 via paper tape and the PDP was started. A picture was presented on the display. 2) The 1604 read the contents of the PDP-4 memory into its memory. 3) The 1604 then zeroed the portion of its memory containing the PDP-4 information. 5) The 1604 filled the PDP-4 memory with zeroes, this caused the PDP-4 to hang up. 6) The 1604 then read its tape back into its memory. 7) The 1604 transferred the information in its memory to the PDP-4 memory. 8) The 1604 then told the PDP-4 to start executing this program and the PDP-4 resumed, displaying on the face of the 340 screen the same presentation that was being displayed when the data transfers were first set up between the two computers. This was a rather extensive test for the PDP-4/1604 interface and the device performed properly on the first attempt. One more condition remained to be checked before the system could be considered to be operating properly. Since the PDP-4 was on the same data channels as other input/output devices attached to the 1604, it was necessary to prove that no interaction was noted between devices on the same channel and the PDP-4. A missing wire in the interface allowed data to enter the PDP-4 while a card reader on the same channel was operated. The insertion of this wire allowed proper operation to take place.

On Monday, August 17, an overall check of the previously run tests was made and all tests ran satisfactorily.

On Tuesday, August 18, I obtained the signature of H. Quentin Foster, authorized to sign, on the acceptance forms and I took my leave of Fort Meade.

Tom Leonard
Project Engineer

H Anderson

dec INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT Patent Policies

TO Works Committee

FROM J P Hastings

1. Policy. Bob Cesari, from time to time, advises the Company on legal matters not relative to patents and copyrights. This practice was established several years ago and although Cesari is willing to do this, he would prefer an endorsement by Company management to be assured that this is the case. At the present time, for example, he is advising the Company on the Sales Agreement form under draft in the Sales Department.

2. PDP-6 Invention Possibilities. Bob Cesari has compared the number of DEC's patents with competitors such as CDC. He finds we are less active than most of our competitors and has suggested we take a strong look at those areas in the Company that are most apt to produce patents. There is little time remaining to file on inventions resulting from the PDP-6. After discussing the PDP-6 system with Bob Savell, the following are invention possibilities:

I/O Bus
Block Transfer
Adder
The Overall System

Cesari would like to stimulate discussion by management in these and other areas.

3. Other Invention Possibilities. Don White's capacitor diode gate - Cesari is undertaking preliminary search. Steve Lambert's pin connector for racks proposal - Cesari recommends no action until a model is made. Ken Olsen's ceramic chip process - Chicago Telephone and Supply.

4. Infringement. The Company is involved in several possible infringement problems.

A. Illinois Scientific Corporation - basic computer patents.
B. IBM - broad data processing coverage.
C. Cleeton - means of producing variable number of pulses.
D. MIT - magnetic core storage.

5. Legal Decisions. Cesari has cautioned against non-lawyers within the Company making quasi-legal decisions without first obtaining legal advice. Areas most apt to fall in this category would be Purchasing, and Sales (including Customer Relations) where we are making contracts with other organizations.

JPH:ASJ

INTEROFFICE MEMORANDUM

DATE August 24, 1964

SUBJECT Visit by Brookhaven National Labs. and Bell Labs.

TO

H. Anderson	A. Titcomb
P. Samson	A. Kotok
G. Bell	H. Morse
N. Hirst	N. Mazzarese
H. Hyman	B. Colburn
R. Lane	

FROM P. Harris

On Thursday, August 27, 1964, Roger Jones, Dr. Hien, Dr. Love, Eric Willen, and others from the Applied Math. Department of Brookhaven National Labs. will arrive to become more familiar with our software.

They are interested in compiling FORTRAN statements that they will bring in the form of punched cards. Time has been scheduled on the PDP-6 for 11:30 - 12:00 and 2:30 - 3:30.

On Friday, August 28, 1964, representatives from Bell Laboratories will visit DEC to discuss the PDP-6. A demonstration has been scheduled for 11:00 a.m.

INTEROFFICE MEMORANDUM

DATE 24 August 1964

SUBJECT PDP-6 Warranty Maintenance

TO H. Anderson
S. Olsen
N. Mazzarese
T. Johnson
J. Fadiman
Applications Engineers

FROM R. Beckman

I resurrected the attached, which was written and received limited distribution last spring. I think this clearly states the position in regard to warranty maintenance for PDP-6 systems. The only thing that has changed since March is that we now know where the first PDP-6's are going.

Note that this does not commit us to an "on-site" maintenance man. Although maintenance of the PDP-6 systems to which the personnel are assigned will be their primary responsibility, we have to retain the ability to use these people on other jobs.

At the present time there are eight field service people assigned to PDP-6's; one for each of the PDP-6 systems presently on order and the Prototype, and one man responsible for general conduct of all PDP-6 maintenance. Of the eight people, four of them are DEC employees who were moved from other jobs onto the PDP-6 project and four of them are new employees. Our recruiting efforts, both from within the company and from outside, are continuing so that we can cover future requirements.

Please note that the spelling out of warranty maintenance in this way applies only to the PDP-6 systems at the present time.

***

PDP-6 Maintenance Availability

Personnel assigned will be senior technicians or junior engineers, supported by Applications Engineers and Managers of nearest office. Additional back-up available by phone or in person from Maynard. Final number and location of personnel will depend on number and location of systems. At least one man will be available for every system that is over six hours normal travel time from any other system, and at least one man for every two systems in one area.

Each maintenance office will be provided with adequate tools and test equipment. At least one of every type module used in the system will be available in each office, along with some of the more critical and "failure prone" mechanical sub-assemblies. Regional offices will stock additional spares, including those items with low potential usage rate. Additional logistic support available from Maynard.

Warranty maintenance will be provided on a "one-shift" basis. Twenty-four hour on call maintenance available at extra cost. On call maintenance personnel can be provided on a contract basis after expiration of warranty. Such contract maintenance is available on either a one-shift or a twenty-four hour plan.

Warranty and contract maintenance include scheduled preventive maintenance, as deemed appropriate by DEC, as well as any corrective maintenance required. Replacement parts required are included in both warranty and maintenance contract.

The above for publication to customers. The following thoughts on policy for internal use:

1. The first two or three PDP-6's in Australia (or anywhere) will each require at least one maintenance man at first. The importance of insuring successful operation of the first systems is obvious.

2. Any commitment for "twenty-four hour" service will probably require one or two additional men. If we're real lucky we can spread these men over more than one system, but we can't count on it.

3. It must be clearly understood that the maintenance man's first responsibility is maintenance. As the men (and the company) gain experience with the systems, it's quite possible that some of them can contribute to the direct sales effort. To the maintenance man, however, <u>direct sales to new customers has to come a long way behind service to present customers</u>.

RJB 3/3/64

dec **INTEROFFICE MEMORANDUM**

SUBJECT: Proposed Time Sharing System for Universities

DATE: August 25, 1964

TO: To:

FROM: Don A. Witcraft

Environment: There are three basic applications for a computer in a university: Administrative control, education and research. University administrations normally operate a card or batch system for keeping student records, classroom scheduling, payroll, etc. Education and research is conducted on the departmental level where there may be hundreds of computer users clamoring for service. These two factions are frequently at odds when it comes to partitioning a limited computer budget. The proposed system is aimed at satisfying both factions. A batch system is available for administrative use or a service bureau type operation and a multiple station on-line system is available for education and research. It should be noted that the batch system can be guaranteed adequate machine time by allocation of priorities in the system.

User Statistics: Since MIT has the only operational time sharing system in a university environment, only a very limited amount of information is available on the type of use that such a system will get. However, I don't believe that the type of problems run on the MAC system will differ drastically from those of other universities.

The statistics presented here were obtained from Mr. Tom Hastings, Systems Programmer at MAC. The sample was taken from 9:15 to 10:37 A.M. on August 11, 1964. Twenty-four people were active on the system and the sample includes 1706 interactions.

An interaction is the event of a user program taking control of the computer.

Running time per interaction is the time from the start of an interaction until the program is finished or placed in an input or output wait status. It includes user initiated read and write times for the disk.

Elapsed time per interaction is the time between two successive interactions excluding input-output time.

An examination of Figure 2 shows that 52% of the interactions have 50 milliseconds running time or less, 80% of the interactions have 1 second or less running time. This indicates that a great amount of program switching occurs on short programs and the switching time should therefore be very fast. This phenomenon is probably caused by two things: 1) The execution of system commands stored on the disk and 2) a large number of student programs. The first cause could be alleviated by keeping commonly used commands in core as pure procedures.

The MAC system has a 32K user core, a 32K system core, 0.2K drum, 9.2K disk. Programs are swapped between core and drum or core and disk. A maximum of 24 active users and 256 system users is possible. This provides an average user file of about 37K.

No attempt is made to keep more than one program in core. A program is transferred to core, executed for one or more shot times, transferred to drum or disk and the next program is brought in.

Table I: MAC Statistics

Item 1: Number of Interactions
Item 2: % of Total Interactions
Item 3: Average Running Time (seconds)
Item 4: % of Total Running Time
Item 5: Average Elapsed Time (seconds)

Running Time (Sec.)	Item No.	Range of Time Average Core Lengths				
		0 — 4095	4096 - 8191	8192 - 16383	16384 - 32768	Combined
0 to 0.24	1	602	114	150	27	893
	2	35.29	6.68	8.79	1.58	52.34
	3	0.06	0.04	0.05	0.11	0.05
	4	1.68	0.22	0.34	0.15	2.39
	5	4.24	4.20	2.82	4.72	4.01
0.25 to 0.49	1	174	3	5	11	193
	2	10.20	0.18	0.29	0.64	11.31
	3	0.40	0.40	0.40	0.40	0.40
	4	3.45	0.06	0.10	0.22	3.83
	5	3.82	5.81	2.37	13.13	4.34
0.50 to 0.99	1	192	2	1	8	203
	2	11.25	0.12	0.06	0.47	11.90
	3	0.69	0.70	0.82	0.69	0.70
	4	6.62	0.07	0.04	0.27	7.00
	5	5.30	13.83	13.22	14.23	5.78
1.00 to 1.99	1	136	18	17	22	193
	2	7.97	1.06	1.00	1.29	11.31
	3	1.27	1.25	1.29	1.56	1.30
	4	8.56	1.12	1.08	1.70	12.46
	5	10.21	12.68	6.95	42.29	13.81
2.00 to 3.99	1	52	10	5	16	83
	2	3.05	0.59	0.29	0.94	4.86
	3	2.76	3.02	3.10	2.88	2.83
	4	7.11	1.50	0.77	2.28	11.66
	5	33.45	33.08	53.10	52.79	38.32
4.00 to 7.99	1	35	26	9	15	85
	2	2.05	1.52	0.53	0.88	4.98
	3	5.10	5.31	5.80	6.09	5.41
	4	8.85	6.84	2.59	4.53	22.81
	5	62.09	79.34	60.44	135.86	80.21
8.00 to 15.99	1	12	7	10	13	42
	2	0.70	0.41	0.59	0.76	2.46
	3	9.91	10.60	11.98	11.64	11.05
	4	5.90	3.68	5.94	7.50	23.02
	5	72.37	159.87	211.92	216.56	164.81
16.00 to 31.99	1	1	4	6	1	12
	2	0.06	0.23	0.35	0.06	0.70
	3	27.95	24.02	19.12	20.45	21.60
	4	1.39	4.76	5.69	1.01	12.85
	5	531.57	507.21	326.58	506.45	418.86
32.00 to 63.99	1	0	1	1	0	2
	2	0	0.06	0.06	0	0.12
	3	0	47.33	32.80	0	40.07
	4	0	2.35	1.63	0	3.98
	5	0	992.97	709.02	0	850.99

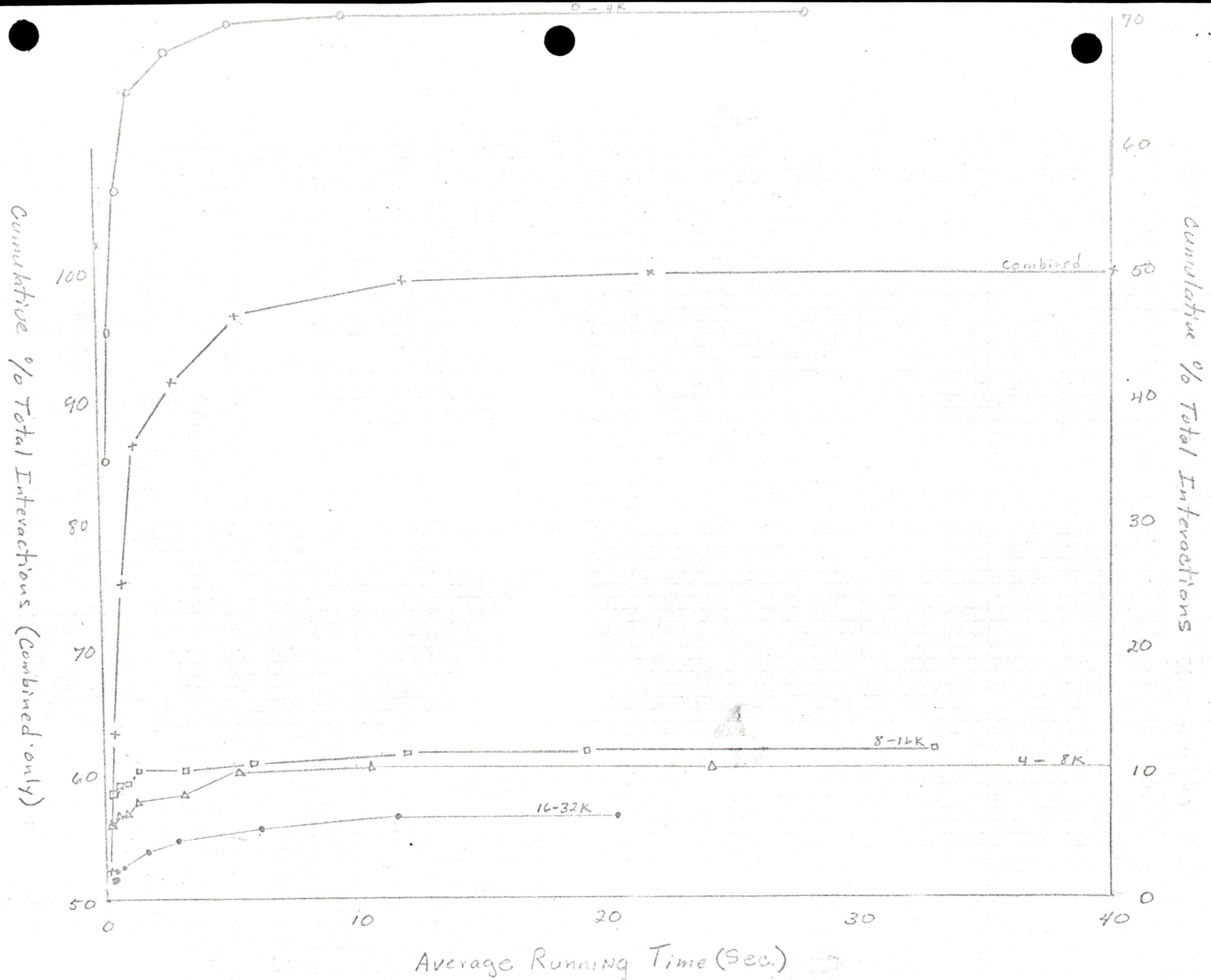


Figure 1: Cumulative % Total Interactions vs. Average Running Time

Figure 2: Cumulative % Total Interactions Vs. Average Running Time

PDP-6 Time-Sharing System Configurations:

Basic Configuration:

Quantity	Equipment	Price
1	Arithmetic Processor - 166	$146,100
1	Core Memory - 163C	126,000
1	Data Communications System - 630 (8 Line System)	14,202
		$286,302

Comment: The Basic Configuration includes only the minimal amount of hardware to perform time-sharing. Consoles should be leased from the telephone company since the lease includes maintenance. This system can be used for such things as JOSS but lacks a general purpose time sharing capability. No provision is made for system program maintenance except via a console.

Paper-Tape Configuration:

Quantity	Equipment	Price
1	Basic Configuration	$286,302
1	Paper-Tape Reader - 760	9,000
1	Paper-Tape Punch - 761	5,500
1	Line Printer - 646	30,000
		$330,802

Card Configuration:

Quantity	Equipment	Price
1	Basic Configuration	$286,302
1	Card Reader (200 cpm)	16,500
1	Card Punch (100 cpm)	29,000
1	Line Printer - 646	30,000
		$361,802

Comment: The Paper Tape and Card Configurations provides for System Program maintenance and a limited processing capability when not time-sharing. It also provides the time-sharing users with hard-copy storage.

Microtape- Paper Tape Configuration:

Quantity	Equipment	Price
1	Paper Tape Configuration	$330,802
1	Data Control - 136	10,000
1	Control Unit - 551	14,000
4	Dual Microtape Transports	19,600
		$374,402

Comment: This is essentially the current prototype configuration.

Microtape-Card Configuration:

Quantity	Equipment	Price
1	Card Configuration	$361,802
1	Data Control - 136	10,000
1	Control Unit - 551	14,000
4	Dual Microtape Transports	19,600
		$405,402

Comment: The last two configurations provide backup storage for time-sharing users. Microtapes are much too slow to permit program swapping. However, several people could edit symbolic tapes while a "main" user is operating. Also, a "pure procedure" version of DDT would allow several time-sharing users to debug concurrently. The system can be used for batch processing when it is not being time-shared or the "main" user could be a batching operator.

Drum-Paper Tape Configuration:

Quantity	Equipment	Price
1	Paper Tape Configuration	$330,802
1	Drum Processor - 167	22,000
1	Drum Control Unit - 236	13,000
1	Drum Unit - 237	75,000
		$440,802

Drum-Card Configuration:

Quantity	Equipment	Price
1	Card Configuration	$361,802
1	Drum Processor - 167	22,000
1	Drum Control Unit - 236	13,000
1	Drum Unit - 237	75,000
		$471,802

Comment: The Drum Configurations provide the first large scale time-sharing capability. In these configurations, the drum holds the users files, including his core image. If there are N users in the system the average file storage per user is limited to $2^{20}/N$ words of storage. For A active users the response time of the system is:

$$\text{Response Time} = \sum_{i=1}^{A} (\text{Fetch latency } (i) + \text{Fetch transfer } (i) + \text{shot } (i) + \text{store latency } (i) + \text{store transfer } (i)) \times 10^{-3} \text{ sec.}$$

If we assume a shot time of 60 ms, on average latency of 16.7 ms, and a maximum user core size of 12,288 words, then the worst response time is approximately 0.1174A seconds.

A	Response Time (seconds)
8	0.9392
16	1.8784
24	2.8176
32	3.7568
40	4.6960
48	5.6352
56	6.5744
64	7.5136

The response time is the time between 60 ms compute shots on a simple round robin scheduling.

This system can be expanded to 64 active users for a cost of $61,720. However, 64 active users would only allow 16K average file capacity per user which is inadequate. Sixteen users (65K) is about the upper limit on file storage.

Drum-Paper Tape-Microtape Configuration:

Quantity	Equipment	Price
1	Drum-Paper Tape Configuration	$440,802
1	Data Control - 136	10,000
1	Control Unit - 551	14,000
4	Dual Microtape Transports	19,000
		$483,802

Drum- Card-Microtape Configuration:

Quantity	Equipment	Price
1	Drum-Card-Configuration	$471,802
1	Data Control - 136	10,000
1	Control Unit - 551	14,000
4	Dual Microtape Transports	19,000
		$514,802

Comment: The Microtape extends the previous Drum systems in file capacity, permitting private files to be stored in a microtape library. This has the disadvantage of requiring a local operator for tape changing. The number of active users has not been increased, but the number of inactive users can be extended indefinitely.

Drum- Paper Tape- Disk Configuration:

Quantity	Equipment	Price
1	Drum-Paper Tape Configuration	$440,802
1	Disk File (19 x 10^6 char.)	94,000
		$534,802

Drum-Card-Disk Configuration:

Quantity	Equipment	Price
1	Drum-Card Configuration	$471,802
1	Disk File (19 x 10^6 char.)	94,000
		$565,802

Comment: The addition of the disk file to the drum systems increases the capacity from 16 users to 48 users with an average file capacity of 65K. The system can handle 64 active users with an average active file capacity of 16K, using additional Data Communication lines. There is no provision for overflow of disk storage or for recovery from disk or drum failure.

Drum-Paper Tape - Disk-Microtape Configuration:

Quantity	Equipment	Price
1	Drum-Paper Tape-Microtape Configuration	$483,802
1	Disk File	94,000
		$577,802

Drum-Card-Disk-Microtape Configuration:

Quantity	Equipment	Price
1	Drum-Card-Microtape Configuration	$514,802
1	Disk File	94,000
		$608,802

Comment: This system extends the file capacity of the preceding system and provide the capability of recovery from disk or drum failure.

Batch Configurations:

The following magnetic tape configurations can be used to supplement the preceding card (or paper tape) configurations yielding a system capable of concurrent time-sharing and batching operations.

Slow Tape System:

Quantity	Equipment	Price
1	[illegible] ontrol -516-520	$ 18,000
4	[illegible] ransports - 50	72,000
		$ 90,000

Medium 4-Tape System:

Quantity	Equipment	Price
1	Magnetic Tape Control-516-521	$ 18,000
1	Data Control -136	10,000
4	Magnetic Tape Transports-570	121,600
		$149,600

Medium 8-Tape System:

Quantity	Equipment	Price
2	Medium 4-Tape Systems for overlapped tape operations	$299,200
	or	
1	Medium 4-Tape System	$149,600
4	Magnetic Tape Transports-570	121,600
		$271,200

System Extension:

There are several alternatives open in extending these systems, depending on the capability desired. The addition of the Fast Memory (162) will increase the processor capability to beyond that of the IBM 7094. Increasing the core memory will have a double effect! 1) the response time will be decreased since less switching will occur and fewer memory cycles will be stolen by the drum, 2) larger problems can be handled. Increasing the drum storage will permit more active users and/or larger active files for the active users. Increasing the disk capacity will increase the number of system users and/or their file capacity.

The open-ended design of the PDP-6 should be stressed. There is no upper bound on the expansion of the users system by suitable overlapping of memory modules. Additional arithmetic processors, drum processors, core memory, disk files and input/output equipment can be added as the need arises.

Cost Analysis:

Table 2 is a summary of the user cost for the systems discussed here. Except where noted, the average active user files, i.e. user's files on the drum, are 65K as are the inactive user files. An average of one 65K file per user is assumed. The maximum response time is based on a simple round robin scheduling with maximum core swapping. In the estimates no provision is allowed for storage of system programs on the drum. This will probably require less than 65K and the active user storage must be decreased by this amount.

It is not unreasonable for a large time-sharing system to provide computing facilities for several universities. For example, the state of Oregon has eight widely separated campuses with a total enrollment of about 30 thousand students. All administrative computing is performed on one campus. A system including fast registers, 32K core, 2 drums, 2 disks, and a 4 tape batch system with high speed printer and card equipment for a cost of $1,135,882, would provide adequate computing facilities for several years to come. I don't believe that Oregon is unique in this respect.

One item that would greatly enhance the multi-university application is the availability of remotely located small computers for peripheral control with microwave transmission to the PDP-6.

Software:

The currently proposed software appears quite adequate for systems not involving drums, disks, and multi-arithmetic processor systems. The extension of the supervisory routine to drums and disks should not be a difficult programming task. I would estimate six-man months. The extension to multi-arithmetic processors is more complicated and can be delayed until completion of the preceding system.

Eventually, I believe all the three American Standard compilers should be made available. Also simulators for the major competitive machines should be developed to ease the user transition to the PDP-6.

Table 2

System Configuration	System Cost	Number Active Users	Cost per Active User	Number System Users	Cost per System User	Max. Response Time (Sec.)	Comments
Basic	286,302	8	35,788				Very limited activity. Typewriter only.
Paper Tape	330,802	8	41,350				Typewriter only or one "main" user
Card	361,802	8	45,225				Same as Paper Tape
Microtape-Paper Tape	374,402	8	46,800				Typewriter only or one "main" user + editing.
Microtape-Card	405,402	8	50,675				
Drum-Paper Tape	440,802 455,004	8 16	55,100 28,438	16 16	27,550 28,438	0.94 1.88	General computing ability.
Drum-Card	471,802 486,004	8 16	58,975 30,375	16 16	29,487 30,375	0.94 1.88	
Drum-Paper Tape-Microtape	483,802 498,004 526,408	8 16 32A	60,475 31,125 16,450	16+ 16+ 32+	30,475 31,125 16,450	0.94 1.88 3.76	+ Microtape backup A: Average Active User file $\leq$ 32K
Drum-Card-Microtape	514,802 529,004 557,408	8 16 32A	64,350 33,063 17,419	16+ 16+ 32+	32,175 33,063 17,419	0.94 1.88 3.76	Requires operator for tape changing
Drum-Paper Tape-Disk	534,802 549,004 577,408 605,812	8 16 32A 48B	66,850 34,313 18,044 12,621	48 48 48 48	11,141 11,438 12,029 12,621	0.94 1.88 3.76 5.64	B: Average Active User file $\leq$ 21K
Drum-Card-Disk	565,802 580,004 608,408 636,812	8 16 32A 48B	70,725 36,250 19,013 13,267	48 48 48 48	11,788 12,083 12,675 13,267	0.94 1.88 3.76 5.64	
Drum-Paper Tape-Disk-Microtape	577,802 592,004 620,408 663,014	8 16 32 64C	72,225 37,000 19,388 10,360	48+ 48+ 48+ 64+	12,038 12,333 12,925 10,360	0.94 1.88 3.76 7.51	C: Average Active User file $\leq$ 16K; Average User file $\leq$ 47K
Drum-Card-Disk-Microtape	608,802 623,004 651,408 694,014	8 16 32 64C	76,100 38,938 20,356 10,844	48+ 48+ 48+ 64+	12,683 12,979 13,571 10,844	0.94 1.88 3.76 7.51	

Other Markets:

DEC has the first commercially available large scale time sharing system in the U.S. market. They should make hay while the sun shines. Competitive systems are from one to two years away in delivery.

The potential market for time-sharing systems is extremely large. To mention a few: Universities, aircraft and aerospace industries, service bureaus, federal, state and some local governments, high schools, large business organizations, etc. It is difficult to think of computer applications in which time-sharing would not be advantageous.

Probably the most lucrative market exists in those organizations employing many programmers. If you consider that approximately half he cost of a computing installation is in equipment and the other half in programmer salaries, a considerable savings can accrue by providing direct machine access for program debugging to many programmers. The situation relative to problem throughput is similar to the transition from serial to parallel computers. These people have the money and the most immediate gain from using time-sharing.

Service bureaus can obtain two major advantages; program debugging for their own personnel and the sale of computer time to small users on a utility type basis. Small organizations can obtain direct access to a large system on a dial up basis and pay only for the time used. In the long run this usage will have the heaviest inpact on the computer industry. Many small users currently without computing facilities will be forced to use these facilities by the pressure from their large competitors.

Summary:

A wide spectrum of time-sharing systems has been presented. Customers can start with a small system and progress to larger systems by the simple aquisition of equipment. No reprogramming is necessary. A large market exists and can be sold by explaining the capabilities of the system, its expandability, and the inherent economic advantages of time-sharing.

H. Anderson

INTEROFFICE MEMORANDUM

DATE August 25, 1964

SUBJECT DATA COMMUNICATION SYSTEMS HARDWARE

TO Computer Guidance Committee FROM J. Smith

E. Harwood
D. Smith

A review of progress to date with D. Smith yielded the below data:

Bell Telephone Laboratories — Delivery Date: 8/15/64

1 - 634S
1 - 632E

Status: (Overdue)

Drawings will be released for construction	3 Weeks
Construction	2 Weeks
Checkout	1 Week
Delivery to Customer	6 Weeks

New Delivery Date 10/12/64

Dow Badische — Delivery Date: ?

1 - 634S

Status: (Overdue)

Same Cycle as Above

New Delivery Date 10/12/64

Hanscom Field — Delivery Date: 11/9/64

1 - 633A
1 - 632B
1 - 635A
1 - 635B

Status: (On Schedule)

Drawings will be released for Construction	3 Weeks
Construction	3 Weeks
Checkout	2 Weeks
Delivery to Customer	8 Weeks

Available for Installation 10/19/64

Western Australia — Delivery Date: 10/20/64

1 - 633A
1 - 632B
1 - 635A
1 - 63B

Status: (On Schedule)

Available for Installation — 9/25/64

- -

PDP-7 New York University — Delivery Date: 11/2/64

1 - 634A
1 - 632C

Status: (On Schedule)

- -

Foxboro — Delivery Date: 12/2/64

1 - 634A
1 - 632C

Status: (On Schedule)

- -

The above dates are based on the assumption that documented diagnostics will be available for Bell Telephone, Dow Badische and Western Australia when required. Pressure should be exerted for their availability within three to four weeks.

H.E. Anderson

INTEROFFICE MEMORANDUM

DATE August 25, 1964

SUBJECT PDP-6 Backup info, etc.

TO R. Lane

FROM Gordon Bell

cc. P. Harris
N. Mazzarese
T. Johnson
N. Hirst
H. E. Anderson

Please have the following sent to local sales offices:

1. I/O Bus Memo (by Dave Gross)
2. Time Sharing Reprints
3. Memory Bus Memo (Alan Kotok)
4. Two memos by Bell, Kotok, Best on 167, 236, and 237.

I would like the index from the PDP-6 document control distributed also, which will be availabe from N. Hirst on IBM cards as a listing.

F65 already has addenda and errata sheets.

I think a corner of the Sales Newsletter should be filled by PDP-6, and include tid bits, etc., each week, and a conscientious attempt made to fill it.

On our next sales meeting a considerable amount of time should be spent on:

**1. The presentation of the PDP-6 hardware, an example of customer presentations. Each person should take home overhead, or 35mm. slides, with an outline of PDP-6.

2. The I/O Bus Hardware system, and how to connect to it, ie. something with which our sales people may identify.

3. Same as 2, except memory bus, with discussion of memories, pseudo memories, processors, etc.

**Mandatory, overdue, etc.

GB/mro

INTEROFFICE MEMORANDUM

DATE August 25, 1964

SUBJECT SPECIAL SYSTEMS

TO Works Committee

FROM Pat J. Greene

On the average the expenditures for operating the Engineering Systems Department has been approximately $14,000 per month. This of course will vary from month to month depending on the nature of the work we are engaged in. Our development cost for labor averages between $2,000 and $4,000 per month.

From last March to the end of July we have shipped approximately $175,000 worth of systems; the major portion being memory test or associated equipment. Profit margins have been running in excess of 50% on the average.

We have under construction at the moment approximately $225,00 worth of equipment, of which $68,000 is computer systems. For the immediate future (orders to be received within six (6) weeks), I can see relatively firm orders for $350,000 - (29 Indiana Gen., 30 Bell Telephone Laboratories, 90 Toh., 75 Hitachi, 129 Keesler).

Since March we have designed and built the following new machines:

1. 2116 - Core Tester
2. 2117 - Core Tester
3. 2118 - Table Top P.P.G.
4. Equipment for sales demonstrations
5. 1525 Memory Tester (under construction)

The following projects have been completed:

1. Pattern Generator for Memory Tester
2. Solid State Switching for matrix selection memories
3. Thin film tester for evaluation of Toko Radio Coil Memory
4. System grounding standards (improved accuracy of EMI machine from 1 mv to .5 mv)
5. Single Calibrator
6. Rectangular pattern for figure "8" sense windings
7. Dual 30 volt supply for back voltage. (Converted 743)
8. Design of 58 - 68 current drivers

Work is now being done on the following projects:

1. <u>59 - 69 current drivers</u> - Forced personnel shifts create an immediate need for circuit design help here.

2. Sense Amp. - First prototype showed good frequency response, but susceptibility to oscillation and poor common-mode rejection. New design is needed here.

3. Discriminator - Model had few minor problems which are now solved. It will be in production soon. New methods are going to be tried ie, "strobe before slice."

4. Reed Relay Sw. - Final packaging almost complete. Mechanical details present a difficult problem for minimum lead length.

5. Testers have been designed and built for the above.

6. Scope Mounted Cur. Cal.- Mechanical details being worked out.

7. Wave Shape Compensation in Core Handler Heads - Experimental designs have been tried but leave much to be desired.

8. Solid Probe Testing - No success at all.

With regard to the matter of technical publications, I have the following comments:

Application Notes have been faithfully distributed, one each month since their introduction. We keep a backlog of about 3. New specifications and price sheets have been made for all of the core testers and PPG's. Memory Test literature is now being prepared along with product bulletins on the individual components.

Some general comments on the Memory Test business might be of interest. Last March I found out that Minn. Honeywell recommended CTC's equipment to core suppliers. They did not insist that they buy but they strongly urged so if they wanted any M.H. business. RCA Harrison has tentatively announced that they are going to market this type of equipment.

People in this business have predicted that by next spring or summer 75% of all the core business will be 20 mill or smaller. It is my feeling that the present day testers are not adequate for this testing. Mechanical layout is the principal system design problem. Two memory exercisers have bean built for engineering and a third is in the design stages. This is not done on a profit and loss basis.

We have done a lot of customer relations work and now people know that we are in the test equipment business. Our position will be seriously jeopardized however, if we do not get the circuit back-up we need. There are now two (2) graduate engineers, two (2) members of staff, one (1) secretary, one (1) expediter and eight (8) tech. wiremen, two of whom will be returning to school in the fall.

INTEROFFICE MEMORANDUM

DATE 25 August 1964

SUBJECT Brown Bear

TO K. Olsen
H. Anderson
S. Olsen
N. Mazzarese
T. Johnson
J. Shields
J. Ridgeway
K. Larsen
G. Henton

FROM R. Beckman

I thought you might be interested in the attached information about the PDP-5 on the University of Washington's oceanographic ship the Brown Bear.

**

UNIVERSITY OF WASHINGTON
SEATTLE, WASHINGTON 98105

Department of Oceanography

20 August 1964

AIR MAIL

Mr. R. J. Beckman
Manager, Customer Relations
Digital Equipment Corporation
Maynard, Massachusetts

Dear Bob:

As you requested in your letter of 17 August, I enclose a preliminary report from Bill Walker on the operation PDP-5 aboard the Brown Bear.

To save time I had a Verifax copy made of Bill's report from which I deleted much oceanographic details of no interest to you. As you can observe, the computer is working well.

As I mentioned previously to Jack Ridgeway, the software is a little weak; this is understandable at this time, however, I wish you would call his attention to Paragraph 5 of Bill's notes.

The ship is due in on/or about 1 September. I will let you know by wire when the date is confirmed.

Cuthbert and I hope that you can be with us at that time.

Yours sincerely,

Monique

Monique Rona
Senior Programmer

MR:jg

Enclosure (1)

PRELIMINARY REPORT: PDP-5 EVALUATION CRUISE
AUGUST 17, 1964

TO: MONIQUE RONA
FROM: BILL WALKER

1. TOTAL OPERATION TO DATE: 100 HOURS

2. JOHN HAS RUN 22 STATIONS OF SIGMA-T AND INTERPOLATION ON BB 275 WHICH CUTHBERT GAVE HIM. IN ADDITION, ALL OF THE THERMOMETERS HAVE BEEN CORRECTED FOR THIS CRUISE AND ALL SIGMA-T AND INTERPOLATION HAS BEEN DONE FOR THOSE STATIONS WHICH HAVE HAD SALINITIES RUN.

3. I WORKED THERMOMETER DATA ON STATIONS LONG ENOUGH TO REALIZE THAT WE NEEDED A FORMAT HEADING ON EACH DEPTH TO USE THE PRINTER OUTPUT AS A WORK SHEET TO DERIVE ACCEPTED DEPTHS BEFORE INTERPOLATION. IT IS AS FOLLOWS:

L = XXXX METERS

L-Z = XXXX METERS

ACCEPTED DEPTH = XXXX METERS

[redacted]

4. WHEN WE FIRST TRIED TO RUN THE THERMO ROUTINE FOR THIS CRUISE, WE FOUND THAT THE COMPOSITE TAPE WHICH YOU AND JOHN RAN OFF WOULDN'T RUN, SO THAT IS WHEN I BEGAN TO WORK UP A PROGRAM TO PUNCH BINARY TAPES. DUE TO ALL OF THE LOCATIONS OCCUPIED BY THERMO, I HAD TO HAND-LOAD IT IN 7721-7777, SINCE THERE IS NO LOADER AVAILABLE. AFTER A FEW DIFFICULTIES, I GOT A TAPE OUT WHICH CONTAINED THERMO AS IT SHOULD BE. [redacted]

5. THIS LEADS TO ANOTHER DIFFICULTY WHICH I AM OVERCOMING. THE DOCUMENTATION OF DEC PROGRAMS LEAVES A GREAT DEAL TO BE DESIRED, AT LEAST COMPARED TO THE WRITE-UPS WE RECEIVE FROM RCL. THE WORST IS THAT FOR THE FLOATING I/O PACKAGE, BUT "EXPENSIVE ADDING MACHINE" HAS SHOWED ME, ALBEIT RELUCTANTLY, HOW TO USE IT. THE DOCUMENTATION FOR THE FLOATING POINT ARITHMETIC PACKAGE IS BETTER, BUT STILL NOTHING GREAT. IT WOULD APPEAR THAT THESE WRITE-UPS WERE STRICTLY IN-HOUSE ITEMS WHICH HAVE SUBSEQUENTLY BEEN PUBLISHED. THE WORST PART OF THE FLOATING I/O IS THAT THE SYMBOLIC PROGRAM WAS WRITTEN IN "MIDAS", THE ASSEMBLY LANGUAGE FOR PDP-1, AND IT DOESN'T READ EXACTLY LIKE PAL. AT ANY RATE, I THINK I UNDERSTAND IT NOW AND WILL BE USING THESE ROUTINES FROM NOW ON.

6. I WROTE A SHORT (55 INSTRUCTION) PROGRAM IN PAL TO CHECK THE PRINTER, PUNCH, READER, I/O COMMANDS AND AUTO-INDEXING ALL AT ONCE, AND I HAVE LET IT RUN FOR HALF-HOUR PERIODS TO TRY TO WORK THE TELETYPE AS HARD AS I WORKED THE FLEXOWRITER. I WILL CONTINUE THIS ROUTINE WHEN I THINK THAT THE TELETYPE HAS NOT BEEN WORKED HARD ENOUGH.

7. JOHN IS STARTING TO LEARN TO PROGRAM THE MACHINE. AS LONG AS HE WANTS TO KEEP ON WITH IT I WILL HAVE HIM RUN SELF-PERPETUATING PROGRAMS ON THE COMPUTER WHILE HE IS WORKING - JUST TO HAVE IT GOING. THIS DOES NOT MEAN THAT WE WILL LET HIM ON PROCESSING THE DATA FROM THIS CRUISE, BUT IT THINK IT IS BETTER FOR HIM TO LEARN TO PROGRAM THAN TO RUN DATA THROUGH FROM [illegible] 275. HE HAS WORKED VERY WELL ON THIS ROUTINE PROCESSING, DOING MOST OF IT HIMSELF, SO I WOULD LIKE TO GIVE HIM A CHANCE AT THE OTHER END OF THE OPERATION BY DOING SOME OF THE ROUTINE WORK MYSELF.

8. I FOUND THE ENGINE ROOM DOOR OPEN ONE EVENING SO I SHUT ALL THE OTHER DOORS AND THE TEMPERATURE ROSE TO 30.5 CELSIUS. I RAN ALL OF THE MAINTENANCE PROGRAMS WITH MARGINAL CHECKS AND COULD SEE ABSOLUTELY NO DIFFERENCE IN OPERATION FROM THAT IN NORMAL (25-27 CELSIUS) TEMPERATURES. IN ADDITION, WE HAVE BEEN RUNNING AT A SPEED THAT HAS SET UP A 4 CYCLE/SEC VIBRATION IN THE UPPER RACK SUPPORT RIG. THE AMPLITUDE (ATHWARTSHIPS) OF THE VIBRATION IS APPROXIMATELY 1 INCH. THIS HAS HAD NO EFFECT UPON OPERATION. NEEDLESS TO SAY, I AM IMPRESSED.

9. WE COULD CERTAINLY USE THE HIGH-SPEED READER. IT IS NOW HIGHLY IMPRACTICAL TO ATTEMPT TO PROCESS ANY DATA ON STATION WITH THE EXCEPTION OF THE THERMOMETER READINGS DUE TO THE READING TIME FOR THE THERMO PROGRAM. THE FASTER READER WOULD MAKE IT FEASIBLE TO RUN ANYTHING ON STATION AND THEN CRAM THERMO INTO CORE IN ABOUT 1 MINUTE WITH THE FAST READER. ANOTHER DEVICE WE THOUGHT ABOUT WAS A CRT DISPLAY WITH A POLAROID CAMERA ATTACHMENT. THE TUBE WOULD DISPLAY A PLOT OF L-Z AS SOON AS THE LAST THERMOMETER WAS PROCESSED, AND THE PHOTOS WOULD BE USED IN COMPARING STATIONS AND CASTS TO FIND BAD THERMOMETERS. OF COURSE, WE COULD GO TO WHAT WE HAVE DISCUSSED BEFORE, AND USE THE PRINTER. THIS WOULD BE EVEN BETTER IF WE LABELED EACH L-Z POINT WITH THERMOMETER NUMBERS, NANSEN BOTTLE NUMBERS, ETC..

10. THAT'S ALL I CAN THINK OF FOR NOW. IF I REALLY GET BOGGED DOWN IN THE FLOATING I/O AND ARITHMETIC ROUTINES I WILL LET YOU KNOW AT LEAST A WEEK BEFORE WE ARE DUE IN. HOWEVER, I FEEL CONFIDENT THAT I WILL BE ABLE TO TELL YOU BY THURSDAY OR FRIDAY THAT THE AOU PROGRAM IS UP AND RUNNING, AND ALL IS RIGHT WITH THE WORLD. FORGIVE THE WORDY MESSAGE, BUT I THINK THAT YOU WANTED TO KNOW ALL, AND THIS IS IT.

REGARDS,

BILL

INTEROFFICE MEMORANDUM

CONFIDENTIAL

DATE 26 August 1964

SUBJECT PEPR; Status Report

TO H. Anderson, G. Bell, R. Best, J. Fadiman, G. Huewe, R. Lane, K. Larsen, J. Leng, N. Mazzarese

FROM John Allen Jones

In recent months a number of people have worked on a project called PEPR. This report summarizes the information presently at hand on the results to date. Ideas on "where do we go from here" are actively solicited and I plan to talk with each of you in the weeks ahead.

The report looks briefly at the market, the system components, a few key personalities, and some miscellaneous considerations.

24 month market, U. S.

	Requirement for: Controller	Computer
MIT	possible	certain
Yale	certain	probable
Stanford/Berkeley (S/B)	certain	certain

30 month market, Foreign

	Controller	Computer
Cambridge	probable	probable
Oxford	probable	probable
Bonn	probable	probable

Controller proposed by DEC: PEPR-2: to be jointly specified by

Pless,	Taft,	Rosenfeld,	Best
MIT	Yale	S/B	DEC

Computer proposed by DEC: PDP-6 with 5 μsecond memory

Where we stand

CONTROLLER: PEPR-1 designed by Pless, Best and Gurley. Delivered to MIT - January 1963. A non-technical relationship (weak) between MIT and DEC has been maintained on this unit and it's modifications until March 1964.

March 1964 ⟶ present: Discussions of PEPR-2 held between Taft and Best. Plans exist for larger joint meeting in early fall.

Outlook: Best's influence will be felt in development of PEPR-2 specs. Quotes will be requested. There's no reason for our not getting this job, in light of our design role.

COMPUTER: PEPR-1 has been operated since delivery with a PDP-1. The current sentiment is that the PEPR controller is seriously limited by the PDP-1.

Present: A concentrated effort in recent months has been made at the MIT installation to sell PDP-6's for this purpose (including an offer to take Pless's PDP-1 in trade). This effort has been made towards MIT's Pless, S/B's Rosenfeld (assisting at MIT for the last 14 months), and Yale's Taft (a frequent visitor). A letter of intent for a PDP-6 has been received from MIT.

Outlook: A PDP-6 order from MIT.

Taft appears convinced that he'd like a 6. It's not clear that he can get the money.

Rosenfeld is uncommitted: It is not clear that Rosenfeld is the key influence on the S/B decision. In fact, we have recently heard two new names in this connection, Margaret Alston and F. Solmitz. (Ken Larsen, can you help us determine who the influential people are?)

PROGRAMMING: Original PEPR programs done with MACRO by Taft. Little active assistance from DEC. Fortran unavailable, and ill feelings towards DEC's "cooperation" in this area may linger.

Present: Estimate is that at least 6 man years have been invested in PDP-1/PEPR programs.

Outlook: A distinct drag on the switch to 6's will be the need for reprogramming. Some fundamental assistance from DEC in this area may be in order.

We may provide this assistance by delivering a PDP-6 oriented DEC programmer with the system that goes to Brookhaven. His function will be to smooth the system "start-up" using the software we provide.

This will enable Brookhaven to get the most out of our software, and will make clear to outside observers that we are not a "hardware only" company. It will also shorten the feedback loop on bugs in our new PDP-6 programs. We should be ready to commit about 2 months, full time, for this purpose.

We are also considering sending this same man on to Plesse's group at MIT. He would repeat the job that he did for Brookhaven, and also actively assist in the new PEPR programming. This would put us in the position of knowing the program side of PEPR as well as the hardware side; and should be a valuable aid in selling future systems.

If we decide to go this route, an offer will be made to Pless in the next few weeks. We see it as requiring 6 months, full time.

Personalities

Pless, MIT: Received PEPR-1, has placed a letter of intent for a PDP-6. Fully cognizant of DEC's past weaknesses (e.g. software).

Rosenfeld, S/B: Has worked on hardware and programming of MIT's PEPR for last year. In spite of our efforts, he does not seem to have a strong committment to DEC.

Taft, Yale: Holds a high regard for DEC and the PDP-6. Very influential at the University and a key American high energy physicist.

Miller, Argonne, SLAC: A confirmed CDC user. Walked out in the middle of Bob Lane's PDP-6 presentation at Argonne. Moves to SLAC January 1965. Claims he wants no "back room" work on the computer decision (refering to salesman's efforts) "Everything will be done by bid." A tough nut.

Other considerations

The Stanford/Berkeley decision on a PEPR system may be made in the next three months. If this is the case, it will precede the purchase of the control and instrumentation computers for SLAC. The SLAC decision will certainly be influenced by the S/B decision.

This kind of cross influence will also be exerted by McCarthy's ideas on buying a PDP-6. It is probable that all three systems will go to the same manufacturer. The importance of getting the first one cannot be overstated.

Foreign

The foreign market for PEPR systems may be greater than it appears on the surface, but it is not too profitable to speculate past the next 30 months. The prospects listed are the only ones that presently seem reasonable. Undoubtedly more will come to light as we begin active marketing.

The foreign market definitely follows the leadership of key U. S. groups. It appears that the best way to reach these people is to act as a reliable information source on techniques and progress in this country. From the domestic point of view, this means close personal follow-up of our existing installation(s). In Europe we need a man to keep in touch with the status of the many groups who think they might someday want PEPR. As a group becomes "hot" and it's funds come closer to being a reality, we will switch from providing general information on the status of PEPR in the U. S. to very specific information that bears on their requirements.

Thanks for
spotting the error
in TM-701. It
has been corrected
in the Sales Newsletter
and on a second
run. (see attached)

R. Belden

A. Anderson

TM-701

SDS MAGPAK vs DECtape*

MAGPAK (source - SDS Magpak announcement)

Uses standard stereo tape cartridge

Speed - 1,000 characters/second

Capacity - 1.5 million (6 bit plus parity) per channel. Because of space required for inter-record gaps and file marks, the useful capacity is slightly less.

4 Channels (tracks)
1. Library (write protected)
2. Temporary Storage
3. Object Programs
4. Source Programs and Data, or Answers

Scan forward and reverse

Overhead criticisms: plastic stereo cartridge binds, cracks easily, is not standard tape width

DECtape

Speed - 15,000 characters/second
90,000 bits/second

Capacity - 3.0 million bits per reel

Read, Write, Search in forward and reverse directions

Fixed Position Addressing - Units as small as a single word may be placed on tape without disturbing adjacent information.

Pre-Recorded Timing and Track Marks

Redundant Recording

Phase Modulation

High reliability - Tested to 2.7×10^9 bits with no error. Microtape is now being used regularly for rapid I/O on the PDP-6

*DECtape is the recently announced new name for DEC's microtape.

R. Belden
8/26/64

INTEROFFICE MEMORANDUM

DATE August 26, 1964

SUBJECT MAC - PDP-6

TO R. Beckman

FROM R. Lane

Dick Mills called me at home last night to advise me of a paper work delay in Phase II of their purchase. There are no problems but he is leaving on vacation and wanted me to know so we would not be alarmed.

They have approval for Phase I (where we end up owing them 5K) and he will process it immediately. But he will leave the $10,000 error in and correct it with Phase II P.O. He and I will get together upon his return (which is after you install their machine)!

Please acknowledge if this is O.K. and what the MAC delivery status is as of August 28, 1964.

CC: H. Anderson
G. Bell
N. Mazzarese
S. Olsen
T. Whalen

INTEROFFICE MEMORANDUM

DATE 28 August 1964

SUBJECT MAC - PDP-6

TO R. Lane

FROM R. Beckman

Alan Kotok and I talked with Professor Minsky on the twenty-fifth. We told him that we expected to deliver the system by the end of September. He had already been informed of a delay in delivery and was not upset. He mentioned that he would rather not have Professor Fano notified of the delay yet since the space for the computer has not yet been prepared and he, apparently, wants to keep the pressure on for that hoping that the computer in the space will wind up being ready at approximately the same time.

I don't see any real problem on the purchase order situation; we've had more complicated arrangements than this in the past and everything managed to work out in the end.

**

cc: H. Anderson ✓
G. Bell
N. Mazzarese
S. Olsen
T. Whalen

RECEIVED
1964 AUG 28 AM 8:25
DIGITAL EQUIPMENT CORP.
SALES DEPARTMENT

ATTN..... HARLAN ANDERSON
GORDON BELL
BOB SAVELL

GEORGE MICHAEL OF THE RADIATION LABORATORY IN LIVERMORE WILL BE IN THE BOSTON AREA NEXT WEEK AND PLANS TO COME TO THE MAYNARD PLANT NEXT WEDNESDAY SEPTEMBER 2ND, PROBABLY IN THE MORNING. HE WOULD LIKE TO SEE YOU AND ANYONE ELSE WHO CAN GIVE HIM SOME ADDITIONAL INFORMATION ON HIS PDP-6. GEORGE IS STAYING AT THE FENWAY COMMONWEALTH MOTOR INN IN BOSTON.

BETTY SWEDENBORG, PALO ALTO OFFICE

END OR GA PLS

DIGITAL MAYN
@
DIGITAL MAYN

INTEROFFICE MEMORANDUM

SUBJECT: JOB ALLOCATION, MECHANICAL DESIGN DATE: August 28, 1964

TO: All Engineers
K. Olsen
S. Olsen
H. Anderson
W. Hindle
J. Hastings
N. Mazzarese
M. Sandler
J. Smith
R. Maxcy
R. Maroney
K. Peirce
H. Crouse
B. Brackett

FROM: Loren Prentice

To better acquaint all engineers and management with job responsibility within the mechanical design department, a memo will be issued periodically as required.

ENGINEER	JOB NUMBER OR EN NUMBER	DESCRIPTION	% COMPLETE
Loren Prentice	P000000000001	General Engineering, Building Layout	--
	P000000000004	Standards	0.5%
	D000000001304	Component Development	30%
	P000000000008	Security	--
	D000000001291	Mechanical Design for 18-36 Series Modules	40%
	P000000000002	New Test Equipment	Parts ordered
	P000000000036	Mechanical Engineering Adm.	--
	P000000000033	Sheet Metal Shop Adm.	--
	P000000000034	Machine Shop Adm.	--
Dick Clemente	DP000000001304	Component Development	45%
	P000000001158	Automatic safety device for spray etching machine	15%

ENGINEER	JOB NUMBER OR EN NUMBER	DESCRIPTION	% COMPLETE
Scott Miller	D000000001018	Memory Tester Dev.	35%
	D000000001136	Relay Microtape Unit Dev. clean-up	50%
	D000000001301	New A-D Develop., case	25%
	D000000001282	PDP-7	95%
	D000000001243	Drum Development	25%
	D000000001291	Mechanical Design for 18-36 Series Modules	95%
	D000000001292	Linc Development	70%
	D000000001315	PDP-5A Development	25%
	D000000001088	Module Packaging for shipment	OPEN
	S000000000005-8005	Paper Tape Spooler	25%
		Computer Cabinet Design	30%
		Product Identification	OPEN
Ron Cajolet	D000000001178	PDP-6 Development	--
	D000000001236	340 Display Development and prototype	97%
	D000000001209	Display development, general	78%
	D000000001023	Mounting panels	--
	D000000001177	PDP-5 Development	
	D000000001282	PDP-7 Development and Prototype	85%
	D000000001297	PDP-7 Memory Development and Prototype	30%
	D000000001023	Mounting Panels, 1943	60%
	C000000002945	Console push button & light section	99%
	P000000001249	2USEC Memory Development and Prototype	--

ENGINEER	JOB NUMBER OR EN NUMBER	DESCRIPTION	% COMPLETE
Phil Backholm	D000000001249	2USEC Memory Development and Prototype	60%
	P000000001288	Automated Board Production Line	90%
	DP000000001291	Mechanical Design for 18-36 Series Modules	85%
	D000000001026	New Magnetic Tape Development to be used prior to model number designation	50%
	DP000000001023	Mounting Panels, PDP-7	50%
	DP000000001304	Component Development	45%
	D000000001243	New Drum Development	20%
	P000000001196	Vacuum Columns for 570 Tape Transport	60%
	C000000020105	Univ. of Australia (PDP-6)	
Dick Richardson	P000000000033	Sheet Metal Shop Adm.	--
	P000000000034	Machine Shop Adm.	--
Dave Nevala	C000000020104	Brookhaven PDP-6	60%
	C000000020105	University of West Australia PDP-6	90%
	D000000001053	Shock Mtg. Standard Cabinets	80%
	DP000000001136	Relay Microtape Unit Dev. reel holder	75%
Ken FitzGerald	D000000001178	PDP-6 Development	90%
	P000000001288	Automated Board Production	50%

INTEROFFICE MEMORANDUM

DATE August 31, 1964

SUBJECT Univ. of Michigan

TO Bob Oakley

FROM Bob Lane

Dr. Uttal of Michigan called on 8-28-64 and requested the presentation which I had offered him some time ago. He wants all literature on PDP-6 and especially firm price quotes. He also wants as part of our proposal a guarantee that time sharing will work.

The date scheduled for the presentation is 9-11-64 subject to your approval and schedule. Please RSVP immediately and get me an advance list of attendees so we can mail them F-65 and other pertinent documentation. Let's really show an advanced front and give them an excellent presentation.

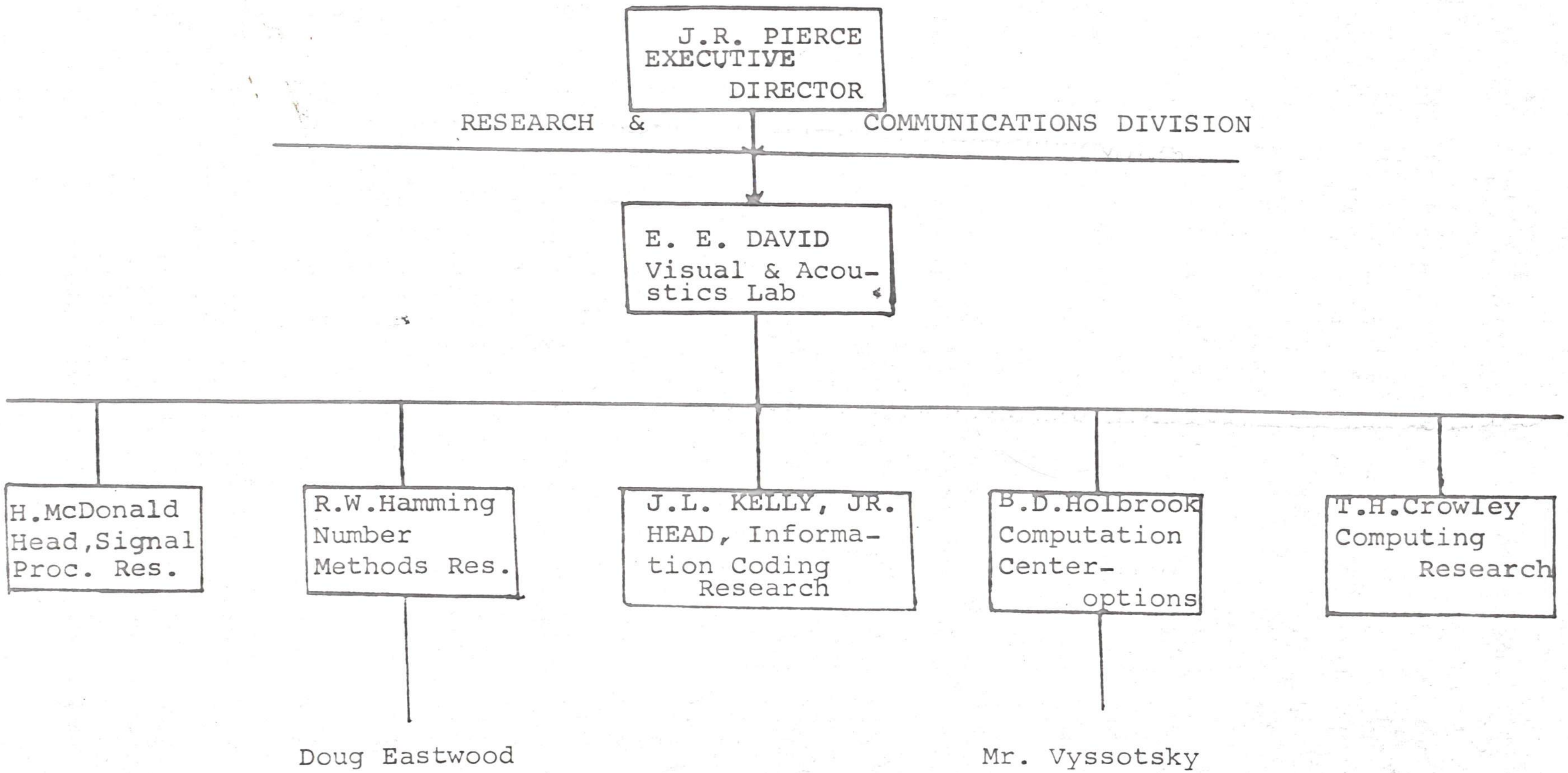
Since much of their work will require special I/O devices and a presentation on the I/O Bus, I will ask A. Kotok to assist. He does an excellent job at this. Also, he knows all the right "Time Sharing Words". We really want to go all out on this.

CC: G. Bell
H. Anderson
N. Mazzarese
T. Johnson
A. Kotok

H. Anderson

ORGANIZATIONAL CHART

Bell Telephone Laboratories, Inc.
Murray Hill, N.J.



D.B. Denniston, NYO
September 1, 1964

R. E. Vernon
August 31, 1964

ENGINEERING PROJECT SCHEDULING SYSTEM

The Project Scheduling System is an engineering planning guide with an automated updating feature. The purpose of the system is to coordinate the engineering effort, both internally and with the various service departments of the Company.

Specifically, the system wil -

A. Serve as a planning guide to the enginmer by helping him to coordinate the various activities within his project.

B. Provide the Chief Engineer with up to date information concerning the projected utilization of engineering manpower.

C. Provide other departments such as Drafting, upon whose services engineering depends, with up to date forecasts of workload requirements.

D. Provide a basis for estimating the engineering budget.

The Scheduling System consists of -

1. A graphical schedule for each project.
2. A program for updating the schedules.
3. A series of computer-generated reports which indicate the latest revision of the project manpower requirements.

The schedule format is similar to that used by the EXPERT system.[1] The engineer is asked to layout on a calendar scale all activities associated with the project, including such non-

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[1]as described in "The EXPERT Approach to Program Control" by Irving C. Zacher, Military Systems Design, Volume 7, No. 5, October, 1963. pp. 26,29.

engineering activities as the preparation of programs and publications. Figure 1 illustrates a hypothetical project schedule.[2] Experience has shown that graphically laying out a project at an early stage aids the engineer in coordinating the various phases of the project and in meeting delivery date requirements. Potential bottlenecks, such as those caused by the failure to order long-lead components at an early enough date, can often be foreseen and thus avoided by scheduling in advance.

Shown on the schedule are estimates of the manpower required for each phase of the project; included in these estimates are the engineering, technician, drafting, production, and publications requirements. From the estimates, manpower loading forecasts, which are updated periodically, are derived.

These summarized estimates provide the Chief Engineer with information regarding the availability of his technical manpower for work on future projects. The service areas are provided with advance notice of the work load requirements for each project and of the approximate dates that the work will be expected.

Experience has indicated that a given service department can effectively schedule its work if it receives advanced notice of that work's arrival in the department; the Scheduling System provides this information.

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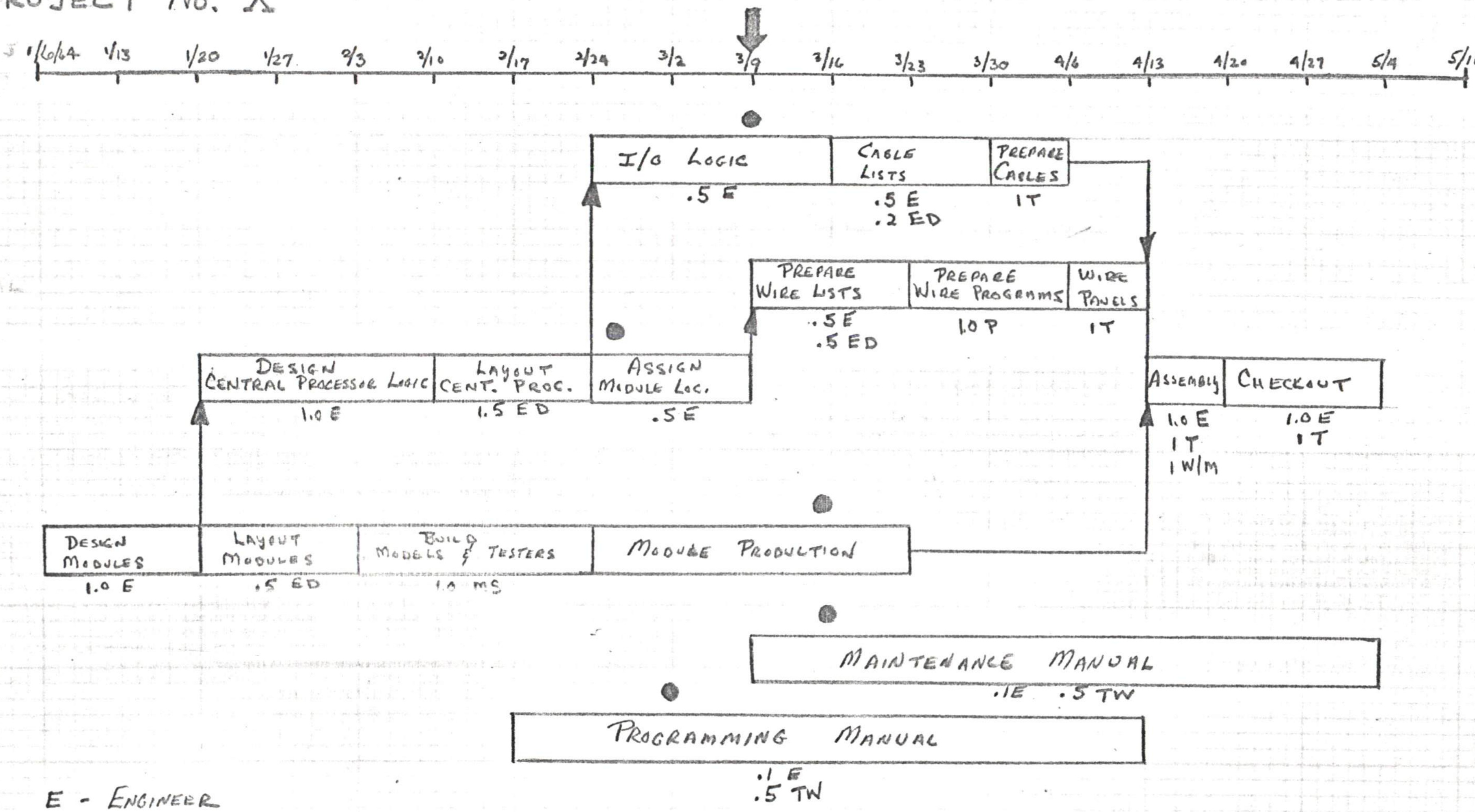
[2] The arrows indicate that a given activity may not be started until certain other activities are completed.

PROJECT NO. X



E - ENGINEER
ED - ELECTRICAL DRAFTSMAN
MS - MODEL SHOP
T - TECHNICIAN
TW - TECHNICAL WRITER
P - PROGRAMMER

⇩ PRESENT DATE MARKER

● ACTIVITY STATUS MARKER

FIGURE I.

The project schedules also provide a quantitative basis for estimating the labor portion of the engineering budget. By applying standard costs to the manpower estimates indicated on the schedule, realistic budgets estimates may be obtained. This technique, as well as aiding managerial planning, tends to give the project engineer a greater appreciation for the costs involved in new product development.

The information required for updating a schedule is the present date and the status of each current activity (as shown by the markers on Figure 1.). This information serves as the input data for a FORTRAN Scheduling Updating Program which operates on a PDP-4 Computer with an 8K memory.

The program acts upon the current status information and, in effect, slides the project activities forward or backward through time, arriving at revised estimates of the starting and completion dates of each activity. In addition, the program re-totals the manpower requirements and prints a revised manpower load report for each service area. Sample output is illustrated in Figure 2.

The system has been designed with the engineer's aversion to "red tape" in mind. Having originally prepared the schedule, not an ominous task, the engineer need only indicate periodically the current status of the project. Up to date reports are issued without his having to re-do the entire schedule.

The system design outlined herein has been completed. Almost all of the current production and development projects have been scheduled by the project engineers. Graphical schedules are now being adapted for computer operation; full-scale operation is imminent.

UPDATING PROGRAM FOR PROJECT NUMBER 1157

PROJECT NUMBER " 1157. PRESENT PERIOD " 5

REVISED SCHEDULE OF UNCOMPLETED ACTIVITIES

ACTIVITY	STARTING DATE	ENDING DATE
1	10	10
2	10	11
3	12	12
4	13	13
5	12	12
6	10	11
7	14	14
8	15	15
9	16	23
10	24	27
11	28	31
12	32	33
13	34	37
14	38	39

MANPOWER LOADS (MULTIPLIED BY TEN) ARE GIVEN FOR EACH HALF-WEEK PERIOD FOR WHICH THE LOAD IS GREATER THAN ZERO.

ELECTRICAL DRAFTING LOAD SUMMARY

PERIOD	MANPOWER REQUIREMENT
34	1
35	1
36	1
37	1

TOTAL MANPOWER LOAD " 2 MAN-WEEKS.

ENGINEERING MANPOWER SUMMARY

PERIOD	MANPOWER REQUIREMENT
10	10
11	10
12	10
13	10
14	10
15	10
24	10
25	10
26	10
27	10
32	10
33	10

TOTAL MANPOWER LOAD " 60 MAN-WEEKS.

TECHNICIAN MANPOWER SUMMARY

10	10
11	10
12	10
14	10
24	10
25	10
26	10
27	10
32	10
33	10
34	10
35	10
36	10
37	10
38	5
39	5

TOTAL MANPOWER LOAD " 75 MAN-WEEKS.

PROGRAMMING MANPOWER SUMMARY

PERIOD	MANPOWER REQUIREMENT
16	1
17	1
18	1
19	1
20	1
21	1
22	1
23	1
28	10
29	10
30	10
31	10

TOTAL MANPOWER LOAD " 24 MAN-WEEKS.

PROPOSED TIME AND COST SCHEDULE: ADA DEPARTMENT 9-1-64 to 7-1-65

A. WORK TO BE ACCOMPLISHED:

1. Modules; (Flip Chip)
   - 1.1 Develop sample and hold module (s)
   - 1.2 Develop multiplexer switch
   - 1.3 Test ADA modules to determine operational parameters and environmental specifications

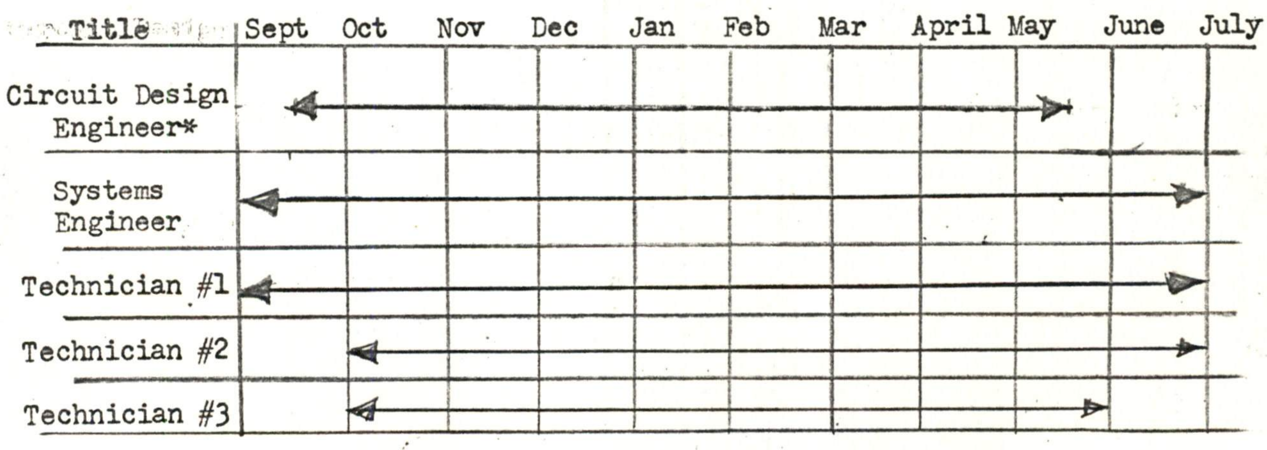
2. Systems (Using Flip Chip modules)
   - 2.1 Develop standard DAC's (8, 10, 12 & 14 bits) with standard interface.
   - 2.2 Develop standard ADC's (8, 10, 12, 13 & 14 bits) with standard interface defined; to include multiplexer and sample and hold circuitry.
   - 2.3 Test new ADA systems to determine operational parameters and environmental specifications.

B. MANPOWER REQUIRED:

1. Engineers (14 man months)
   - 1.1 Sytems Engineer :(10 man months)
     - 1.1.1 Schedule, specify, co-ordinate system/ circuit development.
     - 1.1.2 Propose to and consult with customers regarding special problems.
     - 1.1.3 Provide production with necessary engineering support.
     - 1.1.4 Support sales in specifying O.E.M. ADA equipment.
   - 1.2 Circuit Design Engineer (4 man months)
     - 1.2.1 Develop necessary circuitry to complete Digital's ADA line.
     - 1.2.2 Generate specifications for circuits developed.

2. Technicians (27 man months)
   - 2.1 Systems check out
   - 2.2 Gather systems/ circuit evaluation data.
   - 2.3 Build models and prototypes.
   - 2.4 Assist in expediting rush items.
   - 2.5 Assist in gathering specifications and sources of O.E.M. equipment.

3. Manpower Schedule



* 50% of Design Engineer's time is devoted to this project.

4. Funds Necessary To Support Schedule

Engineering - 14 man months @ $2000 / month	$28,000.
Technicians - 27 man months @ $1000 / month	$27,000.
Materials	$10,000.
Total (9-15-64 to 7-1-65)	$65,000.

C. SCHEDULE FOR NEW ADA LINE

The new ADA line will be offerred as the system components are developed. The line will be complete by April of 1965. Refer to the attached chart for a more complete breakdown.

SCHEDULE FOR NEW ADA LINE