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November 12, 1959

Mr. Harlan E. Anderson
EJCC Publication Committee
Digital Equipment Corporation
Maynard, Massachusetts

Dear Mr. Anderson:

Enclosed you will find four complete copies of the manuscript of a paper "Deposited Magnetic Films as Logic Elements" by A. Franck, G. F. Marette and B. I. Parsegyan, which will be presented by myself at the EJCC in Boston. This paper is submitted on a company proprietary basis and we wish to advise that it should not be used for any other purpose except your review for publication.

We are submitting a set of drawings on vellum untitled, as required. Included with the paper are ozalid copies of these drawings with the appropriate titles attached thereon. We assume that you will entitle the drawings for the paper according to your own specifications.

As requested by you, a representative, either one of the co-authors or myself, will report to the Publication Committee room at the Hotel Statler to concern himself with reading and checking of the material which we are submitting regarding any possible changes or additions with respect to the questions and answers raised at the conference.

I am also enclosing an autobiography of my experience as requested.

With anticipation to participating in the 1959 EJCC, speaking for the authors and myself, I wish to thank you for the consideration and interest that has been given us by the committee on this conference.

Sincerely,

REMINGTON RAND UNIVAC

A. Franck

A. Franck, Manager
Mathematics and Logic Research

AF/dn
Enc.

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DEPOSITED MAGNETIC FILMS AS LOGIC ELEMENTS

By

A. Franck*, G. F. Marette* and B. I. Parsegyan*

SUMMARY

Because of their small size, high switching speeds, and versatile logical properties, vacuum-deposited magnetic film cores offer many advantages in computer applications. They are best known as storage elements in memory arrays. This paper is concerned with the use of these films as logic elements in various modes of operation. Two modes of film-core operation are explained as they pertain to a particular circuit. Also explained are certain principles of array logic. These principles involve writing multiple copies of a word in a film-core array. Then, by the proper arrangement and selection of sense lines linking parts of these copies, some desired result is obtained from the array. This approach makes it possible to perform in one or two clock periods operations that have previously required many clock periods.

These principles are illustrated by a scale-factoring device whose function is to find the most significant digit in a binary word, shift that word to the left until the most significant digit is in a position immediately to the right of the position reserved for the sign bit, and record the number of places shifted

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in an auxiliary register. The methods and advantages of accomplishing these operations with deposited magnetic film-cores are given in detail in the paper.

I. INTRODUCTION

The use of thin magnetic films as storage elements is well known. Several papers on the subject have appeared in the literature, particularly in recent years[1]. Less emphasized, perhaps, is the use of magnetic films as logic elements. The authors' study of this problem has revealed that film elements are both flexible and versatile as logical devices. In some of the subsystem designs investigated, where comparisons between film-element logic and its conventional counterparts were made, definite reductions in both the required number of semiconductor components and the operating time were observed. For instance, throughout all of the designs the use of separate NOT elements was easily avoided by appropriate wiring and biasing of film cores. Use of separate OR elements may also be eliminated by appropriate wiring between film elements. This principle and the component savings it produces are illustrated by the encoder that is described in this paper (as part of the scale-factoring device). By interconnecting film elements to form functional logic arrays (such as

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1. A list of references on this subject appears in an article by A. J. Kolk and J. T. Doherty, "Thin Magnetic Films for Computer Applications," Datamation, vol. 5, pp. 8-12; September/October, 1959.

the shift matrix described below) great gains in speed of entire sequences may often be realized. These logic advantages--together with such properties as small size, high reliability, low power requirements, relative insensitivity to environment, and low cost--make magnetic film elements very desirable as logic devices.

II. LOGICAL PROPERTIES OF FILM ELEMENTS

This section introduces those logical properties of film elements that are used in the scale-factoring device. Specifically, these four ways of using the logical properties of film elements are described:

a. AND logic using the reversible rotation mode of operation;

b. AND logic using the saturable-transformer mode of operation;

c. Inverter logic using the saturable transformer mode of operation;

d. Functional array logic.

a. "And" Logic (Reversible-Rotation Mode). Figure 1 illustrates a method of obtaining AND logic using a film element in the reversible-rotation mode of operation. If inputs to such a film element are x and y, respectively, then the output is xy, as shown.

The "0" state of the film core, represented by the magnetization vector M_0, is made to correspond to the remanant state of the

film core, M_R. A bias field, H_B, transverse to M_O, corresponding to the logical input x, rotates the vector M_O through an angle to a position shown as M_1. Subsequent application of a drive field, H_D, corresponding to a logical input y, in a direction antiparallel to the vector M_O, further rotates the vector M_1, altering the state of the film core to M_1'. (In the reversible rotation mode of operation, application of bias field H_B and drive field H_D is time-sequenced so that the biasing precedes the driving.) Change of the magnetization of the film core from state M_1 to M_1' induces a voltage on the sense line, corresponding to a logical output of "1". No output is obtained unless both the bias field H_B and the drive field H_D are present, as illustrated by the vector diagrams in Figure 1. Logically, then, the output xy is "1", only, and only if, inputs x and y are both "1".

b. AND Logic (Saturable-Transformer Mode). Figure 2 illustrates a method of obtaining AND logic using the film core as a saturable transformer. In this mode of operation, the film core is initially biased to one of its remanant states of magnetization in the hard direction. Its state is then caused to change or not to change in a direction of high permeability, depending upon certain control conditions.

Figure 2 shows the film core as initially biased to the P_2 state. (Means of effecting this initial bias are not shown in the figure.) A bias field H_B, corresponding to logical input x, further biases the film core to state P_1. Application of a drive field H_D, corresponding to logical input y, then causes a change

in the state of the film core. This change is in the steep region of the B-H diagram, so that an output voltage is induced in the sense line. This voltage corresponds to a logical output of "x AND y". A "1" output is obtained only, and only if, the bias field H_B and the drive field H_D are both present.

c. Inverter Logic (Saturable-Transformer Mode). Figure 3 shows a simple method of obtaining logical inversion (i.e. negation) using a film core in the saturable transformer mode of operation. The film core shown in the figure is initially biased to the P_1 state. (Means of effecting this bias are not shown in the figure.) A bias field H_B, corresponding to logical input x, biases the film to the P_2 state. Application of a drive field H_D, in a direction opposite to the bias field, then merely biases the film core toward P_1. It is, however, not of sufficient strength to drive the film core into the steep portion of the B-H curve. Consequently no voltage is induced on the sense winding; this corresponds to a "NOT x" logical output. If, on the other hand, the bias field H_B were absent, meaning a "NOT x" input, the film core would remain in its original biased state at P_1. Application of a drive field H_D would then induce a voltage on the sense winding which would correspond to output x.

d. Functional-Array Logic. A very powerful feature of magnetic film elements is their adaptability to a technique of logic described as functional-array logic. Use of this technique

results in a great saving in time for many operations that may be sequential in nature. An example of a sequential operation is a shifting operation where the total time to shift a number is dependent upon the number of shifts required. The accomplishment of shifting by functional-array logic is explained in detail in this paper. In general functional-array logic may be thought of as an arrangement of information in an array based upon an input word or bit configuration for the purpose of accomplishing a specific logical operation in one step.

In the preceding sections on the saturable-transformer and reversible-rotation modes of operation, the logic of the individual films was presented. Because of their size, it is possible to assemble these film elements in compact arrays and to bias and drive many film elements simultaneously without appreciable time delays or power losses. One such arrangement is illustrated in Figure 4, which is an example extracted from one of the arrays to be presented in a later section.

The function of this array is to sense for an information bit in a position within the input word. The input word is contained in the input register R, and each of the bias generators (B_0-B_4) supplies a bias field to the film element below it if the corresponding input-register stage (R_0-R_4, respectively) contains a "1". This bias field rotates the magnetic vector to the "1" position as indicated in Figure 4(a). If a drive field H_{Di} is applied to a film core thus rotated, an output is induced on a sense line linking that film core.

If driver D_0 is energized after the array is biased, and there is a "1" in input register-stage R_4, an output is obtained on the sense-line X. This simple arrangement could be used as a sign test. The other drivers, D_1-D_4, could also be initiated singly to determine whether input register stages R_3-R_0, respectively, contain binary "1"s. Another way of using the same functional array depends on initiating all drivers simultaneously so that a "0" output indicates that the input word is all "0"s. Various effects can be produced with functional arrays by varying the wiring of the sense, drive, and bias lines. Applications of two of these effects are discussed in Section IV.

III. CIRCUIT FUNCTIONS

The logical operation that will be described to illustrate the utilization of magnetic film elements is that of scale factoring of a data word. In certain number representations this operation is also referred to as "normalizing a number". In both scale factoring and normalizing, a binary word is examined to determine the location of its most significant information bit. The entire word is shifted until this bit is in the highest order non-sign position, and the amount of this shift is stored in an auxiliary register. If the word is given in a complement representation, such as one's or two's complement, the operation is referred to as the process of scale factoring. On the other hand, if the word is represented in the sign and magnitude form, the operation

is referred to as normalizing.

For the purposes of this description the one's complement representation is used. It follows that the leftmost bit of a binary word is the sign bit; "1" for negative numbers and "0" for positive numbers. Therefore the most significant information bit is the leftmost "0" for negative numbers and the leftmost "1" for positive numbers.

IV. CIRCUIT DESCRIPTIONS

The scale-factoring operation consists of three separate operations that are first treated separately in the description that follows and then integrated into one unit in the last portion. The three operations and the order in which they are presented are as follows:

a. Location of highest-order information bit.

b. Shifting.

c. Encoding the amount of shift.

a. Location of Highest-Order Information Bit. In conventional logic circuits, the process of determining the location of the highest significant information bit of a binary word is a time-consuming operation. The method normally used depends on shifting the binary word one position at a time in the direction of most significance. After each shifting operation, a check is made for a difference between the sign bit and the bit occupying the most significant position. If the bits are alike, the word

is shifted again and the check repeated. The first time that the bits are found to be unlike, the word is in its proper position. The amount of shift that has been accomplished is then read from a counter that has been counting the number of shifts. The number of sequential steps and therefore the time for this operation can be large, especially where the word size is large and the highest order information bit appears in one of the lower order positions.

In the preliminary section on functional-array logic, it is shown that logical operations could be performed using functional arrays. An array of this type is illustrated in Figure 5; its function is to determine the most significant information bit in the word "00010". The word is arranged in a 5x5 bit array such that one row contains a negative copy of the word and four rows contain positive copies of the word. Sense lines S_0-S_3 are arranged in such a manner that they couple one bit in the negative row and one bit in each column to the left of that position. The figure shows that one and only one sense line may link bits that are all in the "0" state and that this sense line has a direct relationship to the location of the most significant information bit. The sense lines to the left of this position will always link a bit in the "1" state because of the negative row, and the sense lines to the right will always link a bit in the "1" state because of the column immediately below the highest-order "0" in the negative row. In the example of Figure 5, sense line S_2 is the only sense line

linking bits that are all in the "0" state. This condition dictates that a shift of two positions is required to properly scale the number "00010". If the number had been "001XX", it could be shown by similar means that sense line S_1 would be the only one linking bits all in the zero state, and the corresponding scaling shift would be one.

A method of implementing this logic with film elements is illustrated in Figure 6. The number to be scaled is located in the input register, stages R_0-R_4. If any stage of the input register contains a binary "1", it will initiate one of the corresponding bias generators B_0-B_4. The function of the bias generators is to supply a field transverse to the remanant state of the films linked by its output line. This field is represented by vectors $H_B(1)$ in Figures 6(a) and 6(b). After the films in the array have been appropriately biased by the bias generators B_0-B_4 and B_p, the action of which will be explained later, the film elements are driven by drive generator D. This driver links all films in the array and supplies a field that is antiparallel to the remanant state of the film cores, but not of sufficient magnitude to completely switch the film core with no other applied fields. This field is identified by vectors H_D in Figures 6(a) and 6(b).

Referring to Figures 6(a) and 6(b), the effects of the bias and drive fields are shown for the various rows of films in the array. A permanent bias field---represented by vector H_{Bp} in

Figure 6(a)---is applied to all film elements in the first or negative row of films, where it is desired that a negative copy of the word be represented. This field has the effect of rotating the magnetic state vector away from the remanant direction of magnetization so that, without the application of another biasing field by one of the bias generators B_0-B_4, an output would be obtained on sense lines linking these film elements when drive field H_D is applied. If a field is applied by one of the bias generators, the magnetic state vector is rotated back into alignment with the remanant direction, so that no output is produced on sense lines linking these film elements when drive field H_D is applied. Therefore, in the first row, (1) no output is obtained on any sense line that links a biased film element if there is a "1" in the corresponding input register, and (2) an output is obtained if there is a "0" in the input register. Thus the action of the permanent bias generator B_p produces a negative copy of the input word in the first row. Examination of Figure 6(b) for the remaining rows shows that the converse conditions apply; i.e. a "0" output is obtained on a sense line linking a film element associated with a register containing a "0", and a "1" output is obtained on a sense line linking a film element associated with a register containing a "1".

The array of Figure 6 is arranged in the manner described in the example of Figure 5. A signal to indicate the amount of shift required is obtained by the use of inverters that terminate each sense line. Since only one sense line will have zero signal induced on it, only one inverter will have an output signal. Because a zero or null signal is used to the inverters, the inverters are necessarily gated as indicated in Figure 6.

b. Shifting. For shifting operations, it is also desirable to be able to shift a word an arbitrary number of positions in a time not dependent upon the number of positions shifted. Here again functional arrays are readily applicable. An array for accomplishing the left-shifting of a word two positions is illustrated in Figure 7. As in the example of Figure 5, the word "00010" is used. Five copies of the word are represented in the array, and sense lines are diagonally drawn through the array as shown in Figure 7.

Shifting in this array is accomplished by transferring a selected row of bits via the sense lines to the output register. In the example of Figure 7, an open-ended left shift of two is obtained by selecting the third row and transferring the bits via sense lines S_2, S_3, and S_4 to the output register. Similarly, other shifts can be obtained from the same array by selecting other rows. If, for example, row 1 is selected, a shift of zero is obtained; if row 5 is selected, a shift of four is obtained.

The circuit of Figure 8 illustrates a film-element array for the execution of left shifts. The word to be shifted is originally in the input register R_0-R_4, and bias generators B_0-B_4 are initiated if there is a "1" in the corresponding input register. The bias generators supply a field transverse to the remanant magnetization direction. This field rotates the magnetic state vector in each film element away from the remanant direction so that a drive pulse applied antiparallel to the remanant direction produces an output on a sense line linking that film element. The bias field is represented by vector $H_B(1)$ in Figure 8(a), and the drive field is represented by vector H_{Di}. To implement a shift of from zero to four in this array, one of the shift drivers, D_0 to D_4, respectively, is initiated, and the corresponding row of films is supplied with a drive or interrogation pulse. The sense lines linking the film elements in the interrogated row will have an output signal only where the film element linked is initially biased away from the remanant state. These sense-line signals are coupled to the stages of the output register and the resulting word is in its shifted position.

c. Encoding. In Section IV(a) the amount of shift was determined by locating the position of the most significant bit in a word. This shift count appeared as a unique signal on one of the lines D_0-D_3, as shown in Figure 6. In many applications

it is desirable to store this signal as a binary number. This requires a "one-to-many" translation. An encoder is a device for accomplishing this result.

Physically, a signal representing the number is applied to the encoder input. The output from the encoder then appears as one or more signals, corresponding to the respective "1" bits of the binary representation of the given number. For example, the number "13" would be encoded as "1101" with signals from the output of the encoder setting corresponding stages 3, 2 and 0 of a four-bit encoder register.

Figure 9 shows a three-bit magnetic film encoder with its associated register. Inputs to the encoder are shown as D_1, D_2, D_3 and D_4, corresponding to shift counts of 1, 2, 3 and 4, respectively. (Note that only one of these inputs is active at any given time.) The output from the encoder appears in the scale-factor shift-count register, stages K_2, K_1, K_0. Film elements F_0, F_1 and F_2 act as AND gates operating in the saturable-transformer mode, as described in Section II(b). All three film cores are initially biased to the P_2 state. The input lines are so wired that lines D_1, D_2 and D_4 link film elements F_0, F_1 and F_2, respectively, while line D_3 links both film elements F_0 and F_1. A field H_{Di}, corresponding to a D_i input, biases the film element (or elements) that it links to the P_1 state. The drive generator D_s subsequently supplies a drive field H_{Ds} to all the films. Any film element that is in the P_1 state therefore produces an output signal on its respective sense line. This

output then sets the corresponding scale-factor shift-count register stage to "1".

In the example used to illustrate the scale-factoring operation, where the shift count was 2, a field H_{D2}, corresponding to input D_2, biases the film element F_1 to the P_1 state. Subsequent application of drive field H_{Ds} then produces an output on the sense line of film element F_1, and thereby sets scale-factor shift-count register stage K_1 to "1". Film elements F_0 and F_2 do not have outputs because their states are unaltered, having remained at P_2. Consequently, the scale-factor shift-count register reads "010", which is the binary representation of 2.

V. COMBINED CIRCUIT OPERATION

a. Circuit Operation. Figure 10 is a composite drawing incorporating the circuit for determining the highest order information bit with the circuit required for shifting. Since both of these arrays utilize the same mode of operation, namely, reversible rotation, it is possible to combine them in the same array and use the same bias generators. Inspection of Figures 6 and 8 reveals that certain film elements in each array are not used in the performance of the logic operation. These unused film elements are not included in the combined array of Figure 10.

The operation of the circuit is divided into two major sequences: determination of the highest order information bit, and the shifting operation, with the encoding being accomplished during the shifting operation. After the array has been biased,

the first sequence is initiated by Driver D, which supplies a drive field to the film elements the highest-order information-bit-determination portion of the array. These film elements are linked by sense lines S_1-S_4. These sense lines are coupled to the shift driver inverters D_0-D_3. Since a zero output on one of the sense lines is the required signal to the shift driver inverter, these drivers must necessarily be gated. The output of drivers D_0-D_3 is used to drive the film elements in the shift array and encoding network. The operation of the shift and encoding circuits is as described in Section IV.

In the example of Figure 5, a positive number is used for illustration. If the same approach is applied to a negative number, i.e., the complement in the first row and the number itself in the remaining rows, there is not a unique method of determining the location of the highest order information bit. If, however, the negative number itself is placed in the first row and its complement, or the positive copy, in the remaining rows, the previous rules apply. It follows that some form of gating between the input register stages and the bias generators is necessary. Similarly, since the information in the shift array is in its complement form for negative numbers, some form of gating between the shift array and the output register is necessary. The conditional complementer circuits shown within the dotted line enclosures of Figure 10 accomplish these gating functions.

If the number originally in the input register is negative, R_4 is "1", and the R or negative generator drives the row of P_1

saturable-transformer film elements in both conditional-complementer networks. These P_1 film elements act as AND inverters (i.e., Sheffer stroke function) in both networks and complement the information supplied to the bias generators for the array and again recomplement the information from the array for the proper output representation. If the number in the input register is positive, R_4 is "0", and the $\overline{R}$ or positive generator drives the P_2 row of film elements in the conditional-complementer networks. These film elements are AND gates and allow the information to be transferred directly to the bias generators and output circuits.

The encoding network shown in Figure 9 serves in conjunction with the scale-factoring network of Figure 10. The outputs of shift driver inverters D_1-D_3, which drive the shift array, are also used as the inputs to the encoding network. In this manner the amount of the shift performed is recorded in the shift count register at the same time that the shifted number is entered into the output register.

b. Circuit Timing. A detailed timing sequence for the scale-factor operation is presented in Table I. Included in the table are approximate expressions that might be used to determine execution times on the basis of word length and other circuit parameters. The parameters used are defined as follows:

M = word size in bits

T = transistor rise time

f = film, drive, bias, and sense line transmission time

R = rise time of film element in saturable transformer mode

From Table I the approximate expression for the execution time of the scale-factor operation is

$$\text{max time} = 4T + (4M + 5)f + 2R$$

Assuming a transistor rise time $T = 5$ mμsec, film-element transmission time $f = 0.12$ mμsec, film-element rise time $R = 1$ mμsec, and a word size $M = 36$ bits, the maximum shift time for the scale factor operation would be 39.9 mμsec.

c. Circuit Components. The components required for the scale-factor operation exclusive of the component requirements for the design of the input register and the encoder are as follows:

1. Film elements

$$\text{Input} = 2M$$
$$\text{Output} = 2M$$
$$\text{Matrix} = M^2 + M - 2$$
$$\text{Total} = M^2 + 5M - 2$$

2. Transistors

$$\text{Bias Generators} = M + 1$$
$$\text{Inverter Drivers} = M - 1$$
$$\bar{R} \text{ \& } R \text{ Generators} = 2$$
$$\text{Amplifiers} = M$$
$$\text{Total} = 3M + 2$$

Table II presents the film-element and transistor requirements for encoders of various sizes. For comparison purposes, the number of diodes that would be required for conventional encoders of equivalent size are shown. The input and output components are omitted for both types of encoders.

Since film elements, unlike diode elements, permit the use of more than one input per element, the film-element encoder uses very few film-elements in comparison with the number of diodes in a diode encoder. Furthermore, the only semiconductor devices required are one transistor for each output bit. The number of diodes required for the larger diode encoders would be greater because of the diode OR circuit input limitation. For these encoders the diodes would probably be arranged in a "tree" or "pyramid" configuration, which would result in an increased time requirement for the diode encoder. Without the "pyramid" arrangement, the times for the two encoders are approximately equal.

VI. OTHER APPLICATIONS

The illustration given in this paper utilizes a five-bit word in the one's complement number representation. The method applied, however, is not restricted to this representation, this word size or the particular application which has been described. With minor modifications the device can be adapted to any complement, sign and magnitude, or binary-coded number representation. Devices to perform such operations as locating the least significant information

digit and shifting the word accordingly, or locating a predetermined information digit within a certain field or portion of a word can also be readily designed.

Although this paper is concerned primarily with the application of film-element logic and the design of a specific logical device, the techniques described have a much wider range of applicability. The authors have investigated and designed a variety of logical devices such as decoders, counters, accumulators, and special-purpose devices.

ACKNOWLEDGEMENT

For consultation on the physical properties of magnetic film elements the authors are indebted to members of the Physics Department of Remington Rand Univac (St. Paul), especially Dr. A. V. Pohm[2] and Dr. R. M. Sanders.

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2. Now on the staff of the Department of Electrical Engineering, Iowa State University, Ames, Iowa.

TABLE I

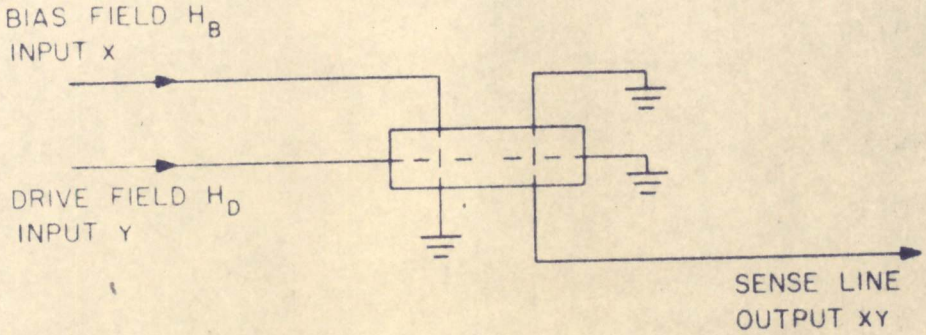
SCALE-FACTOR TIMING SEQUENCE

Test sign				
+	-			
Initiate $\overline{R}$ Generator (T)	Initiate R Generator (T)			
Transmission time (Mf)		Initiate input transfer		
		Conditional complementer Drive transmission time (2f) Film element rise time (R)		
		Initiate bias generators (T)		
		Bias transmission time (Mf + f)	Initiate scale-factor driver (T)	
			Drive- and sense-transmission time (Mf)	
			Initiate inverter driver (T)	
			Drive- and sense-transmission time (Mf)	Encoder bias transmission time (maximum) (Mf)
			Amplifier (T)	Initiate read driver (T)
			Conditional complementer Drive transmission time (2f) Film-element rise time (R)	Drive and sense transmission

TABLE II

ENCODER COMPONENT REQUIREMENTS

Output Word Size (In Bits)	Film-Element Encoders		Diode Encoders
	Film Elements Required	Sensing Transistors Required	Diodes Required
2	2	2	4
3	3	3	12
4	8	4	32
5	20	5	80
6	48	6	192



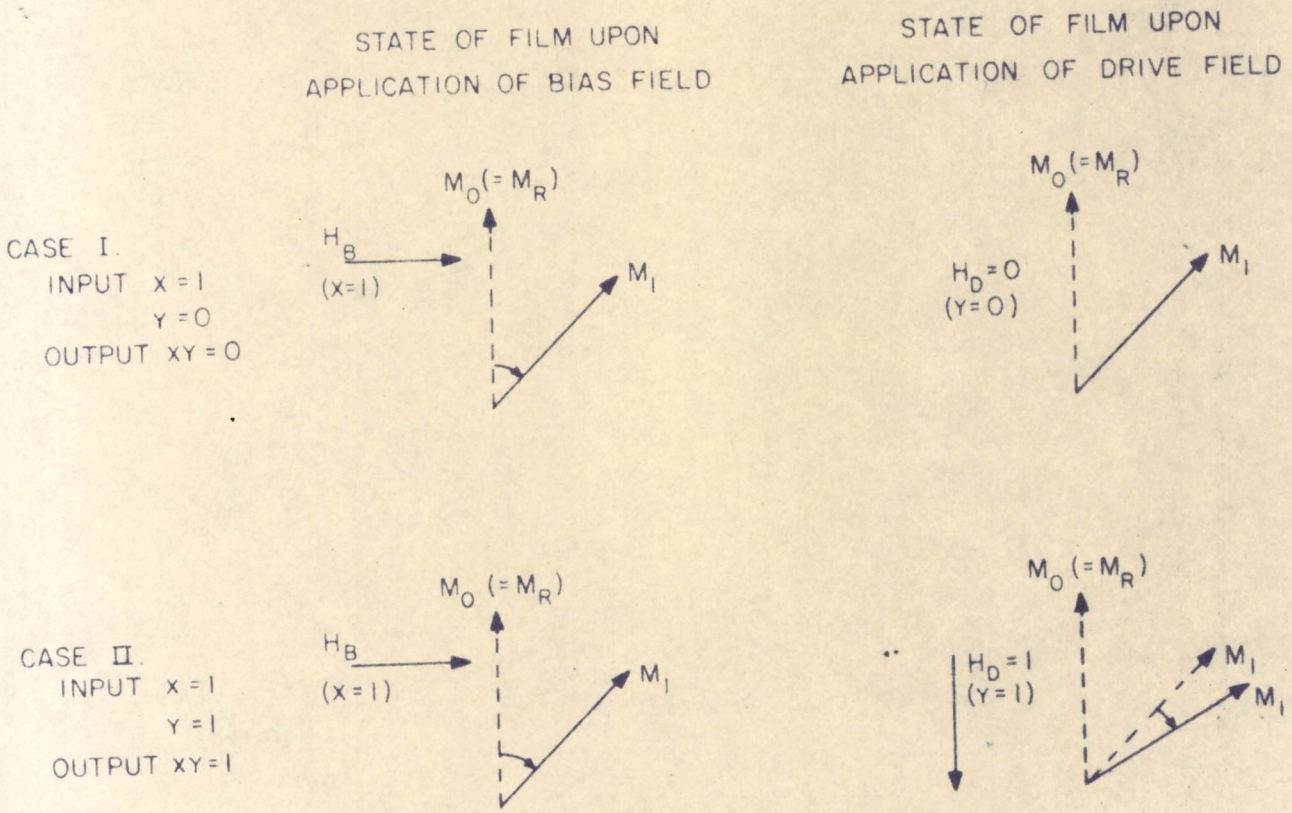


Figure 1. AND Logic (Reversible-Rotation Mode).

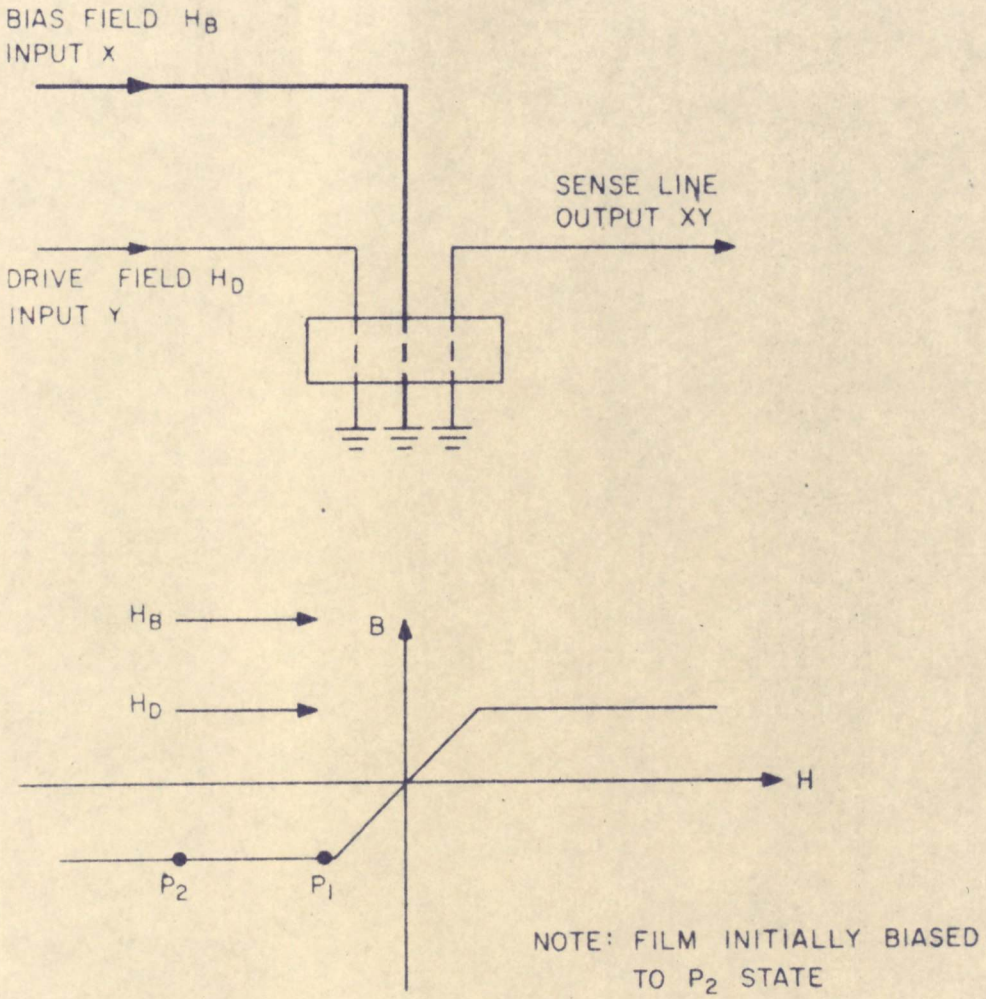


Figure 2. AND Logic (Saturable-Transformer Mode).

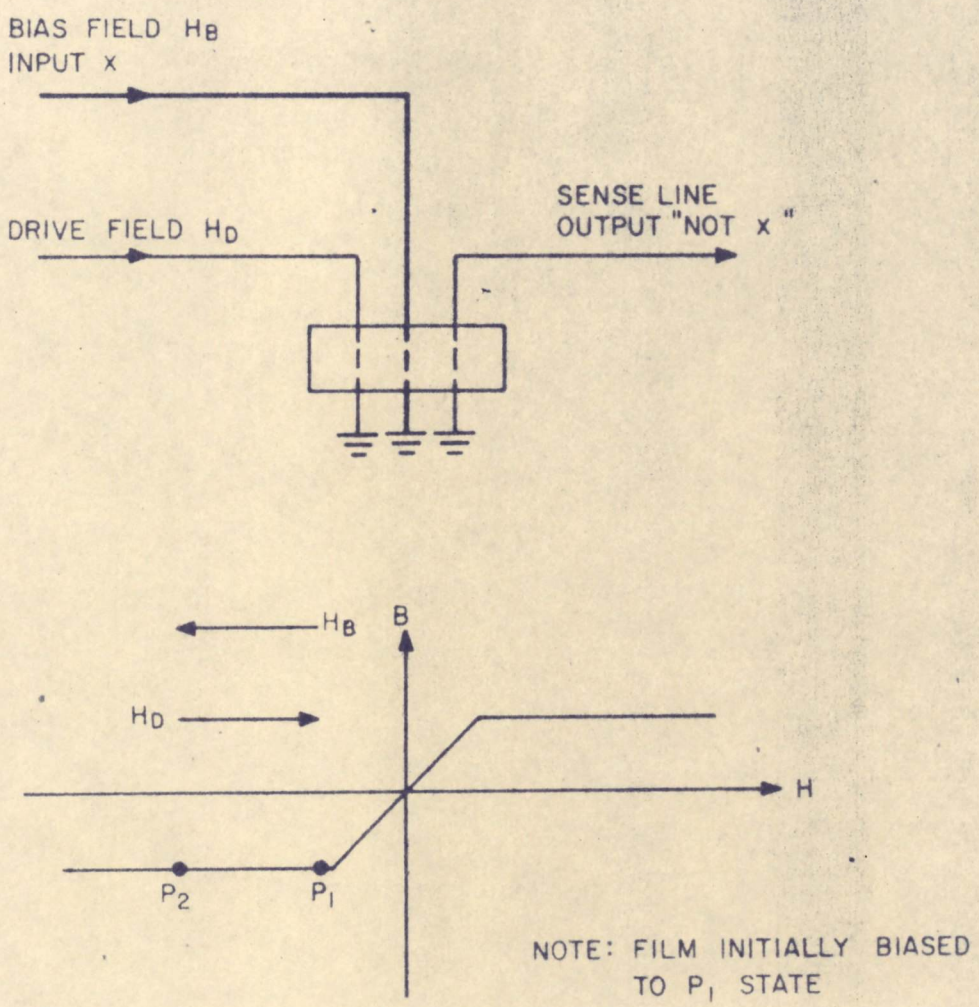
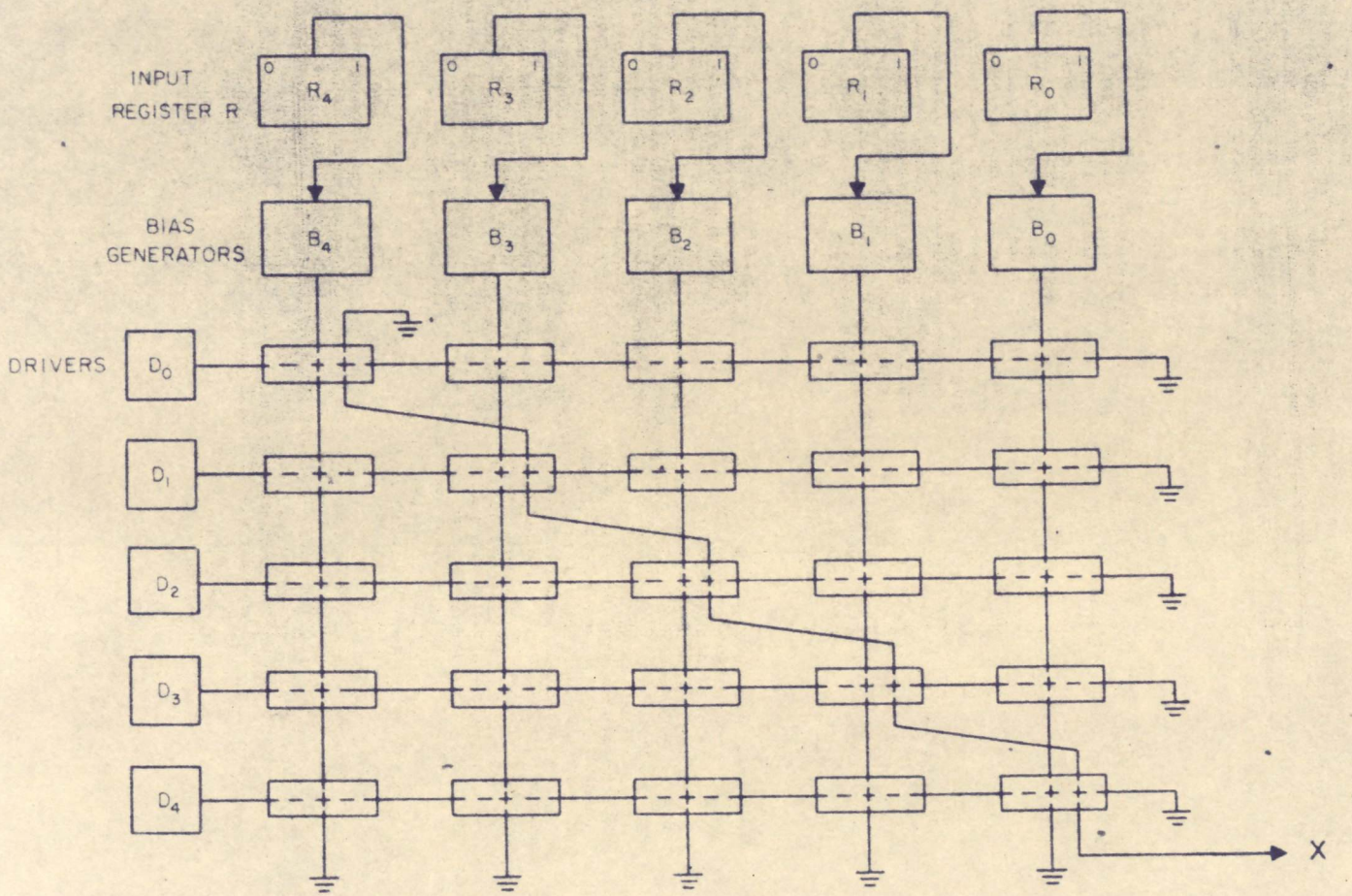


Figure 3. Inverter Logic (Saturable-Transformer Mode).



(a)

$$X = D_0R_4 + D_1R_3 + D_2R_2 + D_3R_1 + D_4R_0$$

(b)

Figure 4. (a) Film Magnetization Directions; (b) An Example of Functional-Array Logic.

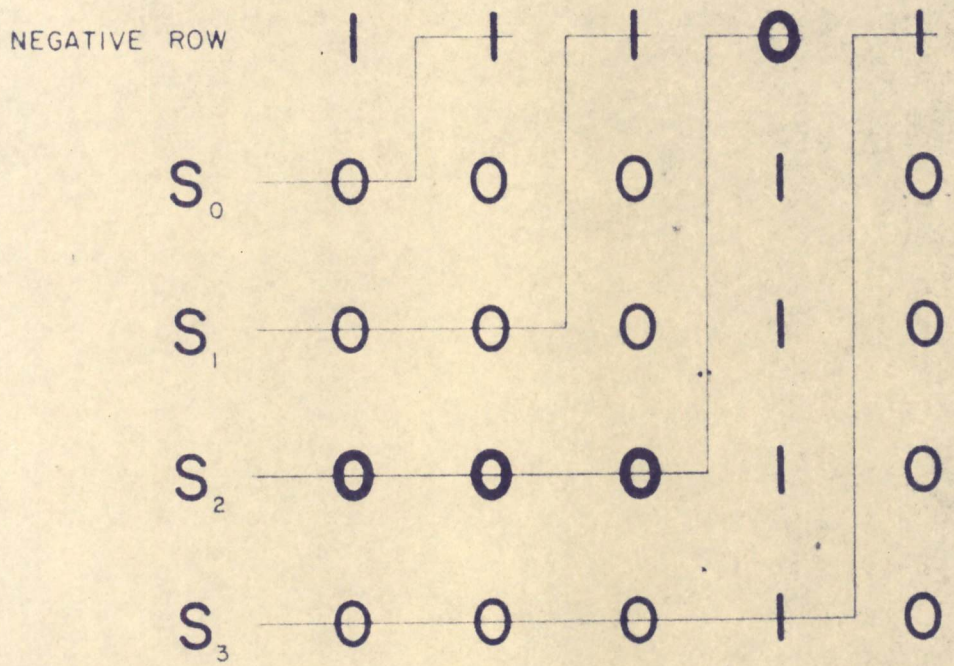
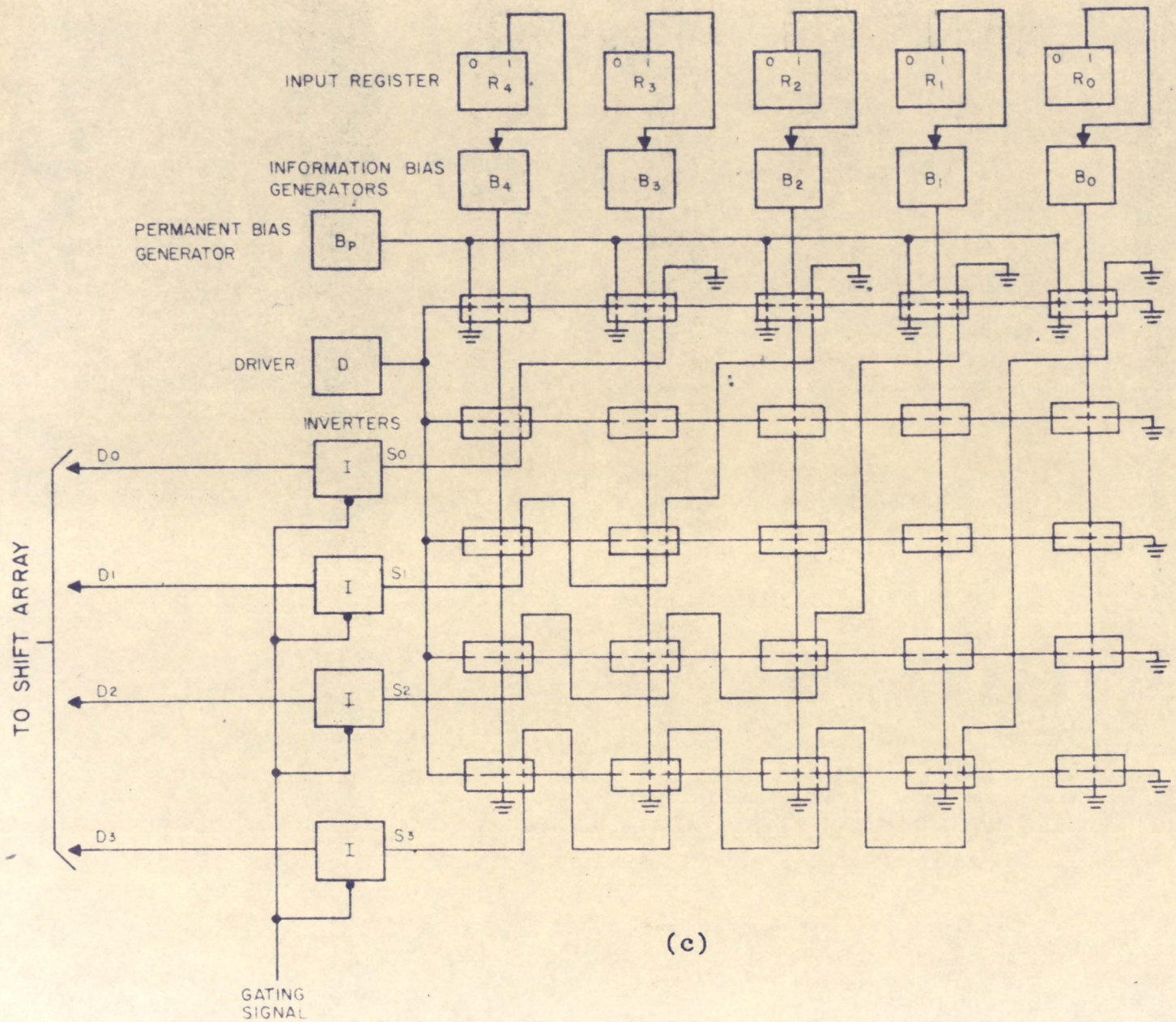
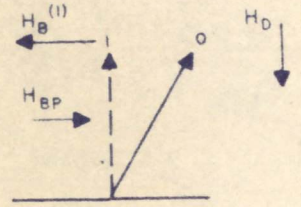


Figure 5. Functional Array for Determining Most Significant Information Bit.





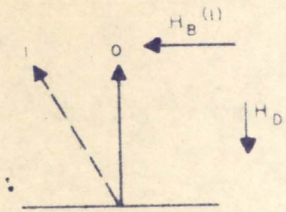


Figure 6. (a) Film Magnetization Directions of Row 1 (negative row) for Zero Bias;
(b) Film Magnetization Directions of Rows 2-5 for Zero Bias;
(c) Network for Determining Most Significant Information Bit.

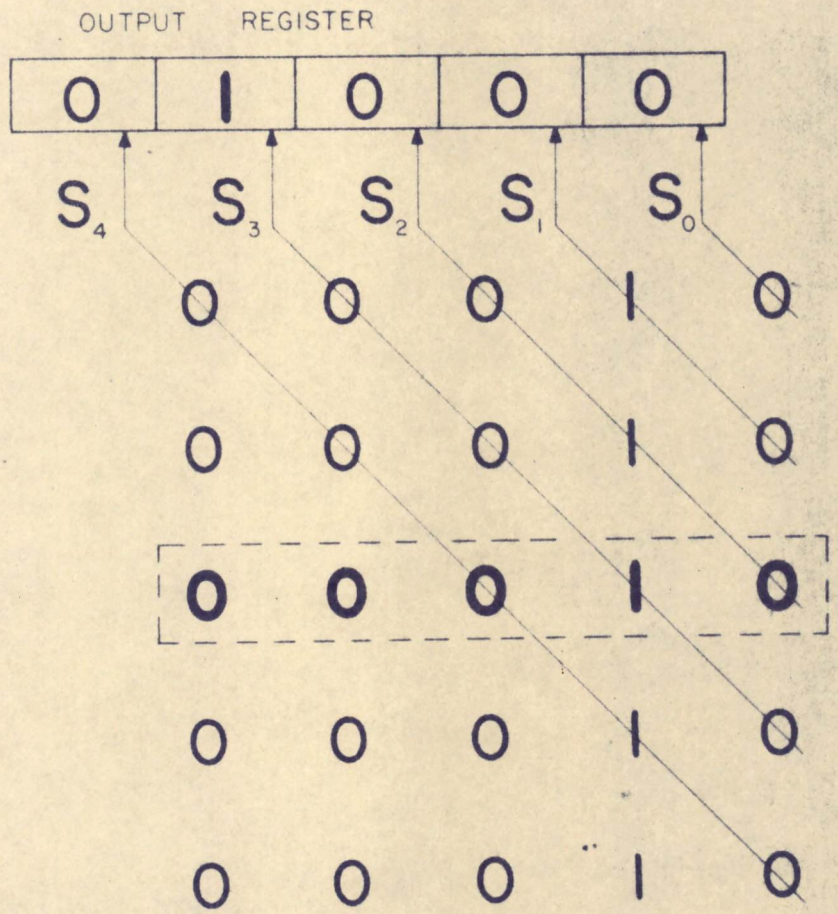
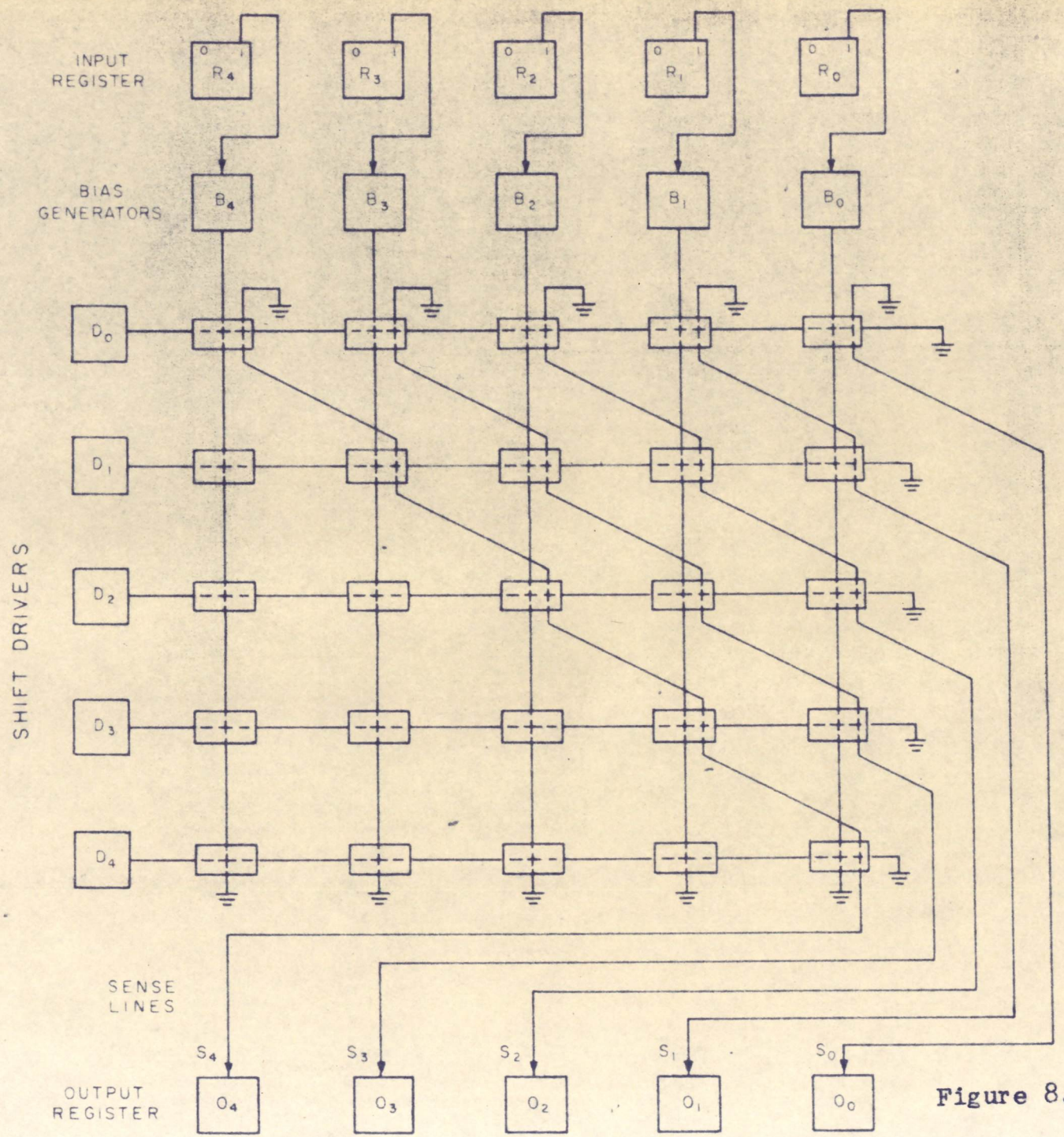
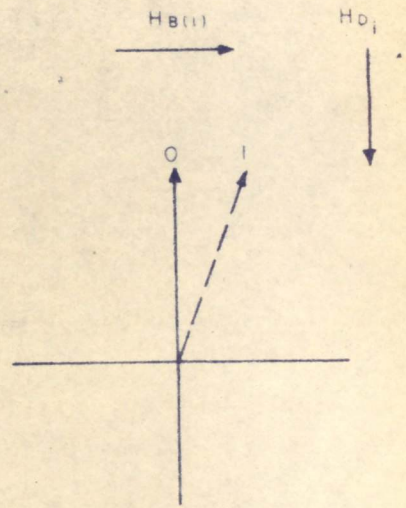


Figure 7. Functional Array for Left-Shifting a Word.

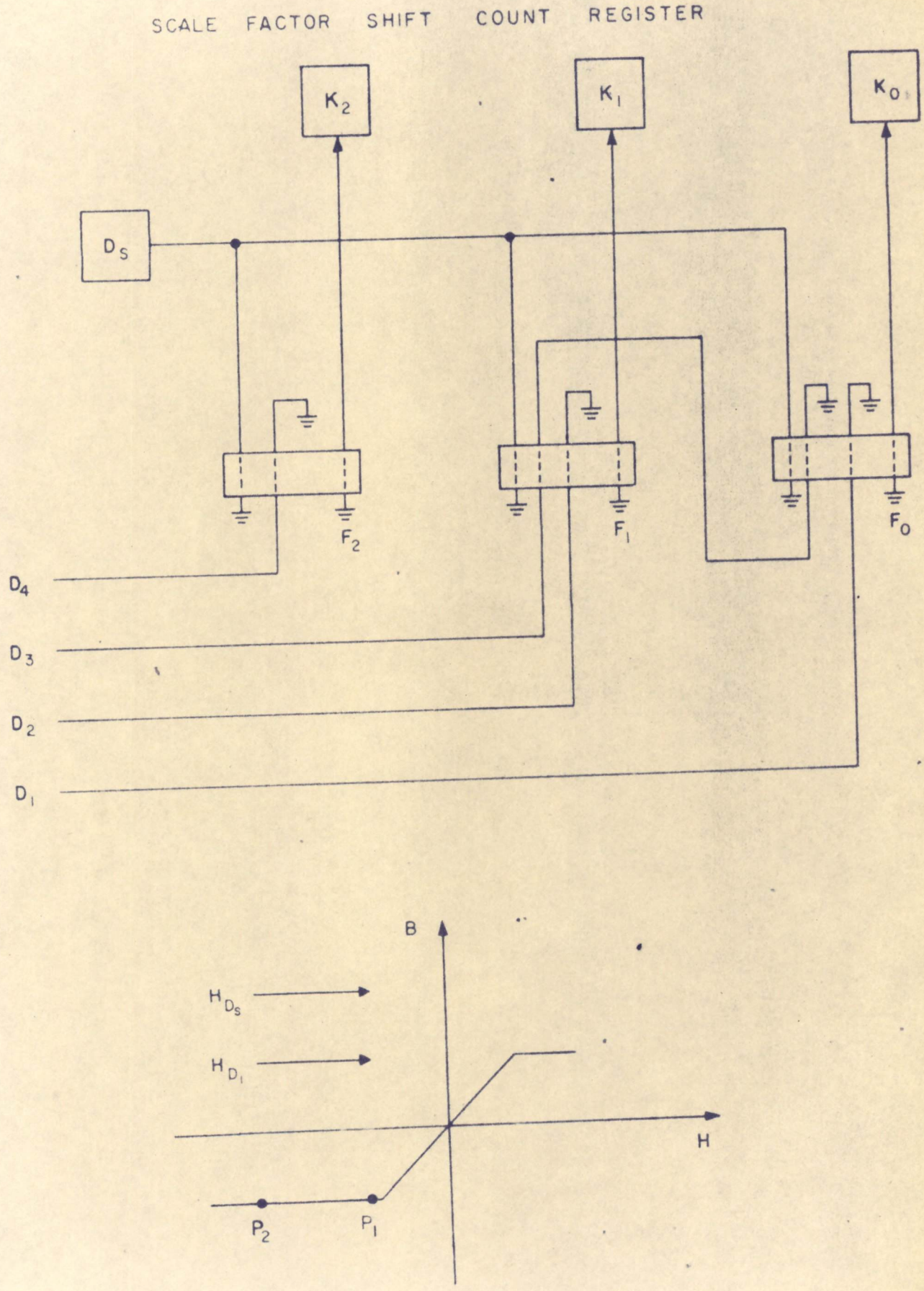


(b)



(a)

Figure 8. (a) Film Magnetization Directions; (b) Network for Left-Shifting Operation.



NOTE: ALL FILMS INITIALLY BIASED TO P_2 STATE.

Figure 9. Scale-Factor Shift-Count Encoder.

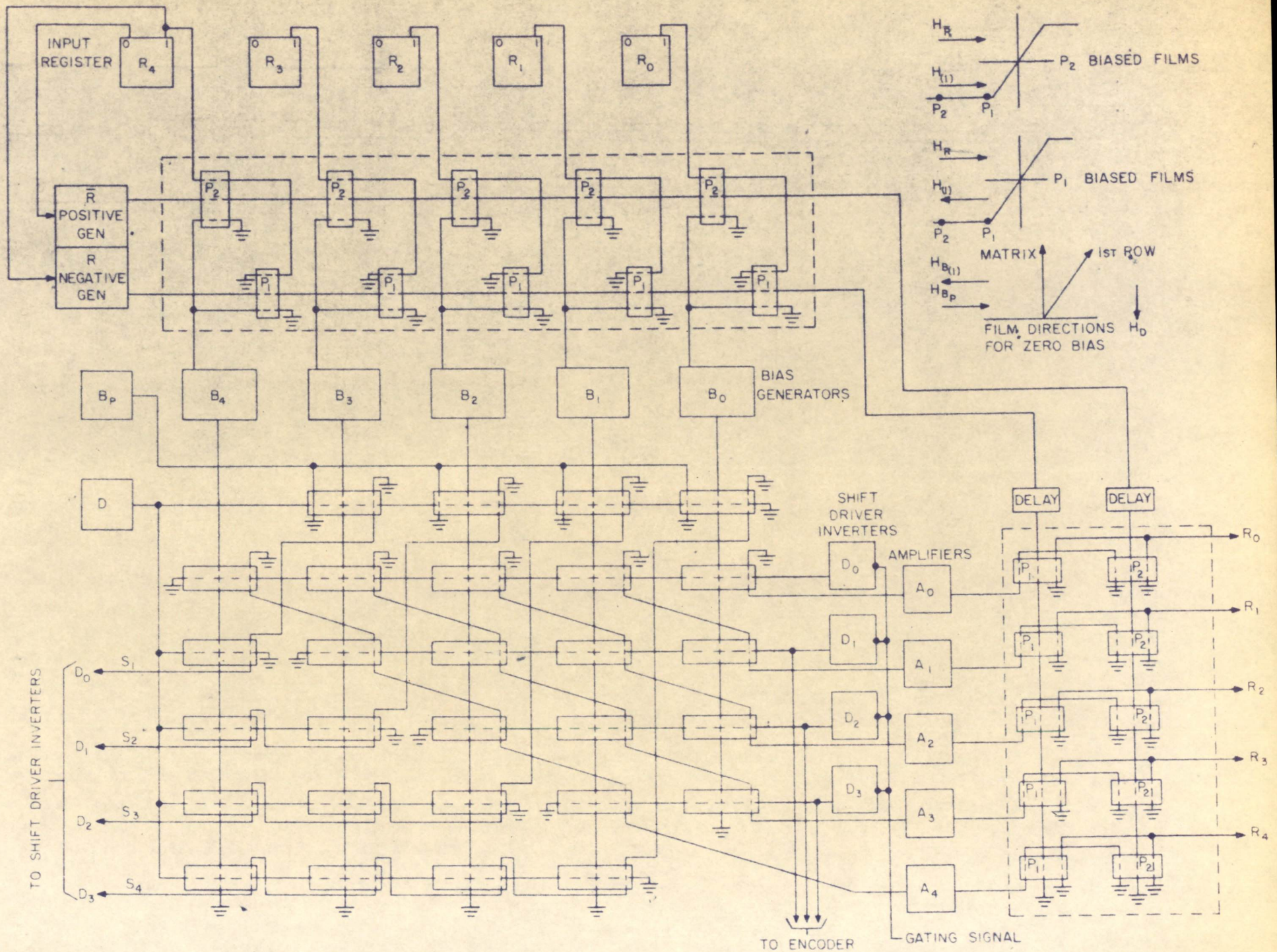


Figure 10. Scale-Factor Network.

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION

BAldwin 3-0600

19th STREET & WEST ALLEGHENY AVENUE
PHILADELPHIA 29, PA.

November 13, 1959

Mr. Harlan E. Anderson, Chairman
1959 EJCC Publication Committee
Digital Equipment Corporation
Maynard, Massachusetts

Dear Mr. Anderson:

I am enclosing the paper for presentation at the Eastern Joint Computer Conference. You will notice that the paper is in two parts: Part 1 is by Messrs. Eckert, Chu, Tonik, and Schmitt. This part will be delivered by Mr. Eckert. Part 2 is by Messrs. Lukoff, Spandorfer, and Lee. This part will be delivered by Mr. Lukoff

I am enclosing photographs and biographies, which were also requested.

If there are any comments that you care to make, I would appreciate hearing from you.

Very truly yours,

REMINGTON RAND UNIVAC
Div. of Sperry Rand Corp.

H. Lukoff

H. Lukoff, Chief Engineer

HL/at

Enclosures

BIOGRAPHY - HERMAN LUKOFF

Mr. Herman Lukoff graduated from the Moore School, University of Pennsylvania, in October 1943 with a BS degree in Electrical Engineering.

After graduation, he was involved in circuit development on the ENIAC project. He engaged in radio-radar maintenance in the United States Navy from July 1944 to June 1946. Upon release, he joined the EDVAC project at the University of Pennsylvania.

Mr. Lukoff joined the Electronic Control Company, later incorporated as the Eckert-Mauchly Computer Corporation, in September 1947. He was a member of the Univac staff engaged in the design of BINAC and Univac circuits. When Eckert-Mauchly joined Remington Rand, Mr. Lukoff was successively promoted to Univac I Project Engineer in charge of a group of engineers and technicians, responsible for the test and delivery of the first 10 Univac I systems to customers.

In 1955, Mr. Lukoff was named LARC Project Coordinator, and in 1956, an Engineering Director.

Mr. Lukoff has been with the LARC Project from its beginning stages to the present, and is now Chief Engineer, Commercial Engineering I.

He is a senior member of the IRE.

BIOGRAPHY - WILLIAM F. SCHMITT

Mr. William F. Schmitt was born in 1926. He attended the University of Pennsylvania from 1944 to 1950 with interruption for military service. In 1950 he was graduated with distinction from the Moore School of Electrical Engineering having been elected to Sigma Xi, Tau Beta Pi and Eta Kappa Nu.

Upon graduation he joined Remington Rand Univac where he has been employed in the fields of programming, system engineering and logical design. He is presently manager of the logical design department in which capacity he was responsible for the logical design of the LARC system and the LARC system elements.

Mr. Schmitt is a member of the American Physical Society.

BIOGRAPHY - ALBERT B. TONIK

Mr. Albert B. Tonik was born in 1925. He graduated high school in 1943 and entered the Army for three years. In 1949 he graduated from the University of Pennsylvania, majoring in Physics and elected to Phi Beta Kappa. He continued studies at night. He has worked for more than ten years at Remington Rand Univac, and is now Manager of the Design Programming Department. He has helped to define the specifications and make extensive use of Univac I, Univac II, Univac Solid State Computer and LARC; also, developed maintenance routines for them.

He is a member ACM and SIAM, and recently presented a paper on LARC "Sympathetic Programming" at the International Conference on Information Processing in Paris.

BIOGRAPHY - J. CHUAN CHU

Mr. J. Chuan Chu started in the computer field in 1943 as part of the team of J. Presper Eckert and John W. Mauchly working on ENIAC at the University of Pennsylvania. He subsequently joined the Reeves Instrument Company working on fire control, and then became Senior Scientist for the National Argonne Laboratory in Chicago.

At Argonne, where he was placed in charge of computer development, he participated in the development of three large-scale computers. Two of these were used by Argonne itself, and one was used at the Oak Ridge National Laboratory.

Mr. Chu joined RRU in January 1956 as an assistant chief engineer. He was successively promoted to Associate Director of Engineering; Director of Research; Chief Engineer, Product Planning, and Chief Engineer, Commercial Engineering.

The current LARC development is the sixth large-scale computer in which Mr. Chu has either participated or directed.

BIOGRAPHY - J. PRESPER ECKERT

Mr. J. Presper Eckert graduated with a MS degree in 1943 from the Moore School of Electrical Engineering at the University of Pennsylvania. At Moore, Mr. Eckert worked on the ENIAC project with Dr. John W. Mauchly, assistant professor of electrical engineering.

In October 1946, Mr. Eckert and Dr. Mauchly formed a partnership, the Electronic Control Company. Fourteen months later, they incorporated themselves as the Eckert-Mauchly Computer Corporation. In March 1950, Remington Rand assumed control of Eckert-Mauchly Corporation, later renaming it the Univac Division.

Mr. Eckert was honored for his pioneering work in electronic computer development when he received the Howard N. Potts Medal of the Franklin Institute, Philadelphia, in 1949. In 1956, he was elected a fellow of the IRE.

BIOGRAPHY - FRANCIS F. LEE

Mr. Francis F. Lee was born January 28, 1927 in Nanking, China. He received his B.S. degree in Electrical Engineering in 1950 and M.S. degree in 1951, both from the Massachusetts Institute of Technology.

After his graduation he worked at the Research Laboratory of Electronics and the Servomechanisms Laboratory, both at M.I.T., where he did research and development work on the Sinotype machine which is a keyboard operated type-setting machine for Chinese, and the numerically controlled machine tools.

He left M.I.T. and joined RCA, in Camden, in June 1955, where he worked on the Sales Recorder Computer of the Bizmac System.

He joined Remington Rand Univac in 1956 as a project engineer on LARC. He has been responsible for the design, construction and testing of the LARC Input-Output Processor. He is at present a Department Manager in charge of the LARC Processor.

Mr. Lee is a member of Tau Beta Pi, Eta Kappa Nu and a senior member of the IRE.

BIOGRAPHY - LESTER M. SPANDORFER

Dr. Lester M. Spandorfer was born in Norfolk, Virginia, October 16, 1925. He received the BSEE and MSEE from the University of Michigan in 1947 and 1948, and the Ph.D. degree in 1956 from the University of Pennsylvania. Until 1951 he was with Bell Telephone Laboratories working on the design of wideband feedback amplifiers, transmission systems, and microwave equipment. At the Moore School of Electrical Engineering, he was in charge of the University of Pennsylvania Computing Center and also formed and directed a group for the Signal Corps for research and development on automatic telephone switching circuits and systems. In 1957, he joined Remington Rand Univac where he is presently responsible for the high-speed central computer of the LARC System.

Dr. Spandorfer is a member of Tau Beta Pi and Sigma Xi.

File Copy

DESIGN OF UNIVAC® - LARC SYSTEM

Part 1

J. P. Eckert, J. C. Chu, A. B. Tonik, W. F. Schmitt

This talk is a progress report and in many respects a final report on the Univac® - LARC system which has been developed by Remington Rand Univac. It is a companion not only to another talk on LARC design being given at this time but with an earlier talk given three years ago to the E. J. C. C. in New York.[I]

The talk three years ago described the objectives of a system still in the design stage. This talk describes progress since then. In order to prepare for this talk we have, of course, reviewed the one delivered three years ago. What we read was quite interesting. We found that in one sense of the word we have no progress to report. Fortunately in the larger sense of the word we have great progress to report. The area in which no progress, or more precisely no change, has been made deals with the design objectives of the LARC system. All of the goals set up for the LARC system three years ago have been very safely achieved. None of the speeds of any of the operations in the LARC system have been changed. Basic decimal-checked addition takes exactly one microsecond as described three years ago. Memory cycle times of both one microsecond and four microseconds have been adhered to.

By a conservative design approach and by choosing existing

I. Univac-Larc, The Next Step in Computer Design - J. P. Eckert Proceedings, 1956 Eastern Joint Computer Conference, A I E E Special Publication T-107, Pp. 16, 17, 18, and 19

components, we expected LARC to be completed in 1958. Although we did use then existing components, modifications required to increase reliability on some of the components along with the logical complexity of the system delayed completion until 1959. If we had compromised our speed or reliability objectives, the delay would have been much shorter.

Now we come to the point where great and for computer engineering unusual progress can be reported. We have precisely met and proven the validity of our original goals on the world's fastest, most versatile computing and data processing system as described in our earlier published talk. Figure #1 shows a typical LARC system as it would appear in an operating installation.

The original objective of the LARC system was to build a good system which pressed the limits of the art while still maintaining balance between the various elements of the system. We feel a good system is one in which everything involved is accomplished in a manner which is not only dependable but consistent in the degree to which it presses the art at the time the design is frozen. The talk of three years ago established the goals. We have now accomplished them in the area of logic circuits, high speed memories, input-output equipment, and most important of all in overall system organization. Further we have established an automatic procedure for the prodigious record keeping required to carry out such a design. The companion paper will discuss this point further.

By a balanced system we mean a system designed to obtain the greatest work output for costs involved. Since the problems faced by different users vary, considerable flexibility of the input-output equip-

ment and the memory equipment of the Computer is required. In addition to providing more flexibility in these areas than any other existing system, the LARC system has the added flexibility of enabling either one or two computing units to be included as part of the system to allow increased speed.

Computers and Processor

A basic LARC system contains a Computer and a Processor, each of which has most of the attributes of a general purpose Computer but perform different functions in the system. The primary function of the Processor is the flexible, parallel, and coordinated control of all input-output equipment and transfers between this equipment and the memory system. The Computer is designed to perform rapid arithmetic computation with a minimum of interference.

The two Computers in an expanded system, see Figure #2, can be programmed and controlled to solve jointly a single problem or each can solve independent problems. The Processor is designed to take care of the input-output and other on-line equipment needs of both Computers and to do any necessary editing of the input-output data. If input-output demands are not excessive, it may also be used to run various side routines such as sorting and merging. It receives compact instructions from the Computer and expands them by program to provide the control, interlocking, and timing required to operate simultaneously a large group of on-line equipment. This function requires only limited arithmetic ability.

To allow for simultaneous communication between the various units (a necessity with the high degree of parallel operation achieved) with a minimum of switching circuitry, a time slot system of inter-unit

communication is used. Time slotting of the elements of a Computer is quite new and is one of the features which has given LARC such a great increase in speed and flexibility without a corresponding increase in cost.

In LARC we sought to minimize the total amount of electronic equipment by considering the logical design as a whole rather than seeking to optimize the equipment required for each individual instruction. For example, there are many methods of performing multiplication which reduce the number of individual addition operations required without expanding equipment requirements. We examined a number of these multiplication methods and picked the arrangement which required the minimum amount of equipment, not just for multiplication but for all of the machine instructions, frequently making compromises on some specific instruction. A modified short-cut multiplication procedure was finally employed that requires only one addition per multiplying digit and allows 11 by 11 digit products to be formed in 8 microseconds. Floating point multiplication of 9 by 9 digits also takes 8 microseconds, the extra time being used for normalizing. The division process is a fixed length requiring 5 cycles or 2 1/2 microseconds per quotient digit and requires 28 microseconds for a floating point division or 32 microseconds for a fixed point division.

The pulse code in LARC was carefully chosen to yield a ten percent chance of a single digit superposition error not being detected. Of course, since most such errors occur on several digits, the chance of not detecting such an error is remote. However, where a single digit must be transferred special checking circuits are employed to reduce this possibility or some

special circumstance is noted which makes the chance of detection far greater.

The names Processor and Computer assigned to the central units of the LARC are somewhat misleading. The entire LARC system may be considered a data processor. What we call the Processor in the LARC system contains a computer of its own in addition to all of the circuits necessary to synchronize the on-line equipment into the system. In designing the LARC system, we carefully avoided incorporating any feature that would increase costs unless it realized a much greater proportional increase in over-all speed and performance. On the basis of this criteria alone the incorporation of a computer within the Processor is justified although it does provide other important benefits by way of increasing flexibility and simplifying programming and communication within the system. If the LARC Computer were designed to perform the duties of the Processor, it would require additional instructions and other facilities. In such a system all of the circuits devoted to synchronizing the on-line equipment would still be required. In a typical LARC system, about two thirds of the Processor consist of circuits exclusively involved in synchronizing on-line equipment. The Processor computer represents the remaining one third of the Processor or about one sixth of the equipment and cost of the Computer and Processor combined. Considering also the cost of the on-line equipment used in the system, the incorporation of a computer in the Processor has contributed between one seventh and one eighth to the total cost and complexibility of the LARC system. The LARC Processor, however, may relieve the Computer of half of the work load it

would otherwise have to bear. We, therefore, have achieved as much as eight percent increase in speed for every one percent increase in cost resulting from incorporating the computer in the processor.

Since the program for the Computer and Processor is stored in separate memories, debugging can be done independently so that the programming is usually made easier. Thus we have speeded up LARC without overstepping the state of the art either in circuits or in the demands put upon present day programming technology.

Storage

There are four levels of storage in the LARC system which differ in speed, capacity, and cost per character.

The first level of storage operates on a one microsecond cycle. There are accumulator registers for storing operands and results in arithmetic operations, and there are also index (B) registers for storing constants used in addressing operations. Up to 99 12-digit one microsecond registers may be included in each Computer unit.

The second level of storage is a ferrite-core storage which has a read-write cycle of four microseconds. Figure #3 shows a 10,000 word (600,000 bit) core memory unit. It is accessible to both Computers and the Processor. It serves as both the main storage and buffer storage of the system and as a common communication link between the Computers and the Processor. To increase the rate at which reference may be made to the main storage, it is divided into 2500 word modules. Since the Computers and the Processor have access to the same storage, they can control each others instruction sequences as desired. Nearly 100,000 12-digit words of ferrite-core storage may be included in the system (6,000,000 bits of core storage).

The third level of storage consists of movable head magnetic drums. Figure #4 shows a group of such units. Data can be transferred between the main storage and the drums over one of several simultaneous drum circuits on a data transfer rate of 500,000 decimal digits per second (2,500,000 bits per second). A maximum of seventy-two million digits of drum storage (360,000,000 bits of drum storage) may be included in a system. The drum units are capable of transferring information twenty-five times as fast as the tape units and match the high computing rates of the LARC system. In addition they provide for random access in a fraction of a second. Several drum synchronizers are employed so that computation, and printing data already computed, can proceed in parallel with the loading and unloading of drums to the tape units.

The moving head drums themselves are designed very conservatively. They rotate at 884 R. P. M. They are recorded at 448 pulses to an inch and 29 channels to the inch. Several times this pulse rate and channel density have been achieved in the laboratory on these drums. The magnetic heads which move on a carriage along the top of the drums are moved with moderate accelerations. This is possible since the drums are used in pairs, first moving one head while another head is reading and then alternating so that the synchronizer is never idle. This arrangement allows a very conservative approach to the mechanical problems and a fool-proof head moving mechanism of simple and rugged design driven by a servo motor. The drum assembly is mounted in an air tight enclosure. Inside air is circulated through special filters to collect any dirt particles. The design allows the units to be opened for repair in a non-airconditioned

room. The magnetic heads fly on the hydrodynamically generated air film generated by the rotating surface of the drum. Figure #5 shows a head flying on the surface of a drum. No filtered high pressure air supply which might direct contamination under the head is needed. A simple mechanism lowers the head on the drum without causing even momentary contact with the drum. An electrical circuit detects any contact between head and drum and instantly retracts the head if any contact occurs.

Flying head drum units have been life tested for well over a year continuous operation to ensure that the reliability is consistent with the reliability of the solid state circuit equipment. The order of reliability achieved by these drums is believed to exceed considerably that obtainable on tape or disc equipment at this time.

The fourth level of storage consists of magnetic tape units which transfer data at 20,000 alphanumeric characters per second. Figure #6 shows a group of Univac tape units. The tape units provide for input-output and long term storage of data. LARC presently uses medium speed tape units which not only have the advantage of being compatible with other Univac systems and off-line input-output equipment but have the advantage, due to moderate pulse densities and moderate tape velocities, of being quite reliable. LARC will soon accept faster tape units when faster tape units of high reliability are both available and required. Tape speed is not usually a limitation, however, since the bulk of the input-output load has been taken off of the tape units in the present LARC system by the drum units.

On-Line Equipment

The on-line equipment includes in addition to the tapes and drums used for input-output and intermediate storage:

1. An electronic page recorder, which employs a cathode ray tube and microfilm, is shown in figure 7. It provides high speed recording of output data. Sixty-four symbols are available for tabulating and curve plotting. Plots are complete with titles, scales, and grid patterns. While originally specified at 25,000 characters per second, this has been changed to 20,000 characters per second to allow more accuracy in the curve plotting mode. Figure #8 is a chart of the units for a typical and for an expanded LARC system.

2. Electro-mechanical line printers for multiple-copy printing of numerical characters at 720 lines per minute or printing of combined alphabetic and numeric characters at 600 lines per minute. The synchronizers will provide signals for printers operating up to 1200 lines per minute.

3. A card reader for introducing data into the system directly from punched cards.

4. Console typewriter printers with an attached paper tape reader and punch.

The original design called for a Processor to contain a minimum of five "synchronizers" and a maximum of eight synchronizers as required for simultaneous operation of the various pieces of on-line equipment. The capabilities of the LARC system turned out to be such that in order to provide more flexibility for customer requirements the minimum was

raised to seven and the maximum to fourteen. The synchronizers in themselves have flexibility in the pulse rate they can accept and this along with the concept of the Processor and the optional number of synchronizers that may be used is one of the more important features in obtaining the high speed and flexibility of the LARC system.

LARC Consoles

Supervisory control of the LARC system is achieved through the use of the LARC Operator's Console and the LARC Engineer's Control Console. Figure #9 shows an operating console to the left and an engineering console to the right. The LARC Operator's Console includes a decimal display unit, an automatic typewriter, and an input keyboard. This console is designed for the utmost simplicity of operation and includes only the manual intervention and start and stop buttons. Certain signals from the on-line apparatus are also displayed where operator attention is required.

The LARC Engineer's Control Console includes a replica of the Operator's Console and in addition, all necessary equipment for the monitoring and control of all of the LARC units. A special feature of the consoles is the ability to monitor the operations of the computing unit in a unique way. The digital display units and corresponding binary display units may be connected to any one of a number of key points of the computing unit. Synchronizing equipment allows these registers to display at a particular pulse time and program step selected by the engineer. Various modes of operation including an error display mode for trapping both permanent and intermittent faults greatly reduce trouble shooting time. The console also includes all voltage monitoring and alarm indicators

for the various units, power control for the system, marginal checking controls and all necessary error and contingency indicators.

Complete Parallel Operation

The designer of LARC realized that even with automatic programming some programs must be first written by hand and further the programming must not be so difficult to understand that the people maintaining these machines cannot interpret the situation when trying to locate the fault. For these reasons all of the parallel time-saving features built into LARC were done in a way that would require the minimum of planning on the part of the programmer and would be as similar as possible to his present programming techniques. Therefore, in our system design we have been consistent with the straight forward electronic and mechanical designs employed. Figure #10 shows a list of the equipment in simultaneous operation in a maximum LARC system.

Without exception we have obtained overall system speed without resorting to difficult programming tricks such as might require a knowledge of the detailed timing of the machine and the setting up of complicated interlaced patterns of data and instructions. There are many examples of the point we are trying to make here. The memory organization is one of the best examples. At the time the LARC was conceived we decided to have a very fast core memory (one microsecond cycle time) in combination with a much larger somewhat slower core memory (four microsecond cycle time).

Our first thinking on how to use these two memories was to take all information out of the slower memory and put it in the faster memory, instructions, operands, index numbers, etc. Computing would then be

carried out almost entirely from this fast memory. When we were finished a group of operation results from the fast memory would be returned to the slower memory. This idea led to all kinds of difficulties. First information must be taken out of and put back into the smaller fast memory both rapidly and frequently in most of the problems studied. The large memory being four times slower would have to be separated into several parts so that by a time interlacing system it could keep pace with the small memory. In turn the smaller fast memory would also have to be broken into at least two or three parts so that parts could be loaded and unloaded while another part was in use. In addition the fast memory could no longer be a hundred words or less and still be effective. It would usually have to be at least one thousand words. Even then this complicated process would not work on many problems where the nature of the information coming in is such that one does not know a few hundred words ahead where his next instructions and data are coming from. Since LARC is a very fast new machine and will be used in problem areas which have not been well investigated we did not feel that the introduction of such restrictions on the programming would be practical. Less is gained by this arrangement than one might expect.

Instruction routines are frequently long enough between transfer instructions that they might just as well be taken from the slower memory, interlaced in the same way as would be required to transfer to the fast memory. Some small loss of time using only the slower memory can occur when a transfer order is encountered due to interruption of the interlace pattern. A similar argument will often hold for strings of data. Thus

the faster memory, except for accumulator and index registers, does not help the speed situation much but would be a considerable program complication. In LARC, however, to facilitate matters still further rather than purely time slotting all of the memories together to get a high speed flow of information, we have done this in such a way that the interrelationship is automatic and does not have to be programmed. Up to eight, one half microsecond subdivisions of the four microsecond memory cycle are provided for time slot operation. The programmer does not have to plan how to intermix information in order to achieve the time slotting necessary to match memory speeds to the Computer. Because of the time slot system the four microsecond memory system looks almost like a one half microsecond memory in an overall system sense.

In this system it is possible for the Computer to ask for information which is not yet available. This is because the Computer receives orders ahead of their execution time in order that circuits have time to set up without delaying the operation. Since LARC is to achieve its speed without the programmer being required to give attention to timing problems occasioned by parallel operation, special circuits accommodate the situation when inconsistent logical demands occur. These circuits very rarely delay computation in actual operation.

When two computing units are used in a LARC system the common memory system allows either separate operation of the units or alternately any degree of interplay desired. A common memory system and certain common instructions provide the means of interrelating operation. To handle the priority problem involved in the parallel operation of many different units,

the memory units give preference to the input-output synchronizers first, then the Processor, and finally the computing unit.

One kind of parallelism not commonly thought of as parallelism occurs with LARC's one microsecond decimal self-checking adder. Clearly we could convert input data into binary form and checking could be done by program. These extra operations take additional time as well as additional programming effort. In LARC's decimal-checking adder these operations are effectively combined in parallel with the arithmetic operation. A binary unchecked adder would have to be considerably faster to equal the speed of LARC's decimal-checking adder. The adder is normally used as part of a sequence in which an instruction is obtained, corrected as necessary by an index register, exponents are sensed, numbers are shifted as necessary, the sum is obtained, and finally the sum and new exponents are put in an arithmetic register. All of these operations take place in four microsecond interval.

LARC does not expect the programmer to take care of such timing and interlocking problems. Parallelism has been obtained in a system that does not reduce flexibility or require advanced programming technology.

We feel that LARC is a very important step forward in system design in that all of its units are in balance both in regard to speed, reliability, and cost for the present state of the art. Sufficient flexibility has been designed so that as new auxiliary equipment is developed it can be effectively added to the system. Univac I was a better balanced system than any other computer of its era. This statement has never been challenged. The LARC system is similarly well balanced.

Modular Units of a Typical and Completely Expanded UNIVAC LARC System.

EQUIPMENT NAME	TYPICAL	EXPANDED
Magnetic Core Storage Units (2500 words each)	8	39
Computers	1	2
Multipurpose Fast Registers (per Computer)	26	99
Processor	1	1
Drum-read Synchronizers	2	3
Drum-write Synchronizers	1	2
Tape Read-Write Synchronizers	2	4
Electronic Page Recorder Synchronizer	0	1
High-Speed Printer Synchronizer	1	2
Card Reader Synchronizer	0	1
Console Printer Synchronizer	1	1
Tape Positioning Checker	1	1
Magnetic Drum Storage Units (250,000 words each)	6	24
Uniservo II Magnetic Tape Units	12	40
Electronic Page Recorders	0	2
High-Speed Printers	1	2
High-Speed Card Readers	0	1
Control Consoles	1	2
Numeric Keyboards (one per Console)	1	2
Alphanumeric Console Printers (one per Console)	1	2

Figure #8

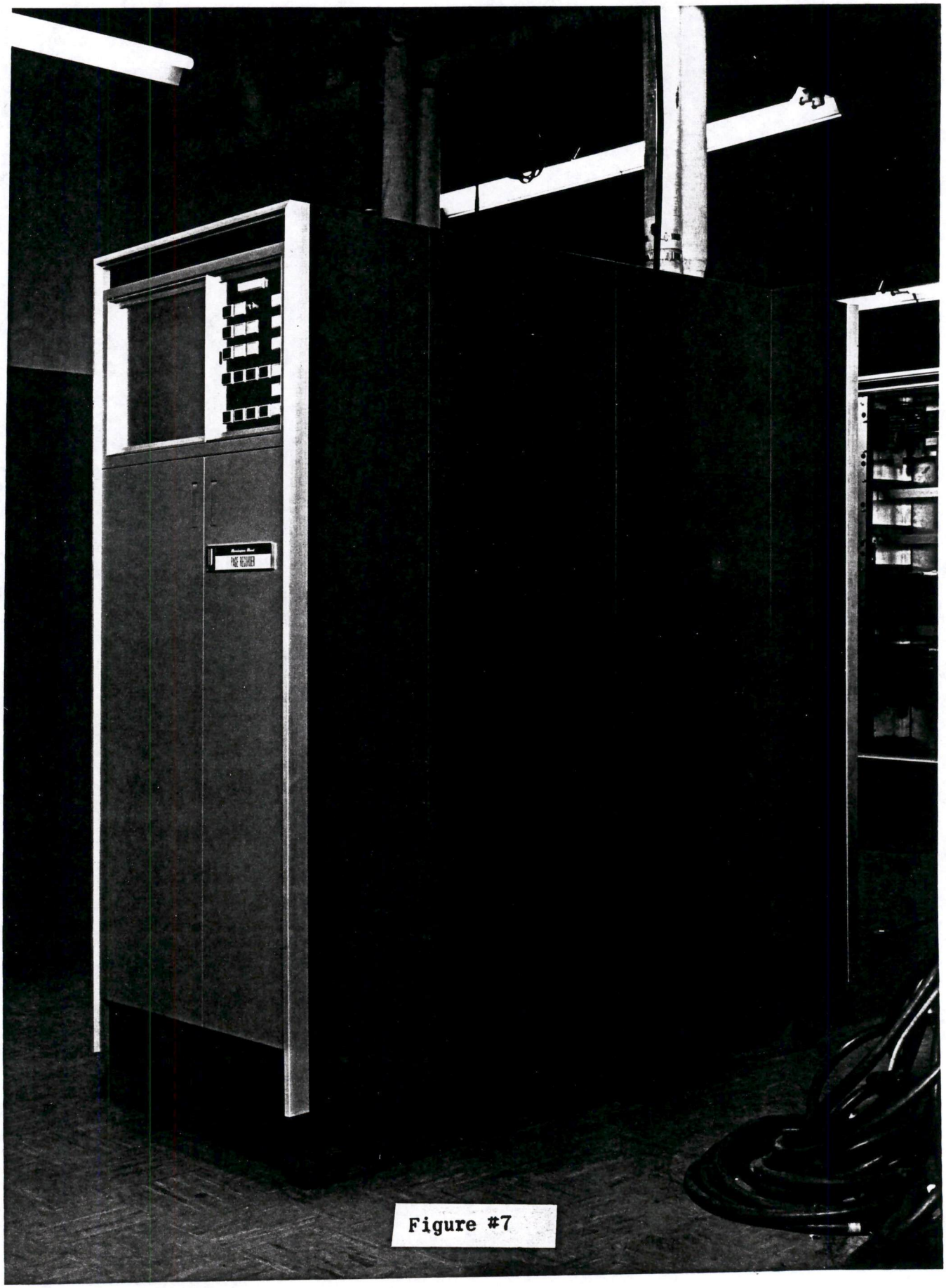


Figure #7

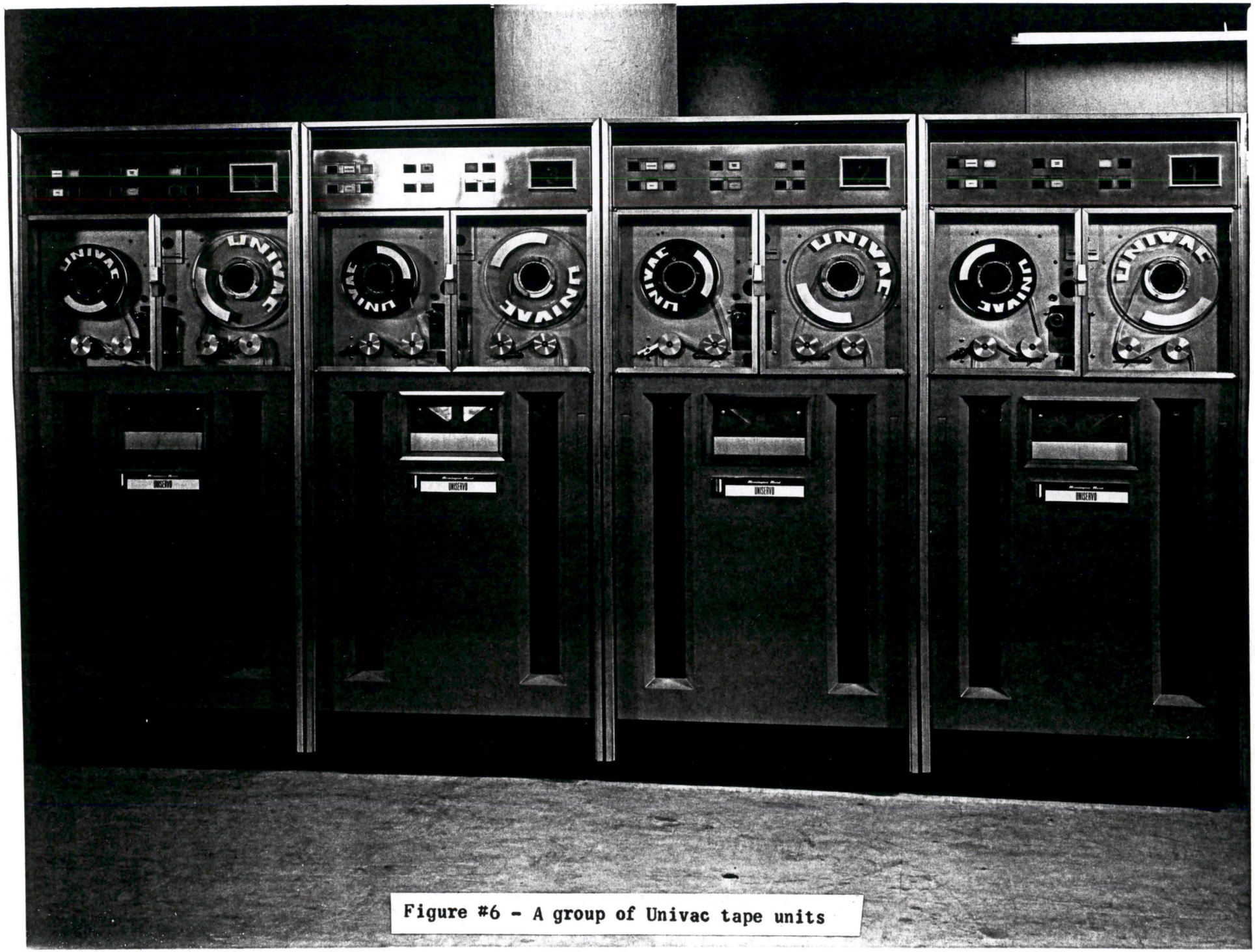


Figure #6 - A group of Univac tape units

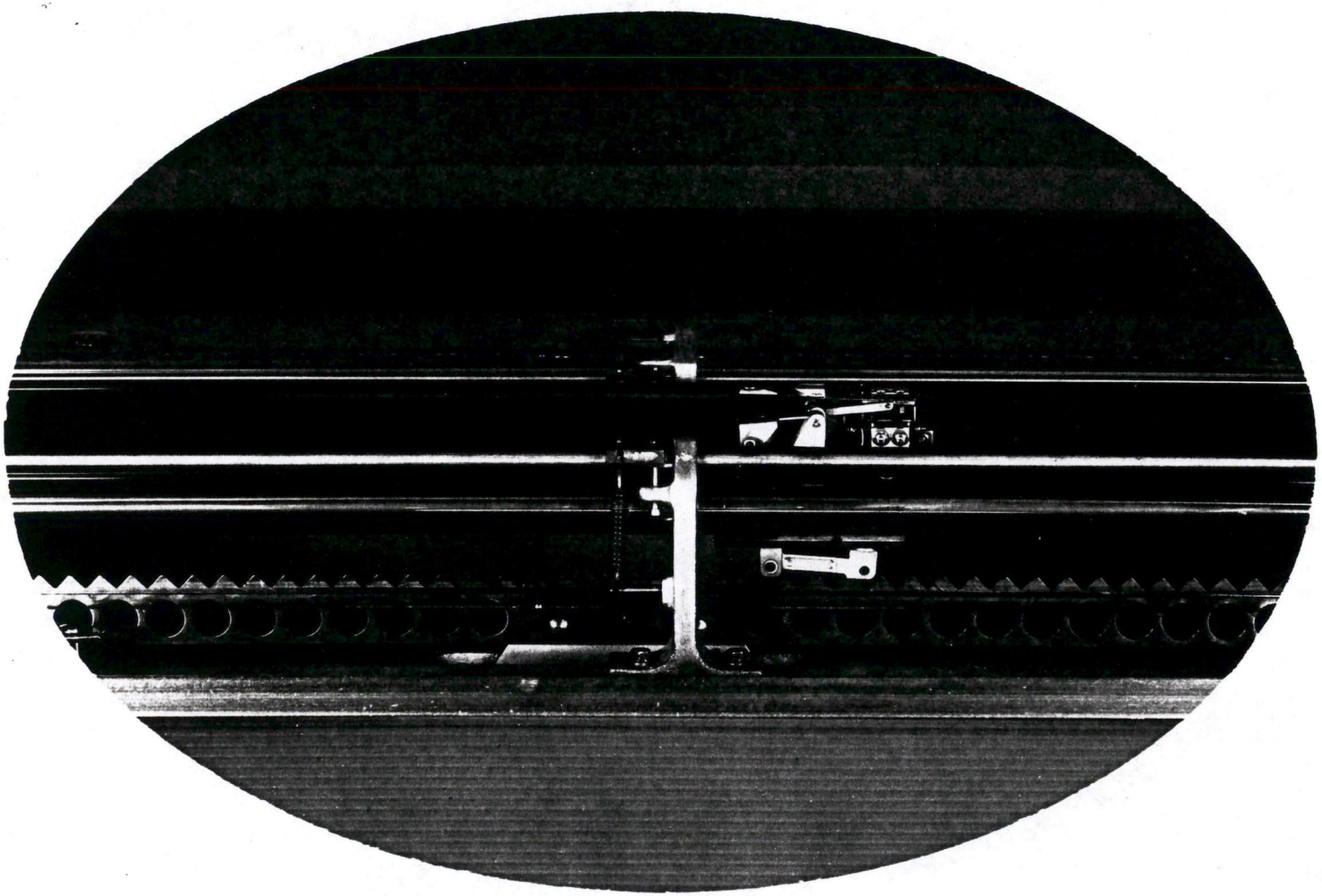


Figure #5 - A head flying on the surface of a drum

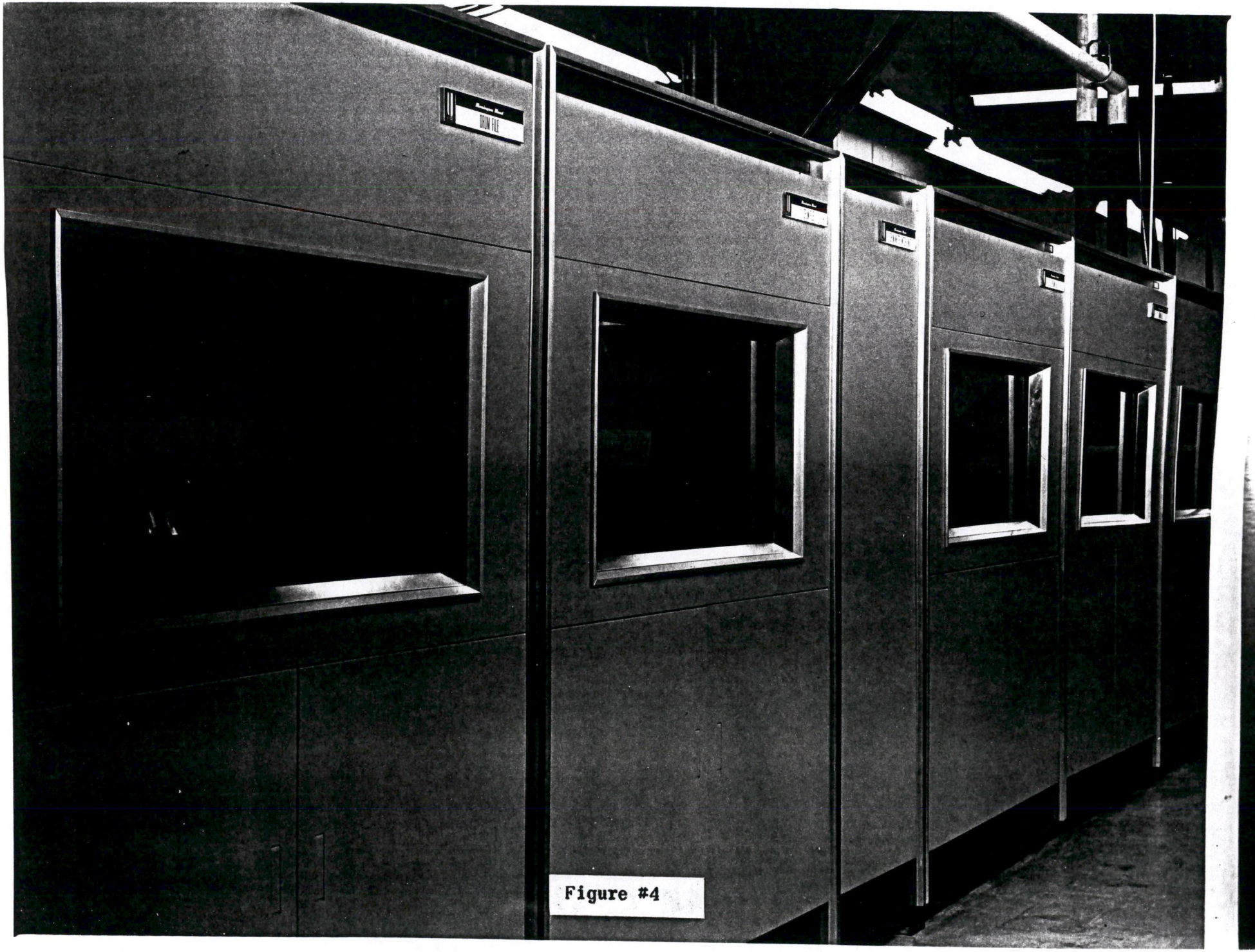
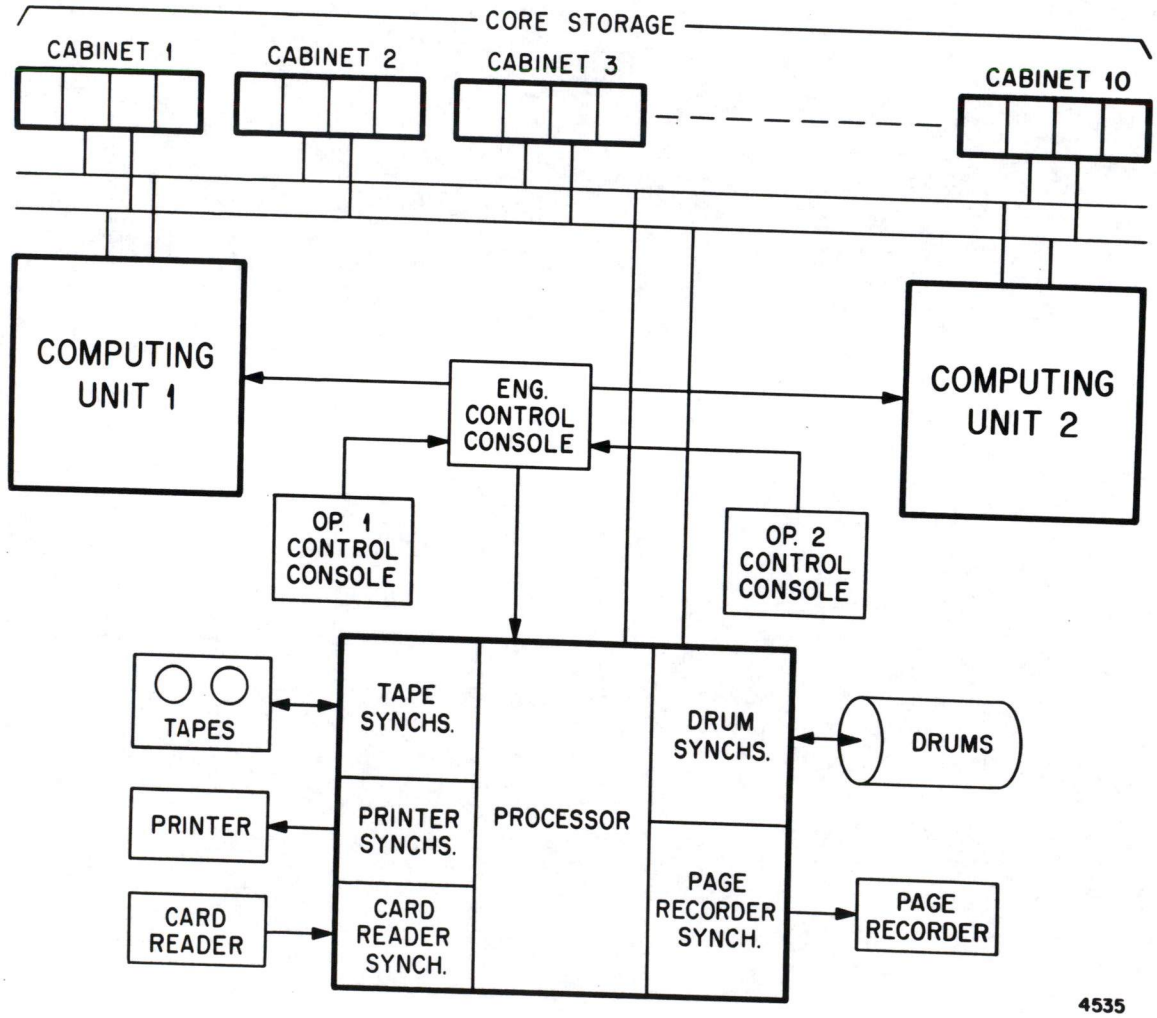


Figure #4

Figure #3 - A 10,000 word (600,000 bit) core memory unit



Block Diagram of A LARC System

Figure #2

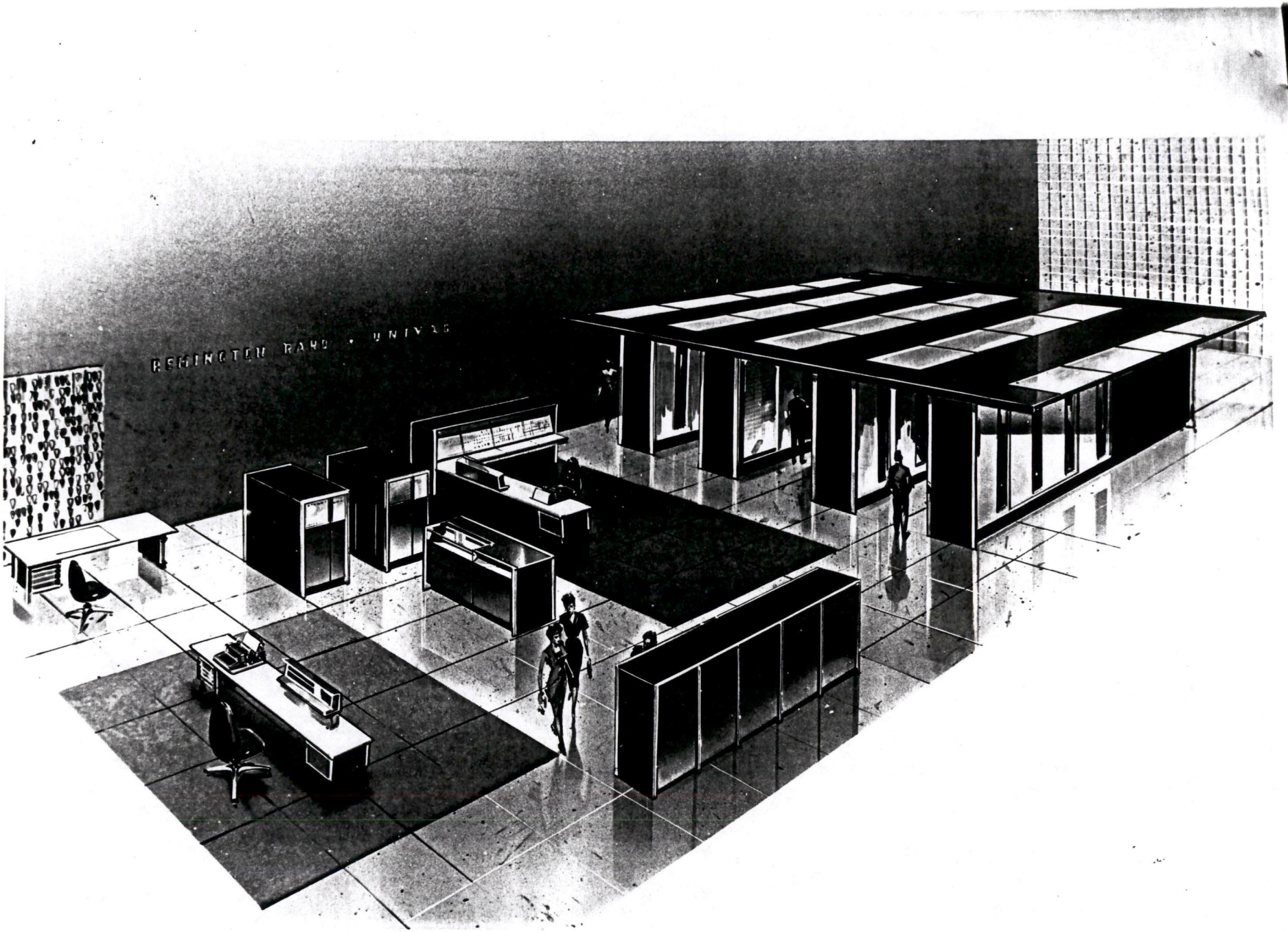


Figure #1 - A typical LARC system as it would appear in an installation

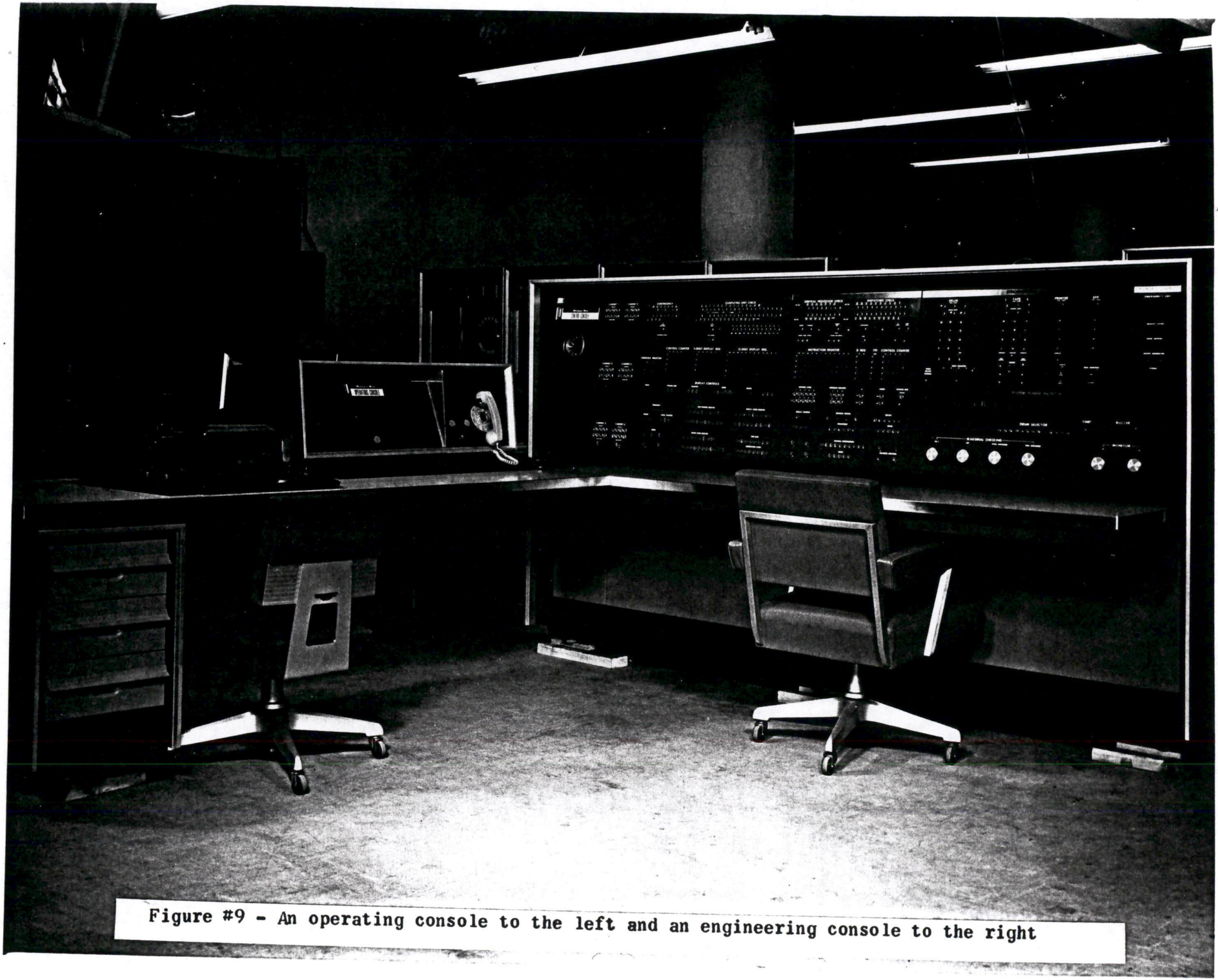


Figure #9 - An operating console to the left and an engineering console to the right

Figure #10 - Complete Parallel Operation in Larc

A list of equipment in simultaneous operation in an expanded LARC system

1. Input-output equipment

   Read from 3 drum units

   Write on 2 drum units

   Position drum head assemblies

   Read from 2 tape units

   Write on 2 tape units

   Position a tape unit or check read a tape unit

   Rewind all tape units as required

   Print on 2 line printers

   Record on electronic page recorder

   Print on console printer

   Read fast card reader

   Operate decimal display unit

2. Computers

   Compute on data by 2 computing units

   Edit or compute on input-output data and control on-line equipment by input-output Processor

3. Operation of instructions in computing unit

   Different parts of five consecutive instructions are performed at once.

4. Decimal arithmetic

   60 bit parallel self-checking arithmetic circuits

5. Automatic checking

   During operation of instruction examine for possiblity of tracing, programmer making a mistake, and computer making a mistake.

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DESIGN OF UNIVAC® - LARC SYSTEM

Part 2

H. Lukoff, L. M. Spandorfer, F. F. Lee

This paper describes the engineering design features of the LARC solid-state computer. The initial job in the LARC development program consisted of determining the type of circuitry and logic that would meet the speed requirements, which called for a decimal self-checking adder which could add 2 11-digit numbers in 1 microsecond and 8 microseconds for a multiplication operation. The basic machine timing was determined by the multiplication instruction; it requires 11 additions of partial products, several cycles devoted to the generation of multiples of the multiplicand and a few more cycles for handling signs and transfer of results to a register. Sixteen operations have to be accomplished in 8 microseconds; thus the basic repetition rate is 2 megacycles or, in other terms, information must be capable of entering the arithmetic circuits every half microsecond.

We realized that the circuitry had to be faster than anything then devised in order to meet these speed specifications. A program was set up to consider all conceivable variations of solid-state circuits in order to select the best circuit. Our definition of "best circuit" was primarily based on a figure of merit formula given in Figure 1. The formula is based on the following considerations: The more drives or

output a circuit has the more logically useful it is. Similarly, the more logical levels included within the circuitry the better it is. In particular, an AND/OR circuit is logically more powerful than an OR circuit by itself. On the other hand, the greater the transit time (electrical delay plus a portion of the rise time) the poorer the circuit. Also, the number of times the circuit can be used per second is an important factor that determines how many will be needed for a given task. A circuit having a long recovery time, such as a blocking oscillator, would be poor. Finally, the lower the cost of the components the greater the figure of merit. Reliability is also reflected into the figure of merit through the cost factor. In general, the lower the cost the fewer the components involved and the greater the reliability. As a first approximation, all factors in the equation are assumed equally weighted, but it should be remembered that low transit time per logical level was what was wanted most, but not at too high a price for the amount of equipment involved. If for some reason one factor is considered more important than another it can have a multiplier or exponent applied. On this basis the circuit shown in Figure 2 was selected. If the figure of merit is normalized at 100 for the circuit selected it may be compared to others, such as the DCTL with 2.8 or the transistor transformer combination having a figure of merit of 4.1, or a similar circuit to Figure 2 with a feedback diode to prevent saturation. This latter combination produced a figure of merit of 52.5. The circuit in Figure 2 is recognized as a basic AND inverter or OR inverter circuit. The surface barrier transistor was selected for use with this basic LARC circuit because it was the only high speed transistor that was reliable and in mass production at the time of circuit design.

Diodes are used to perform the logical operations, and transistors perform the negating and amplifying function. The same diode network acts as either an AND circuit or an OR circuit, depending upon the polarity of the incoming signal. When used as an AND circuit all inputs must be low (-3v) in order for the transistor to turn on. When used as an OR circuit any input going high (0v) will act to turn the transistor off. The transistor is operated into saturation and at cutoff; therefore, the output swings from -3 to approximately 0 volts and is directly coupled to the next circuit. Effective switching occurs during the first 1/2 volt of the transition. The resistor network R1, R2, and R3 provides the proper transformation of DC levels to the base of the transistor. The capacitor, C1, acts to supply extra current in initially turning the transistor either on or off. R4 is used to provide a minimum load on the circuit to limit the storage time of the transistor and also to provide current for discharging the stray capacitance. The circuit is designed to accept a fan-in of as many as 13 inputs and is capable of providing 3 full drives output. However, with the use of mutual exclusion (load sharing) it may fan out to several additional places. The maximum output capacity allowed for this circuit is 80 micro-microfarads.

Now, let us consider how the basic circuit is used to perform logic in LARC. The circuits are used in cascade so that they form an AND/OR, AND/OR, etc. chain. Ideally it would be desirable to continue in this fashion. However, pulse timing becomes inaccurate and therefore retiming must occur in certain places. This is accomplished by means of the pulseformer circuit shown in Figure 3. This circuit permits a logical operation to be performed at its input. The first transistor stage operates a gating network which then selects either a positive or negative timing

pulse (90 mus. wide) to set or reset the following flip-flop combination. The flip-flop can only be set or reset at precisely timed one-half microsecond intervals. A chain of logic is depicted in Figure 4. The sequence is started when pulseformer 1 initiates a transition at one of the timed intervals. The wavefront progresses through the chain of AND/OR circuits where the necessary logical operations take place. The maximum transit time per circuit under worst case conditions is forty millimicroseconds. Allowing for 9 levels of logic the wavefront arrives at the timing gate of the second pulseformer in 360 millimicroseconds after it leaves the first pulseformer. Since the timing pulse at the second pulseformer is scheduled to arrive in 500 millimicroseconds, the difference of 140 millimicroseconds is allowed for timing pulse jitter, pulseformer operation and safety factor. Under normal operating conditions the average propagation time of the signal has been found to be 20 millimicroseconds. Thus there is a very large factor of safety in the circuit timing. The circuit transit time corresponds to 25 megacycles. If less than 6.6 levels of logic are employed between pulseformers there is the danger of the signal propagating too fast and arriving at the pulseformer before the previous clock pulse has disappeared. To prevent this it is necessary to add sufficient delay elements to pad the chain to the minimum delay levels. Padding delay has been required in fewer than 10 per cent of the logical chains.

In addition to the basic logical circuit, the pulseformer and the delay element already mentioned, there are several other high-speed circuits. One is a high-power amplifier capable of producing about 10 times as much current output as the basic circuit and can therefore drive

32 basic circuits. However, this circuit pays for its extra output by consuming 3 levels of delay. Another useful circuit is a scaled down basic circuit to operate at 1/3 the power level. Thus, one of the basic circuits can drive 9 of the lower level circuits. The lower level circuit, however, consumes 1.6 delay levels. The last useful high speed element is the high power amplifier coupled with the pulseformer to form a high power pulseformer.

The fact that LARC circuitry is clocked allows the use of what is called the "pulse envelope system," or more familiarly, "non return to zero logic (N R Z). If direct coupled circuitry is used in asynchronous circuits with N R Z logic, two difficulties appear. Either the length of delay through all logical paths must be predicted and be reasonably constant or a signal from a circuit must be derived to tell when the logic in a chain has been completed. If the former method is used in a parallel computer there is no advantage over the clocked system.

In the arithmetic circuits, for example, many logical paths operate in parallel. Therefore, if a delay element is to signal when the last of the data has come through, it must have a delay equal to the clock pulse spacing in a synchronous machine. On the other hand, if the signal itself is used to tell when an operation is completed, there is the problem of discriminating between a normal signal and the "spikes" (switching transients). This is because a gate with one input being turned on at the same time another input is being turned off will, for a finite signal rise time, allow a spike to come through, as shown in Figures 5a and 5b.

Now if a return to zero or regular pulse system is used there is always a dead space between signals. All signals return to zero during this dead interval and avoid the spike problem. However, the speed at

which pulses can now be put through the circuit (for equal rise and fall time) will be halved because of twice the number of transistors. Since LARC transistor circuit delays are quite stable, less than a two to one timing margin is allowed in the clocked circuits. Thus the necessity of using return to zero signals would decrease the data rate by more than asynchronous operation would increase it.

Asynchronous operation not only requires more equipment, has no apparent speed advantage, but makes testing and maintenance more difficult since no definite points to trigger an oscilloscope can be found since timing depends on actual circuit parameter and the actual signals present.

A large number of logical configurations involving adders, complementers, and other devices were examined. Methods of multiplication and division were chosen carefully, not just on the basis of speed, but the circuits were examined to find out how many drives an individual element need provide so that an overall minimization of the speed through a chain of these elements might be made. Since the product of current gain times the band width for a given transistor is normally constant it is possible to estimate the delay through a network given the number of drives required at each level.

With a simple fan-out network, this optimum occurs with three drives; however, there is no assurance that this is the optimum for an adder network. Although it was suspected that the same limitations were probably true in actual circuits, many circuits were carefully laid out and it was shown that not only were three drives adequate but such an arrangement provided the optimum speed. Further, the current gain of

the surface barrier transistors is low and made more drives undesirable. With high speed mesa transistors now becoming available, LARC speeds could have been achieved with circuits that allowed more drives. Thus fewer transistors would be required in the circuit. Studies show that perhaps 15 per cent to 20 per cent of the transistors might be eliminated in this way. Nevertheless, if the objective is to obtain optimum speed out of the newer mesa transistors, in direct coupled circuitry, use of the present design based on three drives would still be applicable.

Since many, many thousands of high speed circuits are employed in the machine, it is obvious that the packaging is an extremely important consideration, otherwise wire lengths become too great and exceed the 80 micro-microfarad circuit allowance. Also, crosstalk problems could become severe with longer lead lengths. A study and optimization program showed that it was necessary to compromise at a maximum of ten circuits per printed circuit card. This was a compromise between achieving efficient packing densities and minimizing the number of different card types. Larger numbers of circuits per card provide higher packaging efficiencies because DC voltages and clock lines utilize a smaller total number of backboard contacts. A successful solution to the basic and conflicting problems of circuit speed and capacitance and crosstalk minimization was largely achieved by the development of a special connector which provided a large number of connections with the smallest possible backboard area. Figure 6 is a photograph of a typical LARC printed circuit card. The connector which is affixed to the end of the card has 42 through connections in it, in addition to the guide pins which also carry through the ground

connection. Connectors are held to the printed circuit board by means of a metal framework around the card, which also acts to eliminate any problems with card misalignment or warpage. The back half of the card nearest the connector contains five circuits. The other half contains five additional circuits. Test terminals are electrically connected to the outputs of each one of the ten circuits. The seven basic circuits are used with different configurations of input diodes. This results in a total of 30 different types of high speed cards. Spare diodes and transistors are removed where not needed, for economic reasons. Spare cards used for maintenance purposes have all diodes and transistors in place. Card dimensions are approximately 3 1/2" by 9". This shape was chosen to obtain the necessary volume for housing the components. Female contacts are used on the card connector so that there is no possibility of damage which might occur if male contacts had been used. The wires observed on the package serve the function of providing connection between the floating female contacts and the printed circuit wiring. Lower stray capacitances are also achieved and input-output printed circuit wire bottlenecking is reduced. The male connectors are packaged extremely close in the basic modules which go together to form the backboard. Figure 7 is a photograph of a module backboard before wiring. The degree of packing efficiency is very high when it is realized that 88 per cent of the backboard wiring area is composed of connectors. As a consequence of this and the close packing of contacts there are over 6000 wire terminations per square foot. Reducing the backboard area in this way has allowed the use of wires sufficiently short so that no special line driving elements are necessary. It was necessary to leave small spaces (30 mils) between

connectors to permit a small amount of air flow for cooling purposes. All wiring on the backboard is done with taper pins. With this high a wiring density, as shown in Figure 8, it becomes impractical to consider soldered or wire wrapped connections. The connectors are color coded to make the job of terminal identification much easier for the wiremen. Each terminal on the connector is bifurcated and appears as two taper pin holes so that it is possible to propagate the chains of wires without using auxiliary tie points. The wiring is extremely dense and piles up to a depth of several inches over most of the backboard. Throughout the development phases of the program accessibility to the backboard was a matter of gravest concern, since it was impossible to accurately predict or simulate actual backboard wiring buildup. We have since installed many thousands of wiring changes and have fully proven that the wiring technique is indeed practical. We have developed new technology and new tools for working with this new high wiring density. Figure 9 is a photograph of special tools, which includes long armed taper pin inserters and extractors, pin point light sources and a BORESCOPE, originally developed for examining the inside of a gun barrel, but has proven effective for penetrating the mass of backboard wire and giving the wiremen a close-up view of the connector.

In order to reduce the congestion on the backboard, very fine steel core copper wire was used with a thin teflon insulation. The physical strength of size 30 steel core wire is approximately equal to copper wire of twice the cross sectional area. Reduction in wire size not only helped to reduce congestion but also produced a necessary reduction in the stray wiring capacitance.

One of the more serious problems that could occur with many thousands of transistor circuits operating simultaneously is that of crosstalk and other noises being coupled into the transistor circuits. Crosstalk effects were calculated as much as was possible and further experimentally checked in the laboratory. To prevent crosstalk due to coupling between backboard wires, twisted pair is used for any wire lengths greater than about nine inches. Although tests indicate that twice this length could be used under worst tolerance conditions, approximately 23 per cent of the backboard wires are twisted pair. The twisted pair is composed of very fine steel core teflon insulated wires with a capacitance of 8 to 9 micro-microfarads per foot. A network of taper pin ground straps is provided at each 1/2 inch interval over the entire backboard to form a ground plane. The twisted pair ground wires terminate at these ground straps. All framework elements of the module carrying ground currents are gold plated so that the contact resistance between abutting structural members is low and stable over a long period of time despite atmospheric conditions. Common coupling on the DC voltage lines is minimized by the use of very wide strip transmission lines having extremely low impedances. Strip transmission lines are mounted in vertical columns behind the backboard. These lines have an impedance in the region of 30 milliohms (.03 ohms). Timing pulse signals to pulseformers are also available on similar strip transmission lines.

Usually 3 DC voltages are distributed to the printed circuit packages through the strip transmission lines. Up to 6 voltages are available for other miscellaneous card types.

The task of laying out the backboard wiring and positioning the various circuits in such a way as to avoid too much wiring load on any one circuit, as well as the problem of keeping an inventory of all circuit cards, would have been impractical had this not been accomplished by processing the data on a Univac® data processing system. Thirty-five different categories of information, as well as complete production wiring tables, were generated by the Univac system to supply necessary information for production, maintenance, manufacturing inventory and engineering test of LARC. For example, printouts were obtained on wires sorted by lengths, potentially bad cases of stray capacity or crosstalk, spare diode and circuit positions, checks on certain types of logical errors, and general data vital for testing and maintenance. All logical revisions which were made during the test period were handled in this automated and systematic manner.

The automated backboard program guaranteed that wiring changes could be made without fear of overlooking any of the myriad of details involved in the change. Figure 10 shows one page of a printout of the backboard wiring table.

Solid-state power supplies are used throughout the system. Each cabinet has its own set of power supplies and controls so that lead lengths between card library and power supply can be kept to a minimum. The lead impedances between power supplies and the card library are kept low by the use of bus bars with electrolytic filter capacitors distributed along the length of the bars. The supplies are all voltage regulated either by shunt transistor regulators or, in the case of the very high current supplies, transistor driven magnetic amplifiers. The size, cost and time of response

of the power supplies have been reduced by the use of 400-cycle 3-phase input power derived from a motor alternator set. The motor alternator also has the advantage of providing complete line isolation and will produce full output even though power line "dropouts" occur for as long as 3 seconds. The power supply design has proven extremely reliable with voltage regulation much better than the specified 2 per cent.

A major virtue of the circuitry not found in many high speed computer circuits is its adaptability to a simple and effective marginal checking system. Varying the collector return voltage has proven to be an effective way of determining the beta margins of the circuit. Figure 11 is an actual plot showing how the collector return voltage may be varied to determine the beta margin, which is perhaps one of the most variable and critical of the transistor parameters. The extremely difficult problem of switching individual portions of the very low impedance voltage distribution system has been avoided by varying the voltage over the whole unit rather than in a given area. The location of a weak circuit is indicated logically by error detecting circuits which are located at strategic points throughout the logic of the machine. Thus almost no equipment not already present for continuous checking is necessary to provide very effective marginal checking. An overall marginal check can be performed simply by flipping a switch at the engineer's console while an engineering test routine is being run on the unit. A comprehensive voltage monitoring system is used to detect the fact that a particular power supply voltage is drifting out of tolerance. This fact causes visual & audible indications before a voltage drifts far enough out of tolerance to cause actual errors.

The voltage monitor makes use of solid-state elements.

The Computing Unit and Processor are each supplied with a system of fast magnetic registers which are composed of fast-switching tape-wound cores having a read-regenerate or clear-write cycle of 1 microsecond. The fast-register core consists of 4 wraps of 1/8 mil thick, 1/32 wide, 4-79 molybdenum permalloy tape on a 50 mil diameter stainless steel bobbin and has a read, a write and an output winding. The register uses one core and diode per bit and is organized on a word selected basis. As employed in the Computing Unit, information write-in or read-out is done in 60 bit parallel form. Figure 12 is a photograph of a fast register package. The cores and diodes are contained in the small rectangular boxes and are arranged in a 26 x 30 array. Two of these packages are used to form 26 registers of 60 bit storage. More of these packages may be plugged into the Computing Unit to make available a maximum of 99 registers that can be used interchangeably for indexing or arithmetic operations.

To carry out the logical operations in parallel fashion, large quantities of circuits are required. To present some idea of magnitude, a few of the statistics will be listed. 8800 printed circuit cards are used in the basic system, with approximately 3700 in the Computing Unit, 3200 in the Processor and 1800 in the memory. This represents a total of 62,000 transistors in the entire typical system, with approximately 57,000 of them being surface barrier transistors. 28,000 transistors are used in the Computing Unit alone. The number of logical diodes in the system is approximately 2.8 times the number of transistors used. 75,000 wires are used on the backboard of the Computing Unit.

With these large quantities of components used in the system, it is quite obvious that reliability is a major problem and, therefore, a big part of the LARC development program was concerned with component reliability. Many of the basic component selections were made on the basis of reliability rather than cost. All components used in the system were subjected to extensive reliability tests. The resistors used in the circuitry, for example, are of the 1/2 watt size, even though circuit dissipation is in the milliwatt region. The 1/2 watt resistor available at the start of the project proved to be much superior to the smaller wattage sizes. A large engineering effort was required to achieve the high reliability obtained in the LARC printed circuit card connector. The contact pressures are accurately designed to be in the 4 to 6 ounce range per contact. The use of electro-polishing and 200 micro-inches of gold permits the connector to be withdrawn and inserted 400 times while still retaining gold both on the male and female contact area. This is an important point in view of the low voltage and current levels encountered. All circuits are designed to work under worst tolerance conditions assuming 4 per cent variation in DC supply voltages, a 3 per cent variation in the value of the resistors and the end of life transistor beta. Three units of beta over the end of life beta required are specified for new transistors. For example, for a transistor driving 3 loads, an old age beta of 9 is required; a transistor with a beta of 12 minimum is initially inserted in the circuit. Under nominal tolerance conditions the circuit will function even if the beta drops to 6. The most pessimistic calculations of reliability have predicted a mean free error time of at least 11 hours which is 3 hours beyond that called for

by the specifications. Typical power requirements of the system are 15 KVA of 400 cycle power for the Computing Unit, 56 KVA for each memory unit and 18 KVA for the Processor. The power factor is .5 because of the type of regulated power supplies employed. Most of this power is actually dissipated within the power supplies.

Each unit of the system has its own cooling equipment built into the base of the unit. A heat exchange and blower system circulate 75° F maximum temperature air up the backboard and through the card library; the air then returns through the front side of the machine to the base area, thus forming a close circuit path. The circuits will operate over a much wider temperature range but internal cooling is used to guarantee long life and reliability. Operation is reliable over a room temperature range of 32 to 110° F.

The LARC system is being readied for the customer acceptance test. All units of the system are functioning. The Computing Unit, in conjunction with the memory, has been running test routines for many months. Although the overall long-term reliability data on the system is not yet available, preliminary information is very satisfactory. Runs of about 12 hours have yielded one or no intermittent errors. Fortunately, the very few failures encountered thus far have been of the catastrophic variety, such as open or shorted components (probably due to abuse during testing) rather than a change in parameter value which leads to marginal operation and accompanying difficulty in isolation. It is extremely gratifying that no circuit redesign of any sort has been found necessary since the commencement of test. This has led to an

unusually rapid testing of the overall system. The efforts put into very thorough engineering beforehand have paid off handsomely.

Many people were involved in making the LARC program a success and it would be impossible to list them all by name. Recognition must be granted to them for their part in this major engineering achievement.

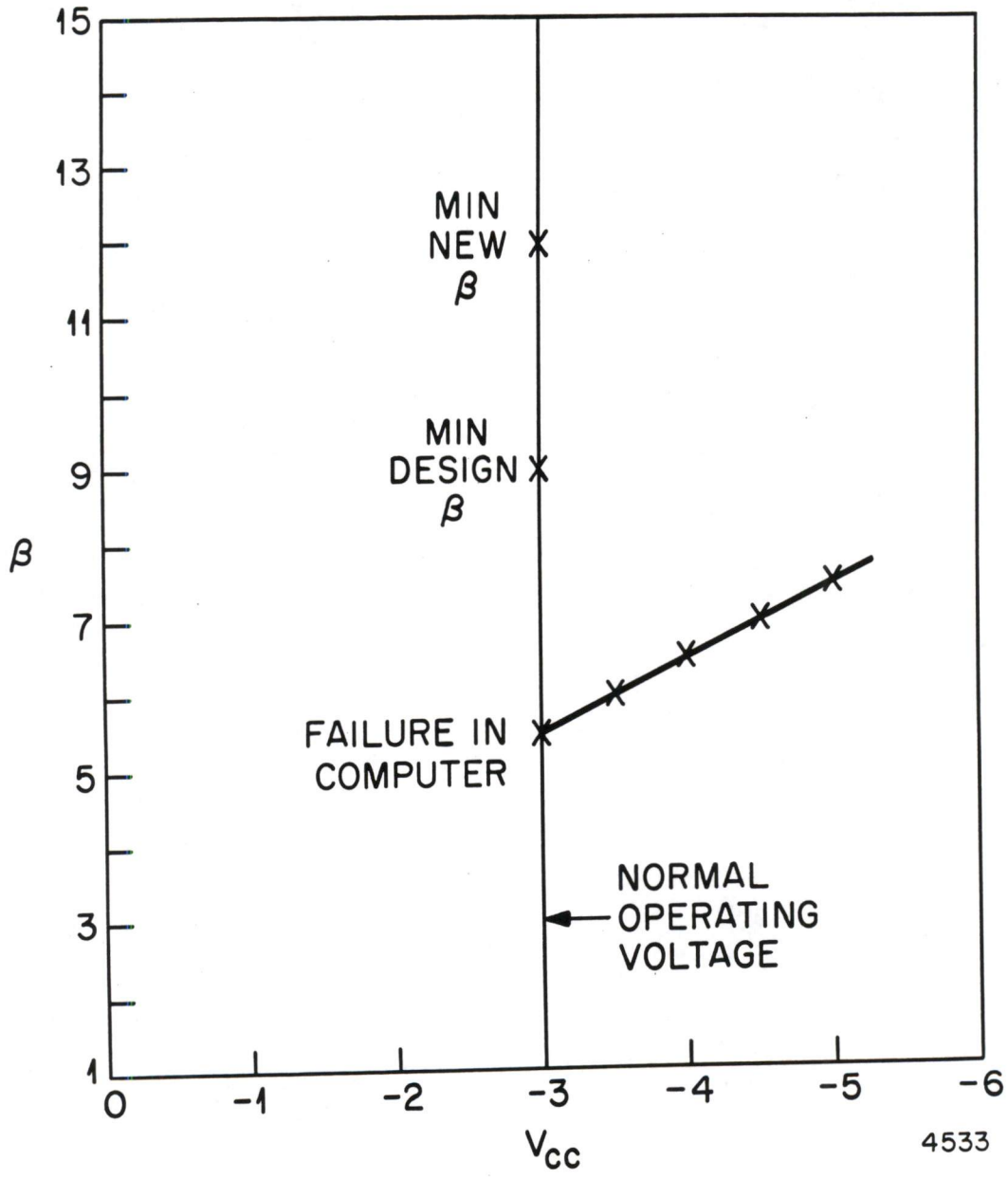

Figure 11. Circuit Failure as a Function of V_{CC} and β

WIRING TABLE FOR LARC COMPUTING UNIT

MODULE 3 TO MODULE 4

LINE	TYPE	COLOR	LENGTH	FROM TERMINAL	TO TERMINAL	LENGTH	WIRED	CHECKED
(1)	SINGLE	WHITE	(3.0)	3B62 UL ORANGE (03B)	4C01 LR BROWN (40B)	( )	( )	( )
(2)	SINGLE	WHITE	(3.0)	3B62 LM WHITE (31A)	4B03 UM YELLOW (14B)	( )	( )	( )
(3)	SINGLE	WHITE	(3.5)	3C62 UL ORANGE (03B)	4C02 UR BLACK (16A)	( )	( )	( )
(4)	SINGLE	BROWN	(4.0)	3B59 LL VIOLET (28B)	4B02 UM ORANGE (13A)	( )	( )	( )
(5)	SINGLE	GREEN	(4.0)	3B63 LL ORANGE (23B)	4B05 LM GREEN (35A)	( )	( )	( )
(6)	SINGLE	GREEN	(4.5)	3B60 LM WHITE (31A)	4B03 LL BLUE (27B)	( )	( )	( )
(7)	SINGLE	YELLOW	(4.5)	3D63 UR BLACK (16B)	4C05 UL YELLOW (04A)	( )	( )	( )
(8)	SINGLE	YELLOW	(5.0)	3B57 UM VIOLET (08B)	4B01 LL YELLOW (24B)	( )	( )	( )
(9)	SINGLE	BROWN	(5.0)	3B57 LR BLACK (36A)	4B02 UR BLUE (17B)	( )	( )	( )
(10)	SINGLE	WHITE	(5.5)	3B57 UM GRAY (09B)	4B01 LR BROWN (40B)	( )	( )	( )
(11)	SINGLE	BROWN	(5.5)	3B57 UL BLACK (06A)	4B02 UL ORANGE (03B)	( )	( )	( )
(12)	SINGLE	YELLOW	(5.5)	3B60 UR VIOLET (18A)	4C02 UR BLACK (16B)	( )	( )	( )
(13)	SINGLE	GREEN	(5.5)	3B63 LR GRAY (39B)	4C07 UR WHITE (21A)	( )	( )	( )
(14)	SINGLE	YELLOW	(5.5)	3B63 LM YELLOW (34A)	4C01 LL YELLOW (24B)	( )	( )	( )
(15)	SINGLE	YELLOW	(5.5)	3D63 UR VIOLET (18B)	4C07 UL BLACK (06A)	( )	( )	( )
(16)	SINGLE	WHITE	(5.5)	3E60 UR WHITE (21A)	4E05 UR BROWN (20B)	( )	( )	( )
(17)	SINGLE	BROWN	(5.5)	3E60 UR VIOLET (18A)	4E05 UR BLUE (17B)	( )	( )	( )
(18)	SINGLE	WHITE	(5.5)	3E61 UR WHITE (21A)	4E06 UM YELLOW (14B)	( )	( )	( )
(19)	SINGLE	WHITE	(5.5)	3E61 UM GRAY (09A)	4E06 UM BROWN (10B)	( )	( )	( )
(20)	SINGLE	GREEN	(5.5)	3E61 UL ORANGE (03A)	4E06 UL ORANGE (03B)	( )	( )	( )
(21)	SINGLE	YELLOW	(5.5)	3E62 UR VIOLET (18A)	4E06 LL YELLOW (24B)	( )	( )	( )
(22)	SINGLE	GREEN	(6.0)	3D63 UR BLUE (17B)	4C07 UR GREEN (15A)	( )	( )	( )
(23)	SINGLE	BROWN	(6.5)	3B62 UR VIOLET (18A)	4C02 UL ORANGE (03B)	( )	( )	( )
(24)	SINGLE	BROWN	(6.5)	3D60 UL BLACK (06A)	4E05 LM WHITE (31B)	( )	( )	( )

Figure 10.

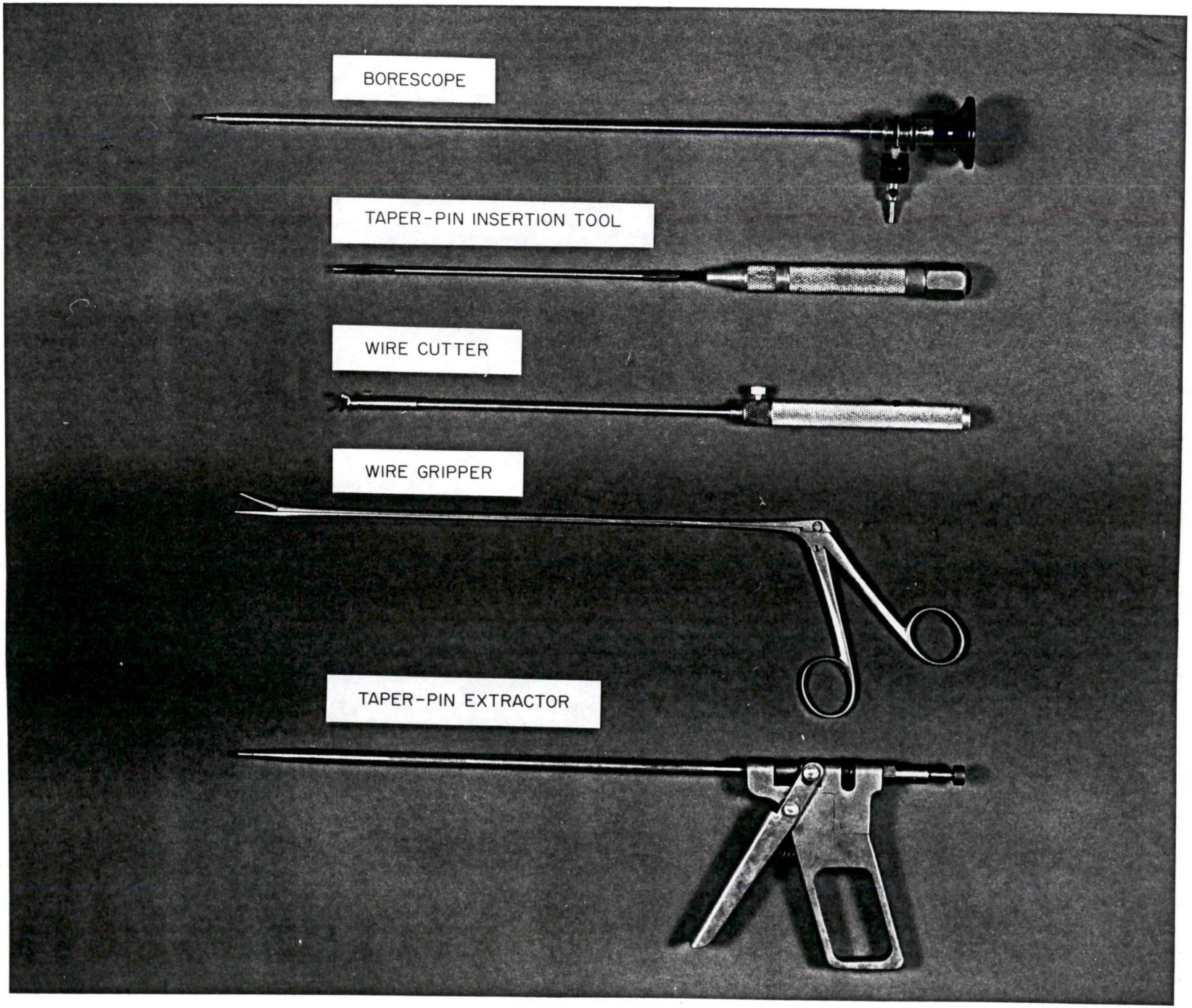
BORESCOPE
TAPER-PIN INSERTION TOOL
WIRE CUTTER
WIRE GRIPPER
TAPER-PIN EXTRACTOR

Figure 9.

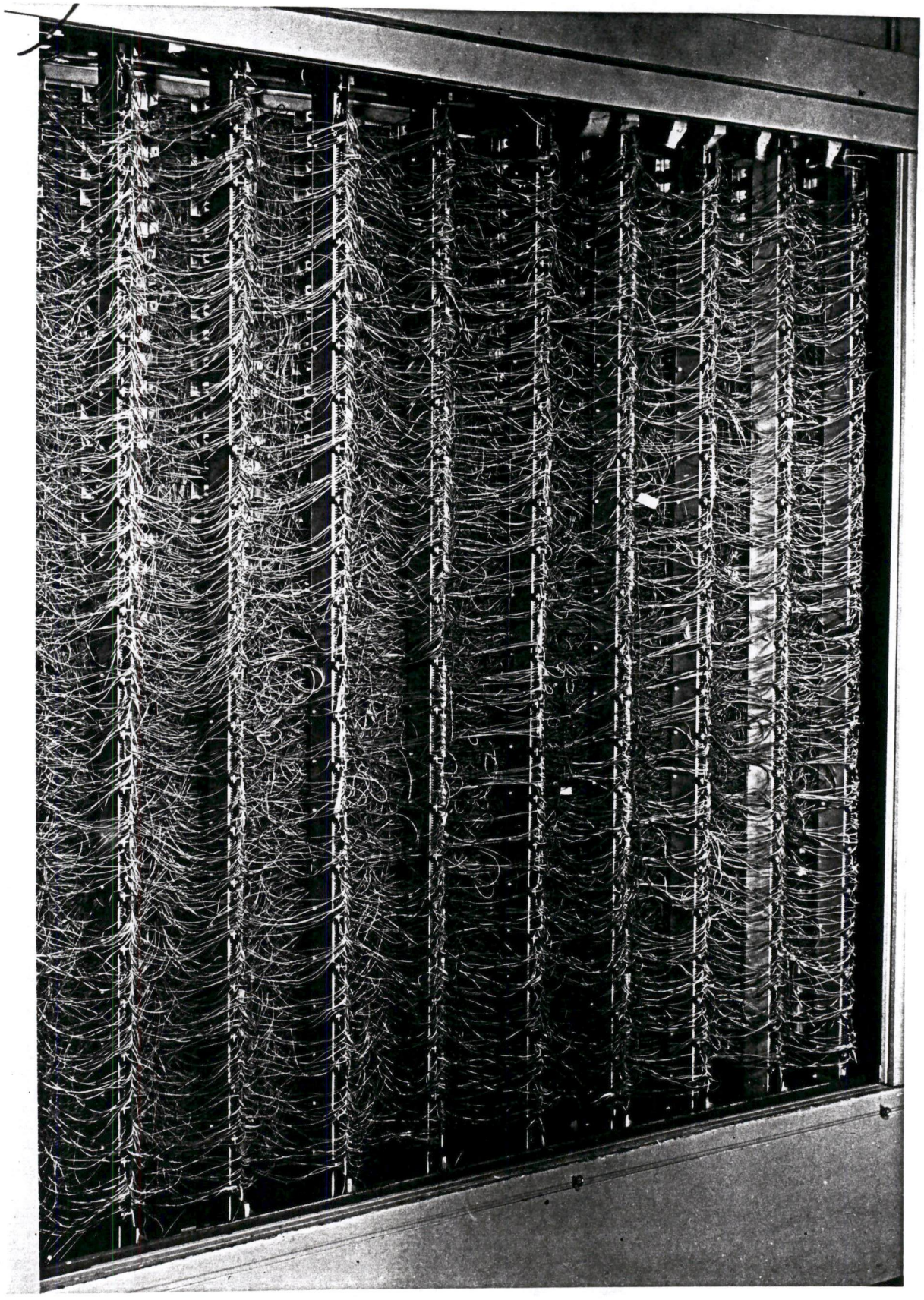

Figure 8.

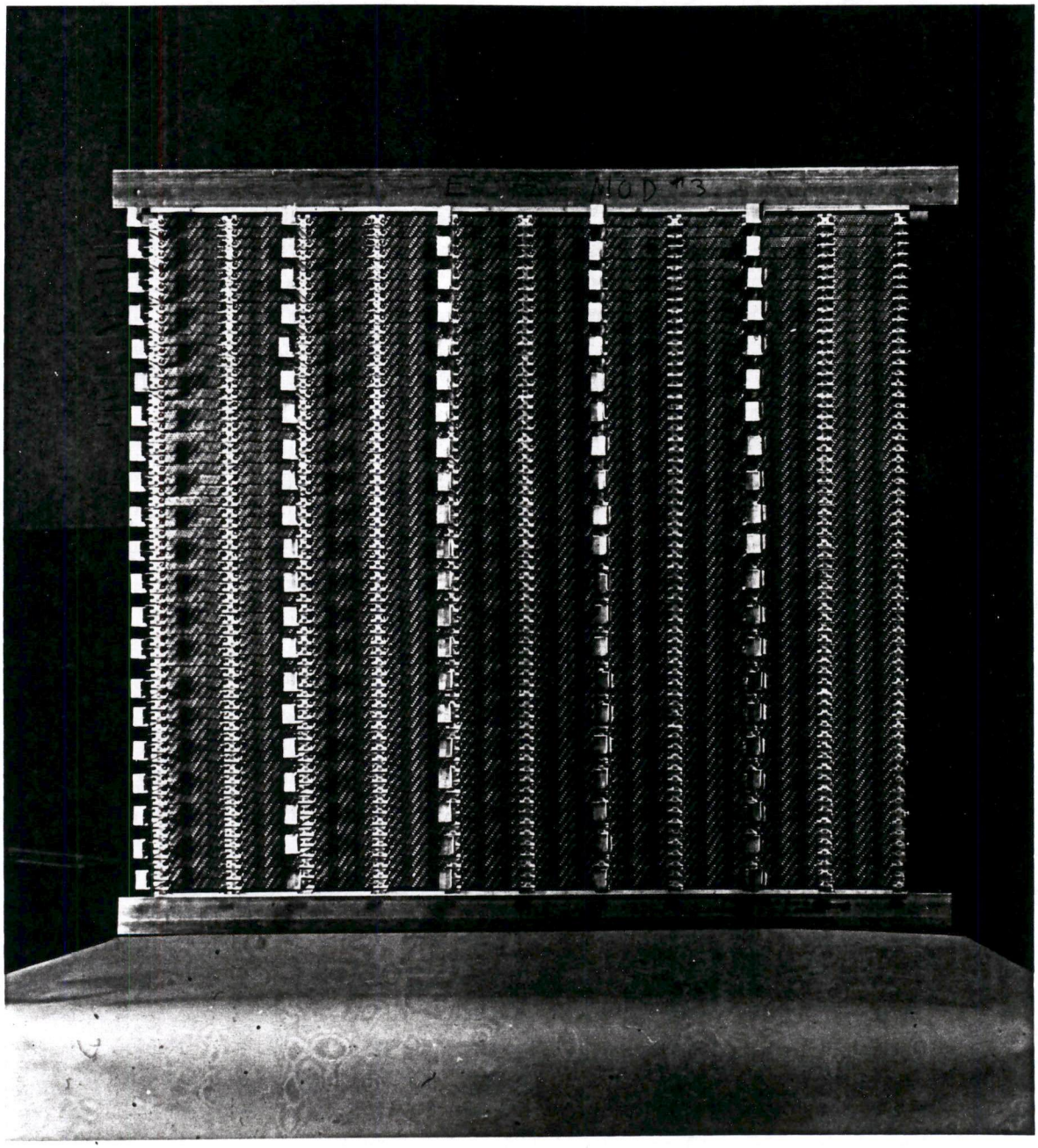

Figure 7.

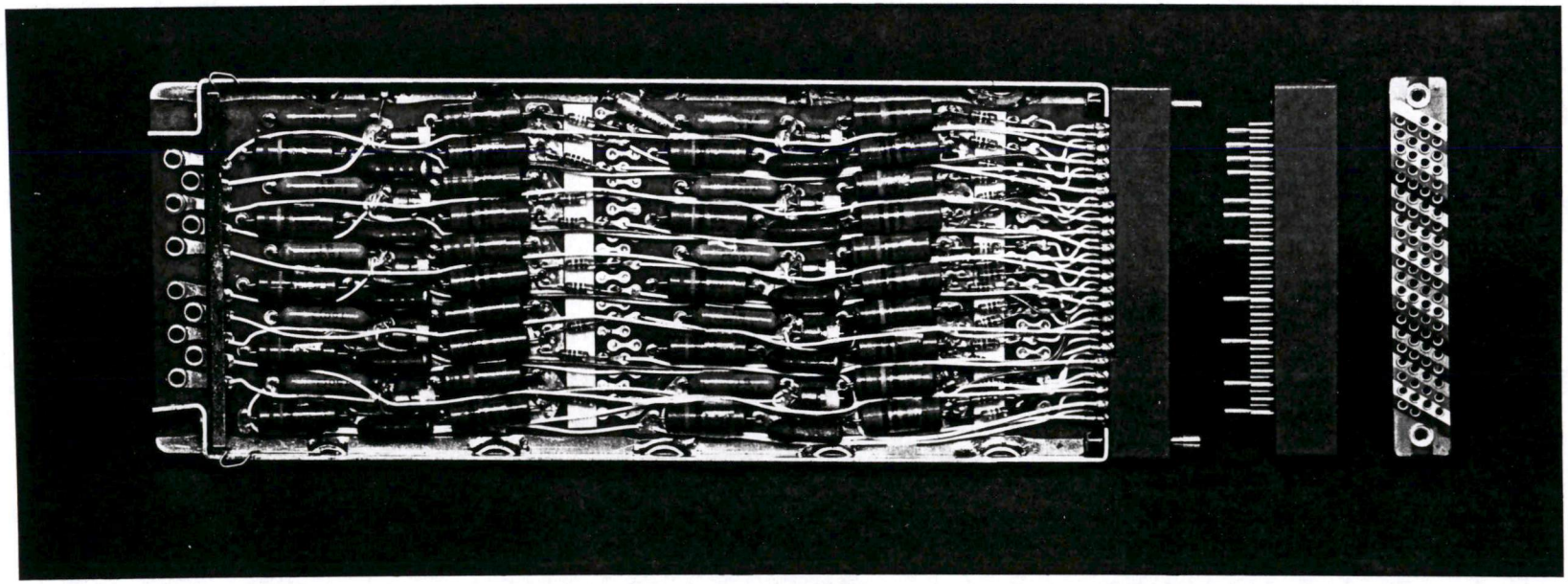

Figure 6.

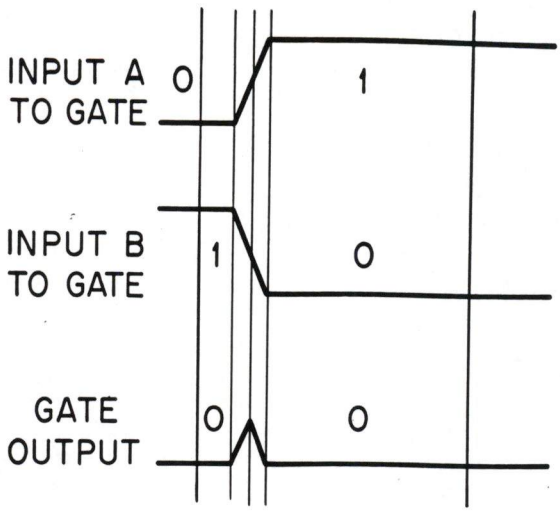

Figure 5a. "Spike" Formed Due to
Overlap of Gating Signals

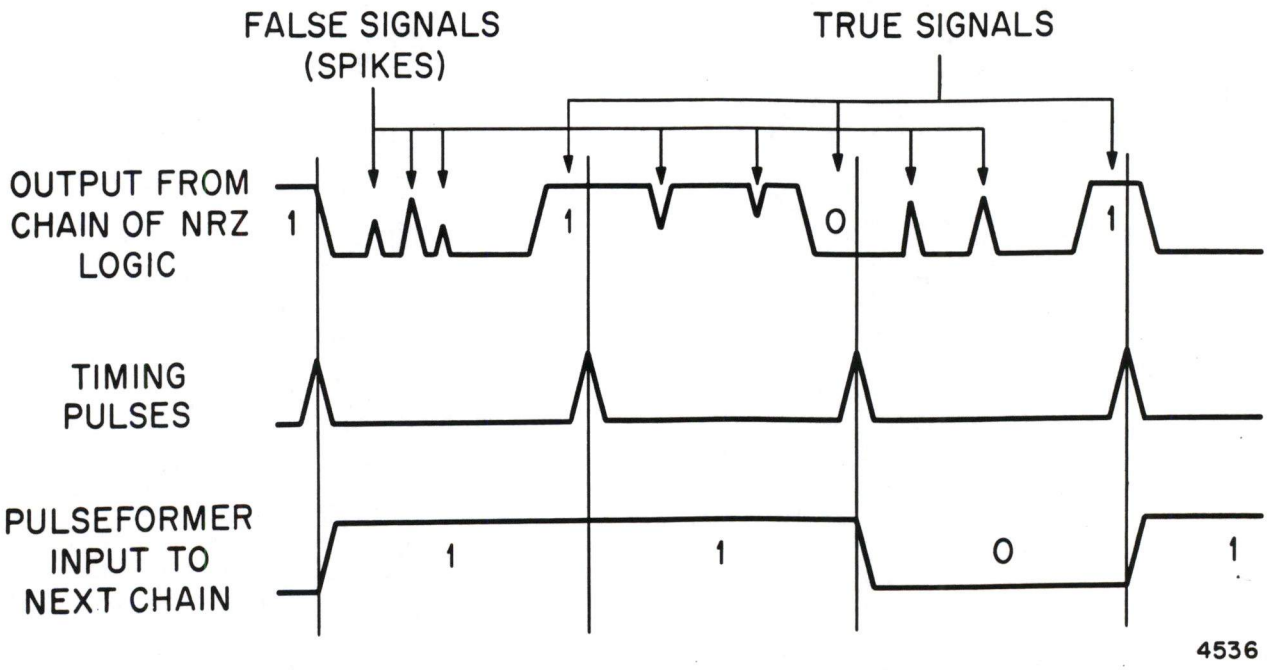

Figure 5b. Discrimination Against "Spikes" Occurring
in a NRZ System Using Clocking Methods

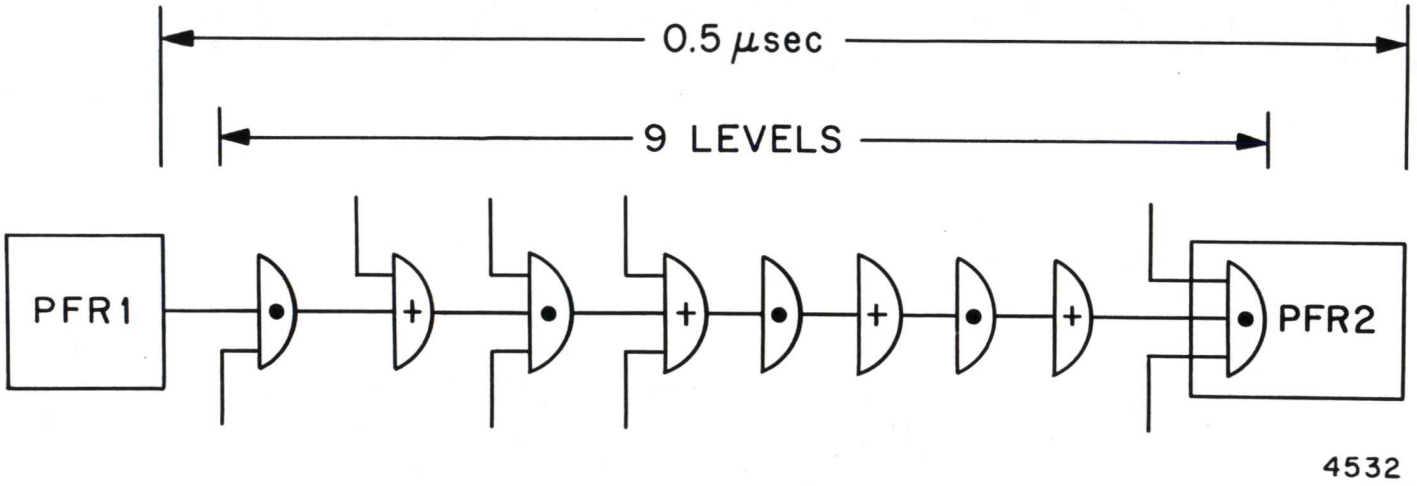

Figure 4. Logical Chain

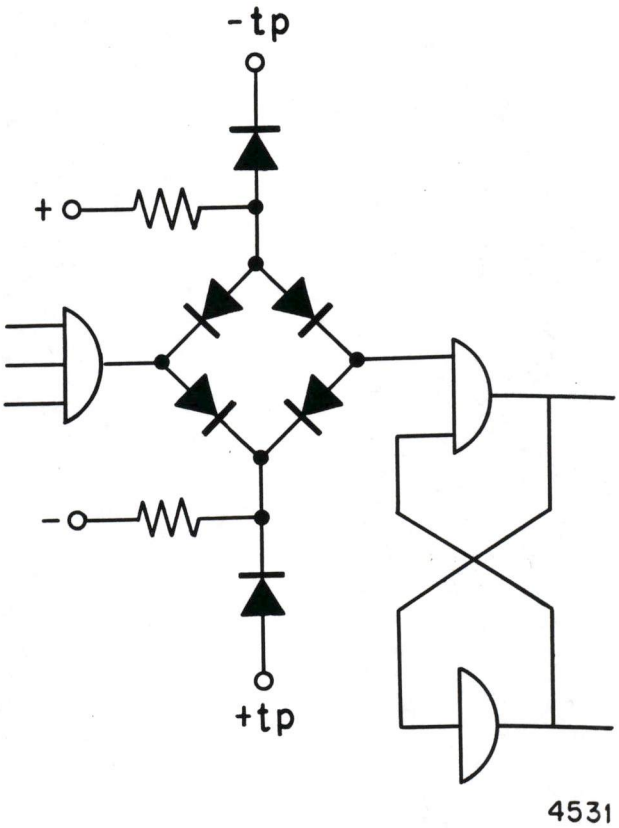

Figure 3. Pulseformer

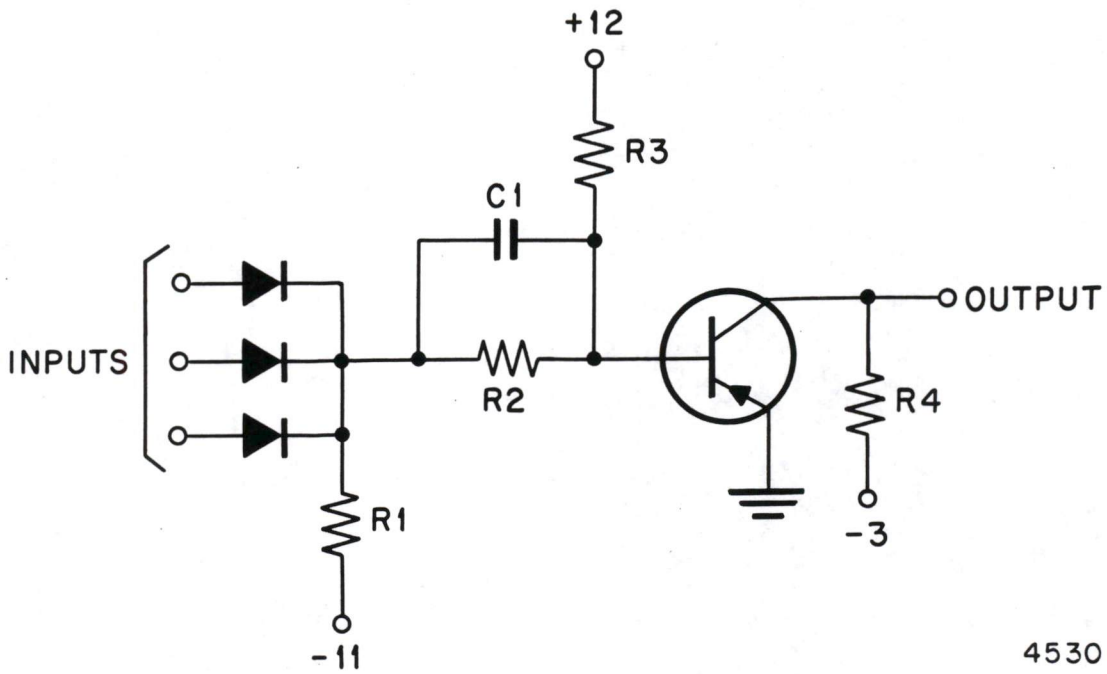

Figure 2. Basic High Speed Circuit

$$\text{Figure of Merit} = \frac{(\text{Drives})\ (\text{Logic Levels})\ (\text{Repetition Rate})}{(\text{Transit Time})\ (\text{Cost})}$$

4534-R1

Figure 1.

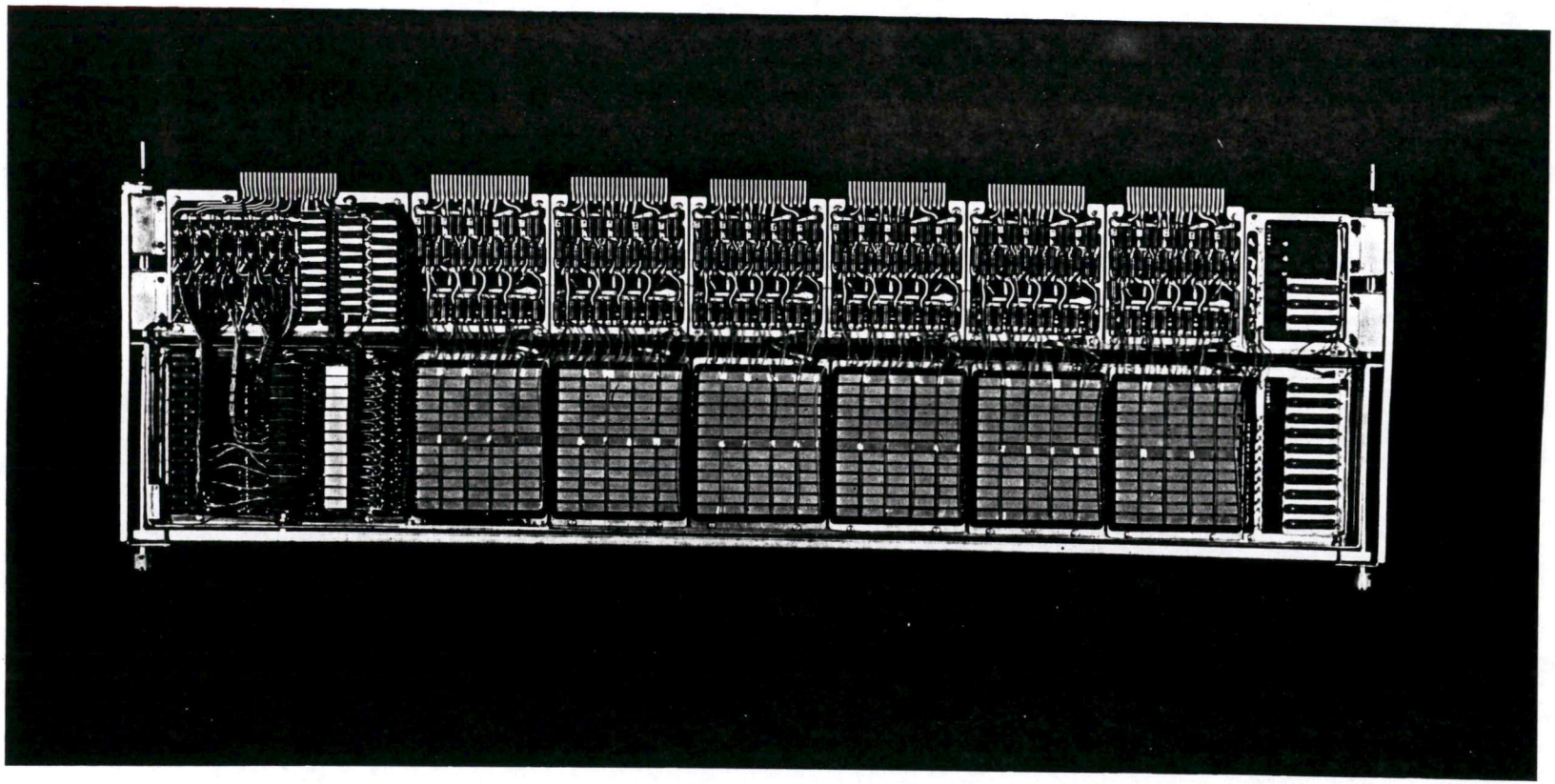

Figure 12.