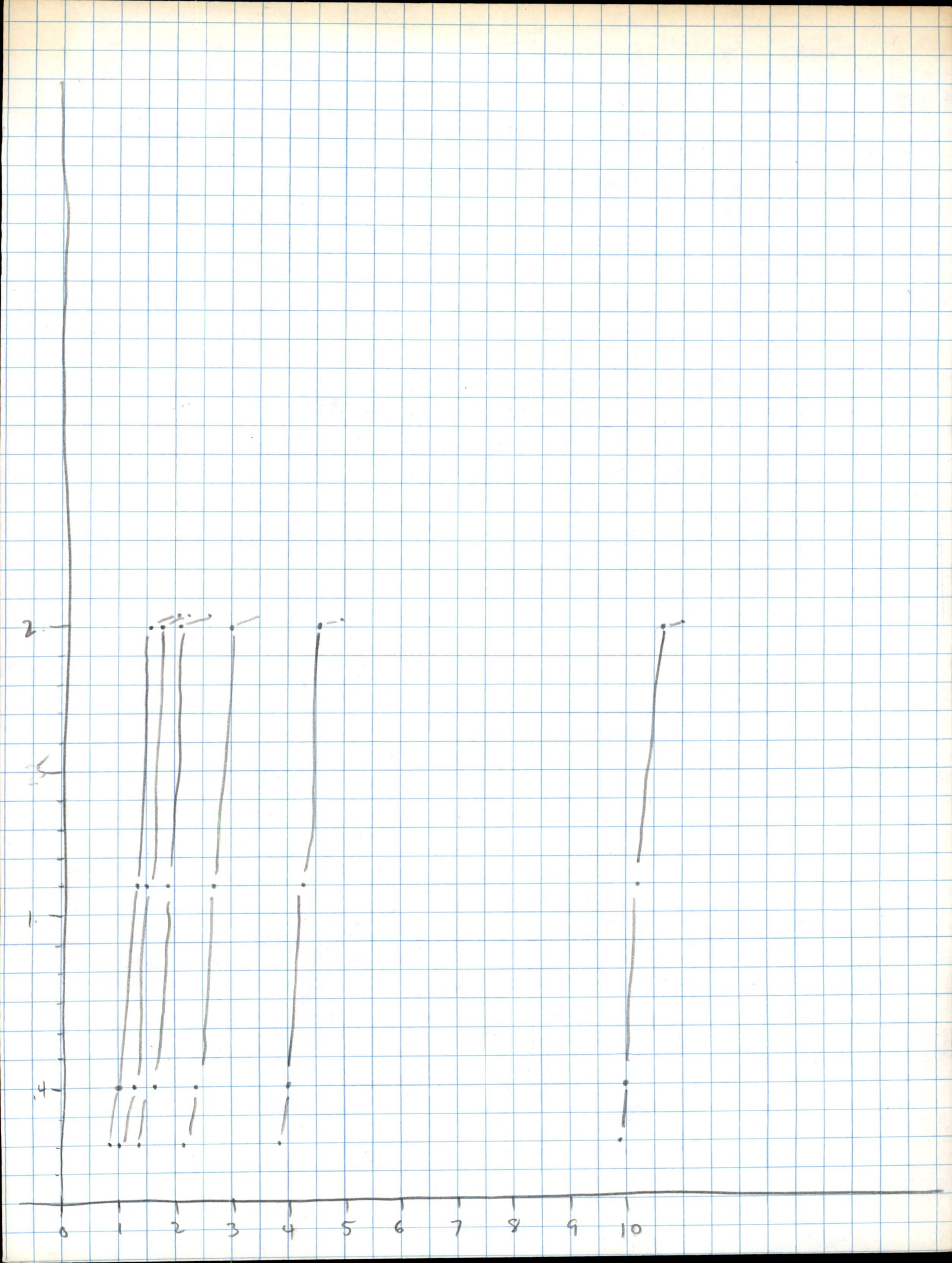
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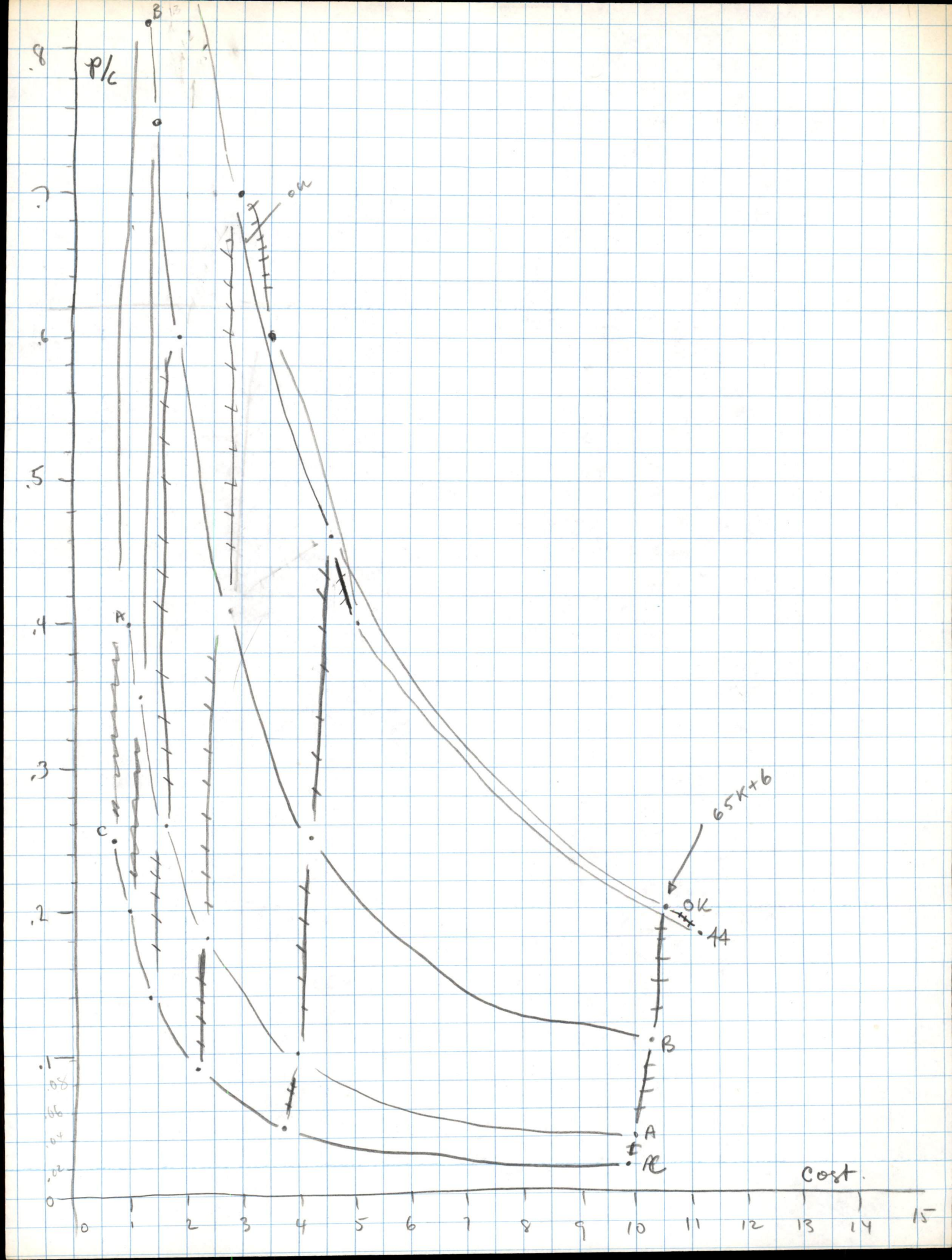
p/c
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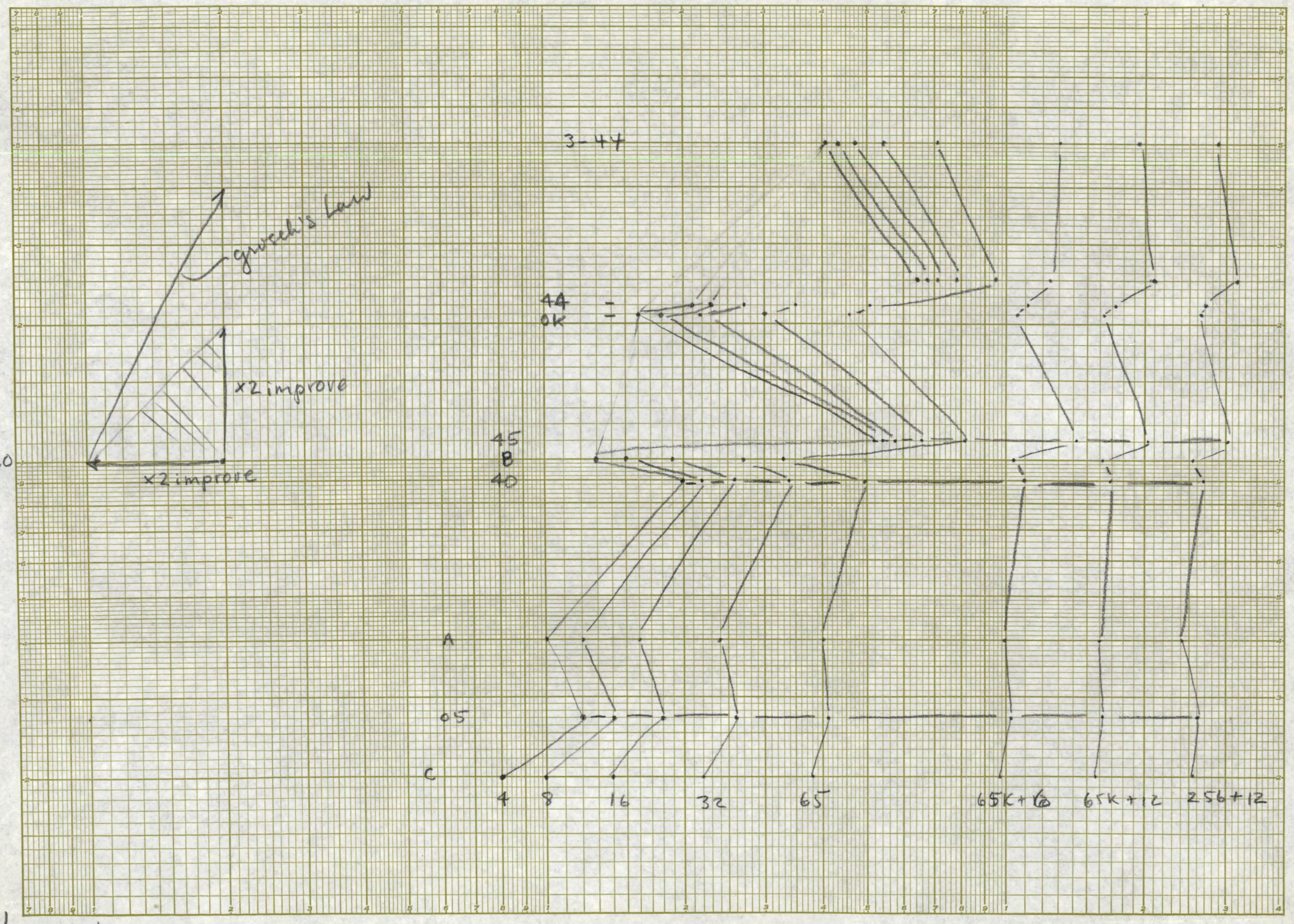
NO. 3123. LOGARITHMIC: 2¾ BY 2 3¾-INCH CYCLES.
CODEX BOOK COMPANY, INC. NORWOOD, MASSACHUSETTS.
PRINTED IN U. S. A.



GB
6/17/74

OBSERVATIONS

-1. Dilemma: 11 hard to build fast and cheaply at low end, although semis now overcome these problems. Instruction set + UNIBUS (can be changed) has problems of user space >32 or 64 K words. What if we change instruction set to get larger addresses?

0. Real problem is that we don't speak #'s. Each person has a different configuration and objective function in mind. We must get to point that one strategy can be proved (with $ #'s) better than another.

1. Development group has had trouble in presenting alternatives in a way to be looked at. As a result, projects have to be started without homework... frustration ensues when realigned.

2. Tend to push a given machine too far to overlap another machine. Ie. every machine does everything and competes. This is a small problem compared with the plethora of operating systems.

3. I have a queasy feeling about the strategy I see, because it is too much like the software strategy. Everyone is happy with incremental, tiny projects that don't take us anywhere, and produce a number of competing systems, each with below average capability.

   A. We need spare people resources.

   B. $ expensive too.

   C. The overall structure isn't aesthetically pleasing. Transition problem from 11 to 10.

   D. Low end could use much more. (Not for A.K., but because the trend is to distribute, and solve problems by part.)

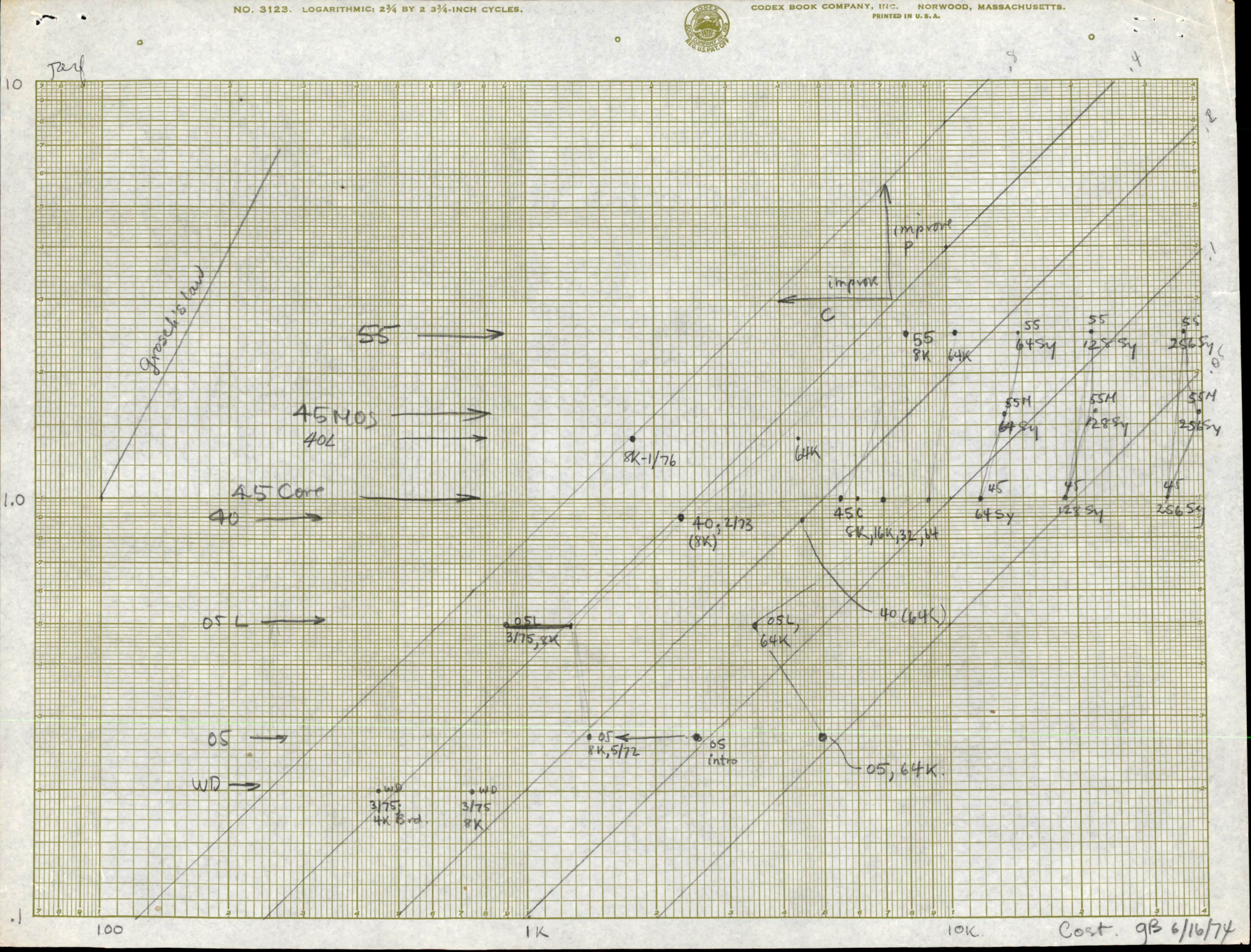
4. Must build carefully at knee of cost/performance curve.

5. We tend to look at the $.processor not $.computer systems. This optimizes only 1 point. Also, we think in instructions/second, not instructions/month or terminal cost, etc.

6. Don't realize that as CPU speed increases, the memory size has to also, thus making CPU cost unimportant (in the IBM series, a machine is relatively balanced with 1 byte of memory for each instruction per second the processor executes). As memory is added, so must the peripherals be. Thus, system balance problem is even worse. Eg. assuming a KA10 requires about 160 K worlds to be balanced (640 K bytes.) Assuming an 11/45 is roughly the same speed, then it is under-memory by a factor of 4 now. Even 11/40 is memory poor.

7. Boxes and configurations are probably the real hidden cost and delays here. We're only slightly on the way to solving the problem. A single backplane for low and mid (WD to 402) would go along way. 40, 45, 55, and 85 would all be relatively different.

8. We must do at least a factor of two projects: costs must be better and performance/cost must be greater than 2.



9.5 3.2 6.3 .27 p.1 old 700ns 4

	05	40	45	A	B	C	OK	44	3/44	70
P	.27	.9	1.	.42	1.1	.2	2.1	2.1	5	2.5
# P.	1.0	1.8	5.0	.8	1.1	.6	1.4	1.9	3.9	6.3
.2 C(4K)	1.2	2	5.2	1.	1.3	.8	1.6	2.1	4.1	6.5
P/C	(.22)	.45	.2	.42	.85	.25	1.3	1	1.2	.38
.4 C 8K	1.4	2.2	5.4	1.2	1.5	1.	1.8	2.3	4.3	6.7
P/C	.19	.4	.19	.35	.75	.2	1.2	.9	1.2	.37
.8 C 16K	1.8	3.6	5.8	1.6	1.9	1.4	2.2	2.7	4.7	7.1
P/C	.15	.35	.17	.26	.6	.14	.95	.8	1.1	.35
1.6 C 32K	2.6	3.4	6.6	2.4	2.7	2.2	3.	3.5	5.5	7.9
P/C	.1	.26	.15	.18	.41	.09	.7	3.2 .6	.9	.32
3.2 C 65K	4.2	5	8.2	4	4.3	3.8	4.6	5.1	7.1	9.5
4.3 P/C	.06	.18	.12	.1	.25	.05	.46	.4	.7	.26
9.2 65K+6	10.2	11	14.2	10	10.3	9.8	10.6	11.1	13.1	15.5
P/C	.02	.08	.07	.04	.11	.02	.2	.19	.4	.16
15.2 65K+12	16.2	17	20.2	16	16.3	15.8	16.6	17.1	19.1	21.5
P/C	.017	.05	.05	.026	.066	.013	.13	.12	.26	.12
25K 256K+12	26.	26.8	30	25.8	26.1	25.6	26.4	26.9	28.9	31.3
	.01	.03	.03	.016	.042	.008	.08	.08	.17	.08

3.2 12 .27 26

.01→ 1.2

COMPANY CONFIDENTIAL

Gordon Bell

digital INTEROFFICE MEMORANDUM

TO: Operations Committee
CC: R. Clayton
W. Long
J. Marcus
R. Savell
E. Kramer

DATE: June 27, 1974

FROM: Andy Knowles

DEPT: Small Computer Products

EXT: 3043 LOC: 5-2

JUL 01 1974

SUBJ: 11 STRATEGY SUMMARY

The following are the machines the users and the builders agreed to at 5 P.M., 6/26/74.

Machine #	Description	Speed	Cost (8K mem box P.S.,etc.)	First Ship
PDP-11/05L	2 Board (incl mem) replacement for PDP-11/05	2.0 µsec	$1.1K est	3/75
PDP-11/05 HM	Faster 11/05L with memory management 3 boards (incl memory & memory management)	1.2 µsec	$1.4K est	7/75
PDP-11/44	MOS Memory Speed 11, user µcode, excel-lent I/O Bandwidth	0.6 µsec	$2.3K est	6/76
PDP-11/55	11/45 Life Extender Fast to market machine	0.4 µsec	$9.0K	6/75
PDP-11/85	Low Cost PDP-10 This is not an 11!	1.4 µsec	$3.4K	9/76

We also agreed to:

1) Continue work on WD chip set, in July circulate the proposed machine for review after two - three more weeks of builders work. It is expected that this machine will be a PDP-11 instruction set compatible, non-unibus LSI machine aimed at the computer-on-a-board market and the VT51, etc.

2) Adopt the management consultant philosophy expressed previously and appoint three management consultants as chairman of 11 steering committees.

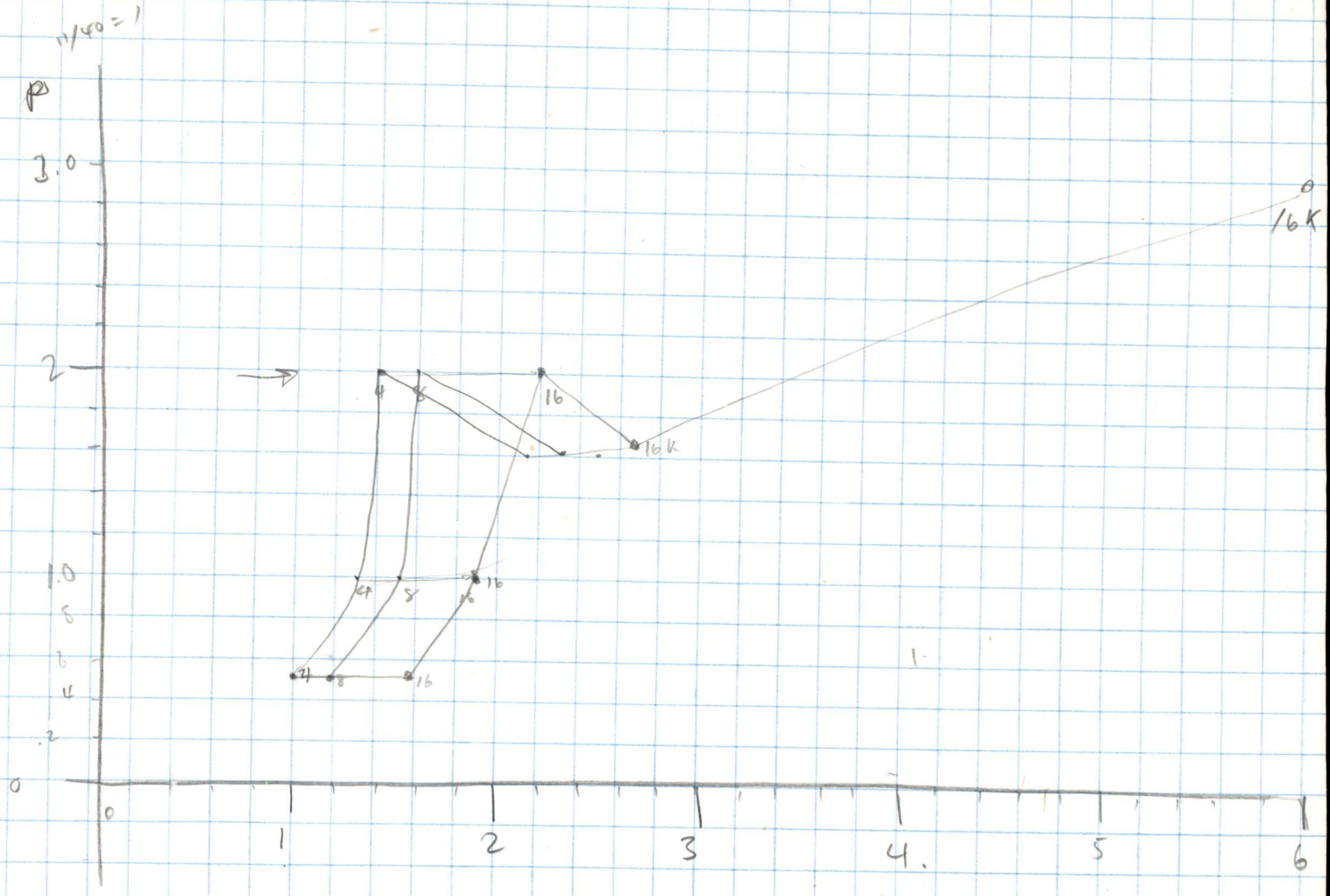
Bill Long	chairman	low end	11/05 WD PDP-11/05L PDP-11/05HM
Julius Marcus	chairman	mid - upper end	PDP-11/44 PDP-11/55
Ed Kramer	chairman	overlap end	PDP-11/85

3) Sell to other users via management consultants.

4) Meet again in September.

5) Robin Frith will act as major communicator.

/smc


P
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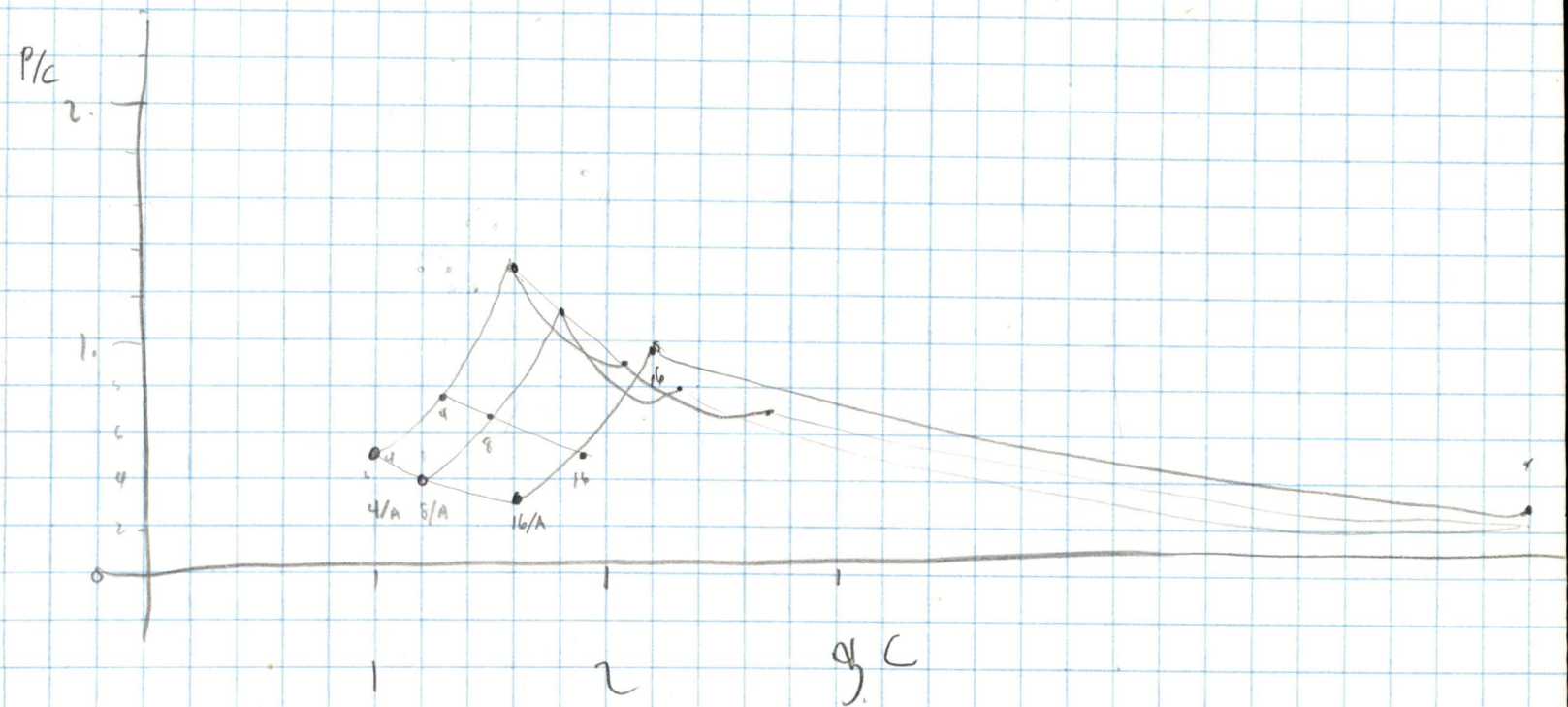
P/C
2.
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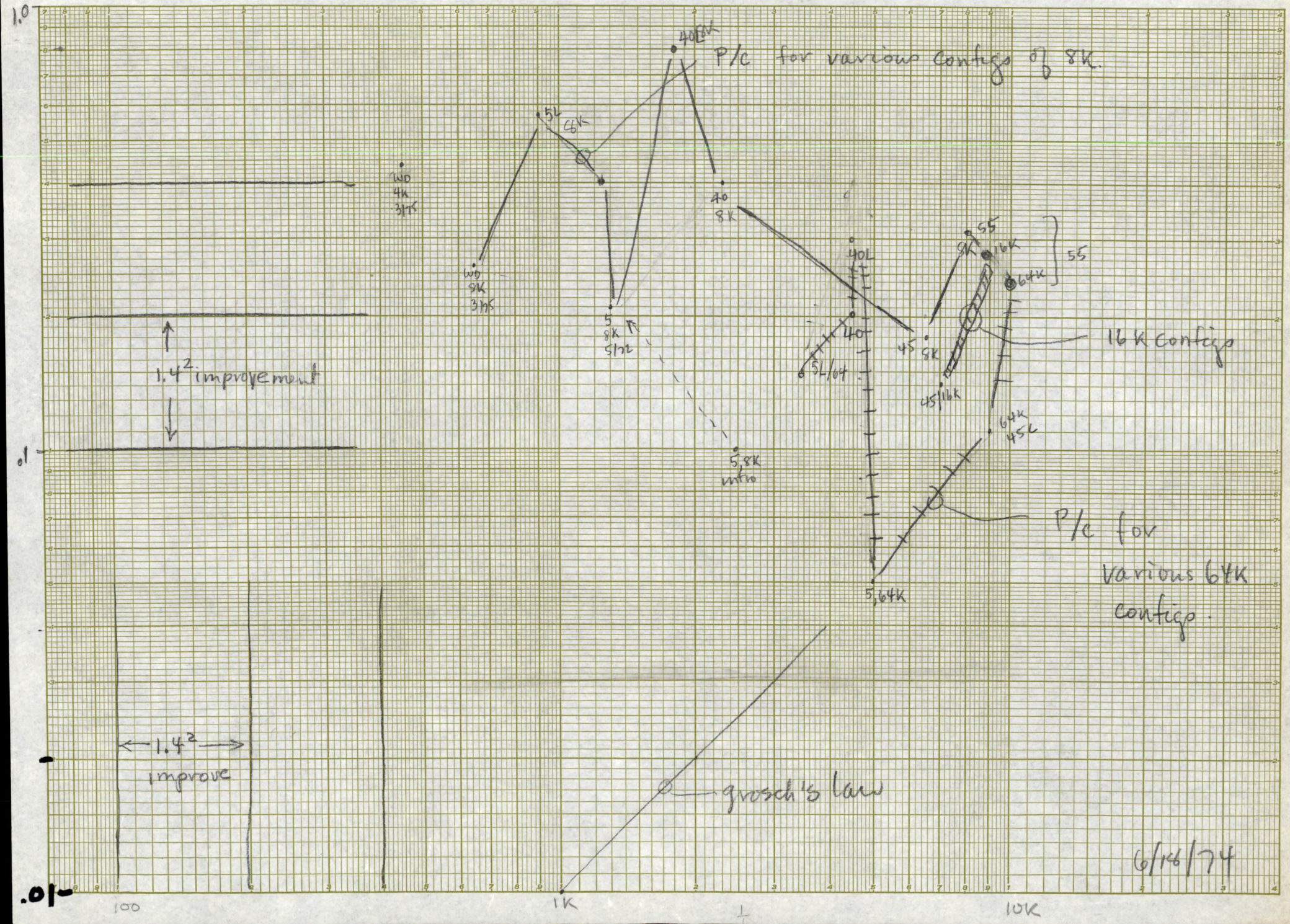
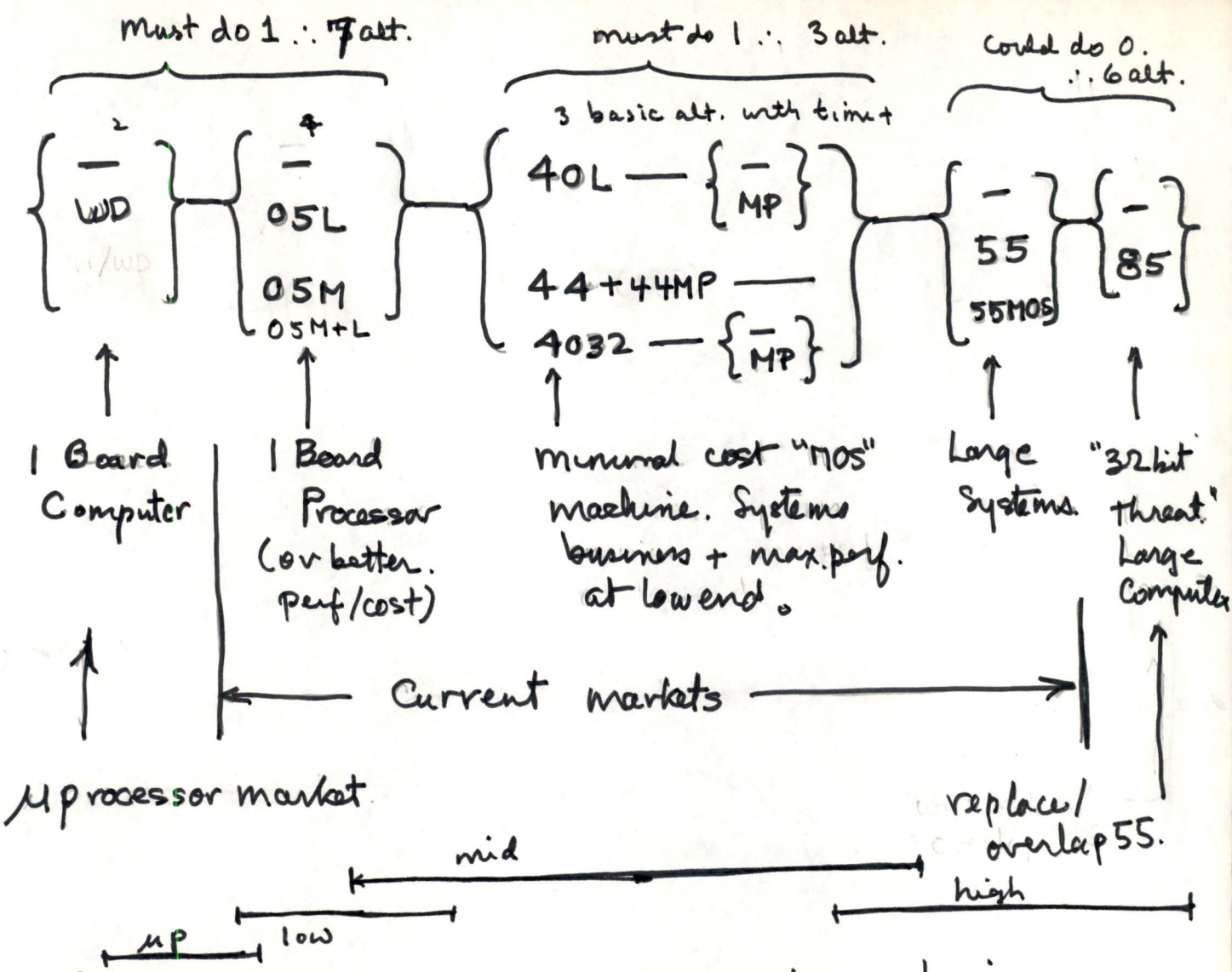
8/A
16/A
1
2
q/C



GB
6/17/74

	P/C	TIME (REG +) (PERF.)	TIME FP+	COST (MEM.)	1st DELIVERY	OPTIONS	PROBLEMS AND [ADVANTAGES]
WD		5? (2.0)	40	45 (4K board only)	3/75	FP, user microcode.	Risk. Config. def. needed. What about serial bus, UNIBUS, WD bus, no bus. [fast micro-code,FP, cheaper bus, processor-on-a-chip.]
05L		2.0 (.5)	150	85 1.1 (8K)	3/75	--	OK
05M		2 + (.5)	150	1.3 (8k)	6/75	Mem. mgmt.	OK
40L		.7 (1.4)	10~20	1.8 (8K)	12/75	DEC micro-code	Can it be done easily?
4032		.6 (1.6)	10~20	? (8K)	12/75	"	How much?
44+44MP		.6 .3 (1.6 3.2)	10~20	2.4 (16K)	6/76-6/77?	User 4 code; multi-PC	High risk. New busses and options. [nice structure]
55		.4 (2.5)	3~4	8K (0)*	6/75	45	Lots to do. [Faster than MOS machine at core prices. Reliable. Big enough memory. Realize 45 potential.]
55 MOS		.6 (16)	3~4	5K (0)	3/75?	45	Me too. Won't be better (cheaper) and much faster than MOS machines.
85		1.0 (2)	3~4	7.5 (32KW)	9/76	11 inst. too?	New busses and options? Software? Probably must execute 11 code. [Good against 32 bit vis a vis address space. 11/55 is higher performance?]
05		3.7 (.27)	250	1400 (8K)	5/72		
40		1.1 (.9)	20	2.3 (8K)	2/73		
45		1 (1)	3~4	8.7 (32K)	5/72		



Grammar expressing alternatives being Considered as per early June 1974.

gfB.

Easy solution: Is it a good one?

- Pick 1 each from each categories.
- Development is in place. Everyone has a project.
- Something for each market group.
- Sense: WD; 05L iff cost +1 board is met; 40L; 55; 85.

11/55

GB
6/17/74

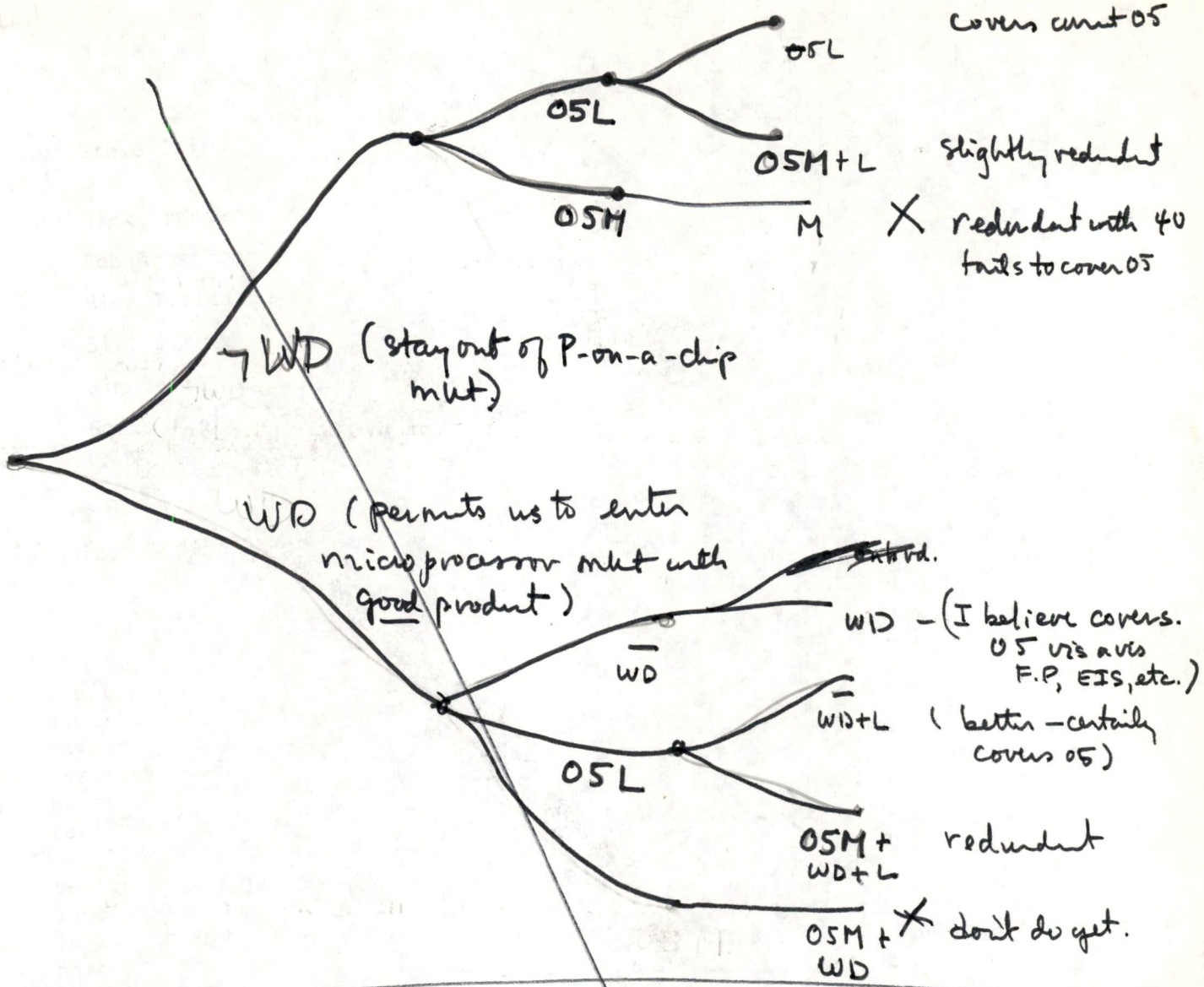
We're behind in doing this great product:

MACHINE	PC COST	PERF.	76 MEMORY (64, 128, 256K) Cost	TOTAL COST ($3XM_p+Pc$)	COST/PERF
45	5	1	2.3*, 4.6, 9.2	11.9, 18.8, 32.6	11.9, 18.8, 32.6
45 MOS	5	1.6	2.9, 5.8, 11.6	13.7, 22.4, 39.8	8.5, 14, 24.9
55	8	2.5	2.3, 4.6, 9.2	14.9, 21.8, 35.6 (25%) (15%) (10%)	6.0, 8.7, 14.2

ALSO ADDRESSES SELLING LOTS MORE MEMORY AND PERIPHERALS. NOW LET'S GET THE SOFTWARE AND TROUNCE HP IN TIME-SHARING AND BATCH.

HAS ADVANTAGE OF BEING FASTER THAN MOS, AT CORE PRICES. WE SHOULD BE ABLE TO STAY OUT OF COMPETITORS REACHES.

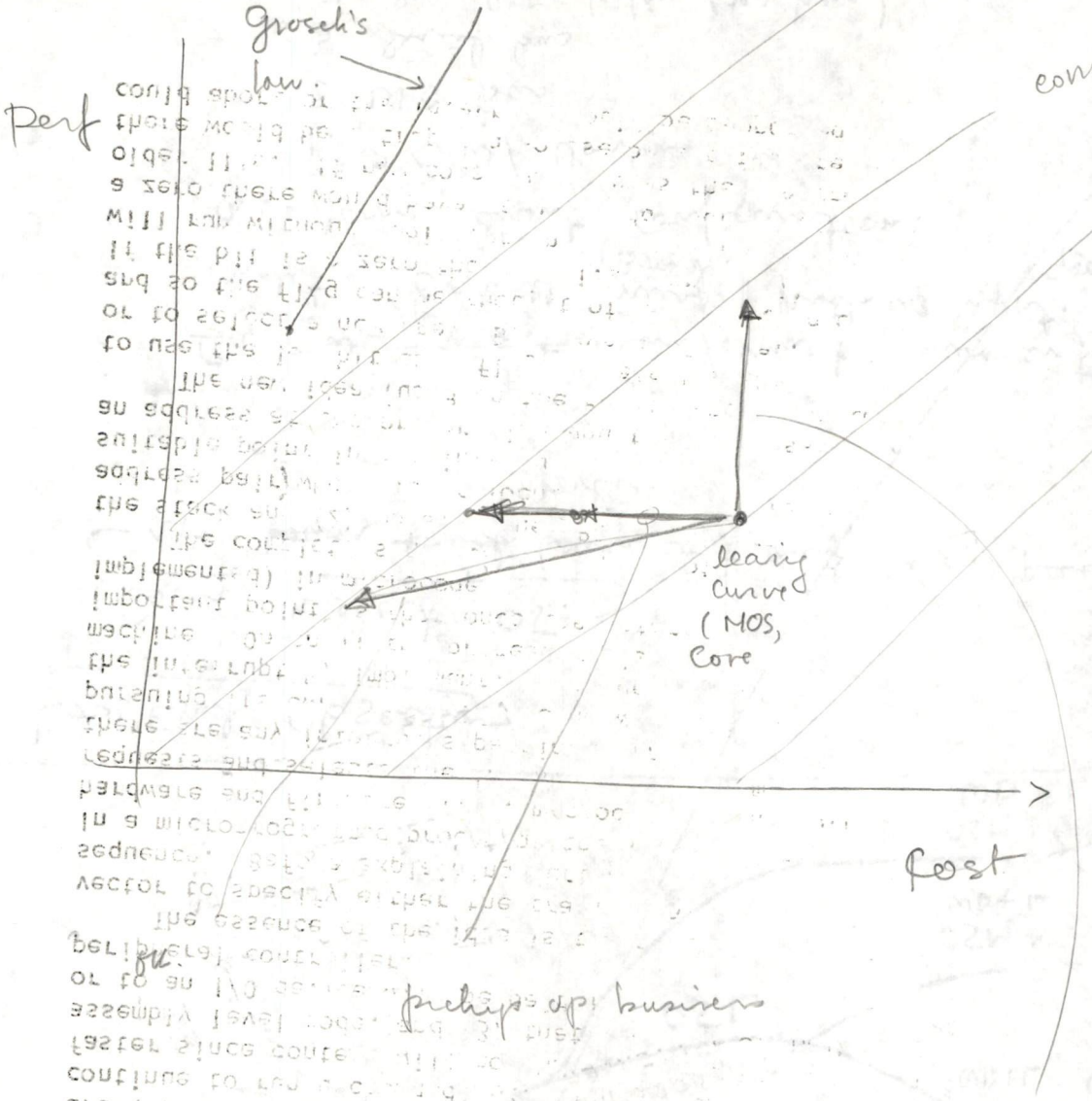
*$580/16K FOR CORE; $734 FOR 16K MOS



Low End Objectives

1. Cover present 05.
   at ~~lower~~ ~~much~~ lower cost and x 2 ~~price/perf.~~ perf/price

2. ~~Can we, must~~ Can / must we enter C-on-a-board mkt. Or will micros push up apart? Can we wait for good bipolar to samurai?
   questions about (Board) configuration:
   1. 0-2K w/ Unibus
   2. WD Bus
   3. Serial bus
   4. Single interface (no bus.)

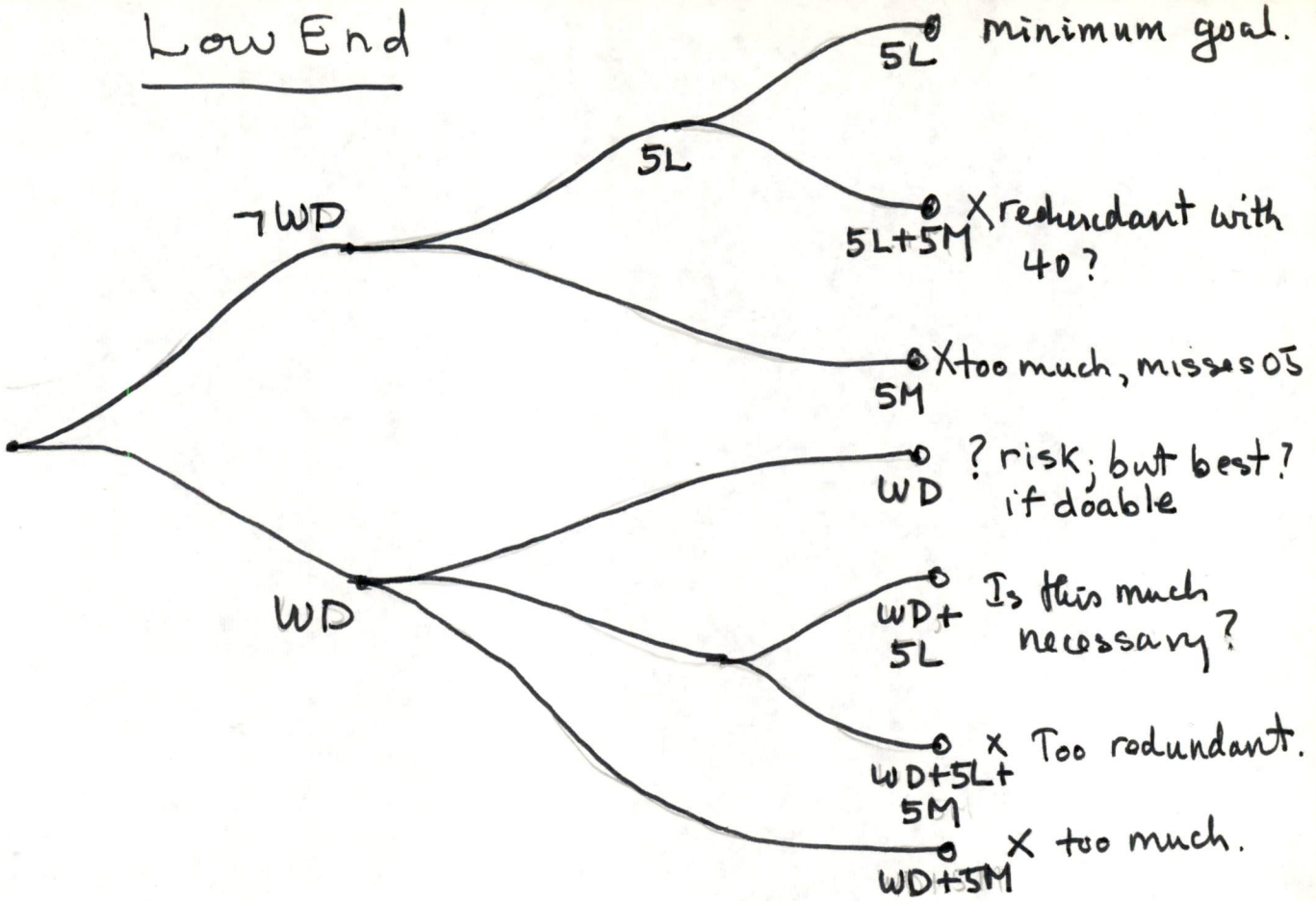


perhaps appl business

I doubt if this is valid. Since Pc is already ok.

1. Show iso- p/c.
2. Movement along K = #, K = perf.
3. Grosch's law.
4. Observe
   a. 8K. case; — too small } ∀ Pc
   b. 64 K case ok
5. a. Systems right.

Low End



Low End Objectives

1. Cover 05 at lower price (850?) and perf/cost x 2 of 05. Get Processor on a board.
2. Can/must we enter Computer-on-a-board market? Or will P-on-a-chip pick us apart? Can we wait for better bipolar to do this?
3. Define board for very low end.
   1. 1~2K~4K w/ Unibus.
   2. WD Bus
   3. Serial bus.
   4. Simple interface (eg. Processor Modules).

GB 6/16/74

To: Steve Teicher

CC: Dick Spencer
Bob Armstrong
Mike Titlebaum
Bill Strecker
Jim Bell
Gordon Bell

From: Chuck Kaman
Date: June 3, 1974
LOC: R&D
Phone: x4365

Topic: Adding Channel Capability to the 11 Family

In this brief note a method for adding channel capability to the 11 series of processors is presented. The aspects of the approach which are worthy of note are (1) that the base machine is unmodified so that already existent code will continue to run unchanged, (2) that response to some interrupts will be significantly faster since context will not have to be changed and since microcode will replace assembly level code, and (3) that the cost of implementing a block transfer from or to an I/O device will be paid in the processor instead of (necessarily) in each peripheral controller.

The essence of the idea is to use the low bit of the address in the interrupt vector to specify either the traditional interrupt sequence (low bit=0) or a new sequence. Before explaining further a short discussion of interrupts is given. In a microprogrammed processor the interrupt system is provided by a combination of hardware and firmware (i.e., microcode). The hardware receives the interrupt requests and selects the 'winner'. The firmware asks by use of a branch whether there are any interrupts pending. If the answer is 'NO' the microprogram continues pursuing its own ends. If the answer is 'YES' the microcode proceeds to service the interrupt by implementing the definition of an interrupt as given for the machine. On an 11 the proceedure is to save the PC and PS on the stack. The important point is that once the interrupt is recognized it is serviced (i.e., implemented) in microcode.

The complete sequence for interrupt service is to (1) push the PC and PS on the stack and (2) obtain a new PC and PS from two locations in memory (from the address pair) whose lower location is specified by the interrupting device at a suitable point in the interrupt sequence. Thus, the interrupting device provides an address at the proper time and this address is available to the microprogram.

The new idea (used on the PDP-10 and known to 11 old-timers, I believe) is to use the low bit as a flag to select either the original definition of an interrupt or to select a new one. Both types of interrupt service are provided by microprogram and so the flag can be thought of as selecting one of two microcode sequences. If the bit is a zero the old (i.e., original) sequence is used. Thus, any old code will run without modification. If the low bit in an interrupt vector address were a zero there would have been an odd address trap on that interrupt on any of the older 11's. If new code (which uses the feature) were to be run on an old machine there would be a trap and so use of the feature would either be detected so the user could abort or the interrupt could be supported by software at the assembly level.

The microcode to service the interrupt in channel mode is thus selected by setting the low bit of the interrupt address. This allows any device to be run in channel mode. Any device which issues an interrupt when it wishes service can take advantage of this additional microcode. The microcode can be simple allowing just a block transfer or it could be more complex, controlled by a channel control block which might contain information on where to transfer what information, how much to transmit, when to stop transmitting (a count) and where to interrupt to (old style) when the transfer is complete (count=0). In addition an error interrupt location could be provided (note that the hardware knows much more about the type of error at the micro level than at the macro level). For communciations applications the incoming information (note need of a byte/word indicator) could be translated through a table to search for a particular set of characters. One could go on and on. The type of system provided should be selected to be powerful and simple to use.

Using the above scheme an interrupt-per-transfer device can be converted to a pseudo-NPR device in that the transfer to memory can take place without changing the process being executed in the processor. State is not changed and hence need not be saved. Since the technique works for ANY interrupt device this enhancement is also of use to users who add their own equipment.

A word of caution. Adding to a processor frequently leads to difficulties since one must consider other aspects of the problem besides the action of the enhancement. For instance, one must consider interrupt latency, system loading, and state saving. To reduce interrupt latency one allows the processor to be interrupted. This requires any state of more than temproary value to be stored. If this cannot be done without a major change to the architecture then a means must be found to circumvent the problem. In our case the maximum length of the block I/O must be kept short (say 5-10 microseconds). If the microprogram checks for interrupts before it has changed any registers, then it can abort if it wishes. In our case this is not possible because we are implementing the very system which is involved in servicing the interrupt.* In any event, the interrupt latency of an 11/40, for example, is at least 15 microseconds since this is the time between checks for interrupts pending which is used in the implementation of the floating point (FIS). System loading becomes a problem when the microcode uses its ability to cycle the memory (and the Unibus) at full speed, not letting any other users in. Further discussion of the fine points should be made after the design of a specific form of the enhancement is put forth. The previous discussion should indicate the need for system considerations.

* Not strictly true.

Dolphin System Proposal and Implementation Plan

Author: Vic Ku
Secretary/Typist: Ruth Jobin
Product Manager: John Jorgensen
System Program Manager: Vic Ku
Software Program Manager: Peter Hurley

Date: January 5, 1979

Table of Contents

1. Introduction

This document is intended to present to Digital Equipment Corporation Management a system implementation plan of the high-end DECsystem-10 and -20 architecture design to meet the needs of the 1980's in the areas of system availability, price/performance and functionality (both hardware and software).

The primary goals of the Dolphin Systems are:

* 1/2 of DECsystem 2060 manufacturing cost.
* 2.6 to 5.2 times 2060 performance.
* FCS at Q4/FY81, volume at Q2/FY82
* System will be highly reliable and available.
* VAX compatible (except CPU)

The following people reviewed and approved the contents of this document:

Dale Cook
Tom Dundon
Tom Eggers
John Grose
Peter Hurley
John Jorgensen
Alan Kotok
Vic Ku
Peter Lawrence
Jim McElroy
Franco Previd
Mike Robey
Pat Sullivan
Bill Walton
Phil Wilson
Sultan Zia

2. Dolphin System Goals

- Growth Product for DEC System 10/20 installed base for early 80's
- Technology Leader to yield highly competitive P/P System (>30% per year over KL10)
- Improve Fortran, Cobol and Logic performance as compared to KL10
- Improve P/P and reliability of Mass Storage and Communication Subsystem as compared to KL10
- High Availability and easy to maintain/repair
- Low cost of ownership
- Open, extendable design: Market life - 5 years minimum
- Avoid compounding risks
- Exploit the best ideas/lessons learned from KL/KS/VAX and the competition
- Provide functional base for:

  Foreign Device Connect
  Transaction processing
  Time sharing
  Batch
  Distributed Processing
  Distributed Data Base Management

- Maximize commonality with High End VAX implementation

3. Performance

System/CPU

Logic = 2.6 x KL10 Model B = IBM 3032
(logic mix, compiling SP1111 or MR1CD1)
Cobol = 5.2 x KL10 Model B = 1.7 x IBM 3031
(executing Cobol CPU profile)
Cobol = 4.0 x KL10 Model B (Executing Cobol I/O Profile)
Fortran = 4.2 x KL10 Model B = IBM 3032
(with Arithmetic Processor Accelerator,
Heavy Floating Point mix, executing SP1111)
Fortran = 1.8 x KL10 Model B
(Single Precision, without Arithmetic Processing Accelerator)
Fortran = 1.0 x KL10 Model B (Double Precision, without Accelerator)
Dolphin Bus Aggregate Data Bandwidth = 60 - 80 MB/S
APL = 2.6 to 5.2 times KL10 Model B (9-bit byte CPU Data Path, Arithmetic Processing Accelerator and the basic CPU speed-up will provide the performance up-lift. More precise performance estimates will be available by Q4/FY79)
SMP (2 CPUs) - Tightly coupled. 1.6 to 1.7 times the capacity of a Uniprocessor System

Communication Throughput

- Asynchronous = 3 x KL10 Model B (As of today)
- Synchronous = 4 x KL10 Model B (As of Today)
- TPS = 4 x KL10 Model B (As of today)
- Support up to 8 Graphic/buffered Terminals at 256 KB/s each (not available on KL10)
- Support DEC System 10/20 Systems (up to 16 per ICCS Bus Specification) with ICCS Linking capability with a total aggregate throughput of 8 MB/s.
- A detailed report on Dolphin's communication throughput and CPU overhead figures will be made available by February, 1979

Disk Throughput

- Max disk throughput = 1000 pages/sec = 2.6 xKL10 Model B
- Disk Transfer rate = 2.6 x KL10 Model B (RP07+ vs RP06)
- Cost/MByte of R81 is 3.8 times better than RP06
- Cost/MByte of RP07 is 2.9 times better than RP06

4. Compatibility

- SMP (up to 2 CPUs)
- Multiprocessing system scheme for larger than 2 CPUs will be recommended by Q1/FY80
- Runs TOPS-10/20 monitors
- VAX compatible (I/O controllers, Console, Dolphin bus, MCA technology, Memory Control and MOS array). New I/O drivers needed, new VAX CPU and Arithmetic Processing Accelerator (APA required)

5. Time to Market (the following system delivery dates depend heavily on the assumption that the requested project fundings in Section 13 are approved)

- Basic System on Tops-10/20 - FCS Q4/FY81 (Subject to Product Line and Field Service Approval)
  102 test completed - Q4/FY81
  DMT (4 systems) completed - Q1/FY82
  Volume Q2/FY82

  - Class A Computer room environment
  - TOPS-10 release 7.03, TOPS-20 Release 6
  - 2 Corporate Cabinets
  - Max configuration
    - 1 CPU, 2K cache, 4K microcode, APA (Arithmetic Processor Accelerator, optional)
    - 4 MW memory (64K MOS, 512K increments)
    - 1 Console, F-11 based
    - 8 I/O channels - UBA (Unibus Adaptor), MBA (Massbus Adapter), ICCS Port (Comm, UR)
    - 64 Async, 8 Sync, 2 LP, 1 CR

- New Disk Subsystem on TOPS-10/20 - FCS Q2/FY82
  Volume Q4/FY82
  - ICCS Port (HSC50, R81 Disk)

- SMP System, I/O and Memory Expansion - FCS Q2 FY/83
  Volume Q4/FY83

  - Dolphin Bus Repeater (DBR)
  - Shared Pages Data Integrity Box
  - High Availability System
  - Class A computer room environment
  - TOPS-10 Release 7.04, TOPS-20 Release 6
  - 4 Corporate Cabinets
  - Max Configuration
    - 2 CPUs each with 2K cache, 4K microcode, APA (optional)
    - 8 MW memory (64K MOS, 512KW increments)
    - 14 I/O channels, UBA, MBA, ICCS Port
    - 2 Consoles (F-11 based)
    - 1 Dolphin Bus Repeater Pair
  - 128 Asyn, 16 Syn, 4 LP, 2 CR
  - Number of Asyn and Syn lines can be extended with up to two more cabinets

- VMS - CPU/APA - not part of Dolphin Implementation Plan. A separate proposal and implementation plan will be made available by February, 1979

6. Availability

- MTBF (inherent, any hardware malfunction)

CPU	3344 hours
Small System	341 hours
Medium System (Removable Disks)	228 hours
Medium System (Fixed-media Disks)	228 hours
Large System (SMP)	116 hours

- MTBF (operational, redundant hardware options are included to increase the availability of systems. Failing system elements could be logically disabled and repaired at preventive maintenance time; many options can be repaired on line.

CPU	3344 hours
Small System	402 hours
Medium System (Removable Disks)	968 hours
Medium System (Fixed-media Disks)	437 hours
Large System (SMP)	77700 hours

- 93.9% (Basic System) to 99.95% (Hi Availability SMP System)
- One software crash per three weeks (TOPS-20)
- Mechanical failure (connectors, etc.) will be made available and will be factored into the above MTBF figures by Q1/FY80

7. Installation and Support

- System MTTR = 2 hours
- Max System TTR = 3 hours
- System Installation takes approximately 30 hours of labor
- Incremental software update
- Warranty cost is approximately 3% of System MLP per year
- Maintenance price is 6% - 8% of System MLP per year
- System Mean Down Time < 4 hours

3. System RAMP and Data Integrity Features

- Remote Diagnostic
- Early warning on low voltage and high temperature
- User mode diagnostic
- Dynamic System reconfiguration
- Optimized cooling/packaging for computer room environment
- ECC on Dolphin Bus, RAMS and memory
- CPU and I/O Instruction retry/data path parity
- Bus Recorder/Monitor
- MCA IC Socket
- 30 second battery backup on memory and console
- MCA chip isolation hardware and diagnostic
- Fault isolation to system components
- System error logging/reporting
- Power fail recovery (for power failure of less than 30 seconds)
- Integrated, Intelligent, Maintenance/Operational Console
- Etch backplanes
- Loopback diagnostic for I/O controllers
- Modular power supply regulators
- On line UR/Comm controller and device repair
- On Line Mass Storage device repair
- Redundant I/O controller capability (2 MBAs on the same Massbus; 2 UBAs on the same Unibus)
- Ability to logically disconnect failing options (MBA, etc.) from the Dolphin bus via console control
- On line CPU, mem, I/O controller repair (SMP or multiple bus system only)
- Insure Disk data Integrity (complete disk transfer upon power fail, write check, no error on clock stop)
- Job checkpoint/restart (some limitations)
- Dual port Disks
- Down-line Load
- Up-line Dump
- High Availability Comm/UR subsystem (Hydra Style) limits failures to single user
- Comm/UR ICCS Bus protected by parity and CRC
- Time of date meter powered by long-life battery

9. Functionality

Software (available on TOPS-10 and TOPS-20 except where noted)

Cobol 79 (TOPS-20 only)
Cobol 68/74
Fortran
Algol
APL
DBMS/IQL
PL1
TPS (TOPS-20 only)
BLISS
x.25 (TOPS-20 only)
Basic
RMS (TOPS-20 only)
Sort/merge
Macro/Link
Security Additions (TOPS-20 only)
SMP Support
Macro Command Generator
Editors
Programmer's workbench (TOPS-20 only)
Transparent network file system (TOPS-20 only)
Disk to Disk backup (TOPS-20 only)
DECNET support
Mountable Device Allocator (MDA)
Remote Job Entry (RJE)
Remote Terminal Concentration (RTC)
Remote Command Terminals
Application Terminals (TOPS-20 only)
2780/3780 Emulation/termination
HASP Multileaving Emulation/termination
DECNET Routing/complex Topology
Network Virtual Terminals

System/Hardware

- Dolphin Bus Interface Chip set
- 3 Interchangeable backplane I/O slots (UBA, MBA, Dolphin Bus Repeater and ICCS Port can be inserted into any I/O slots)

Communication

- Synchronous terminal support up to 56K Baud (16 lines maximum)
- Synchronous/Asynchronous terminal support up to 19.2 K Baud (192 terminals maximum, duty cycle dependent)
- Local buffered (Graphic, Word-Processor) terminal support up to 256K Baud each (3 lines maximum)
- Local high speed interprocessor interconnect of up to 16 processors with up to 3M Byte/sec aggregate throughput (up to 2 ICCS Ports)

Memory

- 64K MOS chip
- Memory access time < 467ns
- Memory cycle time < 396ns
- 512KW increment; 4 MW max per MA30
- ECC correction (single error correcting, double error detecting scheme)
- Memory address protected by parity throughout the memory control/memory array
- Memory control logic controlled by micro-code
- 30 second battery back-up
- VAX compatible (Architecture transparent)
- Support SMP system via Dolphin Bus Repeater

MCA

- 600 to 300 Gate Equivalent Per MCA (Comet = 400 gates equivalent)
- IIL diagnostic logic to provide isolation to chip level
- Typical power dissipation = 4 watts
- Maximum power dissipation = 5 watts
- 68 pin leadless JEDEC package
- Heat sink is permanently attached to MCA package
- Simple gate (2 input OR gate) delay < 1.3ns
- Complex Macro (4 to 1 Multiplexor, Flip Flop) delay < 1.8ns
- MOSAIC 1 (Isolated Base) process
- Prime source is Motorola
- Second source is Worcester/Hudson(DEC)
- Cost per MCA is highly volume dependent and will cost $37 in FY82 per MCA based on a total of no less than 2000 Systems shipped over a 5 year period (500 per year at high volume years)

APA (Arithmetic Processing Accelerator)

- Speeds up Single and Double Precision Floating Point Instructions
- Speeds up Single and Double Precision Integer Instructions
- Accelerates Data Type conversion Instructions
- Performs basic mathematic functions (SIN, COS, EXP, etc.)
- A 72-bit data path is provided to speed up some operations (Double Precision Multiple, for example) by as much as 9.5 to 1 times over KL10 Model B
- A 13-bit data path is provided to allow exponent calculation on standard and extended range numbers

CPU (I/E/M Boxes)

- Support full extended addressing with a Virtual Memory Space = 2 **3Ø words = 1 billion words

- Support all KL1Ø user mode instructions except KA1Ø Double Precision floating point instructions

- Support Expanded-Range Double-Precision Floating Point instructions (11 bit exponent, range of 1Ø ** +/- 3Ø7)

- Support New Cobol Instructions

    - Packed Decimal Arithmetic
    - 9 bit bytes
    - Display (Character String) Arithmetic
    - EBCDIC Support

- Microcode addressing space = 16K works

- Microcode implemented = 4K words

- Ibox (Instruction Prefetch/Decode) - to pipeline operations to improve price/performance of CPU

- 2 Way Associative hardware page table (1 way associative on KL1Ø) to improve TOPS-2Ø paging performance with extended addressing

- 2K Cache (same organization as KL1Ø)

Mass Storage

- RP06 (R), RP07 (F), RP07 + (F)
- R80 (F), R81 (F), RM04 (R)
- TM03/TU77
- TM78/TU78
- DX20, TU70/71/72, TX03/TX05

R = Removable
F = Fixed-media

Unit Record

- LP07 equivalent (1200 LPM) and LP26 equivalent (600 LPM) band type line-printers with Hydra controller. LP20 will not be upgradeable.

- CD20 A/C (300 and 1200 CPM) card-reader with Hydra controller. Older controller will not be upgradeable.

Future Extensions (Product Line Special Request and Funding Needed)

- Integral Motor Generator Power System
- PASCAL
- Mini System
- Card Punch
- KL10 I/O Bus
- IBM channel
- Array processor
- KL10 DMA20
- Paper Tape Reader and Punch
- COM (Fiche)
- Unibus Switch
- Other Special Interfaces

10. Technology

- Corporate Cabinets
- Extended Hex modules (PC or Multiwire modules; to be determined by March, 1979)
- Macro Cell Array (ECL)
- Press Pin Connector
- Modular Power Supplies (switching regulator)
- 1K/4K ECL RAM
- 64K MOS Memory Chip
- LSI IC Socket (MCA only)
- Noise Spec for Processor Cabinet
  - Noise Power Emission Level (Ref 10** - 12 watt) < 7.4 Bels
  - Sound Pressure level at bystander position < 63 db (A)

11. Manufacturing Cost, Cost/Performance

		Dolphin*** Cost	KL10 Model A Cost (MB20)	Ratio of Dolphin Cost to KL10 Cost	Overall P/P Improve	P/P Improve per year
Average System*	Logic	76.5K	170.0K	45.0%	6.9	31.8%
	Fortran	80.0K	170.0K	47.0%	10.7	40.3%
	Cobol	76.5K	170.0K	45.0%	13.6	45.2%
Main Frame**	Logic	40.0K	88.0K	45.5%	6.9	31.8%
	Fortran	43.5K	88.0K	49.4%	10.2	39.3%
	Cobol	40.0K	88.0K	45.5%	13.5	45.0%

		Dolphin*** Cost	KL10 Model B Cost (MB20)	Ratio of Dolphin Cost to KL10 Cost	Overall P/P Improve	P/P Improve per year
Average System*	Logic	76.5K	170.0K	45.0%	5.3	42.2%
	Fortran	80.0K	170.0K	47.0%	8.9	54.8%
	Cobol	76.5K	170.0K	45.0%	11.3	62.4%
Main Frame**	Logic	40.0K	88.0K	45.5%	5.8	42.2%
	Fortran	43.5K	88.0K	49.4%	8.5	53.4%
	Cobol	40.0K	88.0K	45.5%	11.3	62.4%

		Dolphin*** Cost	KL10 Model B Cost (MF20)	Ratio of Dolphin Cost to KL10 Cost	Overall P/P Improve	P/P Improve per year
Average System*	Logic	76.5K	158.0K	48.4%	5.4	61.9%
	Fortran	80.0K	158.0K	50.6%	8.3	83.1%
	Cobol	76.5K	158.0K	48.4%	10.5	95.7%
Main Frame**	Logic	40.0K	76.1K	52.6%	4.9	57.5%
	Fortran	43.5K	76.1K	57.2%	7.3	76.5%
	Cobol	40.0K	76.1K	52.6%	9.7	91.3%

*Average System (excluding FA&T) consists of:

1 CPU, 1 Console
512 KW memory
1 APA (Fortran only)
4 Disks (R81), 2 Disk Channels (ICCS Ports)
1 Tape (TU78), 1 Tape Channel (MBA)
1 ICCS Port (Comm, UR)
64 Asy, Lines. 5 Terminals
2 Syn. Lines
1 Line Printer (600 LPM)

**Main Frame (excluding FA&T) consists of:

1 CPU, 1 Console
512 KW memory
1 APA (Fortran only)
1 Channel (MBA)
1 ICCS Port

***Based on costs @ 12 months after FCS (Q4/FY82) and a total of 2000 Dolphin Systems built/shipped over a five year period.

12. Major Milestones

- Breadboards
  - Two will be built
  - Data Path MCA's will be used
  - Control logic MCA's will be emulated with 10K ECL chips
  - Multiwire and wirewrap modules
  - 5 MHz to 10 MHz clock (final system clock = 60 MHz)
  - Console Power On - 3/79
  - CPU Power On - 11/79
  - System Runs functional Diag - 5/80
  - System Runs Monitor - 11/80
  - Functionalites identical to Prototypes

- Prototype
  - Three Basic Systems will be built
  - Data Path and Control Logic MCA's will be used
  - 50 - 60 MHz Clock
  - Console Power On - 4/80
  - CPU Power On - 8/80
  - Basic Sys Runs Funct Diag 10/80
  - Basic Sys Runs Monitor 12/80
  - 102 Test completed - 3/81
  - Engineering release completed - 3/81

- Pilots
  - Fifteen or more will be built by Manufacturing
  - FCS - 6/31
  - DMT (4 System) completed - 8/81

13. Development Cost (K)

Hardware

	FY79	FY80	FY81	FY82	Total $(K)
CPU Design $(K)	1673	2592	2129	672	7066
Memory	227	680	266	74	1247
Technology (circuit/mech)	542	1418	897	151	3008
MCA/tools	363	336	--	--	699
Release Eng.	--	44	73	77	194
ICCS/HSC-50	--	224	280	100	604
Console	--	285	211	44	540
Hydra Comm	47	162	167	68	444
ICCS Interprocessor/ Graphic Links	--	54	TBS (Q4/79)	TBS (Q4/79)	54
UBA	113	172	130	51	466
MBA	120	330	310	40	800
Total $	3085K	6297K	4463K	1277K	15,122 K

Total Hardware 15,122 K

Software

	FY79	FY80	FY81	FY82	Total	Total $(K)
Monitor (Man-Quarter)	6.2	22.2	34	16	78.4	$ 862.4
Comm	2	11.5	27	8	48.5	$ 533.5
Language	25	41	42.5	44	152.5	$1677.5
Document	1	14.5	50.5	26	92	$1012.0
SQM	2	13	20	18	53	$ 583.0
Total(Man-Quarter)	36.2	102.2	174	112	424.4	$4668.4
Total $	398.2K	1124.2K	1914K	1232K	4668.4K	$4668.4

Total Software 4668.4 K

Manufacturing Start-up Cost and New Product Cost

	FY79	FY80	FY81	FY82	FY83	Total$ K
New Product Start-up Cost	32	296	493	79	--	900
4 QV (Quick-Verify Stations)	--	--	90	30	--	120
2 Option Test Stations	--	--	50	50	--	100
FA&T Test Systems	--	--	--	250	--	250
APT System Upgrade	--	--	100	--	--	100
MCA IC Tester Depreciation	--	200	100	50	25	375
Total $	32K	496K	833K	459K	25K	1845K
				Total Manufacture		1845K

14. Development Risks

- MCA Technology affects speed, reliability, cost and schedule
- MCA IC Socket (availability and reliability)
- MCA IC layout (IDEA system functionality and reliability) Placer and Router availability and effectiveness)
- 4K ECL RAM (availability, reliability, cost)
- 64K MOS (availability, reliability, cost)
- Hydra Communication package (availability, functionality, cost)
- Disk/Magtape (ICCS Bus availability, functionality, cost)
- Engineering Releases (resource, elapsed time)
- Level of Fiscal Project Funding affects functionality, performance and schedule
- Cobol 79 Schedule (availability on FCS)

15. Manufacturing Goals

- To reduce manufacturing cost
  - Increase the level of testing in the Volume area to reduce FA&T cycle time/cost
  - MCA on IC Socket would reduce debug and repair costs
  - Modular power supplies would reduce inventory and repair costs
  - The partitioning of CPU cabinet into four distinct and testable sections (CPU, I/O, Memory, Comm) would reduce total test time, capital outlays and repair costs
  - Utilize existing capital equipment (APT, etc.)

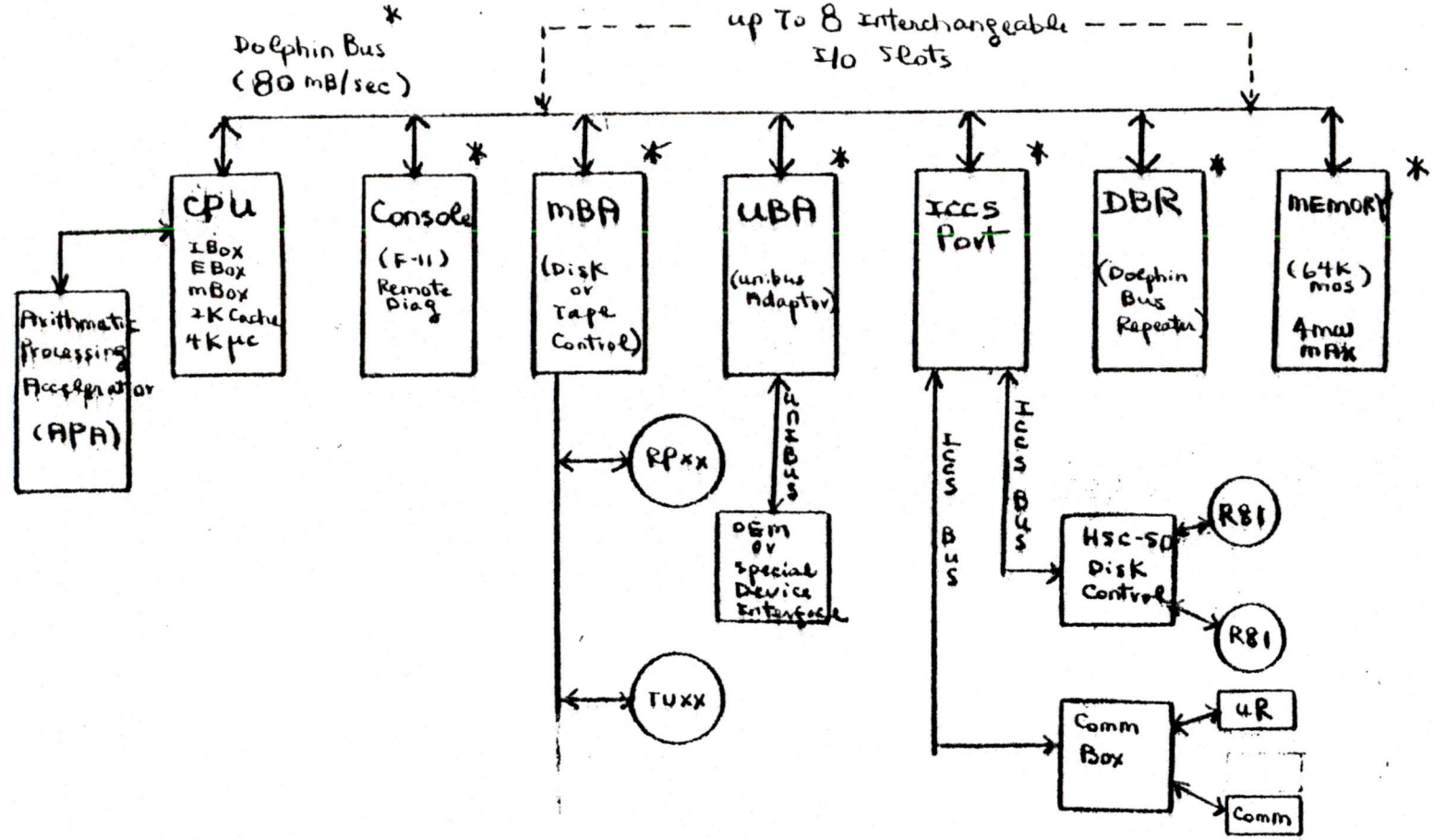
- To improve quality of final system product
  - MCA chip level diagnostic
  - Etch backplanes
  - Improve QC and acceptance procedures
  - IC and MCA chip burn-in
  - Rigorous PMT effort

- Preliminary Manufacturing Plan Available - Jan. 1979
- Detailed Manufacturing Plan Available - July, 1979

16. Field Service Goals

- To minimize the number of possible system interruptions
    - Rigid site planning and environment requirements/specifications
    - Provide 24 hours DDC System reconfiguration service
    - Provide remote hardware degradation analysis (interrogate system error file, etc.)
    - To provide tight system revision control
- To minimize the impact of system interruption
    - Use option or subsystem specialist to reduce repair time
    - Intensive option specialist training course
    - Rely heavily on DDC remote diagnostic center to reduce debug/travel time
    - To improve the quality of Field Service spares to reduce spares cost
- To minimize the installation time
    - Rigorous system acceptance before and after shipment
    - Provide feedback to Manufacturing for process control
    - Special installation training/documentation

- Preliminary Field Service Plan Available January, 1979
- Detailed Field Service Plan Available April, 1979

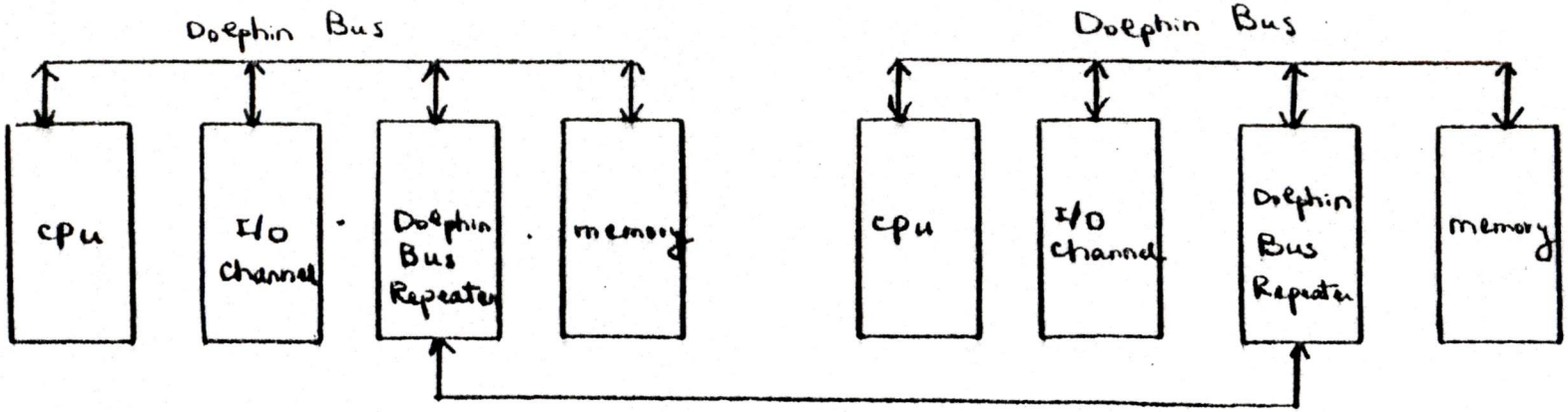


* VAX Compatible

Dolphin System Block Diagram

Diagram A

Vic Ku
Jan 3, 1979



Dolphin SMP Block Diagram

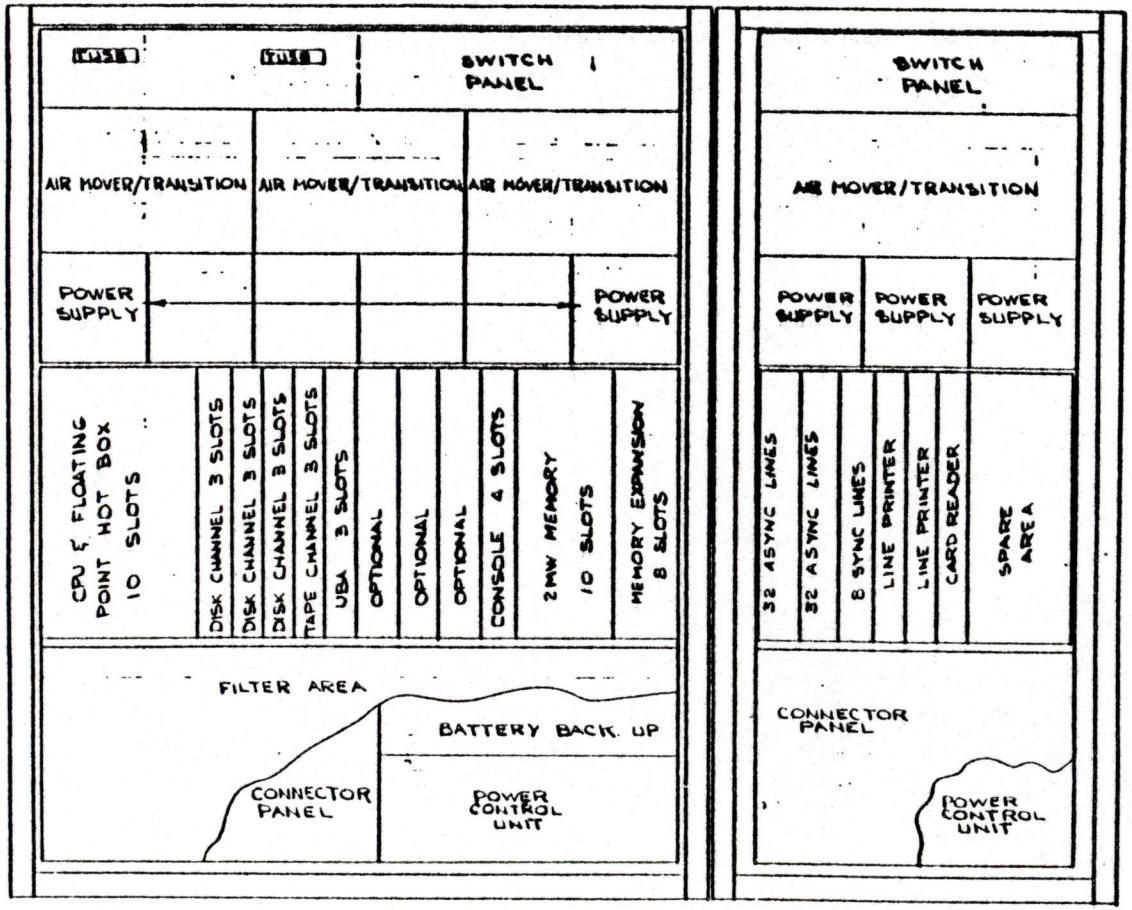
Diagram B

Vic Ku
12/78

1 CPU
4MW Memory
Console (F-11 based)
Fortran Accelerator

5 Disk Channels
1 Tape Channel
1 Unibus Adaptor
3 Spare I/O Channels
(Tape, Disk, Unibus Adaptor and/or Bus Repeater)

64 Asyn Lines
8 Syn Lines
2 Line Printer Controllers
1 Card Reader Controller
Spare Unit Record Slots



DOLPHIN BASIC SYSTEM

Diagram C

12/7/78

PM COMMITMENT TO P/L

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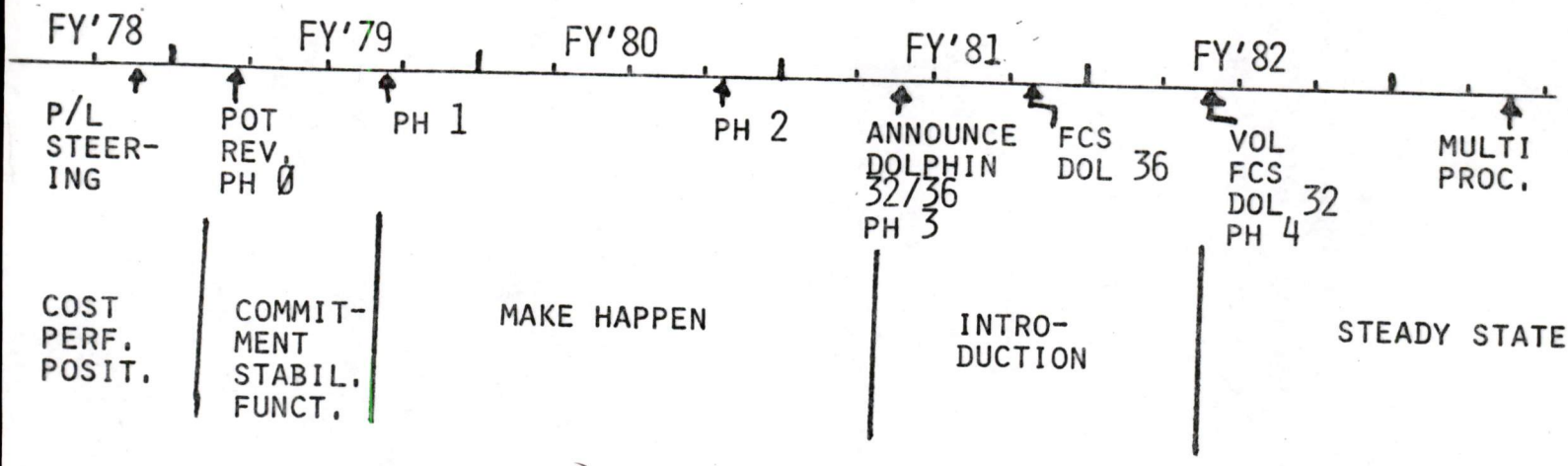
CALENDAR:



REQUIREMENTS SATISFIED

COMPETITIVE LARGE SCALE SYSTEM

- PROTECTS TOPS 10/20 CUSTOMER BASE
- ATTACK VEHICLE FOR NEW BUSINESS

HIGH TECHNOLOGY

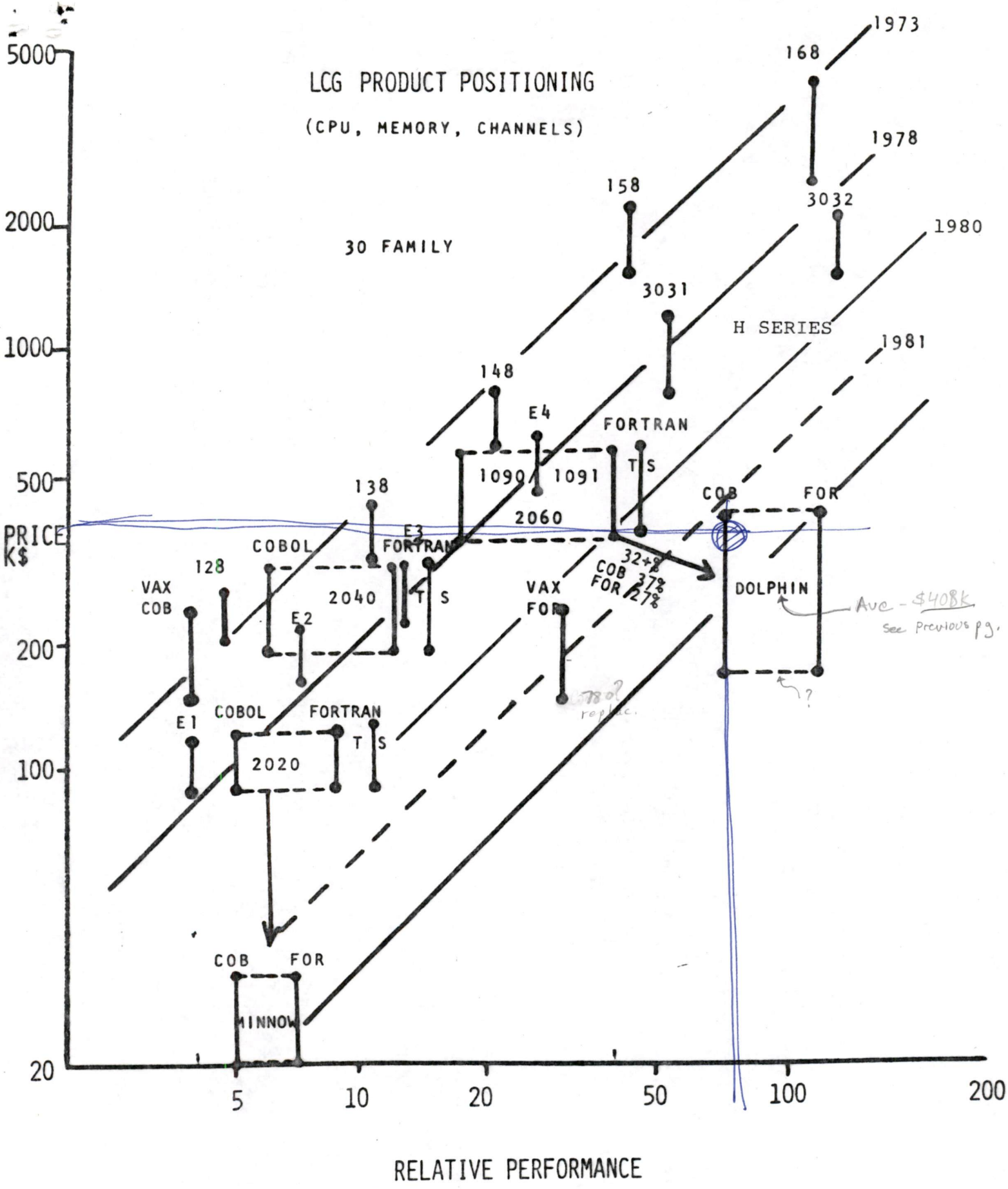
- COST PERFORMANCE ≥ 32%/YR. OVER KL10B & MB20
  3032 AT 1/4 THE PRICE
  1.5 x 3031 AT 1/2 THE PRICE
  > 2.0 x KL AT 1/2 COST: COBOL 5.1 X, FORTRAN 3X
- MINIMUM 5 YEAR PRODUCT LIFE
- LEADING EDGE MAINFRAME SYSTEM
  - DISTRIBUTED PROCESSING
  - INTERACTIVE/T.P.
  - BATCH
  - EASE OF USE
  - RAMP/SUPPORT
  - SYSTEM BALANCE: I/O, CPU, COMM.
  - DATA BASE

TIME TO MARKET: FCS Q4 FY'81

INVESTMENT OPPORTUNITY:

	AUG '78	JAN '79
UNITS	2032	2032
AVG. SYSTEM	$408K	$408K
REVENUE	$830M	$830M
DEV. COST	$ 19M	$ 24M*
RATIO OF RETURN	43.7	37.7

*NOW INCLUDES SYSTEMS SOFTWARE



COMPANY CONFIDENTIAL

JSJ 11/78

DIGITAL

INTEROFFICE MEMORANDUM

JAN 22 1980

1-274

TO: Distribution

DATE: 1/17/79
FROM: John Jorgensen
DEPT: LCG Product Management
EXT: 6281
LOC/MAIL STOP: MR1-2/E78

SUBJ: DOLPHIN Phase 1 Review

During August 1978 DOLPHIN was reviewed by the Large Systems POT as part of the Phase Ø review process. Approval was given to proceed. At this time a Phase 1 Business Plan and an Engineering Plan with commitments to detailed product specifications has been prepared. A summary of these plans is attached.

Prior to the Phase 1 Review, we want to reaffirm that DOLPHIN meets the requirements for DEC's "Top-of-the-Line" mainframe product in the FY'82 to FY'87 time frame. DOLPHIN is today defined. It will be implemented as defined over the next 24 months. Even now any changes in that definition will jeopardize FCS of Q4 FY'81. For this reason we are planning to review DOLPHIN with the Commercial and Technical Product Line Groups to obtain their buy-in to the DOLPHIN Business and product Plans. These reviews are scheduled for February 9 with the Technical Products Group and February 27 with the Commericial Products Group.

Since the August DOLPHIN Review there has been a move to build our product capabilities for the 1980's on the VAX VMS architecture. This has some exciting opportunites and some challenges in terms of providing high-end mainframe products to protect and grow our existing base and expand the base thus maintaining market leadership. We will be able to discuss the DOLPHIN response to these opportunities and challenges at the Product Line Group Meetings.

/amc

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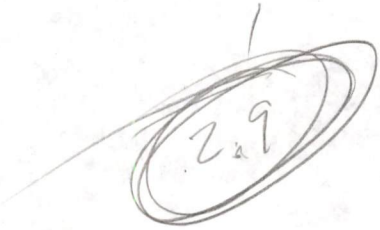
3.9 Cont



PRELIMINARY 2080 PLAN

8-May-79

Engineering Group Manager: Ron Bingham
2080 Product Manager: Per Hjerppe
2080 Project Manager: Don Lewine

CHAPTER 1

SUMMARY

1.1 EXECUTIVE SUMMARY

The 2080 is a KL10 follow-on machine. The 2080 will provide about 2.4 X a KL10 at less than 2020 prices [a 7.9 price/performance improvement over the KL10E]. First customer ship is scheduled for Q4 of FY82.

The total engineering budget is 6706K, however only 1599K are required in FY80.

TOTAL 36 BIT BUDGET REQ'MT VS 4/5 M TODAY?

1.2 GOALS

The 2080 goals, in order of priority, are:

1. Time to market (most important)
2. Performance greater than 2 x KL10E
3. Lowest possible cost of ownership
4. RAMP
5. Minimum engineering budget (least important)

1.3 PRODUCT DESCRIPTION

The 2080 is built out of high speed ECL 100K logic. The 2080 CPU is pipelined and many have several instructions in execution at any given time. The memory uses 64K MOS chips and a four word fetch to provide low cost high speed memory.

All I/O is done via ICCS ports. The 2080 is viewed as a processing node on a distributed computer network. The ICCS system will provide enough features to support all of the types of I/O currently done on a 2060.

The 2080 will be about 2.4 x KL10E [+/- 15%] in average compute performance. This is based on a "logic mix" doing editing, compiling programs, sorting, etc.

The 2080 uses new packaging technology to provide a more reliable and maintainable package. In addition, heavy use of automatic error correction should provide greatly improved availability.

A much more complete product description is given in chapter 3.

1.4 CO-REQUISITES

The 2080 depends on the following new products:

1. The 64K MOS memory chip.
2. The intercomputer interconnect scheme (CI). In particular, the 2080 system requires all of the following ICCS devices:
    1. Low speed asynchronous communications.
    2. HSC50 memory hierarchy management providing high performance disk and tape support.
    3. Network gateways to DECNET, SNA, etc.

STATUS IN CURRENT PLAN?

1.5 SYSTEM COSTS

ESTIMATED MANUFACTURING COSTS
Average 2080 system

1	CPU	14.6	
1	FPA	3.5	
512K	MAIN MEMORY	10.2	
4	ICCS LINKS	4.8	
1	HSC50	3.7	
2400MB	DISK STORAGE	33.6	[R81 PRICE]
2	TAPE DRIVES	15.0	
64	ASYNC LINES	6.2	
1	LINE PRINTER	5.5	
5	TERMINALS	2.5	
	F. A. & T.	3.0	
		102.6K	

A similar 2060 system has a transfer cost of 285.4K. This results in a price performance improvement of 6.7 over the 2060 system. There is a factor of 7.9 price performance improvement on the CPU and MEMORY subsystem.

This configuration assumes substantial growth in the amount of online disk storage.

1.6 SUMMARY SCHEDULE

We believe we stand an excellent chance (better than 90%) of meeting the following schedule:

Project starts	July 79
Design complete	July 80
Proto power on	November 80
Monitor runs	May 81
Pilot power on	August 81
Pilot runs monitor	September 81
Start DMT	September 81
First customer ship	June 82

June 82 is the earliest first customer ship date to which we can firmly commit. However, if we get all the resources we need, and things go fairly well, we could meet the following schedule:

Project starts	June 79
Design complete	April 80
Proto power on	June 80
Monitor runs	October 80
Pilot power on	December 80
Pilot runs monitor	January 81
Start DMT	January 81
First customer ship	June 81

We do not believe that there is more than a 50% chance that we can ship a product in June 1981.

1.7 RELATION TO OTHER DEC PRODUCTS AND OVERALL DEC STRATEGY

The 2080 contributes to Digital's basic product strategy by:

1. Providing cost-effective 10/20 systems through building hardware that runs current operating systems.

2. Converging on ease of DEC 20 to VAX movement through data conversion routines and cost-effective, high speed networks.

1.8 RISKS

1. Fairchild 100K logic may not work as well as we hope. It may be too slow, too expensive or hard to package. We might have MCA as a fall back, if VENUS uses MCA parts.

2. MERCURY and HSC50 may not work at all, or may only work on HYDRA.

3. It may be very difficult (or take a long time) to staff up for this project. Over half the DOLPHIN design team has either left the company or transferred to other plants. We have lost most of the people with heavy 36-bit experience.

4. The 36-bit marketing and sales may die before we can get the machine to market.

CHAPTER 2

DESIGN ALTERNATIVES

There were a number of ways to go in the design of 2080.

1. Build DOLPHIN as proposed.

2. Build a simplified DOLPHIN, using all MCA parts.

3. Build a machine out of left over DOLPHIN MCA parts and off the shelf ECL 10K. This machine would use MCA parts for datapath and ECL 10K MSI for control logic. This is the PHOENIX proposal.

4. Build a machine using some other custom gate array (SIEMANS or FAIRCHILD).

5. Build a machine with 100K logic on ceramic substrate.

6. Build a machine with 100K parts mounted on modules.

7. Convert the 2020 design from 74LS to ECL 100K.

8. Design a multi-processor scheme with lots of instructions being executed at once.

9. Cost reduce and speed up the KL10.

Several of these choices were quickly rejected. Here is a comparison of some of the better alternatives:

	PHOENIX (MCA MACHINE)	F100K W/CERAMIC	F100K ON BOARDS	F100K 2020	DOLPHIN
PERF. X KL10E	2.2	2.9	2.5	1.4	2.6
FCS 90%	MARCH 82	JUNE 82	JUNE 82	APRIL 82	APR 81
FCS 50%	APRIL 81	JULY 81	JUNE 81	MAY 81	JAN 81
ENG BUDGET	6179(*)	7337(*)	6706	4742(*)	15500
COST CPU + 512K	26025	27410	24890	20332	33200
$/KL10	12048	9583	10159	14515	12768
PRICE PERF IMPROVEMENT	6.7	8.5	7.9	5.6	6.4
%/YEAR VS KL10E	53	54	53	45	72

Since time to market is an important goal and ECL 100K without ceramic substrates is lowest risk, we chose that technology.

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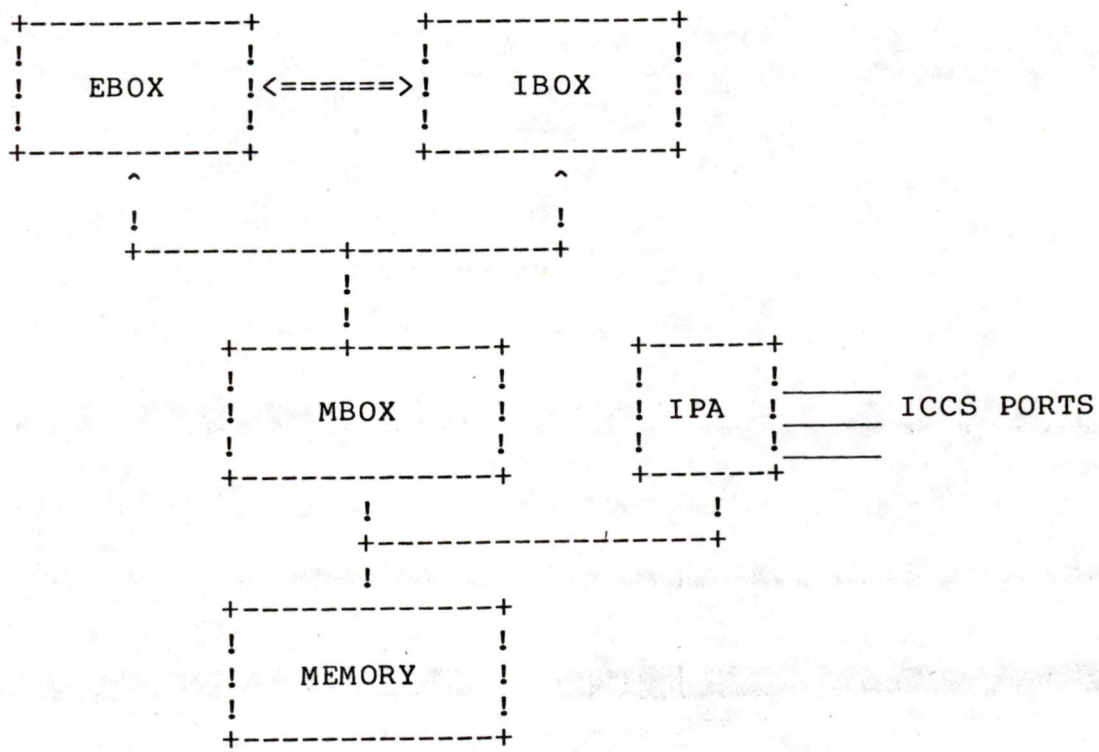
(*) Does not include an FPA.

CHAPTER 3

PRODUCT DESCRIPTION

3.1 DESCRIPTION



The internal CPU structure looks very similar to the DOLPHIN. There is a IBOX and an EBOX to allow two instructions to get executed at once and an MBOX with a 4K cache. However, the DOLPHIN bus has been eliminated. This provides the following advantages:

1. The machine is less expensive to build because an expensive component has been eliminated.

2. The machine runs faster because the delay between memory and cache has been reduced. This speeds up cache refills and makes the memory access time

lower.

3. The machine is less complex. This should make it easier to design and maintain.

Because our tightly coupled multi-processing software requires shared memory and we have eliminated the backpanel bus, we can not run TOPS-10 symmetric multi-processing. There is no TOPS-20 multi-processing support, yet. High speed networks seem to better support the long term corporate strategy.

3.1.1 Processor

The processor consists of three logical blocks, IBOX, EBOX, and MBOX. There are also hooks for an arithmetic accelerator.

3.1.1.1 MBOX - The MBOX is the heart of the 2080 system. The MBOX contains the cache and paging. All the other parts of the system connect to the MBOX radially.

3.1.1.2 IBOX - The IBOX is used as an intelligent instruction prefetcher. The IBOX allows effective address calculations and instruction fetches to be overlapped with instruction execution. This greatly enhances performance by allowing all cache cycles to be used productively.

3.1.1.3 EBOX - The EBOX is the real computer. This is the instruction execution unit where the answers are calculated. The EBOX is microprogrammed and allows for some new instructions to be defined after first customer ship. The 2080 will not support user microcode in any general way, however, a customer may write special microcode at his own peril.

3.1.1.4 Arithmetic Accelerator - This optional box is used to speed up FORTRAN compute performance of the 2080 system. It is more than the classic floating point accelerator because it also includes speedup hardware for integer multiply and divide as well as some "built-in" FORTRAN functions.

3.1.2 Memory

The memory system uses 64K MOS memory chips. The memory is arranged so that four words are read at once. This means that the minimum memory size is 256K (4 x 64K). The most likely case would pack memory into 512K blocks. This will make 512K the minimum configuration.

3.1.3 I/O

All I/O takes place via the ICCS bus. This requires that we have the following devices available on the ICCS network:

1. Large, fast disks. These will be used for both file storage and paging.

2. Magnetic tape suitable for backing up the disk.

3. Low speed (up to 9600 baud) asynchronous communications.

4. Network communication.

5. Standard unit record gear. Things like line printer, card reader, etc.

One way to get unit record, asynchronous communications and DECNET is via an ICCS adapter on the UNIBUS and a PDP-11 gateway.

3.2 SPEED

Based on cache bandwidth and estimated memory access times times the 2080 should be about 2.6 x KL10E. Since there may be places where the CPU can not keep up with memory the CPU performance is most likely to be 2.4 x KL10E. The HSC-50 and ICCS ports are expected to provide an I/O bandwidth to support this amount of computer power.

These performance numbers refer to a logic mix. That is a compiler, editor, or operating system. We do not expect FORTRAN execution performance, without a hotbox, to be much better than a KL10E, some heavy double precision programs may even run slower than a KL10E. A hotbox would provide about a 4:1 speedup for those programs. We expect most systems to be sold with an arithmetic accelerator.

3.3 ENVIRONMENT

Class A

3.4 RELIABILITY/MAINTAINABILITY

3.4.1 Integral Fault Detection And Maintenance Features

These features aid in the diagnosis of hardware errors and in the efficient maintenance of the system. Specific features include the following:

1. A Diagnostic Console, consisting of a microcomputer load device and console terminal, provides both local and remote diagnosis of system errors and simplifies system bootstrap. Simple commands replace lights and switches. The diagnostic console provides faster and easier maintenance procedures and increases availability.

2. A diagnostic bus which allows the console processor access to state information within and to discrete test points to facilitate module/chip replacement strategies.

3. Memory error correcting code (ECC) will correct all single bit memory errors, and will detect double-bit memory errors.

4. ECC is provided on much of the internal storage in the 2080 CPU. This allows maintenance to be deferred and also avoids crashes due to intermittent failures.

5. A watchdog timer in the console processor will detect hung machine.

6. The software and console will provide for optional automatic reboot in case of failure.

7. The system clock will use a frequency synthesizer to allow the clock frequency to be set from the console. This allows clock margining as well as the ability to set the clock frequency higher as part speeds improve.

8. Memory management and the cache may be disabled by diagnostics to aid in isolating hardware problems.

3.4.2 Fault Tolerance Features

These features provide the means to continue processing without loss of information, even though hardware errors may be occurring. specific features include the following:

1. ECC on main memory.
2. ECC on internal storage (cache, page tables, microcode, etc.)
3. Extensive retry and fail soft features will attempt to prevent a fault from crashing the system.
4. The software performs dynamic bad block handling for disk structures.

3.5 PHYSICAL CHARACTERISTICS

The physical characteristics will be specified at a later date. We would like to keep the total floor space for a 2080 system within about 10 percent of the space required for a 2020 system.

3.6 POWER REQUIREMENTS

The 2080 CPU, MEMORY and I/O control will consume about 3400 watts.

3.7 SYSTEM PROGRAMMING

The 2080 will require a large software effort to support the ICCS I/O structure. The device drivers for tape, disk, and communications will all have to be rewritten. The structure of both TOPS-10 and TOPS-20 allows one to write new device drivers by making fairly local changes, however, the software effort is large.

In order to reduce the software costs, we will maintain maximum exec mode compatibility and total user mode compatibility with the KL10E.

3.8 MAINTENANCE PHILOSOPHY

An independent console CPU and TU58 will be used for local and remote diagnosis of the 2080 CPU cluster. A new set of CPU micro diagnostics will be required. Their goals will be to support isolation to a group of five chips in X% of all faults.

The 2080 CPU, memory and ICCS cluster should have an MTBF of 1800 hours and an MTTR of 2.5 hours. Based on these assumptions the BMC should be less than $350/month.

3.9 RANGE AND FLEXIBILITY

The fundamental heart of the DECsystem 2080 is not its central processing unit, but rather its innovative, inter-computer communications. By means of this unique interconnect system, additional computing power can easily and modularly be expanded.

The 2080 box itself is tightly bounded. Memory can range from 2MB to 16MB. ICCS ports range from 1 to 8.

3.10 RELATIONSHIP TO OTHER DEC PRODUCTS

3.10.1 To Existing DEC Products

The 2080 is a major new hardware product and does not support the current generation of UNIBUS and MASSBUS peripherals. It does support and require DECNET as well as current terminals.

3.10.2 Other Products That This Product Is Dependent Upon

We need the products of the new interconnect strategy. In particular, we expect to use:

1. MERCURY communications concentrator to provide:
    1. Async lines which require low CPU overhead and have timely echo.
    2. Sync lines which support multi-drop terminals, remote stations, graphics terminals, and network interconnect.

3. Unit record equipment. This will be 90% line printers.

2. HSC50 memory hierarchy management providing:

1. Disk interconnect supporting R80, R81, STC8650, etc.

2. Tape interconnect supporting some form of high performance, cost effective tape system.

NOTE

This means that the corporate interconnect strategy must support 36-bit data in a cost-effective way.

3.11 STANDARDS TO BE FOLLOWED

All applicable DEC hardware standards will be followed. The 2080 will be tested to DEC STD 120 class A environment.

TOPS-10 and TOPS-20 do not fully support DEC STD 110 (escape sequences). See software project plans for details.

3.12 TECHNICAL RISKS

There are several major area's of technical risk: interconnect, ECL 100K logic and mechanical packaging.

3.12.1 Interconnect

The 2080 is counting on the corporate interconnect to meet its goals. Several things can go wrong here:

1. The whole interconnect scheme may fail.

2. The interconnect strategy may be later or more expensive than needed for 2080.

3. The interconnect hardware/software may not support 36-bit data.

The 2080 could use MASSBUS and UNIBUS for I/O. While this gives us a fall back position, it does not allow addon VAX.

3.12.2 ECL 100K Logic

Digital does not currently use any 100K logic. While all the spec sheets look very good, we do not know what the actual rules will work out to be.

Because 100K has very fast rise times (.7 ns.), we may not be able to use multi-wire modules.

Very few vendors make 100K logic, so there may be supply problems. The risk of supply problems is not as great with 100K as with the MCA or comet gate array.

3.12.3 Mechanical Packaging

We are hoping to use very large modules (24" x 24") mounted on heat sinks. There will be no backpanel at all. This is new and innovative, however, it may not work.

CHAPTER 4

MARKET DESCRIPTION AND REQUIREMENTS

4.1 THE NEED

The DECsystem-10 and DECSYSTEM-20 customer base represent a significant market opportunity. If DIGITAL does not respond to the market demand, several things can happen:

1. DIGITAL will miss the opportunity.

2. If we fail to provide cost effective hardware to protect our customer's software investment, customers who buy -10s and -11s may seek a new vendor. This could impact more than just 36-bit business.

3. An obvious market opportunity would exist for a new competitor.

4.2 THE SOLUTION

The DECsystem-2080 is not just a computer, but a network solution to the software compatibility and VAX migration problems. The 2080 allows a customer to run all his current programs without any modification and add future applications by adding VAX systems onto his network.

To appeal to the current base, the DECsystem-2080 must be at least twice the performance of a KL10, provide more uptime with a lower cost of service, and have a much better price/performance number than the KL10E. The 2080 must also look respectable compared to IBM and the rest of the industry.

CHAPTER 5

FINANCIAL

5.1 UNIT COST STRUCTURE

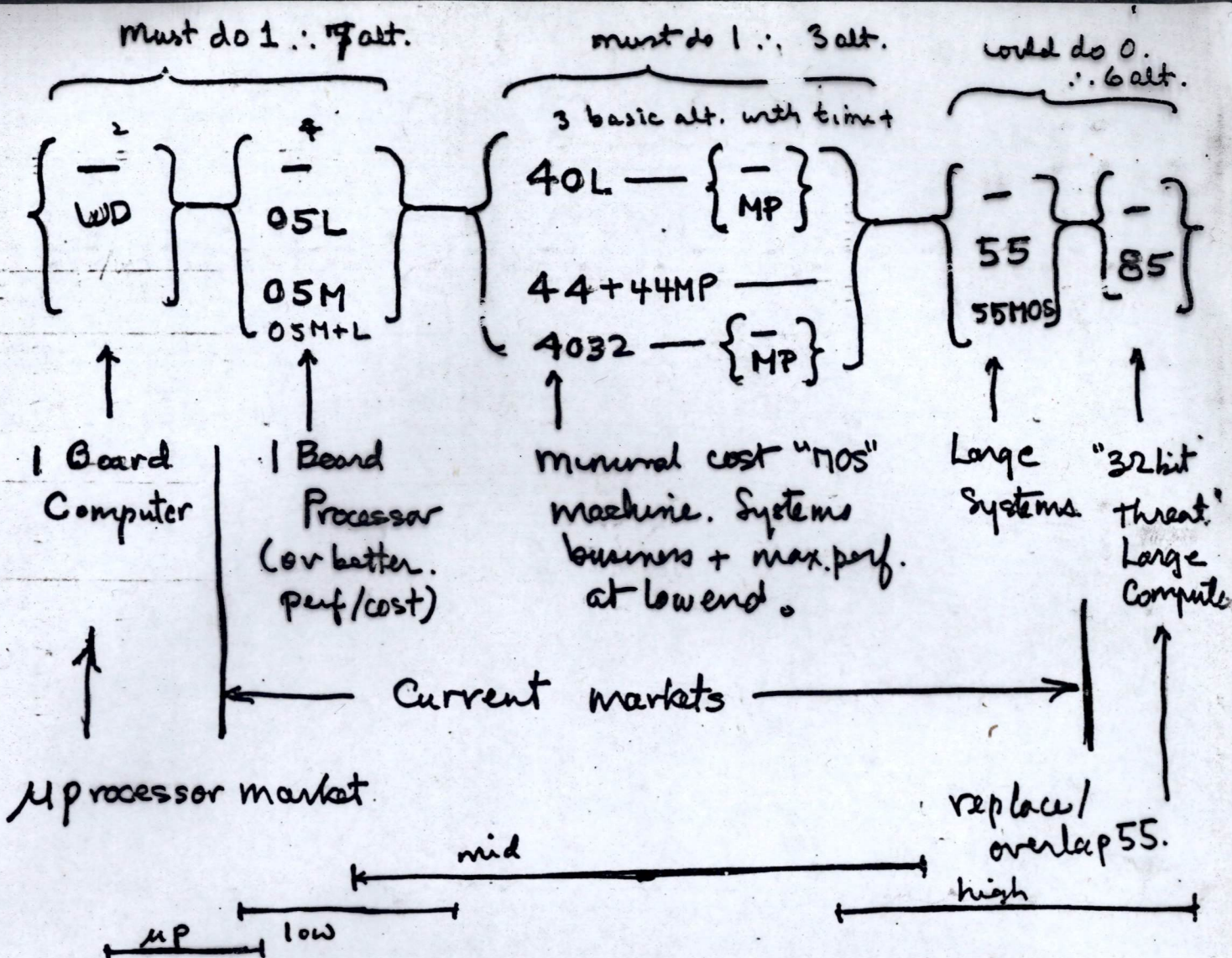
Unit costs are based on volume levels one year after FCS. This assumes that all parts are purchased nine to twelve months prior to ship. There is no allowance for inflation.

CPU

CPU MODULES	6882	
CPU CABINET	600	
POWER SUPPLY	1700	
POWER CONTROL	295	
CPU INTERCONNECT	415	
CPU HOUSING	250	
FANS	375	
FAULT SENSING	78	
A/C WIRING	75	
DUCTWORK, FILTERS	160	
MISC	500	
CONSOLE	1200	
VT100	500	
CPU ASSEMBLE & TEST	1600	
	14630	CPU

MEMORY

MEMORY ARRAY	6370	
CONTROL	800	
INTERCONNECT	390	
CHECKOUT	1000	
POWER SUPPLY W/BATTERY	1700	
	10260	



Grammar expressing alternatives being Coindered as per early June 1974.

gB.

Easy solution: Is it a good one?

- Pick 1 each from each categorie.
- Development is in place. Everyone has a project.
- Something for each market group.
- Sense: WD; 05L iff cost +1 board is met; 40L; 55; 85.

11/55

GB
6/17/74

We're behind in doing this great product:

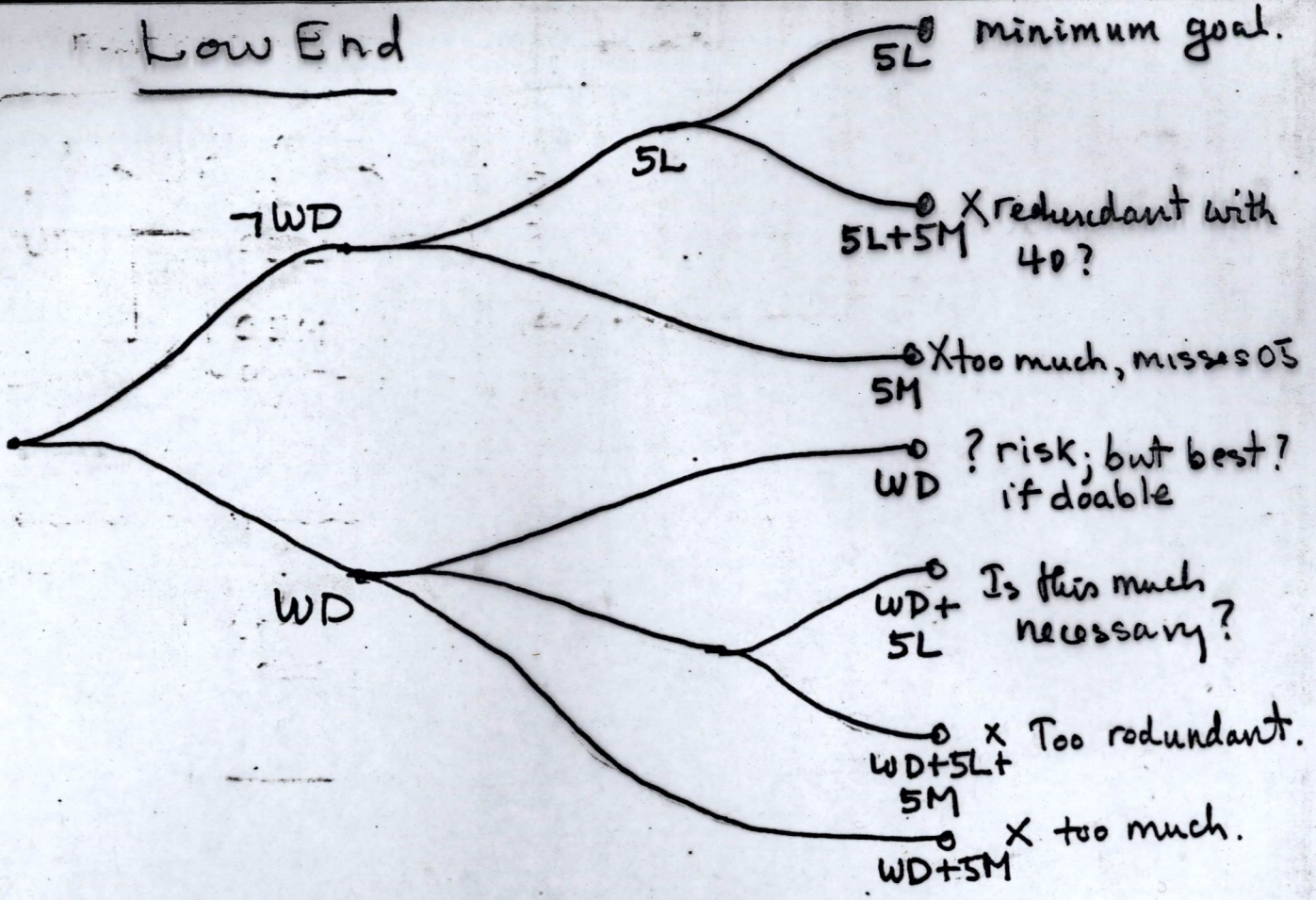
MACHINE	PC COST	PERF.	76 MEMORY (64, 128, 256K) Cost	TOTAL COST ($3XM_p$+Pc)	COST/PERF
45	5	1	2.3*, 4.6, 9.2	11.9, 18.8, 32.6	11.9, 18.8, 32.6
45 MOS	5	1.6	2.9, 5.8, 11.6	13.7, 22.4, 39.8	8.5, 14, 24.9
55	8	2.5	2.3, 4.6, 9.2	14.9, 21.8, 35.6 (25%) (15%) (10%)	6.0, 8.7, 14.2

ALSO ADDRESSES SELLING LOTS MORE MEMORY AND PERIPHERALS. NOW LET'S GET THE SOFTWARE AND TROUNCE HP IN TIME-SHARING AND BATCH.

HAS ADVANTAGE OF BEING FASTER THAN MOS, AT CORE PRICES. WE SHOULD BE ABLE TO STAY OUT OF COMPETITORS REACHES.

*$580/16K FOR CORE; $734 FOR 16K MOS

Low End



Low End Objectives

1. Cover 05 at lower price (850?) and perf/cost x 2 of 05. Get Processor on a board.
2. Can/must we enter Computer-on-a-board market? Or will P-on-a-chip pick us apart? Can we wait for better bipolar to do this?
3. Define board for very low end.
   1. 1~2K~4K w/ Unibus.
   2. WD Bus
   3. Serial bus.
   4. Simple interface (eg. Processor Modules).

GB 6/16/74

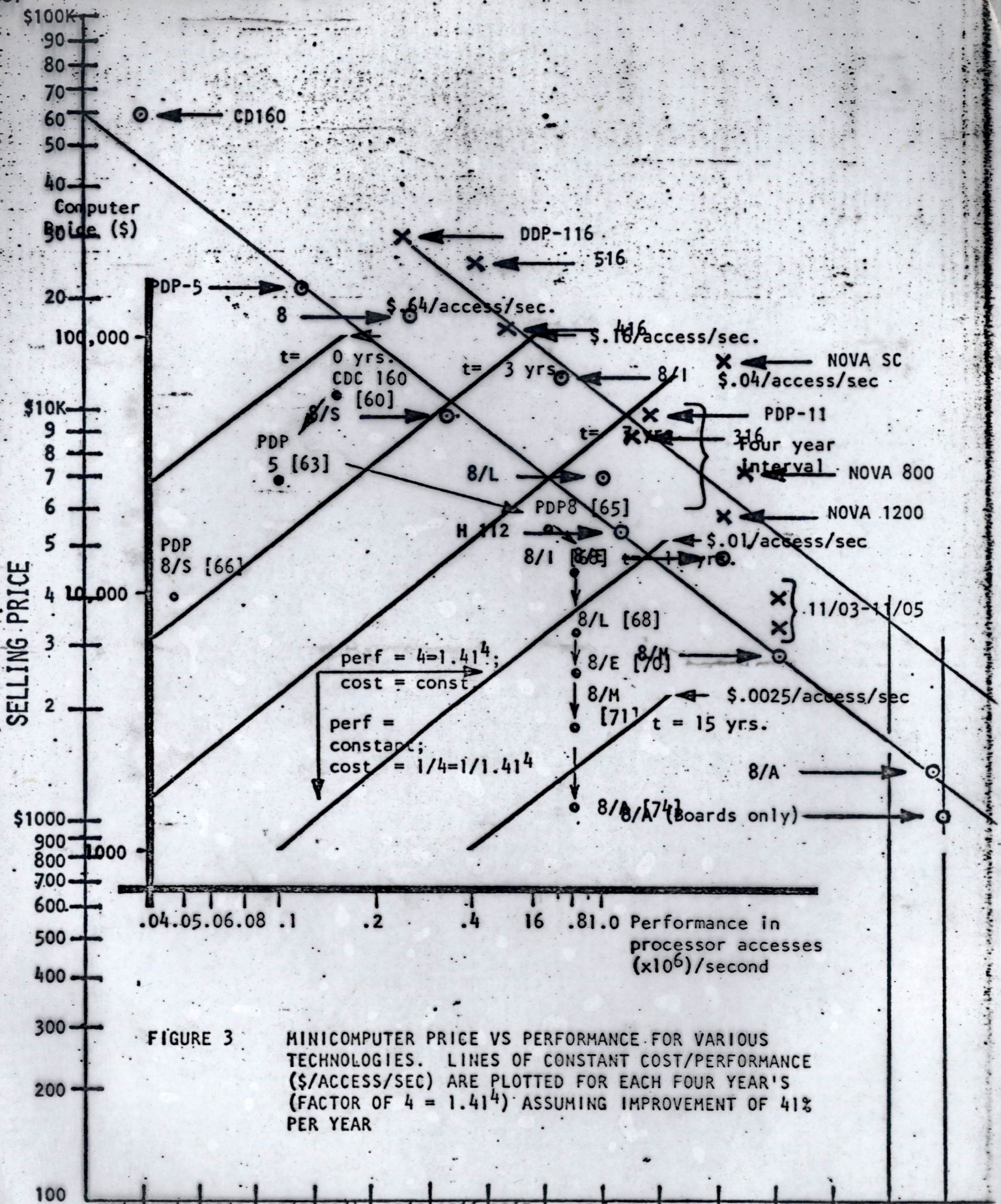
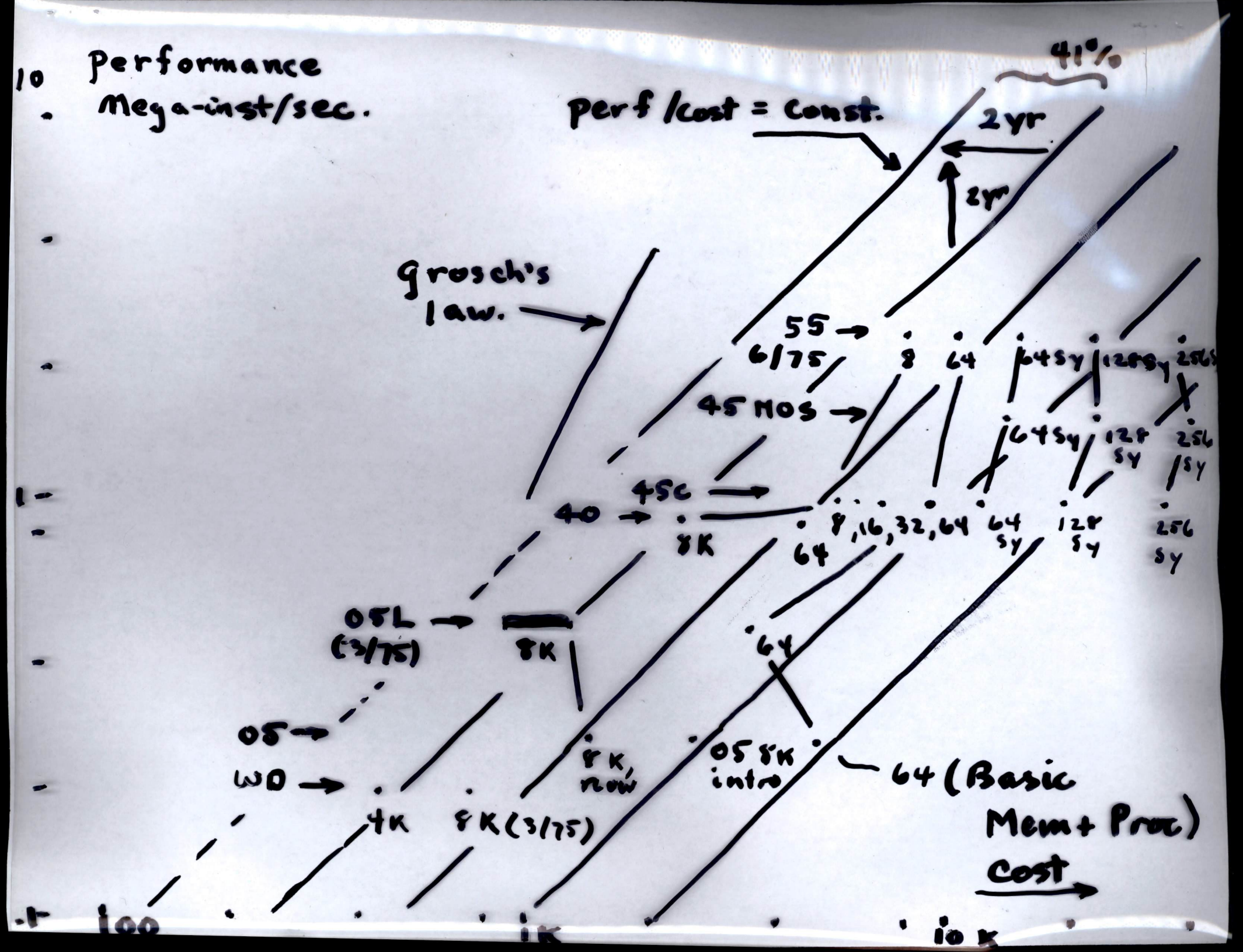


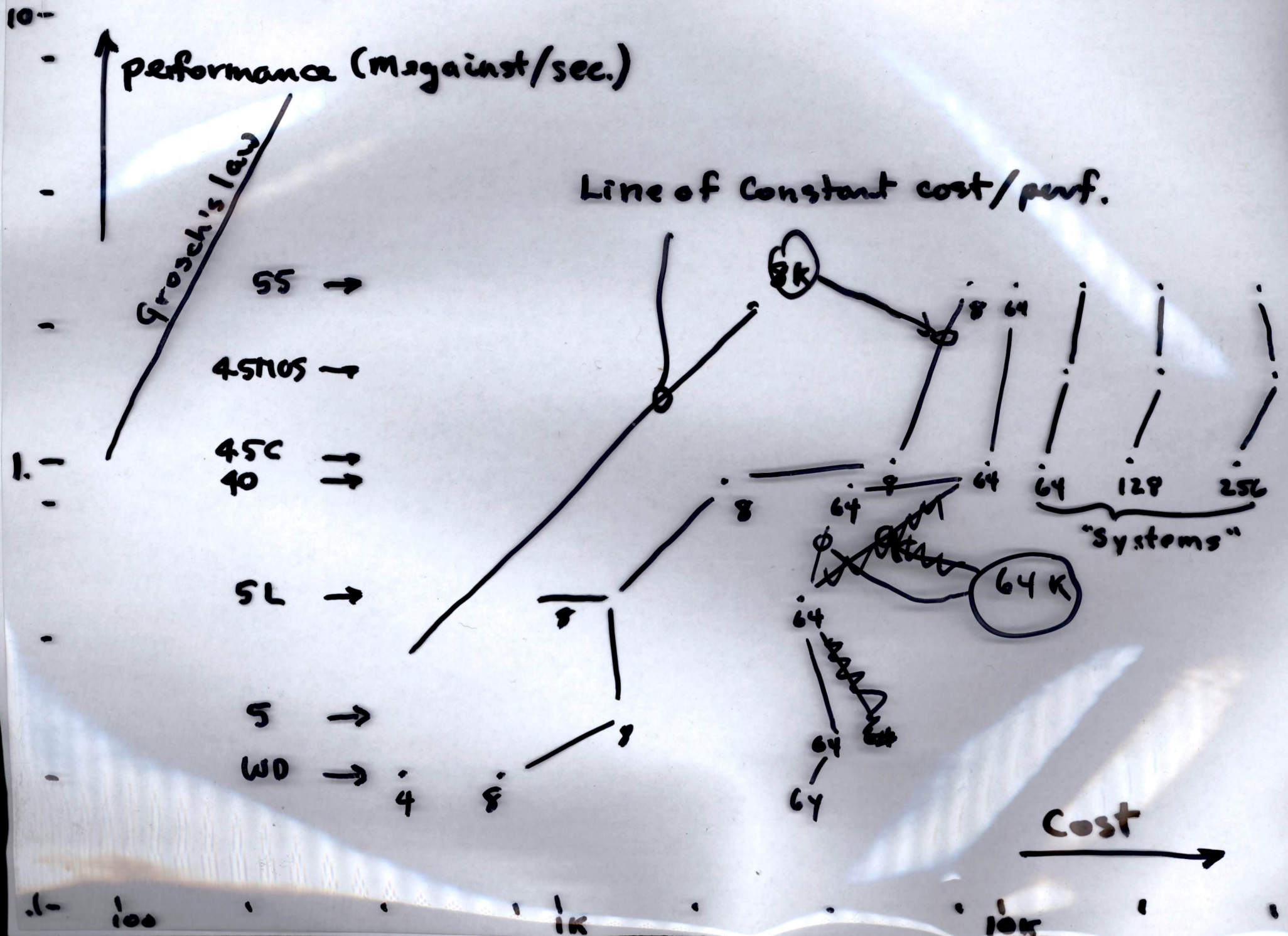
FIGURE 3 MINICOMPUTER PRICE VS PERFORMANCE FOR VARIOUS TECHNOLOGIES. LINES OF CONSTANT COST/PERFORMANCE ($/ACCESS/SEC) ARE PLOTTED FOR EACH FOUR YEAR'S (FACTOR OF 4 = 1.41^4) ASSUMING IMPROVEMENT OF 41% PER YEAR

FIGURE 2 SELLING PRICE VERSUS FIRST DELIVERY DATE FOR MINICOMPUTERS

GB
6/17/74

	P/C	TIME (REG +) (PERF.)	TIME FP+	COST (MEM.)	1st DELIVERY	OPTIONS	PROBLEMS AND [ADVANTAGES]
WD		5? (2.0)	40	45 (4K board only)	3/75	FP, user microcode.	Risk. Config. def. needed. What about serial bus, UNIBUS, WD bus, no bus. [fast micro-code,FP, cheaper bus, processor-on-a-chip.]
OSL		2.0 (.5)	150	85 1.1 (8K)	3/75	--	OK
05M		2 + (.5)	150	1.3 (8k)	6/75	Mem. mgmt.	OK
40L		.7 (1.4)	10~20	1.8 (8K)	12/75	DEC micro-code	Can it be done easily?
4032		.6 (1.6)	10~20	? (8K)	12/75	"	How much?
44+44MP		.6 .3 (1.6 3.2)	10~20	2.4 (16K)	6/76-6/77?	User ~~4~~ code; multi-PC	High risk. New busses and options. [nice structure]
55		.4 (2.5)	3~4	8K (0)*	6/75	45	Lots to do. [Faster than MOS machine at core prices. Reliable. Big enough memory. Realize 45 potential.]
55 MOS		.6 (16)	3~4	5K (0)	3/75?	45	Me too. Won't be better (cheaper) and much faster than MOS machines.
85		1.0 (2)	3~4	7.5 (32KW)	9/76	11 inst. too?	New busses and options? Software? Probably must execute 11 code. [Good against 32 bit vis a vis address space 11/55 is higher performance.]
05		3.7 (.27)	250	1400 (8K)	5/72		
40		1.1 (.9)	20	2.3 (8K)	2/73		
45		1 (1)	3~4	8.7 (32K)	5/72		


Performance
Mega-inst/sec.
10
1
.1
perf/cost = Const.
41%
2yr
2yr
Grosch's law.
55
6/75
8
64
64Sy
128Sy
256Sy
45 MOS
64Sy
128 Sy
256 Sy
45C
40
8K
8,16,32,64
64
64 Sy
128 Sy
256 Sy
05L (3/75)
8K
64
05
WD
4K
8K (3/75)
8K now
05 8K intro
64 (Basic Mem + Proc)
Cost
100
1K
10K


10
performance (Megainst/sec.)
Grosch's law
Line of Constant cost/perf.
55
4ST105
45C
40
5L
5
WD
1.
.1
100
1K
10K
Cost
8K
8
64
64
64
128
256
"Systems"
64K
8
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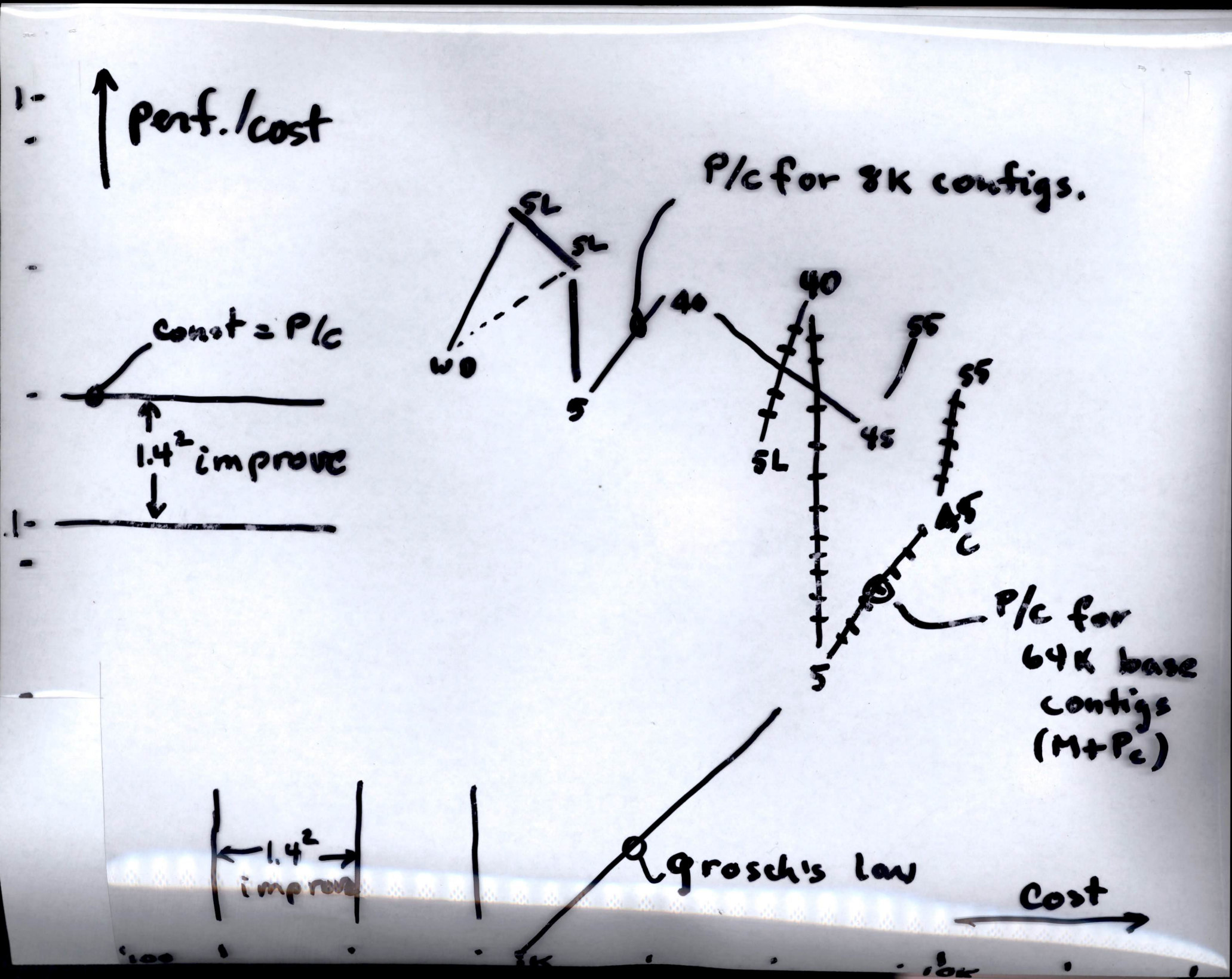
64
64
64
64
64
64
4
8


perf./cost
P/c for 8K configs.
cost = P/c
1.4² improve
1.4² improve
Grosch's law
Cost
P/c for 64K base configs (M+P_c)
100
1K
10K