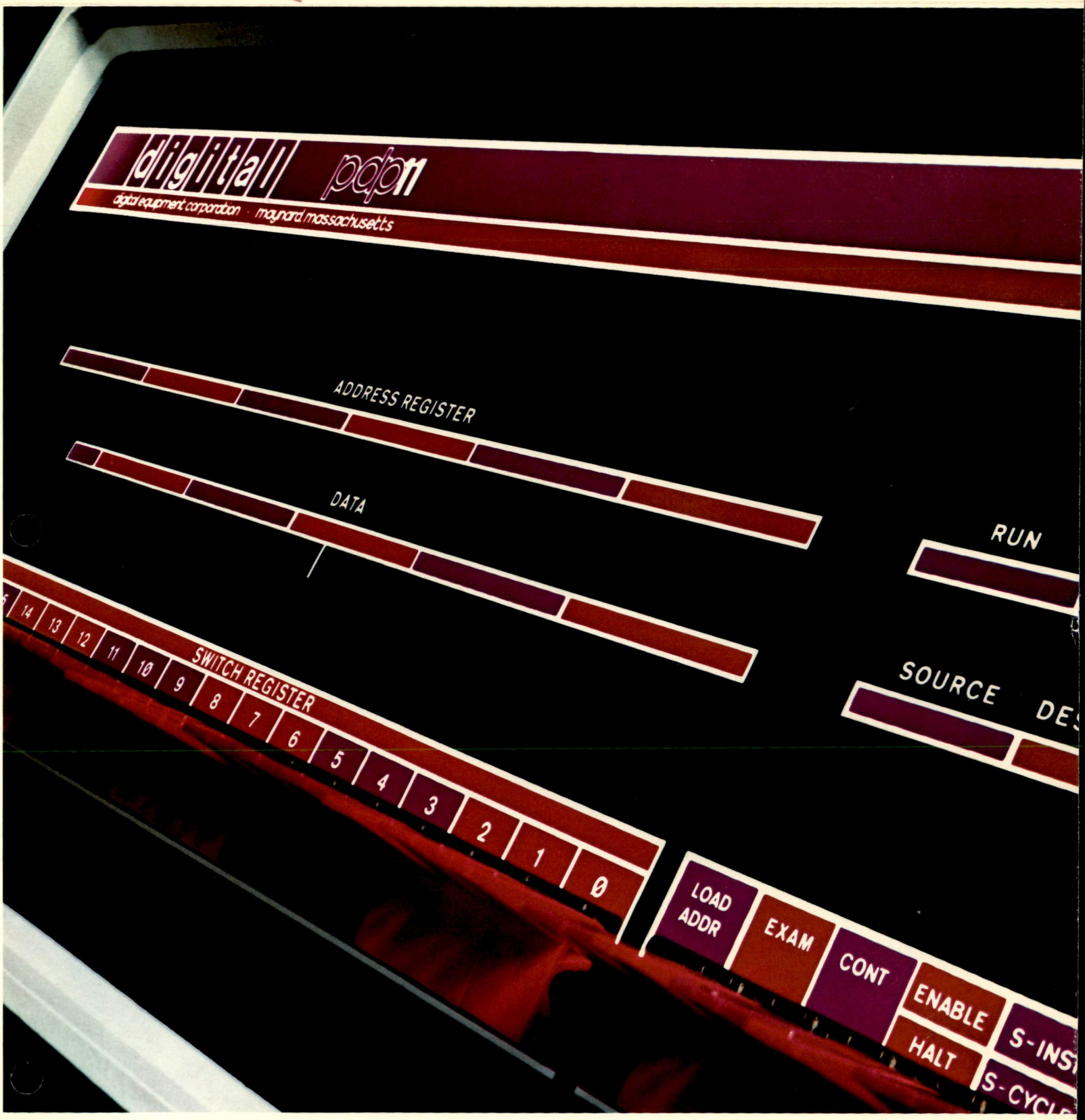
The Next PDP-11's in a Series of Winners



pdp11 memo

TO: Operations Committee

June 21, 1971

FROM: Andy Knowles

SUBJECT: Product Announcement Plans (New PDP-11's)

It is proposed that Operations Committee approve announcement of the new smallest versions of the PDP-11 family.

The Machines

11/03*	3½" X 17" X 19" rack or drawer mountable A small computer, fully '11 compatible, designed for use in small configurations by primarily the OEM. Very attractive for dedicated applications as size is small.
11/05*	5¼" X 19" X 23" rack mountable A larger packaged version of 11/03, allowing larger memories and increased peripheral interface space for the OEM requiring more flexibility.

BOTH MACHINES FULLY UNIBUS AND 11/15 INSTRUCTION SET COMPATIBLE.

* If future market requirements dictate, CPU's and memories may be mounted vertically in 10½" high box allowing use of all 11/20, and 11/25 peripherals and memories within the box. A very powerful future feature allowing tremendous utilization of the space when 10½" is required by memory or I/O interfaces.

MACHINES AT A GLANCE

	11/03	11/05
CPU (Unibus compatible) (11/15 binary compatible)	Standard	Standard
Serial interface to 4800 baud (TTL level)	Optional	Standard
Power Fail and Restart	Standard	Standard
Single line, multi level interrupts (a la 11/15)	Standard	Standard
NPR line with multi device capability (a la 11/15)	Standard	Standard
Programmer's Console	Standard	Standard
Approx. 3.3 μsec reg. to reg. (add speed) vs. 2.3 for 11/20 ≈.850 for 11/25 ≈.290 for 11/45	Standard	Standard
Power Supply	16 amps	16 amps
Memory	4K 850 nsec cycle time 8K max. in box 3½" high	4K 850 nsec cycle time 8K 12K 16K - max. in box 5¼" high
Peripheral Interface Support General Purpose Prewired Pheripheral Slots for KL11 TTY DR11-A General 16-bit I/O M792 Boot Loader CR11 Card Reader LP11 Line Printer CM11 Mark Sense Reader KW11-P Clock PC11 H.S. Reader/Punch PR11 H.S. Reader	# of slots available 1	# of slots available 2 with 12-16K core. # of slots available 5 with 4-8K core
Communications I/O Mounting Slots (DF11 Terminating Options)	# of slots available 1	# of slots available 2
Size	3½" X 17" X 20"	5¼" X 17" X 20"
Mounting	19" rack or small drawer in any position	19" rack

MARGINS

From Past Experience

The average OEM percentage discount for the existing OEM QDA's on 11's is 13.6%. The average current PDP-11 OEM system is valued at $19,500 and generally represents

CPU and Memory (10K average memory)	$10,700
Peripherals including basic TTY	8,800
	$19,500

In the Future

The new average OEM percentage discount on the 11/05 and the 11/03 CPU and memory will be about 29% as derived from the current distribution of machines over signed QDA's and an expected larger number of machines per QDA. Gross margin of an average 8K core only machine is shown at the expected average and maximum discount levels.

11/05 - Recommended price is $4,595 - quantity 1 for features noted on page 2, 4K of memory is $2,600 - additional 4K is $2,395 - 8K chunks are $4,995, etc.

At a quantity of 20-50 or 29%	At a quantity of 200 or 38%
List Price for 8K then = $6,990	List Price = $6,990
X .71	X .62
NET SALE = $4,962	NET SALE = $4,333
EST. COST = $1,800	EST. COST = $1,800

$$\frac{\text{NET SALE - COST}}{\text{NET SALE}} = \% \text{ Gross Margin}$$

Gross Margin = 64%	Gross Margin = 58%

11/03 - Recommended price is $4,095. Other conditions same as 11/05.

At a quantity of 20 - 50 or 29%		At a quantity of 200 or 38%	
List Price for 8K is	$6,490	List Price =	$6,490
	X .71		X .62
NET SALE =	$4,607	NET SALE =	$4,023
EST COST =	$1,750	EST. COST =	$1,750
Gross Margin =	62%	Gross Margin =	56%

11/05 4K gross margin under the same conditions at $4,595 list is (cost est. $1,500)

Qty 20 - 50	200+
54%	47%

11/03 4K gross margin under the same conditions at $4,095 list is (cost est. $1,450)

Qty 20 --50	200+
50%	43%

NOTE: Estimated cost and derivation of gross margin is engineering data and does not include variances, contingencies, warranties, etc. Actual gross margins will be less and during preparation of final pass at Ops Committee we will have better data.

Detail of CPU, box, supply and memory cost are available as it exists engineeringwise.

No, Pete's guys haven't really had a chance to add their expertise to the estimates. Neither have Al's.

THE MARKET

THE "IRON" MARKET

Defined by negligible peripherals, services, relatively low performance. Dedicated controller type equipment is required; i.e., 8-12K core average, powerfail-restart, serial communications interface, box and power supply. The typical customer may or may not want a front console. A high cost and discount conscious marketplace.

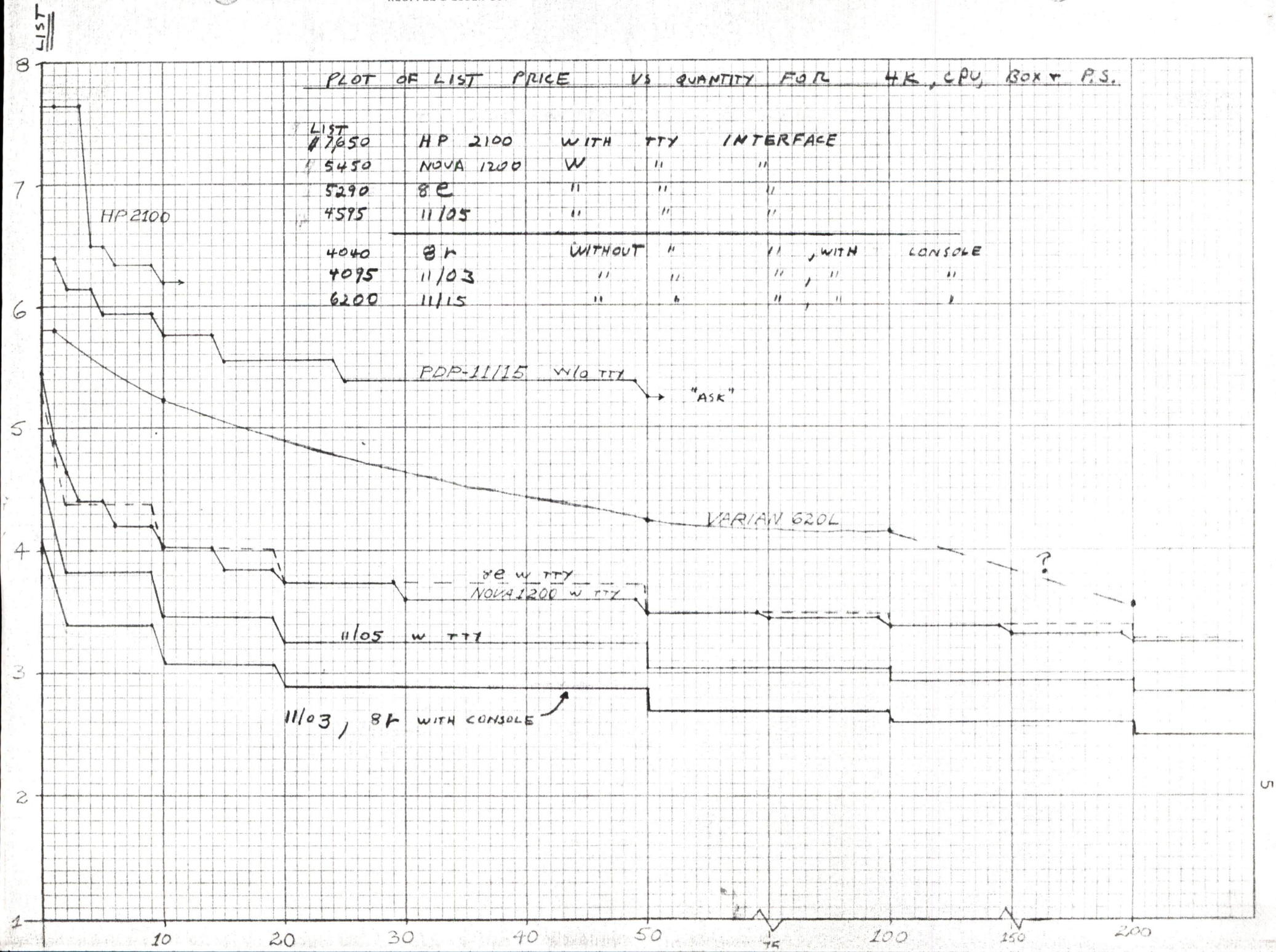
THE COMPETITION

Competition is increasing in numbers and intensity. DG is the current leader, being the first strong competitor into this market with 16 bits. Others are following. The iron market currently is thought to divide as follows:

Current Booking Rate/Yr (Millions of $'s)

PDP-8	10
PDP-11	1
DG 1200	10
HP	1
Honeywell	1
Varian	2
Interdata	2
GA	2
CA	2
Misc.	12
	$43 M Total

Competitive machines and pricing are shown on the attached chart along with new Digital offerings in the market at the suggested list price and new OEM discount schedule.



PDP-11/03, PDP-11/05 PRICE LIST

Type Number	Description	Prerequisites	Price	Mounting Code	Space Requirements	Monthly Maint. (Est.)	Field Installation Rates (Est.)	Discount Status
PDP-11/03A	Computer consisting of: 1. KF11 Central Processor 2. 4K x 16 Read/Write Core Memory 850 ns 3. Basic 3½" Mounting Box and Power Supply 4. Programmers Console 5. Schematics Mounted in a 3½"x17"x20" box. It has space for a total of 8K of core memory, one small peripheral controller, and a serial communications control to 4800 baud.	None	$4095			75	$250	Yes
PDP-11/03B	As above, but includes 8K of core memory	None	$6490			100	$250	
PDP-11/05A	Computer consisting of: 1. KF-11 Central Processor 2. 4K x 16 Read/Write Core Memory 850 ns 3. Basic 5¼" Mounting Box and Power Supply 4. Teletype Control 5. Programmers Console 6. Schematics Mounted in a 5¼" mounting box allowing 12-16K of core memory and two small peripheral controllers or 4-8K core memory and five small peripheral controllers, and a serial communications control to 4800 baud.	None	$4595			75	$250	Yes
PDP-11/05B	Same as 11/05A but includes 8K of core memory	None	$6990			100	$250	
Mounting Options								
Mtg-11	Hardware necessary to mount the PDP-11/05 in a standard 19" rack Does not include cabinet or slides.	PDP11/05 or PDP11/03	$50				$ 75	Yes
Core Storage								
MM11-K	4K words of 16 bit read/write core memory. 850 ns cycle time.	PDP11/05 A&B	$2600	A	3	25	$150	Yes
MM11-L	8K words of 16 bit read/write core memory. 850 ns cycle time.	PDP11/05 A&B	$4995	A	3	50	$150	Yes

Peripheral Devices

The following list of peripheral devices mount in the available small peripheral controller slots in the PDP-11/05 basic box. These devices may be found in the PDP11/20 price list.

BM792 YA & YB	Bootstrap Loaders
CR11	Card Reader
PC11	High Speed Paper Tape Reader Punch
KL11	Teletype Controller
LP11	Line Printer
DR11A	General Purpose Interface

All other peripheral devices on the PDP11/20 price list require the standard BA11ES PDP-11 Extension Mounting Box and H720 Power Supply for proper mounting and operation. The larger peripheral devices such as the Magtape and Disks are compatible with the UNIBUS which is the common element of the PDP-11 family of computers.

System Software and Services Policy

System Software

1.	Assembler	
2.	Editor	
3.	Debugger	
4.	Floating Point Package	
5.	I/O Executive	
6.	Binary Dump	
7.	Octal Dump	
8.	Programming Manual	$100.00

Diagnostic Software (Listings & Tapes)		$100.00
Maintenance Manual		$100.00
Training	- Two weeks of hardware and one or two weeks of software training	$900.00

On-Site Warranty - The warranty for any or all elements of the system is the sum of the published monthly maintenance prices for those elements.

Installation - Each element of the system is installed according to the published price.

TERMS AND CONDITIONS OF SALE
(For 8's and 11's, OEM sales only)

A new, aggressive discount schedule is proposed allowing DEC a highly competitive position in the OEM "iron market". End user sales are protected by the existing separate end user discount schedule. The list price for equipment affected by the new OEM discount schedule allows adequate gross margin. The significant "system" OEM business currently committed to PDP-11's is protected by the discount schedule for peripherals and existing PDP-11's.

NOTE: Discount starts at quantity 2.

DISCOUNT SCHEDULE
(Applies to CPU's & Memories Only)
(8/e, 8/r, 11/03, 11/05)

Qty CPU's	Discount
2-9	17%
10-19	24%
20-49	29%
50-99	34%
100-199	36%
200 +	38%

DISCOUNT SCHEDULE
(Applies to Peripherals & Options Built by DEC Now & Also Includes 11/15, 11/20's As Exist)

2-9	7%
10-19	13%
20-49	16%
50-99	18%
100-199	20%
200 +	Ask Maynard

TERMS AND CONDITIONS OF SALE continued

1. Documentation and Diagnostics

The OEM buyer receives one set of reproducible diagnostics solely for use on DEC computers with the first system ordered. One set of circuit schematics will be provided with each machine. Additional sets of documentation and training courses are available at a nominal fee.
Training - No training is included under these terms and conditions. Training will be available per a price schedule.

2. Warranty

The equipment is warranteed under these OEM terms and conditions to be free from manufacturing and material defects for a period of 30 days after delivery. Under this warranty, equipment purchased from DEC which becomes defective will be repaired by DEC at a location to be designated by DEC at the time of purchase, the cost of freight to be borne by the purchaser, never further in distance, however, than the DEC plant in Maynard, Massachusetts.

In addition, DEC equipment sold under these terms and conditions is warranteed for a supplementary 30 days after the OEM's end user's equipment of which DEC's is a component is delivered. Such delivery must occur within six months of original delivery and the OEM buyer must notify DEC of date of shipment of equipment to the end user within five days of the date of said shipment in order that this warranty be in effect. Repair terms for the supplementary 30 days will be the same as for the first 30 days so noted. All systems modules are warranteed against defects for a period of one year. Under this warranty, equipment purchased from DEC which becomes defective will be repaired by DEC at a location to be designated by DEC at the time of purchase, the cost of freight to be borne by the purchaser, never further in distance, however, than the nearest DEC manufacturing plant.

3. Special Conditions

The OEM may market DEC equipment as part of a larger system or with the addition of proprietary software under its own trademarks and tradenames. The OEM may remove, at no cost to DEC, any DEC trademark, tradename or other identification

from any equipment purchased under these terms and condition provided DEC agrees to remove, in writing, without any price reduction and at such additional expense to buyer as is involved to DEC.

Purchase orders for all DEC products to be discounted under these terms and conditions must be received by DEC with sufficient lead time so that normal delivery can be scheduled by DEC during the effective period of these terms and conditions. No delivery will be scheduled until a binding purchase order is received from the OEM at DEC, Maynard, Massachusetts.

Prior to fulfilling the quantity commitment of this agreement, the OEM will receive a discount equal to one half that specified by the appropriate quantity on the contained schedule, or the discount successfully completed last year, whichever is greater. This QDA is to be accompanied by a monthly release schedule to reflect the gross total subscribed. Machines will be released against this schedule unless a change is received at Maynard, Massachusetts, 60 days prior to the first day of the month of release effected. The OEM must release within 40% of the original release schedule. If the OEM fails to do so, he will revert to the next lower discount level.

If the OEM fails to release for delivery during the effective period of these terms and conditions (normally one year), the number of products required under these terms and conditions, the discounts for the equipment shall be recalculated using the actual quantities delivered. Unearned discounts will be billed back with 8% interest (from the due date of each invoice previously issued and the bill back date).

Payment terms are net 30 days. If payment exceeds 30 days from the date of DEC invoice, an interest charge of 1.5% per month on the unpaid balance will be charged accordingly.

All other current protection will be added to DEC OEM agreements so constructed.

Hardware-Software Service Content of PDP-8/e, PDP-8/r, 11/20, 11/15, 11/03, 11/05

	BASIC PDP-8/e	BASIC PDP-8/r	11/20	11/15	11/03	11/05
PRICE	$4,990	$3,690	10,800	$6,200	$4,095	$4,595
CP	Yes	Yes	Yes	Yes	Yes	Yes
Memory	4K by 12 bit	4K by 12 bit	4K by 16 bit	4K by 16 bit	4K by 16 bit 8K by 16 bit	4K by 16 bit 8K by 16 bit
Console	Programmers	Operators	Programmers	Programmers Controllers (-$200)	Programmers	Programmers
TTY Control	KL8-E	None	Yes	No	No	Yes
Schematics	Yes	Yes	Yes	Yes	Yes	Yes
Diagnostics	Yes	No	Yes	Yes	No	No
Sys. Programs	Yes	No	Yes	No	No	No
Installation	Yes	No	Yes	Yes	No	No
Warranty	90 day on site	30 day return to Depot	90 day on site	30 day on site	Depot 30/30	Depot 30/30
Training	2 credits	None	1 Unit	None	None	None
Prime Market	End User & OEM	OEM Only	End User	OEM	OEM	OEM

FORECAST

FY '72

	Q1	Q2	Q3	Q4
# of units		15	150	300
$ value (net) (≈8K machines 25% discount)		.080M	.52M	1.65M

SCHEDULE

July 9, 1971	Proto Running
Oct. 15, 1971	Release to Production
Nov. 1971	First Deliveries from Factory

digital equipment corporation

digital INTEROFFIC

KEN OLSEN
12-1

MAR 28 1973

TO: Engineering Managers
Marketing Managers
Operations Committee
Product Line Managers
Software Engineering and Services Managers

DATE: March 2, 1973

FROM: Software Engineering Managers

DEPT: Software Engineering

EXT : 4067

SUBJ: PDP-11 Operating Systems Characteristics

Attached are five tables of characteristics for the major PDP-11 operating systems as they exist now -- and as they are currently planned over the next year. Of particular interest is an exhaustive list of PDP-11 peripherals with an indication of which systems support them. It is hoped that this information will be valuable in Fiscal 1974 product planning. Additional copies are available from David Stone's office.

jmab

Attachment

PDP-11 SYSTEM SUPPORT TABLES

Key:		
	X	Supported now
	Rn	Supported with Release n (see Release Definitions below)
	Dash (-)	No support planned
	Want	No support planned at present, but desirable
	Possible	Could be supported by specified system
	N.A.	Not applicable

Named systems within tables indicate that the feature is supported by the specified system only.

Release Definitions

CAPS-11

Cassette programming system for an 8K PDP-11 with dual cassette drives. This small operating system includes a monitor, editor, relocatable assembler, linker, and PIP.

R1 - May 1973
R2 - Q2FY74 (includes BASIC)
R3 - Not scheduled, likely Q3FY74 (includes FORTRAN)

RSX-11A

Small-scale, real-time, multi-tasking executive designed for core-only and core/disk systems and the papertape environment.

R1 - March 1973

RSX-11B

Medium-scale, real-time executive with disk support.

R1 - Pre-release #1, October 1971
R2 - Pre-release #2, December 1971
R3 - February 1972
R4 - April 1972
R5 - August 1972
R6 - May 1973

RSX-11C

Medium-scale, real-time executive with core-only capabilities.

Release dates same as for RSX-11B

RSX-11D

Large-scale, real-time executive with emphasis on process control.

R1 - May 1973
R2 - Not scheduled, likely December 1973
R3 - Not scheduled

RSTS

11/20-based, BASIC-only, time-sharing system with up to 12 users.

R1 - August 1971
R2 - November 1971
R3 - March 1972 (V3C-32)
R4 - October 1972 (V4A-12)
R5 - Not scheduled (V4B)

RSTS/E

11/40/45-based, BASIC-only, time-sharing system with up to 32 users.

R1 - May 1973

MUMPS

Stand-alone operating system supporting a language and a data base structure designed to provide a basis for building multi-user, time-sharing applications systems oriented towards commercial and medical markets. The string processing capabilities of the MUMPS structure are best realized in order entry and retrieval, inventory control, personnel and medical record, and scheduling system.

R1 - January 1973
R2 - September 1973

RT-11

Small, single-user operating system that will run on an 8K PDP-11 with mass storage. The system will contain device-independent, interrupt-driven I/O and will allow users to effectively program the PDP-11 in the real-time (and non real-time) environments. The command language will be compatible with TOPS-10; source level and file compatibility with RSX-11D programs is a goal.

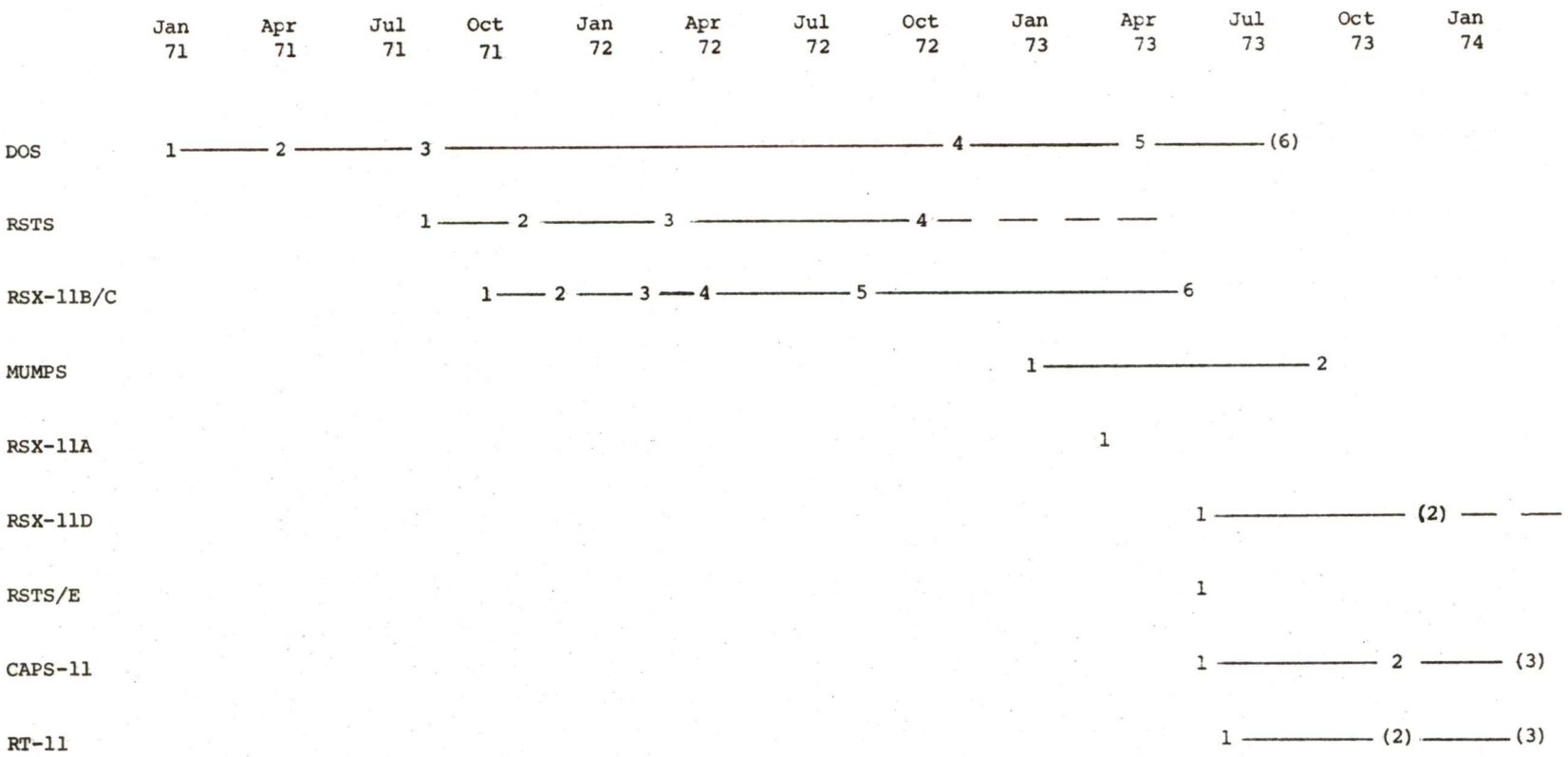
R1 - June 1973
R2 - Not scheduled, likely Q2FY74
R3 - Not scheduled, likely Q3FY74 (includes FORTRAN)

DOS

Single-user, disk operating system designed for program development.

R1 - January 1971
R2 - April 1971
R3 - August 1971 (V4A)
R4 - November 1972 (VØ8-Ø2)
R5 - April 1973 (VØ8-Ø8)
R6 - Not scheduled, likely Q1FY74

PDP-11 Operating System Release Plan



Release numbers in parentheses are tentative only.

Dotted lines indicate that additional, but unscheduled, releases are planned.

Table 1

System Support of Hardware

HARDWARE ITEM		SUPPORTING SYSTEMS									
		CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
AA11-D	Digital-to-Analog Converter Subsystem	-	-	-	-	-	-	-	-	-	-
AD01-D	Analog-to-Digital Conversion Subsystem - High Level	-	R1	X	X	R1	-	-	-	-	-
AFC11	Master Low-Level Differential Analog Input Subsystem	-	R1	X	X	R1	-	-	-	-	-
AFC8XA	2nd, 3rd, 5th, or 6th Expander Low-Level Differential Analog Input Subsystem	-	-	X	X	-	-	-	-	-	-
BA14	Digital-to-Analog Converter Subsystem	-	-	-	-	-	-	-	-	-	-
BA614	Digital-to-Analog Converter	-	-	-	-	-	-	-	-	-	-
UDC11	Master Digital Input/Output Subsystem	-	R1	X	X	R1	-	-	-	-	-
BM792-YA	Paper-Tape Bootstrap Loader	-	-	-	-	-	-	-	-	-	-
BM792-YB	Bulk Bootstrap Loader	-	-	X	X	-	X	R1	X	R1	X
BM792-YC	Card-Reader Bootstrap Loader	-	-	-	-	-	-	-	-	-	-
MR11-DB	Multi-Device Bulk Storage Bootstrap Loader	-	-	X	X	R1	X	R1	X	R1	X
CD11	1000 cpm Reader for 80-column punched cards	-	-	-	-	R2	-	-	-	-	R6
CM11	200 cpm Reader for 40-column marked cards	-	-	-	-	-	X	R1	-	-	X
CR11	300 cpm Reader for 80-column punched cards	-	-	-	-	R1	X	R1	Want	-	X
DC11-Ax	Dual Clock & System Unit Mounting	-	-	-	-	-	X	R1	X	-	-
DC11-DA	Full-Duplex Serial Module Set	-	-	-	-	-	X	R1	X	-	-
DH11	Asynchronous 16-line Multi-Speed Multiplexer	-	-	-	-	R3	-	R1	R2	-	-
DJ11	Asynchronous 16-line Single-Speed Multiplexer	-	-	-	-	-	-	-	-	-	-

Table 1 (Cont.)

System Support of Hardware

HARDWARE ITEM		SUPPORTING SYSTEMS									
		CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
DL11-A	Current Loop Serial Line Interface	-	-	X	X	R1	X	R1	X	-	X
DL11-B	EIA RS232C Serial Line Interface	-	-	-	-	-	X	R1	X	-	-
DL11-C	Current Loop Serial Line Interface	-	-	-	-	-	-	-	X	-	-
DL11-D	EIA RS232C Serial Line Interface	-	-	-	-	-	-	-	X	-	-
DL11-E	Modem Controlling EIA RS232C Serial Line Interface	-	-	-	-	-	X	R1	X[1]	-	-
DM11-Ax	Asynchronous 16-line Single-Speed Multiplexer	-	-	-	-	-	-	-	-	-	-
DM11-BB	Modem Control Multiplexer	-	-	-	-	-	-	R1	-	-	-
DM11-DA	Line Adapter for four local terminals	-	-	-	-	-	-	R1	-	-	-
DM11-DB	Line Adapter for four EIA lines	-	-	-	-	-	-	R1	-	-	-
DM11-DC	Line Conditioning for four EIA RS232C compatible lines	-	-	-	-	-	-	R1	-	-	-
DN11-AA	System Unit Mounting	-	-	-	-	-	-	-	-	-	-
DN11-DA	Module Set Interface	-	-	-	-	-	-	-	-	-	-
DP11-CA	Data/Sync Register Extender	-	-	-	-	-	-	-	-	-	-
DP11-DA	Full/Half-Duplex Synchronous Interface	-	-	-	-	-	-	-	-	-	-
DP11-KA	Internal Clock	-	-	-	-	-	-	-	-	-	-
FP11-B	Floating-Point Processor (11/45)	R2	-	-	-	R1	R5	R1	R2	R1	X
KD11-B	11/10 Central Processor	R1	R1	X	X	-	-	-	X[3]	R1	X
KA11-B	11/15 Central Processor	R1	R1	X	X	-	X	-	X[3]	R1	X
KA11	11/20 Central Processor	R1	R1	X	X	-	X	-	X[3]	R1	X
KD11-A	11/40 Central Processor	R1	R1	X	X	R1	X	R1	X[3]	R1	X
KB11	11/45 Central Processor	R1	R1	X	X	R1	X	R1	X[3]	R1	X
	Memory Limitations	8-28	4-28	16-28	16-28	24-124[2]	24-28	40-124	28-124 (R2)	8-28	8-28

[1]Modem control supported in Release 2.

[2]For Release 2 with BATCH, core limitations are 32 - 128.
For Release 2 with BATCH and Real-Time Processing, core limitations are 40 - 128.

[3]Release 1 requires EAE; Release 2 supports EIS.

Table 1 (Cont.)

System Support of Hardware

HARDWARE ITEM		SUPPORTING SYSTEMS									
		CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
KT11	Memory Management Option	-	-	-	-	R1	-	R1	R2	-	-
KE11-A	Extended Arithmetic Element (EAE)	-	-	X	X	-	X	-	X	-	X
KE11-E	Extended Instruction Set (EIS 11/40)	R2	-	-	-	R1	-	R1	R2	R1	X
KE11-F	Floating Point (FIS 11/40)	-	-	-	-	R1	-	R1	R2	-	R5
KG11-A	Communications Arithmetic Element	-	-	-	-	-	-	-	-	-	-
KL11-A	Full-Duplex Interface - 110 baud	-	-	X	X	R1	X	R1	X	-	X
KL11-B	Full-Duplex Interface - 150 baud	-	-	X	X	R1	X	R1	X	-	X
KL11-C	Full-Duplex Interface - 300 baud	-	-	X	X	R1	X	R1	X	-	X
KL11-D	Full-Duplex Interface - 600 baud	-	-	-	-	R2	X	R1	X	-	-
KL11-E	Full-Duplex Interface - 1200 baud	-	-	-	-	R2	X	R1	X	-	-
KL11-F	Full-Duplex Interface - 2400 baud	-	-	-	-	R2	X	R1	X	-	-
KW11-L	Line Frequency Clock	-	R1	X	X	R1	X	R1	X	-	X
KW11-P	Programmable Real-Time Clock	-	-	-	-	R2	X	R1	X	-	X
GT40	Graphic Terminal	-	-	-	-	-	-	-	-	-	-
LA30-P	Parallel DECwriter Hard-Copy Terminal	R1	R1	X	X	R1	X	R1	X	R1	X
LA30-S	Serial DECwriter Hard-Copy Terminal	R1	-	X	X	R1	X	R1	X	R1	R5
LT33-DC	ASR-33 Hard-Copy Terminal with Paper-Tape Reader/Punch (no binary)	R1[4]	R1	X	X	R2	X	R1	X[4]	R1[4]	X
LT33-CC	KSR-33 Hard-Copy Terminal without Paper-Tape Reader/Punch	R1	R1	X	X	R1	X	R1	X	R1	X
LT35-DC	ASR-35 Hard-Copy Terminal with Paper-Tape Reader/Punch (no binary)	R1[4]	R1	X	X	-	X	R1	X[4]	R1[4]	X
LT35-CC	KSR-35 Hard-Copy Terminal without Paper-Tape Reader/Punch	R1	R1	X	X	R1	X	R1	X	R1	X
LP11-F	300 lpm Printer - 80 columns, 64-characters	R1	R1	X	X	R1	X	R1	X	R1	X
LP11-H	300 lpm Printer - 80-columns, 96-characters	-	-	X	X	R1	X	R1	X	-	X

[4] No reader/punch support

Table 1 (Cont.)

System Support of Hardware

HARDWARE ITEM		SUPPORTING SYSTEMS									
		CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
LP11-J	300 lpm Printer - 132-columns, 64-characters	-	-	X	X	R1	X	R1	X	-	X
LP11-K	300 lpm Printer - 132-columns, 96-characters	-	-	X	X	R1	X	R1	X	-	X
LP11-R	1200 lpm Printer - 132-columns, 64-characters	-	-	-	-	R2	-	-	X	-	R6
LP11-S	800 lpm Printer - 132-columns, 96-characters	-	-	-	-	R2	-	-	X	-	R6
LS11	Centronix Line Printer	R1	R1	X	X	R2	R5	R1	R2	R1	R6
LPS-11	Lab Peripheral System	-	-	-	-	R2	-	-	-	R1	-
PC11	300 cps Paper-Tape Reader, plus 50 cps Paper-Tape Punch	R1	R1	X	X	-	X	R1	X	-	X
PR11	300 cps Paper-Tape Reader	R1	R1	X	X	-	X	R1	X	-	X
RK05	1.2-million-word Moving-Head DECpack Disk Drive	-	R1	X	X	R1	X	R1	X	R1	X
RP02	10-million 16-bit-word Moving-Head Disk Pack Drive	-	-	-	-	R2	-	-	R2	-	-
RP03	20-million-word Moving-Head Disk Pack Drive	-	-	-	-	R2	-	R1	R2	-	R6
RS11	262K Fixed-Head Disk Drive	-	R1	X	X	R1	X	R1	X	-	X
RS64	64K-word DECdisk Fixed-Head Disk Drive	-	R1	X	X	-	X	-	-	-	X
TA-11	Cassette	R1	-	-	-	-	-	-	-	R1	R6
TU10-EX	9-channel Tape Transport	-	-	-	-	R1	X	R1	X	-	X
TU10-FX	7-channel Tape Transport	-	-	-	-	R1	X	R1	X	-	X
TU56	Dual DECtape Transport	-	-	X	X	R1	X	R1	X	R1	X
VR01-A	Tektronix RM503 Oscilloscope Display	-	-	-	-	R3	-	-	-	-	-
VR14	7" x 9" Point Plot Display	-	-	-	-	-	-	-	-	-	-
VT01-A	Tektronix 611 Storage Tube Display	-	-	-	-	R3	-	-	-	-	-
VT05	Alphanumeric CRT Terminal (300 baud)	R1	R1	X	X	R1	X	R1	X	R1	X

Table 2

Media of System Distribution

MEDIA	SYSTEMS									
	CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
Paper Tape	-	R1	X	X	-	-	-	-	-	X
Cassettes	R1	-	-	-	-	-	-	-	-	-
DECtape	-	R1	X	X	R1	X	R1	X	R1	X
Magnetic Tape - 7-channel	-	-	-	-	R1	R5	R1	X	-	X
Magnetic Tape - 9-channel	-	-	-	-	R1	R5	R1	X	-	X
RK (Disk) Cartridge	-	-	X	X	-	R5	-	-	R1	-
RP03	-	-	-	-	-	-	-	-	-	-

Table 3

System Support of Programs

PROGRAMS	SUPPORTING SYSTEMS									
	CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
SORT	-	-	-	-	R3	R5	R1	-	-	COS-520
Editors: Batch Editor	-	-	-	-	R1	-	-	-	-	-
Interactive Editor	R1	-	X	X	R3	X	R1	-	R1	X
LINKER	R1	-	X	X	R1	N.A.	-	-	R1	X
OVERLAY	-	-	X	-	R1	X	R1	X	R1	X
CREF	-	-	-	-	R2	N.A.	-	-	R2	X, except 8K versions
SYSGEN	-	R1	-	-	R1	X	R1	X	R1	X
File Manipulation: PIP	R1	-	X	-	R1	X	R1	-	R1	X
BACKUP	-	-	-	-	Want	R5	R1	X	-	-
Librarians	-	-	-	-	R1	N.A.	-	N.A.	R1	X
Debugging: ODT	R1	-	X	X	R1	N.A.	-	-	R1	X
DDT - Assembler & higher level	-	-	-	-	Want	N.A.	-	-	-	-
TRACE	-	-	-	-	-	-	-	X	-	-
File Compare: Source	-	-	-	-	R2	-	-	X	-	R5
Data file	-	-	-	-	R2	-	-	-	-	-
Accounting Routines	-	-	-	-	Want	X	R1	-	-	-
PATCH	-	-	-	-	R1	Minimum available	-	X	R1	Minimum available
Data Editing	-	-	-	-	-	-	-	X	R1	-
Data Acquisition	-	-	X	X	R1	-	-	X	R1	-

Table 4

System Support of Languages

LANGUAGES	SUPPORTING SYSTEMS									
	CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
FORTRAN IV	R3	-	OTS only	OTS only	R1	-	-	-	R3	X, with minimum of 12K
FORTRAN 45/40	-	-	-	-	R2	-	-	-	-	-
ASSEMBLER: MACRO/NON-MACRO	R1 PAL-11S	-	-	-	R1	-	-	-	R1	X
MUMPS	-	-	-	-	R2 dependent	-	-	X	-	-
COBOL 11	-	-	-	-	R2	-	-	-	-	-
RPG II	-	-	-	-	R3	-	-	-	-	X
ALGOL	-	-	-	-	-	-	-	-	-	-
FOCAL	-	-	-	-	-	-	-	-	-	-
BASIC	R2	-	-	-	R3	X	R1	-	R1	-
DIBOL	-	-	-	-	-	-	-	-	-	-

Table 5

System Support of Products

PRODUCTS	SUPPORTING SYSTEMS									
	CAPS-11	RSX-11A	RSX-11B	RSX-11C	RSX-11D	RSTS	RSTS/E	MUMPS	RT-11	DOS
Interactive 1-user Disk System	-	-	X	X	-	-	-	-	R1	DOS-11
Interactive 1-user Disk and/or DTA with Real Time	-	-	X	X	-	-	-	-	R1	-
Interactive 1-user Disk with Communications	-	-	-	-	-	-	-	-	Possible	DOS/COMTEX
1-user Commercial/BATCH	-	-	-	-	R2	-	-	-	-	COS-500
BATCH 1-user	-	-	-	-	R2	-	-	-	Possible	DOS/BATCH
Interactive n-user RPG	-	-	-	-	R3	-	-	-	-	-
Interactive n-user Real-Time	-	R1	-	-	R1	-	-	-	-	-
BASIC - small number of users	-	-	-	-	R3	Mini RSTS	-	-	-	-
BASIC - n-user, medium number of users	-	-	-	-	R3	X	R1	-	-	-
BASIC - n-user, large number of users	-	-	-	-	-	-	R1	-	-	-
Multi-stream high-thruput BATCH	-	-	-	-	R2	-	-	-	-	-
MUMPS low-entry	-	-	-	-	-	-	-	X	-	-
MUMPS high-performance, communications support	-	-	-	-	-	-	-	R2	-	-
High-thruput Communication System, n-user disk	-	-	-	-	R3	-	-	-	-	-
Multi-tasking with BATCH	-	-	-	-	R2	-	-	-	-	-
Multi-tasking without BATCH	-	R1	X	X	R2	-	-	-	-	-
Limited time-sharing with BATCH	-	-	-	-	R3	-	-	-	-	-
Limited time-sharing without BATCH	-	-	X	X	R3	-	-	X	-	-
General purpose time-sharing with BATCH	-	-	-	-	-	-	-	-	-	-
General purpose time-sharing without BATCH	-	-	-	-	-	-	-	X	-	-
Lab Application Support	-	-	X	X	-	-	-	-	R2	-

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: February 16, 1973

FROM: Roger Dow

DEPT: Central 11 Marketing

EXT : 2488

Gordon Bell - 3/5

SUBJ: SOFTWARE SUPPLIED WITH PDP-11's

Present Situation

There is a feeling that we ship too much software with PDP-11 equipment. I have been looking into the situation and have gathered and examined samples of hardware manuals, customer print sets, programming manuals and program descriptions (listings). I have talked to many of the people involved in generating, controlling, and using this material.

A complete set of programming software for the PDP-11/10 fills up a 1 cubic foot box. At least 2/3 of this is for maintenance (diagnostic) purposes, rather than reference by the customer. Four trays of paper tape software would be included, 2 of them for diagnostics. Field Service is planning on using a cassette for the loading of diagnostic programs.

My Assessment

An unsophisticated customer would be staggered by the amount of software he received with his equipment. Most customers would not use the diagnostic material, but Field Service needs it when they service the equipment (Field Service can't be expected to carry everything). Hardware and systems software manuals are absolutely needed by the customer.

There is probably some duplucation in the material. Sometimes 2 sets of diagnostics are sent out when a CPU and peripherals are involved. OEM's get extra sets of software they shouldn't get, because there is not adequate record keeping in the various manufacturing plants where the equipment is shipped from. OEM's are supposed to get free software only with the first system.

The fastest payoff to DEC would be to eliminate some of the punching and free distribution of paper tapes to customers. There is already a punching capacity problem. We should charge for more of the software that is presently free.

RECOMMENDATIONS

Very Soon

Stop sending customers (for free) the basic paper tape diagnostics, tests 1 through 13, on the PDP-11/05 and 11/10. Almost all field failures can be detected by the higher level diagnostics, which would still be supplied. Field Service and Engineering are running some experiments to see if this can really be done without detrimental effects. Elimination of these paper tapes and program listings would represent a significant dollar savings.

Near Future

Eliminate shipping the basic paper tape diagnostics for ALL PDP-11s. When agreement and implementation is accomplished on the first recommendation, I will push for this. Eliminate sending the extra software to OEM's by working out a better method of control. Eliminate sending out some systems diagnostics (CTP & GTP) when only the basic CPU is ordered. Eliminate sending paper tape when there is another medium available, such as cassettes or mag tape.

Longer Term

On hardware and software manuals, develop an overall, sensible approach on what different types of manuals there should be, what contents or subject matter in each one, and what level of reader it is to be used by. Set standards for contents, style, etc. Eliminate duplication of material when several manuals are always sent out together. The writing groups are encouraged to talk to Central 11 Marketing in the early stages of the writing, so we can help in establishing goals.

On customer print sets, investigate eliminating drawings such as ROM listings, wire lists, mechanical drawings, and Teletype modification prints.

DISTRIBUTION

R. Anundson
R. Armstrong
R. Baillie
S. Beiferman
C. Brooks
R. Cady
R. Clark
B. Delagi
D. Finn
J. Hittell
M. Horovitz
T. Karpowski
A. Knowles
J. Meany
M. Moffa
T. Mullane
K. Olsen
I. Paton
C. Spector
P. Tays
S. Teicher
D. Zereski

digital INTEROFFICE MEMORANDUM

TO: Dave Knoll

DATE: March 3, 1972

FROM: Bob Antonuccio

DEPT: Manufacturing

SUBJ: PDP11 SHIPMENTS

All PDP11 shipments (1120 & 1115) through March 1, 1972 are listed below:

FY'70	Q4	90
FY'71	Q1	200
	Q2	190
	Q3	220
	Q4	260
		870
FY'72	Q1	300
	Q2	410
(2 mos)	Q3	300
		1010
TOTAL		1970

Of these, 193 units are consigned to in-house users:

Production Test	67
Other In-House	58
Regional Offices	33
Capital Equipment	21
Prog. & Training	14
	193

pjs

Copy A. Knowles
K. Olsen ✓
P. Kaufmann

digital INTEROFFICE MEMORANDUM

TO: Product Line Managers
CC: Andy Knowles
Stan Olsen
Jack Shields
Bob Puffer

DATE: December 11, 1972

FROM: Julius Marcus

DEPT: DECcomm

SUBJ: Cassette-Based Diagnostics

For your information and planning, the DECcomm Product Line has funded the placing of sequential diagnostics on cassettes for cassette distribution on PDP-11's. The cassette system is the TA11/TU60 unit.

If you have any inputs on what you would like to see in this area, please make your suggestions to John Hittell.

I feel this is a necessary item in order to make the cassette system successful and useful in the market, so we are moving ahead.

mr

pdp11 memo

SUBJECT: ELI GLAZER/TADIRAN/MILITARIZED PDP-11

TO: Ted Johnson
cc: Jean Claude Peterschmitt
Ken Olsen

DATE: February 18, 1972

FROM: Andy Knowles

We do not have or will not have the engineering and marketing manpower to pursue Eli's proposal further, hence I am recommending that we turn Eli/Dr. Harrel off. Having had direct engineering and marketing experience with full blown mil spec machines/contracts/licenses, please go on faith or something when I close with the note that Eli is naive in that he doesn't really know what he would be getting us into.

s

INTEROFFICE MEMORANDUM

TO: Andy Knowles

DATE: February 8, 1972

cc: Jean-Claude Peterschmitt

FROM: Ted Johnson

DEPT: Sales, 5-3

SUBJ: ELI GLAZER/TADIRAN/MILITARIZED PDP-11

Eli has told Dr. Harel that I would be willing to talk with him about the above idea. Basically he is saying they would militarize the 11 for half of what we could ($300,000 DEC, $150,000 Tadiran) creating a new product opportunity.

Assuming they could do it, we would consider:

1. Market potential
2. The risk of licensing our design
3. The market risk (Arab countries) of a tie-up with an Israeli company

in addition to the ease and risk of working with them.

Have we considered doing this ourselves in the future? Should we contract someone to do this on some ! sis - either here or there?

JCP should comment on 3. You and I should decide (and Ken, if necessary) on whether to pursue this and whether we should turn this fellow off.

MEMORANDUM

22nd December , 1971.
EG/JB

TO : TED JOHNSON , VICE PRESIDENT SALES, MAYNARD

FM : ELI GLAZER, TEL AVIV

RE: MILITARISED VERSION OF PDP11

I am enclosing letters that I sent to Andy Knowles with reference to the above. The advantages to the Digital Equipment Corporation in having someone produce a full military specification version of the PDP11 are the following:-

There will be consideration of the use of the PDP11 in air traffic control and other semi military and military applications in which we do not presently compete. That market is currently in the hands of Univac 1218, Rohlm-Nova and possibly Varian. The MilSpec range would be the ground and ground mobile as opposed to airborne. Further, there would be a market for non Mil Spec supporting systems wherever this became a requirement.

The examples of applications which come to mind which come from my experience on Long Island, include the following:

Military communications' networks.

Air traffic control.

Ground support equipment for computerised maintenance of avionics equipment for the military.

Ultra severe commercial environment such as remote traffic control or utility control stations.

The cost of developing such a system in the States would probably be of the order of $300,000. The cost here in Israel is approximately half of that and is one reason why this may be a good place for that kind of work to be done. Tadiran has specific experience in this field and is well suited for the job at hand. In any case, since they are a potential O.E.M. customer here in Israel, I would suggest that you meet with Dr. Harrel to discuss the matter when he visits the States in the near future.

Since the question of licencing would be new to us and since we are really unaware of the market value of this proposal, we can certainly use that (as you have indicated) as ample reason for being cautious in the matter.

I am enclosing my letter to Dr. Harrel discussing the matter.

SUMMARY

Outline of Proposal

1. License to manufacture only a full mil. spec. PDP-11 processor, memory and basic processor options.

2. Talaran would be proposed licensee - others could be explored.

3. Marketing in U.S. could be done by GT & E military sales division

- or -

4. DEC could act as an outlet.

5. Sales of Computer software and services would be handled by DEC.

6. DEC would be sole source for non militarized prototype and Rugged versions of the PDP-11 and its options.

7. DEC guarantee of purchase of a run of successful production units would be its "investment".

8. Know-how - software for production - test equipments - royalty fees would all be negotiated.

9. Time from start of project to first production prototype about 24 months.

Questions to be answered

1. Are we interested ?

- if so -

2. What is our estimate of the market. (Certainly the Long Island military industry had requirements - the recent FAA - 1000 processor for air traffic desplays - would have been a potential).

3. What number of units could we guarantee.

K. Olsen

digital INTEROFFICE MEMORANDUM

TO: Ken Olsen
Phil Laut
John Fisher

DATE: August 9, 1973

FROM: Gordon Bell GB

DEPT: Engineering

EXT : 2236

SUBJ:

I'm absolutely adamant about our need to immediately completely isolate the small and large PDP-11/s clearly because

1. Historically this has been a good decision (eg. PDP-6).

2. Historically our mid-range machine has not been as profitable as small machine (minimals) - summary data for PDP-1,7,9,15 available indicates only 22% net contribution over the last 10 years.

3. Our support now is weighted in favor of 11/45, being subsidized by 11/05. (Virtually all software.)

4. The 11/45 will be hit in 6 months by several 32-bit machines, which may cause us to take resources from small. Certainly there will have to be regrouping and another machine started. (The lifetime of this machine may be about 3 years - whereas a small 11 is probably only good for 2-2½ years.

5. The sales/support effort will also be higher due to increased complexity with software and size.

6. This last year should have been the most profitable for 11/45. It was not clear that it was up to corporate average. Although next year may be more profitable, demands will occur to increase spending.

8/13 gordon sent to Olsen plus

fr. Oct. Woods

Problem

INTEROFFICE MEMORANDUM

SUBJECT MURDER OF THE PDP-11 AS LAB-COMPUTER

DATE September 11,1975

fete - 2-4

OCT 3 1975

TO Willy Kister, Geneva EHQ FROM Jean-Paul Müller, Zürich

cc: Roni Stebler, Zürich
Jean Friederich, Zürich

Jean-Paul

G.B. discuss with regular op Comittee or MDRA Comm.

15 SEP 1975

SEP 26 1975

Please find the delinquent paper attached.

This must be circulating among users and competitors.

Most of the killing statements are true, although some of them distorted realities.

I have marked key statements for easier reading.

I feel very strongly that we must react violently to such pamphlets:

1) By correcting mistakes which have been broadcasted for good reasons and by letting the world know it.

2) By contacting the author, because obviously he is a frustrated PDP-11 customer.

The only people able to do this, in my opinion, are in the product-line.

The lesson for sales out of this is that we must:

a) better inform our customer about the use of our products and our service- and sales policies

b) do better customer hand holding

Please discuss this with Ed. Kramer.

Regards Assume this is true;

Can we discuss some of why / who in the Woods of October.

Are there going to be enough Market people there to enough to discuss anything (eg. AK + WH)?

Ken Olsen

digital

OCT 30 1975

INTEROFFICE MEMORANDUM

TO: See Distribution

DATE: 22 OCT 75
FROM: Lloyd Dickman
DEPT: R & D Group
EXT: 6159
LOC/MAIL STOP: ML3-4/E41

file 2-4

SUBJ: EXTENDING THE PDP-11 INSTRUCTION SET

These are strong statements about the future of the PDP-11

This memorandum outlines a methodology for new instructions on the PDP-11. The design and implementation of these instructions will require your input and active participation. In order to enable me to serve as an effective advisor to these efforts, I shall welcome your reactions and specific comments on this document.

Some work has already been done. I have completed a first pass of a commercial string and decimal instruction set. A limited amount of time has been spent looking at bit data types and boolean operations for industrial and telephone use.

Reasons for extending the -11 instruction set:

1) There is a great deal of growth potential left in the -11. Until the first VAX-11 implementation arrives, we must still actively enhance the -11 line.

2) Product lines would benefit from instruction set enhancements by improvement of performance and throughout for specific requirements.

3) An early introduction of new data types and instructions will ease the transition to VAX-11. The concepts will be familiar to users, and we will have gained some experience in their application.

MIL-11

KEN O.

FYI

This is a good description of the current ROCM discussion. This will progress further when Tom Siekmann, John Buckley, & I visit them later this week. It would seem they really want to do a militarized PPP-11. This whole area (Rolm, Raytheon, Bunker Ramo etc) will call for a formal decision in a few weeks. We will be preparing a formal recommendation.

Dick C.

ROLM CORPORATION ■ 18922 FORGE DRIVE, CUPERTINO, CALIF. 95014 (408) 257-6440 TWX: 910-338-0247

2/18

Company CONFIDENTIAL
cc Tom Siekman
Your comments please.

John Buckley
Julius Marmie
Bob Huberfeld.

September 12, 1975

Mr. Richard J. Clayton
Vice President, Computer Systems Development
Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Dear Dick:

I want to express our appreciation for your hospitality during our visit and especially for the openness and frankness with which you approached what must be for both companies, a complex negotiation.

I believe we made significant progress toward our mutual objectives on several key issues. I believe it would be useful to record the views of our mutual objectives, the positions we have reached, and the actions which lie ahead. I believe the attachment to this letter summarizes our current positions, and would appreciate any comments on this summary.

On ROLM's behalf, we continue to be very enthusiastic about the prospects for a family of ROLM produced Mil Spec PDP-11 products. We are especially encouraged by your proposal for close and cooperative relationships. We are very pleased to learn that you would like the first product to be essentially a cost performance enhancement to the PDP-11/45 and that you would work with us on the development of this product prior to its introduction and announcement.

We are comfortable with the concept of "symmetrical exclusivity" and your understanding of our business needs to continue support of our customers committed to our 16XX family by analogy to your PDP-8 family.

We have arranged with John Buckley for your visit to our Cupertino plant on Tuesday, September 23. At that time, you will be able to meet with Ken Oshman and other key members of the ROLM management team. We plan to have a specific proposal to review with you at that time including:

- a counter-proposal on royalty, exclusivity and sublicensing;

- a quantitative estimate of our needs for technical assistance from DEC on the initial product. (Our current thinking, assuming access to all available documentation, is that we will need 10-20 man days of consultation.)

- details on ROLM's management commitment (via R&D plan) to establish the PDP-11 as our major new thrust in Mil Spec computers.

It would be helpful for us to review more details of your view of the available market for Mil Spec PDP-11 over the next two to three years. It would also be helpful to have details on the patent package you propose licensing.

It is our understanding that we both desire to proceed expeditiously and that it is feasible to reach an agreement and get full DEC management approval by the end of October. We are proceeding and committing resources on that basis.

Again, thank you very much for the hospitable reception you extended us last week. I look forward to seeing you again in the near future.

Very truly yours,

Eugene W. Richeson

Eugene W. Richeson

EWR/ks

Attachments
1 - Summary of ROLM's Objectives and Position
2 - Summary of DEC's Objectives and Position

cc: (w/attachments)
Andrew C. Knowles
Julius L. Marcus
M. Kenneth Oshman

Summary of ROLM's Objectives and Position

1. ROLM seeks an exclusive world-wide license to manufacture and sell severe environment Mil Spec versions of DEC's PDP-11 family of computers. Such Mil Spec products would be software and I/O compatible with DEC commercial counterparts. All software which DEC offers for commerical versions would be available from ROLM to Mil Spec customers on a licensed basis for use on Mil Spec machines purchased from ROLM. Software from ROLM would be available at prices equal to or greater than software from DEC.

2. ROLM proposes to pay a royalty of 3% of the net sales price of all products sold which resulted from a DEC design or resulted in licensed use of DEC software.

3. ROLM would vigorously pursue the development and marketing of a family of Mil Spec PDP-11 computers over an initial 18-month period by investing a minimum of $600,000.00 of our own funds to develop such product(s). Thereafter, ROLM would continue to invest R&D funds to the extent of 10% of sales of Mil Spec PDP-11 related products.

4. ROLM anticipates royalty based sales of at least $2.5M in 1976, $7.5M in 1977, and a minimum of $10M annually thereafter.

5. ROLM would like the license valid for five years with our option to renew for five years. It should cover spare parts as well as all specific products (hardware and software) in the PDP-11 family. ROLM also seeks the rights to sublicense, subject to DEC's concurrence.

6. ROLM would continue to support customers committed to the 16XX family of computers. This would include completion of R&D projects now under way and possible future projects which might be required to extend cost/performance benefits resulting from technology advancements. The 16XX line would not converge in compatibility with any other commercial computer line.

7. ROLM is willing to restrict "field of use" to Mil Spec type of equipment which are likely to be priced at approximately twice the price of DEC's commercial products, but ROLM seeks freedom to sell these Mil Spec type products to industrial and commercial markets for severe environment products world-wide wherever the opportunity for sales exists.

Summary of DEC's Objectives and Position

1. DEC wants to introduce a Mil Spec PDP-11/XX as soon as possible. (XX is an unannounced product designed to supersede the 11/45 with cache memory, memory management, floating point hardware, unibus and probably some communications related I/O). The product would have essentially equivalent performance with the 11/45 but with about half the IC complexity and a lower price than the 11/45.

2. DEC seeks a licensee who is not producing commercial computers and who would not compete with DEC in DEC's product line.

3. DEC seeks a licensee who will sell Mil Spec products to DEC on an OEM basis where DEC sells a "package deal" or where Mil Spec PDP-11's would be integrated with other DEC products.

4. DEC wants the PDP-11 trademark identified with the product (e.g., "ROLM PDP-11/45M" for Mil Spec).

5. If ROLM is the licensee, DEC would like to discourage future involvement with DEC's major competitors through a license agreement incorporating "symmetrical exclusivity." During the period of exclusivity, ROLM desires DEC not to license other companies to manufacture and sell Mil Spec versions of the PDP-11 family nor to manufacture Mil Spec versions itself; DEC desires ROLM not to seek license to manufacture and sell Mil Spec versions of other commercial computers which compete with DEC.

6. DEC has substantial patent protection on the PDP-11 family and would sue to prevent unlicensed use of this technology. DEC would like to define a "field of use" for the patents (such as Mil Spec) to describe our license. DEC believes that once they license us they can be forced by antitrust law to license anyone else to the patents although at much higher rates.

7. DEC is seeking a closely cooperative long term relationship including cooperation in development of unannounced products, marketing and possibly including field service.

8. DEC wants no product divergence, insuring full compatibility with their line. All features and options would, to the extent practical, employ the same technique.

9. DEC wants the Mil Spec PDP-11/XX designed to meet Mil E-5400, Mil E-16400 as a minimum and to offer full Mil-Q-9858 at least as an option.

10. DEC believes the market for a Mil Spec PDP-11/XX to be $30-$40M on an annual basis within two years.

11. DEC seeks no prepayment or front-end money for this license. DEC prefers all investment made in the eventual success of the product. DEC has no interest in equity ownership of ROLM.

Summary of DEC's Objectives and Position

12. Following the initial product introduction, successive products in the Mil Spec PDP-11 Family might likely be a Mil Spec LSI-11/X and a PDP-11/70M. The intention of the relationship is for a continuous and ongoing Mil Spec product line serving the needs of the marketplace with available technology.

13. DEC takes issue with ASPR 7-109.4 relative to software and does not plan to comply. Unless this is resolved, this policy would also extend to ROLM as a licensee.

14. DEC understands ROLM's need for continued support of customers committed to ROLM's 16XX product line to be similar to DEC's need for continued support of the PDP-8 product line. This might include technology related enhancements to cost/performance. The intent of "symmetrical exclusivity" would be satisfied as long as the compatibility of the 16XX line does not converge with new commercial computers.

15. DEC's assessment of ROLM's intent to make the Mil Spec PDP-11 ROLM's dominant new Mil Spec product family will come primarily from understanding ROLM's planned computer R&D resources allocation over the next two years.

16. DEC is simultaneously considering other companies as potential licensees, and expects to present at least two proposals together with a recommendation to DEC's management for action in October.

17. DEC proposes that any technical assistance beyond the initial agreement be paid for at the prevailing rate.

18. DEC proposes that royalty be 12% on CPU and I/O and 6% on memories. DEC proposes that software should be offered by ROLM as a standard OEM customer of DEC.

INTEROFFICE MEMORANDUM

NOV 12 1974

TO: Dick Clayton 5-2
Bill Long PK3-1
Julius Marcus PK3-1

cc: John Fisher 12-1
Roger Handy PK3-2

DATE: November 8, 1974

FROM: Bob Huberfeld RH

DEPT: Federal Government Marketing

EXT: 221 LOC: Washington, D. C.

SUBJ: Meeting to Discuss Mil Spec Mini-Computers

Ken Olsen
Gordon Bell
any specific
viewpoints!

It appears that the time is ripe for DEC to discuss and decide on a course of action and timetable for the development of a Mil Spec PDP-11 processor.

Dick C.

We have been able to pin down the market, for this type of 16-bit machine, to be in the range of 3000-4000 systems per year.

Univac sells 1000 AN-YUK 20's to Navy alone every year (probably 1500-2000/year in total).

CDC reportedly sells 1000 Mil Spec 16-bit CPU's per year.

Rolm shipped approximately 300 Mil Spec NOVAS last year.

Varian has announced a Mil Spec machine.

Interdata will have a Mil Spec machine developed by Hughes.

We have been approached by Sylvania, General Dynamics, Base 10 and other firms to either license them or put them on contract to develop such a system. These systems house OEM's of ours, very clearly see the need and the market.

NSA, Rome Air Development Center, FAA and other end user government agencies have requested us to enter this market. Many projects that are being prototyped now on PDP-11's will need Mil Spec systems for field implementation in the future.

For the continuance and extension of our presently strong position in this Military/Security Market, we need this product, and need it as soon as possible. We also have defined many commercial users for this product.

I've scheduled a meeting to discuss this subject on Wednesday, November 20, from 3:00 to 5:00 p.m. in the Customer Conference Room A, PK3-2, (Pole 6-D). If you have any questions before that time, please call me at X221 or X222 in Washington, D. C. See you on the 20th.

Regards,

→ Dick Clayton
can we do IT ourselves?
Ken

/gmc
Attachments

digital

INTEROFFICE MEMORANDUM

LOC/MAIL STOP

TO: Marketing Committee
OOD
cc: List

DATE: July 9, 1975
FROM: R. Clayton/T. Coleman TC
DEPT: Computer Systems Development
EXT:
LOC/MAIL STOP: ML5/E71

SUBJ: PDP-11 Reliability & Quality Control Brochure/Dissemination of MTBF Data

Attachment: Table of Contents for subject brochure

Recommendations

1. Complete the engineering verification of the calculated MTBF numbers and distribute these to Product Line management for their discretionary use.

2. Turn the brochure draft over to PPG for final editing, artwork and layout with a targeted availability date of late August. (Note: Engineering, Manufacturing and Product Lines are currently reviewing this draft - See attached Distribution list)

What We Want From You

Concurrence or documented disagreement with the above recommendations no later than 7/25. The proposed brochure is somewhat controversial since it focuses attention on the sensitive issue of reliability. Preliminary discussion with various Marketing managers and salesmen resulted in our conclusion that this type of document is needed and will serve a real need in the field.

Drafts of this brochure have been distributed throughout the Marketing, Engineering, Field Service and the Manufacturing organization. (See attached distribution list) Additional copies of the brochure draft are available upon request. We expect to receive any required technical corrections via this review. We do solicit your constructive criticism for improving this document. For example: We're uncomfortable with the use of the RAS acronym - it's too IBMish. Do you have a better idea?

Please insure that any corrections or constructive inputs are received by July 25.

Background

Central Engineering has been on the receiving end of an increasing number of inquiries and demands from the Product Lines, sales force and customer base relative to:

(a) the need for MTBF data on our products, particularly for those sophisticated sales situations where lack of MTBF numbers results in a disqualification of the bid.

(b) lack of knowledge and understanding concerning all the good things DIGITAL is doing as a corporation to insure that we deliver nothing but quality products.

Central Engineering has initiated 2 separate projects, both of which are nearing completion, to assist the field sales force in responding to these situations.

MTBF DATA

We have developed a semi-automated system for calculating MTBF in accordance with Mil Handbook 217B. Preliminary failure rates have been calculated for most of the PDP-11 processors, memories, peripherals, controllers and interfaces and are currently being reviewed by the project engineers responsible for these products. It is our expectation that these numbers will be available in final form within 30 days.

Reliability and Quality Control Brochure

We have drafted a brochure which focuses on some of the more interesting and significant procedures and organization which have been implemented to control quality.

This brochure can best be categorized as general interest in nature and will be high in picture content. It has 3 primary objectives:

(1) Convincing customers and prospects that DIGITAL really does care about quality and that DIGITAL is making substantial committments in terms of people, facilities and dollars to deliver nothing but quality products.

The implied question: Can competitive minicomputer manufacturers without DIGITAL's financial resources make these same claims?

(2) Selling the sales force on the idea that the corporation really does care about quality and that they have no reason to take a defensive posture.

(3) An internal "turn-on" for manufacturing and engineering personnel, driving home the need for continued efforts in the areas of quality control and reliability.

MTBF REPORT

The companion document to the Reliability and Quality Control Brochure deals with MTBF data. It will be distrubuted for review within 30 days. This document, proposed for restricted distribution at the Product Line management level, will consist of 4 sections:

(1) An introduction to MTBF including some of the background and history leading up to the acceptance of Mil Handbook 217B as the reliability standard. It will also include a summary of the differences between 217A and its successor, 217B.

(2) A description of the approach DIGITAL has used in calculating MTBF's in accordance with 217B.

(3) A detailed look at the supporting detail for just one DIGITAL product - the PDP-11/04.

(4) A tabular listing of calculated MTBF's for most of the products listed below. We have already computed failure rates on the electronics portion of all of these equipments and have asked the responsible engineering organizations to scrutinize the results prior to releasing the MTBF data to the Product Lines for selective dissemination to customers and prospects. It is our expectation that we will provide actual MTBF's as measured in the factory for some of the peripherals and terminals having a high mechanical content.

11/05-KA
11/35-SC
11/45-CA
11/50-FS
TC11
TA11
KE11-B,E,F

MM11S,MF11S
MM11K,MM11L,MF11L
MF11-LP,MML-LP
MS11-BC,BD,BR,BT
MS11-CC,CM,CP

RP04-AA
RS03-AA
RS04-AA
TM02-CA,FA
TU10-EA
RK05-AA
TU56
RP03

DH11,-AA,AB,AC,AD,AE
DJ11,-AA,AB,AC
DL11,-B,C,D,E
DM11-DA,DB,DC
DN11-AA,BA,DA

GT40-AA
GT42-AA
GT44-AA
VT11-AA
LPS11-SA,E
LPSAD-12,NP

BM873-YA,YB
KT11-C,D
H960-CA,DA,DH,EA,EH
RP11-CA
RS11
11/04-AA
11/70-CA

MF11-U,UB,UC,UP,UR,US
MM11-U,UP
MJ11-AA,AB,AC,AD,AM,AY,AZ
MS11-E,J

RX11-AA
LA30-CA
LA36-CA
VT50-AA
CR11
CD11A
CM11FA
PC11

DP11,-DA
DQ11,-AA,AB,BB,DA,EA
DR11-B,C,K
DV11-DA
DV11-AA,BA

LPSAM-E,SG
BA408
LPSVC
LPSDA
LPSDR-A

M9301-YA,YC
KW11-L
RH70
RH11
RK11-D
DL11-A
FP11-B

LP11,-VA,WA,SA
LS11-A
LV11-BA
RF11
RX01
LT33-DC
LT35-DC
VR14-LC

Table of Contents

Section One — Tangible benefits of RAS at the system Level. The PDP-11/70 system is used as an example and typifies DEC's committment to maximize system availability through synergistic advances in:

- software design
- hardware design
- diagnostic design

Section Two — Introducing a New High Volume Product to Manufacturing

New DEC high volume products must successfully pass multiple screening tests before they are ever committed to volume manufacturing in order to ensure that the product meets or exceeds its RAS expectations. Overviews of:

- conceptual design process
- breadboard/prototype evaluations
- Systems Integration Testing
- Design Maturity Testing
- Process Maturity Testing
- Process Control

Section Three — Quality Control

In order to ensure that only the most reliable components go into its products and to ensure that quality is maintained at all levels of the manufacturing and assembly processes, DEC has implemented comprehensive quality control measures as typified by:

- Centralized Components Engineering
- Incoming Component Screening
- Multilayer Board Testing
- Logic Module Testing

Section Four Assembly, System Testing and Installation

Before being released for shipment, all DIGITAL products undergo rigorous acceptance tests in the manufacturing plant that built them. In addition, DIGITAL also assembles the complete system to be shipped to the customer and tests it interactively with representative software as a final acceptance test prior to customer delivery:

- Volume Manufacturing Acceptance Tests
- Final Assembly and Test
- Field Installation Acceptance Tests
- Installation Feedback System

LIST (Received copies of brochure draft)

OEM	J. Meaney		
	A. Campbell		
	B. Long		
LDP	D. Frost		
	J. Schwartz		
	E. Kramer		
IPG	J. Davis		
	M. Marshall		
	B. Vachon		
EPG/ECP	C. Spector		
	G. Whitmore		
	D. Fernald		
DECCOMM/TELCO	R. Cady		
	M. Mensh		
	J. Marcus		
BUS	D. Riordan		
	T. Barnett		
	I. Jacobs		
Mfg.	D. Knoll	H. Lemaire	R. Amann
	J. Cudmore	J. Lebate	A. Hirsch (WM)
	J. Smith	J. Cranston	J. Hawkes (WM)
	B. Hanson	D. Dawes	R. Feener
Field Service	J. Shields		
	A. Zins		
	J. Barclay		
	J. Lacey		
H/W Eng.	J. Carnes	S. Orr	R. Puffer
	A. Ryder	G. Saviers	R. Morris
	W. Demmer	R. Payton	B. Croxon
	R. Platz	E. Corell	V. Bastiani
S/W Eng.	W. Munson	J. Levy	
	M. Woolsey	D. Pavloch	
	P. Christie	C. Neal	
Sales	G. Moore		
	C. Hubler (Waltham)		
	J. Hannahs (Houston)		

Section Four ASSEMBLY, TESTING AND INSTALLATION

In the previous sections, we have detailed some of the cautionary screens DIGITAL employs to insure that products committed to volume production are in fact inherently reliable as well as some of the steps taken to control the quality of components, sub-assemblies and logic modules that go into these products.

In this final section, we will look at some of the acceptance tests DIGITAL employs to insure that the system delivered to your site meets your expectations.

PDP-11/70 ACCEPTANCE TESTING

Basic Assembly

Photograph

- Basic Assembly & Test Area for PDP-11/70 in WM.
- A. Hirsch to supply

Manufacturing personnel marry pre-tested sub-assemblies (power supplies, memory, fans, logic modules etc.) in the processo cabinet. Multiple passes of a Quick Verify diagnostic are executed to insure that the system is operational. The system is quality checked to insure correct revision status, that all connection are tight and that at a gross level the system is operational.

Vibration and Timing Tests

Photograph

- Nylon rod being run across board handles.
- 11/70 Test Area WM

While the 11/70 is running the Quick Verify diagnostic, an 8" nylon rod is passed horizontally across the module handles four times in each direction, while a technician monitors the system for adverse reaction. This test is a valuable tool in detecting cold solder joints or loose wires. All timings are clock adjusted and another pass of Quick Verify is executed.

UNIBUS Testing

Photograph

- 11/70 in environmental test chamber for UNIBUS testing.

The system is then placed in an environmental chamber and the UNIBUS is exercised for one hour with diagnostic software while the temperature is held at 120°F.

Burn-In Testing

The system is then exercised continuously with diagnostic software and a special CPU exerciser for an extended period of time while the temperature is cycled between 50°and 120°F.

Heat is perhaps the biggest culprit in prematurely aging electronics and causing failure. The thermal stresses encountered in this test, while non-destructive, do an excellent job of weeding out "weak-sisters" that might cause premature system problems.

The duration of this burn-in test is legislated by the QC organization and is adjusted as necessary to eliminate infancy problems. As of this writing, 11/70's were undergoing 13½ hours of heat cycling or acceptance burn-in.

- 2.5 hours at 120°F
- 2.0 hours at 50°F
- 2.5 hours at 120°F
- 2.0 hours at 50°F
- 2.5 hours at 120°F

Modules failing during heat cycling are swapped out for spares that were previously heat tested. Machines failing during the first 2 cycles (4.5 hours) are restarted in heat as a new machine. Those failing in the last 3 cycles (9 hours) undergo a module swap and are then restarted until they run the last 9 hours error free.

Each and every DIGITAL major unit (processor, tape drive, disk drive, terminal) undergoes burn-in as part of its acceptance. It's almost a certainty that DIGITAL products will deliver the performance you expect because that performance is demonstrated before the product even leaves the factory and the product's infant mortality runs its course before the product is shipped.

Photograph
- Large No. of LA-36's undergoing burn-in.
- Westfield

Photograph
- Large No. of RP04's undergoing burn-in.
- Westfield

Photograph
- Large No. of TU16's undergoing burn-in.
- Westfield

Final Assembly & Test (FA & T)

After having successfully passed its acceptance test in volume manufacturing, completed major units (CPU's, memories, peripherals, controllers, etc.) are sent to finished goods inventory at one of DIGITAL's Final Assembly & Test (FA & T) plants. FA & T assembles the actual configuration to be delivered to the customer's site and tests the system interactively in a simulated user environment under realistic software to be doubly sure that the system will meet the customer's expectations.

DIGITAL has recently implemented a major program called MAST (Modularized Acceptance and System Test) to insure uniform, quality testing for all PDP-11 systems. MAST consists of 3 phases: System Checkout, System Acceptance, and Field Installation. These 3 phases are closely related with sub-set, super-set relationships so that in the event that a problem is discovered during field installation it can be related to a specific failing in manufacturing and specific corrective actions can be implemented. DIGITAL feels that MAST minimizes the possibility of undetected system problems reaching the customer's site.

System Checkout

Photograph

System Checkout Area for 11/70's in Westminster.

FA & T assembles the system in the customer specified cabinetry, marries devices with their controllers and integrates all ordered system options. Quality checks are made to insure the equipment is at the latest revision level, all required cables are in place, all connections and wiring are snug, documentation is complete etc.

Diagnostic software packages identical to those used by Field Engineering are used to serially and interactively checkout each of the newly integrated syb-systems.

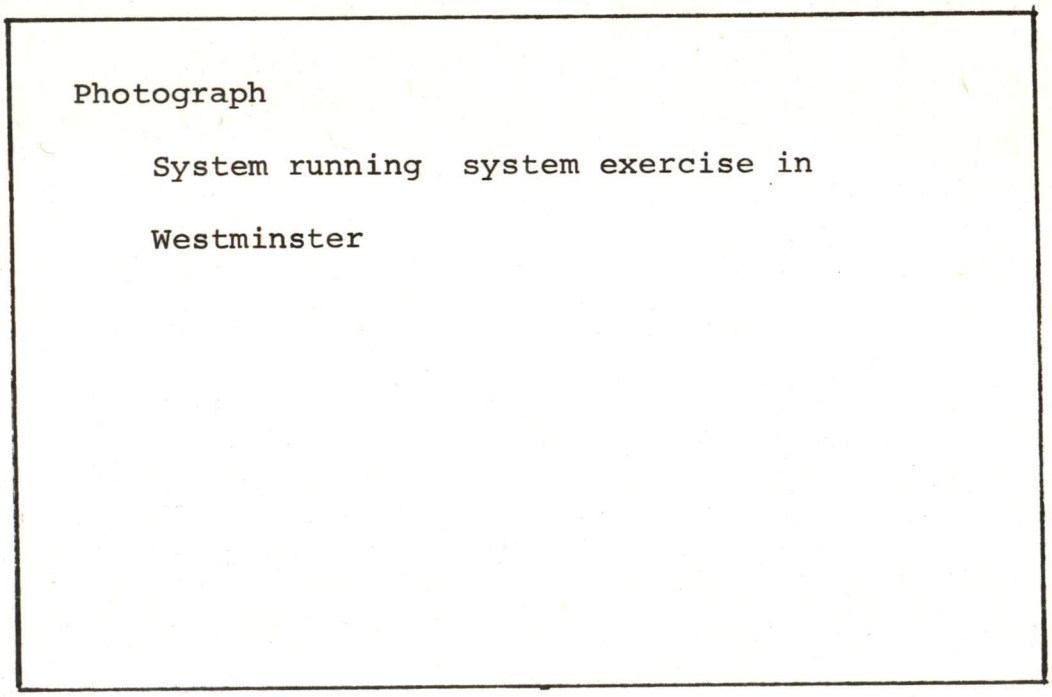
Photograph

11/70 system in environmental test chamber for heat cycling test as a system

The newly integrated system is then placed in an environmental test chamber where the temperature is cycled for 24 hours while the system is being exercised interactively with diagnostic software (DEC/X-11). Temperature extremes are naturally constrained by the temperature limits of the least tolerant system element. The system then undergoes a second series of quality and paperwork checks.

System Acceptance

The System Acceptance phase is a formal quality check on the entire system designed to simulate customer usage. A system exerciser based on the RSTS/E operating system allows the system to be exercised with a workload typical to that which the customer will expect the system to process: matrix inversions, fast Fourrier transforms, disk sorts, compiles etc. Additional system exercisers based on the RSX-11 real time operating systems are currently under development.

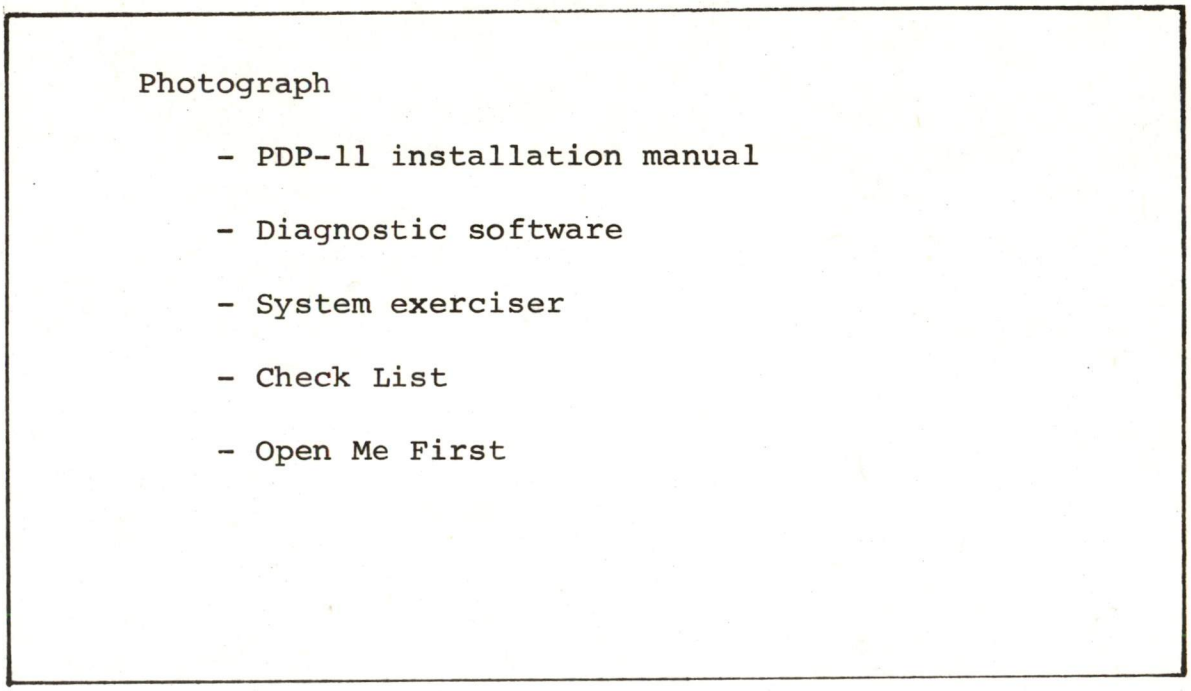


In addition to the system exerciser test, the configuration is also subjected to multiple passes of sub-system diagnostics to verify sub-system reliability and DEC/X-11 to verify that the system operates correctly in an interactive environment.

The system then undergoes a final series of quality and paperwork checks, undergoes cosmetic touchup and is then carefully packaged for shipping.

Field Installation

Installation procedures shipped with the system detail the steps to be followed in physically assembling the system, integrating the various system elements and for running Acceptance tests. Field Engineering also performs a final quality check and audit to insure that all hardware is at the correct revision level, that all connections and wiring are snug, that no shipping damage occurred and that all applicable hardware, software, and documentaion is present and accounted for.



Field Engineering subjects the system to extensive Acceptance tests on the customer's site using the same diagnostics and the system exerciser that were previously run in the factory. These tests:

- reduce installation and customer acceptance time
- relate system testing to system usage by providing a test base for the total system (hardware and software)

- provide a compatible bridge and feedback loop between factory testing, field installation and customer utilization.

Information Feedback Loop

Installation of new DIGITAL computer systems are currently running at a rate in excess of 1000 per month. For every system installation, Field Engineering compiles a report detailing all problems encountered, corrective action taken and identifies the specific system number and serial number of the troubled unit.

These reports are forwarded to DIGITAL's Maynard headquarters where they receive high visibility. Manufacturing is usually able to correlate the problem to a breakdown in a specific process and even to the responsible individual allowing the corporation to take immediate, specific corrective action.

Because of all the testing and qualification that DIGITAL products are subjected to prior to leaving the factory, problems detected during installation are fast becoming a rarity. The probability has been greatly increased that your system installation will be a smooth problem free one, that your system will be immediately productive and that the chance of problems immediately following installation has been greatly reduced.

Let's take a look at some of the steps involved in building a complex, high density, multilayer board and some of the tests which screen the output of the board production facilities.

Note to reviewers:

Suggest that the photo essay which follows of how a PC board is manufactured and components attached be told in tutorial form in a 2 page spread as illustrated below. Each of the 4 corners have a larger photo with captions on these tests:

- Coupon Analysis
- Bed of Nails Board Testor
- Visual Inspection following Component Insertion
- XOR/GR1792 Board Testors

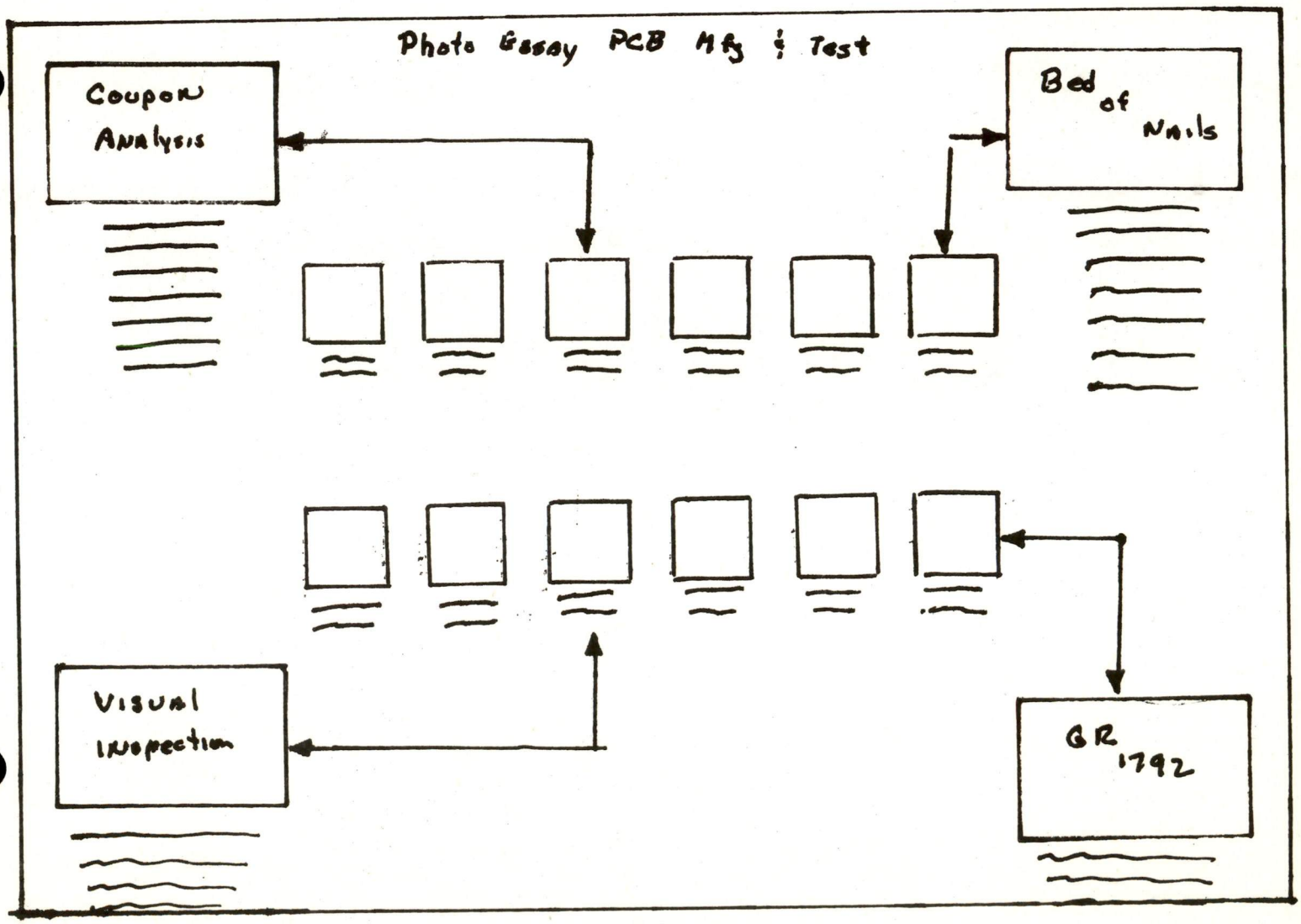


Photo Essay on Manufacturing a Typical Multi Layer PC Board

Acceptance Testing

Incoming stock tests:

- Epoxy to glass ratios
- Lamination bonding
- Copper conditions
- Physical dimensions

Image Transfer

Photographic negative of PC artwork for the desired circuit created on glass and transferred to copper surface using a dry film photographic technique.

Chemical Etching

Selective etching away of the copper surfaces to form "clearance pads" in the case of the inner power/ground planes and leaving only the desired circuit in the case of the ~~extreme~~ exterior copper planes.

Lamination Press

The various layers are laminated together under high pressure (200psi) and at high temperature ($350^{o}F$) for maximum bonding.

Numerically Controlled Drilling

Numerically controlled equipment drills holes for component insertion.

Deposition Plating

A thin coating of copper is deposited on the printed circuit lines and on the sides of the newly drilled holes (PTH - plated through holes).

Photo Essay on Manufacturing a Typical Multi Layer PC Board

Coupon Clipping

"Coupons" or cross-sections of PTH's are taken on a sample basis and microscopically examined to insure unformity and quality of copper coating.

Gold Plating

"Fingers" or electrical contact points of boards are coated with 24K gold for best possible electrical contact. (Hex board uses $3.37 gold at 1975 prices).

Visual Inspection

100% of all boards inspected:

- Broken circuit lines
- Bridged lines
- Centering of pads on holes
- Uniform gold coating
- Hole plating
- Delamination
- Accurate Fabrication

Bed of Nails

100% of all boards are electrically tested using the DIGITAL developed "Bed of Nails" board tester to insure that there are zero bridged or broken circuit lines.

Photograph

- Blow up of board cross-section
- Labeled to identify faults with microscopic dimensions for appreciation of fine tolerance

Photographic montage showing:

- Bed of Nails Testor
- Terminal
- Block Interfaces close-up

Photographic montage showing:

- Print out from terminal with captions for rework

Coupon Analysis

Cross sections of Plated through Holes (PTH's) are taken from each lot of boards produced and examined under a microscope in laboratory conditions to measure the thickness and uniformity of the copper deposition plating. If the sample fails to meet specified standards, the entire lot is scrapped.

"Bed of Nails" Board Tester

DIGITAL had designed its own electrical board tester to insure that there are no "shorts"-where the copper was not completely etched away between circuit lines or "opens"-which are broken circuit lines in the PCB's produced by its board production facilities.

Unique interfaces for the different board types being tested contain thousands of electrical pin contact points (hence, the bed of nails nomemclature) that make electrical contact with the plated component holes.

This tester can completely check out the most complex multi layer board in less than 20 seconds including the load and unload time and isolates faults to specific locations for rework as necessary.

Photo Essay: Component Insertion and Testing of PC Boards

Automatic Sequencer

Pre-tested axial lead components are packaged on reels. The automatic sequencer can simultaneously handle 80 different reels and outputs a new reel of components properly orientated and sequenced for insertion into PCB's with numerically Controlled Insertion Equipment.

Automatic IC Insertion

Pre-tested IC's which are machine insertable are inserted into the PCB with numerically controlled insertion equipment.

Automatic Axial Lead Insertion

Sequenced axial lead components packaged on reels are inserted into the PCB with numerically controlled insertion equipment.

In Line Visual Inspection

After each of the automatic insertion steps, the PCB undergoes an in line visual inspection to ensure:

- correct component orientation
- Leads penetrate holes
- No crimping of leads

Hand Insertion

Components that are not compatible with automatic insertion equipment are then inserted by hand.

In Line Visual Inspection

QC check station verifies:

- Correct component orientation
- Leads penetrate holes
- No crimping of component leads

Photo Essay: Component Insertion and Testing of PC Boards

Wave Soldering

The PCB is then pre-heated to avoid "cold solder joints", treated with flux for maximum solderability, and then floated through a bath of molten solder (500°F) to maximize the electrical contact to component leads. (Solder bath chemically analyzed every 3 hours).

Quality Check

Quality control check station ensures:

- No open holes in component lead area
- Measures solder height for conformance to specification
- No bridging or breaks in circuit lines

Hand Insertion

Components that are not compatible with wave soldering process are hand inserted.

Electrical Functional Testing

Sophisticated programmable board testers, computer driven, exercise the board functionablity using a battery of diagnostics.

Photograph

Taken through the large test station magnifying glass showing a close-up the type fault (crimped lead) that the technician is looking for

Photograph

- XOR testor with PDP-1
- GR 1792 with PDP-8

Photograph

- Close up of tested board with arrows identifying faults

Visual In-Line Inspection

After each of the component insertion steps (manual and automatic) as well as after the wave soldering process step, a QC check station verifies the quality of the process just completed.

Digital is also actively involved in investigating the use of computer driven visual inspection techniques.

Electrical and Functional PCB Testing

DIGITAL is currently using sophisticated, computer driven, programable board testers of its own design such as the XOR and the new GR 1792 which is driven by a PDP-8.

These testers exercise approximatley 95% of board's functionality via a battery of diagnostic tests and are able to isolate any faults to specific locations for rework as necessary.

Parts Control

Controlling parts acquisition is an eqaully important aspect of overall quality control.

DIGITAL's Manufacturing Central Planning organization maintains a master file (DECPARTS) for all of the parts and components used in its products. This system involves three data bases:

1. A microfilm data base containing microfiche copy of purchase specs, purchased part listings by part number, and by functional and descriptive order, part rating listing and ECO revision status.
2. Qualified Vendor Data Base which includes: DEC Part Numbers, the approved vendors for each part and the vendors part number, incoming inspection procedure document number used to test parts at incoming inspection and detailed information in the parts rating.
3. EDP Master Parts File containing the DEC part number, the spec status, and the parts rating.

Photograph

- Page from Microfilm Data Base
- Labelled to identify and interpret information
- Vendors names to be deleted to avoid controversy
- R. Amann to supply

The net result of this system is that detailed parts information is available instantaneously to any DIGITAL designer, buyer, or incoming acceptance tester anywhere in the world.

- all new parts are supported by a purchase specification.
- engineering change orders to purchase specs update the system bi-weekly.
- qualified vendor information is used to update the system bi-weekly.
- incoming acceptance procedures are correlated to part numbers.
- objective parts rating information is available on all components.
- proliferation of parts and vendors is substantially reduced
- DIGITAL is able to maintain control over a very complex component acquisition system.

Use of DECPARTS by design engineer to select component for new design:

Photograph

- Page from qualified vendor Data Base
- Labelled to identify and interpret information
- Vendors names deleted to avoid controversy
- R. Amann to supply

A DIGITAL designer can interrogate the DECPARTS system to determine if the proposed part:

- is recommended for new designs
- is compatible with DEC manufacturing processes
- is testable and if incoming inspecting procedures and test equipment are available
- has passed standard DEC qualification tests or has had sufficient use to be considered qualified
- has released purchase specifications
- has multiple approved sources

PDP-11 RELIABILITY and QUALITY CONTROL BROCHURE

Final Draft

July 9, 1975

Tom Coleman
X2009
ML5-2/E71

INTRODUCTION

Your computer system represents a substantial financial investment and is critical to the success of your business because of the processes which that computer now controls or because of the automated applications which are now dependant on that computer. When that computer fails for whatever reason, it costs you money, it disrupts schedules and it causes endless aggravation.

Reliability, Availability and Serviceability (RAS) are the three watchwords which typify what you rightly expect from your computer system. You expect it to be reliable - it shouldn't fail very often; you expect it to be available to process your workload and not disabled for repairs; and you expect it to be serviceable so that down time to repairs is minimized. DIGITAL EQUIPMENT CORP. agrees with you and is making sincere efforts to meet your quality expectations.

The rapid technological advances in electronics make it relatively easy to build more cost effective computer products, DIGITAL's current PDP-11 offerings represent at least a five-fold improvement in terms of price and performance since the world's largest selling computer family was introduced five years ago.

Technological advances by definition also provide reliability improvements particularly at the component and subassembly level. Today's integrated circuits (IC's) and the use of large scale integration (LSI) not only provide far more performance than their transistor predecessors but they're also far more reliable reducing the chance of computer malfunctions because of component failure.

However, significant improvements in reliability, availability and serviceability at the system level cannot be brought about by technological advances alone. Nor can significant improvements be achieved overnight. In order to build quality system products requires a continuing corporate committment to RAS beginning with the conceptual design of a product and continuing through every stage of manufacturing and assembly. It also requires a substantial dollar investment in terms of people, test equipment and facilities. DIGITAL IS MAKING THAT COMMITMENT AND DIGITAL IS MAKING THAT INVESTMENT.

The pages that follow will touch briefly on some of the things DIGITAL is doing <u>today</u> to respond to your quality expectations.

Table of Contents

Section One — Tangible benefits of RAS at the system Level. The PDP-11/70 system is used as an example and typifies DEC's committment to maximize system availability through synergistic advances in:

- software design
- hardware design
- diagnostic design

Section Two — Introducing a New High Volume Product to Manufacturing

New DEC high volume products must successfully pass multiple screening tests before they are ever committed to volume manufacturing in order to ensure that the product meets or exceeds its RAS expectations. Overviews of:

- conceptual design process
- breadboard/prototype evaluations
- Systems Integration Testing
- Design Maturity Testing
- Process Maturity Testing
- Process Control

Section Three — Quality Control

In order to ensure that only the most reliable components go into its products and to ensure that quality is maintained at all levels of the manufacturing and assembly processes, DEC has implemented comprehensive quality control measures as typified by:

- Centralized Components Engineering
- Incoming Component Screening
- Multilayer Board Testing
- Logic Module Testing

Section Four — Assembly, System Testing and Installation

Before being released for shipment, all DIGITAL products undergo rigorous acceptance tests in the manufacturing plant that built them. In addition, DIGITAL also assembles the complete system to be shipped to the customer and tests it interactively with representative software as a final acceptance test prior to customer delivery:

- Volume Manufacturing Acceptance Tests
- Final Assembly and Test
- Field Installation Acceptance Tests
- Installation Feedback System

Section One Tangible Benefits of RAS at the System Level

Photograph

Large PDP-11/70 Configuration

DIGITAL's newest system, PDP-11/70, typifies the corporation's RAS philosophy. Compared to its immediate predecessor, the PDP-11/45, the 11/70 is a much larger system, more complex and far more powerful. But maintenance prices are about 15% less than those of a comparably configured 11/45 and average repair times are estimated to be 1/3 less.

This maintenance price reduction in the face of rising manpower costs and soring inflation is made possible by a combination of reliability and serviceability advances in operating software, in diagnostic software and the 11/70 itself such as:

- Error Logging
- On Line Diagnostics
- Bootstrap ROM
- New diagnostic device handlers
- Extensive Parity checking
- Multiple new error registers
- Use of Light Emitting Diodes
- Conservative Design Approach

The net result is that:

- the 11/70 features precise rapid fault isolation with minimum repair time.
- the 11/70 is a "fail-soft" system allowing critical processing to continue by bypassing failed system elements when faults do occur
- the 11/70 maximizes availability or system "uptime"

Let's take a closer look at some of these specific RAS features.

Error Logging (Supported by RSX-11M, RSX-11D, RSTS/E and IAS)

Photograph

Error Log Printout (RSTS/E)

- Labels and captions interpreting information

The operating system automatically records detailed status information on all detected errors whether correctible or not as well as a history of retries and corrective actions taken. This error history is initially recorded in a portion of the Operating System memory and perodically transferred to a pre-allocated disk file where it can be interrogated by the field service engineer or the user.

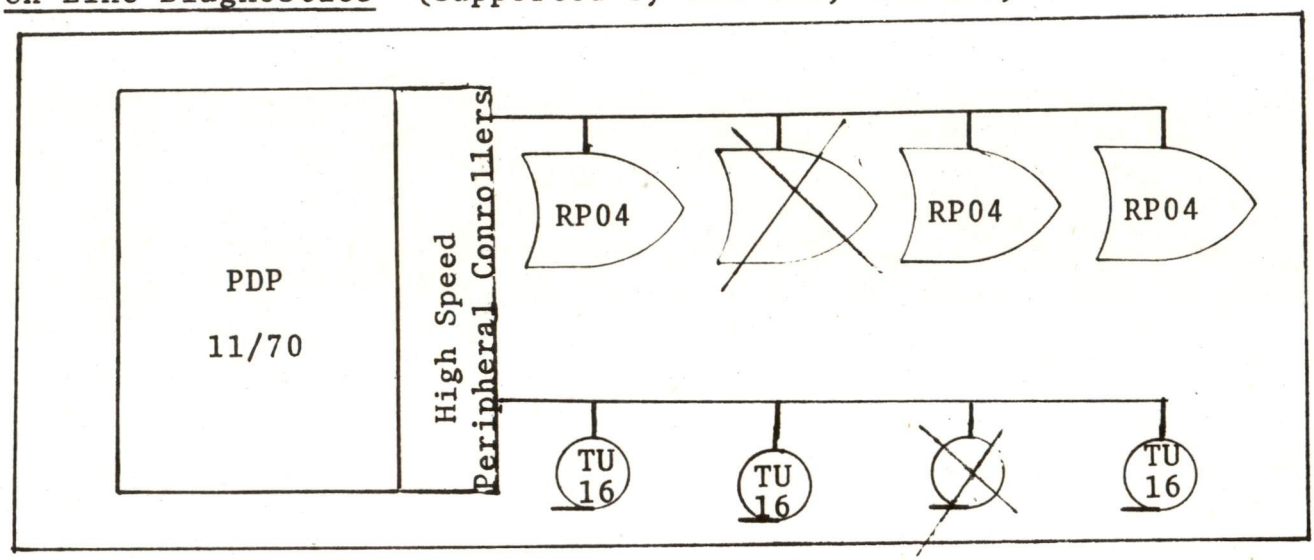
This error log is extremely significant as an anticipatory diagnostic tool. Scanning this information tells the DP manager or FS technician, for example:

- Read/write errors on moving head disks have significantly increased in the last 48 hours. All of these errors were automatically corrected by the system by retrying the operation and did not adversly affect the user in any way. However, it is time to clean the R/W heads to forestall future problems.

- Disk drive #4 exhibits an abnormal number of correctible errors relative to other devices in the system. Requires preventive maintenance to avoid future problems.

This information is also an extremely effective tool for the field-service technician in terms of diagnosing a "sick" system. The technician gets an early indication of where problems exist before using his diagnostic tools and is able to tackle the problem in a much more direct way than if this information were not available.

On Line Diagnostics (Supported by RSX-11M, RSX-11D)



The user or field service technician is able to run diagnostics on I/O devices of questionable status concurrent with processing. Newly written diagnostic device handlers for all of the major peripherals supported by these operating systems provide a vehicle for exercising the full device functionality of the questionable peripheral as well as looping on error conditons for diagnosis without tying up the subsystem controller or other devices of the same type on that controller.

The user or field service technician mounts a scratch disk pack on the device to be diagnosed and logically deletes this resource from the system allowing processing to continue while diagnosis takes place.

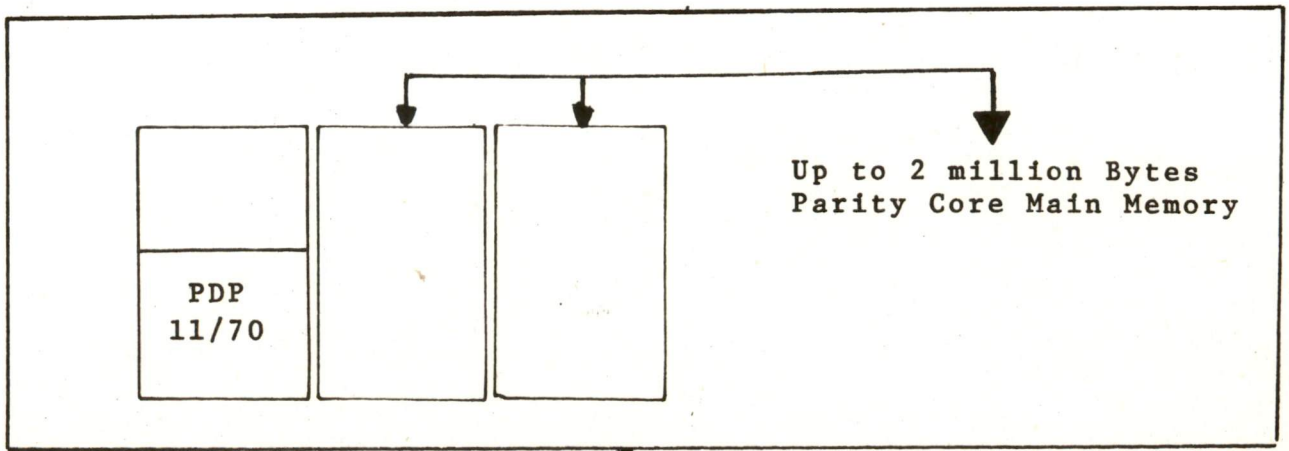
RP04 Error Correction and offset Head Positioning (Supported by RSX-11M)

Photograph RP04	RP04 Specifications - extract from High performance Peripherals Brochure

PDP-11/70 systems configured with RP04 moving head disks (88MB per spindle provide advanced recovery capabilities such as:

- error bursts of up to 11 bits occurring in a data field are automatically detected and corrected by a dynamic error correction algorithm without having to re-read the incorrect sector
- in the event that multiple attempts to read are unsuccesful, the read/write head positoner on a RP04 is automatically moved about the track centerline in both directions in small incremental steps to correct for slight mechanical misalignments between the RP04 R/W heads and the disk pack being read.

Parity Memory (Supported by RSX-11M, RSX-11D, RSTS/E and IAS)



These operating systems utilize the hardware's parity error detection logic to isolate faulty memory and prevent its use by user tasks thereby insuring data integrity.

RSTS/E automatically and dynamically responds to a hard parity error in the user portion of main memory by logically deleting memory in 1 KW blocks and reconfiguring itself. Only the user utilizing the bad block of memory is affected and he is aborted.

RSX-11M, 11-D, and IAS respond to hard parity errors in the user portion of main memory by freezing the user task occuping that portion of memory and not allowing other user tasks to be rolled into that area. The user then has the opportunity to take whatever action he deems to be appropriate.

These are only a few of the many reliability, availability and serviceability features built into DIGITAL's software products. Consult the appropriate system documentation for additional information on these features as well as:

- device independence
- disk pack initialization
- disk synchronization
- device timeout
- bad sector blocking
- magnetic tape skip/rewrite for bad spots on tape
- file recovery
- file protection codes
- disk copying utilities - on line/off line

- segregating user tasks from each other and from the operating system
- automatic retry - correct
- error handling routines
- etc.

PDP-11/70 Diagnostic Complex

Photograph

- M9301 Diagnostic ROM Boostrap Loader

Whenever the 11/70 is bootstrapped, the Diagnostic ROM Bootstrap Loader M9301:

- verifies that the system elements required to load the system monitor or diagnostic software are functioning properly (cache, CPU, memory management, and main memory)
- exercises the instructions necessary to boot the system
- tests the memory area to be used by the secondary boot which actually loads the system monitor or diagnostics

The DEC/X11 Subsystem Exerciser is a common diagnostic for all PDP-11's designed to exercise the UNIBUS. DEC-X11 is built modularly to match the exact customer configurations. It isolates interactive device problems on the UNIBUS to the offending device or devices for remedial attention.

Subsystem Diagnostic

The 11/70 also features its own newly written subsystem diagnostic which:

- first serially and then interactively exercises each of the core subsystems (CPU, Memory Management, Cache, FPP, UNIBUS, MAP, UNIBUS, Memory and Mass Bus Devices)
- outputs to the F.S. technician an English text message that details which subsystem is malfunctioning and which stand alone diagnostic should be loaded.

Stand Alone Diagnostics

Photograph

- Print Out from Diagnostic Message Log
- Labels and Captions to interpret information
- J. Lacey can provide

Having isolated problems to a specific subsystem, the field serviceman selects from a battery of newly written stand alone diagnostics in

order to further isolate the problems to a replaceable module. These stand alone diagnostics are written from the logic prints and trace the logic flow through the various ROM states. These Diagnostics isolate the fault to the function level (generally a single board) and frequently isolates the problem to a specific gate or chip. The field engineer then replaces the malfunctioning board.

DIGITAL has a 95% confidence level in the ability of this new battery of diagnostic tools to speedily and successfully diagnose malfunctions to the module level

Extensive Parity Checking

Block Diagram 11/70 Parity Checking Scheme
- Shows where parity is generated and where it is checked
- Extract from PDP-11/70 Processor Handbook pg 7-5

- Parity is checked on address and data transfers between the high speed peripherals and their controllers
- Parity is checked on data transfers between high speed peripheral controls and main memory
- Parity is checked on data transfers between the CPU and main memory
- Parity is checked on data and addresses within cache

A parity bit is associated with each byte (8 bits) of information and is checked by the 11/70 parity logic. The possibility of an undetected

parity error occurring is near zero.

Transient parity errors in cache are automatically corrected by re-reading correct information from main memory which always backs up cache. Under software control, the user can disable one or both cache groups in the event of a hard parity error in cache allowing critical processing to continue by bypassing the faulty cache group(s) in the unlikely event that the systems cache should fail.

Multiple Error Registers

The 11/70 features ten 16-bit error status registers which record detailed error status information the instant an error occurs. This information vastly improves the ability of the operating system and diagnostics to pinpoint the cause of the malfunctions to recover if possible and substantially reduces repair times.

Register	Used For
• CP Error Register	Source of abort or trap used vector at location - illegal halt - odd address error - non existent cache memory - Red Zone stack limit - UNIBUS time out - Yellow Zone stack limit
• Low Address Register	Lowest 16 bits of 22 bit address
• High Address Register	Upper 6 bits of 22 bit address Type of operation: DATI,DATAIP,DATO,DATOB
• Memory System Erra Register	Localizes memory failure to cache or core and isolates to odd/even word within cache
• Maintenance Register	Checks the parity checkers and is used for margining main memory
• Control Register	Used for disabling one or both cache groups
• Hit/Miss Register	Verifies that cache is working
• (3) Memory Management Register	Verifies that memory management is functioning properly and isolates faults within memory management.

Use of Light Emitting Diodes

Photograph - PDP-11/70 Memory Board - Show LEDS lit - Captions and labels for understanding	Photograph - Massbus Controller Board - Show LEDS lit - Captions and labels for understanding

The 11/70 designers placed light emitting diodes (LEDS) on the logic boards used for the high speed peripheral controllers and main memory. These LEDS give the field service technician a visual indication of where problems exist, which boards are active and assurance that the boards are installed correctly.

An interesting and effective characteristic of the LEDS is that they can stay lit indefinitely. This is very helpful in a situation where a transient parity problem temporarily existed in memory, was successfully by-passed, and never occurred again. The LED that lit up when that failure occurred remains lit indefinitely providing the field service technician with useful information even if his visit is weeks after the occurence so that he can replace the marginal memory module before real problems occur.

Conservative Design Approach & Design for Good Operating Conditions

- The 11/70 utilizes field proven Shottky TTL logic
- The use of new components was kept to an absolute minimum. Only 4 new IC's were introduced out of the hundreds used in the 11/70

- Seventeen ball bearing fans used in 11/70 processor cabinet for ideal air flow
- Main Memory packaged in its own dedicated cabinetry away from the heat pollution of the CPU. Main memory is run at slightly less than its rated specification thereby using less power and generating less heat. High performance with fast memory access achieved via cache
- Each main memory frame is independtly cooled front to rear via louvered front door with 2 ball bearing fans per frame for ideal air flow.

One of DIGITAL's fundamental design philosophies is to use worst case component specifications as the basis for logic design. This approach minimizes, for example, the possibility of timing problems or susceptibility to failure because of deteriorating or hostile environmental conditions.

For example, a component vendor's specification typically states minimum/maximum propagation delay characteristics assuming low density use under ideal conditions (25° C). DIGITAL, however, independently determines the component's true characteristics in high density use with less than ideal conditions (70° C) and then uses the worst case numbers as its basis for logic design.

Photograph

74S00
Quadruple 2 input NAND gate

	Vendor Spec	DEC Spec
Propagation Delay (Min)	2NS	1.75 NS
Propagation Delay (Max)	5NS	8.5 NS*
Loading (Density)	Low	Heavy
Temperature	25° C	70° C

*DIGITAL's design point

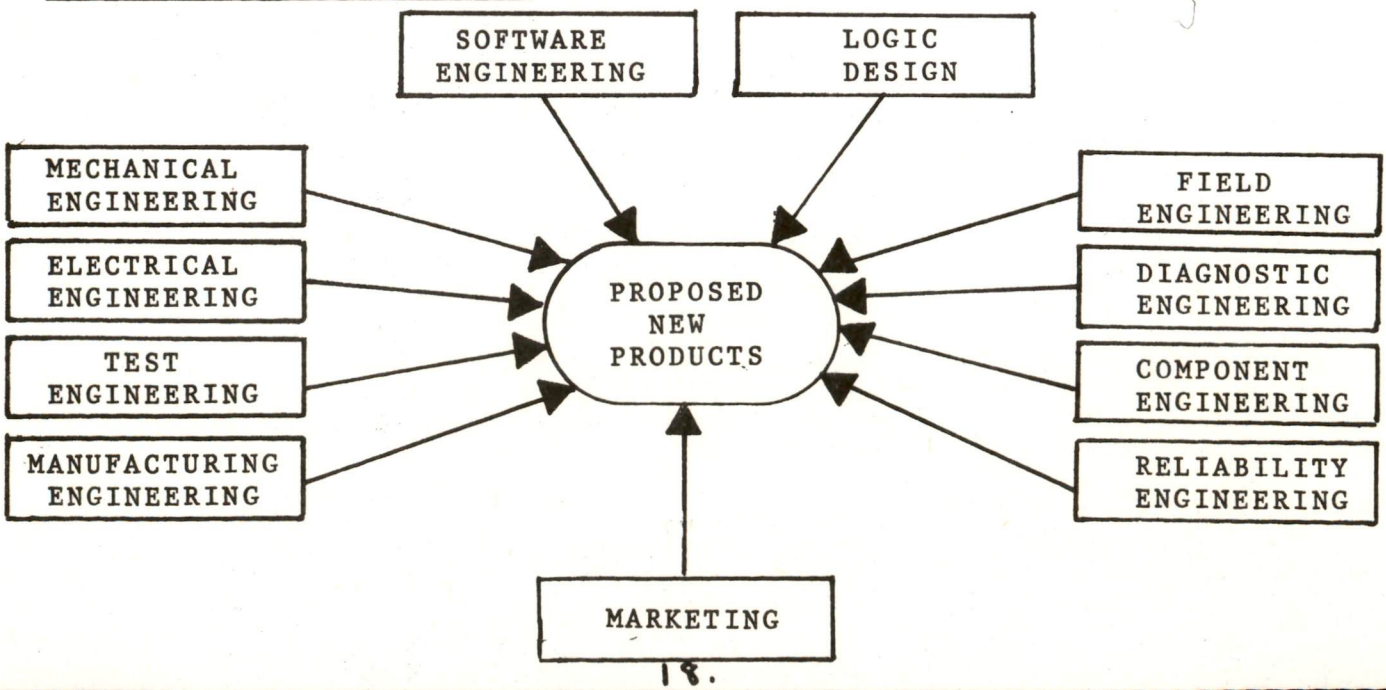
Section Two: INTRODUCING A NEW HIGH VOLUME PRODUCT TO MANUFACTURING

Before a new high volume product is released to manufacturing for production, it first has to successfully pass multiple screening tests designed to insure that:

- the product meets marketing requirements not only in terms of price/performance, but also in terms of reliability,serviceability and availability.
- the product is capable of achieving its performance goals
- the product is compatible with other system elements in full interactive use in a complex operating environment
- the product can meet its reliability and serviceability expectations
- the corporation has positive control over the myriad of manufacturing and assembly processes required to build the product

In this section we'll examine how DIGITAL qualifies a conceptual design, verifies the engineering model and thoroughly de-bugs the unit before it is even released to volume manufacturing

Conceptual Design Reviews



Newly proposed Digital products are carefully scrutinized from multiple vantage points during a series of conceptual reviews prior to receiving the go ahead to advance beyond the paper stage.

These reviews do not merely pay lip service to the various organizations involved, but are intense work sessions aimed at insuring that the proposed product:

- benefits from the problems and successes of earlier products of a similar nature
- anticipates maintenance requirements and incorporate features that simplify fault isolation thereby reducing the time required to effect repairs
- addresses system availability requirements by incorporating features which correct transient problems whenever possible, provide status to the system executive and avoids the "weak link" syndrome that will crash the system if the product fails
- recognizes the need for compatibility with the manufacturing processes involved and incorporates an adequate testing plan
- does not entail excessive risk in the areas of new technologies or new components. Extensive investigation and analysis with documented results and with back-up alternatives are required before "newness" is introduced.
- has an agressive but achievable reliability goal stated in of Mean Time Between Failures (MTBF) as measured in hours.

Breadboard and Prototype Debug

PHOTOGRAPH BREADBOARD	PHOTOGRAPH PROTOTYPE

The breadboard and prototype debug stages are essentially an engineering verification that the proposed new product can in fact meet its functional objectives. However, even at this stage of the design, field engineering, software engineering, manufacturing engineering, diagnostic engineering and others are very actively involved insuring that the new product is reliable, maintainable, compatible with other Digital products and manufacturing processes and that the new product will in fact meet customer expectations.

System Integration Testing

PHOTOGRAPH

SYSTEMS INTEGRATION TEST LABORATORY

System Integration Testing

Before a new PDP-11 product is released to volume manufacturing, it is first rigorously exercised in a controlled environment in the system integration laboratory. The primary concern is to ensure the electrical and functional integrity of the new product within full and complex operating systems environment with particular emphasis on bus interaction.

Specifically, these tests are designed to:

- expose latent product problems that reveal themselves only in a highly interactive systems environment.
- determine operational margins within a systems configurations
- validate compatibility specifications with respect to pre-existing hardware or software

Prior to system integrations testing, the new product must successfully undergo device level verification testing relative to its engineering test specifications. The actual product submitted for system-integration evaluation must be at least a limited production release version representative of the volume product to be shipped.

Within the representative system environment, systems integration testing is able to determine:

- Bus voltage margins
- Bus timing margins
- Bus crosstalk characteristics
- Conditions & rate of latency errors
- Tolerance to external EMI
- Level of intra cabinet RFI

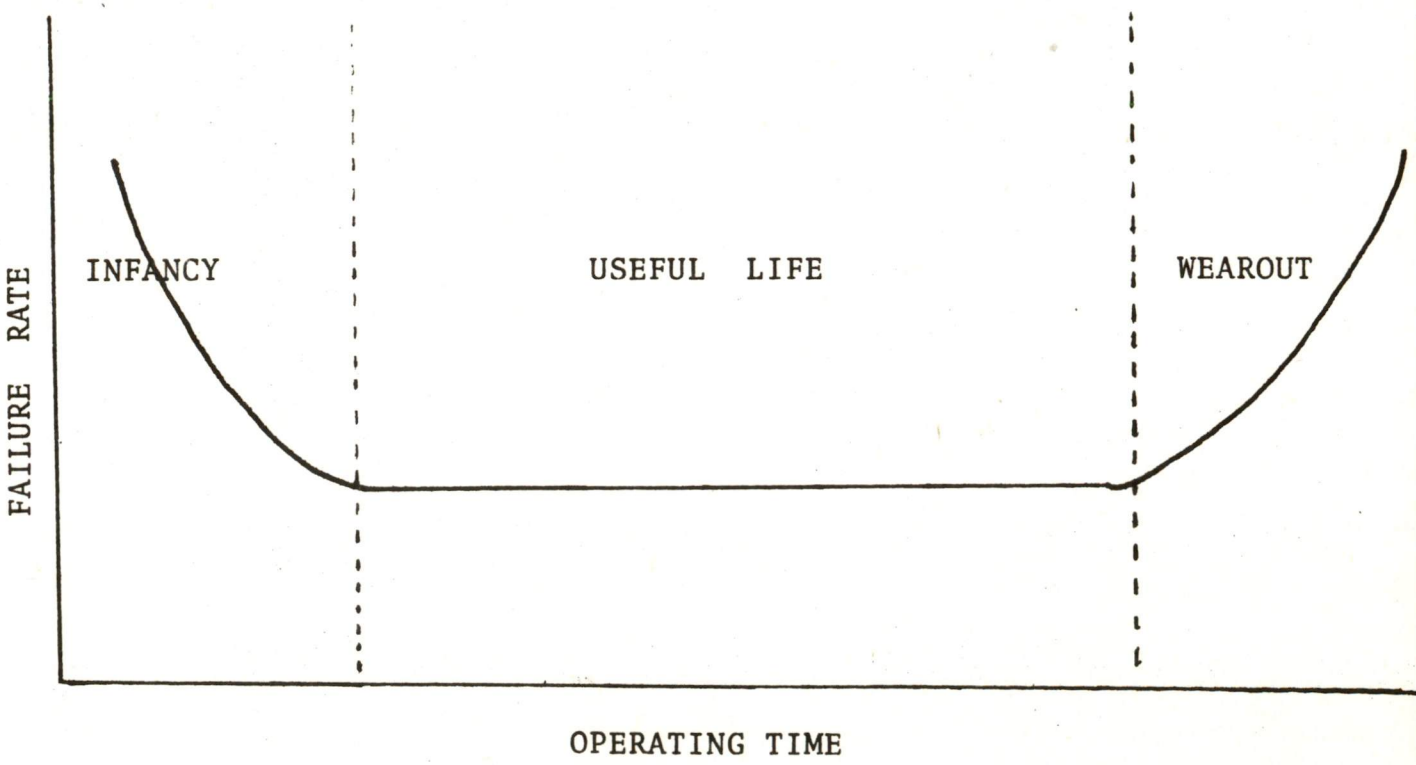
- Specific configurations constraints
- Operational margins with trouble-shooting extender boards
- Tolerance to extra-cabinet electrostatic discharge effects

In addition to the specific objectives of individual tests, extended operation under various diagnostics and operating system application loads verify that the new product operates correctly and reliably in a fully interactive systems environment with major peripherals and software systems.

As a result, that class of problem generally categorized as "interactive or system" in nature is weeded out before the product is committed to manufacturing.

Design Maturity Testing and Process Maturity Testing

The tendency of a device to fail over a period of time, i.e. failure rate, when displayed against age or time results in the widely known and accepted bath tub curve shown below:



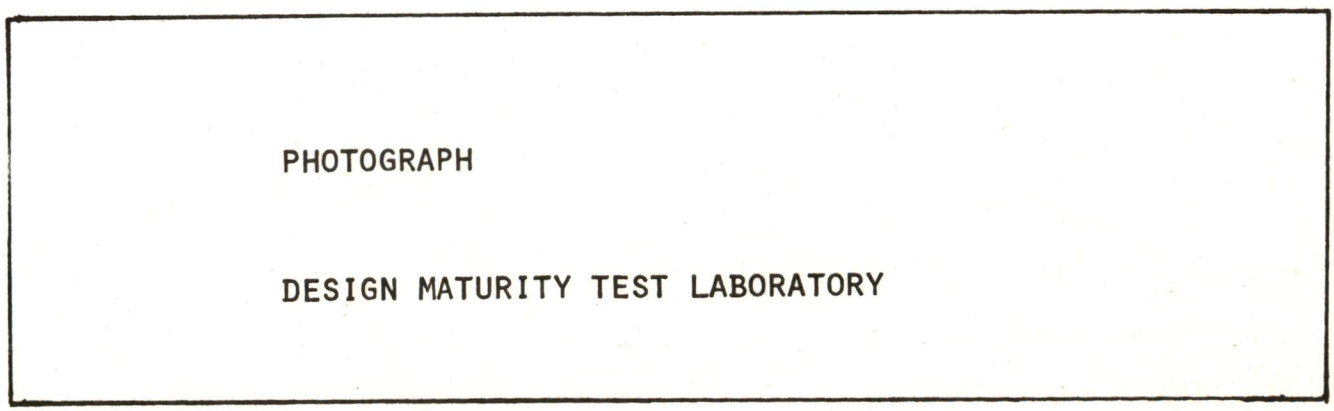
Failure rate after a product is constructed decreases with time through the period of infancy until it becomes relatively constant with time. The failure rate then remains at a constant level for a prolonged period (providing the equipment is maintained as required) until wearout is approached, at which point the failure rate begins to increase.

The value of the constant failure rate for a product is constrained by the elements of the design -- such as the stress levels at which parts are operated or the overall quality of the parts chosen. The ultimate reliability of the product can be decreased considerably by oversights in the design.

The Design Maturity Test is essentially a redesign of the product involving the introduction of engineering improvements until the product is capable of achieving its MTBF goals

The Process Maturity Test is designed to weed out the infant mortality of the new product and to insure that manufacturing has control over the myriad of manufacturing and assembly processes involved so that high quality copies of the product can be produced in volume.

Design Maturity Test



In the design maturity test, a small number of prototypes and/or early production units (10 to 20) are exercised for extended periods of time (months). The primary objective of this test is the detection of design deficiencies which detract from the ability of the new product to achieve its MTBF goals. The measurement of MTBF in hours is used as a quantitative measure to determine how close the product is to its potential reliability as determined by its complexity (predicted reliability)

Design improvements are introduced as necessary and the testing is of sufficient duration so that Reliability Engineering is able to observe the MTBF at a 90% confidence level before the product is committed to volume manufacturing.

The test is conducted using realistic functional software such as diagnostics and exercisers at environmental extremes within the advertized capabilities of the product. The test incorporates parametric measurements and overstress probing to determine safety margins, boundaries and design weaknesses. Variable operating conditions peculiar to the product such as speed, options, interfaces, etc. that are significant to the products performance are also duplicated.

Only after DIGITAL's design team has assured itself that the product can meet its specified MTBF goal is the product released to volume manufacturing.

Process Maturity Testing

PHOTOGRAPH

- PROCESS MATURITY TESTING
- SUGGEST LARGE NO. OF LA36's

The next step towards volume production is to perform a maturity test on the production processes used in volume manufacturing. DIGITAL subjects the initial production run of about 120 units to an extended "burn in" period of approximately 100 hours per unit.

Analysis of the data collected during approximately 10,000 hours of Process Maturity Testing:

- Provides information for maturing the production process
- establishes the critical control points that need to be monitored to maintain quality control
- determines the characteristics of a product's "infancy" in order that only a product which has completed its infancy is shipped.

The success of this newly implemented program has been nothing less than phenominal. The first two DIGITAL products to have fully benefitted from this testing - the LA36 DECwriter II and the VT50 Keyboard CRT

terminal realized a ten fold improvement in measured MTBF and substantially exceeded their design expectations.

Process Control

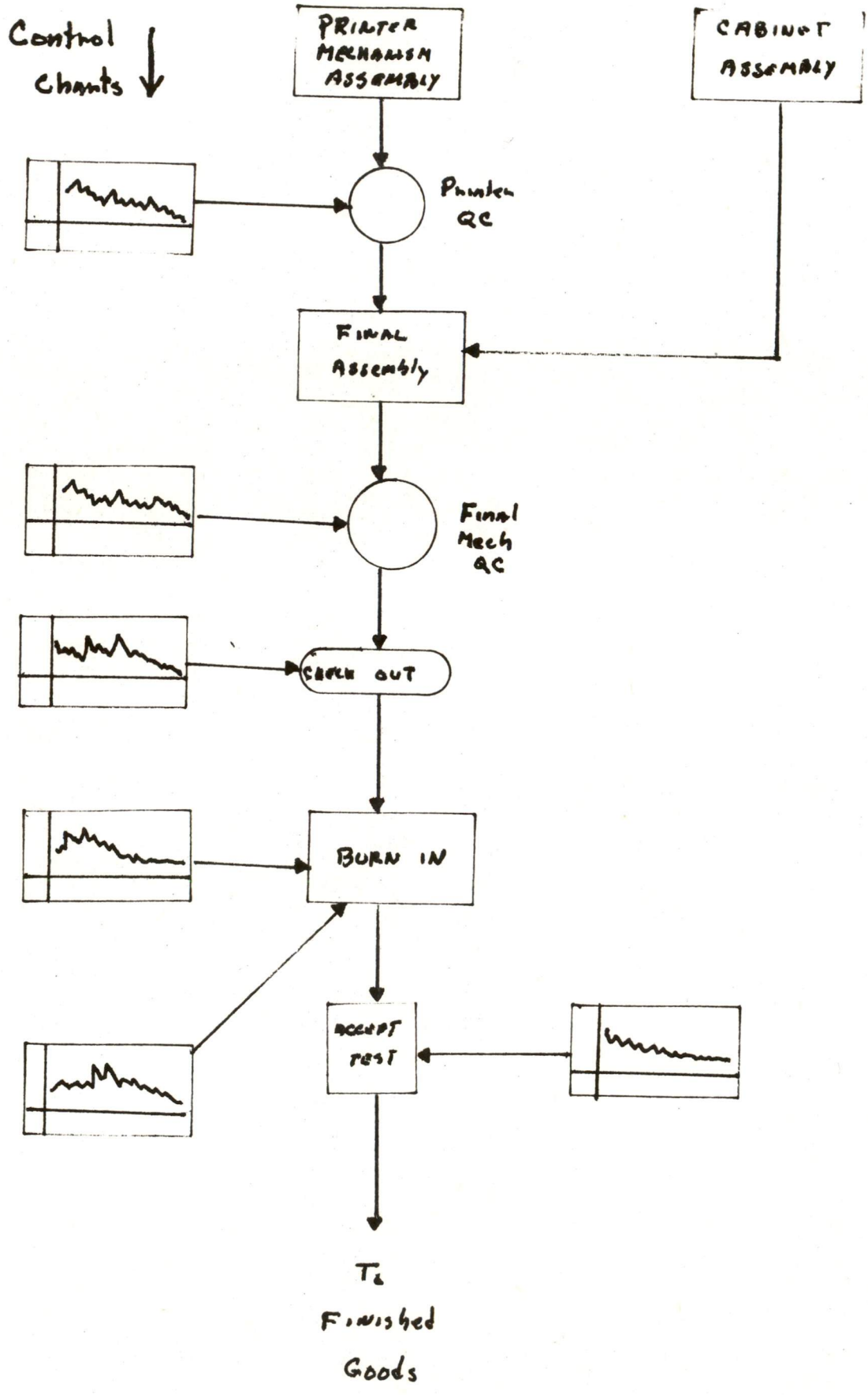
Once the proper burn-in period and mature MTBF are extablished for a product, it is absolutely essential that the degree of control demonstrated in reaching these points be maintained. Continuous, sensitive measurements must be taken in order to provide assurances that the production processes involved remain under control.

The data base established in previous testing forms a historical baseline useful in analyzing day-to-day performance and failure data.

DIGITAL is using control charts that continuously track detected defects at each quality control points. This enables the QC organization to determine whether or not the individual processes are under control. This data alerts QC to a situation where an individual process has broken down and enables corrective action to be taken immediately at the source of the problem.

Let's take a simplified look at how DIGITAL has implemented this system with LA36 production. QC check stations have been established at each of the critical process points in LA36 production. QC technicians test the output of each of these processes against established standards and record any defects observed. This data is transcribed to control charts for each lot produced and analyzed to determine the quality trend

LA 36 Control Chart Locations



The information on the control charts flags the specific process step which is causing problems. Quality control then works directly with the supevisor of that process step in eliminating the problem which could be caused by any of a variety of reasons:

- new personnel who don't adequately understand the process
- introduction of new subassemblies or assembly steps
- equipment out of calibration
- etcetra

PHOTOGRAPH

- LA36 CONTROL CHART

- EXTRACT FROM J. CRANSTON'S PRESENTATION

This approach insures that DIGITAL remains in control of its manufacturing processes.

Section Three Quality Control

So far, we've taken a look at some of the types of testing that precede the introduction of new products as well as a look at how DIGITAL maintains control over its assembly processes.

Quality control, however, begins far deeper in DIGITAL's organization. In the pages that follow, we'll look at just a few of these behind the scenes activities that control the quality of the components and logic modules used in DIGITAL products.

COMPONENTS ENGINEERING

At its Maynard, Mass. headquarters, DIGITAL has established a centralized Components Engineering Group which is chartered to:

- evaluate and test new technologies and components
- qualify vendors and parts for use in DIGITAL products
- perform detailed failure analysis on malfunctioning components
- legislate quality screening tests for incoming materials

The Component Engineering Group is staffed by experts in each of the tecnical disciplines which constitute the backbone of computer systems design. These individuals have superior academic and professional credentials and typically have ten or more years of experience in their chosen specialties such as:

- diodes
- linear semi-conductors
- semi-conductor processing
- digital transistor semi-conductor design
- semi-conductor testing

- semi-conductor processing
- semi-conductor manufacturing
- LSI chip set semi-conductor design
- relays, switches, connectors
- lamps
- capacitors
- magnetics
- resistors, crystals, hybrids
- chemistry and bonding agents
- electro mechanical parts

Component Engineering's MOS/LSI evaluation laboratory typifies the capabilities of this organization. This facility, which represents in excess of $1M invested in sophisticated test equipment, precision microscopic, viewing equipment and elaborate photographic equipment has enabled DIGITAL to:

- evaluate on a sample basis an LSI vendor's process control and device reliability enabling the corporation to make intelligent primary and secondary source decisions
- create a mutual trust/respect relationship with LSI vendors by enhancing DEC's knowledge of IC technologies
- evaluate the "reality" of significant new IC technologies

Photograph MOS/LSI Laboratory	Photograph - Blow-up LSI chip - Labelled to show faults - Captions for understanding - R. Amann to supply

The custom LSI chip set for the LSI-11 is a case in point. DIGITAL's electrical and functional testing of sample lots not only uncovered faults but Component Engineering dissected the chips and was able to correlate the test results with a physical fault traceable to specific shortcomings in the vendor's process control. As a result DIGITAL's supplier upgraded its assembly and inspection processes before this component was used in DIGITAL products.

INCOMING INSPECTION

A primary function of Component Engineering is the legislation of adequate incoming acceptance inspection testing to insure that the raw material received from its suppliers meet DIGITAL's high quality standards. The QC organization in each of DIGITAL's manufacturing complexes use the screening tests defined by Component Engineering to weed out faulty or marginal components before they're ever introduced to the DIGITAL manufacturing processes.

The decision as to the level of acceptance screening required for raw material is based upon DIGITAL's many years of high volume manufacturing experience (more than 40,000 DIGITAL computers are installed worldwide). This experience translates to indepth knowledge of the components being used and how they're affected by DIGITAL's manufacturing practices and an acute awareness of the quality standards of the corporation's suppliers. These tests run the gamut from random sampling of incoming lots of raw material for conformance to physical specifications (e.g. fasteners, sheet metal, cabling, etc.) to 100% functional testing of active electronic components (e.g. IC's, transitors,

MOS chips, etc.).

For example, each and every one of the millions of IC's purchased by DIGITAL undergoes:

Photograph

Thermal Shock Testing of Incoming IC's

Thermal shock testing by being alternately dipped in cold water at 34°F for 3½ minutes and then being dipped in hot water at 212°F for 3½ minutes. This cycle is repeated five times. The thermal stresses encountere cause marginal components with bonding problems to fail subsequent functional and parametric testing.

Photograph

Pressure Cooker Test of Incoming IC's

Protective Encapsulation Testing - Each IC is pressure cooked for 1 hour at 135°F to see if humidity under pressure will penetrate the component's protective coating. Marginal or faulty components fail the subsequent functional & parametric tests.

Photograph

Functional Testing of Incoming IC's

Parametric and Functional Testing - DIGITAL uses highly specialized test equipment which measures the ability of pre-stressed components to meet their specifications when power is applied.

As a result of these tests, DIGITAL rejects 2.5% of incoming IC's but also realizes a yield of 99.96% of IC's during the balance of the manufacturing process.

Photograph

- 722 Power Supply undergoing incoming acceptance testing in environmental chamber
- Ingrid in WM to supply details

The H722 power supply is subjected to more than 8 hours of thermal stress testing @ 70°C under full load conditions as part of its acceptance test. The H722 is used in DIGITAL's industrial 1430/1435 programmable controller which may have to withstant hostile environmental conditions in a factory or a warehouse.

These tests are only a representative sample of the care and cautions DIGITAL exercises in screening components and vendor purchased sub-assemblies to maximize quality in DIGITAL's end products.

PRINTED CIRCUIT BOARD (PCB) PRODUCTION

DIGITAL exercises an equal amount of quality control over the products the corporation produces itself as is typified in PCB production. DIGITAL is currently producing in excess of 200,000 PCB's monthly to meet its own internal requirements. These logic boards vary in size from the "single" board measuring 2.5" x 8.5" to a large "hex board" measuring 1.5" x 8.5". DIGITAL uses a variety of single sided double sides and multilayer boards in satisfying its needs.

fdc-PDP11-2-4

digital INTEROFFICE MEMORANDUM

TO: Operations Committee

DATE: September 19, 1974

FROM: Robin Frith

DEPT: Computer Systems Development

EXT: 3850 LOC: 5-2

SUBJ: PDP-11 Strategy Status

Attached is a brief summary of the status of PDP-11 Strategy and of the product developments resulting from this strategy.

/st
Attachment

CONFIDENTIAL

JULY PDP-11 STRATEGY

RESULTS OF AUGUST 28 MEETING - NO CHANGE IN STRATEGY

UNKNOWNS THAT MAY AFFECT STRATEGY:

1. SPEED AND DELIVERY OF 11/05HM (11B05)
   1200 NSECS TO 800 NSECS

2. NEED AND VIABILITY OF THE 11/44
   VIRTUAL ADDRESS EXTENSION

   IS THE 11/44 THEN A 32-BIT MACHINE?

3. HOW MUCH OF THE DEC SYSTEM 10 SOFTWARE CAN THE 11/85 USE, OR DOES THE 11/85 HAVE TO START FROM SCRATCH?

   CONFLICTING GOALS?

CONFIDENTIAL

CURRENT STATUS

11/05L — 5¼" VERSION
- NO CHANGE IN SCHEDULED DELIVERY
- COST FOR MINIMUM PACKAGE NOW $997

CRITICAL PATH ITEMS:
- TPS POWER SUPPLY
- SPC MOS MEMORY

10½" VERSION
- NO COMMITMENT
- BA11K TOO EXPENSIVE
- 2 x 5¼" BOXES?

11/05HM
- NOT YET STARTED ON DESIGN
  JULY DELIVERY MAY SLIP

11/44
- NO CHANGE IN SCHEDULED DELIVERY
- FINAL SPECIFICATION (16 BIT) DUE OUT NOW
- VAX HARDWARE PROPOSAL OUT NOW
- VAX SOFTWARE PROPOSAL DUE 10/15

11/55
- NO CHANGE IN SCHEDULED DELIVERY
- BREADBOARD RUNNING RSX11D, RSTS/E SOFTWARE (STILL ONE BUG IN COMPILATION)
- PLAN IS TO SHIP WITH FIRST PASS BOARD LAYOUT
  IF RE-LAYOUT IS NEEDED, DELIVERY WILL SLIP

11/85
- NO CHANGE IN SCHEDULED DELIVERY
- TRYING TO DEFINE DETAILED GOALS
- FIRST PASS PRODUCT PLAN DUE OUT NOW

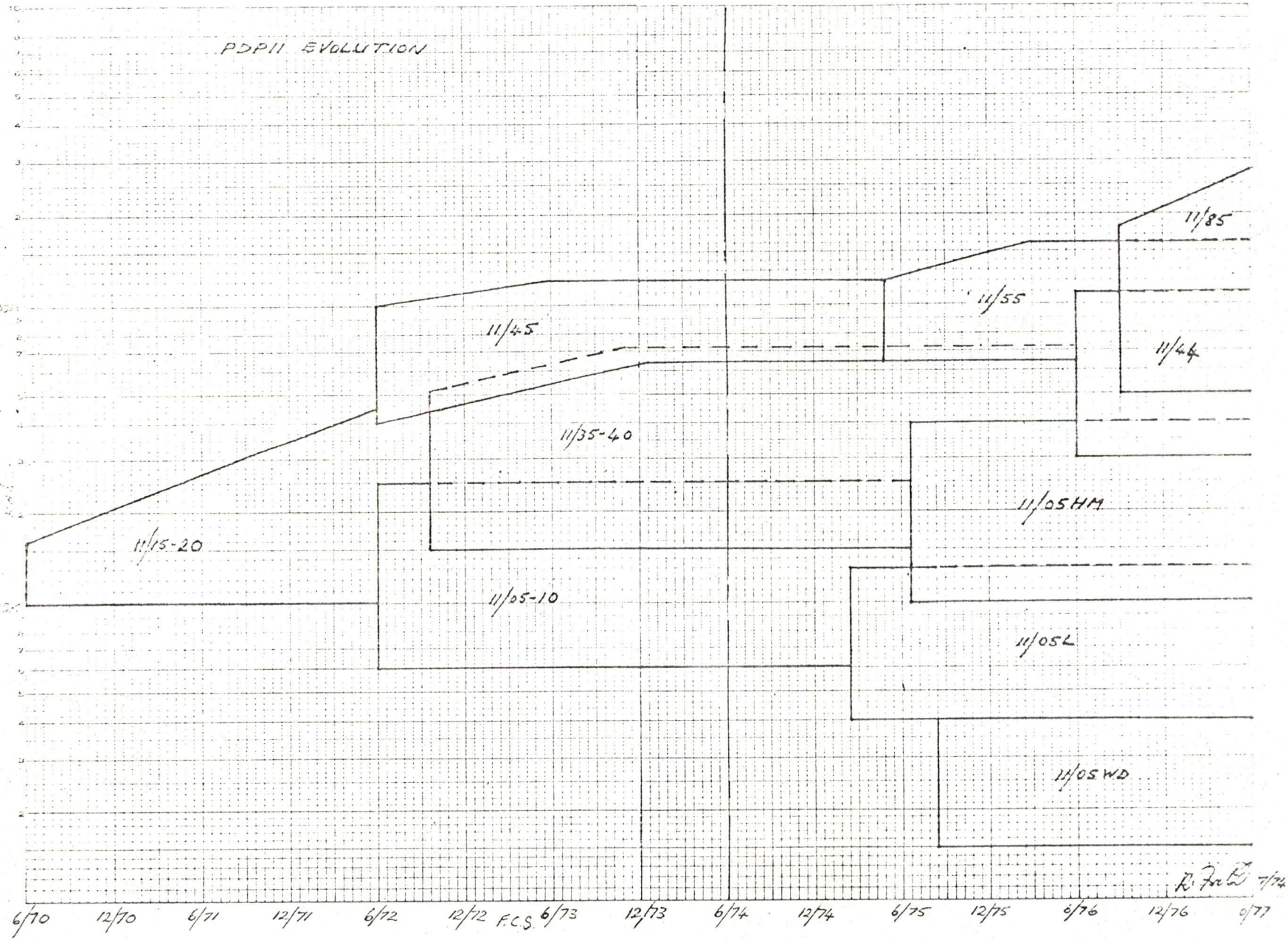
OTHER PRODUCT STRATEGIES THAT NEED UNDERSTANDING

1. LOW, LOW END (USING 11/05 WD CHIPS)
   NEW FAMILY OF PRODUCTS, PDP-11 INSTRUCTION SET
   TWO PRODUCT PHILOSOPHIES:

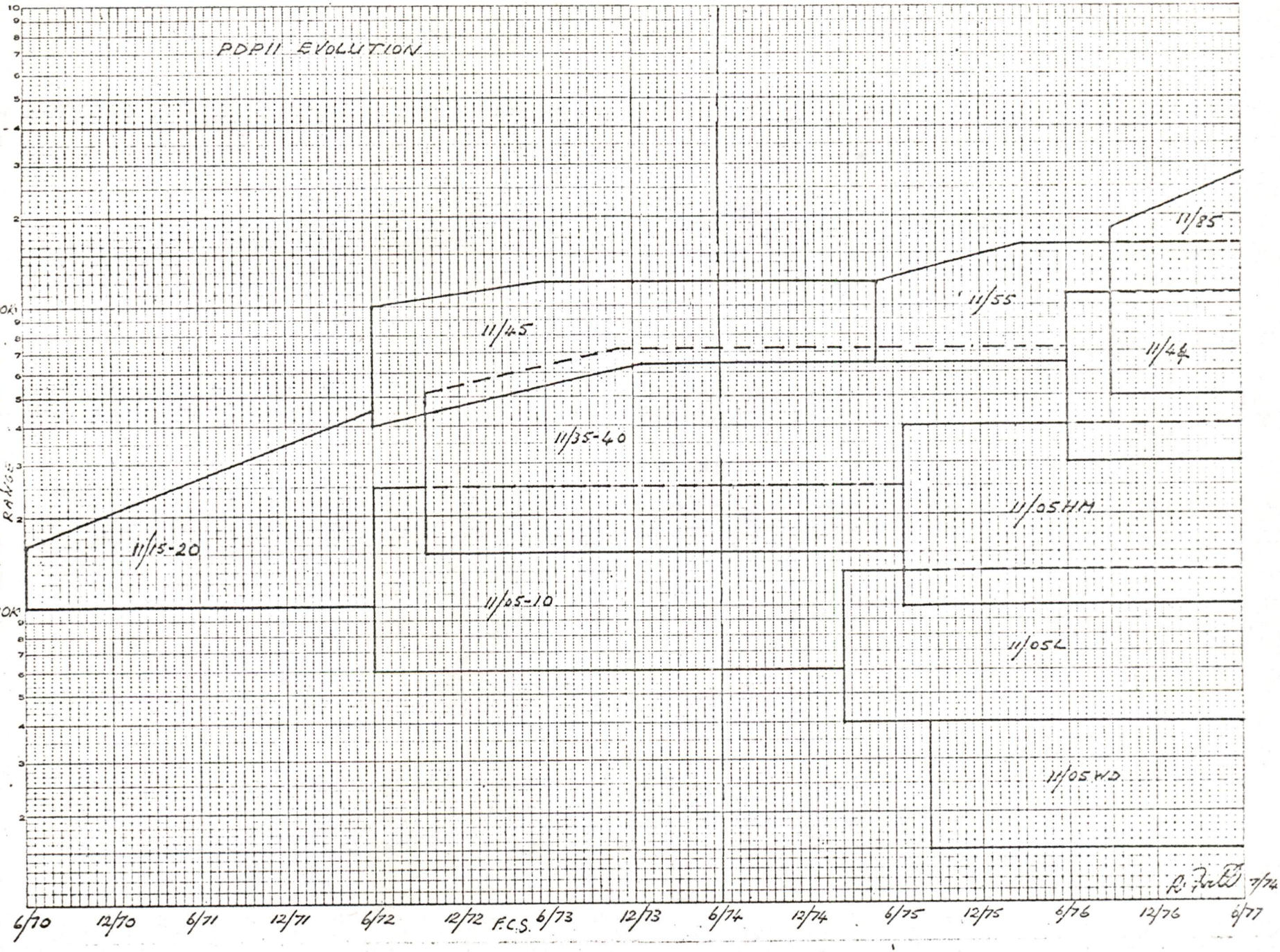
   (A) MODULAR DEVICES WITH WELL-DEFINED INTERCONNECT SCHEME
   CP, MEM, I/O DEVICES ON SEPARATE BOARDS

   (B) SYSTEMS (CPU, MEM, I/O DEVICES) ON A BOARD WITH A NUMBER OF DIFFERENT SYSTEM BOARDS

2. 36 BIT FAMILY
   WHAT ARE THE RELATIONSHIPS BETWEEN 11/85 AND DEC SYSTEM 10, 20 PRODUCTS?



CONFIDENTIAL


PDP11 EVOLUTION
APPROX SYSTEM PRICE RANGE
$100K
$10K
11/15-20
11/45
11/35-40
11/05-10
11/55
11/85
11/44
11/05HM
11/05L
11/05WD
6/70
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6/73
12/73
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12/76
6/77
7/74

digital INTEROFFICE MEMORANDUM

TO: Andy Knowles

Cc: Gordon Bell
Dick Best
Bob Puffer
Jack Smith

DATE: August 2, 1973

FROM: Ken Olsen

DEPT: Administration

EXT : 2300

SUBJ:

Will you look into the reliability of the PDP-11 bus for me so that we can face the question of whether or not we should slow it down or limit its length so that it will always work.

/d

COMPANY CONFIDENTIAL

Ken Olsen

digital INTEROFFICE MEMORANDUM

TO: Ed Kramer, Gordon Bell, Bill Long, Dick Clayton, Bob Savell, Pete VanRoekens, Julius Marcus

CC: Operations Committee

DATE: June 13, 1974

FROM: Andy Knowles

DEPT: Small Computer Products

EXT: 3043 LOC: 5-2

SUBJ: PDP-11 STRATEGY

I believe our first group meeting was quite fruitful. We covered a great deal of ground:

(1) Appointment of "Management Consultants" to the "Product Managers". We evolved this concept to help the decision process for both hardware and software. The management consultants are to be senior group managers who through their interest and presence will champion and sponsor computer hardware and appropriate software products. They will act as consultants to the product managers, major hassle settlers (of hassles between market groups), and sponsors of the products at P.L. Mgr. meeting, Operations Committee meetings, etc.

Computer System	Management Consultant
11/05	Bill Long
11/44 - 11/55	Julius Marcus, Brad Vachon
11/85	Ed Kramer

(2) Notes on 11 family

11/05 series — Seems to be consensus between users and builders that what is being designed is what is desired in the market place by the system users. We will address the 16 Bit computer on a board problem as a separate issue.

11/44 & 11/55 — Deep concern here and considerable disagreement between the users and the builders. The problems derived from

(a) a lack of understanding of what's being designed (by the users)

(b) The failure to accept the architectural limitations of the 11 (Modcomp, inst. set, etc.)

(c) Too much faith in what will come out of Teicher's work (i.e. he'll extend upwards far enough into the 16 bit mid-range to satisfy you users, don't worry, have faith, etc.

We need considerably more discussion and interaction here.

My simple view at this point, yields a less complicated 11 strategy (than say Dick Clayton).

11/05 — Keep going Steve. Bill Long will write down complete functional specs with you.

11/44 11/55 — Two high end, systems machines of which neither will satisfy our competitive needs in terms of competitive, bench mark wise. One of them may have to go. Julius would like the 11/44 to be a hot 16 bit machine, a 11/40R and not a competitor to the 11/55. Keep going on the 11/55 as a marketing smoke screen. Again - mucho more discussion and planning needed here.

11/85 — See users desires. Is that what we are building? If so, users are happy.

Could we please start the discussion "in the middle" (11/44, 11/55) Friday A.M.? Please be prepared to start there.

/sc
Attachments

CONSTRUCTION OF A BUSINESS STRATEGY

Most companies feel they are in a highly competitive business. Most companies regard their competitors as the principal obstacle to either higher profits or faster growth. This is natural and proper. The question is how to compete.

Strategy is the manner of using resources which is expected to provide superior results in spite of otherwise equal or superior capabilities of a competitor.

Games have been classified as: (a) games of chance, (b) games of skill, and (c) games of strategy. For the purpose of this discussion, assume that chance and skill are equally distributed. How can a business firm develop a superior strategy?

We can assume that each firm has a relatively free choice in choosing its businesses. This choice can be expressed in terms of product line, market segments, geographical coverage, or other elements. However, the definition of businesses also determines who it will be competing against. Therefore, freedom to choose the business means freedom to choose who the competitors will be.

Firms are never identical. They have different histories and traditions, different resources, different reputations, different management styles, and often different objectives. These differences may be either strengths or weaknesses, depending upon the strategy chosen. We can assume that such differences exist, and that they are important to the choice of strategy.

We can also assume that neither your own nor your competition's objectives are simple or obvious. There are many tradeoffs between near term profit and long term, between growth and profits, between growth in assets and growth in reported profits, between stability and growth, between dividends and growth, between stockholders, employees, creditors and others. It is reasonable to assume that these differences will result in different goals for different competitors.

It is also safe to assume that the future will produce a substantial amount of change. The change will be in technology, markets, and competitors. Consequently, any strategy must take this change into account.

Based upon these assumptions, the starting point for strategy development should be:

1. Definition of the business area involved.
2. Identification of the significant competitors in that business area.
3. Identification of the differences between you and the significant competitors.
4. A forecast of the changes in the environment which can affect the competition.
5. An identification of your own objectives and any known differences from those of competitors.

These are all very obvious factors, but they should be made explicit since a change in any one requires a reexamination of the entire sequence.

The difficult part of constructing a strategy is the development of the strategy concept. Any strategy of value requires that you

follow a different course from your competitors;

or initiate action which will not be effective for the competitor if he attempts to emulate you;

or follow a course which will have quite different, and more favorable, consequences for you than for your competitor.

The essential element of successful strategy is that it derives its success from the differences between competitors with a consequent difference in their behavior. Ordinarily, this means that any corporate policy and plan which is typical of the industry is doomed to mediocrity. Where this is not so, it should be possible to demonstrate that all *other* competitors are at a distinct disadvantage.

Strategy development, then, consists of conceiving of ways and means to emphasize the value of your differences when compared to competitors. The normal procedure includes:

1. Start with the present business as it now is.
2. Forecast what will happen to its environment in general over a reasonable period of years. This includes markets, technology, industry volume, and competitive behavior.
3. Predict what your performance will be over this period if you continue with no significant change in your policies or methods of operation.
4. If this is fully satisfactory, then stop there, since you do not need to develop any further to achieve satisfaction. If the prediction is not fully satisfying, then continue.
5. Appraise the significant strengths and weaknesses that you have in comparison to your more important competitors. This appraisal should include any factors which may become important: finance, marketing ability, technology, costs, organization, morale, reputation, management depth, etc.
6. Evaluate the differences between your policies and strategies and those of your major competitors.
7. Attempt to conceive of some variation in policy or strategy which would produce a more favorable relationship in your competitive posture in the future.
8. Appraise the proposed alternate strategy in terms of possible risks, competitive response, and potential payout. Evaluate in terms of minimum acceptable corporate performance.
9. If this is satisfactory, then stop strategy development and concentrate on planning the implementation.
10. If a satisfactory result has not been found in the previous stages, then broaden the definition of the present business and repeat the cycle above. Ordinarily, the redefinition of the business means looking at other products you can supply to a market

which you know and understand. Sometimes it means supplying existing products to a different market. Less frequently, it means applying technical or financial abilities to new products and new markets simultaneously.

11. The process of broadening the definition of the business to provide a wide horizon can be continued until one of the following occurs:
    a. The knowledge of the new area becomes so thin that a choice of the sector to study becomes intuitive or based upon obviously inadequate judgment.
    b. The cost of studying the new area becomes prohibitively expensive because of lack of related experience.
    c. It becomes clear that the prospects of finding a competitive opportunity have become remote.
12. If the existing business is not satisfactory and no broadening of the business offers satisfactory prospects, then only two alternatives exist:
    a. Lower the performance expectations.
    b. Reverse the process and attempt to find an orderly method of disinvestment.

The critical element in strategy development is the development of a concept. This is inherently intuitive and cut-and-try, even though first class and skillful staff research is an absolutely essential prerequisite to success.

The process of constructing a business strategy tends to be a continuous cycle. It cannot be otherwise. Strategy development is an art, not a science.

One of a series of informal statements on corporate strategy prepared by members of the staff of The Boston Consulting Group.

RESEARCH AND CORPORATE STRATEGY I

Hit and Run

It is obvious that there are only two routes to leadership in a specific product market. You can invent the product and start with 100 percent of the market. Alternately, you can take the market away from the competitor who first dominated it.

There is an underlying business philosophy implicit in a business strategy that is dependent on invention.

This philosophy produces a sequence of:

— Invent.

— Skim the cream with high profit margins.

— Lose cost differential.

— Abandon.

— Replace with a new invention.

This pattern can be described more specifically in terms of a competitive product life cycle.

— The inventor establishes a very high initial profit margin on 100 percent of the relevant market. The market grows rapidly. He has far lower costs than potential competitors.

— The profit margin and growth attract competition as soon as patent protection expires or licenses become available.

— Competitors price to penetrate the market. Their growth is faster than the pioneer's, but since their volume is small, the pioneer still grows while attempting to maintain the price level.

— The pioneer maintains margins but loses market share. Competitors' relative costs decline much faster as they grow faster.

— Eventually the faster growth of competitors more than absorbs all of the industry growth creating unused capacity. The pioneer's efforts to maintain existing facility operations at normal levels or to grow produce a declining price level for everyone.

— Over capacity and declining price continue until capacity additions are discouraged. Characteristically, some producer does continue to add capacity and preempts most of the growth. The pioneer characteristically regards the product as a "commodity" long before this point is reached and therefore slows further investment of his own.

— Eventually the principal survivor, who usually is not the pioneer, has a dominant share of a product-market which is growing slowly by then. The costs of this survivor declined as his market share grew, i.e. the experience curve effect. His profit margins tend to be highly satisfactory if he has an adequate lead in market share.

This dominant survivor has a profitable business that is almost immune to normal competition. Past experience has discouraged competitive interest. The by now slow growth makes it very difficult for a competitor to grow rapidly by preempting industry growth. The remaining competitors have higher costs. His own profit margin can be safely leveraged giving a very high return on his shareholder equity.

As long as this principal survivor is content with a cash throw off equal to his cost differential, he has great security. He can set a price level which will make competitive investment unattractive and still provide net cash generation that continues to grow indefinitely at a modest rate. Only a significant mistake on his own part is apt to threaten his profit margin or his market position thereafter. His profit is a function of his relative market share in the relevant segments.

Many competitors seem to have an interest only in the R&D and high margin portion of this cycle. This security of a stable, secure and rewarding profit margin and position in a "commodity" seems to be of little attraction to them. Their emphasis on current profit margin rather than market share maintenance accelerates such a cycle.

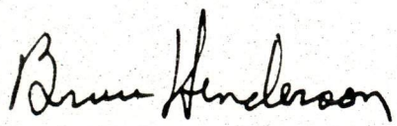
This pattern has developed at an increasing rate in recent years. When competition reduces a product to a "commodity" in a short time span, then much of the value of research investment is effectively cancelled by the inability to capitalize on R&D long enough. The pioneer's investment in R&D becomes very high risk accordingly.

Such a product cycle is inherently high risk for *all* competitors.

Late entries into a product begin with an inherent cost disadvantage. To grow, they must invest heavily at a low or negative profit margin. For them, the investment must always be justified by hope of future profit instead of current return. There is always the risk that the leader — with lower costs — will prefer holding share to holding margin. If that happens before costs become equivalent, then the challenger's entire investment becomes nearly worthless. This risk is unavoidable for the follower who buys share from the innovator.

For the pioneer the risk is high too. Failure to continually produce new products will result in gradual liquidation of the firm. If product profitability life becomes too short, then the investment in research becomes a cost burden instead of a source of competitive advantage.

In this pattern of competition, *the pioneer bets the company on its ability to continually produce new high margin products.* If loss of share is too fast or the rate of new product introduction is inadequate, then the company's growth and profitability will both inevitably decline.



Bruce D. Henderson

A companion piece "Research and Corporate Strategy — Bet on Success" will be distributed as the next Perspectives.

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One Boston Place, Boston, Massachusetts 02106

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PERSPECTIVES

RESEARCH AND CORPORATE STRATEGY

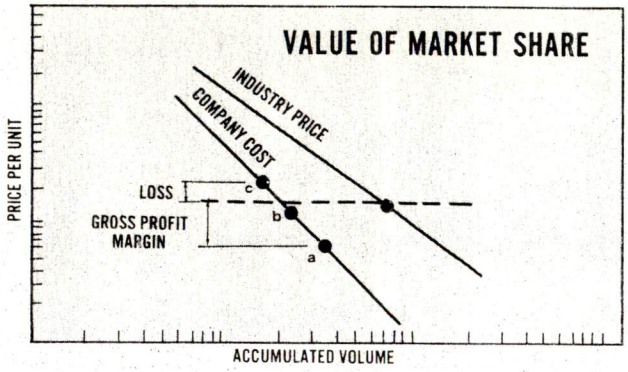
I

The Boston Consulting Group

FAILURE TO COMPETE

The dominant producer in every business should increase his market share steadily. Failure to do so is prima facie evidence of failure to compete.

Cost and market share are inversely related. The highest market share should produce the lowest cost as a result of the experience curve effect. At least part of that superior cost should be passed on to the customer in lower prices or better quality. That in turn should lead to faster growth of the leading competitor.



Failure to gain market share even with superior costs is failure to compete. This failure is also a failure to achieve even lower costs.

Competitors' market shares should be unstable. Low cost competitors should displace higher cost competitors. Customers should share the benefits of lower cost with those suppliers who make it possible. Any failure to gain market share even with lower cost is self-evident restraint of trade.

Displacement of high cost competitors by lower prices benefits the customer. It leads to benign monopoly. No monopoly can be justly accused of exercising monopoly powers if it does not raise prices more than the extent of inflation.

Failure of an industry to concentrate is failure to compete and a failure of the national economy to optimize productivity and reduce inflation.

Bruce Henderson

Bruce D. Henderson

PUBLIC POLICY NOTE

See your lawyer before gaining market share if you are a leader. What is best for the customer and the country is not necessarily legal.

digital INTEROFFICE MEMORANDUM

TO: Dave Best
Andy Knowles
Julius Marcus
Bob Savell

DATE: June 12, 1974

FROM: Ed Kramer

DEPT: LDP/BIO

EXT : 2425

SUBJ: PDP 11 STRATEGY MEETING #1 (USERS)

The object of this first meeting was to specify in as little detail as possible what we thought the goals were for the new 11 products currently under development.

The first objective was to specify cost and delivery dates and to establish these two criteria as being inviolate. Any modification to these criteria will be formally proposed once they have been accepted.

SECTION I 11/05 Replacement

1. Greater than two times cost/performance of the current 11/05

2. Must fit 11E10 peripheral controllers in the same box

3. Must maintain current SPC slot compatibility

4. 20,000 hours MTBF; ten minutes MTTR (board swap)
Cost: (transfer) $850. Includes box, power supply, CPU, 8K MOS memory, and console.
Delivery: 500 units delivered by Q4 FY75.

SECTION II 11/40 Replacement

1. Must be code compatible with current 11/40

2. Integral EIS. Optional FIS.

3. User micro code. 150 nanoseconds per internal cycle.

4. The I/O must be modified to allow fast response in handling interrupts (probably handled at the micro code level).

5. I/O buses must handle RK06/TU16 + 50 KC communications I/O.

6. Must handle MOS memory with parity.

7. Basic instruction time 600 nanoseconds for register to

(OVER)

register add

8. Must handle up to 128K words of memory.

9. Must have at least UNIBUS I/O

10. Must handle core memory (16K and 32K sense stacks)

11. Must have faster context switching than current 11/40

12. Must contain facilities in hardware to enhance FORTRAN execution.

13. Must have hooks for multi-processors, at least for redundancy purposes.

14. MTBF 8,000 hours, MTTR 15 minutes
Cost: $1,800 and includes box,CPU, 8K memory, power supply, no console. Box must be large enough to handle at least four additional system units and include 64K of memory.
Delivery: Q2 FY76 100 units shipped

SECTION III 11/45 Replacement (11/55)

1. DO WHATEVER IS POSSIBLE TO ENHANCE THE PERFORMANCE OF THE MACHINE AND MAKE THIS PRODUCT DELIVERABLE IN JANUARY 1975.

IV. 11/85

1. VIROS compatible

2. Must be able to run PDP 11 programs at approximately 11/40 speeds (probably through emulation).

3. Basic processor cycle time to run at memory speeds (depends on what memory is available at ship time, i.e., 32K sense memory).

4. Must contain UNIBUS I/O

5. Must be capable of running an operating system similar to RSX11M/D.
Cost: $4,000, includes 32K memory, box, power supply, CPU
Delivery: Q4 FY76 for 25 units.

digital INTEROFFICE MEMORANDUM

TO: Julius Marcus
Andy Knowles
Bill Long
Bob Savell
Ed Kramer
CC: Dick Clayton
Gordon Bell

DATE: June 6, 1974

FROM: Bruce Delagi BD

DEPT: 11 Engineering

EXT: 3563 LOC: 5-5

SUBJ:

In your discussions on the "11 strategy" it would be helpful to me if you could resolve the following questions:

1. Do we believe that 75% of the current 11/45 business can be migrated over to a -10 if we permit our customers to retain their hardware interfaces, higher level language code, and their data bases but not their machine level code?

2. Do we want to be in the systems-on-a-board business? If so, can we think of such systems as dedicated controllers: no fancy busses, and very limited memory capacity? Is it important that this product be an -11? If we build the right product here, wouldn't every controller designer in the company use it? If we could build a product that represented the right way to design controllers at DEC, wouldn't the outside world want it? We have an enormous advantage over INTEL in this company in the staff of logic designers we have. This should help us understand what our customers' logic designers really want.

3. Is there a limit short of our ability to design that should restrict the number of products we make (e.g. sales and field service training, spareing, loss of economies of scale, forecast accuracy, thinning of support coverage, ability to communicate with the product lines about the development plan,...).

I believe that focusing on these questions is the prerequisite to useful work on deciding the specifics of product placement.

/gml

PDP-11 is out to take over your plant.

PDP-11/45 and PDP-11/40. The real-time computer systems with all the raw power you could ever need.

All the speed. (Up to 3 million instructions per second on the PDP-11/45.)

All the capacity. (248K bytes main memory, 320 million bytes on disk.)

All the flexibility. Our powerful RSX-11D operating system handles a limitless number of tasks, with over 250 priority levels.

RSX-11D has everything you need to run your whole plant, get all the information you want out of it, and do whatever you want to do with what you've learned.

All for half the cost of plant systems that cannot do nearly as much.

And that's not the half of it.

Even after you've put RSX-11D on your production lines, there's enough power left over to do the other things that need doing. Production reports. Lab testing. Quality control. Inventory control. Management reports. Engineering calculations. Even plant security.

All at the same time. And yet each totally protected from the other by hardware.

RSX-11D is a powerhouse of a real-time system. With dynamic memory and disk file allocation, multi-tasking foreground operation, spooled I/O, and on-line batch processing. But it's a powerhouse that adapts to your needs. With easy FORTRAN IV programming and ISA standard real-time calling conventions.

Last year, our newest PDP-11's took the medium scale computer world by storm. Three months after we introduced them, PDP-11/40 and PDP-11/45 were the hottest computers we'd ever made. And we've made a lot. Over 23,000.

Guess what's going to happen now that they're both available to plants like yours.

Send for the information.

Digital Equipment Corporation, Maynard, Mass. 01754. (617) 897-5111. European headquarters: 81 route de l'Aire, 1211 Geneva 26, Tel: 42 79 50. Digital Equipment of Canada Ltd., P.O. Box 11500, Ottawa, Ontario K2H 8K8. (613) 592-5111.

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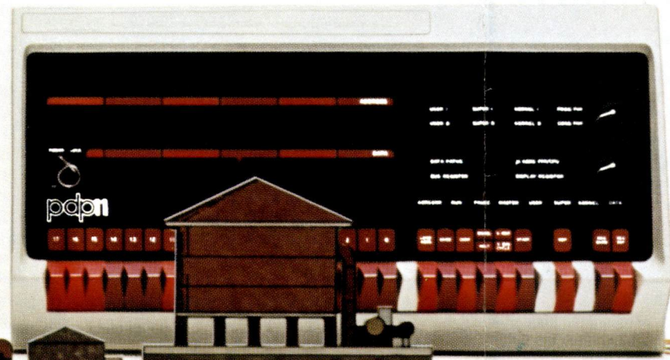


INTEROFFICE MEMORANDUM

TO: Gordon Bell, Lorrin Gale, Bruce Delagi, Chuck Kaman, Ken Olsen, Dave Peters

CC: John Fisher

DATE: October 15, 1973

FROM: Roger Cady

DEPT: Engineering 12-1

EXT : 2328

SUBJ: CONTROLLERS, CABLES, PACKAGING

This memorandum serves as a vehicle for the combining of several ideas on ways to improve PDP-11 peripheral controller packaging, cabling, and hardware. It is the result of discussions with numerous people on various related subjects. It would appear that the goals for any redefinition of packaging should include:

1. Reduced manufacturing costs, simpler configuration rules, fewer parts to stock, etc.

2. Improved testability in the manufacturing phase, improved access and serviceability in the field.

3. Increased reliability--as it relates to cabling, power distribution, simple parts layout, lack of crowding, etc.

4. Improved interconnection method (e.g. improved UNIBUS) where signals travel a better defined pathway.

5. Provision for expansion of system concepts at larger end including multiported devices and memories, wider data bus, etc.

6. Include memory as an ingredient in the concept of flexible peripheral controller configuration.

Part 1 - Backpanel

Two present products help lead the way to improvements. The 8 OMNIBUS and the DD11 concept have proven themselves to be a good way of producing backpanels for smaller logic building blocks. By standardizing the wiring, there is an increase in flexibility without a corresponding increase in costs. Furthermore the packaging of 8's has become much simpler (mechanically) because the pin side of the OMNIBUS need not be accessible. Just compare the 11/05 package to the 8/M.

Standardizing the backpanel also standardizes some test vehicles for module testing. PDP-11 Engineering (Larry Condon) has developed an XOR tester for small peripheral controllers that plug into DD11 backpanels. Increased effort towards standardized testing could pay larger rewards in manufacturing as well as make equipping of field service repair depots much less costly.

Conclusion 1 - Expand and improve the concept of standardized backpanel.

1. Increase size of DD11 type panel to 20 (±) slots.

2. Develop mounting scheme for panel (see Fig.1) which allows easy access to modules, no access to pins, and easy access to power supply electronics.

3. Make panels mount similar to 1943's except recessed for modules--no box or other encumberances. Use the cabinet for the structural support--don't sell except in DEC standard cabinet (short or tall).

4. Use multilayer PCB backplane--control impedance of UNIBUS signals by adjusting line widths and/or glass epoxy thickness. Delete all wiring runs between area A, B and C,D,E,F (vertical along slot). This makes PCB simple.

5. Use PCB to distribute ground, +5. Perhaps also additional voltages via pre-assigned pins (-15, +15, +20, -5).

6. Delete UNIBUS wiring along area A,B. Bus would run in C,D,E,F (1) and out C,D,E,F (20). See companion paper on UNIBUS extensions for use of area A,B. This requires relayout of some existing small peripheral controllers, but this is a minor inconvenience as relayed out controllers will be 100% compatible with old ones.

Part 2 - Controllers

Present small peripheral controllers are successful because they utilize common mounting hardware (above) and because they require no specialized in/out connector mounting hardware requirements for peripheral cables. In general, BERG type headers are mounted on the controller module and the cable is plugged directly in. Major problem areas are, however:

1. Cables tend to get bulky and work loose. This is primarily because there must be slack to facilitate slide-out boxes, and because of inadequate places to tie cables down. The 11/40, 45 box is the best present solution, but far from perfect. Cables work loose from header. No locking mechanism; no cable strain relief. No indexing (polarizing) of BERG type cables.

2. Variety of cables that are required: round, flat, grounded, floating, 4 to 40 conductor. Variety of terminations at far end.

3. Small peripheral controllers easily sit on a single quad module. Complex controllers don't, can't seem to make it on a single hex module. Therefore, some mechanism must be available for handling multiple board controllers in the standardized backpanel.

Conclusion 2 - Improve the existing scheme for handling peripheral control cables.

1. Rigid mounting of backpanel solves many of the cable handling problems. Cables can be routed, and tied, or clamped (Dakcta clamps, please) in place right up to the module, leaving only enough service loop to unplug it from the module.

2. Improve header and mating plug design:

   A. Polarizing notch, pin or other mechanism.

   B. Incorporate the new AMP locking contact into both ends of the plug so that pulling on wires or vibration won't work the connector loose.

   C. Design in a strain relief into the plug so cable is securely fastened.

   D. Pursue conversion to new viking design if that better solves above problems and reduces assembly costs.

3. Standardize a few cables: since the real cost in cables tends to be the termination cost and the inventory cost (too many or too few), we should worry less about wasting a few conductors. Ecologically, this is bad (copper is scarce) but perhaps we should pursue aluminum conductor cables anyway. There is no need to have 4 conductor and six conductor cables.

   A. Define a small, medium, and large round cable for cabling to free standing peripherals. (I.e. TTY, LA30: 8 cond.; Modems: 20 cond; card readers, line printers: 40 cond.) Define the far end connector and buyout peripherals should be so specified. Yes, it will cost us to get the special, but probably far less than our internal costs of not having the right cable.

   B. Define a flat cable (one or two sizes) for internal to cabinet peripheral cabling. Far end terminated like near end.

   C. We should end up with 6 or so cables, in 2 or 3 lengths each for a total of 15-18 cables. We probably now use 500.

   D. We have to look at MASSBUS--as it has unique problems that require additional study.

4. We need to solve the problem of controllers that don't fit into one hex module. The obvious solution is an 8/E over the back connector scheme. This has limitations (interference with die cast handles, serviceability, etc.). Alternatives:

   A. Flat cables like 11/40 CPU. Bad from cable dress and reliability points. Discard this idea.

   B. Build accordian module (Fig.2) with permanent or semipermanent interconnect between boards. Second board may (or may not) plug into the backpanel. Develop new cast "hinge-handle".

Part 3 - Controller Density/LSI

We should be making better use of LSI in controller design. It appears mandatory that we develop some custom chips that help us interface to the UNIBUS and reduce the DIP count on new designs. Such functions as now performed by M105, M7821, M795, M796 modules might well be integrated.

The definition of an NPR/Status/Control Module might be a reasonable approach to the implementation of 2 board (hinged type) controllers where one board is always the same: BUS interface, status, control, NPR, NPG, word count, current address, timeout, parity all included. Then the implementation of a DMA card reader, for example, requires the addition of a unique module that interfaces the CR to this building block--i.e. receives/transmits signals to CR and does code conversion, checking, etc.

Conclusion 3: Develope LSI circuits to aid in interfacing to the UNIBUS. A subsequent paper will define these chips.

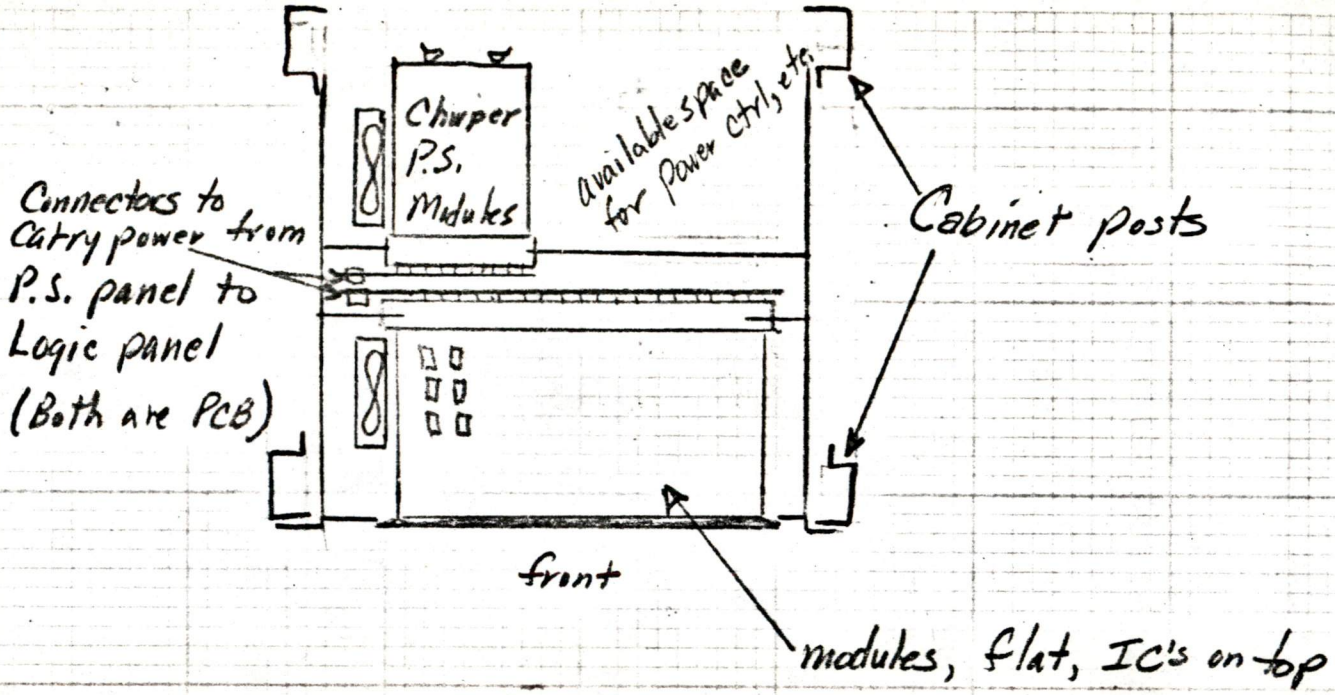
Part 4 - Memory

It is obvious that adoption of a standard panel requires that memory be designed to plug into such a panel. Present core memory designs are not readily adaptable. Semiconductor designs are readily adaptable to such a configuration. Jim Beatty estimates that a 16Kx16/18 bit array with UNIBUS interface and control can fit into a single hex module, using the 4K MOS chips.

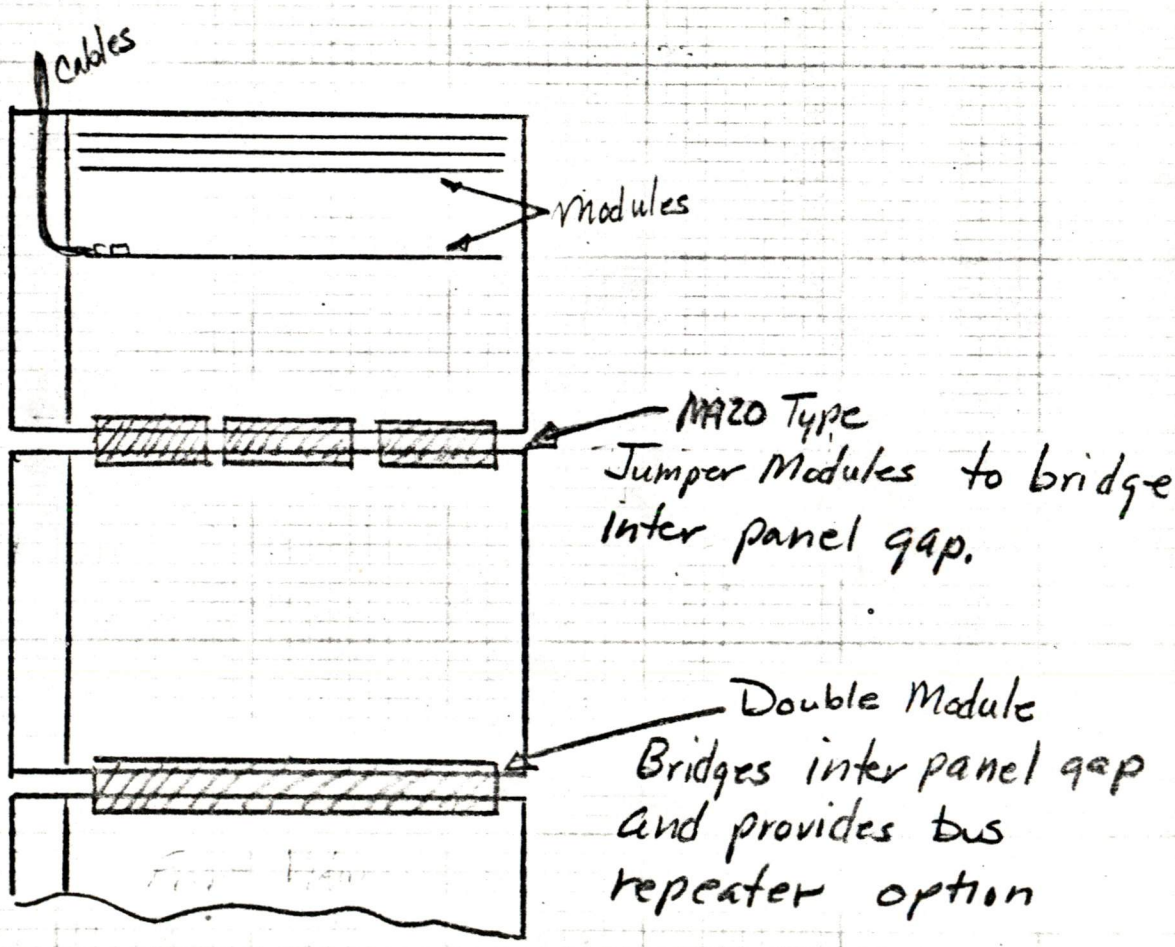
Core memory presents a bigger problem for 16K & 32K sense. These are now multiboard units requiring a special backpanel. It does not seem advantageous to try to "accordian" package a 4 board memory subsystem. Thus, we will probably have to live with a unique backpanel for core. This, however, can have the same mounting as the standard "peripheral" panel since it will be an MLB backpanel, and access to the pins need not be readily available. If necessary, that core mounting panel could be as in Fig. 3, using chirper power units intermixed with memory modules. This allows access to pins from back of machine, but at a lower cabinet density than with power units mounted in back of standard panels.

RC:mjk

Attachments--2



Top View



front view

Figure 1

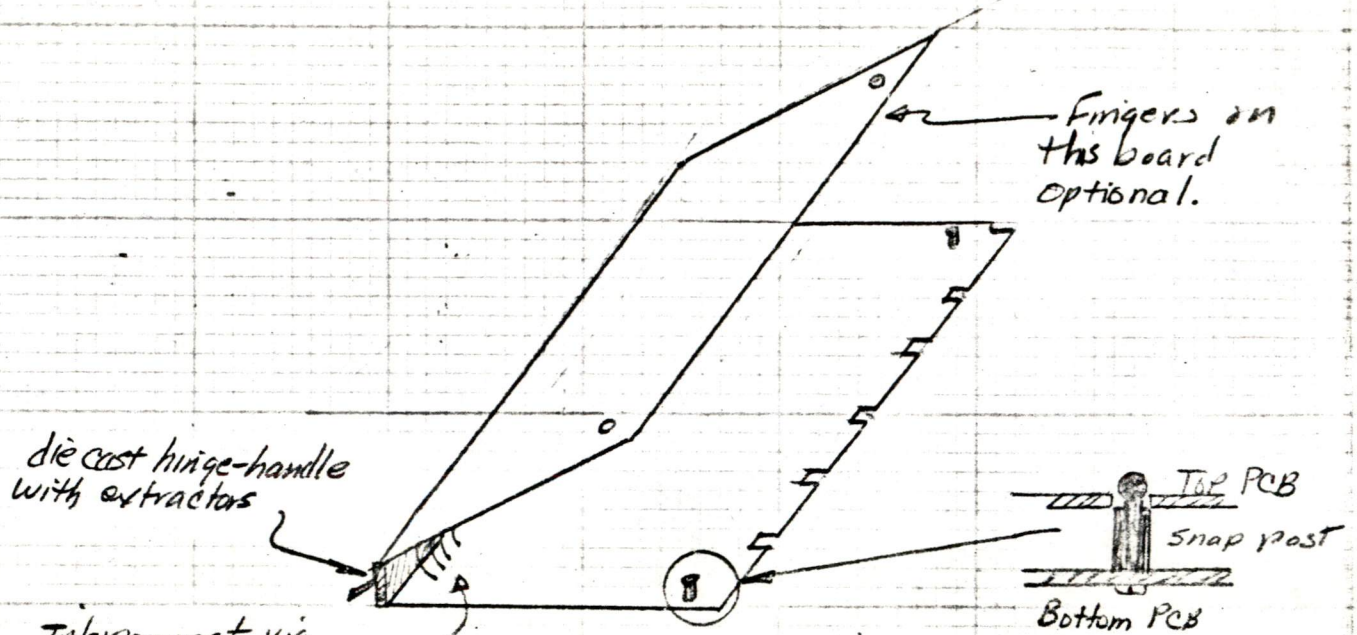


Figure 2

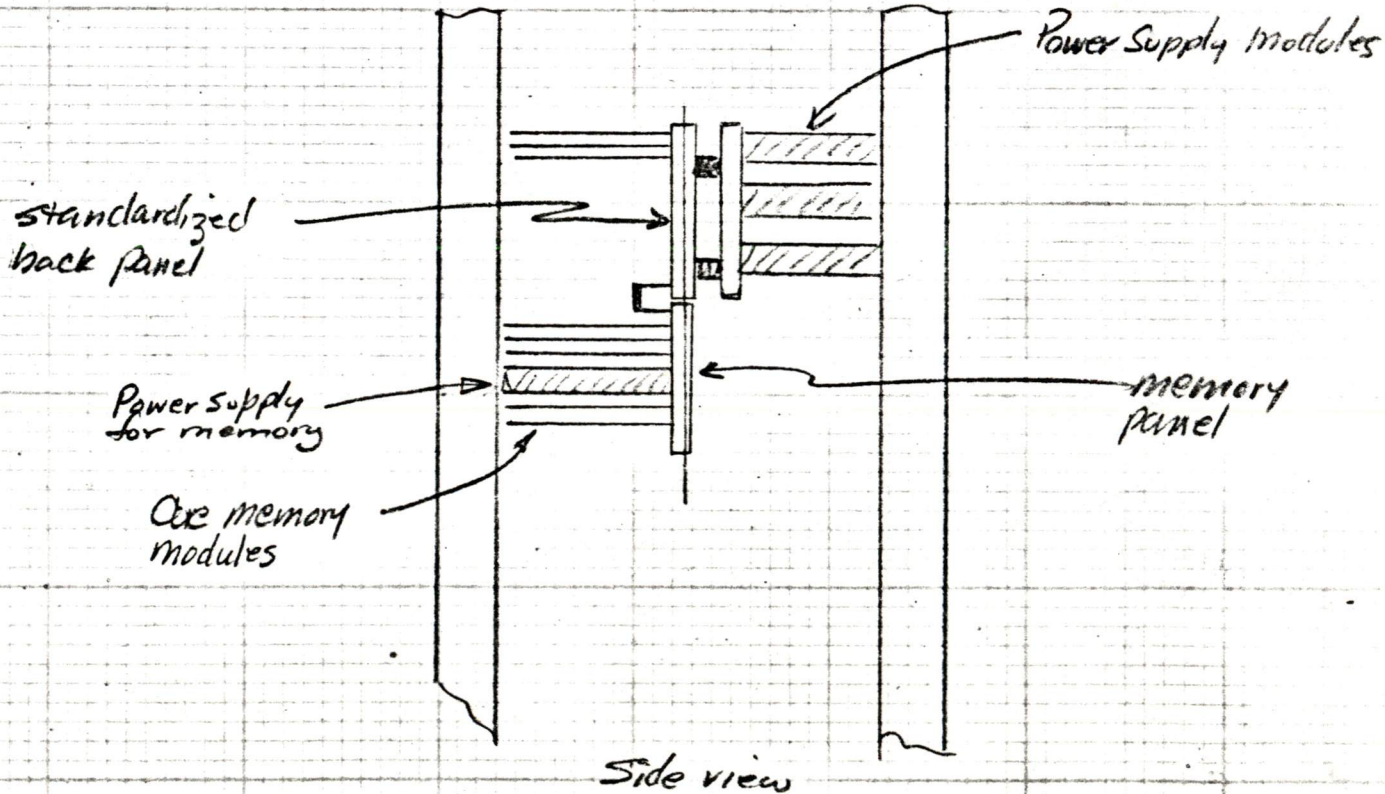


Figure 3

digital INTEROFFICE MEMORANDUM

TO:

DATE: February 7, 1972

2-3

FROM: Larry Portner

DEPT:

SUBJ:

INTRODUCTION

The Operations Committee has asked me to evaluate a PDP-11 group proposal concerning the way we deal with our software products. Presented with the opportunity to evaluate the proposal (prepared by Don Alusic and Bob Anundson), I would like to broaden the scope and reconsider our entire approach to the development and marketing of software-related services.

The concept of treating software like a product has many implications; like the more familiar hardware product, we must be prepared to discuss all the costs, including development (engineering), distribution, installation, and warranty. We must consider the competitive nature of the product. We must define the quality and quantity of our support, and provide the mechanisms for maximizing profits through lower support costs. We should take advantage of the profit opportunities available when additional services are required; we should package the software product modularly so the customer can purchase only what he needs, and we must provide only what has been purchased. We should use our software and related services to enhance our competitive position; we should give our salesmen the flexibility to put together the most effective total package of hardware, software and support.

From a mechanical standpoint, we must provide a uniform product identification scheme that will apply for all products across the company, and can be dealt with uniformly by order processing, the salesman, the customer, the Program Library, Software Support, and other involved organizations.

In summary, we propose to treat software and software-related services as products, and establish the budgetary, financial and organizational basis for doing so effectively.

A review of the broadened proposal is attached; it was prepared by Mel Woolsey, Hank Spencer, David Stone, Dave Schroeder and myself for your consideration.

We propose to treat software and software-related services as products, and establish the budgetary, financial, and organizational basis for doing so effectively, in time to budget appropriately for FY '73. To do so, we must:

1. Work with the Product Lines to establish prices for existing and planned software products.

2. Budget software installation and warranty on the basis of number of units to be shipped and a defined support committment.

3. Establish a uniform product identification system for all products.

4. Create a viable software licensing posture as part of our standard terms and conditions.

5. Establish a subscription service to allow the customers to buy a series of updates, newsletters, and other relevant information.

6. Establish the accounting and administrative systems to track costs, control expenses, and register profits.

What are the benefits?

1. Recover development and support costs by charging for software and related services.

2. Improve our competitiveness in the iron Market by pricing and selling software products and services separately.

3. Quantified support obligations allows minimized support cost, increased profit and better management of support costs.

4. Limit costs of supplying free services and increase profit potential - limit use of software to those who help pay for it.

5. Licensing of software products discourages the plug compatible market.

6. Limit support expenses to those who paid for the license and are entitled to the support.

7. Improve account servicing and responsiveness.

8. Provide modularized expense concept - buy as much or as little as you need: software, hardware, services, systems.

9. Uniform product naming unifies the DEC image.

10. Ordering and order processing is simplified by naming of software products, services and systems.

11. Software-related items can get into the standard waiver system to simplify distribution problems and control them better.

12. Uniform corporate system allows uniform terminology and administration.

13. Provide a financial measure of Programming Dept. performance.

14. Encourage more competitive approach to software development.

15. Encourage optimization of resource allocation to

    testing

    documentation

    support

    customer training

    specialist training

    distribution

    etc.

16. Single individual responsible to Product Line provides focus for negotiation and performance.

17. Simplify Product Line budgeting.

18. Decrease administrative costs.

Potential Difficulties

1. OEM sub-licensing of software may lead to paperwork hassle.

2. Product naming which identifies market group may lead to multiple names for the same product, which would be confusing.

3. Selling to plug-compatible OEMs would be more difficult because of price of software product.

file (3)

digital INTEROFFICE MEMORANDUM

2-3

TO: Gordon Bell
Bob Puffer

DATE: October 17, 1973

FROM: Ken Olsen

DEPT: Administration

EXT : 2300

SUBJ: LONG RANGE PDP-11 PLANS

If the Board of Directors, by some stroke of genius or stroke of stupidity, said by edict that we could only make two PDP-11's two or three years from now, which two machines would we build?

If we then concentrated all our resources on those two machines, like a PDP-11 and 11/45, how cheap and how fast could we make them? How much would we LSI; how much would we concentrate on making inexpensive power supplies? After all these resources are concentrated on these two machines, with this grand, massive effort and all the details from packaging power supplies to LSIing parts of it and to a better interconnection system, would there then be any need for a cheaper machine, a machine between the two, or a machine somewhat more powerful than the biggest one? Might the concentration of engineering and the high production quantity make these so low priced that no one could afford any other machine?

/ma
attachment

digital INTEROFFICE MEMORANDUM

TO: Gordon Bell
Jim Cudmore
Pete Kaufmann
cc: Distribution

DATE: October 2, 1973

FROM: Joe St. Amour

DEPT:

EXT: 2596 LOC: 1-4

SUBJ: OVERALL GROWTH WITH ZERO POPULATION GROWTH

There is an interesting rumor that IBM has a five year plan that calls for a 20% per year growth with zero population growth. I believe that such a plan is possible, and that all growth companies should have long range plans that head in this direction.

However, we haven't even started, we don't have a plan, and our present lack of structure (complete independence) will never let us get there. Maybe we don't want to, but we should at least look.

In my view, the right solution will require total company participation, with across the board compromise and agreement. It probably will even dictate how we organize, how we design product, how we design production/test lines, and how and where we build product.

The solution does violate freedoms which exist today and which are a major reason for our present success. (Will this same freedom limit our potential growth?)

Some of the new requirements are:

1. More standardization - not of today's product/component - but based on a fresh look at the overall situation.

2. More unique equipment for manufacturing - designed to build and test standard units in high volume at low cost.

3. More, longer range Mfg Engineering developments where processes are developed the same way we develop products.

4. An in-depth understanding of total cost. This means look at all overhead expenses, all before and after sale expenses, as well as direct labor.

Some of the new requirements are: (continued)

5. A better understanding of corporate goals, major operating philosophy, major product groupings and constraints (if any).

I believe this is worth pursuing to the point of making a preliminary proposal. I would appreciate your comments.

Distribution:

Operations Committee
Manufacturing Staff
Manufacturing Business Managers
Engineering Managers
Mfg/Eng. Committee
Product Line Managers

NOV 28 1973

digital INTEROFFICE MEMORANDUM

2-3

TO: Dave Thomas, 1-5

DATE: November 27, 1973

CC: Ken Olsen
Andy Knowles
Stan Olsen
Bob Puffer

FROM: Julius Marcus

DEPT: DECcomm

EXT: 3191 LOC: PK3-1

SUBJ: New Memory System for Current PDP-11's

May I encourage you to propose aggressive PDP-11 memory engineering activity to drive down the cost of memory. We are 12-18 months or more away from new family machines. Competition is strong in the form of new CPU/memory systems from D.G., G.A., and Interdata, with more around the corner.

Lowering the cost of memories on the existing 11's can

extend the life of the current machines

give us competitive products in the absence of the new proposed PDP-11's

Memories and packaging are the swing factors in the cost of our systems. Perhaps you could formulate a plan for rushing a memory system into production which would allow further cost reduction in the 16K and 32K versions of the 11/05, 11/10, 11/35, 11/40, and 11/45.

Regards.

mr

12/3/73 G. Bell

2-3

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 24 October, 1973

FROM: Bob Gray

DEPT: 11 Engineering

EXT: 3444 LOC: 1-2

SUBJ:

This compendium consists of:

1) PDP11 Hardware Review Committee 22 October meeting minutes

2) Background Documents for the 29 October meeting
   a) Unibus Parity
   b) Low end TU16

3) Documents describing the current PDP11 planning process.

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 23 October, 1973

FROM: Bob Gray

DEPT: 11 Engineering

EXT: 3444 LOC: 1-2

SUBJ: PDP11 HARDWARE REVIEW COMMITTEE - 22 October, 1973

Present: C. Spector, B. Delagi, B. Gray, L. Wade, L. Hughes, M. Mummolo, D. Finn, B. Savell, C. Ball, M. Tomasic, J. Buckley, P. Laut, A. Psyhogios.

Parity Memory Discussion

Charlie Spector presented a proposal to sell only 18 bit 16K word systems. His research showed a $22 unit cost increase to do this. He cited the following advantages for such a policy:

- easier upgrade to RSX11-D and RSTS
- increased % parity sold
- market gimic to combat foreign add-on

Several questions were raised:

1) Would CPU's (11/40 and 11/45 - YES, 11/05 - NO) support parity?
2) Would RSTS (YES-now!) and RSX11-D (YES-March Phase II) support parity?
3) Would this effect memory production (Bob Gray and Mario Mummolo to investigate).

The Committee approved, in principle, providing production volumn is not effected, selling only 18 bit systems. The Committee also supported the pricing strategy set forth by Charlie Spector and urged its approval by the Products Committee.

10½" PDP11/10 Pricing

Charlie Spector's proposal to price the 10½" 11/10 $300 above the 5¼" version was discussed. The Committee agreed that only the Products Committee had authority to approve prices.

There was controversy over whether the 5¼" version should continue to be made available to End Users.

M. Tomasic - yes - will be required by competition (D.G.)!

Steve Teicher will determine impact on 11/10 production if all end user systems are to be 10½" resulting in converting some 5¼" boxes to 10½" boxes.

The New Generation

Bruce Delagi presented a revised "interesting CPU list"

- Micro PDP11 (20 chip)
- Computer on a Board
- Intelligent Terminal - products?

- 11/05 R - various LSI strategies
- 11/05 Multiprocessor
- 11/40-L-at ½ cost
- 11/40 Multiprocessor
- 11/45 - L - at ½ cost

- 11/45 Mem System - 4X physical space, 32 memory, more I/O bandwidth

- 11/6X - solve virtual address, 32 bits

- KLL10 - low cost

During the next few days the following will be compiled for each alternative

- Mfg. Cost
- Resources Required
- $
- time

The above equipment list will be matched against business product needs in an attempt to narrow down the recommention.

There will be an all Day meeting on Wednesday, November 7th. The goal is: to discuss product alternatives, market segment analyses, and to recommend the best two product strategies (collection of product alternatives).

Memory Group Presentation - Dave Thomas

Dave Thomas gave a briefing on the state of his department. He will be issuing to among others, the HPRC, State of the Art - Memory Report about November 15.

Hanging Issues

1) 18 bit stacks - Will this decrease production output? Bob Gray and Maria Mummolo to report on this after seeing Henry La Mere.
2) Unibus Parity - Bob Gray to present briefing next week.
3) Parity on 11/05 - Steve Teicher will investigate incorporating memory parity support in the 11/05.
4) Bob Gray will get a revised Committee Mailing List together.
5) Steve Teicher - will report impact on 11/10 production if all end user systems are 10½" box.

October 29th Agenda:

1) Unibus Transfer Parity - a status briefing by Bob Gray.
2) Communications and Network Communications Plan by Don Alusic.
3) TM02/TU16 - John Levy and Tony Arrighi will present the feasability report on a cost reduced version. Tentative budget, schedule information will be presented.

November 5th Agenda:

1) Meet November 7th instead .
2) First day of Woods Meeting Agenda.

digital INTEROFFICE MEMORANDUM

TO: PDP11 Hardware Product Review Committee

DATE: 24 October, 1973

FROM: Bob Gray

DEPT: 11 Engineering

EXT: 3444 LOC: 1-2

SUBJ: STATUS OF UNIBUS TRANSFER PARITY

The most recent Unibus parity proposal (September 25) has as a goal to "recover" from transient transfer errors. This requirement implies the creation of a new Unibus signal line and considerable engineering expense. We believe recovery is necessary at the High end for such products as RSTS and RSX11-D.

A subset of this Transfer Parity specification could be created to merely "detect" parity errors. Such "detection" would bring the system to a halt!

The project is essentially on hold, pending the outcome of items 1 through 3 of the 11 October memo and a clearer picture of the Unibus's place in high end systems.

There may be much better places (diagnostics, FA&T procedures, improved FS Training, repackaging, etc.) to spend $100K to $150K to improve PDP11 Availability and that will not decrease performance by 10-20%.

RG/ju

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: 11 October, 1973

FROM: Bob Gray BG

DEPT: 11 Engineering

EXT: 3444 LOC: 1-2

SUBJ: Bus (Unibus) Parity Status and Meeting Notes

This memo relates, in addition to the events of the 3 October meeting, further discussions between myself and Mark Olsen.

An attempt was made to define the "problem" the Unibus Parity was intended to solve. Mark Olsen and I in a discussion following the meeting came to the conclusion that the major problem is MTTR (Mean Time To Repair). We believe that "reliability" is basically an individual system checkout/acceptance function and also a basic engineering design function.

In a brief analysis of the Computer Systems Lab system #7, there were some 5-6 service calls where the system was "intermittent". In each such case, the service time was about five (5) hours. It is this type of failure and resultant down time which strikes fear in the heart of KL1Ø land.

Mark and I further agreed that we had no idea why such problems took so long to repair. To approach this we propose to select a set of intermittent failure reports and debrief the field service representative in each case. We would probe:

approach to the problem
diagnostics used
system access
tools available
what took most time
problems.

Hence vis-a-vis the KL10, we are broadening the focus to better understand the MTTR problem and what really are the constituant parts and problems that can be improved.

In the meantime, several investigations will be performed:

1) Don Vonada - will "voltage margin" individual Unibus lines in an attempt to see if certain signals are more sensitive than others.

2) Don Vonada - will create a data base of "failure rate" (MTBF) at various Terminator voltage values.

3) Bob Stewart - will use the data base created by 2), to predict the MTBF due to "transient" errors on the Unibus under normal conditions (Terminator voltage at +5V).

The results of 3) will provide a measure of the importance of Unibus Parity as a maintenance tool.

4) Bob Stewart - will attempt to find holes in the current (25 September 1973) Unibus Parity Scheme.

Meeting Notes

Mark Olson restated that the KL10 wished to support the eventual Unibus Parity Spec, but that a DEC 1 cutoff date existed.

Steve Teicher asked for the cost in time and dollars to put parity in a device. He further questioned whether parity was the rational approach to the problem. He further questioned the nature of the problem itself!

Several questions were raised about KI/KL10 handling of parity.

a) What does disk do with transfer error?
b) What does mem do with transfer error?
c) What does CPU do with parity error?
d) Was the KI10 mem bus more subject to errors than the Unibus?

The Broader View

It is my belief that the next generation of PDP11 processors will support a bus parity. The form/complexity of the scheme chosen depends on whether the Unibus remains the main system bus for high end products. I suspect that it will not. Further, the Parity scheme needs to take into account the reliability/repairability needs of such Product Lines as Business, Industrial and Communications.

The greater needs should be clearer by early November.

Retraction: Bob Stewart is not the designer or responsible for the M7259 module - as was suggested in the 14 September meeting notes.

BG/ju

digital INTEROFFICE MEMORANDUM

TO: Distribution

DATE: September 25, 1973

FROM: Bob Gray

DEPT: 11 Systems Engineering

EXT: 3444 LOC: 1-2

SUBJ: "Bus Parity for the Unibus" (E20-Ø7521)

Attached is the new Unibus "Bus Parity" Specification. It is a compatible system - both with non parity devices and with Memory Parity Devices.

It is expected that certain ambiguities will be found in the scheme as described here. In addition, the "maintenance mode" description is both preliminary and incomplete.

This document is submitted for review purposes only.

Your comments are requested - either in writing or by phone - Ext. 3444.

CONTENTS

1. Unibus Parity Specification Goals
2. Implications of Goals
3. General Description of "Bus Parity"
4. Maintenance Mode
5. Implementation

Unibus Parity Specification Goals

1) Upward Compatability - The Unibus Parity Specification must allow the free intermixing of devices which do not support Unibus Parity, those that support Memory Parity and those that do support Unibus Parity.
2) Error Detection and Recovery - The Unibus Parity Specification must allow the change in any single bit of the Data or Address or Control lines to be detected. The Specification must allow recovery from the detected error.
3) Decrease Mean Time To Repair - The unit Parity Specification will encourage hardware aids to isolate the cause of Unibus transfer errors.

Implications of Goals

Upward Compatability - is necessary, as we expect mass redesign of all Unibus devices is not possible, and, even if it were, it would not be desirable to restrict "add-ons" to old systems.

Recovery - The more stringent requirement is that the signals allow at least one "hardware controlled" retry of the "Unibus Cycle." This implies that the Transfer Error signal reach the Master during the Unibus cycle that had a transfer error.

There are at least two levels of "recovery". All imply that the Unibus Master be "signaled" that a Bus Transfer Error was detected. At issue is: how soon must the Master be signaled following error detection?

Multiuser systems (RSTS, RSX11-D and KL10) require the ability to recover from transient errors.

This signaling requirement also is required to retry the instruction containing the reference and with any scheme of software check pointing.

An "interrupt" type of signaling would work only where a "system re-boot" procedure was acceptable as a recovery mechanism.

New Unibus Signals - the above two requirements make necessary at least one new signal line on the Unibus. This signal would be the "Unibus Transfer Error" signal. We believe that several new signal lines could be made available by utilizing some of the present "clustered" ground pins. Don Vonada (E20-07519) is committed to determine what,if any, lines could be made available.

Note that this would require changes (ECO's) to Unibus cables, terminators, jumpers, repeaters and all backpanels. (An alternative might be to define a seperate cable assembly/system - designated the "Unibus Parity Bus!")

General Description of "Bus Parity"

The signals BUS PA L, BUS PB L and a new signal BUS TRF ERR L will be used for Bus Parity information. PA asserted by the bus device asserting the Data bits indicates that Bus Parity is being transmitted by that device. PB will be the parity bit. TRF ERR will indicate a Unibus Parity Error.Parity will be computed on the Control, Address and Data signals combined. The parity will be odd.

DATO and DATOB

A. MASTER

The master computes odd parity on the combined Control, Address and Data. It asserts the PA line indicating that the PB line contains the state of the parity bit. It asserts the state of the computed parity bit on the PB line. For timing purposes, the PA and PB lines will be treated as "Data" lines.

B. SLAVE

The slave computes the parity on the received combined Control, Address and Data. It then compares it with the state of the received parity on the PB line. If the computed parity is different from the received parity, a Bus Parity Error has occurred. The Slave will set a "Bus Parity Error" bit in its Control and Status Register. This will also assert BUS TRF ERR L.

On a Bus Parity Error, the slave will capture as much "data received" involving the erroneous transmission as possible. This includes capture of the Control and "Address received" as well as the "Data received." In addition, the Data must not be "accepted" when a Bus Parity Error is detected. It should not pass it on or perform any normal actions on it.

If the Slave is memory, the memory must not modify the location as received Address may be bad.

DATI & DATIP

A. SLAVE

The slave will assert the PA line indicating that the PB line contains the state of the parity bit. The slave will assert the state of the computed (Control, Address and Data) parity bit on the PB line. If, however, the slave is a device equipped with Memory Parity, (memory) and it has also detected a Memory Parity Error, the slave will follow the rules for Memory Parity. That is, it will not assert the PA line and it will signal the Memory Parity Error by asserting the PB line. If the device receives a DATI or DATIP following a DATIP, it must first restore the data to the original DATIP location before responding to the new cycle request.

B. MASTER

The master computes the parity on the combined transmitted Control, Address and received Data. It then compares it with the received parity on the PB line. Note that the received parity has been created by the slave using the Control and Address it received and Data it transmitted. Again, parity has been checked on the

combined Control, Address and Data. Either a change in Control or Address bit - as received by the slave, or a change in Data bit - as received by the master will result in a Bus Parity Error.

Master is NPR device - The master may, at it's option, make one or more "Unibus Cycle Retrys." Failing this, or lacking such direct retry capability, the master will set a "Unibus Parity Error" bit in its Control and Status Register." This, in turn, will in the normal mode of operation cause the device to interrupt to its normal interrupt vector.

On a Bus Parity Error, the master will capture as much "Data received" involving the erroneous transmission as possible. In addition, the Data must not be "accepted" when a Unibus Parity Error is detected; it should not pass it on or perform any normal actions on it.

Master is Processor - The master may, at its option, make one or more "Unibus Cycle Retrys." Failing this, or lacking such a direct retry capability, the processor will set a"Unibus Parity Error Flag"in the PSW and vector thru location 114. The processor should capture the "Data received."

Maintenance Mode - All devices capable of being bus Master must have a facility for "hanging" the system. BUS TRF ERR will be used to hang the system. BUS TRF ERR,and hence the hang condition, will be cleared with INIT.

Implementation

A. The effects of adding signal BUS TRF ERR to the Unibus must be investigated. A particular pin must be chosen.

B. An implementation plan, will have to be created to 1) change the Unibus and 2) have devices redesigned or designed to support the specification.

C. All assemblys, cables and options that interface the Unibus must be ECO'd to make the chosen pin a "signal."

D. New Devices must be designed to the Unibus Parity Specification.

digital INTEROFFICE MEMORANDUM

TO: Bob Gray

CC: Bob Puffer
Pete Van Roekens
Mel Woolsey
Bernard LaCroute
Gerry Hornik

DATE: October 24, 1973

FROM: Larry Wade

DEPT: Software Engineering

EXT: 3689 LOC: 12-2

SUBJ: TU16/RH11 Support

I have discussed the TU16 and RH11 issues with Pete Van Roekens and we can provide the current data at this time.

1. It seems to make sense to support the TU16 and the RPØ4 in the same system at the same time. The 1600 bpi capability is important to backup of the RPØ4.

2. We believe that the TU16 should be supported under RSX-11M, RSX-11D and RSTS/E, in releases which are not scheduled. The individual product managers for these products (Bernard LaCroute for RSX-11M, Mel Woolsey for RSX-11D and Gerry Hornik for RSTS/E) are aware of these devices and are factoring support into their plans.

3. We believe that it is reasonable to design the system software for the RSØ4, RPØ4 and TU16 to operate from a separate control or to allow any mixture on a control and Pete intends to do so. However, we have serious concerns about marketing this capability without a great deal of consideration for the configuration and the application. It is highly unlikely, for example, that a customer could tolerate a TU16 and an RSØ4 on the same control.

4. The project plans will substantiate this direction as they are issued.

LW/kwrc

#930

digital INTEROFFICE MEMORANDUM

TO: PDP-11 Hardware Steering Committee

DATE: October 12, 1973

FROM: Bob Puffer

DEPT: Disk Engineering

EXT: 2863 LOC: 1-3

SUBJ: TU16 Pricing Strategy

The TU16 is a compromise product, just like the TU10. It's not cheap enough for the single drive OEM or lab application; it's not fast enough nor does it have enough features to be ideal for the DECsystem 10. It does, however, fit well into most of our mid-range systems business. Given that we only want to manufacture one ½" tape drive in-house and that we want it to cover the widest possible range of applications, it's a good choice. We can hang on to some of the low-end business because customers want to buy everything from DEC, and we can move it into some of the high-end business strictly on the basis of price.

The TU16 does offer significant improvements in reliability over the TU10. The TU10 has been criticized for excessive maintenance, and I think it is generally recognized that its controllers are pretty sad products. We should be able to sell reliability hard, specifically to those customers who have been critical of our MAGtape products in the past. The TU16 is configured so that nine-track NRZ versions can be field upgraded to 1600 bpi by adding modules to the TM02 formatter box. This feature should also be used as a positive sales tool. In effect, we guarantee an easytransition to higher density recording and protect the customer against obsolescence.

As I see it, the price goals ought to include the following:

1. A TU10 replacement for the single-drive user at a price comparable to that of the TU10.

2. Improved gross margin over the TU10.

3. Better markups than the TU10 (or at least ones that are no worse).

The above implies a low-ball, single-drive system and pricing that gets our margin back on multiple-drive configurations and on the 1600 bpi feature. I would propose one way of doing this as follows:

1. Price the seven-track single-drive system at $11,380 vs. the current $10,745 for the TU10. This is the low-ball and has a lower markup (2.44) than we now have on the TU10 (2.74). But the price is so close we shouldn't lose any business.

2. Price the nine-track single-drive system at $11,595 vs. the current $10,745 for the TU10. The nine-track drive will cost $50 more than the seven-track because the head is more expensive. Also, it's the nine-track drive that offers the field upgrade capability to 1600 bpi, so it should not be hard to get a couple of hundred dollars more for this version.

3. Sell slave drives at $7,605 for the seven-track and $7,820 for the nine-track vs. the current $7,505 for the TU10. Because the TU16 slave drive is about $200 less expensive than the TU10, and because these prices are somewhat higher, our markups would be improved from about 2.5 to better than 2.7. Since slave drives are predominantly used in a large systems environment, getting more money for the product in those markets which are less price sensitive than Lab and OEM makes sense.

4. Price the 1600 bpi PE system (which includes 800 bpi capability - software switchable) at $14,450. This appears to be competitive. A single-drive system would have a 2.88 markup.

5. Sell an upgrade kit for giving nine-track NRZ systems 1600 bpi capability at a price of $2,833, plus field installation charges. This kit would have a markup of 9.68.

6. Put the TU16 on a class 2 discount schedule.

I have calculated the effect of the above prices in the attached tables. In a nutshell, if we could convert between 20% and 25% of our TU16 customers to PE, we would end up with the same margins on TU16 products as we currently have on the TU10 at a substantial increase in our gross margin. Given that IBM is now shipping about 80% PE to 20% NRZ drives, I think that 25% conversion is a very conservative short-term goal (within six months). I would further expect that this percentage would grow significantly during the next two years to better than 50%, and as it grew our margins would continue to improve because of the more favorable mix. By selling nine-track NRZ drives with an upgrade capability, we would also have created a substantial add-on business for PE upgrade kits. This would be a very lucrative captive business, given its markup of 9.68.

This is not intended to be an "aggressive" strategy. We won't pick up a lot of new low-end business. What we should be able to do, however, is to hang on to our TU10 base (400 per quarter) and phase out the TU10 drive, pick up some 1600 bpi incremental business, improve the reliability of our tape products in the field, and create a potential market for profitable add-on drives and upgrade kits. We would also have succeeded in increasing the number of RH11 Massbus controls in the field. These

are a target for add-ons of our other Massbus peripherals when we develop software that allows us to mix different devices on the same control. Although this is not a feature we can push at this time, it certainly is something we want to push in the future. I have not considered the reverse problem of pricing a TU16 drive and formatter to be added on to an existing RH11. We do need to face this issue now, however, or risk having a set of inconsistent prices when we start selling mixed devices on the same control.

The attached tables are a summary of cost and markup calculations.

leb
Att.

C-Bob Peyton
Andy Knowles
Bill Chalmers
Ron Bingham
Ulf Fagerquist
Jim Willis
Bill Long
Ed Kramer
Dick Clayton
Brad Vachon
Win Hindle

Bob

TU16 Pricing Proposal

R. W. Puffer
Oct. 8, 1973

(FY74 Standards)	Cost TU10/TM11	Sell TU10/TM11	Markup	Cost TU16/RH11	Sell TU16/RH11	Markup	Δ GM	Markup
7 Track Drive	2948	7505	2.55	2780	7605	2.74		
9 Track Drive	3008	7505	2.50	2830	7820	2.76		
NRZ Control	1220	3240	2.66	1886	3775	2.00		
PE + NRZ Control	--	--	--	2181	6630	3.04		
(Gross Margin) 7-Track System (Single Drive)	(6577) 4168	10745	2.58	(6614) 4666	11380	2.44	37	-.14
(Gross Margin) 9-Track System NRZ only (Single Drive)	(6517) 4228	10745	2.54	(6879) 4716	11595	2.46	362	-.08
(Gross Margin) 9-Track System NRZ & PE (Single Drive)	--	--	--	(9439) 5011	14450	2.88	2922 (over NRZ)	+.34 (over NRZ)
Upgrade Kit - Adds PE to NRZ 9-Track Drives	--	--	--	(2560) 295	2855* + Field Installation	9.68	--	--

(Costs include complete checkout of PE and removal of working modules)

*We must price spare modules so their sum is greater than the price of this kit.

Assume the sale of 100 one-drive systems - -

-NOW

25% -7 Track Cost/Sell	75% -9 Track Cost/Sell	Total Cost/Sell
104,200/268, 625	317,000/805,875	421,200/1,074,500
		2.55 Markup

Becomes

20% -7 Track Cost/Sell	50% -9 Track Cost/Sell	30% -PE Cost/Sell	Total Cost/Sell
93,320/227,600	235,800/579,750	150,330/433,500	479,450/1,240,850
			2.59 Markup

Or

20% -7 Track	55% -9 Track	25% -PE	
93,320/227,600	259,380/637,725	125,275/361,250	477,975/1,226,575
			2.57 Markup

Or

20% -7 Track	60% -9 Track	20% -PE	
93,320/227,600	282,960/695,700	100,220/289,000	476,500/1,212,300
			2.54 Markup

Markup on TU16 at assumed prices is better than markup on TU10 if more than 20% of the drives get sold with PE.

digital INTEROFFICE MEMORANDUM

TO: PDP11 Hardware Products Committee

DATE: 24 October, 1973

FROM: Bruce Delagi BD

DEPT: 11 Engineering

EXT: 3563 LOC: 1-2

SUBJ: 11 PLANNING PROCESS

There seems to be confusion concerning the details of the current 11 Planning Process. To clarify, Dave Stone, Lorrin Gale and I have cooperated in laying out:

1. Technical subcommittees to hash out issues like:
   - virtual addressability - how clean can a PDP-11 architectural enhancement solution be?
   - multiprocessors and RSX11D/RSTS operating system enhancement - is there something easy to do that provides significant improvement?
2. Responsibilities to people charged with documenting (in a specific manner) alternative product proposals - using the output of the above subcommittees.
3. The gathering of shareable, discussable market/product inputs from the product lines.
4. Responsibilities to specific people to perform a competive analysis of DG, Varian, Datacraft, GA, CA, HP, SEL, Burroughs, Modcomp, XDS, Interdata, IBM, and CDC.
5. A pre-woods (all day) meeting on November 7 with the 11 Hardware Products Committee and others to discuss product alternatives, market analysis and competitive data as gathered above, to identify questions needing answering, and to focus further work on the 2 most interesting product strategies.
6. A woods meeting on December 12 and 13 to pass through the digested data from above in the light of two alternative strategies selected above and to make a final selection of the products that will be developed.

Attached are documents relative to each of these items. Comments are welcome.

digital INTEROFFICE MEMORANDUM

TO:

DATE: 24 October, 1973

FROM: Bruce Delagi BD

DEPT: 11 Engineering

EXT: 3563 LOC: 1-2

SUBJ: INPUTS TO THE 11 PLANNING PROCESS

There are 3 categories of input to the 11 plan:

1. Product line analysis by market segments: DEC penetration of the market segment, rate of growth of segment, DEC's planned rate of growth in the segment, and the single product (system) that will do most toward achieving this planned rate.

2. Some interesting product proposals:
Product goals, system configuration, system manufacturing cost, development time, development budget (with manpower assumptions), dependencies on other projects underway, applications of this product, and the problems in current offerings that this product overcomes. This is all derived from the data put together by the technical task forces on:
   a. Multiprocessors for operating systems enhancement - (Craig Mudge)
   b. Virtual and physical addressability, caches and bus bandwidths - (Bob Stewart)
   c. User microprogramming and instruction set enhancements - (Jim O'Loughlin and Jack Burness)
   d. Reliable computing - (Chuck Kaman)

3. Competitive Analysis
What products do our competitors have now? What resources do they have to develop new products? What direction do they seem to be pursuing? What rumors are afloat? What markets does the competitor now own? What markets are we losing to them that we now own? How equipped are they to compete in the iron vs. OEM systems vs. end user business?

digital INTEROFFICE MEMORANDUM

TO: J. Meany
C. Spector
B. Vachon
J. Marcus
I Jacobs
D. Clayton

DATE: 11 October, 1973

FROM: Bruce Delagi

DEPT: 11 Engineering

EXT : 3563

SUBJ:

In order to guide the PDP-11 development groups in proposing PDP-11 product strategies, Dave Stone and I are asking your help in understanding your business and business plan. The best communication method seems to us to be a description of each of the (up to 5) major segments of your business and for each of these segments:

- the current growth rate of that segment in the industry as a whole. (dollars)
- the percent of that market segment that DEC currently owns (dollars)
- the percent of that market segment that you plan to own for DEC in calender 1976 (dollars)
- the PDP-11 centrally funded product (system) development that will do most toward helping you achieve that plan.

Please organize this data as one typed sheet per segment. Dave and I are planning to allocate time on the first day of the PDP-11 Woods Meeting (October 31 and November 1) for your presentations of this information to the assembled group. Delivery of these sheets to Judy Underwood by 22 October will permit inclusion in the Woods Meeting Package. Allowing people to think about this information and product alternatives before such a meeting turns out to be one of the best ways to ensure informed discussion and good decisions (ones we can stick to). Please help:

1 sheet per market segment
22 October, Judy Underwood, 11 Eng. 1-2

digital INTEROFFICE MEMORANDUM

TO:

DATE: 24 October, 1973

FROM: Bruce Delagi BD

DEPT: 11 Engineering

EXT: 3563 LOC: 1-2

SUBJ: PDP-11 PRODUCT ALTERNATIVES (FORMAT)

So that all product proposals answer the same questions, I'd like to state the topics that should be discussed for each proposal:

1. Product goals - what should the product be to be successful? (e.g. solve virtual address problem, cost 1/2 current 8K 11/05, . . .)
2. Product (system) configuration. Show design center and minimum system.

   Primary Storage - how much.

   CPU - architecture, add R, R time.

   Secondary Storage - how much, access time, transfer time, modularity.

   Language Processors - FORTRAN, COBOL, RPG, ALGOL. Optimized for . . . diagnostics compile time execute time, execute space, size of compiler (for how many symbols); Size of runtime system; total size of compiler (including overlays).

   Operating System - optimized for task latency, throughput, or terminal response time? Core resident requirements, total size, disk storage requirements including all utilities and language processors.

   Terminal(s) - diagnostic load capability, off-line capability, hard copy, fonts, baud rate (burst and sustained).

   Communications Interfaces - number, special communication features, thruput goals.

   System Back-up Device - What is it? Is there one?

   User Back-up Device - in a multiuser system, how does a user assure that his work is preserved?

   Other I/O - line printer, card reader . . .

3. System manufacturing cost - separate out system components and include 12% of component cost as systems integration cost or demonstrate why it will be lower.
4. Development time, budget and manpower assumptions - if proposal counts on other projects underway, so state.
5. Applications of this product (including software applications that we can build on this product).
6. Problems in current offering that this proposal overcomes.
7. The weaknesses in this product proposal.

Each proposal should have a summary 1 page cover sheet that addresses the 7 areas above.

Product alternatives will be pulled together as follows:

Controller (20 chip cpu with memory and serial bus) - Steve Teicher
Computer on a Board - Bob Gray
11/05 R - Steve Teicher
- no LSI (pull off TTY & line clock)
- LSI Unibus control logic in cpu (only)
- LSI data path and data path control
- LSI both arithmetic and Unibus portions of the machine.

Smart Terminal - Bob Gray
Cheap 11/40 (3 boxes) - Jim O'Loughlin
Souped up 11/40 w/Schottky and cache - "40S" - Chuck Kaman
11/40 or 11/45 multiprocessors - Pete vanRoekens
11/45 Memory System (physical address space, bandwidth (IO and mem) - Bob Stewart
"Easy" extension of 11 architecture to 32 bits - (32 bit arithmetic, 24 bit virtual space) - Larry Wade
KL1ØL = Len Hughes
PDP-1Ø w/o cache option
PDP-10 w/cache option
Schotky PDP-10 w/cache option

Summaries are due 31 October at 12 noon. They should be brought to Bob Gray in 11 Engineering.

digital INTEROFFICE MEMORANDUM

TO:

DATE: 24 October, 1973

FROM: Bruce Delagi

DEPT: 11 Engineering

EXT: 3563 LOC: 1-2

SUBJ: 11 COMPETITIVE INFORMATION

To structure the competitive information input I'll lay out the questions we will answer:

For each competitor:

- what markets is the competitor in?
  - what share do they have of these markets (0-20%, 20-50%, 50-80%)
  - are they growing faster than us in those markets (where are we losing ground)
- what are the sales of the competitor (computer division) last year.
- how equipped are they to compete in the iron vs. systems business.
- where is the competitor putting its development efforts
  - what products are they selling now
  - what have they announced recently (are they going to be a technology threat)
  - rumors?
  - how much development dollars did they spend last year (products = operating systems, languages, and hardware).

This information should be on 2 sheets per competitor. The first sheet should hold the answer to the first 3 (market oriented) questions and the second sheet should hold the answer to the last (product oriented) question.

This competitive information will be developed by:

DG - Jack Burness
Varian - Gerry Dulaney
Datacraft - Dan Riordan
GA - Dave Best
CA - Mike Tomasic
HP - Dan Riordan
SEL - Bill Kieswetter

Burroughs - Dan Riordan
Modcomp - Dan Riordan
XDS - Bill Kieswetter
Interdata - Dave Stackpole
IBM - Larry Wade
CDC - Dan Riordan

Competitive sheets are due 31 October at noon. They should be brought to Bob Gray in 11 Engineering.

digital INTEROFFICE MEMORANDUM

TO:

DATE: 24 October, 1973

FROM: Bruce Delagi BD
David Stone
Lorrin Gale

EXT: 3563 LOC: 1-2

SUBJ: PDP-11 WOODS MEETING AGENDA

The PDP-11 Woods Meeting will be on December 12 and December 13, beginning at 8:30 am December 12 and at 12:00 (for lunch) on December 13 for all attendees. (Development groups will caucus from 8:30 to 12:00 on December 13. It is our intention to focus on long range issues in the 2-5 year time frame. We see this meeting as helping us to set directions for our organizations both in terms of projects and organization structure.

Wednesday, December 12

8:30 - 11:00 - PDP-11 Development Strategy: Alternative Products
(Chairman - Bruce Delagi)

A presentation by development managers of product possibilities. For each product proposal, data should be provided on:

- goals
- system configuration - cpu, primary & secondary storage, operating system, languages, terminal(s), communications interface, system backup device, user backup device, other I/O (line printer card reader).
- system manufacturing cost - separate out system components, include 11% of component cost as system integration cost (or demonstrate why it will be lower).
- development time, budget, and manpower - if proposal counts on other projects underway so state.
- applications of this product (including software applications that we can build on this product).
- problems in current offerings that this proposal overcomes.
- weaknesses in this product proposal.

11:00 - 12:00 - Product Line Presentations (Chairman - David Stone)

Ten minute presentations by:

J. Meany, OEM	J. Marcus, Communications
C. Spector, LDP	I. Jacobs, Business
B. Vachon, IPG	D. Clayton, Computation, Education, 11/45

"For each of the (up to) 5 major segments in my business

- current growth rate of that segment in the industry as a whole
- current percent of the market owned by DEC
- planned percent of the market owned by DEC in 1976
- the single product development that will do most toward achieving this plan".

Discussion will be limited to questions for clarification. Handouts (1 page per segment) will be distributed with the meeting package.

12:00 - 1:00 - Lunch.

1:00 - 2:00 - PDP-11 Development Strategy: Alternative Strategies (Bruce Delagi)

A short presentation of alternative combinations of proposed products. For each strategy there will be:

- a summary resources drain
  - totals
  - allocation between "high", "middle", and "low"
- effect on the timing of the next architecture
- effect on the PDP-10/PDP-11 "GAP" ("overlap?")
- strengths of the strategy
- weaknesses of the strategy

2:00 - 5:00 - PDP-11 Development Strategy: Discussion (Chairman, D. Stone)

Product alternatives not mentioned
Strategy alternatives not discussed
Questions, Answers, Opinions
Roundtable on views

Thursday, December 13

8:30 - 12:00 Development Group Caucus
- did we hear any consensus? Did we think/hear of new strategies and products? Do we have a strategy to recommend based on what we heard?
- Generate new data as appropriate

12:00 - 1:00 Lunch

1:00 - 2:00 - Networks Presentation - J. Marcus, D. Alusic
The networks strategy and alternatives generated by the Networks Committee
- how rapidly is "networks" growing
- which market areas are most affected?

2:00 - 3:00 - Applications not tools - D. Stone
To what extent are we going into the complete, turn key system business?
What are we going to do this time better than last time (when we blew it)?

3:00 - 4:30 - Planning, Management, and Review Processor: Discussion (chairman, D. Stone)

4:30 - "What I heard" - brief summaries to improve accuracy of communication

D. Clayton	J. Marcus	A. Knowles	B. Puffer
C. Spector	B. Vachon	W. Hindle	
J. Meany	I. Jacobs	G. Bell	

PDP-11 MICROPROGRAMMING

J.F.O'Loughlin

I. PDP-11 ARCHITECTURE (BACKGROUND)

- A. UNIBUS Interface
  - 1. Separation of Machine Elements
  - 2. Strength of a Common Interface Specification
- B. Instruction Set
  - 1. Multiple Address Modes
  - 2. Multiple Register
  - 3. Multiple Word Instructions
- C. System Stack
  - 1. Subroutine and Instruction Usage
  - 2. Interrupt Usage

II. MICROPROGRAMMING

- A. General Comments
- B. Specific Application to PDP-11 Processors

III. DESIGN GOALS

- A. PDP-11/20
- B. PDP-11/40
- C. PDP-11/05
- D. PDP-11/45

IV. MICROPROGRAMMING DESIGN TOOLS

- A. Breadbroad
- B. Software
  - 1. Debugging
  - 2. Documentation
- C. Simulator for Floating Point

V. IMPLEMENTATION

- A. PDP-11/20
- B. PDP-11/40
- C. PDP-11/05
- D. PDP-11/45

} Data Path & Micropath together; Number of general registers, states; Commentary on microword relationship to data path!

- E. Summary Charts
  - 1. Processor State Complexity
  - 2. IC Count
  - 3. Microprogramming Characteristics

VI. MICROPROGRAM EXPANSION

- A. Integral - PDP-11/40
  - 1. Expansion Instruction Set
  - 2. Floating Instruction Set

B. Separate - PDP-11/45 FPP

VIII. SUMMARY & CONCLUSIONS

A. Design
   1. Procedural (Segmentation)
   2. Developmental (Data Path & Flow Diagram)
   3. Documentation

B. Product Hardware
   1. Microprogramming Relationship to Design Goals
      a. PDP-11/40
      b. PDP-11/05
      c. PDP-11/45
   2. Size - Module Number
   3. Production
      a. Uniqueness of PROM's & ROM's
         1. Trade off between the two.
         2. Vendor delivery problem.
      b. Engineering changes
      c. Training

MICROPROGRAMMING THE PDP-11's

J.F.O'Loughlin

INTRODUCTION:

The recent microprogramming of three PDP-11 machines provides a unique opportunity to review the effects of microprogramming on a fixed architecture machine. Three separate design groups were involved (PDP-11/05, PDP-11/40, and PDP-11/45) each with specific design goals. Central to each of these efforts was the absolute requirement for common (or subset) software, common peripherals, and a background of common corporate resources and hardware. Comparisons are made to the original non-microprogrammed PDP-11/20 machine.

A total hardware development and implementation viewpoint is attempted. Microprogramming may reduce the size of a machine, alter its data paths or increase its speed; it can also alter the techniques of project documentation and development. The microprogramming impact is placed in perspective; it is a major element in the design of the new machines but it is not the only element. The continued development of denser integrated circuits is important; so also is the altering application of the machine which in turn affects design goal. The minicomputer is not theoretical; it is pragmatic both in application and design. This paper is so presented. The choices made for the PDP-11's may be right for them, but may have other meanings in another or future design.

PDP-11 ARCHITECTURE:

The fixed architecture under consideration is that of the PDP-11; three salient features should be noted: the UNIBUS[R]; the Instruction Set with multiple address modes and registers; and the System Stack for subroutines and interrupts.

R Registered Trademark of Digital Equipment Corporation

The UNIBUS provides the interconnection between components of the computing machine in Figure 1. This interconnection with its attendant specifications provides both a physical and logical discipline among components. Physically the UNIBUS provides signals consisting of: data; address; data control; bus ownership control; and power on-off control. The data transfers are asynchronous with interlocking control signals; four types of transfers can be initiated by a bus master device (DATA IN, DATA IN PAUSE, DATA OUT and BYTE DATA OUT). Note that bus mastership is required for data transfer and can be provided for any element on the UNIBUS , not just the processor. The processor, however, does have a slightly greater than equal role on the UNIBUS , it contains the logic that arbitrates the bus ownership. Two classes of non-processor ownership are provided: Non-Processor Request (Direct Memory Access) which occurs throughout processor operations; and Bus Request (usually effecting Interrupts) which occurs only at instruction completion and depends upon peripheral request priority versus program priority.

The discipline of the UNIBUS specification requires some logic cost within each system component; this cost, however, is well returned in the generality of the component interfaces. Specialized I/O instructions are not needed as I/O device registers (control and storage) occupy normal UNIBUS address space. Direct Memory Access transfers occur directly between the participating devices (disk and memory, for example) without processor interaction. Subsets of UNIBUS control are allowed; some devices are only master (processor registers) or slave (memory); others devices only acquire bus control for INTERRUPT operations. This flexibility accommodates the need for minimum logic and cost in some peripherals and allows power and speed in others. The various new processor accommodates the UNIBUS specifications in different ways - each meets the specification but implementation and speed may differ.

The Instruction Set of the PDP-11 machines is relatively strong and diverse. Over 400 instructions exist with their major characteristics as follows: multiple address modes; multiple general purpose registers, double and single operand instructions, byte or word operation, processor status word, and a predilection for stack operations. Figure 2 indicates the double and single operand instructions in reference to the address modes and general registers. Instructions can involve Register to Register, Register to Memory, Memory to Register, or Memory to Memory operations. Of special value is the inclusion of the Program Counter (PC) and the processor Stack Pointer (SP) within the General Registers; this allows relative and system stack ordered instructions. Most instructions provide for word or byte operation with the processor monitoring byte operations and odd address utilization. Bus errors (odd address, stack limit or non-existent memory) result in specific trap responses. A portion of a Processor Status word provides for a number of Branch Instruction conditions by storing characteristics of the last instructions data; the word also contains program priority to determine bus ownership upon peripheral bus request.

A system stack accommodates both subroutine response and processor interrupt response; processor trap instructions also utilize this stack. The specific sequence of operation for the Jump to Subroutine, Return from Subroutine and Interrupt response are noted in Figure 3. The Subroutine instructions use of the linkage register (RX) provides for arguments or addresses of arguments; the use the system stack (SP) allows nesting of subroutines and interrupts. The Interrupt response indicates the transfer of both the Program Counter (PC) and the Processor Status (PS) word to the system stack. The new PC and PS comes from the peripheral transmitted vector address and allows a change in program operation and the priority of program operation.

MICROPROGRAMMING:

Microprogramming as a concept for machine implementation was noted in 1951 by Professor Wilkes. Initial implementations were upon the larger machines with a variety of control store devices. At Digital, the medium sized PDP-9 machine used a magnetic E core implementation for its control store. Widespread use of microprogramming in the minicomputer field came only after Large Scale Integrated (LSI) circuits provided Read Only Memory (ROM) and the related Programmable Read Only Memory (PROM). These devices allow a direct, practical application of the economical advantages of LSI without the design time and cost requirements of custom LSI. Only the ROM pattern needs to be custom, the basic integrated circuit layout is standard and uniform. These devices provided the starting point for microprogramming the PDP-11 machines.

Given the means for economical microprogramming, should PDP-11's be done that way? The PDP-11 machines are strong yet complex, with this complexity providing the threshold for consideration of a microprogramming design. The Instruction Register operation code is not specifically laid out for microprogramming, but generalities exist in the format for the address modes. The asynchronous nature of the UNIBUS data and ownership transfers appears neither for nor against microprogramming; however, the separation and generalization of UNIBUS elements with defined interfaces is very characteristic of the microprogramming design concept. The need for optional, incremental expansion lends itself to microprogramming.

DESIGN GOALS:

The design goals for the machine provide a necessary reference for interpretation of the existing designs and the microprogram application to those designs. Note that microprogramming is not noted as a goal, it is an unspecified technique.

The PDP-11/20 primary design goal was for a fault free implementation of a lasting architecture. The implementation utilized off-the-shelf components. No major use was made of LSI or MSI components.

The PDP-11/40 is the follow-on machine for the PDP-11/20. Its major goals are improved price (less than a PDP-11/20) and performance (Register to Register operations in less than a microsecond) with optional, incremental expansion.

The PDP-11/05 is a minimum logic implementation with the belief that such an implementation is low cost. Some original effort was directed at a single module board design of a PDP-11 subset or a non-PDP-11 machine. Software and peripheral costs, however, require a PDP-11 machine and the present two board machine resulted with low cost, and consequentially low speed, the criteria.

The PDP-11/45 is a state of the art machine specifically designed to provide raw computational power. Both MOS and Bipolar semiconductor memory are provided with a separate Floating Point Processor. Cost was not an originally specified item with multilayer logic boards and high speed Schottky logic always considered necessary.

MICROPROGRAMMING DESIGN TOOLS:

A major microprogramming design tool is the computer driven Read/Write Control Store of Figure 4. A bipolar scratch-pad type memory interfaces to the processor breadboard; the word width and depth is that of the control store for each machine. The processor breadboard provides the micro address and control for the read only interface to the breadboard. Input and change for the control store comes through the UNIBUS interface to the PDP-11/20 system. This system is supported by Teletype, Paper tape and software.

Two types of software are provided: on-line debugging programs; and documentation programs. The on-line debugging program allows examination and modification of the breadboard control store. Input commands and data are checked, paper tape output is provided for generating Programming Read Only Memories (which then can be used as masters) and for generation of machine and IC documentation. Machine documentation is generated on a PDP-10, System 40 machine. Programs allow: the conversion of the PDP-11 papertape to a standard ROM (256 words X 4 bits) format; the generation to complete microflow for machine documentation; and the ability to edit for engineering changes.

A design tool enhanced by microprogramming was a simulator of the PDP-11/45 separate Floating Point Processor. With the data path and control strongly characterized by the microprogram flow diagrams, each register could be assigned a program memory location and each microtransfer directly simulated.

IMPLEMENTATIONS:

PDP-11/20 - The block diagram of Figure 5 indicates the simple nature of this original PDP-11 implementation. The Adder has latch registers on each input with a separate output register for Bus Address storage. The Scratch Pad general registers receive their inputs from the Adder output and provides output to each Adder input. A figure eight data path exists between the UNIBUS , the Adder, and the Scratch Pad.

Control for the data path comes from combinational logic decoding shift registers containing machine states. Four types of state information are utilized: major machine state (Fetch, Execute, etc.); instruction states within the major machine states (ISR1, ISR2, etc.); bus control states within instruction states (BSR1, BSR2, etc); and the Instruction Register decode. Usually four to six gate levels exist between the shift registers and the control signal to the data path.

PDP-11/40 - The block diagram of Figure 6 directly concerns itself with speed, generality and some economy. Register to Register transfers that require the loading of both Arithmetic Logic Unit (ALU) inputs with Scratch Pad Memory information and UNIBUS data are accommodated by direct paths. The need for a UNIBUS address to quickly initiate bus operation is accommodated by direct path to the Bus Address Register from the ALU output and the Scratch Pad Memory. The location of the Scratch Pad Memory between an outgoing data bus (DMUX) and an ingoing data bus (BUS D) allows the further addition of other memory or processing elements; this important generality allows expansion. The data struction while more complicated than the PDP-11/20 still is economically tuned to data interaction with core memory on the UNIBUS.

Direct microcontrol is exerted upon the Data Path for the multiplexors and Scratch Pad Memory selection; a single logic gate level is required for clocking signals. Only a small portion of the microcontrol word is used indirectly through decoding, these fields relate to constant generation or alteration of Arithmetic Logic Unit response as a function of Instruction Register decode. The minimum loop time (140 nanoseconds) for microword control (address, microdata output, buffer loading) matches the time for the most cirtical data path transfer (Scratch Pad Memory to the B Register at the ALU input). Different microtiming cycles are also provided for arithmetic operation through the ALU (200 nanoseconds), and for complete data cycles from the Scratch Pad Memory, through the ALU and back to the Scratch Pad Memory (300 nanoseconds). The microword is buffered so that next word look-up can occur during present word operation. The next microword base address is provided completely by the present microword; branching information inputs to the NOR gates prior to the microword buffer. This branching input location requires that branch conditions be specified by the microword, one microword before the branch.

PDP-11/05 - The block diagram of Figure 7 reflects economies in the number of data paths and data registers. Operations performed directly in the PDP-11/40 and PDP-11/45 often require two or more cycles. The Scratch Pad Memory must pass data through the Arithmetic Logic Unit (ALU) and output multiplexor to load the B Register on the ALU inputs. Byte operations for data justification require several rotate operations instead of a single swap operation. The UNIBUS interface is similar to that of the PDP-11/20. A separate Bus Address Register is provided, but data outputs require the holding of data through the ALU and its input registers. The emphasis is on economy with time being the major sacrifice.

The microcontrol of the PDP-11/05 continues these economies. The microword is used directly from the Read Only Memory; no buffer register is provided for the data protion of the microword. The microword access time is accommodated with the data operation time in the total microcycle time (300 microseconds). Fewer data path elements result in fewer microcontrol bits.

PDP-11/45 - The block diagram of Figure 8 is complex with multiple interconnections and multiple registers for speed. Two copies of the Scratch Pad Memory allow direct and simultaneous input to the Arithmetic Logic Unit (ALU) for register to register, double operand instructions. Other duplicate registers are also provided for the Instruction Register, the Program Counter and the data registers, B Register and B Register A on the ALU input. Multiplexors allow the direct transfer of data usually requiring multiple data cycles in other machines; hardware is exchanged for time. Some of the multiplexors receive and transfer data to the semiconductor memory bus with most of the data path optimized to the cycle time of these high speed memories.

The extra logic elements in the data paths would require excessive time were it not for the use of Schottky integrated circuits. These high speed gates reduce throughput delay time, but require the use of multilayer circuit

board with internal ground planes, restricted signal length, and terminators on some signal lines.

The microcontrol section of the PDP-11/45 processor utilizes a buffer register on the Read Only Memory (ROM) for speed. The microbranching network alters the base microaddress before the buffer register; because of multiple timing states the branch is called within the word preceding the branch. The CONTROL BUFFER and the ADRS BUFFER are clocked at different times within a single microword timing state.

SUMMARY CHARTS are provided for the details of implementation and the effects of microprogramming on the various machine designs:

PROCESSOR STATE COMPLEXITY - (Figure 9) indicates the number of control states and data storage required within each processor.

PROCESSOR IC COMPLEXITY - (Figure 10) indicates the number and types of Integrated Circuit (IC) packages used in the processor. The availability of Medium Scale Integration (MSI) devices puts into perspective the contribution of the microprogramming control of the Large Scale Integration (LSI) devices.

PROGRAM CHARACTERISTICS - (Figure 11) compares the use of the control store in each of the processors.

EXPANDABILITY:

All the processors can be expanded along the UNIBUS with peripherals and through UNIBUS switches with other processors. The PDP-11/45 within its own backplane provides a separate microprogrammed Floating Point Processor in addition to the Semiconductor Memory Bus. Only the PDP-11/40 processor provides for expansion of the microprogram directly in terms of words and width. Figure 12 notes the expansion of the microstore for an Expansion Instruction Set, and for a Floating Point Instruction Set. The microword length is also extended in each case to provide control for the extended data path logic. This logic is

placed across the DMUX outgoing bus and the BUS D in going bus noted in the Block Diagram of Figure 7; the microcontrol store is expanded by module interconnecting cables on the wired-or ROM outputs. Within this expansion, the microcontrol bits for basic machine control which are unnecessary to the option, are ommitted.

SUMMARY AND CONCLUSIONS:

Very real advantages existed for each machine in the design phase. The precise order of the microcontrol provides for a direct, specified interface to the data path. Machine operation can be almost completely defined by the flow diagram and data paths. Some initial data path and microlength changes occur early in the design, but by the time the machine is breadboarded, the changes usually concern the microword. Microwords are added, control bits within the words are changed; the debug of the machines reflected this changes and the ease of making them.

Product hardware also benefitted from microprogramming. Each machine directly used microcontrol to meets its design goals. The PDP-11/05 consists of two module boards only because of the LSI influence of the ROM's used for microcontrol and decoding. The major advantage of the PDP-11/40 consists of speed with direct control of the data path reducing machine cycle time. The majority of credit for fewer IC's in the PDP-11/40, however, must go to the general use of MSI and LSI integrated circuits independent of microcontrol. Completely unique and dependent upon microprogramming is the PDP-11/40 expansion possible for the Expansion Instruction Set and the Floating Instruction Set. No other technique, except microprogramming, would allow these simple single module expansions. The PDP-11/45 used microcontrol for speed and some economy in control logic in addition to a segmentation of design. On any large machine, the ability to define segments of design, so as to apply more people effectively, is important.

The only concern for microprogramming comes from production considerations.

Production benefits derive from the lower module counts and the ability to replace modules in the PDP-11/05 and PDP-11/40 machines in production and in the field. Greater effort is then exerted at the module test and repair level (a lower level of production) rather than at the machine test level. The order of the microcode and of the machine also allows some simplification in training.

The only reservation on microprogramming comes from a production aspect of the initial reason for microprogramming. The advantages of standardized Large Scale Integration (i.e. noncustomized) exist mostly at the design and engineering prototype level where the application of a pattern to a Programmable Read Only Memory in an engineering atmosphere is immediate, and faster than changing logic and its associated etch boards. In the Production environment, however, the micropattern in a ROM from a vendor is a custom design. No other customer can use the design, delivery becomes a matter of IC yield with the vendor reluctant to have an inventory of your design. Careful long range purchasing is necessary to insure that all ROM patterns are present at module build. Some slippage can be accommodated by the use of Programmable Read Only Memory but only at a cost in time and money. Given this production-vendor relationship, one of the often mentioned advantages of microcode dissipates: Engineering changes will not be made against microcode, except as a last resort.

REFERENCES:

Processor Handbooks, Digital Equipment Corporation

PDP-11/20/15/r20 Processor Handbook, 1972

PDP-11/40 Processor Handbook, 1972

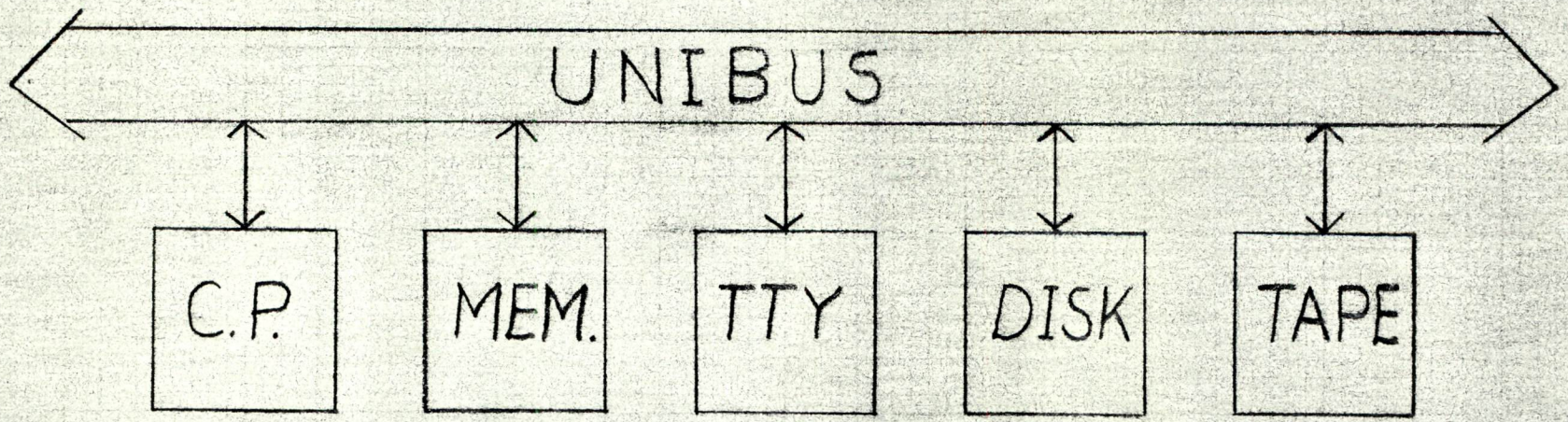
PDP-11/05 Processor Handbook, 1972

PDP-11/45 Processor Handbook, 1972

Microprogramming, Principles and Practices, Samir S. Husson, 1970, Prenctice-Hall

Computer Structures: Readings and Examples, Gordon Bell and Allen Newell, 1971, McGraw Hill

FIGURE 1: UNIBUS



BIDIRECTIONAL

ASYNCHRONOUS, INTERLOCKED

DYNAMIC OWNERSHIP

I/O ADDRESSABLE AS MEMORY

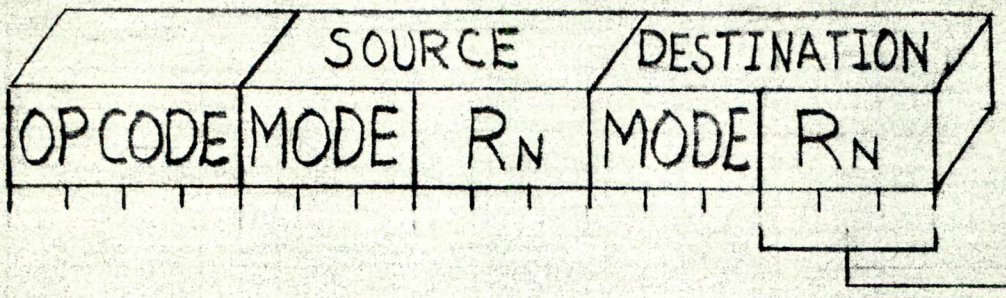
DATA SIGNALS, OWNERSHIP SIGNALS

VECTORED INTERRUPT

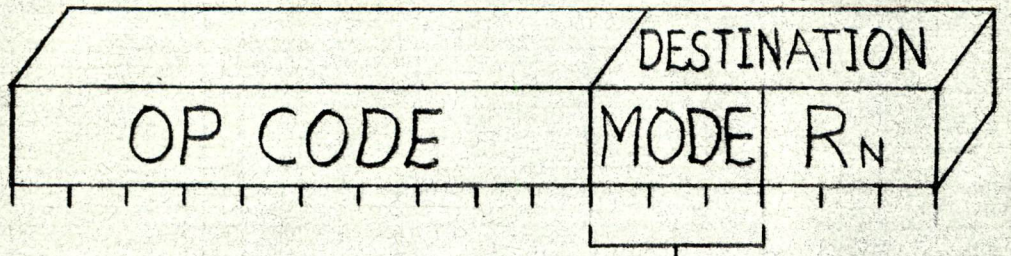
STANDARD SPECIFICATIONS

FIGURE 2: INSTRUCTION FORMAT

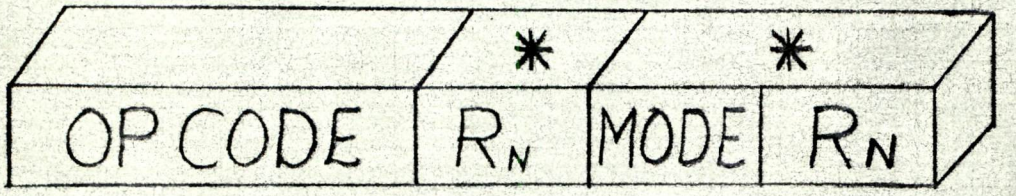
DOUBLE OPERAND



SINGLE OPERAND



ONE + HALF OPERAND



* SOURCE OR DESTINATION

REGISTERS

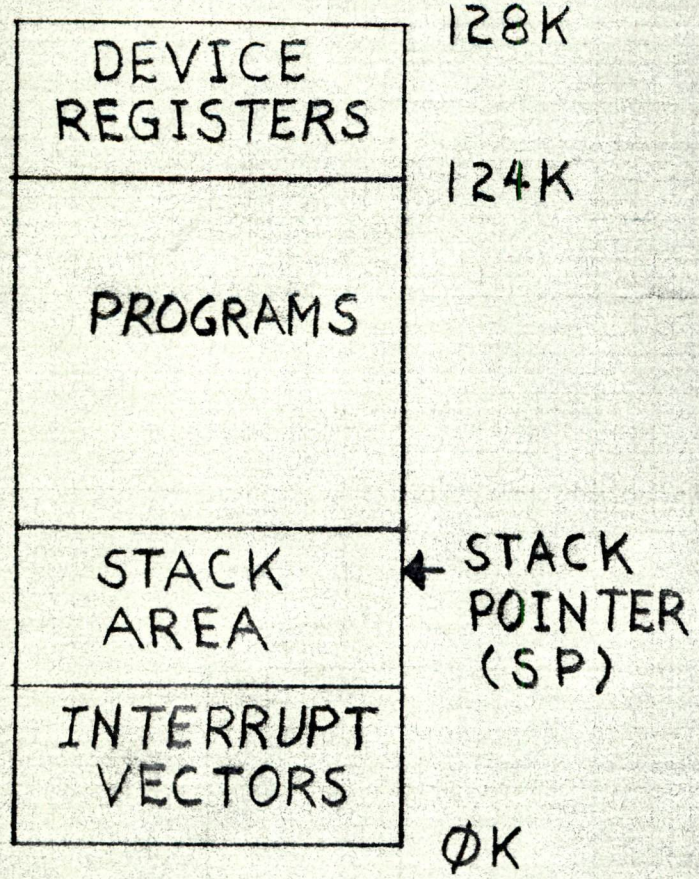
R0	ACCUMULATORS
R1	ADRS. POINTER
R2	STACK POINTER
R3	INDEX
R4	
R5	
R6	STACK POINTER
R7	PROGRAM COUNTER

MODES

0	REGISTER
1	REG DEFERRED
2	AUTO-INCREMENT
3	AUTO-INCR. DEFERRED
4	AUTO-DECREMENT
5	AUTO-DECR. DEFERRED
6	INDEX
7	INDEX DEFERRED

FIGURE 3: STACK OPERATIONS

MEMORY MAP



SP = STACK POINTER
R_N = GENERAL REGISTER
PC = PROGRAM COUNTER
DEST = DESTINATION ADDRESS
PS = PROCESSOR STATUS
VECTOR ADRS FROM PERIPHERAL

STACK ORDERED OPERATIONS

JUMP TO SUBROUTINE

$\downarrow(SP) \leftarrow R_N$
$R_N \leftarrow PC$
$PC \leftarrow DEST$

RETURN FROM SUBROUTINE

$PC \leftarrow R_N$
$R_N \leftarrow (SP)\uparrow$

INTERRUPT SERVICE

$\downarrow(SP) \leftarrow PS$
$\downarrow(SP) \leftarrow PC$
$PC \leftarrow$ (VECTOR ADRS)
$PS \leftarrow$ (VECTOR ADRS +2)

RETURN FROM INTERRUPT

$PC \leftarrow (SP)\uparrow$
$PS \leftarrow (SP)\uparrow$

FIGURE 4: MICROPROGRAMMIG BREADBOARD

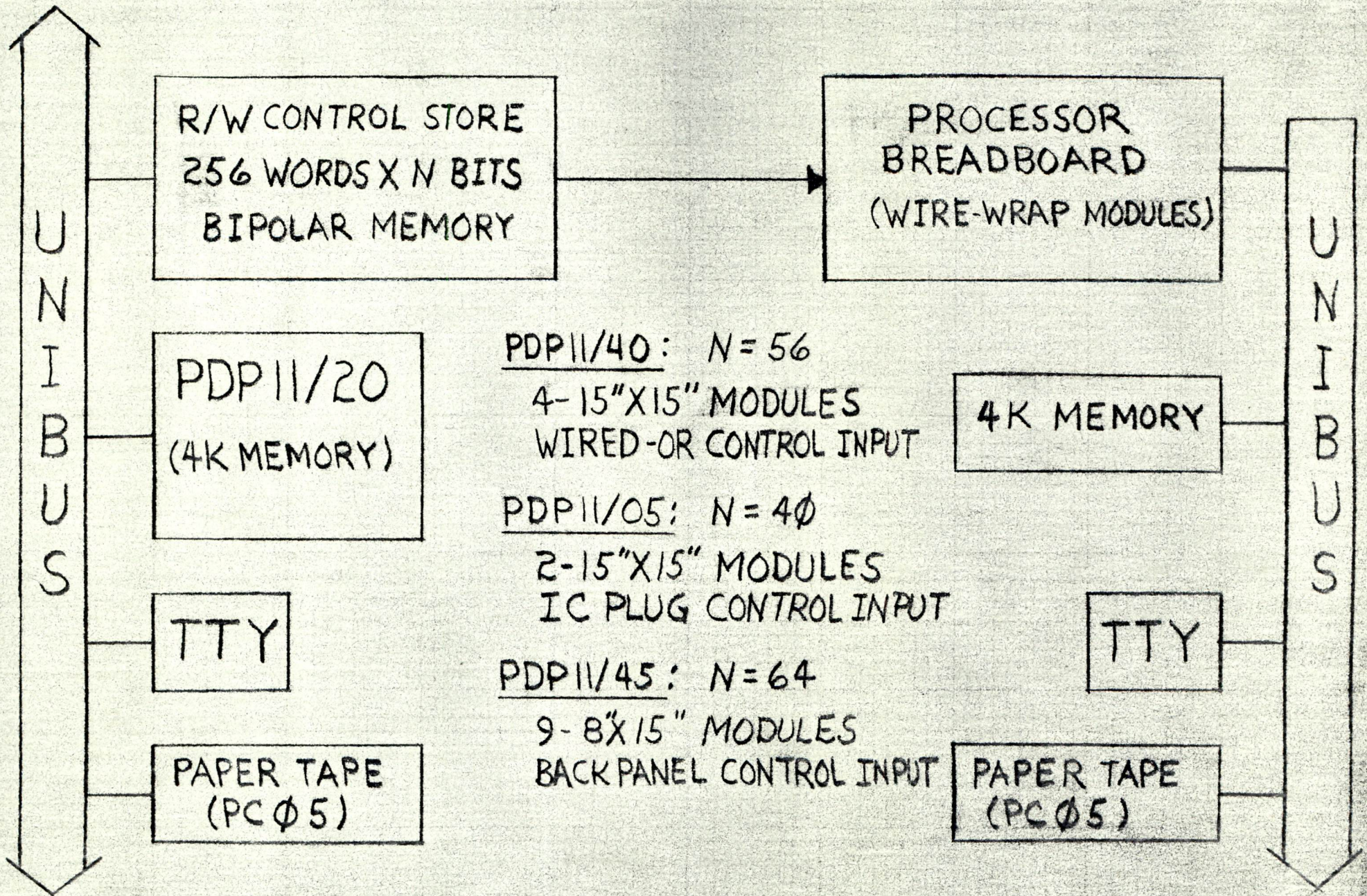
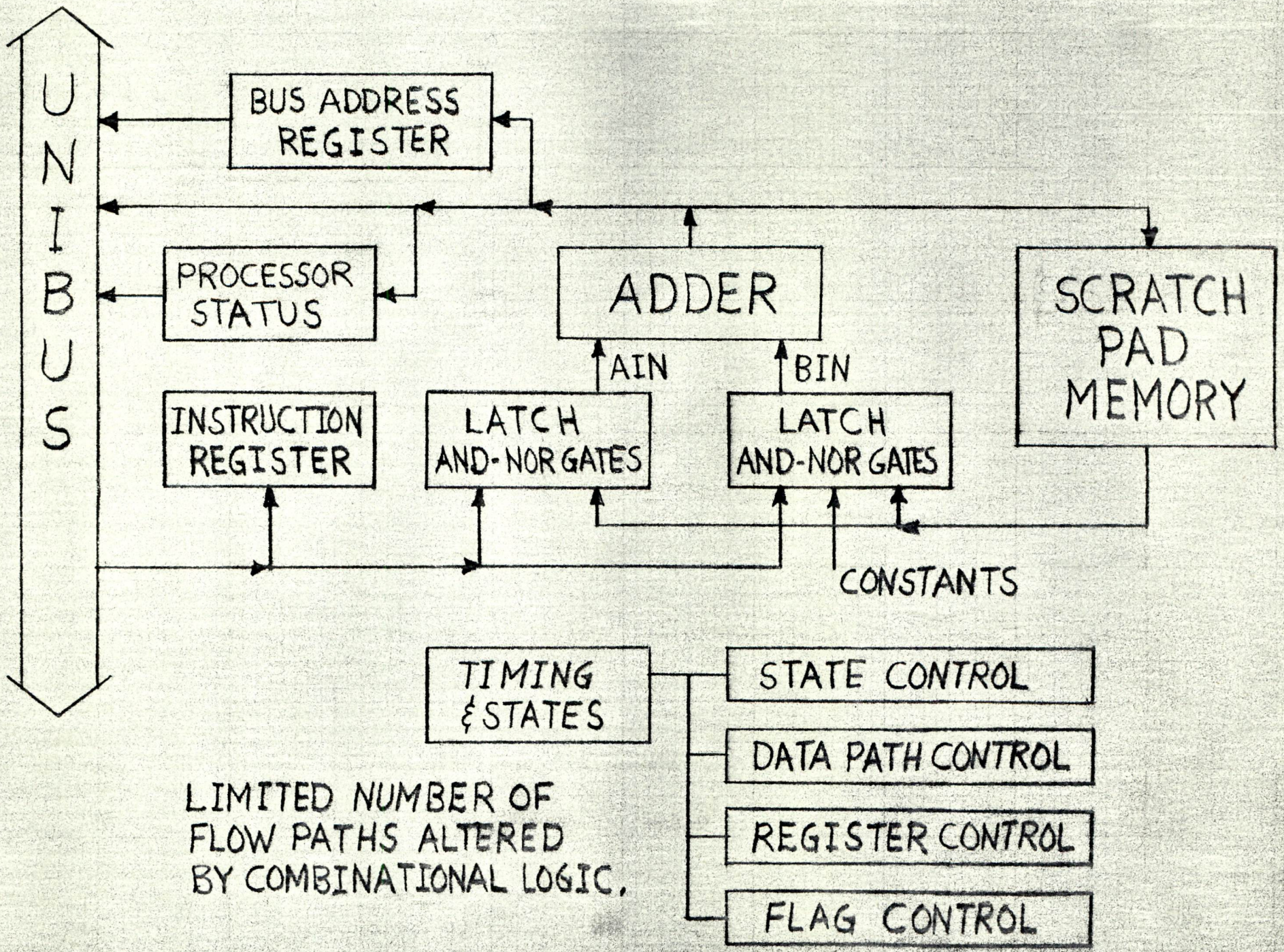


FIGURE 5: PDP 11/20 BLOCK DIAGRAM



LIMITED NUMBER OF FLOW PATHS ALTERED BY COMBINATIONAL LOGIC.

FIGURE 6: PDP 11/40 BLOCK DIAGRAM

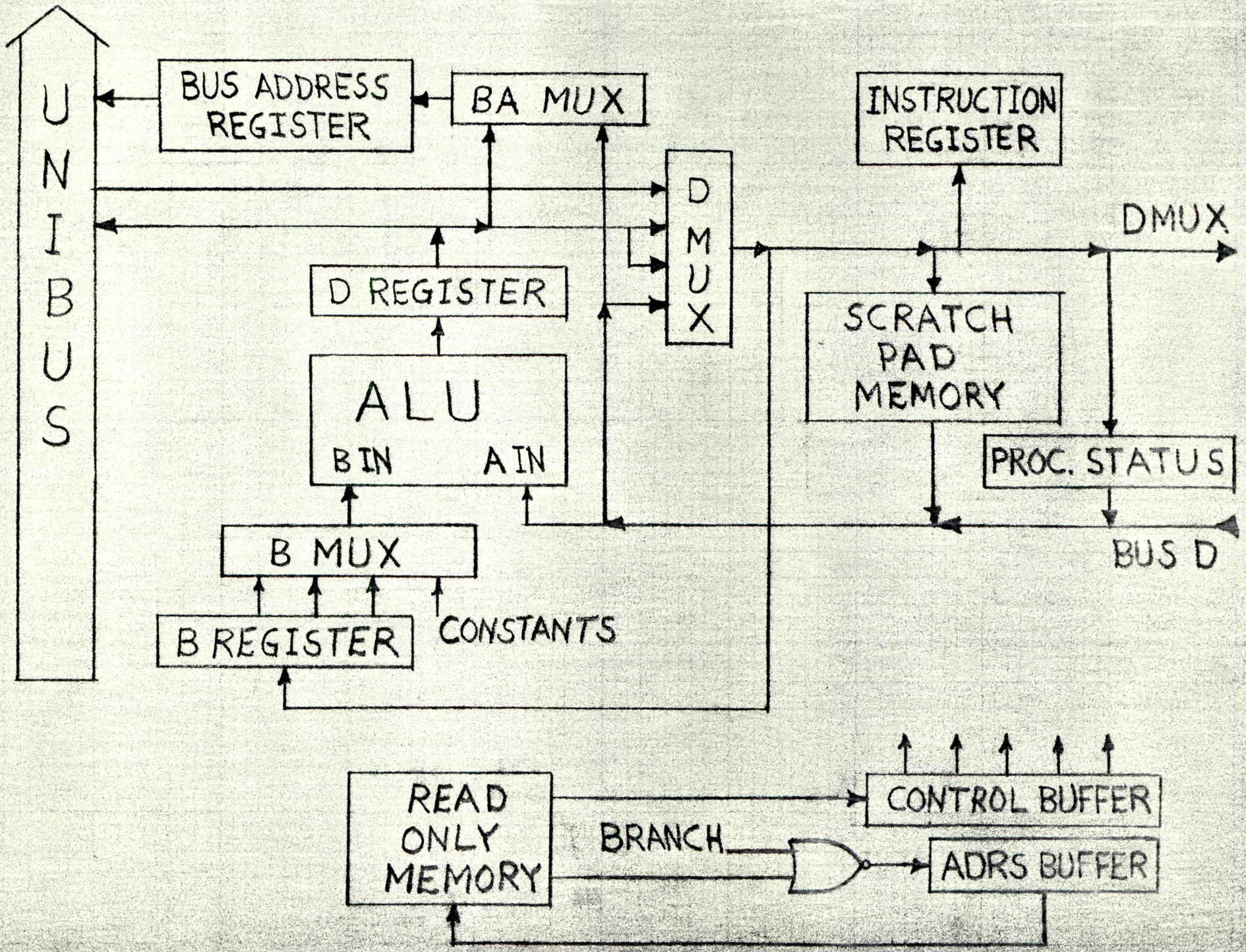


FIGURE 7: PDP11/05 BLOCK DIAGRAM

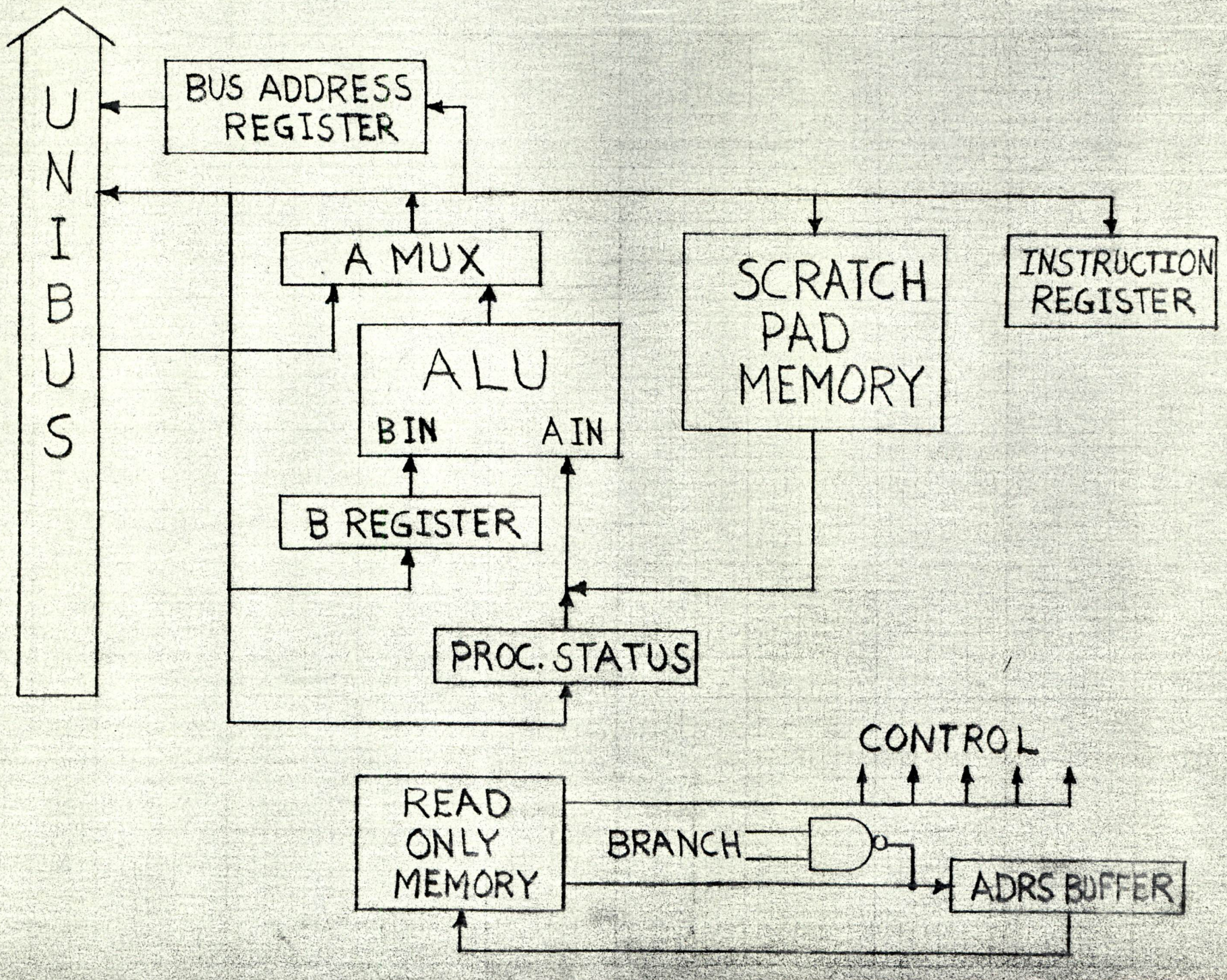


FIGURE 8: PDP 11/45 BLOCK DIAGRAM

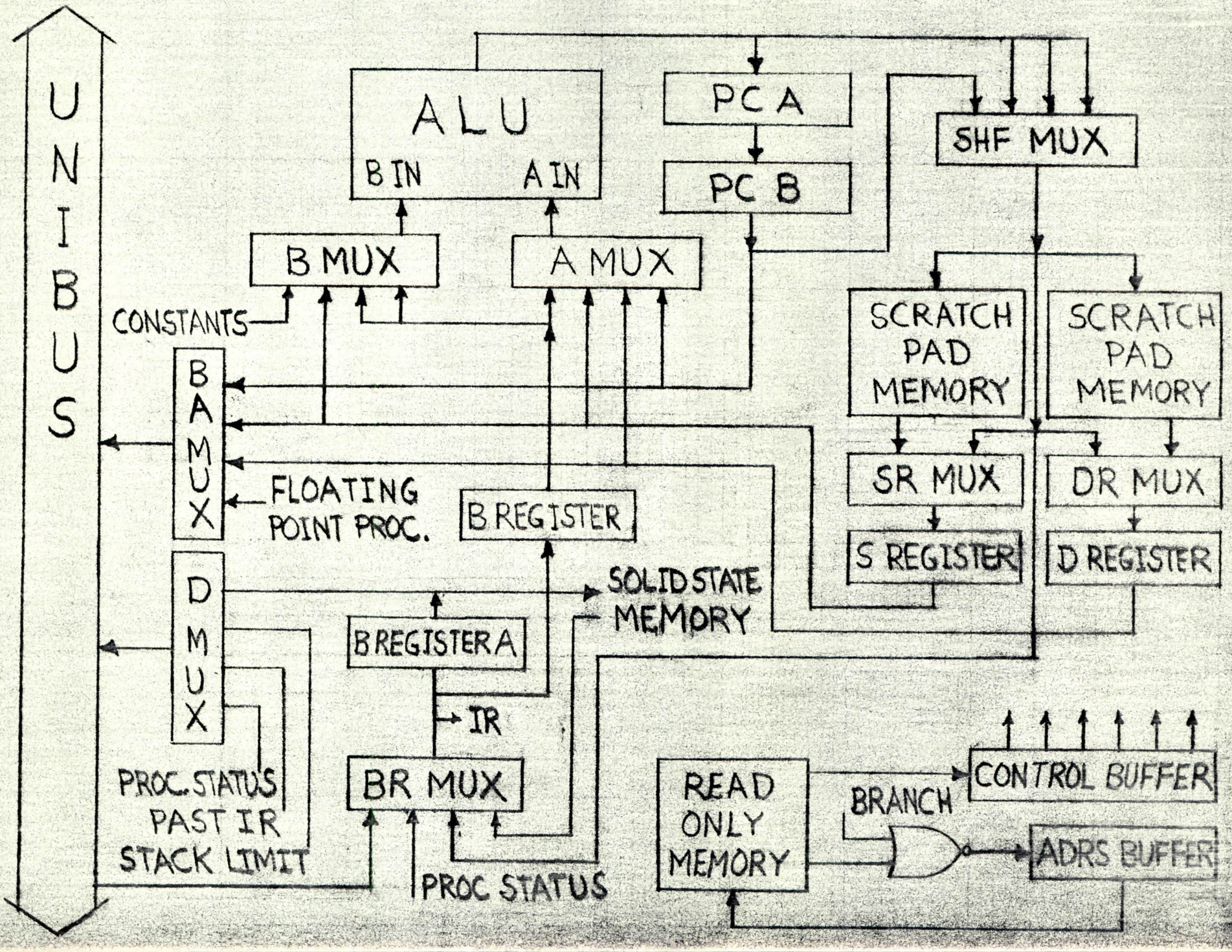


FIGURE 9: PROCESSOR STATE COMPLEXITY

MACHINES:	PDP11/20	PDP11/40	PDP11/05	PDP11/45
CONTROL				
SINGLE FF'S	67	54	65+9*	119
ROM'S (DECODE)	–	–	18 †	3 †
ROM'S (CONTROL)	–	56 BITS X256 WDS	40 BITS X256 WDS	64 BITS X256 WDS
WORD USUAGE		251 WDS	249 WDS	256 WDS
STORAGE				
CONTROL	16X1 (IR)	16X1 (IR) 56X1 WD	16X1 (IR)	16X2 (IR) 64X1 WD
DATA PATH	20 WDS	20 WDS	19 WDS	25 WDS

* THE PDP11/05 INCLUDES ASR INTERFACE.

† ROM'S ARE 8 BITS X 32 WDS.

FIGURE 10: PROCESSOR IC COMPLEXITY

IC'S (PACKAGES) \ PDP'S	11/20	11/40	11/05	11/45
SIMPLE LOGIC (GATES, FF'S)	504	332	129	519
MSI LOGIC (REGISTER, MUX'S)	19 (4%)	63 (15%)	37 (18%)	146 (21%)
LSI LOGIC (ALU'S, ROM'S)	—	22 (5%)	37 (18%)	31 (4%)
UNIBUS	105 (20%)	86 (21%)	50 (25%)	78 (11%)
TOTAL IC'S	523	417	203	696
IC TYPES	27	53	60	78

FIGURE 11: MICROPROGRAM CHARACTERISTICS

ITEMS \ MACHINES	11/05	11/40	11/45
SPEED RATIO*	0.8	1.85	2.04 CORE 3.58 MOS 4.92 BIPOLAR
WORDS	256	256	256
BUFFERED	NO	YES	YES
BITS	40	56	64
DIRECT	40	49	49
ENCODED	4‡	7	15
TIMING	157 NS † 315 NS 630 NS †	140 NS 200 NS 300 NS	150 NS

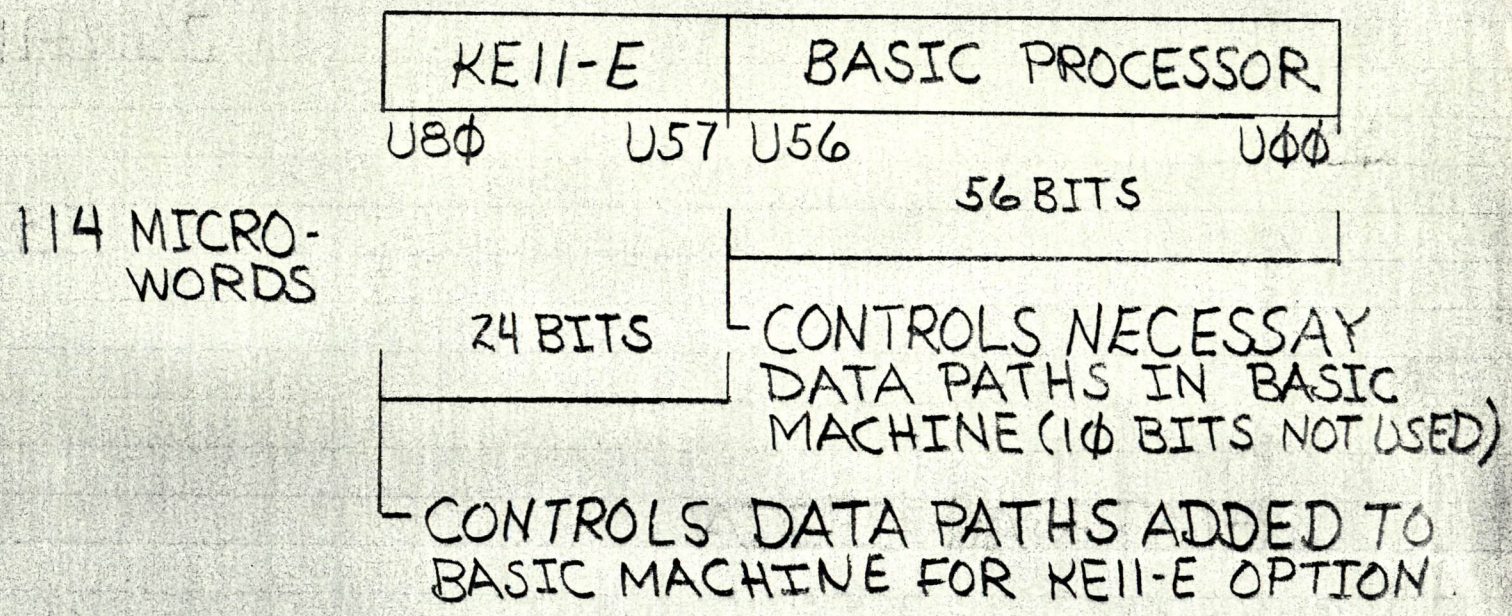
* RATIO OF MACHINE SPEED RELATIVE TO A PDP11/20, COMMON INSTRUCTION MIX, SAME CORE MEMORY.

‡ FOUR MICROPROGRAM BITS HAVE DOUBLE USUAGE.

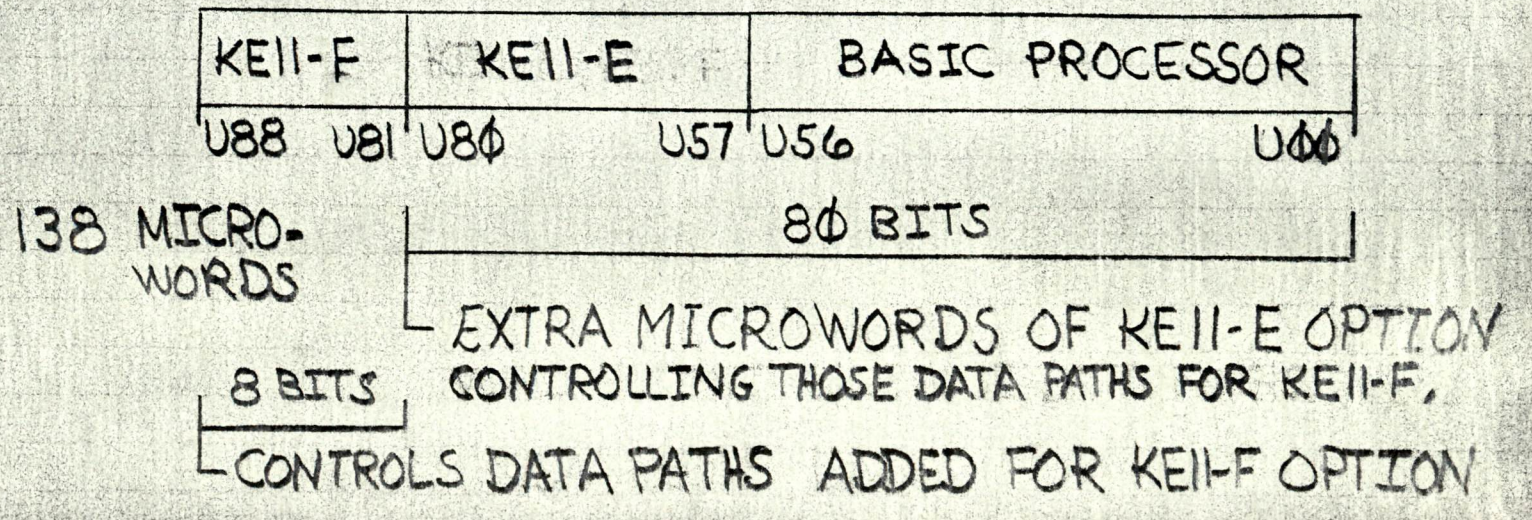
† SPECIAL CYCLES FOR SHIFT ON BYTE OPERATIONS (157 NS) AND FOR CONDITION CODE ALTERATION (630)

FIGURE 12: PDP 11/40 MICROWORD EXPANSION

KE11-E: EXPANSION INSTRUCTION SET
(MULTIPLY, DIVIDE, ARITHMETIC SHIFTS)



KE11-F: FLOATING INSTRUCTION SET
(FLOATING: ADD, SUBTRACT, MULTIPLY, DIVIDE)



digital INTEROFFICE MEMORANDUM

TO: Operations Committee

DATE: April 19, 1973

FROM: David Stone

DEPT: Software Engineering 12-2

EXT : 3741

David

SUBJ:

At Win's request I am presenting you with my current PDP-11 software product plans. The attached material represents an overview of -11 software and a total Software Engineering Budget proposal for FY74. I will discuss this with you on April 30.

(Additional, more detailed strategy information will be published between now and then as a continuing dialogue with the product lines.)

DS/jmab

Attachments

THE PROBLEM

BUILD A COMPATIBLE SET OF SOFTWARE WHICH SPANS A PRICE RANGE OF TWO ORDERS OF MAGNITUDE.

THE SOLUTION

- NO ONE SOLUTION

- BUILD A MINIMAL SET OF PRODUCTS WHICH SPAN THE MARKETS AND THE PRICE RANGE.

PDP-11 OPERATING SYSTEMS

	OEM	LDP	COMMERCIAL	COMPUTATION	IPG
LOW END (10K - 30K)					
PAPER TAPE	X	X			
CAPS-11	X	X			
RT11	X	X			X
**RSX-11A	X	X			X
MID RANGE (30K - 75K)					
**DOS	X	X			X
DOS/BATCH		X	X	X	X
RSTS-11			X	X	
**RSX-11B, C		X			X
MUMPS-11			X		
*RSX-11D SUBSET	X	X			X
HIGH END (75K - 250K)					
RSX-11D		X	X	X	X
RSTS/E			X	X	
MUMPS/45			X		
*BTS			X	X	

* BEING DEFINED

**PHASING OUT

PDP-11 LANGUAGES

FORTRAN

FORTRAN/11 - COMPLETE
FORTRAN/45 - JUNE 74

COBOL-11

LEVEL 1 - JANUARY 74
LEVEL 2 - JANUARY 75

BASIC

RSTS - COMPLETE
SINGLE USER - SUMMER 73

ALGOL-60

LIKELY CUSTOMER DEVELOPED

APL

LIKELY CUSTOMER DEVELOPED

RPG-II

COMPLETE

MACRO-11

COMPLETE

PL/1

INVESTIGATION

BLISS-11

BEING EVALUATED

SOFTWARE PRODUCT SHIPMENTS

	INSTALLED BY FY74	INSTALLED IN FY74
RSX-11A	10	100
RSX-11B, C	100	20
RSX-11D	30	220
RSX-15	60	40
DOS/BATCH	1,200	720
RT11	0	1,200
RSTS	200	240

FY74
AREAS OF EMPHASIS

TOTAL SOFTWARE PRODUCT

PLANNING
MONITORING
SUPPORT PLAN
EFFECTIVENESS EVALUATION

HARDWARE/SOFTWARE/SERVICE INTEGRATION

RP04 CONSULTING
ACCEPTANCE TEST PACKAGE
ERROR LOGGING CODING

MINIMIZE COMPONENTS

STOP DOS DEVELOPMENT
STOP MUMPS DEVELOPMENT
PHASE OUT RSX-11A, B, C,
COMBINE BASIC AND FORTRAN NEEDS

EXPLORE NETWORK OPPORTUNITIES

SOLVE KEY PROBLEMS

RSX-11D SUBSET

HIGH-END COMPUTATIONAL SYSTEM

COORDINATE PDP-11 SERVICES

DEVELOPMENT TOOLS

ENTRY LEVEL TRAINING

HARDWARE COORDINATION

digital INTEROFFICE MEMORANDUM

TO: List

DATE: April 4, 1973

FROM: David Stone

DEPT: Software Engineering 12-2

EXT : 3741

SUBJ: Software Engineering Budget Plan - FY73-FY75

The attached information is the basis for a consolidated Software Engineering spending plan for the next two fiscal years. While data has been collected about all parts of Software Engineering expenses, particular emphasis has been placed on PDP-11 software development plans. A new mechanism for funding the majority of PDP-11 software is proposed - the creation of a pool of shared PDP-11 software development dollars against which proposals can be made for projects intended to benefit more than one market area. The PDP-11 data is presented using my judgement as to which projects will be shared. In general, operating systems, languages, and support expenses fall into this category. This plan is a recommendation and a first draft; relevant inputs have been collected where possible, but in the interests of timely distribution some guesses were made. Careful review and suggestions are solicited.

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QUARTERLY SPENDING RATE ANALYSIS	6
SUMMARY OF SHARED PDP-11 SOFTWARE DEVELOPMENT FISCAL YEAR 1974	7
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A SHARED PDP-11 PROGRAMMING PROPOSAL

The Problems

Although steps have been taken to unify PDP-11 planning, they have not yet resulted in a coherent corporate strategy to create the most profitable products in an effective way. Support costs are increasing geometrically, products are proliferating, uniform corporate policies are lacking and our customers are unable to move their work from one product to another with ease (and in many cases can't transfer data between multiple systems in any reasonable way). The current product line funding structure for software exacerbates these problems by encouraging unnecessary product differentiation and making shared development hazardous.

New Directions

There have been three major shifts in DEC philosophy over the past year which bear directly on this proposal.

- The emergence of software as a product.
- The sharing of software products across product lines and vice-presidential areas.
- The increasing centralization of corporate engineering resources.

Each of these new directions exerts pressures on the way in which we perform the development process and has contributed to the problems cited. A modification to that development process is proposed.

Goals

1. Create a unified corporate software product plan, especially in the PDP-11 area; ensure good corporate visibility of overall plans.
2. Produce fewer, higher quality, more profitable software products and services through an improved development process and reduced support costs.
3. Perform software product development for basic systems products which ensures:
   - . covering and penetrating selected market areas
   - . building less components but combining them into the same or a greater number of products
   - . allowing facile inter-system communication
   - . creating a simple way for customers to upgrade from one product to another

4. Ensure consistency between corporate hardware and software development plans.

5. Incorporate proven, cost-effective technology into the software product development process.

6. Save money where possible without compromising product quality.

The Mechanism

To accomplish the above goals, I believe that two types of corporate action are necessary:

1. Create a shared PDP-11 software development budget pool related in some clear way to the relevant product line statements,

and

2. Create a mechanism for proposing, reviewing, and approving Software Engineering development projects to be funded from the shared pool.

In addition, I believe that certain specific "general support" projects should be approved - projects which would be very difficult to justify to an individual product line, but which are clearly profitable to the corporation as a whole.

Financial Summary

To provide a reasonable basis for understanding the financial impact of this proposal, comparable data for fiscal years 1972 through 1975 are presented in the following graph. Detailed data for fiscal years 1973 through 1975 are attached as a separate appendix; the data are summarized at a number of levels to provide easier access to the information they contain. In essence, a total Software Engineering budget increase from $5,341,000 (FY73) to $6,775,000 (FY74) or 27% is proposed. The budget is broken into four areas:

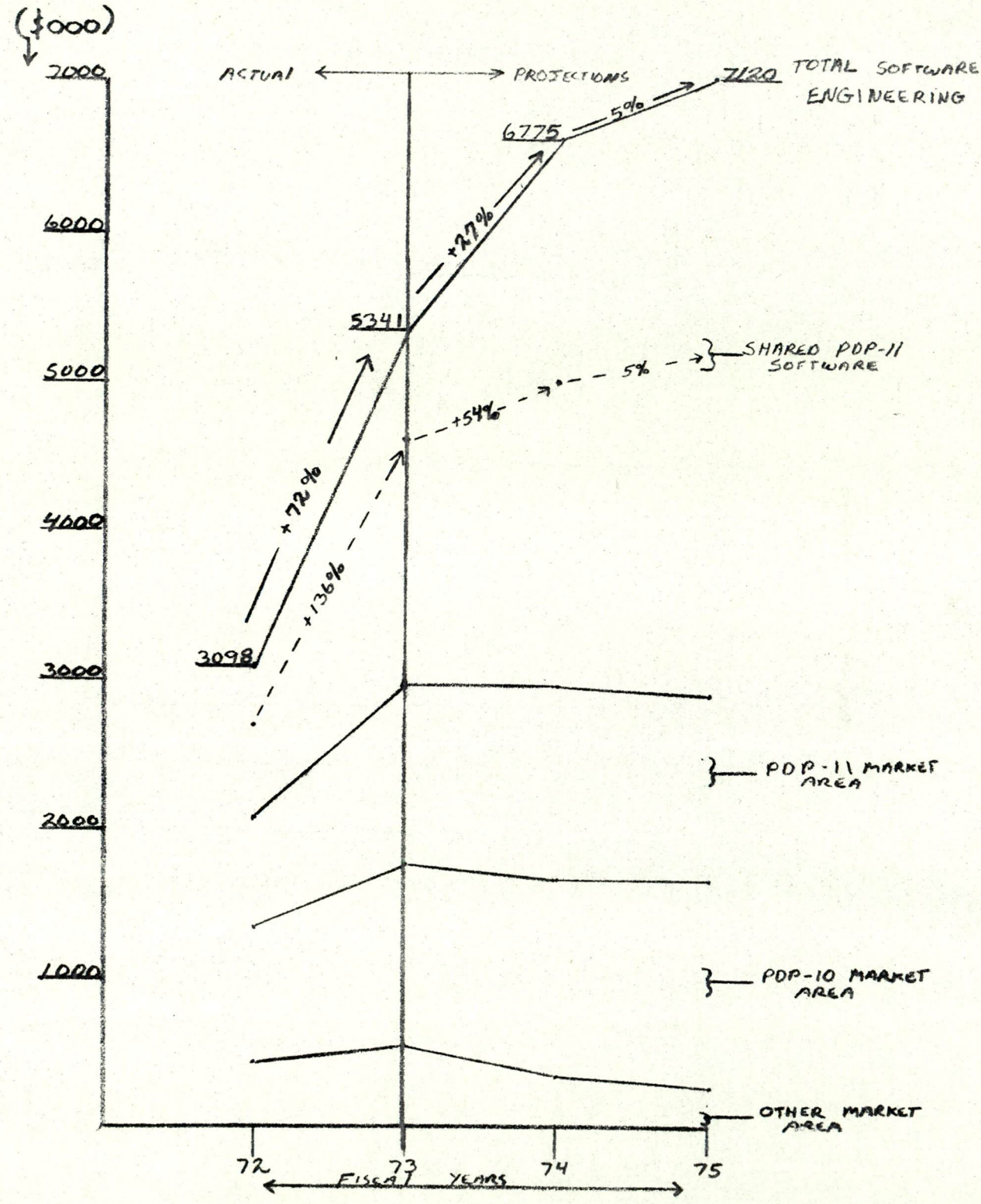
1. PDP-11 Shared Development - the pool of shared money this proposal addresses (up 54% for FY74).

2. PDP-11 Market Area Development - the per-product line money for specifically single market products (up 7% for FY74).

3. DECsystem-10 Market Area Development (up 23% for FY74).

4. Other Market Areas (down 61% for FY74).

(The figures projected for FY75 are roughly equal to those for FY74.)



ANNUAL SOFTWARE ENGINEERING EXPENSE BY MARKET GROUP

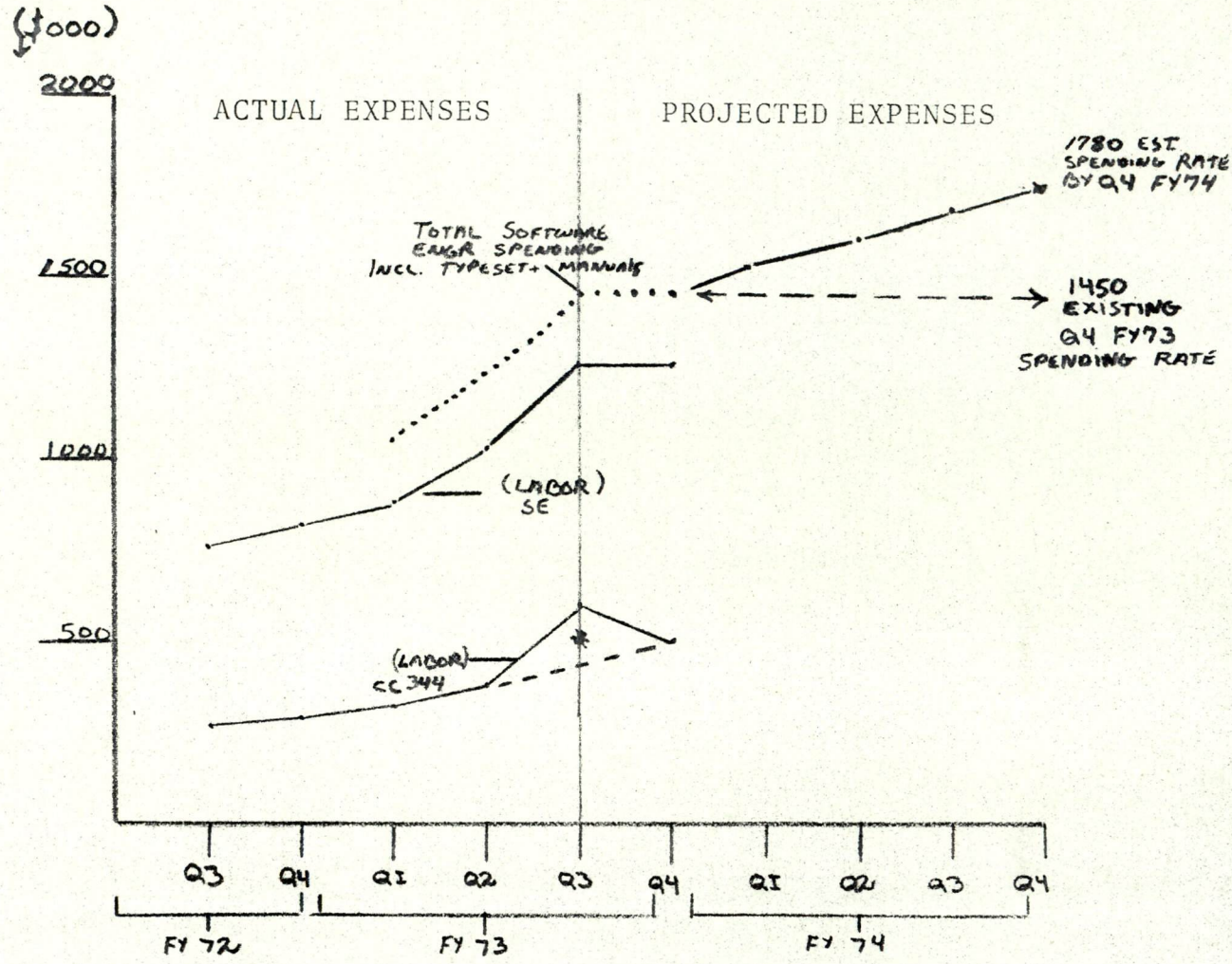
SOFTWARE ENGINEERING BUDGET PROJECTION
FY73-FY75
($000)

See Page		FY73	FY74	FY75
A2	PDP-11 Market Areas (Non Shared Project)	1,196	1,280	1,225
A3	DECsystem-10 Market Areas	1,210	1,490	1,480
A4	Other Market Areas	561	345	295
A5	Shared PDP-11 Software	2,374	3,660	3,480
	Contingency for Future Unknowns	-	-	640
	TOTAL SOFTWARE ENGINEERING	5,341	6,775	7,120

NOTES

These figures cover all Software Engineering expenses for Programming, Writing, and Software Manual Production (cost centers 241, 341, 342, 343, 344; "Y" Expense 550, 551, 552, 553, 554). Shared PDP-11 Software is the name applied to PDP-11 Operating Systems, Languages, and Support which are part of products sold by more than one Product Line. (It is not P.L. 96, which constitutes only a small part of such Shared Projects.) Substantial programming expenses not under Software Engineering control are not included.

Page references are to the Appendix.



(1) QUARTERLY SPENDING RATE ANALYSIS

LEGEND

* Q3 INCLUDES 100K COBOL CONTRACT

NOTE

(1) Q4 FY73 SPENDING RATE FOR FY74 WOULD BE $6 MILLION. PROPOSED INCREASE TO $6.8 MILLION IS 13% OVER CURRENT RATE

A Summary of Shared PDP-11 Software Development for Fiscal Year 1974

(A detailed cost breakdown is presented as an appendix.)

I. Small Systems (In Progress) (see page A6 for cost details)

1. Finish and support CAPS-11 as our low-end cassette-based system ($30K).

2. Support RSX-11A as our low-end real-time multi-tasking system ($30K).

3. Finish and support RT-11 as our combined real-time and program development system. Basic is the primary development language ($90K).

4. Create a small, fast Fortran to run under RT-11 and RSTS or RSX. This product would be of the WATFOR flavor ($80K).

II. Medium Systems (In Progress) (see page A7)

1. Stop DOS/BATCH development in Q1 with release nine. Do maintenance only ($120K).

2. For the RSTS family, support the existing 11/20 RSTS and extend RSTS-E as a first class Basic time-sharing system. Add RJE capability and compatible file system with RSX-11D, new peripherals, etc. ($180K).

3. Continue substantial development on RSX-11D to create already committed Batch support for release two. Push RSX-11D as the world's best process control real-time system for larger applications ($450K).

4. Continue to support the current RSX-11D Fortran (medium-sized) under both RSX-11D and DOS/BATCH. Implement 11/45 optimized Fortran (requiring FPP) to run under RSX-11D (June 1974) ($270K).

5. Continue current COBOL-11 effort to provide January 1974 release with RSX-11D release II (as ANS-73 level 1). Extend COBOL beyond that to level 2 ($180K).

III. New Products (see page A9)

1. Cover the system gap left by RSX-11A, RT-11, and RSX-11D by investigating an OEM flavor operating system aimed at DG's RDOS (small, multi-tasking, supports development). This system could be based on RSX-11A, RT-11 or a subset of RSX-11D but will in any case be the basis for an RSX-11D network of small systems ($150K).

2. Extend our grip on the top end of the program development and applications system area by investigating a general purpose time-sharing system (probably not allowing assembly language). Candidates for this system's base are RSTS-multi-language and RSX-11D with a Time Sharing Option ($180K).

3. Extend RSTS-E (independent of RSTS-ML) to keep RSTS as the top-performing high-end PDP-11 time-sharing system ($120K).

4. Investigate new language support (PL1?) ($30K).

5. Provide two people to work with shared engineering on new memory hierarchies and new system architecture ($60K).

IV. General Support Projects (see page A10 for costs)

General Support projects are summarized in two ways. First, a brief statement about each project is listed; and second a table showing which projects impinge on the goals and problems is given.

1. BLISS-10/BLISS-11 - Support FORTRAN-10 (written in BLISS-10) as well as FORTRAN-11 (to be written in BLISS-11). Products developed by Carnegie-Mellon; we just modify slightly and maintain.

2. Hardware Pool - In July 1973 we will have about 1 million dollars retail worth of PDP-11 hardware. Current expectations are that by July 1974 we will need 2.5 million dollars worth. Specific needs are:

   a. A competent engineer/manager to run, plan, and configure these systems.

   b. A set of cross-bar switches to enable fast, fault-free reconfiguration for testing software on all legal systems (two four-CPU complexes are planned; each can operate stand-alone with one or more of four different peripheral mixes.) This project should be in Bruce Delagi's budget.

   c. A DECsystem-10/PDP-11 data link to allow easy transmission of data from the 10-based software tools (see 3. below) to the 11 testing systems and vice versa.

3. 10-11 Software Tools - Unify and maintain all DECsystem-10-based software tools for PDP-11 development. Included are MACX11, MACY11, LINKX11, LINKY11, a librarian, and sysgen capability.

4. MIMIC - Continue current support for this DECsystem-10-based simulator by adding new peripherals as they are developed and maintaining old ones.

5. Shared Engineering Support - Provide a man to Grant Saviers to create device handler strategies in conjunction with design of the device and the controller.

6. Network Coordination - Define, implement, and enforce corporate software policies regarding network interconnection of our systems. Includes communications protocols, data semantics, command languages, etc.

7. Field Test Administration - Define and implement procedures ensuring that maximal benefit is gained from the field test of all major products. Provide good communication to and from customer sites, software services, and Software Engineering. Keep records on effectiveness of various sites.

8. Acceptance Tests - As part of product release procedure, ensure that an adequate acceptance test is created to support:

   a. the manufacturing floor,

   b. field service on-site,

   c. software services personnel,

   d. our contract to be paid for the accepted software.

   Create tests for those products already developed which are to be sold.

9. Product Planning - Create a two-man staff of highly competent software product planners within Software Engineering to propose an overall software product strategy for the corporation in conjunction with the product lines. This group will disseminate accurate and timely planning and competitive analysis information to the people who need it (e.g., the PDP-11 Operating Systems Characteristics memo dated March 2, 1973). They will also generate new product proposals for review by the PDP-11 Shared Software Development Committee.

10. Entry Level Training - This function will be responsible for the hiring, training, and integration of entry-level (college-graduate mainly) personnel into Software Engineering. It is an essential part of stabilizing the programmer salary structure and gives us an ideal mechanism to implement the corporation's Equal Employment Opportunity action program. This money will be used to pay for the first six months work/training of approximately twenty people over the year.

11. Evaluation of Purchased Software - As we start to sell software products, it becomes more profitable to encourage our customers to create application packages for our machines. When we buy them, however, we must subject them to an adequate evaluation process to ensure that they meet the quality standards for our products. This shared part of those

evaluations will ensure that uniform procedures are developed and followed.

CORPORATE DIRECTIONS / SUPPORT PROJECTS	BLISS-10/ BLISS-11	HARDWARE POOL	SWITCHES	10-11 DATA LINK	10-11 SOFTWARE TOOLS	MIMIC	SHARED ENGINEERING SUPPORT	NETWORK COORDINATION	FIELD TEST ADMINISTRATION	ACCEPTANCE TEST	PRODUCT PLANNING	ENTRY LEVEL TRAINING	EVALUATION OF PURCHASED SOFTWARE
software as product									X	X	X		X
sharing products								X			X		
centralized engineering							X				X		
GOALS													
less products/components	X							X			X		X
higher quality products	X						X		X	X	X	X	X
unified product plan								X			X		
inter-system communications			X	X				X			X		
customer upgrades								X			X		
hardware/software coordination							X				X		
new, proven technology	X		X	X	X	X							
save money		X	X	X	X	X			X	X		X	
PROBLEMS													
poor profit											X		
support costs	X								X	X	X		X
lack of policies									X		X		X
inter-connection & upgrade			X	X				X			X		
too many products								X			X		X

APPENDIX

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PDP-11 MARKET AREAS

	FY73		FY74		FY75	
	Maint	Dev	Maint	Dev	Maint	Dev
Business		246*	30	30	60	60
Communications		171*	60	210	90	240
DECNET		55	10	50	20	40
LDP		183*	30	190	30	220
MUMPS-11		161	30	30	30	60
TYPESET-11 (Gross Estimate)		330	50	460	75	200
11 Area's Manual Production		50		100		100
Subtotal 11 Market Areas		1,196	210	1,070	305	920
TOTAL 11 MARKET AREAS MAINTENANCE & DEVELOPMENT		1,196		1,280		1,225

*Maintenance not separated from Development

DECSYSTEM-10 MARKET AREAS

	FY73		FY74		FY75	
	Maint	Dev	Maint	Dev	Maint	Dev
DECsystem-10 Software	300	760	330	985	360	920
Manual Production		150		175		200
Subtotal 10 Market Areas	300	910	330	1,160	360	1,120
TOTAL 10 MARKET AREAS MAINTENANCE & DEVELOPMENT	1,210		1,490		1,480	

OTHER MARKET AREAS

	FY73		FY74		FY75	
	Maint	Dev	Maint	Dev	Maint	Dev
MUMPS-15	53	-	-	-	-	-
PDP-8	39	177	60	60	60	60
PDP-15	159	-	60	90	100	-
TPL	33	-	25	-	25	-
Other Manual Production	-	100	50	-	50	-
Subtotal Other Market Areas	284	277	195	150	235	60
TOTAL OTHER MARKET AREAS MAINTENANCE & DEVELOPMENT	561		345		295	

Excluded Areas:

TYPESET-8
TYPESET-10
Medical Systems
CSS
Advanced Systems (10)
Lorrin Gale
Programming done by product lines

(NO Diagnostics
SDC
or Software Support
is included.)

SHARED PDP-11 SOFTWARE

See Page		FY73	FY74	FY75
A6	Small PDP-11 Existing Systems and Extensions			
	Operating Systems	191	120	60
	Languages	16	140	90
	Support & Other	98	100	60
	Subtotal Small PDP-11 Existing Systems	305	360	210
A7	Medium PDP-11 Existing Systems and Extensions			
	Operating Systems	1,124	750	270
	Languages	404	600	450
	Support & Other	196	300	300
	Subtotal Medium PDP-11 Existing Systems	1,724	1,650	1,020
A8	Shared Manual Production	345	515	690
A9	New Shared PDP-11 Systems			
	Operating Systems	-	510	720
	Languages	-	30	180
	Support & Other	-	595	660
	Subtotal New PDP-11 Systems	-	1,135	1,560
	GRAND TOTAL SHARED PDP-11 SOFTWARE	2,374	3,660	3,480

SHARED SMALL PDP-11 EXISTING SYSTEMS AND EXTENSIONS

See Page		FY73 Maint	FY73 Dev	FY74 Maint	FY74 Dev	FY75 Maint	FY75 Dev
	CAPS-11		34	30	-	30	-
	RT-11		118	30	30	30	-
	RSX-11A, B, C	39	-	30	-	-	-
	Subtotal Small Operating Systems	39	152	90	30	60	-
	Subtotal Maintenance & Development	191		120		60	
	Basic	-	16	30	30	30	-
	Fortran	-	-	-	80	30	30
	Subtotal Small Languages	-	16	30	110	60	30
	Subtotal Maintenance & Development	16		140		90	
A10	Support & Other	59	39	-	100	-	60
	Subtotal Maintenance & Development	98		100		60	
	Subtotal Small PDP-11	98	207	120	240	120	90
	TOTAL SMALL PDP-11 MAINTENANCE & DEVELOPMENT	305		360		210	

SHARED MEDIUM PDP-11

See Page		FY73 Maint	FY73 Dev	FY74 Maint	FY74 Dev	FY75 Maint	FY75 Dev
	DOS/BATCH	82	169	120	-	60	-
	RSTS	44	104	30	30	-	-
	RSTS-E	-	99	30	90	60	-
	RSX-11D	-	626	150	300	150	-
	Subtotal Medium Operating Systems	126	998	330	420	270	-
	Subtotal Maintenance & Development	1,124		750		270	
	COBOL-11	-	251	-	330	60	120
	FORTRAN	23	130	30	240	30	240
	Subtotal Medium Languages	23	381	30	570	90	360
	Subtotal Maintenance & Development	404		600		450	
A10	Support & Other	16	180	-	300	-	300
	Subtotal Maintenance & Development	196		300		300	
	Subtotal Medium PDP-11	165	1,559	360	1,140	360	660
	TOTAL MEDIUM PDP-11 MAINTENANCE & DEVELOPMENT	1,724		1,650		1,020	

SHARED PDP-11 MANUAL PRODUCTION

	FY73	FY74	FY75
Software Manual Production (Originals)	120	180	240
Software Manual Reprints & Diagnostics (Including SDC Printing)	225	335	450
GRAND TOTAL SHARED PDP-11 MANUAL PRODUCTION	345	515	690

SHARED PDP-11 PROJECTS
NEW OPERATING SYSTEMS & LANGUAGE

See Page		FY73 Maint	FY73 Dev	FY74 Maint	FY74 Dev	FY75 Maint	FY75 Dev
	OEM Operating System RSX Network Node RSX ABC			-	150	60	90
	RSTS Multi-Language RSX-T/S			-	180	60	180
	New System Architecture			-	60	60	150
	RSTS-E Extensions			-	120	-	120
	Subtotal New Operating Systems			-	510	180	540
	Subtotal Maintenance & Development			510		720	
	New Language				30		180
A10	Support & Other				595		660
	TOTAL SHARED PDP-11 (NEW OPERATING SYSTEMS & LANGUAGE) MAINTENANCE & DEVELOPMENT			1,135		1,560	

SHARED PDP-11 PROJECTS
SUPPORT AND OTHER

	FY73		FY74		FY75	
	Maint	Dev	Maint	Dev	Maint	Dev
BLISS-10/BLISS-11	30*	-	45	45	45	45
Hardware Pool Management	30	-	30	-	60	-
Engineering 10-11 Data Link	-	-	-	45	15	-
10-11 Software Tools (MACRO,Linker)	15	15	30	30	30	30
MIMIC	-	88	30	40	30	40
Shared Engineering Support (RP04, etc.)	-	8	-	30	-	60
Network Coordination & Policies	-	15	-	60	-	60
Field Test & Administration	-	30	-	60	-	60
Product Planning	-	-	-	60	-	60
Acceptance Test Generation (Includes Mfg Support)	-	30	15	75	30	90
Entry Level Training	-	10	-	150	-	200
General Maintenance	53	-	-	-	-	-
Evaluation of Purchased Software	-	-	-	60	-	90
Subtotal Support & Others	98	196	150	655	210	735
TOTAL SUPPORT & OTHERS MAINTENANCE & DEVELOPMENT	294		805		1,005	
Shared By:						
Small PDP-11	98		100		60	
Medium PDP-11	196		300		300	
New PDP-11	-		595		660	

*Funded by DECsystem-10; not included in totals