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B-129

Memorandum 6M-3284 Sup. #2

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SUBJECT: DISPLAY LINE DRIVER (THEORETICAL ANALYSIS)

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Date: July 20, 1956

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Abstract: The orignal M note described the operation of the display line driver in general terms. The first supplement analyzed the individual stages within the amplifier thoroughly. This note combines the analysis of supplement 1 to develop the behavior of the amplifier as complete entity. Several results are obtained from the theretical analysis which are useful for adjustment of the amplifier.

The amplifier common mode square-wave response should not be adjusted for any faster response time than is absolutely necessary because of a loss in the common mode rejection properties of the amplifier.

The amplifier should not be used to drive loads under 500 ohms without an appropiate reduction of maximum output swing. Failure to do so will cause excessive power dissipation in the output tubes resulting in reduced life.

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

General

The complete line driver was described in very general terms in the original note. The first supplement described and analyzed the individual stages as separate entities. This paper analyses the complete amplifier theoretically. Drawing E75792 (Fig. 0.1) is a complete circuit schematic.

1.1 Differential Mode Analysis

Figure 1.1.1 (SA-65908) is a block diagram showing the complete signal flow path for the differential amplifier. All KG numbers refer to previously derived transfer functions given in supplement one. The numbers and letters between the KG functions refer to corresponding voltage test points shown in E75792. If the four transfer functions in the forward path, $K_9\ G_9$ (Fig. 3.4.2, supplement #1 SB-48744-G), $K_7\ G_7$ (Fig. 3.3.2, supplement #1, SB-48743-G), $K_5\ G_5$ (Fig. 3.2.2, supplement #1, SB-48742-G), and $K_1\ G_1$ or $K_3\ G_3$ (Fig. 3.1.2, supplement #1, SB-48741-G), are multiplied together (db magnitudes and phase angles added) as shown in Fig. 1.1.2 (SA-65921), they can be replaced by a single forward gain transfer function $K_A\ G_A$. Since the transfer function of the output stage differs for SD and DD, two separate functions are required and will be differentiated by a second subscript, $K_{AS}\ G_{AS}$ for SD and $K_{AD}\ G_{AD}$ for DD. Figure 1.1.3 (B-48756-G) is a plot of these two transfer functions.

Figure 1.1.4 (SA-65920) repeats Figure 1.1.1 with the simplified forward gain transfer function. It can be shown for this diagram (see Eq. A-11) that the overall differential transfer function is:

Eq. 1.1.1 $$K\,G_{DIFF} = \frac{K_{11}\,G_{11}\,K_A\,G_A}{1 + K_{13}\,G_{13}\,K_A\,G_A}$$

This function can more easily be evaluated if it is rewritten as:

Eq. 1.1.2 $$K\,G_{DIFF} = \frac{K_{11}\,G_{11}\,K_B\,G_B}{K_{13}\,G_{13}}$$

where

Eq. 1.1.3 $$K_B\,G_B = \frac{K_{13}\,G_{13}\,K_A\,G_A}{1 + K_{13}\,G_{13}\,K_A\,G_A}$$

The function $K_{13}\ G_{13}\ K_A\ G_A$ is the differential open loop gain of the line driver and is plotted in Fig. 1.1.5 (B-48755-G). It is obtained by multiplying the separate $K_{13}\ G_{13}$ and $K_A\ G_A$ functions (db magnitudes and phase angles of Fig. 3.5.2 supplement #1, SB-48754-G, and Fig. 1.1.3 of this supplement added together).

The function $K_B\ G_B$ is the differential closed loop response of the line driver and is plotted in Fig. 1.1.6 (SB-48765-G) for SD, and Fig. 1.1.7 (SB-48767-G) for D.D. This function is obtained by plotting $K_{13}\ G_{13}\ K_A\ G_A$ on an M-N contour chart Fig. 1.1.5a (SA-48781-G) and Fig. 1.1.5b (SA-48782-G) and replotting from a new set of coordinates the function $K_B\ G_B$ (the M-N contour chart DL-1433 permits the graphical evaluation of the function $\frac{A}{1+A}$ when A is known graphically as a complex variable).

On Fig. 3.5.2 supplement #1, SB-48754-G the curves for G_{13} are subtracted from the curves for G_{11} and the results added to $K_B G_B$ (Figs. 1.1.6 or 1.1.7 of this supplement). The result is the overall transfer function KG_{DIFF} (Eq. 1.1.2) which is plotted in Fig. 1.1.8 (SB-48768-G) for SD, and Fig. 1.1.9 (SB-48769-G) for DD. It will be noticed that the addition of the input characteristic $K_{11} G_{11}/K_{13} G_{13}$ decreased the frequency response of the total differential amplifier. The addition of speed-up capacitors across the input resistors R_3, R_4, R_{11} and R_{12} in Fig. 3.5.1 of the first supplement could have caused a rising characteristic in the vicinity of 100KC and extended this frequency response. This was not done in the present amplifier because non-linearities (discussed in section 1.3 of this supplement) cause a considerable peaking of the frequency response in this vicinity under certain differential input conditions and the addition of the speed-up capacitors would have accentuated the peaking more severely. Although a slight peaking is desirable to speed-up the square-wave response of the amplifier, too severe a peaking causes undesirable ringing of the square wave. R35-1 is supplied to control the roll-off of the frequency response and thus control the rise time characteristic of a square-wave response.

1.2 Common Mode Analysis

Fig. 1.2.1 (SA-65909) is a block diagram showing the complete signal flow path for the common mode response of the line driver. As in section 1.1 all KG numbers refer to transfer functions derived in supplement one, and numbers and letters between KG functions refer to voltage test points on E75792.

Fig. 1.2.2 (SA-65919) shows two simplifications which can be made in the complete diagram. The four transfer functions in the forward gain can be combined to a single forward gain transfer function $K_C G_C$ ($K_{10} G_{10}$ Fig. 3.4.3 supplement #1, SB-48745-G, $K_8 G_8$ Fig. 3.3.2 supplement #1, SB-48743-G; $K_6 G_6$ Fig. 3.2.2 supplement #1, SB-48742-G; and $K_2 G_2$ or $K_4 G_4$ Fig. 3.1.2 supplement #1, SB-48741-G). This new function ($K_C G_C$) is plotted in Fig. 1.2.3 (SB-48763-G). Since this function differs for the type of display the amplifier is used for, a second subscript is added to differentiate for the two uses. Thus $K_{CS} G_{CS}$ is the forward gain transfer function for SD, and $K_{CD} G_{CD}$ for DD.

The second simplification is obtained by combining the four feedback transfer functions into a single function $K_D G_D$ ($K_{18} G_{18}$ Fig. 3.8.2 supplement #1, SB-48759-G; $K_{17} G_{17}$ Fig. 3.7.2 supplement #1, SB-48758-G; $K_{16} G_{16}$ Fig. 3.6.2 supplement #1, SB-48757-G: and $K_{15} G_{15}$ Fig. 3.5.3 supplement #1, SB-48753-G). This function is plotted in Fig. 1.2.4 (SB-48764-G).

Fig. 1.2.5 (SA-65925) is the simplified common mode transfer diagram of the line driver. The overall common mode transfer function for this circuit (see appendix B, Eq. B-12 is)

Eq. 1.2.1 $$KG_{cm} = \frac{K_{12} G_{12} K_C G_C}{1 + K_C G_C (K_D G_D - K_{14} G_{14})}$$

This transfer function can be solved more easily if it is rewritten:

Eq. 1.2.2 $$K G_{cm} = \frac{K_{12} G_{12} K_E G_E}{K_F G_F}$$

where

Eq. 1.2.3 $$K_E G_E = \frac{K_F G_F K_C G_C}{1 + K_F G_F K_C G_C}$$

and

Eq. 1.2.4 $$K_F G_F = K_D G_D - K_{14} G_{14}$$

Several methods are available for evaluating $K_F G_F$. The most obvious, and most time consuming, would be to obtain both $K_D G_D$ and $K_{14} G_{14}$ algebraically from their composite equations from suplement #1. The second method would consist of evaluating $K_D G_D$ and $K_{14} G_{14}$ at several points from their graphs, obtaining their vector difference and replotting. The method chosen was a strict graphical manipulation. If equation 1.2.4 is rewritten in the form:

Eq. 1.2.5 $$K_F G_F = \frac{K_D G_D}{K_H G_H}$$

where

Eq. 1.2.6 $$K_H G_H = \frac{(-K_D G_D / K_{14} G_{14})}{1 + (-K_D G_D / K_{14} G_{14})}$$

the entire solution can be obtained graphically. First the curve for $K_{14} G_{14}$ (Fig. 3.5.4 supplement #1, SB-48762-G) is subtracted from $K_D G_D$ (Fig. 1.2.4 of supplement #2 SB-48764-G) and the phase angle shifted $+180^\circ$. This gives $-K_D G_D / K_{14} G_{14}$. This curve is transferred to an M-N contour chart (Fig. 1.2.5a SA-48780-G) and $K_H G_H$ is read off directly. Since $K_D G_D$ is much greater than $K_{14} G_{14}$ in the region below one megacycle for R35-2 equal to five kilohms, $K_H G_H$ is approximately unity for this band. For R35-2 equal to zero $K_D G_D$ does approach $K_{14} G_{14}$ within this band and there is some interaction between the positive feedback of $K_{14} G_{14}$ and the negative feedback of $K_D G_D$. This causes a variation in the gain and phase of $K_H G_H$ in the vicinity where this happens. The resultant $K_H G_H$ curve is plotted in Fig. 1.2.6 (SB-48766-G). The curves for $K_H G_H$ are then subtracted from $K_D G_D$ and the result is $K_F G_F$ (also plotted in Fig. 1.2.6) for the two extreme values of R35-2.

$K_E G_E$ (Eq. 1.2.3) is obtained by first adding the curves for $K_F G_F$ (Fig. 1.2.6) and $K_C G_C$ (Fig. 1.2.3) to obtain the product $K_F G_F K_C G_C$. $K_F G_F K_{CS} G_{CS}$ is plotted in Fig. 1.2.7 (SB-48770-G) and $K_F G_F K_{CD} G_{CD}$ is plotted in Fig. 1.2.8 (SB-48771-G). These product curves are next transferred to the M-N contour charts Fig. 1.2.8a SA-48783-G and Fig. 1.2.8b SA-48784G and separate curves for $K_E G_E$ replotted. $K_{ES} G_{ES}$ for SD is plotted in Fig. 1.2.9 (SB-48772-G), and $K_{ED} G_{ED}$ for DD is plotted in Fig. 1.2.10 (SB-48773-G).

The overall transfer function for the common mode, KG_{cm}, is finally obtained by adding the curves for $K_{12} G_{12}$ (Fig. 3.5.4 supplement #1, SB-48762-G) and $K_E G_E$ (Fig. 1.2.9 or 1.2.10, and subtracting the curve

for $K_F G_F$ (Fig. 1.2.6). The two overall transfer functions (one for SD and one for DD) are plotted separately in Figs. 1.2.11 (SB-48776-G), and 1.2.12 (SB-48775-G).

In Figs. 1.2.8a and 1.2.8b it will be noticed that when R35-2 is set to zero, the gain of $K_F G_F K_C G_C$ is greater than unity as the phase shift crosses the 180° axis. This indicates that the amplifier is oscillating, and the curves in Figs. 1.2.9 and 1.2.10 are not valid for this condition. However, they are carried through to Figs. 1.2.11 and 1.2.12 merely to indicate the direction in which the magnitude and phase characteristics of the frequency response will change as R-35-2 is varied from its maximum value of five kilohms to zero.

An analysis of Eq. 1.2.2 and the calculated DC gains of the various transfer function shows that the common mode gain of this amplifier at very low frequencies is -51db. In other words the attenuation to common mode signals on the input terminals of the amplifier is 51db (approximately 350:1).

Figs. 1.2.11 and 1.2.12 indicate that as the frequency increases the attenuation decreases to approximately 25 db (18:1) in the range from 10Kc to 100Kc with R35-2 set at its maximum value. As R35-2 is decreased the rise time characteristic of the common mode response are improved but at a further loss of attenuation to common mode variations. In adjusting the amplifier common mode response, care must be taked not to attempt to improve the rise time characteristics anymore than necessary because of the loss of this attenuation.

It will also be noticed that even though much attenuation can be lost in the 10Kc to 100Kc region by varying R35-2, relatively no change is produced in the high attenuation of the amplifier to 60 or 180 cycle power supply ripple.

1.3 Non-linear Effects In Line Driver

The previous two sections have analyzed the amplifier for both differential and common mode signals from a purely linear balanced approach. Because of the tolerances in components it can not be guaranteed that the two sides of the amplifier are balanced. However, even if perfect components are assumed, considerable non-linearity exists because of the large voltage swings involved in the output stage. As the differential output voltage swing increases, the operating points of the two sides of the output stage begin to separate, the amount of separation being a function of the differential output voltage. As these operating points separate, they enter regions of increased and decreased gm simultaneously causing the gain and frequency response of the two sides to differ. Since the voltage swings within the preamp are considerably smaller, it can be assumed that all the existing non-linearity is caused by the output stage. From this consideration it can be seen that the analyses in sections 1.1 and 1.2 apply only for very small signal excursions in a region where the gains of the two sides of the amplifier are identical.

In the differential mode analysis of section 1.1 the differential transfer function was given as

Eq. 1.1.1 $$KG_{DIFF} = \frac{K_{11} G_{11} K_A G_A}{1 + K_{13} G_{13} K_A G_A}$$

However, if it cannot be assumed that the forward gains of the two sides are equal, that is $K_{AA} G_{AA} \neq K_{AB} G_{AB}$, where $K_{AA} G_{AA}$ is the gain of the A side and $K_{AB} G_{AB}$ is the gain of the B side, then a more complicated expression must be used. If the two unequal gains are related to the balanced gain some simplication can be achieved. Thus, letting

$$K_{AA} G_{AA} = K_A G_A (1 + \delta_A)$$

$$K_{AB} G_{AB} = K_A G_A (1 - \delta_B)$$

where both δ and δ are themselves complex functions of frequency relating the two gains, Eq. A-12 of appendix A gives the complete differential response of the amplifier, E_{OD} is the differential output voltage, and E_D and E_C are the differential and common mode input voltages respectively.

Eq. A-12 $$E_{OD} = \frac{K_{11} G_{11} K_A G_A \left\{ E_D \left[\frac{2 + \delta_A - \delta_B}{2} + K_A G_A (K_D G_D - K_{13} G_{13})(1 + \delta_A)(1 - \delta_B) \right] + E_C (\delta_A + \delta_B) \right\}}{1 + K_A G_A K_D G_D \left(\frac{2 + \delta_A - \delta_B}{2} \right) + K_{13} G_{13} (K_A G_A)^2 (K_D G_D - K_{13} G_{13})(1 + \delta_A)(1 - \delta_B)}$$

It will be noticed that now the amplifier produces a differential response from both differential and common mode inputs (E_D and E_C). If these responses are separated by superposition, the variation of each response can be compared to the linear balanced gain. This has been done in Appendix A in Eq. A-14 and A-16.

Eq. A-14 $$\frac{E_{OD}/E_D}{KG_{DIFF}} = \frac{(1 + K_{13} G_{13} K_A G_A) \left[1 + \frac{\delta_A - \delta_B}{2} + K_A G_A (K_D G_D - K_{13} G_{13})(1 + \delta_A)(1 - \delta_B) \right]}{1 + K_A G_A K_D G_D \left(1 + \frac{\delta_A - \delta_B}{2} \right) + K_{13} G_{13} (K_A G_A)^2 (K_D G_D - K_{13} G_{13})(1 + \delta_A)(1 - \delta_B)}$$

Eq. A-16 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{(1 + K_{13} G_{13} K_A G_A)(\delta_A + \delta_B)}{1 + K_A G_A K_D G_D \left(1 + \frac{\delta_A - \delta_B}{2} \right) + K_{13} G_{13} (K_A G_A)^2 (K_D G_D - K_{13} G_{13})(1 + \delta_A)(1 - \delta_B)}$$

In this present amplifier it can be shown that $K_D G_D \gg K_{13} G_{13}$ throughout its operating range when $R_{35} = 2 = 5K$ (Compare Fig. 1.2.4 showing $K_D G_D$ with Fig. 3.5.2 of supplement 1 showing $K_{13} G_{13}$ in the region below 1MC). Fig. 1.1.6 and 1.1.7 also indicate that $K_A G_A K_{13} G_{13} \gg 1$ in the region below 10Kc. Under these conditions Eq. A-14 and A-16 reduce to A-17 and A-18 in Appendix A.

Eq. A-17 $$\frac{E_{OD}/E_D}{KG_{DIFF}} = 1$$

Eq. A-18 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{K_{13} G_{13} K_A G_A (\delta_A + \delta_B)}{1 + K_D G_D K_{13} G_{13} (K_A G_A)^2 (1 + \delta_A)(1 - \delta_B)}$$

Equation A-17 shows that under the conditions that $K_D G_D \gg K_{13} G_{13}$ and $K_A G_A K_{13} G_{13} \gg 1$, the differential response of the amplifier to differential inputs remains virtually unchanged despite any unbalance in the forward gain of the amplifier. However, Eq. A-18 shows that as the unbalance increases the differential response becomes more and more susceptible to

common mode input signals. Figure 1.3.1 (SA-48777-G) shows a plot of this response under the conditions existing for $f < 10Kc$ as the unbalance factors δ_A and δ_B vary. The plot shows primarily the response for independent variation of δ and δ using only the real portion of the δ variations to simplify the plot. Two special cases are also shown, one for $\delta_A = \delta_B$, the other for the case where the gain on one side changes as the reciprocal of the gain change on the other (that is if $K_{AA}\, G_{AA} = 2K_A G_A$ then $K_{AB}\, G_{AB} = \frac{1}{2}K_A\, G_A$). The expected variations in the gains will generally fall between these two cases. The curve for $\delta_B = 1$ is the case of a single-sided amplifier and shows the improvement of this differential amplifier over a similiar single-sided amplifier for the rejection of common mode inputs.

The common mode response of the amplifier was treated in section 1.2 with the transfer function given as

Eq. 1.2.1 $$KG_{cm} = \frac{K_{12} G_{12}\, K_c G_c}{1 + K_c G_c (K_D G_D - K_{14} G_{14})}$$

For the same reasons stated in the differential analysis, this equation must also be reanalyzed for unbalanced conditions. Letting the normal balanced forward gain to common mode signals be $K_C\, G_C$, and $K_{CA}\, G_{CA}$ and $K_{CB}\, G_{CB}$ be the forward gain to common mode signals for the A and B sides respectively, assume $K_{CA}\, G_{CA} \neq K_{CB}\, G_{CB}$. Relating these unbalanced gains by the complex unbalance factors γ_A and γ_B gives

$$K_{cA}\, G_{cA} = K_c G_c (1+\gamma_A)$$

$$K_{cB}\, G_{cB} = K_c G_c (1-\gamma_B)$$

Equation B-14 of Appendix B gives the complete common mode response of the amplifier.

Eq. B-14 $$E_{oc} = \frac{E_c K_{12} G_{12} K_c G_c \left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14} (1+\gamma_A)(1-\gamma_B)\right] + E_D K_c G_c K_{12} G_{12} (\gamma_A + \gamma_B)/4}{1 + K_c G_c K_D G_D \left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14} (1+\gamma_A)(1-\gamma_B)\right] - (K_c G_c K_{14} G_{14})^2 (1+\gamma_A)(1-\gamma_B)}$$

Breaking this equation by superposition and relating the components to the balanced transfer function gives Eq. B-15 and B-18 of Appendix B.

Eq. B-15 $$\frac{E_{oc}/E_c}{KG_{cm}} = \frac{\left[1 + K_c G_c (K_D G_D - K_{14} G_{14})\right]\left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14} (1+\gamma_A)(1-\gamma_B)\right]}{1 + K_c G_c K_D G_D \left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14} (1+\gamma_A)(1-\gamma_B)\right] - (K_c G_c K_{14} G_{14})^2 (1+\gamma_A)(1-\gamma_B)}$$

Eq. B-18 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\left[1 + K_c G_c (K_D G_D - K_{14} G_{14})\right](\gamma_A + \gamma_B)/4}{1 + K_c G_c K_D G_D \left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14} (1+\gamma_A)(1-\gamma_B)\right] - (K_c G_c K_{14} G_{14})^2 (1+\gamma_A)(1-\gamma_B)}$$

The plot of $K_H\, G_H$ (Fig. 1.2.6) indicates that $K_D\, G_D \gg K_{14}\, G_{14}$ in the region $f < 100K_c$. Similarly the plot of $K_E\, G_E$ (Fig. 1.2.9 and 1.2.10) indicates that $K_C\, G_C\, K_D\, G_D \gg 1$ in the region $f < 10K_C$. Using these inequalities simplifies equations B-15 and B-18 to B-17 and B-20 of Appendix B.

Eq. B-17 $$\frac{E_{oc}/E_c}{KG_{CM}} = 1$$

Eq. B-20 $$\frac{E_{oc}/E_D}{KG_{CM}} = \frac{\gamma_A + \gamma_B}{4\left[1 + \frac{\gamma_A - \gamma_B}{2} + K_c G_c K_{14} G_{14}(1+\gamma_A)(1-\gamma_B)\right]}$$

Equation B-17 indicates that the common mode response of the amplifier to common mode signals remains constant for frequencies less than 10Kc despite any degree of unbalance. Equation B-20 indicates that as the unbalance factors increase the susceptibility of the common mode response to differential input signals increases. Figure 1.3.2 (SA-48779-G) shows a plot of this response as the unbalance factors vary. The two special cases are again plotted ($\gamma_A = \gamma_B$ and $1+\gamma_A = \frac{1}{1-\gamma_B}$) with the actual amplifier generally varying between these two cases. The case of $\gamma_B = 1$ is the case of a single-sided amplifier and indicates the advantage of this amplifier over a single-sided amplifier in rejecting common mode inputs.

1.4 Maximum Allowable Differential Swing from Line Driver

The maximum differential output swing available from the line driver is determined by the output stage. Two separate considerations are necessary: first, the necessity to maintain a fixed mean level, and secondly to stay within the allowable dissipation ratings of the stage.

1.4.1 Maximum Output Fixed by Mean Level Requirement

Figure 1.4.1 (SA-66073) is a much simplified configuration of the line driver output stage. R_O is the total resistance of the plate load resistors of the output stage, R_L is the equivalent resistance of all consoles being driven by the output stage, E_{bb} is the supply voltage, e_m is the mean level of the output referred to ground, e_{od} is the differential output swing, E_{p1} and E_{p2} are the voltages at the plates of the output tubes, and i_1 and i_2, are the currents being drawn by the output tubes.

The maximum swing in one direction will occur when one side of the output stage is completely cut-off, and the other side is drawing its maximum current. Assuming that i_1 is cut-off completely, then E_{p1}, the voltage on the plate of the "1" side is:

Eq. 1.4.1a $$E_{p1} = e_m + \frac{e_{od}}{2}$$

The differential output voltage at this time is

Eq. 1.4.1b $$e_{od} = (E_{bb} - E_{p1})\frac{R_L}{R_O}$$

Solving equations a and b simultaneously for e_{od} gives

Eq. 1.4.1c $$e_{od} = \frac{E_{bb} - e_m}{\frac{R_O}{R_L} + 0.5}$$

For E_{bb} = 250V and e_m = 45V this output becomes:

Eq. 1.4.1d $$e_{od} = \frac{205}{\frac{R_O}{R_L} + 0.5}$$

Since e_{od} can swing this amount in both directions, the total maximum differential peak to peak output voltage becomes twice this value:

Eq. 1.4.1e $$e_{od(pp)} = \frac{410}{\frac{R_o}{R_L} + 0.5}$$

This equation is plotted in Fig. 1.4.2 (SA-48712-G) for a range of $0.1 < \frac{R_o}{R_L} < 10$. As R_L approaches an open circuit this value approaches 820V output. For any given ratio R_o/R_L the amplifier must be operated below this calculated value or the mean level control circuit will fail to function.

1.4.2 Maximum Output Fixed by Tube Dissipation

Considering Fig. 1.4.1 again, E_{p1} is the plate voltage of the output stage at any given output voltage and can be expressed as:

Eq. 1.4.2a $$E_{p1} = e_m - \frac{e_{od}}{2}$$

The current through this side is then

Eq. 1.4.2b $$i_1 = \frac{E_{bb} - E_{p1}}{R_o} + \frac{e_{od}}{R_L}$$

Solving equations a and b simultaneously gives:

Eq. 1.4.2c $$i_1 = \frac{1}{R_o}\left[E_{bb} - e_m + e_{od}\left(\frac{R_o}{R_L} + 0.5\right)\right]$$

The voltage across the output tubes is

Eq. 1.4.2d $$e_b = e_m - \frac{e_{od}}{2} - E_K$$

where E_K is the cathode voltage referred to ground.
Under these conditions the plate power dissipated in the output tubes is $e_b i_1$.

Eq. 1.4.2e $$P_b = \frac{1}{R_o}\left[E_{bb} - e_m + e_{od}\left(\frac{R_o}{R_L} + 0.5\right)\right]\left[e_m - \frac{e_{od}}{2} - E_K\right]$$

For any fixed value of R_o and for a given maximum power dissipation of the output stage.

Eq. 1.4.2f $$P_{b\,MAX}\, R_o \gg \left[E_{bb} - e_m + e_{od}\left(\frac{R_o}{R_L} + 0.5\right)\right]\left[e_m - \frac{e_{od}}{2} - E_K\right]$$

Solving this inequality for R_o/R_L gives:

Eq. 1.4.2g $$\frac{R_o}{R_L} \ll \frac{P_{b\,MAX}\, R_o}{e_m - E_K - \frac{e_{od}}{2}} + \frac{e_m - E_{bb}}{e_{od}} - 0.5$$

From the circuit in Fig. E75792 and known operating conditions the following values can be substitued:

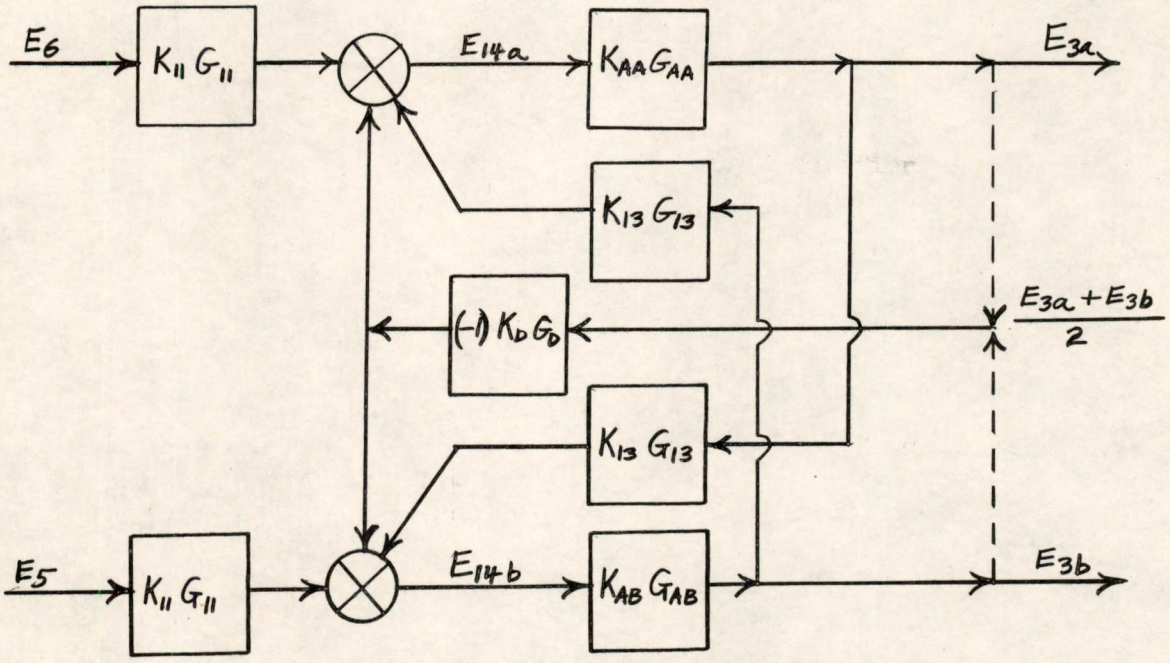
E_{bb} = 250 V

e_m = 45 V

E_K = -150 V

Appendix A

Differential Response of Complete Amplifier



Consider the Above Circuit for Differential Mode Response:

(All K_n G_n Functions Will Be Written as K_n to Simplify Notation)

A-1
$$\begin{cases} E_{3a} = E_{14a} K_{AA} \\ E_{3b} = E_{14b} K_{AB} \end{cases}$$

A-2
$$\begin{cases} E_{14a} = E_6 K_{11} + E_{3b} K_{13} - \frac{E_{3a} + E_{3b}}{2} K_D \\ E_{14b} = E_5 K_{11} + E_{3a} K_{13} - \frac{E_{3a} + E_{3b}}{2} K_D \end{cases}$$

A-3
$$E_{3a} = E_6 K_{11} K_{AA} + E_{3b} K_{AA} \left(K_{13} - \frac{K_D}{2}\right) - E_{3b} \frac{K_{AA} K_D}{2}$$

A-4
$$E_{3b} = E_5 K_{11} K_{AB} + E_{3a} K_{AB} \left(K_{13} - \frac{K_D}{2}\right) - E_{3b} \frac{K_{AB} K_D}{2}$$

Solving Equations A-3 and A-4 For E_{3a} and E_{3b}:

A-5 $$E_{3a} = \frac{K_{AA} K_{11} \left[E_6 \left(1 + \frac{K_{AB} K_D}{2} \right) + E_5 K_{AB} \left(K_{13} - \frac{K_D}{2} \right) \right]}{\left(1 + \frac{K_{AA} K_D}{2} \right) \left(1 + \frac{K_{AB} K_D}{2} \right) - K_{AA} K_{AB} \left(K_{13} - \frac{K_D}{2} \right)^2}$$

A-6 $$E_{3b} = \frac{K_{AB} K_{11} \left[E_5 \left(1 + \frac{K_{AA} K_D}{2} \right) + E_6 K_{AA} \left(K_{13} - \frac{K_D}{2} \right) \right]}{\left(1 + \frac{K_{AA} K_D}{2} \right) \left(1 + \frac{K_{AB} K_D}{2} \right) - K_{AA} K_{AB} \left(K_{13} - \frac{K_D}{2} \right)^2}$$

The Differential Output Voltage Can Be Defined As:

A-7 $$E_{OD} = E_{3a} - E_{3b}$$

A-8 $$E_{OD} = \frac{K_{11} \left[E_6 K_{AA} - E_5 K_{AB} + K_{AA} K_{AB} \left(K_D - K_{13} \right) \left(E_6 - E_5 \right) \right]}{\left(1 + \frac{K_{AA} K_D}{2} \right) \left(1 + \frac{K_{AB} K_D}{2} \right) - K_{AA} K_{AB} \left(K_{13} - \frac{K_D}{2} \right)^2}$$

The Input Voltage Can Be Defined in Terms of Its Differential And Common Mode Components:

A-9 $$\begin{cases} E_6 = E_c + E_D/2 \\ E_5 = E_c - E_D/2 \end{cases}$$

A-10 $$E_{OD} = \frac{K_{11} \left\{ E_D \left[\frac{K_{AA} + K_{AB}}{2} + K_{AA} K_{AB} \left(K_D - K_{13} \right) \right] + E_c \left(K_{AA} - K_{AB} \right) \right\}}{\left(1 + \frac{K_{AA} K_D}{2} \right) \left(1 + \frac{K_{AB} K_D}{2} \right) - K_{AA} K_{AB} \left(K_{13} - \frac{K_D}{2} \right)^2}$$

Letting $K_{AA} = K_{AB} = K_A$

A-11 $$\boxed{K G_{DIFF} = \frac{E_{OD}}{E_D} = \frac{K_{11} K_A}{1 + K_{13} K_A}}$$

$$\frac{E_{OD}}{E_c} = 0$$

IF $K_{AA} \neq K_{AB}$

LET $\begin{cases} K_{AA} = K_A(1+\delta_A) \\ K_{AB} = K_A(1+\delta_B) \end{cases}$

A-12 $$E_{OD} = \frac{K_{11}K_A\left\{E_D\left[1+\frac{\delta_A-\delta_B}{2}+K_A(K_D-K_{13})(1+\delta_A)(1-\delta_B)\right]+E_C(\delta_A+\delta_B)\right\}}{1+K_AK_D\left(1+\frac{\delta_A-\delta_B}{2}\right)+K_A^2K_{13}(K_D-K_{13})(1+\delta_A)(1-\delta_B)}$$

E_{OD} is the superposition of two components, one due to the differential input, and one due to the common input. These two components will be analyzed separately.

A-13 $$\frac{E_{OD}}{E_D} = \frac{K_{11}K_A\left[1+\frac{\delta_A-\delta_B}{2}+K_A(K_D-K_{13})(1+\delta_A)(1-\delta_B)\right]}{1+K_AK_D\left(1+\frac{\delta_A-\delta_B}{2}\right)+K_A^2K_{13}(K_D-K_{13})(1+\delta_A)(1-\delta_B)}$$

A-14 $$\frac{E_{OD}/E_D}{KG_{DIFF}} = \frac{(1+K_{13}K_A)\left[1+\frac{\delta_A-\delta_B}{2}+K_A(K_D-K_{13})(1+\delta_A)(1-\delta_B)\right]}{1+K_AK_D\left(1+\frac{\delta_A-\delta_B}{2}\right)+K_A^2K_{13}(K_D-K_{13})(1+\delta_A)(1-\delta_B)}$$

A-15 $$\frac{E_{OD}}{E_C} = \frac{K_{11}K_A(\delta_A+\delta_B)}{1+K_AK_D\left(1+\frac{\delta_A-\delta_B}{2}\right)+K_A^2K_{13}(K_D-K_{13})(1+\delta_A)(1-\delta_B)}$$

A-16 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{(1+K_{13}K_A)(\delta_A+\delta_B)}{1+K_AK_D\left(1+\frac{\delta_A-\delta_B}{2}\right)+K_A^2K_{13}(K_D-K_{13})(1+\delta_A)(1-\delta_B)}$$

FOR $K_A K_{13} \gg 1$ AND $K_D \gg K_{13}$

A-17 $$\frac{E_{OD}/E_D}{KG_{DIFF}} = 1$$

A-18 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{K_{13}K_A(\delta_A + \delta_B)}{1 + K_A^2 K_{13} K_D (1+\delta_A)(1-\delta_B)}$$

Under low frequency operation

$K_A \approx 52db$ $K_{13} = -21db$ $K_D \approx 42db$

Thus for $\delta_A \gg 0$ AND $1 \gg (1-\delta_B) \rangle 10^{-4}$

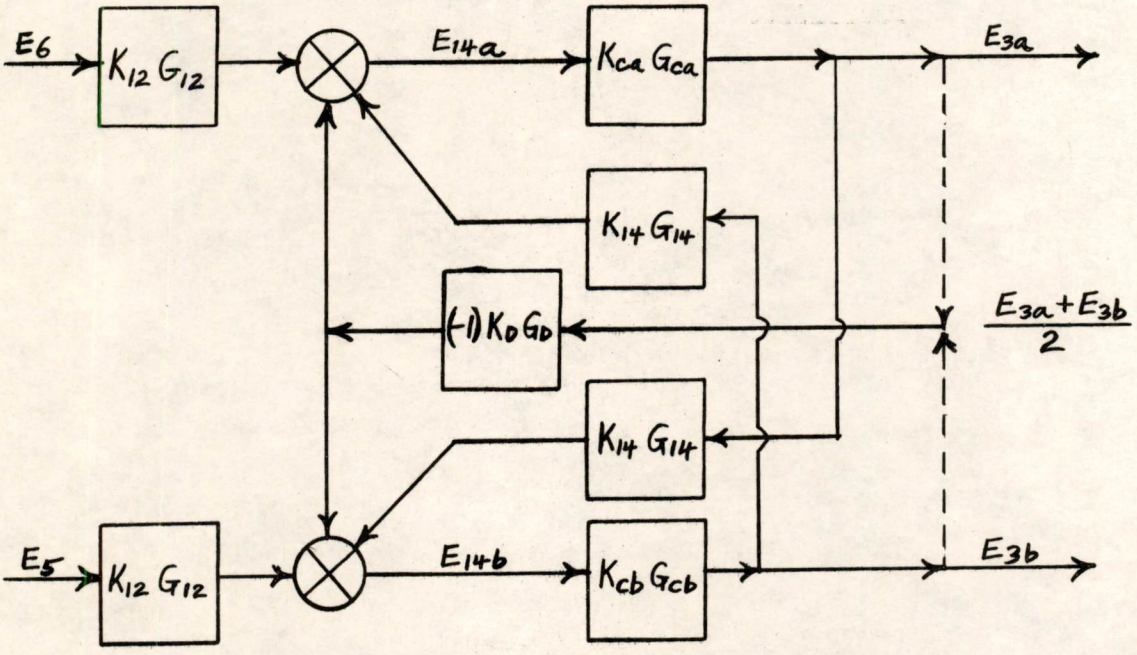
A-19 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{\delta_A + \delta_B}{K_A K_D (1+\delta_A)(1-\delta_B)}$$

FOR $\delta_B = 1$

A-20 $$\frac{E_{OD}/E_C}{KG_{DIFF}} = \frac{2K_{13}}{K_D} \approx -57db$$

Appendix B

Common Mode Response of Complete Amplifier



Considering the above circuit for common mode response:
(All K_n G_n functions will be written K_n to simplify notation)

B-1
$$\begin{cases} E_{3a} = E_{14a} K_{ca} \\ E_{3b} = E_{14b} K_{cb} \end{cases}$$

B-2
$$\begin{cases} E_{14a} = E_6 K_{12} - E_{3a} \frac{K_D}{2} + E_{3b} \left(K_{14} - \frac{K_D}{2}\right) \\ E_{14b} = E_5 K_{12} - E_{3b} \frac{K_D}{2} + E_{3a} \left(K_{14} - \frac{K_D}{2}\right) \end{cases}$$

B-3 $$E_{3a} = \frac{E_6 K_{12} K_{ca} + E_{3b} K_{ca} \left(K_{14} - \frac{K_D}{2}\right)}{1 + \frac{K_{ca} K_D}{2}}$$

B-4 $$E_{3b} = \frac{E_5 K_{12} K_{cb} + E_{3a} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)}{1 + \frac{K_{cb} K_D}{2}}$$

Solving equations B-3 and B-4 for E_{3a} and E_{3b} gives:

B-5 $$E_{3a} = \frac{E_6 K_{12} K_{ca} \left(1 + \frac{K_D K_{cb}}{2}\right) + E_5 K_{12} K_{ca} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)}{\left(1 + \frac{K_D K_{ca}}{2}\right)\left(1 + \frac{K_D K_{cb}}{2}\right) - K_{ca} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)^2}$$

B-6 $$E_{3b} = \frac{E_5 K_{12} K_{cb} \left(1 + \frac{K_D K_{cb}}{2}\right) + E_6 K_{12} K_{ca} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)}{\left(1 + \frac{K_D K_{ca}}{2}\right)\left(1 + \frac{K_D K_{cb}}{2}\right) - K_{ca} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)^2}$$

The common mode variation of the output, E_{OC}, can be defined as:

B-7 $$E_{oc} = \frac{E_{3a} + E_{3b}}{2}$$

B-8 $$E_{oc} = \frac{E_6 K_{12} K_{ca} \left(1 + K_{14} K_{cb}\right) + E_5 K_{12} K_{cb} \left(1 + K_{14} K_{ca}\right)}{2\left[\left(1 + \frac{K_D K_{ca}}{2}\right)\left(1 + \frac{K_D K_{cb}}{2}\right) - K_{ca} K_{cb} \left(K_{14} - \frac{K_D}{2}\right)^2\right.}$$

If the input voltages are redefined in terms of the differential input, E_D, and the common mode input, E_C:

B-9 $$\begin{cases} E_6 = E_c + E_D/2 \\ E_5 = E_c - E_D/2 \end{cases}$$

B-10 $$E_{oc} = \frac{E_c K_{12}(K_{ca}+K_{cb}+2K_{14}K_{ca}K_{cb}) + \frac{E_D}{2} K_{12}(K_{ca}-K_{cb})}{2\left[1+\frac{K_D}{2}(K_{ca}+K_{cb}+2K_{14}K_{ca}K_{cb}) - K_{ca}K_{cb}K_{14}^2\right]}$$

Letting $K_{ca} = K_{cb} = K_c$

B-11 $$E_{oc} = \frac{E_c\ K_{12}K_c(1+K_{14}K_c)}{1+K_cK_D(1+K_{14}K_c) - K_c^2K_{14}^2}$$

B-12 $$\boxed{K G_{cm} = \frac{E_{oc}}{E_c} = \frac{K_{12}K_c}{1+K_c(K_D-K_{14})}}$$

B-13 $$E_{oc}/E_D = 0$$

FOR $K_{ca} \neq K_{cb}$

LET $$K_{ca} = K_c(1+\gamma_a)$$
$$K_{cb} = K_c(1-\gamma_b)$$

B-14 $$E_{oc} = \frac{E_c K_{12}K_c\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right] + E_D K_{12}K_c(\gamma_A+\gamma_B)/4}{1+K_DK_c\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right] - K_c^2K_{14}^2(1+\gamma_A)(1-\gamma_B)}$$

B-15 $$\frac{E_{oc}/E_c}{KG_{cm}} = \frac{\left[1+K_c(K_D-K_{14})\right]\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right]}{1+K_DK_c\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right] - K_c^2K_{14}^2(1+\gamma_A)(1-\gamma_b)}$$

The normal values of specific transfer functions at low frequencies are:

$K_c = +15db$ $K_D = +41db$ $K_{14} = -16db$

$K_D \gg K_{14}$ AND $K_cK_D \gg 1$

Letting $K_D \gg K_{14}$ first gives

B-16 $$\frac{E_{oc}/E_c}{KG_{cm}} = \frac{(1+K_cK_D)\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right]}{1+K_cK_D+K_cK_D\left[\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right]}$$

$$\frac{E_{oc}/E_c}{KG_{cm}} = \frac{1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)}{1+\frac{K_cK_D}{1+K_cK_D}\left[\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right]}$$

Then letting $K_cK_D \gg 1$

$$\frac{K_cK_D}{1+K_cK_D} \approx 1$$

B-17 $$\frac{E_{oc}/E_c}{KG_{cm}} \approx 1$$

B-18 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\left[1+K_c(K_D-K_{14})\right](\gamma_a+\gamma_b)/4}{1+K_DK_c\left[1+\frac{\gamma_a-\gamma_b}{2}+K_{14}K_c(1+\gamma_a)(1-\gamma_b)\right]-K_c^2K_{14}^2(1+\gamma_a)(1-\gamma_b)}$$

FOR $K_D \gg K_{14}$

B-19 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{(1+K_cK_D)(\gamma_a+\gamma_b)/4}{1+K_cK_D+K_cK_D\frac{\gamma_a-\gamma_b}{2}+K_c^2K_DK_{14}(1+\gamma_a)(1-\gamma_b)}$$

$$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{(\gamma_a+\gamma_b)/4}{1+\frac{K_cK_D}{1+K_cK_D}\left[\frac{\gamma_a-\gamma_b}{2}+K_cK_{14}(1+\gamma_a)(1-\gamma_b)\right]}$$

FOR $K_cK_D \gg 1$ $\frac{K_cK_D}{1+K_cK_D} \approx 1$

B-20 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\gamma_a+\gamma_b}{4\left[1+\frac{\gamma_a-\gamma_b}{2}+K_cK_{14}(1+\gamma_a)(1-\gamma_b)\right]}$$

Considering two special cases:

First: $\gamma_a = \gamma_b = \gamma$

B-21 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\gamma}{2\left[1+K_cK_{14}(1-\gamma^2)\right]} = \frac{\gamma}{2K_cK_{14}\left(\frac{1+K_cK_{14}}{K_cK_{14}} - \gamma^2\right)}$$

FOR $K_cK_{14} = -1db = .891$

B-22 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\delta}{1.78(2.12-\delta^2)}$$

Secondly: $(1+\gamma_a)(1-\gamma_b) = 1$

$$\gamma_b = \frac{\gamma_a}{1+\gamma_a} \; ; \; \gamma_a + \gamma_b = \frac{\gamma_a(2+\gamma_a)}{1+\gamma_a} \; ; \; \gamma_a - \gamma_b = \frac{\gamma_a^2}{1+\gamma_a}$$

B-23 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\gamma_a(2+\gamma_a)/2}{2(1+K_cK_{14})(1+\gamma_a)+\gamma_a^2}$$

FOR $K_cK_{14} = -1db = .891$

B-24 $$\frac{E_{oc}/E_D}{KG_{cm}} = \frac{\gamma_a(2+\gamma_a)}{2\left[3.78(1+\gamma_a)+\gamma_a^2\right]}$$

Appendix C

Glossary of Symbols

DD - Digital display. The portion of the entire display system which is exhibited on the typotron tubes.

E_{3a} - Voltage of amplifier output terminal, marked 3_a in Fig. 0.1 (E75792), measured with respect to ground.

E_{3b} - Voltage of amplifier output terminal, marked 3_b in Fig. 0.1 (E75792), measured with respect to ground.

E_5 - Voltage of amplifier input terminal E_5, marked 26_b in Fig. 0.1 (E75792), measured with respect to ground.

E_6 - Voltage of amplifier input terminal E_6, marked 26_a in Fig. 0.1 (E75792), measured with respect to ground.

E_7 - Voltage of amplifier input terminal E_7, marked 27b in Fig. 0.1 (E75792), measured with respect to ground.

E_8 - Voltage of amplifier input terminal E_8, marked 27a in Fig. 0.1 (E75792), measured with respect to ground.

E_C - Common mode input voltage to amplifier terminals E_5: E_6, or E_7: E_8. It is defined as $(E_5 + E_6)/2$, or $(E_7 + E_8)/2$.

E_D - Differential mode input voltage to amplifier terminals E_5 : E_6, or E_7 : E_8. It is defined as $(E_5 - E_6)$, or $(E_7 - E_8)$.

E_{OC} - Common mode output voltage from amplifier output points 3_a and 3_b. It is defined as $(E_{3a} + E_{3b})/2$.

E_{OD} - Differential mode output voltage from amplifier output points 3_a and 3_b. It is defined as $(E_{3a} - E_{3b})$.

G - The frequency variant portion of a circuit transfer function. If the transfer function is a complex number in the form

$$KG = \frac{(a_1+jfb_1)(a_2+jfb_2)\cdots\cdots(a_n+jfb_n)}{(c_1+jfd_1)(c_2+jfd_2)\cdots\cdots(c_m+jfd_m)}$$

where a_n, b_n, c_m, and d_m are all constant terms, then G is defined as:

$$G = \frac{(1+jfb_1/a_1)(1+jfb_2/a_2)\cdots\cdots(1+jfb_n/a_n)}{(1+jfd_1/c_1)(1+jfd_2/c_2)\cdots\cdots(1+jfd_m/c_m)}$$

K - The constant portion of a circuit transfer function. If the transfer function is a complex number in the form shown above, then K is defined as:

$$K = \frac{a_1 a_2 \cdots\cdots a_n}{c_1 c_2 \cdots\cdots c_m}$$

$K_1 G_1$ - The differential mode gain of the output stage (Fig. 3.1.1 of supplement 1) when this stage is loaded with a standard S. D. load. It is the ratio of the differential output at terminals 3a and 3b to the differential input at 5a and 5b. Its equation is given in Eq. 3.1.1 of supplement 1. $K_1 G_1$ is plotted in Fig. 3.1.2 of supplement 1.

$K_2 G_2$ - The common mode gain of the output stage (Fig. 3.1.1 of supplement 1) when this stage is loaded with a standard S.D. load. It is the ratio of the common mode output at terminals 3a and 3b to the common mode input at points 5a and 5b. Its equations is given in Eq. 3.1.2 of supplement 1, $K_2 G_2$ is plotted in Fig. 3.1.2 of supplement 1.

$K_3 G_3$ - The differential mode gain of the output stage (Fig. 3.1.1 of supplement 1) when this stage is loaded with a standard D.D. load. It is the ratio of the differential mode output at terminals 3a and 3b to the differential input at points 5a and 5b. Its equation is given in Eq. 3.1.3 of supplement 1. $K_3 G_3$ is plotted in Fig. 3.1.2 of supplement 1.

$K_4 G_4$ - The common mode gain of the output stage (Fig. 3.1.1 of supplement 1) when this stage is loaded with a standard D.D load. It is the ratio of the common mode output at terminals 3a and 3b to the common mode input at points 5a and 5b. Its equation is given in Eq. 3.1.4 of supplement 1. $K_4 G_4$ is plotted in Fig. 3.1.2 of supplement 1.

$K_5 G_5$ - The differential mode gain of the output driver stage (Fig. 3.2.1 of supplement 1). It is the ratio of the differential mode output at points 5a and 5b to a differential mode input at points 10a and 10b. Its equation is given in Eq. 3.2.1 of supplement 1. $K_5 G_5$ is plotted in Fig. 3.2.2 of supplement 1.

$K_6 G_6$ - The common mode gain of the output driver stage (Fig. 3.2.1 of supplement 1). It is the ratio of common mode output at points 5a and 5b to the common mode input at points 10a and 10b. Its equation is given in Eq. 3.2.2 of supplement 1. $K_6 G_6$ is plotted in Fig. 3.2.2 of supplement 1.

$K_7 G_7$ - The differential mode gain of the buffer cathode follower (Fig. 3.3.1 of supplement 1). It is the ratio of the differential mode output at points 10a and 10b to the differential mode inputs at points 12a and 12b. Its equation is given in Eq. 3.3.1 of supplement 1. $K_7 G_7$ is plotted in Figs. 3.3.2 of supplement 1.

$K_8 G_8$ - The common mode gain of the buffer cathode follower (Fig. 3.3.1 of supplement 1). It is the ratio of the common mode output voltage at points 10a and 10b to the common mode input at points 12a and 12b. Its equation is given in

Eq. 3.3.2 of supplement 1. K_8 G_8 is plotted in Fig. 3.3.2 of supplement 1.

$K9_a$ $G9_a$ - The differential mode gain of the differential amplifier stage (Fig. 3.4.1 of supplement 1) with R35-1 equal to zero ohms. It is the ratio of the differential mode output at points 12a and 12b to the differential mode inputs at points 14a and 14b. Its equation is given in Eq. 3.4.1 of supplement 1. $K9_a$ $G9_a$ is plotted in Fig. 3.4.2 of supplement 1.

$K9_b$ $G9_b$ - The differential mode gain of the differential amplifier stage (Fig. 3.4.1 of supplement 1) with R35-1 equal to 50K. It is the ratio of the differential mode output at points 12a and 12b to the differential mode inputs at points 14a and 14b. Its equation is given in Eq. 3.4.2 of supplement 1. $K9_b$ $G9_b$ is plotted in Fig. 3.4.2 of supplement 1.

K10 G10 - The common mode gain of the differential amplifier stage (Fig. 3.4.1 of supplement 1). It is the ratio of the common mode output at points 12a and 12b to the common mode input at points 14a and 14b. Its equation is given in Eq. 3.4.3 of supplement 1. K10 G10 is plotted in Fig. 3.4.3 of supplement 1.

K11 G11 - The differential mode transfer function of the input circuit to the differential amplifier (Fig. 3.5.1 of supplement 1). It is the ratio of the differential mode output at points 14a and 14b to the differential mode input at points E5 and E6, or E7 and E8. Its response is given in equation 3.5.1 in supplement 1 and is plotted in Fig. 3.5.2, also in supplement 1.

K12 G12 - The common mode transfer functions of the input circuit to the differential amplifier (Fig. 3.5.1 of supplement 1). It is the ratio of the common mode output at points 14a and 14b to the common mode input at points E5, E6, E7 and E8. Its response is given in Eq. 3.5.5 of supplement 1 and is plotted in Fig. 3.5.4 also in supplement 1.

K13 G13 - The differential mode transfer function of the input circuit to the differential amplifier (Fig. 3.5.1 of supplement 1). It is the ratio of the differential mode output at points 14a and 14b to the differential mode input at points C1 and C5. Its response is given in Eq. 3.5.2 in supplement 1 and is plotted in Fig. 3.5.2 also in supplement 1.

K14 G14 - The common mode transfer function of the input circuit to the differential amplifier (Fig. 3.5.1 of supplement). It is the ratio of the common mode output at points 14a and

- 14b to the common mode input at points C1 and C5. Its response is given in Eq. 3.5.4 of supplement 1 and is plotted in Fig. 3.5.4 also in supplement 1.

K15 G15 - The common mode transfer function of the input circuit to the differential amplifier (Fig. 3.5.1 of supplement 1). It is the ratio of the common mode output at points 14a and 14b to the input at point 16. Its response is given in Eq. 3.5.3 in supplement 1 and is plotted in Fig. 3.5.3 also in supplement 1.

K16 G16 - The transfer function of the reference driver cathode follower Fig. 3.6.1 of supplement 1. It is the ratio of the output at point 16 to the input at point 18. Its response is given in Eq. 3.6.1 of supplement 1 and is plotted in Fig. 3.6.2 also in supplement 1.

K17a G17a- The transfer functions of the reference amplifier Fig. 3.7.1 of supplement 1 with R35-2 equal to zero. It is the ratio of the output at point 18 to the input at point 22. Its response is given in Eq. 3.7.1 of supplement 1 and is plotted in Fig. 3.7.2 also in supplement 1.

$K17_b$ $G17_b$ The transfer function of the reference amplifier Fig. 3.7.1 of supplement 1 with R35-2 equal to 5K. It is the ratio of the output at point 18 to the input at point 22. Its response is given in Eq. 3.7.2 of supplement 1 and is plotted in Fig. 3.7.2 also in supplement 1.

K18 G18 - The transfer function of the input circuit to the reference amplifier Fig. 3.8.1 of supplement 1. It is the ratio of the output at point 22 to the common mode input at points C1 and C5. Its response is given in Eq. 3.8.1 of supplement 1 and is plotted in Fig. 3.8.2 also in supplement 1.

K_A G_A - The differential forward gain transfer functions of the balanced differential amplifier for small signals. It is the ratio of the differential output at points 3a and 3b to the differential input at points 14a and 14b. It is generally specified with a 2nd subscript to designate a specific use.

K_{AA} G_{AA} - The forward gain transfer function to small signals in side A of the differential amplifier. It is the ratio of the output signal at point 3a to an input signal at point 14a when the signal at points 14b is equal but of opposite phase to the signal at 14a.

K_{AB} G_{AB} - The forward gain transfer function to small signals in side B of the differential amplifier. It is the ratio of the output signal at point 3b to an input signal at

- point 14b when the signal at point 14a is equal but of opposite phase to the signal at 14b.

$K_{AD}\ G_{AD}$ - The differential forward gain transfer function of the balanced differential amplifier for small signals when the amplifier is used to drive the D.D. display lines. It is the ratio of the differential output at points 3_a and 3_b to the differential input at points 14a and 14b. $K_{AD}\ G_{AD}$ is shown to be the product of $K_3\ G_3$, $K_5\ G_5$, $K_7\ G_7$, and $K_9\ G_9$. It is shown schematically in Fig. 1.1.2 and its response is plotted in Fig. 1.1.3.

$K_{AS}\ G_{AS}$ - The differential forward gain transfer function of the balanced differential amplifier for small signals when the amplifier is used to drive the S.D. display lines. It is the ratio of the differential output at points 3_a and 3_b to the differential input at points 14_a and 14_b. $K_{AS}\ G_{AS}$ is shown to be the product of $K_1\ G_1$, $K_5\ G_5$, $K_7\ G_7$, and $K_9\ G_9$. It is shown schematically in Fig. 1.1.2 and its response is plotted in Fig. 1.1.3.

$K_B\ G_B$ - The differential closed loop response of the differential amplifier. It is generally specified with a 2nd subscript to designate a specific use.

$K_{BD}\ G_{BD}$ - The differential closed loop response of the differential amplifier for small signals when the amplifier is used to drive the DD display lines. It is the ratio of the differential output at points 3a and 3b to the differential input at points 14a and 14b when the output is closed to the input through K13 G13. Its response is given by Eq. 1.1.3 and is plotted in Figs. 1.1.5b and 1.1.7.

$K_{BS}\ G_{BS}$ - The differential closed loop response of the differential amplifier for small signals when the amplifier is used to drive the SD display lines. It is the ratio of the differential output at points 3a and 3b to the differential input at points 14a and 14b when the output is closed to the input through $K_{13}\ G_{13}$. Its response is given by Eq. 1.1.3 and is plotted in Figs. 1.1.5a and 1.1.6.

$K_C\ G_C$ - The common mode forward gain transfer function of the balanced differential amplifier for small signals. It is the ratio of the common mode output at points 3a and 3b to the common mode input at points 14a and 14b. It generally specified with a 2nd subscript to designate a specific use.

$K_{CA}\ G_{CA}$ - The forward gain transfer function to small signals in side A of the differential amplifier. It is the ratio of the output signal at point 3a to the input signal at

- 14a when the signals at points 14a and 14b are equal.

$K_{CB}\ G_{CB}$ - The forward gain transfer function to small signals in side B of the differential amplifier. It is the ratio of the output signal at point 3b to the input signal at point 14b when the signals at point 14a and 14b are equal.

$K_{CD}\ G_{CD}$ - The common mode transfer function of the balanced differential amplifier for small signals when the amplifier is used to drive the D.D. display lines. It is the ratio of the common mode output at points 3_a and 3_b to the common mode input at points 14_a and 14_b. $K_{CD}\ G_{CD}$ is shown to be the product of $K_4\ G_4$, $K_6\ G_6$, $K_8\ G_8$, and $K_{10}\ G_{10}$. It is shown schematically in Fig. 1.2.2 and its response is plotted in Fig. 1.2.3.

$K_{CS}\ G_{CS}$ - The common mode transfer function of the balanced differential amplifier for small signals when the amplifier is used to drive the S.D. display lines. It is the ratio of the common mode output at points 3_a and 3_b to the common mode input at points 14_a and 14_b. $K_{CS}\ G_{CS}$ is shown to be the product of $K_2\ G_2$, $K_6\ G_6$, $K_8\ G_8$ and $K_{10}\ G_{10}$. It is shown schematically in Fig. 1.2.2 and its response is plotted in Fig. 1.2.3.

$K_D\ G_D$ - The total feed-back transfer function between points C_1, C_5 and 14_a and 14_b. It is shown to be the product of $K_{15}\ G_{15}$, $K_{16}\ G_{16}$, $K_{17}\ G_{17}$, $K_{18}\ G_{18}$. It is shown schematically in Fig. 1.2.2 and is plotted in Fig. 1.2.4.

$K_E\ G_E$ - Composite transfer function used to simplify the solution of the common mode transfer function of the amplifier. Its mathematical expression is given in Eq. 1.2.3. It is generally specified with a second subscript to denote its use.

$K_{ED}\ G_{ED}$ - The expression for $K_E\ G_E$ when the amplifier is used to drive the D.D. lines. Its solution is obtained by using Figs. 1.2.8 and 1.2.8b to solve Eq. 1.2.3. Its final solution is plotted in Fig. 1.2.10.

$K_{ES}\ G_{ES}$ - The expression for $K_E\ G_E$ when the amplifier is used to drive the S.D. lines. Its solution is obtained by using Figs. 1.2.7 and 1.2.8a to solve Eq. 1.2.3. Its final solution is plotted in Fig. 1.2.9.

$K_F\ G_F$ - Composite transfer function is used to simplify the solution of the total common mode transfer function of the amplifier. Its mathematical expression is given in Fig. 1.2.5. Its final solution is plotted in Fig. 1.2.6.

KG_{CM} - The overall common mode transfer function of the display line driver. Its mathematical solution is given in Eq. 1.2.1. Its behavior is plotted in Fig. 1.2.11 when the amplifier is used in driving the S.D. lines and in Fig. 1.2.12 when used for D.D. lines.

KG_{DIFF} - The overall differential transfer function of the display line driver. Its mathematical expression is given in Eq. 1.1.1. Its behavior is plotted in Fig. 1.1.8 when the amplifier is used to drive the S.D. lines and Fig. 1.1.9 for the D.D. lines.

S.D. - Situation display. The portion of the entire display system which is exhibited on Charactron tubes.

γ_A - A frequency dependant complex variable used to compare the common mode forward gain transfer function of the line driver (K_C G_C) under large signal behavior. It is defined in appendix B prior to Eq. B-14. γ_A relates the large signal gain of side A to the balanced small signal gain.

γ_B - A frequency dependant complex variable used to compare the common mode forward gain transfer functions of the line driver (K_C G_C) under large signal behavior. It is defined in appendix B prior to Eq. B-14. γ_B relates the large signal gain of side B to the balanced small signal gain.

δ_A - A frequency dependant complex variable used to compare the differential transfer function of the line driver (K_A G_A) under large signal behavior. It is defined in appendix A prior to Eq. A-12. It relates the large signal gain of side A to the small signal balance gain.

δ_B - A frequency dependant complex variable used to compare the differential transfer function of the line driver (K_A G_A) under large signal behavior. It is defined in appendix A prior to Eq. A-12. It relates the large signal gain of side B to the small signal balance gain.

List of Illustrations

Fig. 1.2.6	(SB-48766-G)	Amplitude and Phase Response of Total Common Mode Feedback Transfer Function
Fig. 1.2.7	(SB-48770-G)	Common Mode Open Loop Transfer Function $K_F G_F K_{CS} G_{CS}$ for S.D. Display Line Driver
Fig. 1.2.8	(SB-48771-G)	Common Mode Open Loop Transfer Function $K_F G_F K_{CD} G_{CD}$ for D.D. Display Line Driver
Fig. 1.2.8a	(SA-48783-G)	Evaluation of $K_{ES} G_{ES}$ from $K_F G_F K_{CS} G_{CS}$ for Display Line Driver
Fig. 1.2.8b	(SA-48784-G)	Evaluation of $K_{ED} G_{ED}$ from $K_F G_F K_{CD} G_{CD}$ for Display Line Driver
Fig. 1.2.9	(SB-48772-G)	Common Mode Closed Loop Transfer Function $K_{ES} G_{ES}$ for S.D. Display Line Driver
Fig. 1.2.10	(SB-48773-G)	Common Mode Closed Loop Trnasfer Function $K_{ED} G_{ED}$ for D.D. Display Line Driver
Fig. 1.2.11	(SB-48776-G)	Common Mode Overall Transfer Function KG_{CM} for S.D. Display Line Driver
Fig. 1.2.12	(SB-48775-G)	Common Mode Overall Transfer Function KG_{CM} for D.D. Display Line Driver
Fig. 1.3.1	(SA-48777-G)	Differential Response to Low Frequency Common Mode Input (Display Line Driver)
Fig. 1.3.2	(SA-48779-G)	Common Mode Response to Low Frequency Differential Input (Display Line Driver)
Fig. 1.4.1	(SA-66073)	Equivalent Output of Line Driver
Fig. 1.4.2	(SA-48712-G)	Theoretical Operating Limits Line Driver Output Stage
Fig. 1.4.3	(SA-48774-G)	Limits on Peak-to-Peak Differential Output Voltage from Line Driver with 336 ohm Plate Load Resistor in Output Stage

Signed:

Henry E. Zieman

Henry E. Zieman

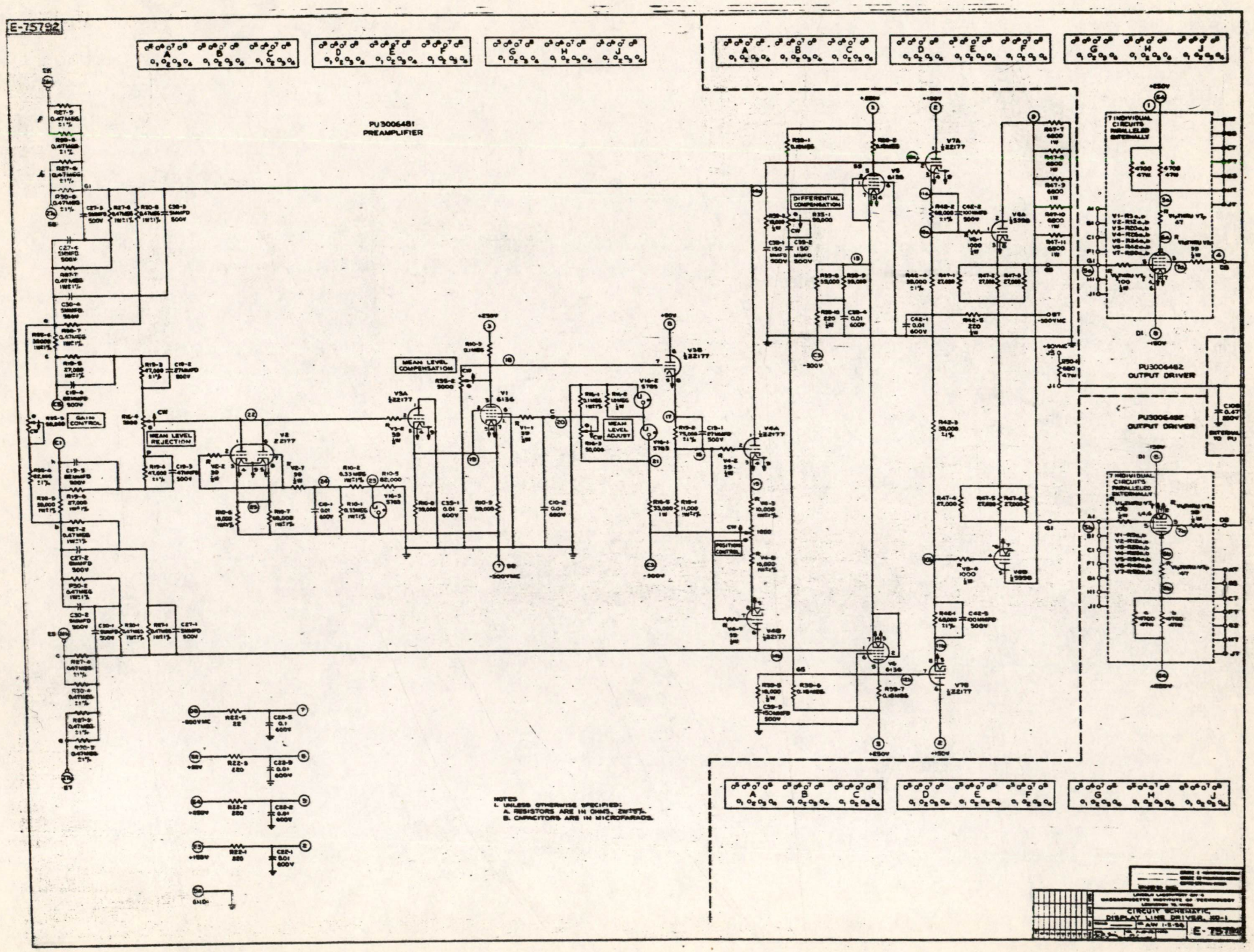
Joseph Kriensky

Joseph Kriensky

HEZ:JK:ec

Attachments:

Fig. 0.1	E 75792
Fig. 1.1.1	SA 65908
Fig. 1.1.2	SA 65921
Fig. 1.1.3	B 48756-G
Fig. 1.1.4	SA 65920
Fig. 1.1.5	B 48755-G
Fig. 1.1.5a	SA 48781-G
Fig. 1.1.5b	SA 48782-G
Fig. 1.1.6	SB 48765-G
Fig. 1.1.7	SB 48767-G
Fig. 1.1.8	SB 48768-G
Fig. 1.1.9	SB 48769-G
Fig. 1.2.1	SA 65909
Fig. 1.2.2	SA 65919
Fig. 1.2.3	SB 48763-G
Fig. 1.2.4	SB 48764-G
Fig. 1.2.5	SA 65925
Fig. 1.2.5a	SA 48780-G
Fig. 1.2.6	SB 48766-G
Fig. 1.2.7	SB 48770-G
Fig. 1.2.8	SB 48771-G
Fig. 1.2.8a	SA 48783-G
Fig. 1.2.8b	SA 48784-G
Fig. 1.2.9	SB 48772-G
Fig. 1.2.10	SB 48773-G
Fig. 1.2.11	SB 48776-G
Fig. 1.2.12	SB 48775-G
Fig. 1.3.1	SA 48777-G
Fig. 1.3.2	SA 48779-G
Fig. 1.4.1	SA 66073
Fig. 1.4.2	SA 48712-G
Fig. 1.4.3	SA 48774-G


E-75792
PU3006481
PREAMPLIFIER
PU3006482
OUTPUT DRIVER
PU3006482
OUTPUT DRIVER
DIFFERENTIAL COMPENSATION
MEAN LEVEL COMPENSATION
MEAN LEVEL REJECTION
MEAN LEVEL ADJUST
GAIN CONTROL
POSITION CONTROL
INDIVIDUAL CIRCUITS PARALLELED EXTERNALLY
NOTES
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, 2W 5%.
B. CAPACITORS ARE IN MICROFARADS.
CIRCUIT SCHEMATIC
DISPLAY LINE DRIVER, 100-1
E-75792

SA-65908

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
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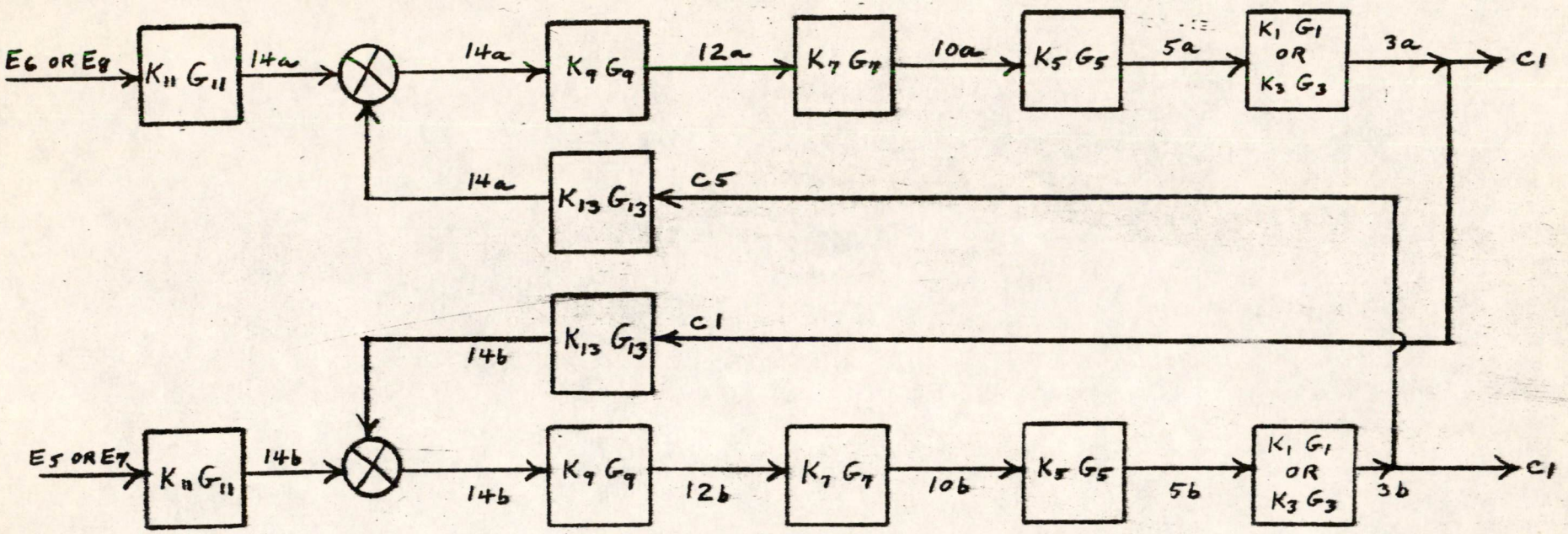

FIG. 1.1.1

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LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

COMPLETE DIFFERENTIAL TRANSFER FUNCTION OF DISPLAY LINE DRIVER

SCALE:
DR. HE Zieman
ENG. HE Zieman
CK.
APPD.
SA-65908

8M-7-54-Boston Blue Print

SA-65921

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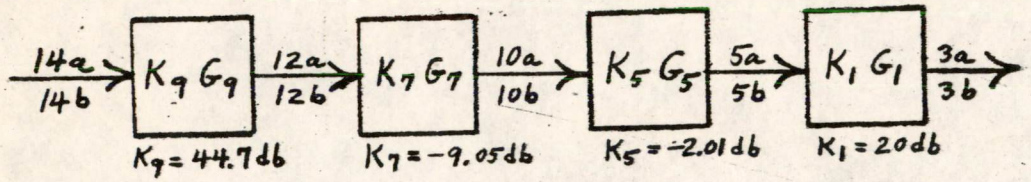
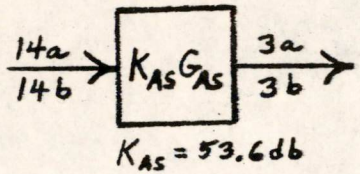
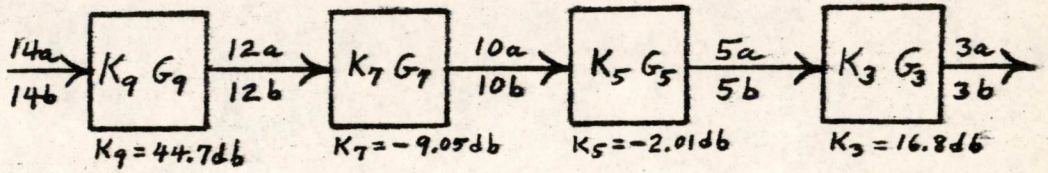
SD (SITUATION DISPLAY)





DD (DIGITAL DISPLAY)



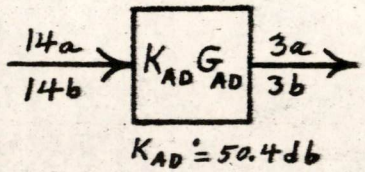


FIGURE 1.1.2

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LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

DIFFERENTIAL FORWARD GAIN TRANSFER FUNCTION OF DISPLAY LINE DRIVER

SCALE:
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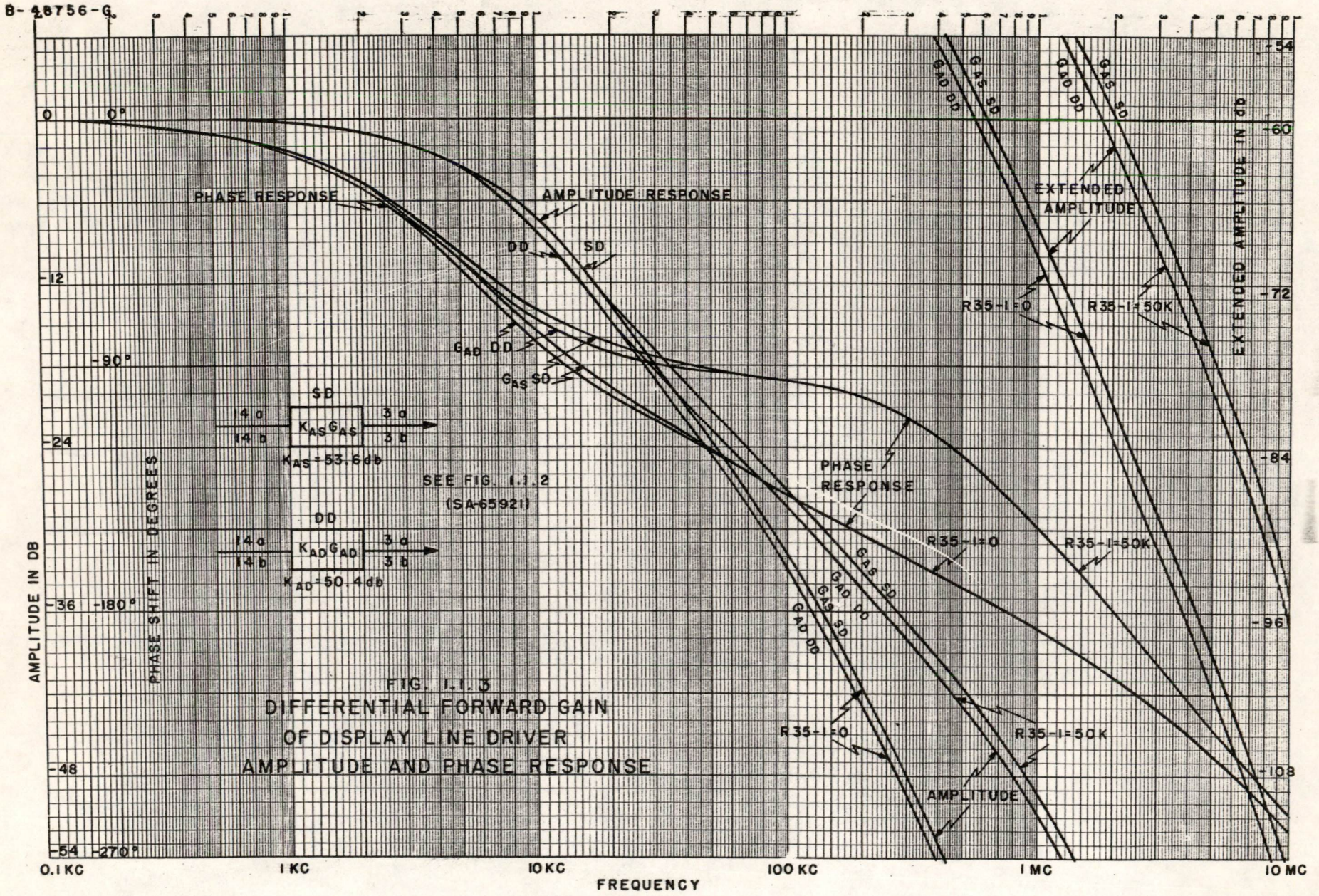

FIG. 1.1.3
DIFFERENTIAL FORWARD GAIN
OF DISPLAY LINE DRIVER
AMPLITUDE AND PHASE RESPONSE

SA-65920

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

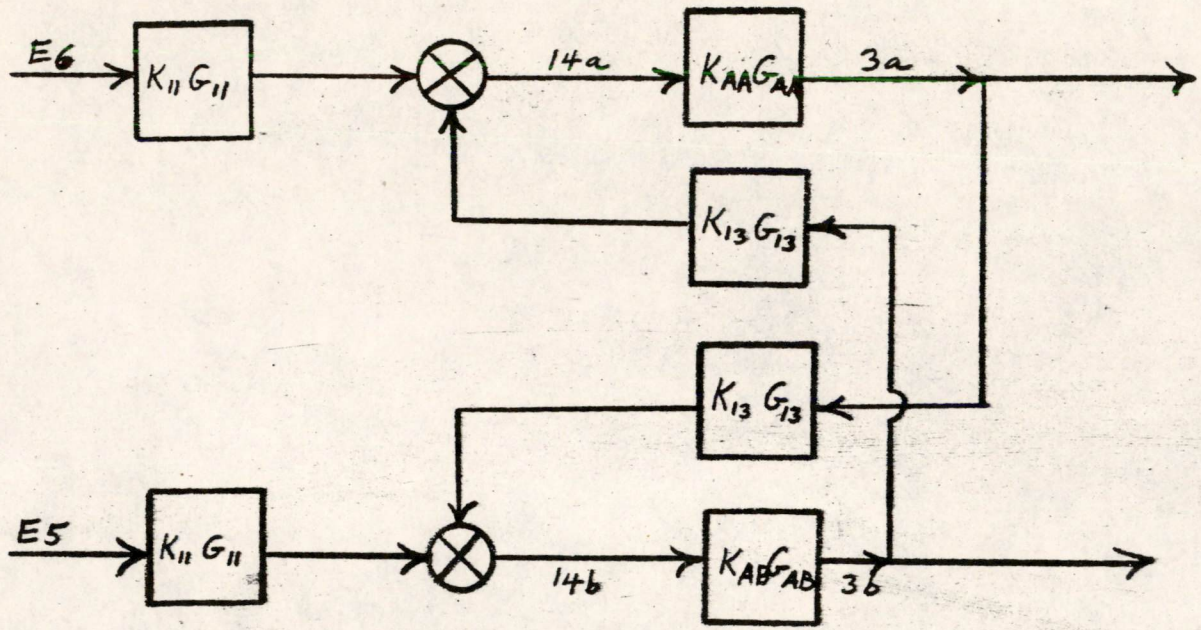

FIGURE 1.1.4

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-1		7/2/58	JHC

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

SIMPLIFIED DIFFERENTIAL TRANSFER FUNCTION OF DISPLAY LINE DRIVER

SCALE:
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CK.
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SA-65920

8M-7-54-Boston Blue Print

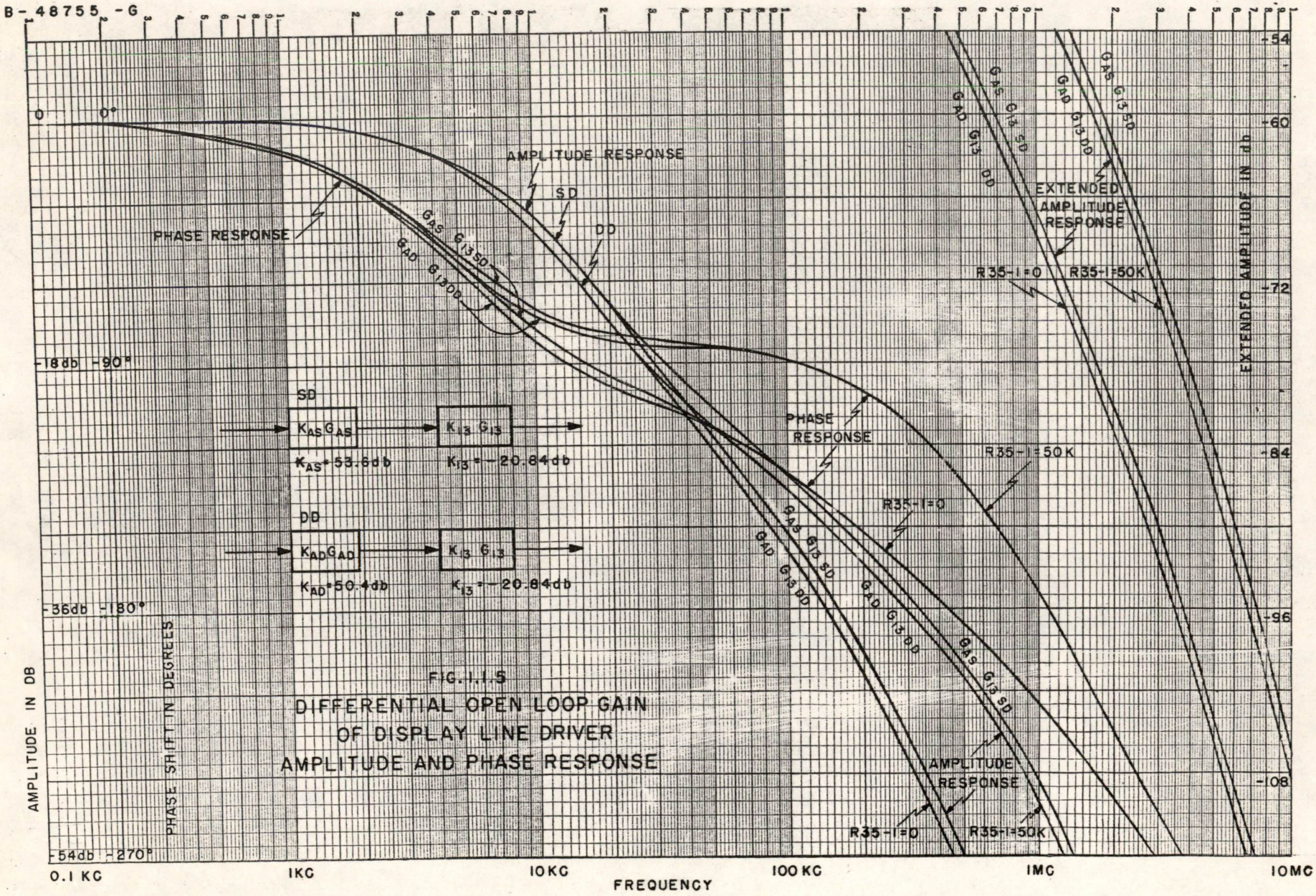
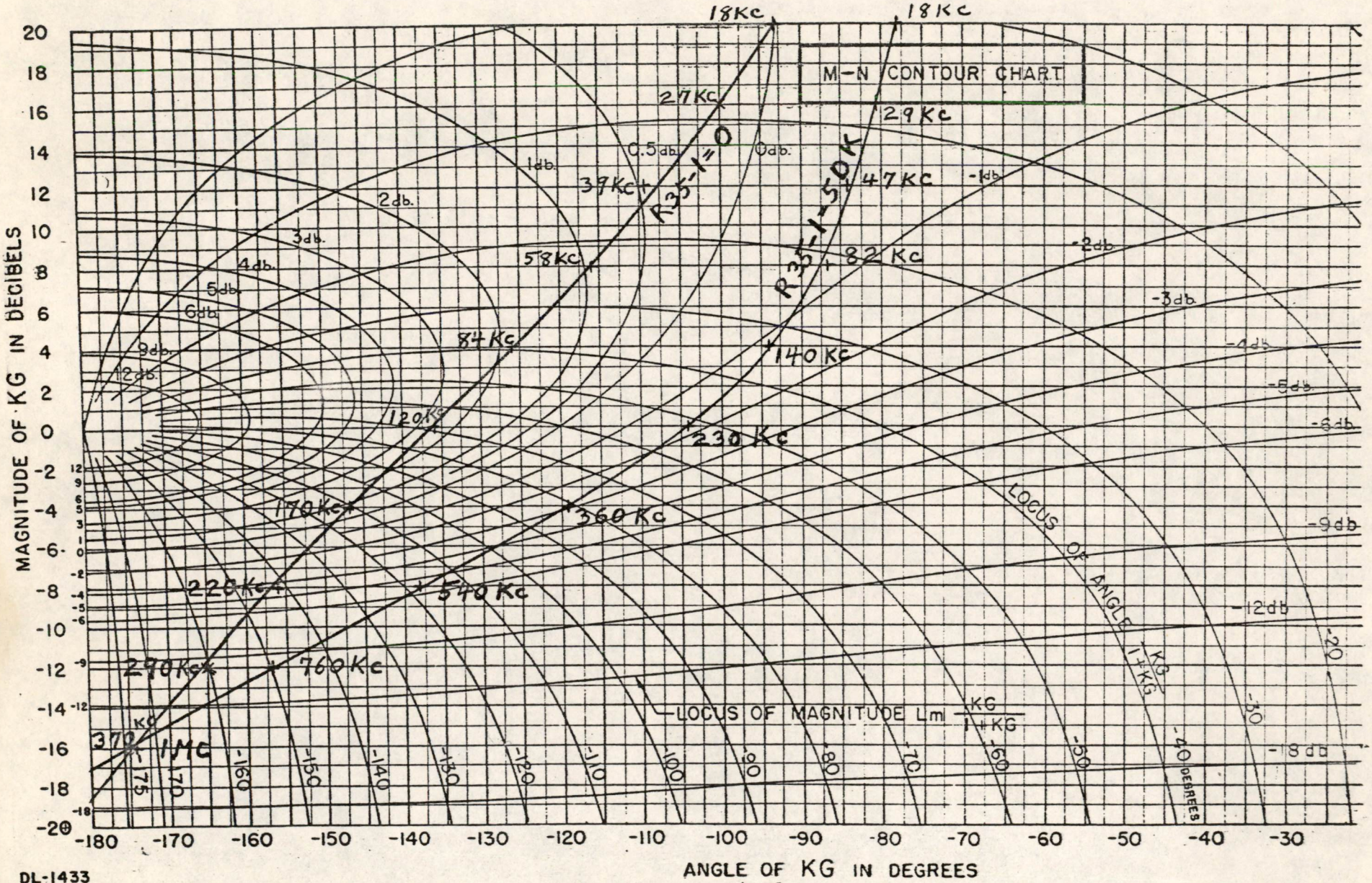


FIG. 1.1.5

DIFFERENTIAL OPEN LOOP GAIN OF DISPLAY LINE DRIVER AMPLITUDE AND PHASE RESPONSE

SA-48781-G



DL-1433

FIGURE 1.1.5a

EVALUATION OF $K_{BS}G_{BS}$ FROM $K_{AS}G_{AS}K_{13}G_{13}$

S.D. DISPLAY LINE DRIVER

SA-48781-G

SA-48782-G

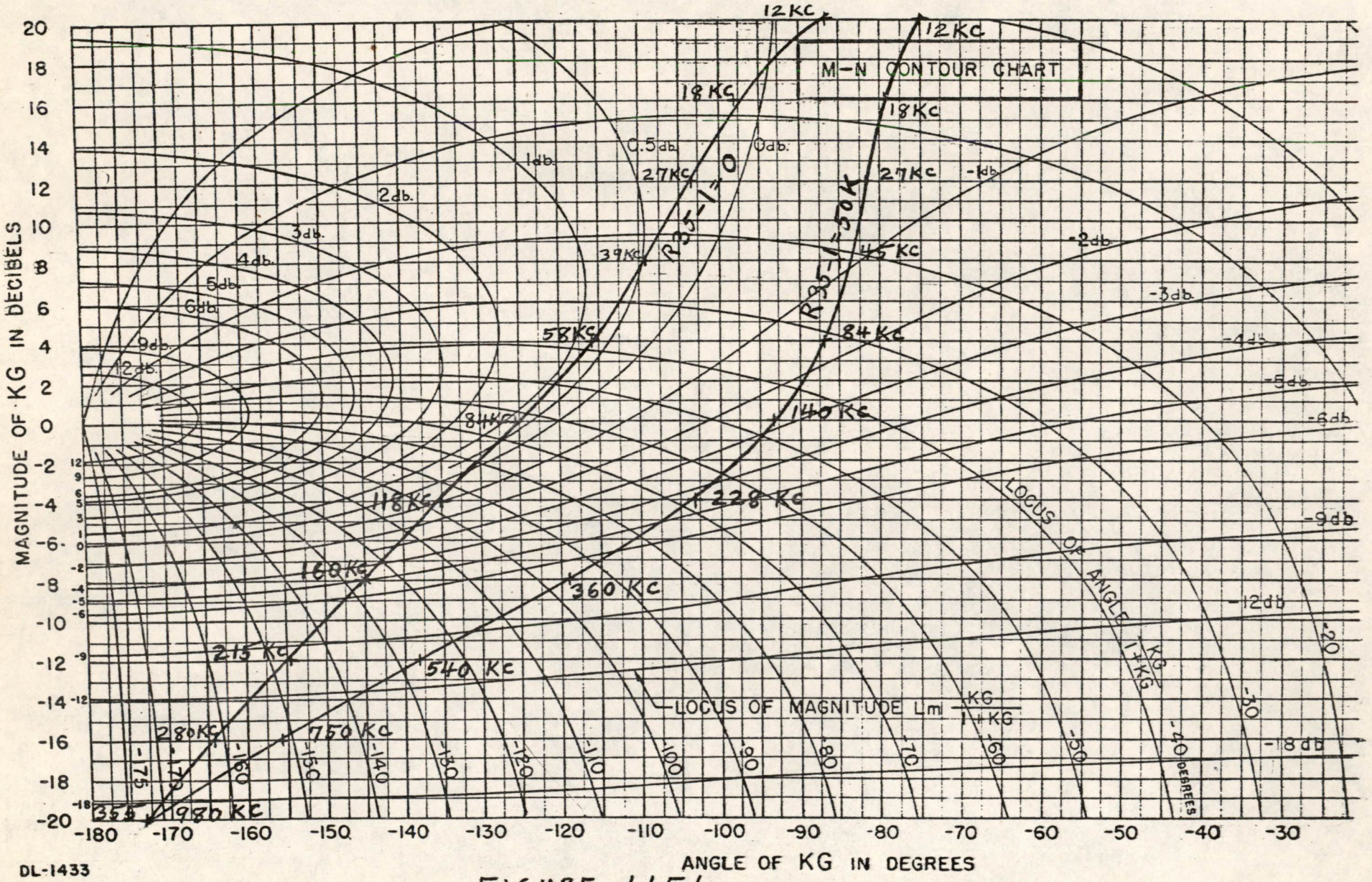


FIGURE 1.1.56

EVALUATION OF $K_{BD}\,G_{BD}$ FROM $K_{AD}\,G_{AD}\,K_{13}\,G_{13}$
D.D. DISPLAY LINE DRIVER

SA-48782-G

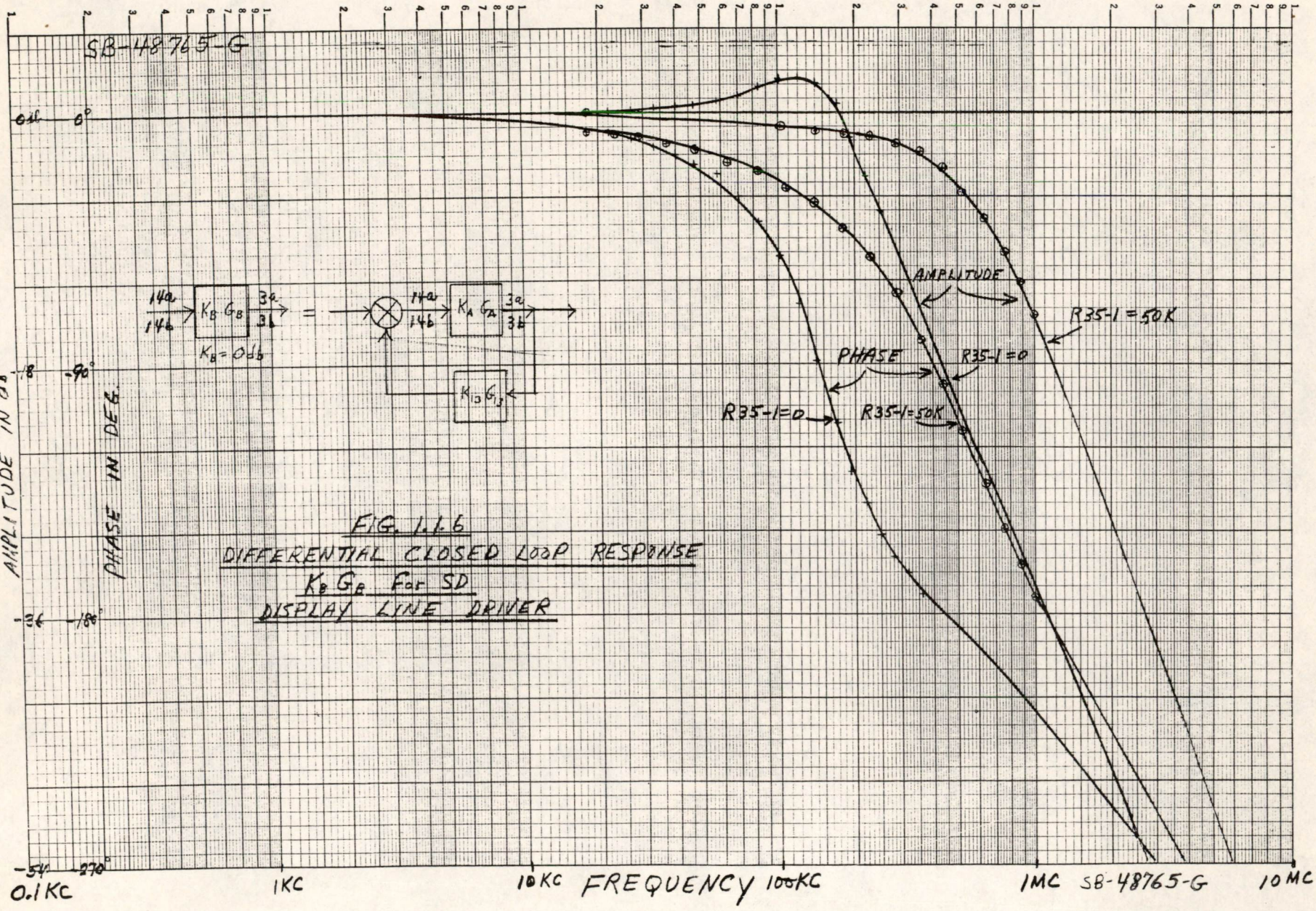


FIG. 1.1.6

DIFFERENTIAL CLOSED LOOP RESPONSE

$K_B G_B$ For SD

DISPLAY LINE DRIVER

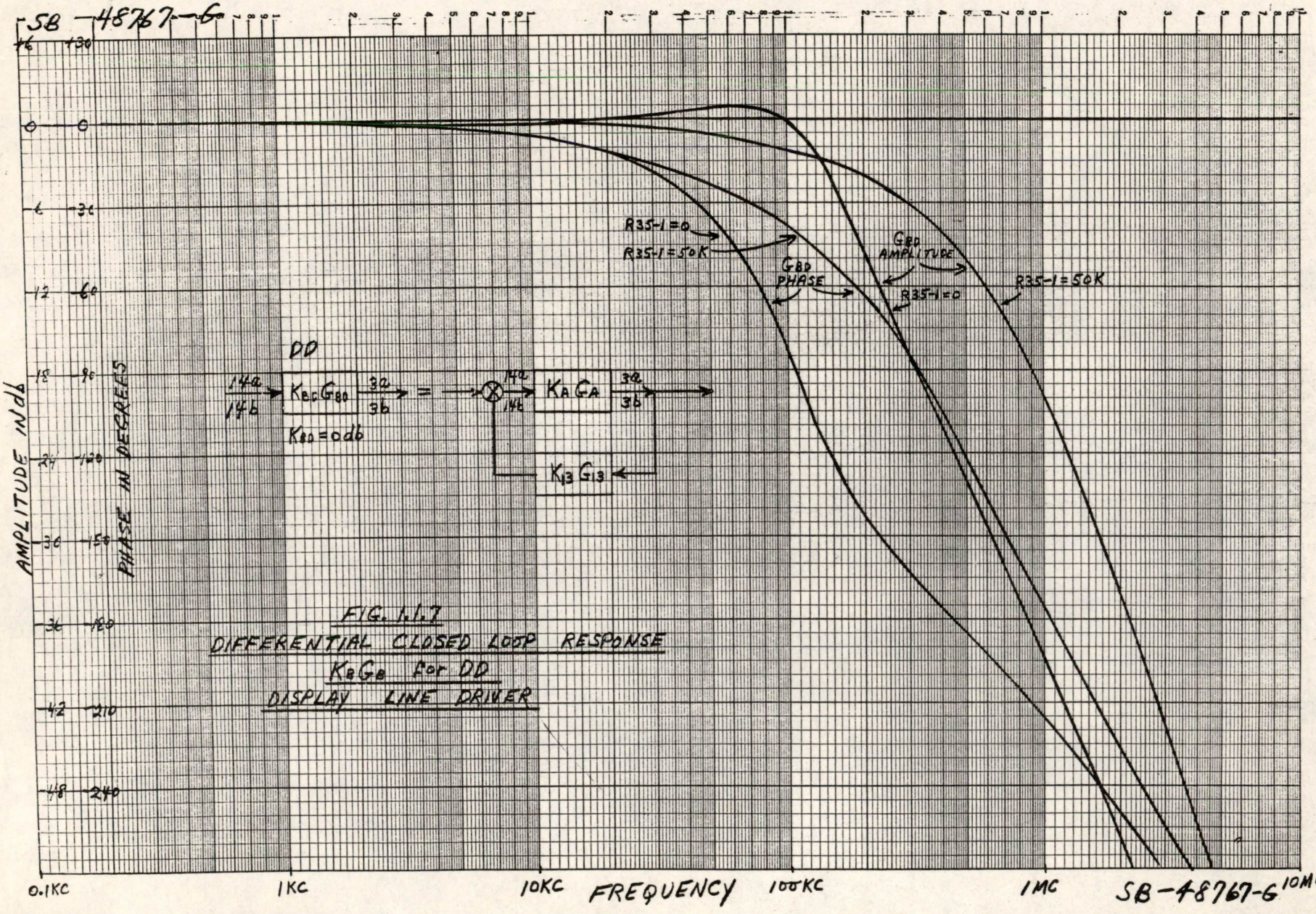


FIG. 4.1.7
DIFFERENTIAL CLOSED LOOP RESPONSE
KBGB For DD
DISPLAY LINE DRIVER

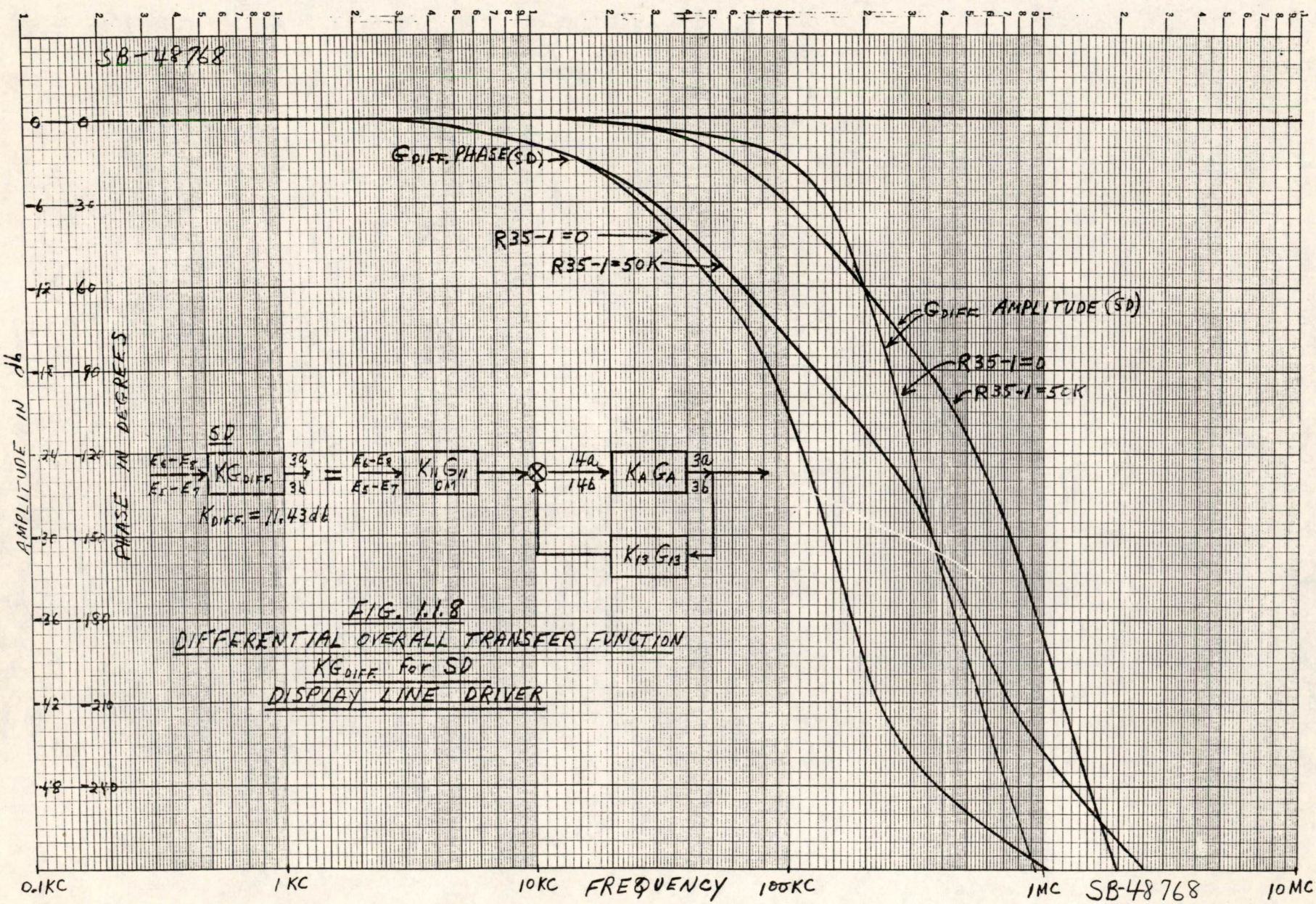


FIG. 1.1.8

DIFFERENTIAL OVERALL TRANSFER FUNCTION

$KG_{DIFF.}$ For SD

DISPLAY LINE DRIVER

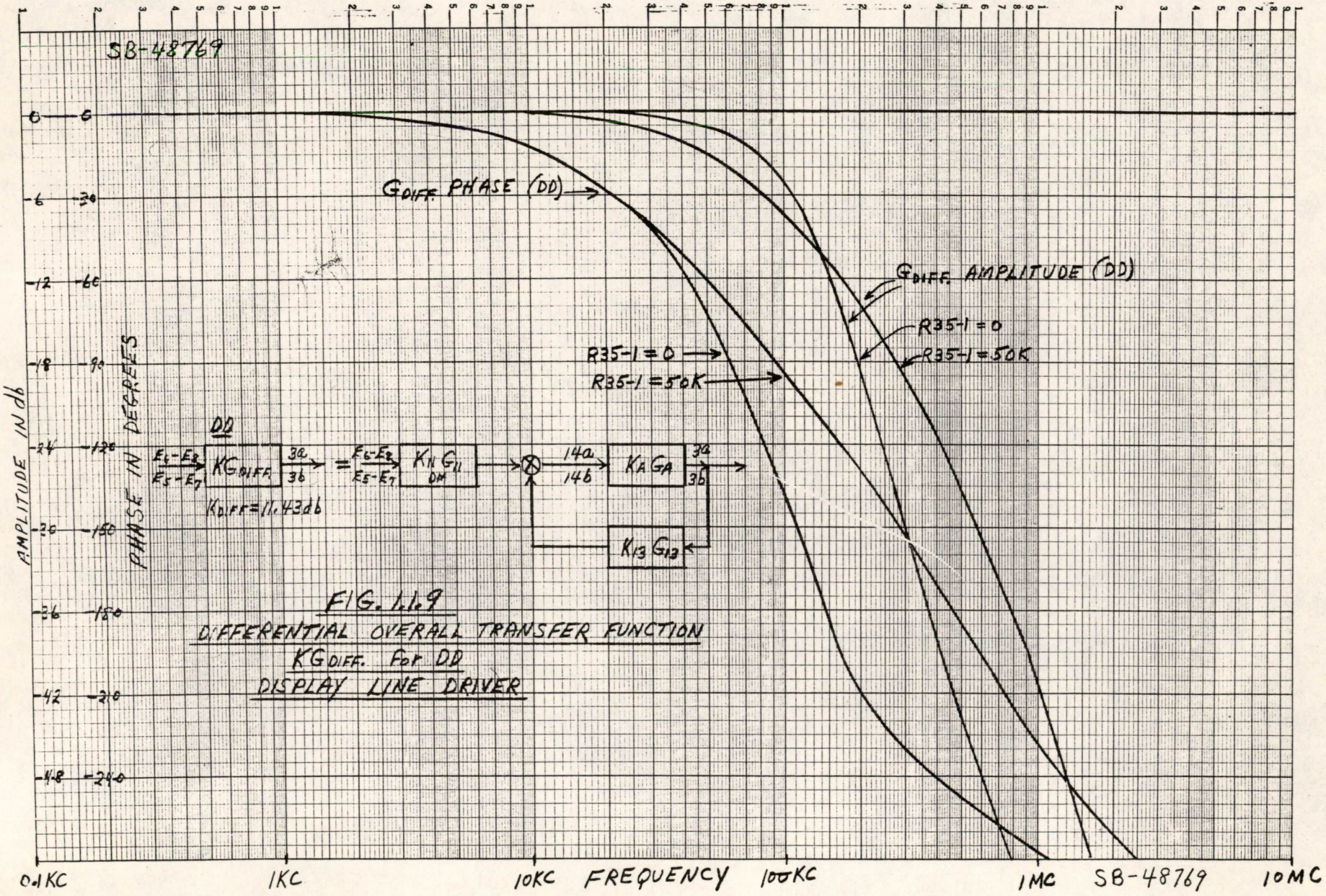


FIG. 1.1.9

DIFFERENTIAL OVERALL TRANSFER FUNCTION
KG DIFF. For DD
DISPLAY LINE DRIVER

SA-65909

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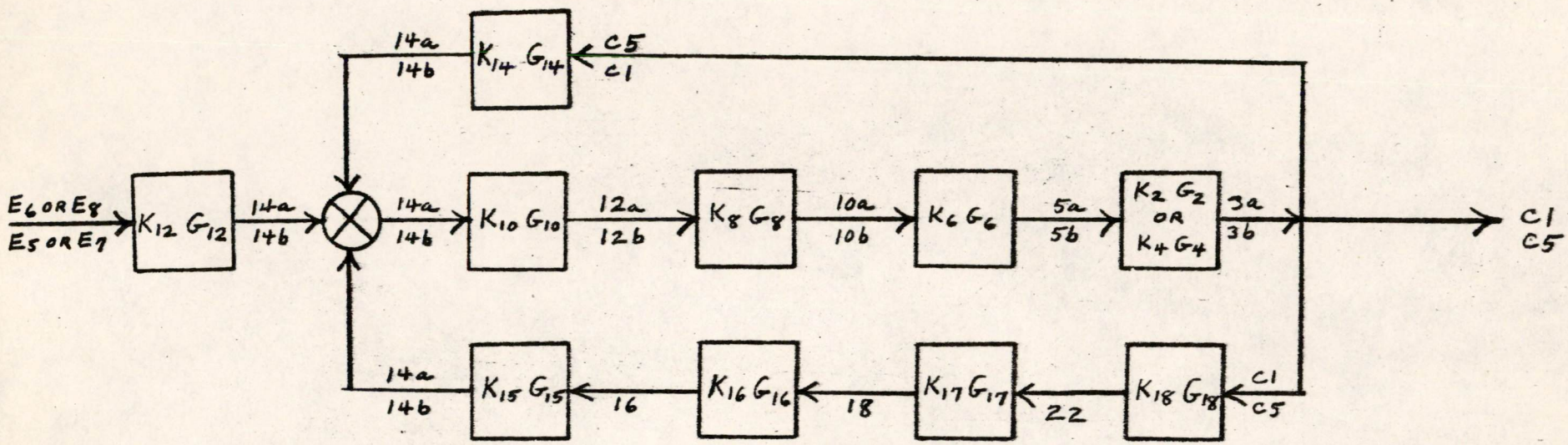

FIG. 1.2.1

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LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

COMPLETE COMMON MODE TRANSFER FUNCTION OF DISPLAY LINE DRIVER

SCALE:	DR. H E Zieman	SA-65909
ENG. H E Zieman	CK.	APPD.

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SA-65919

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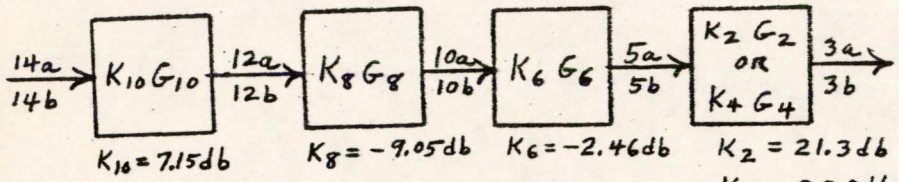
FORWARD GAIN TRANSFER FUNCTION

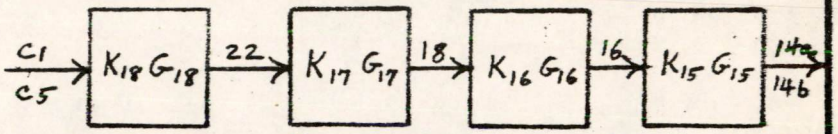


$K_{10} = 7.15db$ $K_8 = -9.05db$ $K_6 = -2.46db$ $K_2 = 21.3db$ $K_4 = 20.0db$

$K_{CS} = 16.94db$

$K_{CD} = 15.64db$

FEEDBACK TRANSFER FUNCTION



$K_{18} = -0.83db$ $K_{17} = 43.23db$ $K_{16} = -18.1db$ $K_{15} = 17.2db$

$K_D = 41.6db$

FIGURE 1.2.2

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ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

COMMON MODE TRANSFER FUNCTION SIMPLIFICATIONS

SCALE:	DR. H E Zieman	SA-65919
ENG. H E Zieman	CK.	APPD.

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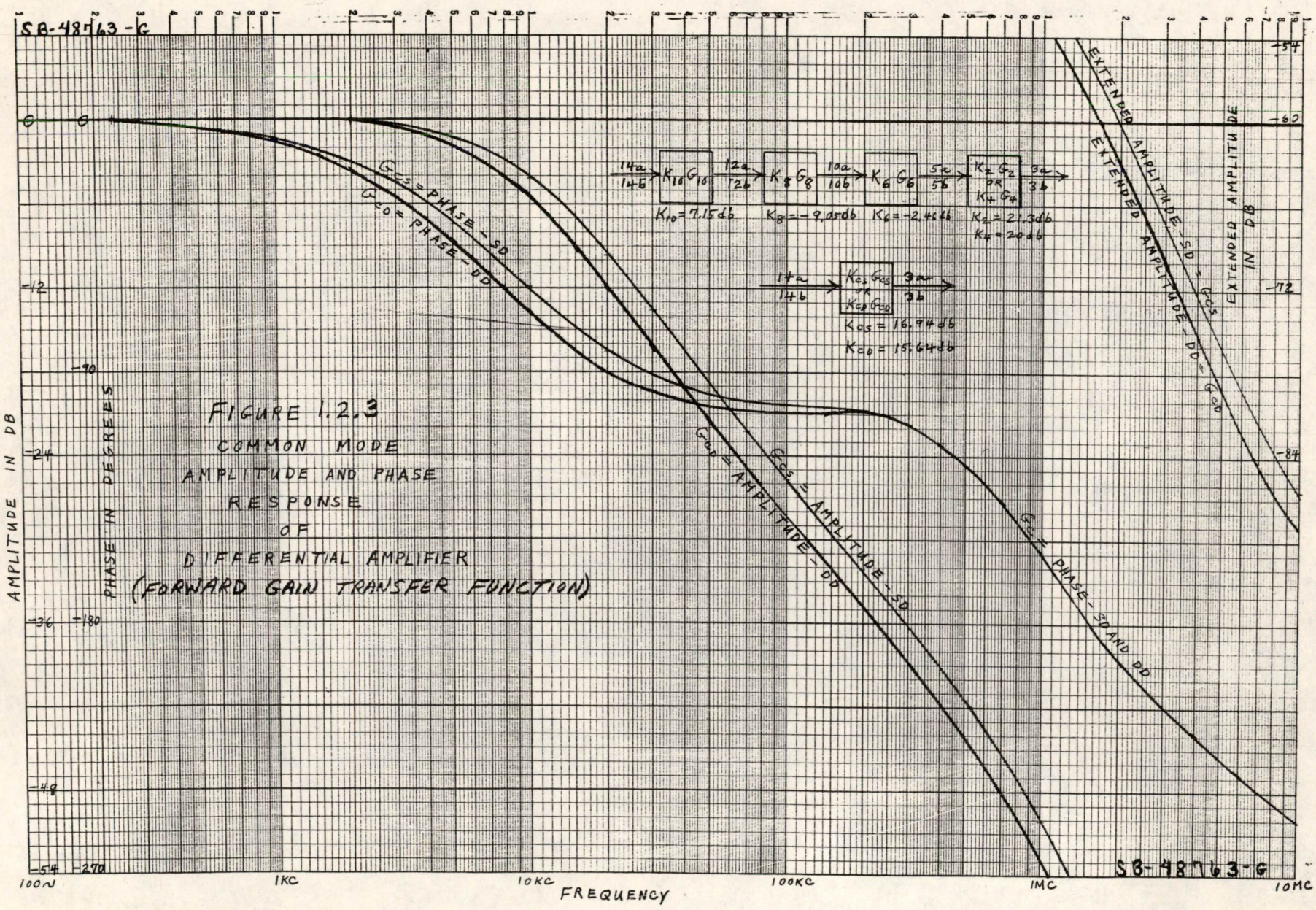

FIGURE 1.2.3
COMMON MODE
AMPLITUDE AND PHASE
RESPONSE
OF
DIFFERENTIAL AMPLIFIER
(FORWARD GAIN TRANSFER FUNCTION)

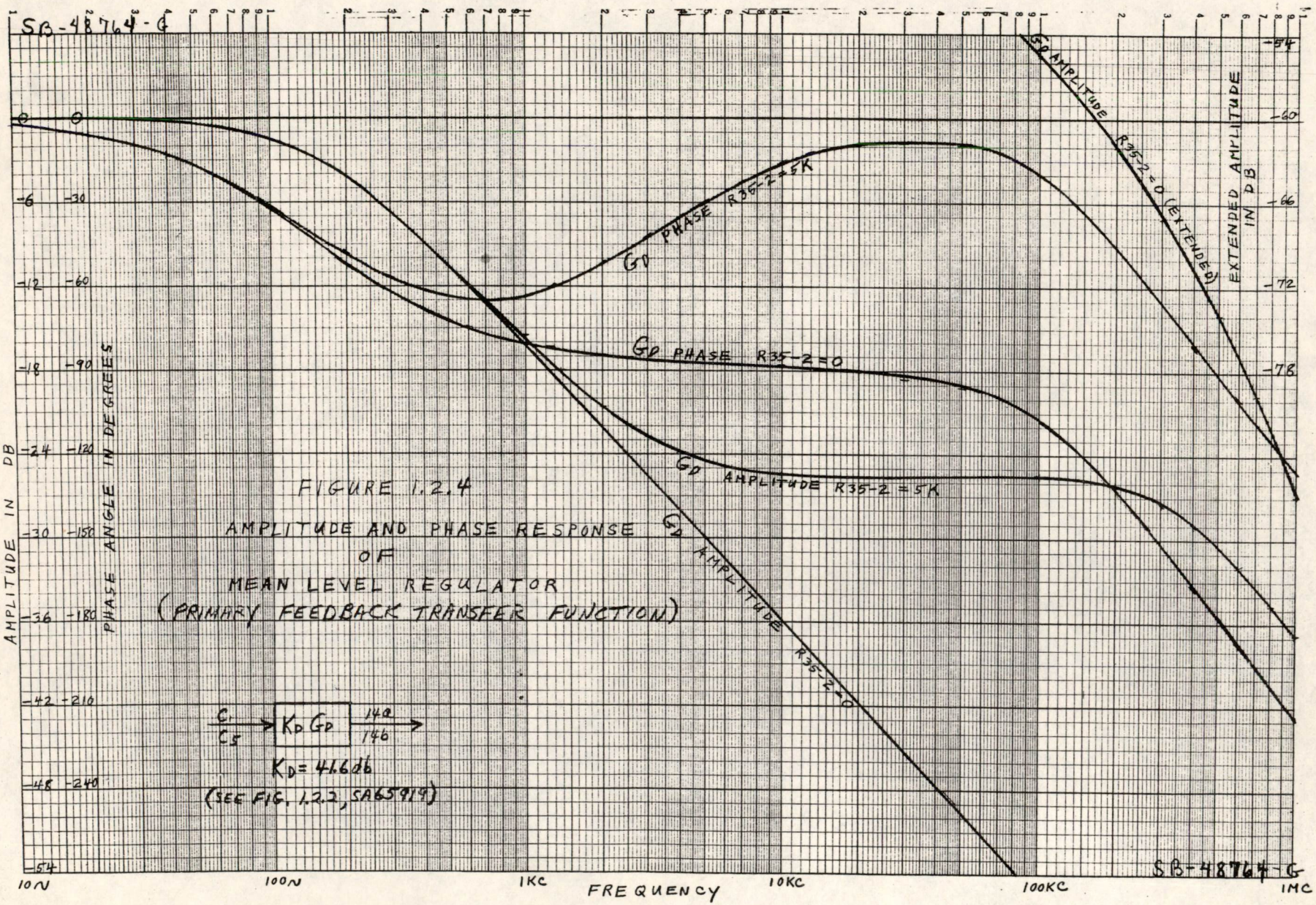

FIGURE 1.2.4

AMPLITUDE AND PHASE RESPONSE OF MEAN LEVEL REGULATOR (PRIMARY FEEDBACK TRANSFER FUNCTION)

SA-65925

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

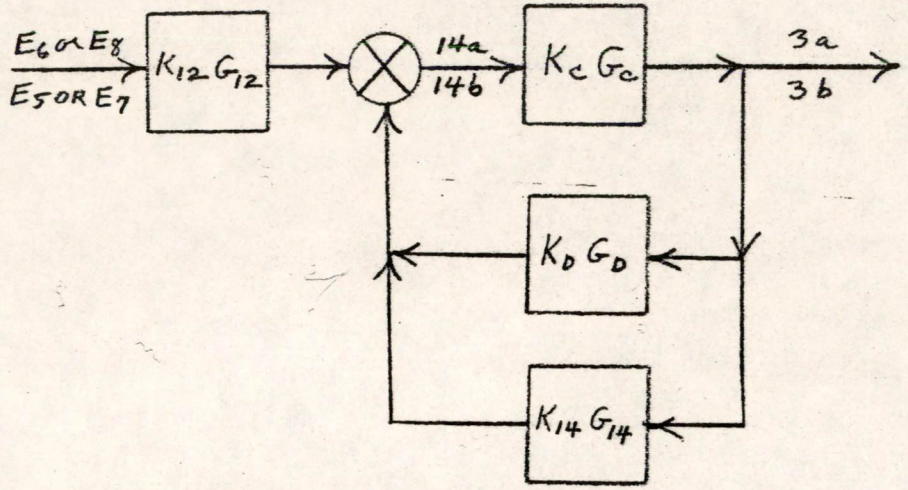

FIGURE 1.2.5

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

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-19			
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-11			
-10			
-9			
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-6			
-5			
-4			
-3			
-2			
-1			

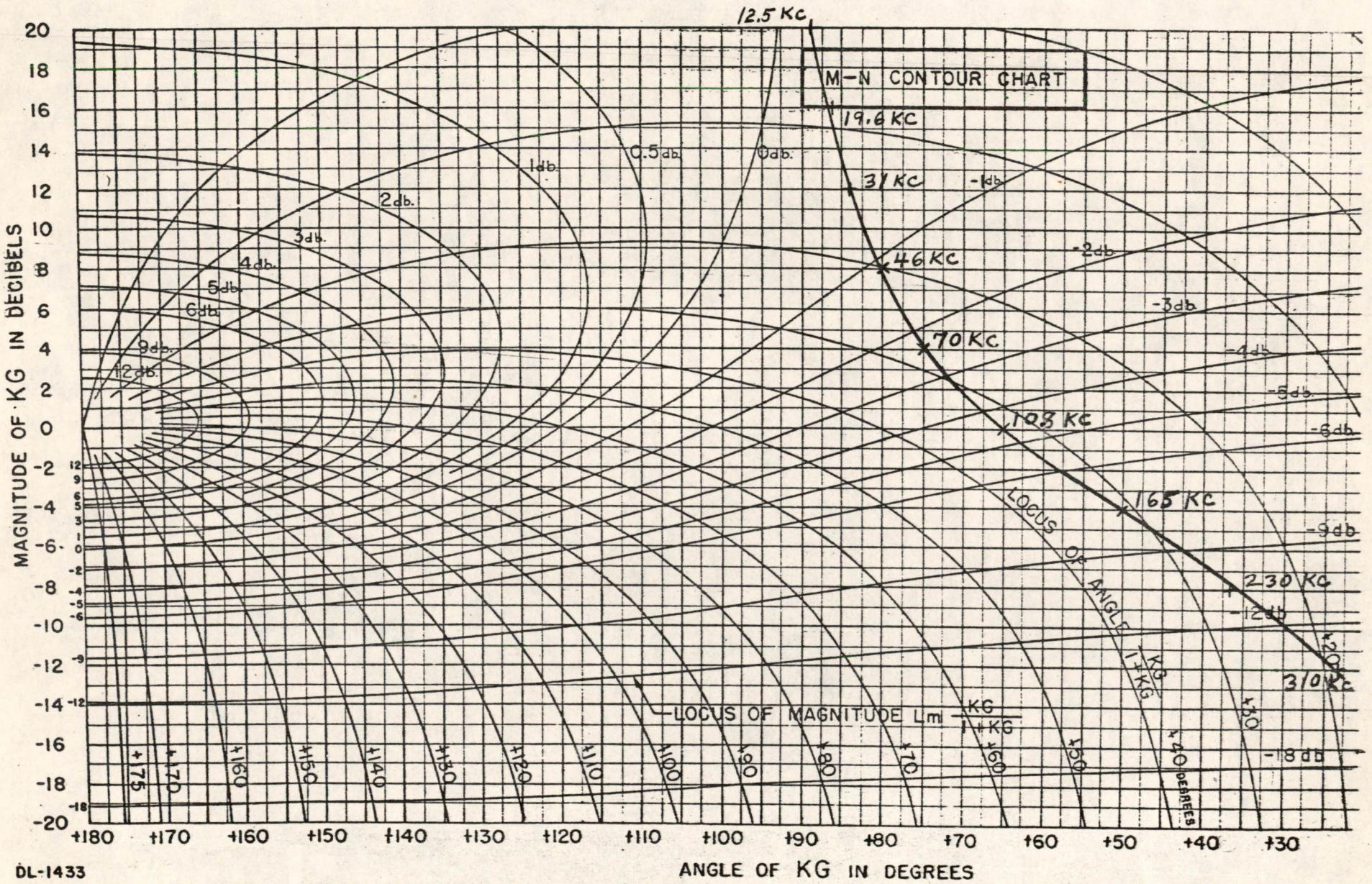
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

SIMPLIFIED COMMON MODE TRANSFER FUNCTION OF DISPLAY LINE DRIVER

SCALE:
DR. H E Ziemann
ENG. H E Ziemann
CK.
APPD.
SA-65925

8M-7-54-Boston Blue Print

SA-48780-G



DL-1433

FIGURE 1.2.5a

EVALUATION OF $K_H G_H$ FROM $-K_D G_D / K_{14} G_{14}$

DISPLAY LINE DRIVER

SA-48780-G

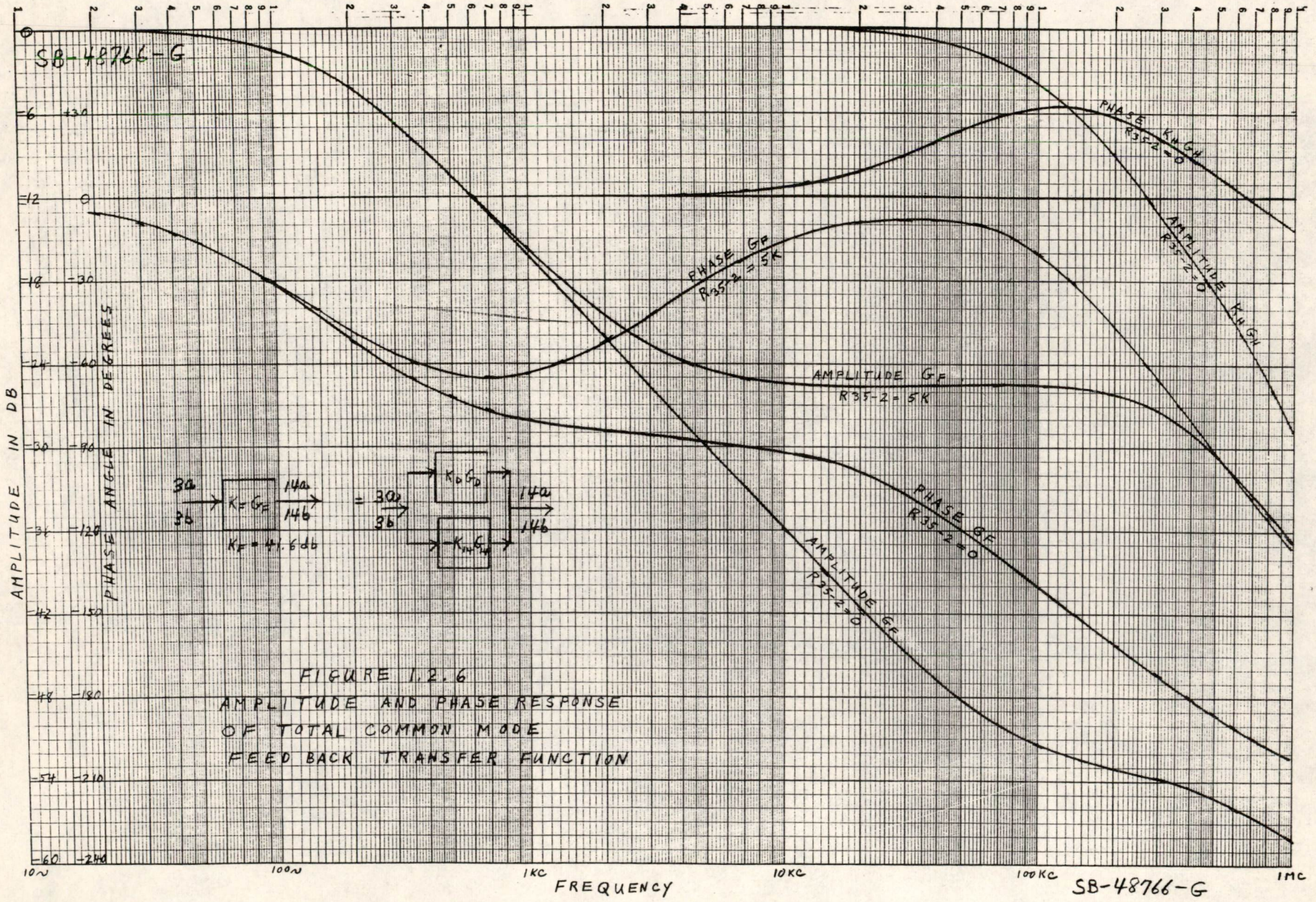


FIGURE 1.2.6
AMPLITUDE AND PHASE RESPONSE
OF TOTAL COMMON MODE
FEED BACK TRANSFER FUNCTION

SB-48766-G

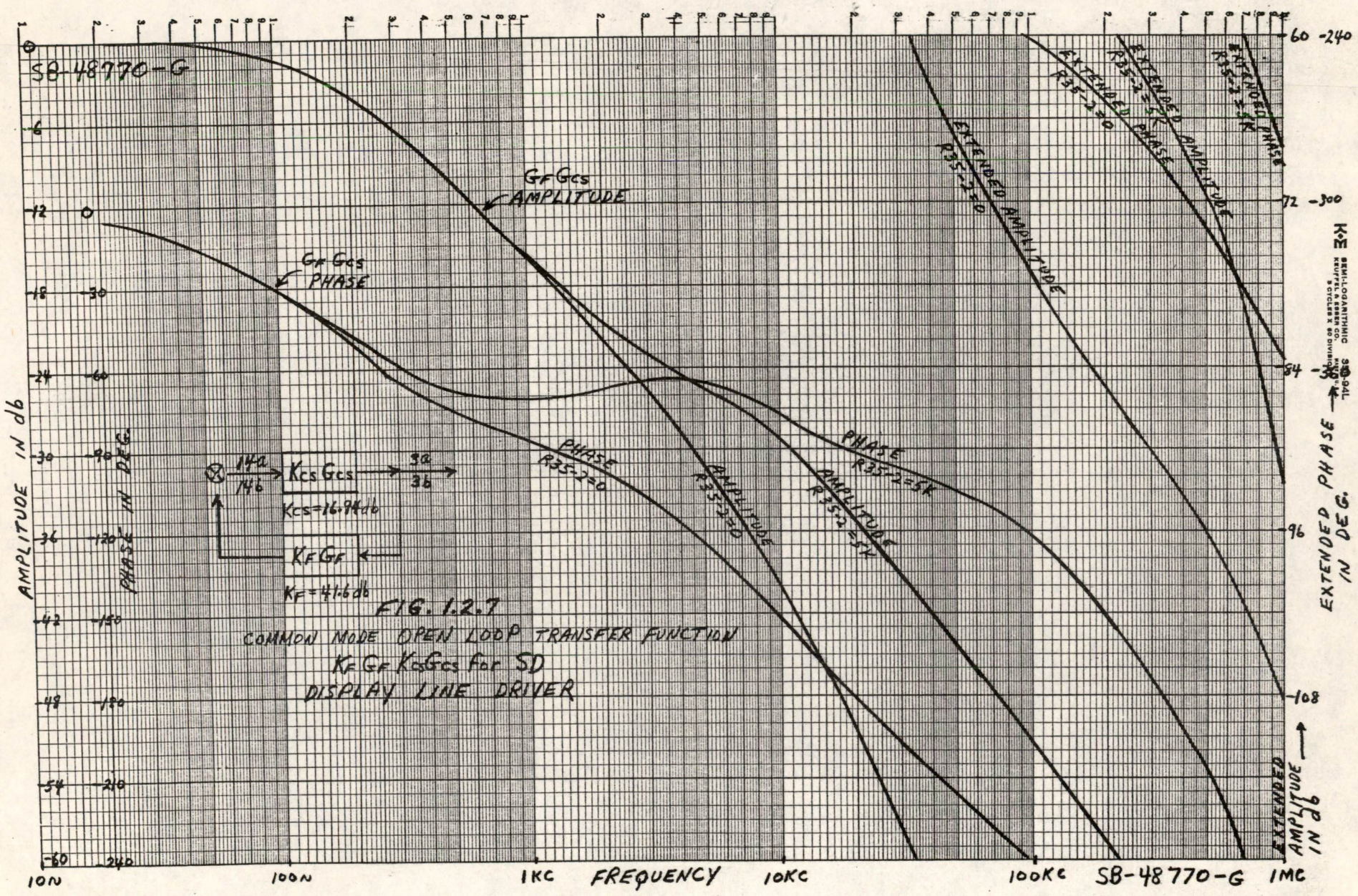
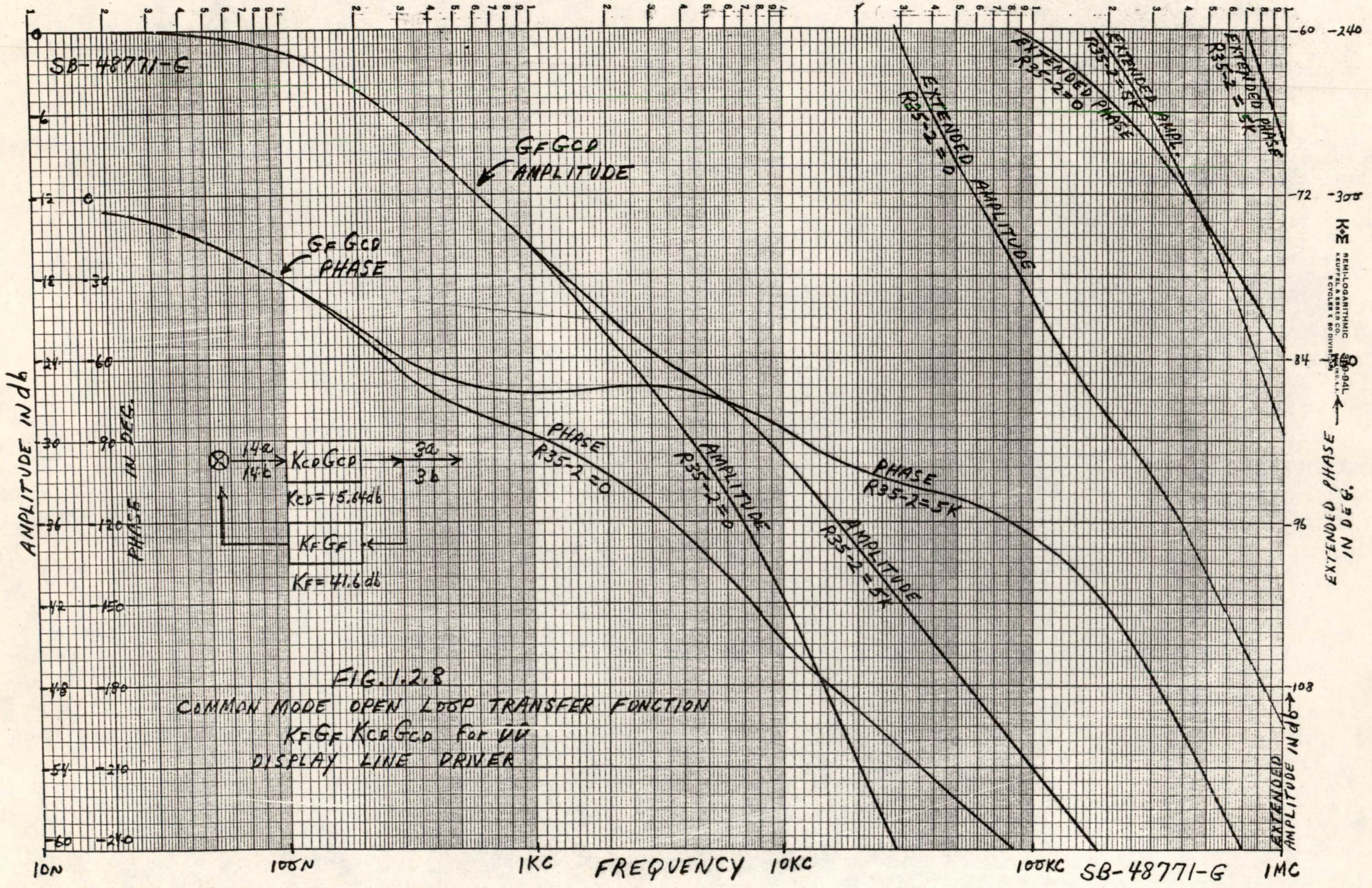


FIG. 1.2.7

COMMON MODE OPEN LOOP TRANSFER FUNCTION

$K_F G_F K_{CS} G_{CS}$ For SD

DISPLAY LINE DRIVER


SB-4877I-G
GFGCD AMPLITUDE
GFGCD PHASE
PHASE R35-2=0
AMPLITUDE R35-2=0
PHASE R35-2=5K
AMPLITUDE R35-2=5K
EXTENDED AMPLITUDE R35-2=0
EXTENDED PHASE R35-2=0
EXTENDED AMPL. R35-2=5K
EXTENDED PHASE R35-2=5K
14a
14b
KCDGCD
KCD=15.64db
KFGF
KF=41.6db
3a
3b
AMPLITUDE IN db
PHASE IN DEG.
EXTENDED PHASE IN DEG.
EXTENDED AMPLITUDE IN db
FREQUENCY
10N
100N
1KC
10KC
100KC
1MC
SB-4877I-G
KE
SEMI-LOGARITHMIC
KEUFFEL & ESSER CO.
FIG. 1.2.8
COMMON MODE OPEN LOOP TRANSFER FUNCTION
KFGF KCDGCD FOR ΔV
DISPLAY LINE DRIVER

SA-48783-G

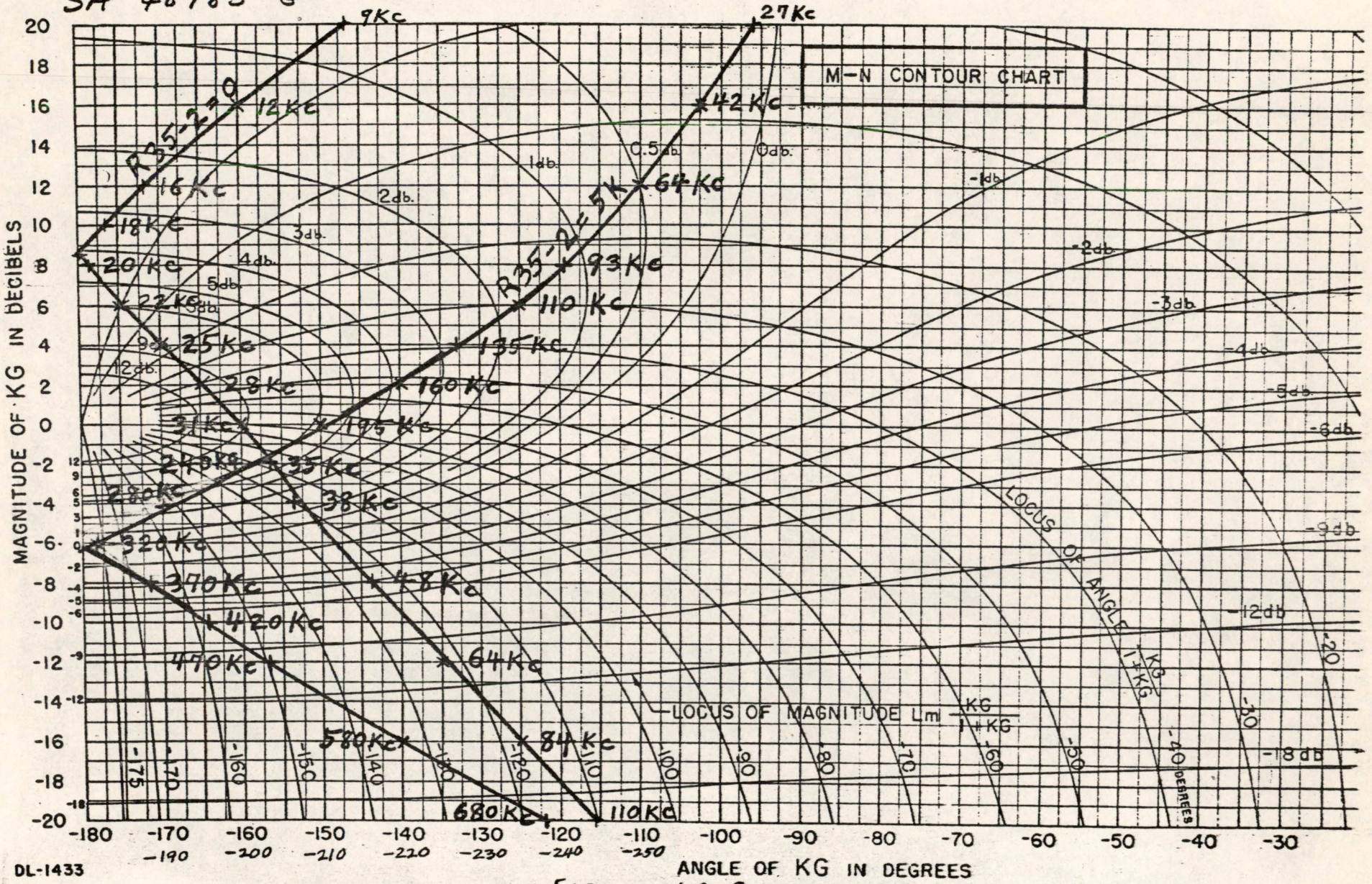


FIGURE 1.2.8a

EVALUATION OF K_{ES} G_{ES} FROM $K_F G_F K_{CS} G_{CS}$
DISPLAY LINE DRIVER

SA-48783-G

SA-48784-G

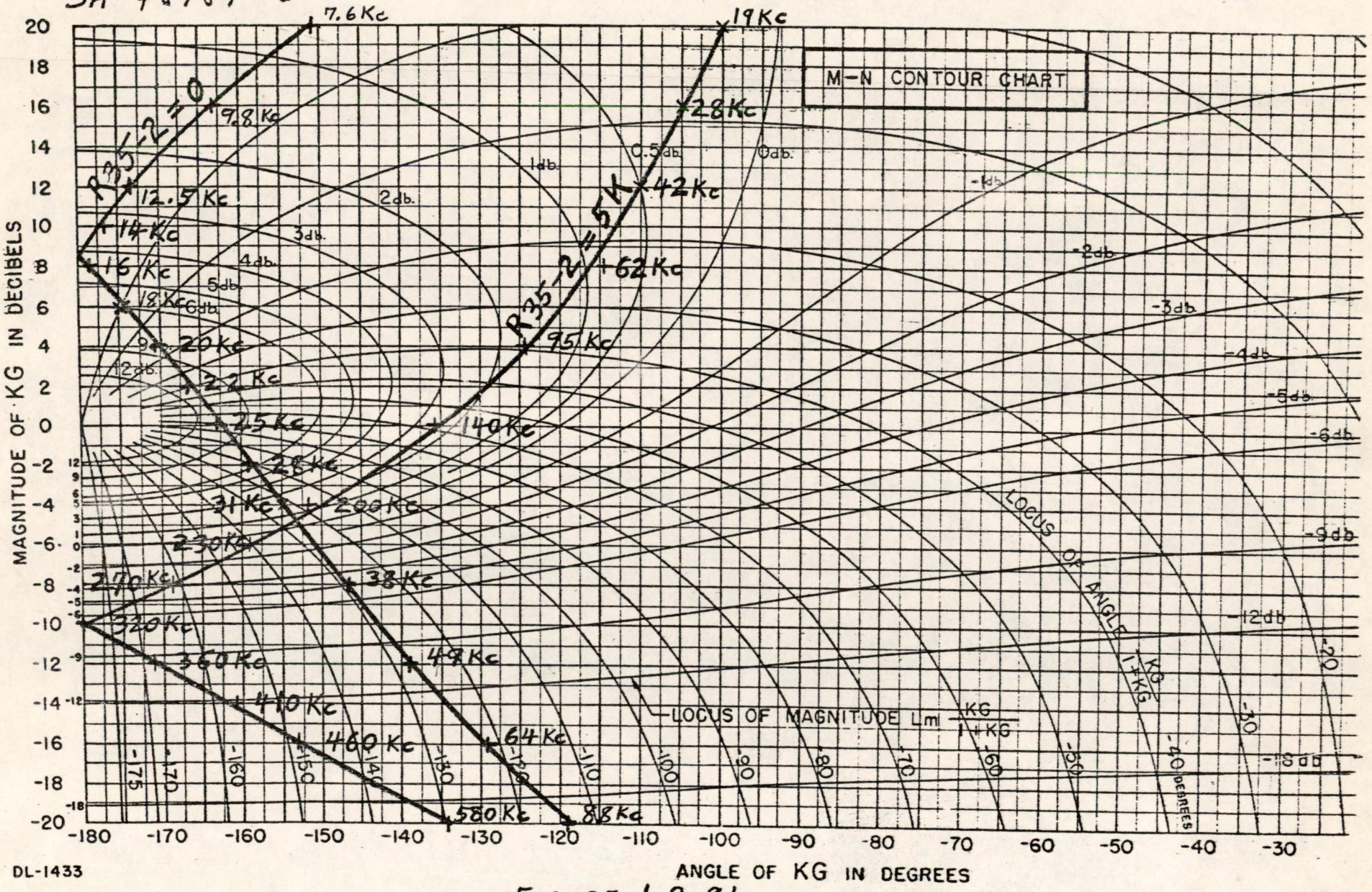


FIGURE 1.2.8b

EVALUATION OF $K_{ED} G_{ED}$ FROM $K_F G_F K_{CD} G_{CD}$

DISPLAY LINE DRIVER

SA-48784-G

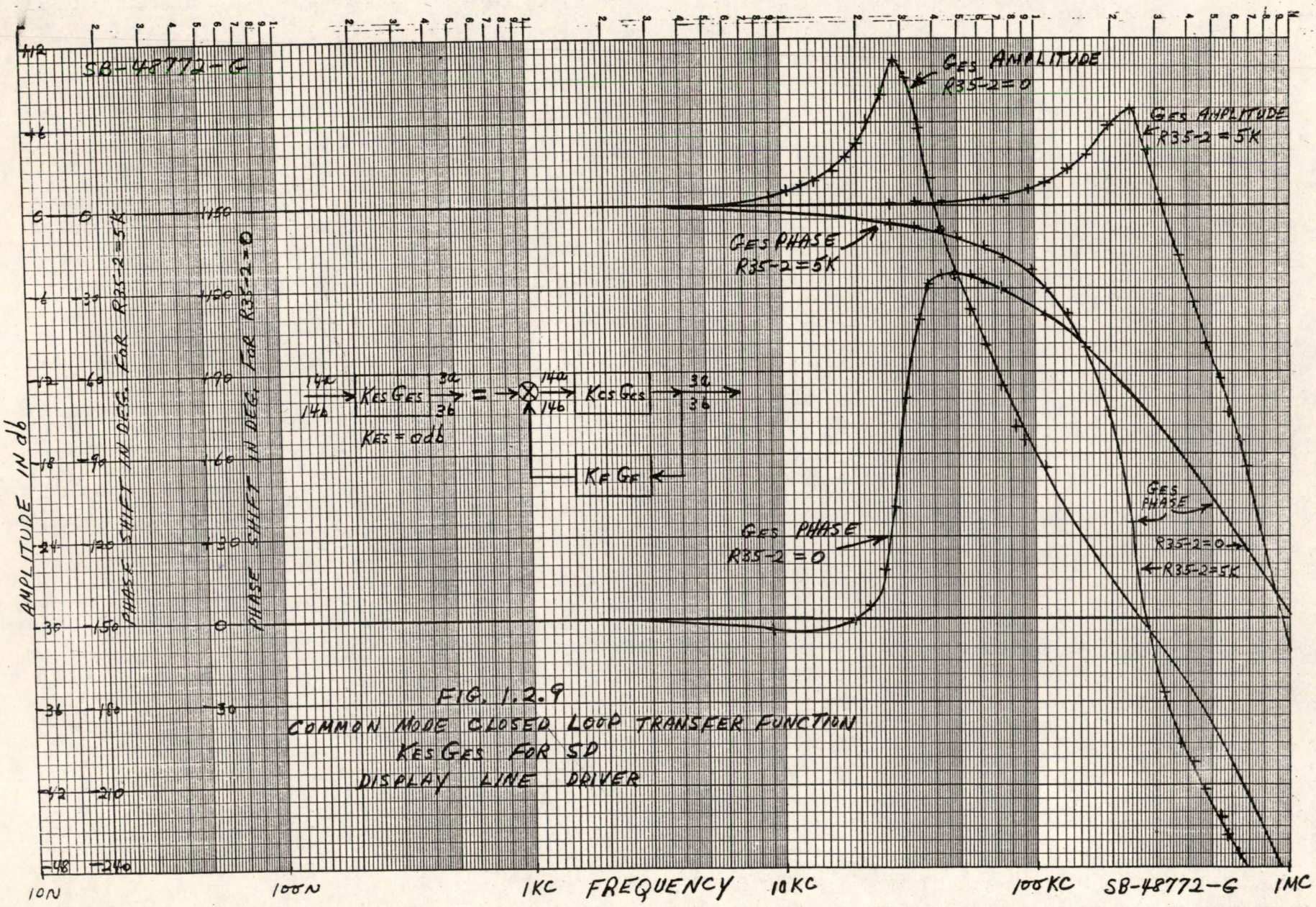


FIG. 1.2.9
COMMON MODE CLOSED LOOP TRANSFER FUNCTION
KES GES FOR SD
DISPLAY LINE DRIVER

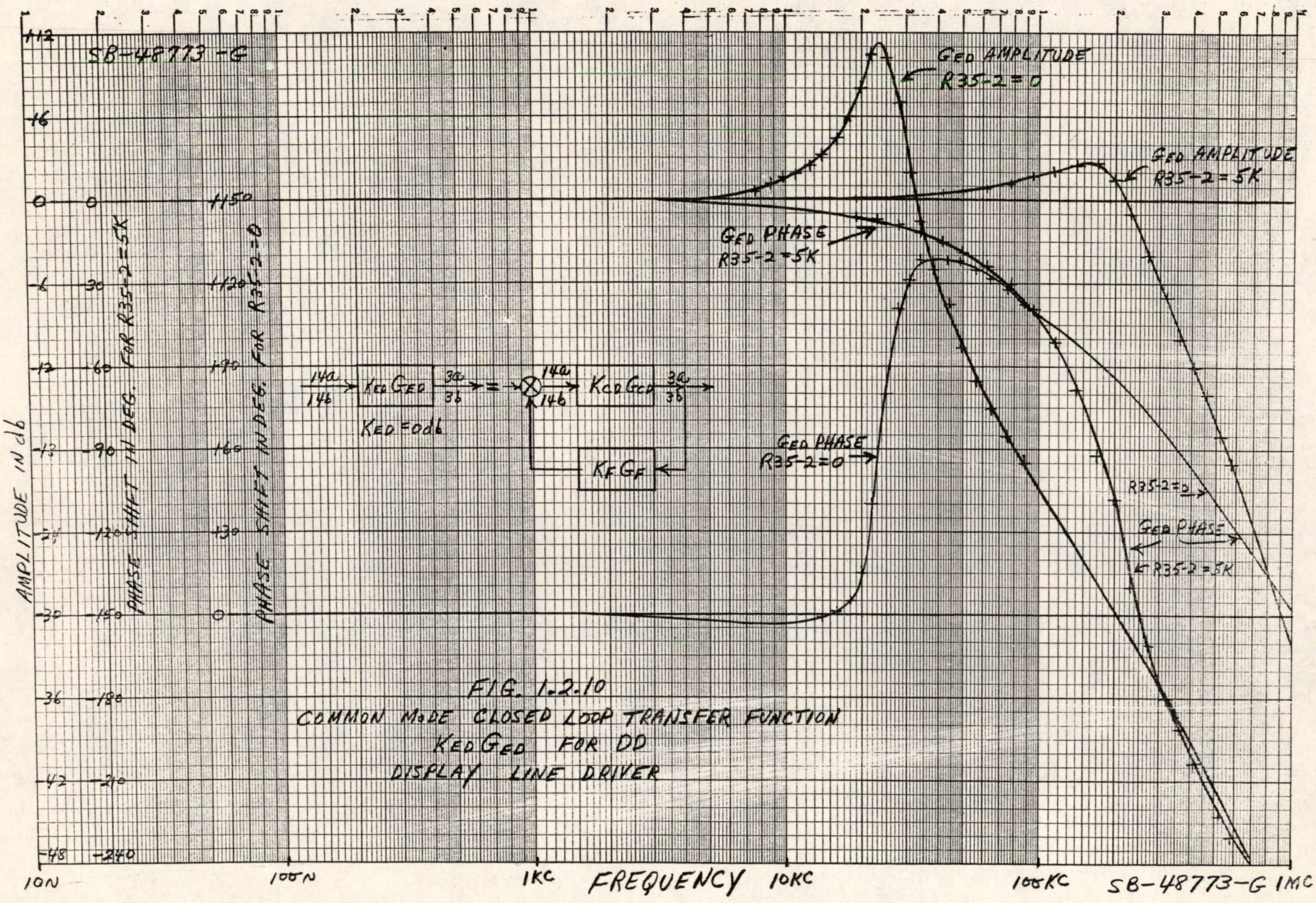


FIG. 1.2.10
COMMON MODE CLOSED LOOP TRANSFER FUNCTION
$K_{ED}G_{ED}$ FOR DD
DISPLAY LINE DRIVER

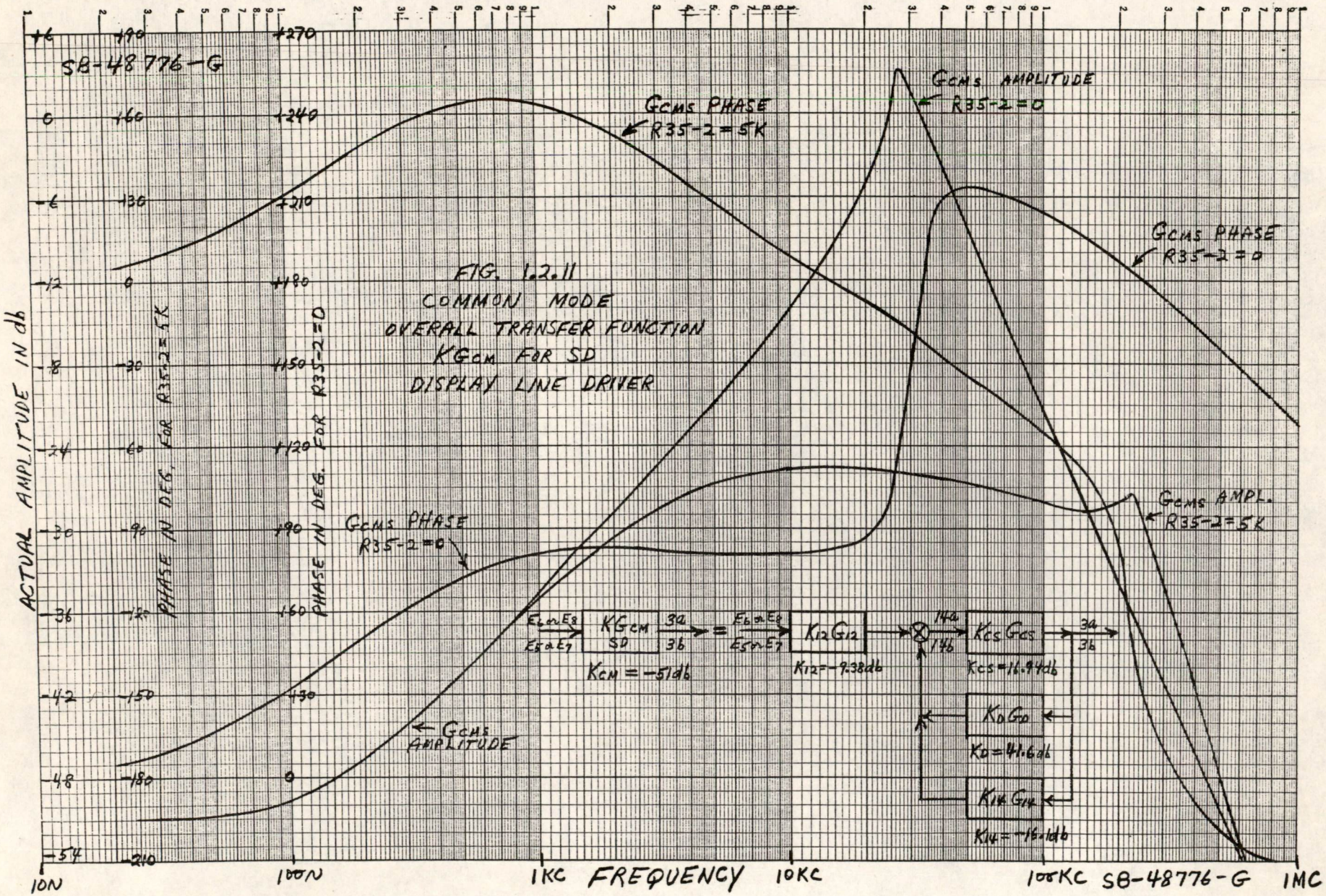


FIG. 1.2.11
COMMON MODE
OVERALL TRANSFER FUNCTION
KGCM FOR SD
DISPLAY LINE DRIVER

K&E SEMI-LOGARITHMIC 359-04L
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 60 DIVISIONS

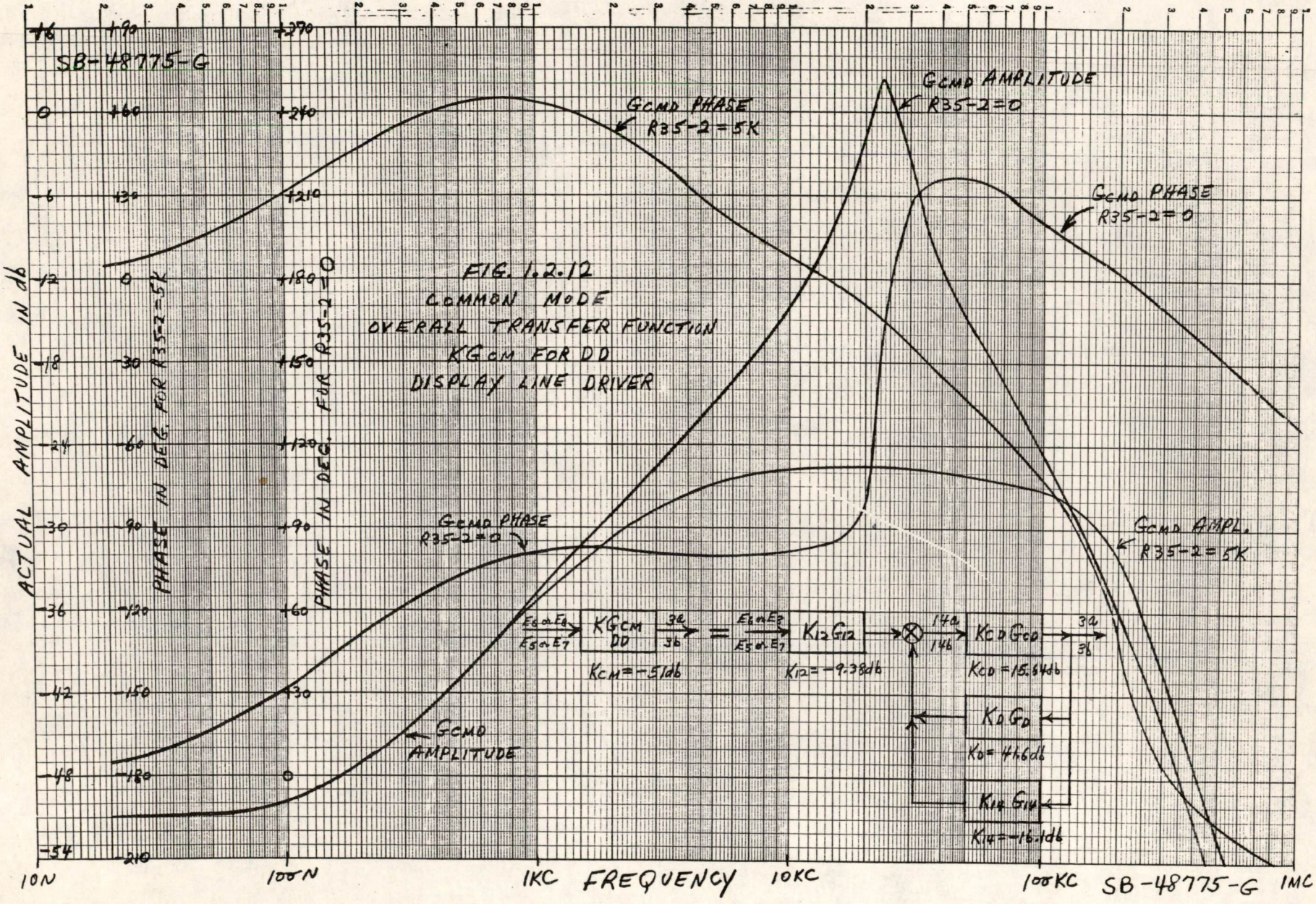


FIG. 1.2.12
COMMON MODE
OVERALL TRANSFER FUNCTION
KGCM FOR DD
DISPLAY LINE DRIVER

359-71 KEUFFEL & ESSER CO.
Semi-Logarithmic, 3 Cycles × 10 to the inch,
5th lines accented.
MADE IN U. S. A.

SA-48777-G

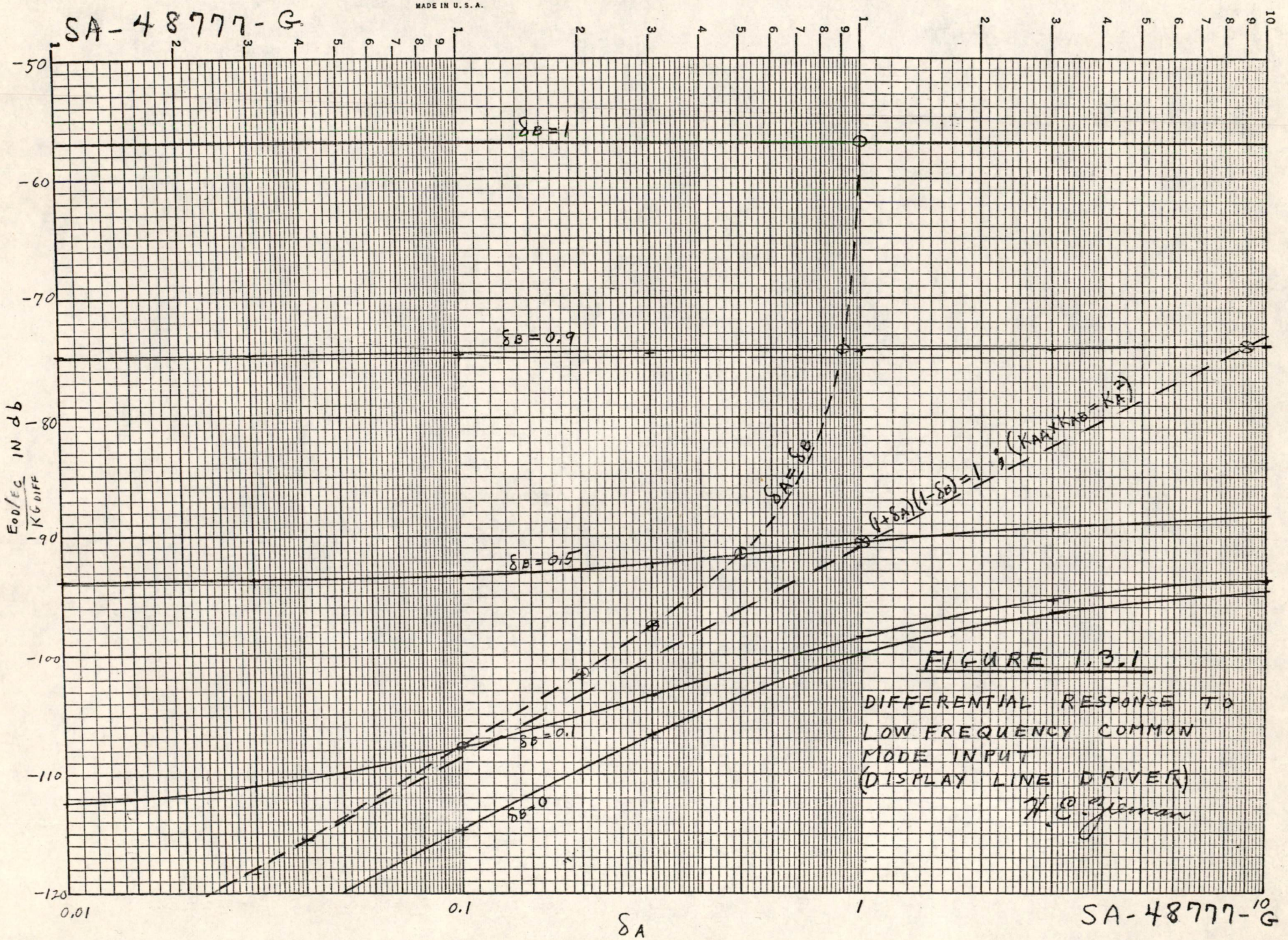


FIGURE 1.3.1

DIFFERENTIAL RESPONSE TO LOW FREQUENCY COMMON MODE INPUT (DISPLAY LINE DRIVER)

W. C. Gilman

SA-48777-10G

359-71 KEUFFEL & ESSER CO.
Semi-Logarithmic, 3 Cycles × 10 to the inch,
5th lines accented.
MADE IN U. S. A.

SA-48779-G

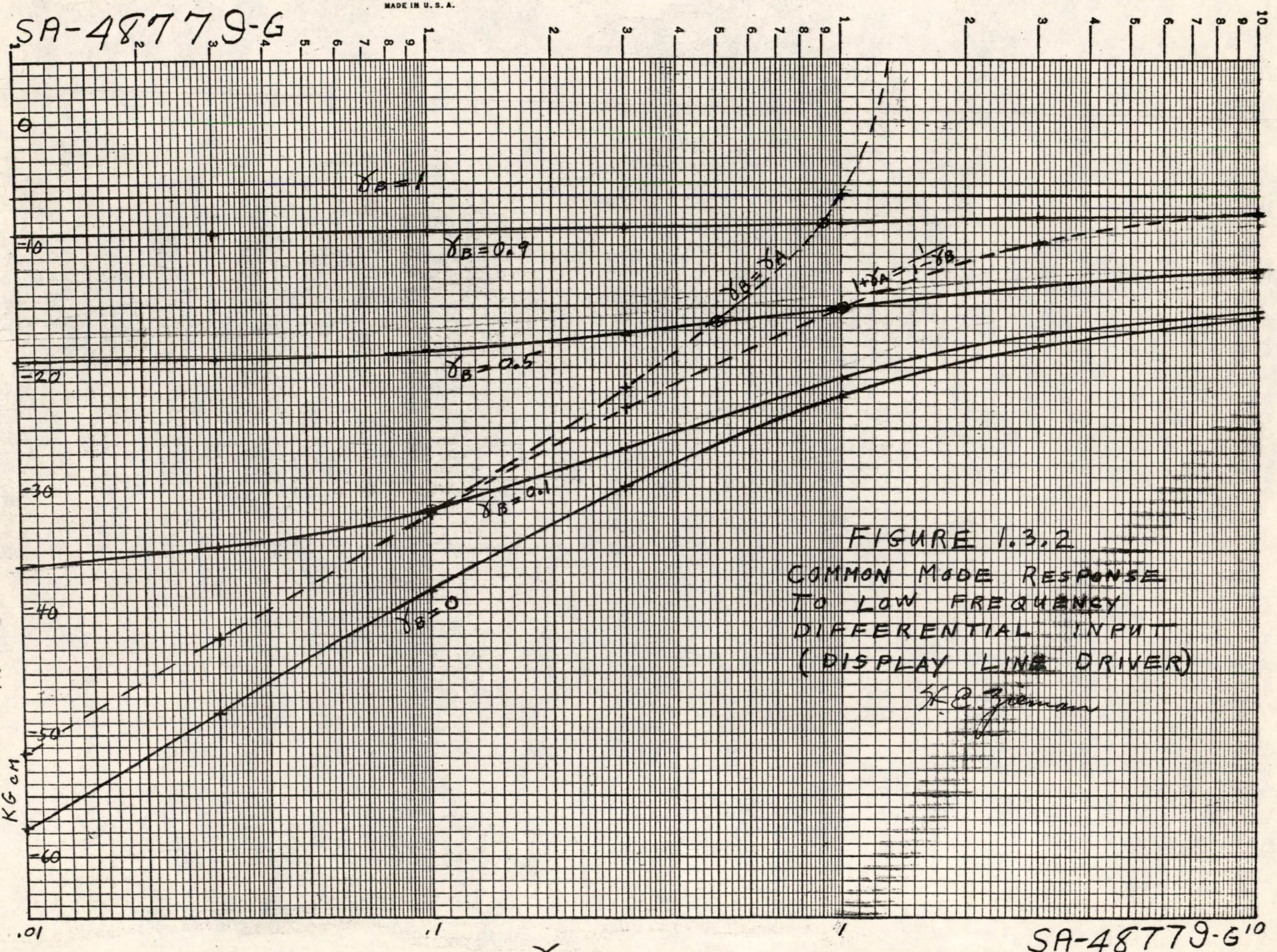


FIGURE 1.3.2
COMMON MODE RESPONSE
TO LOW FREQUENCY
DIFFERENTIAL INPUT
(DISPLAY LINE DRIVER)
K. E. Zeeman

SA-48779-G 10

SA-66073

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

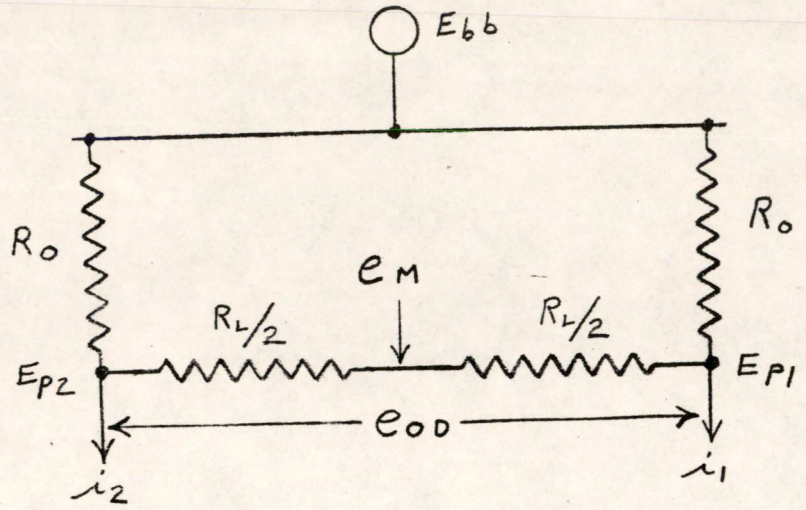


FIGURE 1.4.1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
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-3			
-2			
-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

EQUIVALENT OUTPUT OF LINE DRIVER

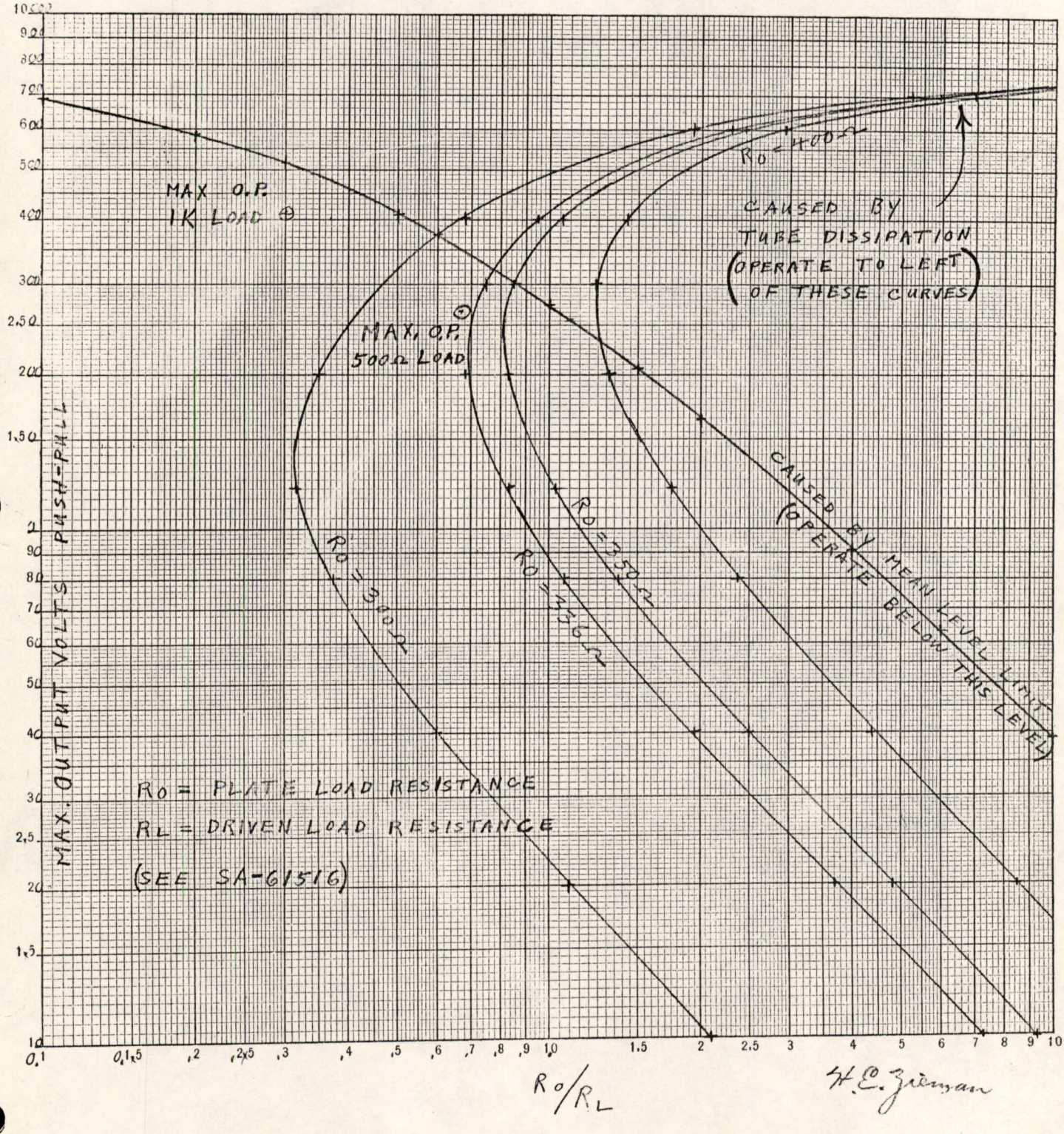
SCALE:
DR. H. E. Ziemann
ENG. H.E.Z.
CK.
APPD.
SA-66073

8M-7-54-Boston Blue Print

SA-48712-G

FIGURE 1.4.2

THEORETICAL OPERATING LIMITS
LINE DRIVER OUTPUT STAGE



SA-48712-G

359-71 KEUFFEL & ESSER CO.
Semi-Logarithmic, 3 Cycles × 10 to the inch,
5th lines accented.
MADE IN U. S. A.

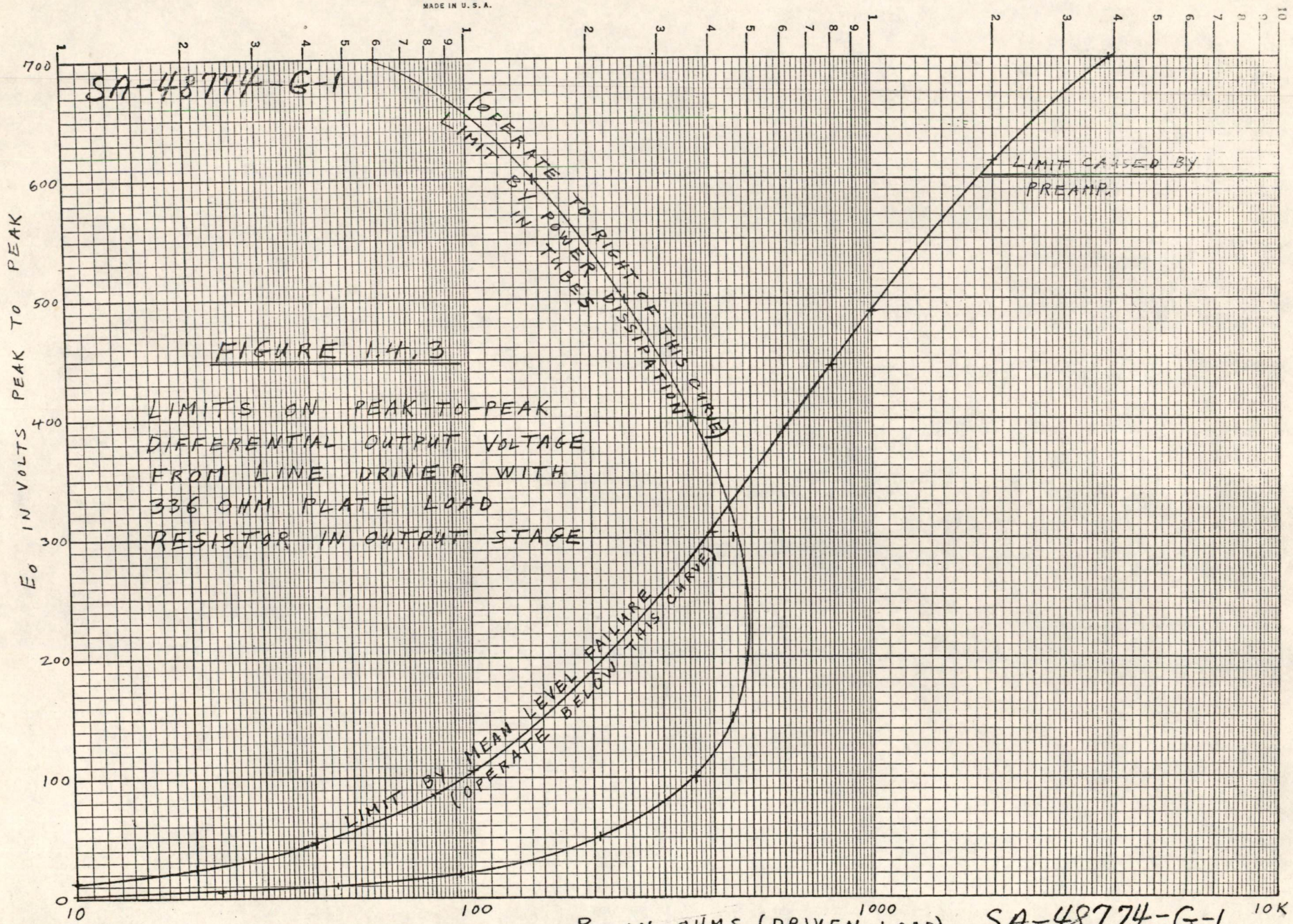


FIGURE 1.4.3

LIMITS ON PEAK-TO-PEAK DIFFERENTIAL OUTPUT VOLTAGE FROM LINE DRIVER WITH 336 OHM PLATE LOAD RESISTOR IN OUTPUT STAGE

Memorandum 6M-3316

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRANSISTOR CIRCUITS FOR DRIVING COINCIDENT CURRENT MEMORIES

To: Memory Section, R. R. Everett

From: Kenneth H. Olsen

Date: 21 January 1955

Approved: DRB
David R. Brown

Abstract: Transistors can be made to pass large currents as needed in magnetic memories by turning off the currents while the transistors are being switched.

Some transistors have the very useful property of being able to pass large currents with only very low voltage drops across the transistor - and therefore, only low power dissipation. Although at the present time the allowed dissipation of fast transistors is small compared to the peak power needed to drive a large coincident-current memory, we may be able to drive memories, if we are careful to pass the large currents only when there is very low voltage across the transistor.

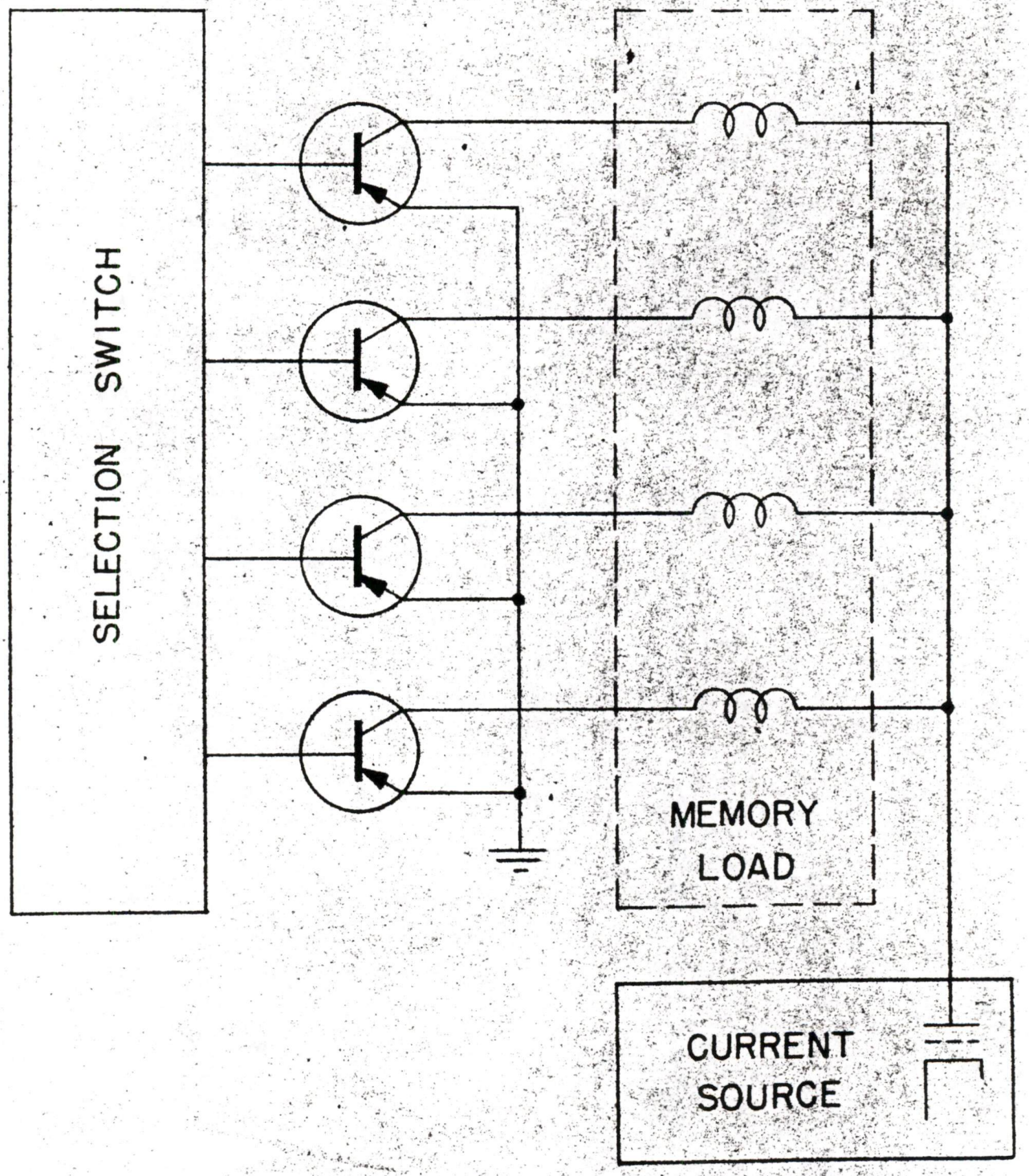
Figure 1 schematicly shows four transistors driving four coordinate lines of a memory. We first turn on the selected transistor with current from the selection switch. Then we pulse the vacuum tube current source and pass current through the selected memory line and the "on" transistor. Because this transistor is "on", it drops little voltage and so dissipates low power. After the current source is turned off the selection switch can be changed and a different transistor selected.

Signed: Kenneth H. Olsen

KHO/dg

Attachment: Drawing A-61619

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.



TRANSISTOR MEMORY DRIVER

A-61619
MN

K. Olsen

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: FORWARD AND REVERSE RECOVERY IN TRANSITRON TYPE T-6 GOLD BONDED GERMANIUM DIODES

To: D. R. Brown

From: G. A. Davidson

Date: February 28, 1955

Approved: Torben Meisling
Torben Meisling

Abstract: The Transitron T-6 Diode has been tested to determine how the forward recovery characteristics vary with the amplitude of forward current flowing. The initial high forward resistance falls to its final value with a time constant of .20 microseconds. On the average, the resistance changes from 46 to 31 ohms with 10 ma of forward current and from 7.7 to 2.7 ohms with 300 ma of forward current. Reverse voltage was found to have little effect on forward recovery characteristics and forward recovery characteristics were not duty cycle sensitive. The reverse recovery characteristics were important with a forward current of 100 ma only if forward current was flowing during the 2 μs preceding the reverse voltage.

Introduction

In the design of a two-core-per-bit stepping register, it would be desirable to eliminate the resistor in the coupling loop by choosing a turns ratio such that the diode resistance would be equal to the required loop resistance.

The diode resistance is a function of the current flowing through it and also of the time since current started flowing through it, so a study of the T-6 Diode was undertaken to assemble enough data to allow the stepping register to be designed.

Reverse Recovery Measurements

To observe the reverse recovery characteristics of the T-6 Diode, the circuit in Fig. 1 was used. The positive current generator had a rise time of about 0.3 microseconds and was set to deliver 20 ma into the 1K ohm resistor through the IN 38 diode developing a final back voltage on the T-6 diode of 20 volts. The negative current generator had a rise time of about 0.1 microseconds and was set to deliver 100 ma of forward current to the T-6 diode.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The delay units were adjusted so that the reverse voltage was applied more than 2 microseconds after the pulse of forward current. There appeared across the 10 ohm measuring resistor in series with the T-6 diode, a pulse of voltage representing reverse current that was approximately 1 ma in amplitude and 0.2 microseconds in length. It was probably due to stray pickup because the size of the pulse was constant as long as the reverse voltage was applied at least 2 μs after the end of the forward current pulse. The pulse also might have come from the initial current necessary to establish the charged carriers that give the diode its high back resistance.

As the end of the forward current pulse and beginning of the reverse voltage pulse were brought closer together, a new pip appeared that decreased exponentially in amplitude. The less the time between the two pulses, the greater the amplitude of the pip. With one microsecond separation, the pip had an amplitude of 2 ma, while for 1/2 microsecond it had an amplitude of 4 ma, and when the pulses were overlapping, the full 20 ma that the positive current driver was delivering was going through the T-6 diode in the reverse direction. Since the reverse voltage is essentially being applied through a 1000Ω resistance, the actual back voltage on the diode rises slowly. The data are not the same as would be obtained with a perfect voltage source. Some sketches of the waveforms are shown in Fig. 2. Since reverse voltage would not be applied to a diode immediately after it has been conducting in the forward direction, as it does in the single-core-per-bit stepping register, the study of the reverse recovery characteristics was not continued.

Forward Recovery Measurements

The forward recovery characteristics were measured using the circuit shown in Fig. 3. The details of rise time of the current-source waveforms and the points measured on the diode waveform are shown in Fig. 4. The initial peak on the diode voltage waveform caused some concern until it was found to have been caused by coupling through the grid to plate capacity of the 6CD6's. The same effect was observed with a 1 M ohm resistor across the output terminals of the core driver.

To measure the time to recover from maximum voltage to steady state voltage (corresponding to the change from maximum resistance to steady state resistance) the voltage across the diode was amplified until the distance from peak to final voltage occupied 3 cm on the Textronix 514D oscilloscope (about the maximum amplification possible). Time was measured from the point where the voltage across the diode initially had the value "e_f" to the point where the voltage had decreased 2/3 of the distance from the peak to the final value.

The average characteristics of twenty Transitron T-6 diodes are as follows:

Forward Current	10 ma	100 ma	300 ma
Maximum Resistance	45.9 ohms	10.9 ohms	7.73 ohms
Final Resistance	30.9 ohms	4.89 ohms	2.71 ohms

$R_{maximum}/R_{final}$	1.49	2.19	2.85
T (time 2/3 decay)	0.183 μs	0.215 μs	0.173 μs
Equation of Decay	$31+15\exp(-\frac{t}{0.17\times10^{-6}})$	$4.9+6\exp(-\frac{t}{0.20\times10^{-6}})$	$2.7+5.02\exp(-\frac{t}{0.16\times10^{-6}})$

At first the results were thought to be dependent on the duty cycle but the following table indicates that the characteristics are stable over a wide range of duty cycles.

Current, in ma	10	10	10	10	10	10	10	10
Pulse Rate	100cps	100cps	1KC	1KC	10KC	10KC	100KC	200KC
Pulse Length, s	1.2	75	1	71	1	51	1.0	1.2
Resistance Peak, ohms	41	44	41	41	41	42	43	41
Resistance Final, ohms	32	29	32	29	32	29	32	28

Current, in ma	100	100	100	100
Pulse Rate	100cps	1KC	10KC	100KC
Pulse Length, s	1.2	1.3	1.1	0.9
Resistance Peak, ohms	16.8	16.6	16.8	16.8
Resistance Final, ohms	6.7	6.6	6.6	6.9

One diode was used for the first nine readings and one for the last four readings.

These tests have shown that with 100 ma of forward current the reverse recovery of the diode is accomplished within 2 μsec of the end of the forward current. In fact, if the reverse voltage is applied to the diode more than 1 μsec after the end of forward current the recovery effect can be practically ignored. When a forward current is applied to the diode, the initial resistance is never more than three times the static resistance, and thus this ratio might be used as a conservative estimate of the forward recovery situation. The time constant of this recovery is of the order of 0.2 μsec. Moreover, this forward recovery characteristic is not sensitive to duty cycle changes. This information will enable us to design core shift registers such that the diode resistance is just the right part of the total loop resistance.

Signed: G. A. Davidson
G. A. Davidson

GD/md

Distribution: Fig. A-61442

Group 63, Staff
B.B. Paine

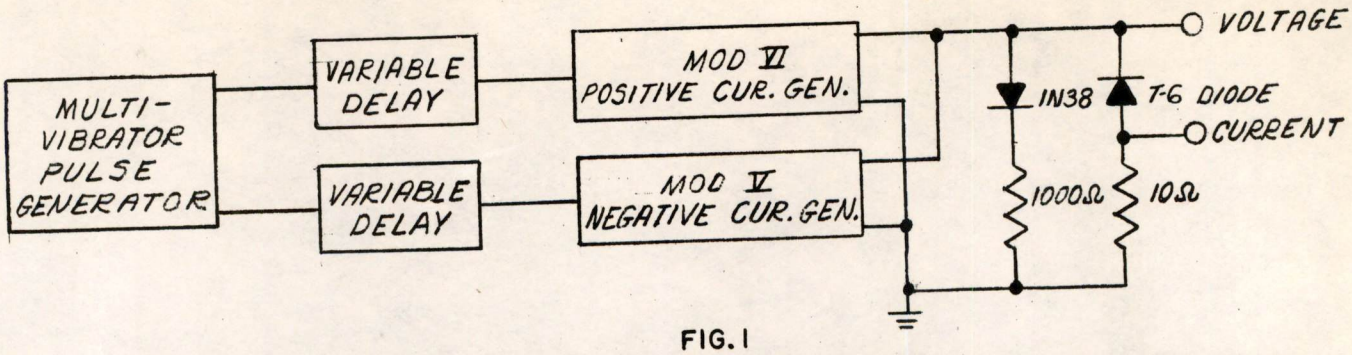


FIG. 1

BLOCK DIAGRAM FOR DIODE REVERSE RECOVERY MEASUREMENTS

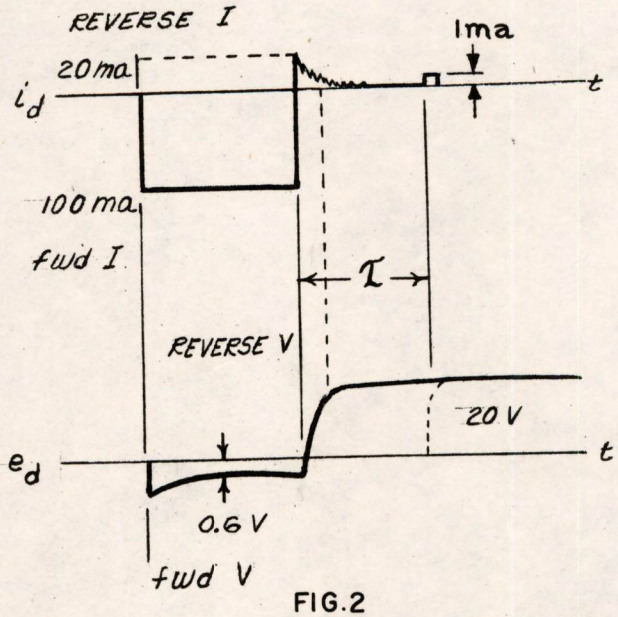


FIG. 2

DIODE VOLTAGE WAVEFORMS FOR REVERSE RECOVERY MEASUREMENTS

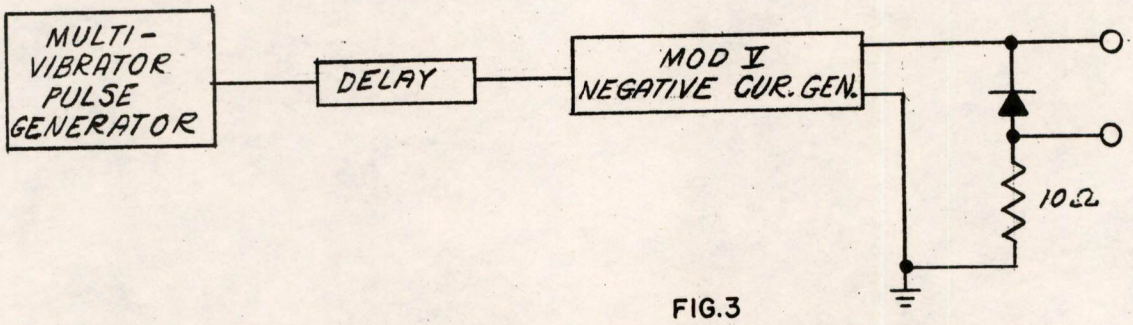


FIG. 3

BLOCK DIAGRAM FOR DIODE FORWARD RECOVERY MEASUREMENTS

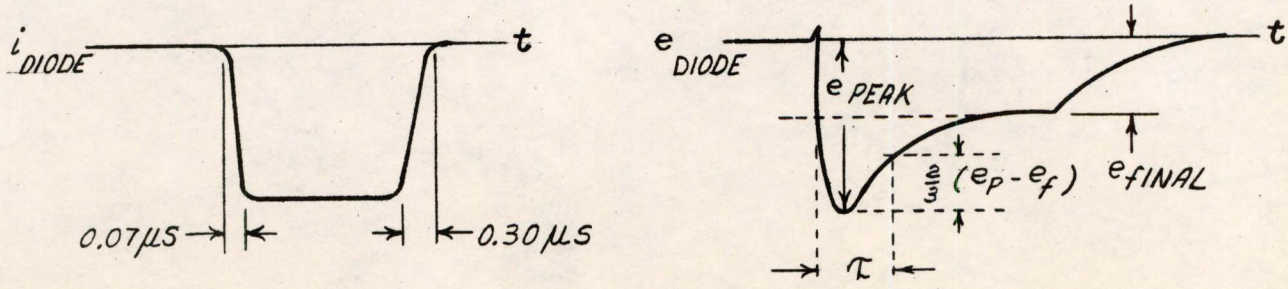


FIG. 4

WAVEFORMS OF DIODE CURRENT AND VOLTAGE DURING FORWARD RECOVERY

A-61442

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: ANALYSIS OF RECENT PERFORMANCE RECORDS FOR THE WHIRLWIND COMPUTER SYSTEM

To: Distribution List

From: Edwin S. Rich

Date: 1 March 1955

Approved: S. H. Dodd, Jr.

Abstract: Comprehensive records of all system failures in the Whirlwind computer and its associated terminal equipment over a 20 week period show that the average uninterrupted operating time between failure incidents was 10.6 hours. The average time lost for each of the 244 incidents was 22.8 minutes. The percentage of operating time usable was 96.5 per cent. Computer alarms accounted for 37 per cent of the stoppages but only for 12 per cent of the lost time. Failures caused by design weaknesses required more time for correction on the average than the other classes of failure analyzed. Assuming that some major improvements in weak sections of the system had been carried out, it was estimated that the same failures might have averaged only 16.8 minutes of lost time per failure.

1.0 COMPUTER-PERFORMANCE RECORDS

1.1 Coverage

Following the revisions in the Cape Cod Direction Center facilities in July, 1954, the Whirlwind computer and its associated input and output system entered a period in which the equipment has remained relatively stable. In September, 1954, the procedures for gathering and evaluating performance data on the computer system were somewhat revised. This was done to permit more comprehensive analyses of system reliability with particular emphasis on interrupting failures. In general, the new procedures provide more complete data on all computer stoppages and a bi-weekly review and summary of these stoppages. The records are intended to reflect all failures in the computer and its terminal equipment that would have caused interruptions if the Cape Cod System had been in full scale operation continuously. Actually, for a large fraction of the time that the computer was in use, much of the Cape Cod terminal equipment was not required. (This terminal equipment comprises about 40 per cent of the entire system

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

which has approximately 12,700 tubes). Under these circumstances, failures in the terminal equipment may not have resulted in loss of computer time. Failures which do not cause interruptions, however, must be considered in order to obtain an accurate picture of system performance. These are considered to be "potentially interrupting" and are given the same weight as those that actually halted operations.

1.2 Organization of Records

Past Whirlwind computer experience had indicated that most of the interrupting failures could be placed into a relatively few categories which defined either the cause of the failure or its principal symptom. In the record system set up last September, the following categories were selected:

Tubes	(cause)
Wiring, cabling, jacks, connectors, etc.	(cause)
Circuit components (other than tubes)	(cause)
Blown fuses	(symptom)
Computer alarms	(symptom)
Design weaknesses	(cause)
Miscellaneous	

The failures listed in the blown-fuse and computer-alarm categories are ones for which true causes cannot be immediately determined. In general, such failures have no associated equipment damage. Examples of incidents in the miscellaneous category are an insulation breakdown on a phenolic panel, an air conditioning failure, an unseated tube or loose wire inadvertently caused while doing essential maintenance, and a malfunction of a piece of terminal equipment which cleared up before the fault could be found.

For each failure, the amount of time lost is that time required to restore the system to operation after the interruption. In the majority of the component and circuit failures, this includes the time required to isolate and replace the defective item. In the newer sections of the system having plug-in units, it may include only the time to locate and replace the plug-in unit. For computer-alarm stoppages, it includes the time required to photograph the control and indicator panels and to record pertinent data on the program being run at that time. This information is then studied at leisure to detect possible causes of the alarms.

The records of interrupting and potentially-interrupting failures are further broken down to show those which must be charged against the system and those which can be attributed to new equipment installation or revision. Because the central computer and its terminal equipment are an integral electrical system, failures in new equipment can cause transients which interrupt the computer, even though the new equipment is logically independent of the rest of the system. Therefore, until a new installation

has been debugged and adequate routine-maintenance procedures have been worked out, failures attributable to such equipment are not counted against the system.

2.0 ANALYSIS OF PERFORMANCE DATA

Several figures are needed to adequately describe the reliability of an electronic system. In general, system reliability is reflected in the amount of unscheduled down time caused by interrupting failures and in the amount of scheduled down time required for preventive maintenance. Since the amount of down time for different types of interrupting failures varies widely, the frequency of such failures is also an important factor in describing system reliability. In the following paragraphs such reliability figures for the Whirlwind computer and its associated Cape Cod terminal equipment are given. These figures were derived from an analysis of data gathered over the 20-week period from 28 September 1954 to 10 February 1955.

2.1 DERIVATION OF LOST-TIME AVERAGES

It was pointed out previously that sections of the Cape Cod terminal equipment are not involved in some of the computer applications work so failures in this equipment may not cause loss of computer time. Considering this varied use of the computer, two alternatives for obtaining representative figures of system reliability are suggested. Either (1) the analyses are restricted to the central computer alone, or (2) all failures (both interrupting and potentially interrupting) are counted and lost-time data is extrapolated to give a measure of over-all system reliability. The second method was chosen for the following reasons:

a. Accurate records had been kept of all potentially-interrupting failures that had been detected and the number of such failures was consistent with the number of actual lost-time incidents;

b. The central computer is not representative of some of the terminal equipment;

c. Since the terminal equipment is always on and can indirectly affect the central computer, isolation of failures to the central portion of the computer in some cases is questionable;

d. The records of time spent on preventive maintenance cannot be broken down among different sections of the system.

To determine the theoretical, or extrapolated, lost time for each category of failures, the average lost time per lost-time failure was calculated, and this average was multiplied by the total number of failure incidents (interrupting and potentially interrupting) in that category. The sum of the extrapolated figures for all categories is the

total lost-time figure desired. This figure divided by the total number of failure incidents is the average lost time per incident for all incidents.

In determining the average lost time per failure for three of the categories, a few incidents were not considered in computing the averages because the time lost was disproportionately long. The failure-duration distribution for the three categories alarms, miscellaneous, and fuses is shown in Fig. 1. One incident in each of the first two categories and two incidents in the third were disregarded. A study of the records showed that three of these incidents had occurred during time assigned to the systems engineering group and that more time was spent in a thorough analysis of the failures than otherwise would have been required to restore operation. The fourth incident was a major air-conditioning failure which occurred on a week-end when service personnel were not readily available.

In Table I the number of lost time incidents and the amount of actual lost time for each category of failures are listed in the first two columns. The third and fourth columns show the number of incidents and corresponding lost-time figures used in computing the averages given in the last column.

TABLE I

LOST-TIME-FAILURE DATA

Category of failure	Number of lost-time incidents	Total minutes lost time	Data excluded in computing averages		Average lost time per incident (Minutes)
			Number of incidents	Minutes lost	
Computer Tubes	15	447			29.8
Power Supply Tubes	7	412			59.0
Wiring, Cables, etc.	6	220			36.7
Components	8	349			43.6
Blown Fuses	15	346	2	160	14.3
Alarms	83	652	1	60	7.2
Design Weaknesses	15	1093			73.0
Miscellaneous	40	1626	1	750	22.5

Using the averages of Table I, extrapolated lost-time figures were calculated to reflect all failure incidents. These figures are shown in Table II. The totals in this table determine that the average time lost for the 244 failure incidents is 22.8 minutes.

TABLE II

EXTRAPOLATED LOST-TIME DATA

Category of failure	Number of no-lost-time incidents	Total number of failure incidents	Average lost time per incident (minutes) (FROM TABLE I)	Total extrapolated lost time (Minutes)
Computer Tubes	12	27	29.8	805
Power Supply Tubes	1	8	59.0	472
Wiring, Cables, etc.	1	7	36.7	257
Components	8	16	43.6	697
Blown Fuses	18	33	14.3	472
Alarms	8	91	7.2	655
Design Weaknesses	1	16	73.0	1168
Miscellaneous	6	46	22.5	1035
Totals		244		5561

$$\text{Average lost time per incident} = \frac{5561}{244} = 22.8 \text{ min.}$$

2.2 Analysis of Failure Categories

The extrapolated lost-time and average lost-time figures for the various categories of failures as given in Table II contain some interesting points. The failures in three categories, tubes (computer types and power-supply types combined), design weaknesses, and miscellaneous, were responsible for 63 per cent of the time lost, while 70 per cent of the failure incidents were in the alarm, miscellaneous, and blown-fuse categories.

The relative contributions of the various categories are better shown by the data in Table III. Each class of failures has three quantities listed, its percentage of the total failure incidents, its percentage of the total lost time, and the ratio of its average lost time per incident to the over-all average lost time per incident. Extremes in this data occur for the alarm and the design-weakness categories. Alarms were by far the most frequent type of failure while design weaknesses required the most time for correction. The computer records show that in several of the cases of design weakness, the marginal checking or other preventive maintenance facilities were inadequate so incipient trouble had not been detected and signal tracing techniques were required to locate the fault.

TABLE III

COMPARISON OF FAILURE CATEGORIES

Category of failure	Percent of total number of failure incidents	Percent of total lost time	Ratio of lost-time average for category to lost-time average for all incidents
Computer Tubes	11.0	14.5	1.3
Power Supply Tubes	3.3	8.5	2.6
Wiring, Cables, etc.	2.9	4.6	1.6
Components	6.6	12.5	1.9
Blown Fuses	13.5	8.5	0.6
Alarms	37.3	11.8	0.3
Design Weaknesses	6.6	21.0	3.2
Miscellaneous	18.8	18.6	1.0

Since tubes are known to have the highest failure rate of all components in a computer system, an estimate of the number of stoppages caused by tubes is of interest. For this estimate it is assumed that about 85 per cent of the alarms and blown fuses were caused by tube defects. With this assumption, then, approximately 60 per cent of the total incidents and 40 per cent of the time lost may be attributed to tube failures.

Some information on component-failure rates can be derived from historical records on the system. During the 20-week period in question, a total of 437 tubes were replaced in the system. Replacements for accidental damage were excluded. Since 35 of these were interrupting or potentially interrupting failures, about 92 per cent of the failures were located during scheduled maintenance periods. The tube-failure rate for all causes, computed from the data already given and from the total-operating-time figure listed in Section 2.3, is 1.49 per cent of the tube complement per 1000 hours. The rate for interrupting tube-failures is 0.12 per cent of the tube complement per 1000 hours. These tube-failure rates compare favorably with similar data which has been derived in the past by the group working on tube testing and evaluation.

The records on component replacement show that a total of 101 components other than tubes were replaced. Since there were 16 interrupting or potentially-interrupting failures caused by such components, about 84 per cent of the total failures were handled during scheduled maintenance time.

2.3 Over-All System Performance

By considering the total computer operating time and the amount of preventive maintenance and new installation work that was done, an

over-all picture of system performance can be obtained. Significant figures are the following:

Total computer operating time	2675 hours
Total extrapolated lost time (calculated from averages)	92.7 hours
Average uninterrupted operating time between incidents	10.6 hours
Failure incidents per 24-hour day	2.19
Percentage operating time usable	96.5 per cent

The figure given above for percentage usable operating time as calculated from the extrapolated lost-time agrees closely with a figure of 96.2 per cent which is the actual percentage of "applications time" usable during the 20-week period as determined from operator reports. Applications time is the time during which the system is used by programming groups rather than by engineering and maintenance personnel.

A summary of the preventive maintenance and installation work is shown in the plots of Fig. 2. New installation and modification projects were essentially completed by the middle of the period. The required preventive maintenance also decreased and for about three months has remained relatively constant at about 1.25 hours per day.

A study of the failure frequencies over the 20-week period since September, 1954, does not show any meaningful variations. The total failure incidents as well as the number in each category are plotted for each two-week period in Fig. 3. Although the total number of failures dropped slightly during the last 8 weeks, the failure patterns for the various categories are too inconsistent to consider the decrease as a significant trend.

3.0 ESTIMATED PERFORMANCE OF IMPROVED SYSTEM

A review of the system-failure records points up the fact that a few sections of the computer have been responsible for an appreciable fraction of the lost time. If an engineering effort to improve these sections were justified, it seems reasonable that a significant reduction in lost time might be realized. In order to obtain some impression of what the system-performance record might be if this work were done, each incident was reviewed and lost-time figures were reduced for failures in those sections that might be improved. In making the estimates it was further assumed that all failures were repaired as rapidly as practicable as if they had occurred during applications time.

The data to be presented is not intended as proof that an improvement program should be undertaken on the Whirlwind system. Rather it it given to permit more realistic estimates of the reliability that might be expected in a new system design.

A summary of the estimated time lost under the conditions described above is given in Table IV. The largest reduction in time lost appears, as might be expected, in the design-weakness category, and some reduction is shown in all categories. If major system improvements had been accomplished, the number of failures in the design-weakness and miscellaneous categories could be expected to decrease. Since this would tend to balance any optimistic estimates for the other categories, the calculated average of 16.8 minutes lost-time per failure would seem to be reasonable.

TABLE IV

ESTIMATED LOST-TIME DATA FOR IMPROVED SYSTEM

Category of failure	Number of lost-time incidents	Estimated lost time (minutes)	Average estimated lost-time per incident	Total number of failure incidents (From Table II)	Extrapolated estimated lost time (Minutes)
Computer Tubes	15	292	19.5	27	527
Power Supply Tubes	7	262	37.5	8	300
Wiring, Cables, etc.	6	145	24.2	7	169
Components	8	239	29.9	16	478
Blown Fuses	15	149	9.9	33	327
Alarms	83	563	6.8	91	618
Design Weaknesses	15	623	41.6	16	667
Miscellaneous	40	865	21.6	46	993
Totals				244	4079

Average estimated lost time per incident =

$$\frac{4079}{244} = 16.8 \text{ min.}$$

Edwin S. Rich

Edwin S. Rich

ESR/bj

Attached: B-62051
A-62050
B-62049

Distribution:

MIT

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N. N. Alperin
P. R. Bagley
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W. J. Canty
J. E. Crane
A. R. Curtiss
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L. D. Healey
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R. A. Imm
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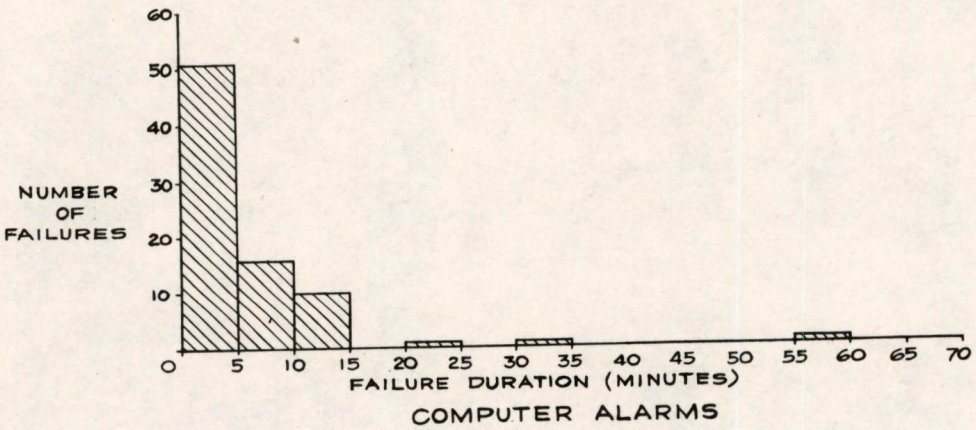
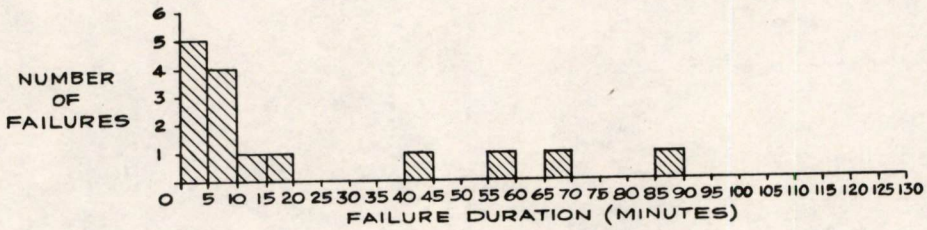
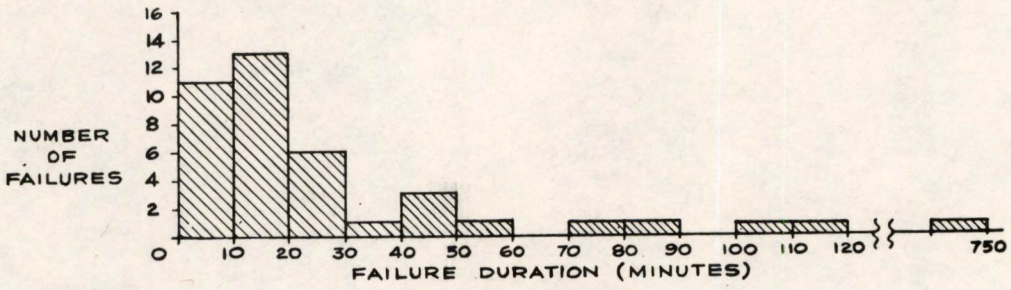


COMPUTER ALARMS



BLOWN FUSES



MISCELLANEOUS

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FIG 1

FAILURE — DURATION DISTRIBUTION

FOR DIFFERENT TYPES OF INTERRUPTIONS

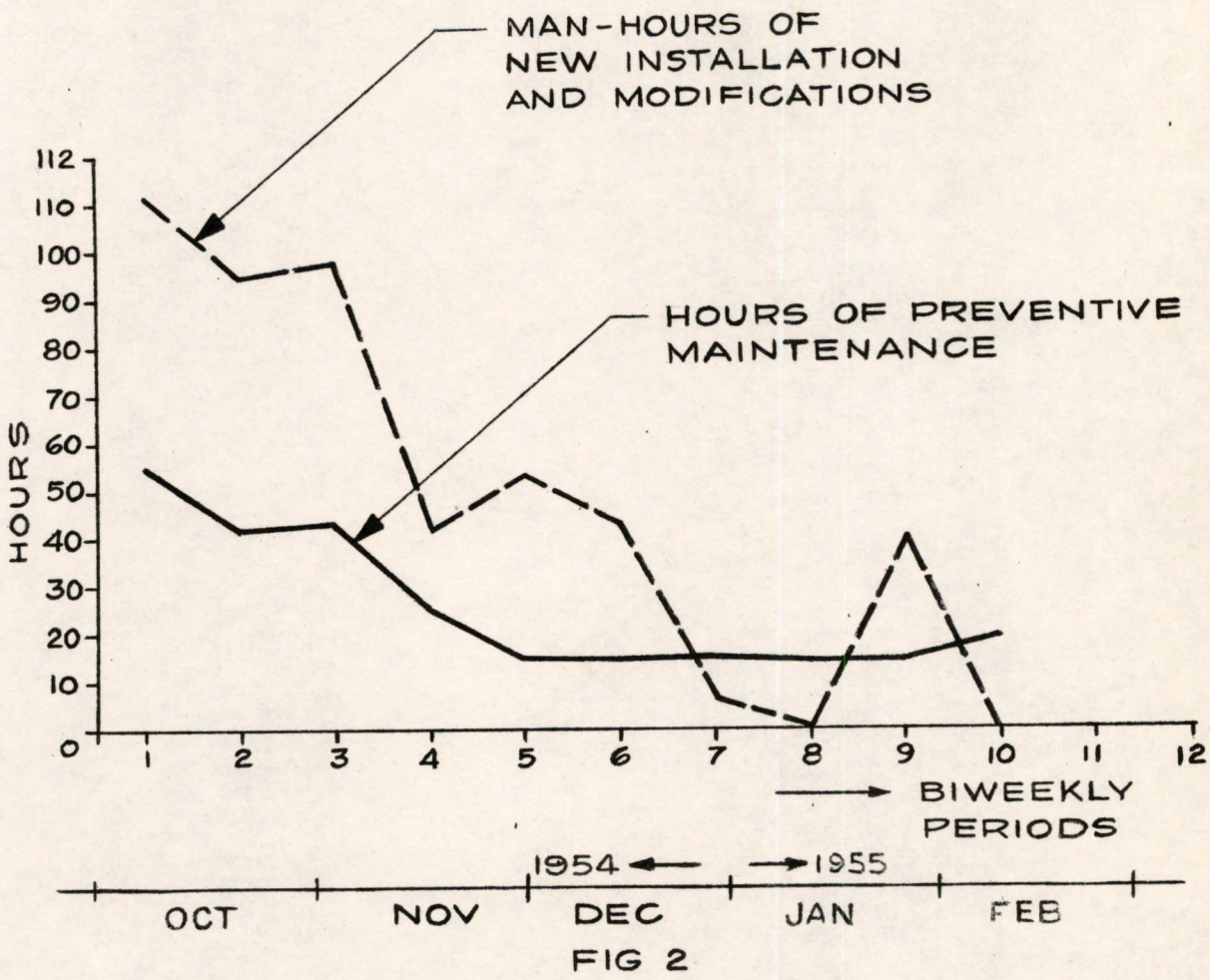

FIG 2

SUMMARY OF INSTALLATION
AND MAINTENANCE WORK

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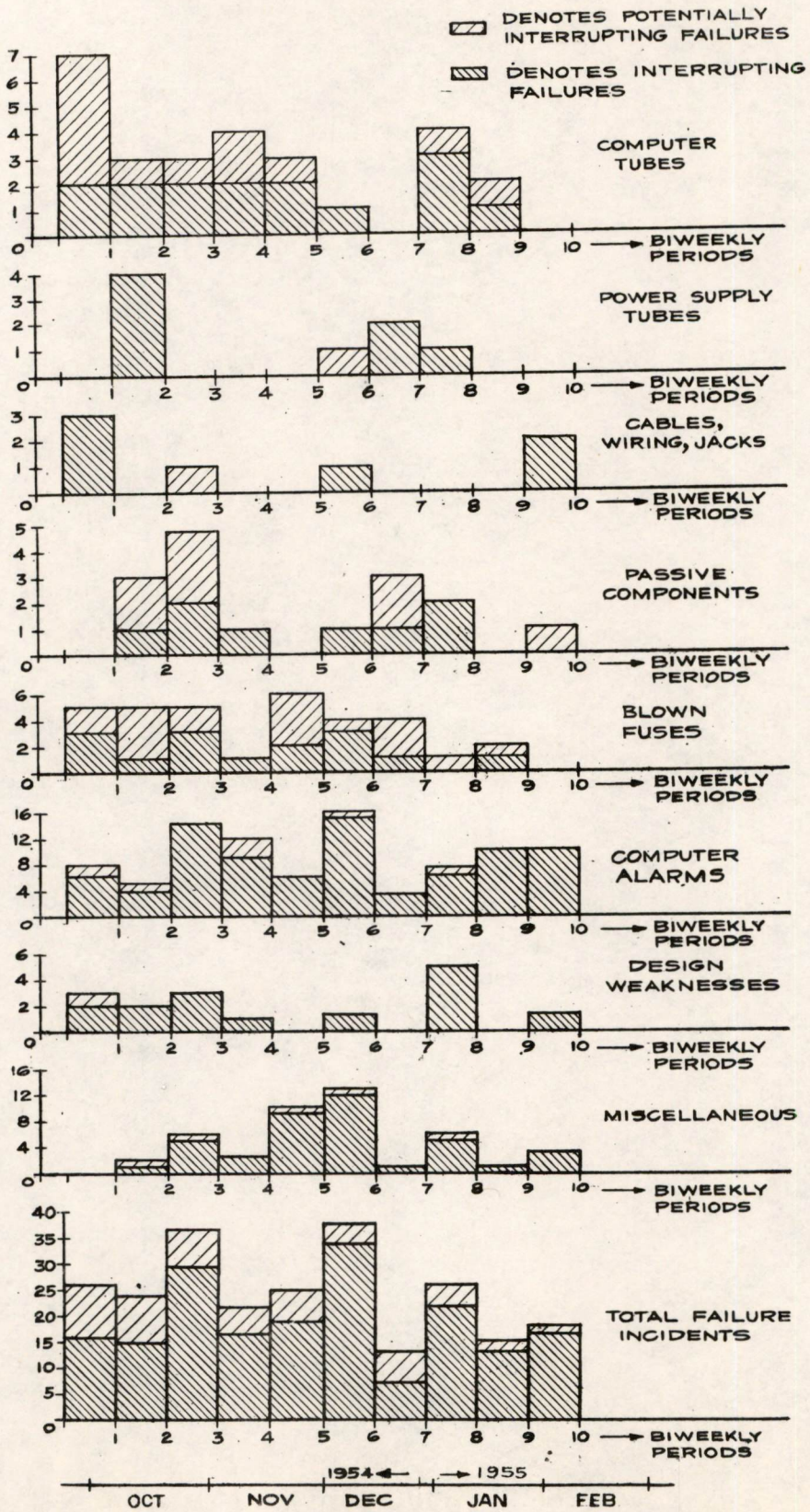

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FIG 3

INTERRUPTING — FAILURE FREQUENCIES

K. H. Olsen
B-188A

Memorandum 6M-3417

F. Williams Sarles, Jr.
March 7, 1955

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: A Transistorized Amplifier-Discriminator for Core Memory Output Sensing

STATEMENT OF THE PROBLEM

The information output of a coincident-current magnetic-core memory of the type used in Whirlwind I (WWI) and the Memory Test Computer (MTC) is essentially the presence or absence of ±0.1-volt, 1-microsecond pulses at specified times. The problem, in brief, is to develop and construct experimentally a transistor system to convert the memory output into the presence and absence of standard computer pulses. In WWI and MTC, standard pulses are 0.1-microsecond long, varying from +20 volts to +40 volts in amplitude; those in a proposed transistor computer will be about 0.1-microsecond long and between -0.5 volt and -3 volts in amplitude. The techniques to be used in a transistor sensing amplifier will involve difference-signal amplification, conversion of the positive and negative pulses from the memory into unipolarity pulses, conversion of these unipolarity pulses into standard computer pulses, and pulse-mixing techniques to allow the use of multiple sense windings in a memory plane. Preliminary investigations have indicated that presently available transistors are capable of handling the greater part of the necessary circuitry.

HISTORY OF THE PROBLEM

Recent developments in Division 6 of Lincoln Laboratory have led to proposals for the development of a new general-purpose computer. One of the primary objectives in the design of this system is a reduction in size and power requirements through the use of transistors wherever possible. In addition, the potentially higher reliability of transistors over vacuum tubes should ultimately result in an increase in over-all reliability of such a system.

A 256 x 256 coincident-current magnetic-core memory will be incorporated in the computer. As stated previously, the memory information output consists of the presence or absence of ±0.1-volt, 1-microsecond pulses at specified times; these must be converted into the standard pulses used in the computer. Four vacuum-tube sensing amplifiers have been designed in conjunction with 32 x 32 and 64 x 64 memories, but no efforts have been made thus far to use transistor circuitry.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

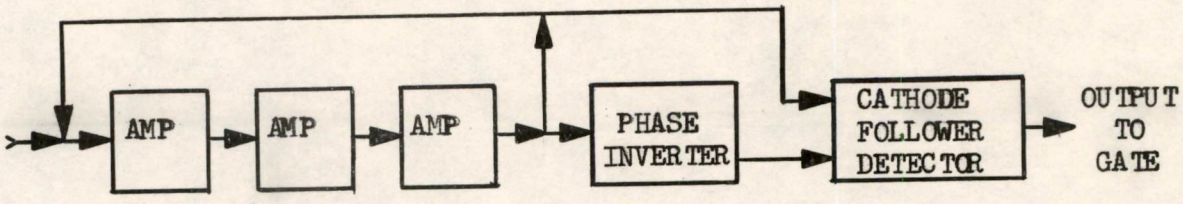
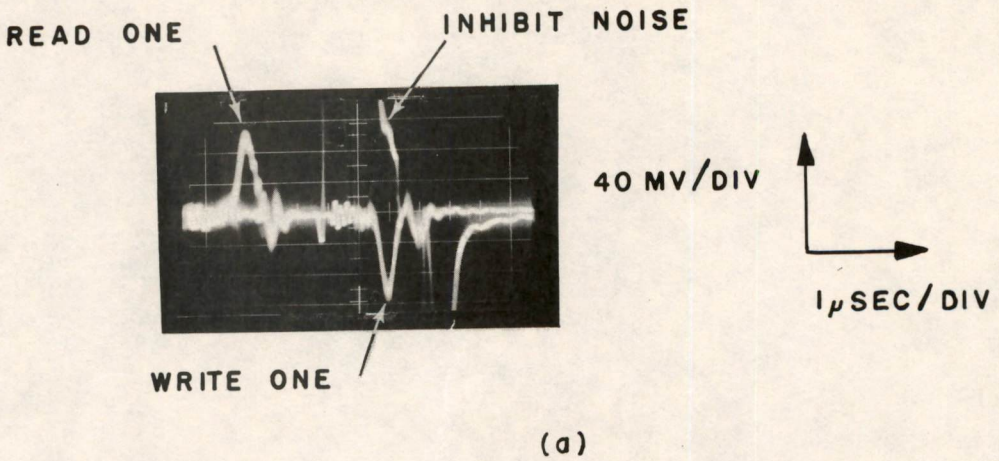


Fig. 1 - Mod. I Sense Amplifier Block Diagram

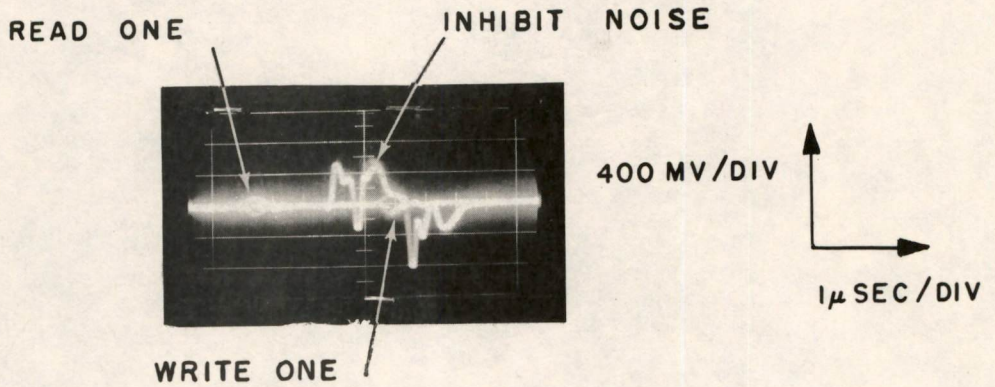
The Mod. I vacuum-tube sensing amplifier (Fig. 1) has a single-ended input into three cascaded pentode amplifiers operating in a feedback loop. The third stage drives one side of a cathode-follower detector and a phase inverter which in turn drives the other side of the detector. The detector output can then set a gating circuit which is strobed, or sampled, at the proper time by a standard 0.1-microsecond pulse.

In experimental setups, this amplifier may have been adequate, and it was used for a while in the WWI memory system. However, it finally proved unsatisfactory because of capacitive noise pickup by the sensing winding. Figure 2a shows the difference voltage across the sense winding with neither side connected to ground. The first pulses are ONEs being read out of a 128 x 128 memory plane; the pulses occurring about 4 microseconds later are ONEs written back into the memory plane. Figures 2b and 2c show the results of grounding either side of the sense winding. The noise has increased considerably, and half of the ONEs have disappeared or at least seem to be greatly reduced in amplitude.

Such a situation obviously requires an amplifier with a balanced input and common-mode rejection; these conditions may be achieved with a transformer or a difference amplifier. Accordingly, the Mod. II sensing amplifier was designed using triode difference amplifiers throughout as indicated in Fig. 3. The output of four cascaded difference amplifiers drives a cathode-follower detector which in turn operates a standard gating circuit.



(a)



(b)

FIG. 4

SENSE-WINDING OUTPUT SHOWING INHIBIT NOISE

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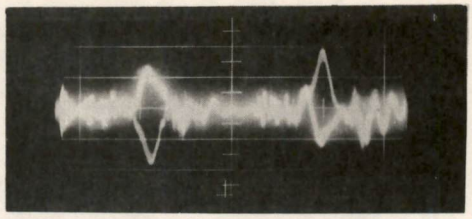

FIG. 2a

SENSE-WINDING OUTPUT WITH NEITHER SIDE GROUNDED

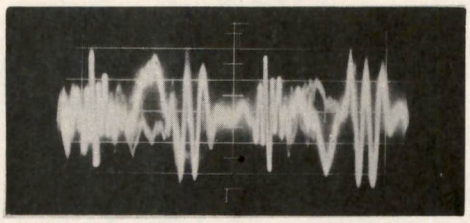

FIG. 2b

SENSE-WINDING OUTPUT WITH ONE SIDE GROUNDED

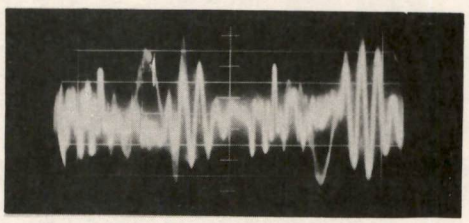

FIG. 2c

SENSE-WINDING OUTPUT WITH THE OTHER SIDE GROUNDED

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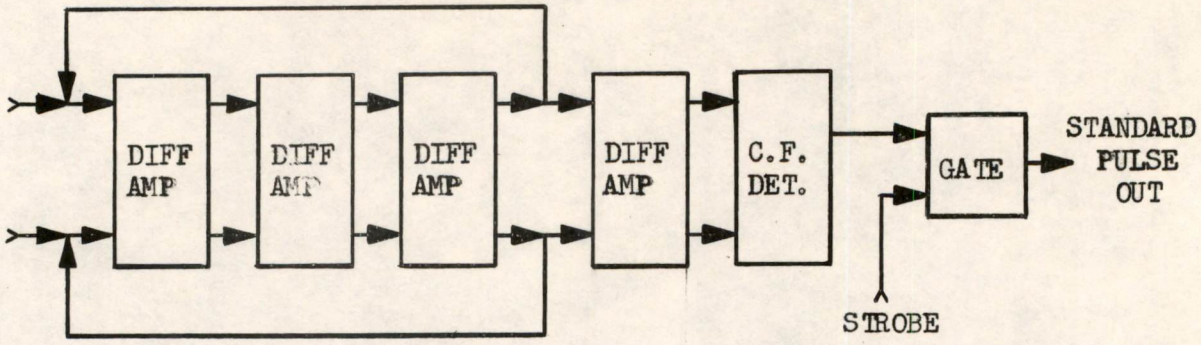

Fig. 3 - Mod. II Sensing-Amplifier Block Diagram

With the Mod. II amplifier, a new problem arose. The use of an inhibit winding for writing information into the memory greatly reduces the number of cathodes required for driving the memory, but operation of this winding disturbs nearly every core in the inhibited memory plane during the rise and the fall of the inhibit pulse. The summations of these disturbances result in pulses which may be as high as 1 volt, as shown in Figures 4a and 4b. By the time these pulses reached the fourth stage of the Mod. II sensing amplifier, they were of sufficient amplitude to cause blocking in this stage.

A second problem was involved in the RC time constants of the interstage coupling circuits. These were originally 70,000 microseconds but were later reduced to 1000 microseconds because of difficulties encountered with extraneous low-frequency transients. In the case of a 64 x 64 memory, C. Laspina indicates that an RC time constant of 200,000 microseconds would be preferable in view of certain pulse sequences which might occur[1].

Efforts to overcome these difficulties resulted in the Mod. III and Mod. IV sense amplifiers. The Mod. III unit was designed by the WWI group for use in the WWI memory. About the same time, the Mod. IV amplifier was designed for use in the MTC. Both units incorporate a transformer input as shown in Fig. 5.

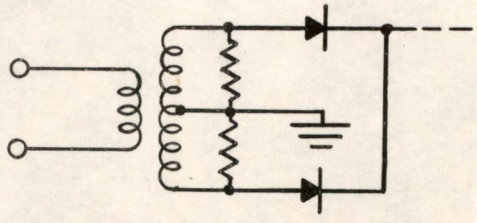

Fig. 5 - Input Circuit of Mod. III and Mod. IV Sensing Amplifiers

1. Laspina, C. A., "Basic Circuits - Sensing Amplifier, Preliminary Specifications, PB#20" M-2274, Digital Computer Laboratory, M.I.T., 3 July 1953.

Since only unipolarity pulses can appear at the output of this curcuit, it is followed by an a-c coupled amplifier with clamping diodes between stages, which eliminates both time-constant problems and blocking difficulties.

The pulse transformer introduced its own difficulty in the form of recovery time. Since the voltage-time integral at the output of a pulse transformer must ultimately be ZERO, application of a positive pulse at the input will result in a negative overshoot, or vice versa, as illustrated by the solid trace in Fig. 6.

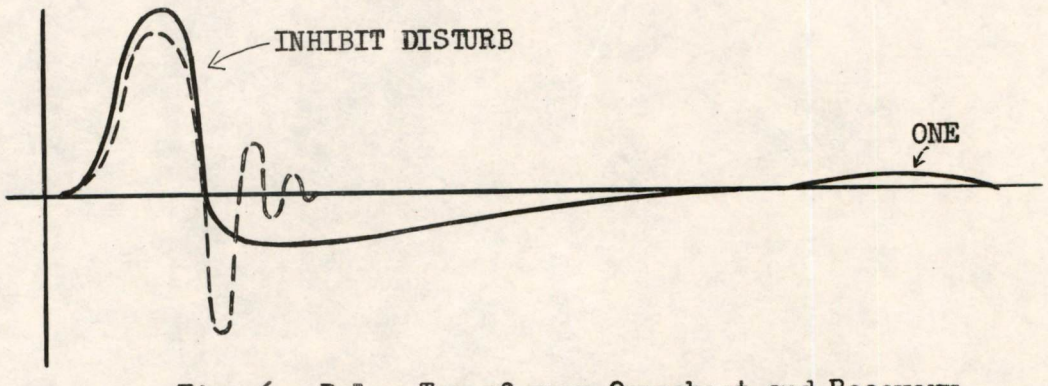

Fig. 6 - Pulse Transformer Overshoot and Recovery

In the memory cycle, information pulses follow the inhibit pulses, but if information occurs while the overshoot from the inhibit pulse is still present, erroneous data may result. Consequently, it is desirable to reduce the recovery time in order to attain a minimum cycle time in the memory. Recent experiments by R. Zopatti at Lincoln Laboratory indicate that the recovery time can be reduced to about 1.5 microseconds by connecting a few turns on the transformer across 1 or 2 ohms of resistance. This results in the dotted trace in Fig. 6 and does not seem to impair the quality of the information pulses.

Vacuum-tube circuitry has not yet yielded a completely satisfactory solution to the sensing problem. It is expected that transistor techniques, although possibly introducing problems of their own, will circumvent some of the inherent difficulties of previous vacuum-tube designs.

PROPOSED PLAN OF ATTACK

Since it is immediately apparent that any system of sensing will require a balanced input and common-mode rejection, the approaches can be divided into two classes, transformer inputs and difference-amplifier inputs.

An important factor to be considered in the design of the sensing amplifier is the total delay time throughout the unit. This delay is usually defined as the time elapsed between the peak amplitude of a ONE at the input and the peak amplitude of the corresponding standard pulse at the output of the unit. WWI and MTC have been designed in such a manner that if a ONE has not arrived at the output of the sensing amplifier by a given time, the computer assumes that the information is a ZERO.

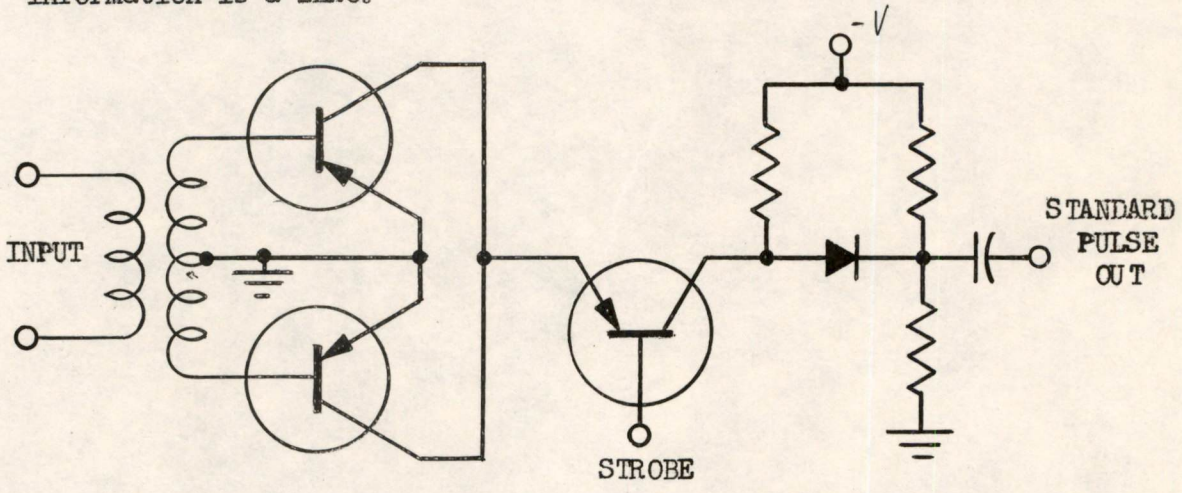

Fig. 7 - Transformer Input Circuit

Figure 7 shows a circuit which could be used with a transformer input. This circuit has the advantage of extreme simplicity but involves the disadvantages of transformer recovery time and delay time through the transformer. Experimental verification of the operational feasibility of the circuit should be a simple matter. If it proves feasible, the major problem will be an investigation of the methods of reducing transformer recovery and delay time.

The alternative to a transformer input is the use of a difference amplifier. A preliminary investigation has been started toward the development of suitable circuitry for this purpose. This has revealed that the primary difficulties in such circuitry would be d-c unbalance because of parameter variations in the transistors and d-c drift. In this case, the major problem would be an investigation of the techniques for minimizing these difficulties.

If a satisfactory difference amplifier can be developed, ONE pulses can easily be changed to unipolarity pulses by the use of diode rectifiers at the output of the circuit. Conversion of the 1-microsecond memory pulses to 0.1-microsecond pulses will be attempted either through the use of a two-transistor chain gate following the diodes or by gating the difference amplifier itself so that it is inoperative except during strobe time. Figures 8 and 9 show possible circuits incorporating these methods.

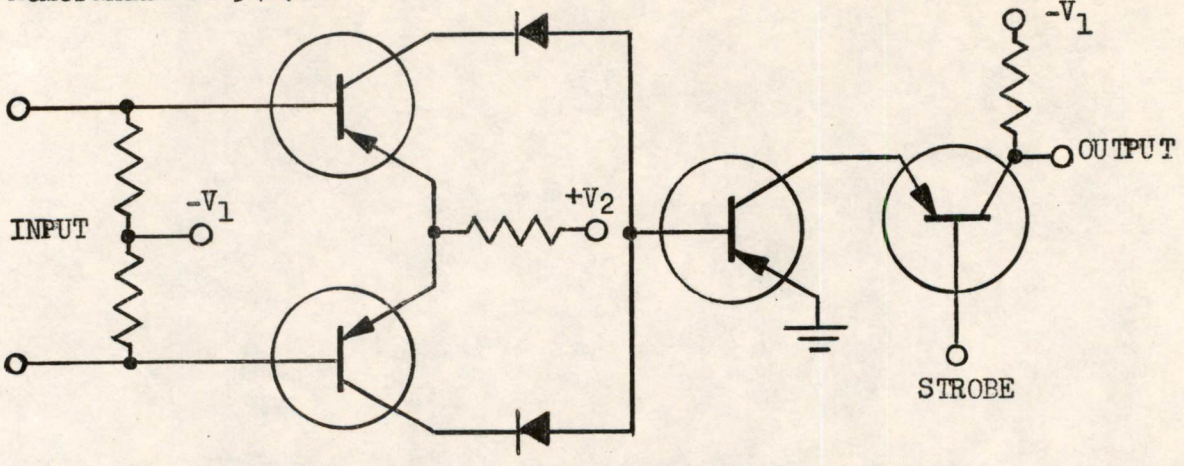

Fig. 8 - Difference Amplifier with Gated Output

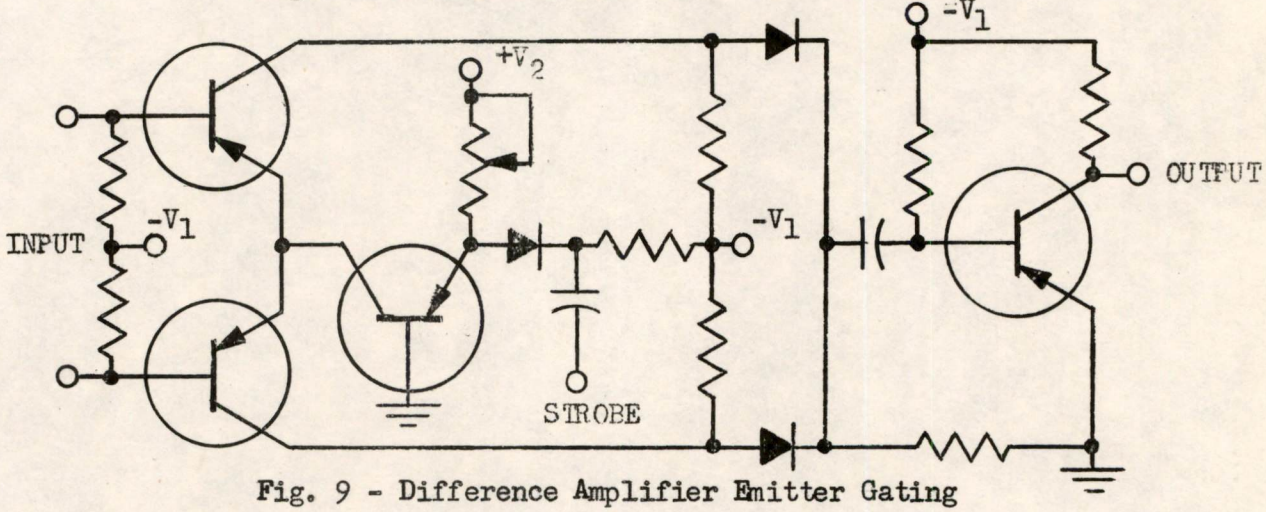

Fig. 9 - Difference Amplifier Emitter Gating

A 256 x 256 memory plane will probably contain at least four sensing windings. All of the circuits contemplated have been designed with diode outputs to allow these outputs to be mixed. In the case of the circuit of Fig. 9, for example, this could be accomplished as shown in Fig. 10.

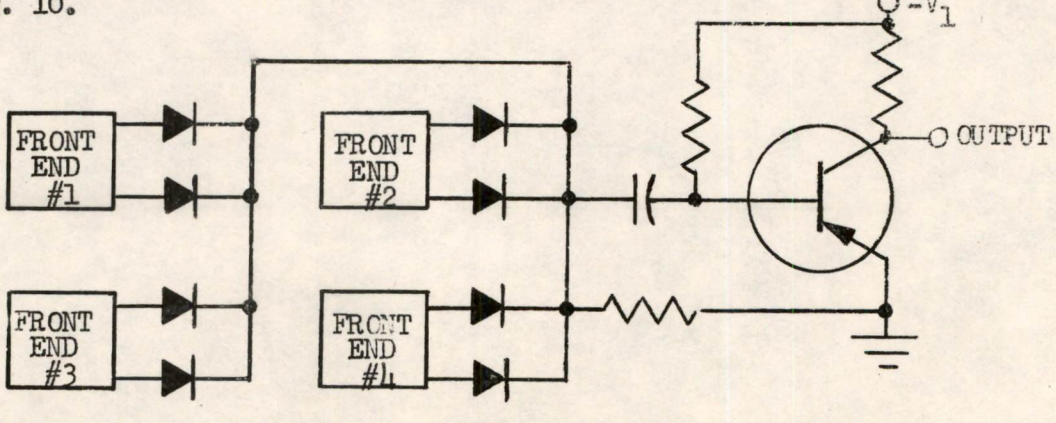

Fig. 10 - A Possible Mixing Scheme Using the Circuit of Fig. 9

A ONE in any winding will turn on one diode which in turn back-biases all other diodes, thereby discriminating against noise from the unselected windings. The previous circuits are contemplated for use in a transistor computing system. Followed by a vacuum-tube power amplifier, they should be suitable for possible use in the MTC and WWI systems. This is the one instance when vacuum-tubes would be necessary, as no available transistors can supply a 0.1-microsecond pulse at a power level of 10 watts.

PROPOSED PROCEDURE

1. Experimental verification of the feasibility of the transformer input circuit of Fig. 7 will be attempted.

2. If this circuit proves feasible, methods for minimizing transfoermer recovery and delay time will be analyzed.

3. At the same time, investigation will continue to develop a suitable difference amplifier for a sensing system.

4. If a satisfactory difference amplifier results, the gating schemes mentioned will be incorporated with the amplifier and evaluated.

5. If a 256 x 256 plane with multiple sense windings is available, an experimental model incorporating the more satisfactory techniques will be built and tested. In any case, a model suitable for use with MTC will be built and tested.

EQUIPMENT NEEDED

All necessary equipment is available from Lincoln Laboratory.

ESTIMATED TIME

Preparation of Proposal	50 hours
Further search of literature	20
Experimental work and analysis	165
Correlation of results and formulation of deductions and conclusions	40
Preparation of thesis	75
	350

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DATE: March 7, 1955

FWS,jr./dg

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the Thesis.

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

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SUBJECT: PULSE AMPLIFIERS (MODELS A, B, AND C)

To: Those Listed

(mixer-input) mod II B (+250)
C (+150)

From: Bruce Barrett

Date: March 28, 1955

(non mix input) mod III B (+250)
C (+150)

Approved: R. L. Best
R. L. Best

Abstract: Light or heavy relatively constant loads may be driven by the $_{A}$PA and $_{B}$PA, respectively. The $_{C}$PA characteristics make it better suited to driving loads which may vary from light to medium - heavy. An $_{A}$PA and $_{C}$PA combination will drive loads which vary from light to extremely heavy.

INTRODUCTION

A comparison between the $_{A}$PA, $_{B}$PA, and $_{C}$PA permits a rational choice among the three so as to satisfy given load and pulse output amplitude requirements. It is possible to choose a pulse amplifier and terminating resistor so that a standard pulse* will appear across any reasonable load provided that a standard pulse is the input to the pulse amplifier. That is, these three pulse amplifiers make it possible to realize the standard transfer characteristic* over a wider range of loads than was heretofore practicable.

The same bogie 7AK7 was used for making each of the curves in figures 4 to 8 inclusive.

MODEL A PULSE AMPLIFIER

The Model A pulse amplifier ($_{A}$PA) is shown in Fig. 1; its transfer curves are shown in Fig. 4. Notice that the $_{A}$PA is unsaturated for inputs less than 25 volts and saturated for inputs greater than 25 volts and that the output varies greatly with load (behavior explained by the fact that in this circuit the tube saturates at a given amount of plate current). The plate current is limited by over-suppression, the result of a tightly wound suppressor tied to a fixed low voltage.

The transfer curves show that the $_{A}$PA can satisfy standard pulse and transfer characteristic requirements* provided the load is not too heavy and the terminating resistor is chosen properly.

*See transfer characteristic and standard pulse specifications in Appendix I.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

MODEL B PULSE AMPLIFIER

The $_{B}$PA (Fig. 2) is like the $_{A}$PA except that it is tetrode connected - that is, the suppressor is tied to the plate. A comparison of the transfer curves of the $_{B}$PA (Fig. 5) with those of the $_{A}$PA (Fig. 4) shows that the $_{B}$PA can deliver more power into any load for a given input pulse, and that (for 270-ohm and 91-ohm loads) it saturates at a fixed output current. This effect is due to plate bottoming - i.e., the plate voltage drops to the lowest level it can assume and yet maintain the plate current at the level demanded by the load. Increasing the input pulse above the saturation level has no effect on the output pulse amplitude on either of these load curves.

The 47-ohm curve shows it to be impossible to terminate the $_{B}$PA low enough to insure a maximum output of 40 volts while still achieving unity gain for a 20-volt input. Terminating the $_{B}$PA at a high value yields an output pulse of excessive amplitude. Hence, the $_{B}$PA relies on a fairly heavy non-linear load to meet standard transfer-characteristic requirements.* (Most computer loads are nonlinear.) Therefore, the $_{B}$PA is used only for loads too heavy for the $_{A}$PA.

MODEL C PULSE AMPLIFIER

The $_{C}$PA (Fig. 3) is like the $_{B}$PA except that it has a plate-supply voltage of 150 instead of 250. Comparison of its transfer characteristics (Fig. 6) with those of the $_{B}$PA (Fig. 5) shows that, like the $_{B}$PA, the plate bottoms on the $_{C}$PA, so that its output is relatively independent of the load when it is driven with a large pulse. Comparison of transfer curves of the $_{C}$PA and the $_{A}$PA shows that for the critical input amplitudes of 20-25 volts the $_{A}$PA will deliver more power into any load. The advantage of the $_{C}$PA over other pulse amplifiers is that it can meet standard pulse and transfer characteristic requirements* for light loads and that the terminating resistor can always be made high without need for tailoring. This is particularly advantageous where load and driver are in separate frames and where the distance between these frames is not exactly known. An additional advantage of the $_{C}$PA is its unique ability to drive a load that varies from no load to maximum while still meeting standard transfer-characteristic requirements.* Examples of such loads are capacitor-diode gates, diode-capacitor gates, and loads switched through relays.

When the plate of the $_{C}$PA bottoms most of the tube current goes to the screen grid. Hence, the $_{C}$PA can only be used for low duty cycle signals (up to 200 - kc/ repetition rate for 0.1 μsec pulses).

$_{A}$PA - $_{C}$PA COMBINATION

For loads which vary from very heavy to very light and which require a standard pulse over these extremes, a two-tube driver is used; this consists of an $_{A}$PA followed by a $_{C}$PA. This combination will set a range of $_{B}$FF's (any number from zero to 17) through 14 feet of co-ax delivering a standard pulse at the output of the $_{C}$PA throughout this

* See transfer characteristic and standard pulse specifications in Appendix I.

range of loads. A 270-ohm terminating resistor was satisfactory for this range of loads. It's value was not critical.

The 270-ohm $_{A}$PA terminating resistor is normally used in the $_{A}$PA - $_{C}$PA combination (Fig. 7). In the event that a device with a peak current rating of 150 milliamperes (such as the Z or W diode in a capacitor-diode gate) is used in the grid circuit of the $_{C}$PA, the 180-ohm resistor is required to cut down the peak grid current (Fig. 8).

The $_{C}$PA screen-grid dissipation limits the use of this combination to repetition rates below 200 kilocycles.

SUMMARY

The use of the pulse amplifiers may be summed up as follows:

Light fixed or varying loads: $_{C}$PA, since it may always be terminated in 270 ohms and this termination need never be tailored.

Loads too heavy for $_{C}$PA: $_{A}$PA

Loads too heavy for $_{A}$PA: $_{B}$PA

Loads varying from light to very heavy: $_{A}$PA - $_{C}$PA combination

Signed: Bruce Barrett
Bruce Barrett

BB/er

Drawings

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A-61919
A-61928
A-61929
A-61930
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Appendix I

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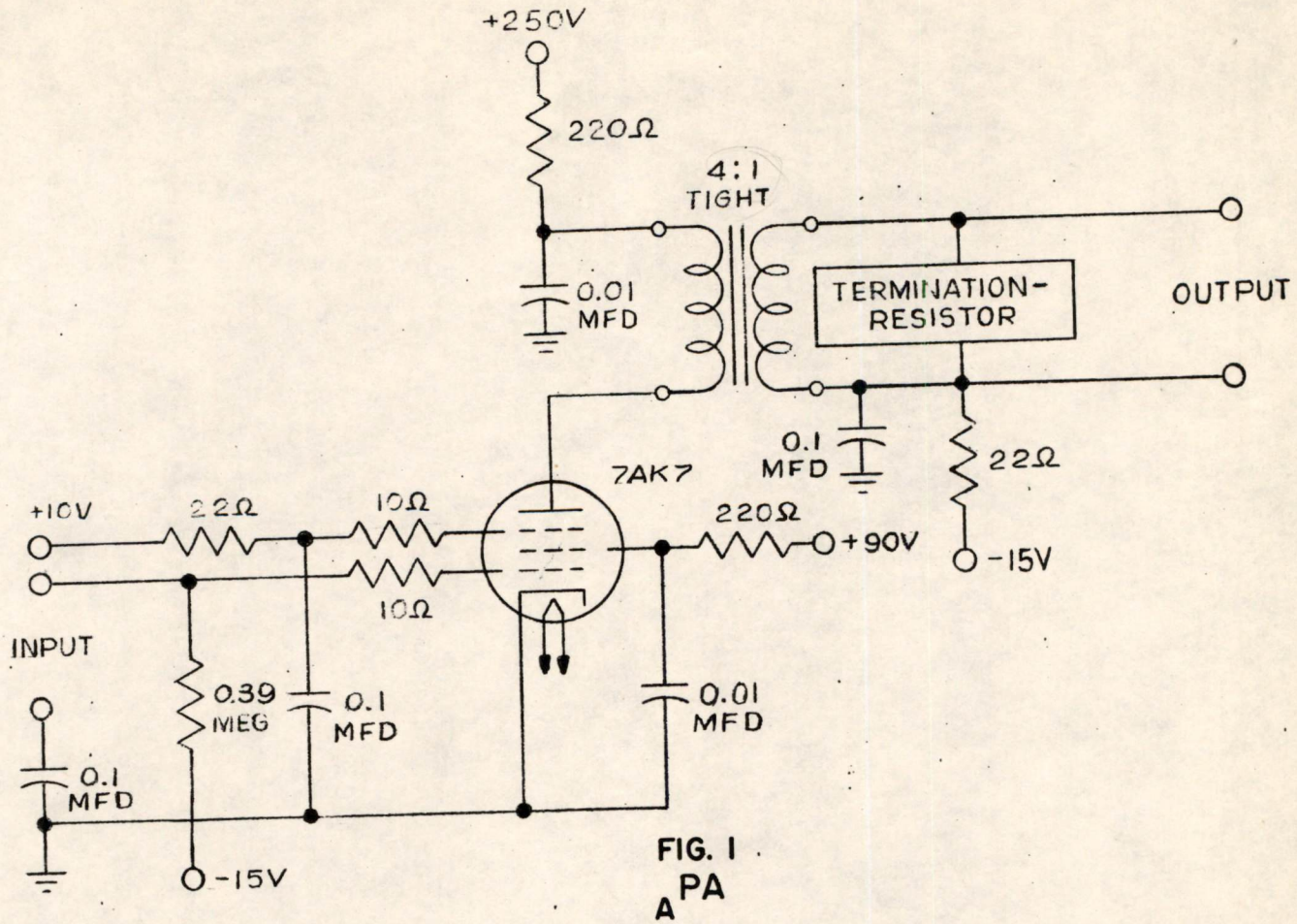


FIG. 1
A PA

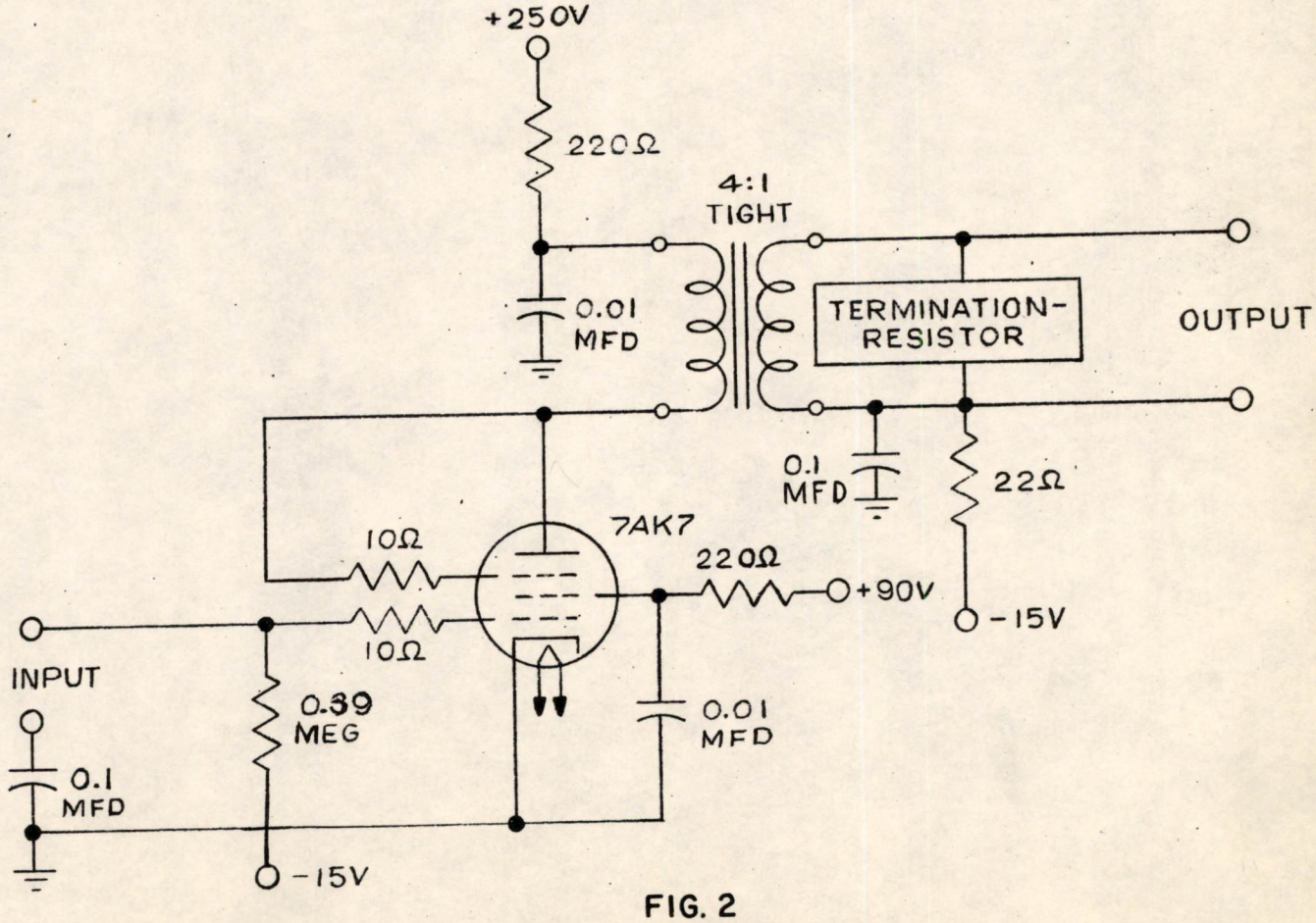


FIG. 2
B PA

9-61918

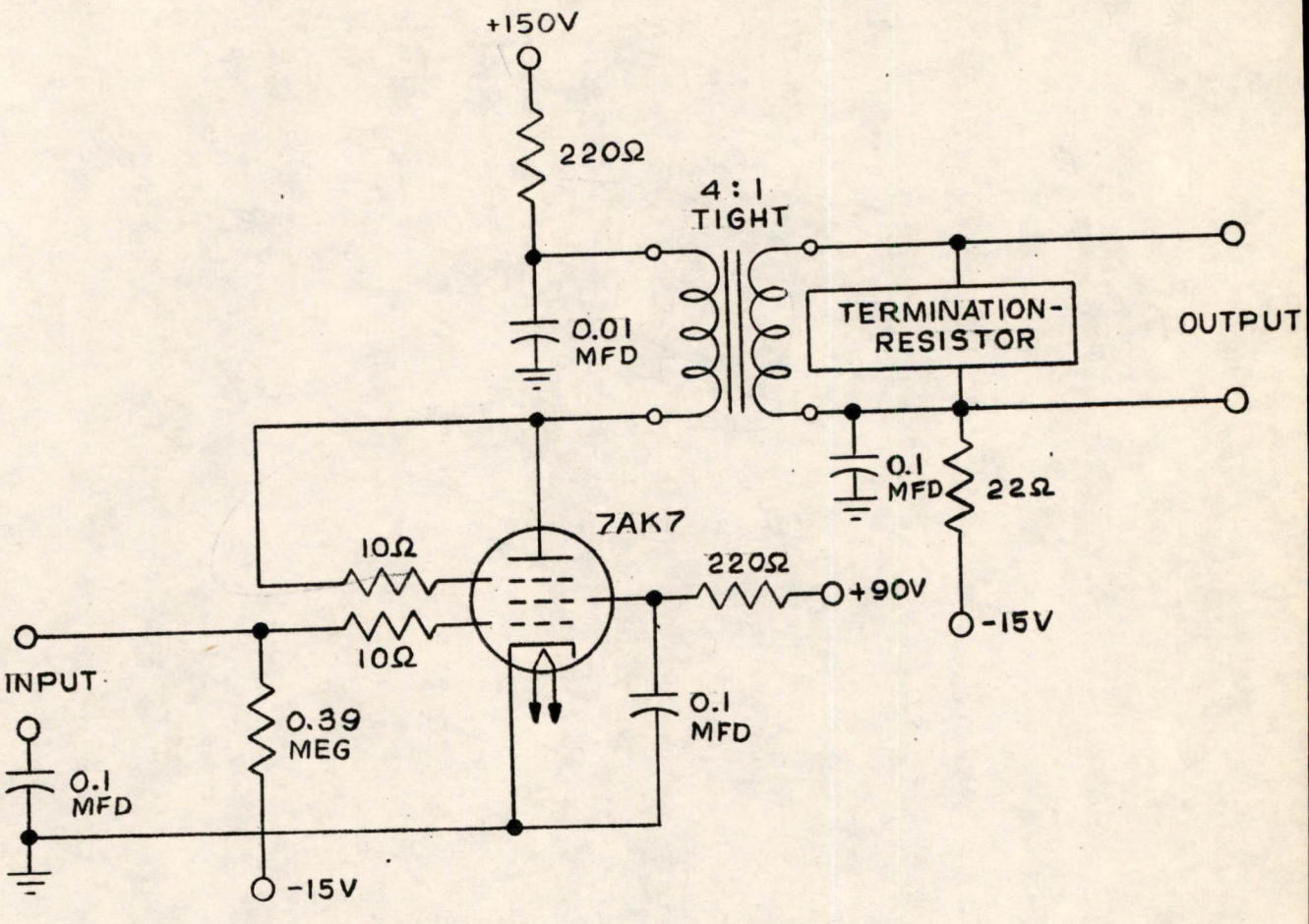


FIG. 3

PA

C

A-61919

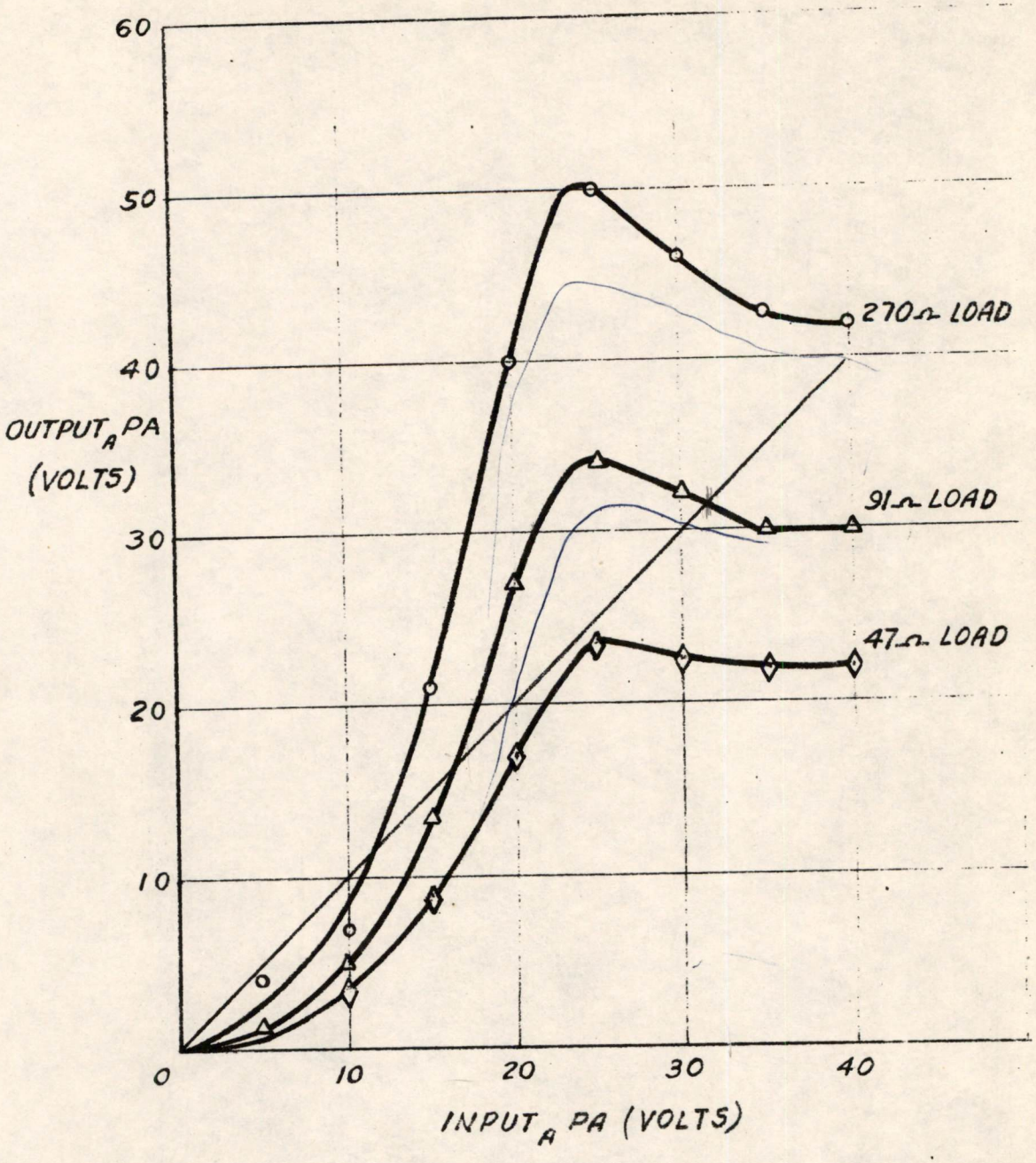


FIG. 4

A PA TRANSFER CHARACTERISTICS

A-61928

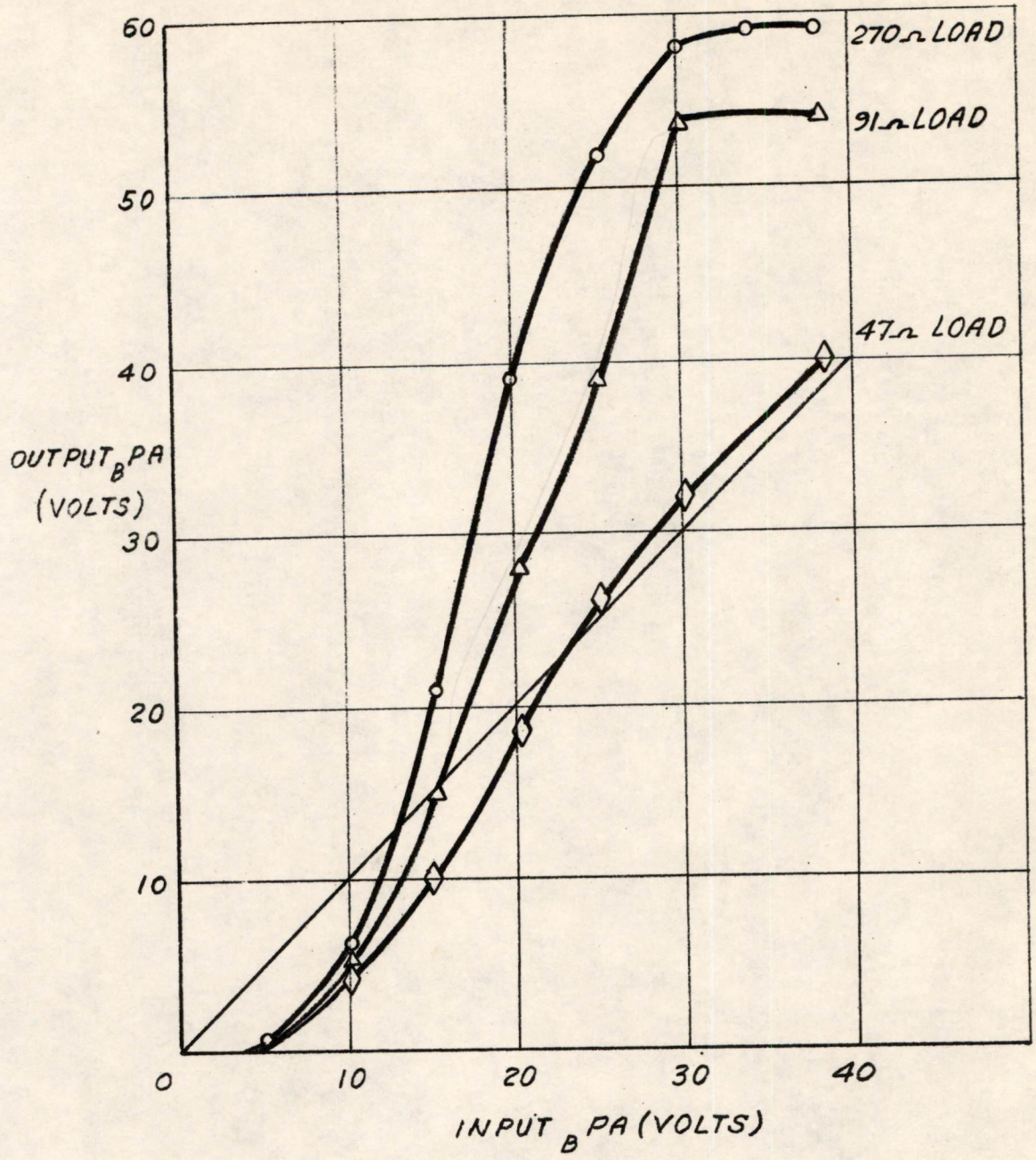


FIG. 5

$_B$PA TRANSFER CHARACTERISTICS

A-61929

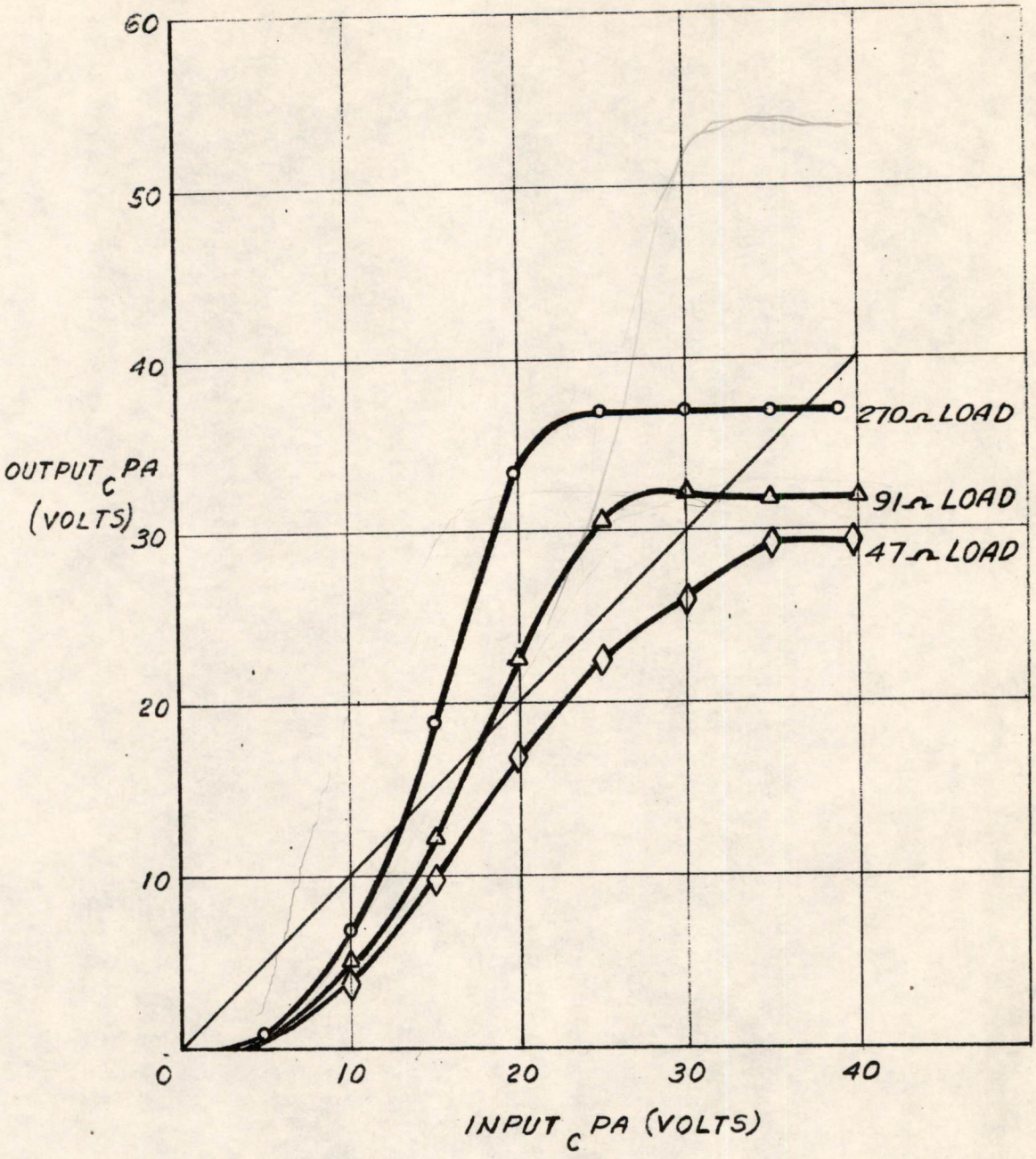
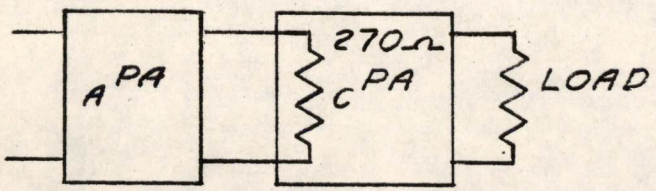


FIG. 6

C PA TRANSFER CHARACTERISTICS

A-61930



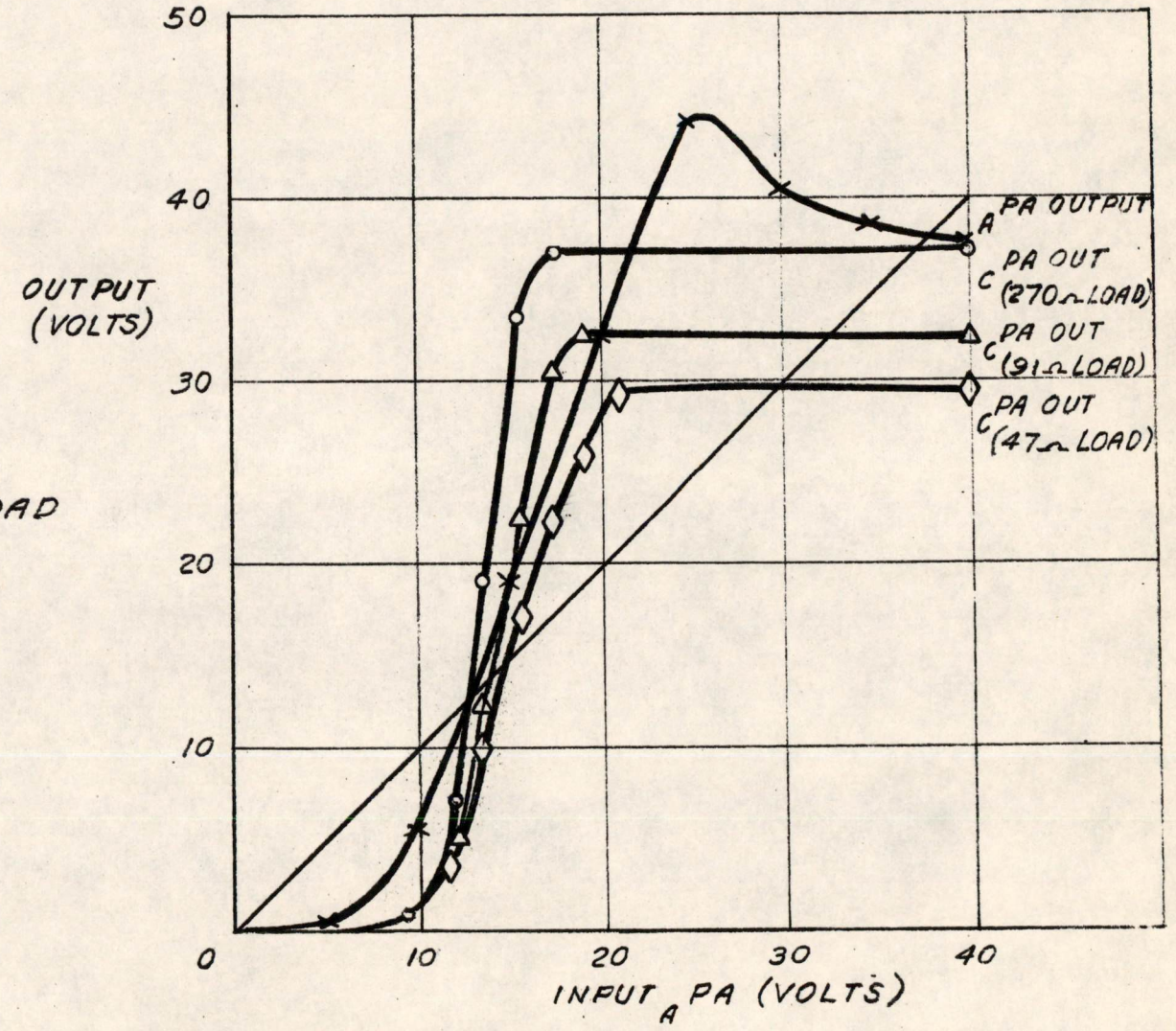
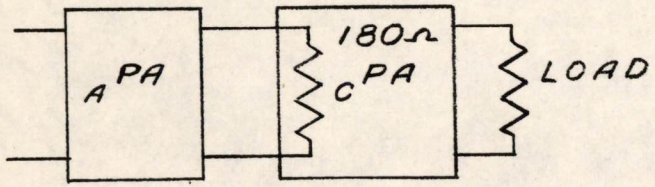


FIG. 7
A PA - C PA TRANSFER CHARACTERISTICS
(A PA TERMINATED IN 270Ω)

A-61932



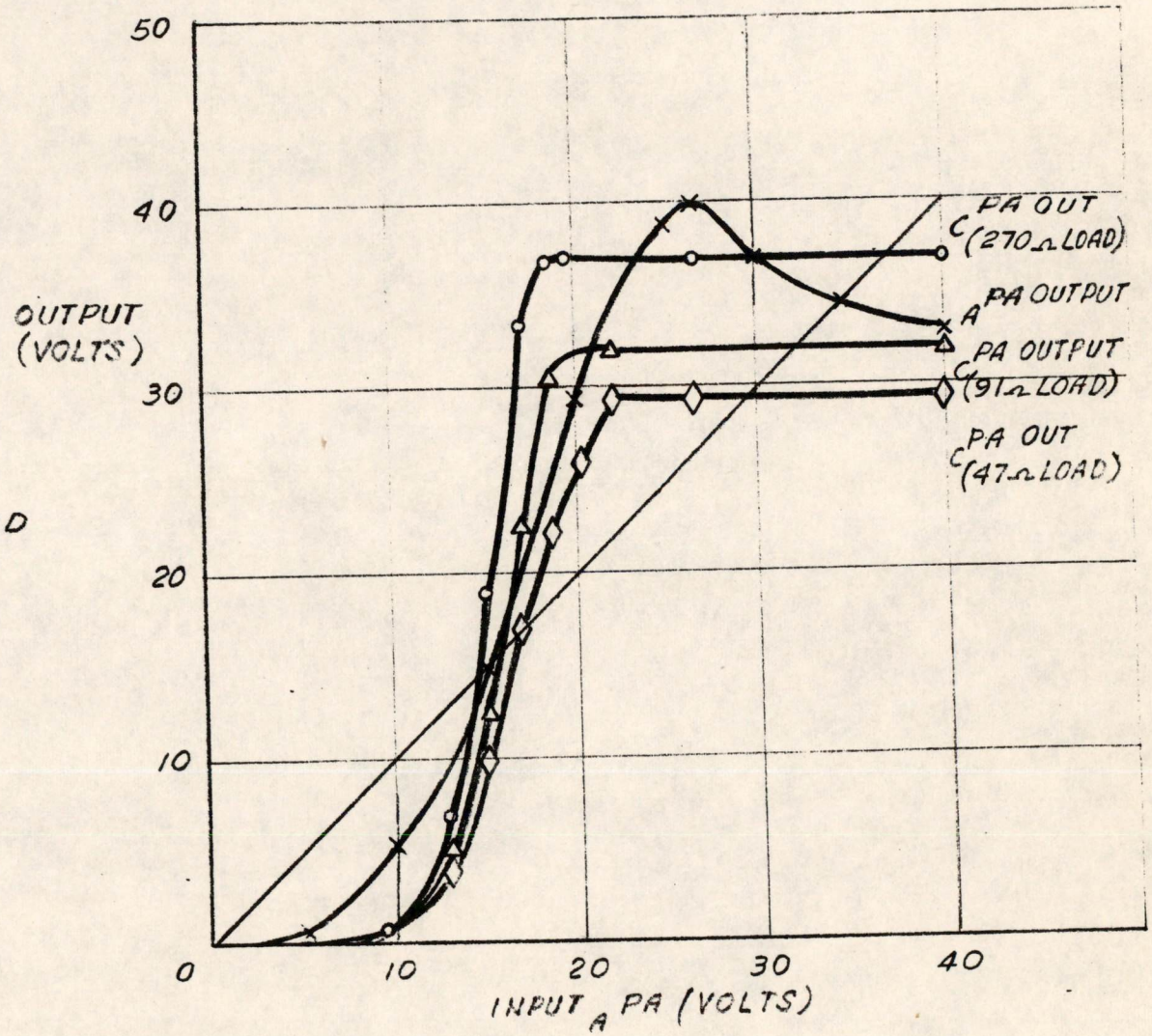


FIG. 8

A PA - C PA TRANSFER CHARACTERISTICS

(A PA TERMINATED IN 180Ω)

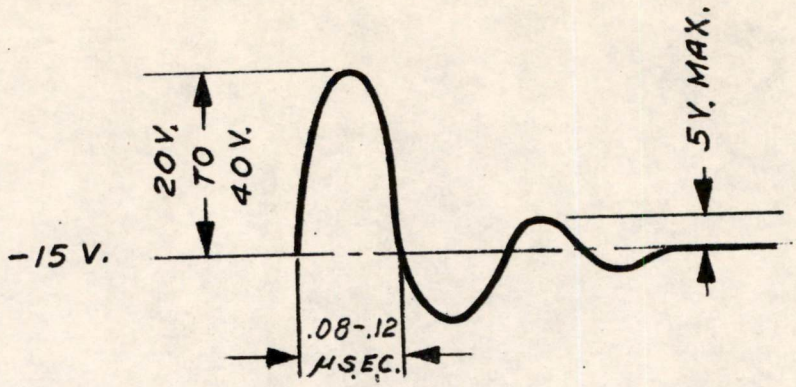


FIG (a)

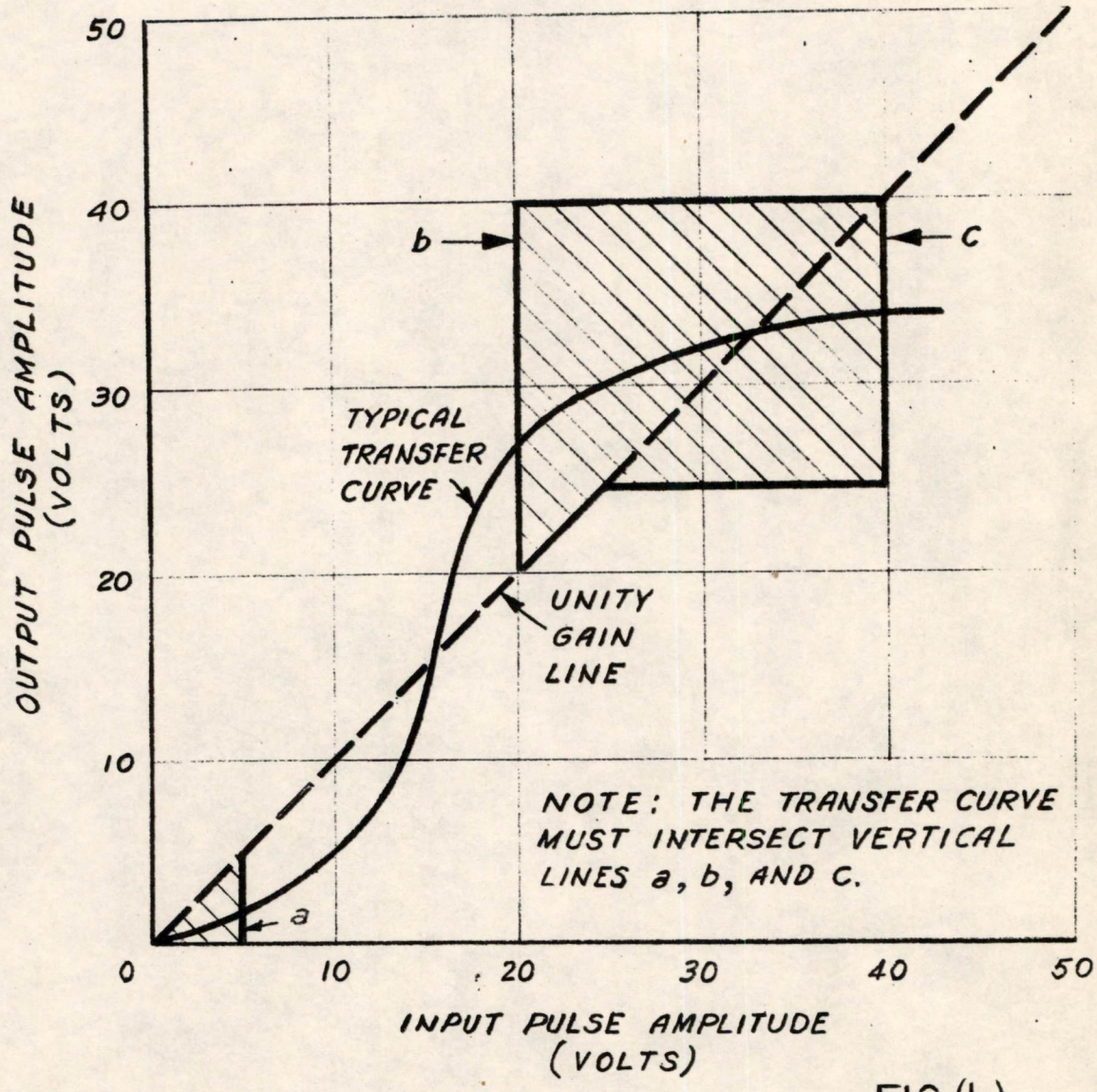


FIG (b)

APPENDIX I

(EXCERPTED FROM CIRCUIT APPLICATIONS SECTION OF MRD BOOK)

APPENDIX I

(Excerpted from Circuit Applications Section of MRD Book)

Standard Pulse

A standard pulse is defined to be a positive pulse whose shape may vary from a triangle to a square wave (the normal shape is a half sine wave), to be from 20 to 40 volts in amplitude, to be from 0.08 to 0.12 μsec in duration and whose maximum allowable positive overshoot is 5 volts.

Standard Transfer Characteristic

The standard transfer characteristic shall yield a gain of less than unity for inputs of 0 to 5 volts, greater than unity for inputs from 20 to 25 volts, and for inputs of from 25 to 40 volts the output shall be from 25 to 40 volts. The output shall never exceed 40 volts. See figure (b) of Appendix I.

K. Olsen

EXPERIMENTS ON A THREE-CORE CELL FOR HIGH-SPEED MEMORIES

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Magnetic Memories

The coincident-current magnetic-core memory was suggested in 1949 by Jay W. Forrester[1] as a reliable, random-access storage medium. Development of the first working memory of this type, for the Memory Test Computer at M.I.T., established conclusively the superiority of such a memory over competitive systems and paved the way for others to exploit the new device.

The coincident-current memory uses two properties of ferromagnetic materials[2], (Fig. 1) non-linearity and remanence, to perform the basic functions, selection and storage, required of a multiple-register memory. As shown in Fig. 2, each core in an array lies at the intersection of a unique set of x, y, and z coordinate wires. The remanent-flux state of a given core determines whether it holds a ONE or a ZERO. Simultaneous half-amplitude current excitations on one of each set of x and y lines cause a single core in each z or digit plane to receive full switching current while all other cores in the plane remain essentially unchanged. If the core holds a ONE, a large voltage is induced on a sense winding which links all the cores in a digit plane; a ZERO produces a small output. In order to write into the core, currents opposite in direction to the original excitations are supplied, and the core is switched back to the ONE state. If a ZERO is to be written into any digit plane, a half-amplitude pulse in the read direction is also applied during write time on the appropriate digit winding; thus, the core is prevented from switching to the ONE state.

Two important characteristics of this system are:

1. An entire row and column in each digit plane are "half-driven," producing small, spurious outputs on the sense winding which tend to mask the signal from the selected core.

2. Switching time of the core is fixed by the knee of the hysteresis loop of the material since this establishes the allowable current excitations on the coordinate lines.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

These are the two outstanding limitations on the coincident-current memory. The first tends to limit the size of the array from which a signal can be easily detected and places fine restrictions on core uniformity. The second limits the speed of operation which depends on the switching time of the core. It has been found experimentally that the product of switching time and net field applied to the core is approximately a constant, S_W, (called the switching coefficient) for a given material[3]. The governing equation is:

$$S_W = (H-H_0)\ T$$

where T is switching time, H is applied field, and H_0 is an intercept value usually related to the knee of the loop. The restrictions on current range impose a corresponding restriction on memory cycle time, or the time between successive memory accesses.

These two limitations are the price paid for performing both selection and storage functions in a single core.

External Selection

A system has been developed[4] which essentially assigns the performance of these two functions to separate cores and thereby overcome the restrictions mentioned above. A similar system has been proposed independently by Dr. R. J. Slutz of the National Bureau of Standards[5].

Consider the problem of using switch cores in a magnetic-core memory to perform the selection function completely external to the memory cores themselves. Such a selection system must be capable of subjecting any memory core in a selected register to either of two cycles:

Read, Write ZERO ($R\text{-}W_0$)
or Read, Write ONE ($R\text{-}W_1$)

without exciting any other cores in the array. (A ZERO and a ONE are stored in the usual manner as shown on the hysteresis loop of Fig. 1.) For cycle $R\text{-}W_0$, it is only necessary to have a sequence which begins and ends with a current pulse of positive polarity. For the $R\text{-}W_1$ cycle, all that is required is that the first pulse be positive and the last negative. These two cycles are shown in Fig. 3. Note that a switch core must always be reset to its original flux state before the start of a new cycle, that is, its output will always be symmetrical and made up of two oppositely poled pulses. This is

ideal for the R-W_1 cycle since it can be performed by a single switch core. The R-W_0 cycle cannot come from a single core, however, but can be produced by the combination of two switch-core outputs (A and B, Fig. 4). The two cycles thus obtained are shown in Fig. 4.

The A and B drives are shown overlapped for minimum time, yielding a three-beat cycle. It is evident from above that the minimum number of switch cores needed is one per register to supply output A (each core in the register receives it) and one core per bit to supply output B (each core may or may not receive this, depending on whether a ONE or a ZERO is being written). A winding through all the B cores of a given digit plane can be used to provide an inhibit current which prevents output B when a ONE is to be written. Although only one A core is theoretically required per register, the system described here uses one per bit, thus making the cell a symmetrical three-core unit (Fig. 5) for ease of construction and to eliminate the large size core needed to drive an entire register.

The switch cores are all biased by a negative current. A two dimensional system of excitations switches a single core while only driving other switch cores in the plane along the saturated portion of the hysteresis loop. The output currents from these partially-selected switch cores are the only excitations passed on to non-selected memory cores.

By a complete separation of switching and memory functions, the cores are no longer restricted by the critical requirements on driving currents and hysteresis-loop squareness imposed by coincident-current operation. The hysteresis loop required for a coincident-current memory is shown in Fig. 1. Ideally, the loops required for switch and memory cores in the proposed system could be as shown in Fig. 6. The main requirement of the switch core is that it be saturable; of the memory core, that it have two distinct remanent-flux states. The poorer the saturability of the switch core the greater the partial-select excitations the memory core must withstand without changing flux state.

Experimental Results

In order to determine the feasibility of this system and to measure its operating characteristics, a series of experiments was performed on individual three-core cells. These were aimed at seeing how operation was affected by variations in the flux ratio between switch and memory cores, coupling-loop impedance, input current, pulse timing, and core material.

Experiments[6] indicate that for best operation the switch core should have at least 6 times as much flux as the memory core, and the coupling loop between the two cores should be resistive. Scope photographs for a cell incorporating these principles are shown in Fig. 7.

Figs. 7a and b show typical voltage outputs for the two switch cores when ONEs and ZEROs are being stored alternately. Fig. 7c shows the memory-core outputs for a ONE and a ZERO superposed. Ideally, the switch core should contain just sufficient flux to support the voltage drop in both the coupling loop and the memory core. Coupling-loop resistance must be large enough so that the inductive time constant of the switch-core secondary is short thus making it possible to squeeze the pulses close together. It cannot, of course, be made larger without limit, otherwise insufficient secondary current will be supplied to switch the memory core. Fig. 8 shows ONE and ZERO outputs superposed for each of three improper designs. In Fig. 8a, the switch core has insufficient flux and does not completely switch the memory core. In Fig. 8b, the coupling loop has no added resistance, and the current pulses decay slowly making it impossible to run the pulses close together. (The cell operates perfectly if pulses are spaced further apart giving an overall cycle time of 3 microseconds.) In Fig. 8c, too much resistance has been added to the loop, limiting secondary current so that the memory core does not switch fully. In all three cases it is almost impossible to distinguish between a ONE and ZERO.

In experimenting with various core materials, it was found that a wide range could be made to work satisfactorily. The best results were obtained, of course, for materials having the squarest loops. Here it was possible to obtain a ONE-to-ZERO ratio of about 15 to 1, ONE-to-half-select ratio of 250 to 1, and a complete cycle time of 0.4 microsecond. (Voltage ratios are for peak values.) As in coincident-current memories, a canceling sense winding minimizes the effects of partially selected outputs. For such a winding the difference between partial-select outputs for a core holding a ONE and for a core holding a ZERO becomes the significant factor. For the cell tested, this difference was too small to measure accurately.

Memory Criteria

The memory system described above is only one of a very large number which uses the magnetic core as its basic element. Any engineering design which attempts to translate this into a practical working device might well use the following criteria to measure and evaluate various systems:

1. Reliability, which is most easily estimated by tube count and margins;

2. Size (number of registers x number of places = number of bits);

3. Cycle time, the minimum time between successive readouts;

4. Cost, mainly determined by core specifications and quantity, wiring complexity, and tube count.

Design Considerations

The principal disadvantages of the three-core-cell memory lie in the increased complexity of construction and the large number of cores which are used. The construction difficulties arise primarily from the small coupling loops linking each memory core to its two switch cores. Such problems tend to increase core interspacing. As a result, it is felt that this type of system will be most useful in memories of relatively small size, up to a few thousand registers. Since the problem of half-select noise in coincident-current memories is not too significant in these small sizes, one of the principal advantages of the three-core system is wasted. It would seem that the greatest advance could be made by concentrating on speedier cycle times as the main goal for the system since - ideally - there is no upper limit to the excitations which can be applied to the cores. The principal problem is that the high currents needed here mean more tubes; also, faster switching times mean larger back voltages from cores (possibly counterbalanced by a reduction in flux through a change in core size and/or material).

The power generated in the core goes up as the square of the speed. This is because the energy required per cycle to switch a core is roughly proportioned to the inverse switching time, and the number of cycles possible per second increases at about the same rate. The heat generated in the core because of this power loss can have a serious effect on the pulse response of ferrite materials. Fortunately, there is a wide range of core characteristics over which this system should work well so that system operation ought not to be too sensitive to heating at these high speeds.

Probably the most important single criterion for choosing cores for this system is a low value of the switching coefficient S_W, which implies relatively low driving currents for a given speed of operation and low power loss with consequently reduced heating.

Preliminary Design of Plane

Successful experimentation with three-core cells has led to a preliminary design for a single 16 x 16 plane (Fig. 9). This plane will use novel construction methods to overcome the wiring complexities inherent in the system. The switch cores (both A and B) are all on one side of a single board. The memory core is on the other side suspended between two lugs on a piece of bus. The resistance wire, which forms the small coupling loops when connected to the lugs, is wound on in continuous lengths rather than being handled in small separate pieces. The grid of driving lines is wired on the switch cores in much the same way as in a conventional coincident-current memory.

The switch cores to be used in this plane will be 80 mils O.D., 50 mils I.D., 30 mils height, or about one-and-one-half times the size of the memory core used in the Memory Test Computer. The memory core will be about one-sixth the size of the switch core. At present, there is no simple way to fabricate such a small core. For this experimental plane, the simple expedient of boiling down larger cores in acid will be used. The plane will be designed to operate with a complete cycle time of less than 1 microsecond. It is felt that this is fast enough to be a worthwhile goal without entailing too many complications in the associated electronics. The core material will be an experimental mixture provided by the General Ceramics Company. The memory core signals should be of the order of 0.2 or 0.3 volt. It is hoped that the driving currents required will be no higher than about 2 amperes.

The long-range practicality of this type of memory system depends largely on the ability of alternative devices to do the same job. At the present time, the coincident-current memory seems to be the only other system which offers the possibility of operating within the range of 1-microsecond cycle time. This would require the use of a high-coercive-force material which still maintains the requisite hysteresis-loop squareness at high pulse rates. The development of such materials is, in any case, a worthwhile goal along with the long-range problem of reducing S_W (and, therefore, power requirements) for memory materials in general.

JR/dg

Drawings: A-61950
A-58815
A-61951
A-61952
A-61953
A-61954
A-61997
A-61998
A-61955

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3. Menyuk, N., Energy Dissipation in Square-Loop Ferromagnetic Materials with Specific Application to Switch Cores, Report M-2160 (May 12, 1953), Division 6, Lincoln Laboratory.

4. Raffel, J. I., Switch for Register Selection in a Magnetic-Core Memory, Report R-234, Pages 75-78, (May 24, 1954), Division 6, Lincoln Laboratory.

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6. Bradspies, S., A Magnetic-Core Memory with External Selection, S.M. Thesis (January 1955), Electrical Engineering Department, M.I.T.

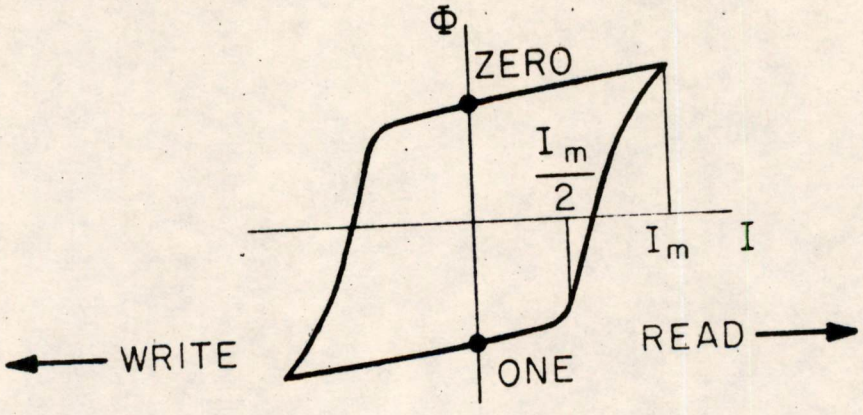


FIG 1

TYPICAL MEMORY CORE HYSTERESIS LOOP

A-61950

A-58815

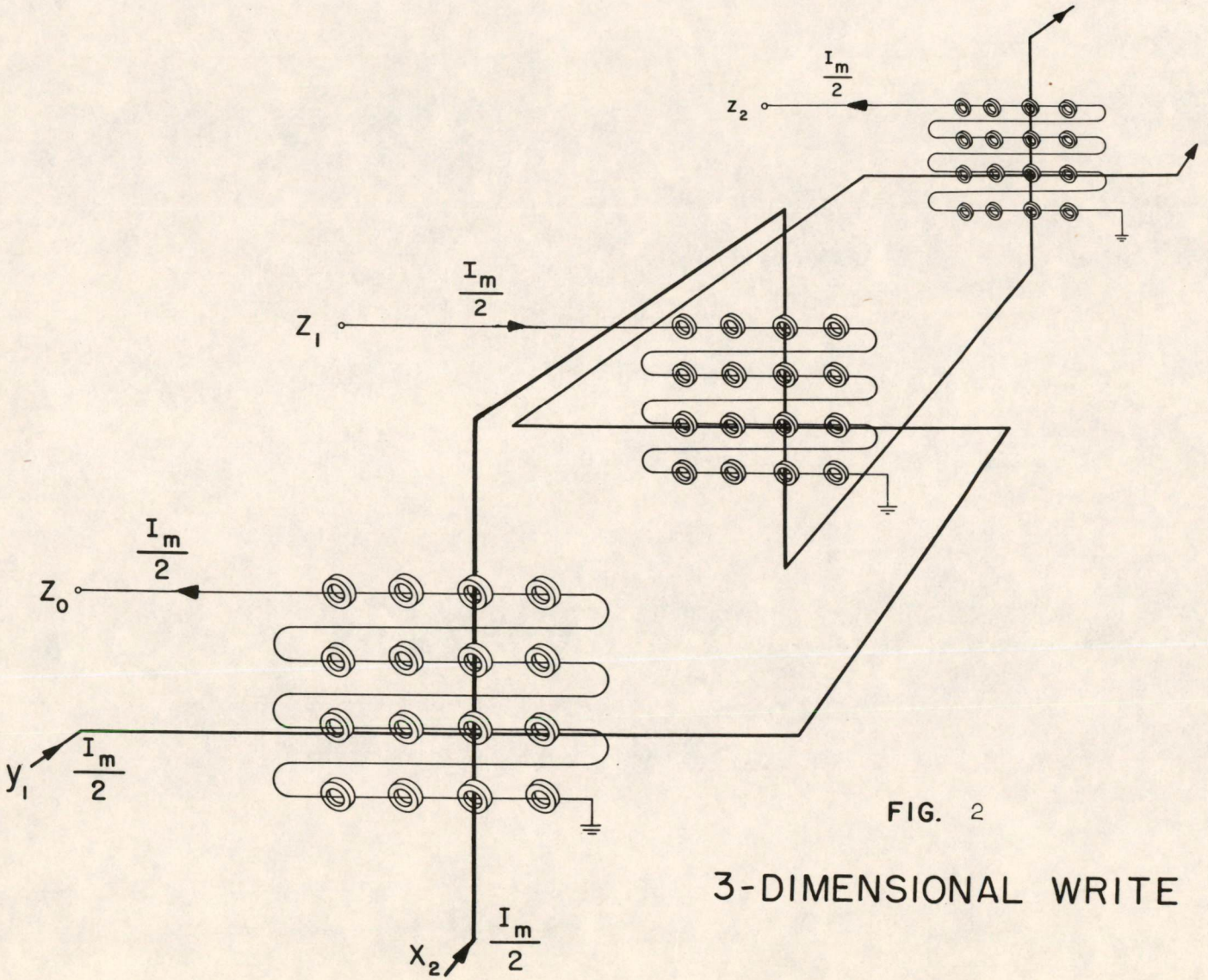


FIG. 2

3-DIMENSIONAL WRITE

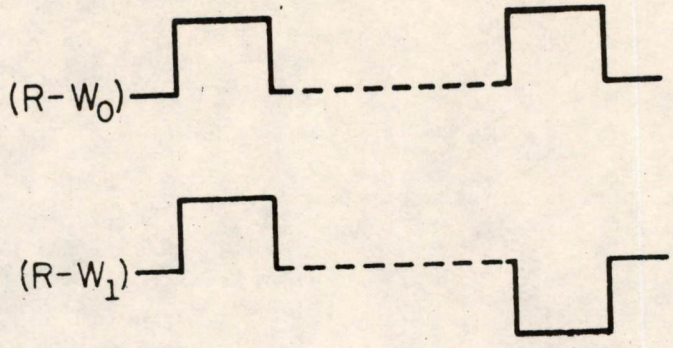


FIG. 3

PULSE SEQUENCES REQUIRED FOR DRIVING MEMORY

A-61951

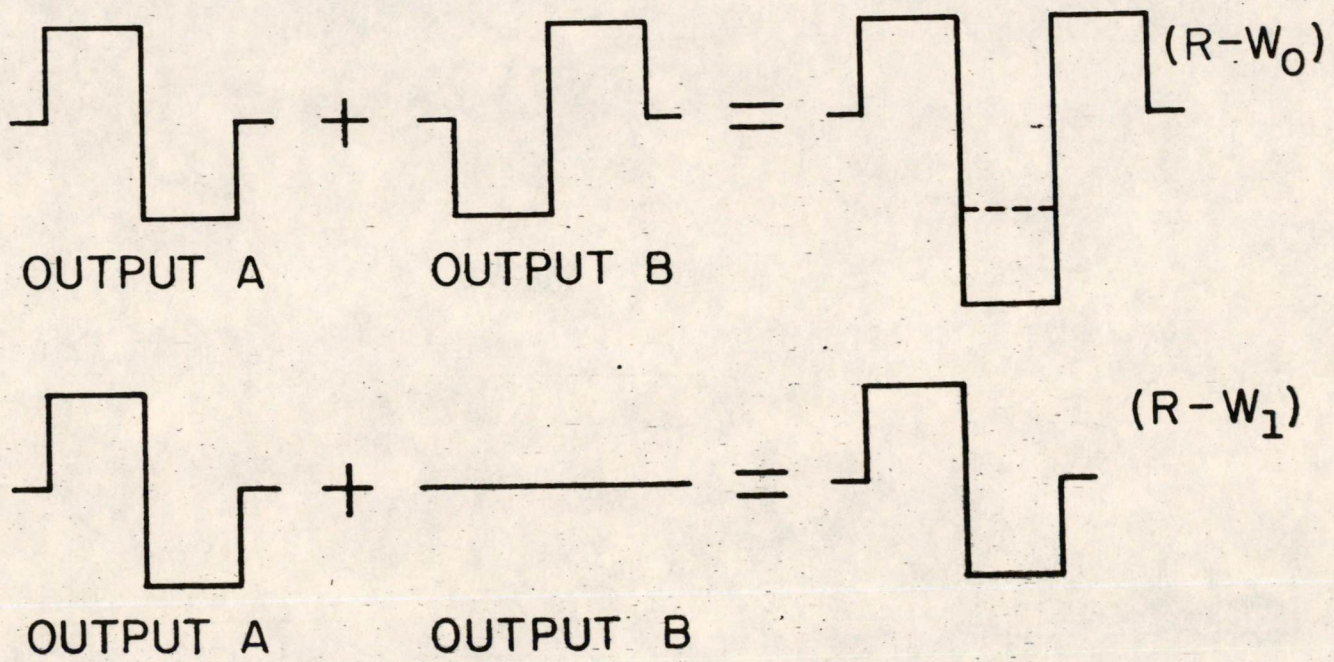


FIG. 4

COMBINED OUTPUTS TO PRODUCE R-W_0 AND R-W_1 CYCLES

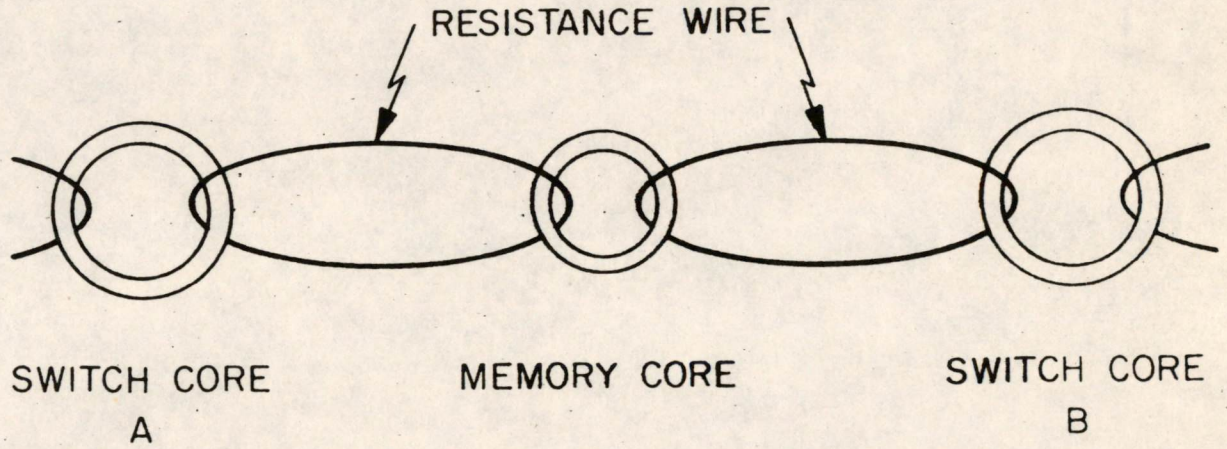


FIG. 5
THREE CORE CELL

A-61954

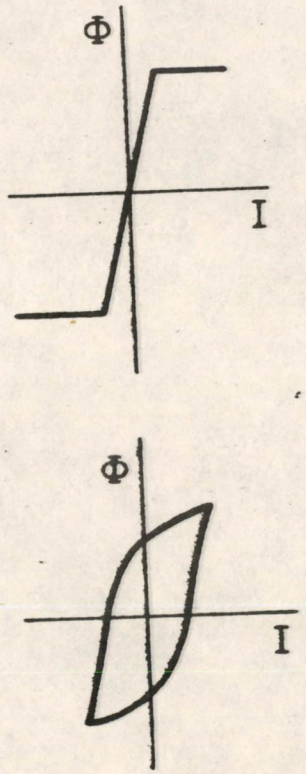
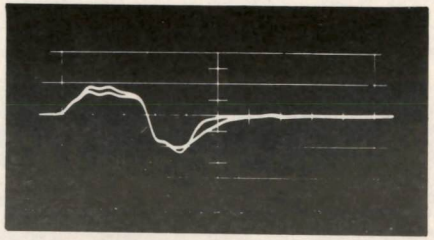
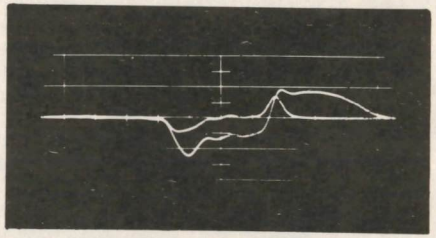


FIG. 6

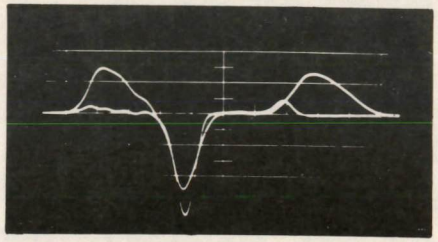
THEORETICALLY USABLE SWITCH AND MEMORY CORE LOOPS



SUPERPOSED VOLTAGES ACROSS SWITCH CORE A
FOR READING ONES AND ZEROS



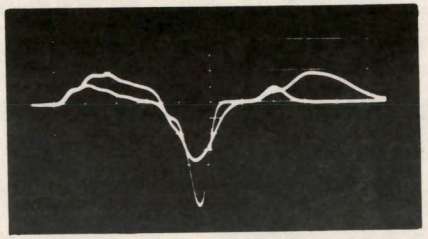
SUPERPOSED VOLTAGES ACROSS SWITCH CORE B
FOR WRITING ONES AND ZEROS



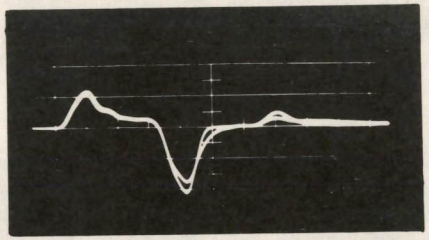
SUPERPOSED MEMORY CORE OUTPUT FOR
ONE AND ZERO

FIG. 7

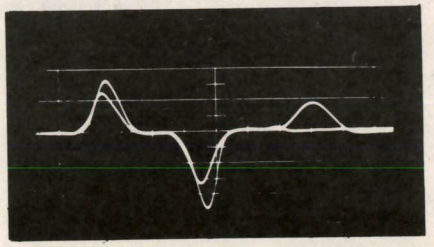
TYPICAL CELL VOLTAGES
(0.1 μSEC/CM)



CASE OF TOO LITTLE FLUX IN SWITCH CORE



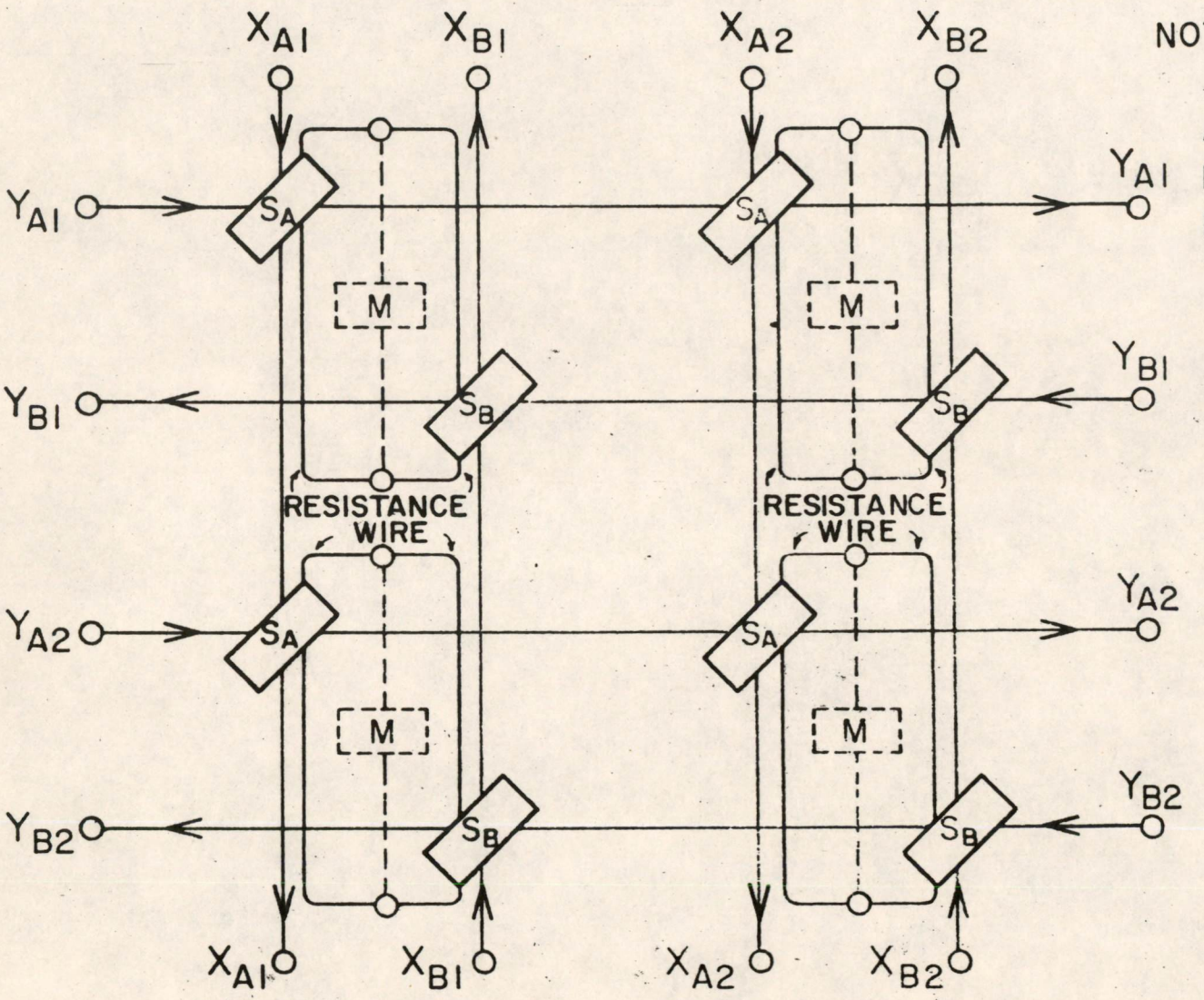
TOO MUCH RESISTANCE IN COUPLING LOOP



TOO LITTLE RESISTANCE IN COUPLING LOOP

FIG. 8

MEMORY CORE OUTPUT, ZEROS AND ONES
FOR THREE CASES OF IMPROPER DESIGN



NOTE:

SWITCH CORES ARE ON ONE SIDE OF PHENOLIC BOARD, MEMORY CORES ON THE OTHER. NOT SHOWN ARE BIAS WINDINGS LINKING EACH SET OF SWITCH CORES AND SENSE WINDING LINKING MEMORY CORES.

FIG. 9

2 X 2 MEMORY PLANE USING THREE CORES PER CELL

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: IMPROVED MEMORY CORES PRODUCED IN LINCOLN LABORATORY

To: Group 63 Staff

From: F. E. Vinal

Date: 13 April 1955

Approved: DRB

D. R. Brown

Abstract: Recent memory core production in the Lincoln Laboratory pilot plant has offered an improved variety of cores for experimental project use. Typical characteristics are shown for these cores and the principal advantages to be derived from their use are discussed. A comparison of characteristics is made between our cores and those commercially available. The basis of selection of superior cores is described and the extent of production capacity for our pilot plant is given. Methods which may be employed to improve further the characteristics of memory cores of this type are suggested, and, to some extent, the degree of further improvement which may reasonably be expected is noted.

Introduction

For some months, the Chemistry Section of Group 63 has been producing for project use a variety of memory cores improved over those obtainable commercially. The properties which have been improved, as well as the degree of improvement, have been the subject of considerable discussion, leading in some instances to misunderstandings about our cores, their properties and their use. It is the purpose of this memorandum to present enough data about our cores to enable engineers to make "educated guesses" about their performance in various applications, and to make clear that although considerable progress has been made with memory cores, there is plenty of room for further improvement and the development of special adaptations.

Performance

The "proof of the pudding" for our memory cores will, of course, be their performance in the coincident-current-memory application. All test data has been taken with this application in mind, and, thus far, only one set of operating conditions has been intended, namely, the use of the

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

cores at a driving current of 820 ma. and in a matrix using a 2:1 ratio of currents for selecting and disturbing pulses. The performance of our present production under these conditions is summarized in Figure 1.

Since these cores have been reduced in cylindrical height to about 0.022" to provide output voltages more comparable to commercially available cores, one might not see at once that the cores represent an improvement over commercial cores. While offering an adequate output signal voltage, these cores also exhibit excellent discriminating signal ratios between the dV1 peak voltage and the dVz at strobing time. In addition, the decreased half-selected output signals of the smaller cores offers a considerably reduced back voltage on the driving circuits, permitting larger matrices. In combination with the above advantages, the switching time of the cores also has been shortened by about 0.15 microsecond at 820 ma. driving current, to a practical operating value of 0.98 microsecond.

In order to compare the properties of the current core production here with commercial cores, the data on our cores have been normalized by preparing some in a cylindrical height of 0.025", the size commercially available. Performance data for these cores are compared in Figure 2 with data taken from published advertising literature of the General Ceramics Corporation.

Testing and Yields

The current IBM core specifications used to purchase cores for the FSQ-7 machines stipulate as principal performance requirements that the cores intended for use at 820 ma. driving current and 2:1 selection ratio shall each pass tests for

(1) 75mv. minimum signal for uV1 voltage at a current drive of 740 ma. and a strobing time of 0.55 microsecond.
(2) 45mv maximum signal for the peak dVz voltage when examined with disturbing pulses of 470 ma. (2:1.15 selection ratio).

The cores must, therefore, qualify under test conditions more severe than the subsequent matrix operation (2:1 selection ratio).

Because of low values of the dVz signals from cores made here (this might be restated to say because of the high squareness ratio ($R_{s,max}$ = 0.865) over the 740 ma. to 940 ma. range of the above qualification tests) it has been possible to select or test cores for our use on an even more stringent basis. For our own use, cores are qualified only if they meet a minimum output signal of 80mv for the uV1 voltage and are rejected if the dVz signal rises above 28 or 29mv.

On this restricted test basis, batch yields are consistently 95% or better. A 99% yield is not unusual. Occasional batches fail, but when they do, they fail miserably (yields of 25%), and in each case the

cause of failure has been traced to faulty equipment or human error. The manufacturing process is now apparently a stabilized and reliable method and will consistently produce high quality cores if permitted to do so by equipment and operators.

Production Facilities

Combining the interest of this laboratory in maintaining an emergency source of supply position for the FSQ-7 machines with our production for local advance development work, facilities for production at a maximum rate of 250,000 cores per week will soon be available. Currently, the maximum rate is approximately 120,000 per week. The increased production will be achieved simply, through better furnace loading techniques and more adequate core pressing facilities, capable of pressing cores much more rapidly than our present equipment. Core testing facilities can handle, approximately, the current output of cores in normal working hours. Much could be gained in an emergency by operating this automatic testing equipment on a broader schedule.

Further Work

Because of the emphasis on memory access time for the Lincoln Laboratory's interests, continued effort will be made to reduce further the switching time of the cores without sacrificing driving currents or other factors. From the examination of Figure 1, one can realize that the current core production is probably providing an unnecessarily large operating margin at the high driving current ranges. It seems obvious, therefore, that the entire set of curves may be shifted slightly to the left. Such a procedure should further decrease the switching time at 820 ma. operating current by about 0.1 microsecond. Likewise output voltage for the uV1 would be increased substantially (possibly 25mv.) which could be used as such or used to decrease again the core height and gain further on the advantages which would accrue. Less obvious improvements are likely by tampering with the chemical composition and processing techniques. Experimental work of this character will be carried on along with other experimental work to produce materials for special adaptations. Large scale production of cores resulting from this experimental work will not be available for some time, and for the present, memory core production from our pilot plant will be stabilized for the production of the cores for which typical characteristics are illustrated in Figure 1.

Signed: F. E. Vinal

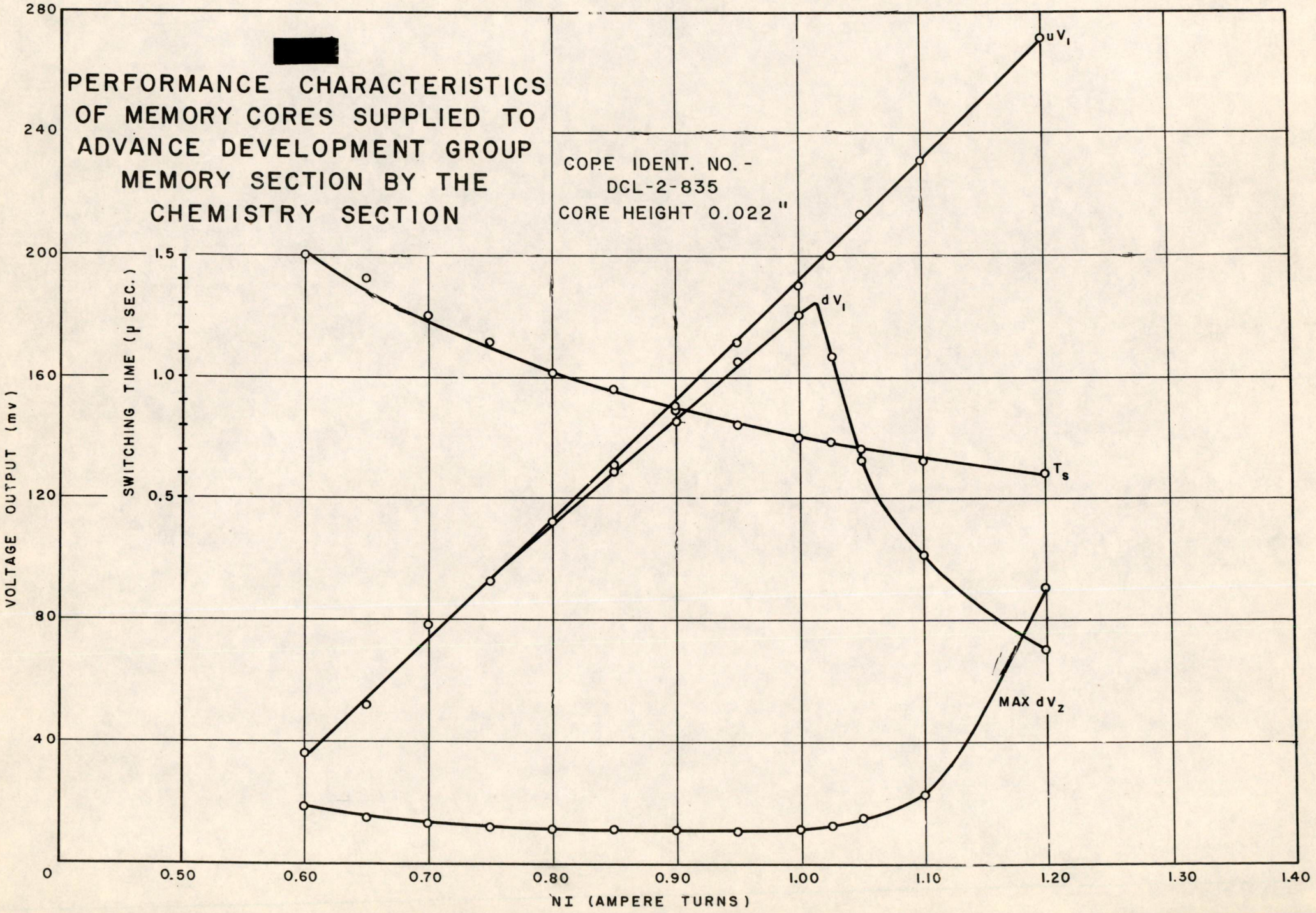
F. E. Vinal

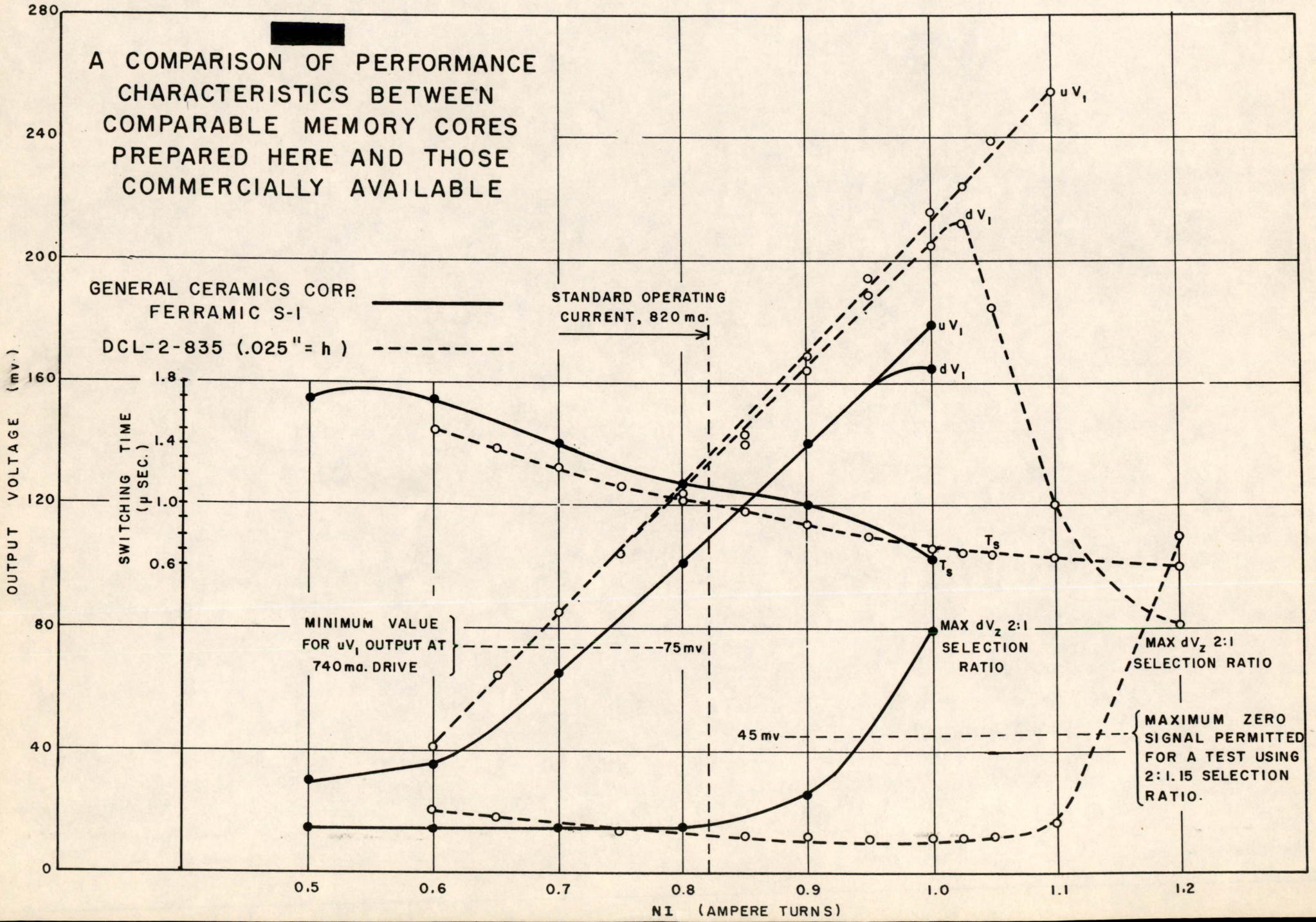
FEV:fm

Distribution: Group 63 Staff
Group Leaders and Section Chiefs, Division 6
J. W. Gibson, IBM

Drawings Attached: Figure 1 A-62423
Figure 2 A-62424

A-62423


[redacted]
PERFORMANCE CHARACTERISTICS OF MEMORY CORES SUPPLIED TO ADVANCE DEVELOPMENT GROUP MEMORY SECTION BY THE CHEMISTRY SECTION
COPE IDENT. NO. - DCL-2-835
CORE HEIGHT 0.022"
uV1
dV1
Ts
MAX dVz
SWITCHING TIME (μ SEC.)
VOLTAGE OUTPUT (mv)
NI (AMPERE TURNS)
280
240
200
160
120
80
40
0
1.5
1.0
0.5
0.50
0.60
0.70
0.80
0.90
1.00
1.10
1.20
1.30
1.40


A COMPARISON OF PERFORMANCE CHARACTERISTICS BETWEEN COMPARABLE MEMORY CORES PREPARED HERE AND THOSE COMMERCIALLY AVAILABLE
GENERAL CERAMICS CORP. FERRAMIC S-1
DCL-2-835 (.025" = h)
STANDARD OPERATING CURRENT, 820 ma.
OUTPUT VOLTAGE (mv.)
SWITCHING TIME (μ SEC.)
uV1
dV1
Ts
MINIMUM VALUE FOR uV1 OUTPUT AT 740 ma. DRIVE
75mv
MAX dVz 2:1 SELECTION RATIO
45mv
MAXIMUM ZERO SIGNAL PERMITTED FOR A TEST USING 2:1.15 SELECTION RATIO.
NI (AMPERE TURNS)

Copy # 26

DRAFT

DRAFT 4-15-55

Memorandum 6M-3536

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: DESIGN CONSIDERATIONS FOR AN EXPERIMENTAL COMPUTER

To: R. R. Everett

From: W. A. Clark

Date:

Approved: _____

Abstract: A preliminary logical design for a real-time-control computer, with system capabilities approximating AN/FSQ-7, eliminates buffer storage and centralizes control of input-output transfers. High-speed transistor circuits and a random-access storage system of 2.5 million to 5 million bits make possible significant simplifications in system logical design. Breakpoint operation similar to that of DYSEAC, but using many program counters, promises great flexibility in the handling of terminal equipment. This memorandum deals primarily with the features of the multiple-program-counter system.

Introduction

The design proposed here (TX-1) is the first member of a family of parallel, single-address computers for real-time control now under study in Group 63. This family has the following principal characteristics:

1.) Surface-barrier transistor circuitry
2.) Large core memory (2.5-5 million bits)
3.) Multiple program counter logic.

The TX-1 has been designed with the system capabilities of the AN/FSQ-7 in mind but with no attempt to meet the detailed specifications of the SAGE system. It is essentially a "bufferless" machine as opposed to the FSQ-7 which provides buffer drums between the central machine and various terminal devices. In the TX-1, information passes more directly into and out of the memory unit of the central computer. All transfers of information are programmed by means of minor sequences of read-in or read-out operations which are executed on a "demand" basis during interruptions of the major program or of one another. This method of getting information in and out of the central computer, which requires the use of an additional program counter for each minor sequence, is the distinctive feature in which the system logical design of the TX-1

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

differs significantly from that of the FSQ-7.

This note deals primarily with the features of multiple program counter operation of the TX-1 in a control application with roughly the input-output requirements of the SAGE system. Where possible, correspondence with equivalent features of the FSQ-7 will be pointed out. However, not enough is known yet about the details of the transistor circuit "building blocks" to permit the drawing of block diagrams of the TX-1 in anything approaching final form. It is hoped that this summarization of some of the early thinking of the Group 63 Logical Design Section will serve to stimulate further thought and comment.

Influence of Large Core Memory on Design

The fact that large core-arrays (256 x 256 x 36) are now feasible for use in the central memory of the computer makes possible two major simplifications in a system of FSQ-7 proportions which will be realized in the TX-1:

1.) Consolidation of Auxiliary Storage

In the FSQ-7, the storage of the program and associated tables is distributed over 8 physically-independent yet logically-equivalent drums. Consequently an obvious logical simplification results from the lumping together of this storage into fewer large core-arrays. One 256 x 256 array is the equivalent of about 5 or 6 drums.

2.) Elimination of Separate Intermediate Buffer Storage

In the FSQ-7, one drum serves as a buffer of input information; another 3 drums, output information. Of these output buffer drums, 2 hold information for the display system and enable it to run at a higher rate by redisplaying old information several times between changes of data. All of this buffer storage can be eliminated if provision is made to address the central memory on an "in-out break" basis. In the case of the display system, the central memory must give up additional cycles for the redisplay of old information, but this requirement is not a limiting one at FSQ-7 rates.

The total storage capacity of the FSQ-7 including drums and its internal core memory is about 4.5 million bits, almost entirely in 32 bit words. This is roughly the equivalent of two 256 x 256 x 36 core arrays.

The TX-1 will be so designed that it can operate 2 independent memory units concurrently, getting an instruction from one unit while the other unit is referring to the operand of the previous instruction.

Thus, by arranging to store the program in one unit and the operating data in the other, a significant increase in speed of operation is possible. This increase has been estimated to be about 70 percent. The design will, of course, also permit the program and its operanda to be stored in the same memory unit with a corresponding reduction in operating speed in this mode.

The TX-1 System Design

The "in-out break" mentioned above is somewhat like that of the FSQ-7. However, because of the absence of large-scale buffering, all terminal devices with critical timing requirements (for example, phone line receivers) must have a guarantee of access within certain time limits. The fact that all devices time-share the same memory unit will mean that one device will, in general, have to tolerate interruptions by other devices with higher priority. This fact greatly devalues "block transfers" of information and furthermore makes it necessary for each terminal device to "remember" what it was doing at the time of the interruption. In the TX-1, this function of storage of memory addresses during interruptions is handled partly by the use of index registers and partly by means of additional program counters in a manner later described.

Figure 1 is a simplified block diagram of the TX-1 showing only the principal information paths. The various terminal devices, labeled T_1, T_2, etc., are shown as being connected to the central computer by busses for simplicity. Each device includes enough storage to enable it to function between central memory accesses. The Memory consists of one or more 256 x 256 arrays, depending on the intended application of the computer and also includes a small toggle switch test memory. The Arithmetic Element will be assumed to be essentially like that of the FSQ-7 in logical structure for the purposes of this note.

The Terminal Selector is, as the name implies, a device for selecting one and only one terminal device and connecting it up to the central machine. This selection is made at designated interruption points in the program sequences. Some sort of priority system is implied such that terminal devices with critical timing requirements can be handled along with devices of less urgency. A "demand chain" similar to those appearing in the terminal system of the FSQ-7 satisfies the general priority requirement. In addition, an "in-out switch" is required to permit the central machine to select terminal devices directly, for example, to switch "off" units into the demand chain.

The Program Element consists of a set of program counters (one for each terminal device), a set of index registers, and an adder (see Fig. 2). To run a system of the size of SAGE, about 100 index registers and somewhat fewer program counters might be required. These might all be consolidated into one 256 register core-array with an access time of about 1-microsecond and a cycle time of half that of the central memory. Such a consolidation would have the advantage that the proportion of program counters to index registers is not fixed.

The primary function of the Program Element is to supply addresses to the Memory according to the requirements of the stored program. These addresses come from either a program counter or the adder register. The particular program counter in operation during any given machine cycle depends on which terminal device has been selected by the Terminal Selector, and the address it contains is indexed by one each time it is used, in the usual way. The index register in use during a given cycle depends, as in FSQ-7, on an index register number stored with the instruction being executed. The contents of the designated index register are added into an adder with the address-half of the instruction being executed, and the sum is then sent to Memory as the address of the operand designated by the instruction. Except for the fact that the TX-1 has several program counters and must select one of them at a time for any given cycle, the Program Element operates in essentially the same way as in FSQ-7.

To summarize: the word structure of a typical instruction, add, which requires its operand base-address, K, to be modified by the contents of index register j is

j add K

If index register j contains the number J, then the address of the operand (addend) is J + K.

We can now focus attention on the multiple program counter logic:

Multi-Sequence Operation

The TX-1 is a multi-sequence computer employing a set of program counters, each one of which marks the progress in its own sequence of instructions and is brought into operation at the request of an external device with which it is associated. In this respect, the TX-1 design is an extension of the 2-sequence DYSEAC of the National Bureau of Standards.

The program operating in the TX-1 can be thought of as consisting of a major program sequence and several essentially independent minor sequences. The major sequence is the large real-time control program corresponding to the single program of a one-sequence computer like Whirlwind. Each minor sequence is devoted primarily to transferring information between the computer and a corresponding terminal device.

These sequences are interleaved in time in an arbitrary fashion. The timing will depend largely on the requirements of the terminal devices themselves. However, interruptions in any sequence can occur only at points designated by the sequence itself. These

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See 6M-3144 "The Multi-Sequence Program Concept" for a general description of multiple program counter operation.

breakpoints are marked by the presence of a "one" in a breakpoint bit stored with each instruction. A sequence may thus retain control of the computer by preventing interruption for as long as necessary to carry out required transfers, communicate with other sequences, etc. At each breakpoint the Terminal Selector selects the terminal device with the highest priority and connects it to the computer for the next computer cycle. Of course, the peak rate load of the entire terminal system will determine the maximum intervals between breakpoints in the sequences. The average input and output rates will limit the complexity and length of the sequences. The overall average number of transfers might require 10 to 15 percent of computer time at anticipated FSQ-7 rates.

The illustrated instruction must then include an indication of the status of its breakpoint bit:

*j add K

where the asterisk will be taken to mean that interruption is not permissible and that the next instruction to be executed will come from this same sequence.

Example of an In-Out Word Transfer

To illustrate a typical machine cycle, consider the example shown in Fig. 3. Terminal device #2 requires its next word from Memory and has been selected by the Terminal Selector as the subscriber with the highest priority.

The cycle begins (a) with the selection of the program counter to be used during the cycle, in this case PC#2. The address 101, subsequently indexed to 102, designates the next instruction to be executed in sequence number 2 and is sent to Memory as shown in (b). This instruction, 13 rdo 4000, indicates that index register 13 is to be used to modify the address of the operand, and the address-base 4000 and index register number are transferred to the Program Element (c). Inasmuch as index register 13 contains the number 7, the address of the operand becomes 4007 and this register is selected in Memory (d). The Control decodes the instruction rdo (read out) and transfers the contents of register 4007, which happens to be 666, to the in-out bus to which T_2 is connected (e), and the operation is complete. No asterisk appears with the instruction in this example, and hence a breakpoint is indicated. Thus the next instruction in sequence 2, stored in register 102, will not be executed until T_2 next requests, and is granted, control of the computer. Eventually the sequence folds back on itself after a branch instruction which resets program counter #2. Also, at some point in the sequence index register 13 is indexed and sensed for overflow, and reset as required.

Notice that reset values used in such a minor sequence may be supplied by the major sequence. This permits the major sequence, for example, to apportion internal storage among several input devices according to need. Also, one sequence can determine the progress of

another sequence by examining its program counter.

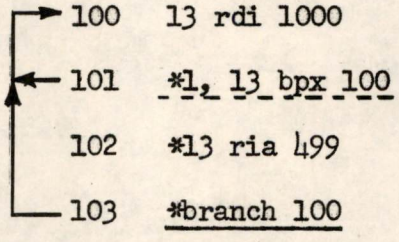
Examples of Minor Sequences

The following examples will help to illustrate some of the ways in which minor sequences might be used. First, it is necessary to describe the functions of the orders appearing in the examples: Most of these are found in the FSQ-7 order code. (K is the address of a register in the central memory.)

cad K: Clear accumulator and add in contents of K
aor K: Add one to contents of K (performed in AE)
fst K: Store Acc contents in K
branch K: Reset selected program counter to value K
k rdx K: Read contents of index reg. k into reg. K
k ria K: Reset index reg. k to the value K
j, k bpx K: If index reg. k is positive, reduce it by amount j and branch to K. If index reg. negative, ignore instruction.
bsn K: Branch to K if indicator in selected terminal device is set.
rdi K: Read word from selected terminal device to reg. K
rdo K: Read word from reg. K to selected terminal device

Except for the three orders which make special use of index registers, any of the above may be prefixed by an index register number.

Example 1: Input device assigned registers 1000 to 1499 for storing input data. Recycles if this assigned zone exceeded. Uses index register 13; program sequence stored in regs. 100-103.



The program counter for this sequence starts at 101 when request for machine cycle is granted. If assigned zone is not exceeded, index reg. 13 is counted down by 1 and sequence branches to 100, reads in word, and gives up control (no asterisk on instruction in 100 indicates breakpoint). Program counter ends up at 101. If zone was exceeded, index reg. 13 is reset to 499 before word is read in.

This example represents a minimum program-storage sequence. Note that each read-in requires the execution of 2 instructions (except when the zone is exceeded at which time 4 instructions are momentarily required). By expanding the sequence, the number of instructions per read-in can be reduced to nearly 1 as the following example shows:

Example 1a: (Same requirements as Example 1.)

```
100   13 rdi 1003
101   13 rdi 1002
102   13 rdi 1001
103   13 rdi 1000
104   *4, 13 bpx 100
105   *13 ria 496
106   *branch 100
```

Except for end-of-zone reset, this sequence uses 1.25 instructions per read-in. The feature of expanding sequences in this manner can, of course, generally be employed to reduce instruction time.

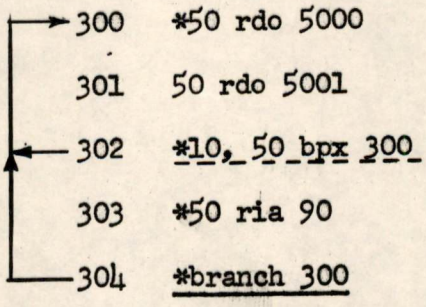
Note that if several input devices use the same program counter in the sequence of example 1, then they all load data indiscriminately into the one zone 1000-1499. A separate sequence for each results in separate zones for each device.

Example 2: Time of arrival to nearest t-seconds of input data of example 1 is required.

```
200   13 rdx 1500
201   13 rdx 1501
203   13 rdx 1502
204   13 rdx 1503
205   *branch 200
```

Terminal device consists of timer which requests machine cycle every t-seconds. Current intra-zone location read into 1500 on first cycle. t-seconds later, current location read into 1501, etc. These mark boundaries of data in the zone which are within t-seconds of one another. In this case, major sequence uses this information at least once every 4t-seconds.

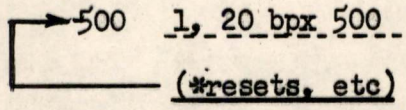
Example 3: Continuous, cyclic read-out (for example, to a display system) of every 10th pair of registers in zone 5000 thru 5091. Index reg. #50 used.



Example 4: Dynamic stop (imposed, for instance, by major sequence to shut off input device momentarily).

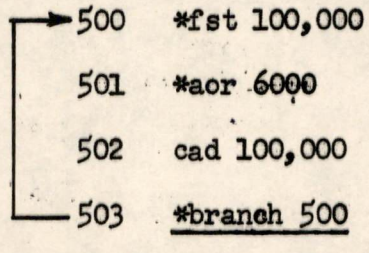
```
400   branch 400
```

Example 5: Clock time to within t-seconds required in index register 20:



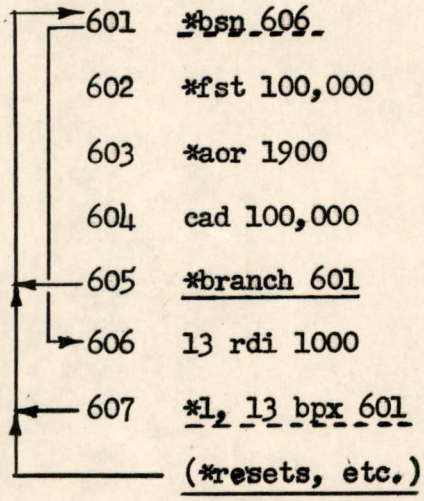
Terminal device consists of timer requesting cycle every t-seconds.

Example 5a: Clock time to appear in register 6000.



Same terminal device as in previous example. Sequence starts in 503 with branch. Next instruction empties accumulator for use by this sequence. Count is made in register 6000, accumulator restored on 502, and sequence gives up control until next timing event.

Example 6: Input device with parity on input word. Word is to be read in only if parity indicator is set. Count of failures to read in to appear in reg. 1900.



Program counter for this sequence starts from 607. If zone not exceeded, executes sense instruction in 601: Branches to 606 if selected parity indicator set, then reads in and gives up control. If indicator not set, increases count in 1900, restores accumulator and gives up control at 605.

These examples illustrate the flexibility of the multiple sequence technique and should suggest other applications not mentioned here. An important application which needs study is the programmed generation of displays. There is some hope that a display system like that of the FSQ-7 might be simplified to a considerable extent by special display sequences operating at different rates.

This flexibility in handling terminal equipment is an extremely important feature. The ultimate application of the machine in a control system may be largely unknown and yet will not appreciably affect the design of the central computer. By stressing the construction of computer programs rather than terminal equipment a considerable gain in system flexibility is achieved.

Signed Wesley A. Clark, Jr.
Wesley A. Clark, Jr.

WAC/md/jg

Drawings Attached:
Figure 1 - SA-62428
Figure 2 - SA-62414
Figure 3 - SA-62458

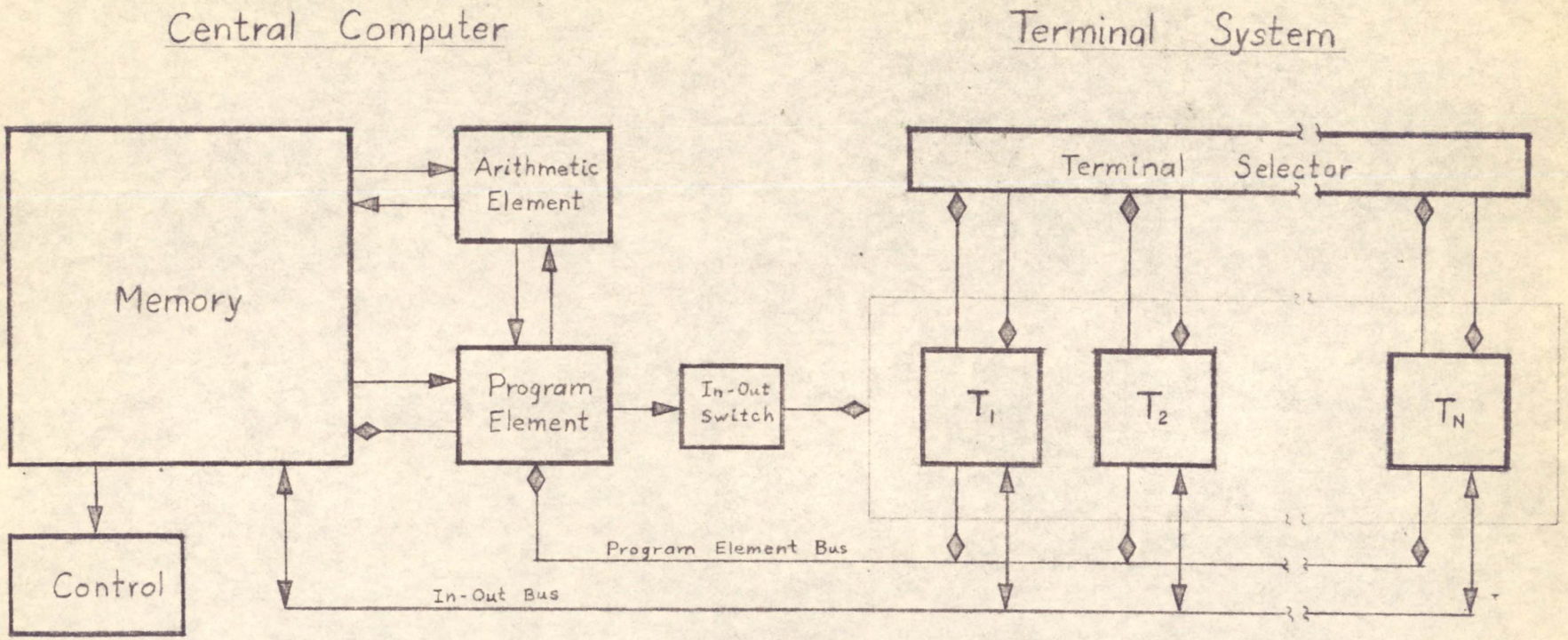


Figure 1

Simplified System Block Diagram of the TX-1

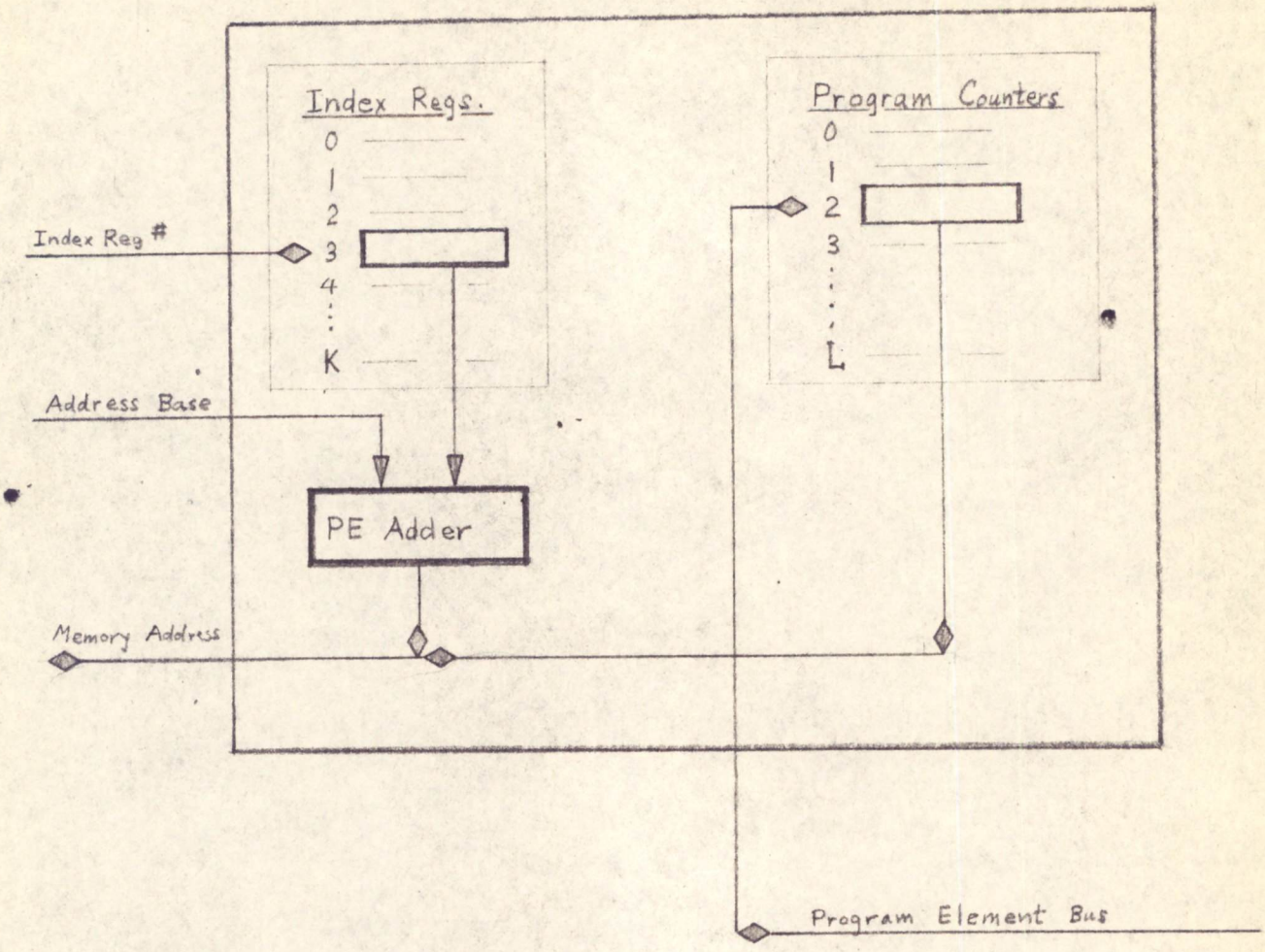


Figure 2

Program Element

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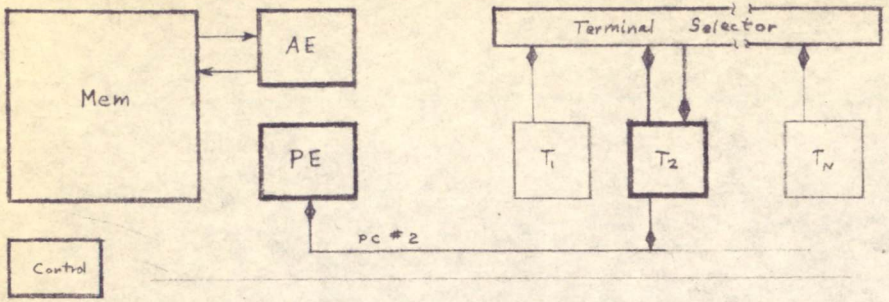
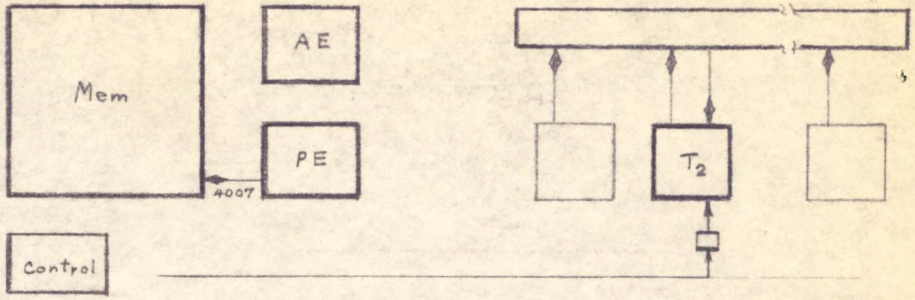
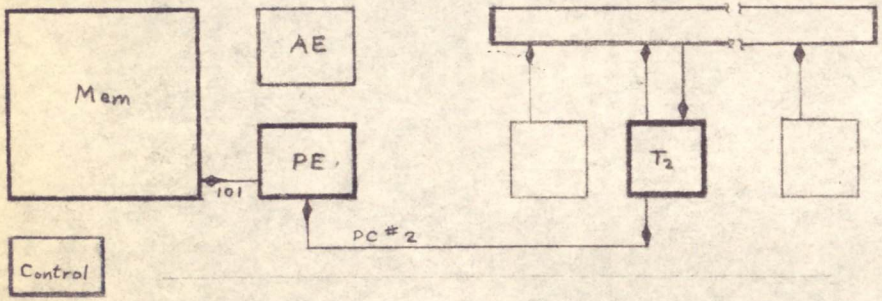


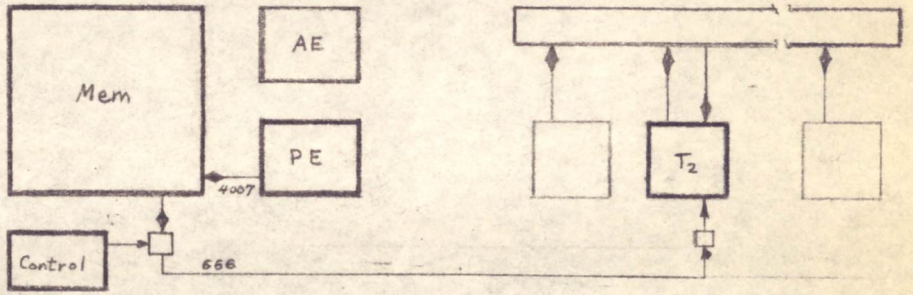
(a) Terminal Device #2 Selected



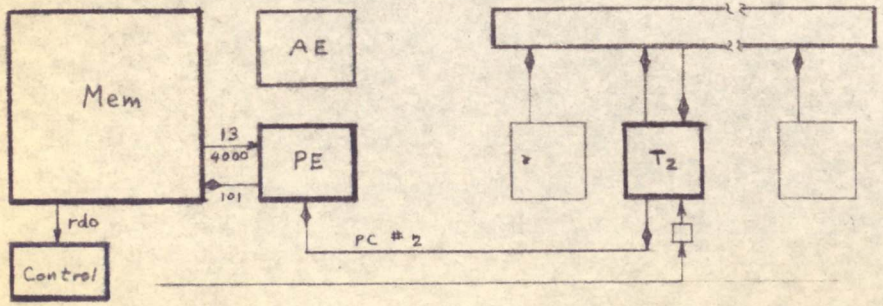
(d) PE Adder Returns Operand Address 4007



(b) Next Instruction Location to Memory



(e) Contents of 4007 Read Out to T_2



(c) 13 rdo 4000 Read from Memory

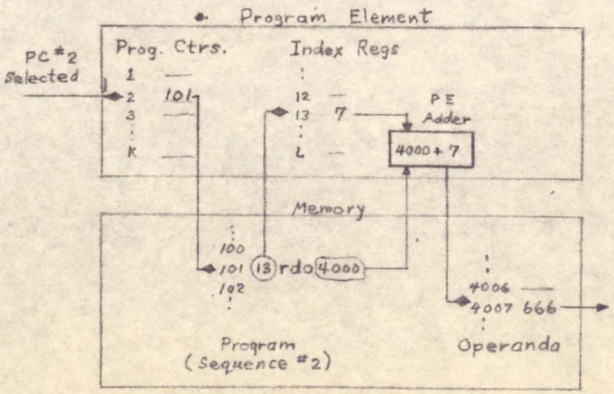


Figure 3

Example of In-Out Word Transfer

H. Olsen

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TYPICAL SBT STATIC CHARACTERISTICS

To: Group 63 Staff

From: Edmund U. Cohler

Date: May 31, 1955

Approved: Torben Meisling
Torben Meisling

Abstract: Measurements on surface barrier transistors show that certain simple approximations may be made to represent its static characteristics. The input in saturation is a 125Ω resistor in series with a 0.30 volt battery. In the active region it is a 0.13 volt battery in series with a much higher resistance (300- 800Ω). The saturation beta at 5 milliamperes of collector current varies roughly from 7 to 25 and changes about 7.5 percent/ma (more current giving lower β) in the range 2.5 ma $< I_c <$ 10 ma. The I_{coe} or grounded-emitter collector reverse current is roughly equal to $I_{co}/(1-\alpha)$ and runs from 5-25 μ amperes. Grounded emitter characteristics of some typical transistors are included.

Grounded Emitter Input Characteristics

The photographs of Fig. 1b show the superposed input and transfer characteristics for a batch of 19 surface barrier transistors in the circuit of Fig. 1a. The inputs characteristic in the saturation region can be approximated by a battery and resistor. In the batch shown the battery (e_b) does not vary noticeably from 0.30v while the resistance varies from 95 to 165 ohms. Fig. 2 is the input and transfer characteristic of a typical (but not average) surface barrier transistor. The active region of operation can be defined by the straight line portion of the transfer characteristic, (see Fig. 2). In the active region, the input characteristic cannot be approximated by the same battery and resistor as were used in the saturated case. The "active" value of the resistor will vary considerably from transistor to transistor depending on the beta of the transistor, but the battery is relatively constant at about 0.13 volts. Fig. 3 summarizes these results in straight line approximations, and an equivalent circuit.

The input characteristic will be little affected by the collector circuit. In the saturated region, the load resistance and supply fix

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

the value around which the emitter current will vary and the battery-resistor approximation is very insensitive to such variations. In the active region, the collector circuit is completely isolated from the base circuit by a back-biased diode and an equivalent current generator. Thus, the collector circuit has very little effect on the base input characteristic in either region, (see Fig. 2).

In summary, the base input characteristics are reasonably uniform from transistor to transistor, and may be accurately represented by certain piecewise linear characteristics.

Saturation Beta

In discussing the active transfer characteristics, we are mostly interested in the end points of the active region because we traverse the active region in the transient only. This end point can be described in terms of saturation beta which is roughly defined as the ratio of the saturation collector current to the base current on the verge of saturation. This definition has meaning for the surface barrier because the collector current break point between the active and saturated regions is rather sharply defined. For instance, in the transfer characteristics of Fig. 2 the base current at the break is about 0.55 milliamperes for a saturation collector current of 5.9 milliamperes thus giving a saturation beta of 10.7. Measurements of saturation beta were made on twenty surface barrier transistors and plotted as a function of normal beta in Fig. 4.

The saturation beta measurements were made by adjusting I_b until I_c reached its maximum value (V_{cc}/R_c) and then reducing I_b until I_c was 0.05 milliamperes less than its maximum value. The normal beta measurements were made by inserting 1 milliampere into the emitter and measuring the base current at $V_{cb} = 0$. There is a definite correlation between the saturated and the normal value. The saturated value is always lower than the normal value. One reason the saturation beta is lower is that beta decreases with increasing collector current. The measurement of saturation beta was taken with about three milliamperes in the collector while the measurement of the alpha was taken with about one milliampere in the collector.

To determine the variation of saturation beta with collector current, measurements of this parameter were made on ten different transistors whose normal alphas ranging from .880 to .971 (at 0 volts). The method of measurement was slightly different from that used in obtaining the data in Fig. 4. Collector current and base current were adjusted to give a V_{ce} of 0.200 volts and the beta taken at that point. The curves obtained were normalized by dividing by the value of beta obtained at a collector current of 5 milliamperes. These normalized curves for the ten transistors are shown in Fig. 5.

In addition, twenty more transistors were chosen at random, and their saturation beta measured by this new method at a current of 5 milliamperes. This value of saturation beta was plotted vs normal beta (measurement previously described) for all thirty transistors (Fig.6).

Moreover, an integrated distribution of the saturation betas of the batch was drawn up in Fig. 7. This method of determining saturation beta is not consistent at low collector currents and results in the dispersion of the beta vs collector current curves at low collector currents. From Fig. 5 we may roughly approximate the saturation beta in the range of collector currents from 2.5 milliamperes to 10 milliamperes by:

$$\beta \text{ saturation } (I_c) = \beta_{sat}(5ma) \times \left[1 - .075 \ (I_c - 5) \right]$$

Grounded-Emitter Saturation Current

The current which flows in the collector circuit of a grounded emitter stage when the base is open will be called I_{coe}. From the simple equivalent circuit of the transistor we expect this to be larger than the grounded base saturation current (I_{co}) by a factor of $1/(1-\alpha)$. Fig. 8 shows the results of measurements of I_{coe} plotted as a function of $I_{co}/(1-\alpha)$. The agreement is not perfect because of several factors. The collector resistance may vary from the grounded emitter connection to the grounded base connection (other than by a factor of $1/(1-\alpha)$). The alpha measured and used in the calculations is for a collector current of about 1 milliampere while the collector current flowing in the I_{co} and I_{coe} measurements is of the order of a few microamperes.

Grounded-Emitter Collector Characteristics

Certain other pertinent parameters, such as r_{cr} and the resistance of the collector-emitter circuit, can be obtained from the grounded-emitter collector characteristics. Typical curves are given in Figs. 10 and 11.

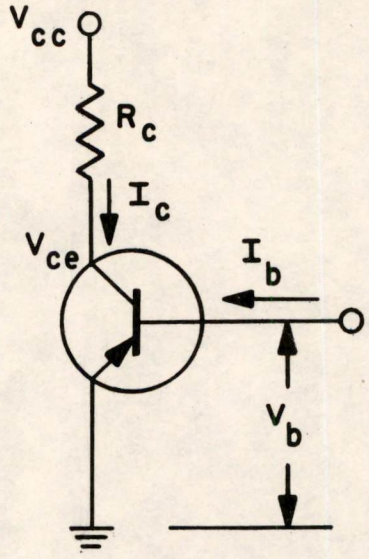
Edmund U. Cohler

Edmund U. Cohler

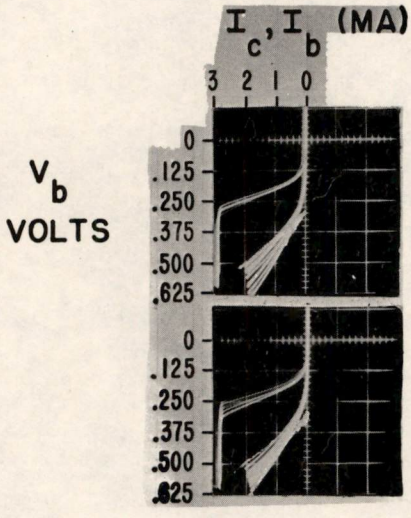
EUC/md

Distribution: Group 63 Staff

Fig. 1 - A62878
2 - A62879
3 - A62880
4 - A62881
5 - A62882
6 - A62853
7 - A62854
8 - A62892
9 - A61465-1
10 - B48672G



(a)



TRANSISTOR NUMBERS:
114-117, 119-121, 124, 126

TRANSISTOR NUMBERS:
104 - 113

(b)

FIG 1

GROUNDED EMITTER STAGE SCHEMATIC & CHARACTERISTICS

A-62878

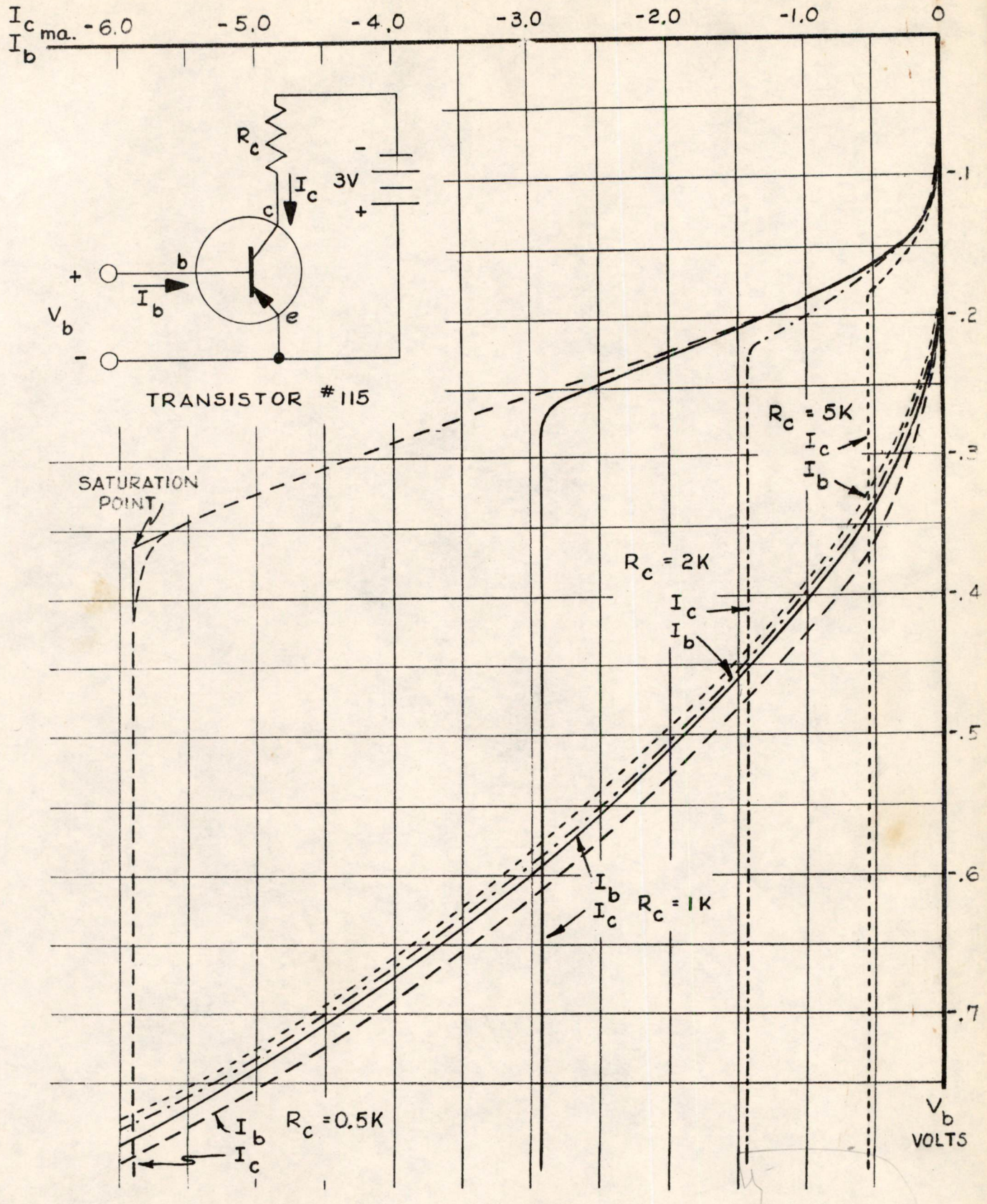


FIG. 2

GROUNDED EMITTER STAGE INPUT & TRANSFER CHARACTERISTICS

A-62879

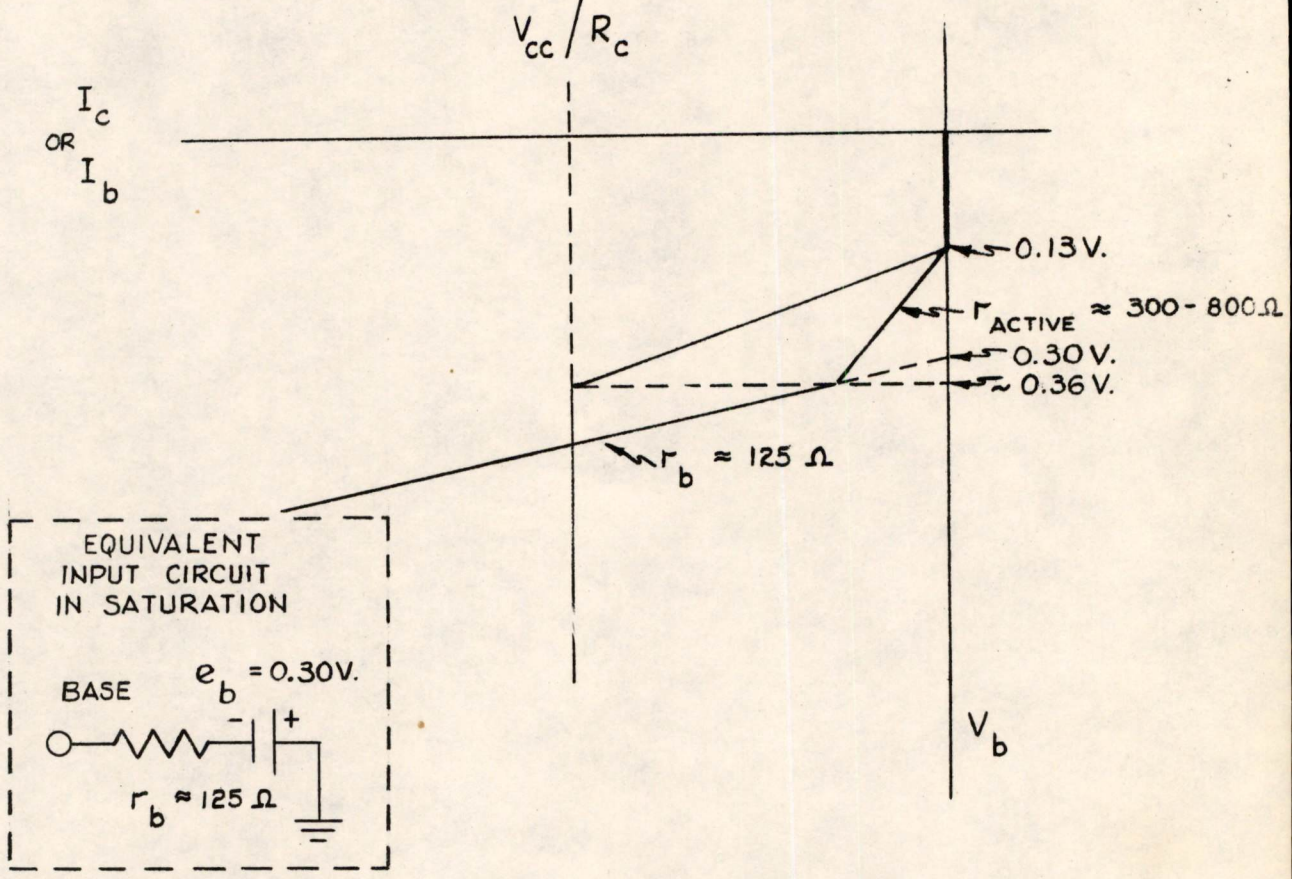
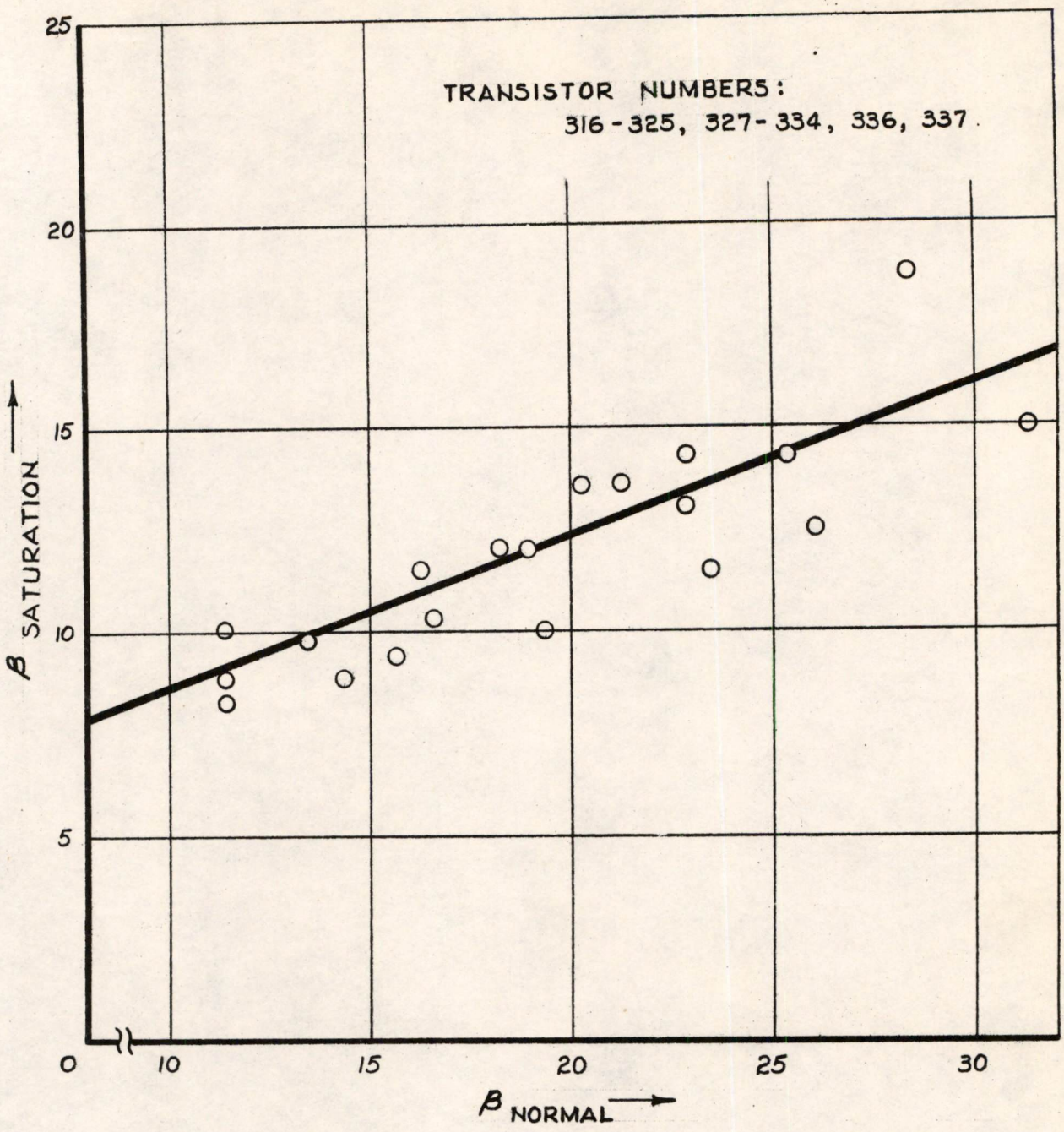


FIG. 3

STRAIGHT LINE APPROXIMATION OF SBT CHARACTERISTICS



DATE : 3-7-55

FIG. 4

SATURATION β vs. NORMAL β IN SBT'S

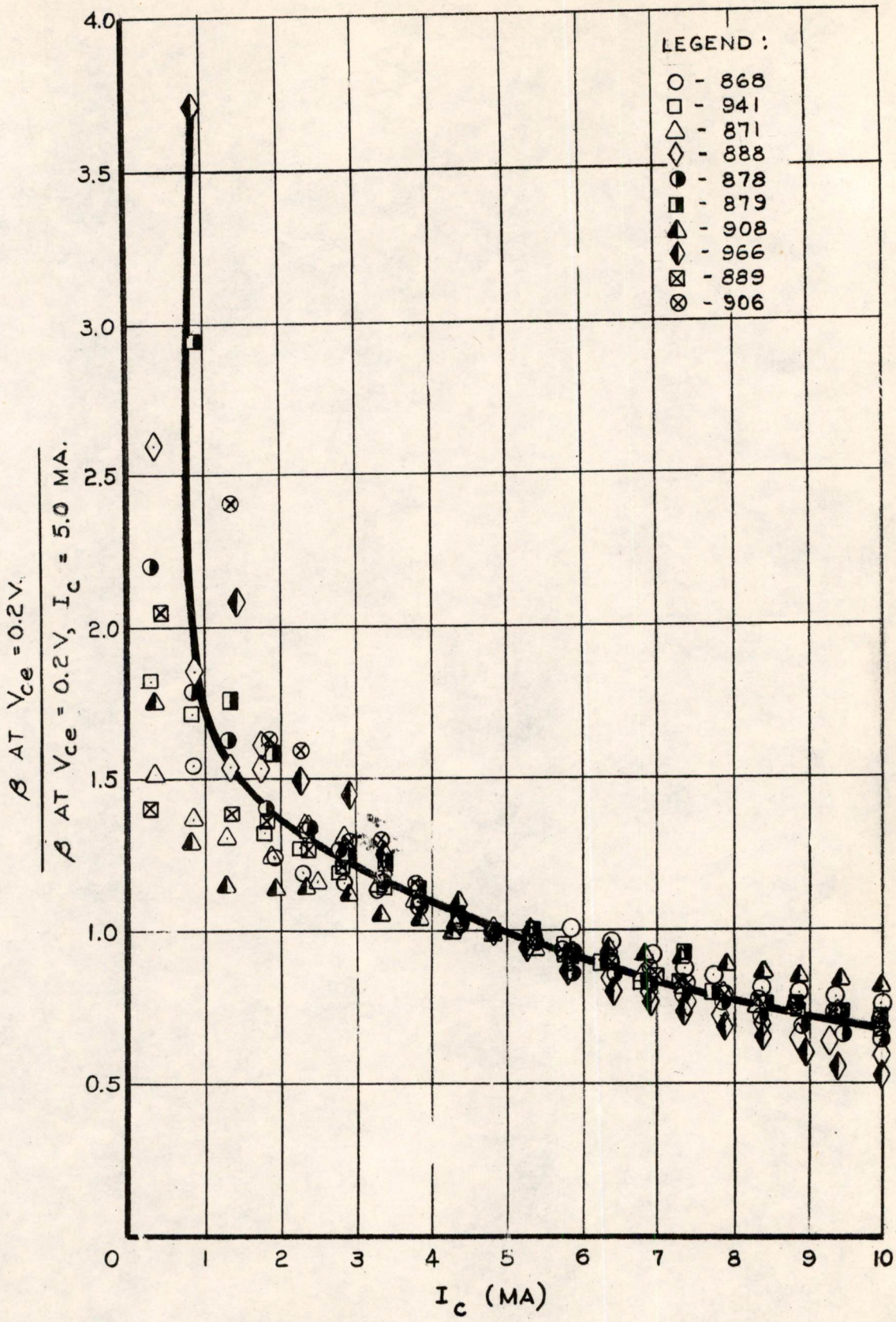


FIG. 5

SATURATION β vs. COLLECTOR CURRENT

A-62882

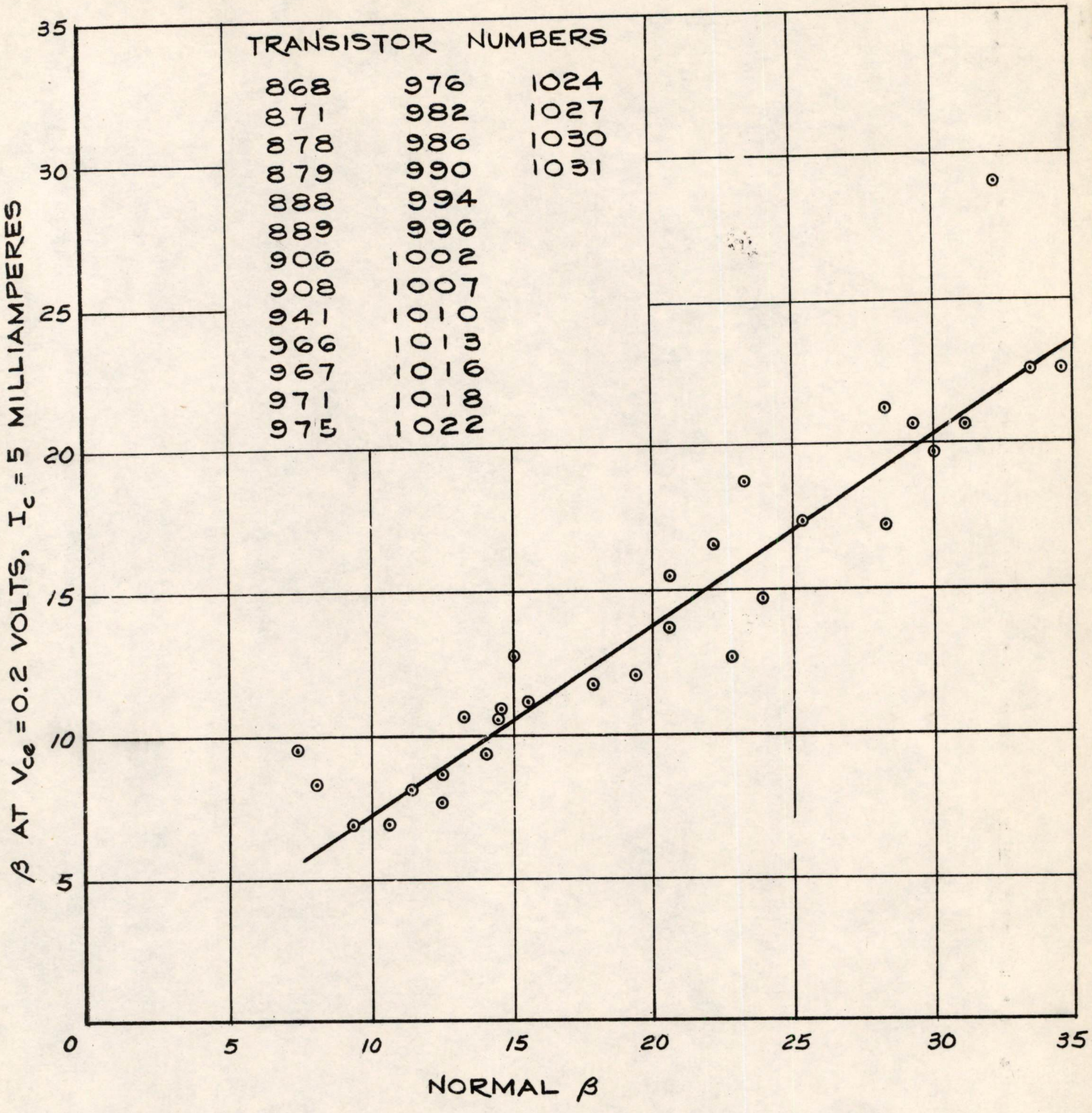


FIG. 6

SATURATION β vs. NORMAL β IN 30 SBT's

DATE: 5·15·55

A-62853

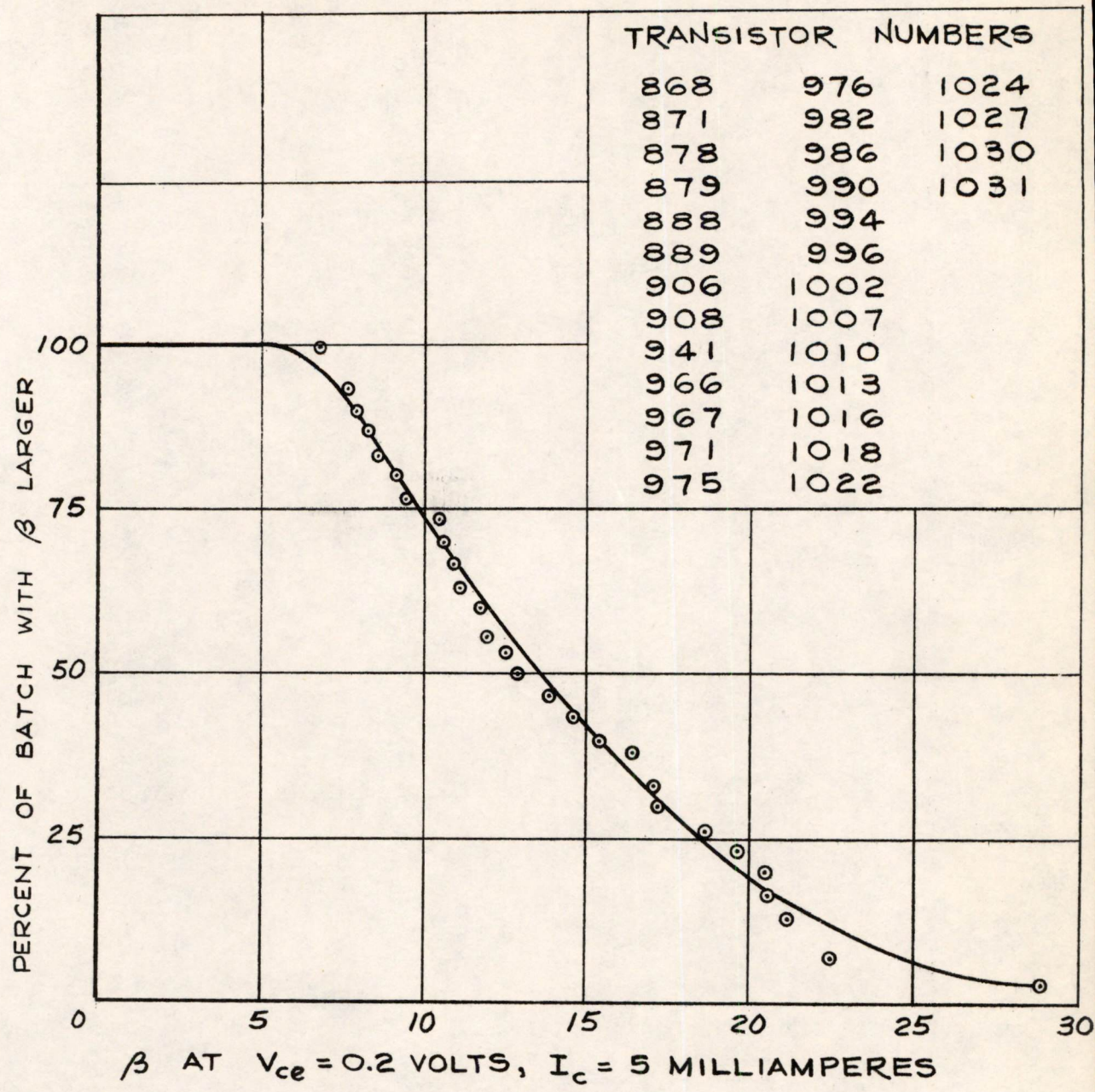


FIG. 7

DISTRIBUTION OF SATURATION β IN A BATCH OF 30 SBT's

DATE: 5·17·55

A-62854

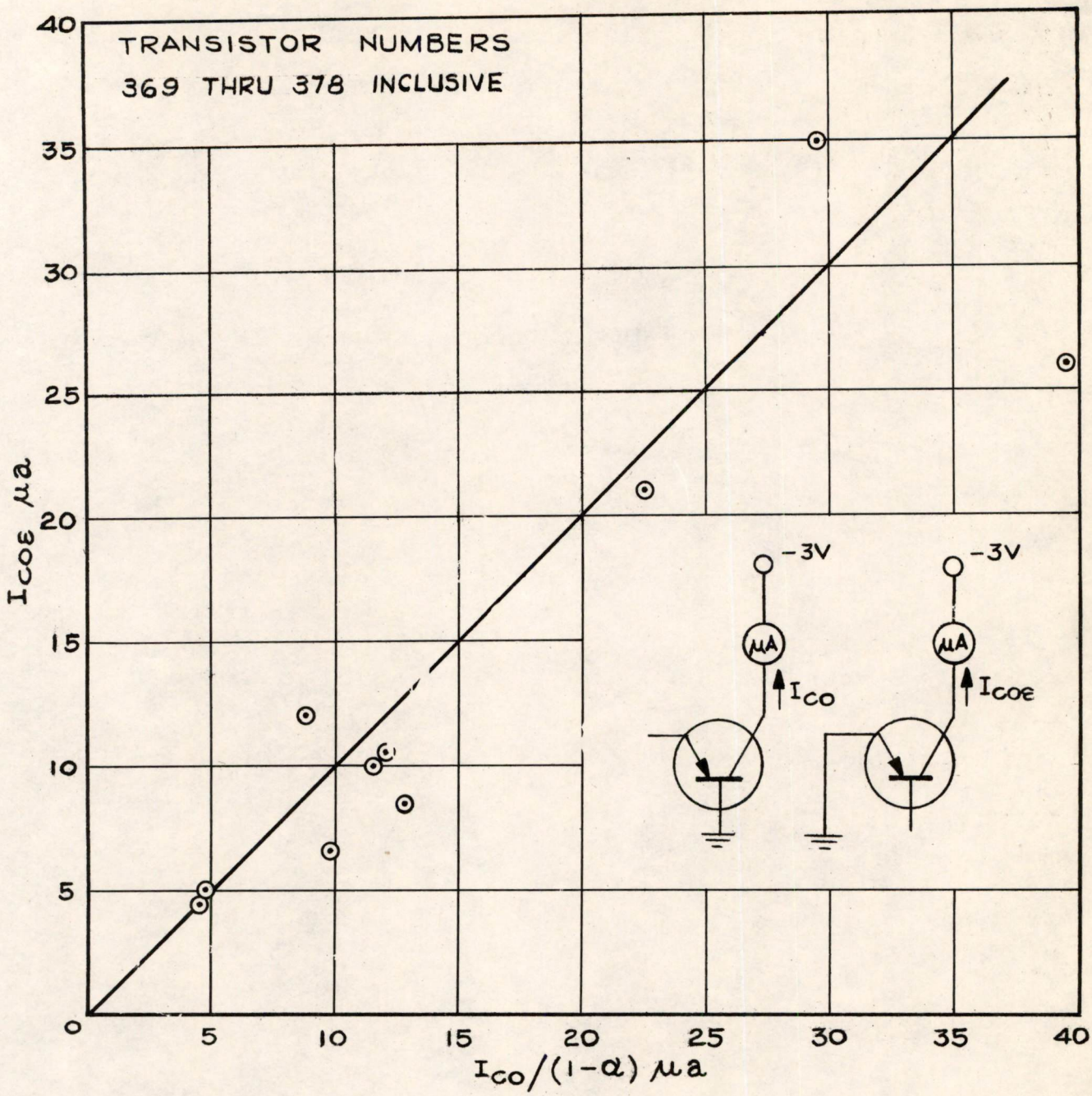


FIG. 8

GROUNDED – EMITTER SATURATION CURRENT VS $I_{CO}/(1-\alpha)$ IN SBT'S

A-62892

TRANSISTOR #48 BY M. PETERSEN - DEC. 1954

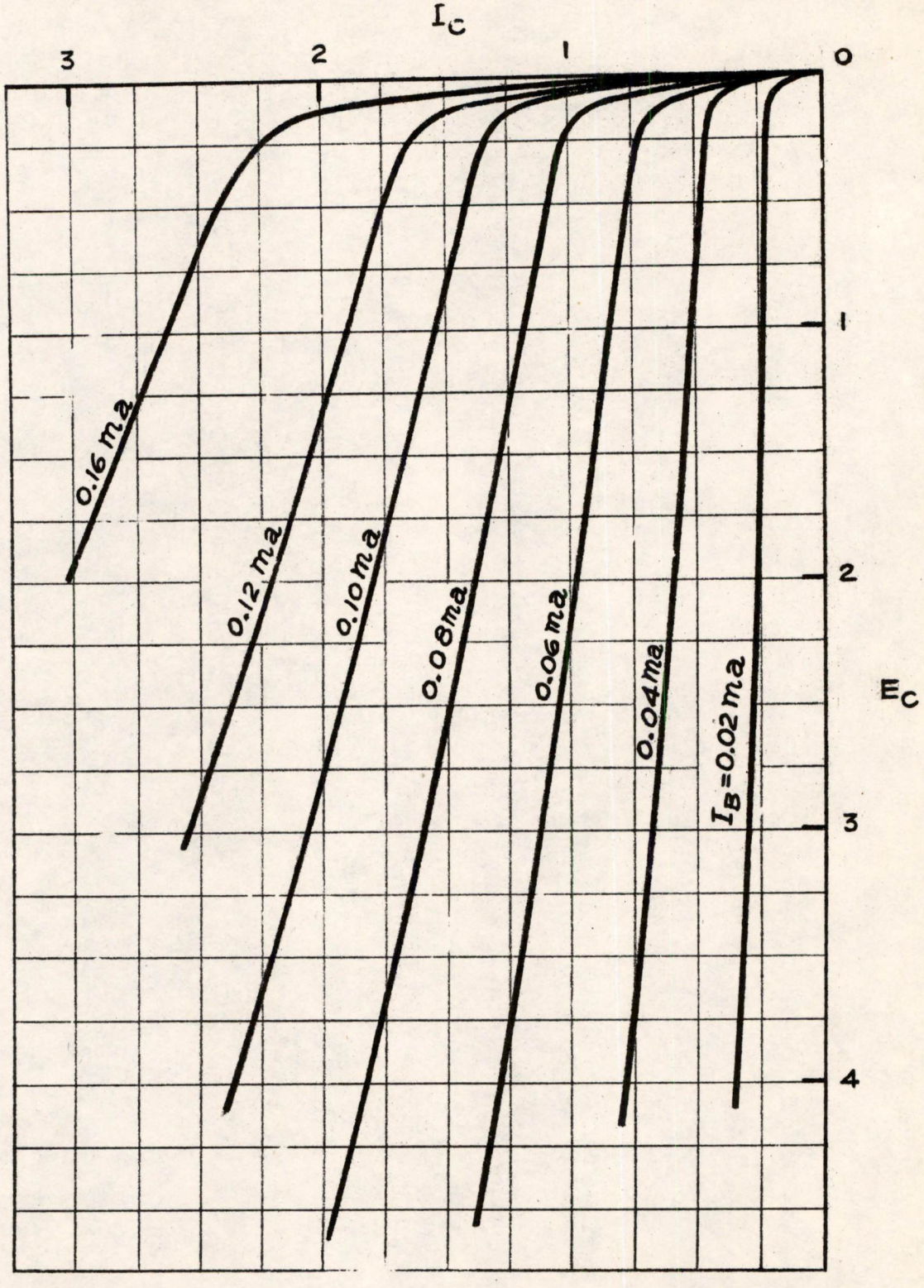


FIG. 9

TYPICAL SBT CHARACTERISTICS
GROUNDED EMITTER
I_C vs E_C

B-48672-G

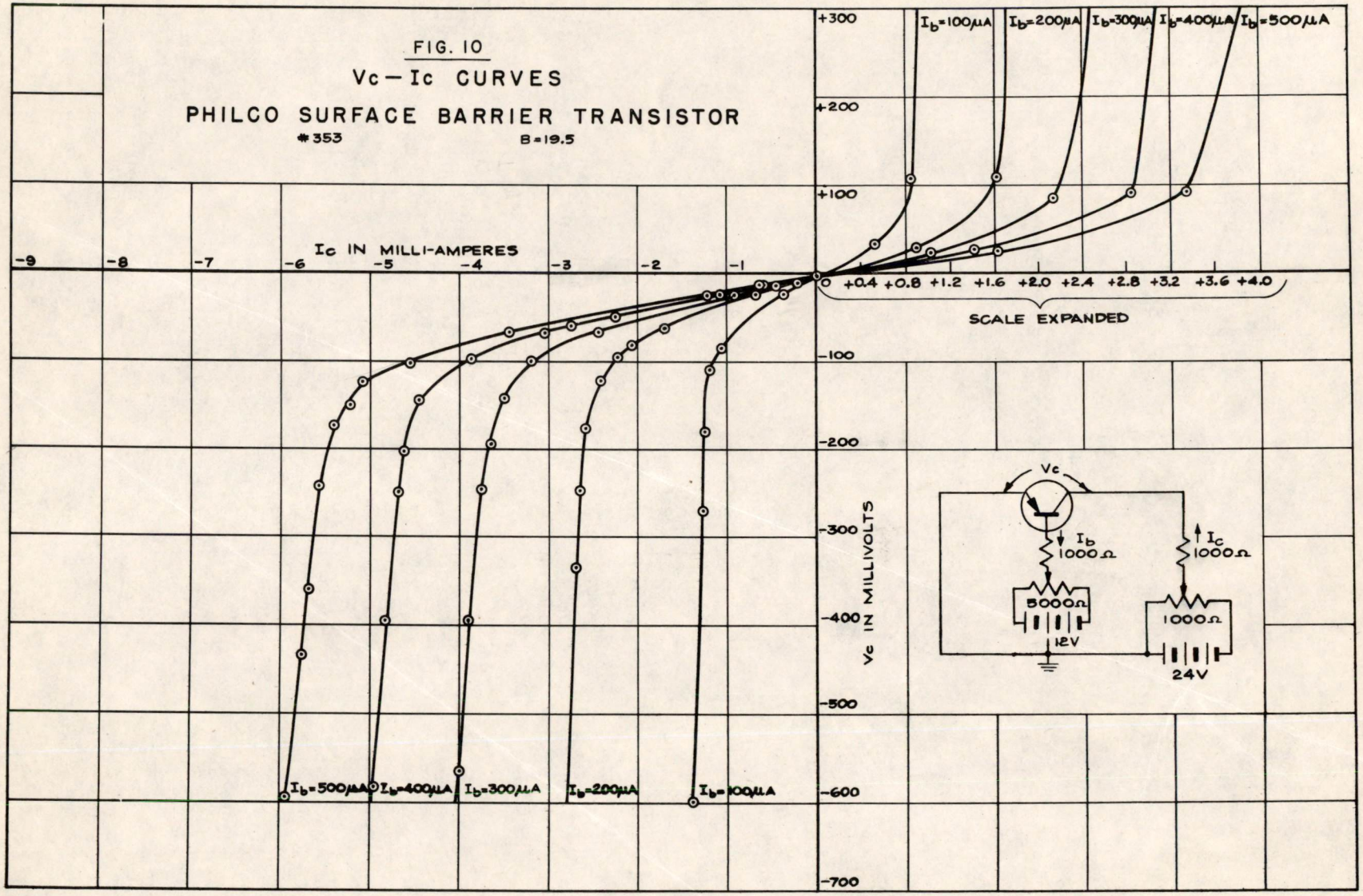


FIG. 10
Vc — Ic CURVES
PHILCO SURFACE BARRIER TRANSISTOR
#353
B=19.5
Ic IN MILLI-AMPERES
-9
-8
-7
-6
-5
-4
-3
-2
-1
Ib=500μA
Ib=400μA
Ib=300μA
Ib=200μA
Ib=100μA
+300
+200
+100
-100
-200
-300
-400
-500
-600
-700
Vc IN MILLIVOLTS
Ib=100μA
Ib=200μA
Ib=300μA
Ib=400μA
Ib=500μA
0
+0.4
+0.8
+1.2
+1.6
+2.0
+2.4
+2.8
+3.2
+3.6
+4.0
SCALE EXPANDED
Vc
Ib
1000Ω
5000Ω
12V
Ic
1000Ω
1000Ω
24V

R. Best

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: SURFACE-BARRIER TRANSISTOR PULSE GENERATOR

To: D. R. Brown

From: M. E. Petersen

Date: 17 June 1955

Approved: Torben Meisling
T. H. Meisling

Abstract: A surface-barrier transistor pulse generator has been developed and built to produce negative polarity pulses of 50 to 100 millimicroseconds duration at rates from 4 to 10 megacycles. The circuit will generate a pulse of 1 volt minimum amplitude with any combination of transistors within specifications. The pulse duration is continuously variable. Repetition rate is controlled by a Hartley oscillator covering the range of 4 to 10 megacycles with plug-in coil assemblies.

Introduction

Recent work in surface-barrier transistor circuits has indicated a need for a transistor pulse generator of flexible design which would produce negative pulses of 50 to 100 millimicroseconds duration at rates up to 10 megacycles.

After preliminary investigation it was decided to use a variable delay line to obtain the desired pulse width and a sine-wave oscillator to determine the pulse repetition rate. The sine-wave oscillator was selected primarily because of lack of a stable transistor relaxation oscillator circuit for frequencies above 5 megacycles.

Circuit symbol numbers used in the following sections refer to the attached schematic diagram.

Method of Operation

The sine-wave output of Q1 is half-wave rectified by Q2. The negative pulses from the emitter of Q2 go to both the inverter Q3 and the delay line.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The inverter is normally off and Q4 is saturated. When a negative pulse is applied to the base of Q3, it saturates and turns Q4 off. Since Q5 is normally off, this initiates a negative pulse at the collector. When the delayed negative pulse reaches the base of Q5, Q5 saturates to terminate the pulse initiated by Q4.

The emitter follower Q6 is used to secure a low impedance output.

Discussion of Circuit

The oscillator was designed for self biasing operation to eliminate the need for two supply voltages. Because of the wide variation of β in surface-barrier transistors, the network of R1, R2, and R3 was adjusted to the values shown to give adequate output without exceeding the transistor power rating for any transistor with a value of β ranging from 12 to 45 as measured on the standard laboratory β tester (I_b set at 50 μa with V_{cb} at - 3 v). L2 is an RF choke.

L1 and C1 are the tank circuit of the oscillator. The L/C ratio is determined by the requirement of maximum power output. C2 is the feedback capacitor. L1 and C2 are mounted together on a plug-in unit. C2 was selected to give nearly constant oscillator output voltage over the range covered by each coil.

L3 and C3 were selected for optimum performance over the entire frequency range. The addition of C3 to this impedance coupling network eliminated the difficulty with resonant frequencies encountered when using only L3 and C4.

L4 and C8 improve the response of the inverter. The rather large value of L4 is necessary to keep one-half the resonant period of the collector circuit longer than the longest pulse to be generated. C8 bypasses the series resistor R4.

R5 is the maximum value which will allow a low β Q4 to saturate. C5 as shown gives the shortest fall time for Q4.

The delay line shown is a General Radio variable delay line. Any delay line of approximately 200 ohms impedance can be used. However, since the fall time of the output pulse depends on the rise time of the negative pulse applied to the base of Q5, the cut-off frequency of the delay line should be several times higher than the oscillator frequency.

L6 is used to terminate the delay line because it was found that when the oscillator frequency exceeded 5 megacycles the emitter of Q2 failed to return to zero after a pulse if the delay line was terminated by the characteristic impedance of the line. This negative voltage saturated Q5 continuously to clamp the output at zero.

To secure the shortest possible fall time for Q4, the collector circuit was made resonant by using L5 as a load. R6 is bypassed for pulse frequencies by C9. If the resonant period of the collector circuit is twice the delay in the delay line, a half sine wave pulse is generated. When the delay is longer or shorter than one-half the resonant period, the inductor causes asymmetry in the output pulse. Since a range of pulse widths is to be generated in this circuit, it was necessary to select a resonant period which would permit generation of short pulses and still maintain good pulse shape for the long pulses. The value shown is the minimum value which will produce a symmetrical 100 millimicroseconds pulse. For a 55 millimicrosecond pulse, 6.8 microhenries gives a more symmetrical pulse of greater amplitude. A value of 2.7 microhenries was used for a pulse of approximately 45 millimicroseconds duration.

Since L5 aids Q5 in terminating the pulse, the output pulse fall time is less dependent on the rise time of the pulse coming through the delay line. This eases the specifications for the delay line and keeps the pulse duration nearly constant over wide changes of oscillator frequency.

R7 is the maximum value of resistance in the emitter follower which will give satisfactory fall time for the output pulse. This value also permits the use of standard 90 ohm coaxial cable in coupling to other circuits.

Summary

This pulse generator has produced negative pulses of 50 to 100 millimicroseconds duration at rates from 4 to 10 megacycles. The low frequency limit is set by the rise time of the sine-wave generator and the delay line termination. The high frequency limit is set by the pulse duration since the duty cycle cannot exceed 50 percent.

The maximum output amplitude ranges from 1 to 2 volts depending on the pulse repetition rate and the β of the transistors used.

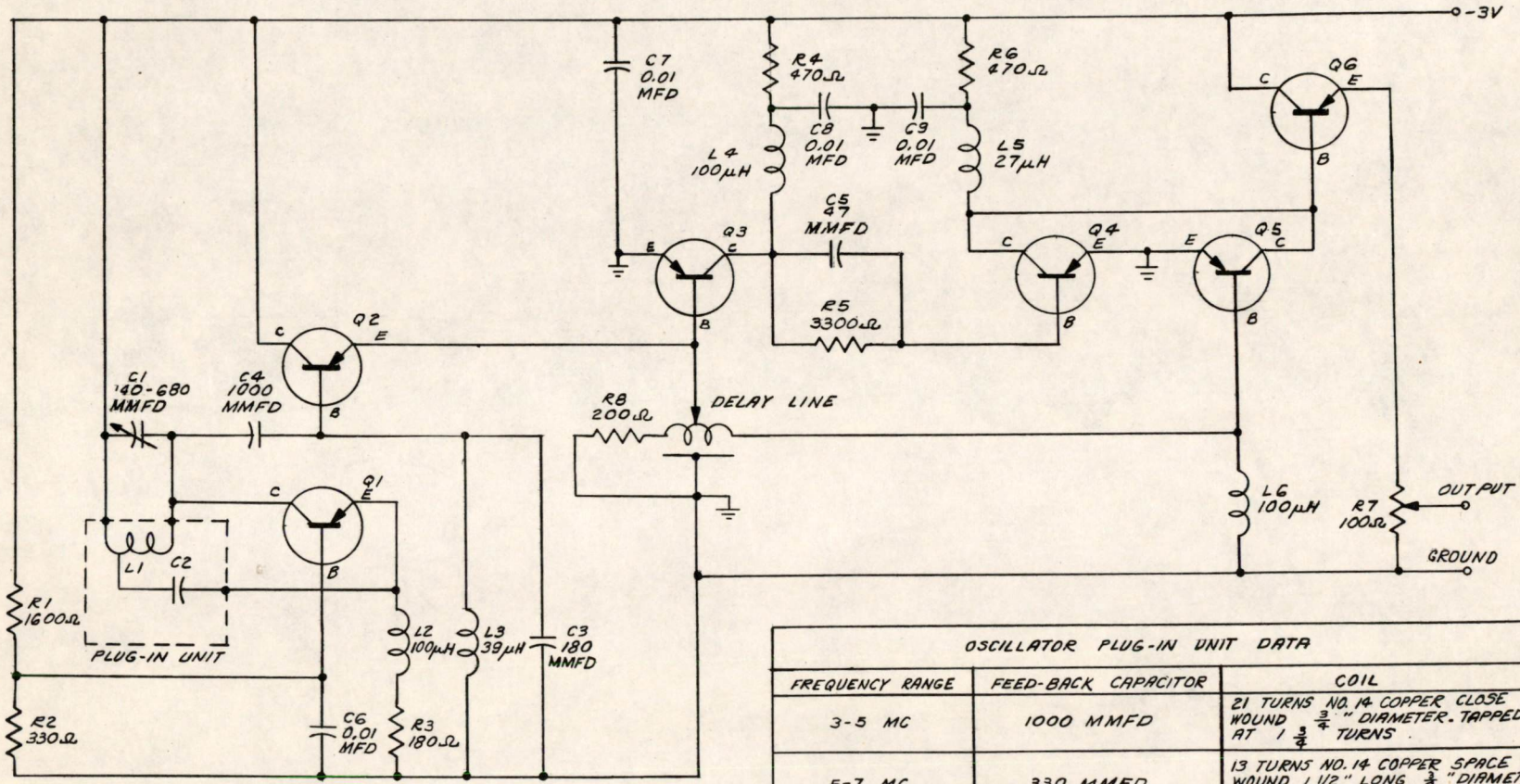
Two models of this circuit have been built and tested recently. Results with both indicate no critical circuit dress problems if normal procedures are followed.

Signed Marvin E. Petersen
Marvin E. Petersen

MEP/jg

Drawing attached:
B-63130

cc: R. Best, N. H. Taylor, D. A. Buck, M. Epstein, L. Jedynak, F. W. Sarles, M. Cerier, G. A. Davidson, P. Griffith, K. Konkle, J. Harrington, I. Lebow, R. H. Baker, R. McMahon, Group 63 Staff



OSCILLATOR PLUG-IN UNIT DATA		
FREQUENCY RANGE	FEED-BACK CAPACITOR	COIL
3-5 MC	1000 MMFD	21 TURNS NO. 14 COPPER CLOSE WOUND $\frac{3}{4}$" DIAMETER. TAPPED AT 1 $\frac{5}{4}$ TURNS.
5-7 MC	330 MMFD	13 TURNS NO. 14 COPPER SPACE WOUND 1 1/2" LONG $\frac{3}{4}$" DIAMETER. TAPPED AT 1 $\frac{3}{4}$ TURNS.
7-12 MC	150 MMFD	7 1/2 TURNS NO. 14 COPPER SPACE WOUND 1 1/2" LONG $\frac{3}{4}$" DIAMETER. TAPPED AT $\frac{3}{4}$ TURN

TRANSISTOR PULSE GENERATOR CIRCUIT

K. Olsen

Memorandum 6M-3717

George A. Davidson
June 27, 1955

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: A TRANSISTOR SELECTION SYSTEM FOR A MAGNETIC-CORE MEMORY

STATEMENT OF THE PROBLEM

A multiposition transistor selection system is to be designed that will be operated by the 2n inputs from a transistor memory-address register and that will allow random selection of one of 2^n output lines. The selected output line is to present a low impedance to ground and be capable of conducting a stated range of current amplitudes that may or may not include both directions of current flow. The non-selected output lines must present a high impedance to ground.

HISTORY OF THE PROBLEM

In the development of electronic computers an important element was the system for selection of numbers or words in the memory. With the large storage capacity possible in the magnetic-core memory which was proposed in 1949 by J. W. Forrester,[1] an elaborate system became necessary to perform the random access selection. (Reference 2 and Fig. 1.1 give a fairly complete description of the operation of the memory.)

In general, selection information[3,4] for the magnetic-core memory is supplied by a n-binary-digit memory-address register which is followed by cathode followers on each of the 2n output lines (see Fig. 1.2). The cathode followers drive a diode matrix[5] which, for a given state of the memory address register, selects one of the 2^n output lines.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Each output line drives an amplifier which in turn drives two AND gates. As is indicated in Figure 1.2, one of the AND gates in each output line is connected to a READ driver and the other AND gate in each output line is connected to a WRITE driver. When either of the drivers is turned on only one AND gate will be open and allow current to flow through a pulse transformer[6] which will couple the signal to the correct selection line.

With the development of the large (256 x 256 x 37) memory,[7] the reliability of the selection system depends mainly on the reliability of the vacuum tubes. Large heavy-duty tubes are required to handle the high currents (410 ma) needed for the ferrite core memory. Filament power must be supplied to all the tubes continuously and the resulting heat must be dissipated without damage to temperature sensitive components in the memory system. The necessary power cooling mechanism not only increases space requirements and total power input, but must be included in the reliability considerations of the complete selection system.

When the point-contact transistor appeared with its prospect of extreme reliability, long life, high efficiency and small size, computer engineers began to develope circuits that would replace the vacuum tube with its previously mentioned faults.[8,9] The point-contact transistor, however, has major defects such as low power dissipation, sensitivity to high temperature, sensitivity to humidity, and lack of uniformity. As a result, S. Oken of MIT in a Master's Thesis[9] reported that he was unable to drive the ferrite memory cores directly with

point-contact transistors or with early junction transistors. He did develop a core driver consisting of a point-contact flip-flop driving a grounded-base junction transistor (to increase the output impedance) that was capable of driving several metallic cores. Since the switching time of the metallic cores is 10 microseconds when used in coincident-current operation, reverse recovery problems were not as great as would be expected in a ferrite core memory with 1 microsecond operation. The supply voltage of the transistor driver must be high enough to keep the output current constant when the cores are switching and, as a result, the dissipation in the transistor will be high when the cores are not switching. Therefore, the number of cores to be driven is limited by the maximum dissipation of the transistor.

K. Olsen[10] has suggested using the transistor in the saturated state where dissipation will be low even if both READ and WRITE generators cause current to flow through the same transistor. The outputs of all the non-selected transistors will be subjected to the memory plane back voltage, but these transistors will be open circuited and there will be little or no dissipation.

R. Baker and R. McMahon of Lincoln Laboratory are also working on a scheme in which only the non-conducting transistor must absorb the back voltage. The main difference between the two schemes is that, in the first, the transistor is saturated and bilateral, and in the second, is non-saturated and unilateral. In the latter arrangement two transistors and a pulse transformer are required. Both systems require an external READ and WRITE current source.

The work of P. Gray[11] and others[12,13,14] on the transient response of junction transistors used as a current source provides a general indication of the circuit configuration having the shortest turn-on and turn-off time.

Some useful techniques have been obtained from the work of N. T. Jones[15] who tested the recovery time of point-contact transistors in terms of parameters which facilitate comparison of different units.

PROPOSED PROCEDURE

The transistor memory-address register that will be the input to the proposed selection system has already been designed by members of the computer development group at Lincoln Laboratory. The maximum output current and the output impedance are two parameters that will determine, in part, the circuitry that follows. Because the expected output current will be on the order of 1 ma, grounded emitter stages will be used to increase the current amplitude. There are three possible places for the amplification: before the matrix where there are 2n lines, after the matrix where there are 2^n lines and within the matrix where there are more than 2^{n+1} units.[16]

Since reverse recovery is a problem in diodes capable of carrying the 20 to 100 ma currents that are required to drive the selection transistor, it is unlikely that all of the amplification can take place before the diode matrix. If the selection transistor requires more than one driver after the diode matrix a transistor matrix will be considered as a possible element. Such a matrix will be desirable if it would

eliminate more diodes and transistors than it added, or if the response times are decreased.

The non-saturated mode of operation uses the transistor* in the grounded collector configuration. When one of the drivers is pulsed, current will flow into the emitter of the transistor that has the low base voltage. Since the emitter diode was floating prior to activation of the current source, it will take some time for the holes to diffuse to the collector. Therefore, the initial voltage drop and the instantaneous power dissipation will be high. When the current source is withdrawn, holes will recombine, but, with no field to aid the process, the base driver will still be the main element in the turn-off process unless the base is kept positive with respect to the collector even when this particular line is selected. Since this technique is being studied by another group at Lincoln Laboratory, this thesis will be directed towards the saturated mode of operation.

With the emitter grounded and a resistor connected from the collector to a negative supply, the collector current will be very small if the base current is zero. As the base current is increased the collector current will increase and the collector to emitter voltage will decrease. When the point is reached where increasing the base current will neither increase collector current nor reduce collector to emitter voltage, the transistor is said to be in saturation. The

---

*The following discussion applies to PNP transistors.

ratio of collector current to base current at the transition point is the d-c saturation current gain, B_s. If a current source is connected to the collector instead of the resistor and battery, the circuit corresponds to the saturated configuration proposed by Olsen.[10] Let a step of base current be applied to the transistor and let a narrow pulse of current be forced out of the collector by the current generator. If the pulse of current occurs shortly after the base current, then the voltage from collector to emitter will not be the low d-c value. As the current pulse is delayed more, the collector voltage decreases exponentially to its low d-c value. The saturation current gain, B_s, is not constant but varies inversely with base current. The gain is not the same for both directions of collector current and is greater for current out of the collector. One of the first tasks will be to determine B_s as a function of the above parameters for various transistors.

If the transistor is used bilaterally, some advantage will be gained by first pulsing current out of the transistor and then later into the transistor. This follows because, in most PNP transistors, the forward current gain is greater than the reverse current gain which, however, increases with time. It may also be desirable to shape the base current so that the transistor does not become over saturated if one position remains selected.

During the first phase of the turn-off time the base to emitter resistance is very low. In the second phase the base voltage rises to its final value. The external circuitry determines the current flow in the first phase and the ultimate base voltage in the second case. The

optimum driving circuits will be determined from the requirements of the turn-off time and the information derived from measurements on the above phenomenon.

One end of each memory line will be tied to both current sources and the other end will go to individual transistors; thus, the voltage across the memory load of one line will be applied to the outputs of all the non-selected transistors. The base of a non-selected transistor must always be more positive than the collector to emitter voltage so that, for the positive peak load voltage, no load current will flow. Therefore, the maximum load to be driven is determined by the voltage rating of the transistor which must not be exceeded by the sum of the base voltage and the negative peak load voltage.

To maintain the proper current through the selected winding, the reverse currents through the non-selected transistors must be small. As the size of the core memory increases, the added number of reverse current paths creates an increasingly acute problem.

The three important characteristics of the final transistor appear to be:

1. It should have a high current gain at high values of collector current.
2. The recovery time should be short when driving the base with a reasonably low impedance voltage source.
3. The pulses of voltage on the non-selected transistors should not cause appreciable current flow.

There may be other techniques of operation that will allow the transistor more time to recover than the straight forward selection system now used in the memory. If the transistor is returned to the open state as soon as the drive current has stopped, more time would be allowed for reverse recovery. The use of one transistor for READ and one for WRITE would also reduce the recovery requirements. Because the emitter element is smaller than the collector, it is possible that if the two leads, collector and emitter, are interchanged in the above circuit that reverse recovery time would be decreased.

EQUIPMENT NEEDED

The test equipment needs can be fulfilled through the use of Burroughs Unitized Equipment which is available at Lincoln Laboratory. Materials will also be supplied by Lincoln Laboratory

ESTIMATED TIME

Preparation of Proposal	75
Further search of literature	20
Experimental work & analysis	180
Correlation of results and formulation of conclusions	50
Preparation of thesis	75
	400

SIGNED: George A. Davidson
George A. Davidson

Date: June 27, 1955

GAD/dg

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

APPROVED: Richard D. Thornton
Richard D. Thornton
Instructor of
Electrical Engineering

Distribution: Staff, Group 63
D. Baker
R. McMahon
D. Shansky

Drawings: A-58815
B-63065

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A-58815

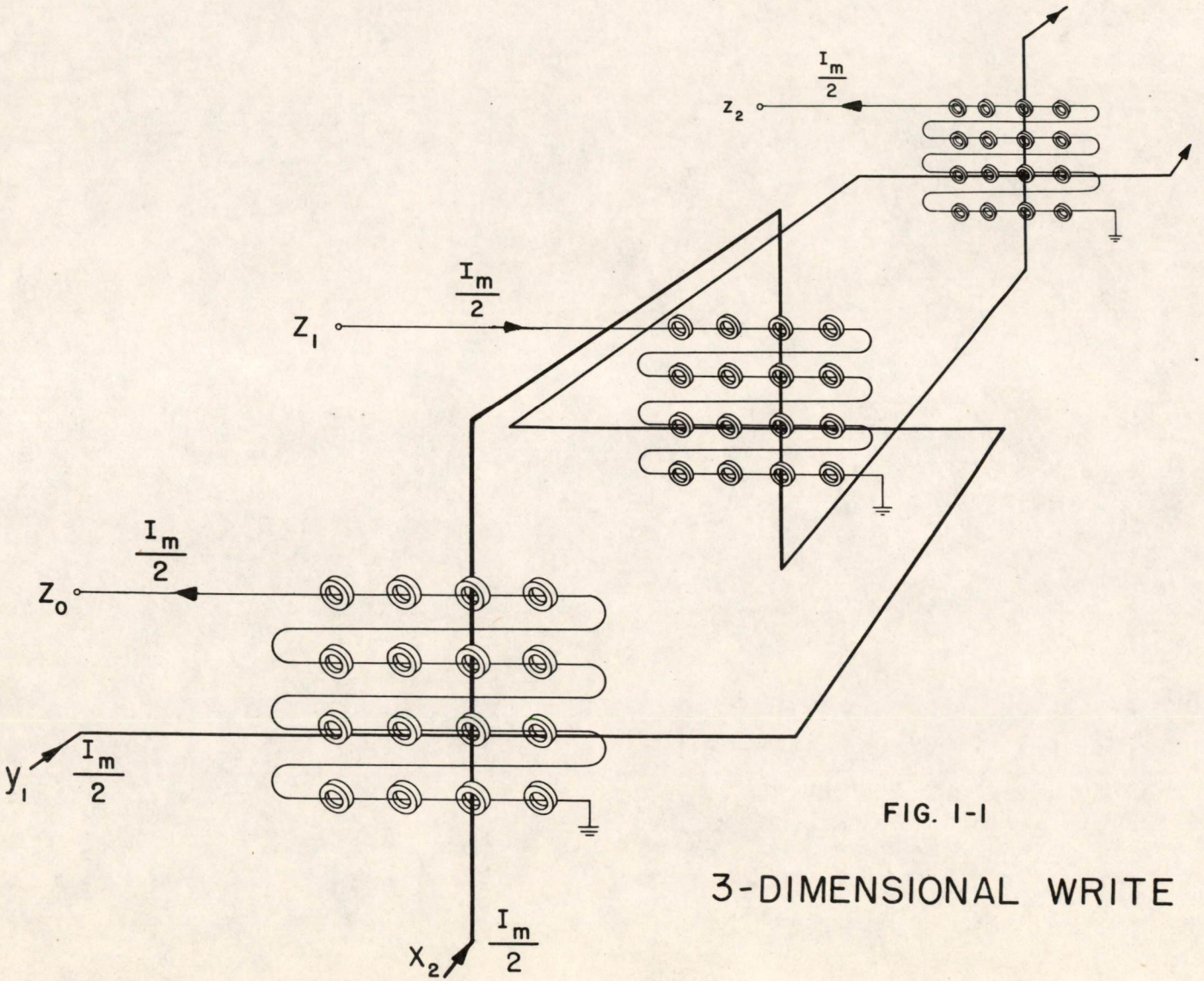

FIG. 1-1

3-DIMENSIONAL WRITE

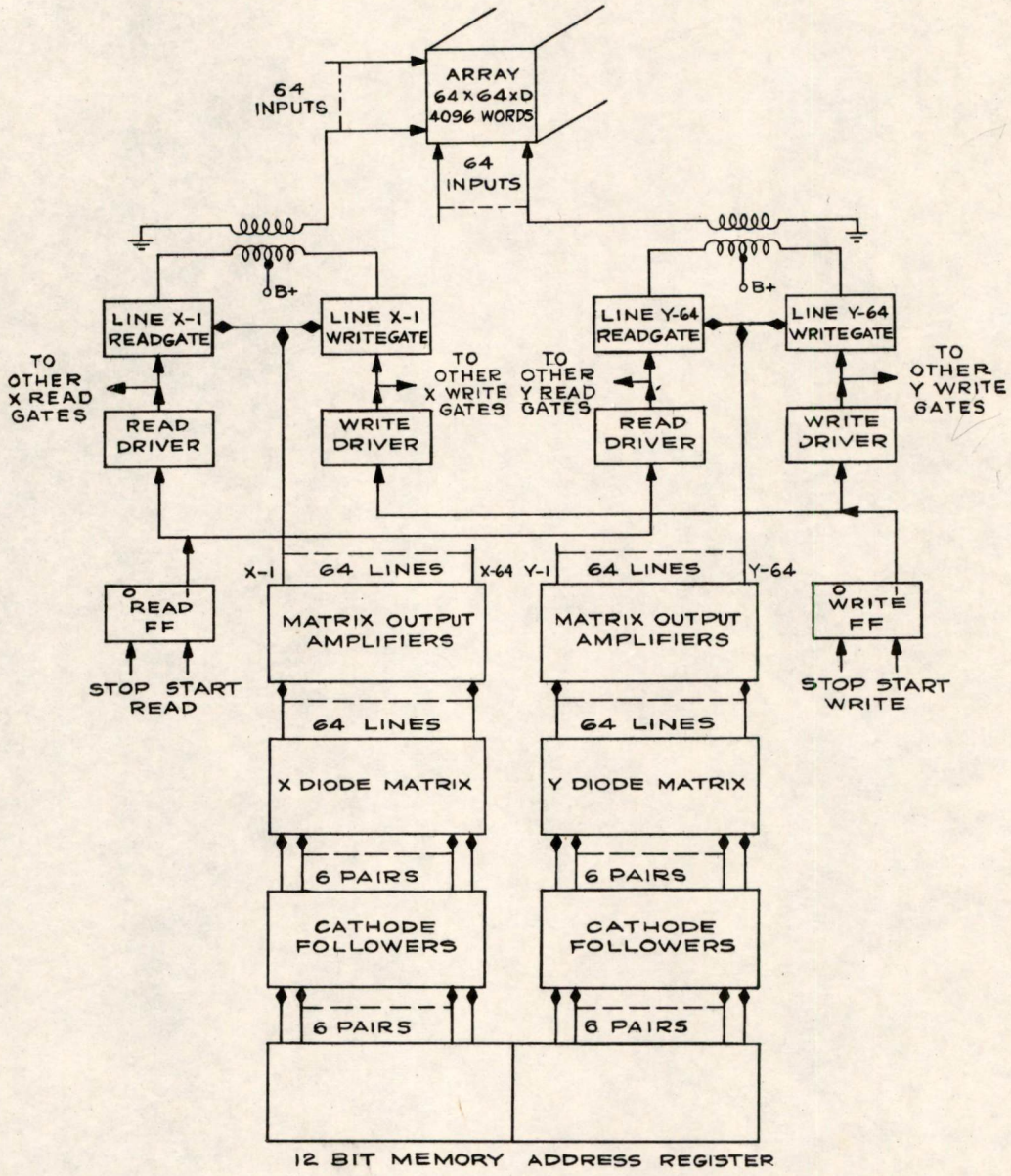

FIG. 1.2
SELECTION SYSTEM BLOCK DIAGRAM

H Anderson

2.3.0

Memorandum 6M-3768

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: AN/FSQ-7 PROGRAMMING COURSE OUTLINE

To: Distribution List

From: Philip R. Bagley

Date: 20 July 1955

Approved: J. F. Jacobs

J. F. Jacobs

Abstract: A tentative outline is presented for the AN/FSQ-7 Programming Course (18 July - 16 September 1955).

The outline below is a tentative outline of the topics in the AN/FSQ-7 Programming Course. The course is being taught by IBM and is under the supervision of Robert Lowe. The first session is being given at the Lexington Field Station from 18 July through 16 September 1955. Class notes for the course are being published in a limited quantity. Questions concerning the course or course notes should be directed to Robert Lowe at the Lexington Field Station (extension 5418) or to the writer, Room C-147, extension 5470.

AN/FSQ-7 PROGRAMMING COURSE OUTLINE

I. Introduction

- A. General Properties of Computers
- B. Basic Components of Electronic Computers
- C. Principal Applications
- D. Number Systems

II. FSQ-7 Computer Properties

- A. Introduction
  - 1. Purpose
  - 2. Logical Elements

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

B. Physical Components of Central Computer

1. Core Memory
2. Arithmetic Registers
3. Control Registers

C. Word Format

1. Introduction
2. Data

D. Programming

1. Purpose
2. Definition
3. Elementary Examples

E. FSQ-7 Operation Codes

F. Flow Diagrams

G. Timing

1. PT
2. OT
3. Pause
4. Break-in
5. Machine Commands

H. Index Registers

1. Definition
2. Physical Index Registers
3. Indexing Instructions
4. Branching Control Using Index Registers
5. Index Reference
6. Address Modification
7. Benefits

III. Programming Techniques

A. Symbolic Programming

1. Advantages

2. Form

3. Use of Symbolic Addresses

4. Symbolic Assembly Program

B. Table Look-Up

C. Sorting

D. Subroutines

E. Program Testing

F. Programming Considerations Associated with Machine Errors and Checks

G. Fundamentals of Scaling for Fixed Point Computing

IV. Input-Output Devices

A. Punched Cards

1. Method of Recording Data on Cards

2. Method of Reading Cards

3. Forms of Data Read Into FSQ-7

4. Card Types for FSQ-7

B. Card Reader

1. Card Reader Ready

2. Read Instruction

3. Programmed End of File

4. Buttons and Lights on Card Reader

5. Manual Operation of Card Reader

6. Card Reader Timing

C. Card Punch

1. Program Control of Punching
2. Special Program Control of Punching
3. Card Punch Reader
4. Buttons and Lights on Card Punch
5. Manual Operation of Card Punch
6. Card Punch Timing

D. Line Printer

1. Programmed Operation of Printer
2. Printer Ready
3. Buttons and Lights on Printer
4. Control Panel
5. Carriage Control
6. Sense and Operate
7. Manual Operation
8. Line Printer Timing

E. Magnetic Drum

1. Operation
   a. Physical Description
   b. Terminology
2. Uses of Magnetic Drums with the AN/FSQ-7
   a. As Auxiliary Storage
   b. As a Time Buffer
3. Location of Information on the Drums
   a. Address Mode
   b. Interleaving
   c. Status Mode

F. Magnetic Tapes

1. Physical Description and Checking

2. Storage by Record and File and Use

3. Machinery Bookkeeping for Preparedness, Readiness, Record and File

4. Programming

V. Machine Checking and Maintenance

A. Test Memory

1. Purpose

2. Physical Arrangement

3. Control

B. Maintenance Console

1. Purpose

2. Controls

C. Manual Control at the Console

1. Inserting Words into Core Storage

2. Starting and Stopping Computer

3. Displaying Contents of Selected Registers

D. Sense Instruction

1. Definition

2. Description of Sense Units

3. Parity Checking

Signed: Philip R Bagley
Philip R. Bagley

PRB:ttf

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SUBJECT: TRANSISTOR CIRCUITS COURSE
NUMBER 1. INTRODUCTION

To: Distribution List

From: Donald J. Eckl

Date: July 20, 1955

Approved: DRB
David R. Brown

Abstract: This is the first in a series of notes covering material presented in lectures on transistor circuits for engineers. The introductory material below contains fundamental ideas about semiconductors which should be known by the transistor circuit designer. These ideas are presented in a simplified form but will serve as a basis for some future discussions later on.

The transistor is a solid state device, making use of a semiconductor as a medium for transporting charge, which is capable of producing a power gain. The properties of semiconductors make possible the control of a large current passing through one pair of electrodes of the transistor by means of a small current through a second pair of electrodes. This first note will discuss briefly the more important properties of semiconductors for transistor applications.

Metals, Semiconductors, Insulators

A metal is a solid in which the electric field E is everywhere zero, i.e., it is a body in which no space charge can exist. The resistivity of a metal is extremely low; copper, for example, having a resistivity of about 1.7×10^{-6} ohm-cm. Insulators, however, will support a space charge and are characterized by very high resistivity, of the order of 10^{15} ohm-cm.

Semiconductors fall in a class between these two extremes. They can contain a limited space charge and in a pure state, where they are called intrinsic semiconductors, may have resistivities of a few ohm-cm to several thousand ohm-cm at room temperature. For example, intrinsic germanium is about 60 ohm-cm and intrinsic silicon is about 60,000 ohm-cm at 25°C.

Another way of illustrating the difference between metals and semiconductors is to consider the number of conduction electrons. In

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

metals this is about 10^{22} electrons per cc. Semiconductors range from 10^{11} to 10^{17} conduction electrons per cc, or one for every 10^{5} to 10^{11} electrons in a metal.

Impurity Semiconductors

Most semiconducting materials are not pure or intrinsic. Small amounts of impurities added to a semiconducting material will considerably reduce the resistivity. Therefore, the resistivity of a given sample can be controlled by its purity. The amount of impurity necessary to produce material useful for transistors is of the order of 10^{15} impurity atoms per cc whereas the normal population of semiconductor atoms is about 10^{22} per cc. That is, we are dealing with impurities of 1 part in 10 million.

Temperature and Conductivity

The relation between temperature and conductivity for an intrinsic semiconductor is shown below in Fig. 1.

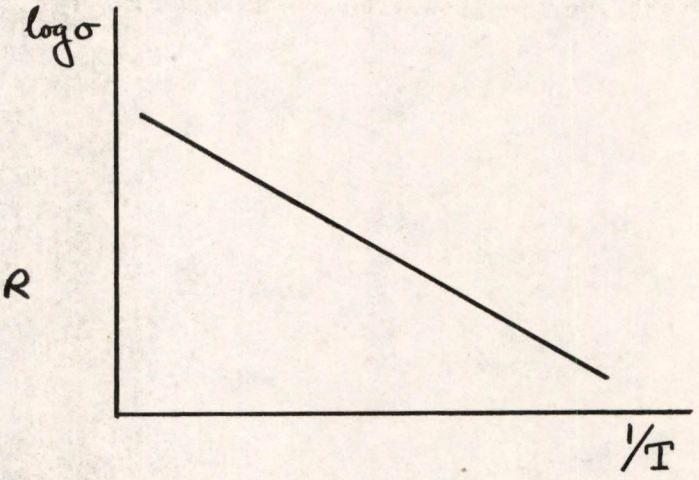


FIG. 1
INTRINSIC
SEMICONDUCTOR

The conductivity σ increases with the absolute temperature T. If impurities are added to the semiconductor the conductivity is increased and the variation with temperature is as shown in Fig. 2.

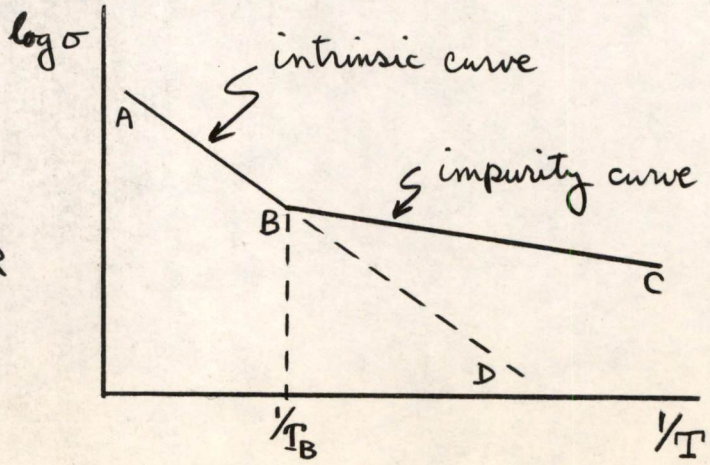


FIG. 2
IMPURITY
SEMICONDUCTOR

In the interval BC the impurities control the value of the conductivity. However, above the temperature T_B the impurities no longer have any effect and the material behaves like an intrinsic semiconductor with the curve ABD. Since transistors depend on the properties of impurity semiconductors, this temperature T_B would represent the point where no transistor action could take place and, therefore, an absolute temperature limit for the device. In actual practice circuit failure would probably occur considerably below this temperature.

Crystalline Structure

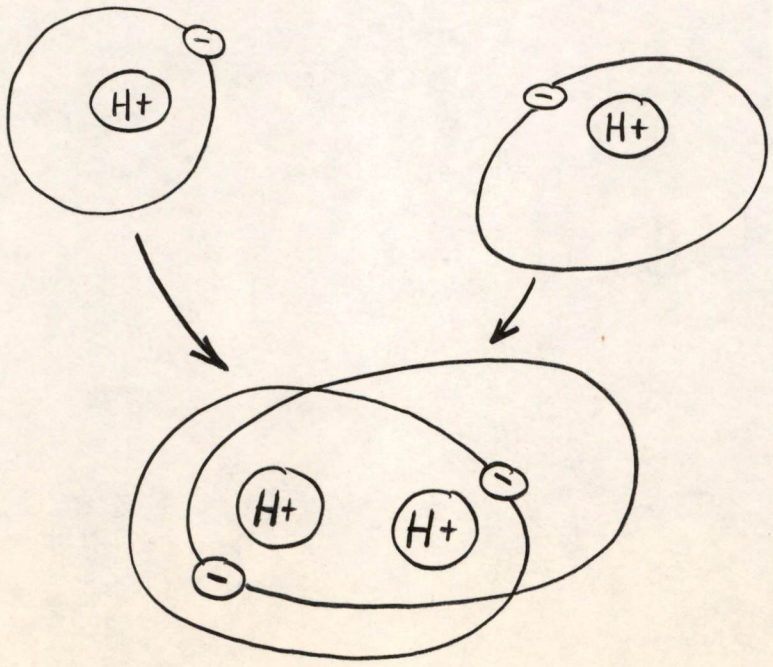
The atoms in a semiconductor form a crystalline structure, i.e., they arrange themselves in a regular pattern throughout the material. Moreover, the atoms in which we are interested are all members of the 4th column of the periodic table which is reproduced in part below in Fig. 3. The numbers in each column represent the positive charge on the nucleus of the atom.

FIG. 3

P-Type III		IV		N-Type VI	
B	+5	C	+6	N	+7
Al	+13	Ge	+14	P	+15
Ga	+31	Si	+32	As	+33
In	+49	Sn	+50	Sb	+51
Tl	+81	Pb	+82	Bi	+83

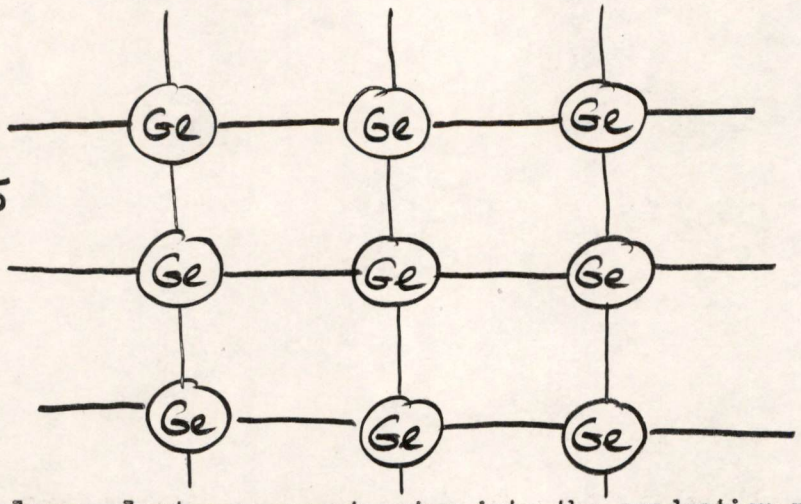
The 4th-column atoms all have four valence electrons and form valence crystals which are held together by electron-pair binding, i.e., pairs of electrons from different atoms form bonds which hold the crystal together. It is not within the scope of this paper to go into the details of atomic bonds but the sketch below may help to convey the idea.

FIG. 4



Two hydrogen atoms with single valence electrons are shown coming together to form an H_2 molecule which has electrons associated with both atoms. The "dual ownership" of the electrons by the two atoms serves to bind the molecule together. This can be represented by the symbol (H)—(H) In a similar manner a germanium crystal can be represented by:

FIG. 5

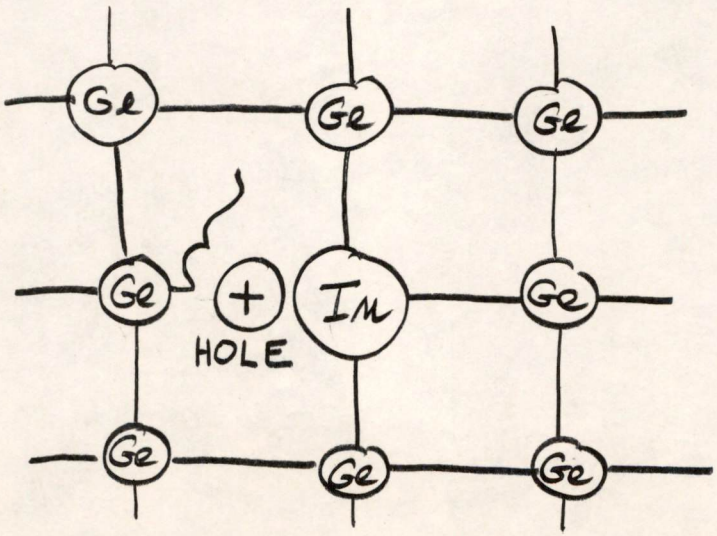


These valence electrons cannot enter into the conduction process since they are not free to move about.

Donors and Acceptors

If we now replace one of the germanium atoms in Fig. 5 by an impurity atom from the 3rd column of the periodic table in Fig. 3 the crystal will appear as follows:

FIG. 6

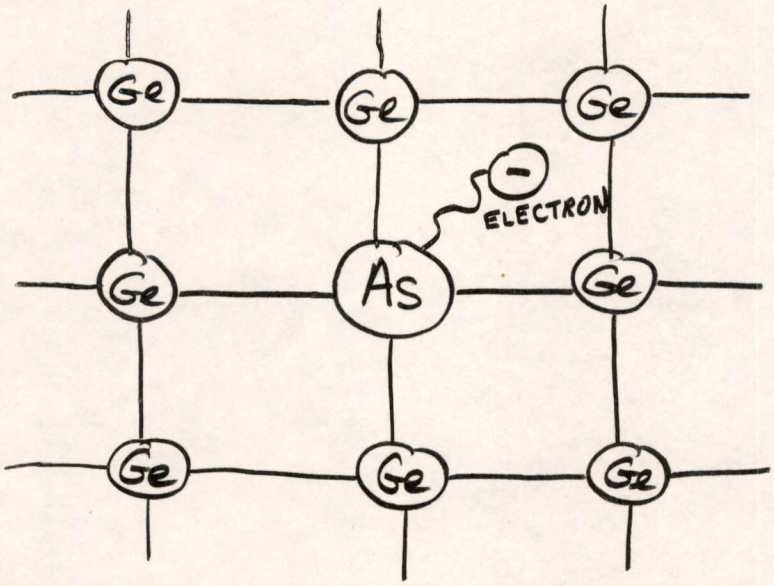


Since the indium atom has only three valence electrons one bond will be incomplete leaving a hole in the crystal. As other valence electrons can now move in to fill this gap the hole effectively moves through the

crystal and acts like a positive charge which can conduct current. Impurities of this type are called acceptors since they can accept valence electrons and the resulting impurity semiconductor is called a P-type semiconductor since the charge carriers are positive holes.

If a germanium atom is replaced by an element in column VI the situation is as follows:

FIG. 7



An extra electron is now available which is free to conduct current. An impurity of this type is called a donor since it provides conduction electrons, and the impurity semiconductor is called an N-type semiconductor since the charge carriers are negative electrons.

The two types of charge carriers mentioned above, holes and electrons, are important in transistors. Electrons have a mobility, $\mu = \bar{v}/E$, of 3600 cm^2/volt-sec while holes have a mobility of 1700 cm^2/volt-sec. These mobility figures indicate the velocity of the carrier under a field of 1 volt/cm. However the base region in a transistor is traversed by carrier diffusion rather than acceleration by an electric field. The diffusion rate is directly related to the mobility, the diffusion constant being

$$D = \frac{1}{40} \mu \quad cm^2/sec.$$

Therefore electrons will move through the transistor at a higher speed than will holes.

Operation of a pnp Transistor

Consider a transistor made up of N-type semiconducting material surrounded by P-type on either side. Three connections, emitter, base, and collector, are made to the three regions respectively as shown in Fig. 8.

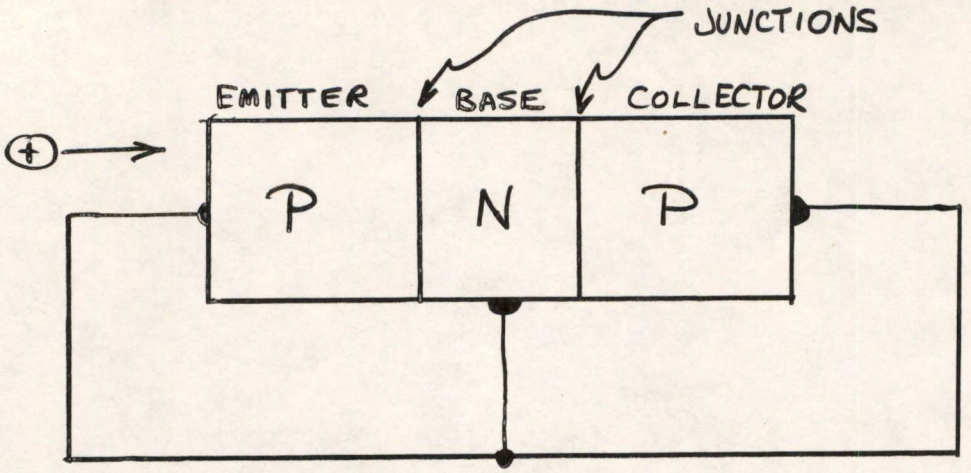


FIG. 8 A PNP JUNCTION TRANSISTOR

This is a pnp junction transistor and is represented schematically by

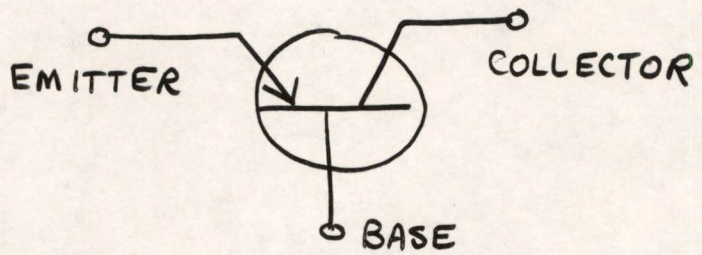


FIG. 9

If we consider the potential of a positive charge (or hole) passing from emitter to collector with all 3 elements grounded it will appear as shown in Fig. 10.

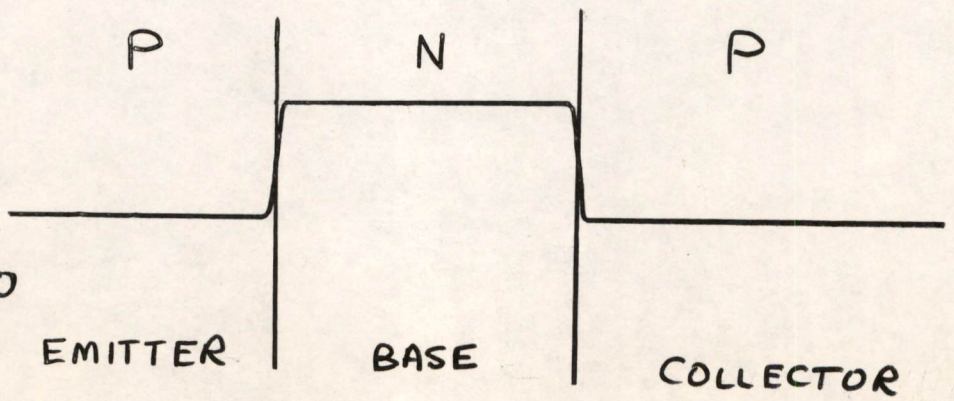


FIG. 10

When normal bias voltages are applied to the transistor as shown in Fig. 11 the potential diagram takes the form shown:

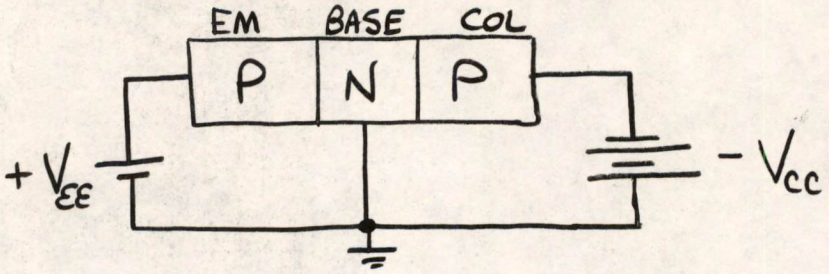
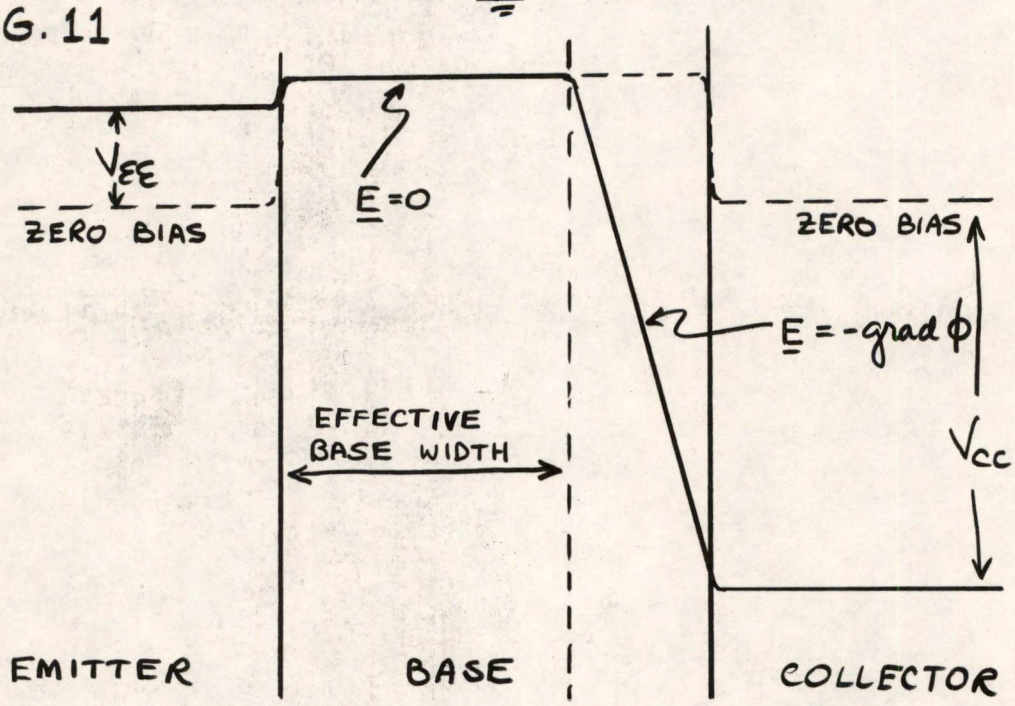


FIG. 11



Note particularly that there is no electric field through the largest part of the base region. Therefore, holes from the emitter must diffuse through the base until they reach the field in the collector region where they are accelerated into the collector.

Now consider a typical pnp which has a geometry as shown in Fig. 12. A hole leaving point A in the emitter under the influence of an emitter-base voltage moves through the base region by diffusion. The probability of its taking paths 1--6 to the collector is considerably greater than for path 7 into the base circuit. This is true for any hole leaving the emitter.

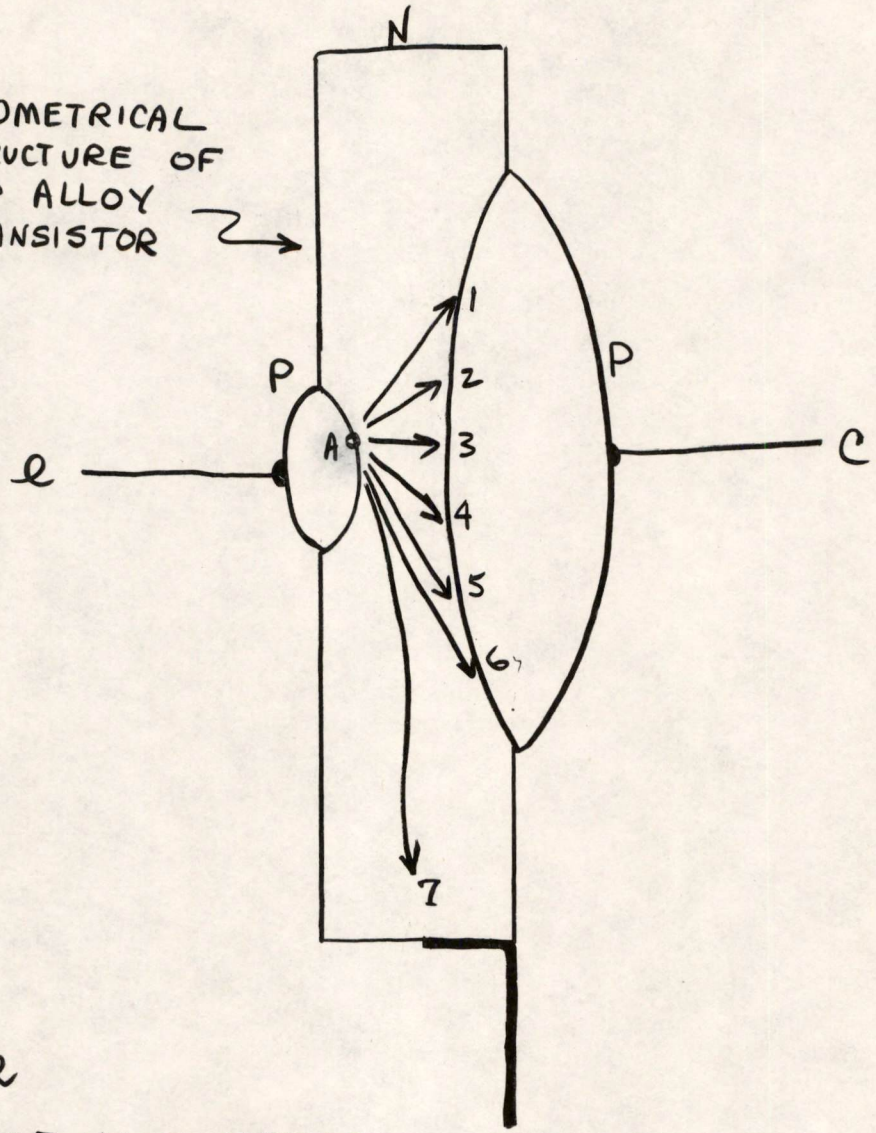


FIG. 12

PATHS OF HOLE INJECTED INTO BASE AT POINT A.

Therefore most holes will reach the electric field at the collector and be carried away into the collector. It is only when a very large current is flowing from emitter to collector that a reasonable number of holes can diffuse into the base -- say 2 percent or less of the total. Therefore, looking at the problem another way, if we require a certain current to flow in the base, we must have a much larger current flowing in the

collector circuit. This is how we get a current gain in the transistor. A small base current will produce a large collector current.

This is, of course, an oversimplified picture but it does serve as an illustration of the transistor mechanism.

With the above introduction we will go into equivalent circuits in the second lecture.

Donald J. Eckl

Donald J. Eckl

DJE/md

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Subject: TRANSISTOR CIRCUITS COURSE
NUMBER 2. EQUIVALENT CIRCUITS OF TRANSISTORS

To: Distribution List

From: Donald J. Eckl

Date: August 1, 1955

Approved: DRB
David R. Brown

Abstract: A number of different equivalent circuits are used to represent the transistor and an understanding of these is imperative to the circuit designer. The open-circuit impedance representation, the equivalent-T representation, and the hybrid representation are all commonly used. An important modification of the standard T-circuit was made by J. M. Early. A π-variation of this has proven useful for surface-barrier transistors.

1.0 Open-Circuit Impedance Representation of a Transistor

Suppose we consider the transistor as a four-terminal device as shown below in Fig. 1. The transistor can be represented as a

a.)

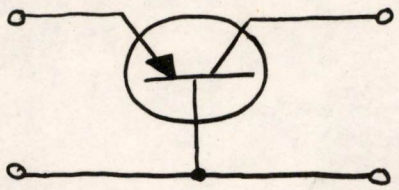
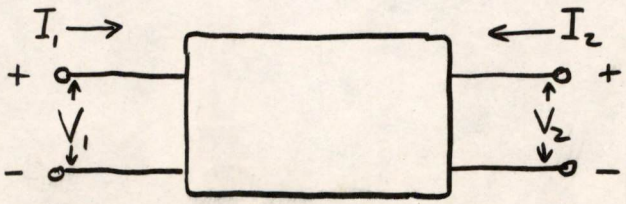


FIG. 1



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

"black box" with input and output currents and voltages as specified. A general representation of such a black box is given in Fig. 2 with the circuit equations written below.

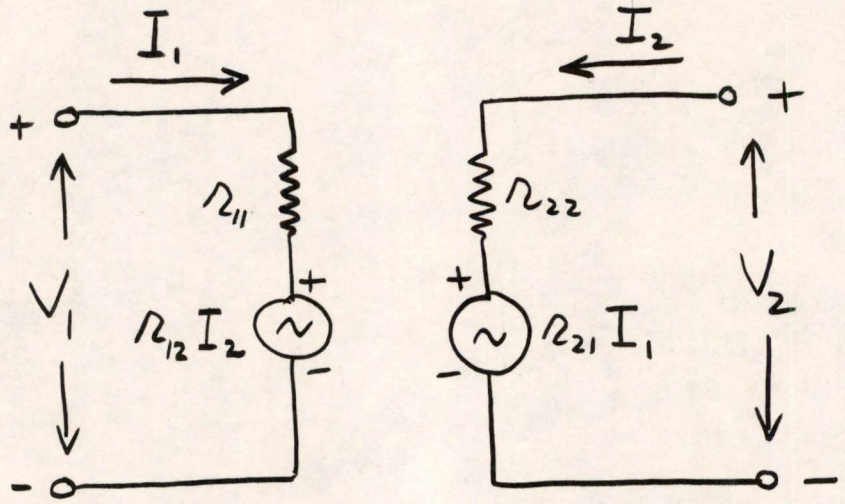


FIG. 2 - FOUR TERMINAL NETWORK

$$V_1 = r_{11}I_1 + r_{12}I_2 \qquad (1)$$

$$V_2 = r_{21}I_1 + r_{22}I_2 \qquad (2)$$

We can express the coefficients of the currents by the following derivatives:

$$\left[\frac{\partial V_1}{\partial I_1}\right]_{I_2 \text{ CONST}} = R_{11}. \qquad \left[\frac{\partial V_2}{\partial I_1}\right]_{I_2 \text{ CONST}} = R_{21}.$$

$$\left[\frac{\partial V_1}{\partial I_2}\right]_{I_1 \text{ CONST}} = R_{12}. \qquad \left[\frac{\partial V_2}{\partial I_2}\right]_{I_1 \text{ CONST}} = R_{22}.$$

These coefficients r_{ij} are called the open-circuit impedances of the transistor since they are the relations between current and voltage (i.e. impedance) in equations (1) and (2) if one current is made zero (i.e. open-circuited). If these impedances are known, then equations (1) and (2) specify the operation of the transistor and Fig. 2 is an equivalent circuit. There are, however, other more useful representations.

2.0 Equivalent-T Representation

Perhaps the most common and generally useful representation of a transistor is the T-equivalent circuit. This is largely because it presents a picture readily related to the actual physical construction of the transistor. The equivalent-T circuit is drawn in Fig. 3. Here the subscripts c and e are used for collector and emitter. Equations (3) and (4) represent the circuit.

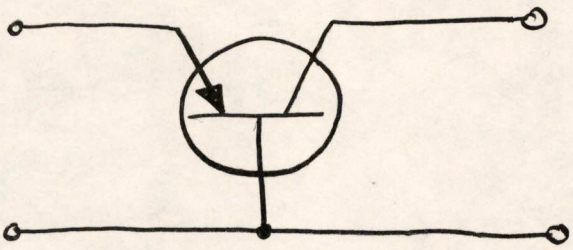
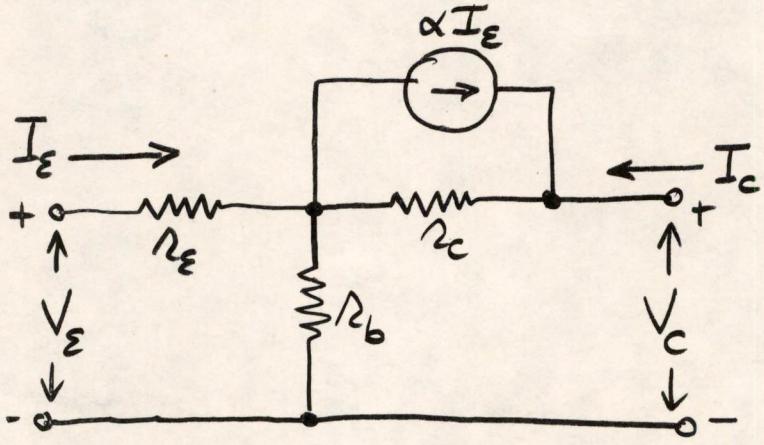


FIG. 2



$$V_e = (r_e + r_b)I_e + r_b I_c \qquad (3)$$

$$V_c = (\alpha r_c + r_b)I_e + (r_c + r_b)I_c \qquad (4)$$

If we now rewrite (1) and (2) with new subscripts we get:

$$V_e = r_{11} I_e + r_{12} I_c \tag{1a}$$

$$V_c = r_{21} I_e + r_{22} I_c \tag{2a}$$

Comparing the two sets of equations above gives the following relations between the equivalent-T impedances and the open-circuit impedances:

$$r_{11} = r_e + r_b$$

$$r_{12} = r_b$$

$$r_{21} = \alpha r_c + r_b$$

$$r_{22} = r_c + r_b$$

These quantities can be expressed by the derivatives given before and, in particular, the base and collector resistances are given by:

$$r_c \approx r_{22} = \left| \frac{\partial V_c}{\partial I_c} \right| I_e \text{ const}$$

$$r_b = r_{12} = \left| \frac{\partial V_e}{\partial I_c} \right| I_e \text{ const}$$

Suppose we consider equation (2a) and take derivatives:

$$\partial V_c = r_{21} \partial I_e + r_{22} \partial I_c .$$

Now keep V_c constant and we get

$$0 = r_{21} \partial I_e + r_{22} \partial I_c .$$

or

$$-\left[\frac{\partial I_c}{\partial I_e}\right]_{V_c} = \frac{r_{21}}{r_{22}} = \frac{\alpha r_c + r_b}{r_c + r_b} . \tag{5}$$

Let us now define this quantity as

$$\alpha \equiv \text{short-circuit current gain.}$$

The "short-circuit" part of the definition arises from the requirement that V_c be constant (or zero).

$$\therefore \quad \alpha \equiv \left[\frac{\partial I_c}{\partial I_e}\right]_{V_c \text{ const}}$$

It is now necessary to redesignate the previous α in the equivalent circuit by the symbol α_e for "alpha, equivalent circuit".

Then, $$\alpha = \frac{\alpha_e r_c + r_b}{r_c + r_b} \approx \alpha_e.$$

or, $$\alpha_e = \alpha - \frac{r_b}{r_c}(1 - \alpha).$$

The two quantities α and α_e are very nearly equal and are quite often used indiscriminately, but it should be kept in mind that they are different.

It is possible to convert the current generator in the equivalent-T to a voltage generator as shown in Fig. 3a.

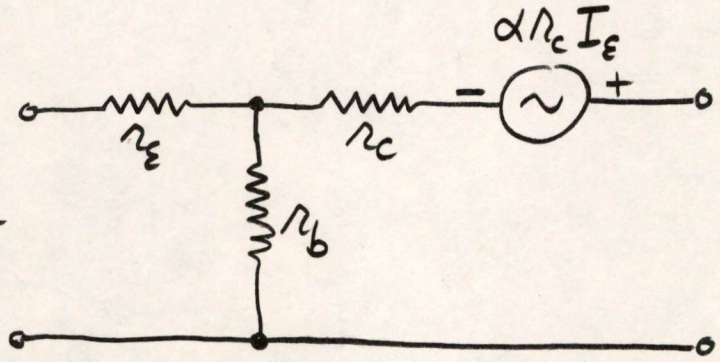


FIG. 3a

3.0 Hybrid Parameters

These are another set of transistor parameters which are used extensively in small signal work and increasingly of late in specifications. They are called hybrid because they make use of both current and voltage as independent and dependent variables. The equivalent circuit in terms of the hybrid parameters is shown in Fig. 4.

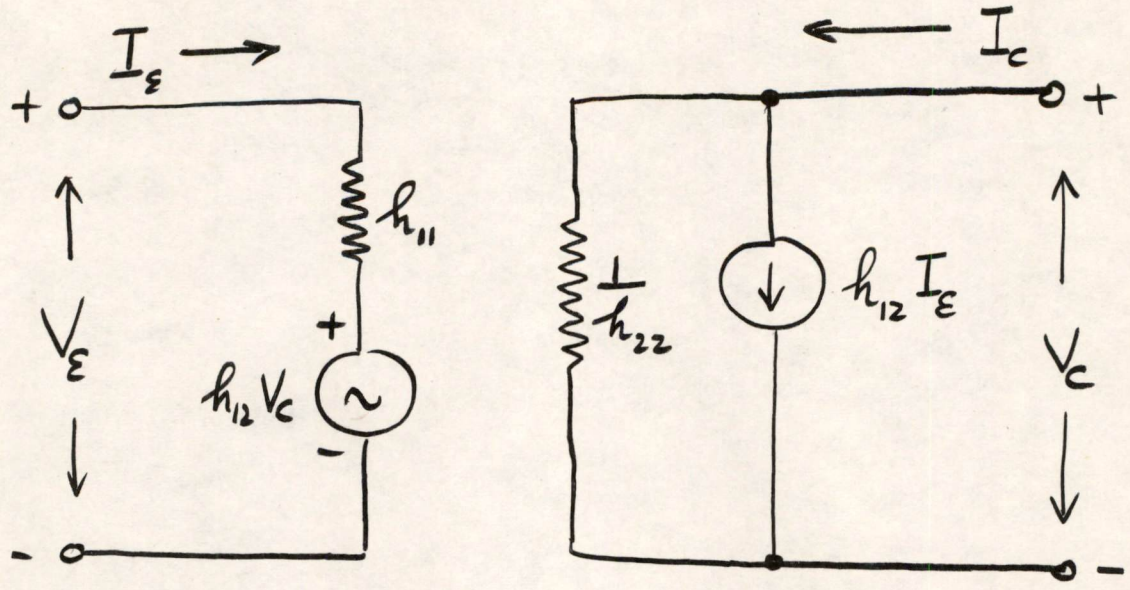


FIG. 4 - EQUIVALENT CIRCUIT USING HYBRID PARAMETERS

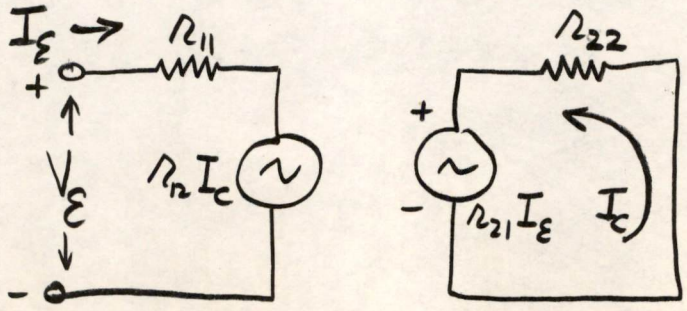
$$V_e = h_{11} I_e + h_{12} V_c \quad (6)$$

$$I_c = h_{21} I_e + h_{22} V_c \quad (7)$$

From equation (6) we can see by making $V_c = 0$ that,

h_{11} = <u>short-circuit input impedance</u>

Consider this in terms of open-circuit impedances as shown below:



From the collector circuit,

$$-I_c = \frac{r_{21}I_e}{r_{22}}$$

$\therefore$ the emitter generator $= r_{12}I_c = -\frac{r_{12}r_{21}I_e}{r_{22}}$

$$\therefore V_e = r_{11}I_e - \frac{r_{12}r_{21}}{r_{22}}I_e$$

Thus the short-circuit input impedance,

$$h_{11} = r_{11} - \frac{r_{12}r_{21}}{r_{22}} .$$

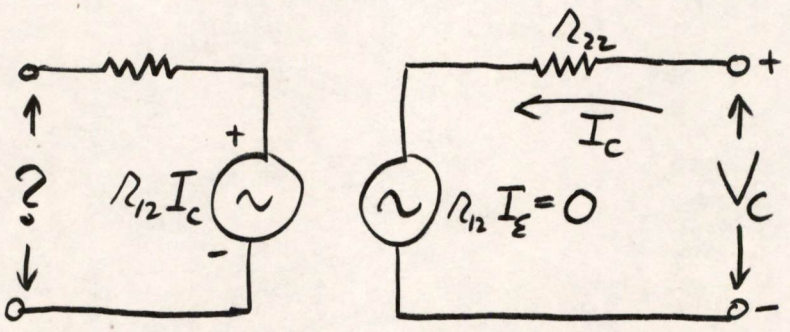
or $$\boxed{h_{11} = r_e + r_b(1 - \alpha).} \qquad (8)$$

The short-circuit input impedance is also often expressed as $1/g_{11}$ where g_{11} is the short-circuit input conductance.

By making $I_e = 0$ in equation (6) we see that,

$$h_{21} = \underline{\text{open-circuit feedback parameter}}.$$

In terms of open circuit impedances we can calculate this as follows:



From the collector circuit, $I_c = \frac{V_c}{r_{22}}$.

$\therefore$ the emitter generator, $r_{12}I_c = \frac{r_{12} V_c}{r_{22}}$.

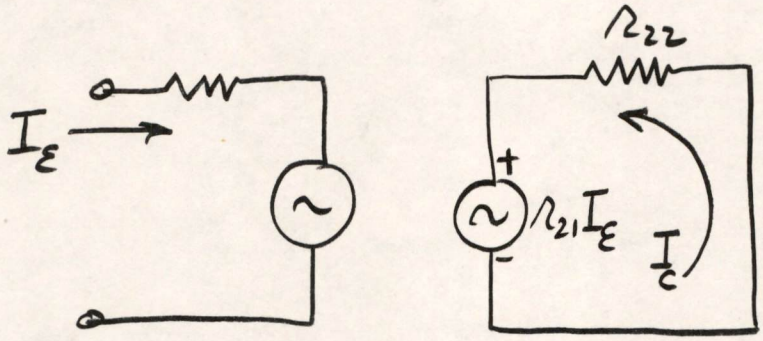
$$\therefore V_e = \frac{r_{12}}{r_{22}} V_c$$

Thus, the open-circuit feedback parameter,

$$h_{12} = \frac{r_{12}}{r_{22}}$$

or
$$\boxed{h_{12} = \frac{r_b}{r_b + r_c}.} \qquad (9)$$

This quantity, the fraction of the collector voltage appearing at the open-circuited emitter, is also referred to as μ_{ec}. By setting $V_c = 0$ in equation (7) we find h_{21} = short-circuit transfer function. From the open-circuit impedance representation we get,



In the collector circuit $I_c = - \frac{r_{21}I_e}{r_{22}}$.

$\therefore$ the short-circuit transfer function,

$$h_{21} = - \frac{r_{21}}{r_{22}} = - \frac{\alpha_e r_c + r_b}{r_c + r_b} = - \alpha$$

$$\boxed{h_{21} = - \alpha.} \qquad (10)$$

By setting $I_e = 0$ in equation (7) we get h_{22} = open-circuit output admittance. This is just $1/r_{22}$.

$$\therefore \boxed{h_{22} = 1/r_{22} = \frac{1}{r_b + r_c}.} \qquad (11)$$

We can therefore redraw the circuit in Fig. 4 representing the hybrid parameters as follows:

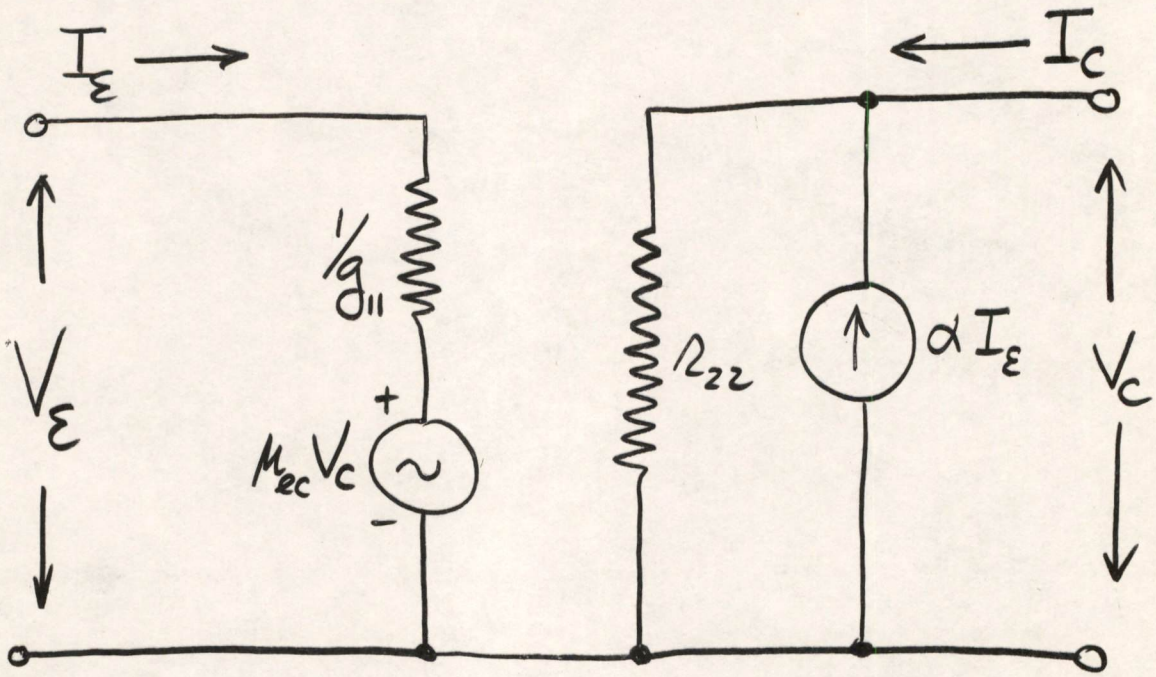


FIG. 5 - EQUIVALENT CIRCUIT FOR HYBRID PARAMETERS

$$h_{11} = 1/g_{11} \qquad h_{21} = -\alpha$$

$$h_{12} = \mu_{ec} \qquad h_{22} = 1/r_{22}$$

4.0 Early Modification of Equivalent Circuit

The measured values of r_c were found to be 1 or 2 MΩ, which is considerably below the theoretical value predicted for the equivalent-T circuit. J. M. Early of BTL resolved this difficulty by considering the change in collector space-charge width with collector voltage (now referred to as the "Early effect"). If we consider the potential diagram in Fig. 6 we see that as the collector voltage increases the effective base width decreases.

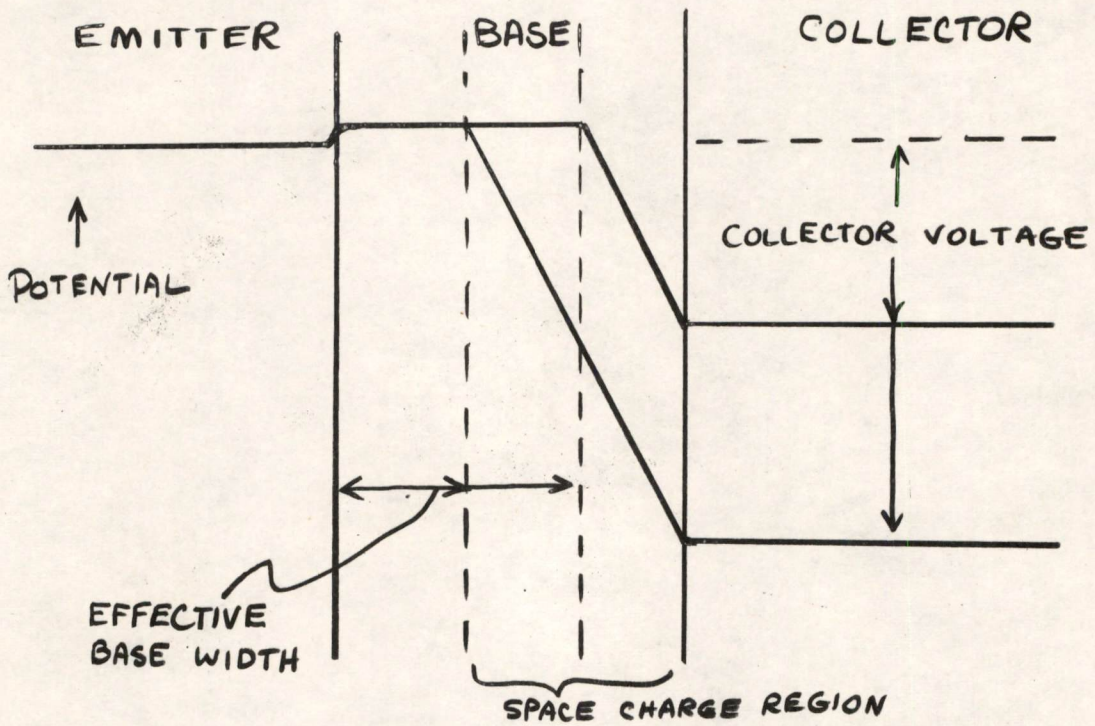


FIG. 6 - SPACE CHARGE WIDENING CAUSING BASE WIDTH TO DECREASE.

The effect of decreasing the base width is twofold: a decrease in hole-current loss by recombination of holes and electrons; and a decrease in the base impedance to hole injection by the emitter. Both of these factors tend to increase α, the current gain. Now, the open-circuit collector conductance,

$$g_c = \frac{1}{r_{22}} = \left[\frac{\partial I_c}{\partial V_c}\right]_{I_e} \approx I_e \left[\frac{\partial \alpha}{\partial V_c}\right]_{I_e} \approx 1 \text{ micromho.}$$

Thus, the low value of collector resistance is the direct result of space-charge widening or Early effect. The decrease in base width also causes an increase in base resistance but this is normally small.

The various effects mentioned above can be represented by the equivalent circuit below. The space-charge variation produces the collector resistance $1/g_c$ and the emitter voltage generator.

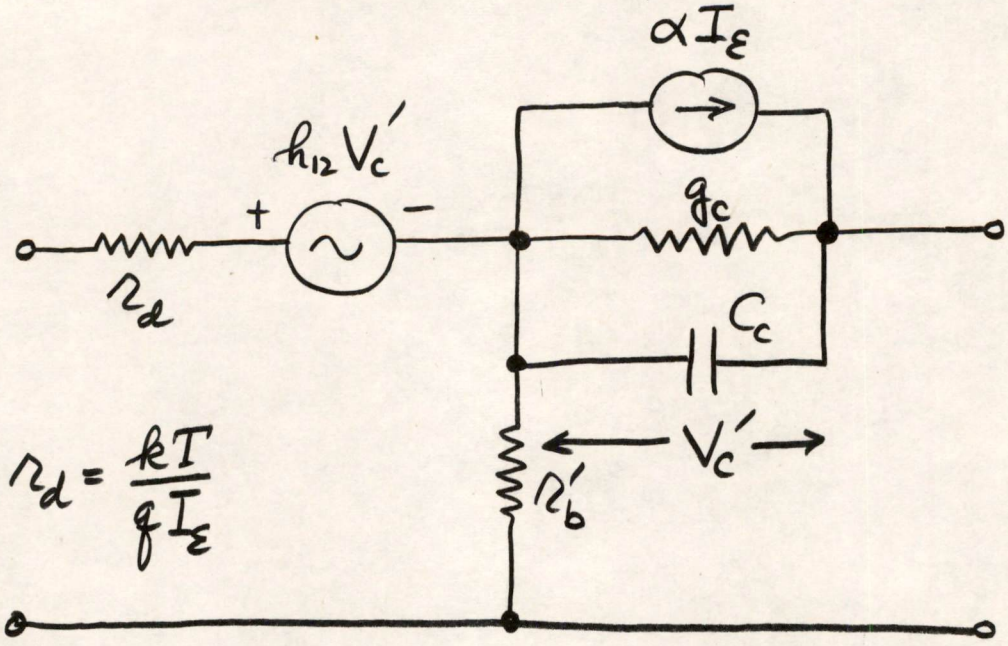


FIG. 7 - EARLY-MODIFIED EQUIVALENT CIRCUIT.

However, it is desirable to eliminate the voltage-dependent generator in the emitter. Doing this gives the equivalent circuit of Fig. 8.

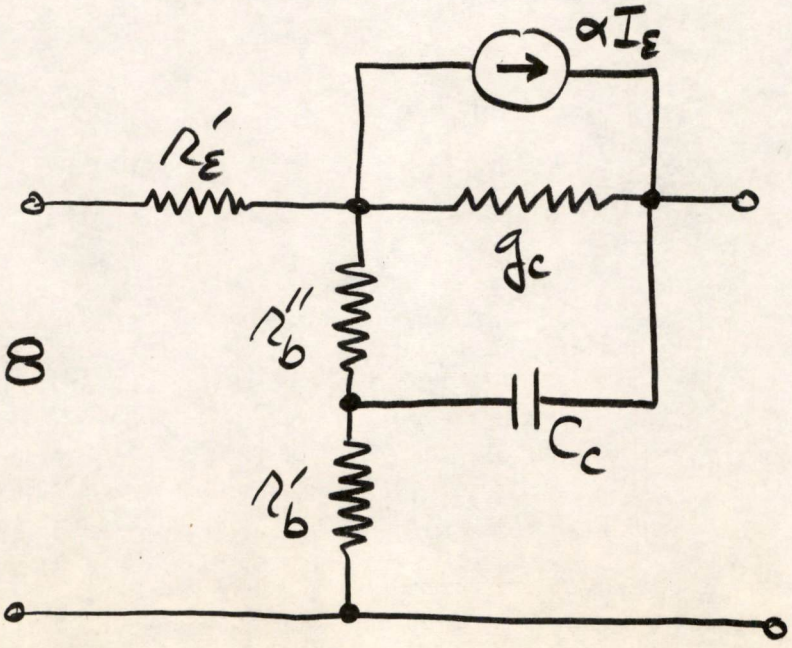


FIG. 8

The parameters in Fig. 8 are related to the previous parameters by the relations:

$$r_b'' = h_{12}\, r_c.$$

$$r_e' = r_d - (1 - \alpha)\, h_{12}\, r_c \approx \frac{kT}{2qI_e} = \frac{13\,\Omega}{I_e}.$$

r_b' = spreading resistance.

The feedback parameter $h_{12} = \frac{kT}{qw}\frac{\partial w}{\partial V_c} = \frac{25}{w}\frac{\partial w}{\partial V_c}$.

where w = effective base width.

Note that at low frequencies,

$$Z_b = r_b' + h_{12} r_c$$

while at high frequencies r_b'' is shunted by C_c and,

$$Z_b = r_b'.$$

Typical values for the parameters shown in Fig. 8 are the following for a pnp audio transistor:

$$r_b' = 300\,\Omega.$$

$$h_{12} = 4 \times 10^{-4}$$

$$r_c = 1\ \mathrm{M}\Omega.$$

$$C_c = 40\ \mu\mu f$$

$$\alpha = .98$$

$$r_b'' = h_{12} r_c = 4 \times 10^{-4} \times 10^{6} = 400\,\Omega.$$

At any frequency where $\omega C > g_c$ the effective base resistance is r_b'. For the above transistor this frequency is

$$10 \times 2\pi f C = g_c$$

$$f = \frac{g_c}{20\pi C} = 40\mathrm{KC}.$$

5.0 Equivalent Circuit for SBT

A final equivalent circuit worthy of note is a π-equivalent proposed by Philco as a characterization of the surface-barrier transistor. This is shown in Fig. 9: The parameter values are related to those previously given by the expressions below:

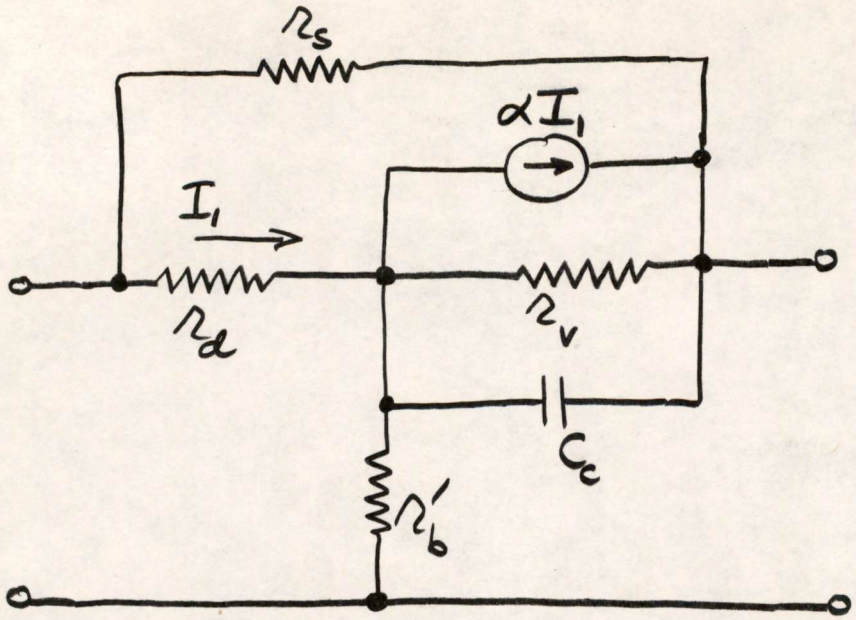


FIG. 9 - SBT EQUIVALENT CIRCUIT

$$r_d = \frac{kT}{qI_e} = r_e' + (1-\alpha)\, h_{12} r_c \,.$$

$$r_v = \left(\frac{r_d}{r_e'}\right) r_c \,.$$

$$r_s = \frac{r_d}{h_{12}} \,.$$

The various parameters required for these equivalent circuits can be obtained from sets of characteristic curves, which will be discussed in the next lecture.

Donald J. Eckl

DJE/md

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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

Subject: TRANSISTOR CIRCUITS COURSE. NUMBER 3. CHARACTERISTIC CURVES.

To: Distribution List

From: D. J. Eckl

Date: 4 August 1955

Approved: DRB
D. R. Brown

Abstract: The equivalent-T parameters can be obtained from the characteristic curves of the transistor. The collector or r_{22} characteristics provide values of r_c and α. The base characteristics give r_b. The grounded emitter curves are in general more useful since they are modified by the factor $(1-\alpha)$ in such a way as to bring out the properties of the transistor in magnified form. Punch-through and avalanche voltages are readily illustrated. In general, for switching applications these curves are more useful in specifying the over-all quality of the transistor than they are for circuit design. This would not necessarily be the case in amplifier design, however.

1.0 Grounded-Base Collector (r_{22}) Characteristics.

In Fig. 1 a typical pnp junction collector-characteristic family is shown. This is a plot of collector (or output) voltage against collector current for different values of I_e. There are three general regions into which the characteristics are divided as shown: Cutoff, Active, Saturation. These are also frequently referred to as Regions I, II, and III. In the Off Region, $I_e < 0$ and both emitter and collector are high impedances. In the active region $I_e > 0$ and r_c is high. This is the normal operating region for the transistor. The emitter is a low impedance. In the saturation region both r_c and r_e are low impedances.

Figure 2 shows the complete set of characteristics with the important parameters indicated. The slope of the curves,

$$\left|\frac{\partial V_c}{\partial I_c}\right|_{I_e} = r_c + r_b \approx r_c.$$

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

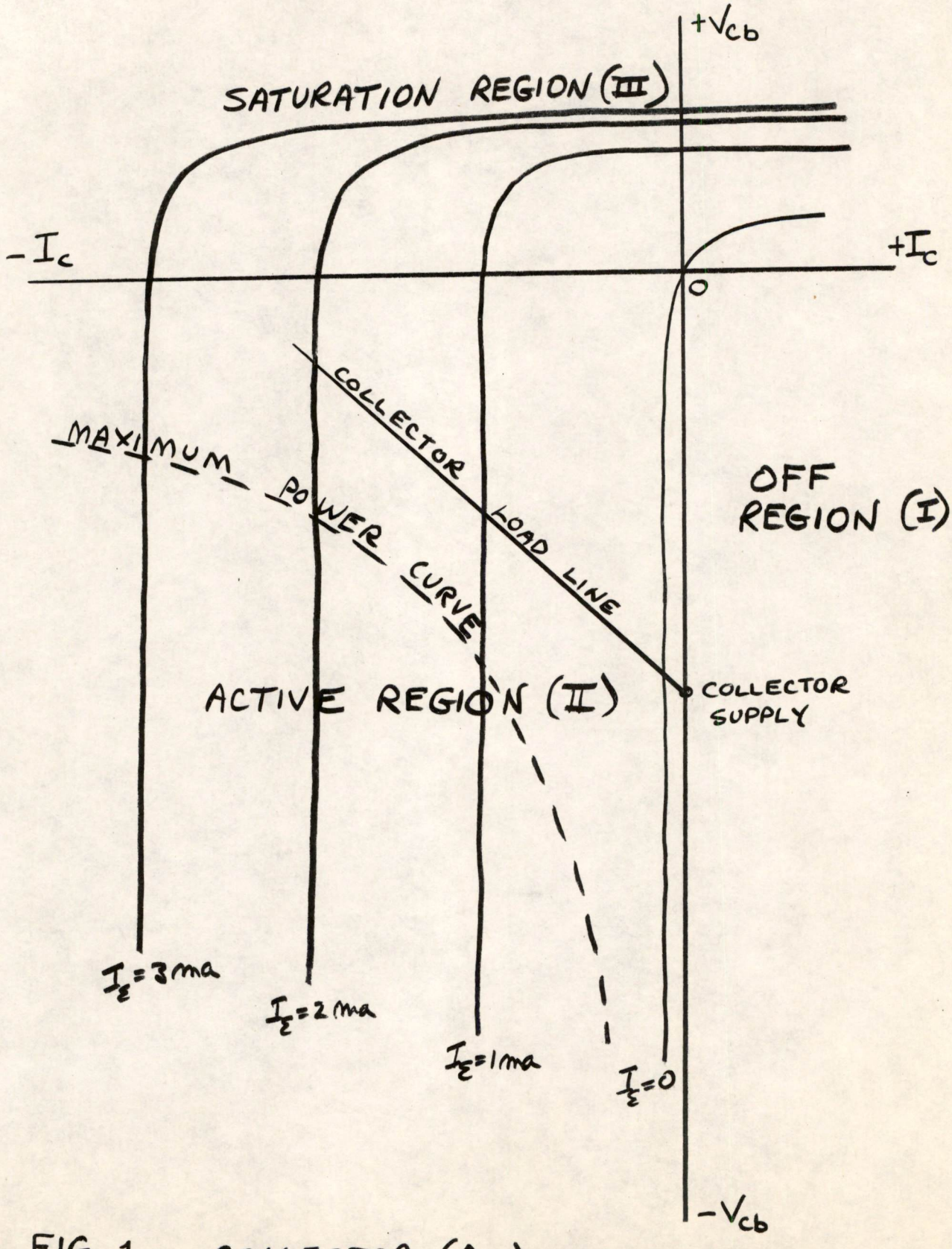

FIG. 1 - COLLECTOR (R_{22}) CHARACTERISTICS

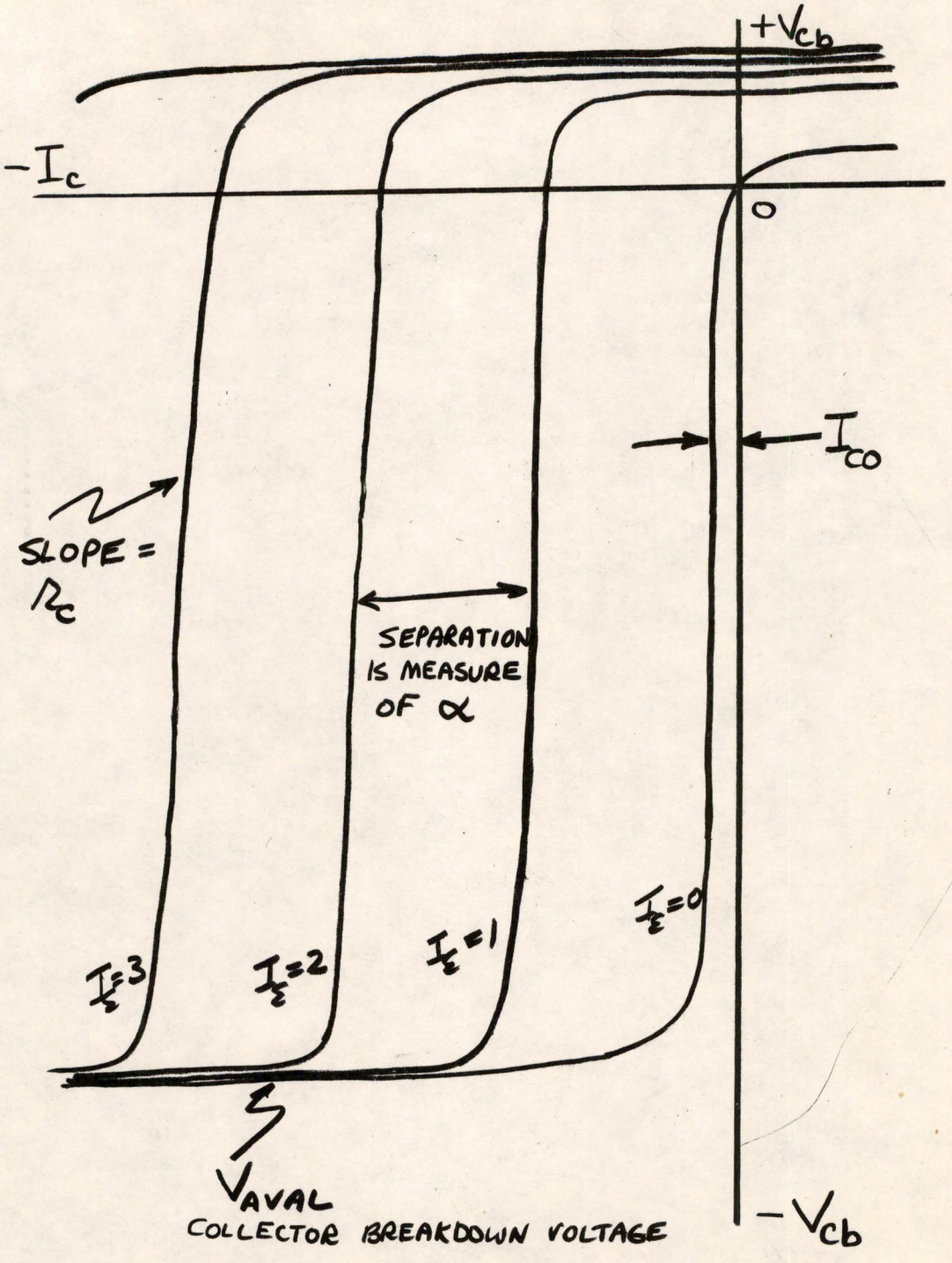

FIG. 2 COLLECTOR CHARACTERISTICS. (GROUNDED-BASE.)

In both the saturation region and the avalanche region the value of r_c is low. The avalanche voltage V_{aval} which is the maximum collector-to-base voltage will be discussed later. The spacing of the curves is a measure of α since

$$\left|\frac{\partial I_c}{\partial I_e}\right|_{V_c} = \alpha.$$

I_{co} is the cutoff leakage collector current. Note also that the collector voltage must go positive to saturate the transistor.

2.0 Grounded-Base r_{12} Characteristics.

The base or r_{12} characteristics are shown in Fig. 3.

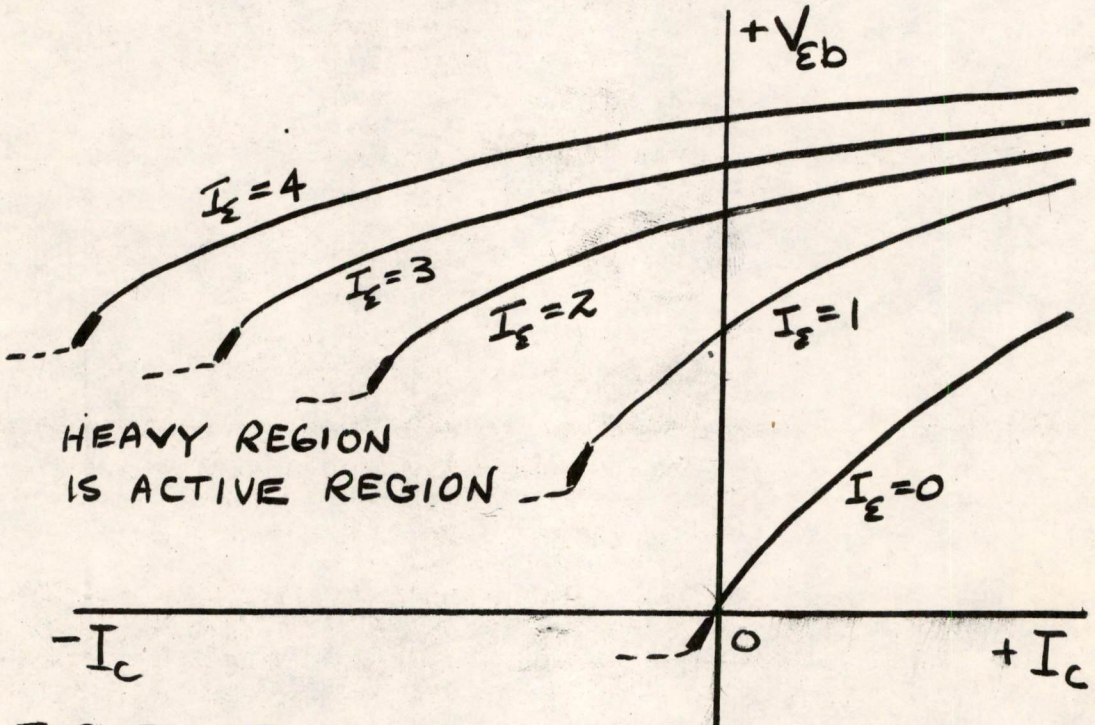

FIG. 3 - BASE CHARACTERISTICS.

The slope of these curves is

$$\left|\frac{\partial V_e}{\partial I_c}\right|_{I_e} = r_b = r_b' + h_{12}r_c.$$

Thus in the saturation region where r_c becomes small the value of r_b becomes smaller than the active r_b. In the avalanche region where r_c becomes low the base resistance will be low as shown by the dotted lines.

3.0 The Grounded-Emitter Circuit.

Suppose we consider the equivalent-T circuit with the emitter grounded as shown in Fig. 4.

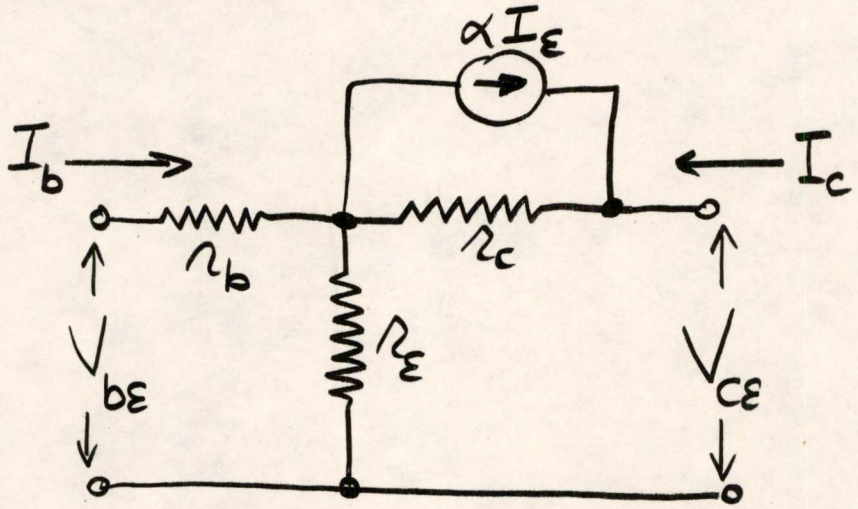

FIG. 4 - GND-EMITTER EQUIVALENT-T.

The current-voltage relations are:

$$V_{be} = (r_b + r_e)I_b + r_eI_c.$$

$$V_{ce} = r_eI_b + \alpha I_e r_c + (r_c + r_e)I_c.$$

But, $$I_e = -I_b - I_c.$$

$$\therefore \quad V_{ce} = (r_e - \alpha r_c)I_b + \left[r_e + (1-\alpha)r_c\right]I_c.$$

The grounded-emitter parameters are the following:

$$r_{11_e} = r_b + r_e.$$

$$r_{12_e} = r_e.$$

$$r_{21_e} = r_e - \alpha r_c.$$

$$r_{22_e} = r_e + r_c(1-\alpha).$$

The grounded-emitter short-circuit current gain is,

$$\alpha_{ce} = \frac{r_{21_e}}{r_{22_e}} = \frac{\alpha r_c - r_e}{(1-\alpha)r_c + r_e} \approx -\left(\frac{\alpha}{1-\alpha}\right) = -\beta.$$

We can now draw an equivalent circuit for the grounded emitter configuration in terms of I_b, the input current. This is shown in Fig. 5.

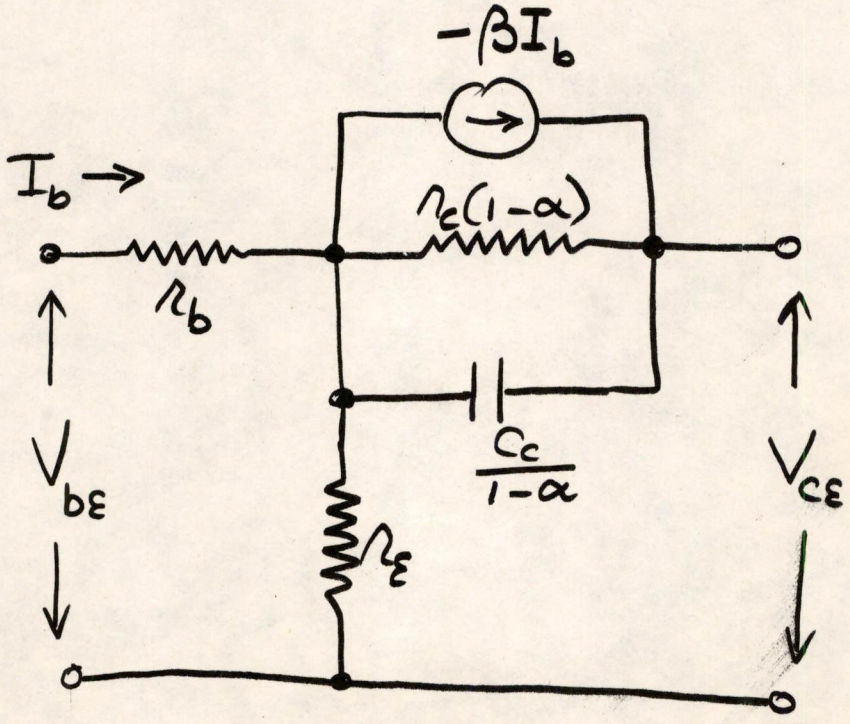

FIG. 5 - GROUNDED-EMITTER EQUIVALENT-T.

The grounded-emitter collector capacity can be evaluated by considering the collector impedance

$$1/Z_c = g_c + j\omega C_c.$$

Z_c would enter into all expressions above in the same way as r_c and would therefore be multiplied by $(1-\alpha)$ in the grounded-emitter circuit. This would give

$$\frac{1}{Z_c(1-\alpha)} = \frac{g_c}{1-\alpha} + j\omega\frac{C}{(1-\alpha)}.$$

Therefore the capacity is effectively multiplied by the factor $(1/1-\alpha)$ which means an increase of 9-50 times.

A more rigorous treatment can be made using the circuit of Fig. 6. The equations given are straight forward. Small letters denote internal currents.

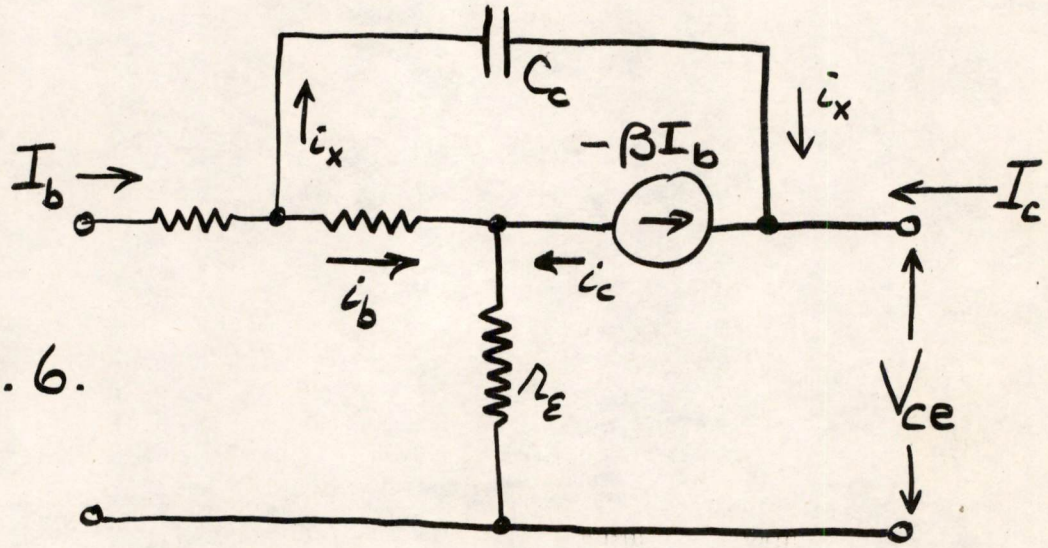

FIG. 6.

We would like to obtain a relationship for collector-voltage rise in terms of external currents and C_c.

$$i_c = \beta i_b.$$

$$I_b = i_b + i_x.$$

$$I_c = i_c - i_x.$$

$i_x \doteq -C_c \frac{dV_c}{dt}$, since the collector voltage appears largely across the collector junction and therefore across C_c.

$$\therefore I_c = \beta i_b + C_c \frac{dV_c}{dt}.$$

$$I_c = \beta(I_b - i_x) + C_c \frac{dV_c}{dt}.$$

$$I_c = \beta(I_b + C_c \frac{dV_c}{dt}) + C_c \frac{dV_c}{dt}.$$

$$I_c = \beta I_b + \beta C_c \frac{dV_c}{dt} + C_c \frac{dV_c}{dt}.$$

$$C_c(1+\beta)\frac{dV_c}{dt} = I_c - \beta I_b.$$

or,

$$\frac{dV_c}{dt} = \frac{I_c - \beta I_b}{C_c(1+\beta)} = \frac{I_c - \beta I_b}{C_c/(1-\alpha)}.$$

Thus the collector capacity is effectively multiplied by the factor $1/(1-\alpha)$ in the grounded-emitter configuration.

4.0 Grounded-Emitter Collector Characteristics.

The grounded-emitter output characteristics are shown in Fig. 7. These are curves of V_{ce} against I_c for various values of I_b. The slopes of the curves are

$$\left|\frac{\partial V_{ce}}{\partial I_c}\right|_{I_b} = r_c(1-\alpha).$$

The separation between the curves is a measure of the current gain, that is,

$$\left|\frac{\partial I_c}{\partial I_b}\right|_{V_{ce}} = \frac{\alpha}{1-\alpha} = \beta.$$

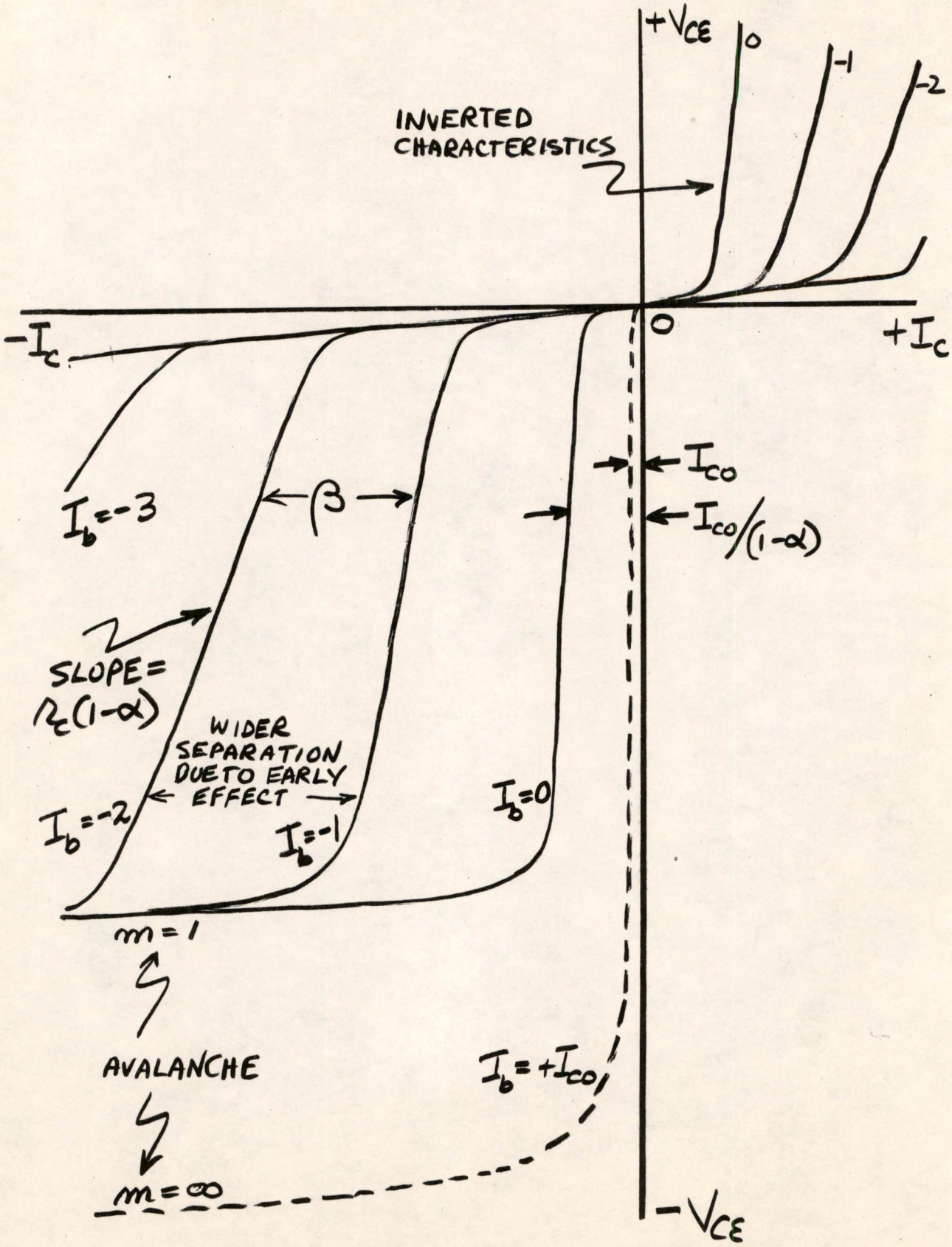

FIG 7. - GROUNDED-EMITTER OUTPUT CHARACTERISTICS

We have already seen that the Early effect causes α to increase with collector voltage. This appears in the grounded-emitter curves as a widening at higher voltages.

The leakage current is now $I_{co}/1-\alpha$. The grounded-base leakage current I_{co} will appear for a positive base current equal to I_{co}.

The inverse characteristics are obtained in the first quadrant by using a positive collector voltage. The collector acts as an emitter in this region.

5.0 Avalanche Breakdown.

In the collector space charge region there is an electric field which accelerates the minority carriers towards the collector. As the collector voltage is increased it is possible for a carrier to gain sufficient energy from the field to produce secondary carriers. A multiplication ratio m can be defined as the ratio of total carriers to primary carriers. We can then define the current gain α as

$$\alpha = m\alpha_0.$$

Where α_0 is the low voltage α. In the grounded-base configuration when $m = \infty$ the current gain becomes infinite and the collector breaks down. This is somewhat similar to an ionization breakdown in a gas. The breakdown voltage is shown as V_{aval} in Figure 2.

In the grounded-emitter configuration, however, the current gain is given by,

$$\beta = \frac{m\alpha_0}{1-m\alpha_0}$$

Therefore, breakdown occurs at the point where $m\alpha_0 = 1$ which will be at a much lower voltage.

6.0 Punch-Through Voltage.

In some cases, particularly in narrow base, high frequency transistors, the emitter-collector impedance breaks down for another reason before avalanche occurs. This type of breakdown is known as punch through. We have already discussed how the space charge region at the collector causes the base region to become narrower. As V_c

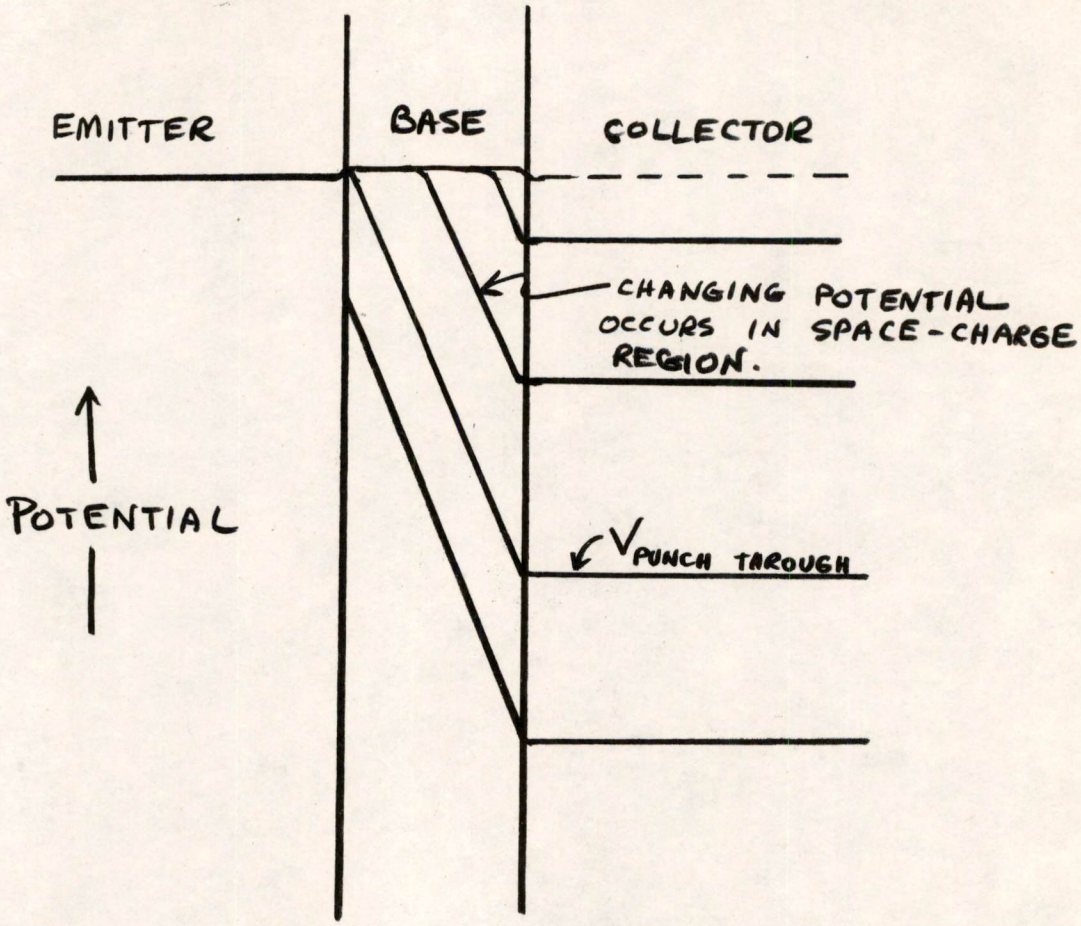

FIG. 8 - PUNCH-THROUGH VOLTAGE

increases the space charge region increases and base width decreases. Eventually a collector voltage is reached where the space charge region extends to the emitter. This is the punch-through voltage. Beyond this point the collector-emitter impedance is low and emitter voltage follows collector voltage.

7.0 Grounded-emitter r_{12} Characteristics.

These characteristics are shown in Fig. 9.

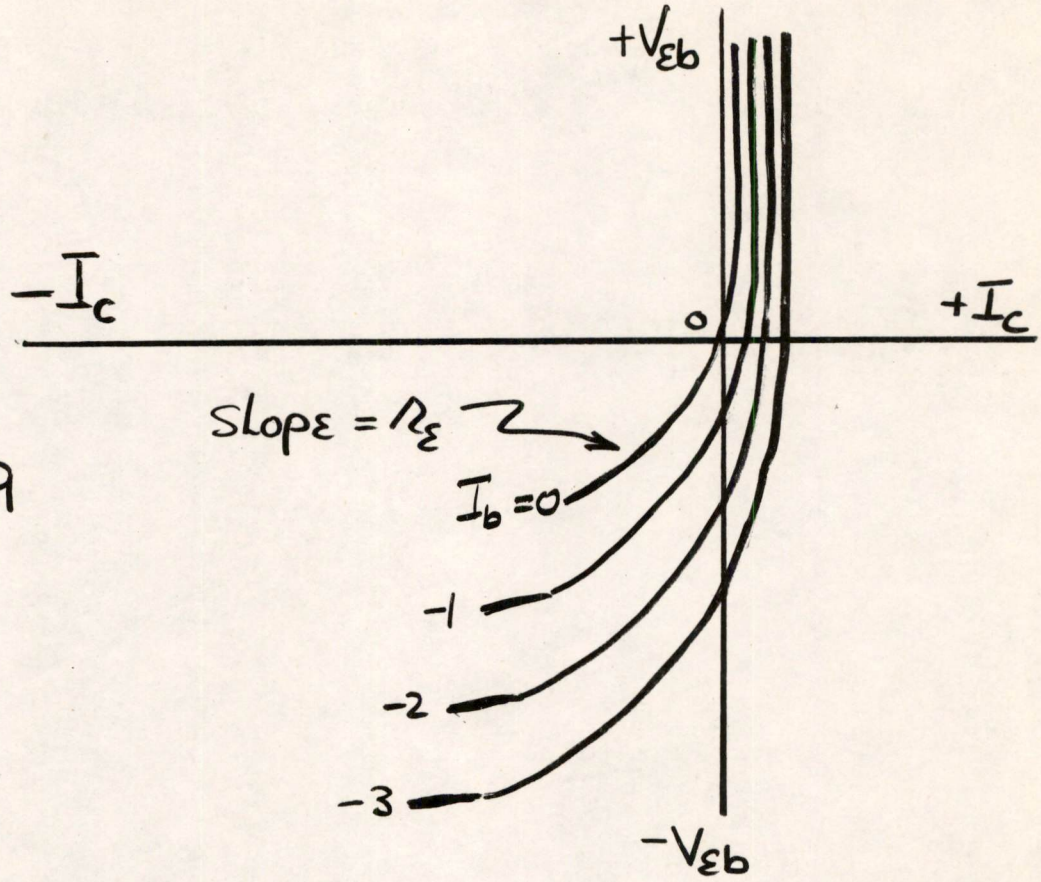

FIG. 9

The slopes of these curves give r_e.

$$\left|\frac{\partial V_b}{\partial I_c}\right|_{I_b} = r_e = \frac{kT}{qI_e} - (1-\alpha)h_{12}r_c.$$

In the saturation region where r_c is small the curves are approximately the theoretical $25/I_e$ ohms. In the active region the value is less.

The next part of this series will cover grounded-base, grounded-emitter, and grounded-collector amplifiers.

Signed: D. J. Eckl
D. J. Eckl

DJE/dg

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Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: MOD III CURRENT CALIBRATOR

To: D. R. Brown

From: R. A. Pacl, Jr.

Date: August 9, 1955

Approved: W H Pickering
for J. B. Goodenough

Abstract: The Mod III Current Calibrator is a rack panel unit of test equipment designed to measure amplitudes up to 10 volts of pulses having a duration of at least two microseconds. Pulses from a low impedance source (less than 100 ohms) can be measured with a total error of less than .25 percent without any special precautions.

Introduction

The Mod III Current Calibrator represents an improved null-type circuit* for more accurately measuring the instantaneous voltage of recurrent waveforms having negligible change of voltage during the time the Calibrator is gated "on". This is particularly useful for rectangular pulses, but equally applicable for other waveforms, down to and including direct current. Besides increased accuracy, one of its major advantages is the fact that as a null-type instrument, the operation is simplified to nulling the output square-wave signal displayed on the scope and reading a Helipot dial (which is calibrated in volts.) This is desirable from an operational viewpoint.

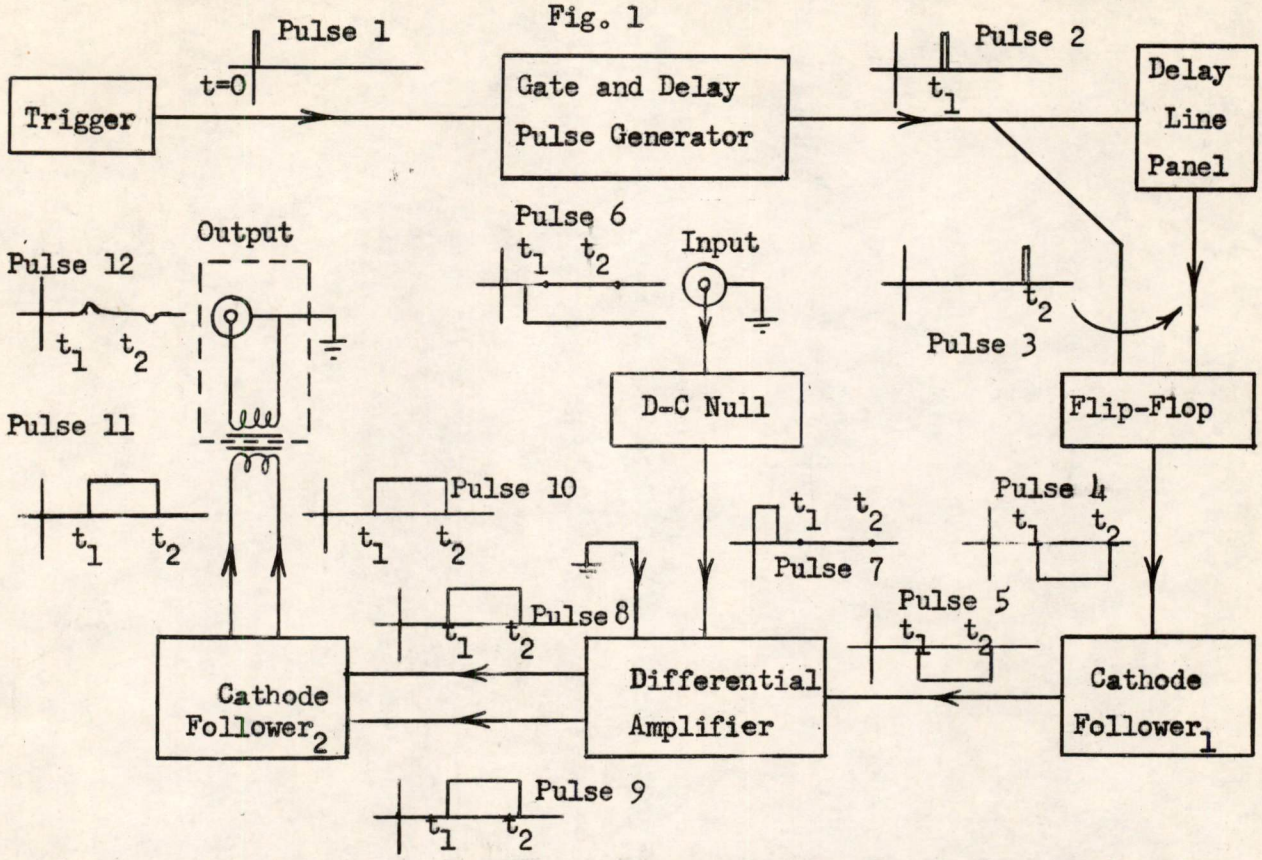
Block Diagram

Figure 1 shows the block diagram of the Calibrator. The components not enclosed by the dotted line are external to the unit.

*The basic idea was hashed out by R. Pacl and J. Childress.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Fig. 1



The trigger is derived from some pulse synchronized with the waveform to be calibrated. The Gate and Delay Pulse Generator and Delay Line Panel are both Burroughs units. The Flip-Flop is the Mod II MTC Hi-Speed type. The input and output signals of the various units are shown in Fig. 1, beginning with the trigger signal (PULSE 1) which is arbitrarily assumed to begin at time t=0. This drives the Gate and Delay Pulse Generator whose function is to provide an output (PULSE 2) delayed by a time t_1, variable from 2 to 80,000 μ seconds. PULSE 2 simultaneously sets the Flip-Flop and drives the Delay Line Panel. The latter generates a signal (PULSE 3) which is used to re-set the Flip-Flop after a time interval, t_2, variable from .05 to 1.9 μ seconds with respect to t_1. These three units in toto provide a gating signal (PULSE 4) whose initiation and duration are chosen according to the pulse to be calibrated. Cathode Follower$_1$ transforms the high impedance output of the Flip-Flop to a low impedance capable of gating the Differential Amplifier.

The Input pulse (PULSE 6) has been drawn arbitrarily as a negative (referred to ground) rectangular pulse having a constant amplitude. All that is actually required is that the amplitude remain essentially constant between t_1 and t_2, which time corresponds to the gating of the Differential Amplifier. The d-c Null in series with the signal provides an accurately known d-c voltage of polarity opposite to but of magnitude the same as the Input pulse. In consequence, the Differential Amplifier sees two ground levels when it is gated on, one being the addition of bucking voltages (PULSE 7) and the other a natural ground reference. The output of the Differential Amplifier (PULSES 8 & 9) is converted from high impedance to low impedance by Cathode Follower$_2$. The output transformer provides voltage amplification and a single-ended output which is displayed on a scope.

Controls and Operation

All controls, adjustments, replacements and connections are located on the front panel (see Fig. 2) with the exception of the power cable and output transformer. The flip-flop is mounted at the upper left-hand corner, and the set and output connections made by BNC connectors. The three remaining BNC connectors are labelled as follows:

OUT - The output from the pulse transformer to the scope.
GATE - The input to cathode follower from the flip-flop output.
IN - The input to the difference amplifier grid through the d-c Null circuit for the pulse to be calibrated.

Reading from left to right along the bottom of the panel, the controls read:

BAL. - A pushbutton switch which grounds the difference amplifier input grid.
POL. - A two position toggle switch which reverses the polarity of the d-c voltage in series with the input signal.
BAL. AMP. - A 10-turn Helipot which is used to balance the difference amplifier prior to measuring the input pulse.

Above the BAL. AMP. control is a large Helipot dial marked

CALIBRATE - A 10-turn Helipot reading 10 volts at maximum clockwise position, indicating the magnitude of the input pulse at null.

To the right of the CALIBRATE dial is a screw driver adjustment marked

ZERO GALV. - A potentiometer which is turned to give a zero reading on the galvanometer.

Next comes the galvanometer. In the upper right-hand corner of the panel is a switch marked

ON-OFF - A toggle switch controlling the B+, filament voltage and protective relay.

At the bottom right-hand corner is a switch marked

GALV. SENS. OFF-LO-HI - A lever type switch connected with the ZERO GALV. potentiometer, which sets 10 volts across the CALIBRATE Helipot when the galvanometer is zeroed.

The cover plate under the galvanometer houses the dry cells, and the mercury standard cells. Before discussing the operation of the calibrator, there are a few precautions which should be observed. NEVER push the galvanometer sensitivity switch through the LO to HI range without stopping to observe the deflection of the galvanometer in the LO position. If the deflection is more than 2 divisions off zero, readjust the ZERO ADJ control to bring the galvanometer to zero. If this doesn't succeed, there is either something wrong or the batteries have deteriorated. NEVER remove any batteries and press the GALV SENS switch. Failure to observe these precautions may ruin the galvanometer movement. The remainder of the controls may be adjusted at random by knob-twiddlers without hazard to person or property.

The first step in setting up the calibrator is obviously to connect the power cable to the male plug on the back of the panel. The ON-OFF switch applies B+ and filament voltage to the calibrator, and also energizes the relay which switches in the batteries. If the galvanometer is zero-adjusted immediately, a drift will be noticed upon subsequent checking. This is due to the fact that the batteries used in the d-c NULL circuit gradually polarize after the load is applied with a concommitant decrease in terminal voltage. This will necessitate frequent rechecking and zero-adjustment until a steady state is reached. It is advisable to check the galvanometer zero immediately prior to using the calibrator in order to minimize any error due to voltage drift.

The Flip-Flop 0 OUT is normally connected to the GATE input with a short cable. This requires that the output from the Gate and Delay Pulse Generator be connected to the SET 1 Flip-Flop input, and the output from the Delay Line Panel to the SET 0 Flip-Flop input. (c.f. Fig. 1). The Delay Line Panel determines the duration of the gating pulse and for input pulses longer than 3 or 4 μ seconds, should be set for maximum delay (1.9 μ seconds) or as long as is necessary to minimize the transient portion of the null output. The Gate and Delay Pulse Generator is set to provide the desired delay between the initiation of the input pulse and the gating pulse. For short input pulses, (less than 3 μ seconds) it may be necessary to replace the Gate and Delay Pulse Generator with a Delay Line Panel to provide a shorter minimum delay. The two remaining connections, IN and OUT, are connected respectively to the input pulse source and the scope. In the event that maximum accuracy is required, it must be borne in mind that even with low-impedance voltage sources, the shunting effect of the calibrator is not entirely negligible. At present, it presents a complex impedance which is essentially resistive for pulses of short duration. The magnitude of this resistive component is approximately 5K but depends on the CALIBRATE setting. For lower frequencies the quadrature component is capacitive and in series with the 5K. For use with Core Drivers, it is customary to insert a known resistance in series with the core and measure the IR drop across it. To facilitate conversion of voltage to current, integral values of resistance are used, particularly 5, 10 and 20 ohms. By using actual resistances of 5.005, 10.02 and 20.08 ohms, the shunting of the calibrator will reduce these values to 5, 10 and 20 ohms, respectively. Since these calibrating resistances

must be checked on a bridge anyhow, this induces no hardship. With regard to the output, any scope having a bandpass of several megacycles will suffice. Since the pulse and gating transients which occur in the output are unwanted signals, it is not particularly advantageous to display them undistorted. The bandpass and transient response should be good enough to show a clearly defined null, however. The Tektronix 514 functions satisfactorily as a null detector.

The pushbutton switch marked BAL is used in conjunction with the BAL. AMP. control to set the null on the scope initially. This functions to balance the differential amplifier by grounding the input grid and shifting the bias on the reference grid. After a null has been obtained, the BAL. AMP. control should be locked in position and not disturbed until the Differential Amplifier is rebalanced. The stability of the Differential Amplifier depends upon a number of factors, viz., the length of the warm-up time, the d-c mains, the mechanical shock to which the calibrator may be subjected, and the characteristics of the particular tubes used. It is advisable to check the balance immediately prior and subsequent to calibrating the input pulse. This offers no guarantee that the balance won't shift during use, but it is reasonable to assume this if the balance shows no change.

The POL. switch indicates the polarity of the d-c voltage in series with the pulse. Hence, the reading will be opposite to the polarity of the incoming pulse.

The CALIBRATE control is a 10 turn Helipot with a linearity of .05 percent of maximum output voltage. In order to achieve maximum accuracy, it is necessary to use the Helipot near maximum resistance, i. e., to calibrate voltages on the order of 10 volts. In the event that smaller voltages must be calibrated and accuracy cannot be sacrificed, two possibilities present themselves. The circuitry could be revised to give lower full-scale voltages, say 5, 2, or 1, or the calibrator could be checked against a K-2 potentiometer. The former possibility will be discussed under Circuit. The latter, tho more tedious, has much to commend it. The K-2 can be used for checking the linearity over the whole range, and a calibration chart drawn up to cover some or all of the range. Since the K-2's range is limited to 1.6 volts, it would be necessary to add standard cells in series for higher CALIBRATE voltages. This method has two advantages, in that the accuracy of the K-2 is very good, and one calibrator could be used to cover a greater range with greater accuracy. However, the resolution at the lower end of the dial is not as good percentage-wise, i.e., a fixed resolution error of say 1 division would be .1 percent at full scale, but 1 percent at one-tenth of full scale.

The ZERO GALV. control, the galvanometer, and the GALV SENS switch are all part of the d-c NULL (cf. Fig. 1) circuit, which is basically a potentiometer. (See CIRCUIT). The ZERO ADJ control determines the magnitude

of the voltage appearing across the CALIBRATE Helipot such that $10.00 \pm .005$ volts will appear across the Helipot when the galvanometer reads zero with the GALV SENS switch in the HI position (maximum sensitivity).

The removable cover encloses the batteries used in the potentiometer circuit. The larger taped unit consists of 8 Burgess 5R dry cells, series connected to give 12 V. The phenolic cylinder in the lower right-hand corner of the box houses 8 Mallory RMIR Mercury cells used for the standardizing voltage. NOTE: The case of the RMIR is positive, and must be inserted with the case contacting the rear terminal. Failure to observe this precaution could result in damage to the cells and galvanometer.

The remaining dry cell is used in the amplifier balancing circuit. (See CIRCUIT).

Display

The 514 Tektronix scope used to display the output was operated at maximum sensitivity, viz., 30 mv/cm. When the calibrator has been nulled, the output appears as a small hump of arbitrary polarity, followed by a gently sloping line and another hump of polarity opposite to the first one. The humps are due to the common-mode component of the output, caused by the gating pulse. The output transformer removes a large part of this but not all.

As the display gradually moves off null, the gently sloping portion goes either positive or negative. The humps are simultaneously distorted and as the off-null signal is increased, they soon lose their identity.

The humps may be rendered symmetrical by adjustment of the trimmer capacitors C_8 and C_9 in the plate circuit of V_2. This helps somewhat in nulling the calibrator.

Circuit

The Burroughs units are described in R-215. The Flip-Flop used in the calibrator is the MTC Flip-Flop Mod II. The circuit schematic is shown in Fig. 4. It is triggered by a positive .1 μ second input pulse of between 20 and 40 volts amplitude. The output levels are + 10 and - 30 V. For further information, the reader is referred to page 18 of the Plug-In Manual and Engineering Note E-543.

The output of the Flip-Flop is a-c coupled to V1, both sections paralleled. The cathodes are normally +25 volts, cutting V-2 off. The negative pulse from the Flip-Flop cuts V1 off, permitting the cathodes of V2 to drop to equilibrium bias. With the BAL switch depressed, the grid

of V2A is held at ground, and the bias on the grid of V2B is varied by the BAL AMP control to give a null. Irrespective of the inequalities between the two sections, the important point is that with the grid of V2A at ground, the output is zero. If the BAL switch is released, and the input pulse balanced by the CALIBRATE control to produce a null, then we may assume that the grid of V2A is again at ground, and that the algebraic sum of the input pulse and the d-c NULL is zero, or their magnitudes are equal. The outputs of V2A and V2B are coupled to the cathode followers V3A and V3B. The differential output of the cathode followers is amplified and converted to a single ended output by the output transformer T_1. This transformer utilizes a Ferramic H core (1/4 ID x 5/8 OD x 3/8 HIGH) coated with silver conducting paint as an interwinding shield to provide electrostatic shielding. (See Parts List). The common mode component of the signal would otherwise couple capacitively into the scope and swamp the null signal because of its magnitude.

There are transients in the null signal which arise because of the assymmetry of the two halves of the Differential Amplifier and Cathode Follower$_2$. The amount of effort required to render both halves symmetrical would be prohibitive. The addition of the two trimmer capacitors in the plates of V2 represents a minimum attempt. In some instances, they have caused considerable transient reduction by careful balancing.

Decoupling filters are used in all voltage leads to reduce the effect of line transients. There has been no evidence of trouble in this respect.

The potentiometer circuit is typical. The CALIBRATE Helipot is carefully measured on a Wheatstone Bridge and a series resistor (R1), wound to this value multiplied by 0.0836. The current through them is adjusted for a voltage drop of 10.836 volts, 10.000 of which appear across the Helipot. This voltage is compared with the 10.836 volts developed by the mercury cells, which can be initially calibrated within .01 percent and which will retain their calibration within .05 percent over a period of several months. Since essentially no load is placed upon the mercury cells, their voltage will remain relatively constant independent of temperature. (The output will be 10.836$\pm$.002 from 60° to 100°F.) The galvanometer will easily resolve 1 millivolt, or .01 percent of the voltage across the Helipot.

It will be noticed that the output of the potentiometer is not applied directly in series with the input pulse, but rather transferred to a capacitor through two isolating resistors. This has a dual function. It permits bypassing the potentiometer to ground, thereby eliminating the shielding which would otherwise be required and it reduces the capacitive shunt load on the pulse source.

There are a number of circuit modifications which suggest themselves in the interest of greater accuracy. For smaller pulse amplitudes, a lower resistance Helipot could be used in series with a fixed resistor to replace the standard 10K Helipot. This could be done as a physical replacement, or the Helipots could be ganged together and alternately switched

into the circuit. The feasibility of ganging more than two Helipots is open to conjecture. It would also be possible to devise a switching arrangement similar to the one used in the Deka-Pot. This would involve switching the Helipot into various positions in a decade attenuator, the first significant figure of the reading being determined by the position occupied in the attenuator. Needless to say, the most obvious method of obtaining greater accuracy is to obtain better Helipots. This can be done, but the best linearity available would only result in an improvement of 200 percent. The use of a decade-switching attenuator with the present Helipot would result in 1000 percent improvement, at substantially reduced cost.

Conclusion

The over-all accuracy was stated to be better than .25 percent. This assumes that the calibrator is used for voltages in excess of 5 volts, or the upper half of the dial. At the 5 volt setting, the possible error in the Helipot would induce at most .1 percent error. The drift of the mercury cells, the sensitivity of the galvanometer and the resolution of the scope could all contribute another .07 percent independent of the Helipot setting. It should be pointed out, however, that for smaller pulses, the scope resolution occupies a greater proportion of the error.

For high impedance voltage sources, the resistive and capacitive shunting may introduce an error, but the resistive portion can be calculated and compensated for.

If accuracy were paramount, it would be possible to halve the .25 percent error previously quoted, but this would require several modifications as well as the utmost care in calibration and operation.

Robert A. Pacl, Jr.

RAP:m
Distribution: Group 63 Staff
Drawings: A-62286, Fig. 2
A-61569, Fig. 3
A-55281, Fig. 4
A-61571, Parts List

A-62286

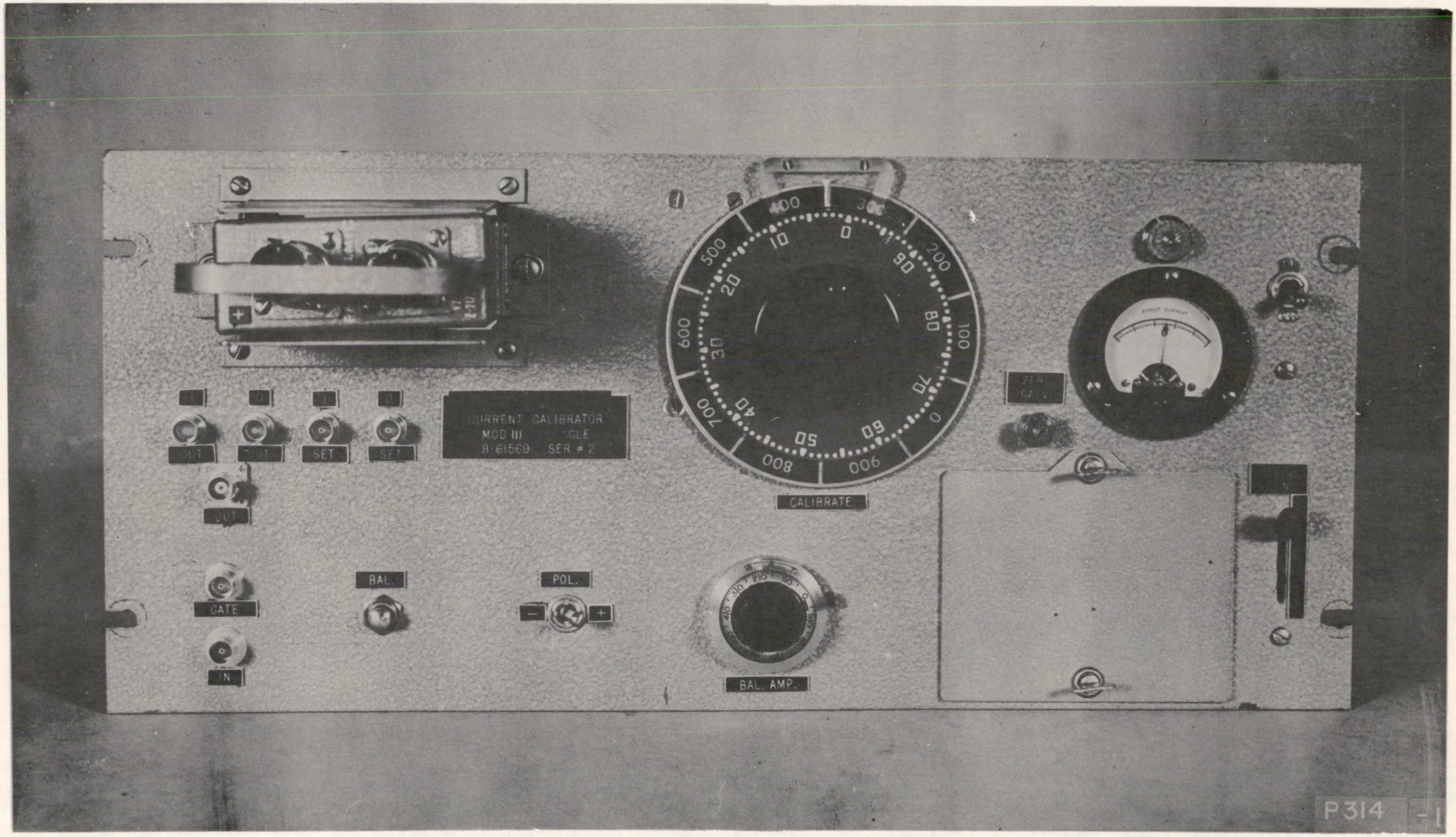


FIG. 2

CURRENT CALIBRATOR

MOD III

C-61569-I

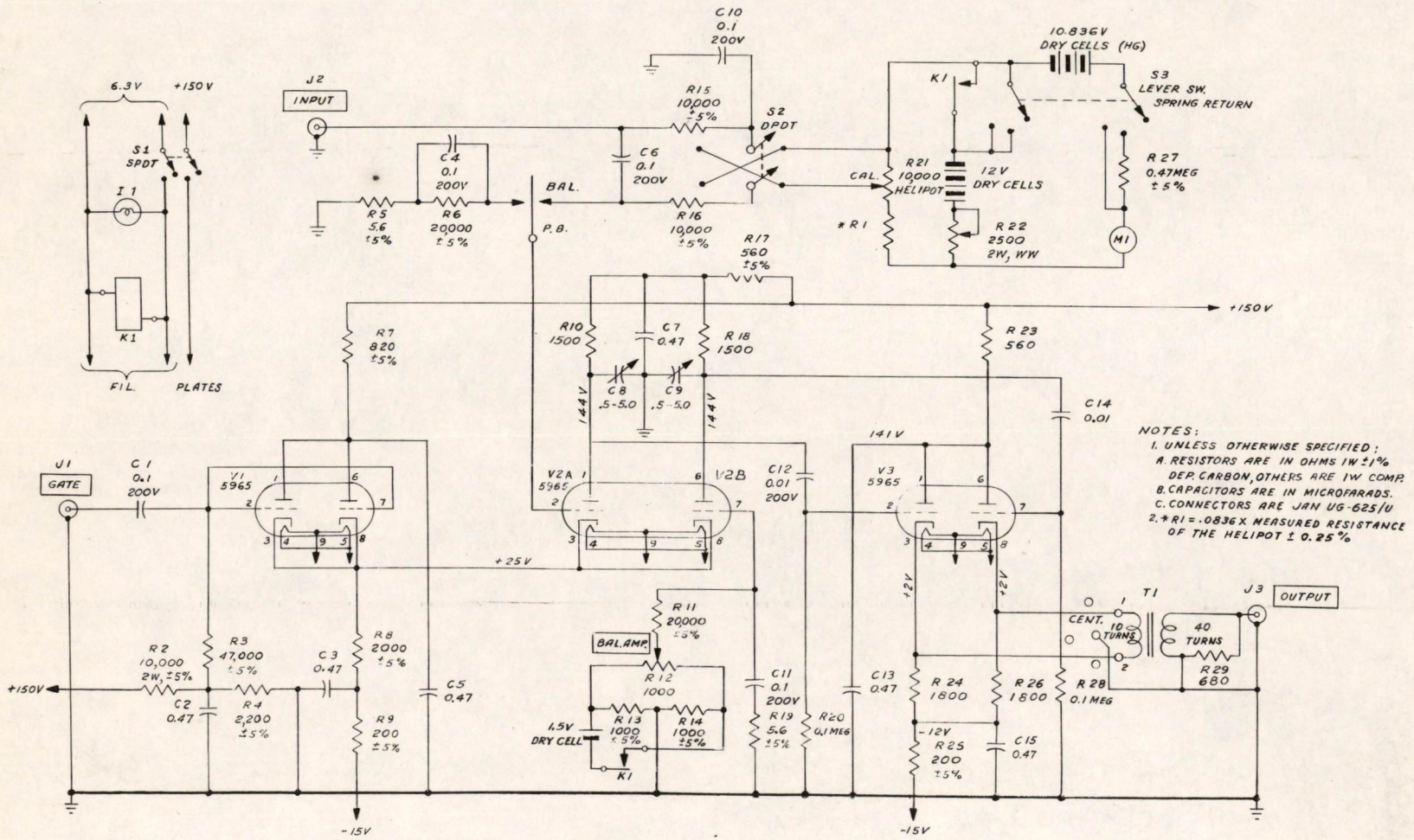
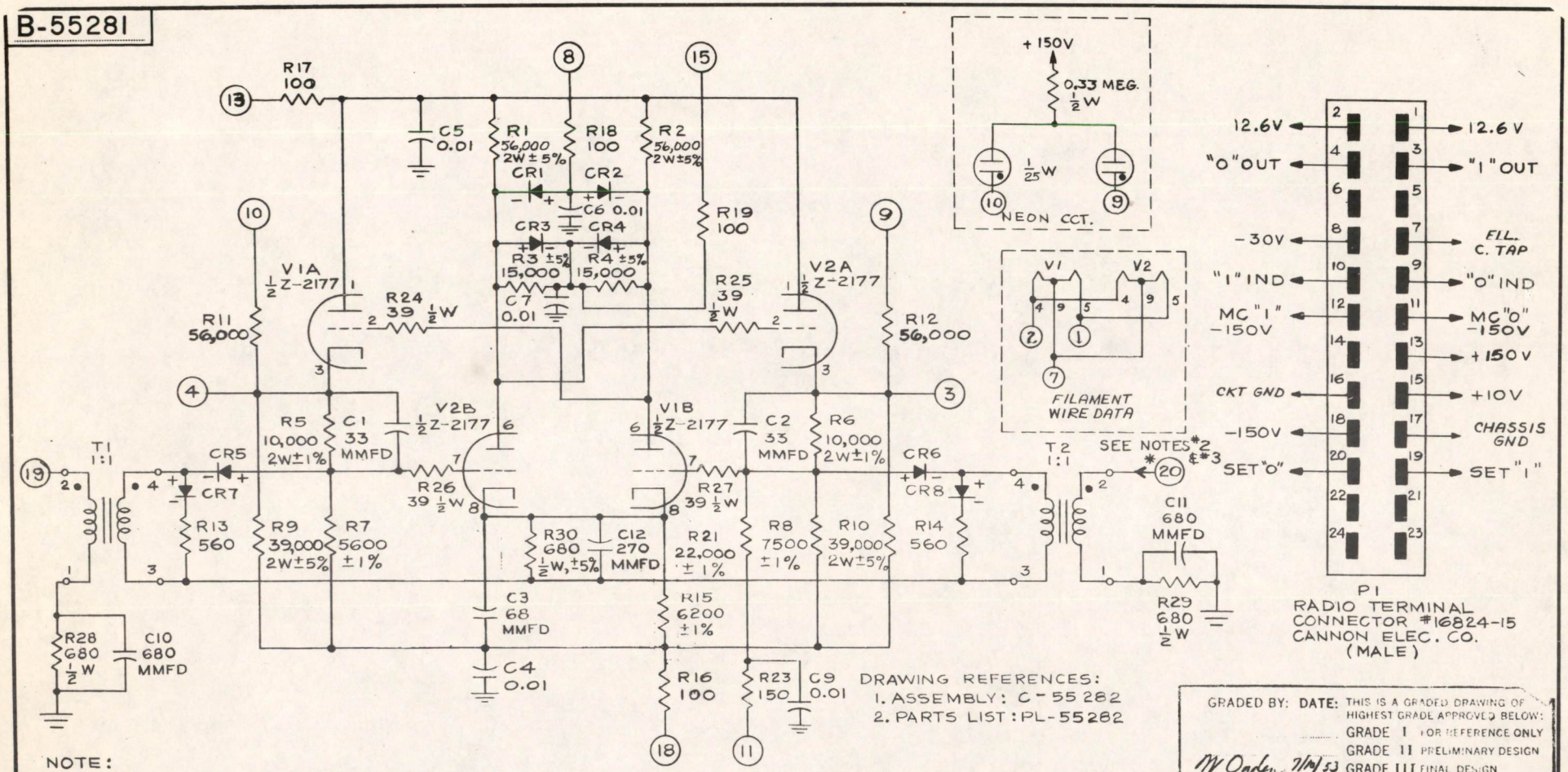


FIG. 3

CIRCUIT SCHEMATIC

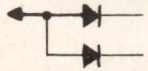
CURRENT CALIBRATOR MOD. III

B-55281



DRAWING REFERENCES:
1. ASSEMBLY: C-55282
2. PARTS LIST: PL-55282

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS 1 WATT ±10%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. MIXING DIODES TO BE PLACED EXTERNAL TO FLIP-FLOP.



3. FOR POSITIVE INPUT, INTERCHANGE PINS 1 AND 2 OF T1 AND T2.

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
M Ogden 7/14/53 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10	6820	8-24-54	WC
-9	5818	6-24-53	WO.
-8	5732	6-24-53	WO.
-7	5619	5-13-53	WO.
-6			
-5			
-4			
-3			
-2			
-1			

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
PLUG-IN-UNIT MOD II FLIP-FLOP, MTC

SCALE: —— DR. R B 7-6-53 B-55281

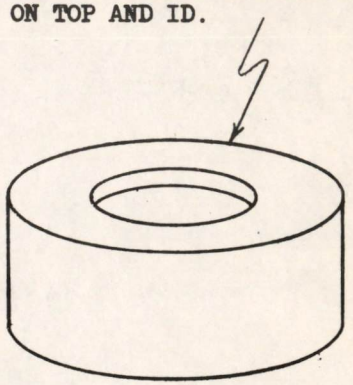
ENG. 9 July 53 CK. 7-9-53 APPD. 7-10-53

FIG. 4

A-61571

1. POTTER & BRUMFIELD KRP 11A RELAY, 6 VOLT AC COIL, DPDT CONTINUED.
2. 0.01 μfd, 200V SPRAGUE VITAMIN Q MATCHED PAIR, ±1%.
3. 0.47 μfd, 600V SPRAGUE VITAMIN Q SCREW NECK GROUNDED CASE.
4. HELIPOT MODEL A, 10K ± 5%, LIN. ± 0.05%.
5. R_1 WOUND BY HAND, MANGANIN WIRE.
6. 12V BATTERY - 8 TYPE 5R FLASHLIGHT CELLS, SERIES CONN. (BURGESS).
7. 1.5V BATTERY - 1 TYPE 5R FLASHLIGHT CELL.
8. 10.836V BATTERY - 8 TYPE RM1R MALLORY MERCURY CELL.
9. 0.5-5.0 pμf VARIABLE CAP. ERIE TYPE 532-08-0R5.
10. 0.1 μfd, 200 V SPRAGUE VITAMIN Q.
11. BNC MALE PANEL. MTG. COAXIAL CONN.
12. P.B. SW - LIGHT SPRING SNAP ACTION. MICROSWITCH.
13. LEVER SW - MALLORY 6143 INDEXING TYPE (EXTERNAL SPRING RETURN).
14. METER - 2½" SIMPSON 0-25 μAMPS D.C. (CALIBRATED FOR ZERO CENTER).
15. SHIELDED TUBE SOCKETS.
16. CATHODE FOLLOWER OUTPUT CONNECTED TO PINS 1, 2, CENTER GROUND. AMPHENOL TYPE 71, 6 PRONG SOCKET.
17. OUTPUT TRANSFORMER - 10 TURNS #30 WIRE PRI. 40 TURNS #32 WIRE SEC. CORE COVERED WITH SILVER CONDUCTING PAINT AS INDICATED IN SKETCH. FERRAMIC H MATERIAL 1/4 ID. x 5/8 OD. x 3/8 HIGH.
18. PILOT LITE - PROTRUDING BULB & CAP.

COVER CORE COMPLETELY INSIDE, OUTSIDE AND BOTTOM. LEAVE 1/16 GAP BETWEEN CONDUCTING SURFACE ON TOP AND ID.



PARTS LIST, CURRENT CALIBRATOR, MOD III

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRANSISTOR CIRCUITS COURSE
Number 4. Transistor Amplifiers

To: Distribution List

From: Donald J. Eckl

Date: August 19, 1955

Approved: William N. Papian

Abstract: Three usable amplifier configurations exist for the junction transistor. The grounded-base amplifier has the highest frequency response. The grounded-emitter has the largest power gain. The grounded-collector or emitter follower serves as an impedance transformer much in the way of a vacuum tube cathode follower. These circuits have many important differences from their vacuum tube counterparts. An important one is the more marked effect of source and load impedances on their performance. Input and output circuits are not isolated by the transistor.

1.0 Grounded-base amplifier

Suppose we consider the grounded-base circuit shown in Fig. 1.

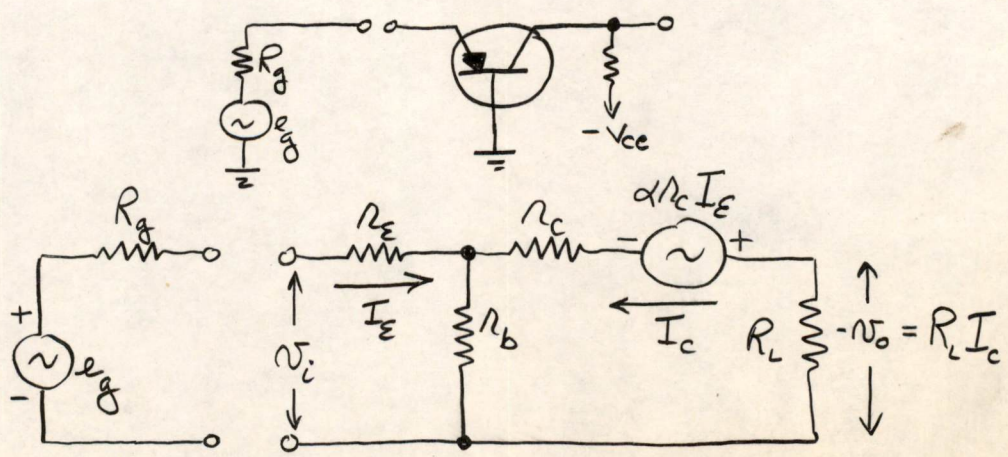


FIG. 1 - GROUNDED BASE TRANSISTOR AMPLIFIER

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The circuit equations are:

$$v_i = I_e(r_e + r_b) + I_c r_b \cdot$$

$$0 = I_e(\alpha r_c + r_b) + I_c(r_c + r_b + R_L) \cdot$$

The determinant is

$$\Delta = \begin{vmatrix} (r_e + r_b) & r_b \\ (\alpha r_c + r_b) & (r_c + r_b + R_L) \end{vmatrix}$$

or
$$\Delta = r_b\left[r_e + r_c(1-\alpha) + R_L\right] + r_e(r_c + R_L) \cdot \qquad (1)$$

$$\Delta \cdot I_e = \begin{vmatrix} v_i & r_b \\ 0 & r_c + r_b + R_L \end{vmatrix}$$

$$I_e = \frac{v_i}{\Delta}(r_c + r_b + R_L) \qquad (2)$$

$$\Delta \cdot I_c = \begin{vmatrix} r_e + r_b & v_i \\ \alpha r_c + r_b & 0 \end{vmatrix}$$

$$I_c = -\frac{v_i}{\Delta}(\alpha r_c + r_b) \qquad (3)$$

The <u>voltage gain</u> is given by:

$$G_v = \frac{-I_c R_L}{v_i} = \frac{(\alpha r_c + r_b)R_L}{\Delta} .$$

There is no phase inversion in the grounded-base circuit. The <u>current gain</u> is given by:

$$A = \frac{I_c}{I_e} = \frac{\alpha r_c + r_b}{r_c + r_b + R_L} .$$

Note that for a short-circuited output ($R_L = 0$) this is simply α.

The <u>input resistance</u> is $R_i = v_i/I_e$.

$$\therefore \quad R_i = \frac{\Delta}{r_b + r_c + R_L} .$$

$$\text{or} \quad R_i = r_e + r_b\left[\frac{r_c(1-\alpha) + R_L}{r_c + r_b + R_L}\right].$$

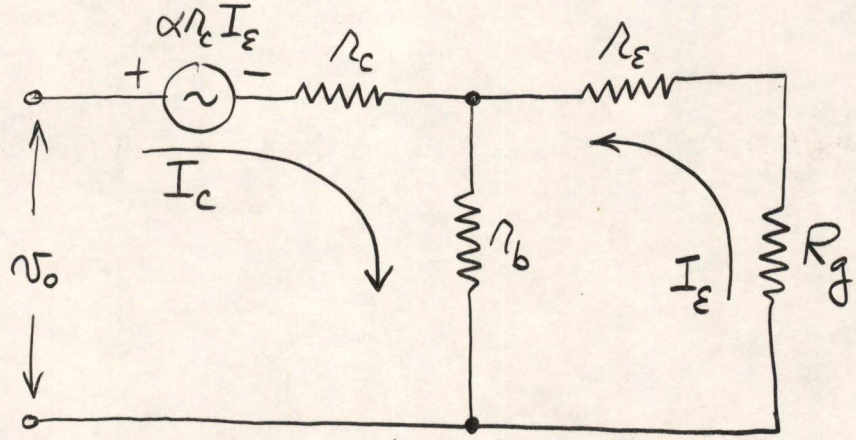
Note that the input resistance depends on the collector load R_L.

The power gain of the circuit is $I_c^2 R_L / I_e^2 R_i$.

$$P.G. = A^2\left(\frac{R_L}{R_i}\right).$$

This expression shows quite clearly how it is possible to have a power gain in the grounded-base circuit even though the current gain is less than unity. The input impedance is of the order of $r_e + r_b \approx 300\ \Omega$ while the output load R_L may be several thousand ohms. It is the higher impedance level of the output circuit which provides the power gain.

To get the output resistance of the grounded-base stage we must apply a voltage to the output terminals and calculate I_c.



$$\begin{cases} 0 = (R_g + r_e + r_b)I_e + r_b I_c . \\ v_o = (\alpha r_c + r_b)I_e + (r_b + r_c) I_c . \end{cases}$$

$$\Delta = r_c(r_e + r_c + R_g) + r_b(R_g + r_e - \alpha r_c).$$

$$\Delta \cdot I_c = \begin{vmatrix} (R_g + r_e + r_b) & 0 \\ (\alpha r_c + r_b) & v_o \end{vmatrix}.$$

The output resistance is v_o/I_c.

$$\therefore R_o = r_c - r_b\left(\frac{\alpha r_c - r_e - R_g}{r_e + r_b + R_g}\right).$$

The output resistance depends on the generator resistance R_g.

If we now make some assumptions about the relative sizes of the quantities in the above expressions, we can obtain simplified versions. Assume:

$$r_c(1-\alpha) >> R_L >> r_e, r_b.$$

Then, $$\Delta = r_c\left[r_e + r_b(1-\alpha)\right].$$

$$G_v = \frac{\alpha R_L}{r_e + r_b(1-\alpha)}.$$

$$A = \alpha$$

$$R_i = r_e + r_b(1-\alpha).$$

$$R_o = r_c\left\{\frac{r_e + r_b(1-\alpha) + R_g}{r_e + r_b + R_g}\right\} \approx r_c.$$

$$P.G. = \frac{\alpha^2 R_L}{r_e + r_b(1-\alpha)}$$

2.0 Grounded-emitter Amplifier

The grounded-emitter circuit is shown in Fig. 2.

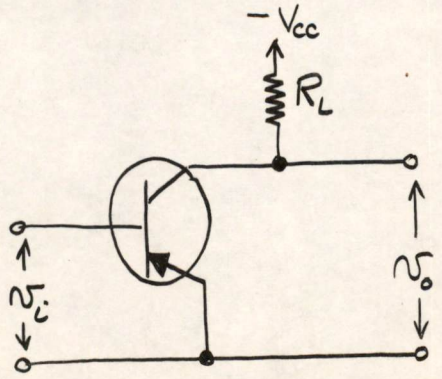


FIG. 2a

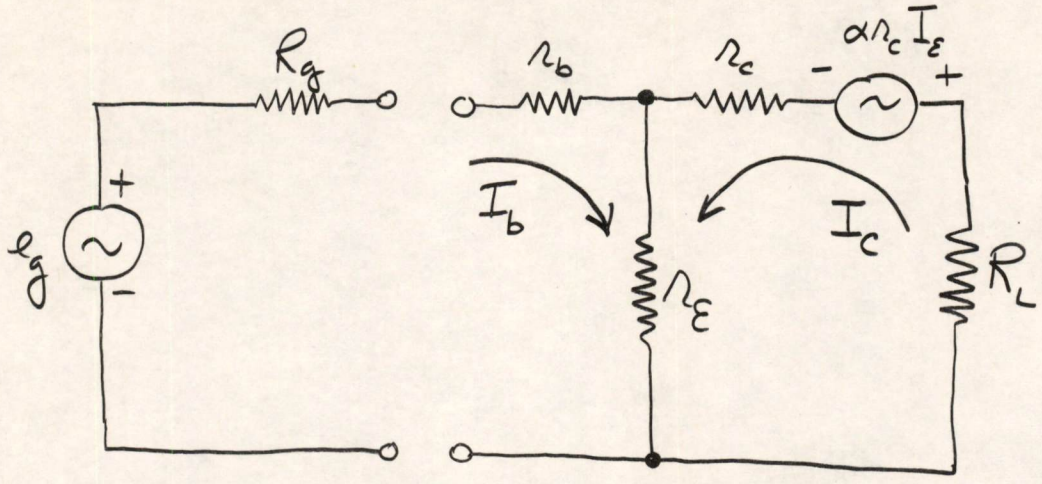


FIG. 2b - GROUNDED-EMITTER AMPLIFIER

$$e_g = (R_g + r_b + r_e) I_b + r_e I_c .$$

$$0 = \alpha r_c(-I_b - I_c) + r_e I_b + (R_L + r_c + r_e) I_c .$$

$$0 = (r_e - \alpha r_c) I_b + \left\{R_L + r_e + r_c(1-\alpha)\right\} I_c .$$

$$\Delta = r_b\left\{r_e + R_L + r_c (1-\alpha)\right\} + r_e (r_c + R_L).$$

This is, of course, the same as for the grounded-base circuit.

$$I_b = \frac{v_i}{\Delta}\left\{r_e + R_L + r_c(1-\alpha)\right\}.$$

$$I_c = \frac{v_i}{\Delta} (\alpha r_c - r_e).$$

The voltage gain for the grounded-emitter circuit is

$$G_v = \frac{-I_c R_L}{v_i} = \frac{-(\alpha r_c - r_e)R_L}{\Delta} .$$

There is a phase inversion in the output signal. The current gain is given by:

$$A = \frac{I_c}{I_e} = \frac{\alpha r_c - r_e}{r_c(1-\alpha) + r_e + R_L} .$$

The input resistance of the grounded emitter circuit is

$$R_i = r_b + r_e\left\{\frac{r_c + R_L}{r_c(1-\alpha) + r_e + R_L}\right\}.$$

The power gain is

$$P.G. = A^2\left(\frac{R_L}{R_i}\right).$$

In this case $A > 1$ so the power gain is larger than for the grounded base circuit.

If the output resistance is calculated as before the result is

$$R_o = r_c(1-\alpha) + r_e\left\{\frac{R_g + r_b + \alpha r_c}{R_g + r_b + r_e}\right\}.$$

If we assume that

$$r_c(1-\alpha) >> R_L >> r_e,\ r_b$$

we obtain the following approximations:

$$G_v = \frac{-\alpha R_L}{r_e + r_b(1-\alpha)}$$

$$A = \frac{\alpha}{1-\alpha}$$

$$R_i = r_b + \frac{r_e}{1-\alpha}.$$

$$R_o = r_c(1-\alpha) + r_e\left\{\frac{\alpha r_c + R_g}{r_e + r_b + R_g}\right\}$$

$$P.G. = \frac{1}{(1-\alpha)}\cdot\left\{\frac{\alpha^2 R_L}{r_e + r_b(1-\alpha)}\right\}$$

3.0 Grounded-Collector Amplifier

The grounded-collector amplifier is shown in Figure 3. This is the transistor equivalent of the cathode-follower and is frequently referred to as an emitter-follower.

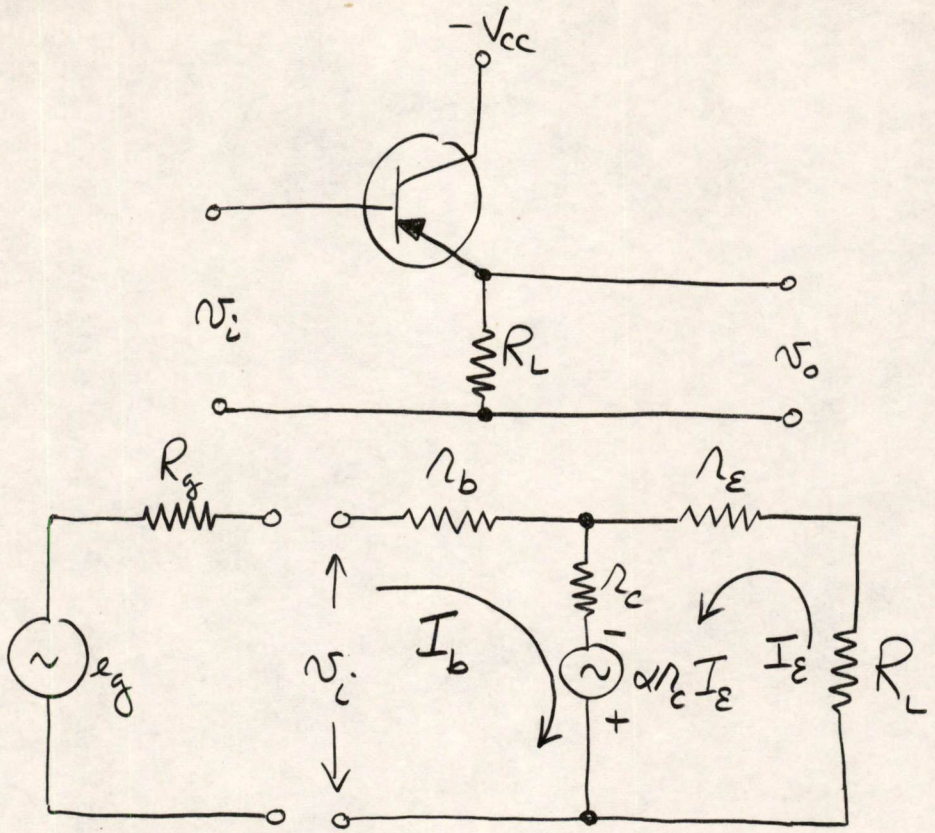


FIG. 3 - GROUNDED - COLLECTOR AMPLIFIER

The loop equations are:

$$v_i = (r_b + r_c)\, I_b + r_c(1-\alpha) I_e$$

$$0 = r_c I_b + \left\{R_L + r_e + r_c(1-\alpha)\right\} I_e .$$

The input or base current is:

$$I_b = \frac{v_i}{\Delta}\left\{r_c(1-\alpha) + r_e + R_L\right\}$$

The output current is:

$$I_e = \frac{v_i}{\Delta} r_c .$$

The voltage gain for the emitter-follower is

$$G_v = \frac{I_e R_L}{v_i} = \frac{r_c}{\Delta} R_L$$

The current gain is normally greater than unity.

$$A = \frac{I_c}{I_e} = \frac{r_c}{r_c(1-\alpha) + r_e + R_L} .$$

The input resistance is

$$R_i = r_b + r_c \left\{ \frac{r_e + R_L}{r_c(1-\alpha) + r_e + R_L} \right\}$$

Note that this is approximately $R_L/1-\alpha$ which is an order of magnitude larger than the emitter resistance R_L.

The power gain is $A^2\left(\frac{R_L}{R_i}\right)$ which is greater than unity because of the A^2 term.

The output resistance is given by

$$R_o = r_e + r_c (1-\alpha) \left\{ \frac{R_g + r_b}{R_g + r_b + r_c} \right\}$$

If we make the same assumptions as before, we obtain the following approximations:

$$G_v = 1$$

$$A = \frac{1}{1-\alpha} = \beta + 1$$

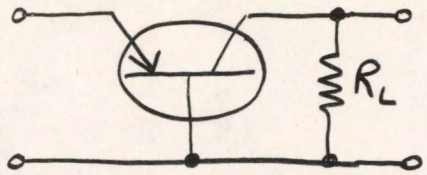
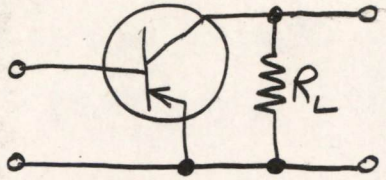
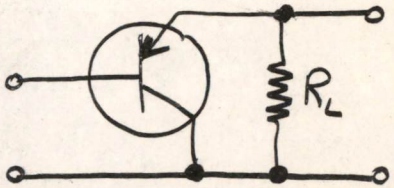
$$R_i = R_L/(1-\alpha) = R_L(\beta + 1)$$

$$P.G. = \frac{1}{1-\alpha} = \beta + 1$$

$$R_o = r_e + (r_b + R_g)(1-\alpha).$$

Note that the circuit has a relatively high input resistance and low output resistance.

A comparison of approximate formulae for the three configurations is given in Fig. 4.

FIGURE 4 APPROX. FORMULAE ASSUMING $r_c(1-\alpha) \gg R_L \gg r_e, r_b$	Grounded-base	Grounded-emitter	Grounded-collector
			
CURRENT GAIN	α	$\frac{\alpha}{1-\alpha} = \beta$	$\frac{1}{1-\alpha} = \beta + 1$
POWER GAIN	$\frac{\alpha^2 R_L}{r_e + r_b(1-\alpha)}$	$\left(\frac{1}{1-\alpha}\right)\left\{\frac{\alpha^2 R_L}{r_e + r_b(1-\alpha)}\right\}$	$\frac{1}{1-\alpha} = \beta + 1$
INPUT RESISTANCE	$r_e + r_b(1-\alpha)$	$r_b + \frac{r_e}{1-\alpha}$	$\frac{R_L}{1-\alpha} = (\beta + 1) R_L$
OUTPUT RESISTANCE	$r_c\left\{\frac{r_e + R_g + r_b(1-\alpha)}{r_e + R_g + r_b}\right\}$	$r_c(1-\alpha) + r_e\left\{\frac{\alpha r_c + R_g}{r_e + r_b + R_g}\right\}$	$r_e + (r_b + R_g)(1-\alpha)$
VOLTAGE GAIN	$\frac{\alpha R_L}{r_e + r_b(1-\alpha)}$	$\frac{-\alpha R_L}{r_e + r_b(1-\alpha)}$	1

4.0 Effect of Load Resistance on Amplifier Performance

In general we are not at liberty to change the internal transistor parameters given in the previous expressions. We can, however, vary the load R_L.

Fig. 5 shows the effect of load resistance on current gain for the 3 amplifiers.

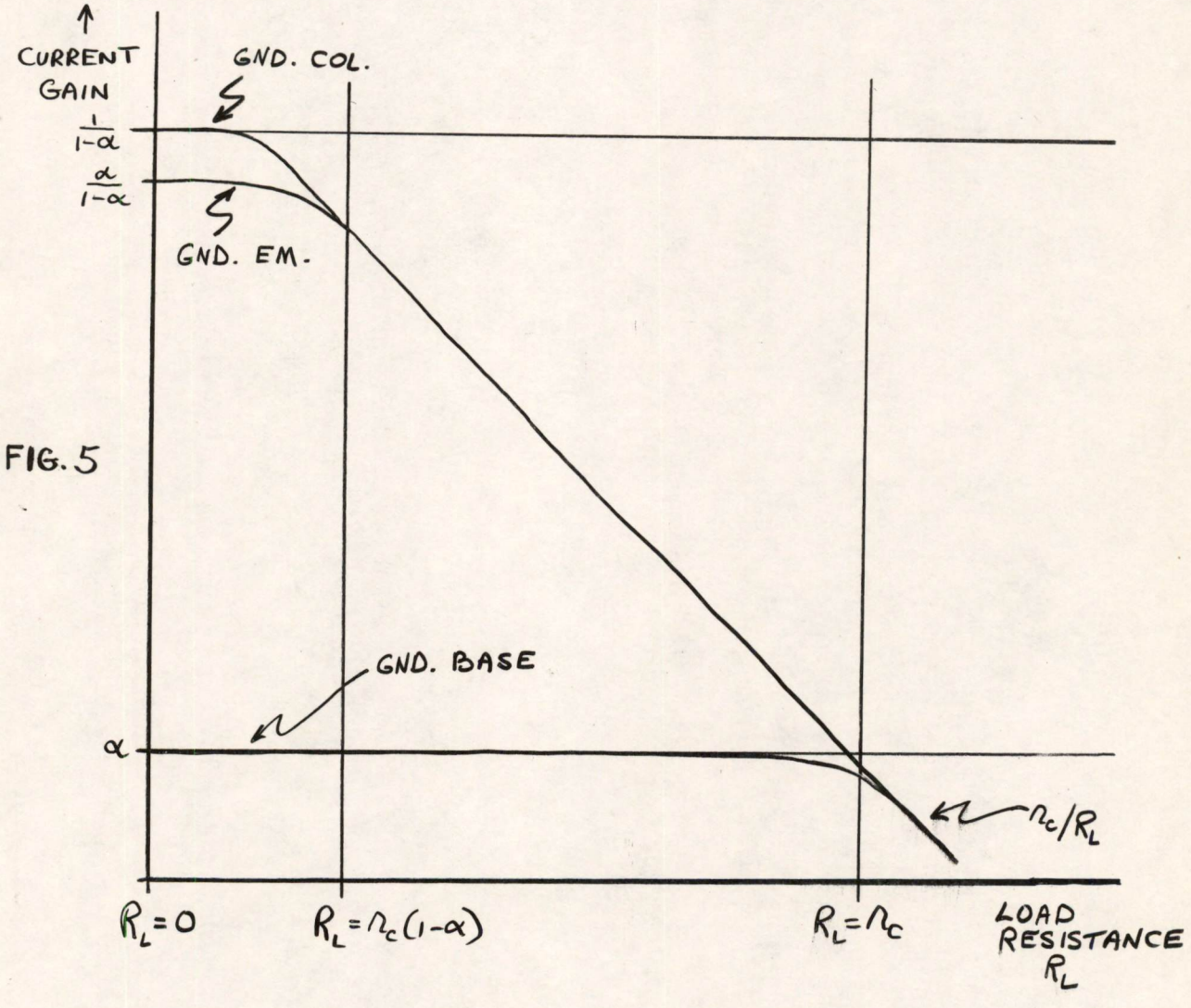


FIG. 5

As R_L becomes greater than r_c all three have a current gain of about r_c/R_L.

The effect of load resistance on input resistance is shown in Figure. 6.

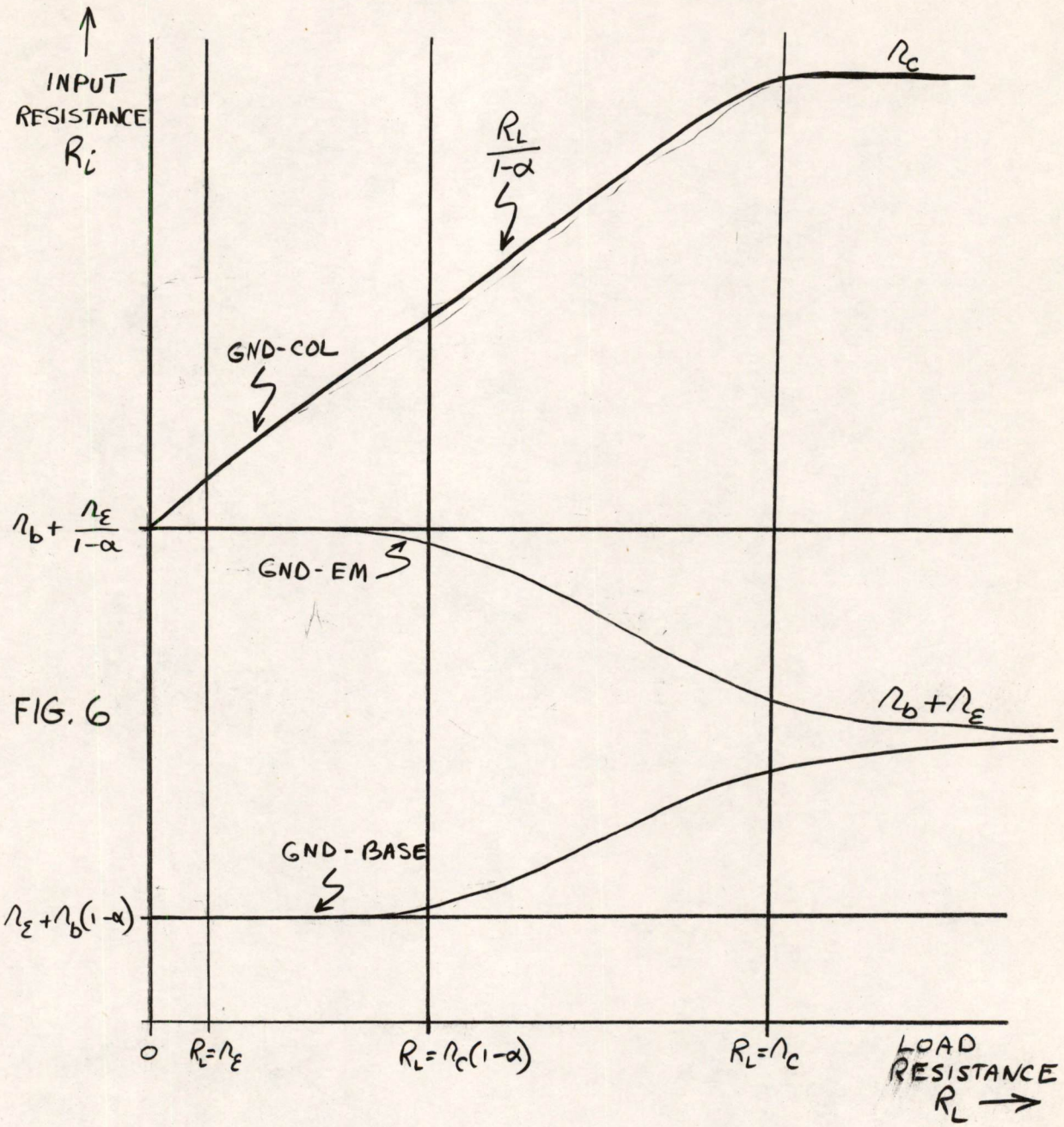


FIG. 6

The effect of the driving generator impedance on the output impedance of a transistor stage is shown in Figure 7. It is important to note the difference in current and voltage drive on the output impedance.

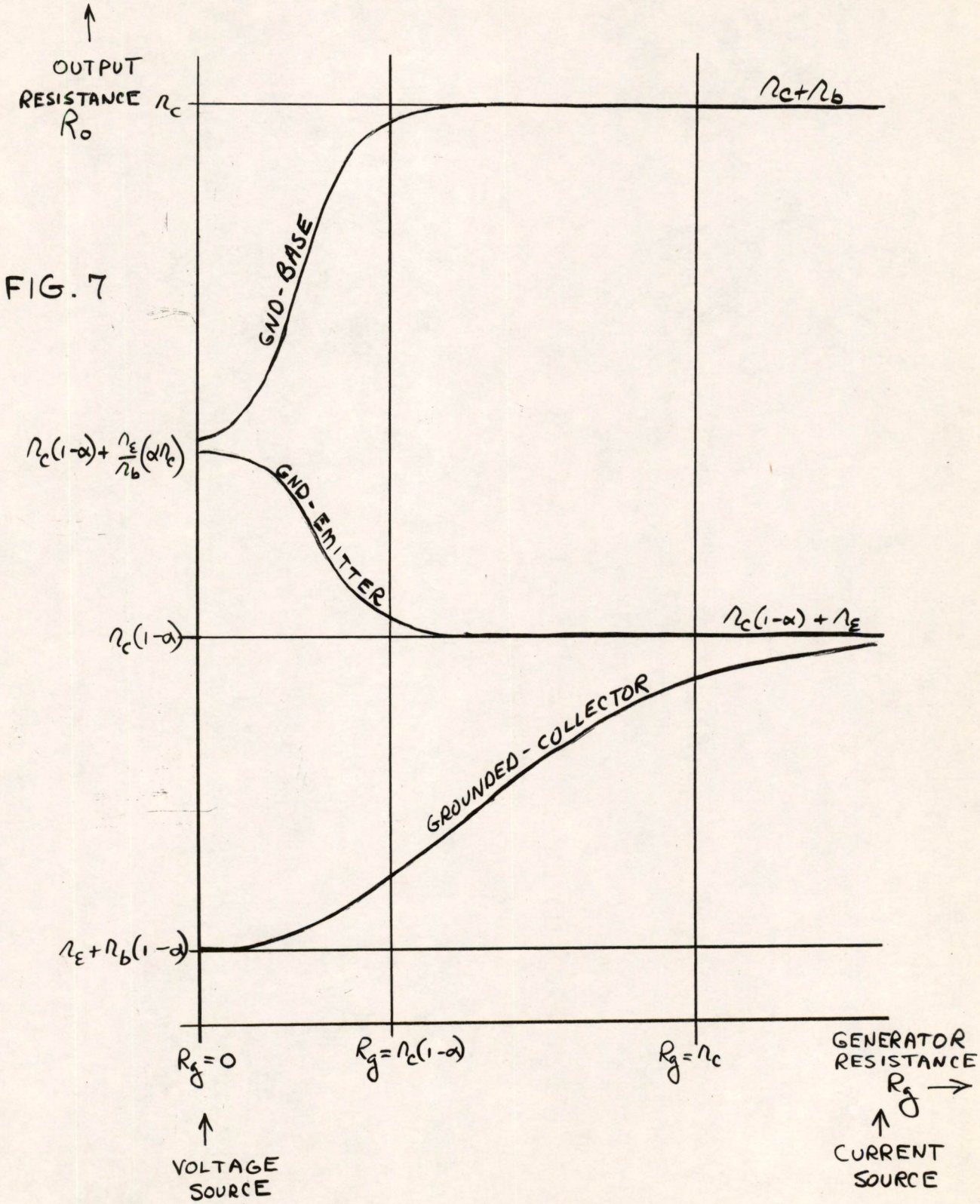

OUTPUT RESISTANCE R_o
r_c
$r_c + r_b$
GND-BASE
$r_c(1-\alpha) + \frac{r_\varepsilon}{r_b}(\alpha r_c)$
GND-EMITTER
$r_c(1-\alpha)$
$r_c(1-\alpha) + r_\varepsilon$
GROUNDED-COLLECTOR
$r_\varepsilon + r_b(1-\alpha)$
$R_g = 0$
$R_g = r_c(1-\alpha)$
$R_g = r_c$
GENERATOR RESISTANCE R_g
VOLTAGE SOURCE
CURRENT SOURCE

FIG. 7

5.0 Frequency Response of Transistor Amplifiers

This is a subject which will be treated in more detail later on. The frequency response of the grounded-base amplifier is due to the variation in current-gain α with frequency. This can be expressed approximately as:

$$\alpha = \frac{\alpha_o}{1 + j\left(\frac{f}{f_{c\alpha}}\right)}$$

where α_o is the low frequency α and $f_{c\alpha}$ is the frequency at which α is $.707\alpha_o$. This expression is only an approximation and, in fact, one which is accurate only for $f/f_{c\alpha} \leq 1$.

The current gain of a grounded-emitter stage is

$$\beta = \frac{\alpha}{1-\alpha} = \frac{\dfrac{\alpha_o}{1 + j\left(\dfrac{f}{f_{c\alpha}}\right)}}{1 - \dfrac{\alpha_o}{1 + j\,(f/f_{c\alpha})}} = \frac{\alpha_o}{1 - \alpha_o + j\left(\dfrac{f}{f_{c\alpha}}\right)}$$

If we now divide top and bottom by $1 - \alpha_o$ we get

$$\frac{(\alpha_o/1 - \alpha_o)}{1 + j\,\dfrac{f}{f_{c\alpha}\,(1 - \alpha_o)}}$$

or $$\beta = \frac{\beta_o}{1 + j\,\dfrac{f}{f_{c\alpha}(1-\alpha_o)}}$$

Therefore the grounded-emitter stage has a frequency response $(1-\alpha_o)$ times that of the grounded-base circuit. This may be 1/10 or less.

The next chapter will discuss temperature stability of transistors.

Donald J. Eckl

Donald J. Eckl

DJE/md

Distribution List

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46. Woolf, B-132
47. Zieman, H., B-132
48. Zopatti, R., B-186