Division 6 - Lincoln Laboratory
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SUBJECT: MAGNETIC CORE SHIFT REGISTER EVALUATOR

To: N. H. Taylor

From: Carl J. Schultz

Date: May 3, 1954

ABSTRACT: The problem of evaluation of magnetic core shift register is presented from the point of view of minimizing the time required to determine operating margins. A brief description of the operation of a shift register is given, together with the procedure involved in determining the operating margins. The method of evaluation used in the system is outlined and an example of the results obtained is shown. No attempt is made to establish criteria for optimizing shift register operating margins - that is a judgment which is reserved for a consideration of the shift register application and requirements.

A. Introduction

The realization of working magnetic core shift registers in the 100 KC range has been in the past a product of the art of combining engineering calculations with intuitively guided experimentation. The determination of the goodness of the product has been a particularly difficult job of evaluation because of the large number of variables involved. Every element in a magnetic core shift register is a factor which affects its operation, and in order that a useful register be born out of the labor of almost endless substitutions and time consuming investigations, it is desirable that a rapid method of experimentation be used. The automatic Evaluator described in this note performs the task of furnishing operating margins for a particular shift register in a small fraction of the time that would be required to find the information under the guidance of a human operator.

B. Shift Register Characteristics

The type of register that is currently being investigated consists of the elements shown in Fig. 1 for the typical stage. The magnetic material that is used for operation at shifting frequencies of 100 KC and above is Mo-Permalloy tape. The magnetic flux of the core must first be set in one direction by a flow of current through the input winding, which is connected to the output winding terminals of the previous stage.

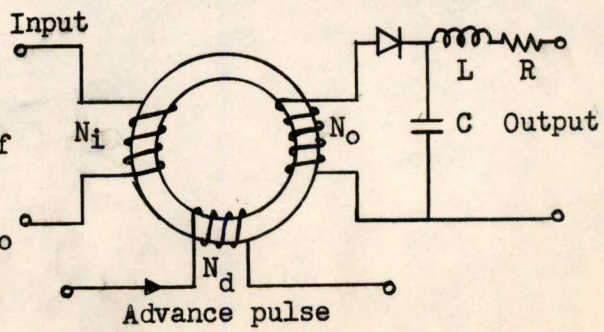


FIG. 1

Then an advance current pulse applied through the advance winding will set the magnetic flux in the opposite direction and will induce a voltage in the output winding. This voltage will cause current to flow in the forward direction of the diode. The capacitor will become charged through the forward resistance of the diode and the core output winding. However, it will discharge through the inductor, resistor, and the input winding of the succeeding stage of the shift register, thereby setting the magnetic flux of that core to the direction that may be defined as "zero". The condition of a core may be sensed at the time of application of the advance pulse. If the core had previously been set to "one," then the voltage induced in the output winding will be large during the advance pulse. If the core had been set to "zero" previously, only a small voltage will be induced in the output winding. The advance current pulse must be of such a duration that it will have ended soon enough in a particular stage of the register to allow the input current supplied from the coupling circuit of the preceding stage to be of sufficient amplitude and duration to set the flux to "one". This depends upon the capacitor discharge current magnitude and duration, which in turn is related to the selected values of R,L,C, the diode, the number of turns on the windings, and upon the previous advance current pulse amplitude and length. The coupling circuit serves to transfer the energy required to switch the succeeding core, and also to prevent energy from flowing in the backward direction to set the previous core to "one".

C. Shift Register Operating Margins

The successful operation of the register depends upon the effective transfer of information from the core originally containing either a "one" or "zero" to the succeeding core. This transfer must be realized by means of the coupling circuit between the two cores. Every element in the coupling circuit, in addition to the advance pulse characteristics and the magnetic core characteristics, becomes a variable which makes the operation of the register either more or less successful. The time-consuming task of combining these variables into an optimized working register can be resolved into a procedure which involves the following steps: (a) Design a coupling circuit for use with cores having particular flux change and switching time characteristics; (b) Construct at least four stages, connected so that the information circulates in the register; (c) Change the advance current pulse amplitude, length, and rise time and observe the limits for which the register continues to store and transfer all combinations of information successfully; (d) Decide whether the resulting margins represent a register which might be useful in a particular application (upon consideration of (1) the effects of advance pulse current driver tube deterioration, and (2) the required operating speed; (e) In the event that the operating margins do not represent a useful register, then, judicious changes of the variables should be made in order to shift the margins in the direction to fulfill the desired requirements, and (f) Retrace parts b, c, d, and e as many times as are necessary to obtain satisfactory limits of operation.

D. Methods of Iteration

One method of obtaining the data outlined in the preceding paragraph involves the complete manual manipulation of all variables, in addition to the manual injection into the register of all possible combinations of "ones" and "zeros" that constitute the storage and transfer pattern of information. This primitive method, when associated with the necessary changing of many patterns of information and of many variables in many stages of the register, places considerable strain upon the mental and physical capabilities of the human control element during the long period of time involved.

Another method involves the use of an electronic control system, which brings about an appreciable reduction in the time consumed and in operator fatigue. The system automatically varies the advance current pulse amplitude and length at a rapid rate and presents, on an oscilloscope, a matrix pattern of intensified spots to indicate successful operations of the shift register. Patterns of information are also changed automatically. All other parameters must still be varied manually, but since that part of the total data-accumulation time is small, little could be gained by further automatizing the procedure.

E. Automatic Evaluation

E.1 System timing

Figure 2 shows the block diagram of the system. An outline of the kind and the order of events that occur after each clock pulse is as follows (numbers indicate events displaced in time, and letters indicate events occurring simultaneously).

1. Time t_1 (clock pulse)

(A) "Clear" pulse occurs - this places the four cores of the register in the "zero" flux condition.

(B) Information "set" counter changes

(FF_1-GT_1, FF_2-GT_2, FF_3-GT_3, FF_4-GT_4)

(a) Counter end carry pulse occurs if the previous counter number was 1111 - and the display scope intensifies if the register output counter (FF_5-GT_5, 2^6 counter) had sensed the proper number (2^6) of "ones" shifted out of the register during all the combinations of binary numbers since the previous 1111.

(b) "Set" pulse generators 1, 2, 3, and 4 (standard 7AK7 gate tube circuit) are open or closed according to the configuration of "ones" held by the Information "Set" counter flip-flops.

2. Time $t_1 + t_2$ (t_2 determined by $G + D_1$)

(A) "Set" pulse generators drive into the magnetic core register and set the cores to the same configuration of "ones" as contained in the Information "Set" counter.

(B) "Advance" pulse burst generator ring (MX_1, $G + D_3$, DE_1, GT_9) closes as a result of the change of state of FF_9.

(C) "Y" Decoder is pulsed if the last number held by the Information "Set" counter was 1111 and the end carry from that counter had opened GT_8. The change of output of the "Y" decoder then causes the following.

(a) Matrix Display 'scope y-position is changed.

(b) "Advance" current pulse amplitude is changed to its next highest value, or to its minimum value if the Y decoder is reset (in this case, the Y decoder produces an end carry and changes the X decoder output, which in turn controls the advance current pulse width and also the Matrix Display 'scope x-position).

(D) Z axis amplifier input is changed by FF_7 - this ends the 'scope intensification pulse which presented a visual indication (on the Matrix Display 'scope) of the successful transfer and storage of information in the shift register.

3. Time $t_1 + t_3$ ($t_3 > t_2$, t_3 determined by $G + D_2$)

(A) A pulse passes through MX_2 and INV_2 and appears at the zero input of FF_6. This closes GT_6 at the beginning of each burst of eight advance current pulses.

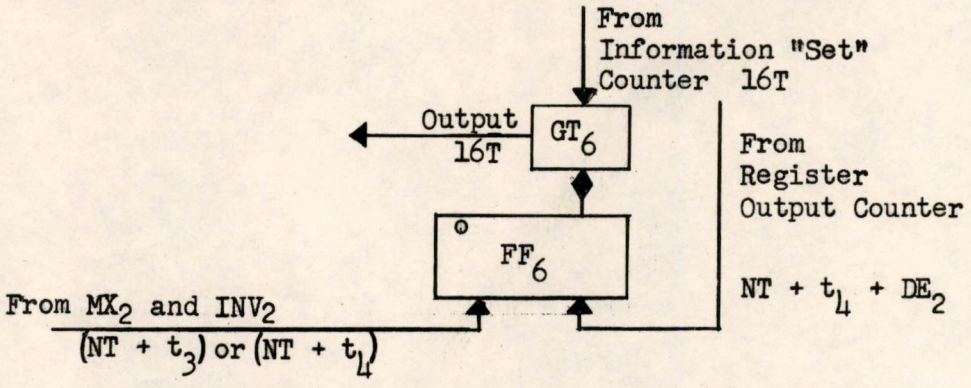
(B) A series of eight pulses is generated in the advance pulse burst generator ring. This pulse burst serves two functions:

(1) It initiates eight advance current pulses that transfer information twice around the 4-stage register (two complete cycles provide greater assurance of successful operation than only one cycle).

(2) After the delay due to $G + D_4$, the pulses are used as strobe pulses which sense the presence of "one" and "zero" output signals from the shift register as they appear at the grid of GT_{10}. The output of GT_{10} then goes to the register output counter (FF_5, GT_5, 2^6 counter) and through MX_2 and INV_2 to FF_6.

E.2 Error Detection

The successful transfer and storage of information in the shift register is determined by the occurrance of an end carry pulse from the Register Output counter just preceding an end carry pulse from the Information "Set" counter. The figure below shows the error detection system with its three inputs, one output, and associated timing. The cycle of operation is repetitive for intervals equal to 16 clock pulses.



T = clock pulse interval

$t_3 = G + D_2 < T$

$t_4 = [t_3 + n(G + D_3) + (G + D_4)] < T$

$1 \leq N \leq 16$
$1 \leq n \leq 8$
} where $N = 15$, $n = 8$ during successful operation

The above arrangment assures that out of any number of shift register output pulses up to $2^{12} - 1$, only a precise count of 2^6 at the proper time will be detected and converted into an intensifying pulse on the Matrix Display 'scope. The occurance of 2^{12} shift register output pulses is eliminated from becoming an indication of a successful operation by a toggle switch setting on the 2^6 lowspeed counter (Register Output Counter) by which FF5 clears FF6 and does not permit the generation of more than a single end carry from the Register Output Counter.

F. Alternate Use of Evaluator

The application of the Evaluator has been extended to include the testing of a magnetic core counter employing the previously described shift register circuitry plus other circuits which perform the logical functions necessary for counting. This application eliminates the use of the Information "Set" counter and three of the "Set" pulse generators, since the number which is held by the magnetic core counter must be changed by a count of "1" for each operation and that is done by the core circuitry. In the testing of the circulating shift register, it is

necessary to change the information by control external to the register in order to completely determine the successful operation for all patterns of binary information. The magnetic core counter is tested for the successful storage and progressive counting through all the combination of four bits of information. If 2^5 "ones" are properly shifted out of the counter, the Matrix Display 'scope will indicate a successful operation for a particular value of current pulse length and amplitude.

G. Equipment

Standard test equipment is used for gate and delayed pulse generators, mixers, delays, 2^6 lowspeed counters, flip-flops and gates. The Matrix display 'scope is a DuMont 304-H. The "X" and"Y" decoders are made of plug-in type flip-flops. The Advance Pulse Generator is shown in block diagram form in Figure 3. The Clear Pulse Generator is similar to Figure 3, except that the "X" and "Y" decoder inputs and associated cathode followers are substituted for by manually operated amplitude and width controls. The Set Pulse Generators are similar to the Clear Pulse Generator, except that they contain 7AK7 current amplifiers rather than 6CD6's.

A feature of the Evaluator which increases its value as a time saver is the flexible arrangement of R, L, and C components. A wide range of values of each of the components has been assembled on rotary selector switches. Values of Resistance can be varied between 33 and 15,000 ohms with 26 intermediate values, C between 220 and 169,000 μμfd, and L between 0.033 and 25 mh. This adequately covers the widest range of values of these components that can be presently expected to be used. Connections between components are made through plug-in type terminal boards and leads. Magnetic cores and associated windings are mounted on minature tube socket assemblies, and diodes are mounted in spring clips. All of these connections and assemblies allow easy replacement and rearrangement of the component parts.

H. Results

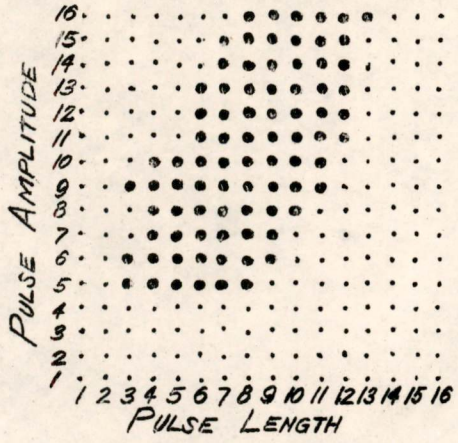
The sketch below shows a sample pattern that appeared in the Matrix Display 'scope during the testing of a 4-stage shift register made of 1/8 mil Mo-Permalloy cores (5/16" diameter, 1/8" wide, 20 wraps). The coupling circuit is of the same configuration as that shown in Figure 1. The component values are:

$$C = 1000 \text{ μμfd}, \quad L = 15 \text{ mh},$$

$$R = 4700 \text{ ohms}, \quad N_o = 100 \text{ turns},$$

$$N_i = 150 \text{ turns}, \quad N_d = 25 \text{ turns}.$$

The rise time of the pulse was 0.3 μsec and the fall time was 0.4 μsec. The intensified spots indicate the coordinates at which the shift register successfully stores and transfers all combinations of four bits of binary information. The shifting rate was 100 KC and a complete display of the matrix appeared at minimum intervals of approximately two seconds.



CONVERSION TABLE

Unit	Pulse Length	Pulse Amplitude
1	1.3 μsec.	2.8 Amp. Turns
2	1.5	3.7
3	1.8	4.5
4	2.1	5.6
5	2.4	6.8
6	2.8	8.2
7	3.2	9.6
8	3.6	10.9
9	4.0	11.8
10	4.4	13.2
11	4.9	14.4
12	5.4	16.3
13	5.9	18.0
14	6.4	19.8
15	6.9	21.3
16	7.3	22.5

I. Discussion of Results

Upon consideration of the results presented on the display 'scope there might arise the question: "How reliable is the information?" The degree of reliability is dependent upon the accuracy of the method of detecting the successful operation of the shift register. That is done in the Evaluator by counting the number of "ones" that are shifted serially past a particular point in the register during the storage and transfer of all possible combinations of four bits of binary information. The error detection system shown on page 5 then allows an indication of successful operation only when precisely the correct number of "ones" have been counted. Although this method does not preclude the possibility that a correct count might occur upon the transfer of one or several incorrect patterns of information during a cycle of operation, the possibility appears to be an extremely remote one. The observer can easily verify the successful operation at any particular value of advance pulse amplitude and width by (a) stopping the X and Y decoders from changing with each clock pulse, (b) displaying the 16 groups of shift register binary outputs during a cycle of operation, and (c) visually checking the number, sequence, and arrangments of the output pulses.

Signed: C. J. Schultz
C.J. Schultz

Approved: J F Jacobs
J.F. Jacobs

CJS/rb

Drawings: C-47094
A-47095

C-47094

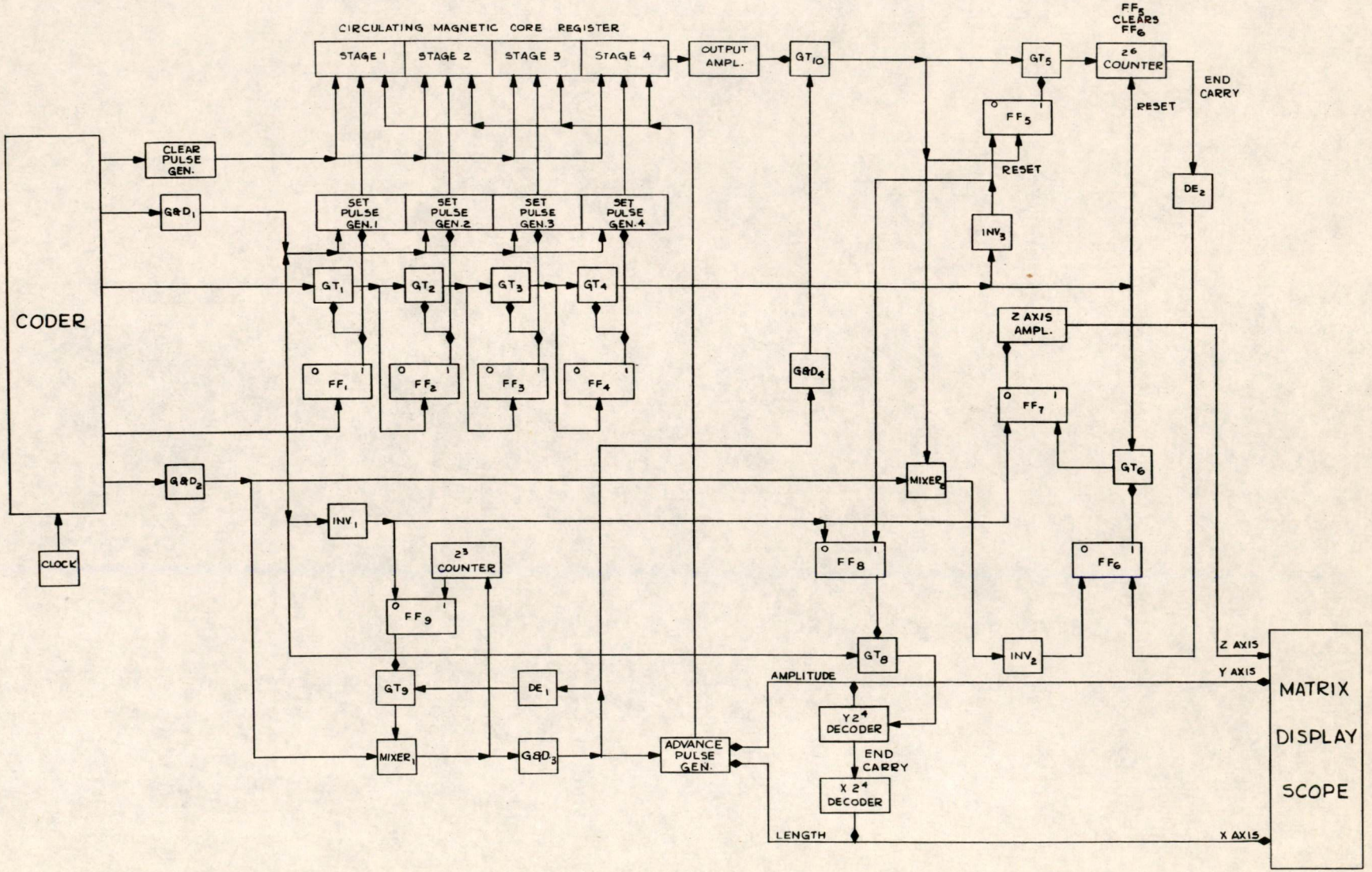


FIG. 2

MAGNETIC CORE SHIFT REGISTER EVALUATOR

A-47095

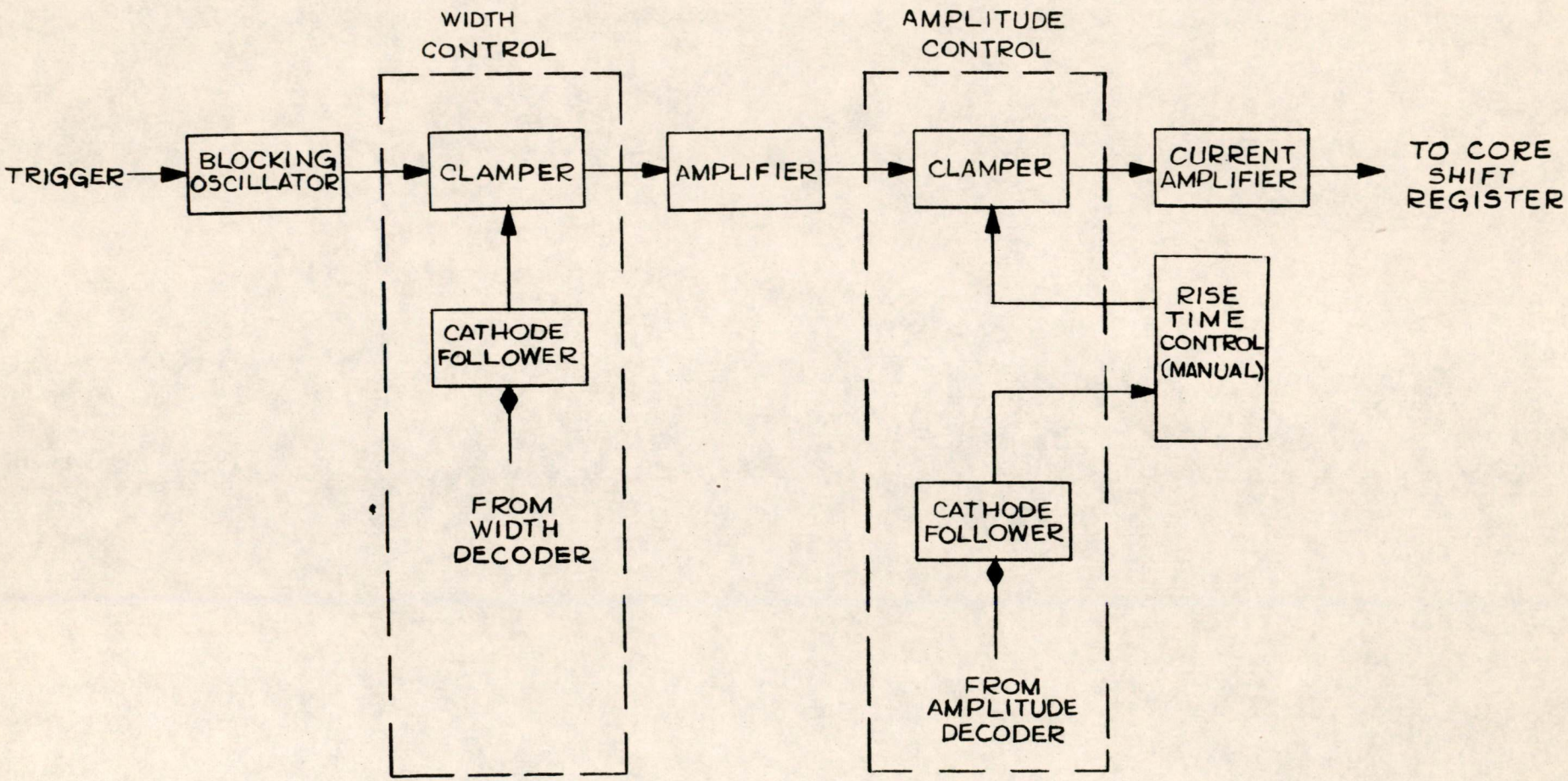


FIG. 3

ADVANCE CURRENT PULSE GENERATOR

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SUBJECT: BLOCKING OSCILLATOR CORE DRIVERS FOR USE IN DISPLAY GENERATOR BUFFER STORAGE

To: N.H. Taylor

From: Eli Anfenger

Date: 11 May 1954

Abstract: A cheap core driver has been built which is a blocking oscillator triggered from a standard pulse. The output pulse lengths are determined by lumped constant delay lines, the amplitude by the B+ to bottoming of the tube excursions. For high current sources the pulse is amplified by a power pentode whose plate is driven from B+ to bottoming and transformed to the desired level.

Introduction

It was desired to develop a cheap drive for use in a display generator buffer storage as illustrated in Fig. 1. In this figure each winding represents the output transformer of a driver. The drivers are returned to voltages such that each core winding is held from conduction because of the switch action of the diode in series with it. The bit and word drivers are 40 volt pulse sources; the bit driver pulsing negatively and the word driver pulsing positively. Either driver alone will reduce the bias on the diode to zero, whereas the coincident operation of both drivers will give a 40 volt source to drive current through the core winding. Read is accomplished by a 150-volt pulse on a second core winding. The read windings are connected in series as dictated by the logical use of the information. A third winding on the core is the output terminals for read.

The requirements for the above circuits are as follows:-

1) Bit Driver

   a) Isolated 40-volt pulse max., 35-volt minimum at 28 ma.

   b) 3 μsec pulse.

   c) Driver must trigger from positive standard pulses +20 v. to +40 v.

d) Driver must be capable of operating in a burst of 8 pulses spaced 10 μsec apart, with a burst repetition rate of 1000 cycles.

2) Word Driver

a) Isolated 40-volt pulse max., 35-volt minimum zero to 800 ma.

b) Good regulation from no load (no cores) to full load (32 cores)

c) 4 μsec pulse.

d) Driver must trigger from positive standard pulses of 10 to 40 volts.

e) Repetition rate 1000 cycles.

3) Read Driver

a) Isolated 150-volt pulse at 1 amp.

b) 1 μsec pulse.

c) Driver must trigger from positive standard pulse 20 to 40 volts.

d) Repetition rate 1000 cycles.

Circuits

1) Bit Driver

The bit driver circuit is shown in Fig. 2. It consists of 1/2 5965 connected as a blocking oscillator. The pulse length is determined by a delay line in the grid circuit. The tube bottoms during the pulse. The 33 K resistor in the plate circuit reduces the overshoot and adds damping for stability. Delay of the Output pulse compared with the input pulse is about 0.2. The characteristic waveforms are shown in Fig. 3.

The input impedance to a pulse which will trigger the blocking oscillator is 400 ohms. The maximum cathode current is on the order of 80 ma. All possible voltage measurements were made directly on the plates of the scope. When the levels were too low to be read this way they were read through the amplifiers and calibration of the scope. In every case when direct and amplifier measurements were compared the amplifier measurements were about 30% higher than the direct measurements. Since all current measurements were made by measuring the drop in a small series resistor, it is assumed these readings are slightly high. Because

of this observation those diagrams that have photographs show approximate voltages when the measurement could not be made directly on the scope plates. The maximum grid voltage during conduction of the tube is +7 volts.

2) Word Driver

Two word driver circuits are shown in Figs. 4a and 4b. Each consists of a blocking oscillator (1/2 5965) driving a power amplifier (6293). The blocking oscillator bottoms. The output is stepped up to drive the power amplifier from cut-off to bottoming. The plate voltage of the power amplifier is transformed to the desired output level. Pulse length (4 μsec) is determined by the delay line in the grid of the blocking oscillator. Characteristic waveforms of Fig. 4b are shown in Fig. 5. The blocking oscillator peak grid voltage is +7 volts; the peak cathode current is about 60 ma. The peak current of the power amplifier cathode loaded (47 ohms) is 300 ma and the screen is 100 ma. Unloaded the peak current is 200 ma on the cathode and 100 ma on the screen.

3) Read Driver

Two read driver circuits are shown in Figs. 6a and 6b. These are essentially the same as the word drivers with the exception of the delay line of the blocking oscillator. Here the pulse length is 1 μsec. Characteristic waveforms of Fig. 6b are shown in Fig. 7. The peak cathode current of the blocking oscillator is about 60 ma; the peak grid voltage is +7. The peak cathode current of the power amplifiers is about 1 amp. and peak screen is about 0.5 amp.

The reason for two types is that at first the maximum B+ was 250 volts but later it was learned that 600 volts would be available.

Circuit Margins

Curves of the input triggering voltage versus bias for the three types of drivers are shown in Figs. 8,9. and 10. These are shown for a bogie 5965 and a down 5965. The characteristic of the bogie and down 5965 are shown in Fig. 11.

It was found that the blocking oscillator worked well when the plate voltage was changed between ± 50 volts, however, the output is a function of the plate voltage. The blocking oscillator also works well when either a 12AY7 or 12AU7 are substituted for the 5965.

A table of screen margins of the 6293 for the various circuits is shown in the table below.

Circuit	Min. Screen Voltage for satisfactory Opr.	Max. Screen Voltage tried	Nominal Voltage
Fig. 4a	90	440	240
Fig. 4b	60	440	150
Fig. 6a	320	590	400
Fig. 6b	210	440	250

Shunting the diodes of the blocking oscillator grid circuits with 10K resistors had no effect on the output of the circuits. Raising the screen voltages on the power amplifiers lengthened the pulse on the order of 0.2 to 0.5 μsec. at the extremes. The delay of the output pulses relative to the input pulses is a function of the triggering pulses. Over the required operating range of triggers the delay is 0.5 μsec at most.

Suggested Improvements

It appears that the only handle for marginal checking the blocking oscillator is the triggering level. If a pentode is used such as a 7AK7 the screen could serve as a convenient handle.

While the maximum tube rating of the 5965 is not exceeded in the present application, an increase in the grid to plate winding ratio of the blocking oscillator transformer would reduce the maximum cathode current and the maximum positive grid voltage. A five to one ratio was tried and found to be marginal for triggering and bottoming. Perhaps a four to one ratio would be a good compromise.

To improve the screen margins of the read driver a circuit configuration as shown in Fig. 6b with the cathode of the 6293 returned to -150v and the blocking oscillator output winding returned to -300v is worth trying. The output transformer will have to be changed.

1) Blocking Oscillator Transformers

Wound on Ferramic H Core F109-3 die size

Grid winding	50T	#36	Formex
Plate winding	150T	#36	Formex
Output winding	57T	#36	Formex

2) Word Driver and Read Driver Blocking Oscillator Transformer

Wound on Ferramic H Core F109-3 die size

Grid Winding	50 T	#36	Formex
Plate Winding	150 T	#36	Formex
Output Winding	225 T	#36	Formex

3) Word Driver Power Amplifier Transformer (Fig. 4a)

Wound on 2 mil Westinghouse L4 Hypersil

Primary	250 T	#36	Formex
Secondary	25 T	#36	Formex

4) Word Driver Power Amplifier Transformer (Fig. 4b)

Wound on 2 mil Westinghouse L4 Hypersil

Primary	375 T	#36	Formex
Secondary	25 T	#36	Formex

5) Read Driver Power Amplifier Transformer (Fig. 6a)

Wound on 2 mil Westinghouse L1 Hypersil

Primary	70 T	#36	Formex
Secondary	35 T	#36	Formex

(Could just as well be 50 turns and 25 turns.)

6) Read Driver Power Amplifier Transformer (Fig. 6b)

Wound on 2 mil Westinghouse L1 Hypersil

Primary	100 T	#36	Formex
Secondary	25 T	#36	Formex

Signed Eli Anfenger
Eli Anfenger

Approved R. L. Best
R. L. Best

EA:cs

Figure Number	Drawing Number
1	A-58979
2	A-58980
3	A-58981
4A	B-58982
4B	B-58983
5	A-58984
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6B	B-58986
7	A-58987
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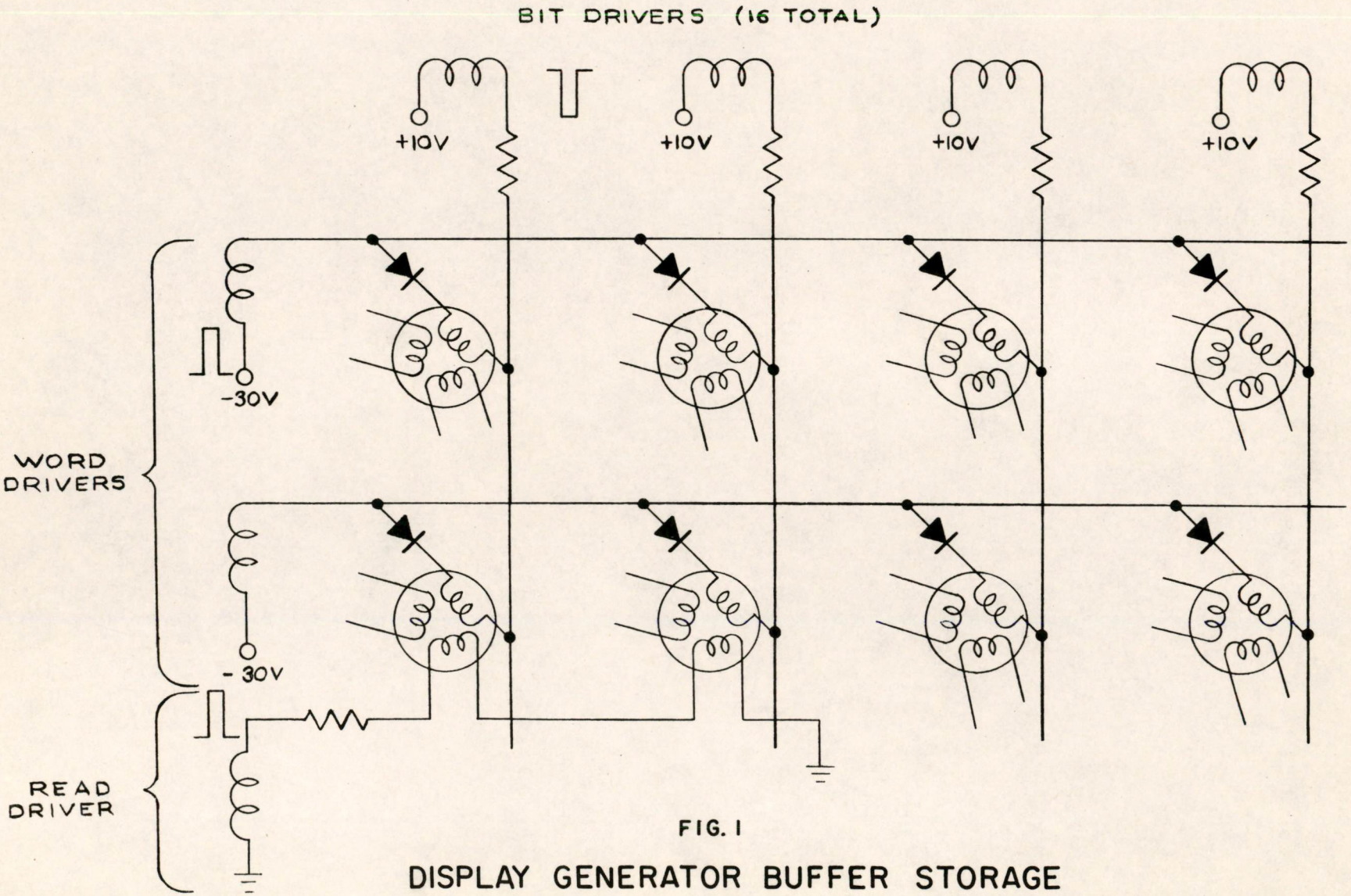


FIG. 1

DISPLAY GENERATOR BUFFER STORAGE

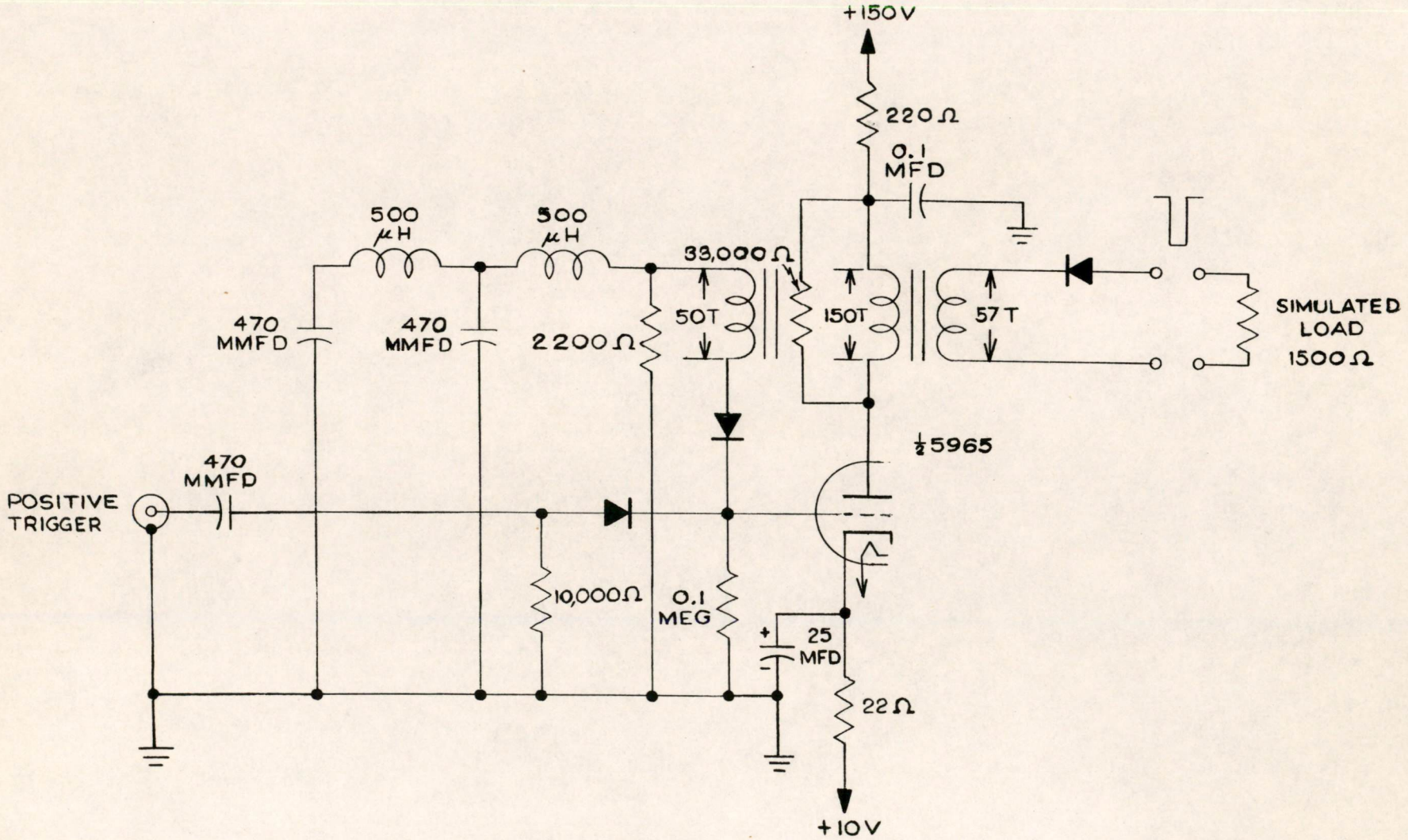
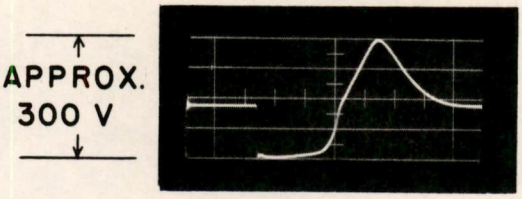
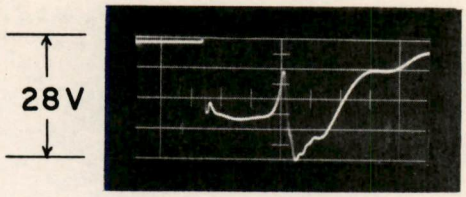


FIG. 2

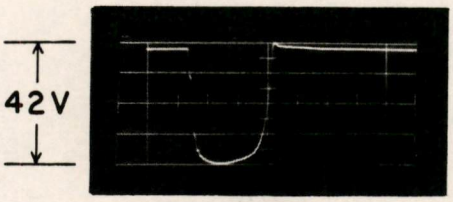
BIT DRIVER



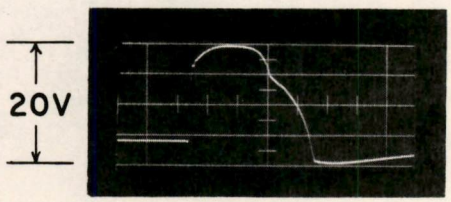
1 μ SEC./DIV.
PLATE VOLTAGE



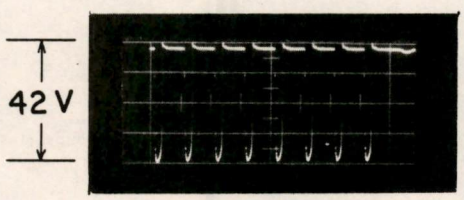
1 μ SEC./DIV.
DELAY LINE INPUT



1 μ SEC./DIV.
OUTPUT VOLTAGE



1 μ SEC./DIV.
GRID VOLTAGE



10 μ SEC./DIV.
BURST OF EIGHT
OUTPUT PULSES

FIG. 3

BIT DRIVER WAVEFORMS

A-58981

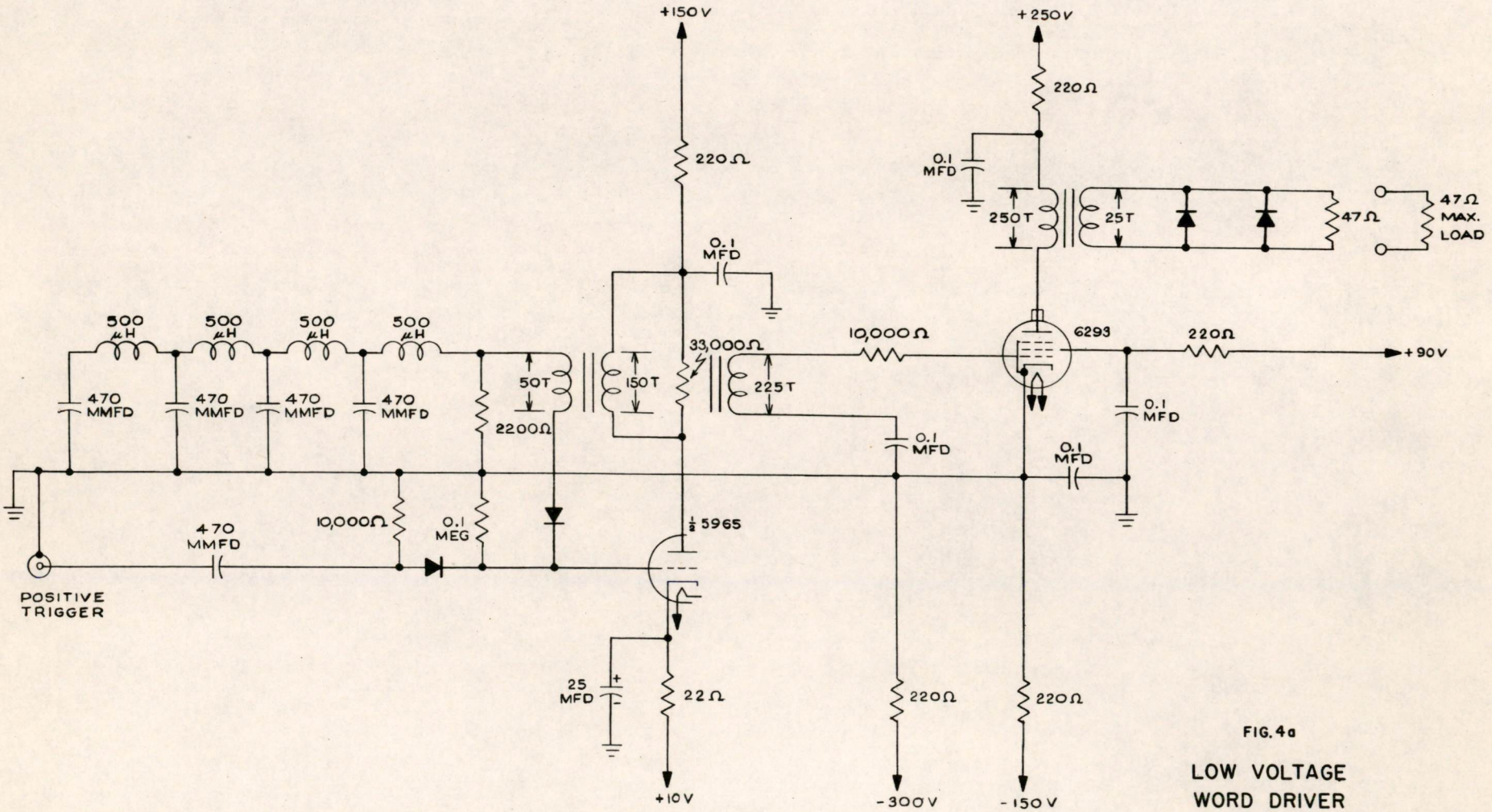


FIG. 4a

LOW VOLTAGE WORD DRIVER

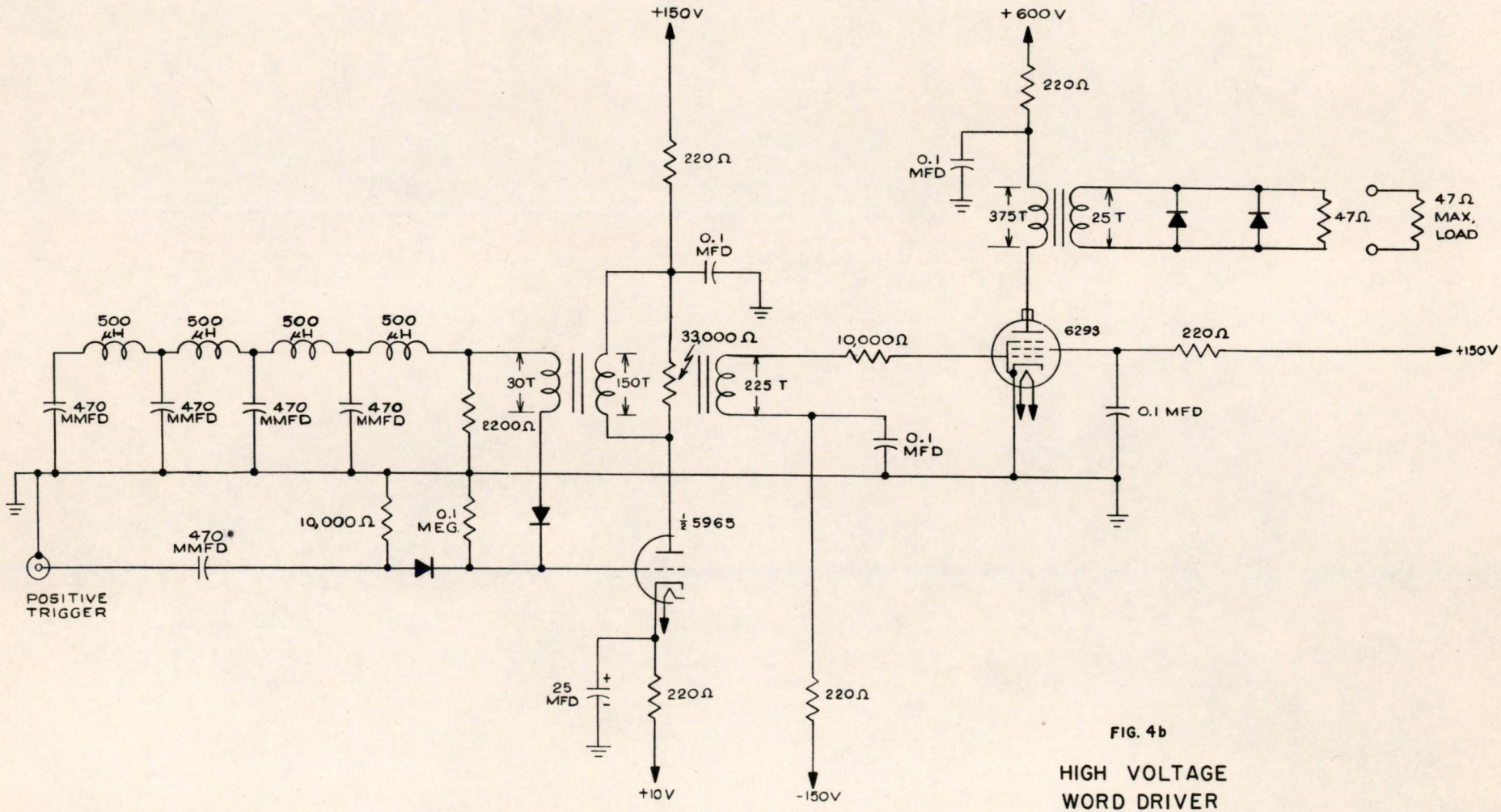
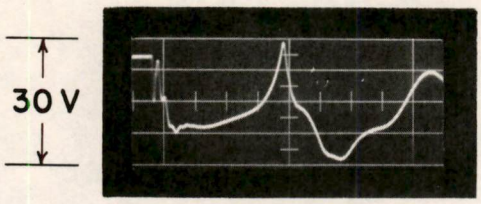
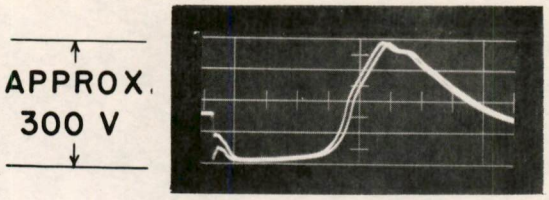


FIG. 4b

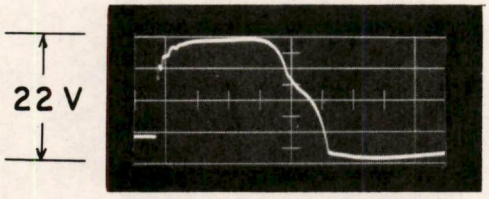
HIGH VOLTAGE
WORD DRIVER



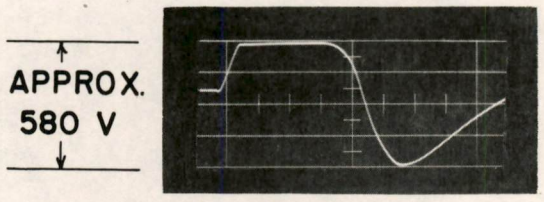
1 μ SEC./ DIV.
B.O. DELAY LINE
INPUT



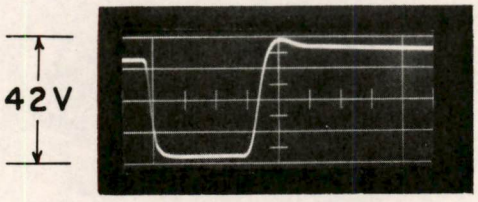
1 μ SEC./DIV.
B.O. PLATE VOLTAGE
(UPPER) (20 VOLT TRIGGER)
(LOWER) (30 VOLT TRIGGER)



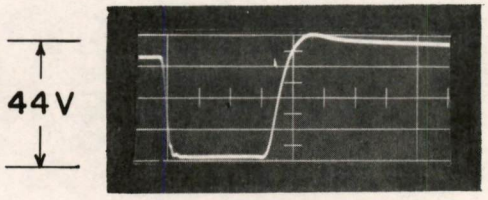
1 μ SEC./ DIV.
B.O. GRID VOLTAGE



1 μ SEC./ DIV.
P.A. GRID VOLTAGE



1 μ SEC./ DIV.
OUTPUT PULSE
(47 Ω LOAD)



1 μ SEC./ DIV.
OUTPUT PULSE
(UNLOADED)

FIG. 5

WORD DRIVER WAVEFORMS

A-58984

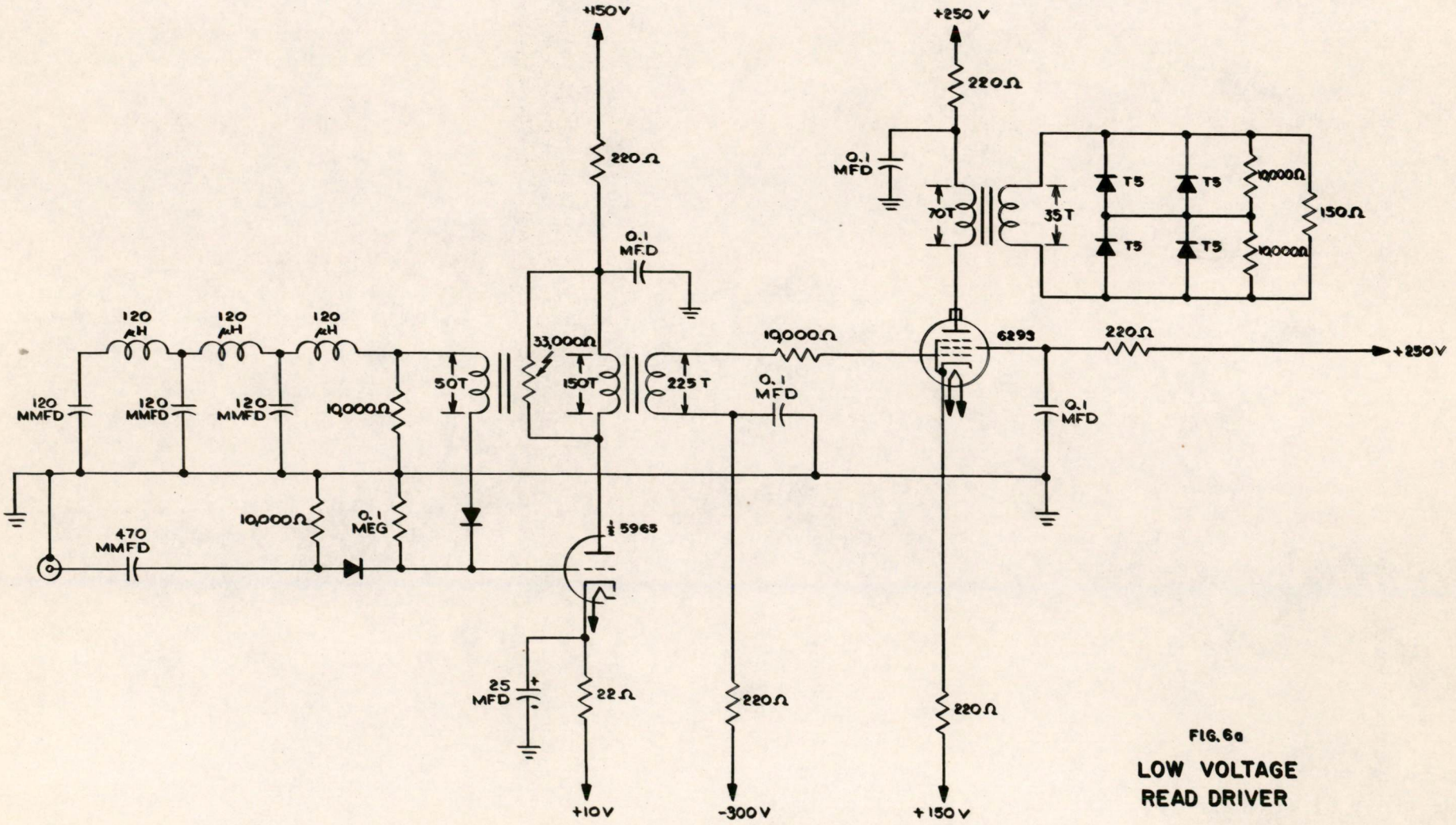


FIG. 6a

LOW VOLTAGE
READ DRIVER

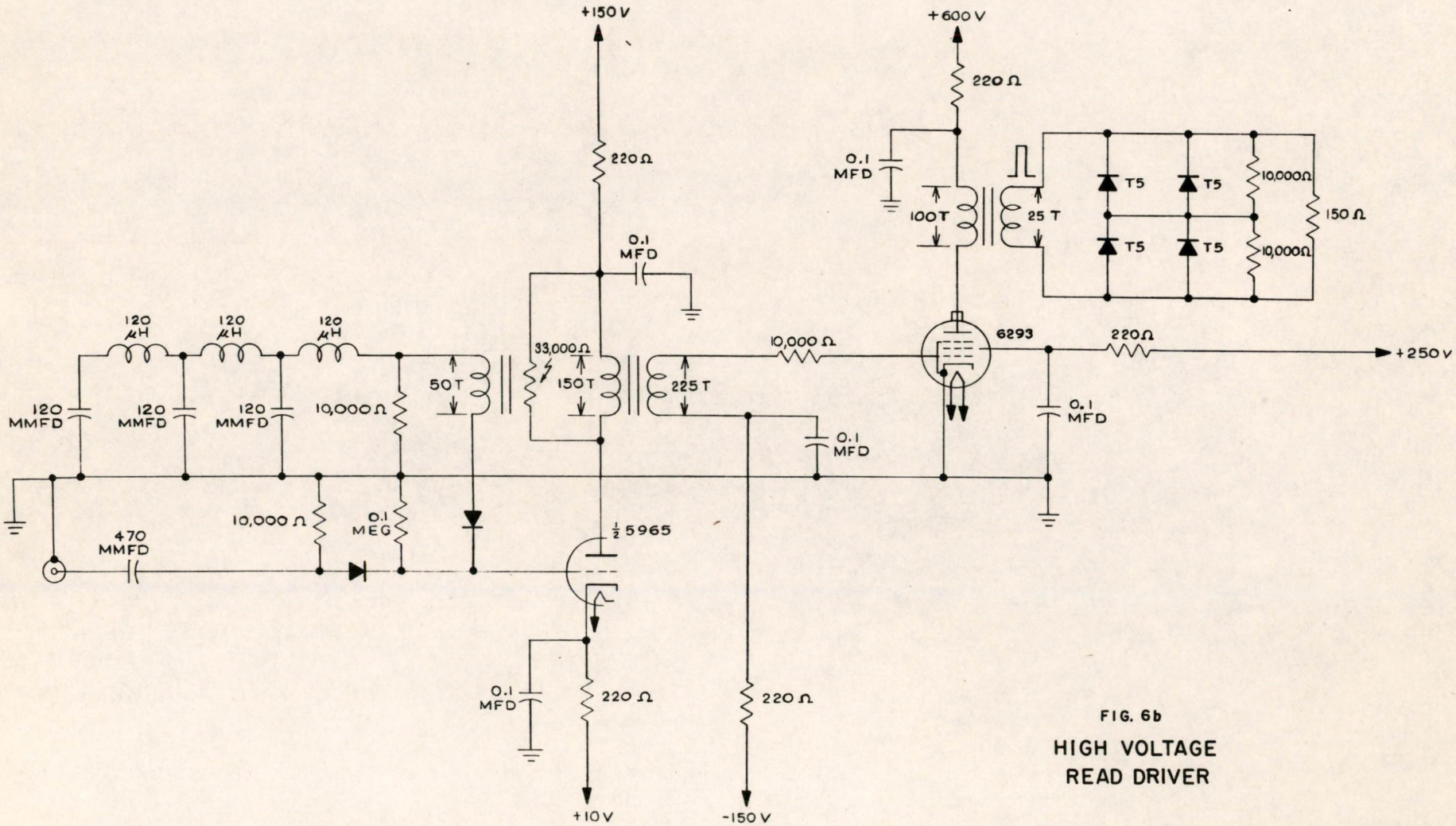
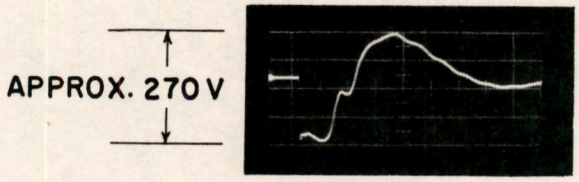
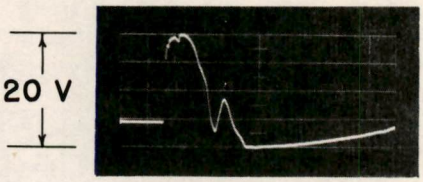


FIG. 6b

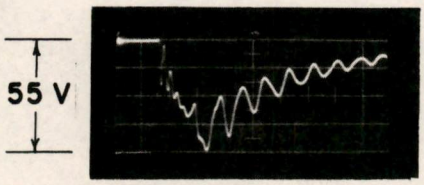
HIGH VOLTAGE
READ DRIVER



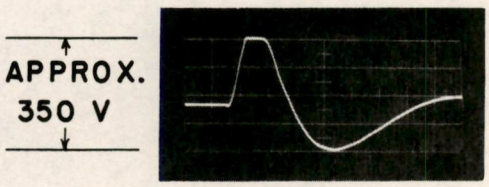
1 μ SEC. / DIV.
B.O. PLATE
VOLTAGE



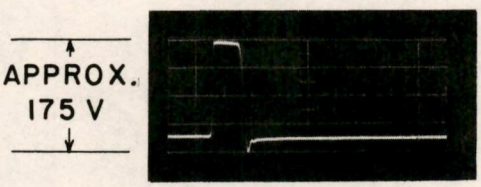
1 μ SEC. / DIV.
B.O. GRID
VOLTAGE



1 μ SEC. / DIV.
B.O. DELAY LINE
INPUT



1 μ SEC./DIV.
P.A. GRID
VOLTAGE



1 μ SEC./ DIV.
OUTPUT PULSE

FIG. 7

READ DRIVER WAVEFORMS

A-5898

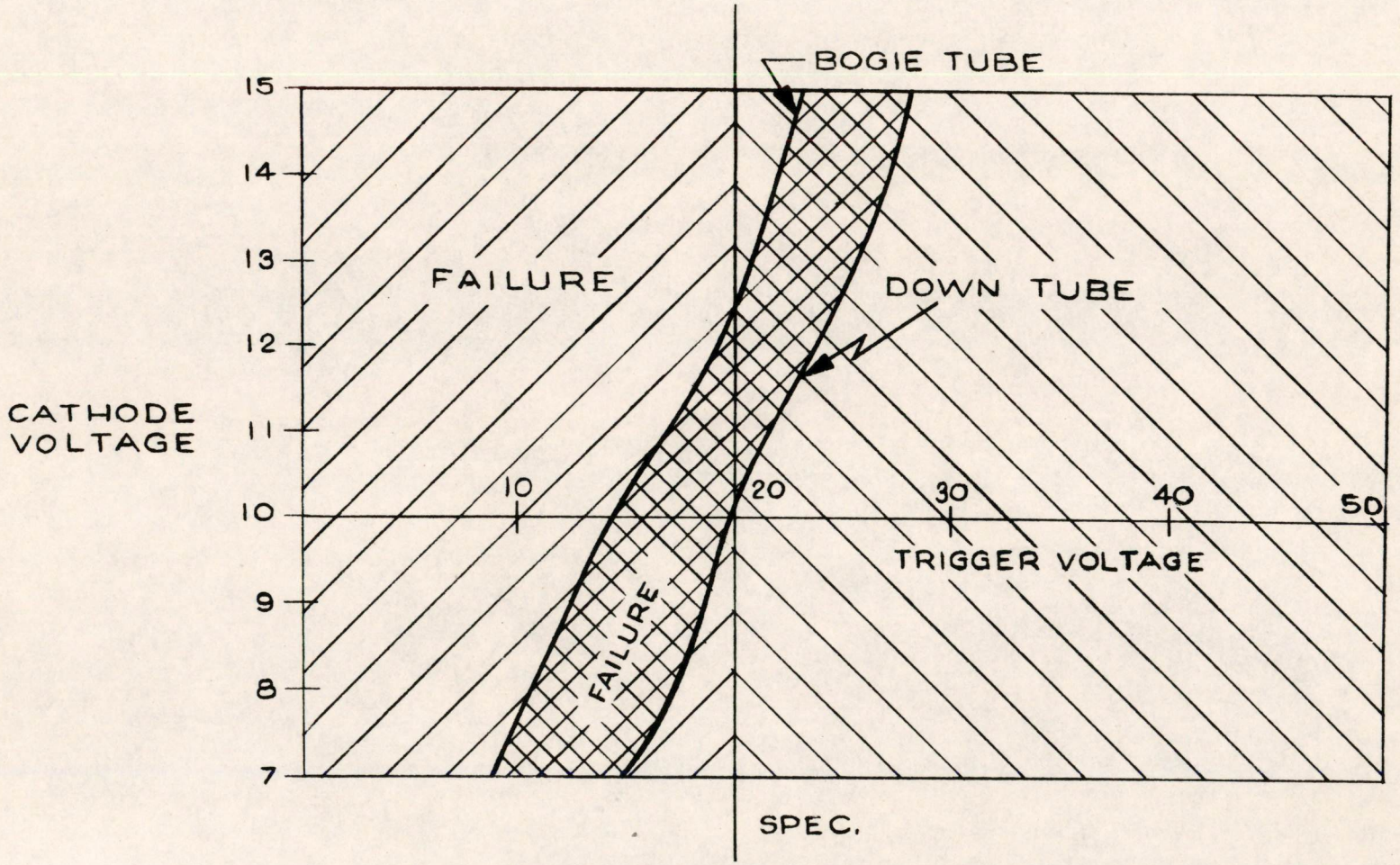


FIG. 8

BLOCK OSCILLATOR, BIT DRIVER

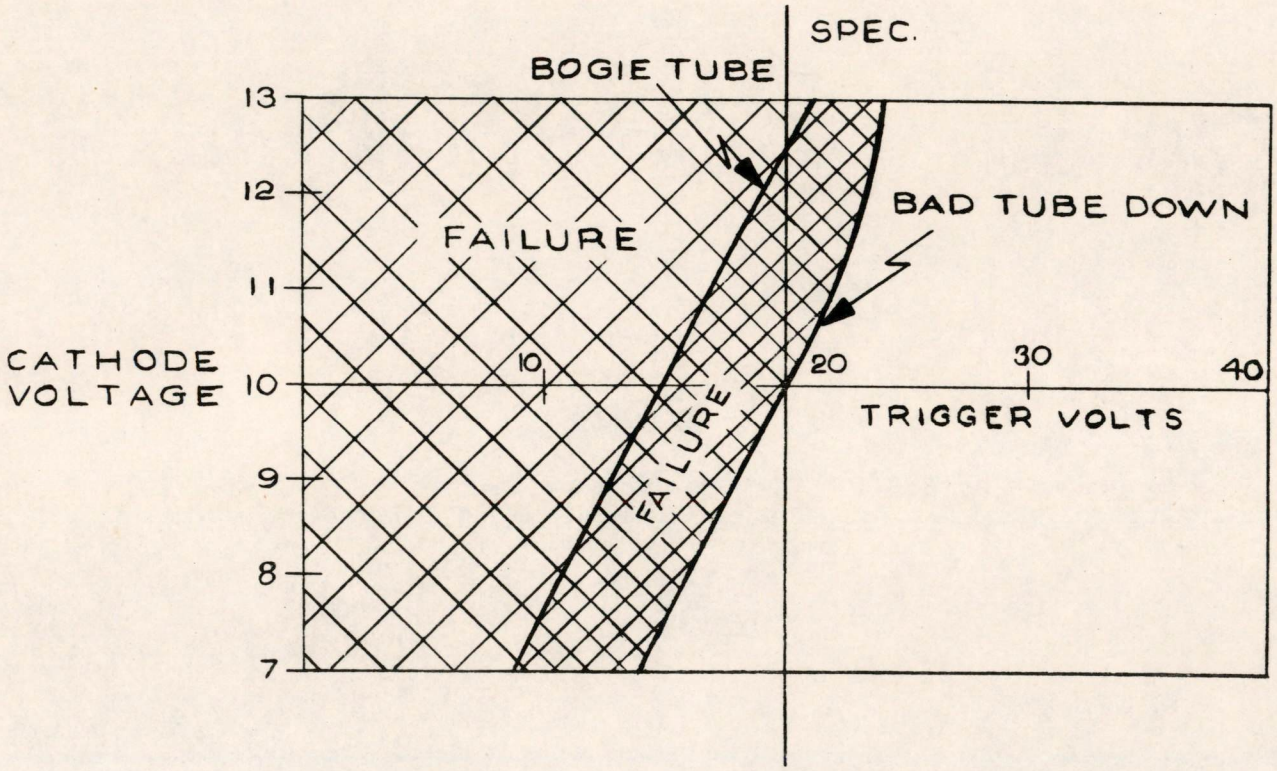


FIG. 9

BLOCK OSCILLATOR, WORD DRIVER

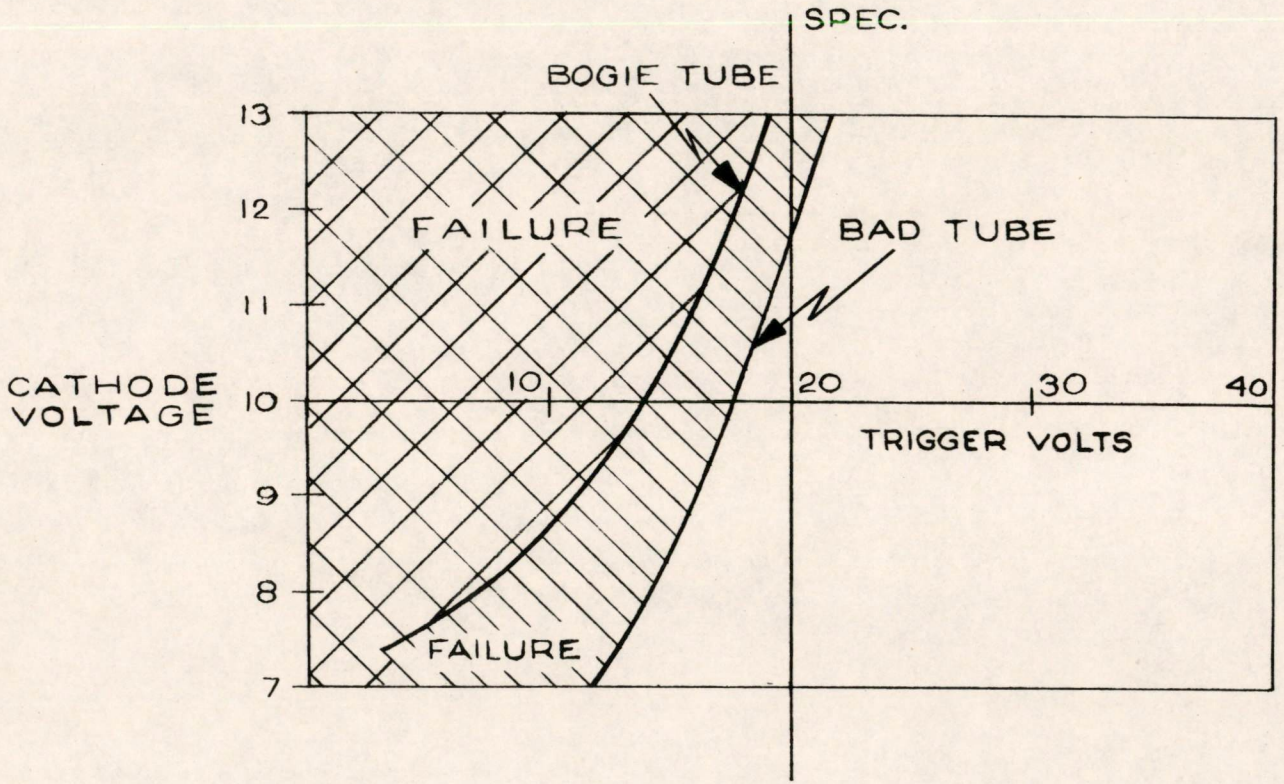


FIG. 10

BLOCK OSCILLATOR, READ DRIVER

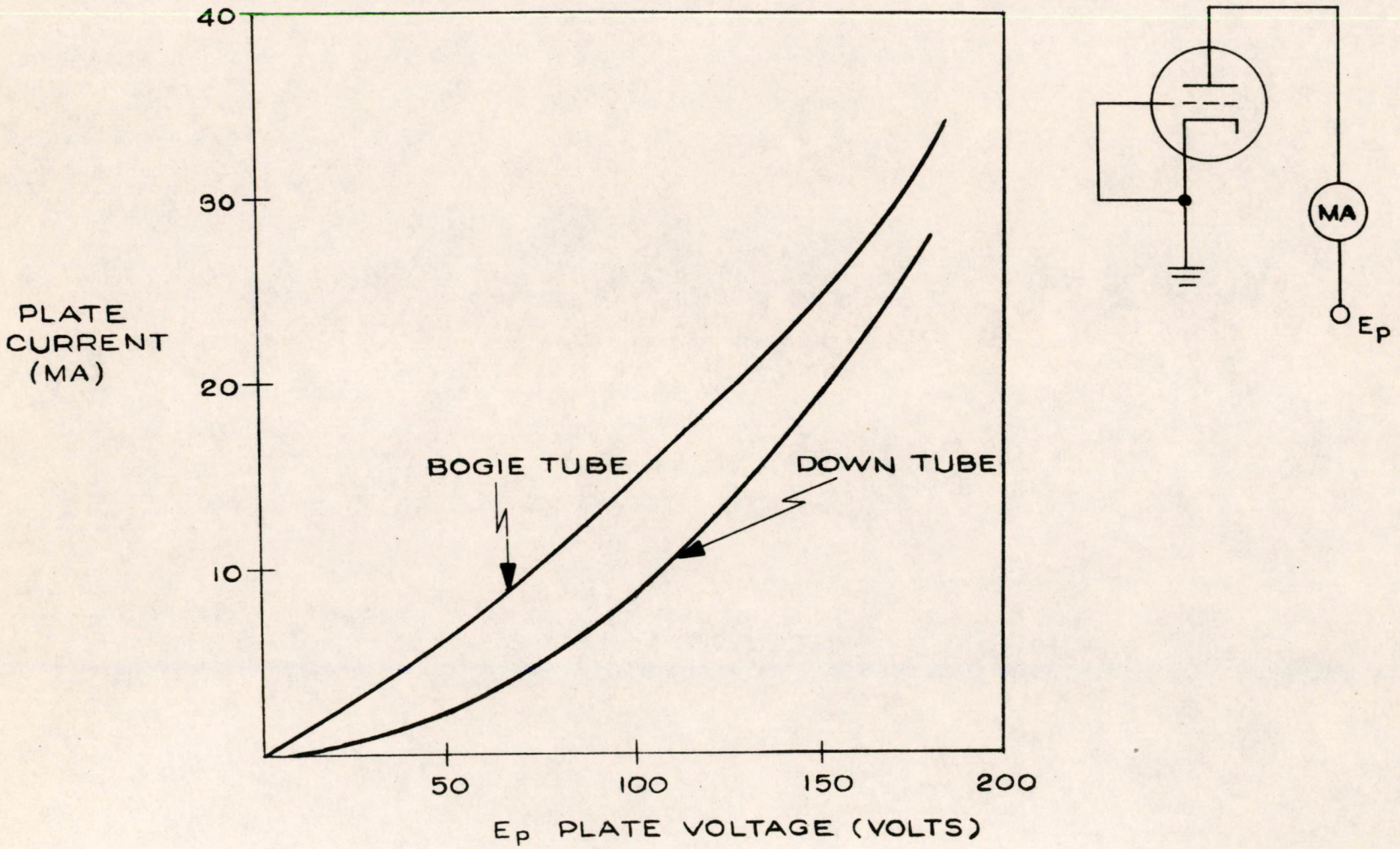


FIG. 11

5965 CHARACTERISTICS

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: BLOCKING OSCILLATOR CORE DRIVERS FOR USE IN DISPLAY GENERATOR BUFFER STORAGE.

To: N.H. Taylor

From: E. Anfenger

Date: June 7, 1954

Abstract: This paper lists the corrections on M-2820

Corrections

1. Page 2 under "word driver" item d, should read 20 to 40 volts instead of 10 to 40 volts.

2. Top of Fig. 1 should read 32 bit drivers instead of 16.

3. Fig. 4a return to -300^{V} should be from lower winding of 225T and condenser should go to ground as in Fig. 4b.

4. Fig. 6a cathode return 6293 should read -150^{V} instead of $+150^{V}$.

SIGNED E. Anfenger
E. Anfenger

APPROVED R L Best

EA:jb

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Division 6 - Lincoln Laboratory
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Cambridge 39, Massachusetts

SUBJECT: ONE ONE OR THE OTHER

To: Group 62 and 63 Staff and Secretaries

From: R. P. Mayer and W. N. Papian

Date: May 28, 1954

Discussion

When one writes a memo using binary numbers, such as one would use to describe one states or zero states in a binary device, he should not use one without at least one special symbol (e.g. ONE, or "one", or "1") otherwise the one is hard to interpret because one does not know whether one means one or one, that is, one one or the other one.

Conclusion:

There exist two small words we call "one,"
Which can cause great confusion, or fun.
Use binary "ONE,"
To distinguish from "one"
So we'll know you mean "ONE" and not "one."

Signed R.P. Mayer
R.P. Mayer

Approved W.N.P.
W.N. Papian

RPM:WNP:cs

N.H. Daggett
John Bennett
W. Wittenberg (IBM)

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: TEST RESULTS ON THE DCL MEMORY PLANE

To: F. E. Vinal

From: E. A. Guditz

Date: 28 May 1954

Abstract: The DCL plane (C25) is compared with a standard MTC plane which has General Ceramics cores. Except for requiring slightly higher driving currents for maximum output, the DCL plane compares favorably with the MTC planes and could, in fact, operate as a substitute MTC plane without seriously impairing the system's margins.

Plane C25, herin referred to as the DCL plane, contains cores made at this laboratory by Group 63. These cores are designated DCL-1-180. The object of this test was to find the optimum driving current for the plane and the worst ONE-ZERO ratio. Data was taken showing the relationship of Sensing Amplifier Gate Tube bias to Strobe Time for four values of driving current and four different patterns.

Patterns of all ONES and all ZEROS were used to find optimum driving current. Data was taken at 1.0a., 0.9a., 0.8a., and 0.7a. The attached graphs SA-48528-G through SA-48531-G show the comparison of the DCL plane (C25-dotted line) with the MTC plane (C21-solid line) under these conditions. Note that the MTC plane has its maximum ONE-ZERO ratio in the 0.8a. to 0.9a. region while the DCL plane has an increasing ONE-ZERO ratio right up to the maximum available driving current of 1.0a. Also, the ONE-ZERO ratio of the DCL plane at this maximum available current is approximately equal to the best ONE-ZERO ratio available from the MTC plane. It should be noted that at the best operating current for the MTC plane the DCL plane has a very good ONE-ZERO ratio and is quite capable of operating in conjunction with MTC planes.

Graphs SA-48532-G through SA-48535-G show the operating margins for the two complementary patterns of complemented pairs-checkerboard for driving current values of 0.8a. and 1.0a. Again it can be seen that the margins are still increasing at the maximum available driving current of 1.0a. In these graphs a comparison is made not with the MTC plane but with and without the Post-Write Disturb current. It is interesting to note that the Post-Write Disturb current is most beneficial for the pattern with zeros in the corners (Graphs SA-48534-G and SA-48535-G). The reason for this is not understood.

Observation of Sensing Winding output voltage showed that the spread in outputs is very small and is as good or better than that observed from the MTC planes.

It is felt that a memory made of planes using these cores and operated at its optimum currents would have operating margins at least equal to those of the present 64 x 64 memory.

SIGNED E. A. Gudita
E. A. Gudita

APPROVED W.N.P.
W.N. Papian

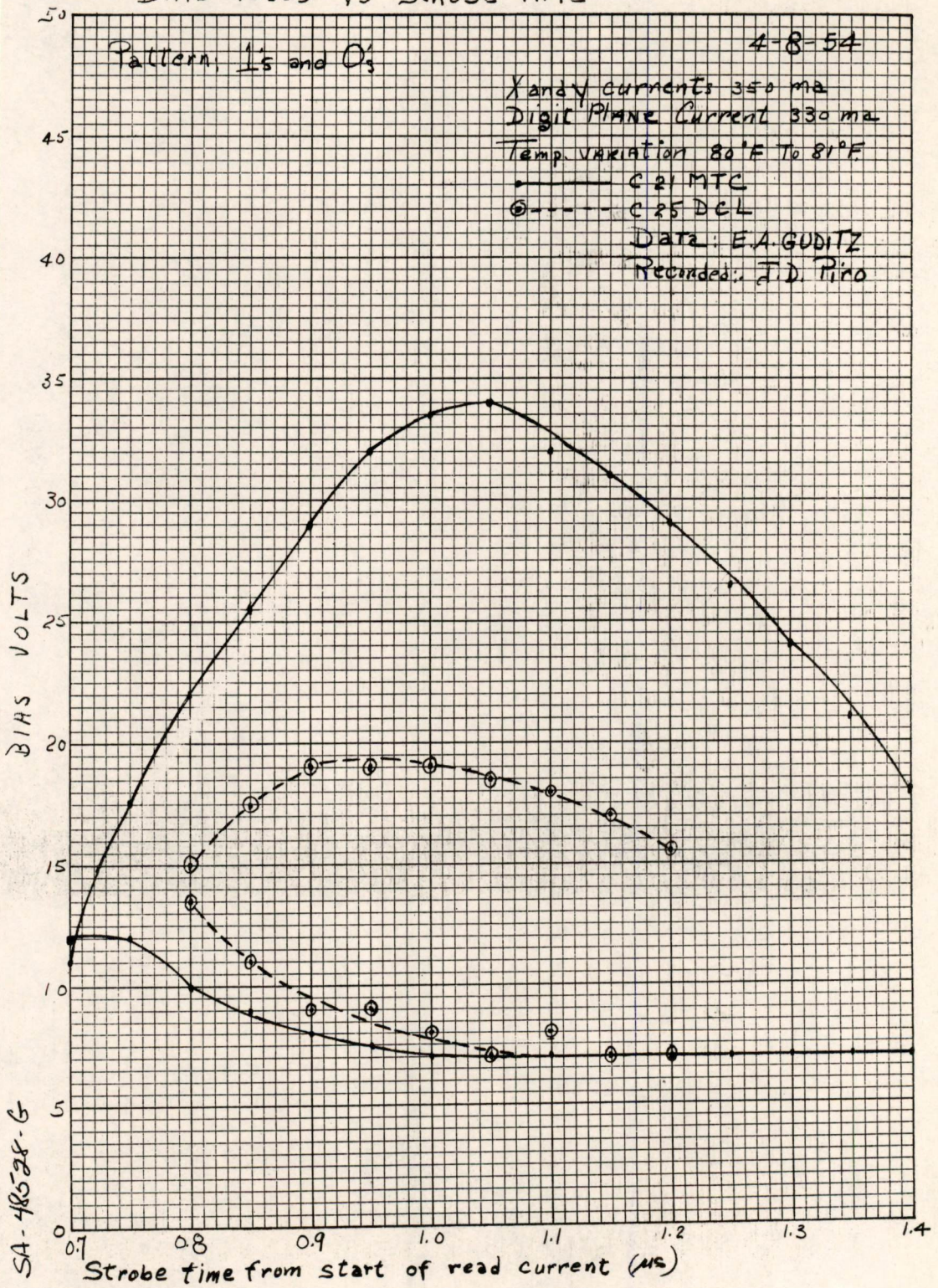
EAG:jb

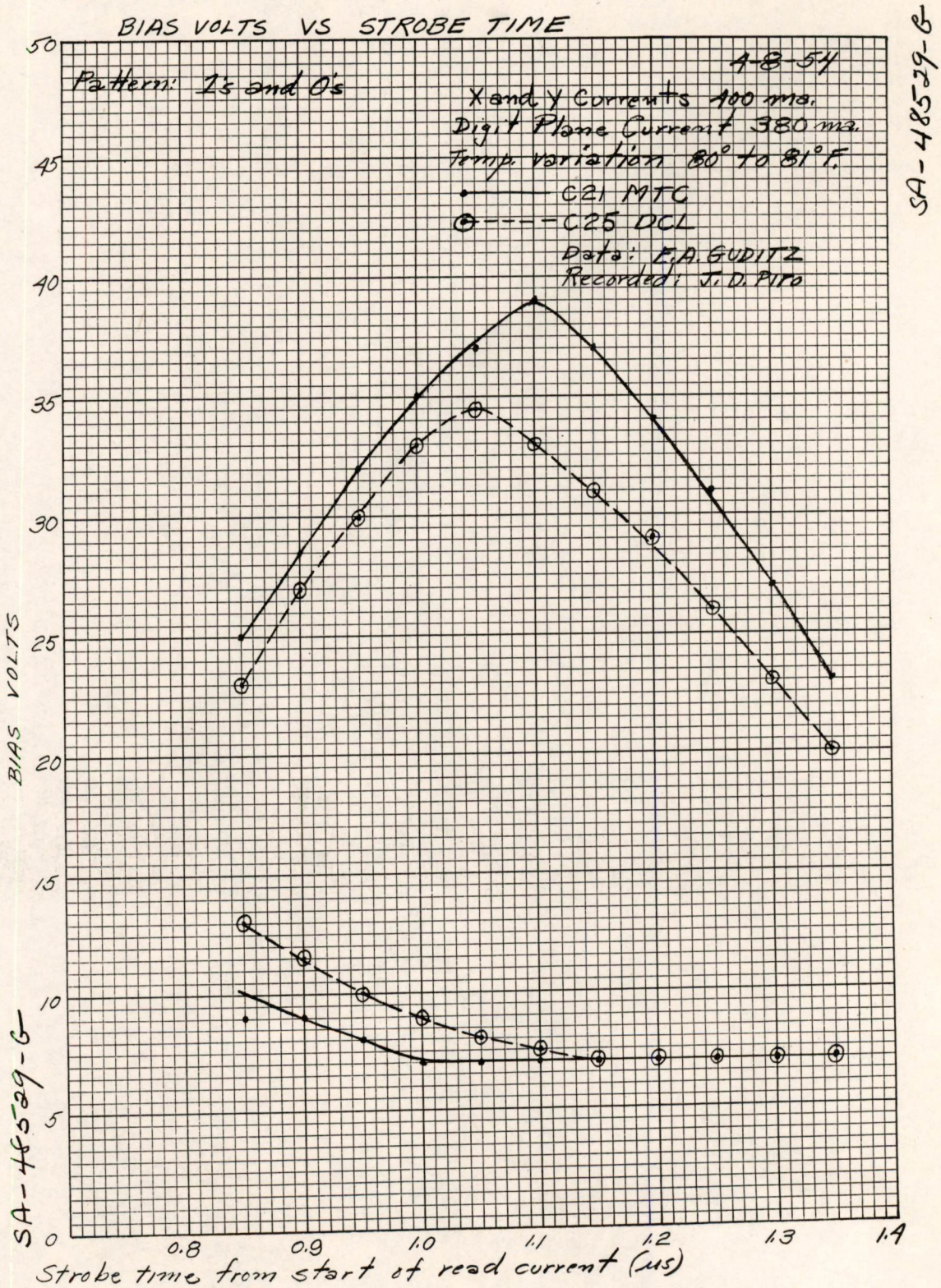
Group 63 Staff (Group 63)
Magnetic Memory Section Staff (Group 62)
W. Wittenberg (IBM)

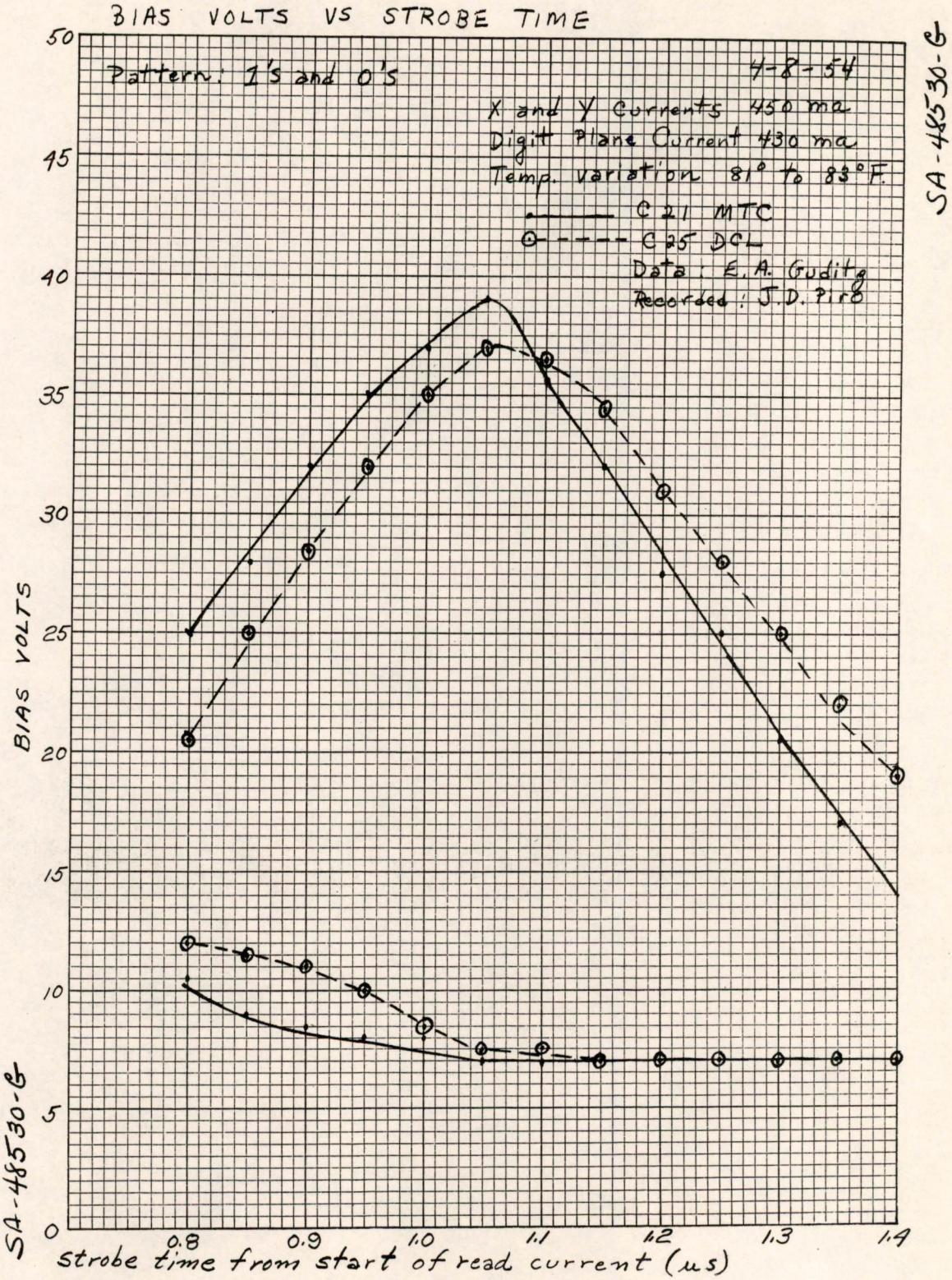
Graphs

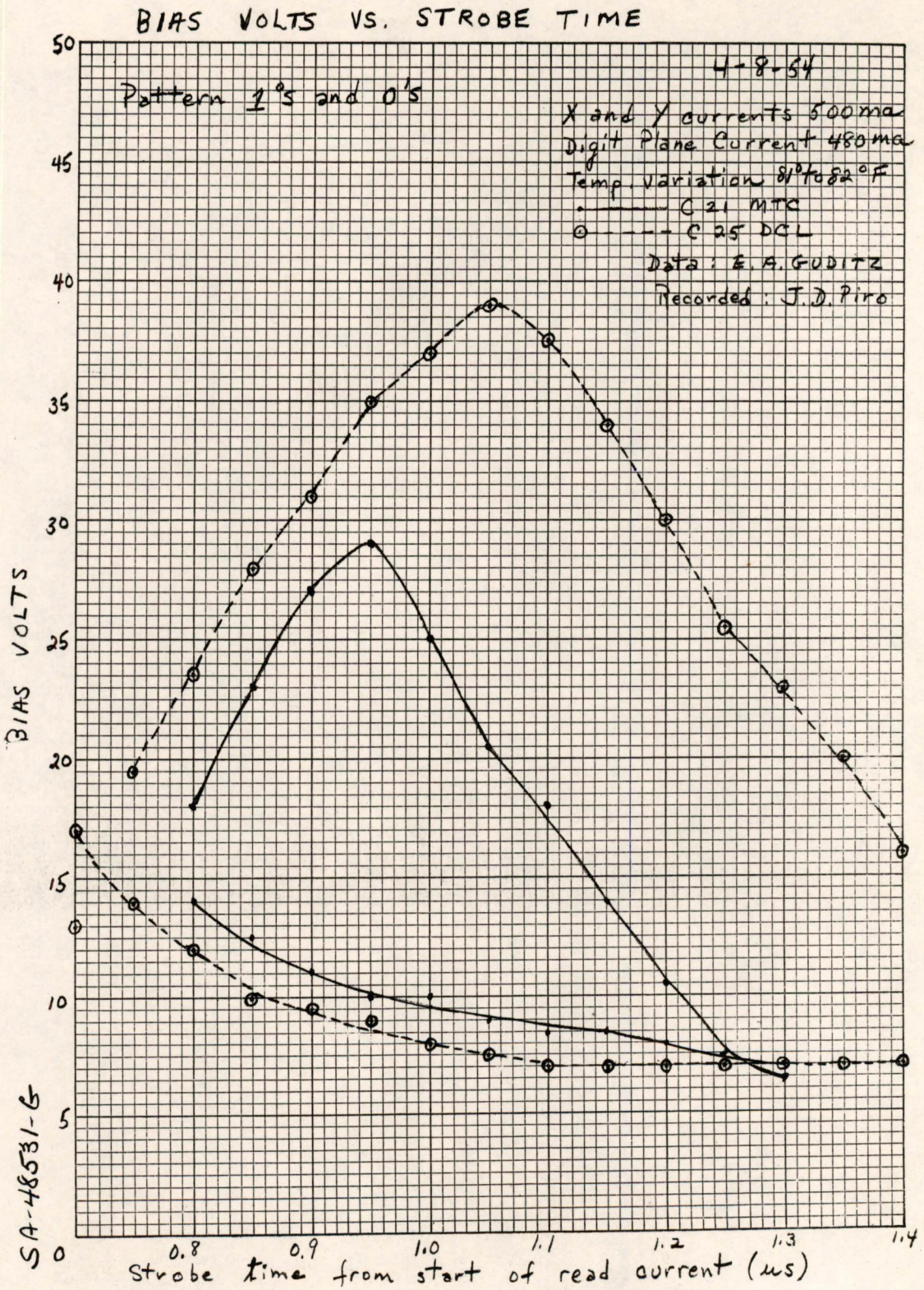
SA-48528-G
SA-48529-G
SA-48530-G
SA-48531-G
SA-48532-G
SA-48533-G
SA-48534-G
SA-48535-G

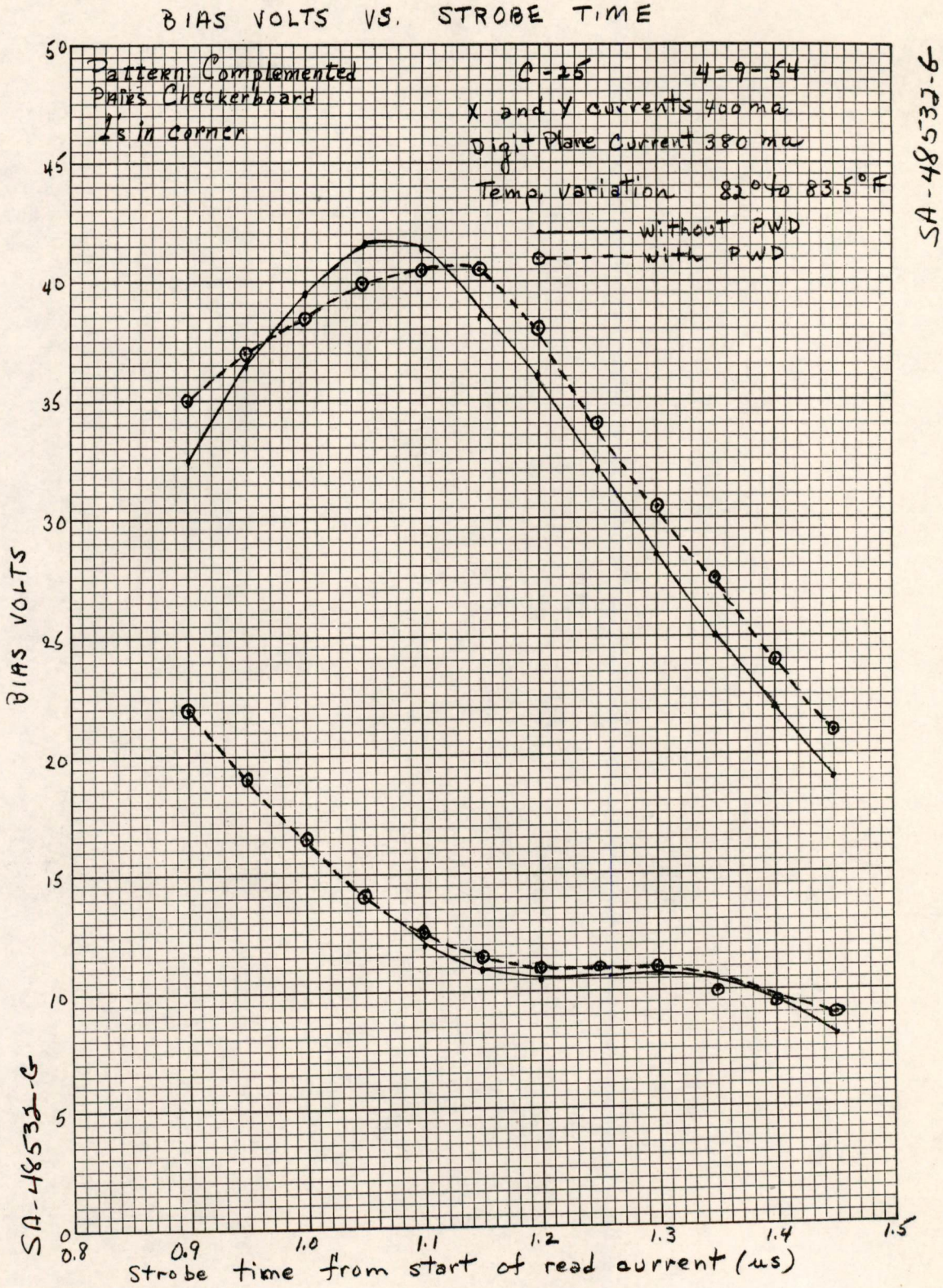
BIAS VOLTS VS STROBE TIME

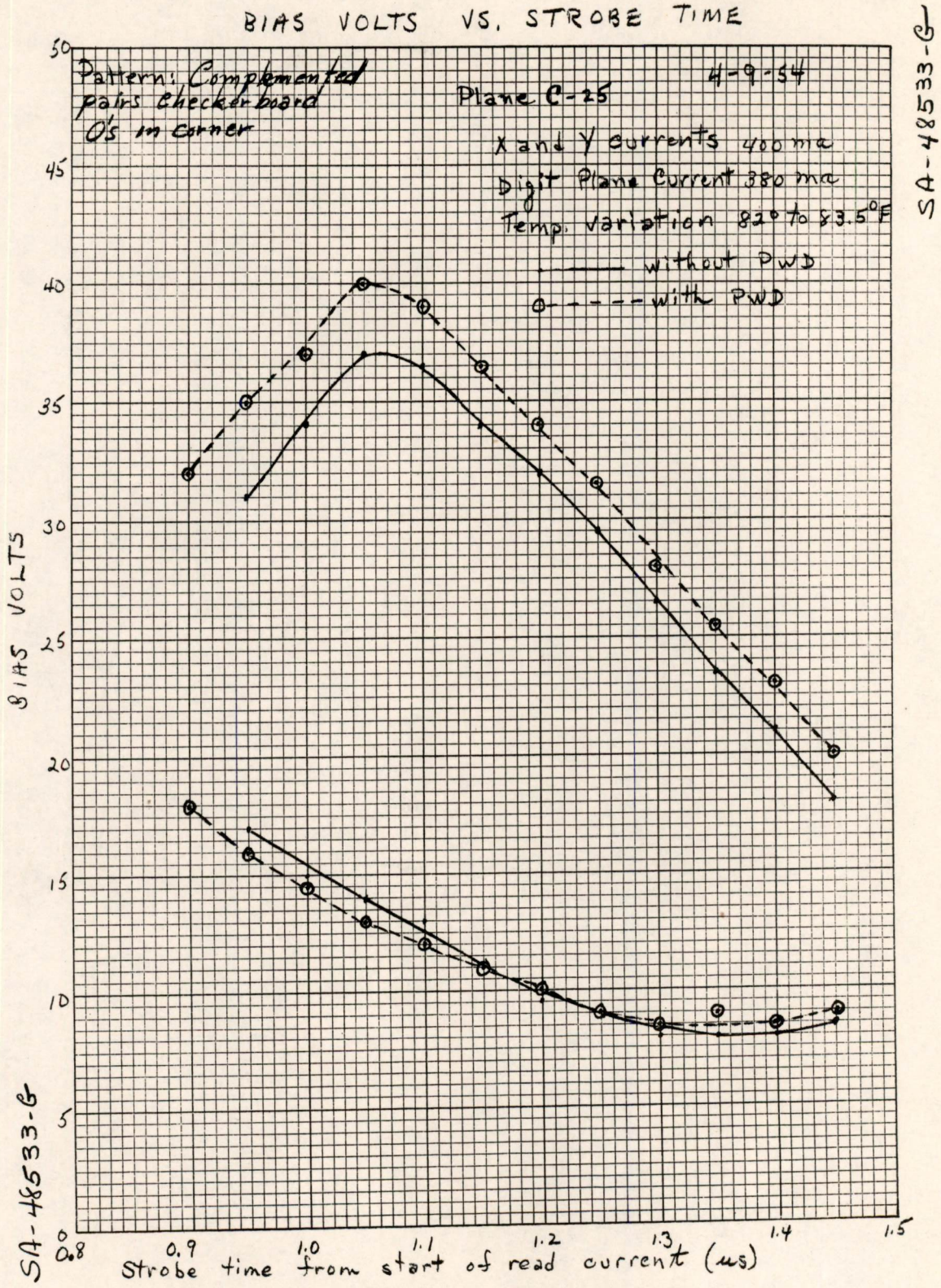


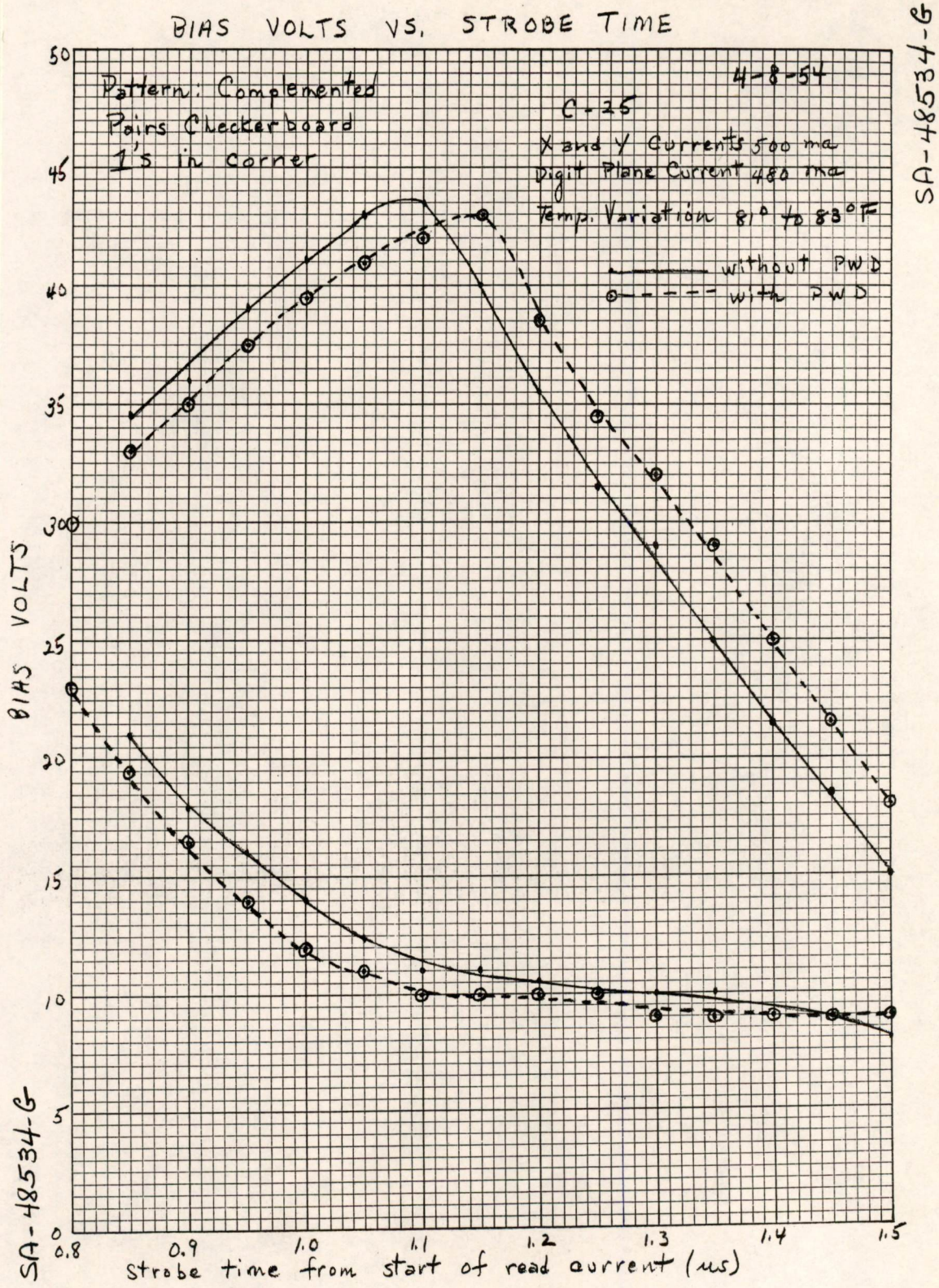

BIAS VOLTS VS STROBE TIME
4-8-54
Pattern: 1's and 0's
X and Y Currents 400 ma.
Digit Plane Current 380 ma.
Temp. variation 80° to 81° F.
C21 MTC
C25 DCL
Data: E.A. GUDITZ
Recorded: J. D. PIRO
SA-48529-G
BIAS VOLTS
50
45
40
35
30
25
20
15
10
5
0
0.8
0.9
1.0
1.1
1.2
1.3
1.4
Strobe time from start of read current (μs)
SA-48529-G

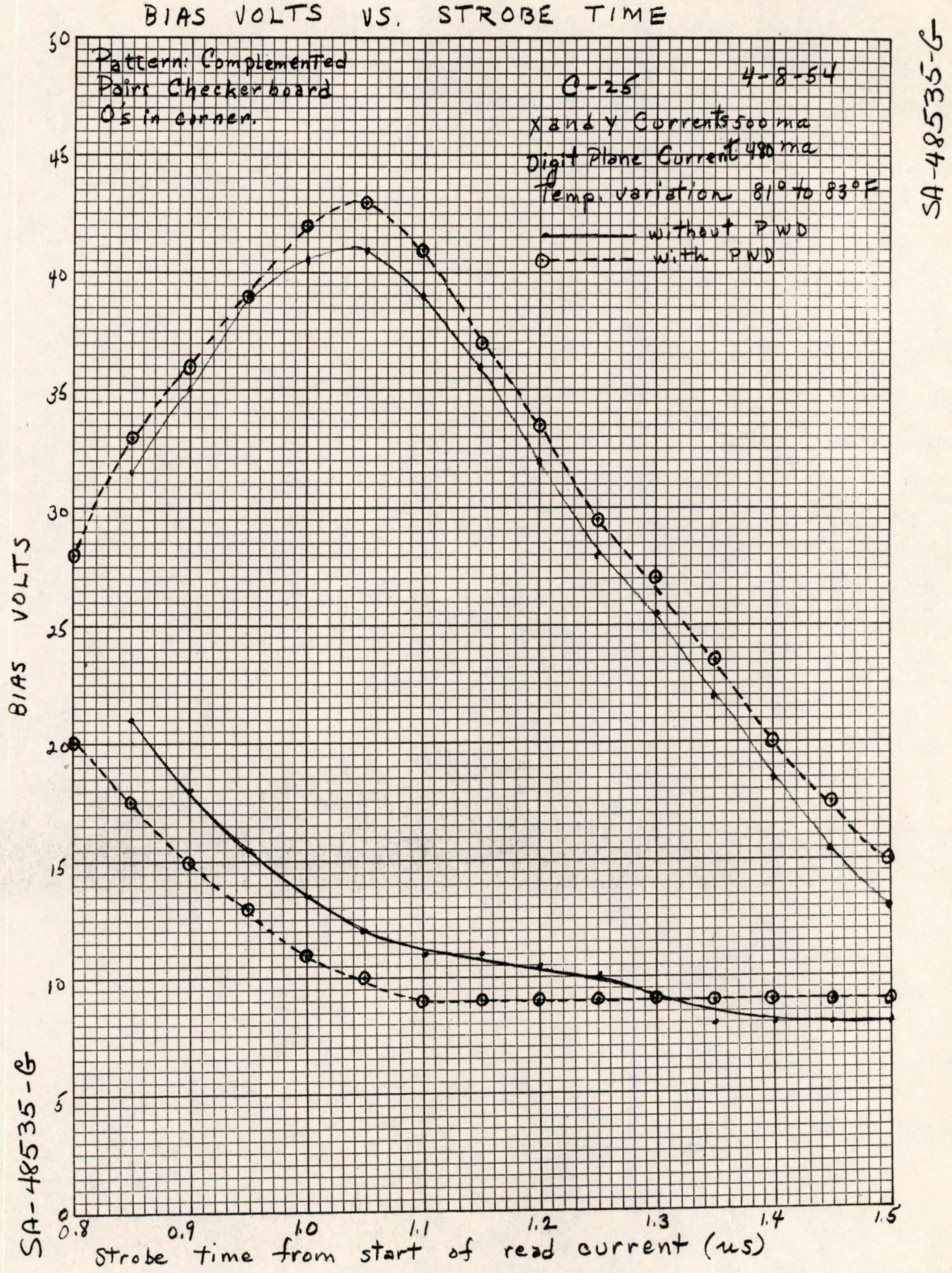

BIAS VOLTS VS STROBE TIME
Pattern: 1's and 0's
4-8-54
X and Y currents 450 ma
Digit Plane Current 430 ma
Temp. variation 81° to 83° F.
C 21 MTC
C 25 DCL
Data: E. A. Gudit
Recorded: J. D. Pir
SA-48530-G
BIAS VOLTS
50
45
40
35
30
25
20
15
10
5
0
0.8
0.9
1.0
1.1
1.2
1.3
1.4
strobe time from start of read current (μs)
SA-48530-G


BIAS VOLTS VS. STROBE TIME
4-8-54
Pattern 1's and 0's
X and Y currents 500 ma
Digit Plane Current 480 ma
Temp. Variation 81° to 82° F
C 21 MTC
C 25 DCL
Data: E. A. GUDITZ
Recorded: J. D. Piro
SA-48531-G
BIAS VOLTS
50
45
40
35
30
25
20
15
10
5
0
0.8
0.9
1.0
1.1
1.2
1.3
1.4
Strobe time from start of read current (μs)
SA-48531-G


BIAS VOLTS VS. STROBE TIME
Pattern: Complemented Plates Checkerboard 1's in Corner
C-26
4-9-54
X and Y currents 400 ma
Digit Plane Current 380 ma
Temp. variation 82° to 83.5° F
without PWD
with PWD
SA-48532-6
BIAS VOLTS
0
5
10
15
20
25
30
35
40
45
50
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
Strobe time from start of read current (μs)
SA-48532-6


BIAS VOLTS VS. STROBE TIME
Pattern: Complemented pairs Checkerboard O's in Corner
4-9-54
Plane C-25
X and Y currents 400 ma
Digit Plane Current 380 ma
Temp. variation 82° to 83.5°F
without PWD
with PWD
BIAS VOLTS
Strobe time from start of read current (μs)
SA-48533-G
SA-48533-G


BIAS VOLTS VS. STROBE TIME
Pattern: Complemented Pairs Checkerboard 1's in corner
4-8-54
C-25
X and Y Currents 500 ma
Digit Plane Current 480 ma
Temp. Variation 81° to 83°F
without PWD
with PWD
BIAS VOLTS
Strobe time from start of read current (μs)
SA-48534-G
SA-48534-G


BIAS VOLTS VS. STROBE TIME
Pattern: Complemented Pairs Checkerboard 0's in corner.
C-25
4-8-54
X and Y Currents 500 ma
Digit Plane Current 480 ma
Temp. variation 81° to 83°F
without PWD
with PWD
BIAS VOLTS
Strobe time from start of read current (μs)
SA-48535-G
SA-48535-G

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: XD-I DIGIT-PLANE DRIVER

To: N. Taylor

From: D. Shansky

Date: 28 May 1954

Abstract: A self-balancing bridge is utilized in conjunction with an "and" and an "or" gate input to satisfy the wave form and gating specifications on the driver for a magnetic core memory digit plane winding.

The digit plane driver is a circuit which combines the logical function of both an "and" and an "or" gate with a regulated pulse current source. For purposes of an explanation of circuit operation it is most convenient to simplify the discussion by describing the operation of the 2 logical blocks independently of one another.

Regulated Pulse Current Source.

This portion of the circuit consists of 5 cathodes in a feedback loop. Two of these cathodes are in a difference amplifier (V_{2II}, V_{3I}), which serves to compare a signal voltage produced by current flow through a sampling resistor, to a constant voltage level established by a potentiometer connected across a power supply. A third cathode (V_{3II}) serves to amplify and invert the output voltage of the difference amplifier and drive the grids of the final tube ($V_{4I,II}$), which is a 5998. The cathodes of the difference amplifier are normally held up to + 10 volts by a cathode follower (V_{2I}), so that these tubes are normally cut off. The inverter-amplifier tube (V_{3II}) is normally conducting, while the driver tube ($V_{4I,II}$) is normally cut off by the presence of a large negative bias. During the pulse, the cathodes of the difference amplifier (V_{2II}, V_{3I}) are allowed to fall by applying a negative gate to the grid of the cathode follower (V_{2I}) whose cathode is connected to the cathodes of the difference amplifier. Therefore, the plate of the difference amplifier will fall and the change in voltage will appear at the grid of the normally conducting inverter. The plate of the inverter-amplifier (V_{3II}) will rise at a rate determined by the plate load resistor and stray, input and output capacities. This change in voltage will be coupled over to the grids of the normally off 5998 turning them on. The voltage developed across the sampling resistor ($R_{29,30}$) by current flowing through the 5998 and the load is fed back to the difference amplifier where it is compared to a reference voltage applied to the other grid of the difference amplifier. During the pulse then, this regulated pulse current source becomes a self-balancing bridge. The back voltage produced

by the load is fed back to the difference amplifier (via C_8) as a common mode signal to insure an adequate current source regardless of load variation.

This particular geometry has resulted in a circuit which has extremely broad tolerances with respect to tubes, component values, and supply voltages, as the accompanying curves indicate, since the circuit inherently adjusts itself to compensate for these variations.

Figure #4, 5 and 6 portray the operating margins of the cathodes in the feed-back loop. The bias on the 5998 output tube was chosen as the marginal checking voltage in each case since the internal loop gain may most conveniently be changed by varying this voltage. A curve on V_{2II} (the cathode follower portion of the difference amplifier) is not included because it was found that the plate supply of this tube could be made negative with respect to the cathode without causing failure. A diode is all that is apparently necessary here. (By way of explanation of this apparently superfluous cathode, I might point out that the specification on output current change was originally $\pm$ 2%. This cathode was included to minimize the change in output current due to variations in contact potential of the difference amplifier. However, in view of the fact that unit failure had to be related to system failure, and in view of the experience gained in M.T.C., failure was defined as a 15% change in current.) In the case of tube V_3 failure was defined as change in output pulse rise time of $\pm$ 0.2 μsec. This change in timing is compatible with system requirements. Failure was defined in similar manner for all the other cathodes in the circuit with the exception of V_1, where the failure was evidenced by a 15% change in output current.

"And", "Or" Gate Circuitry.

Since it was necessary that the grid of V_2 be allowed to fall more than forty volts because of the common mode signal on the difference amplifier (V_2, V_3) produced by the back voltage developed in the load, it was necessary to provide some amplification of the input signal (Flip-Flop output). A 7AK7 was used to provide the necessary amplification and perform the "and" gating function. The output of the "and" gate is fed to a diode negative "or" gate. The other input to the negative "or" gate is connected to the "Post-Write-Disturb" gate generator, which provides a negative going gate of the proper amplitude (+10 to -40).

The margins of operation of the 2 cathodes in this portion of the circuit are shown in figs 2 and 3. In the case of Tube V_2 failure was defined as a change in timing as previously mentioned, while failure of the 7AK7 manifested itself as a change in output current.

Conclusion

As a result of the experimental work which was done in garnering the information upon which the preceding report was based, it became apparent that a redesign of the unit could eliminate some cathodes and

ease the input driving requirements. The Digit Plane Driver has therefore been redesigned so as to eliminate two cathodes and operate from standard voltage levels. This work was not completed in time to meet the XD-1 production schedules. A report on the improved version of this circuit is being prepared and will be forthcoming shortly.

SIGNED David Shansky
D. Shansky

APPROVED R. L. Best
R. L. Best

DS:jb

Attached

Fig 1 B-59149
Fig 2 - SA48525-G
Fig 3 - SA48523-G
Fig 4 - SA48527-G
Fig 5 - SA48526-G
Fig 6 - SA48524-G

B-59149

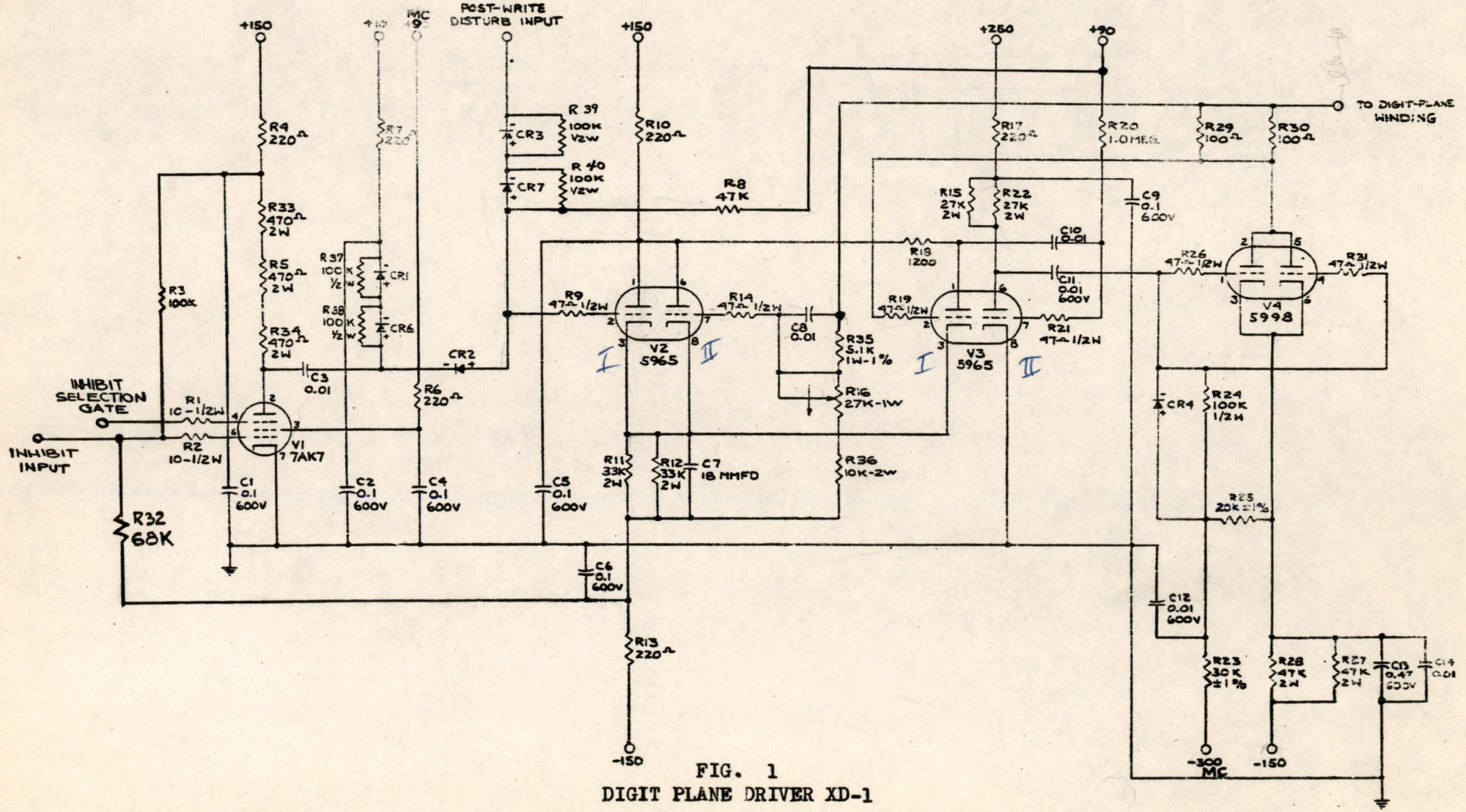


FIG. 1
DIGIT PLANE DRIVER XD-1

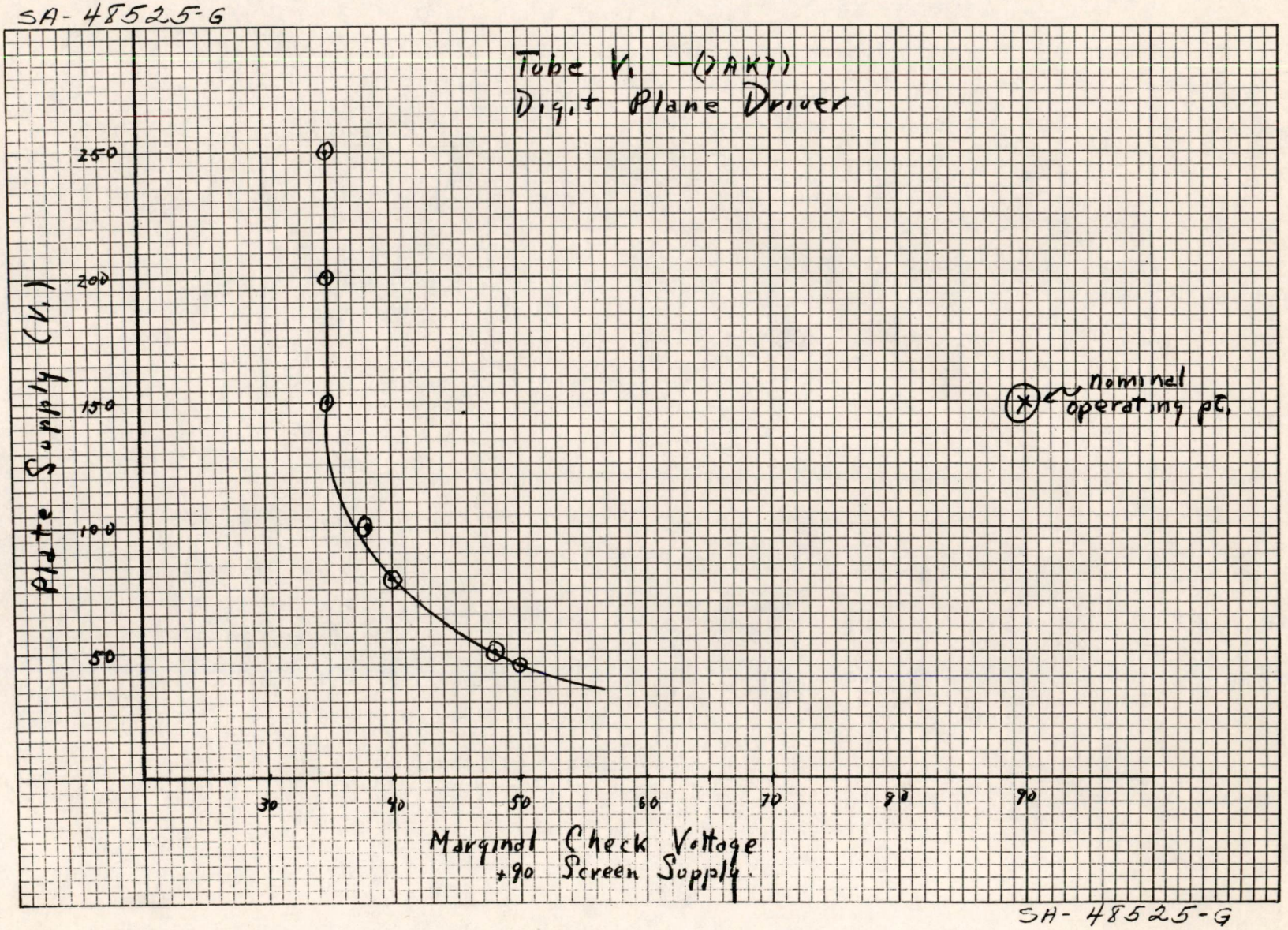

SA-48525-G
Tube V1 — (7AK7)
Digit Plane Driver
Plate Supply (V1)
250
200
150
100
50
30
40
50
60
70
80
90
nominal operating pt.
Marginal Check Voltage
+90 Screen Supply
SA-48525-G

FIG. 2

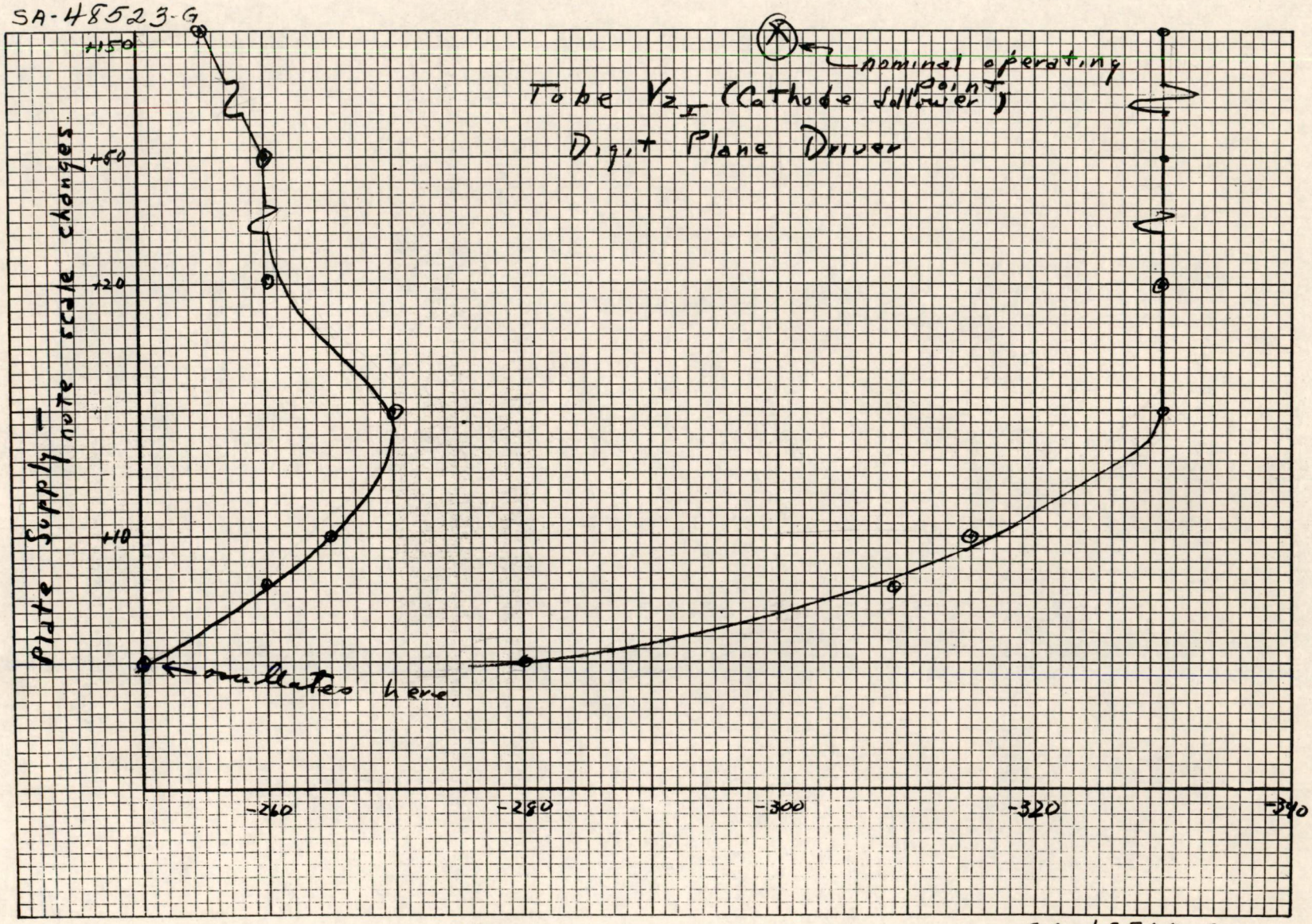
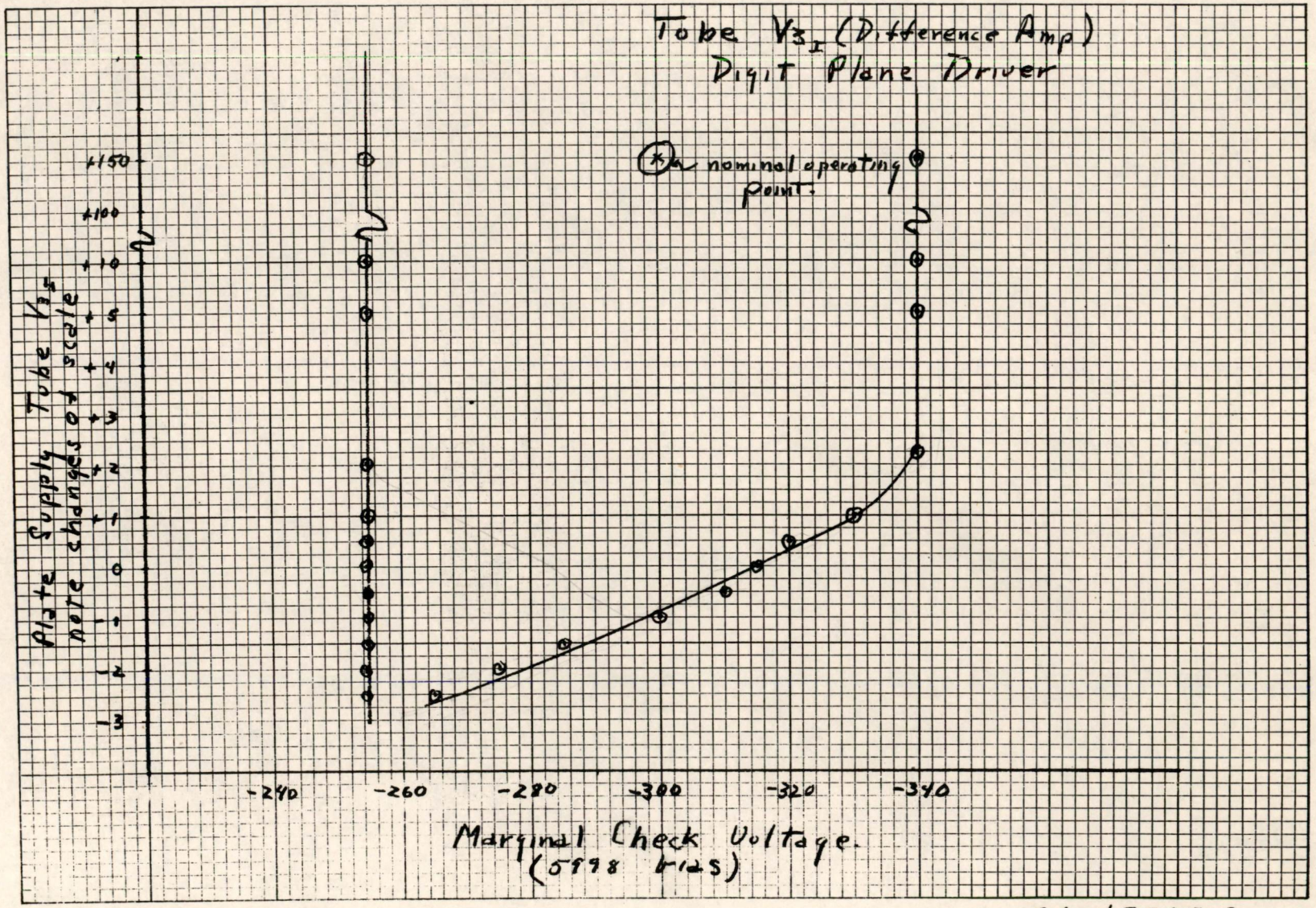

SA-48523-G
+150
+50
+20
+10
Plate Supply note scale changes
nominal operating point
To be V_{Z_I} (Cathode follower)
Digit Plane Driver
oscillates here
-260
-280
-300
-320
-340
SA-48523-G

FIG. 3

SA-48527-G



SA-48527-G

FIG. 4

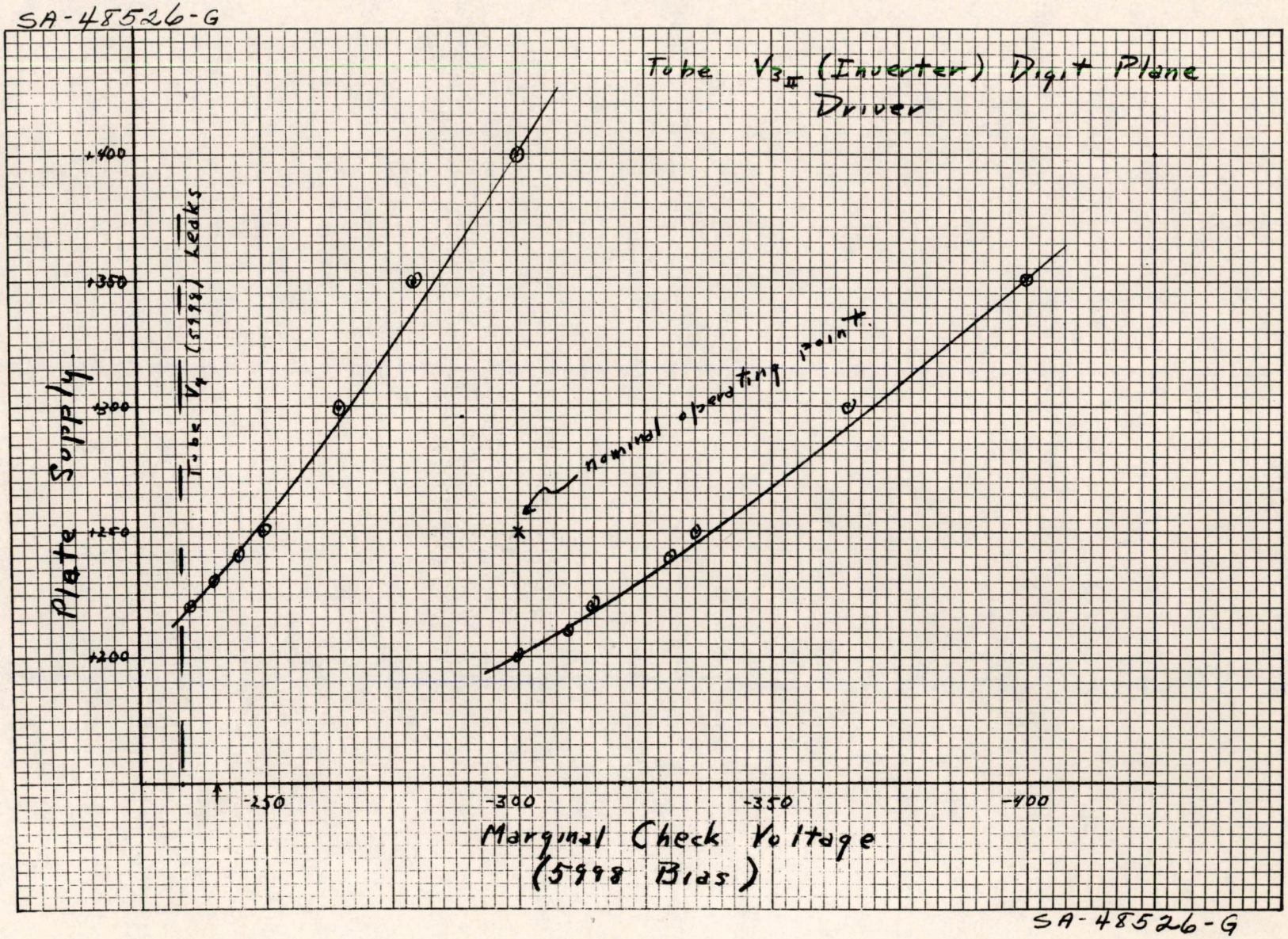

SA-48526-G
Tube V_{3B} (Inverter) Digit Plane Driver
Plate Supply
+400
+350
+300
+250
+200
Tube V_4 (5998) Leaks
nominal operating point
-250
-300
-350
-400
Marginal Check Voltage
(5998 Bias)
SA-48526-G

FIG. 5

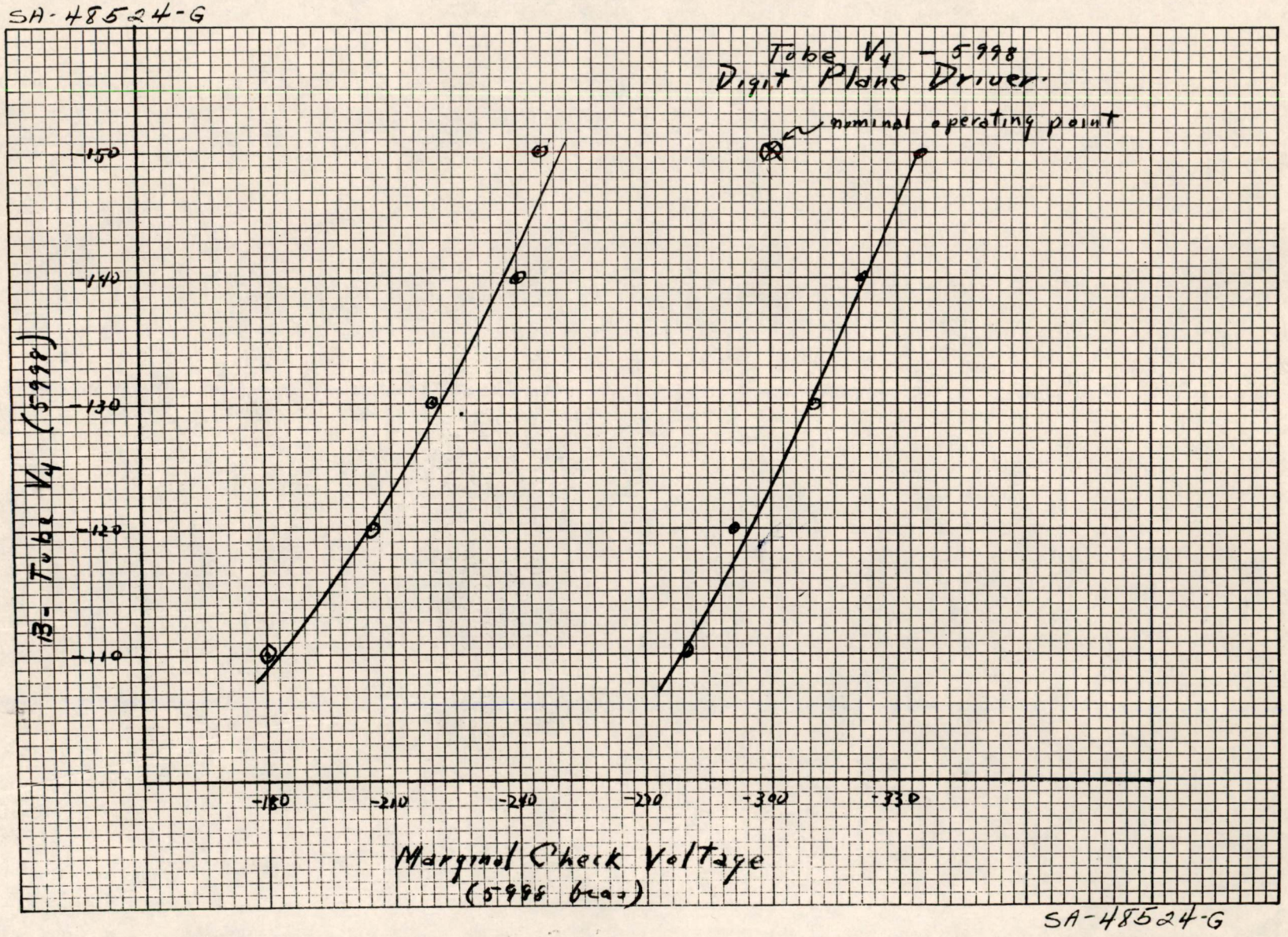

SA-48524-G
Tube V4 - 5998
Digit Plane Driver.
nominal operating point
-150
-140
-130
-120
-110
B- Tube V4 (5998)
-180
-210
-240
-270
-300
-330
Marginal Check Voltage
(5998 bias)
SA-48524-G

FIG. 6

Best

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SENSING WINDING GEOMETRY AND INFORMATION PATTERNS

To: N. H. Taylor

From: J. I. Raffel

Date: July 22, 1954

Abstract: Two properties of the sensing winding used in the Whirlwind I and MTC core memories are common to a large class of winding configurations. These are: 1) maximum partial cancellation of core "noise" 2) no inductive coupling between drive and sense wires. A new winding is suggested to replace the present zig-zag geometry. This should prove easier to implement and preliminary tests on a plane containing both old and new sense windings indicate that the two are electrically equivalent. Since core "noise" is a function of information and sense winding geometry, a different checkerboard pattern exists for this new winding.

In general, checkerboard patterns used for production testing should not be called "worst" patterns since no attempt is made to guarantee the disturbed states of the cores, and these have a considerable effect on sense winding outputs.

For a core memory using a two-dimensional read and consisting of n rows and n columns, all that is required in order to have a "cancelling" winding with respect to "noise" signals from half-selected cores is that the winding pass through half the cores of each row and of each column in one direction and through the remaining halves in the other direction. Consider a square array shown in Figure 1. Each of the first n/2 rows can be made of any of the nCn/2 combinations of n/2 pluses and n/2 minuses. (Plus and minus refer to core polarity with respect to sense winding.) If the next n/2 rows contain the complement configuration to that of the top half, the conditions for a cancelling winding as defined above are fulfilled. Figure 1 shows a typical example of a winding belonging to this class. The MTC-type sense winding has a distribution like that of Figure 2. It is seen to satisfy the necessary conditions also. Another possible geometry which suggests itself is shown in Figure 3. This appears to be the physically simplest configuration which satisfies the necessary conditions for partial concellation of core "noise".

It is now necessary to consider the problem of inductive pick-up. For this the cores can be neglected entirely and only the large closed loops of wire comprising the sense winding need be considered. The requirement for a non-inductive winding, if we neglect end effects and consider the drive wires as infinitely long, is that the $\int \frac{1}{r} dA$ be zero where r is the perpendicular distance between a drive line and a differential area dA as shown in Figure 4. The integral over A in Figure 4 would be made up of the two components A_1 and A_2 of opposing sign following the usual polarity convention for evaluating surface integrals.* The simplest way of guaranteeing this is that the net enclosed are (algebraic sum) at a given distance from any row or column wire is zero. The present sense winding uses two overlapping loops which have equal and opposite components of area with respect to any horizontal or vertical driving line. This has a map as shown in Figure 5 where solid areas and cross-hatched areas refer to loop areas of opposing polarity. If we consider the map of Figure 6 any "checkerboard" pattern of the type shown having an even number of squares on a side will be non-inductive. Here, as with core-noise cancellation, all that is required is that n/2 rows be "half and half" and the other n/2 rows be the complement of the upper half. It is to be emphasized, however, that here we refer to areas comprised of closed loops of wire and not to cores. The winding of Figure 3 is therefore seen to be both cancelling and non-inductive. This winding may be thought of most simply as being composed of four digit-plane type windings, (a single section links all cores in the same direction) connected in series so that adjacent quadrants of the plane are of opposite polarity. In building larger arrays and/or utilizing printed wiring techniques, this type of winding may prove to be much simpler to install than the old zig-zag.

The problem of delta noise has been considered in E-488, M-2351 and M-2568. These analyses show that a so-called "worst" pattern (that is, a condition under which ONEs are smallest and ZEROs largest) results from having one type of information on the positive half of the sense winding and another on the negative half of the sense winding. Using Freeman's terminology** half the cores should be in the "w_1" state and the other half in the "r_z" state on the selected row and column. That is, half the cores should be in the write-disturbed ONE state and half in the read-disturbed ZERO state. In the past no attempt has been made to guarantee that cores had been properly read-disturbed or write-disturbed, the emphasis being placed merely on inserting the proper pattern of ONE's and ZEROs in the array. For production testing of planes this type of test is probably sufficient for obtaining comparisons, but in no case should the results from such tests be used as any absolute indicator of margins and the term "worst" pattern should probably not be used where the disturb condition is not taken into account.

---

*Osgood Advanced Calculus -

**Pulse Response of Ferrite Memory Cores - M-2568

A test plane containing the old zig-zag type of sense winding was wound with an additional winding of the type shown in Figure 3. The experimental results obtained with the new winding of Figure 3 indicated no inductive pick-up, as expected, but in rastering through the array extremely large ZEROs were encountered at certain places. These ZEROs were reduced to normal size by the addition of the post-write disturb pulse and were therefore seen to be attributable to the core output and not pickup.

It next became necessary to determine why this effect was only encountered when testing the new sense winding with its corresponding checkerboard pattern and not when testing the old with its pattern. In each case the memory is filled with a pattern which places ZEROs on one half (the half shown with minuses for instance) the sense winding and ONEs on the other (pluses). The only difference which arises for the two windings is that the halves are composed of different groupings of cores (see Figures 2 and 3). In each case the array is addressed cyclically, a row at a time, starting from the lower left-hand corner. The difference in outputs between the two windings is clearly the result of the difference in information sequencing which results in differences in the disturbed state of the cores in the array. In other words, in both cases we have half the cores in the ONE state and half in the ZERO but no consideration has been given to whether the ZEROs are read-disturbed and the ONEs write-disturbed. A glance at the old checkerboard pattern, Figure 2, indicates that since no more than two ONEs are written consecutively almost all of the cores in the array are, in fact, going to be in the read-disturbed state, having been placed there by the digit-plane driver used for writing ZEROs and therefore there is not even a remote possibility of having the ONEs write-disturbed by chance somewhere in the array.

An examination of the sequence for the new checkerboard pattern, Figure 3, indicates two inherent characteristics which tend to guarantee the proper disturbed conditions for many more cores: 1)Long strings of consecutive ONEs and of consecutive ZEROs are placed in the array at a time. 2) Successive rows (except for the middle pair) have the same information. The results can be best demonstrated by considering two adjacent rows as shown in Figure 7. Writing the last ZERO of the bottom row read-disturbs all the cores in the array (digit-plane-driver pulse). Writing the series of ONEs to finish out the line write-disturbs columns directly above each ONE and hence leaves the ONEs in the second row write-disturbed. (Incidentally, the ZEROs of the bottom row are also write-disturbed.) The first ZERO of the second row is now about to be read out and the ZEROs in its row have been read-disturbed and the ONEs write-disturbed. It is therefore quite reasonable to expect an unusually large noise output. It should be pointed out that even now the disturb condition of all the cores has not been guaranteed. Only the row containing the selected core has been disturbed properly, no attention has been paid to the column, and indeed the cores here are all read-disturbed (except for the one core in the previous row) because the last excitation these cores saw was the digit-plane-driver pulse which occurred when writing ZEROs in the previous row. The ZERO output is therefore still far from the worst case. Figure 8 shows a sketch of the output from the array for this pattern.

Note that the peak value of the maximum ZERO has become alarmingly large, but at strobe-time discrimination is still excellent.

Another effect which has not been sufficiently evaluated is the size of the voltage induced in the sense winding by the digit-plane-driver pulse. This is greatest when all the cores in the plane are in the proper w_1 and r_2 states, and under a true worst condition might very well be large enough to cause the sense-amplifier to block.

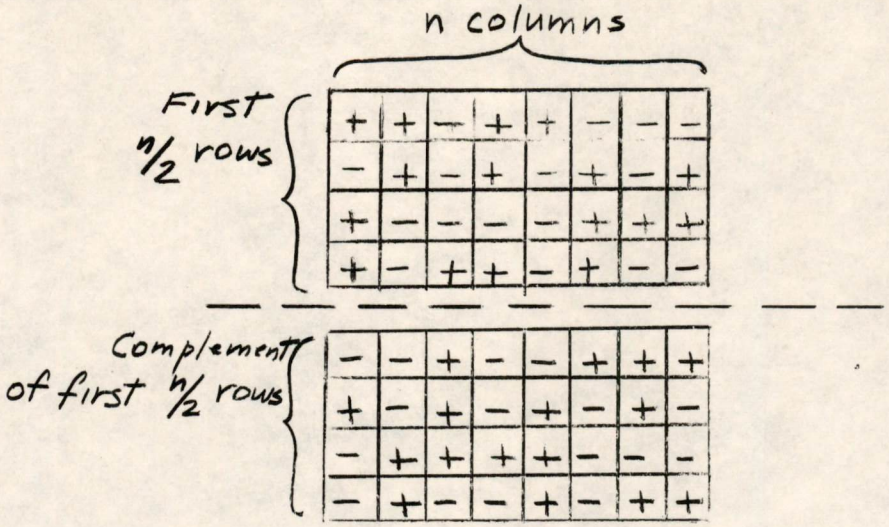
The new sense winding seems to work well and the experimental results obtains with it have served to emphasize the need for a thorough experimental investigation of theoretically predicted "noisy" patternsn. The term worst pattern which was previously used rather loosely to describe checkerboard patterns regardless of the disturbed condition of the cores should be avoided in the future. These patterns are worthwhile as standard tests but by no means represent the most adverse conditions which could be encountered in computer operation. It is hoped that this point has been made sufficiently clear to avoid the necessity of periodic re-discoveries that our test patterns do not give the worst signal-to-noise ratios.

Signed: Jack Raffel
Jack I. Raffel

Approved: W. N. Papian
W. N. Papian

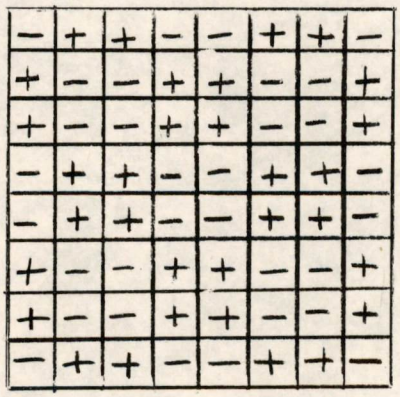
JIR:jd

CC: Group 62 - Engineers
Group 63 - Engineers
W. Wittenberg
N. Daggett
A. Roberts



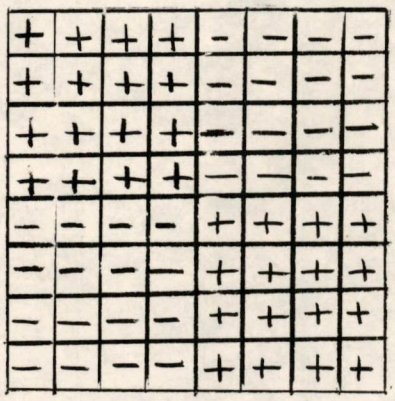
Typical Winding With Core-Noise Cancellation

Fig. 1



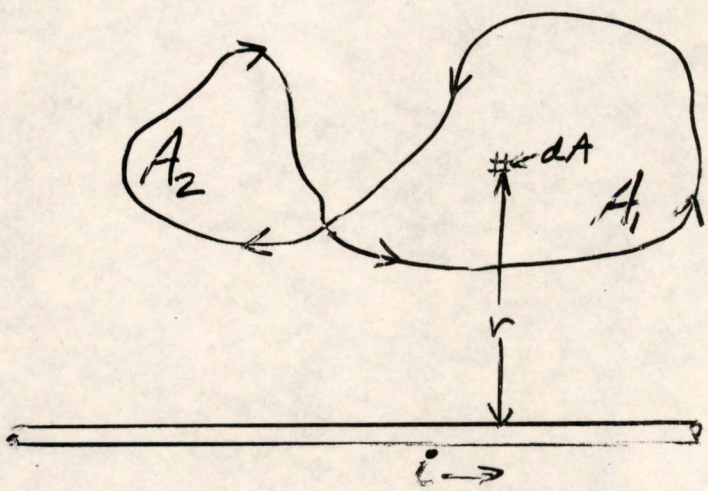
MTC-type Core-Noise Cancellation

Fig. 2



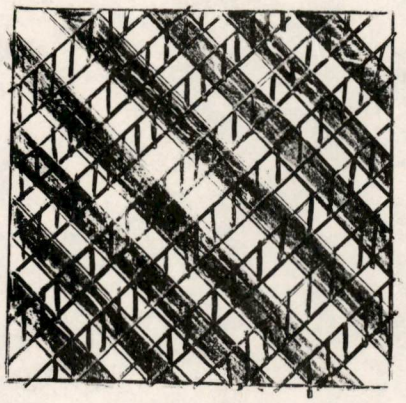
Proposed Cancelling Winding

Fig. 3



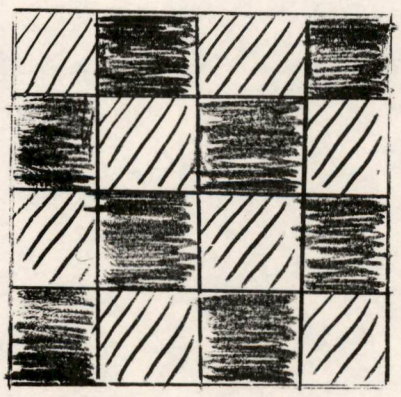
Voltage Induction by Current-Carrying Conductor

Fig. 4



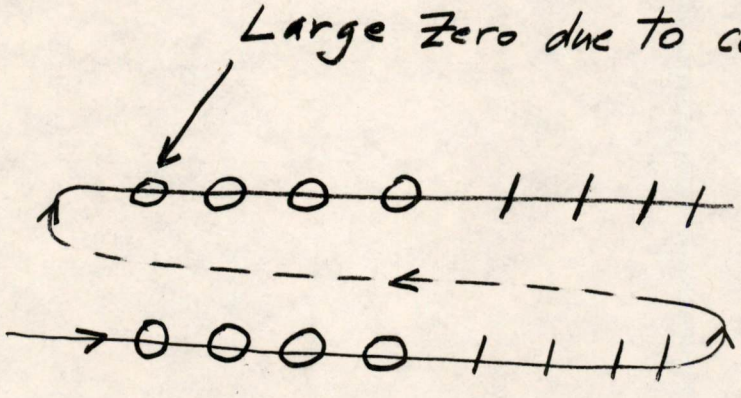
Loop-Area Map For MTC-type Winding

Fig. 5



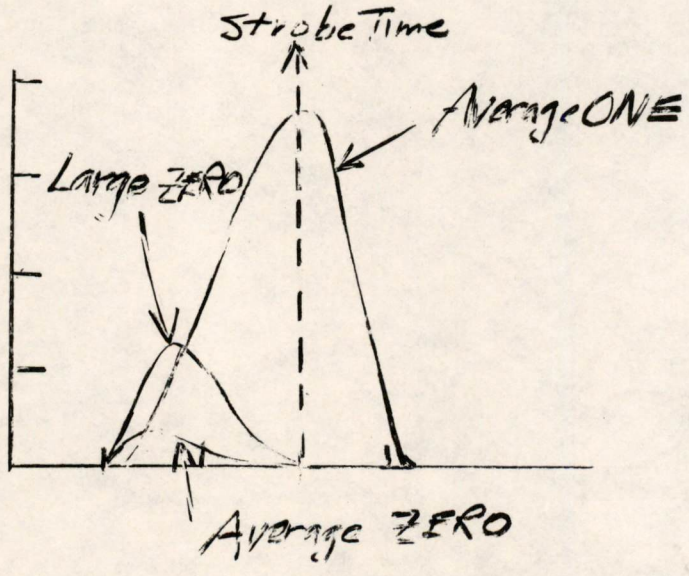
Loop-Area Map For Checkerboard Type

Fig. 6



Sequence For New Winding

Fig. 7



Sketch Showing Relative Sizes of ONEs and ZEROs

Fig. 8

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A CARRY SYSTEM EMPLOYING A MAGNETIC CORE AND TRANSISTORS

To: Transistor Distribution 2

From: S. Oken

Date: August 3, 1954

Abstract: This is a preliminary report on a carry system employing transistors, vacuum tubes and magnetic cores which has been developed as a possible substitute for the flip-flop and gate circuits presently used for the carry system in the arithmetic element. At present this system can be run at a maximum pulse repetition rate of about 350 kc. An output voltage in excess of 15 v can be obtained across a load resistance of 1 k Ω.

1.0 Introduction

A block diagram of one digit of the proposed system is shown in Figure 1. When the partial sum flip-flop is in the "1" position, gate 2 will conduct a pulse to the core if the "A" register flip-flop is in the "1" position[1] and an add pulse is applied to the appropriate line. If the partial sum flip-flop is in the "0" position, the gate cannot be triggered by an add pulse. The carry pulse is assumed to come from a vacuum tube driver which drives the cores of the different digits in series. This is probably the best way to combine transistors, cores, and vacuum tubes. Local elements which drive only a gate and flip-flop, etc., can employ transistors, but a driver which must supply a current or voltage pulse to a whole line of elements should be a vacuum tube.

The transistor gate 2 in Figure 2A is required to set the core to the "1" position (see Figure 2B), if a carry is to be generated. The carry pulse then switches the core back to the "0" position. If the core held a "1", a large negative output voltage will be induced in the output winding by the carry pulse, whereas if it held a zero, a small output pulse will be obtained. The output from the core under these two conditions is pictured in Figure 3.

It should be noted here that the load on the gate is the complement input to a flip-flop and the sensing input to a "high-speed carry gate."

---

1. This is arbitrarily defined. When the flip-flop is in the "1" position, the voltage of the collector attached to the gate circuit is assumed at its most negative value.

The core replaces the carry flip-flop and gate circuit in the present system.

2.0 Details of the Carry System

The schematic diagram of the complete system is given in Figure 2A. The partial sum flip-flop is a transistor flip-flop which is of the non-saturating type.(2) Thus the two stable states of the transistors are the "off" and the "active" states. Circuits of this type can be run at higher repetition rates and with smaller input trigger voltages because they are not plagued by "hole storage" problems.

The gate circuit is essentially one which was designed by C. T. Kirk.(3) The collector voltage of the flip-flop usually swings from about -9 v to - 20 v. When the voltage at point A is -9 v the emitter diode of the gate circuit will be in the reverse direction due to V_4. When the flip-flop is complemented, the voltage V_4 and diode d_1 clamp the collector voltage to about -15 v. Now when a sensing pulse is applied at the emitter, the pulse will be conducted to the core and set it to the "1" position.

3.0 Design of Windings on the Magnetic Core

The design of the windings on the core was performed with the following points kept in mind:

(1) A metallic core should be used because for a given $(NI)_{net}$ it will switch faster than a ferrite core.

(2) In order to reduce both the back voltage on the transistor in the gate circuit and the switching time of the core, a core with the least number of wraps of material, the smallest diameter bobbin, and 1/8 mil tape should be chosen. (The core available was a mo-permalloy core 1/8 mil, 1/8 inch diameter, 1/8 inch depth and 5 wraps.)

(3) The maximum number of turns which can be wound on this core is about 100 turns.

Using experimental data showing the switching time and maximum output voltage from different cores as a function of NI_{net}, an approximation to the switching times and output voltages to be expected may be obtained. In this design the $(NI)_{net} = N_1 I_1 - (N_2 I_2)_{av}$, where the values of N are those shown in Figure 2A. The output wave (Figure 3) can be

---

2. Carlson, W., "A High Speed Transistor Flip-Flop," Air Force Cambridge Research Center, Technical Report 53-16, June 1953.

3. Kirk, C. T., "A Transistor Grounded Base Amplifier as an AND Gate," M-2810, Lincoln Laboratory Division 6, May 7, 1954.

approximated by a triangle; thus $(N_2I_2)_{av} = \frac{(N_2V_2)_{max}}{2R_1}$. Since the output voltage should have a peak amplitude of at least 15 volts, $(N_2I_2)_{av} \cong 0.2$ ampere-turns. The N_1I_1 used for the picture of Figure 3 was ~ 1.5 ampere-turns. This can be increased with a corresponding decrease in switching time and increase in output amplitude since the area under the output voltage curve must be a constant as NI_{net} is varied.

4.0 Selection of a Transistor for the Gate Circuit

The three design criteria for the gate circuit are:

(1) The transistor should not go into the saturated region when driving the cores.

(2) The transistor must be capable of dissipating the power encountered during the operation.

(3) The frequency response of the transistor should be as high as possible in order to decrease the rise time of the output pulse.

From Figure 3 we see that the undesired output voltage across the core when it is set to the "1" position is a positive pulse[4] of about 7 volts. Thus the back voltage induced in the driving transistor circuit is about three times this or about + 20 volts due to the turns ratio. If criterion[1] is to be fulfilled, the value of $V_{cc} - V_b$ should be ≤ -20 volts. Thus $V_{cc} \cong -35$ volts was selected. The current output from the gate circuit is about 12 ma. Therefore, since the pulse is longer than the switching time of the core, the gate circuit is sending 12 ma through a short circuit load for part of the pulse. The peak power rating of the transistor must thus be at least $(V_{cc} - V_4)$ x 12 ma or about 250 mw.

When the carry pulse switches the core to the "0" position, a pulse of about 40 volts is induced across the winding in the gate circuit, opposing V_{cc}. If diode 2 were not included there would be a large hole storage effect since the collector diode would then be switched to the forward direction. Furthermore, a positive pulse would be fed back to the control flip-flop and trigger it. The diode d_2, however, overcomes these difficulties since it reverses at this time. The forward current in the collector diode is thus limited to about 100 μa. Also, due to the voltage divider action the flip-flop receives very little feedback voltage.

Since $I_e = 0$ and $r_c = r_{cf}$, the transistor actually goes into the passive region for a short time so there may be some hole storage effects. Because of the small forward current and short time in the forward condition, they should be negligible.

---

4. This set up pulse output will not be harmful since the following circuit can be designed to trigger on negative pulses only.

5.0 Results Obtained

By increasing $N_1 I_1$ the output voltage can be increased to about 30 v peak amplitude with a 0.2 μsec width. The main limitation to the prf is the setup time of the core which is about 1 μsec. The maximum prf obtained was about 350 kc. The limitations are due to the frequency response of the transistor in the gate circuit and the maximum current obtainable from the gate circuit.

If vacuum tubes alone were used in this system it could, of course, be run at a much faster rate. The decision to use transistors or vacuum tubes, however, will be contingent upon many other factors as well as speed.

Signed Stanley Oken D.J.E.
Stanley Oken

Approved Donald J. Eckl
Donald J. Eckl

SO/jk

Drawings:

Figure 1 B-59506
Figure 2A B-59507
Figure 2B A-59508
Figure 3 A-59509

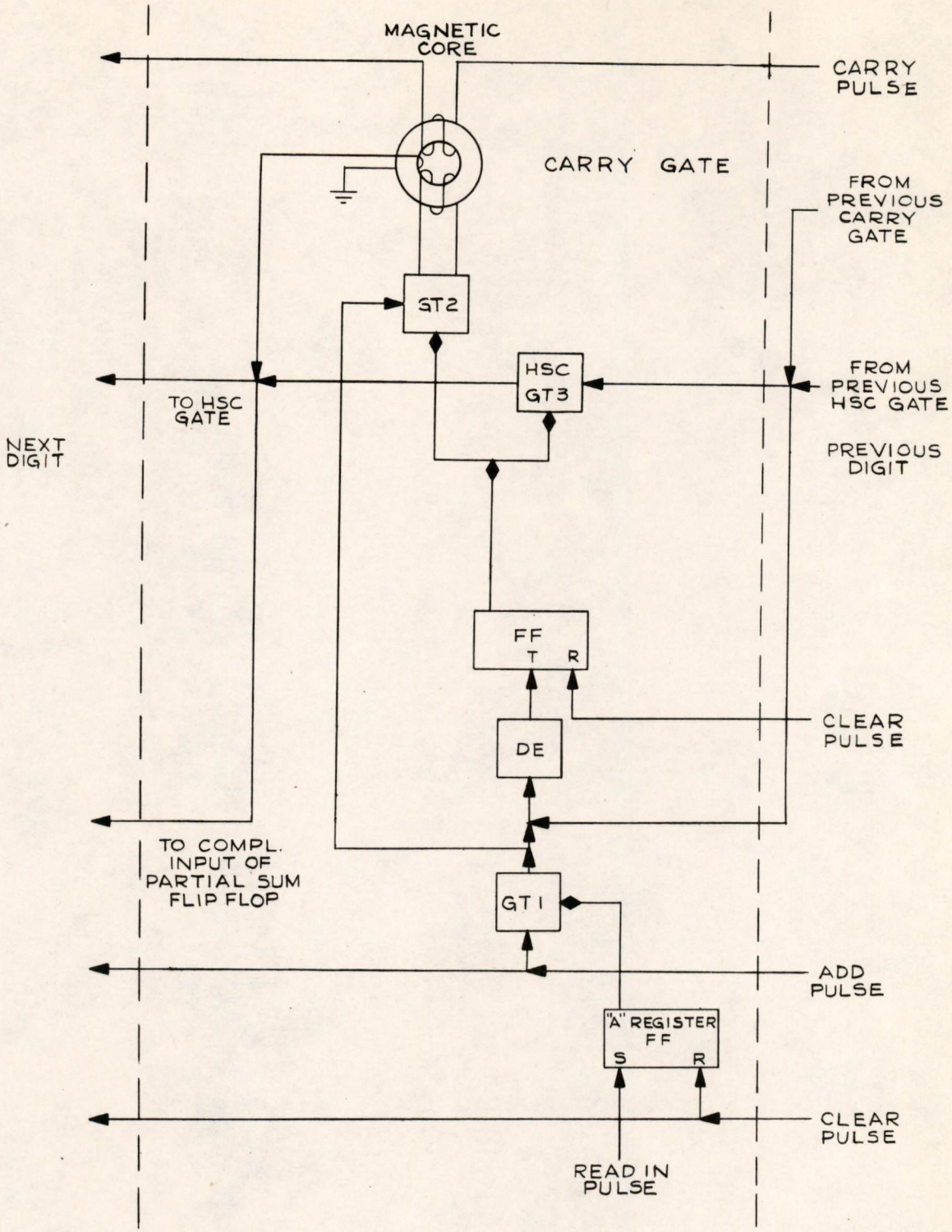


FIG. 1

ONE DIGIT OF ACCUMULATOR

USING THE NEW CARRY CIRCUIT

B-59506

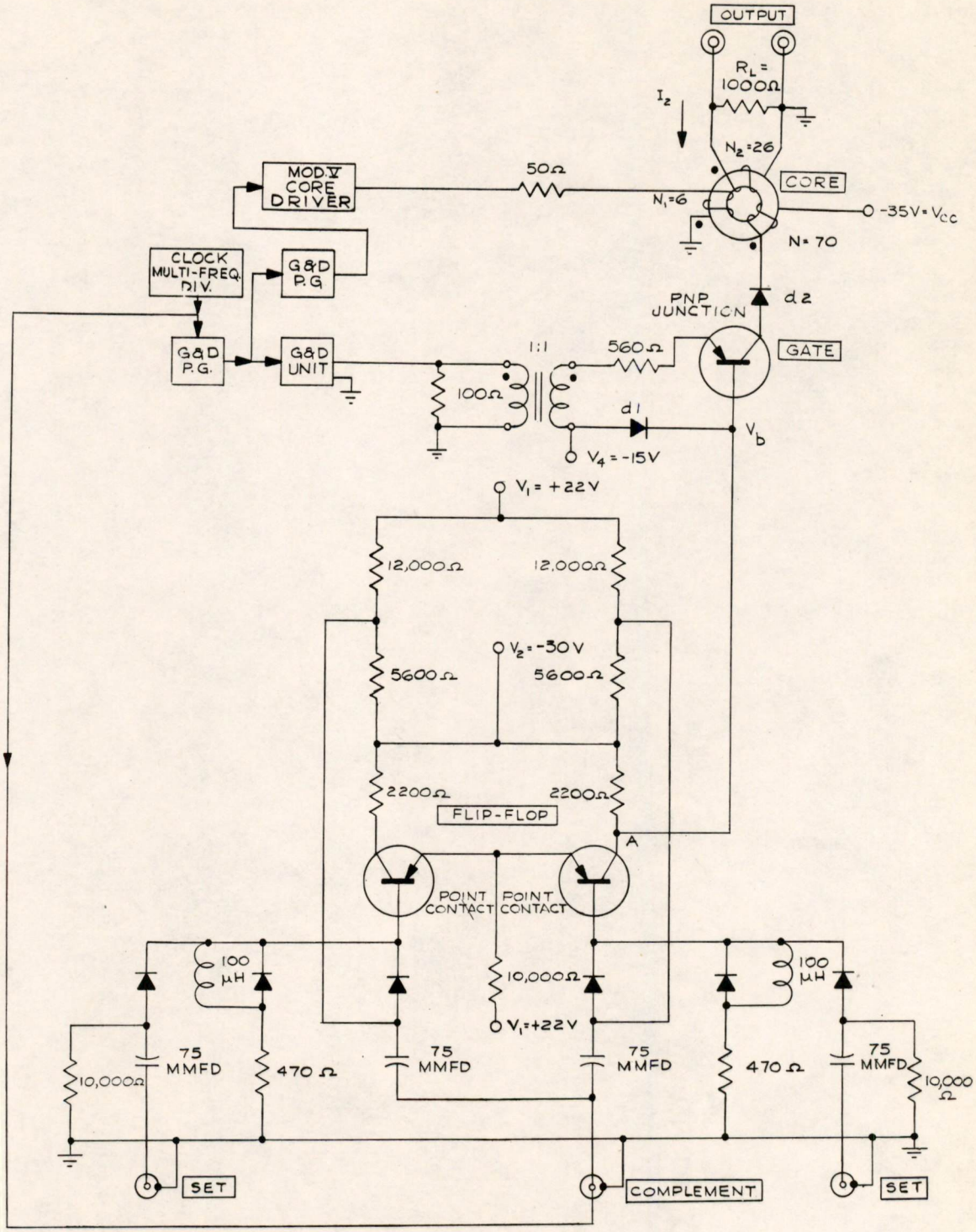


FIG. 2A

SCHEMATIC DIAGRAM OF THE SYSTEM

USED TO TEST THE NEW CARRY CIRCUIT

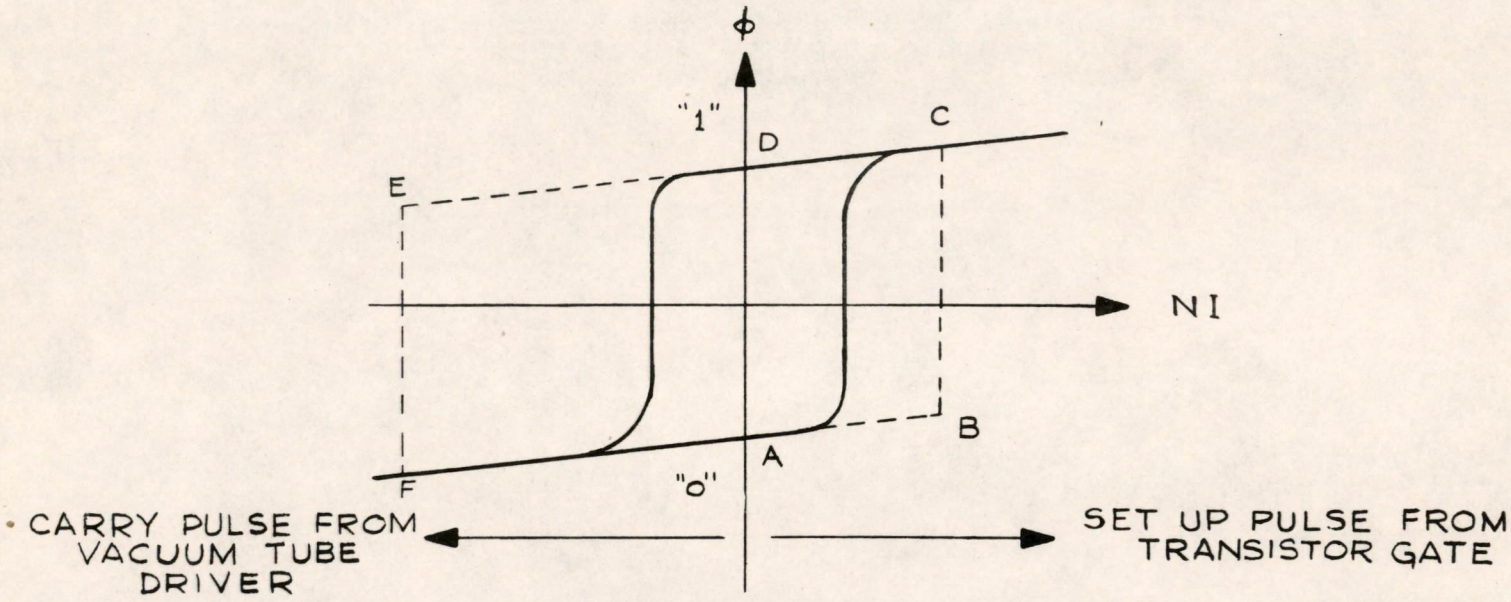
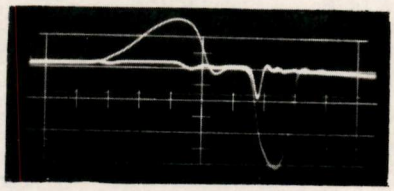


FIG. 2B

THE OPERATING LOCUS ON THE HYSTERESIS LOOP OF THE MAGNETIC CORE



SCALES :

TIME : 0.3 μSEC/div.

VOLTS: 5 V / div.

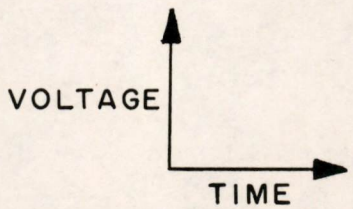


FIG. 3

OUTPUT VOLTAGE FROM THE CORE

A-59509

Distribution List for Transistor Section Distribution 2

Internal Distribution

I. Aronson
R. Best
H. Boyd
D. Brown
R. Burke

R. Callahan
E. Cohler
D. Eckl
H. B. Frost
R. Gerhardt

A. Heineck
J. Jacobs
N. Jones
C. Kirk
W. Klein

C. Laspina
S. Oken
H. Platt
D. Smith
L. Sutro

D. Shansky
C. Schultz
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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: GENERAL CHARACTERISTICS OF GERMANIUM AND SILICON DIODES AND TRANSISTORS

To: Transistor Distribution 2

From: Nolan T. Jones

Date: July 1, 1954

Abstract: The construction and electrical characteristics of currently available germanium and silicon diodes and transistors are summarized. The general order of increasing diode forward resistance is alloy junction, grown junction, bonded, and point-contact. The general order of decreaseing back resistance is grown junction, bonded, alloy junction, and point-contact. Transistors included are grown-junction n-p-n, alloy-junction p-n-p, and point-contact.

1.0 Introduction

A brief description of the physical and electrical characteristics of the common semi-conductor diodes and transistors is presented here as a foundation for later discussions of the minority carrier storage characteristics of these devices. This is Chapter II of the author's thesis, "Minority Carrier Storage in Diodes and Transistors." There are four types of construction: point-contact, bonded, grown junction, and alloy or diffused junction, and two materials used in commercial products: silicon and germanium.

1.1 RTMA Type Numbers

The standard type numbers of the Radio-Television Manufacturer's Association are the familiar 1N series for diodes, 2N for the three element transistors, and 3N for tetrode transistors. The diode type numbers such as 1N34, generally denote that the static characteristics will fall within certain specified limits. These are most often taken at three points: the forward current at +1 volt drop, and the currents at two values of back voltage. They are limits in the truest sense; the static characteristics may vary widely between units from the same manufacturer and between manufacturers, although all may fall within the specified limits for the given type number. A letter suffix on the type number may denote different static characteristics,* construction, or manufacturer from that of the original application for the given type number to the RTMA.

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* Higher back resistance in the 1N34A, 1N38A, and 1N56A

The specification of transistors is in a state of flux at present. Several AIEE-IRE committees are studying the problems, and they will probably make specific recommednations for standardization when their work is completed. The electrical description of transistors is included in several articles in the literature* to which the reader is referred.

2.0 Grown-Junction Diodes

The grown-junction diodes are constructed by the introduction of p-type impurities into the n-type melt as the germanium crystal is being grown, converting the remainder of the crystal to p-type with a higher impurity concentration. Then the ingot is cut into small rectangular prisms about 40 mils square and 120 mils long with the p-n junction normal to the length. Non-rectifying or "ohmic" contacts are soldered to each end and the diode has the cross section of Figure 2.1e. The junction is of high quality, i.e. the electrical characteristics are very similar to the ideal theoretical characteristics of a p-n junction.

The current-voltage relationship in an ideal p-n junction diode is the familiar expression:

$$I = I_o \left[\exp(qV/kT) - 1 \right]$$

where V is the junction voltage, k is Boltzman's constant, T is absolute temperature, and q is the electronic charge. This assumes that ohmic drop is negligible. I_o is a function of the temperature and the impurity concentrations of the germanium. The term kT/q is about 0.026 volt at room temperature, so that for positive voltages large with respect to 0.026 the exponential term is much larger than 1, and for negative voltages of the same magnitude the exponential becomes small compared to 1. This means that the expressions for forward and reverse current become:

$$I_f = I_o \left[\exp(V_f/0.026) \right] \qquad |V_f| > 0.026 \text{ volt.}$$

$$I_r = I_o \qquad |V_r| > 0.026 \text{ volt.}$$

At very high reverse voltages, the junction should exhibit a zener breakdown and the dynamic resistance would drop to a very low value. Present day germanium junction devices do not show a true zener, but an ionization or avalanche breakdown[13] due to carriers crossing the junction under extremely high fields.

The static reverse and forward characteristics of all the diode types are illustrated in figures 2.2 and 2.3 respectively. The curvature of the forward characteristic of the grown junction diode, 1784 #7, indicates that ohmic drop is not negligible in this diode. Since the resistivity of the germanium used in these grown junction diodes is relatively high this ohmic drop could be anticipated. The reverse current for the 1786 grown germanium junction diode is quite constant over a wide range of reverse voltage.

---

* References 1, 2, 3, 4, 5, and 6 present thorough coverage of the subject.

3.0 Alloy Junction Diodes

The first step in the construction of the alloy or diffused junction diodes is the placing of a pellet of p-type impurity on the surface of an n-type wafer, soft-soldered to a conventional ohmic contact base. Under heating the impurity dot melts and dissolves a small amount of germanium at the surface. The device is allowed to cool, and the solution re-crystallizes producing a highly doped p-region. The cross section is Figure 2.1d. The linear forward characteristic of the 1N92 plotted in Figure 2.3 fits the ideal case quite well. The reverse has noticeable curvature and the magnitude of the saturation (or constant) current is high. This is typical of this particular series of alloy diodes and not the construction method.

An alloy silicon diode, Type A1821 #2, is included in the electrical characteristics. The dynamic forward resistance at currents below 1 ma is the same order as the forward resistance of the germanium devices, but the static resistance, or V_f/I_f, is much larger. The reverse resistance is very high at low voltages; the reverse current is usually measured in millimicroamperes in silicon devices. This particular diode shows what is most likely an avalanche breakdown at 37 volts.

4.0 Point Diodes

The point diodes are made by a large number of manufacturers and in a wide variety of types. Many of these, such as 1N34 and 1N38, have been in general use for years, although much less is known of the physics of point devices even at the present. The construction of point diodes is illustrated in Figure 2.1b. An n-type germanium wafer about 40 mils square and 10 to 20 mils thick is soldered to a metal base to make the usual ohmic contact. Then a catswhisker 1 to 2 mils diameter with a pointed or chisel shaped tip is placed in contact with the wafer's surface. A small amount of mechanical stress is added to the whisker for mechanical stability after contact is made. Then the diode is electrically "formed" for mechanical and electrical stability and the desired electrical characteristics. This forming is basically a heating process and may be done by condenser discharge or by alternating or direct currents of the order of an ampere for a fraction of a second. The effect of this forming is to produce a p-type germanium layer under the point, either by diffusion of impurities from the whisker or by heat production of lattice imperfections.[7] The size and quality of the p-region is apparently a function of the amount and length of time of forming, whisker shape, and least important, whisker material.

The principal physical difference between point and bonded diodes is the whisker material and the electrical prosessing. Point diode whisker materials used are hard, high-melting-point materials such as tungsten and molybdenum. In their commercially available forms, these materials often contain small amounts of p-type impurities.[7] In addition at least one manufacturer actually plates the whisker with an impurity material before

construction. During forming the whisker tip retains its shape as the p-region forms, and the whisker apparently does not become physically attached to the germanium. Destruction of common diodes and examination of the surface of the germanium wafers has shown that it is extremely difficult, if not impossible, to determine where the contact had been. The p-n junction is ordinarily of low quality as shown in the electrical characteristics. The current increases directly (though not linearly) as back voltage increases, and the forward characteristic is curved throughout the range.

The electrical characteristics of point diodes are relatively complex functions of resistivity, surface states, and the size and character of the p-n junction. References 1, 2, 8, 9, 10, 11, and 12 furnish information on the subject although none presents a complete point diode theory.

5.0 Bonded Diodes

The whisker material of bonded germanium diodes is a low melting-point material, usually a gold alloy with a p-type impurity material. The electrical processing, or bonding, causes the whisker to melt under the localized heating, and dissolve a small amount of germanium. Cooling allows recrystallization and the result is a small-area, highly-doped p-region. The whisker tip may mushroom, and ordinarily forms a strong mechanical connection to the germanium. Cross section of the bonded diode is shown in Figure 2.1c. The electrical characteristics of the bonded diode illustrated in Figures 2.1 and 2.3, the T5 #29, indicate a high quality junction. Its reverse characteristic has low and fairly constant current. The forward resistance is quite low and the curvature of the forward characteristic is much less than for point devices.

6.0 Grown Junction Transistors

Transistors resemble two diodes on the same germanium wafer constructed so that the forward current in the emitter diode affects the reverse current in the collector diode. The various types of transistors are constructed in the same general way as the diodes of the same type.

Construction of the grown junction transistors is as follows: At a point in the drawing, or growing, of an n-type germanium crystal sufficient p-type impurities are introduced into the melt to cause the germanium to become p-type. The crystal is grown a very short distance and then an excess of n-type impurities is introduced to convert the crystal back to n-type, producing two p-n junctions with a common, thin layer of p-material between. Ohmic contacts are soldered to each end and to the p-region and the n-p-n transistor has the cross section of Figure 2.4d. All commercially available grown junction transistors are n-p-n. Electrical characteristics are illustrated in Figure 2.5a.

Current gain, α, is usually 0.90 to 0.999 and collector resistance, r_c, greater than a megohm.

7.0 Alloy Junction Transistors

Two alloy junction diodes on opposite sides of a very thin wafer produce an alloy or diffused junction transistor. Cross section is shown in Figure 2.4c and electrical characteristics in Figure 2.5b. Both α and r_c are slightly smaller than these parameters for the grown junction transistors; values of 0.85 to 0.99 and 0.3 to 1.0 megohm are typical. Most alloy junction transistors are p-n-p although one alloy n-p-n unit* was marketed for several months.

In normal operation of transistors, the emitter diodes are biased in the forward direction and collectors in the reverse. Forward bias of a p-n junction is p-positive. This means that collector voltage for n-p-n units is positive and for p-n-p negative; hence the inversion of the collector characteristics of these types in Figure 2.5a and 2.5b. The schematic symbol has an arrow in the emitter denoting the direction of forward current flow as in Figure 2.4a.

8.0 Point-Contact Transistors

Construction is illustrated in Figure 2.4b and electrical characteristics in Figure 2.5c. Two contacts are located close together on the surface of an n-type wafer. Only the collector is electrically formed to produce the desired transistor characteristics. The result is that the collector contact area becomes relatively large and its back resistance low. r_c is about 20,000 ohms and α varies from 2 to 3 in most point-contact transistors.

---

* RCA 2N35

Signed Nolan T. Jones per D.J.E.
Nolan T. Jones

Approved Donald J. Eckl
Donald J. Eckl

NTJ/jk

Drawings attached:

Figure 2.1 - A-58472
Figure 2.2 - A-58439
Figure 2.3 - C-58442
Figure 2.4 - A-59105
Figure 2.5 - A-58856

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12. Torrey, H. C., and Whitmer, C. A., Crystal Rectifiers, McGraw-Hill Book Co., New York (1948).

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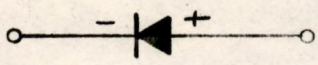
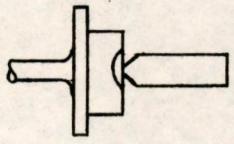
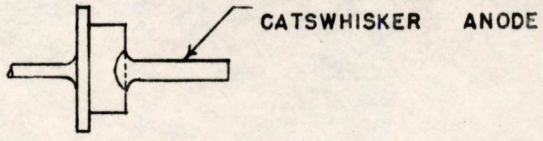


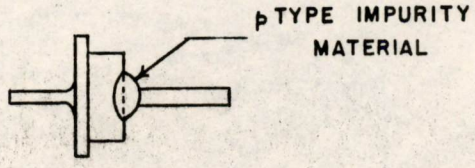
a) SCHEMATIC SYMBOL



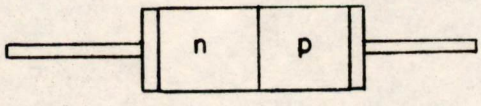
b) POINT CONTACT



c) GOLD BONDED



d) DIFFUSED JUNCTION



e) GROWN JUNCTION

FIG. 2.1

DIODE CONSTRUCTION TYPES

A-58472

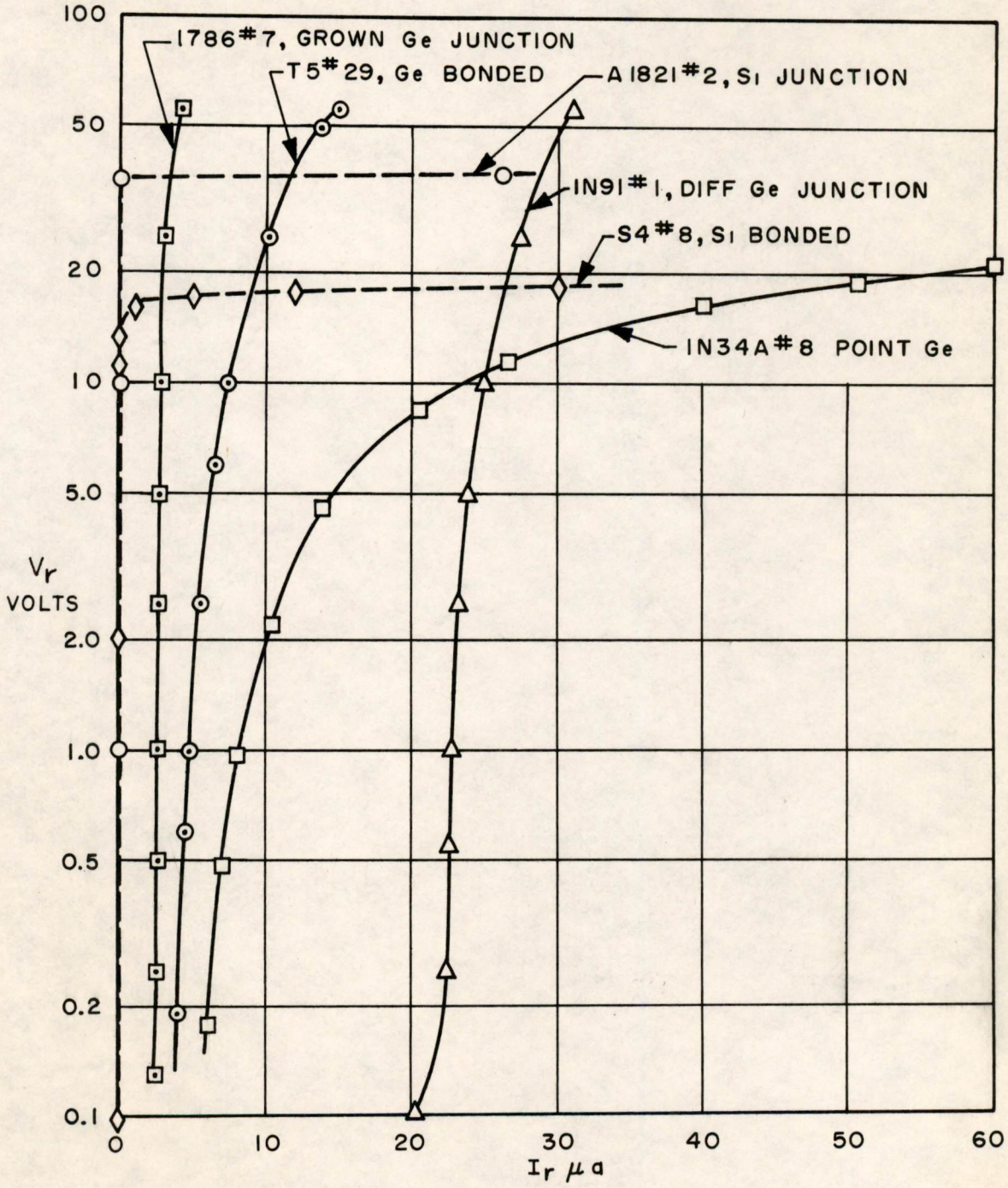


FIG. 2.2

TYPICAL STATIC REVERSE CHARACTERISTICS OF DIODES

A-58439

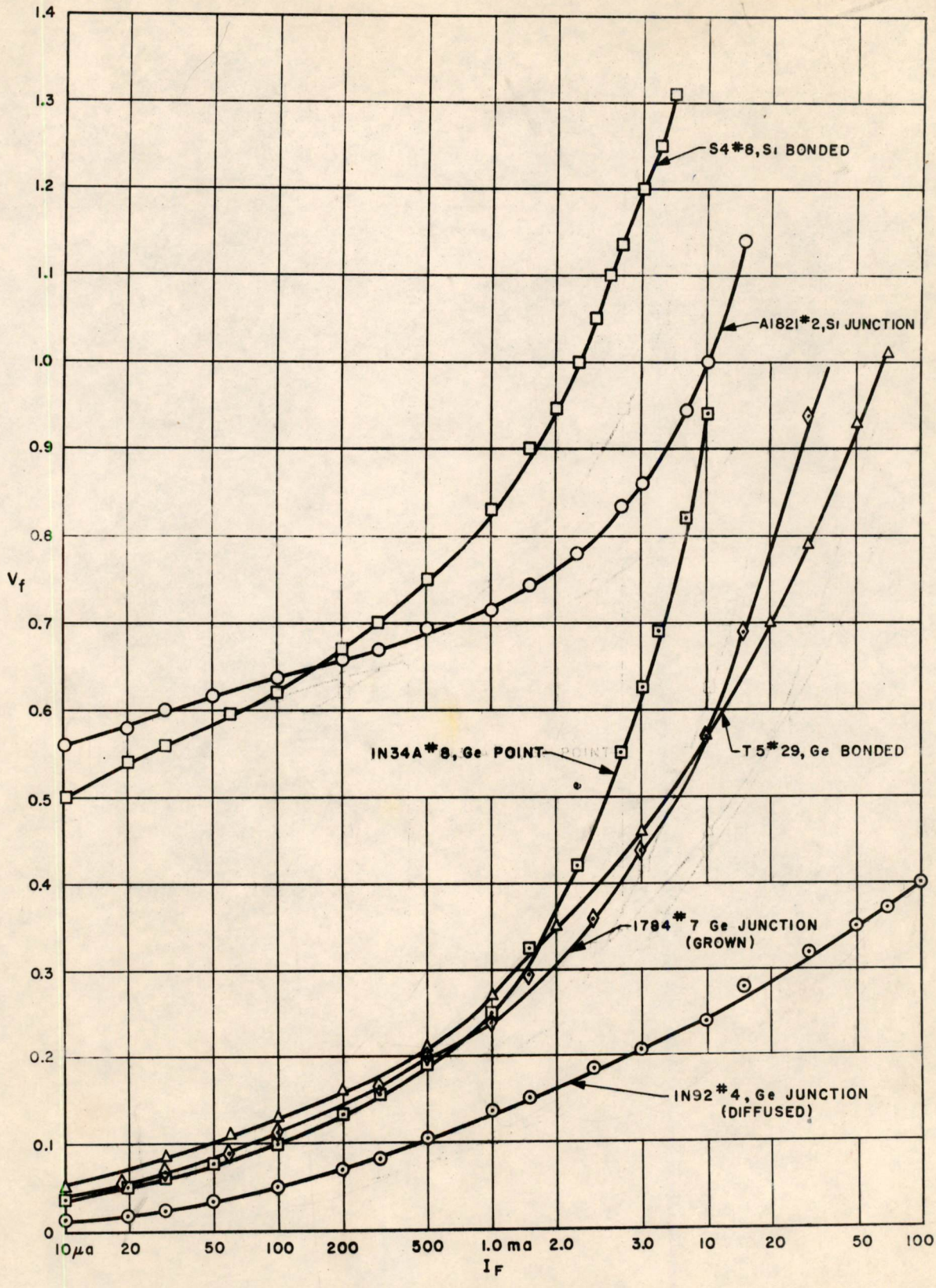
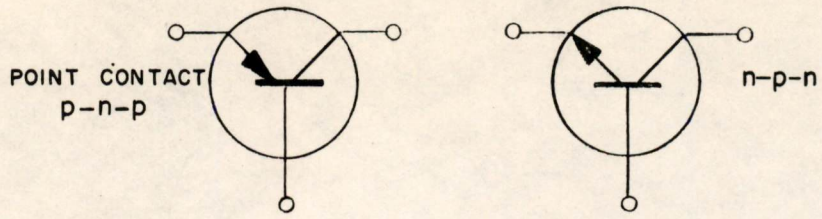


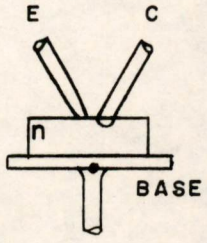
FIG. 2.3

TYPICAL STATIC FORWARD CHARACTERISTICS OF DIODES

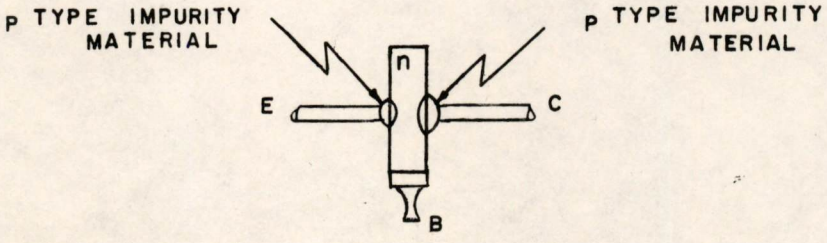
C-58442



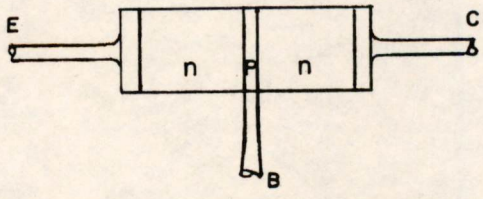
a) SCHEMATIC SYMBOLS



b) POINT CONTACT



c) DIFFUSED JUNCTION

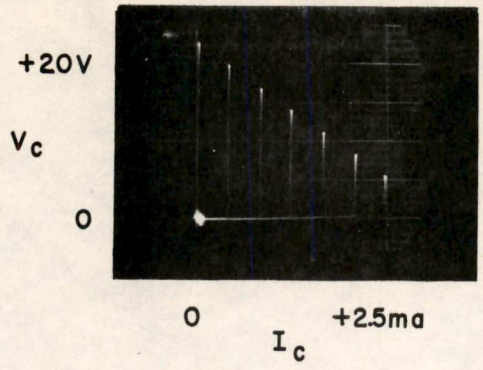


d) GROWN JUNCTION (n-p-n)

FIG. 2.4

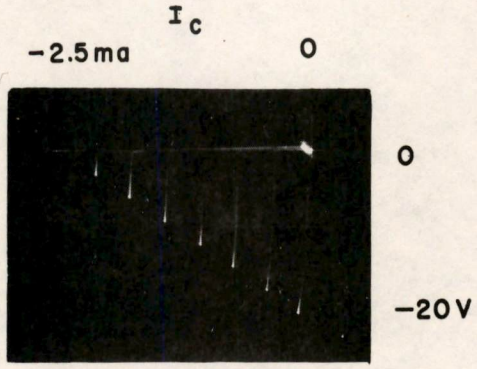
TRANSISTOR CONSTRUCTION TYPES

A-59105

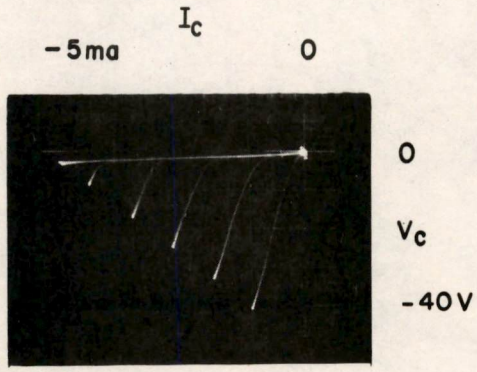


(a) GROWN N-P-N JUNCTION RDR TYPE 2517 NO. 10

ΔI_e = 0.5 ma IN ALL CASES



(b) ALLOY OR DIFFUSED P-N-P JUNCTION CBS-HYTRON 2N36 NO. 2



(c) POINT CONTACT RCA TA 165 NO. R 386

FIG. 2.5

COLLECTOR CHARACTERISTICS OF THE THREE COMMON TYPES OF TRANSISTORS

A-58856

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Subject: MTC Technician Training Manual - Chapter I

To: N.H.Taylor and MTC Personnel

From: A. Vanderburgh, Jr.

Date: December 14, 1954

Approved: W. Ogden, Jr.
W. Ogden, Jr.

Abstract: A technician training course in the troubleshooting of Memory Test Computer was started late in September 1954. This memorandum is the first chapter of a text that will be prepared concurrently with the course.

Although it is slanted toward MTC, the material in Chapter I is applicable to other computers. It consists of an introduction to automatic digital computers, a description of the binary number system, a discussion of available computer components, and a sample programming problem.

Chapter II, which covers the MTC Central Control Block Diagram (SE 37460), has been finished in class and will be available in January 1955.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

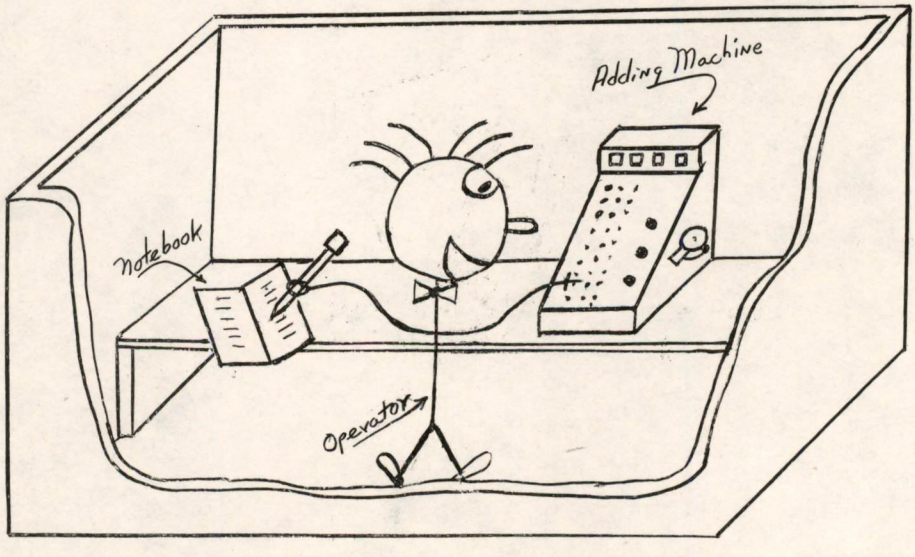
I. Introduction:

Some of the mathematical problems of Science and Engineering can not be solved by direct analytical methods. For various reasons it becomes neccessary to assign numbers to the known variables and seek numerical solutions. In the past, and indeed in the present, these solutions were performed by hand, or with the aid of adding machines and office calculators. Since there is much repetition of simple operations, many of these problems can be solved by untrained personnel who merely follow a set of complete instructions written by the mathematician. There are, however, many problems that require so many operations that human operators are not sufficiently reliable, and in any event would take too long. It is for this latter class of problems that High Speed Automatic Digital Computers are used.

This first chapter will deal with a simplfied human computing system. The first section will describe the system, the second will introduce systems for representing numbers (e.g. Binary - Octal), and the last section will list some of the components that are available for mechanization of the human system. Later chapters will discribe how this mechanization was carried out in connection with the Memory Test Computer (MTC) .

II. Automatic Digital Computers can be considered as further mechanization of Adding Machine techniques.

Let us consider a simple computing system. We will make it simple, because our purpose is to make it completely automatic later on. The diagram below shows the essential components of our system.



Self-Contained Human Computing System
Fig. #1

a. The computing system of figure # 1 consists of a notebook, an adding machine, and an operator. Let us describe these components in detail.

1. The Operator

Our operator can read and write, but his vocabulary is very limited. By convention, he starts at notebook line # 0 and performs the instructions in the order written. The only instructions he can understand are listed below. This list will eventually be extended to include all of the 26 instructions of the MTC instruction code.

Instruction	Abbreviation	Description of Operator's actions.
Add x	ad x	Enter the number on line x into the keyboard. Then push the add button. (See below under "Adding Machine".)
Clear and add x	ca x	Push "Clear" button. Perform "ad x" instruction.
Store x	st x	Erase line x . Copy the number in the Accumulator onto line x .
Transfer if negative to x	tn x	If the Accumulator is negative take next instruction from line x, and proceed in in order from there. If it is positive, ignore this instruction and proceed to the next.

2. The Adding Machine

The adding machine is designed to accommodate 5 digit numbers. Both the keyboard and the accumulating register (Accumulator) can accommodate negative numbers as well as positive. An alarm will sound if the result of an addition is too large. (This is called an OVERFLOW alarm.) There is a set of control buttons. Their functions are as follows:

Add	Adds the number in the keyboard to the number in the accumulator, and leaves the sum in the accumulator.
Clear	Sets the accumulator to zero.

More operations will be added to this list as they are found to be desirable.

3. The Notebook

The notebook contains a list of instructions and numbers that tell the operator how to solve the problem. This list must be prepared by a mathematician and written into the notebook. We will specify that our notebook contains 2048 lines numbered from 0 to 2047. There is room on each line for one instruction, or one number. There is not room for both. Only those instructions that are understood by the operator may be used.

b. The Programmer's Viewpoint

How does this system appear to the mathematician who must use it? In its present state it presents severe limitations. One obvious handicap shows up when we wish to know which of two numbers is the larger. Suppose for example that instructions have been written to store number A on line 73 and number B on line 74, and that the larger is to be used in further computation. If we are restricted to the stated vocabulary, the problem is insolvable. If we introduce a subtract instruction the solution is extremely simple. "Subtract" will be defined as follows:

su x	Subtract from the accumulator the number on line x. Leave the difference in the accumulator. If the difference is zero, it is considered positive.

We are now prepared to write a list of instructions that will enable the operator to solve the problem. One possible list is as follows:

1.	ca73	
2.	su74	The "tr 7" instruction means the same as "tn 7"
3.	tn 6	except that it is independent of the contents of
4.	ca73	the accumulator. It is called "unconditional
5.	tr 7	transfer".
6.	ca74	
7.	halt	

After these instructions are performed, the accumulator will contain the larger of the two numbers A and B.

Questions:

1. If A and B are equal, which one will be chosen?
2. How should the program be changed so that the other would have been chosen?

c. Subtraction with an Adding Machine.

Our overall intention is to completely automatize our computing system; "Notebook", "Adding Machine", and "Operator". With this in mind, some of our specifications will be dictated by engineering convenience. The subtract instruction is a good example of this.

If we were to build subtracting circuits into our adding machine, its size and complexity would be nearly doubled. On the other hand, the circuitry needed to change the sign of one of the numbers is almost negligible. If we add this equipment, we can perform the instruction "su x " by the following proceedure.

1. Copy the number on line x into the keyboard.
2. Change the sign of the keyboard.
3. Push the Add button.

This method is used in Whirlwind I. In MTC, however, electronic considerations make it desirable to leave the keyboard intact. We are allowed to change the sign of the accumulator, but this would give us the wrong answer. That is, we would get the contents of line x minus the contents of the accumulator - the reverse of the desired result. However, since this result is in the accumulator, we can correct it by changing the accumulator sign again. In summary, the instruction "su x" can be performed by the procedure below. The only additional equipment needed is a "complement accumulator" * pushbutton.

To perform "su x",

1. Copy the number on line x into the keyboard.
2. Push the complement accumulator button.
3. Push the add button.
4. Push the complement accumulator button.

Question:

1. How can we do the instruction "clear and subtract x" ?
2. " " " " " " " " "subtract magnitudes x" ?

See MTC Programming Manual M-2527 for definitions of the above instructions.

* As used here the word "complement" denotes an electronic operation that results in changing the sign of the number in question. The mathematical use of the word is described in section III of this memo. The engineering use is discussed in section IV and will be covered in detail in later chapters of this training course manual.

d. Sample Program

Perhaps the most fundamental operation in arithmetic is counting. The familiar addition table can be formed through "counting by ones". The multiplication table can be found by counting additions. Nearly every program written for automatic digital computer solution includes some form of counting. As an example, consider multiplication by counting additions. The product of the numbers on lines 101 and 102 is desired. It is assumed that these numbers will not cause an overflow upon multiplication. (This assumption is justified later on.) Line 105 is to contain the answer. The program below uses this line to contain the partial sums as well. Line 103 contains the "count" and is called the "counter". Line 104 contains the counting increment, in this case it is plus one. Thus:

101	-	Multiplicand
102	-	Multiplier
103	-	counter
104	-	1
105	-	partial sums and answer

The program can be written anywhere in the notebook. For example it could start at line # 507.

507	-	ca 101	} Perform addition
508	-	ad 105	
509	-	st 105	
510	-	ca 104	} Increase counter
511	-	ad 103	
512	-	st 103	
513	-	su 102	} Test Count - if not complete return to 507 to make another addition.
514	-	tn 507	
515	-	halt	

Questions:

1. Overlooking overflow considerations, does this program work if the numbers are 3 and 4 ? Does it work for any numbers? What if the numbers are negative? If not, what changes or additions should be made?

2. Suppose the numbers A, B, and C were stored on lines 101, 102, and 103. How can the present vocabulary be used to find (A + B - C) ?

3. Division can be performed by successive subtraction. Assuming that the numbers A and B are stored on lines 101, and 102, how can the quotient A/B be found. What further assumptions will simplify the program?

e. Fractional Representation for Numbers.

Later on we shall add the instruction "Multiply by the contents of line x " (mh x) to the operator's vocabulary. The ability to multiply brings up the question of number length and the position of the decimal point. Consider a calculating machine with a keyboard length of two digits. With the decimal point at the right , we would have to extend the accumulator two places to the left in order to accomodate the largest products. For instance, 99 x 99 = 9801. If the next instruction were to attempt multiplication by 99 again, we would obtain 9801 x 99 = 970299 . Thus we should be forced to limit the number of successive multiplications or to extend the accumulator indefinitely.

This difficulty is overcome in MTC and WWI through a sacrifice of accuracy. If we consider the decimal point to be at the left, then all numbers in the accumulator and keyboard are less than unity and any product is smaller still. To retain full accuracy from a single multiplication, a right extension of the accumulator is needed. In MTC and WWI this extension is called the"B Register". It is the same length as the accumulator. With the present vocabulary, the B register is not available to the programmer. Multiplication will fill the B register, but as yet no instruction has been specified that will use its contents. An entire class of instructions, the "Shift Class", will be introduced later for this purpose. We shall find that the ability to shift numbers along the extended accumulator will greatly simplify the task of multiplication with an adding machine.

Questions:

1. Does fractional representation affect addition and subtraction?

2. That is, does the position of the decimal point make any difference in a program that does not involve multiplication and division?

3. Does it affect counting?

f. "Coded" Instructions

At present, the operator must be able to read. That is, he must recognize the letters of the alphabet and identify several combinations or words. He must also recognize numbers. For example , numbers are used to specify which line of the notebook a given instruction makes reference to. The lines are numbered from 0 to 2047 - thus there is room on a given line for a line number and some other number that is a multiple of 2048. To make the job of mechanization easier, code numbers are assigned to each operation in the operator's vocabulary. For example, the operation "multiply" is given code #1 in MTC. The instruction mh 607 would be coded as (1 x 2048) + 607 = 02655. The

separation of address and coded operation is obvious when the instruction is written in octal or binary form. This matter is discussed in detail in section III of this memo. The numbers chosen for the various instructions of the vocabulary can be picked at random. In MTC, engineering considerations made it desirable to group instructions with similar functions. For example, all instructions that refer to the notebook have code values less than 16. Those that have no reference to storage have code values greater than or equal to 16. Other computers, such as WWI for example, have completely different code values.

g. Summary

The computing system that has been described has been designed with an eye toward eventual automatization. Through specification of a restricted vocabulary the implication has been made that the operator is to do only what he is told. He is to do nothing on his own iniative. This makes our automatization possible, but it puts the responsibility squarely on the programmer. The program written for multiplication will not work if the multiplier is negative. This shortcoming surely is not the fault of the operator, notebook, or adding machine. The programmer must forsee all such difficulties.

By "coding" our operations as numbers we have made it impossible to tell if a given line in the notebook contains a constant or an instruction. Thus the programmer must inform the operator of the starting point of his program. Since the operator is to perform instructions sequentially there should be no confusion. With this system a programming error could cause the operator to wade through a block of constants as if they were bonafide instructions. The operator does what he is told. He can not tell if it makes sense or not.

Table I is a summary of the present vocabulary. It lists each instruction and gives the programmer's and operator's viewpoints separately. Later chapters in this series will extend this table to the 26 instructions of the MTC Operation Code.

Table I (MTC Instruction Mnemonics)

Instruction	Programmer's Viewpoint	Operator's Viewpoint
Add (ad x)	Add the number stored on line x to that in the accumulator. Leave the sum in the AC. If the sum is zero it is negative.	Copy the number on line x into the keyboard. Push the "Add KB to AC" pushbutton on the adding machine. Proceed to next instruction.
Clear & Add (ca x)	Copy the number on line x into the accumulator.	Push "Clear Accumulator" Proceed as for (ad x).
Subtract (su x)	Subtract the number on line x from the number in the accumulator. Leave the difference in the accumulator. If the result is zero, it is positive.	Copy the number on line x into the Keyboard. Push "Complement AC". Push "Add KB to AC". Push "Complement AC". Proceed to next instruction.
Clear & Subtract (cs x)	Put the negative of the number on line x into the accumulator.	Push "Clear AC" Proceed as for (su x).
Store (st x)	Copy the number in the Accumulator onto line x. Previous contents of x are lost.	Erase line x. Copy the number in the accumulator onto line x.
Transfer (tr x)	Take next instruction from line x.	Take next instruction from line x. Proceed sequentially from this line.
Transfer if neg. (tn x)	If accumulator is negative, proceed as for tr. If AC is positive, ignore this instruction and proceed to the next.	If accumulator is negative, proceed as for tr. If AC is positive, ignore this instruction and proceed to the next.
Multiply (mh x)	Multiply the number in the accumulator by the number in x. The most significant digits of the product are left in AC. The least significant half is stored in the B register.	Without additional equipment, the operator is unable to do this instruction. The means whereby the operator can multiply is discussed in later chapters.
Halt (ha --)	Halt. The address section is not needed	Do nothing. Do not proceed to next instruction.

III. The Octal and Binary Number Systems.

a. Introduction

The paragraphs that follow discuss two number systems that are unfamiliar to most people. In explaining these systems some familiar number system must be used as a language. In this memorandum the "language" used is the decimal number system. Numbers that are not intended to be interpreted decimally will be tagged (b) for Binary, and (o) for Octal.

The use of binary numbers was chosen because of engineering convenience. As will be shown, the binary system dictates the use of "on-off" components such as relays or flip-flops, whereas the decimal system requires devices with ten stable states. Since "on-off" operation is much simpler, it is more desireable from an engineering point of view.

b. Fractions - Decimals - "Radix"

This discussion might just as well begin with fractions since it has been stated that only fractions will be used within the machine. Fractional notation was chosen because it limits overflow problems to the addition and subtraction operations. (Division could still cause trouble, but MTC has no divide operation and hence it does not concern us here.)

When a fraction is represented as a "decimal" there are certain understood rules and descriptions that are so familiar that we seldom think about them. For example:

1. The "decimal point" serves as a reference. Digit positions are counted from this point.
2. Empty positions are indicated by the figure "zero". The use of positions and zeros was a major step in the science of number theory. It is often spoken of as " The Discovery of Zero .". Note that the Romans had no zero!
3. Decimal positions refer to fractions based on the number ten. The first position tells the number of tenths, the second - hundreths, the third - thousandths, and so forth. For example:

$.765$ means $\frac{7}{10} + \frac{6}{100} + \frac{5}{1000}$

$.8005$ means $\frac{8}{10} + \frac{0}{100} + \frac{0}{1000} + \frac{5}{10,000}$

4. Some fractions can be represented <u>exactly</u>. For example:

$\frac{1}{2} = \frac{5}{10} = .5 \qquad \frac{1}{4} = \frac{2}{10} + \frac{5}{100} = .25$

$\frac{1}{64} = \frac{0}{10} + \frac{1}{100} + \frac{5}{1000} + \frac{6}{10,000} + \frac{2}{100,000} + \frac{5}{1,000,000} = .015625$

5. Some fractions can not be represented exactly. For example:

$$\frac{1}{3} = \frac{3}{10} + \frac{3}{100} + \frac{3}{1000} + \cdots + = .333\cdots \text{etc.}$$

$$\frac{1}{7} = .142857\ 142857\ 142857 \text{ --- etc.}$$

These are called repeating decimals.

Note that in writing fractions as decimals, we drop the denominators of our "base ten" fractions and supply the "decimal point" as a reference. For example:

$$\frac{1}{4} = \frac{2}{10} \# \frac{5}{100} = .25 \qquad \frac{1}{2} = \frac{5}{10} \# \frac{0}{100} = .50$$

Note that each digit position can contain any of ten symbols - 0,1,2,3, 4,5,6,7,8,and 9. Mechanization of a "digit position" would therefore require a device with ten positions. (Take a telephone dial for instance.)

The number "ten" has no special attributes. We might have chosen a different set of denominators. "Ten" was probably chosen because human beings have ten fingers. Suppose, for example, that we chose the number "two" as our base. Each succeeding denominator is now twice its predecessor, rather than ten times. Thus:

$$\frac{3}{4} = \frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{0}{16}$$

$$= \frac{1}{2} \# \frac{1}{4} \# \frac{0}{8}$$

$$= .110\ (b)$$

A system based on the number "two" is called the "Binary System". Each position can contain one of two symbols - 0 and 1. Any numerator greater than 1 would reduce to the adjacent position. For example:

$$\frac{2}{8} \Rightarrow \frac{1}{4} \qquad \frac{2}{16} \Rightarrow \frac{1}{8} \qquad \frac{2}{4} \Rightarrow \frac{1}{2}$$

With this system as with the decimal system, some fractions can be represented exactly and some repeat indefinitely. A "point" is used as a reference and empty positions are indicated by zeros. The binary system is exactly analogous to the decimal system. Their only difference is in the base number.

Note that any base number can be used. Ten is commonly used because we are used to it. Two is useful in connection with computers for engineering reasons. Eight and sixteen are used in the computer field as convenient short-hand notations for binary. Twelve is used occasionally because many more common fractions can then be expressed exactly.

The base number of a system is often called the "radix"of the system. Likewise, the reference point is known as the "radix point".

Questions:

1. Change the fraction 2/3 into the forms indicated.

   a. ?/10 + ?/100 + ?/1000
   b. ?/12 + ?/144 + ?/1728
   c. ?/8 + ?/64 + ?/512
   d. ?/2 + ?/4 + ?/8 + ?/16
   e. as a decimal.
   f. in binary form.

c. Powers and Exponents

Representation of mixed numbers and integers with positional number systems is more easily described through the use of exponents or powers. A complete coverage of this mathematical notation can be found in any Algebra book. A review of the basic principles is given here.

1. Six raised to the second power is 6 x 6 or 36. It is written 6^2, and is often called "six squared". Likewise, six raised to the third power, written 6^3 and called "six cubed", is 6 x 6 x 6 or 216. The "power" or "exponent" is written as a superscript and indicates howmany times the "base" is to be multiplied by itself. Thus:

   $a^3 = a \times a \times a$

   $2^4 = 2 \times 2 \times 2 \times 2 = 16$

   $3^5 = 3 \times 3 \times 3 \times 3 \times 3 = 25 \cdot 3$

   $a^n = (a \times a \times a \ldots . a)$ (where "a" appears "n" times)

2. Arithmetic

   a. Addition and Subtraction

   The numbers must be reduced. For example:

   $3^2 + 2^3 = 9 + 8 = 17$

   $3^2 - 2^3 = 9 - 8 = 1$

   b. Multiplication

   If the bases are the same, we multiply by adding exponents. Thus:

   $2^3 \cdot 2^2 = (2 \times 2 \times 2)(2 \cdot 2) = 2 \times 2 \times 2 \times 2 \times 2 = 2^5 = 32$

   c. Division

   If the bases are the same, we divide by subtracting exponents. Thus:

   $\frac{2^3}{2^2} = 2^{(3-2)} = 2^1 = 2$

$$\frac{2^4}{2^2} = \frac{2 \cdot 2 \cdot 2 \cdot 2}{2 \cdot 2} = 2^{(4-2)} = 2^2$$

d. Negative Exponents mean reciprocals. For example:

$$\frac{8^4}{8^7} = 8^{(4-7)} = 8^{-3} = \frac{1}{8^3}$$

$$2^{-3} = \frac{1}{2^3} = \frac{1}{8}$$

a^{-n} means $\frac{1}{a^n}$

e. The "zero" exponent means unity. For example:

$$\frac{5^2}{5^2} = 5^{(2-2)} = 5^0 = 1$$

$$\frac{a^N}{a^N} = 1 = a^{(N-N)} = a^0$$

f. Summary

1. a^n means "a" times itself "n" times.
2. Addition of exponents with <u>like bases</u> is multiplication
3. Subtraction of " " " " is division.
4. Negative exponents mean reciprocals.
5. Zero exponent means unity with <u>any</u> base.

d. Mixed Numbers and Integers.

Using exponent notation, a decimal fraction can be described as follows.

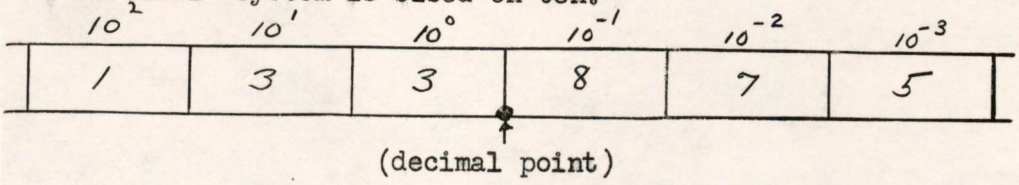
$\frac{1}{4} = 0.25 = 2 \times 10^{-1}$, plus 5×10^{-2}, plus 0×10^{-3}, plus ...

The same fraction in binary form is:

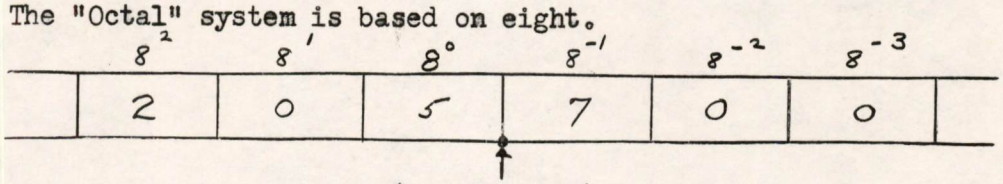
$\frac{1}{4} = 0.01 = 0 \times 2^{-1}$, plus 1×2^{-2}, plus 0×2^{-3}, plus ...

Mixed numbers and integers are handled by an extension of the system to the left. For completeness, all three systems - decimal, binary, and octal are diagrammed on the next page.

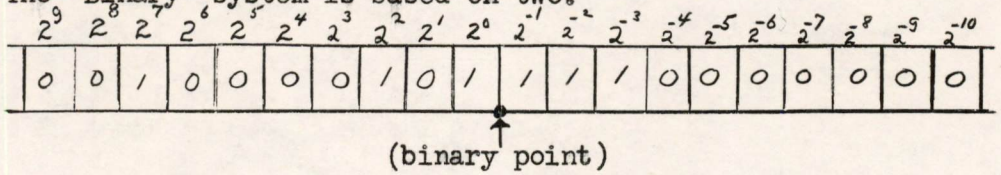
The "Decimal" system is based on ten.



The "Octal" system is based on eight.



The "Binary" system is based on two.



The number expressed above is 133 and 7/8 . In decimal representation, we have 133.875 or:

	1×10^2	= 100.000
plus	3×10^1	= 30.000
"	3×10^0	= 3.000
"	8×10^{-1}	= 0.800
"	7×10^{-2}	= 0.070
"	5×10^{-3}	= 0.005
		133.875

Using octal representation we have 205.700 or:

	2×8^2	$= 2 \times 64$	= 128.000 (d)
plus	0×8^1	$= 0 \times 8$	= 0.000 "
"	5×8^0	$= 5 \times 1$	= 5.000 "
"	7×8^{-1}	$= 7 \times 1/8$	= 0.875 "
"	0×8^{-2}	$= 0 \times 1/64$	= 0.000 "
			133.875 (d)

Using binary representation we have 10000101.111000000 or:

	1×2^7	$= 1 \times 128$	= 128.000 (d)
plus	1×2^2	$= 1 \times 4$	= 4.000 "
"	1×2^0	$= 1 \times 1$	= 1.000 "
"	1×2^{-1}	$= 1 \times \frac{1}{2}$	= 0.500 "
"	1×2^{-2}	$= 1 \times \frac{1}{4}$	= 0.250 "
"	1×2^{-3}	$= 1 \times 1/8$	= 0.125 "
			133.875 (d)

e. Counting

We learn to "count" at an early age. Every small child seems to know when some other child has "more" marbles than he has. The symbols and words used in counting express "how many" in a way that can be understood by others. What is "counting" ? In the terms of the mathematician, " counting" means putting a set of symbols into a one-to-one correspondence with the objects to be counted. In other words, counting symbols or numbering systems are a language. Several such languages are in use today. Four of them are illustrated below.

Roman Numerals	Arabic Base 10 (decimal)	Arabic Base 8 (octal)	Arabic Base 2 (binary)
--	0	0	0
I	1	1	1
II	2	2	10 (b)
III	3	3	11 "
IIII	4	4	100 "
V	5	5	101 "
VI	6	6	110 "
VII	7	7	111 "
VIII	8	10 (o)	1000 "
VIIII	9	11 "	1001 "
X	10 (d)	12 "	1010 "
⋮	⋮	⋮	⋮
XIIII	14 (d)	16 (o)	1110 "
XV	15 "	17 "	1111 "
XVI	16 "	20 "	10000 "

In every-day use, words such as "twenty", "thirty", and "hundred" and the corresponding symbols have a built in decimal bias. In the computer field, identical words and symbols are used with different meanings. In order to be understood, we must specify what language (number system) we are speaking. For example 16 (o) , 14 (d), and 1110 (b) are all equivalent to XIV (Roman). To say or write"sixty" - would be ambiguous unless the system is specified.

f. Conversion

From the diagram in section "d" we see that each position counts by some power of the base. For instance, the second position to the left of the radix point counts by 10's in the decimal system, by 8's in the octal system, and by 2's in the binary system. In general the positions count differently in each system. Notice, however, that the "zero" position is the same for all three systems. It always counts by "ones". We shall use this in all our conversion methods.

Suppose we wish to find the binary representation that corresponds to 0.875 (d). One method is by repeated multiplication by 2. Let us see why this method works. The base of the binary system is 2. The

base of the decimal system is ten. Multiplication by the base in the decimal system moves the number one place to the left. The same is true for the binary system. Consider the number 0.001 (b). In fractional notatation this is 1/8 . Multiplying by 2 we get 1/4 or $0.010_{(b)}$. The number has been shifted to the left. Another example:

0.101	=	1/2	+	1/8	
times 2	=	1	+	1/4	= 1.010 (note shift to left)
times 2 again	=	2	+	1/2	=10.100

Perhaps the conversion method toward which we are leading is becoming clearer. We have found that multiplication by two shifts the number once to the left. Note that the first binary digit is shifted from the 2^{-1} position into the "ones" position ! In the ones position it means the same in any language. Thus by repeated multiplication of two we can spill the binary bits one by one into the "ones" bit position:

.875 (d)
x2
1.750 The first bit is "1".

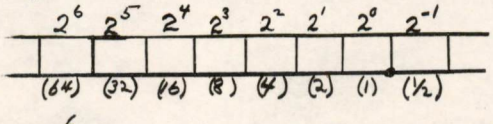
.750
x2
1.500 The second bit is "1".

.500
x2
1.000 The third bit is "1".

.000
x2
0.000 All succeeding bits are "0".

The binary equivalent to .875 (d) is then .11100....

The above method is good for numbers less than one. If the decimal number is an integer, we must resort to another method. If a mixed number, both methods are used. That is, the fractional part and integer part are converted separately. One method for integers is given below. The diagram may be helpful. We wish to convert 30 (d) to its binary form.



What goes into the 2^6 position? ie. How many 64's are there? By trial and error we find that there are no 64's, no 32's, one 16, one 8, one 4, one 2, and no ones. We can now fill in the binary positions. The binary form of 30 (d) is therefore 11110 (b) .

Conversion from decimal to octal is done in a similar manner. Starting with the highest power of 8 that is part of the number, we fill each octal position down to the "ones" position. The fractional part can be handled the same way, or by another method.

Conversion from octal to binary or vice-versa is extremely easy. Notice that three binary bits are equivalent to one octal digit. This can be seen from the fact that the largest binary number in three bits is 111 (b) or 4 + 2 + 1 = 7 (o). The next higher binary number must use the next position and the next higher octal number must do so also. Thus if one memorizes the binary representation for the octal digits from 0 to 7, conversion between octal and binary is accomplished by inspection of each group of three bits.[σ] It is for this reason that the MTC display lights are grouped in sets of three lights each.

Questions:

a. Convert 5 days, 10 hours, 3 minutes, and 30 seconds into seconds.
b. Convert 1100111 (b) into its decimal form.
c. Do you notice any similarity between questions a and b ?
d. Convert 100,000 seconds into days, hours, minutes, and seconds.
e. Convert 43 (d) into its binary form.
f. Do you notice any similarity between questions d and e ?

g. Negative Numbers - Complements

In section II-c we stated that subtraction can be accomplished by adding the negative of the subtractor. Because of engineering considerations we had to add the negative of the subtrahend and hence were forced to change the sign of our answer. This may seem like so much double-talk but it isn't. For example, when the temperature drops from A degrees to B, how far has it dropped ? You might say "(A-B) ". But what if B is ten below (ie - 10)? Suppose they are both negative? Find the temperature drop from A to B for the following values:

A =	and B =
59,	41
59,	-14
-10,	-40
40,	50
-15,	-5

From a consideration of the temperature scale we can derive the following rules for the addition and subtraction of negative and positive numbers.

1. When we write (4-2) we will associate the minus sign with the 2. Thus we could have written (-2 + 4). Since we keep the sign with the number, the order is unimportant.
2. Minus a Minus is a plus. That is: - (-) = + .

[σ] Note also that the octal base "8" is simply related to the binary base "2". That is, $8 = 2^3$. Thus 3 binary bits are equivalent to one octal.

3. -(+) = - , +(-) = - , +(+) = + That is, an odd number of minus signs results in minus, an even number results in plus.

4. The same rules apply for multiplication.

Now that negative numbers are understood we can proceed to outlining the method we shall use for their representation in the machine. We need a system that will add or subtract signed numbers. Since we can change the sign of numbers, we need consider only the addition process.

There is an old parlor trick that gives a clue to the method we shall use. The magician asks for a number from the audience. Leaving room for four more numbers, he writes the sum of all five! Then he asks for the second, writes the third, asks for the fourth, and writes the fifth. Since he has the last turn, he can of course pick a number that will make the sum correct, but he works so fast that it must be magic. The answer he wrote turns out to be correct ! For example:

Step 1	Step 2	Step 3
432073	432073	432073
-	391046	391046
-	608953	608953
-	-	712416
-		287583
2432071	2432071	2432071

Let us look carefully at the numbers the magician supplied:

432073

391046 } = 999999 or(1,000,000 - 1)
608953 }

712416 } = 999999 or(1,000,000 - 1)
287583 }

2432071 = 432073 + 2,000,000 - 2

This can be rewritten.

432073	432073	432073
391046	391046	391046
(999999-391046)	-391046 + 999 999	+608953
712416	712416	712416
(999999-712416)	-712416 + 999 999	+287583
	432073 +1999,998	2432071
		→ +2
		432073

The "end around carry" subtracts 2,000,000 and adds +2. Thus the complements (999999 - 391046 for example) can be used to represent negative numbers.

A method similar to this is used to represent negative numbers in MTC. In the above example, the numbers added to 999999. In the binary case we will choose numbers that add to 111111 (i.e. all "ones"). Thus "minus" 1/4 becomes .101 because .010 + .101 = .111 . In this form, it is impossible to tell whether .101 means - 1/4 or +5/8 . We therefore must supply another bit position to indicate the sign. For convenience we use the left end of the number. Notice that this bit is not considered the 2^0 position. All numbers in the machine are still fractions. A "0" in the sign bit position means that the fraction is positive. A "1" in the sign digit position means that the fraction is negative and has been complemented. Try a few examples:

How would the following be represented?

+ 1/4 ... -5/8 ... +5/8 ... -1/4 ...-1/2

Have you noticed how simple it is to complement a binary number? For example, the complement of 0.010 is 1.101 . We have merely interchanged the ones and zeros ! As we shall see later, this change is easy to accomplish electronically.

h. Arithmetic

In this section we shall discuss binary addition, subtraction, and multiplication. For clarity we shall discuss decimal arithmetic first. Then we shall turn to binary arithmetic, and finally to the manipulation of negative numbers in complement form.

1. Addition

We are all familiar with the process of addition, but before we can design a machine to do the work for us we must outline in gross detail just what addition is. In school, we learn to "add" by memorization of the "addition table" and by following a set of rules concerning carries. The process was somewhat as follows:

a. Consider the "ones" column. Look up the sum in the table. Write the "ones" digit from the table into the "ones" position of the answer. "Carry" the ten's digit from the table to the next column.

b. Consider the next digit column and the previous carry, and proceed as before.

In MTC we shall always limit ourselves to the addition of a pair of numbers - one in the accumulator, and one in the "keyboard" register. We shall use a special method to add in the "carries" as a separate operation.

For example:

```
 .019
+.097
 . 06   (From addition Table)
 . 11   (to carry)
 .116   (Answer)
```

Binary addition is completely analogous. However, before we start we must form the binary addition table:

+	0	1
0	0	1
1	1	10

Binary Addition Table

Now we can add two binary fractions using the binary addition table, and the same rules of addition. For example, 1/4 +1/4 = 1/2 .

```
1/4 + 1/4 = .010
          + .010
            000   (from table)
          + 100   (to carry)
            .100  (answer)    note: 0.100 (b) = 1/2 !
```

What are the rules for addition with negative numbers expressed in complement form? The rules are given below. The paragraph following them shows how they were derived.

1. The "complement" or "negative representation" of a number is found by changing all ones to zeros and all zeros to ones, including the sign bit.

2. The sign bits are considered as part of the number - - that is a "Carry" from the first position to the right of the binary point is added into the sign digit column. (This is "end around carry".)

3. If there is any carry out from the sign digit column, it is added to the extreme right hand end of the number.

4. Overflow i.e. a result greater than unity , is detected by the occurence of an incorrect sign bit. Two fractions with unlike sighs cannot cause overflow. Like signs should produce a result with same sign.

5. All "ones" i.e. 1.111 111 111 111 is the complement of all "zeros" and is called "minus zero". All "zeros" is called "plus zero".

Some examples:

1/2 + 1/4 = 3/4

```
  0.100
+ 0.010    (no end around carry)
-------
  0.110
```

3/4 + 3/4 = 1.5

```
  0.110
+ 0.110
-------
  1.100  = -1/2  (Wrong sign - hence overflow)
```

-3/4 + 3/4 = 0

```
  1.001
+ 0.110
-------
  1.111  = - 0
```

-1/2 + -1/4 = -3/4

```
  1.011
+ 1.101
-------
 (1)1.000
    --> +1     (end around carry)
-------
  1.001  =  -3/4
```

-3/4 + -3/4 = -1.5

```
  1.001
+ 1.001
-------
 (1)0.010
    --> +1     (end around carry)
-------
  0.011  =  +3/8 (Wrong sign - hence overflow)
```

An interesting example is -0 + (-0) or -0 + (+0):

```
  1.111 111
  1.111 111
-----------
(1)1.111 110  = -0
    --> +1
-----------
  1.111 111  = -0
```

```
  1.111 111
  0.000 000
-----------
  1.111 111  = -0
```

Where did we get these rules? Consider a binary number 15 bits long. The last bit is the 2^{-15} position. Let us see what the "end around carry" has accomplished.

First we must get a mathematical notation for the "complement" of a number. In finding complements we changed ones to zeros and vice-versa in order to get the number to add up to "all ones". That is, we subtracted our number from 1.111 111 111 111 111. (The use of 1.111 111 111 111 111 is called the "ones complement" system.)

Notice that this binary number is almost 2. That is, if we add 0.000 000 000 000 001(b) or 1 x 2^{-15}(d) the sum is 2. Now the "complement" of "a" can be expressed:

$$(1.111\ 111\ 111\ 111\ 111 \quad -\text{"a"})$$

or

$$2 - (1x2^{-15}) \quad -\text{"a"}$$

When we add some other negative number say "b" we wish to obtain our answer in the same form! i.e.

$$2 - (1x2^{-15}) \quad -a \ -b$$

Now straight addition gives:

$$\begin{array}{r} 2 - 2^{-15} - a \\ +\quad 2 - 2^{-15} - b \\ \hline 2 + 2 - 2^{-15} - 2^{-15} - a - b \end{array}$$

and "end around carry" removes a "1" from the 2^{1} position and adds a "1" to the 2^{-15} position. It therefore subtracts "2", and adds "2^{-15}". We are left with: $\left[2 - 2^{-15}\right] - a - b$ or $\left[1.111\ 111\ 111\ 111\ 111 - a - b\right]$ —— which is the result we were seeking !

2. Multiplication:

The school-boy method for multiplication is as follows:

1. 1-6x9 is 54 (from table) -4 and 5 to carry
   6x2 is 12 (" ") -2 and 1 to carry ∴ 174
   is first partial Product.
2. 7x9 is 63 (from table) -3 and 6 to carry
   7x2 is 14 (" ") -4 and 1 to carry ∴203
   Second Partial Product.
3. Shift to the left and add.
4. Point off in the multiplier and 2 in the multiplicand.

The school-boy who asks why any of these steps are taken, or "Where did the multiplication table come from?", is quickly squashed. Perhaps he is told that the multiplication table came from the same place that the addition table came from! (And everybody knows that!) Well where did these tables come from! They came from counting! The addition table comes first and from it the multiplication table can be derived.

For example:

What is the sum of 6 and 4. The natural thing to do is count it off on your fingers. Count 6 fingers, then 4 more and the answer is ten. The whole addition table can be found this way and once found it can be memorized. Well then how about the multiplication table? Four "times" six means four groups of six each or six plus six plus six plus six. Thus with the addition table and the rules of addition, we can easily form the multiplication table.

Now let us form the multiplication table for binary numbers. The only symbols are 0 and 1 hence there are only 4 entries.

x	0	1
0	0	0
1	0	1

Binary Multiplication Table

The rules for using this table are the same as for decimal but since there are no "carries", the process is much simpler.

For example: 6/8 x 5/8 = 30/64 (d) = 15/32 (d)

$$
\begin{array}{rr}
 & .110 \\
\times & .101 \\
\hline
 & 110 \\
 & 000 \\
 & 110 \\
\hline
 & .011110
\end{array}
$$

.011 110 = .36 (o)

.36 (o) = 3/8 + 6/64 = 12/32 +3/32 = 15/32 (d) (which checks)

Negative Numbers:

We have no tricky method for multiplication with negative numbers. When the multiplier is negative, we make it positive, multiply, and then make the answer negative again. (This is called "sign control".)

3. Division:

Since MTC has no divide instruction we need not dwell on the subject of division. We are aware that in decimal arithmetic "long division" consists of rules concerning "trial divisions", the multiplication table, subtraction, and shifting. In binary

arithmetic the process is simplified by the lack of carries in the multiplication table. As with multiplication, we work with positive numbers only and supply the proper sign after the division has been acomplished.

Questions:

How would you add with Roman Numerals?
(Hint: Be careful! Do you need a table?)

How about subtraction?

How about multiplication?

In decimal multiplication do we have to shift left?

That is could we have shifted right?

What is 64(0) x 144(0)? (Do not convert to decimal except to check answer.) (Hint: Form the Octal multiplication table.)

1. Summary:

The word "arithmetic" comes from a Greek word that means "to number". To "number" means to assign names and symbols that convey to others the answer to the question "How many?" We found that several numbering systems are in use, some of them "positional" (e.g. Decimal, Octal, Binary), and some "non-positional"(e.g. Roman). The familiar operations of addition and multiplication were considered as faster means for counting "upward". Subtraction and division were faster means for counting "downward". The binary system was chosen for engineering convenience in the storage of numbers, but it was found that it allows important simplifications in the arithmetic operations as well. We decided to learn the octal system because it is a convenient "short-hand" for binary. Finally we noted that since both the decimal and octal systems use arabic symbols, we must specify which is in use.

IV. Available Components

We intend to replace our human computing system with one that is completely automatic. It is to have an high-speed notebook, an electronic adding machine, and an electronic operator. Our automatic machine is to be such that we need only write our instructions into the automatic note-book, and push the "START" button.

The notebook is the heart of the machine. What it is, and what it does is simple. It is similar in operation to the familiar tape recorder. In short, it stores information which can be copied easily, erased easily, and changed easily. Most important of all, these operations can be done in a few micro-seconds.(One microsecond = one millionth of a second.). The physics and engineering that describes how this is done will be covered in a later chapter. For the present we will assume that a high-speed note-book is available.

The adding machine and operator make up the rest of the system. Fortunately they can be made from the same building blocks. The adding machine must be able to manipulate numbers arithmetically. The operator must be able to transfer numbers between the adding machine and the note-book, and he must remember such things as which instruction is to be done next, etc.. The operation of the machine can therefore be separated into two areas:

1. The storage, transfer, and manipulation of numbers.
2. The timing, sequencing, and selection of the above.

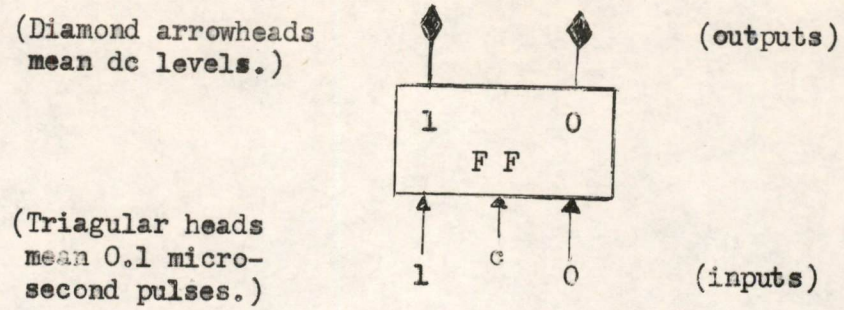
Let us take a look at the components that have been designed to perform these operations.

a. The Mechanization of Numbers - Storage, Transfer, and Manipulation

Storage

To store a binary bit, we need a device that has two stable states - a state we will call "0", and a state for "1". The device must be such that it can be forced to either state, and it must be possible to make it change to the opposite state. The latter requirement is dictated by our desire to use a complenent system for representation of negative numbers. All of these operations are to take place at high speed.

The electronic device used by MTC is called a "flip-flop". It is represented schematically by a"black box" with two outputs and three inputs. We will label the two outputs as the "1" output and the "0" output. In a similar fashion there is a "1" input and a "0" input. There is also a "complement" input. The conventional diagram is shown on the next page.



Block Diagram for a Flip-flop

The major characteristic of a flip-flop is that one output is always "on" or "high", and the other is "off" or "low". That is, the two outputs are never the same. In MTC, "on" or "high" or "up" means that a dc voltage level of +10 volts is available at the so-designated output terminal. The other output will of course be "down". In MTC a voltage level of -30 volts (30 volts below ground) is available at the "down", "off", or "low" terminal of the flip-flop.

The flip-flop is considered to contain a "1" if the "1" output is "high". This condition of operation is also called "set to a "one position", or sometimes just "set".

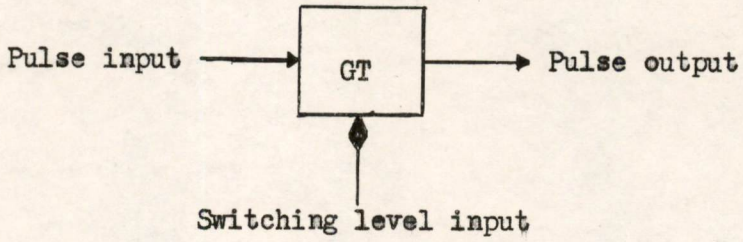
The flip-flop is considered to contain a "0" if the "0" output is "high". This condition is also called "set to a zero", or simply "cleared".

There are three input connections; the "1" input, the "0" input and the "complement" input. The input signal is a voltage pulse such as would result from turning a switch on and off very quickly. In MTC the pulse duration is 0.1 microsecond. The MTC flip-flops respond within 0.5 microseconds.

We are now able to store a number. For our 15 bit binary fractions with the sign bit we require 16 flip-flops. Such flip-flop registers areused in MTC for the "keyboard", the B-register, the accumulator and for many other functions that will be found necessary as we replace more and more of the operator's duties with electronic equipment.

Number Transfers - Copying

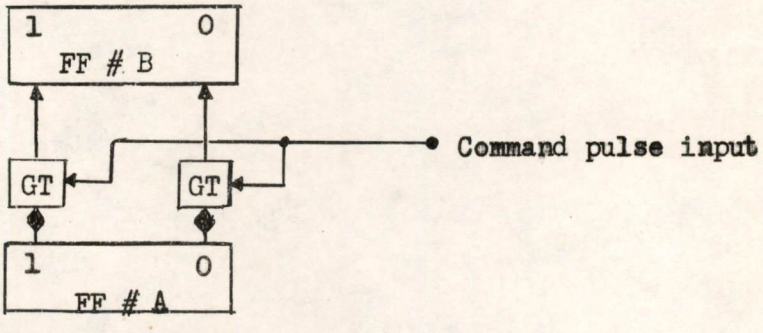
Suppose that we wish to copy a number from flip-flop #A to flip-flop #B. The word "copy" implies that the content of #A is left unchanged. (In computer work the word "transfer" often means the same thing.) Let us consider flip-flop #B. We wish to supply a pulse on the "one" input only if #A contains a one. Likewise we wish to supply a pulse on the "0" input only if #A contains a zero. We need a switch that can be controlled by a dc level such as is obtainable at the output terminals of a flip-flop. Such a switch is called a "gate" or "gate tube". The conventional diagram is shown on the next page.



Block Diagram for Gate Tube

A gate will be "on" if the switching level is "high". In this position the pulse is passed with negligible delay. (Usually about 0.05 microsecond.) A gate will be "off" if the switching level is "low". In this case, the pulse is not passed.

We can use a combination of two gates and a command pulse for number transfer or copying. A possible circuit is shown below.



Copying Circuit

When a pulse appears on the line labeled "command pulse input", the contents of FF #A will be copied into FF #B. The operation will take about 0.55 microseconds. The number in #A is left unchanged.

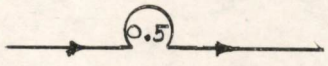
b. Control Functions - Timing, Sequenceing, and Selection

Part of the operation of the computing system consists of the copying or transfer of numbers. Notice that the circuit above will not perform the copying operation until "commanded" to do so by the application of a "command" pulse to the input lead. Let us see what devices we have at our disposal to make sure that these command pulses occur at the proper intervals and in the right order.

The major components we will use for control purposes are:

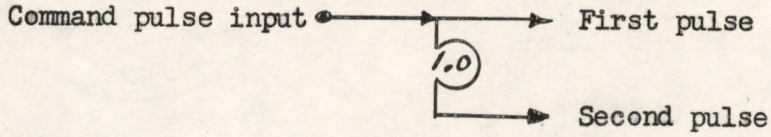
Flip-flops
Gates
Delay Lines
Diode Mixers

We have already discussed the black box characteristics of flip-flops and gates. A delay line is just what the name implies. It is a device that delays a command pulse by a specified amount of time. Schematically it is represented as shown below. The number indicates the length of the delay in microseconds.



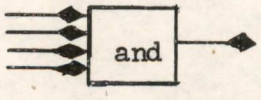
Delay Line - 0.5 microseconds

Delay lines can be used to allow one command pulse to perform a sequence of operations. For example, suppose we need two pulses separated by one microsecond to perform a certain operation. A possible circuit is shown below. The delay lines used in MTC include a pulse amplifier to restore the pulse after the delay. Hence any number can be used in series.

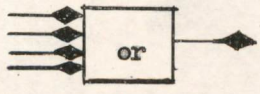


Circuit to Produce Pair of Pulses

Diode mixers are used in MTC in three forms. They are made with the familiar crystal diode. In chapter three of this series we shall discuss the circuitry. Here, we are concerned with the "black box" characteristics. The three mixers we will use are diagrammed below:



"And" or "All" Mixer
(levels)



"Or" or "Any" Mixer
(levels)

"Any" Mixer
(pulses)

Mixers may have several inputs, but only one output. The characteristics are as follows:

1. "And" or "All" mixers - (also called "And gates".) There will be a "high" level at the output terminal only if all of the input levels are "high".

2. "Or" or "Any" mixers - (also called "Or gates".) There will be a "high" level at the output terminal when any input level is high.

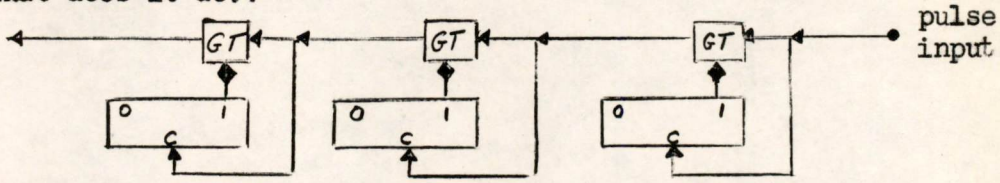
3. It often happens that some circuit is pulsed from several other locations. The pulse mixer is used to keep the input pulses from affecting the other common circuits. It is similar to the "Any" level mixer, the only difference being in the signals that are mixed.

A Few Questions.

1. Extend the "copying Circuit" to handle 4 bit numbers. Note that 8 gates are used. Can this be reduced to 4 gates. What has been lost thereby?

2. We have designed a circuit that produces a pair of pulses. If we have a "clock pulse generator" that is,a device that puts out a series of pulses at specified intervals, we can double the frequency by use of the above-mentioned circuit. Design a circuit to do this and include means for turning it on and off without changing the "clock pulse generator".

3. The circuit shown below is to be supplied with command pulses. What does it do.?

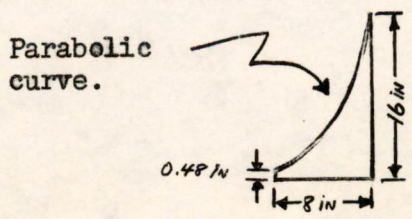


4. Design a circuit that will do the same thing backwards.

V. A Few Words about Programming.

We have discussed a few short programs to illustrate the MTC vocabulary. Let us now discuss a more realistic program. The problem below was chosen because it can be understood by those who do not have a background in mathematics. In actual practice, it probably would not merit machine time.

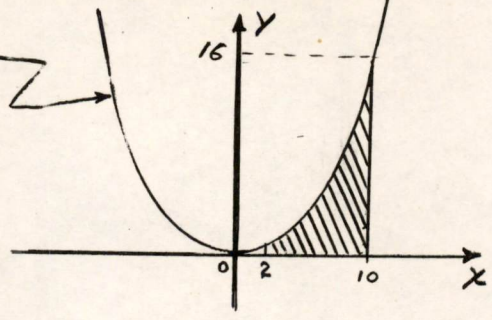
We wish to design an agitator type washing-machine. The problem that is of interest at present concerns the size of the motor. The engineer tells us that he must know the area of the agitator blade in order to compute the load on the motor. The shape of the blade is shown below.



Here are the details of the parabola:

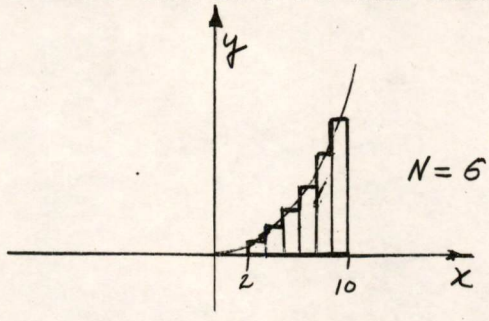
$y = 0.16x^2$

x	y
0	0
±2	0.48
±4	2.56
±6	5.76
±8	10.30
±10	16.00



The shaded part is the area we seek. The equation gives the height of the blade for each point on the base. Now here is a good example of the danger of having a little knowledge. The existence of an equation will send some of us back to study algebra. The fact that seek an area might indicate to some that they had better study integral calculus. But if we were completely unencoumbered by knowledge we might think of drawing one-inch squares on the figure and then obtain the area by counting them. Take a look at our computing vocabulary. Only a glance is needed to see that "counting" is our systems major facility! We shall therefore write a program that will instruct our operator to count a large number of easily outlined areas.

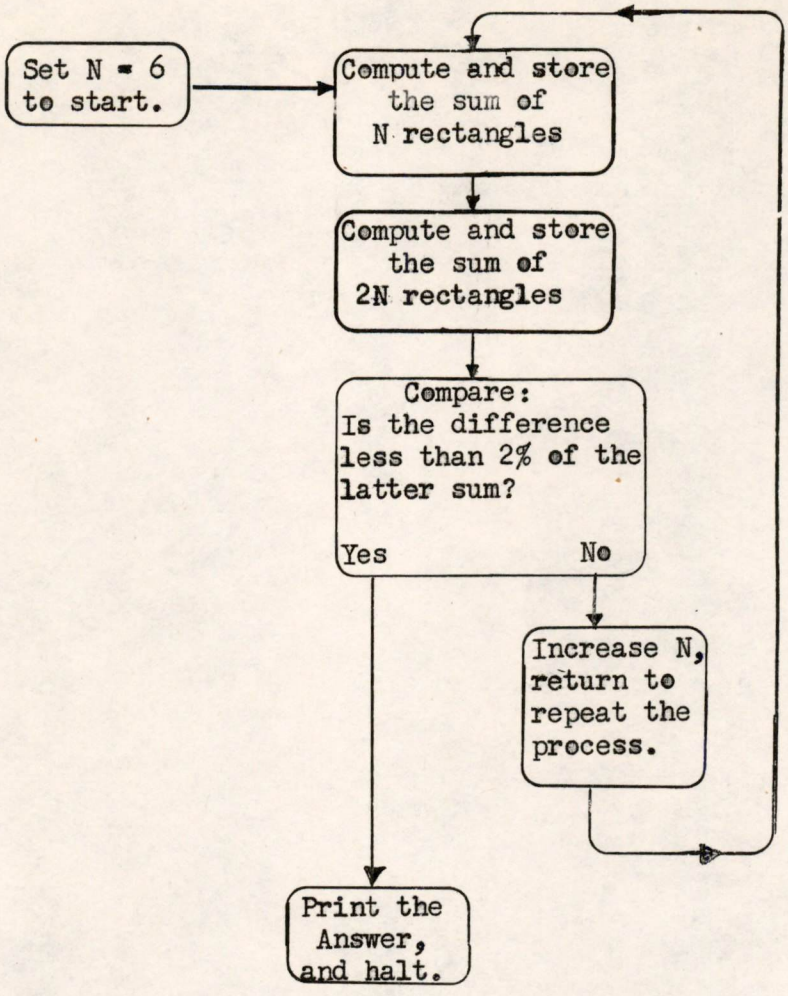
Let us divide the area into several thin rectangles. The thinner



and more numerous they are, the closer the resulting "staircase curve" well be to the true curve. If we add the rectangular areas, we will get an approximate answer. The area of each rectangle is the product of its base and height, where the base is given by eight divided by the number of rectangles chosen, and the height is given by the equation. (The height is equal to $0.16\ x^2$, where x is the distance from the origin of our graph.) All that is left is a means of determining how many rectangles to choose. It can be shown that as the number increases, the difference between successive answers will decrease. For simple curves, the following criterion will serve. (Assume that 2% accuracy is desired.)

> "If the difference between the result for N rectangles and that for 2 times N is less than 2% of the latter result, then the latter result can be accepted as being correct to within + or - 2%. "

The block diagram for our program is therefore as follows:



In writing the program, we write a short program for each block of the above diagram and then put them together. Usually it is wise to test each block separately if possible. Some of these blocks will be easy to program. Others will seem quite difficult. Bear in mind that only the words of the MTC vocabulary can be used! Since we have not yet introduced all of the needed vocabulary, we will not finish the problem here. The enterprising reader should be able to write programs for all the boxes but the last. M-2527, the MTC Programming Manual, contains the needed information for programming the last box. We shall continue the solution in a later chapter.

VI. Summary and Forecast

We have begun a description of the MTC computer by specifying a human system that uses the same vocabulary. The human system that is extremely simple was chosen so that mechanization would be easier. We discussed methods for representation of the process of numbering, and for engineering convenience we chose the binary system. With this in

mind, we investigated the "black box" characteristics of the available components. We found that the computer can be mechanized from flip-flops, gates, delay lines, and mixers in addition to an automatic note-book. Finally, we started the solution of a fairly realistic computer problem.

The tentative outline for the rest of the manual is given below. Each chapter should be available about one month after it has been covered in class. The experience gained in class may dictate changes in the outline so it must be emphasized that the outline below is tentative.

Chapter I - Introduction

a. The Analogous Human System
b. The Binary and Octal Numbering Systems
c. Available Components
d. A Sample Program

Chapter II - An Overall View of MTC

a. From Human Copying to the MTC Bus System.
b. From A Human Operator to Delay Line Control.
c. The MTC Block Diagram of "Central Control".

Chapter III - Specific MTC Circuits

a. The "A Frame" Circuits
b. The Memory Circuits
c. The Control Circuits
d. The In-Out Equipment
e. The MTC Console
f. The MTC Power Supplies

Chapter IV - Programming

a. The Complete MTC Vocabulary
b. The Finished Sample Problem
c. Programming Exercises

Chapter V - Maintenence and Trouble Location

a. Test Programs
b. Marginal Checking
c. Trouble Location Problems

A. Vandebrugh, Jr.

Memorandum 6M-3004

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SUBJECT: TRANSISTOR FLIP-FLOPS FOR HIGH-SPEED DIGITAL COMPUTER APPLICATIONS

To: D. R. Brown

From: Edmund U. Cohler

Date: September 9, 1954

Abstract: The general characteristics of point contact and junction flip-flops are presented. The fastest types are the non-saturating point-contact circuits which will operate at several megacycles. The other types in order of decreasing speed are: saturating point-contact, four-transistor silicon-junction, 4-transistor n-p-n, 4 transistor p-n-p, 2 transistor silicon-junction, 2 transistor n-p-n, and 2 transistor p-n-p. The top speed of the slowest type is about 100 kc, more than an order of magnitude less than the fastest.

The fastest circuits are usually the most sensitive to narrow (less than 0.2 usec) pulses, while the emitter triggered types are most sensitive to low amplitude pulses. The transformer-coupled flip-flop is an an exception to this rule, for it is more sensitive to narrow and low-amplitude pulses than any other type while is not the fastest.

Introduction

This paper is an attempt to summarize some of the designs and capabilities of conventional flip-flops employing transistors. It cannot claim to cover all possible types; it does try to give a general picture of transistor capabilities. Types with which I have had no experience, such as the slave flip-flop or dynamic flip-flop, have been neglected; those I know have been overemphasized. However, experience with these circuits is important because the conventional flip-flop forms the basis of most switching circuits, and is itself the major building block of many computers.

Computer Description

Before I consider the flip-flops themselves it will be wise to give a short description of the computer techniques used at Lincoln Laboratory. The Whirlwind I computer and similar machines use parallel logic which achieves the ultimate in speed and flexibility by sacrificing something to large equipment counts. Most of the logic wired into the machine is implemented with flip-flops and pulse-level "and"

gates. Some explanation is necessary to clarify the terminology we use at Lincoln Laboratory to describe the various types of flip-flop inputs. There are three inputs to the flip-flop: set, clear, and complement. A pulse to either the "set" or "clear" terminal will put the flip-flop into the corresponding state, while a pulse to the "complement" input will always change the state of the flip-flop. The "and" gates employed pass a pulse upon coincidence of a pulse and a high level. Most of the logical nets are realized in plug-in form using these two elements.

Another important facet of these machines should be emphasized. Parallel logic involves relatively large quantities of equipment, and thus each circuit and component must be rigidly reliable. In basic circuit design, this requires a compromise between circuit stabilization and number of components. In order to achieve this goal circuits must be made as simple as possible without sacrifice of good stability.

Terminology

Just as some of the circuit terminology used above is peculiar to Lincoln Laboratory, so is some of the transistor terminology. To clarify this, I will briefly describe the three states (of import to us) of the transistor. First, the state of the transistor in which it is an active element with a power amplification, is called the "active" state. Second, when the current flowing is such that the transistor appears as a low-resistance three-terminal device, like two diodes both conducting to a common cathode, it is said to be in the "on" or saturated state. Third, when it appears as a high-resistance three-terminal device, like two common-cathode diodes back biased, it is said to be "off." These terms correspond closely to the vacuum-tube states of active, saturated, and cut off.

The Two-Transistor Point-Contact Flip-Flop

Design

The most common type of flip-flop is the two-transistor point-contact saturating circuit shown in its basic form in Figure 1. In the lower right-hand corner of Figure 1 is shown the voltage-current characteristic which one observes when looking in at points AA' with R_e removed. This characteristic is called the composite N-curve. It is easily found from the characteristics of the separate transistors and forms the basis for the design of the d-c circuit. A little explanation of this curve will make its use clearer. It is obtained from the single N-curves of the two transistors by adding the emitter currents of each for successive emitter voltages. Each of the branches is then labeled with the states of the two transistors. For instance, the "on-off" branch of the composite curve represents the emitter voltage-current characteristic when one transistor is "on" and the other is "off." Because of the symmetry involved this really represents two different states, i.e., "on-off" or "off-on."

By choosing a suitable load to be inserted in the position of R_e, an operating point may be set anywhere on this characteristic. For instance, to design a saturating flip-flop, one makes the load a simple restistance R_e, whose characteristic intersects the N-curve within the "on-off" region. Moreover, it is desirable that the intersection be just to the right of the valley point. This choice will ensure that one transistor is "on" and the other is "off"; that there is little saturation (thus reducing hole storage to a minimum): and that there is no chance for a third stable state (such as both transistors "on"). Notice that if the load were a resistance of too small a magnitude then there would be two intersections on dark portions of the curve (possible stable points), which would imply three possible stable states: "off-on," "on-off," and "on-on." It is also possible to obtain a stable equilibrium point on the composite N-curve in the active-off region. The vertical load line (current generator) shown in Fig. 1 is typical of such a load line. Thus, a nonsaturating flip-flop might be designed by this method. This, then, indicates how the composite N-curve is used to design the flip-flop for proper steady-state conditions. In addition, several of the possible types of flip-flops to be derived from such a design have been mentioned.

Relative Merits

Saturating Capacitor-Coupled Type. Now it will be well to consider the relative advantages and disadvantages of the various flip-flops of the two transistor type. The simple, saturating, capacitor-coupled flip-flop shown in Fig. 2 has certain advantages over single-transistor and nonsaturating circuits. First, its stability with regard to noise triggering is enhanced by the hole storage in the "on" transistor. Any noise pulse which is too narrow to last beyond the turnoff time of the saturated transistor will fail to trigger the flip-flop, whereas a non-saturating flip-flop, or a single-transistor flip-flop in the "off" state, may be triggered by a much narrower noise pulse. Second, the two-transistor flip-flop is symmetric, which means that it may have gates attached to both sides to provide a logical "and" for both states. The single-transistor flip-flop would require gates of different circuitry to achieve this purpose.

The transient characteristics of a capacitor-coupled flip-flop are determined by the responses of the transistors and the size of the capacitors. In general, the bigger the capacitors are made, the more sensitive the flip-flop becomes, and the wider the range of pulses that can be used for triggering. However, as the capacitors are enlarged the maximum frequency of operation goes down, so that a compromise must be made between sensitivity and speed. The simplest and most sensitive method for complementing such a flip-flop is to apply negative pulses in the emitter circuit. This is accomplished by including a triggering transformer in series with the emitter load (see Fig. 2). A satisfactory set of parameter values is $R_b = R_e = 1500$ ohms, $R_c = 3900$ ohms, $C = 56\ \mu\mu f$, and the supply voltage is -30 volts.

Transformer Coupled Type. An improvement may be achieved in triggering sensitivity by coupling the transient with a transformer instead of two capacitors as is customary. This has the added advantage of causing each of the transistors to act like a blocking oscillator during the switching time which speeds the switching transient. This circuit is shown in Fig. 3. The advantage of the transformer arises partly from this "autoswitching" effect but also from the fact that the transformer couples the current directly from collector to base and the transistor collector acts very much like a current generator in the switching.

Nonsaturating Type. Finally, the nonsaturating circuit of Fig. 4 offers the advantages of speed and sensitivity to narrower triggering pulses. Since there is no saturation of either transistor during operation, there is no delay due to hole storage. This increases the maximum speed with comparable transistors and circuitry by as much as four times and generally about two times. This speed may be a sufficiently important asset to compensate for the concomitant disadvantages. For example, the output levels of nonsaturating circuits are not as consistent as in saturating types unless clamping diodes are added. For example, the output swing may vary by as much as 5 volts in 20 with ordinary variations in the transistors. Moreover, the nonsaturating flip-flop will be more sensitive to narrow noise pulses, just as it is more sensitive to narrow trigger pulses. Such a flip-flop cannot be complemented in the emitter because the impedance of the current generator in the emitter is very large which makes the time constant of the transformer too small to pass a pulse of reasonable width. In this case, triggering may be done with a diode steering circuit (Fig. 4). This causes a decrease in voltage sensitivity of the flip-flop, i.e., a higher amplitude pulse is required for triggering. Finally, the output swing from a nonsaturating circuit is approximately half that from a comparable saturating circuit. Nonetheless, for consistent operation at high speeds this is the best type of circuit that transistors can offer.

Summary. To sum up, the basis of design for the steady-state conditions of the two-transistor flip-flop is the composite N-curve. Various types of coupling circuits may be used to increase the gain of the loop during the switching transients, capacitor coupling being the commonest and cheapest, transformer coupling offering somewhat more sensitivity to the complement trigger. Finally, the choice between saturating and nonsaturating circuitry is based on the relative importance of speed and circuit simplicity (the nonsaturating flip-flop gives about a two to one advantage in speed).

Single-Transistor Circuits

The point-contact transistor offers the unique possibility of designing a two-state circuit with but one transistor. The single-transistor circuits with which we have had the most success are the so-called "current" types described by Williams and Chaplin[1]. The basic

[1] Williams, F.C. and Chaplin, G.B.B.: A Method of Designing Transistor Trigger Circuits; Proc. I.E.E, v.100, n66, Part II, pp.228-248, July, 1953

circuit for such a flip-flop is shown in Fig. 5, along with the simple design equations. This circuit takes advantage of the fact that the transistor in its active state acts very much like a current amplifier and consequently can be designed to switch a current between an external diode and itself. This type of circuitry is very tolerant of transistor parameter variation, and indeed, if the parameters are such as to satisfy the equations, the transistor will work invariably. The equations given apply to design of a saturating-type flip-flop, but a nonsaturating circuit may be designed with the aid of additional clamping diodes.

The obvious economy of this circuit in components, power, and cost gives it great possibilities for computer applications. However, its advantages are not without offsetting difficulties. With but one transistor in the circuit, gates can be tied on at only one point. Thus two different gate circuits are needed if they are to be operative for either state of the flip-flop. Moreover, use of a single transistor imposes all the disadvantages of the nonsaturating flip-flop with none of its advantages (unless a nonsaturating single-transistor flip-flop were used). Specifically the flip-flop is very sensitive to narrow noise pulses when in the "off" state, because there is no saturation to overcome. However, its speed is no better than that of the other saturating types, because hole storage in the "on" state slows up the transient enough to require large coupling condensers (or transformers) which in turn limit the maximum trigger rate. Figure 5, the basic circuit, does not show any provision for complement triggering. In general, the margins on pulse width and amplitude required for successful complementing are not as good in a single-transistor flip-flop as in a two-transistor flip-flop. Nonetheless, with a simple capacitor-coupled steering circuit given by Williams[1] such a flip-flop has been triggered over a range of five to one in both pulse amplitude and pulse width.

Junction Flip-Flops

When I originally undertook to present this paper on high-speed flip-flops, the junction transistors then available did not warrant consideration for such circuitry. However, since then the development in both germanium and silicon junctions has been such that junction flip-flops may be considered for medium-speed applications. I intend, therefore, to describe some of their salient features and capabilities.

The junction flip-flop requires at least two transistors. The proper gain and phase inversion, required for two stable states, is obtained by cross-coupling two grounded-emitter amplifiers. Thus, the basic circuit is similar to the corresponding vacuum-tube circuit. Adding capacitors across the coupling resistors or adding a coupling transformer will serve to increase the loop gain of the circuit during the switching transient. The characteristics of these two types of coupling are similar to those found in point-contact circuits using the same techniques.

Junction flip-flops are invariably operated nonsaturating because of the tremendous hole-storage sensitivity of this type of

transistor. Clamping may or may not be provided to standardize output levels, but the same problems of level variation are present as were found with the point-contact nonsaturating circuits. In general, the fastest of the junctions (among lower priced units) are the silicon n-p-n's which have recently appeared on the market. Following the silicons in order of speed are the grown n-p-n's and the diffused p-n-p's. Because some feeling has existed that there was little promise in point-contact work, there has been great incentive to make high-speed flip-flops with junction transistors. Efforts in this direction have led to circuits similar to vacuum-tube flip-flops which employ cathode followers for cross-coupling. These four-transistor circuits gain about two to one in speed over the two-transistor counterpart. The junction flip-flops may run anywhere from a third to a tenth as fast as the point-contact types. The output swings available from junctions are as great as those from the point-contacts, and the power available is as great or greater. The triggering requirements are similar to those found in point-contact types.

Capabilities of the Various Types of Flip-Flops

In order to present a better idea of the general field of flip-flop performance, I have refrained from giving any quantitative evaluations of the various types up to this point. Now let us consider the actual scope of speeds, output swings and triggering ranges available.

Speed Limits. All saturating types of flip-flops are limited to maximum speeds around 1 megacycle. This applies to well designed circuits employing transistor types which have low hole-storage coefficients. Experience has shown that reaching 1-mc operation requires some selection from production samples of transistors: about 80% of the transistors are acceptable. For computer work or other large systems, circuitry of this type may be relied on to operate atbasic maximum rates of 200 to 500 kilocycles. The waveforms in Figs. 2 and 3 show operation at 500 kilocycles. Nonsaturating circuits using the same transistors will approximately double these limits; they may go even faster, but the waveform begins to deteriorate radically when the pulse-repetition period becomes of the order of the rise and fall times. The waveform shown in Fig. 4 was taken at a pulse-repetition frequency of 3.5 megacycles. However, this was with very high-frequency transistors not now commercially available. Junction flip-flops using p-n-p transistors will operate up to 200 kilocycles with the lower-priced models available from some manufacturers. Use of n-p-n transistors extends this limit to about 300 kilocycles, while silicon n-p-n's will push this speed to 450 kilocycles. With a four-transistor flip-flop using silicon-junction transistors, operation can be obtained at rates as high as 1 megacycle.

Trigger Limits. All of these circuits trigger with pulses in the range of 2 to 30 volts. Generally speaking, circuits which employ steering-circuit triggering are less sensitive but less critical. For instance, with steering diodes a pulse of 15 to 30 volts will trigger the flip-flop at all pulse widths from 0.1 to 2 microseconds while triggering in the emitter with a transformer may be accomplished with pulses from 5

to 20 volts in a range from 0.5 to 1.5 microseconds.

As for the pulse width required, pulses which are too broad or too narrow will fail to trigger any given flip-flop. The lower limit is usually of more concern, because slightly higher speeds may be achieved with narrower pulses. Nonsaturating circuits are best with respect to this criterion; they will trigger easily on a 0.1-usec, 0.5-sine-wave pulse. Most other circuits will not trigger at all on such narrow pulses or else require excessive amplitude. The one exception to this rule is the transformer-coupled saturating type which will trigger on 0.1-usec pulses and is somewhat more sensitive than the capacitor-coupled nonsaturating circuit. The remainder of the saturating circuits require pulse widths in excess of 0.2 microsecond. The upper limit of pulse widths which will trigger a flip-flop depends largely on the storage elements involved in the feedback circuits. Since these elements also affect the speed of the flip-flop there must be some compromise between speed and pulse standardization. Finally, junction transistor flip-flops require pulse widths from 0.2 to 1.0 microsecond. Generally they are subject to the same conditions as have been described for the point contacts but require slightly wider pulses for the same sensitivity.

Output Available. The transistor is essentially a low-power device and as such is more subject to noise interference than vacuum-tube circuitry. In order to rise as far above the noise level as possible, circuits are designed for maximum swings. The swing is limited by the "off" power dissipation in point-contact units and by the reverse breakdown voltage for junction types. These factors limit swings to less than 30 volts in all cases encountered; a more practical value for final design has been found to be about 20 volts. The rise time of the flip-flops is invariably shorter than the fall time, and the fall time may vary from 0.1 microsecond to several microseconds for the slower circuits and transistors. It might be noted that very often, even though high repetition rates will not be encountered in a particular application, it is required that the flip-flop waveform achieve its final value in a short time. This means use of one of the high-speed circuits.

Gates

Before proceeding to the description of a typical application of these flip-flops, it will be well to describe briefly the characteristics of the gates to be used in the system. I have previously explained that the computer involved employs pulse-level gates. In high-speed application, such gates require the following characteristics: they must operate fast; they must isolate the input and output from each other; they must not cause heavy loading on either the pulse source or level source; and they must amplify or regenerate the input pulse. Gates of this description must employ an asymmetric active device, and we have found the transistor to be ideal in that application. Our present circuit is quite simple, and as many as ten gates can be driven from one flip-flop. Moreover, the gate will operate as fast as the flip-flop "sets up." (Further details are beyond the scope of this paper.)

Application for Study

In order to gain insight into the problems involved in the use of transistor circuitry, a small system modeled after an existing section of a vacuum-tube computer was designed and built. The "angular-position counter" and checking circuit (Fig. 6) employ 48 transistors and are designed to provide a tally of positions on the surface of a magnetic-drum memory. They also serve to synchronize the drum with the rest of the computer operation and thus provide a means of reading into, and out of, proper positions on the drum. The basic rate of the counter is 100 kilocycles, at which speed the transistors have little difficulty in performing their jobs. The only use that has been made of junction transistors in this setup is in a pulse amplifier. This amplifier supplies a 20-v pulse to a 200-ohm impedance. There are 11 two-transistor flip-flops in the counter itself, 2 two-transistor flip-flops in the checking circuit, and 1 single-transistor flip-flop in the checking circuit.

This system has been operative for some time, and is revealing to us some of the problems and joys of transistor circuits. The comparative power of the transistor circuit is minuscule: 4 watts as compared with 240 watts for the vacuum-tube system. The size reduction is also impressive. Although the reduction has not yet been carried to its practical limit, the transistor system is about one-tenth of the area of the vacuum-tube system. The cost of constructing computer systemsis very little dependent on the actual price of transistors vs. tubes, so that the transistor circuits are in the same price class as tube circuits even now. Now, for some of the gloomy parts of the picture. Since transistors are small-power devices, power-line noise has become a problem; supplies will require better filtering at high frequencies. Supplying low voltages at relatively high currents and good efficiencies is a problem which is yet to be solved. Finally, the old question of reliability comes up. Generally, the tendency is to blame the device for the failings of the engineer, the major weakness being in the circuitry and associated equipment rather than the transistor. At the time we built this counter the point-contact transistors received were considered relatively good and quite reliable devices. Indeed, one small accumulator incorporating early-model transitors has operated at Lincoln Laboratory for 13,000 hours with only one outright failure. Nonetheless, adverse reports on the economics and reliability of point-contact units have encouraged many manufacturers to leave the field. Our experience with junction transistors shows that they too have had their difficulties, but these are being eliminated with great rapidity. At present some manufacturers are quoting reliability figures for transistors, both point-contact and junction, which are comparable to those usually given for "reliable" tubes.

Signed: Edmund U. Cohler
Edmund U. Cohler

Approved Donald J. Eckl
Donald J. Eckl

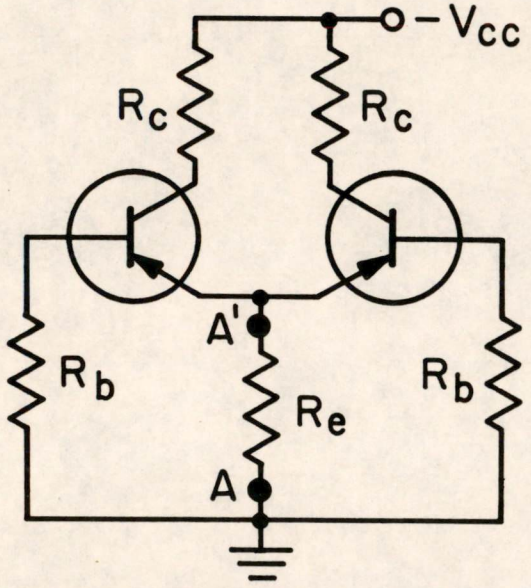
EUC/md

Drawings Attached:

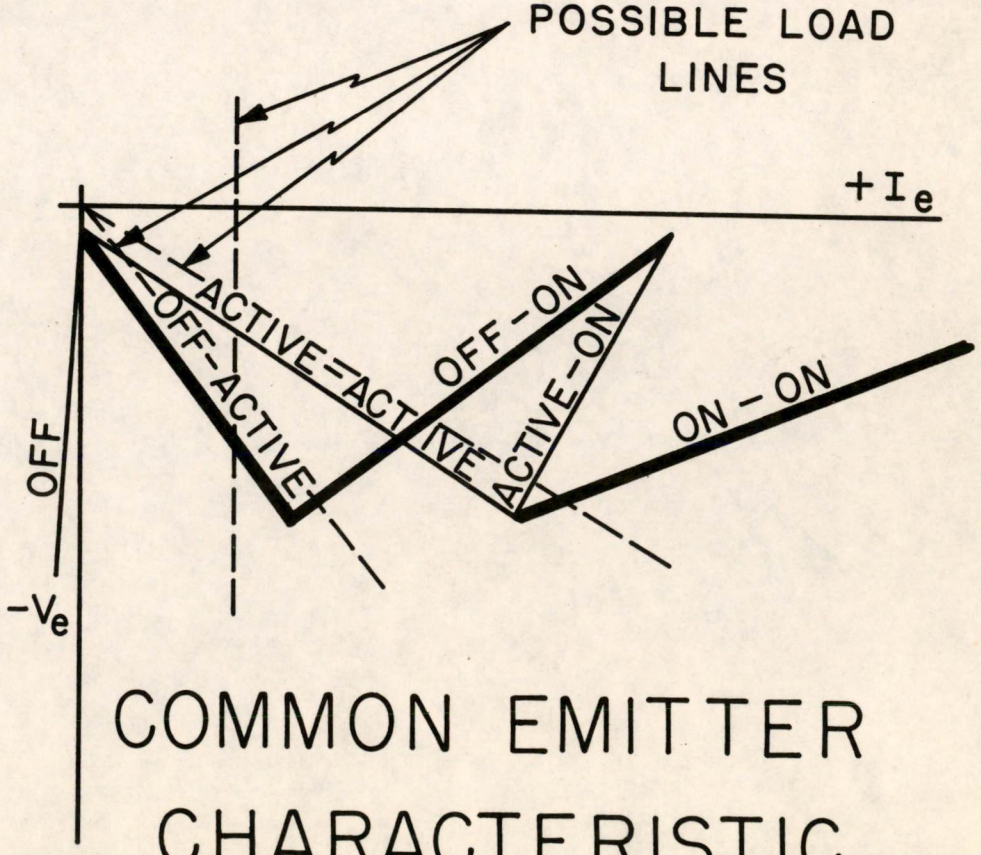
Figure 1 - A59046
Figure 2 - A59049
Figure 3 - A59048
Figure 4 - A59047
Figure 5 - A59050
Figure 6 - A59051

cc: Transistor Section Dist. 2
Staff, Group 63

A-59046
F-2498
SN-811



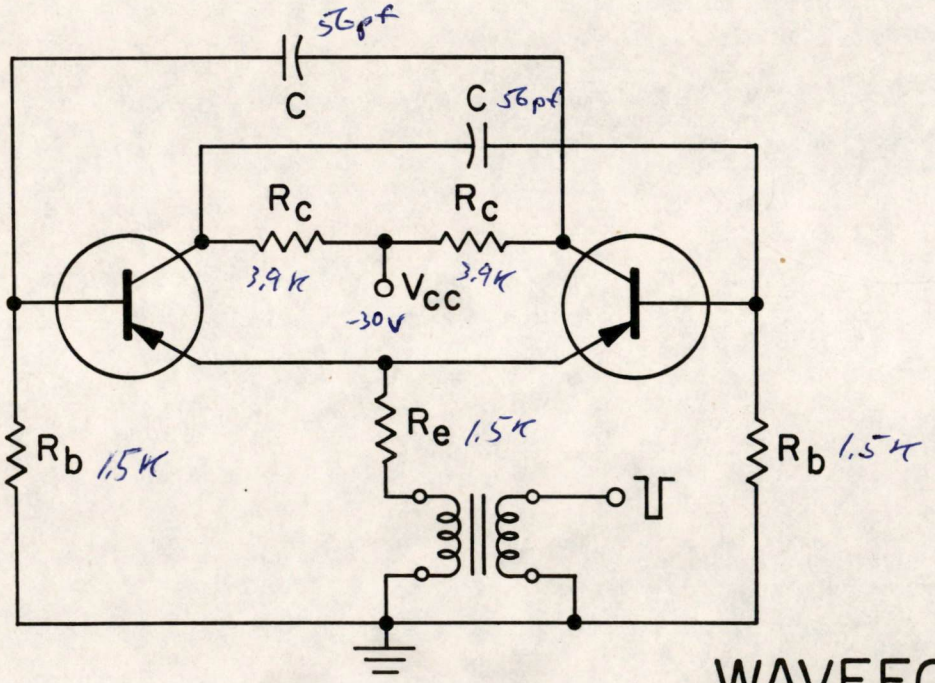
BASIC
FLIP-FLOP



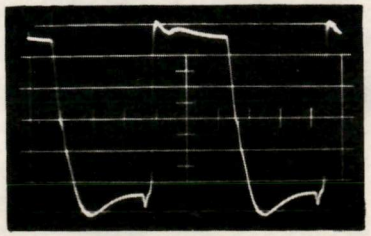
COMMON EMITTER
CHARACTERISTIC

fig 1

A-59049
F-2501
S-814



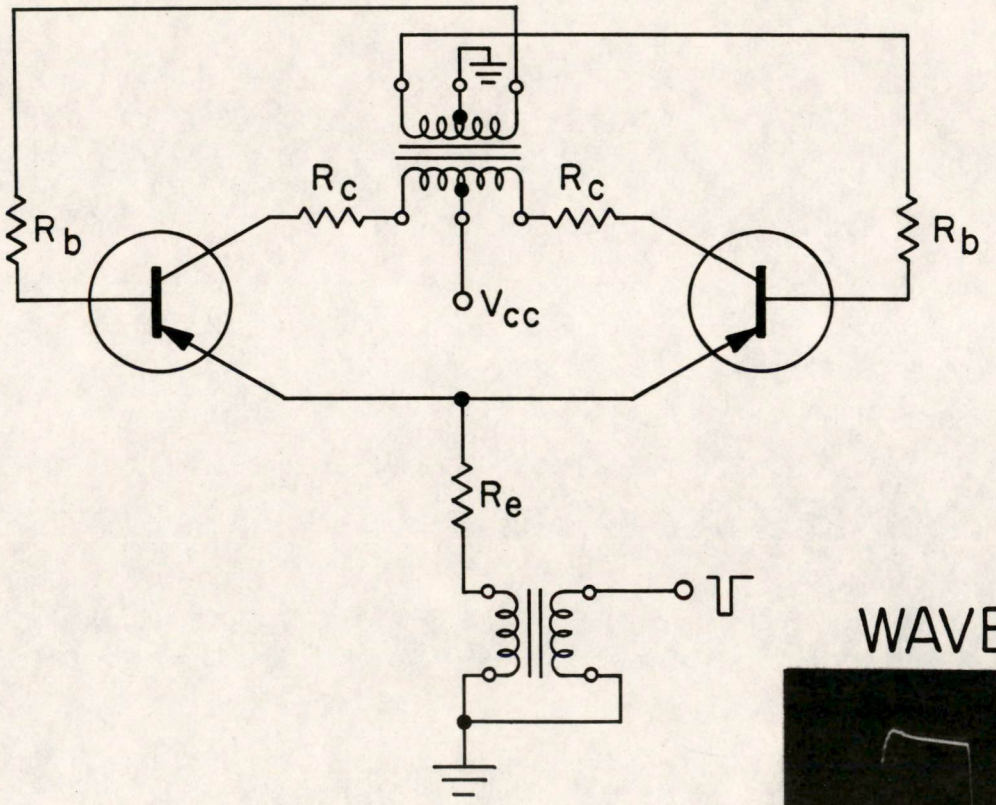
WAVEFORM



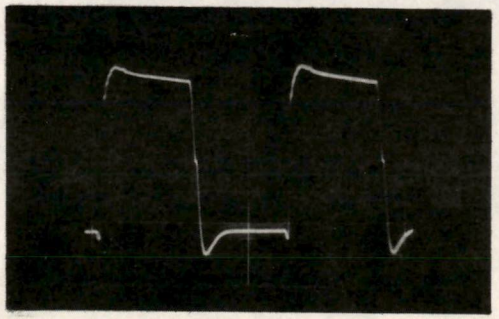
CAPACITOR COUPLED
FLIP-FLOP

fig 2

A-59048
F-2500
S-813



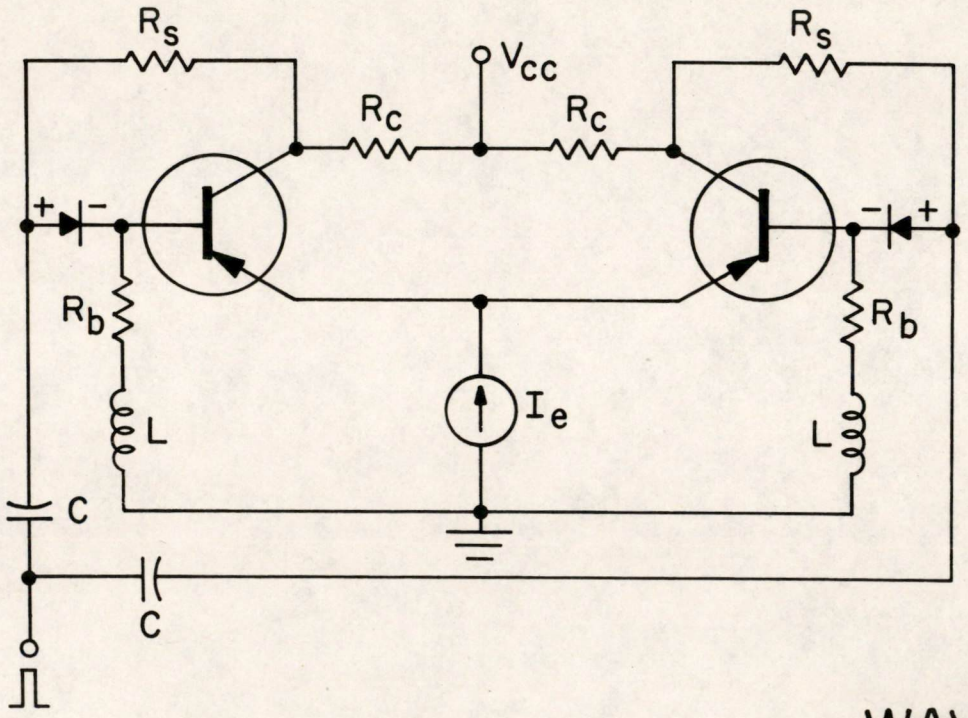
WAVEFORM



TRANSFORMER-COUPLED
FLIP-FLOP

fig 3

A-59047
F-2499
S-812



NON-SATURATING
STEERING-CIRCUIT-
COUPLED FLIP-FLOP

WAVEFORM

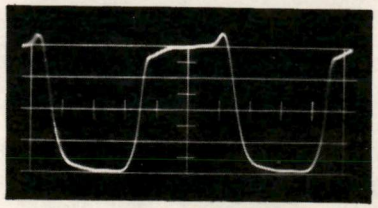
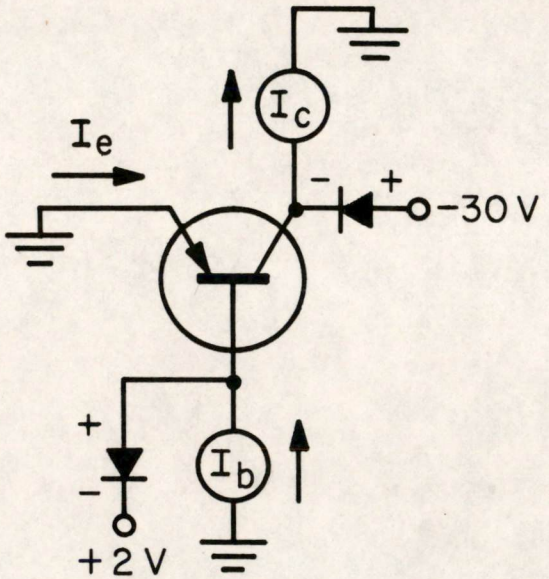


fig 4

A-59050
F-2502
SN-815



$I_e = I_c - I_b$

TO INSURE A SATURATED STATE:

$\alpha I_e \geq I_c$

BASIC SINGLE-TRANSISTOR FLIP-FLOP

fig 5

A-59051
F-2503
SN-816

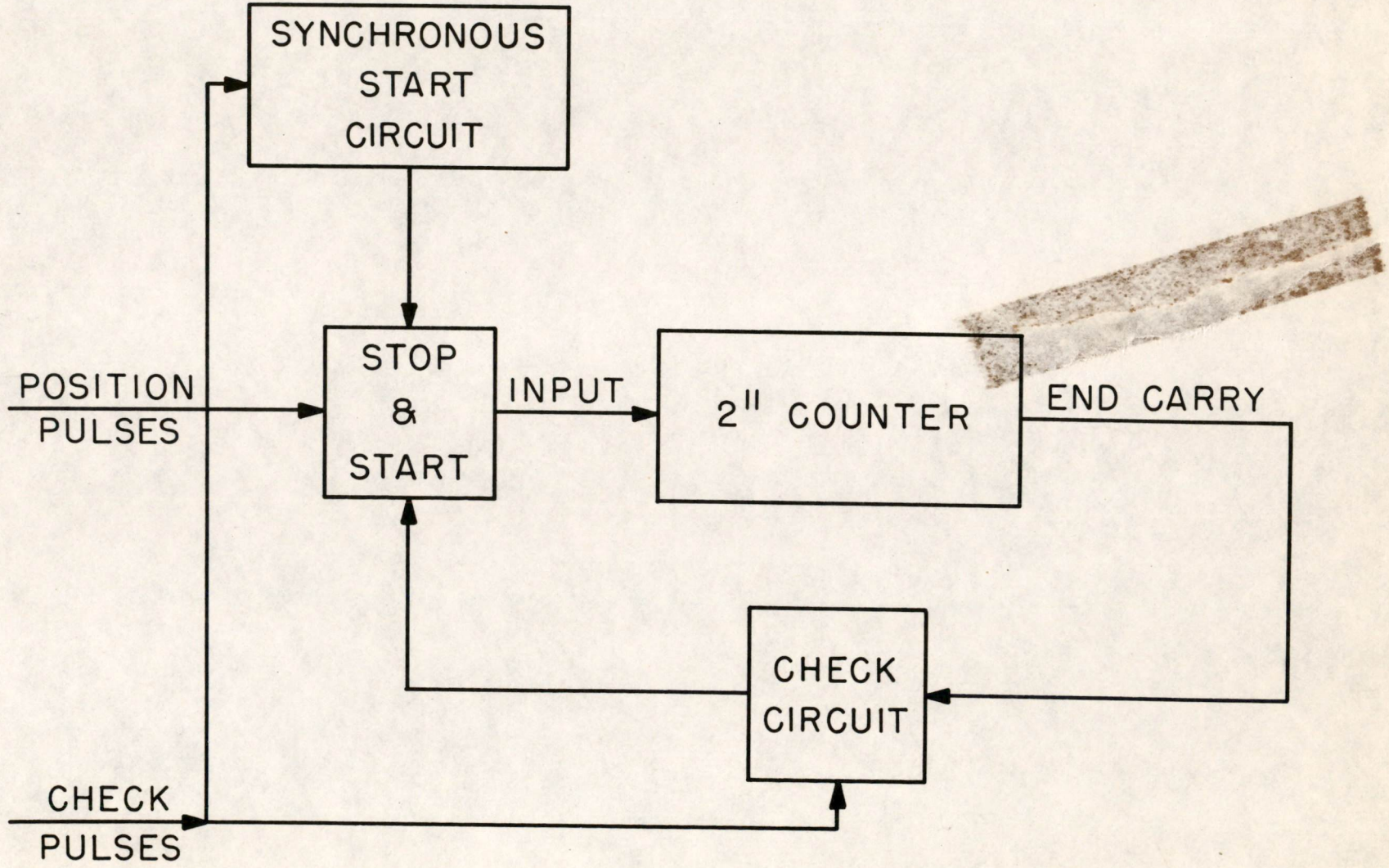


Fig 6

DRUM POSITION DETECTOR

R. Best

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Massachusetts Institute of Technology
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SUBJECT: HIGH-SPEED CORE DRIVER

To: Group 62 Staff; Group 63 Staff

From: S. Bradspies

Date: October 21, 1954

Approved: WNP
W. N. Papian
RLB
R. L. Best

Abstract: A high-speed core driver has been developed. The circuit consists of two pulse amplifiers, a slave flip-flop, a buffer amplifier (which has very rapid rise and fall times), and a current amplifier (Fig. 1). The rise and fall times of the output current pulse are approximately 0.05 microsecond. The current pulse output is negative (as in the Mod V core driver) and its amplitude exceeds 1.5 amps (Fig. 8).

Introduction

A memory system in which the cores are switched by very large currents, and therefore very rapidly, is being developed.[1] Work on this system using the Mod V Core Driver has been frustrating, partially due to the relatively slow rise time of this driver, and mainly because of its extremely slow fall time.* It has been found that the cores switch before the current through them has risen to its final value. The result has been the inability to take any quantitative data on the operation of the memory system. The solution may be a driver capable of rising and falling more rapidly than the Mod V driver does.

Fig. 1 shows a block diagram of the core driver. The first pulse is applied to Pulse Amplifier 1, which has two outputs from its three-winding output transformer - one positive and one negative. This sets the slave flip-flop whose output rises as rapidly as the rise time of the applied pulse. The second pulse applied to Pulse Amplifier 2 clears the flip-flop in the same manner. A trapezoidal wave is applied to a buffer amplifier which has the ability to rise and fall rapidly.

*It is necessary to switch the cores both during the rise and fall of the currents.

[1]Superscripts refer to similarly numbered items in the bibliography.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The low impedance output of the buffer amplifier is used to drive four 6CD6's in parallel. The output is taken from the plates of the 6CD6's and is greater than 1.5 amps in the negative direction; it rises and falls in less than 0.1 microsecond. This current amplifier stage is very much like that found in the Mod V core driver.[2,3]

The outputs of the flip-flop and the buffer amplifier (Figs. 4 and 6) are trapezoidal in order to achieve a rectangular current output. The reason for this situation is the RC combination in the cathodes of the current amplifier tubes (time constant = 0.1 microsecond). If the flip-flop output were rectangular then the current amplifier would have an overshoot (Fig. 9). The RC combination is required to prevent oscillations in the output.

Slave Flip-Flop[4]

The fast operation of the high-speed core driver (Fig. 2) is due to the ability of the slave flip-flop to change states as rapidly as the rise times of the input pulses (for 0.1 microsecond input pulses, the flip-flop can be set in 0.05 microsecond).

In the quiescent condition V2A is on and V2B is off. The output voltage is taken from the plate of V2A, which is normally clamped at -215 volts (in order to hold the current amplifier stage cut off).

The application of a positive 0.1 μsec pulse at input 1 of pulse amplifier 1, results in the application of a positive pulse at point A and a negative pulse at point B (Figs. 1, 2, 3). The diodes, CR4 and V3, pass these pulses and turn V2A off and V2B on rapidly, but only partially. The switching operation finishes slowly by means of the feedback loops. The reason for this peculiar mode of operation has already been explained - - in order to achieve a rectangular current output, the flip-flop output must be trapezoidal.

The waveform at the cathode of V3 (flip-flop output) is shown in Fig. 4 (the d.c. level is -215 volts). The waveform at the plate of CR4 is shown in Fig. 5 (d.c. level is -140 volts). This waveform has a dent in it because the diode's recovery time is not zero (i.e. - some time is required before the crystal diode can switch from the low forward resistance to the high back resistance). A dent such as this could not be tolerated in the output, and so a vacuum diode, V3, rather than a crystal is used. The capacitance from plate and grid to cathode of the 5965 is large compared to that of a germanium diode, however, and this could cause a dent in the output waveform caused by coupling of the pulse's trailing edge (from A) through this capacitance to the output. Two sections in series minimize this effect, and the addition of C15 at their junction helps further to eliminate the dent.

The flip-flop is switched back to its original (steady) state by the application of a positive pulse at input 2 (Figs 3C and D show the pulses at points C and D). In this case, a dent in the output of the flip-flop (Fig. 4) is of no consequence, due to the fact that the current

amplifier stage is well cut off when the flip-flop is down. Thus CR5 may be a germanium rather than a vacuum diode.

The current output is shown in Fig. 8. The amplitude is 1.8 amps and the rise and fall times are each about 0.05 μsec.

The amplitude of the output is controlled by varying the upper clamp voltage of V2A from -150 (maximum output) to -215 (no output). Unfortunately the amplitude control problem is not solved as simply as the above indicates. In order to obtain a rectangular output pulse, the size of the input pulse at point A must be carefully controlled. If the pulse at A is too large, the output appears like Fig. 9; if it is too small, the output is like Fig. 10. The reason for these distorted waveforms follows: The leading edge of the trapezoidal flip-flop output is almost the same height as the pulse at A. The output then approaches the clamp voltage almost linearly. If the slope is too small (pulse at A too large) then the grids of the 6CD6's do not rise as rapidly as their cathodes and, as time progresses, the current output decreases to its steady value (Fig. 9). If the slope is too large (pulse at A too small), then the grids of the 6CD6's rise more rapidly than the cathodes and the current output slowly increases to its final value after the initial jump (Fig. 10). In the ideal case (Fig. 8), the slope of the trapezoid allows the 6CD6 grids to rise just as rapidly as the cathodes rise, resulting in a rectangular output.

Thus, the method of varying the amplitude of the output wave is to observe it and vary both the "amplitude control" (which sets the upper d.c. level of the flip-flop output), and the "input 1 control" (which varies the sizes of the pulses at points A and B).

Fig. 11 shows a 0.1 μsec, 2.1 ampere pulse output from the core driver. This demonstrates the speed with which this circuit operates, for the slave flip-flop has been set and cleared in about 0.1 μsec.

Fig. 12 shows a 1.8 μsec, 1.8 ampere square wave output. This demonstrates the ability of the circuit to hold a fixed output for a relatively long period of time, despite the necessity for using a peculiarly shaped output from the flip-flop.

Buffer Amplifier

The output voltage of the buffer amplifier used in this core driver rises and falls rapidly (Fig. 6). When the flipflop output is down (-215 volts), both the upper and lower tubes (V4) conduct fairly heavily. The plate waveform of the upper tube is shown in Fig. 7.

Upon the application of the rapidly rising edge of the trapezoidal wave to the grid of the upper tube, a large slug of current is drawn, dropping the plate voltage of the upper tube to about -73 volts (Fig. 7); the lower tube is immediately cut off by the feedback arrangement. This means that all the current drawn is used to charge stray wiring capacity and so the cathode follower output rises rapidly. Following this

there is an increase in bias on the upper tube, and a resulting increase in its plate voltage, turning the lower tube on again, but not heavily. Part of the current now drawn continues to charge the capacity (resulting in the steadily increasing voltage of Fig. 6); the rest flows through the lower tube.

When the input to the buffer amplifier suddenly drops, the upper tube tried to go off, but the following circumstances prevent this from happening. The plate voltage of upper tube rises and this results in a large current flowing through the lower tube, whose grid is capacitatively coupled to the plate of the upper tube. This current discharges the wiring capacity, and so the output of the buffer amplifier is forcibly pulled down. The upper tube cannot turn off completely because its cathode falls almost as fast as its grid does.

The remainder of the circuit, the pulse amplifiers[5] and the current amplifier[2,3], present no material that is not well-known, and so no description is given of their operation.

It is to be noted that all waveforms shown were made using a Tektronix 514 oscilloscope in which the input was taken directly to the vertical deflection plates of the scope.

Signed: Sydney Bradspies
S. Bradspies

SB:jd

Attach: D-60687
A-47175
A-60684
A-60685
A-60686

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D-60687

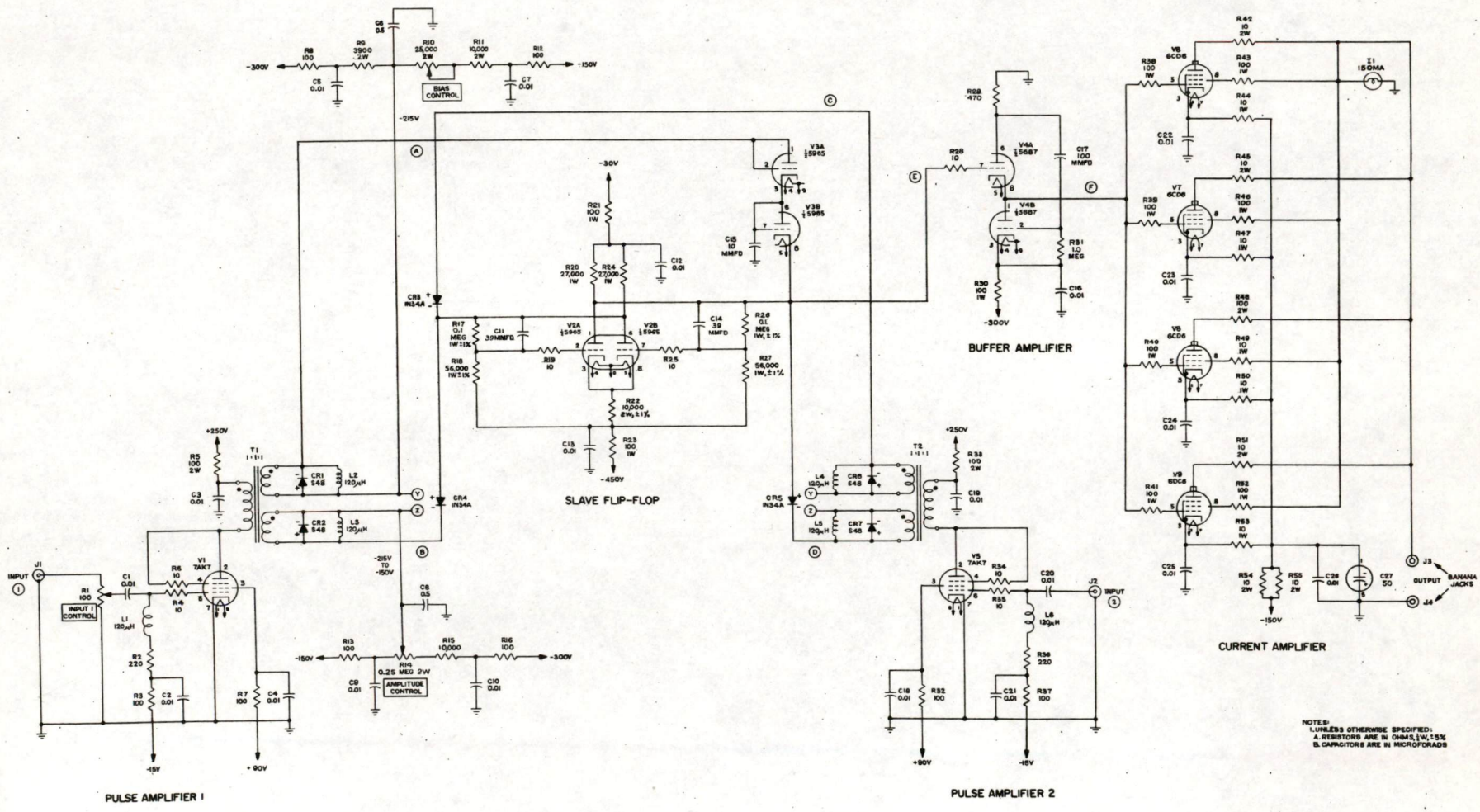


FIG. 2
SCHEMATIC OF HIGH SPEED CORE DRIVER

A-47175

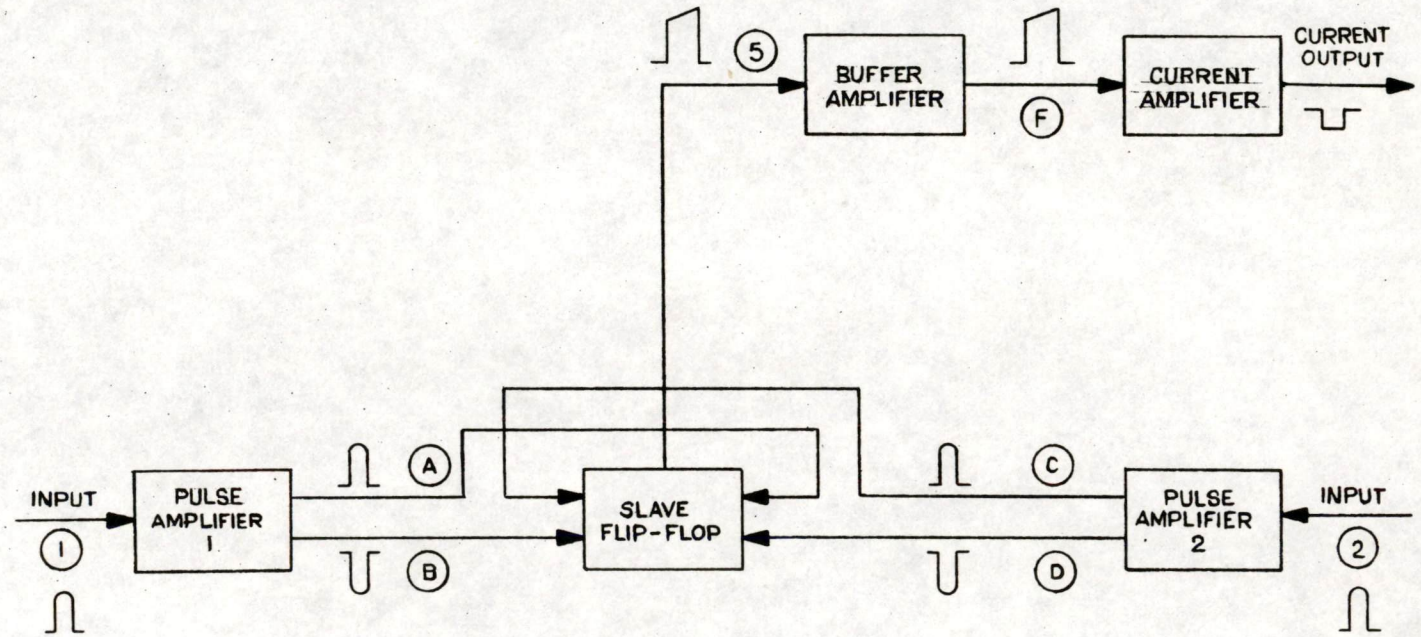


FIG. 1

BLOCK DIAGRAM OF HIGH SPEED CORE DRIVER

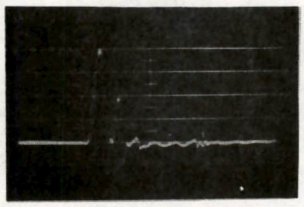


FIG. 3A
VOLTAGE AT POINT A
CORRESPONDING TO FIG. 8

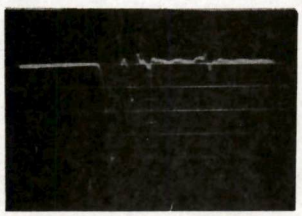


FIG. 3B
VOLTAGE AT POINT B
CORRESPONDING TO FIG. 8

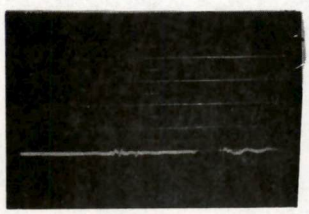


FIG. 3C
VOLTAGE AT POINT C
CORRESPONDING TO FIG. 8

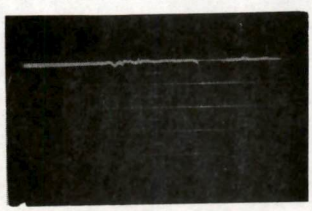
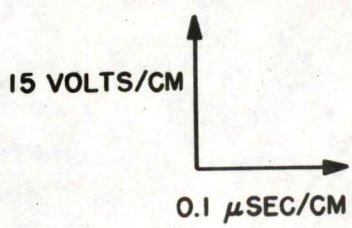


FIG. 3D
VOLTAGE AT POINT D
CORRESPONDING TO FIG. 8



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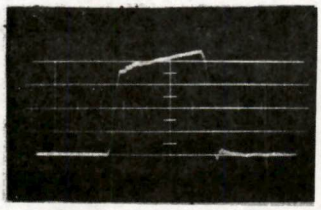


FIG. 4
FLIP-FLOP OUTPUT
(WAVEFORM AT CATHODE OF V3)
CORRESPONDING TO FIG. 8
DC LEVEL=-215 VOLTS

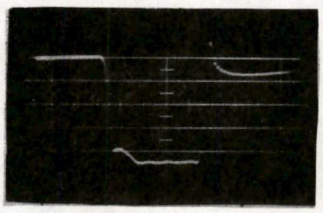


FIG. 5
WAVEFORM AT PLATE OF CR4
CORRESPONDING TO FIG. 8
DC LEVEL=-140 VOLTS

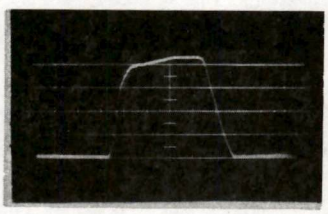


FIG. 6
BUFFER AMPLIFIER OUTPUT
CORRESPONDING TO FIG. 8
DC LEVEL=-210 VOLTS

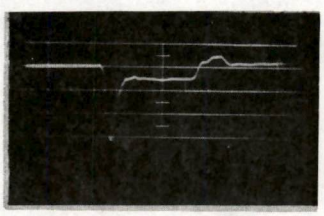
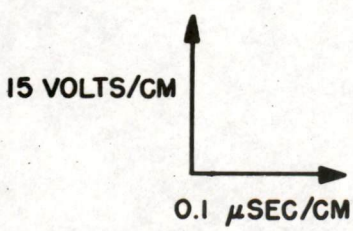


FIG. 7
BUFFER AMPLIFIER PLATE
WAVEFORM
CORRESPONDING TO FIG. 8
DC LEVEL=-27 VOLTS



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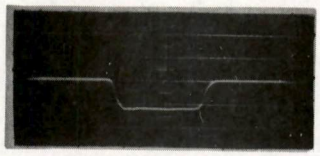


FIG. 8
BEST CORE DRIVER OUTPUT CURRENT (THROUH 10Ω LOAD)

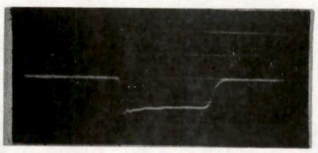


FIG. 9
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO LARGE

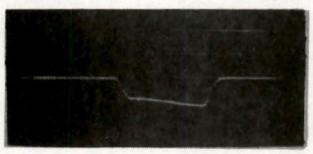


FIG. 10
CORE DRIVER OUTPUT CURRENT (THROUGH 10Ω LOAD) WHEN INPUT PULSE AT 1 IS TOO SMALL

FIG. 11
0.1μSEC CORE DRIVER OUTPUT CURRENT PULSE

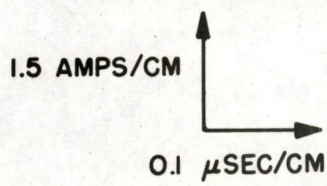
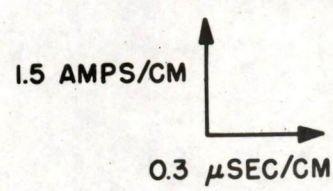


FIG. 12
1.8μ SEC CORE DRIVER OUTPUT PULSE



A-60686

R. Best

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRIGGERING CHARACTERISTICS OF TRANSISTOR FLIP-FLOPS

To: D. R. Brown

From: E. U. Cohler

Date: December 1, 1954

Approval: Torben Meisling
Torben H. Meisling

Abstract: The results of tests made to determine the triggering margins for point-contact and junction transistors are presented herein. Only pulse amplitude vs. pulse width curves were taken for the point-contact transistors, while both those characteristics and pulse amplitude vs. p.r.f. characteristics were investigated for junction transistors. The following conclusions can be stated:

1. Emitter triggering (a complement which depends on storage elements) was more sensitive than steering-circuit triggering. On the other hand, steering-circuit triggering showed less variation of sensitivity with pulse width.

2. Circuits using transformer and capacitor coupling showed speed superiority over capacitor-coupled circuits. Collector-to-emitter type of transformer coupling was fastest.

3. Larger storage elements tend to increase both sensitivity and top speed up to a certain point. Beyond this point the top speed decreases.

4. Ideal trigger pulses are wider for junction transistors than for point contact units due to the lower frequency response of the junctions. The best pulse width for junction circuits is of the order of 0.5μsec.

5. Top speeds for junction circuits with present conventional junction transistors are of the order of 500 kilocycles.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

1. INTRODUCTION

1.1 Scope of Tests

After much work had been done on the best design for a flip-flop circuit it was decided to test the characteristics of different triggering schemes with a variety of flip-flops. The first set of experiments encompassed the pulse amplitude vs pulse width characteristics of several point-contact flip-flops. The trigger source employed generated rectangular pulses whose width and amplitude could be varied. The width-amplitude region in which the pulses succeeded in triggering the circuit was explored and plotted. A parametric family of characteristics was taken for each circuit with the coupling capacity as the parameter.

When the point contact circuits were being tested, there was no high-frequency pulse generator available so that there were no p.r.f. tests on point contact circuits. At a later date these tests were continued on junction flip-flops and data plotted in a similar manner. Moreover the Technitrol pulser was now available and made possible p.r.f. tests on the junction circuits. In examining the p.r.f. characteristics a reasonable pulse width was chosen, and remained fixed throughout the test. The frequency-amplitude region of triggering was then explored and plotted. Because of the wide variety of junction transistors there was some evaluation of the various transistors in these tests, as well as a study of the various circuits and parameters.

1.2 Experimental Procedure

The triggering pulses for the pulse-width vs amplitude tests were obtained from the Hewlett-Packard Pulse Generator (212A). The output was set at some convenient amplitude and the pulse width varied until a triggering failure occurred. This generally happened at two points: a very narrow pulse and a very wide pulse. Failure of triggering was determined by observing the collector wave form and noting the point where the state ceased to change with each trigger. In all but a few cases this was a sharp transition rather than a gradual deterioration of the waveform.

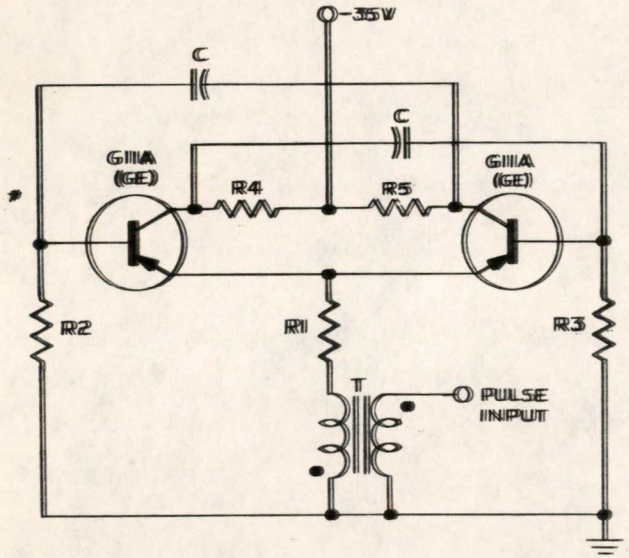
In a few instances it was desired to find the sensitivity of circuits to 0.1 μsec. half-sinewave pulses, and in these tests a Burroughs Clock Pulse Generator was employed in place of the Hewlett-Packard Pulse Generator. The pulse amplitude was varied, and a range of pulse amplitudes found which would trigger the flip-flop.

2. POINT-CONTACT CIRCUITS

2.1 Two-Transistor, Capacitor-Coupled, Emitter-Triggered Flip-Flop

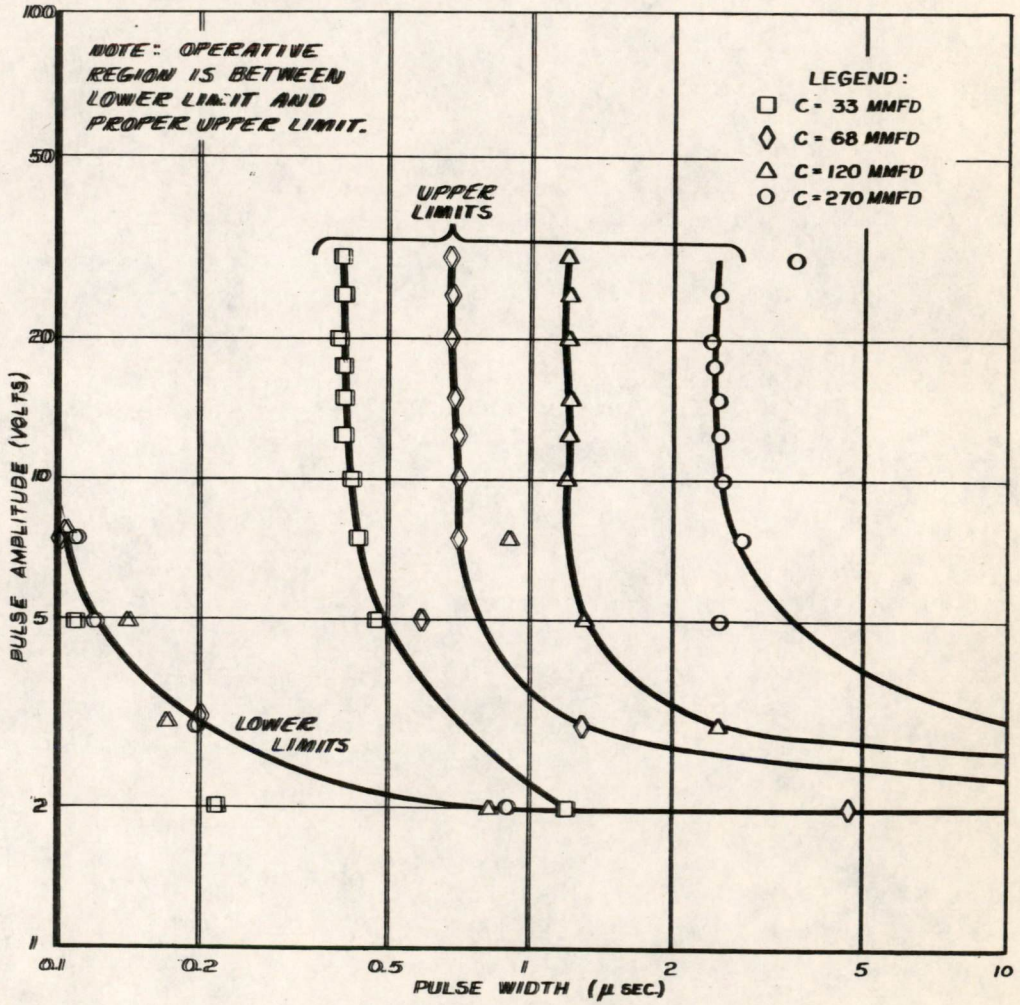
The circuit described in E-557[1] was tested first. In Figure 1 are shown both the circuit diagram and the results of the width-amplitude tests. The transistors used in the circuit were General Electric G11A's. In order to obtain truly comparable results between the various circuits

1. E-557 The Design of a Two-Transistor Saturating Flip-flop, E. U. Cohler, 7-9-53.



T = 50:50 TURNS ON A F262 FERRAMIC-H CORE.
R1, R2, R3 = 1500 Ω
R4, R5 = 3900 Ω
C = SEE TEXT AND ACCOMPANYING GRAPH.

a) CIRCUIT SCHEMATIC



b) PULSE AMPLITUDE vs. PULSE WIDTH FOR VARIOUS COUPLING CAPACITIES.

FIG. 1

THE TWO-TRANSISTOR, CAPACITOR-COUPLED, EMITTER-TRIGGERED SATURATING FLIP-FLOP

we used these same transistors wherever possible. The parameter on the various curves was the coupling capacity. We may infer from these results that:

1. The voltage required to trigger at successively lower widths increases rapidly beyond a certain point. The boundary of operation on the narrow side is little dependent on the coupling capacity, and largely a function of the transistor gain-band width characteristics.

2. There is a maximum pulse width beyond which the circuit becomes inoperative. This width goes down as the voltage is increased, and eventually reaches a minimum which is directly proportional to the coupling capacity. This results from the nature of the triggering cycle which requires that the trigger remit before the circuit equilibrates.[2]

2.2 Other Two-Transistor-Flip-flop Triggering Schemes

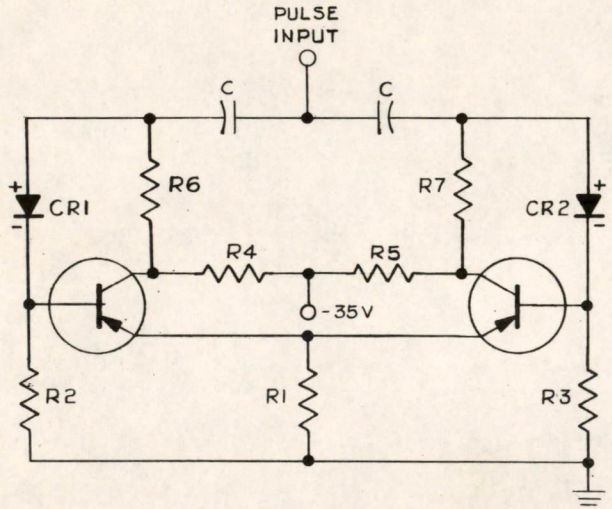
Successively, other triggering schemes were tried, and the results plotted in Figures 2 and 3. Both of these triggering methods were less sensitive than emitter triggering except with very narrow pulses. Consequently, the upper limit on pulse amplitude was not in the range explored. This decrease in sensitivity is due largely to the loss in amplitude which the pulse suffers in passing through the diode steering gates. As can be seen from these curves it is characteristic of steering-circuit triggering that the sole effect of increased capacity in the steering circuit is increased sensitivity.

2.3 Non-saturating Flip-Flop

All of the preceding types of flip-flops had involved the same basic circuit, i.e. the two-transistor saturating flip-flop. The next test was concerned with a different flip-flop developed by Carlson at AFCRC. This circuit was a two-transistor non-saturating type which included a steering circuit for triggering. Emitter triggering was not attempted because the high resistance in the emitter circuit would have dissipated most of the trigger energy. The results of the tests on this flip-flop are plotted in Figure 4, and reveal a basic similarity to the characteristics of the other steering-circuit flip-flops, i.e. sensitivity is dependent on the capacity in the coupling circuit. However, the circuit itself is much more sensitive than saturating flip-flops using similar triggering circuitry. This increase in sensitivity is especially noticeable with narrow pulses. In Figure 5 the sensitivity of the flip-flops of Figs. 3 and 4 have been compared for various values of C_c using 0.1 μsec. half-sinewave pulses.

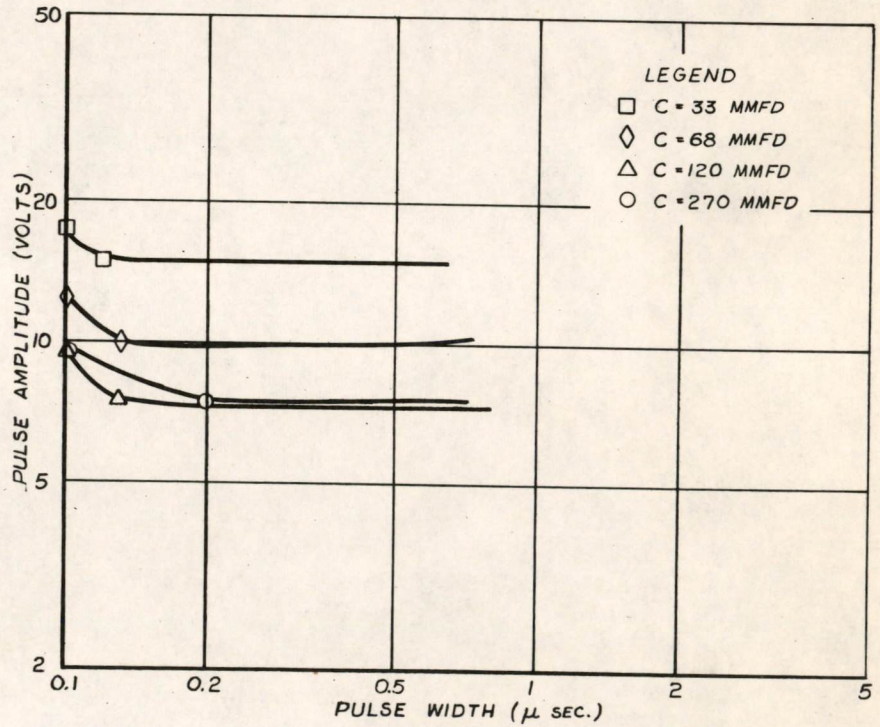
---

2. E-556, A Study of a Two-Transistor Flip-flop, p. 13 discusses this action briefly. However, it ignores the effects of wide pulses which require the trigger amplitude to be less than some upper limit. It can be seen from Fig. 1 that for narrow pulses there is no upper limit on amplitude.



R1, R2, R3 = 1500 Ω
R4, R5 = 3900 Ω
R6, R7 = 10,000 Ω
C = SEE TEXT AND ACCOMPANYING GRAPH
CR1, CR2 = IN34A

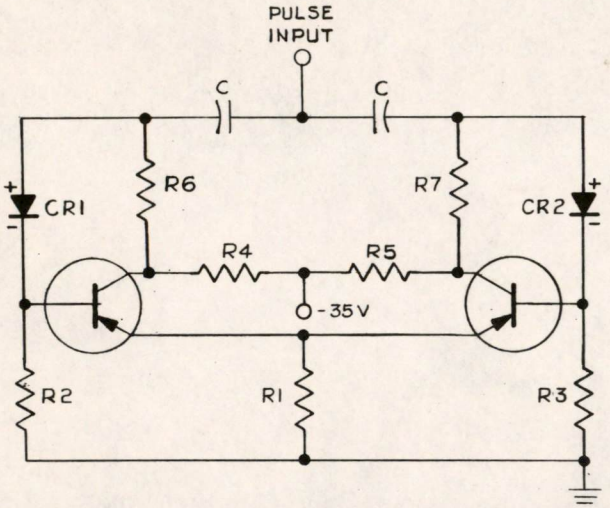
a) CIRCUIT SCHEMATIC



b) PULSE AMPLITUDE vs. PULSE WIDTH FOR VARIOUS COUPLING CAPACITIES

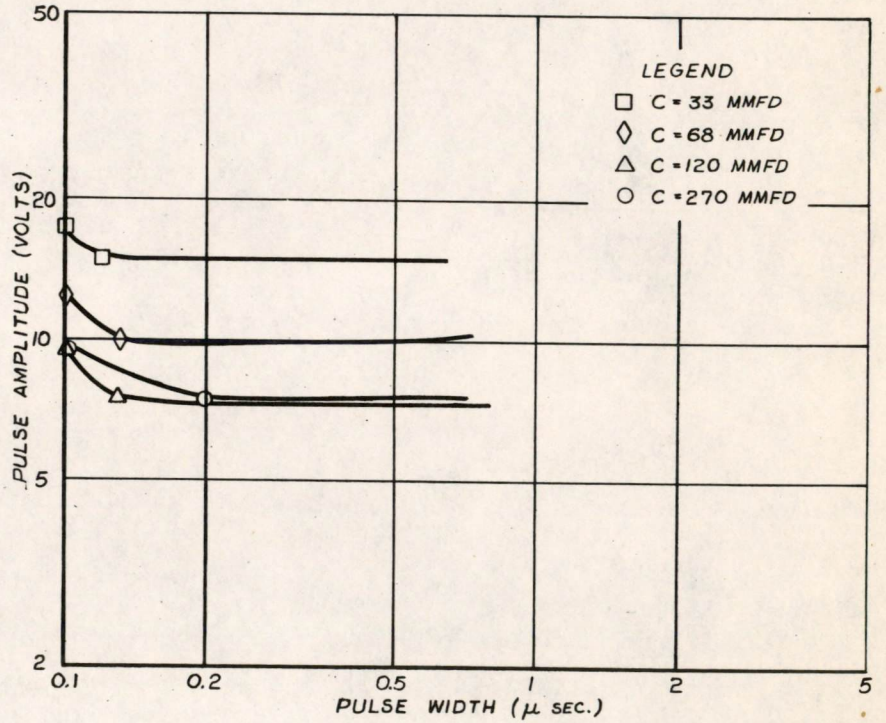
FIG. 3

THE TWO-TRANSISTOR, CAPACITOR-COUPLED, BASE-TRIGGERED, SATURATING FLIP-FLOP



R1, R2, R3 = 1500 Ω
R4, R5 = 3900 Ω
R6, R7 = 10,000 Ω
C = SEE TEXT AND ACCOMPANYING GRAPH
CR1, CR2 = IN34A

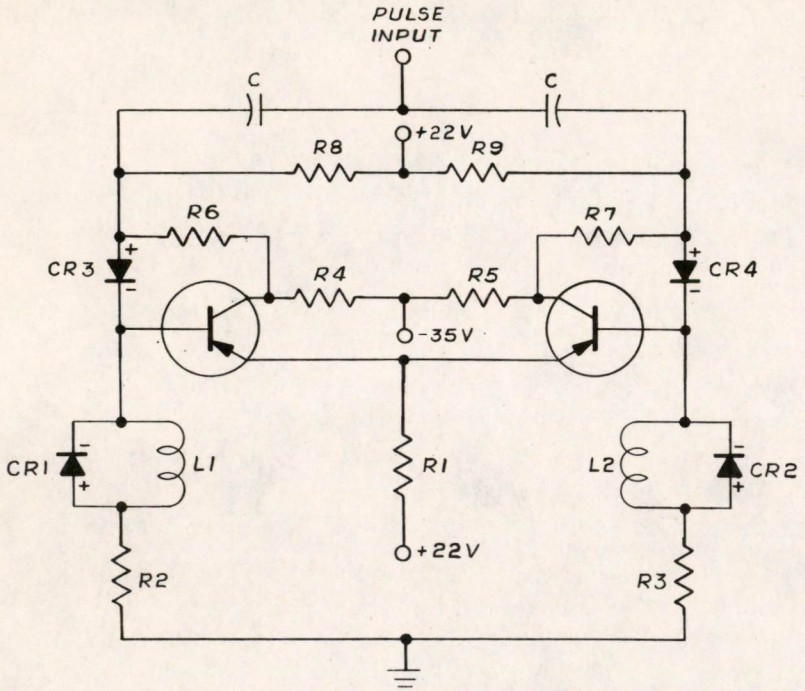
a) CIRCUIT SCHEMATIC



b) PULSE AMPLITUDE vs. PULSE WIDTH FOR VARIOUS COUPLING CAPACITIES

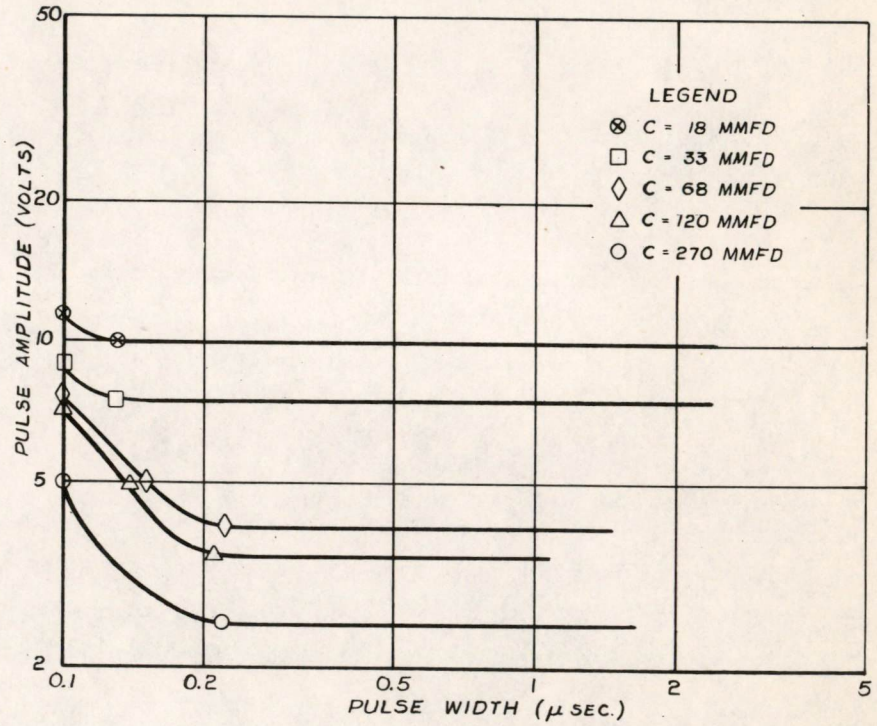
FIG. 3

THE TWO-TRANSISTOR, CAPACITOR-COUPLED, BASE-TRIGGERED, SATURATING FLIP-FLOP



R1 = 10,000 Ω
R2, R3 = 470 Ω
R4, R5 = 2200 Ω
R6, R7 = 5600 Ω
R8, R9 = 12,000 Ω
L1, L2 = 100 μH
C = SEE TEXT AND ACCOMPANYING GRAPH
CR1, CR2, CR3, CR4 = 1N34A

a) CIRCUIT SCHEMATIC



b) PULSE AMPLITUDE vs. PULSE WIDTH FOR VARIOUS COUPLING CAPACITORS

FIG. 4

THE TWO-TRANSISTOR, CAPACITY-COUPLED, BASE-TRIGGERED, NONSATURATING FLIP-FLOP

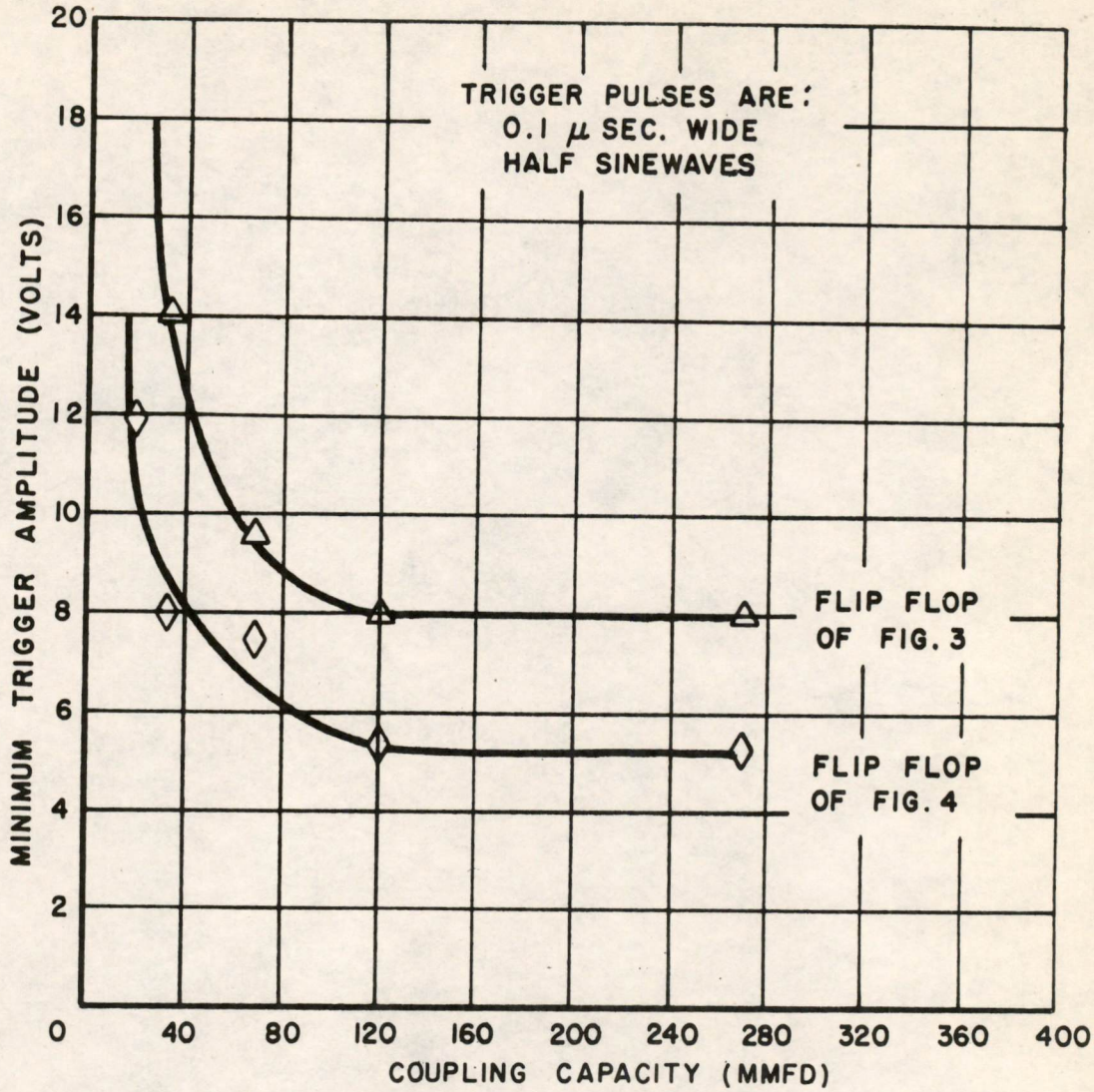


FIG. 5

FLIP-FLOP SENSITIVITY CURVES

A-60439

2.4 Single Transistor Flip-flop

The only single transistor flip-flop on which extensive tests were done is that shown in Figure 6. This particular circuit was propounded by Williams and Chaplin[3] and was considered to be one of the best performers among the single-transistor types. It can be seen from the pulse width vs pulse amplitude tests (Fig. 6b) that the region of operation is not as great for this type of flip-flop as for the two-transistor types. In fact, the curves close on themselves to form closed regions of operation. Successively larger capacities cause successively larger regions of operation and all regions are concentric. It would seem then that the ideal capacity would be the largest possible; however, experience tells us that increasing the capacity will eventually lead to lower maximum p.r.f.'s and diminishing returns in pulse range. Using 0.5 μsec pulses operation was achieved up to at least 670 kc at all capacities. It was not possible to find an upper frequency bound because of lack of equipment to give pulses at high frequencies.

3. Junction Flip-Flops

3.1 Two-transistor Capacitor-Coupled Flip-Flop

The flip-flop shown in Fig. 7 is the simplest of the junction transistor flip-flops. It is a reasonably sensitive flip-flop when triggered in the emitter as shown, but the triggering is rather critical (see Fig. 8). Characteristics were taken only with the parameters shown and it is seen that the top frequency of this circuit is about 200 kc. The pulse amplitude vs pulse width curve is similar to that obtained for a two-transistor point contact circuit with the emitter type of triggering (see Fig. 1).

3.2 Two-transistor Transformer-Coupled Flip-flop

3.21 Collector-Base Coupled

The simple transformer-coupled flip-flop shown in Fig. 9 is somewhat more sensitive and faster than the corresponding capacitor-coupled typed. Some capacitive coupling is used, in addition to the coupling transformer, as a sort of "speed-up" capacity. The effect of the transformer is threefold: It acts as a self-coupling transformer which gives auto-regeneration in each transistor; it provides extra gain in the loop which speeds the switching; and it acts as an inductive compensation for the "rise" of the collector. It should be noted that in this circuit the coupling path is the same for the d-c and transient parts of the feedback, i.e. collector to base.

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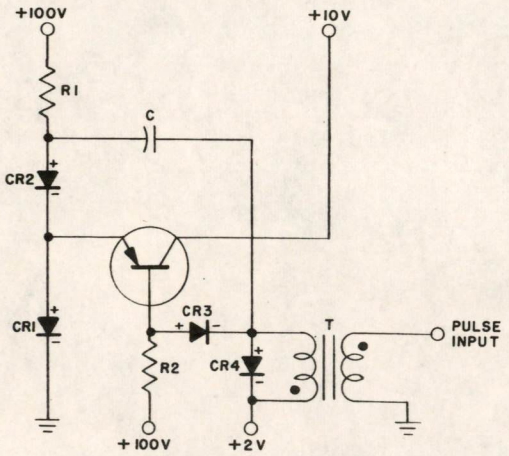
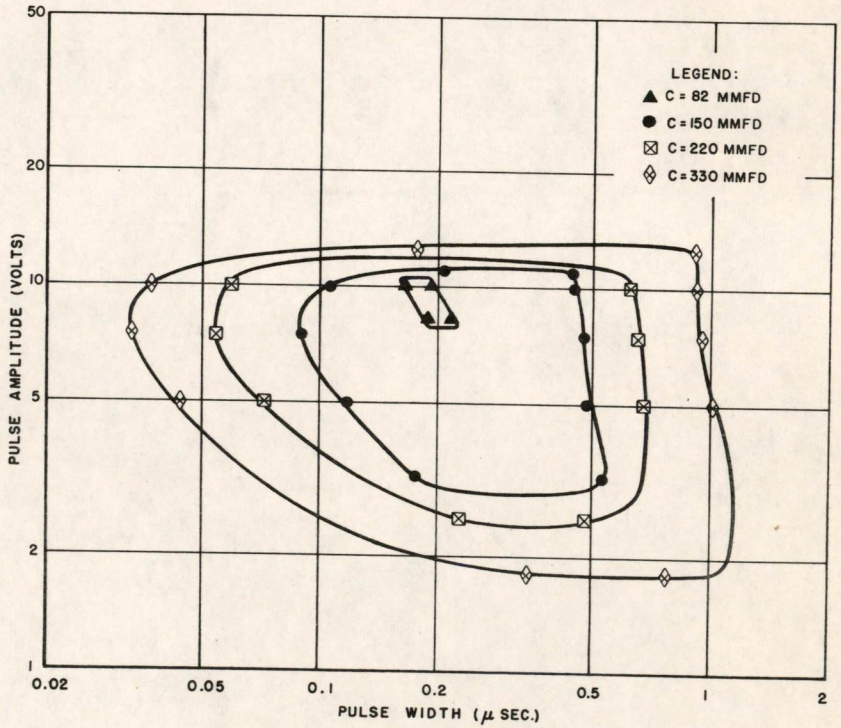
3. Williams, F.C. and Chaplin, G.B.B: A Method of Designing Transistor Circuits. Proc. I.E.E., Vol. 100, No. 63, Pt.III, p.228, July, 1953



T = 50:50 TURNS ON A F262 FERRAMIC-H CORE
R1 = 33,000 Ω
R2 = 47,000 Ω
C = SEE TEXT AND ACCOMPANYING GRAPH
CR1, CR2, CR3, CR4 = IN34A

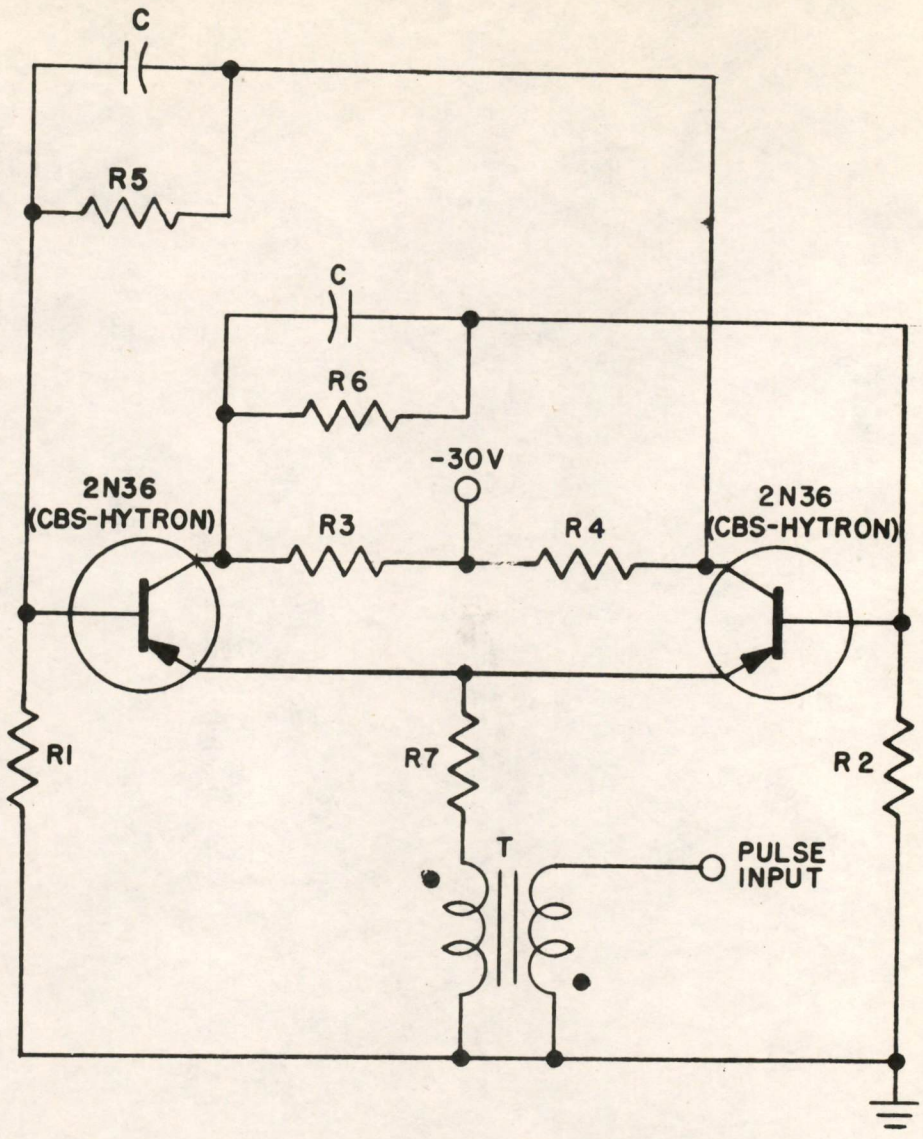
a/ CIRCUIT SCHEMATIC



b/ PULSE AMPLITUDE vs. PULSE WIDTH FOR VARIOUS COUPLING CAPACITIES

FIG. 6

SINGLE-TRANSISTOR, SATURATING FLIP-FLOP



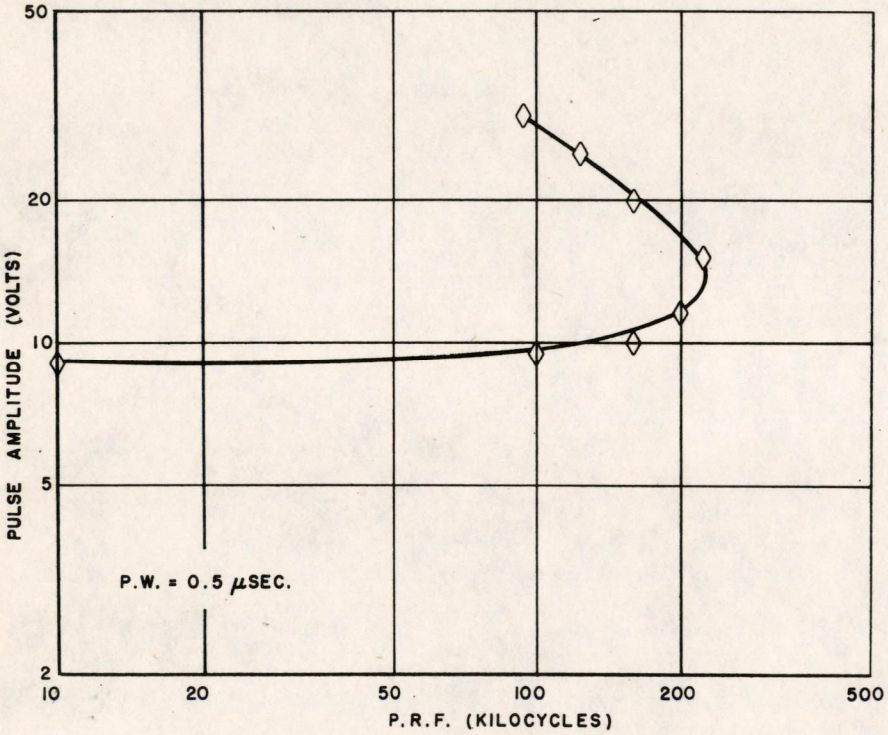
T = 50:50 TURNS ON A F262 FERRAMIC-H CORE
RI, R2, R3, R4 = 3300 Ω
R5, R6 = 18,000 Ω
R7 = 470 Ω
C = 100 MMFD.

FIG. 7

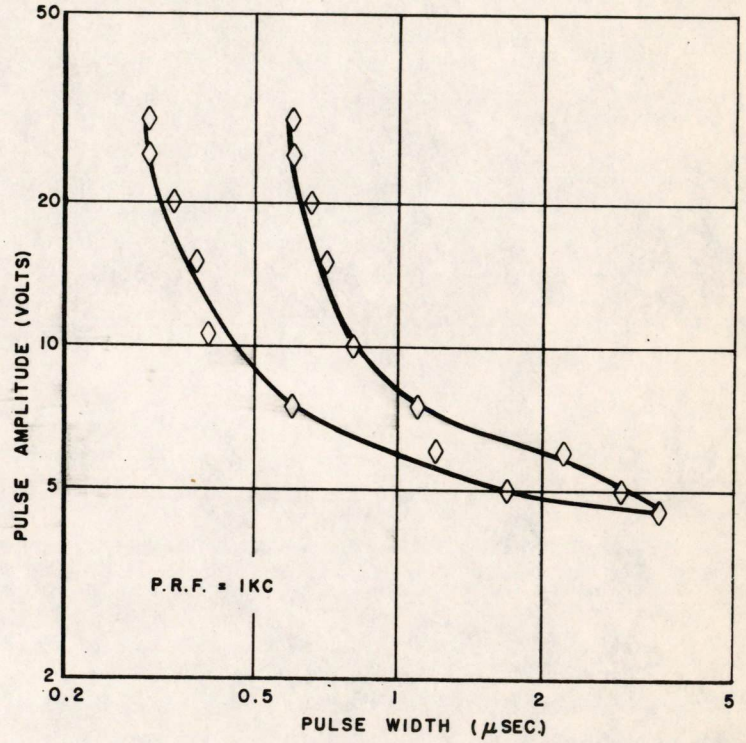
CIRCUIT SCHEMATIC,

TWO-TRANSISTOR, CAPACITOR-COUPLED JUNCTION FLIP-FLOP

A-60441



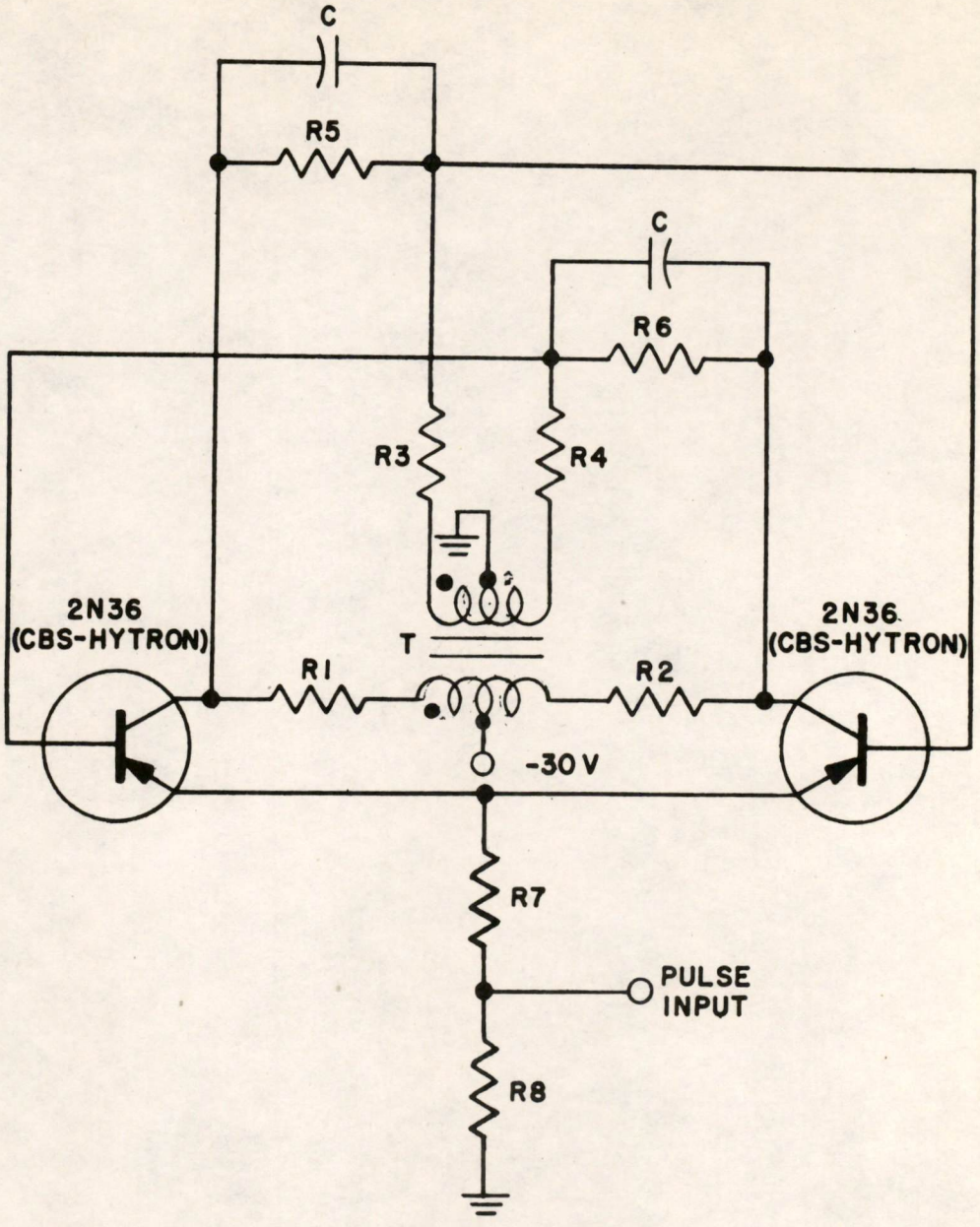
b) P.R.F. CHARACTERISTICS



a) PULSE AMPLITUDE vs. PULSE WIDTH

FIG. 8

TRIGGERING CHARACTERISTICS OF TWO-TRANSISTOR, CAPACITOR-COUPLED JUNCTION FLIP-FLOP



T= SEE TEXT AND SUCCEEDING GRAPHS.
R1, R2, R3, R4 = 3,300 Ω
R5, R6 = 18,000 Ω
R7= 390 Ω
R8= 91 Ω
C= SEE TEXT AND FIG. 10.

CIRCUIT SCHEMATIC

FIG. 9

TWO-TRANSISTOR, TRANSFORMER-COUPLED JUNCTION FLIP-FLOP

A-60443

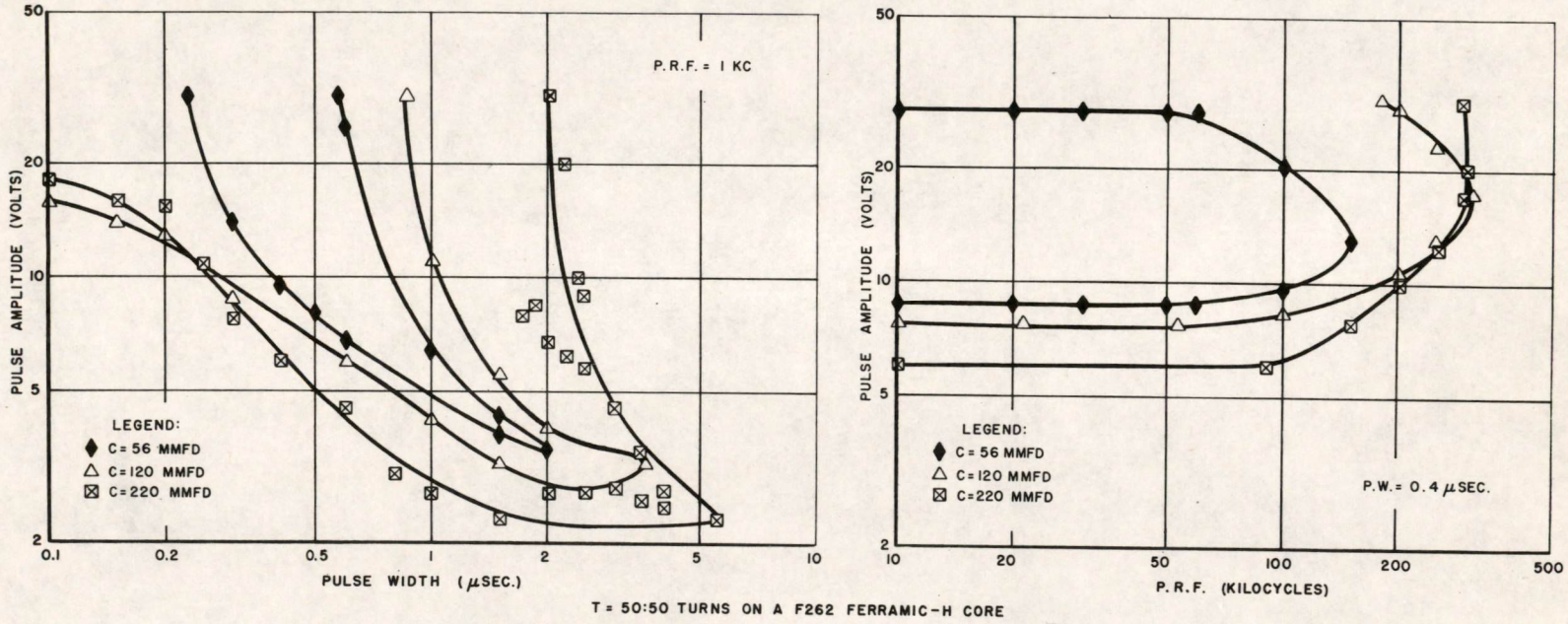
Figure 10 gives a summary of the characteristics of this flip-flop when a coupling transformer is employed with four windings of 25 turns each on a F262 Ferramic H core. This transformer has a total inductance, primary or secondary, of about 600 microhenries. It can be seen that both the p.r.f. and pulse width characteristics are very good for the larger capacities. The pulse width curves are quite characteristic of an emitter triggered circuit. The sensitivity exceeds that of the simple capacity-coupled flip-flop and the top speed is about 50 percent higher with the same transistors.

It was thought that some enhancement of the sensitivity might be obtained by using a larger transformer in the coupling circuit. This was done with a transformer employing four 35-turn windings on a double F262 Ferramic H core, but the results showed little or no gain from the original transformer. We then tried a step-down transformer with two 46-turn windings and two 23-turn windings and succeeded this transformer with a four-winding 18:18 (per half) turn transformer. In each case the results were not much different from the first set.

Using this last transformer, it was decided to compare transistor types in this circuit. The results of the first set of tests on a pair of n-p-n grown junction transistors (Texas Instruments' 202) indicated that the flip-flop performance was about the same as it was with the p-n-p's.... perhaps a little faster. However, the n-p-n silicon transistors of Texas Instruments (901) operated considerably faster and with rather unusual triggering characteristics. These results are shown in Figure 11. It will be noted that these transistors were much more sensitive in this circuit, and much faster. Both the sensitivity and top speed have been increased about twofold. This increase is accompanied, however, by a narrower range of operation in both pulse width and amplitude.

3.22 Collector-Emitter Coupled

It was felt that the major limitation on the speed of the collector-base coupled circuit was the low frequency response of the transistors in the grounded-emitter connection. While the grounded-emitter connection is necessary for the steady-state feedback, it is not at all necessary for the switching-transient coupling. Thus it was decided that the use of a step-down transformer which coupled from collector to emitter would give the effect of a grounded-base amplifier as far as frequency response is concerned while still giving the extra gain required for switching. The transformer which we tried first was 50:25 turns per half on an F262 Ferramic H. core. The circuit employed is shown in Figure 12 while the results of the first set of tests are set forth in Figure 13. The transistors used in these tests were the same p-n-p's as those employed for previous tests so that results can be compared directly. It can be seen on contrasting Figures 13 and 10 that the collector-emitter coupled circuit is comparable in sensitivity and triggering range to the collector-base coupled type while the frequency characteristics are much improved. This circuit was also tested with silicon junction transistors and found to operate considerably faster.

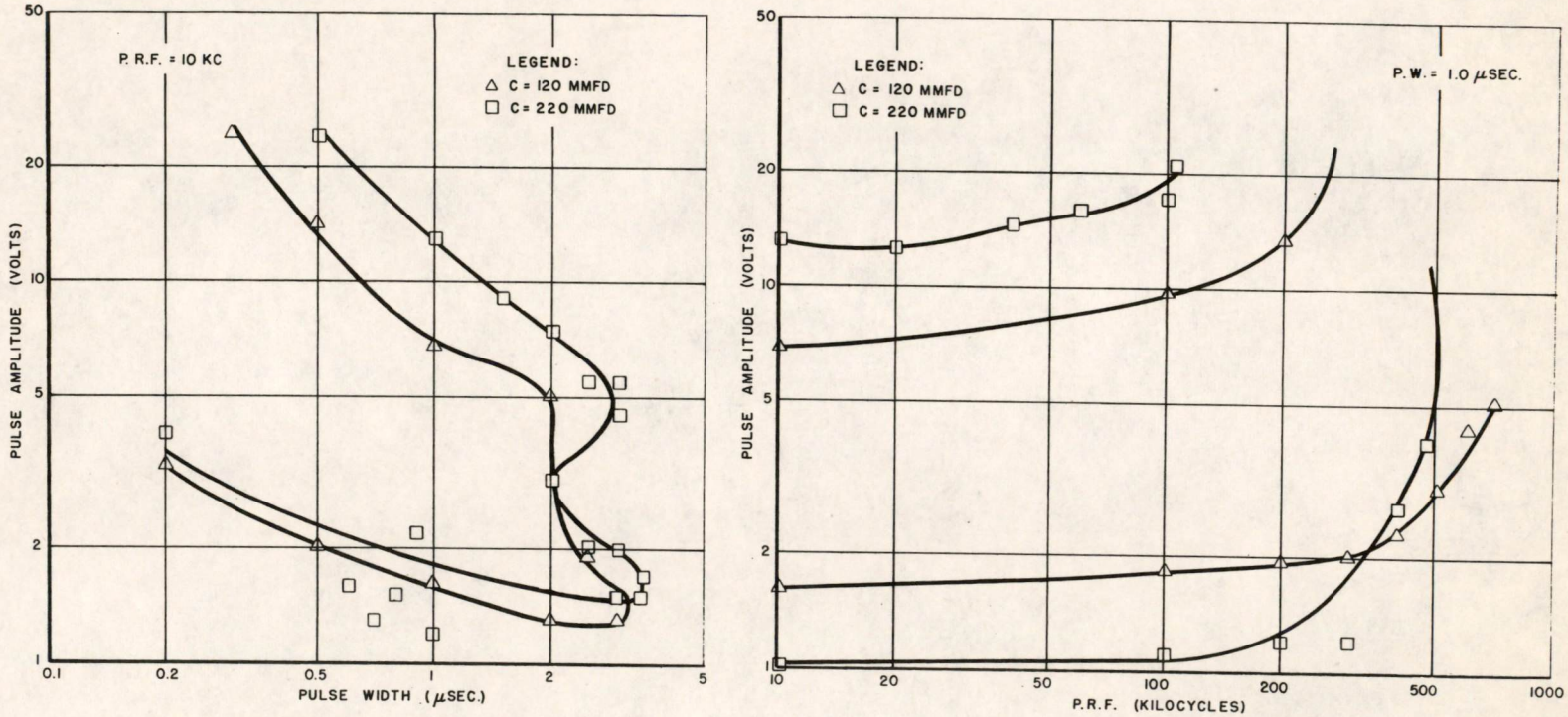


a/ PULSE WIDTH CHARACTERISTICS OF TRANSFORMER-COUPLED JUNCTION FLIP-FLOP

b/ P.R.F. CHARACTERISTICS OF TRANSFORMER-COUPLED JUNCTION FLIP-FLOP

FIG. 10

TRIGGERING CHARACTERISTICS OF TRANSFORMER-COUPLED JUNCTION FLIP-FLOP OF FIG. 9



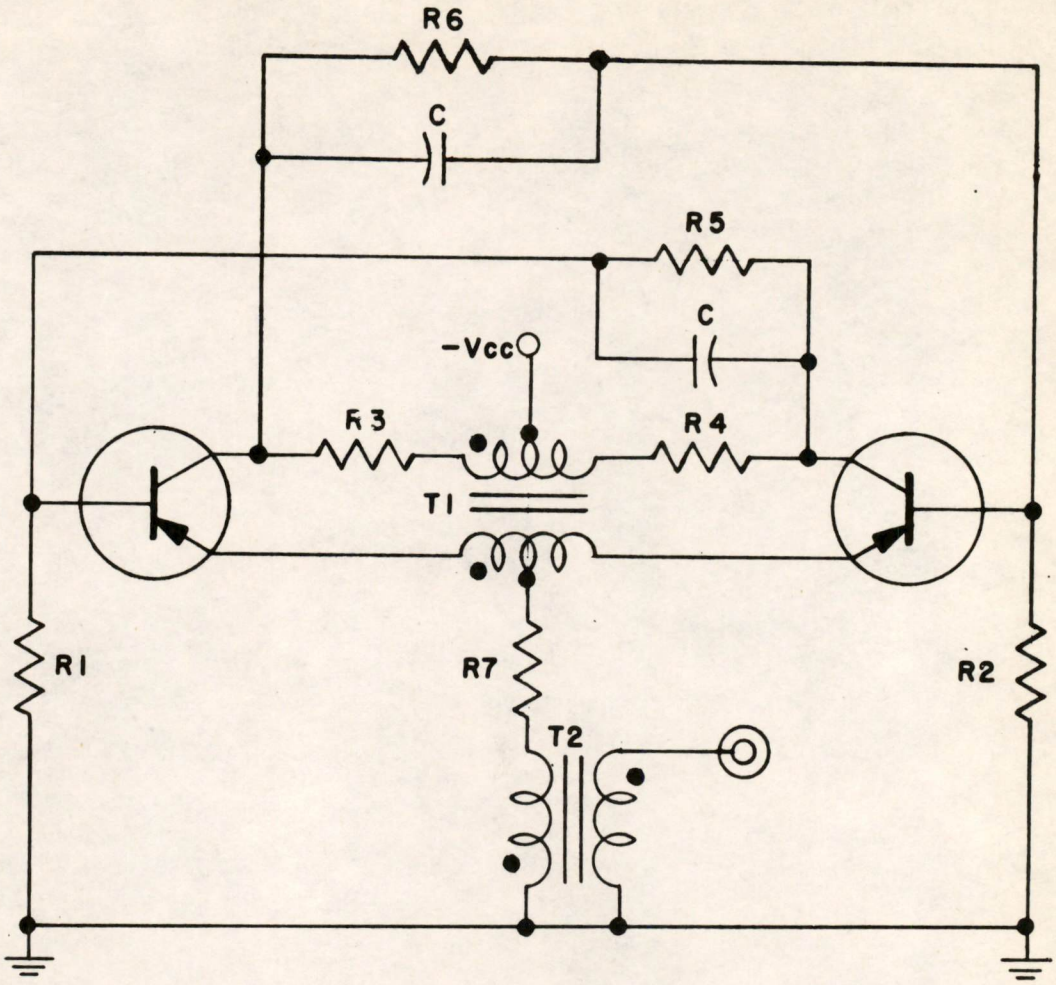
a/ PULSE AMPLITUDE vs. PULSE WIDTH

b/ PULSE AMPLITUDE vs. P.R.F.

TRANSISTORS: T. I. 901's.
TRANSFORMER: 18:18 TURNS / HALF ON A F262 FERRAMIC-H CORE

FIG. 11

A TRANSFORMER-COUPLED JUNCTION FLIP-FLOP USING SILICON N-P-N JUNCTION TRANSISTORS



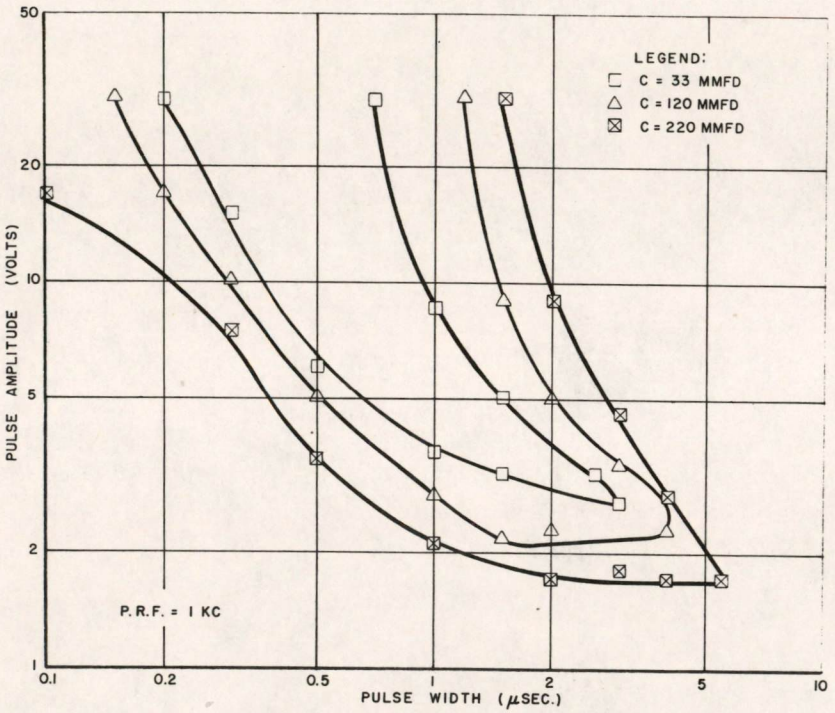
T1 = 50:25 TURNS / HALF ON A F262 FERRAMIC-H CORE
T2 = 50:50 TURNS TOTAL ON A F262 FERRAMIC-H CORE
R1, R2, R3, R4 = 3300 Ω
R5, R6 = 18,000 Ω
R7 = 470 Ω
C = SEE TEXT AND FIG. 13.

FIG. 12

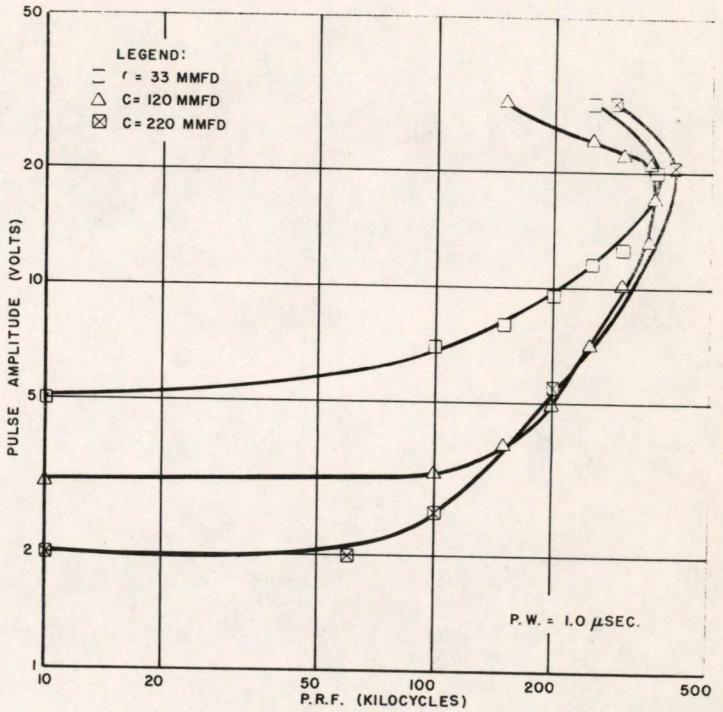
CIRCUIT SCHEMATIC,

EMITTER-COLLECTOR COUPLED JUNCTION FLIP-FLOP

60446



a/ PULSE AMPLITUDE vs. PULSE WIDTH



b/ PULSE AMPLITUDE vs. P.R.F.

TRANSISTORS: 2N36 CBS-HYTRON
TRANSFORMER: 50:25 TURNS/HALF ON A F262 FERRAMIC-H CORE

FIG. 13

TRANSFORMER-EMITTER-COLLECTOR-COUPLED JUNCTION FLIP-FLOP

Texas Instruments' 901's worked up to 600 kc and evidently would have gone faster, but for the fact that the output of the pulse generator was low at those frequencies. One of the sets of characteristic curves is shown in Figure 14 for this transistor.

3.3 Four-transistor Flip-flop

Noting the analogy between the vacuum tube and the transistor, Richard Baker, at this laboratory, decided to increase the top speed of the flip-flop by using "emitter-followers" in the feedback circuit. This corresponds closely to the vacuum tube technique used in the high-speed flip-flop developed here by Hal Boyd.[4] Our tests employed Baker's circuit exactly as he developed it (Fig.15). Only the results using the n-p-n silicon transitors will be presented here. Tests with other transistors revealed relatively the same improvement over the two-transistor circuitry. Figure 16 shows that no improvement is obtained over the emitter-collector coupled flip (compared to Figure 14) when the steering circuit coupling is used. Indeed, the sensitivity is considerably worsened and the top speed is slightly less while the only bright feature is a broadened range of triggering pulse widths. However, in the past it was found that these difficulties were associated with steering circuit type of triggering so that the circuit was slightly modified to employ emitter triggering. Using this type of triggering the typical pulse width characteristics are obtained with much greater sensitivity than was found for steering circuit triggering. Moreover, the top speed with this type of triggering was found to be as high as 900 kc which exceeds the previous circuit by at least 50 percent. This circuit is shown in Fig. 17 and the results are given in Fig. 18.

Signed: Edmund U. Cohler
Edmund U. Cohler

EUC/md

DISTRIBUTION:

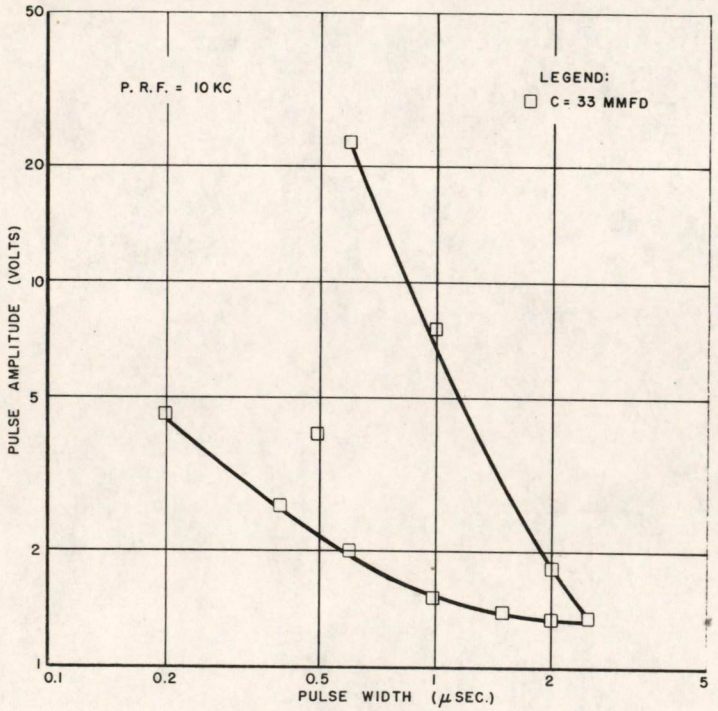
Transistor Distribution (2)

List of Figures:

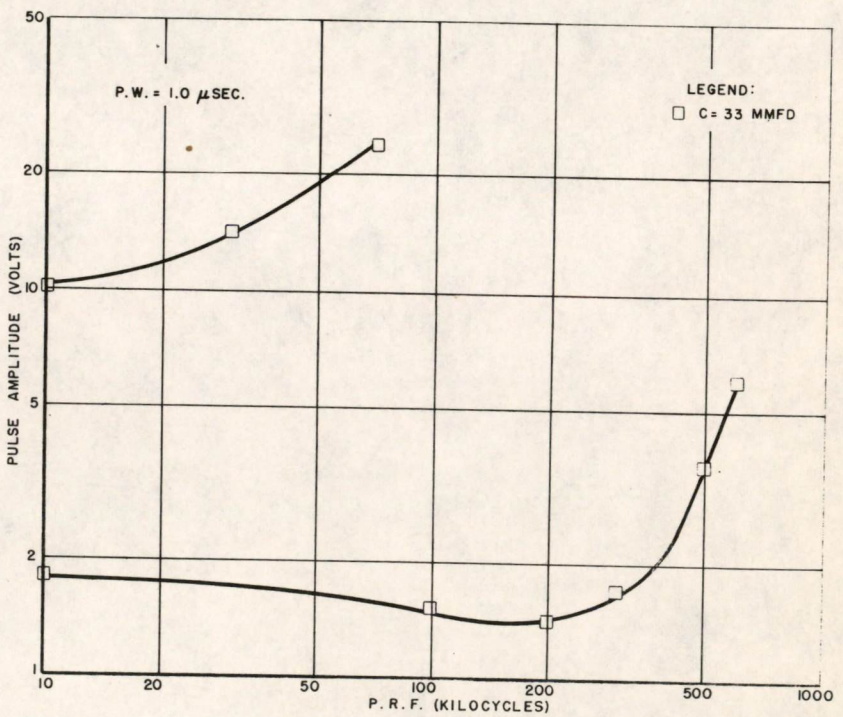
Figure 1 - B-60435(2a) Figure 7. - A-60441(4b) Figure 13 - B-60447(5d)
Figure 2 - B-60436(3a) Figure 8 - B-60442(4c) Figure 14 - B-60448(6a)
Figure 3 - B-60437(3b) Figure 9 - A-60443(4d) Figure 15 - A-60807(6b)
Figure 4 - B-60438(3c) Figure 10 - B-60444(5a) Figure 16 - B-60808(6c)
Figure 5 - A-60439(3d) Figure 11 - B-60445(5b) Figure 17 - A-60806(6d)
Figure 6 - B-60440(4a) Figure 12 - A-60446(5c) Figure 18 - B-60809(6e)

4. Boyd, H.: E526 High-Speed (5965) Flip-Flop, February, 1953

B-60448



a/ PULSE AMPLITUDE vs. PULSE WIDTH

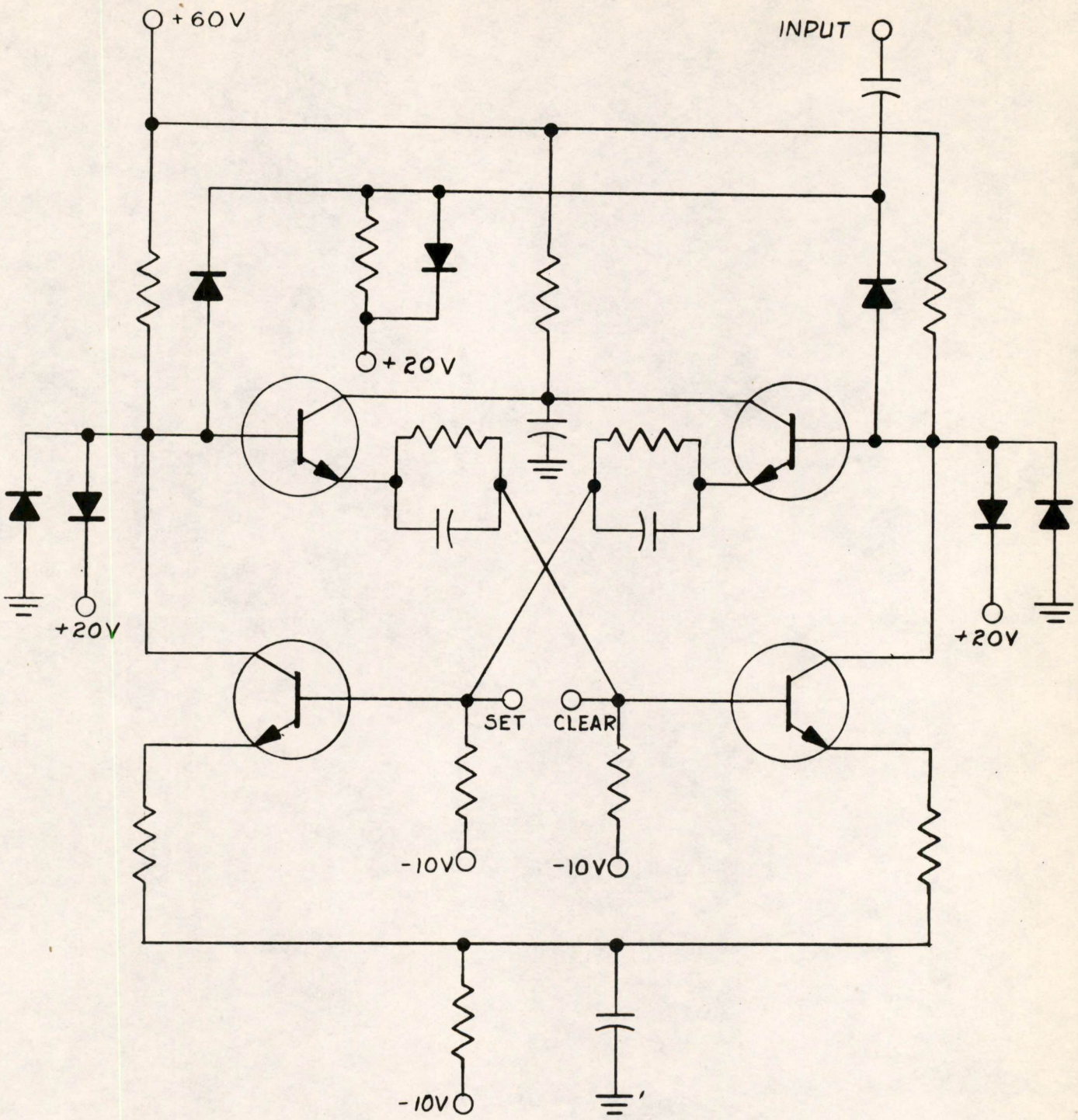


b/ PULSE AMPLITUDE vs. P. R. F.

TRANSISTORS: T. I. 901's
TRANSFORMER: 50:25 TURNS / HALF ON A F262 FERRAMIC - H CORE

FIG. 14

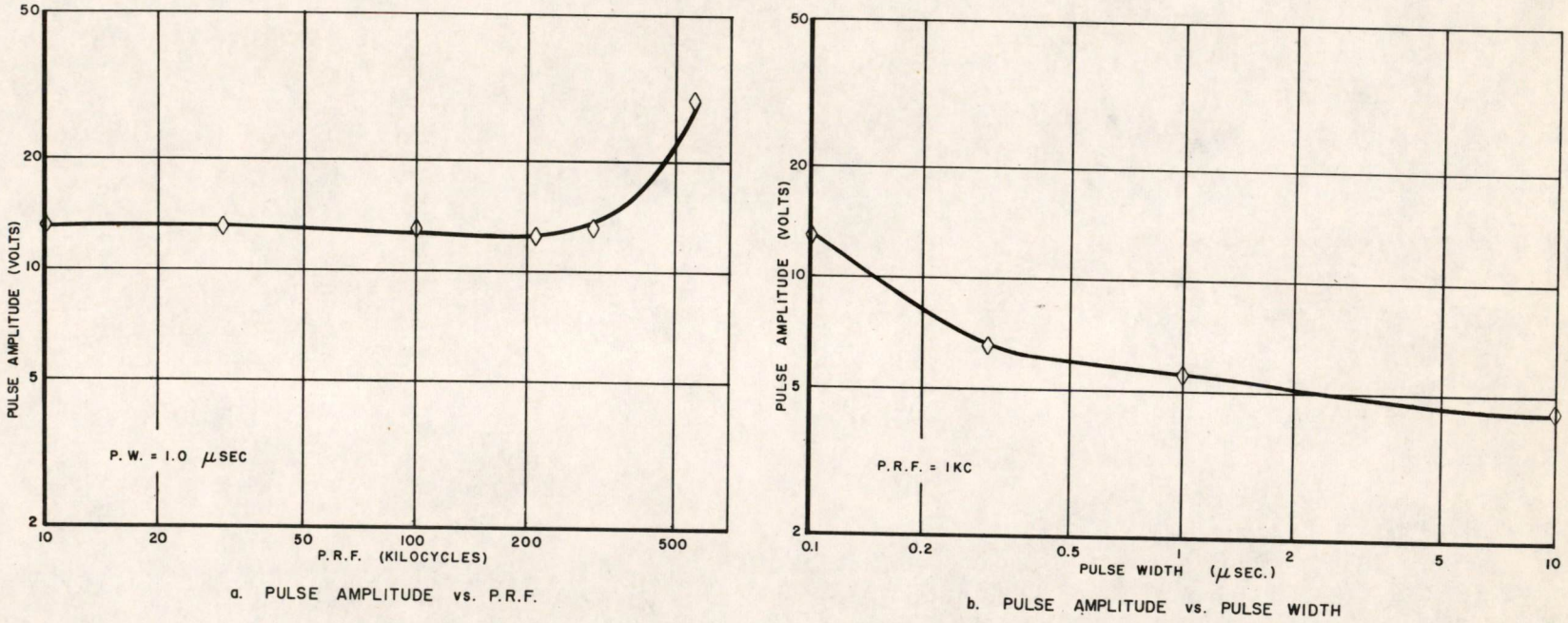
TRANSFORMER-EMITTER-COLLECTOR-COUPLED
JUNCTION FLIP-FLOP USING SILICON TRANSISTORS



A-60807

FIG. 15

R. BAKER'S F4 FOUR-TRANSISTOR FLIP-FLOP



a. PULSE AMPLITUDE vs. P.R.F.

b. PULSE AMPLITUDE vs. PULSE WIDTH

FIG. 16

TRIGGERING CHARACTERISTICS OF THE
FOUR-TRANSISTOR FLIP-FLOP WITH STEERING CIRCUIT

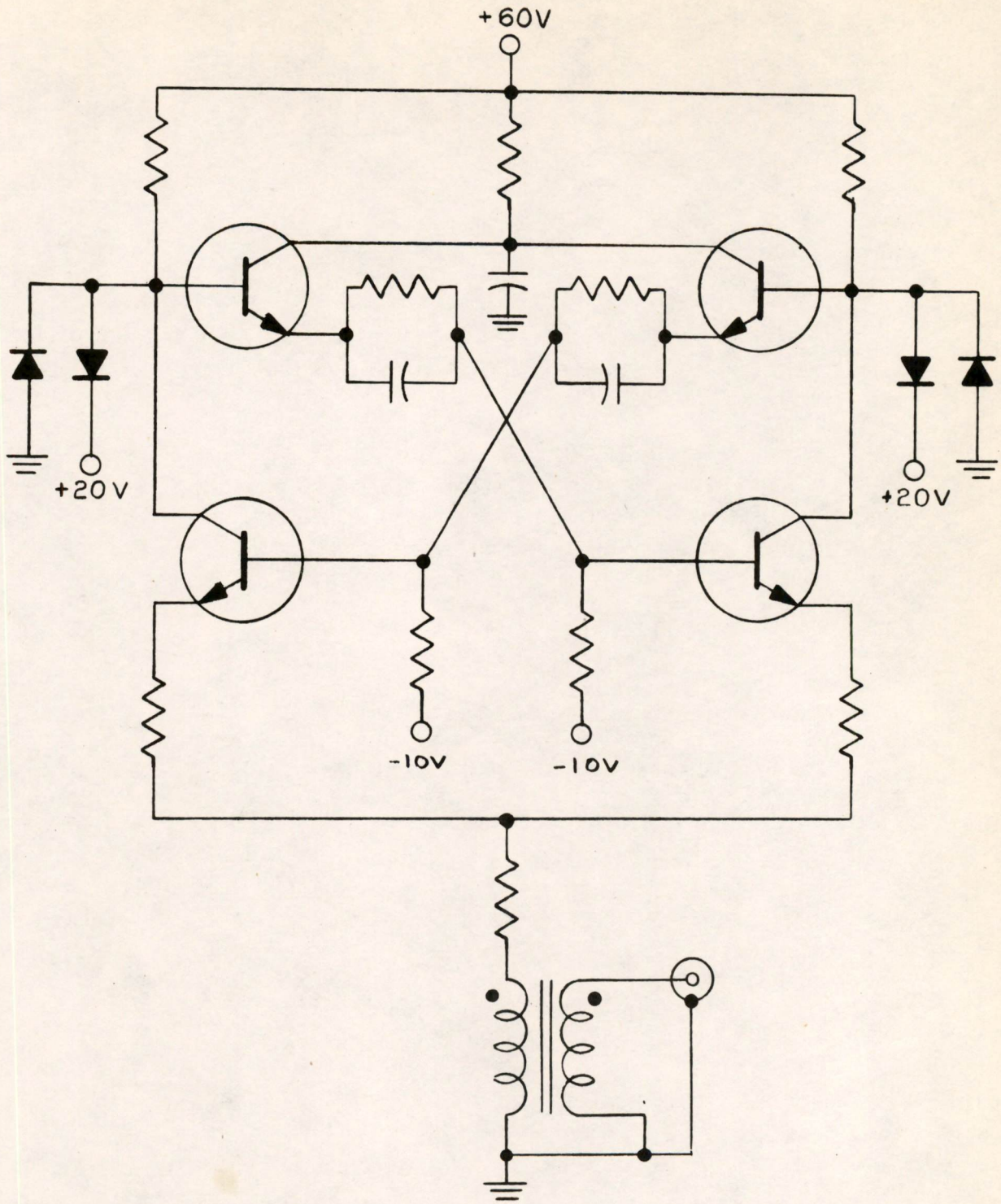
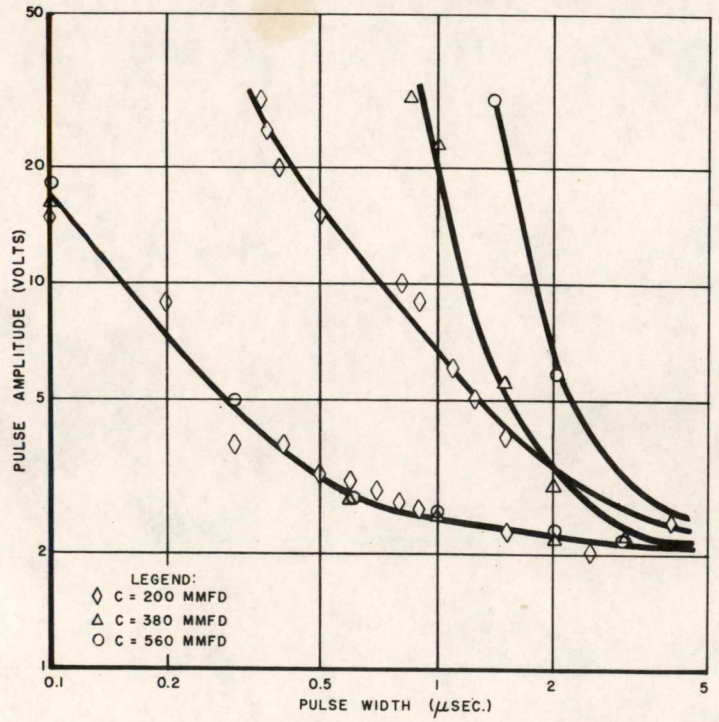
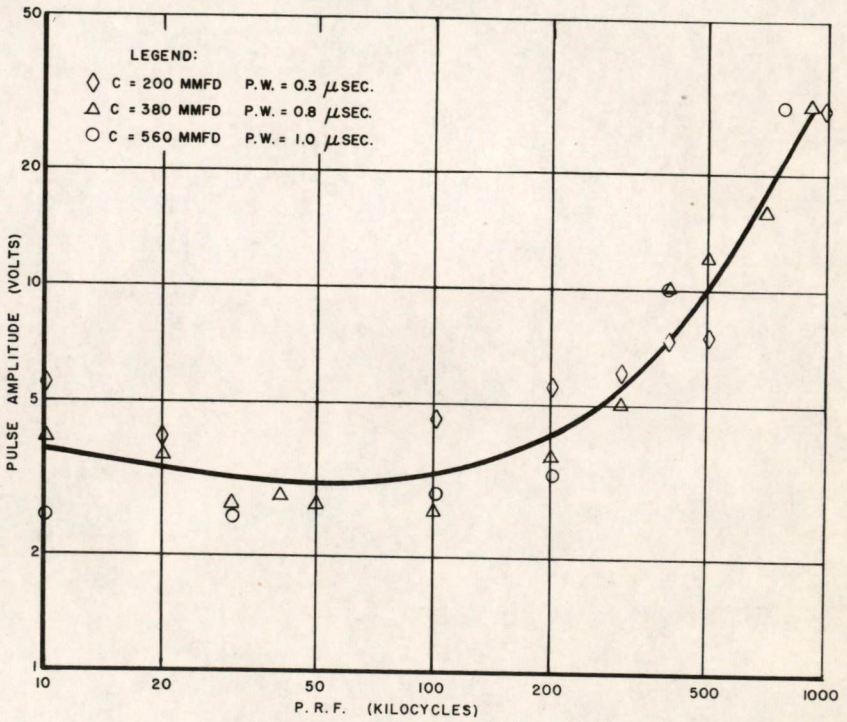


FIG. 17

FOUR-TRANSISTOR
EMITTER-TRIGGERED FLIP-FLOP



a./ PULSE AMPLITUDE vs. PULSE WIDTH



b./ PULSE AMPLITUDE vs. P.R.F.

FIG. 18

CHARACTERISTICS OF FOUR-TRANSISTOR
EMITTER-TRIGGERED FLIP-FLOP

PR. C2100

EX 203

7161

K. Olsen

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: THE MULTI-SEQUENCE PROGRAM CONCEPT

To: R. R. Everett

From: W. A. Clark

Date: 5 November 1954

Approved: N. L. Daggett

Abstract: A computer program operating in a single-program-counter machine consists of a single control-sequence. It is possible to construct computing systems with several program-counters operating a multi-sequence program. In a system consisting of one computer operating many asynchronous terminal devices, multi-sequence operation is generally more efficient than one-sequence operation.

Introduction

It is the object of this note to extend certain ideas concerning the sequence structure of computer programs. In particular, the concept of a computing system operating a program with several independent sequences advancing concurrently is applied to the problem of centralizing the control of a set of asynchronous devices. It will be assumed that the reader is reasonably familiar with the principal logical features of computers of the one-address, stored-program class on which these ideas are based.

By "stored program" we mean an encoded sequence of control words held in an addressable storage element. In the usual mode of operation a control word is removed from this storage and transferred to a central control element which decodes the word and distributes command signals to the various elements of the system. In general, the control word will contain the address of another stored word on which specified operations are to be carried out in an arithmetic element or other operation element.

Control Sequencing

The process of obtaining the control word, decoding it, and carrying out the operations it specifies constitutes one step in the execution of a control sequence. Upon completion of any step in the sequence,

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

the address of the control word for the next step is held in a register variously called the "instruction counter" or "program counter". At the maximum operating rate, the advance to the next step in the sequence occurs automatically upon completion of the current step.

The advance rate can be reduced from this maximum and can also be made to depend on timing events in a device external to the central computer, e.g. a manually-operated pushbutton or even another computer. These timing events can occur aperiodically as long as the maximum rate is not exceeded.

Note that the program as we have described it consists of a single control-sequence. One number only, an address held in the program counter, is required to specify the next step of the sequence. This sequence may be very complex, involving cycles and alternative branches through many subsequences, but control will eventually pass through every subsequence if the program is operated long enough.

The Multi-Sequence Program

It is possible to construct programs of more than one sequence. Consider, for example, a computing system consisting of two intercommunicating stored-program computers. If it is assumed that each computer is operating a one-sequence program requiring to some extent the cooperation of the other computer, then it might be said that the computing system is operating a single two-sequence program. Two numbers, the addresses in the program counters, are required to specify the next double-step of the two-sequence program. This idea may be generalized to an N-sequence program operating in an N-computer system (assuming that there are no computer cliques within the system).

A multi-sequence program can also be constructed for a single computer. The general requirement is that the operation of one sequence must not interfere with the operation of any other. In general, this means that the operating registers of the computer must be time-shared by the sequences. A program counter must be provided for each sequence and the computing system must include an element for deciding which sequence is to be advanced during any given control cycle.

These sequences may be time-interleaved in an arbitrary fashion and each sequence can be advanced step by step at its own rate as determined by timing events in a separate clock associated with the sequence.

Application to a System with Asynchronous Terminal Devices

A multi-sequence programmed computer is well-suited to operation in a system with many asynchronous terminal devices. Consider the general control and communication requirements in this kind of system:

A typical terminal device can appear in one of several states

at any given time. As an example, a tape unit may be running in reverse, it may be in an erase mode, etc. A control element associated with the device determines the transitions from one state to another and initiates data transfers between the device and the computer. In general, the timing of these transfer and transition events is critical within certain limits which depend upon the characteristics of the device and its particular application. For example, a tape reader must read only at those times when a line of data is under the reading heads and must transfer this data before the next line is read.

Now it is possible to simplify the system by centralizing to a large extent the control of many different devices. In particular, it is possible to incorporate many of these control functions into the control element of the central computer and to program the sequences of transitions and data transfers required to operate the devices. It is necessary only to provide the computer with a means of selecting one device at a time and a repertoire of orders for dealing with data transfers and transitions. The problem is that the existence of different timing requirements for a set of devices makes it difficult to incorporate the control sequences of the entire set into a single one-sequence program without sacrifice of computing efficiency. However, an efficient multi-sequence program can be constructed with a separate minor sequence devoted to the operation of each device and a major sequence which constitutes the main body of the program. The advance rate in any minor sequence can be tied to the particular timing requirements of the device being controlled by the sequence. The major sequence is advanced at the maximum rate possible in the remaining computing time. The timing problem is reduced to one of determining the number of devices which can be operated in the allocated computing time without exceeding the maximum rate of the system.

Many terminal devices are concerned almost exclusively with the transfer of data and can be operated without requiring all of the functions of an arithmetic element. Thus if a separate, simplified operation element is provided to deal with just those functions which are required, then the arithmetic element need not be time-shared between the major sequence and the minor sequences for these devices.

Time-Shared Sub-routines

If a sub-routine is constructed in such a way that none of its control-words requires modification during operation of the program, then it may be time-shared in an arbitrarily inter-leaved fashion among the sequences of a multi-sequence program. It is generally possible to do this given enough separately-stored "index-registers" which modify any operand addresses referred to by the control-words of the sub-routine without altering the control-words themselves. Each sequence using the sub-routine then forms its own operand addresses by referring to its own set of index-registers.

In the case of a computing system with many terminal devices,

the possibility of time-sharing sub-routines may mean a considerable saving in program storage space if the system includes several devices which require identical control sequences but different operands. By providing a set of index-registers for each device, only one set of control words need be stored.

As an extreme case, a computing system can be constructed which consists of several identical computers in various phases time-sharing the same program but operating on different sets of data.

Conclusion

Multi-sequence operation offers advantages in the centralization of control in a system consisting of a computer operating asynchronously with many terminal devices. The general concepts of a multi-sequence program may also be of some help in visualizing the operation of a computing system with several intercommunicating computers.

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Division 6 – Lincoln Laboratory
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SUBJECT: DISPLAY LINE DRIVER (INDIVIDUAL STAGE ANALYSIS)

To: C. L. Corderman

From: Henry E. Zieman and Joseph Kriensky

Date: May 18, 1956

Approved: C. L. Corderman
C. L. Corderman

Abstract: The original M-note described the operation of the display line driver in general terms. The purpose of this supplement is to thoroughly analyse the individual stages, presenting sufficient data for the evaluation of the circuit and also for troubleshooting in case of eventual failure. Operating margins, frequency response, power supply requirements and maintenance data for the individual stages are presented.

The results of the margins indicate that the circuit will operate satisfactorily when any tube falls below 60% of bogie, and, in the majority of cases, considerably below 60%.

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

1.0 GENERAL DESCRIPTION

The display line driver is an amplifier which receives a voltage signal from one of the display decoders, amplifies this signal to 3.7 times its value and feeds the output to 74, 126, or 252 parallel display tube input circuits through approximately 1700 feet of coaxial cable (K109A). The line driver contains a gain control to insure that each one can be set to exactly the same gain. The circuit exists in three pluggable units which are one preamplifier P.U. 3006481 and two output P.U.'s 3006482. See 6M-3284, paragraphs 1.1 and 1.2 for a description of the line driver as a differential amplifier and as a mean level regulator. The schematic for this circuit is shown in drawing E75792.

2.0 OUTPUT LOAD SPECIFICATIONS

This paragraph supercedes paragraph 2.0 of 6M-3284. Figure 2.0.1 (SA 65536) is a diagram of the actual input circuit to each pair of deflection plates in a console. This circuit provides a slight control of the gain and position of the signal to accomodate manufacturing tolerances in display tubes. The values of some of the components in the console input are different depending upon the particular plates being driven. Table 2.0.1, referring to Figure 2.0.1 (SA 65536) shows these differences.

Table 2.0.1 ACTUAL CONSOLE INPUT CIRCUIT COMPONENTS (Fig. 2.0.1)

S.D.		R_1	C_1	R_2
	H. Char. Sel.	47K 1W 1%	1000 pf	620K 1W 1%
	V. Char. Sel.	47K 1W 1%	680 pf	360K 1W 1%
	H. Char. Comp.	47K 1W 1%	1000 pf	560K 1W 1%
	V. Char. Comp.	47K 1W 1%	1000 pf	560K 1W 1%
D.D.				
Fed in Parallel By One Line Driver	H. Char. Sel.	47K 2W 1%	270 pf	300K 2W 1%
	H. Char. Comp.	47K 2W 1%	270 pf	300K 2W 1%
Fed in Parallel By One Line Driver	V. Char. Sel.	47K 2W 1%	270 pf	300K 2W 1%
	V. Char. Comp.	47K 2W 1%	270 pf	300K 2W 1%
	H. Char. Defl.	5.1K 2W 1%	1000 pf	100K 2W 1%
	V. Char. Defl.	5.1K 2W 1%	1000 pf	100K 2W 1%

Table 2.0.1 Con't				
D.D. Auxiliary Console		R_1	C_1	R_2
Fed in Parallel By One Line Driver	H. Char. Sel.	47K 1W 1%	390 pf	300K 1W 1%
	H. Char. Comp.	47K 1W 1%	390 pf	300K 1W 1%
Fed in Parallel By One Line Driver	V. Char. Sel.	47K 1W 1%	390 pf	300K 1W 1%
	V. Char. Comp.	47K 1W 1%	390 pf	300K 1W 1%
	H. Char. Defl.	5.1K 1W 1%	1500 pf	100K 1W 1%
	V. Char. Defl.	5.1K 1W 1%	1500 pf	100K 1W 1%

The equivalent console input circuit is shown in Figure 2.0.2 (SA 65537) and the various values depending upon the pair of plates being driven, are indicated in Table 2.0.2.

Table 2.0.2 EQUIVALENT CONSOLE INPUT CIRCUIT (Fig. 2.0.2)					
		R_2	C_2	R_1	C_1
S.D. Console S.D.	V. Sel.	506K	190 pf	232 K	51 pf
	H. Sel.	760	192	224	55
	V. Comp.	206	215	225	51
	H. Comp.	704	199	227	45
S.D. Console D.D.	V. Sel. & Comp.	174	255	107	79
	H. Sel. & Comp.	174	250	107	75
	V. Defl.	106	216	216	69
	H. Defl.	106	212	216	75
D.D. Aux. Console	V. Sel. & Comp.	210	235	111	103
	H. Sel. & Comp.	210	245	111	105
	V. Defl.	120	212	210	106
	H. Defl.	156	247	217	84

The total equivalent load presented to each line driver including the cables and all consoles takes the same configuration as shown in Figure 2.0.2 (SA 65537). The values of each arm in this case are given in Table 2.0.3.

Table 2.0.3		TOTAL EQUIVALENT LOAD TO EACH AMPLIFIER				MAX. VOLTS REQUIRED PUSH PULL
		R_2	C_2	R_1	C_1	
S.D.	V. Sel.	6.84 K	.044 µf	3.14 K	.0038 µf	221 V.
	H. Sel.	10.25	.044	3.02	.0041	118
	V. Comp.	9.55	.046	3.04	.0038	134
	H. Comp.	9.5	.045	3.07	.0033	134
D.D.	V. Sel. & Comp.	1.33	.073	.893	.011	276
	H. Sel. & Comp.	1.33	.073	.893	.011	276
	V. Defl.	.91	.070	1.75	.010	375
	H. Defl.	1.0	.071	1.78	.010	375

2.1 OUTPUT VOLTAGE REQUIREMENTS

For optimum performance of the display tubes, the mean level of the output signal should be held at +45 volts at all times. A special regulator circuit is incorporated to stabilize this mean level. The maximum push-pull voltage required out of any line driver depends upon the particular lines it is feeding. These values are tabulated in the last column of Table 2.0.3. (Example: For a maximum of 375 V. push-pull required, each output terminal of the amplifier must swing from +139 volts to -49 volts.) The rise time should be sufficient to permit the output voltage to arrive to 99.9% of its final value within 20 microseconds.

2.2 INPUT SIGNAL SPECIFICATIONS

The maximum output of a decoder is approximately 240 volts push-pull with a mean level of +150 volts. This output can be controlled by varying the termination on the decoder. For maximum output, the output impedance of the decoder is 11.2 kilohms from each output terminal to +150 volts. As the output voltage is decreased the output impedance is also decreased approaching zero output impedance for zero output volts. For the exact relationship between decoder output voltage and decoder output impedance see 6M-3971.

3.0 INDIVIDUAL STAGE ANALYSIS

3.1 Output Stage

Figure 3.1.1 (SA 61516) shows the circuit schematic of the output stage. The circuit exists in two identical pluggable units 3006482. Drawings 3007699 and 3007701 show the required card assembly and detail to make up this circuit.

Seven tubes in parallel make up each side of this push-pull power amplifier stage. Provision is built-in for this stage to be used with less tubes per side if an application arises where less output power is required. All data presented here refers to seven tubes per side. The circuit is designed to drive the large capacitive, small resistive load of any of the analogue lines (mentioned in Table 2.0.3) feeding the electrostatic deflecting plates of the Charactron and Typotron.

Each of the S.D. lines (to the Charactron) present practically identical loads to the line drivers and similarly each of the D.D. lines (to the Typotron) load the line drivers practically identically. The complex frequency response of this output stage is expressed by four different equations depending upon the lines being fed (S.D. or D.D.) and the mode of operation of the line driver (differential mode, or common mode).

The complex response for S.D. considering the amplifier operating in the differential mode, is (referring to MIT Comp. Book, #880 Pg. 42)

(eq. 3.1.1)

$$\frac{e_o}{e_{IN}} = K_1 G_1 = 20\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1+j\frac{f}{14.8\times10^3}\right)\left(1+j\frac{f}{391\times10^6}\right)}$$

The common mode response for S.D. is:

(eq. 3.1.2)

$$\frac{e_o}{e_{IN}} = K_2 G_2 = 21.3\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1+j\frac{f}{14.9\times10^3}\right)\left(1+j\frac{f}{392\times10^6}\right)}$$

For D.D. the differential mode response is:

(eq. 3.1.3)

$$\frac{e_o}{e_{IN}} = K_3 G_3 = 16.8\,db\ \frac{(-1)\left(1 - j\frac{f}{5.07\times10^9}\right)}{\left(1+j\frac{f}{12.5\times10^3}\right)\left(1+j\frac{f}{391\times10^3}\right)}$$

And the common mode response is:

$$\text{(eq. 3.1.4)}\quad \frac{e_o}{e_{IN}} = K_4 G_4 = 20\,db\,\frac{(-1)\left(1-j\frac{f}{5.07\times10^9}\right)}{\left(1-j\frac{f}{10.7\times10^3}\right)\left(1+j\frac{f}{391\times10^6}\right)}$$

Since these 4 equations are so close, the normalized amplitude and the phase response of all four are given in Figure 3.1.2 (SB 48741-G)

The notation KG with different subscripts to distinguish between responses of different stages or circuits is used throughout this paper. K equals the d-c gain of the circuit under consideration and G equals the frequency variant portion of the amplitude and phase response. This form for the response is used to simplify the graphical solution of the equations.

Consider a circuit with two output terminals (A and B) and two input points (A^1 and B^1). The differential mode output is defined as the voltage at A minus the voltage at B. The common mode output is the mean value of the voltage at A and the voltage B, i.e.,

$$\frac{\text{Voltage at A + voltage at B}}{2}$$

Similarly the differential mode input is the voltage at A^1 minus the voltage at B^1 and the common mode input is:

$$\frac{\text{Voltage at } A^1 + \text{voltage at } B^1}{2}$$

The differential mode response is the ratio of the differential mode output to the differential mode input. The common mode response is the ratio of the common mode output to the common mode input.

Data useful for evaluation and maintenance of this circuit is given in the following tables for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.1.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
3a or 3b	+45
5a or 5b	-172.5
6a or 6b	+41 V.
7a or 7b	+37.2

Table 3.1.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
V_1-R3a,b thru V_7R50a,b, 4.7K 47W 5% (per resistor)	205	43.7	8.94
R_{v1p} thru R_{v7p} 47 ohm 2W 5% (per resistor)	4	87.4	0.359
R_{v1s} thru R_{v7s} 39 ohm $\frac{1}{2}$ W 5% (per resistor)	0.21	5.38	0.0012
R_{v1g} thru R_{v7g} 100 ohm $\frac{1}{2}$ W 5%	0	0	0
R50-1 680 ohm 47W 5%	52.6	77.4	4.07
C100 0.47 µf 200 V.	37.4	----	----
V_1 thru V_7 6146 P-K (per tube)	191	87.4	16.7
V_1 thru V_7 6146 SC-K (per tube)	187	5.38	1.01

Table 3.1.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	1225	306
+90	77.4	6.96
-150	1300	195

Figure 3.1.3 (SA 48736-G) shows how this circuit behaves as the +90 volt marginal check line is varied. Different values of gm for each side of the output circuit were simulated by operating the stage with less tubes in parallel. Under normal operating conditions the amplifier will fail when the gm of each side of the output stage falls below 50% of bogie. With a 40 volt downward swing to +50 volts on the +90 volt marginal check line the circuit will operate until the average gm of the output stage is below 61% of bogie for a 1 K load or below 53% of bogie for a 500 ohm load. The circuit fails sooner under the 1 K load condition because of the larger voltage swing required at the output than for the 500 ohm load condition.

Failure is considered to occur when the line driver output waveform changes in amplitude or when the rise time exceeds specifications.

3.2 OUTPUT DRIVER STAGE

Figure 3.2.1 (SA 61262) indicates the circuitry of the output driver cathode follower which supplies the necessary power to drive the output stage. Drawings 3006878 and 3006879 show the required card assembly and detail to form this circuit.

The complex expressions for the gain of this stage are stated in the following two equations. (Refer to MIT Comp. Book #648, Pg. 45, for detailed solution.)

For the differential mode:

(eq. 3.2.1)

$$\frac{e_o}{e_{IN}} = K_5 G_5 = -2.01\,db \; \frac{\left(1 + j \frac{f}{53.1 \times 10^6}\right)}{\left(1 + j \frac{f}{4.7 \times 10^6}\right)}$$

For the common mode:

(eq. 3.2.2)

$$\frac{e_o}{e_{IN}} = K_6 G_6 = -2.46db \; \frac{\left(1 + j \frac{f}{3.26 \times 10^6}\right)\left(1 + j \frac{f}{49.8 \times 10^6}\right)}{\left(1 + j \frac{f}{1.30 \times 10^6}\right)\left(1 + j \frac{f}{12.7 \times 10^6}\right)}$$

Figure 3.2.2 (SB 48742-G) is a graph of eq. 3.2.1 and eq. 3.2.2 showing the normalized amplitude and the phase response of this stage as it operates in the differential mode and the common mode.

Data useful for evaluation and maintenance of this circuit is given in the following tables.

The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.2.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
9	-40
5a or 5b	-172.5
10a or 10b	-197

Table 3.2.2 COMPONENT LOADING			
Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R47-7 thru R47-11 6.8K 1W 5% (per resistor)	40	5.89	0.236
R47-1 thru R47-6 27K 2W 5% (per resistor)	127.5	4.72	0.601
RV8-1, RV8-4 1K $\frac{1}{2}$W 5%	0	0	0
V8a or V8b, 5998	122.5	14.2	1.74

Table 3.2.3 POWER SUPPLY REQUIREMENTS		
Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (B7)	28.4	8.52

When the -300 volt marginal check line (B7) is swung down we check V8, V7, V4, and V3b. We check V5 and V6 when this marginal check line is swung up. Each of these tubes will be considered separately in the appropriate individual stage analysis where all of the other tubes in the amplifier will be assumed to be at bogie gm.

Figure 3.2.3 (SA 48739-G) shows where the amplifier fails depending upon the amount of marginal check voltage and the condition of $V8_a$ and $V8_b$. Under normal operating conditions the amplifier will fail when the gm of $V8_a$ and $V8_b$ (5998) falls to 8% of bogie gm. If the -300 volt marginal check line (B7) is swung down to -315 volts, then the amplifier will fail if the gm of $V8_a$ and $V8_b$ has gone below 58% of bogie gm.

3.3 BUFFER CATHODE FOLLOWER

The circuit schematic for the buffer cathode follower is shown in Figure 3.3.1 (SA 65907). The card assembly and detail required to form this circuit are shown on drawings 3006876 and 3006877.

The complex expressions for the gain of this stage are given in the following two equations (refer to MIT Comp. Book #648, Pg. 51).

For the differential mode:

$$\text{(eq. 3.3.1)}\quad \frac{e_o}{e_{IN}} = K_7 G_7 = -9.05\,db\,\frac{\left(1+j\frac{f}{23.4\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{52.9\times10^3}\right)\left(1+j\frac{f}{17.7\times10^6}\right)}$$

For the common mode:

$$\text{(eq. 3.3.2)}\quad \frac{e_o}{e_{IN}} = K_8 G_8 = -9.05\text{db}\,\frac{\left(1+j\frac{f}{23.4\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{51.6\times10^3}\right)\left(1+j\frac{f}{14.1\times10^6}\right)}$$

Figure 3.3.2 (SB 48743-G) is a graph of equation 3.3.1 and equation 3.3.2 showing both the differential mode and common mode responses of this stage.

Data useful for the evaluation and maintenance of this stage is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.3.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
10a or 10b	-197
11a or 11b	-15
12a or 12b	17.5

Table 3.3.2 COMPONENT LOADING

Components	Voltage (in volts)	Current (in ma.)	Power (in watts)
R42-1 or R42-2 68K 2W 1%	182	2.67	0.486
R42-3 or R42-4 39K 2W 1%	103	2.67	0.275
C42-2 or C42-3 100pf 500 V.	182	----	----
$V7_a$ or V7b, Z2177	165	2.67	0.440

Table 3.3.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+150	5.34	0.80
-300 (B7)	5.34	1.60

Figure 3.3.3 (SA 48740-G) shows where the amplifier fails depending upon the amount of marginal check voltage and the condition of V_{7a} and V_{7b}. Under normal operating conditions the amplifier will fail when the gm of V_{7a} and V_{7b} falls to 18% of bogie gm. If the -300 volt marginal check line (B_7) is moved to -315 volts the amplifier will fail if the gm of V_{7a} or V_{7b} has gone below 23% of bogie gm.

3.4 DIFFERENTIAL AMPLIFIER STAGE

Figure 3.4.1 (SA 61708) shows the circuitry of the differential amplifier stage. Drawings 3006874, 3070187, 3006875, 3070186 show the required card assemblies and details for this circuit.

The differential compensation control R35-1 allows for an optimum adjustment of frequency response and Nyquist stability for differential mode signals in spite of differences between line drivers due to tolerances of components.

The complex expressions for gain of this stage are stated in the following three equations (refer to MIT Comp. Book #880, Pg. 23).

For the differential mode with R35-1 equal to zero ohms.

(eq. 3.4.1)

$$\frac{e_o}{e_{IN}} = K_{9a} G_{9a} = 44.7db \; \frac{(-1)\left(1+j\frac{f}{58.9\times10^3}\right)\left(1-j\frac{f}{90.9\times10^9}\right)}{\left(1+j\frac{f}{5.63\times10^3}\right)\left(1+j\frac{f}{118\times10^3}\right)}$$

For the differential mode with R35-1 equal to 50K.

(eq. 3.4.2)

$$\frac{e_o}{e_{IN}} = K_{9b} G_{9b} = 44.7db \; \frac{(-1)\left(1+j\frac{f}{21.2\times10^3}\right)\left(1+j\frac{f}{58.9\times10^3}\right)\left(1-j\frac{f}{91.0\times10^9}\right)}{\left(1+j\frac{f}{32.2\times10^3}\right)\left(1+j\frac{f}{4.97\times10^3}\right)\left(1+j\frac{f}{968\times10^3}\right)}$$

For the common mode the response is:

(eq. 3.4.3)

$$\frac{e_o}{e_{IN}} = K_{10} G_{10} = 7.15db \; \frac{(-1)\left(1+j\frac{f}{59.0\times10^3}\right)\left(1+j\frac{f}{6.60\times10^6}\right)\left(1-j\frac{f}{6.55\times10^6}\right)}{\left(1+j\frac{f}{9.39\times10^3}\right)\left(1+j\frac{f}{1.12\times10^6}\right)\left(1+j\frac{f}{23.0\times10^6}\right)}$$

The normalized amplitude and the phase responses of this stage as stated in equations 3.4.1 and 3.4.2 are plotted in Figure 3.4.2 (SB 48744-G). Similarly a plot of equation 3.4.3 is given in Figure 3.4.3 (SB 48745-G).

Data useful for evaluation and maintenance of this circuit is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V while the other is biased at +180 V.

Table 3.4.1 VOLTAGE MEASURMENTS (referred to ground)

Point	Voltage (in volts d-c)
12a or 12b	-17.5
13	-137
14a or 14b	-140

Table 3.4.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R39-1, 2, 6, or 7 180K 2W 5% (per resistor)	267.5	1.48	0.396
R39-8 or 9 39K 2W 5%	163	4.17	0.680
R39-3 or 5 18K ½W 5%	0	0	0
R35-1 50K pot.	0	0	0
C39-1, 3 150 pf 500 V.	17	0	0
C39-2 150 pf 500 V.	0	0	0
V_5 or V_6, 6136, P-K	119.5	2.96	0.354
V_5 or V_6, 6136, SC-K	137	1.21	0.166

Table 3.4.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	5.92	1.48
-300 (C_3)	8.34	2.50

Figure 3.4.4 (SA 48746-G) shows a plot of marginal check data as taken on this stage. To simulate the gm of the tubes decreasing, the screen voltage was decreased and readings were taken at points of failure caused under various combinations of screen voltage and marginal check line voltage. Under normal operating conditions the circuit will fail when the gm of V5 and V6 falls below 11% of bogie gm. This failure point is determined from point A of Figure 3.4.4. From point B of this same figure we determine when the circuit will fail under a 15 volt positive swing on the marginal check line. When the -300 volt marginal check line (B_7) is swung up to -285 volt, the circuit will fail when the gm of V5 and V6 has decreased to 50% of bogie.

3.5 INPUT CIRCUIT TO DIFFERENTIAL AMPLIFIER

Figure 3.5.1 (SA 61709) shows the input circuit to the differential amplifier. The drawings which show the necessary card assemblies and details are 3006880, 3070187, 3006881, and 3070186. First the response of this stage to differential mode signals is considered. Provision is made to adjust the ratio of currents flowing through each half of the input circuit (V_{4a} and V_{4b}) by means of a position control. This allows a control of the d-c levels at the inputs to the differential amplifier, points 14a and 14b, despite component differences in each half of the line driver push pull stages. The position of the beam in the display tube can thus be controlled manually.

The differential output is at the plates of V4 (14a and 14b) with the input between points E5, or E6, and E7 or E8.

The response of this signal is given in the following equation (refer to MIT Comp. Book #880 Pg. 46 for complete solution.) The gain control is set for a normal overall gain from the line driver of 3.7.

(eq. 3.5.1)

$$\frac{e_o}{e_{IN}} = K_{11} G_{11} = -9.41\,db\, \frac{\left(1+j\frac{f}{140\times10^6}\right)\left(1+j\frac{f}{1.51\times10^6}\right)}{\left(1+j\frac{f}{136\times10^6}\right)\left(1+j\frac{f}{87.2\times10^3}\right)\left(1+j\frac{f}{1.93\times10^6}\right)}$$

Another differential response associated with this stage is the output produced between the plates of V_{4a} (14a) and V_{4b} (14b) (the grids of the differential amplifier V_5 and V_6) due to a differential signal between the feedback terminals C1 and C_5. This transfer function is given in the following equation (refer to MIT Comp. Book #880 Pg. 49)

(eq. 3.5.2)

$$\frac{e_o}{e_{IN}} = K_{13} G_{13} = -20.84\,db\, \frac{\left(1+j\frac{f}{67.7\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{87.9\times10^3}\right)\left(1+j\frac{f}{1.92\times10^6}\right)\left(1+j\frac{f}{137\times10^6}\right)}$$

Figure 3.5.2 (SB 48754-G) is the graph showing the normalized amplitude and the phase response for eq. 3.5.1 and 3.5.2.

The response of this stage to a common mode signal which has its output at the plate and input at the grid of V_{4a} or V_{4b} is given in the following expression (refer to MIT Comp. Book #880 Pg. 31) for complete solution.

(eq. 3.5.3)

$$\frac{e_o}{e_{IN}} = K_{15}G_{15} = 17.2db\,\frac{(-1)\left(1+j\frac{f}{884\times10^3}\right)\left(1-j\frac{f}{4.53\times10^6}\right)\left(1+j\frac{f}{130\times10^6}\right)}{\left(1+j\frac{f}{116\times10^3}\right)\left(1+j\frac{f}{1.24\times10^6}\right)\left(1+j\frac{f}{136\times10^6}\right)}$$

Figure 3.5.3 (SB 48753-G) is a plot of eq. 3.5.3 and shows the normalized amplitude and the phase response of this stage for common mode signals.

A fourth response associated with this stage is for an output at the grids of the differential amplifier (V_5 or V_6) due to a common mode signal appearing at the feedback terminals C_1 and C_5. The following equation gives this response (see MIT Comp. Book #880 Pg. 55) for complete solution.

(eq. 3.5.4)

$$\frac{e_o}{e_{IN}} = K_{14}G_{14} = -16.1db\;\frac{\left(1+j\frac{f}{67.7\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{88.3\times10^3}\right)\left(1+j\frac{f}{138\times10^6}\right)}$$

The fifth and last response for this stage is for an output at the grids of the differential amplifier (V_5 or V_6) due to a common mode signal appearing at an input terminal to the amplifier E_5, E_6, E_7, or E_8. This response is stated in the next equation (see MIT Comp. Book #880. Pg. 54).

(eq. 3.5.5)

$$\frac{e_o}{e_{IN}} = K_{12}G_{12} = -9.38db\,\frac{\left(1+j\frac{f}{884\times10^3}\right)\left(1+j\frac{f}{140\times10^6}\right)}{\left(1+j\frac{f}{87.1\times10^3}\right)\left(1+j\frac{f}{1.12\times10^6}\right)\left(1+j\frac{f}{136\times10^6}\right)}$$

Figure 3.5.4 (SB 48762-G) is a plot of equations 3.5.4 and 3.5.5.

Voltage, current, and power data for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V. is given in the following three tables.

Table 3.5.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
14a or 14b	-140
15	-270
26a or 26b	+180
27a or 27b	+150
C1 or C5	+45

Table 3.5.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R27-4, 5, R30-4, 5 0.47M 2W 1% (per resistor)	320	0.68	0.218
R27-3, 6 R30-3, 6 0.47M 2W 1% (per resistor)	290	0.617	0.179
R35-5, 6 39K 1W 1% (per resistor)	14.2	0.364	0.0052
R27-1, 2, 7, 8, R30-1, 2, 7, 8 0.47M 1W 1% (per resistor)	85.4	0.182	0.016
C27-1, 2, 3, 4 C30-1, 2, 3, 4 5pf 500 V. (per capacitor)	85.4	0	0
R35-4 82K 2W 1%	0	0	0
R35-3 50K 2W pot.	0	0	0
R V4-3, R V4-8 10K 1W 1% (per resistor)	28.6	2.86	0.082
Position Control 1K 2W pot.	1.4	2.86	0.008 (required)
V4a or V4b Z2177	130	2.86	0.372

Table 3.5.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (C_3)	5.72	1.72

Figure 3.5.5. (SA 48737-G) shows how the voltage on the plate and on the cathode of V_{4a} or V_{4b} varies as the -300 volt marginal check line B_7 is varied. It is seen that when the marginal check voltage is increased in a negative direction the plate to cathode voltage on each half of V_4 is decreased and the plate current is increased. This therefore, is the direction of swing on the marginal check line which can move the operating point of V_4 so as to cause the line driver to fail earlier. Under normal operating conditions the line driver will fail if the gm of V_{4a} and V_{4b} drops to 44% of bogie gm. If the marginal check line is moved to -315 volts the driver fails if the gm of each half of V4 drops below 76% of bogie.

Figure 3.5.6 (SA 48738-G) shows a plot of line driver failure points using the axes of V_4 filament voltage and marginal check line excursion. A comparison is made between a Z2177 and a 6072 tube, the 6072 having about one half the gm of a Z2177. This curve shows that for a down V_4 (50% down when a 6072 is used for the Z2177) the line driver failure will occur with a smaller excursion on the -300 volt marginal check line, B_7. This simply serves as an additional indication that this particular marginal check line effectively checks V_4. The filament voltage has no effect on the failure point until a critical value is reached which then abruptly causes failure regardless of the amount of marginal check voltage.

3.6 REFERENCE DRIVER CATHODE FOLLOWER

The circuit schematic for the reference driver is given in Figure 3.6.1 (SA 61710). The card assembly and detail for this stage is given in drawings 3006870 and 3006871. The gain for this stage is given in the following expression (refer to MIT Comp. Book #648 Pg. 53).

(eq. 3.6.1)

$$\frac{e_o}{e_{IN}} = K_{16} G_{16} = -18.1\,db\, \frac{\left(1+j\frac{f}{78.6\times10^3}\right)\left(1+j\frac{f}{92.8\times10^6}\right)}{\left(1+j\frac{f}{290\times10^3}\right)\left(1+j\frac{f}{20.7\times10^6}\right)}$$

Figure 3.6.2 (SB 48757-G) is the plot of eq. 3.6.1 and shows the normalized amplitude and the phase response of this stage.

Information helpful in evaluating and maintaining this circuit is given in the following three tables. The data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.6.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
16	-271
17	-77

Table 3.6.1 VOLTAGE MEASUREMENTS (Con't)	
Point	Voltage (in volts d-c)
18	-80

Table 3.6.2 COMPONENT LOADING			
Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R19-1 11K 1W 1%	29	2.6	0.076
R19-2 75K 2W 1%	194	2.6	0.505
C19-1 27pf 500 V.	194	0	0
V_{3b} $\frac{1}{2}$Z2177	167	2.6	0.434

Table 3.6.3 POWER SUPPLY REQUIREMENTS		
Voltage (in volts)	Current (in ma.)	Power (in watts)
+90	2.6	0.234
-300 (C_3)	2.6	0.780

Figure 3.6.3 (SA 48735-G) is a graph of points of failure for the line driver under various combinations of V_{3b} plate supply voltage and -300 volt marginal check line (B_7) voltage. By decreasing the plate supply voltage on this stage, we simulate the action of the tube as it decreases in gm. From the curve it is seen that the lower the gm of the tube, the smaller is the marginal check line excursion (in the negative direction) required to cause failure. Using data from this curve at point A and operating data for this stage and the tube characteristics it turns out that under normal operating conditions the line driver will fail when V_{3b} drops below 10% of its bogie gm. If the -300 volt marginal check line (B_7) is moved to -315 volts then the line driver will fail at point B of Figure 3.6.3 if the gm of V_{3b} drops below 14% of its bogie value.

3.7 REFERENCE AMPLIFIER

The circuit schematic for the reference amplifier is given in Figure 3.7.1 (SA 61711). The required card assemblies and details are shown on drawings 3006872, 3006900, 3070187, 3006873, 3006901 and 3070186.

The mean level compensation control (R35-2) allows for an optimum adjustment of frequency response and Nyguist stability for common mode signals in spite of differences between line drivers due to tolerances of components.

The mean level adjust control (R16-3) allows the mean level reference voltage to be manually preset so that the desired +45 volt mean level at the output of the line driver can be obtained despite differences between line drivers due to tolerances of components.

The complex response of this stage is given in the following two equations. The input is at the grid of V_{3a} and the output is taken at the plate of V_1. (See MIT Comp. Book #648 Pg. 54 for complete solution).

For R35-2 equal to zero:

(eq. 3.7.1)

$$\frac{e_o}{e_{IN}} = K_{17a} G_{17a} = 43.2\,db \; \frac{\left(1 + j\frac{f}{159\times10^6}\right)\left(1 + j\frac{f}{79.6\times10^6}\right)}{\left(1 + j\frac{f}{160}\right)\left(1 + j\frac{f}{102\times10^6}\right)}$$

For R35-2 equal to 5K

(eq. 3.7.2)

$$\frac{e_o}{e_{IN}} = K_{17b} G_{17b} = 43.2\,db \; \frac{\left(1 + j\frac{f}{159\times10^6}\right)\left(1 + j\frac{f}{79.6\times10^6}\right)\left(1 + j\frac{f}{3.18\times10^3}\right)}{\left(1 + j\frac{f}{157}\right)\left(1 + j\frac{f}{4.24\times10^6}\right)\left(1 + j\frac{f}{61.8\times10^6}\right)}$$

The normalized amplitude and the phase response as given by these two equations is plotted in Figure 3.7.2 (SB 48758-G).

Operating data for this stage which is helpful in evaluating and maintaining the circuit is given in the next three tables. The data (as for all corresponding tables in the other sections) is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 V. while the other is biased at +180 V.

Table 3.7.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
18	-80
19	-148
20	-150
21	-172
22	-150

Table 3.7.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R10-3 120K 2W 5%	330	2.75	0.907
R35-2 5K 2W pot.	0	0	0
R10-8, 9 39K 2W 5% (per resistor)	152	3.90	0.594
R16-1 100K 1W 1%	150	1.50	0.225
R16-2 1M ½W 5%	86	0.086	0.0074
R16-3 50K 2W pot.	22	1.50	0.112 (required)
R16-5 33K 1W 5%	128	3.88	0.497
C35-1 .01µf 600 V.	80	0	0
C10-2 .01 µf 600 V.	150	0	0
V_1 6136 P-K	68	2.75	0.187
V1 6136 SC-K	148	1.10	0.163
V_{3a} ½Z2177	148	3.95	0.585
V16-1 WA5783	86	2.38	0.205
V16-2 WA 5783	86	2.29	0.197

Table 3.7.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
+250	2.75	0.687
-300 (D_8)	7.8	2.34
-300 (C_3)	3.88	1.16

Figure 3.7.3 (SA 48760-G) is a plot of points of failure for the line driver depending upon the amount of V_{3a} plate supply voltage and -300 volt marginal check line (D_8) voltage. Decreasing values of plate supply voltage were used to simulate V_{3a} decreasing in gm. From the information on Figure 3.7.3 (at pt. A), operating data for this stage and the tube characteristic curve it is determined that under normal operating conditions the line driver will fail when the gm of V_{3a} has

dropped below 19% of bogie. If the -300 volt marginal check line D_8 is swung to -360 volts failure will occur if the gm of V_{3a} has fallen below 33% of bogie. No effective means for marginal checking V_1 has been found.

3.8 INPUT CIRCUIT TO REFERENCE AMPLIFIER

Figure 3.8.1 (SA 65906) shows the circuitry for this stage. The necessary card assemblies and details are shown on drawings 3006872, 3006900, 3006870, 3006873, 3006901 and 3006871.

The mean level rejection control is provided so that the value of resistance from each feedback terminal (C_1 and C_5) to the plate of V_2 can be made exactly equal. This balance of resistive values is necessary so that the differential signals appearing at the feedback terminals do not affect the mean level of the circuit.

The following equation gives the complex response of this stage for a mean level input at C_1 and C_5 and an output at the plate of V_2 (refer to MIT Comp. Book #880 Pg. 41)

(eq. 3.8.1)

$$\frac{e_o}{e_{IN}} = K_{18}G_{18} = -0.832\,db\,\frac{\left(1+j\frac{f}{71.8\times10^3}\right)\left(1+j\frac{f}{72.2\times10^3}\right)\left(1+j\frac{f}{129\times10^6}\right)}{\left(1+j\frac{f}{59.6\times10^3}\right)\left(1+j\frac{f}{70.3\times10^3}\right)\left(1+j\frac{f}{817\times10^3}\right)\left(1+j\frac{f}{125\times10^6}\right)}$$

The plot of this equation showing the normalized amplitude and the phase response of this stage is given in Figure 3.8.2 (SB 48759-G)

Data which may be used for evaluating and maintaining this stage is given in the following three tables. This data is for d-c operating conditions with each pair of inputs shorted and one set biased at +150 while the other is biased at +180 V.

Table 3.8.1 VOLTAGE MEASUREMENTS (referred to ground)

Point	Voltage (in volts d-c)
C_1 or C_5	+45
22	-150
23	-214
24	-257
25	-256

Table 3.8.2 COMPONENT LOADING

Component	Voltage (in volts)	Current (in ma.)	Power (in watts)
R19-5, 6 27K 1W 1% (per resistor)	68.9	2.55	0.176
R19-3, 4 47K 2W 1% (per resistor)	120	2.55	0.306
R16-4 5K 2W pot.	6.1	2.55	0.045 (required)
C19-4, 5 82 pf 500 V.	68.9	0	0
C19-2, 3 47pf 500 V.	120	0	0
R10-6 10K 1W 1%	44	4.4ma	0.194
R10-7 68K 1W 1%	44	0.65	0.0286
R10-1, 2 330K 1W 1%	43	0.130	0.0056
R10-5 82K 2W 5%	214	2.61	0.558
C10-1 .01 µf 600 V.	43	0	0
V_2 Z2177 (per section)	106	2.55	0.271
V16-3 WA 5783	86	2.48	0.214

Table 3.8.3 POWER SUPPLY REQUIREMENTS

Voltage (in volts)	Current (in ma.)	Power (in watts)
-300 (D8)	7.66	2.30

Figure 3.8.3 (SA 48761-G) is a graph of marginal check data for V2. As the -300 volt marginal check line D8 is swung in the positive direction the plate to cathode voltage on V_2 decreases and the plate current through V2 remains constant. This direction of marginal check line swing effectively checks V_2. Under normal operating conditions the line driver will fail if the gm of V2 falls below 31% of bogie. If the -300 volt marginal check line D8 is moved to -275 volts the amplifier will fail if the gm of V_2 is below 58% of bogie.

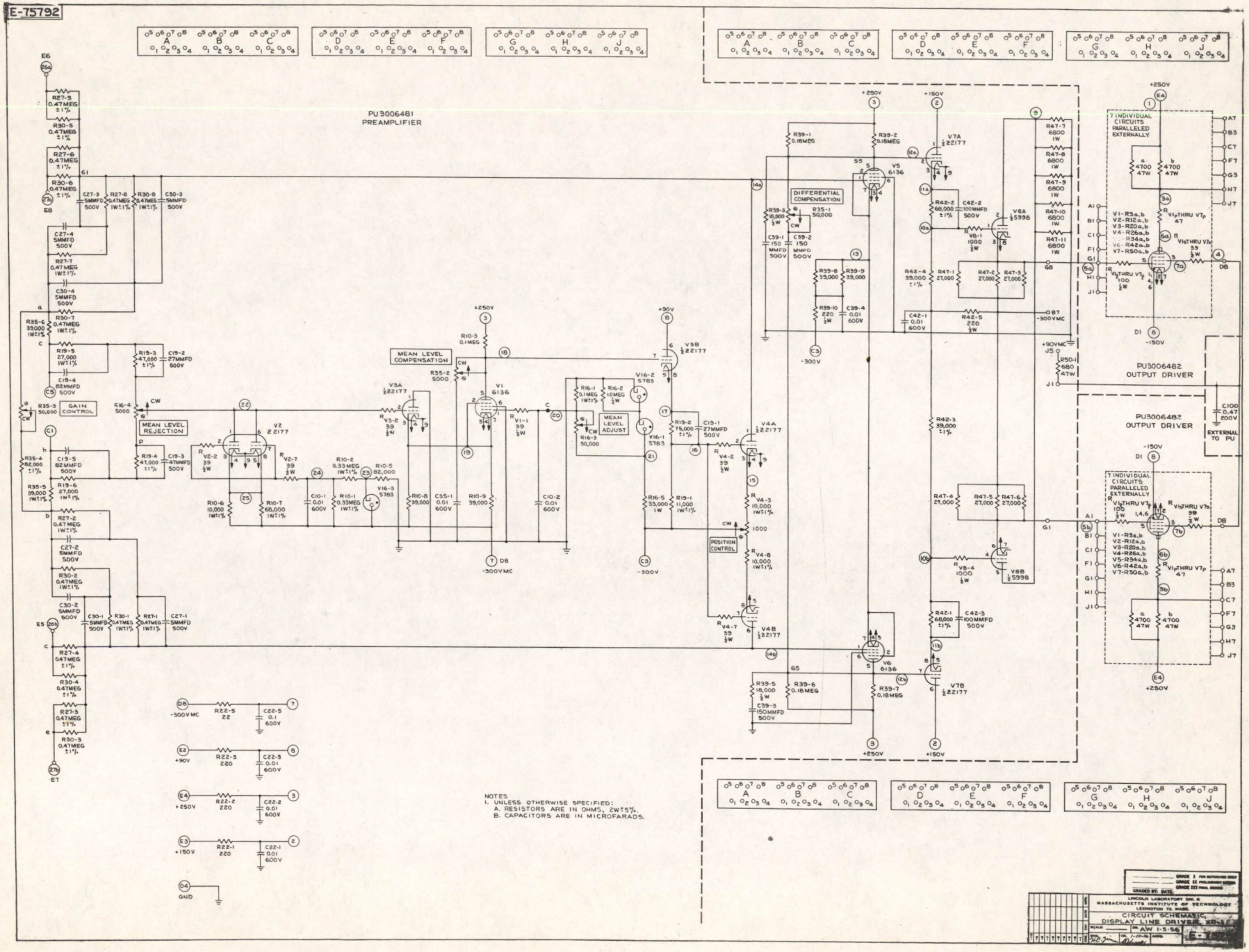
Signed Henry E. Zieman
H. E. Zieman

HEZ:JK:ej

Signed Joseph Kriensky
J. Kriensky

Attachments:

Fig. 1	E 75792
Fig. 2.0.1	SA 65536
Fig. 2.0.2	SA 65537
Fig. 3.1.1	SA 61516
Fig. 3.1.2	SB 48741-G
Fig. 3.1.3	SA 48736-G
Fig. 3.2.1	SA 61262
Fig. 3.2.2	SB 48742-G
Fig. 3.2.3	SA 48739-G
Fig. 3.3.1	SA 65907
Fig. 3.3.2	SB 48743-G
Fig. 3.3.3	SA 48740-G
Fig. 3.4.1	SA 61708
Fig. 3.4.2	SB 48744-G
Fig. 3.4.3	SB 48745-G
Fig. 3.4.4	SA 48746-G
Fig. 3.5.1	SA 61709
Fig. 3.5.2	SB 48754-G
Fig. 3.5.3	SB 48753-G
Fig. 3.5.4	SB 48762-G
Fig. 3.5.5	SA 48737-G
Fig. 3.5.6	SA 48738-G
Fig. 3.6.1	SA 61710
Fig. 3.6.2	SA 48757-G
Fig. 3.6.3	SA 48735-G
Fig. 3.7.1	SA 61711
Fig. 3.7.2	SB 48758-G
Fig. 3.7.3	SA 48760-G
Fig. 3.8.1	SA 65906
Fig. 3.8.2	SB 48759-G
Fig. 3.8.3	SA 48761-G


E-75792
PU3006481
PREAMPLIFIER
PU3006482
OUTPUT DRIVER
PU3006483
OUTPUT DRIVER
DIFFERENTIAL COMPENSATION
MEAN LEVEL COMPENSATION
MEAN LEVEL REJECTION
MEAN LEVEL ADJUST
GAIN CONTROL
POSITION CONTROL
7 INDIVIDUAL CIRCUITS PARALLELED EXTERNALLY
EXTERNAL TO PU
+250V
+150V
+90V
-300V
-150V
-300VMC
GND
NOTES
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, 2W ±5%.
B. CAPACITORS ARE IN MICROFARADS.
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.
CIRCUIT SCHEMATIC
DISPLAY LINE DRIVER, XR-1
SCALE
DR AW 1-5-56
CH
APPR

SA-65536

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY

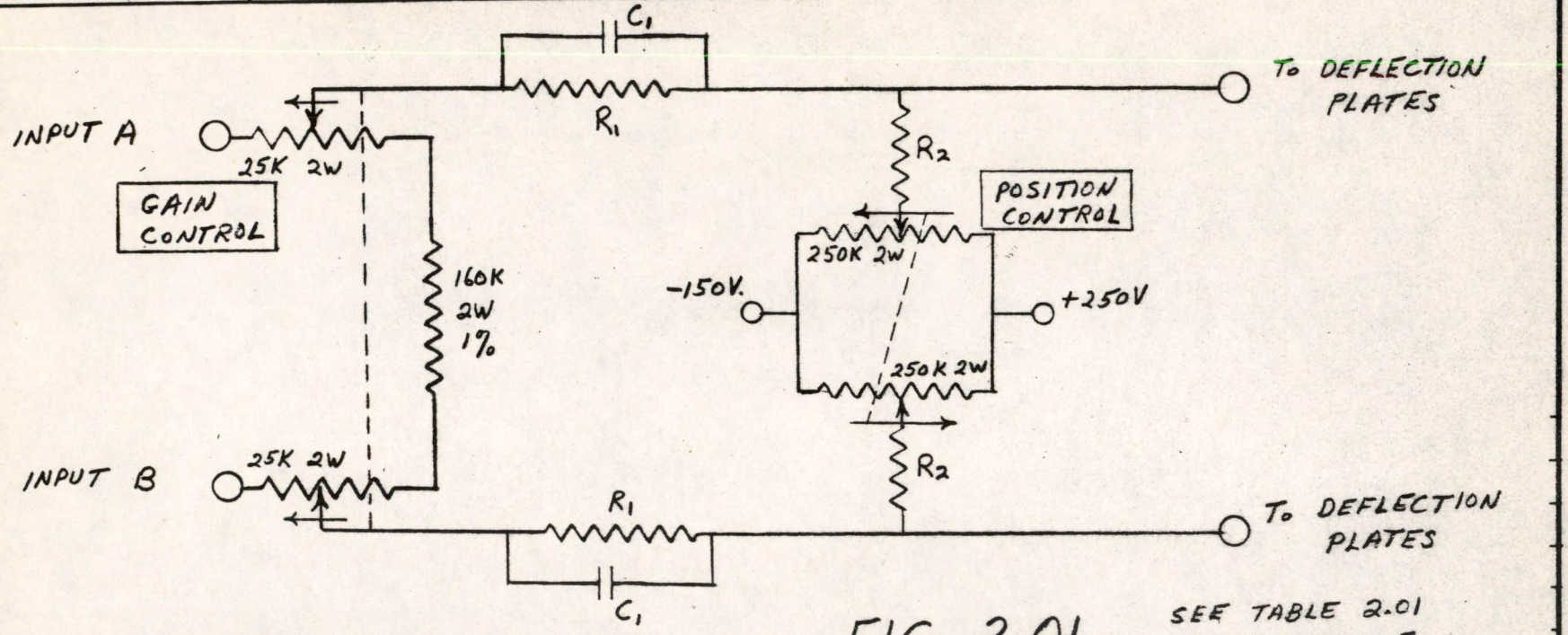


FIG. 2.01

SEE TABLE 2.01 FOR VALUES OF R_1, C_1 and R_2

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-1			
-2			
-3			
-4			
-5			
-6			
-7			
-8			
-9			
-10			
-11			
-12			
-13			
-14			
-15			
-16			
-17			
-18			
-19			
-20			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

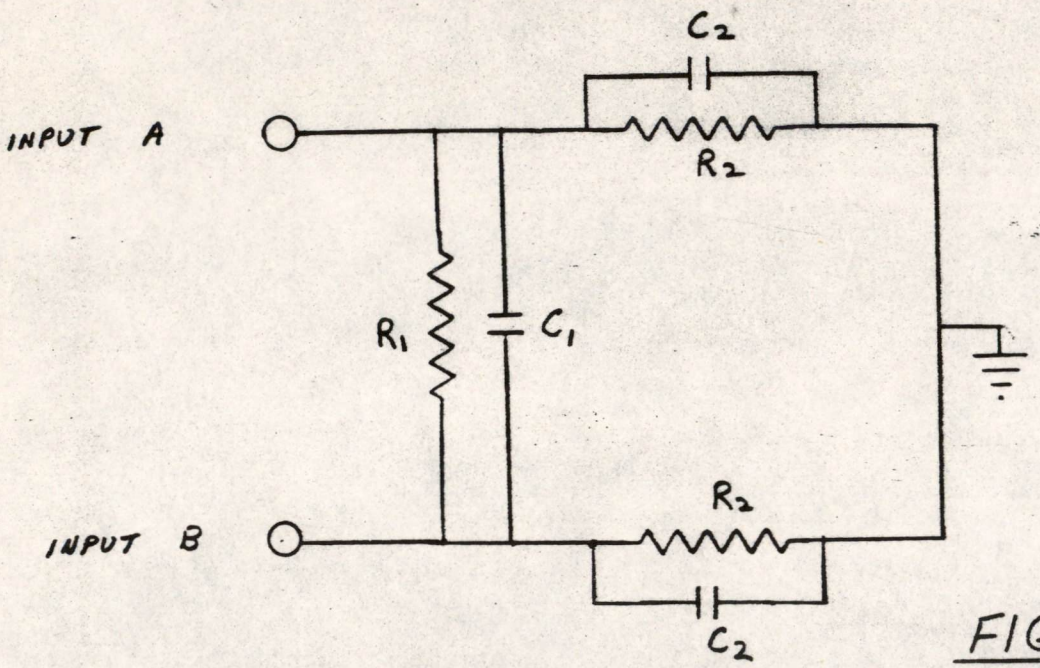
CONSOLE GAIN AND POSITION CONTROL

SCALE:	DR. J. Kreinsky	SA-65536
ENG. J. Kreinsky	CK.	APPD.

8M-7-54-Boston Blue Print

SA- 65537

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



FOR INPUT CKT. TO ONE CONSOLE
SEE TABLE 2.02

FOR TOTAL LOAD ON EACH DRIVER
SEE TABLE 2.03

FIG. 2.02

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

EQUIVALENT CIRCUIT

SCALE: DR. J. Krainsky
ENG. J. Krainsky CK. APPD.
SA- 655 37

8M-7-54-Boston Blue Print

SA- 61516

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY

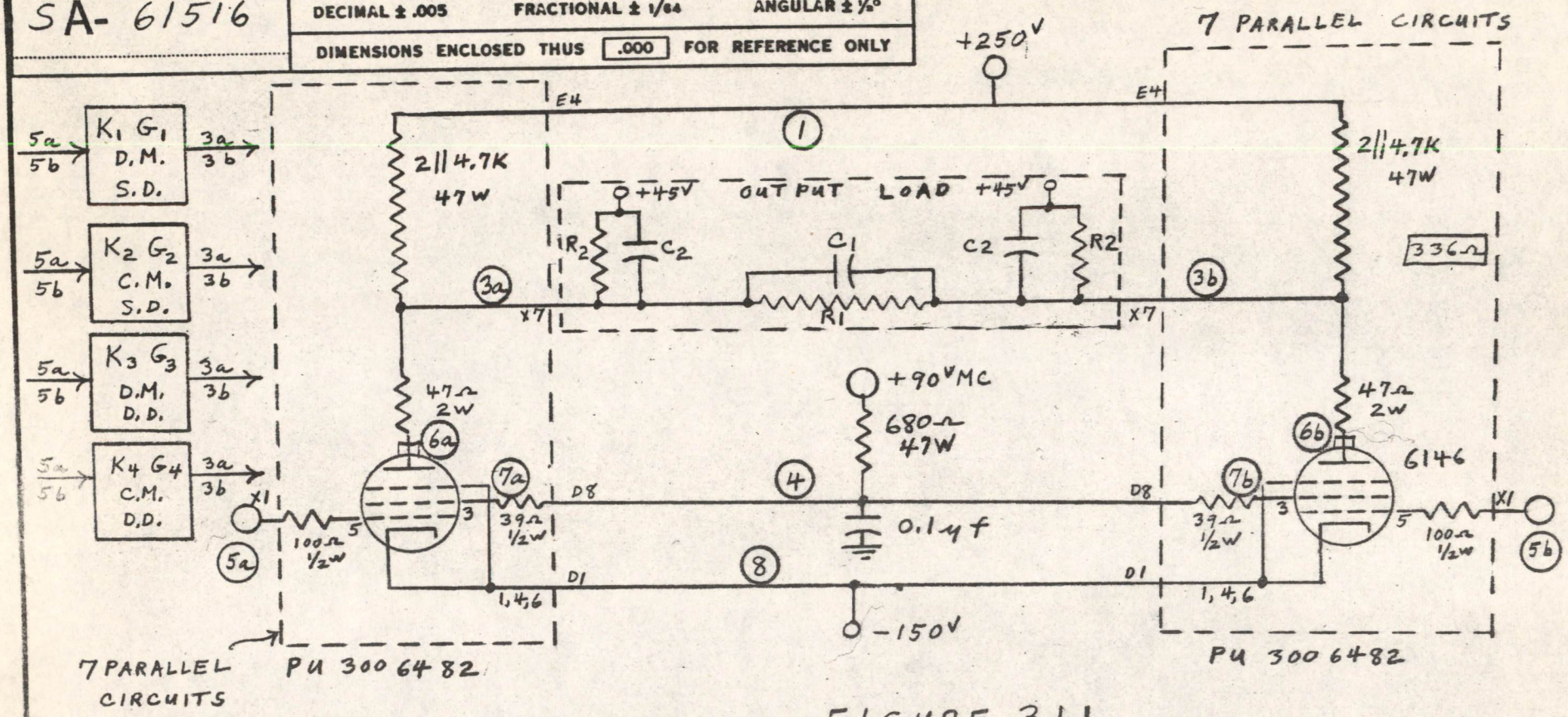


FIGURE 3.1.1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-3		3/4/56	HEZ
-2		7/2/56	HEZ
-1		24/10/56	HEZ

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

LINE DRIVER OUTPUT STAGE

SCALE:
DR. H E Zieman
ENG. H. E. Zieman
CK.
APPD.
SA- 61516

8M-7-54-Boston Blue Print

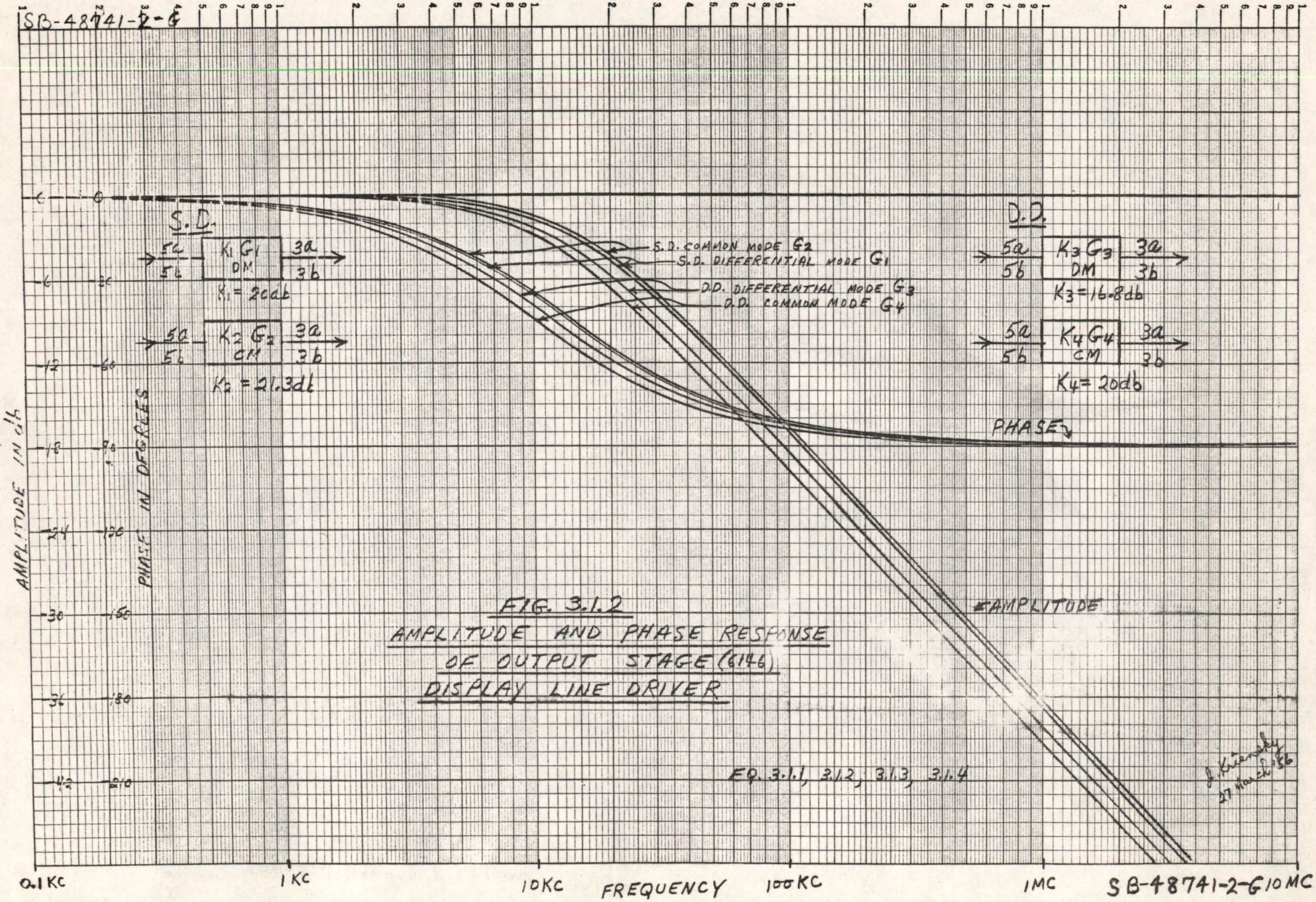


FIG. 3.1.2
AMPLITUDE AND PHASE RESPONSE
OF OUTPUT STAGE (6146)
DISPLAY LINE DRIVER

EQ. 3.1.1, 3.1.2, 3.1.3, 3.1.4

SI-4810.1-1-0

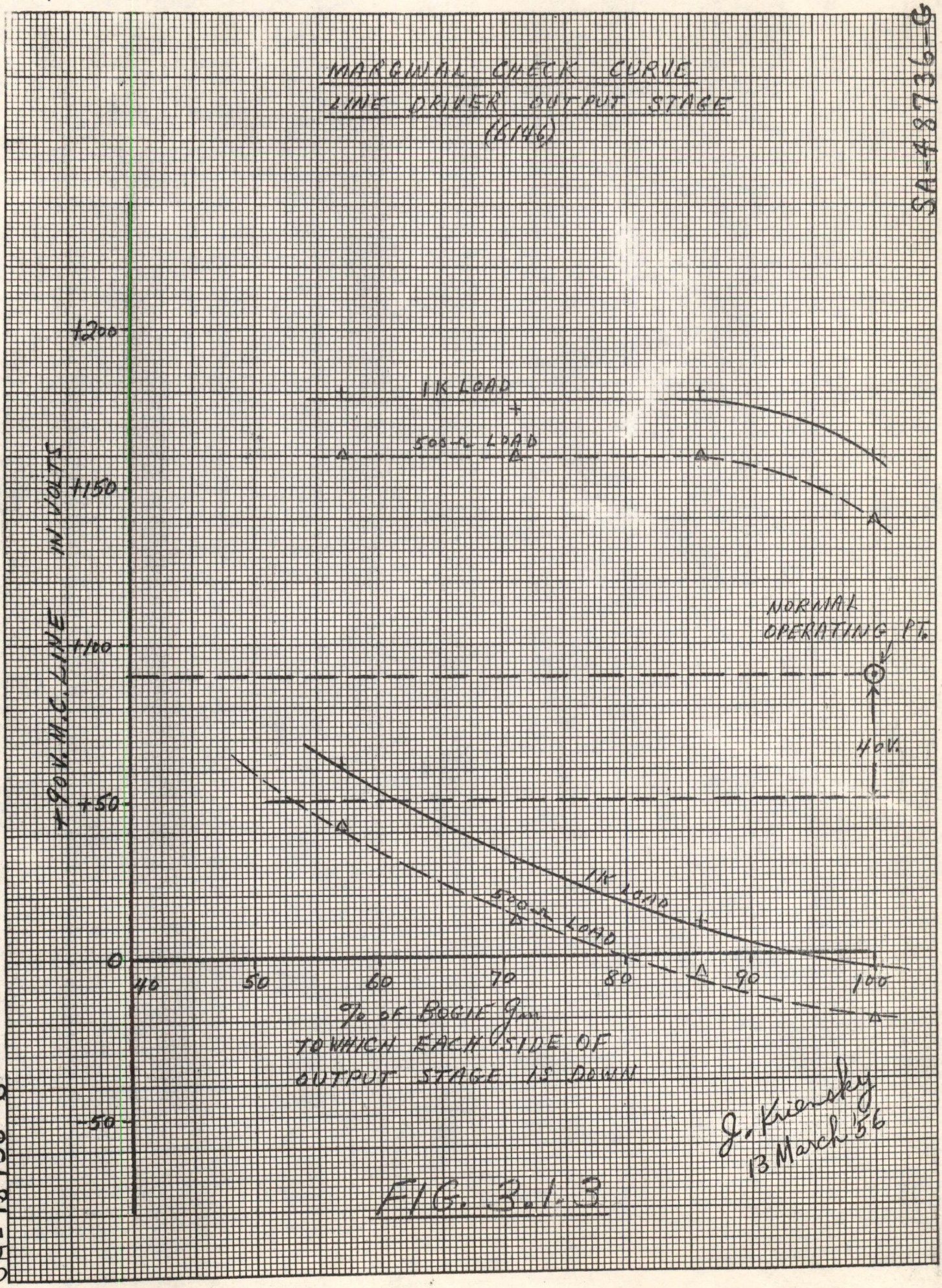


FIG. 3.1-3

SA- 61262

SEE CARD ASSEMBLY
300 6878
SLOT 47

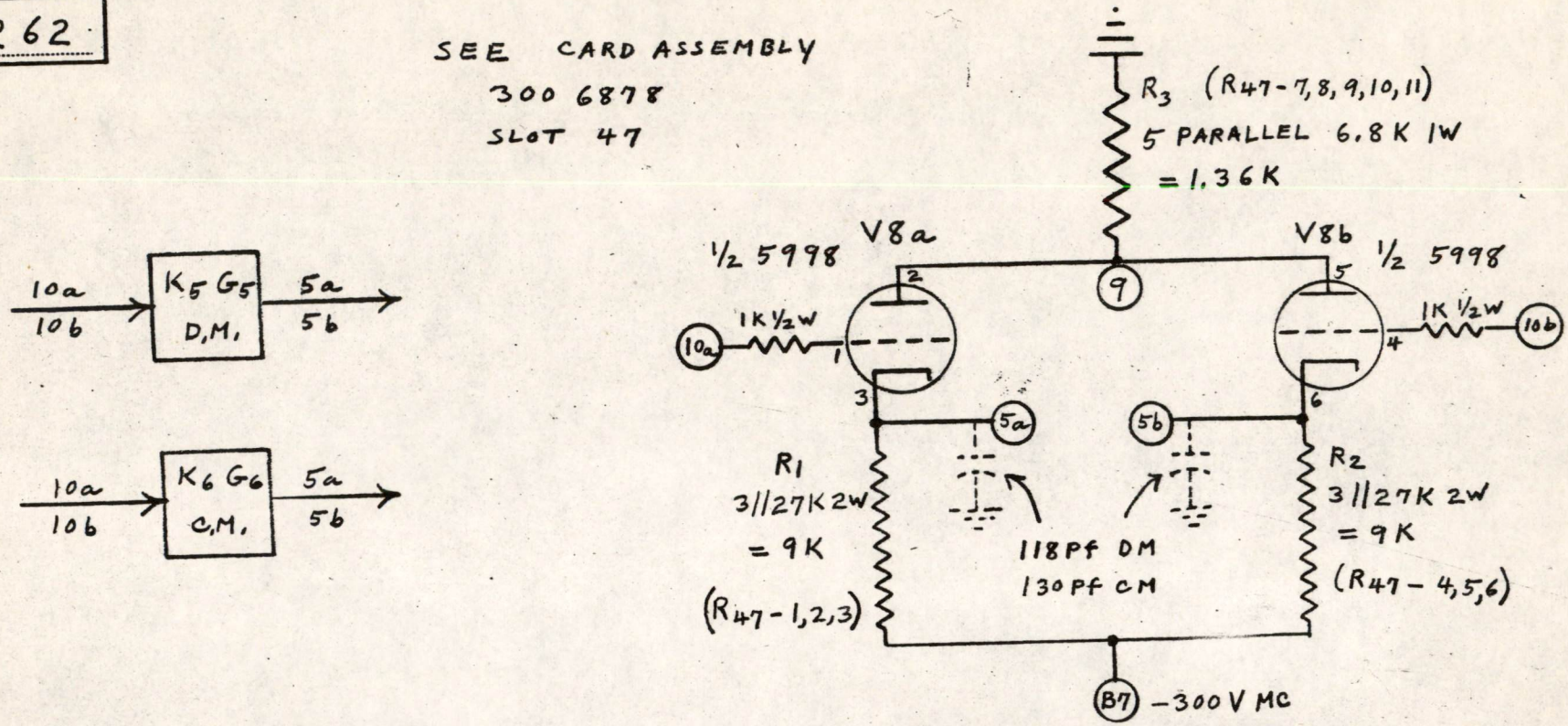


FIGURE 3.2.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/55	HE Z
-2		7/2/56	HE Z
-1		24/10/55	HE Z

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

OUTPUT DRIVER STAGE

SCALE:	DR. HE Zieman	SA- 61262
ENG. HE. Zieman	CK.	APPD.

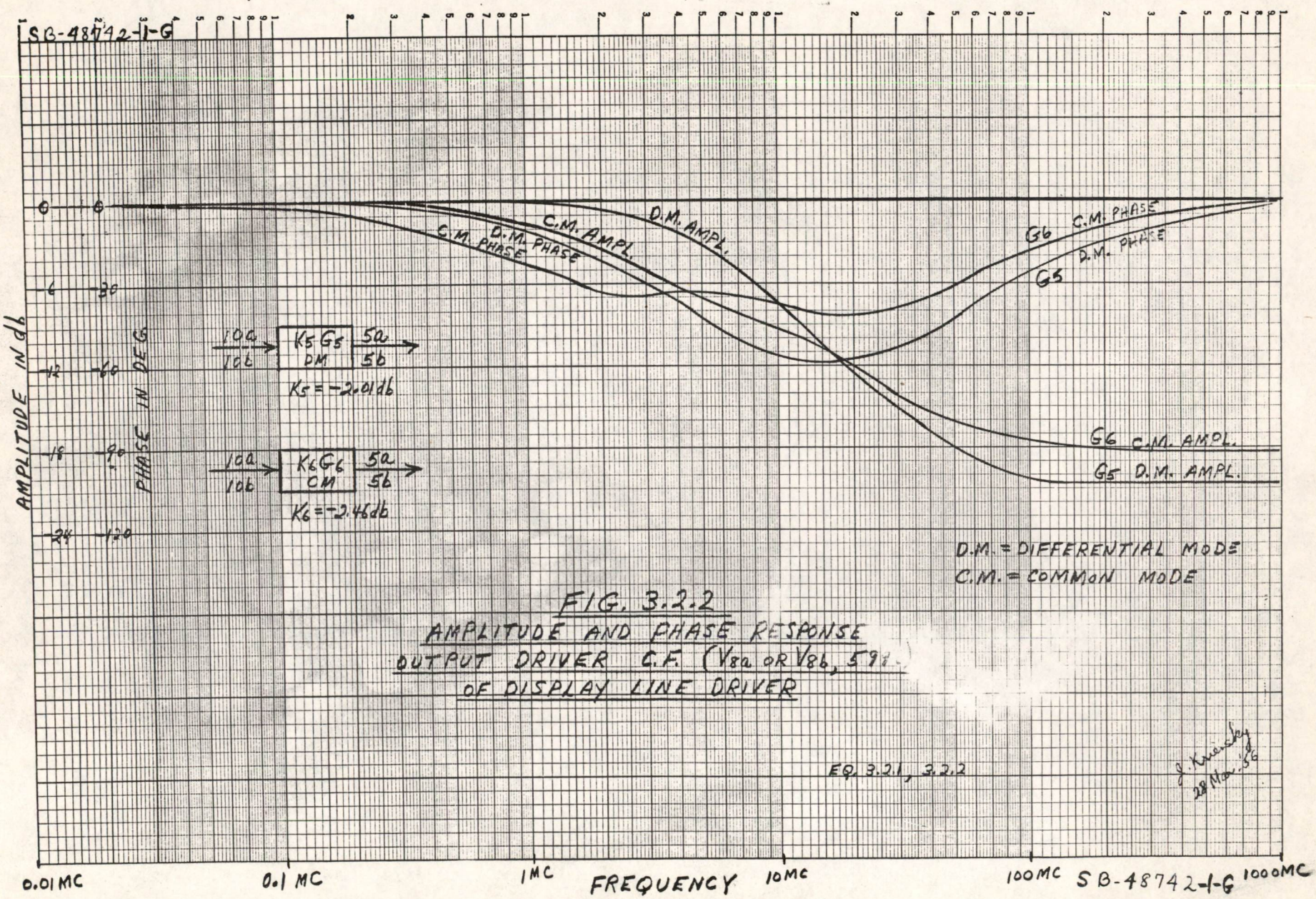


FIG. 3.2.2

AMPLITUDE AND PHASE RESPONSE
OUTPUT DRIVER C.F. (V_{8a} OR V_{8b}, 5 9...
OF DISPLAY LINE DRIVER

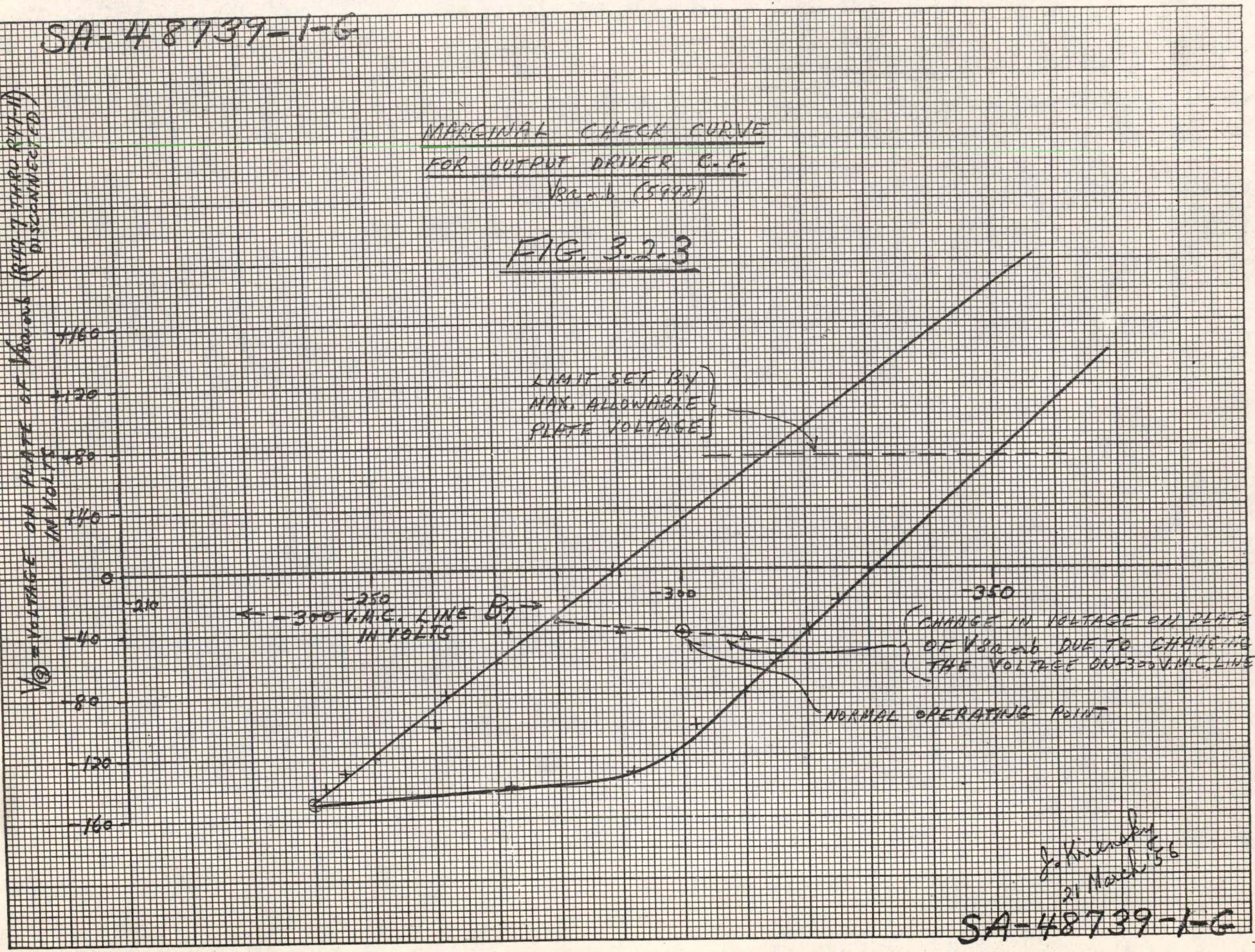
EQ. 3.2.1, 3.2.2

J. Kwiatkowski
28 Mar. 56

SA-48739-1-G

MARGINAL CHECK CURVE
FOR OUTPUT DRIVER C.E.
$V_{B2a,b}$ (5998)

FIG. 3.2-3

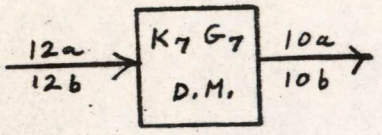


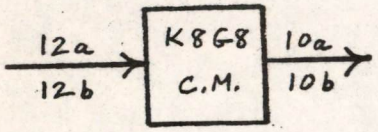
J. Kinsella
21 March '56

SA-48739-1-G

SA-65907

SEE CARD ASSEMBLY
3006876
SLOT 42





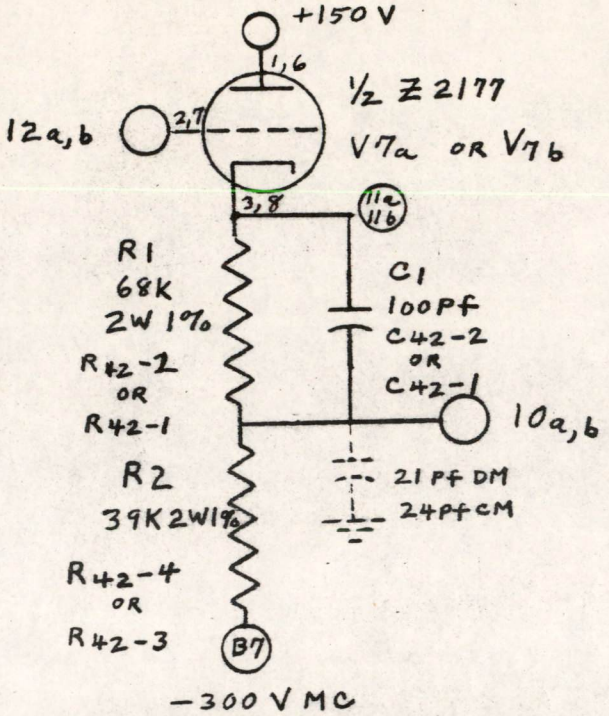


FIGURE 3.3.1

											APPD.
											DATE
											CN#
-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	CHG.	

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BUFFER CATHODE FOLLOWER

SCALE:	DR. H E Zieman	SA-65907
ENG. H. E. Zieman	CK.	APPD.

SB-48743-I-G

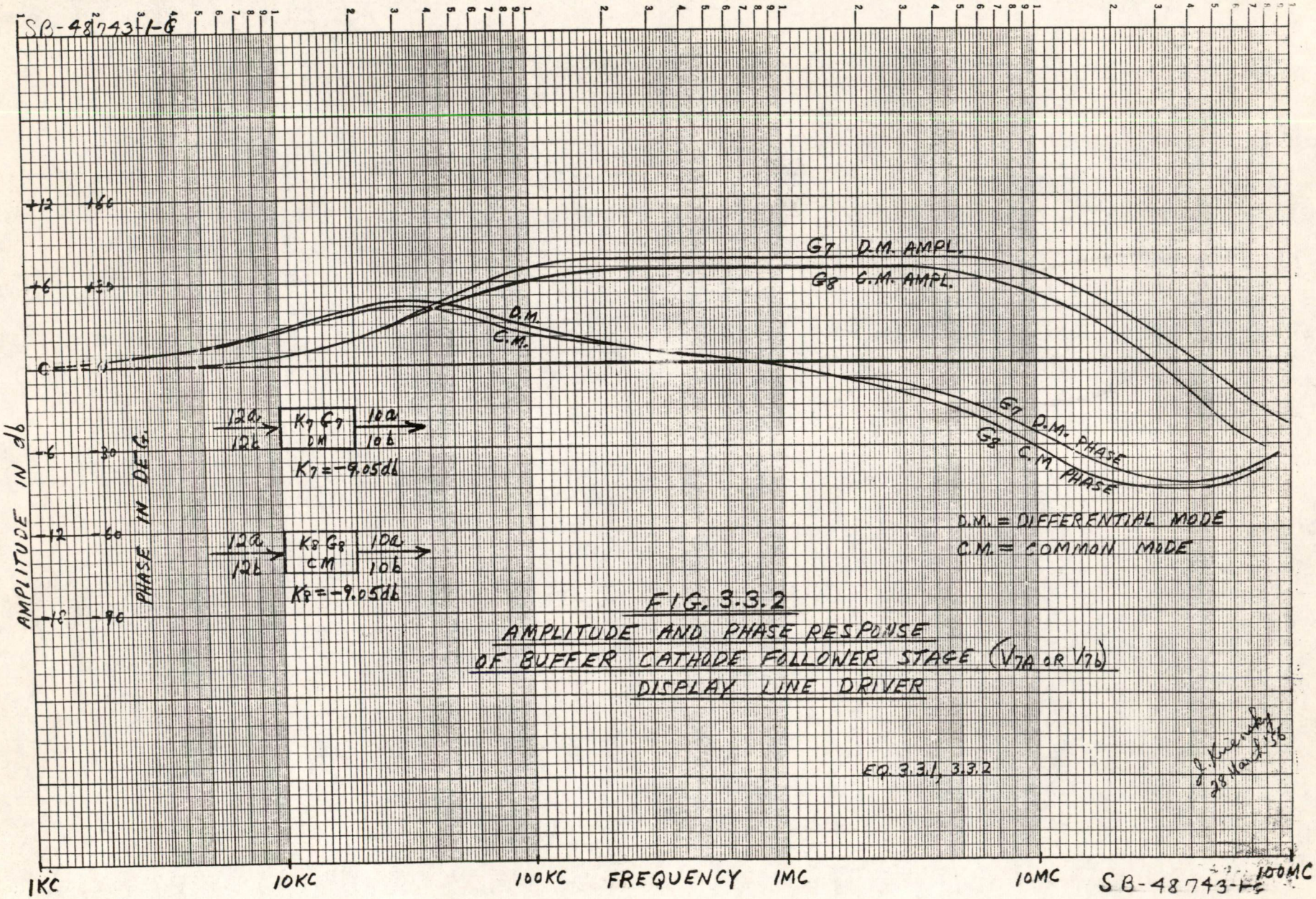


FIG. 3.3.2

AMPLITUDE AND PHASE RESPONSE
OF BUFFER CATHODE FOLLOWER STAGE (V_{7A} OR V_{7b})
DISPLAY LINE DRIVER

EQ. 3.3.1, 3.3.2

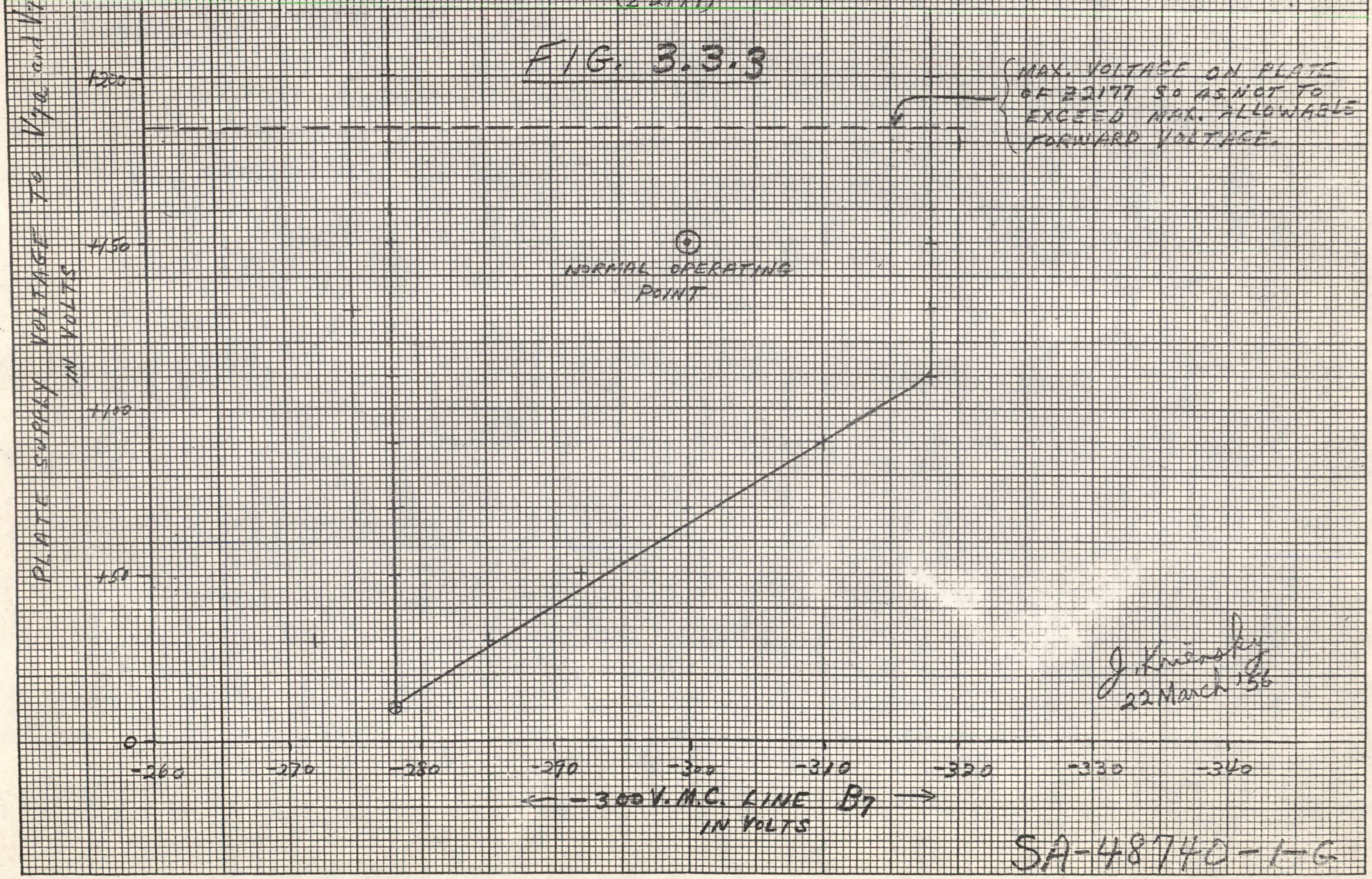
J. Kiernan
28 March 56

SB-48743-I-G

SA-48740-1-G

MARGINAL CHECK CURVE
FOR BUFFER C.E., V_{grab}
(Z2177)

FIG. 3.3.3



J. Kriendler
22 March '56

SA-48740-1-G

SA-61708

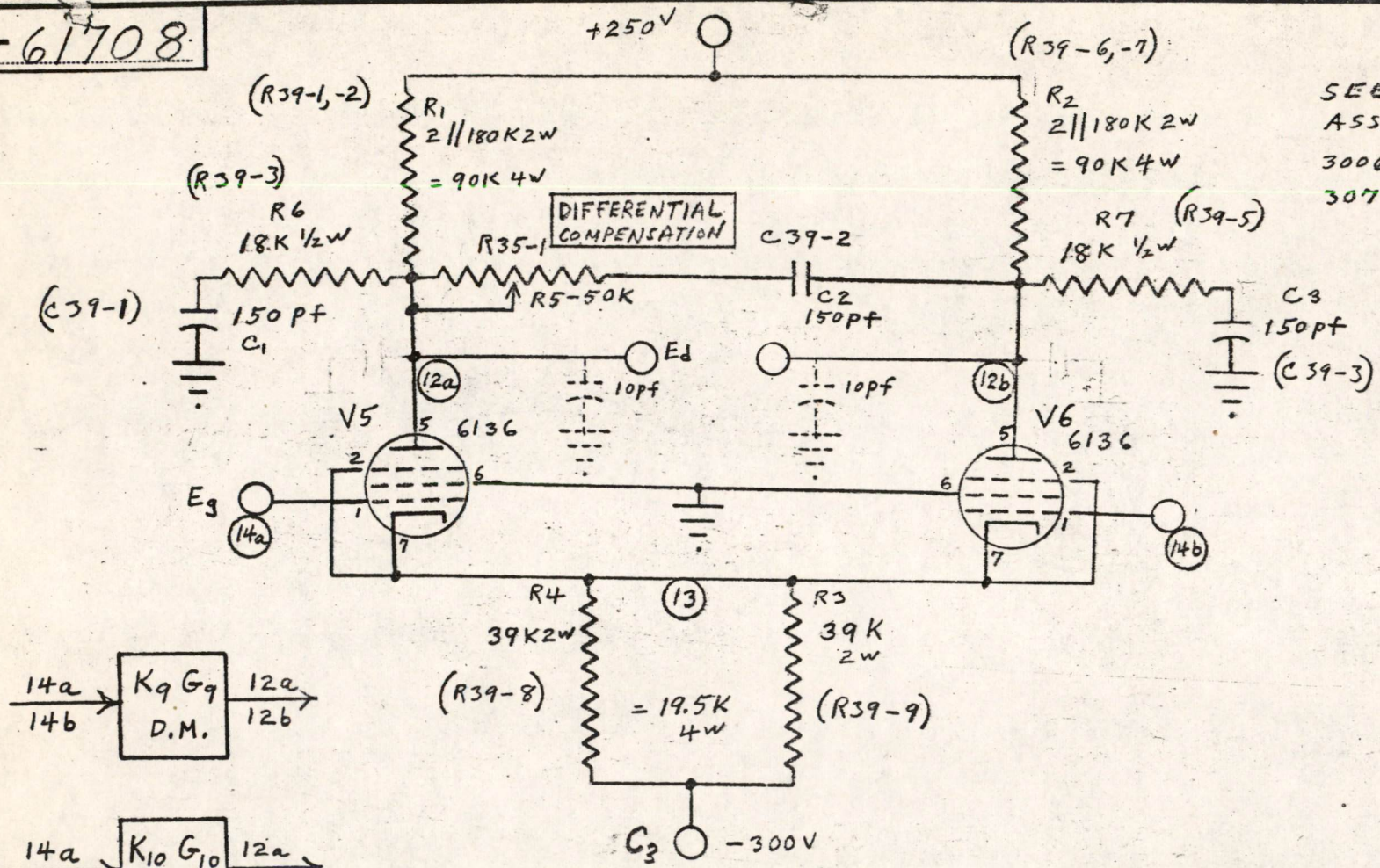


FIGURE 3.4.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/56	HE Z
-2		7/2/56	HE Z
-1		24/10/55	HEZ

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DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO.

DIFFERENTIAL AMPLIFIER

SCALE:	DR. H E Zieman	
ENG. H E Zieman	CK.	APPD.

SA-61708

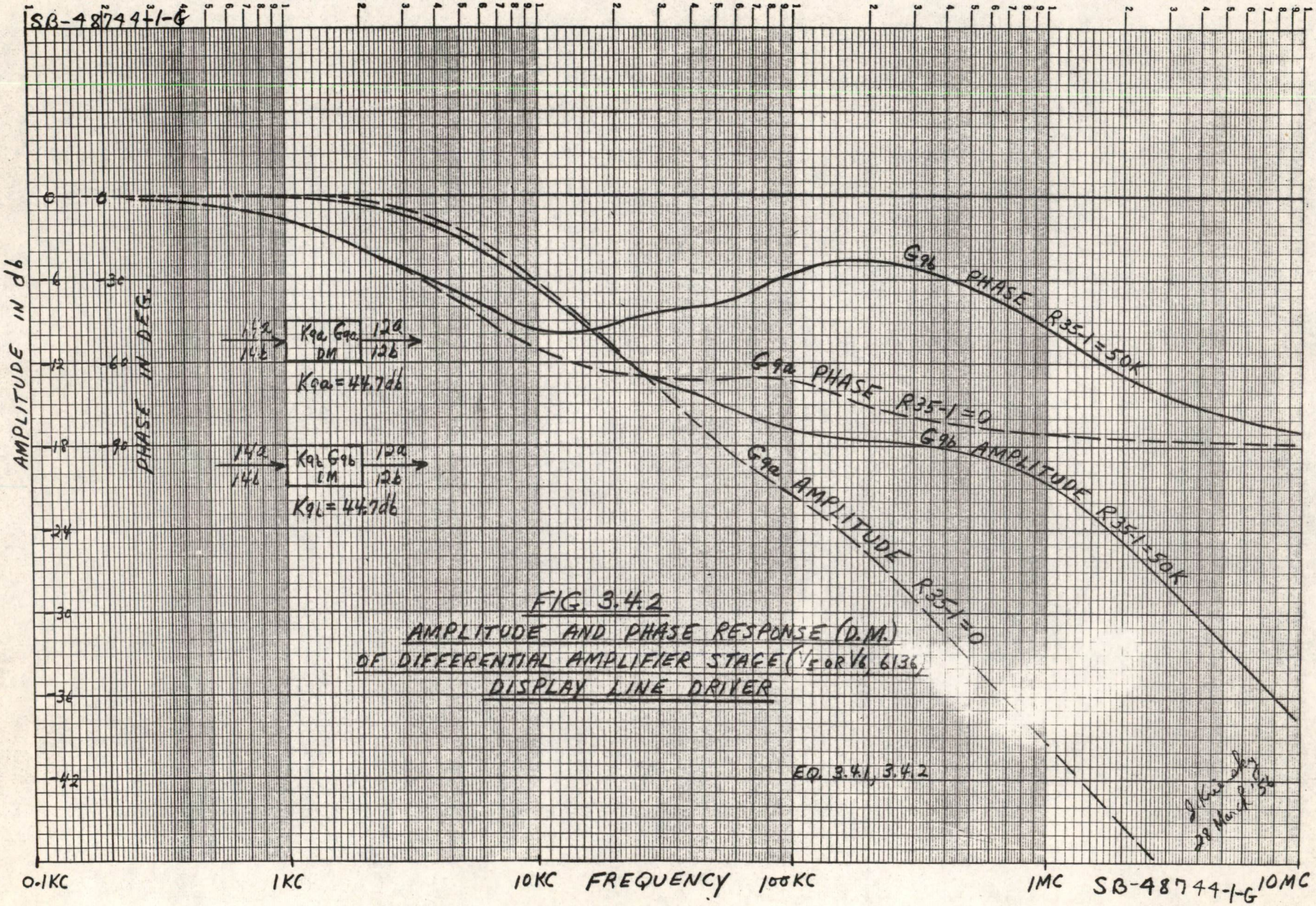


FIG. 3.4.2
AMPLITUDE AND PHASE RESPONSE (D.M.)
OF DIFFERENTIAL AMPLIFIER STAGE (1/5 OR V6, 6136)
DISPLAY LINE DRIVER

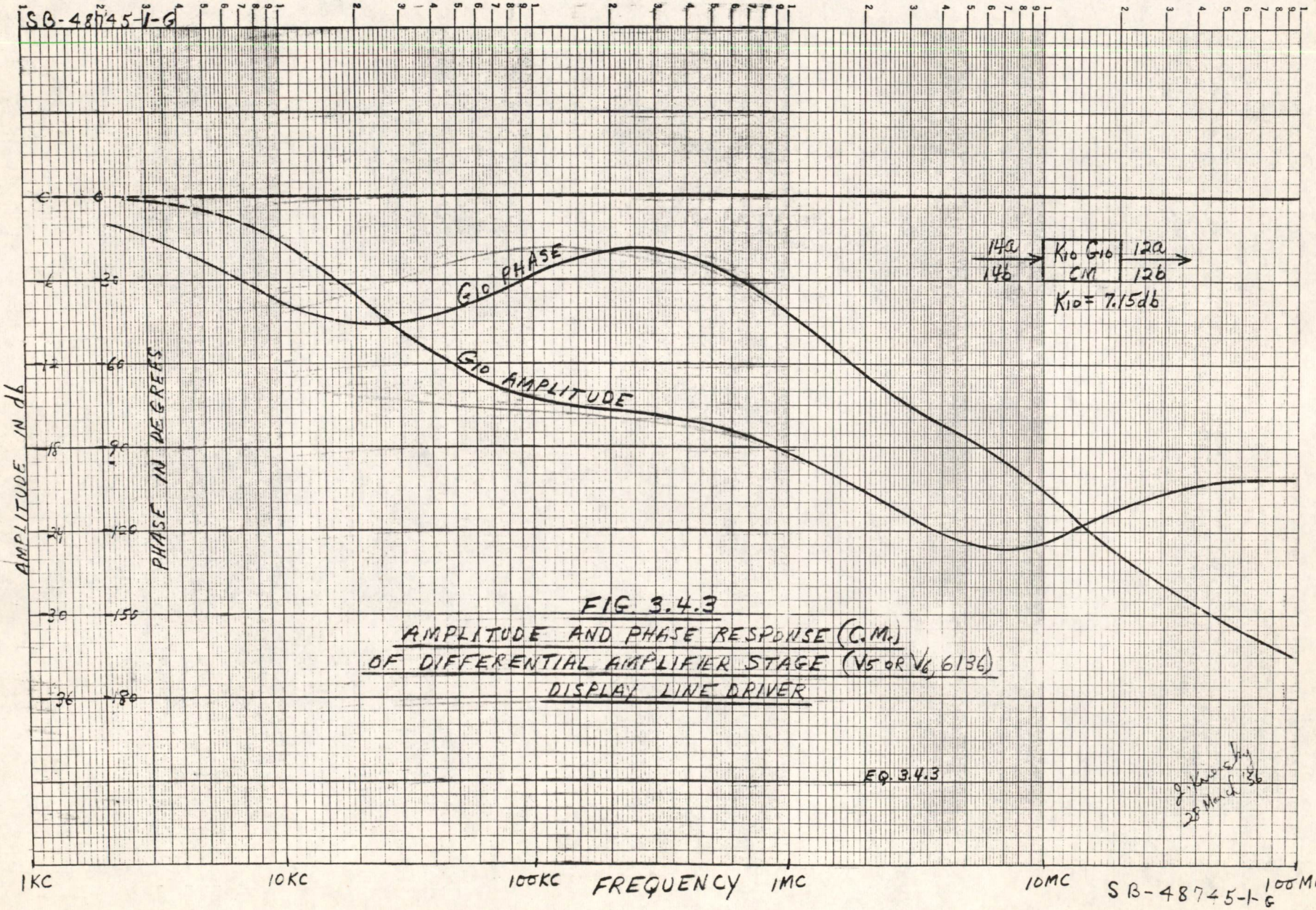


FIG. 3.4.3

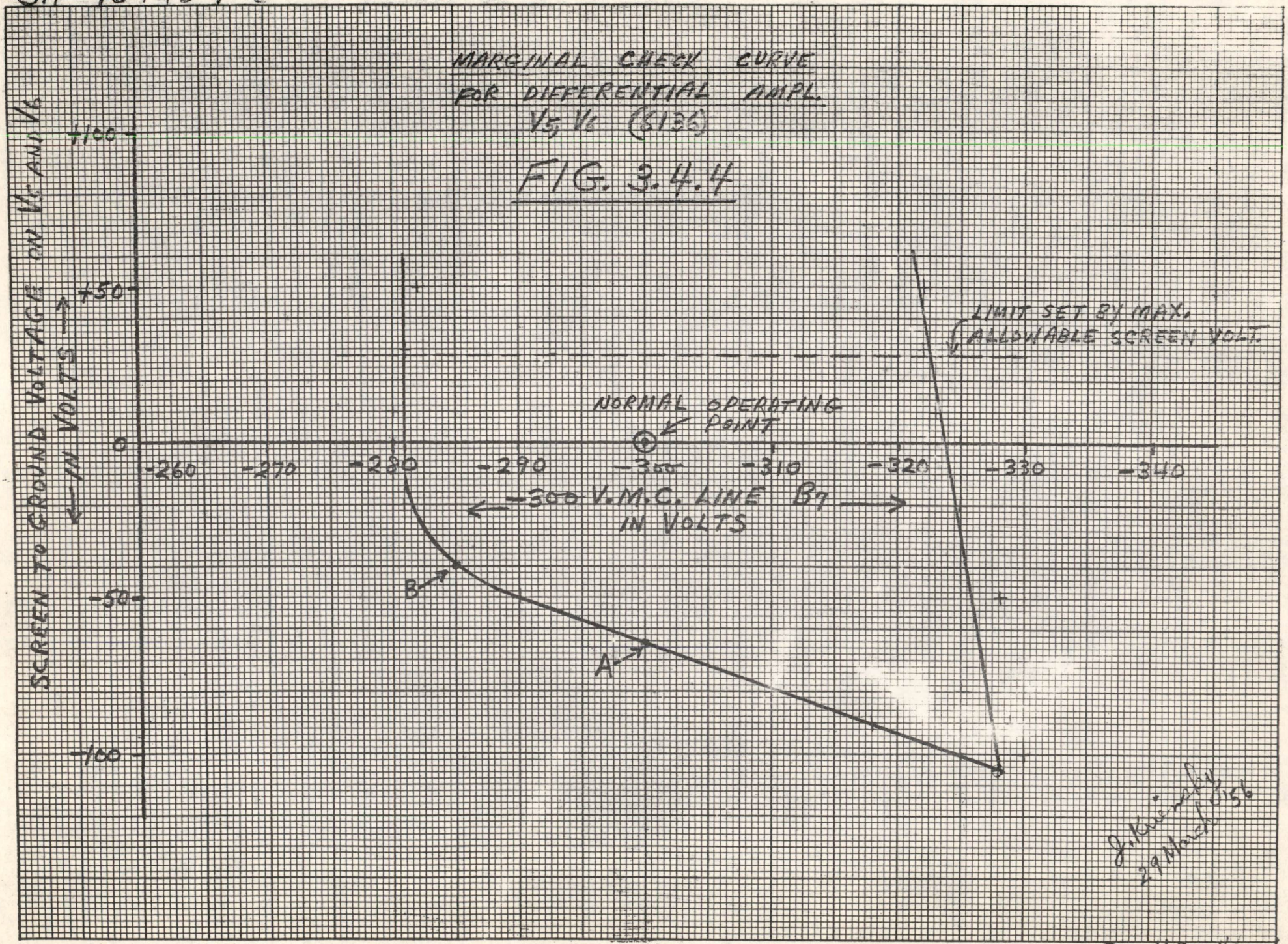
AMPLITUDE AND PHASE RESPONSE (C.M.)
OF DIFFERENTIAL AMPLIFIER STAGE (V_5 OR V_6, 6136)
DISPLAY LINE DRIVER

EQ. 3.4.3

SA-48746-1-G

MARGINAL CHECK CURVE FOR DIFFERENTIAL AMPL. V5 V6 (6136)

FIG. 3.4.4



J. Kaczmarek
29 March 65

SA-48746-1-G

SA- 61709

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY

PLATE LOAD CIRCUIT
ON CARD ASSEMBLIES
3006880 (27,30)
3070187 (35)

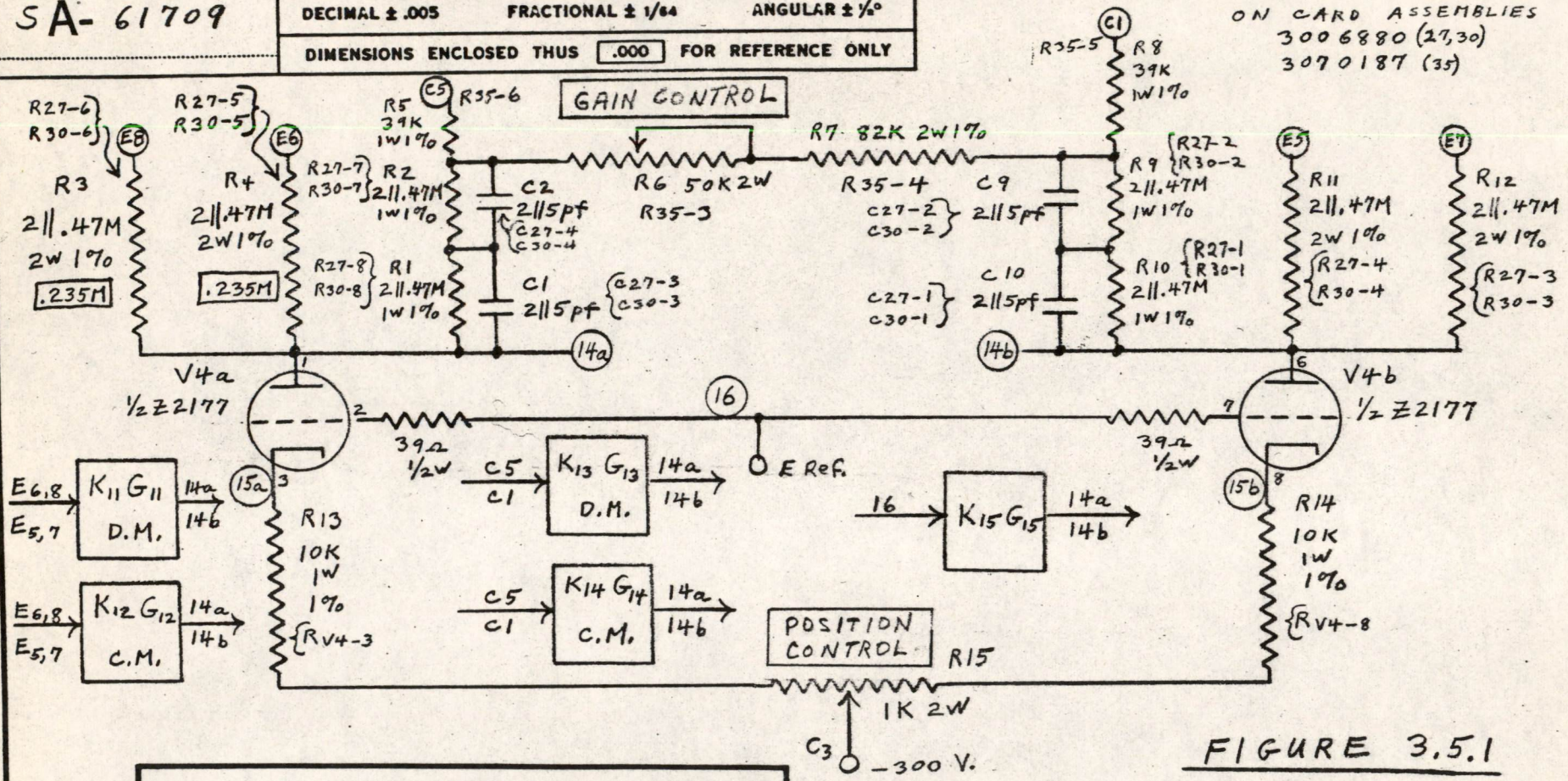


FIGURE 3.5.1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
−3		13/4/55	HE Z
−2		7/2/56	HEZ
−1		25/10/55	HEZ

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

INPUT CIRCUIT TO DIFFERENTIAL AMPLIFIER

SCALE:	DR. H E Ziemann	SA- 61709
ENG. H E Ziemann	CK.	APPD.

8M-7-54-Boston Blue Print

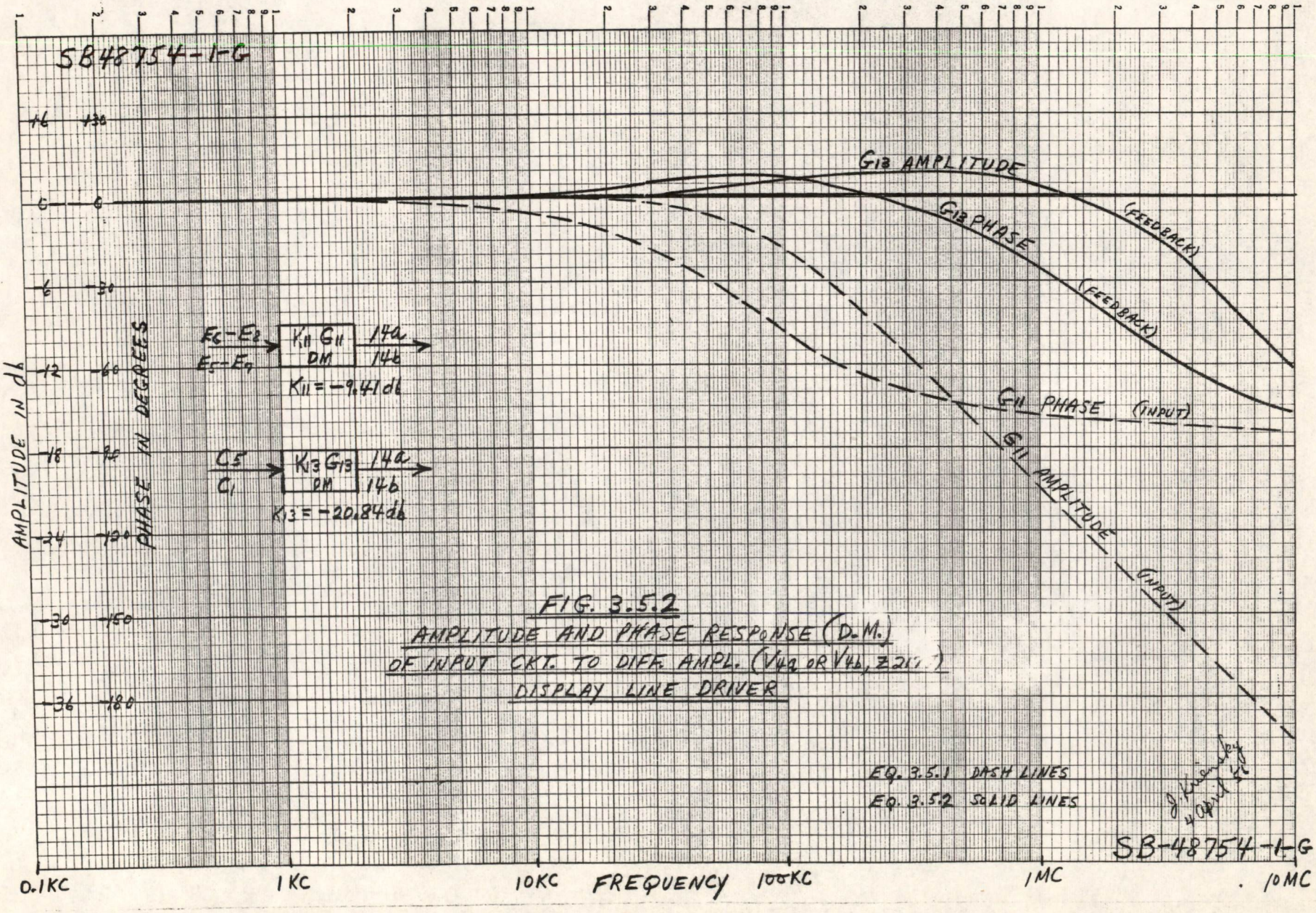


FIG. 3.5.2

AMPLITUDE AND PHASE RESPONSE (D.M.)
OF INPUT CKT. TO DIFF. AMPL. (V_{4a} OR V_{4b}, Z21)
DISPLAY LINE DRIVER

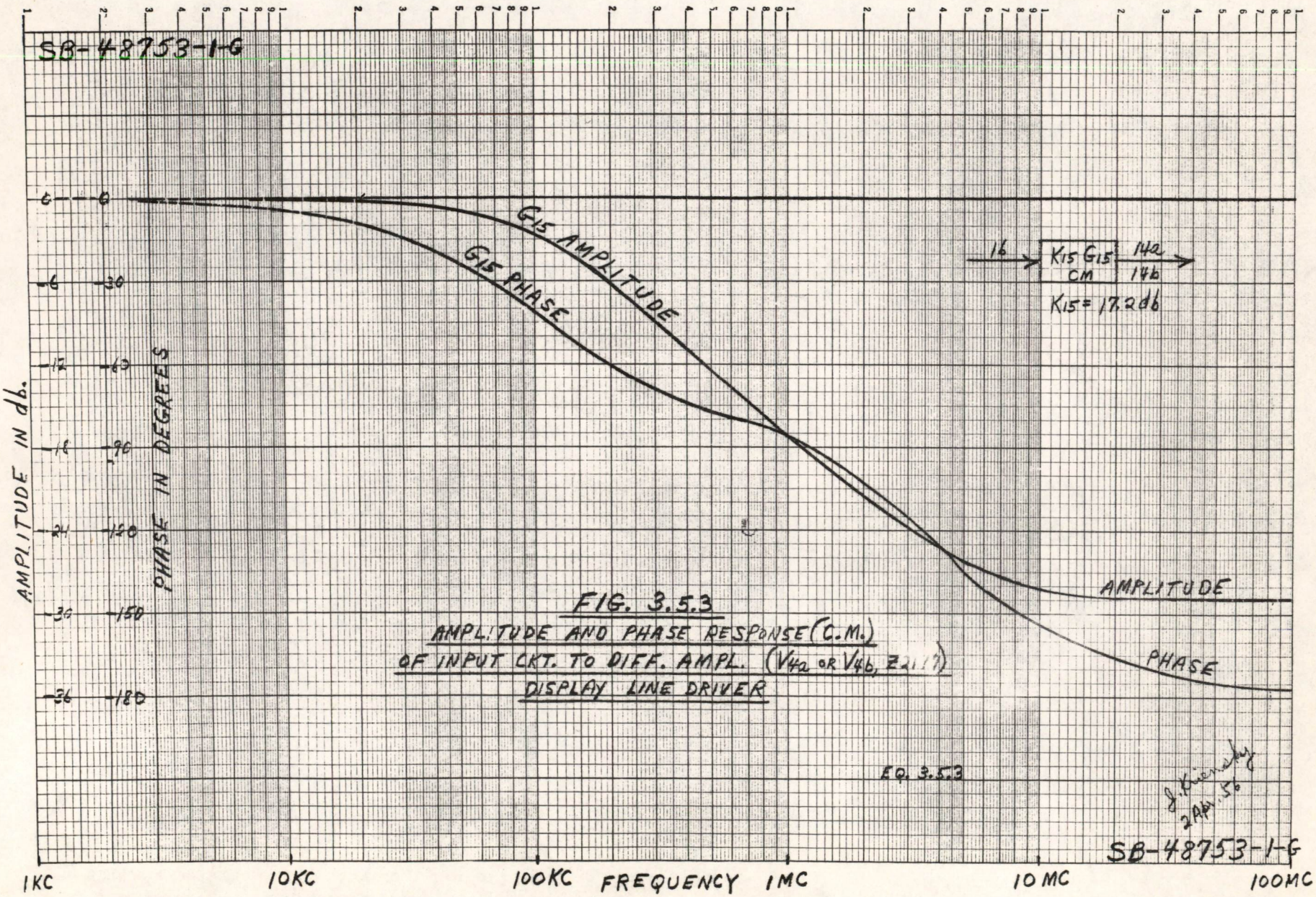


FIG. 3.5.3

AMPLITUDE AND PHASE RESPONSE (C.M.) OF INPUT CKT. TO DIFF. AMPL. (V_{14a} OR V_{14b}, Z21 ?) DISPLAY LINE DRIVER

EQ. 3.5.3

J. Kinsley 2 APR. 58

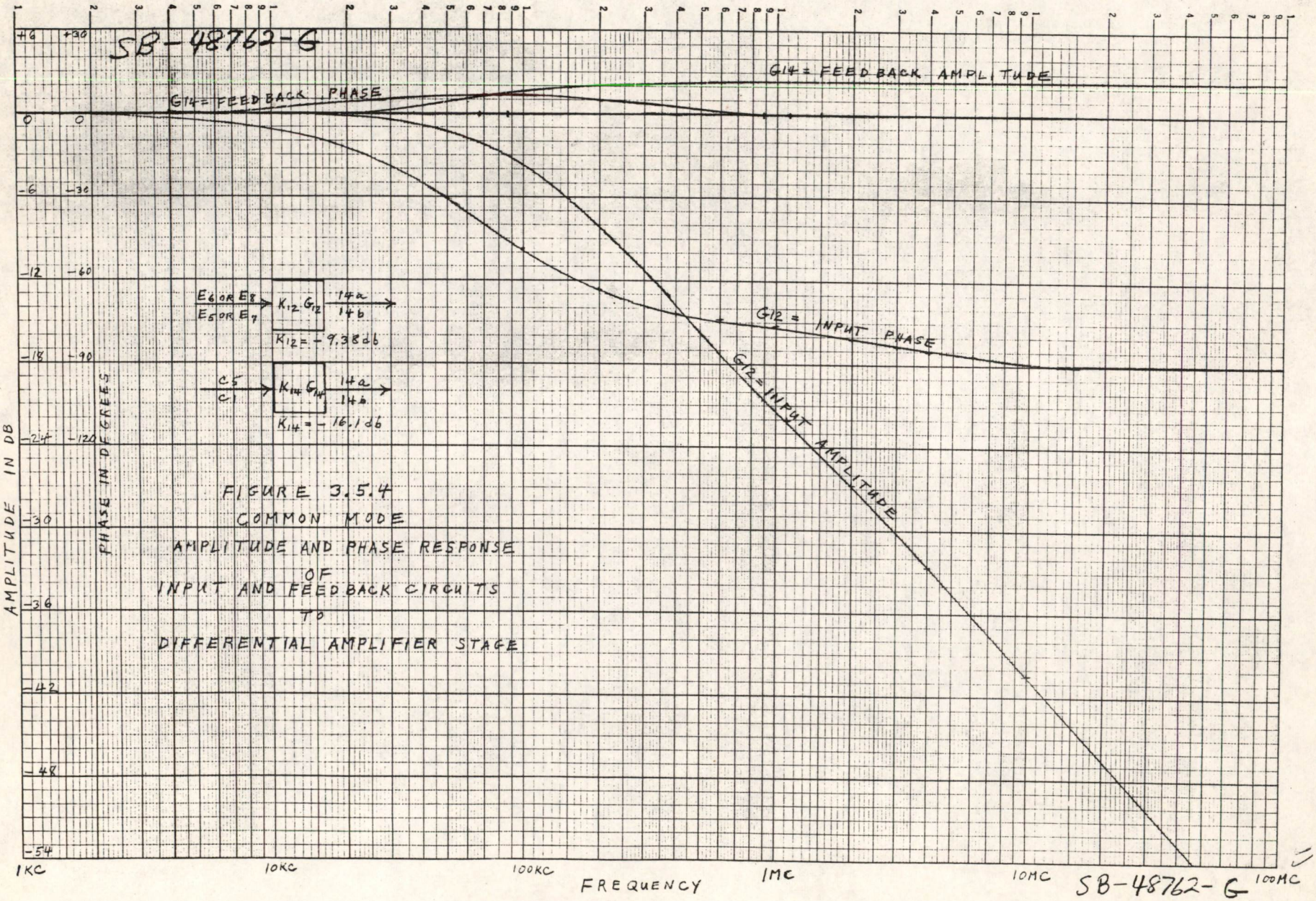
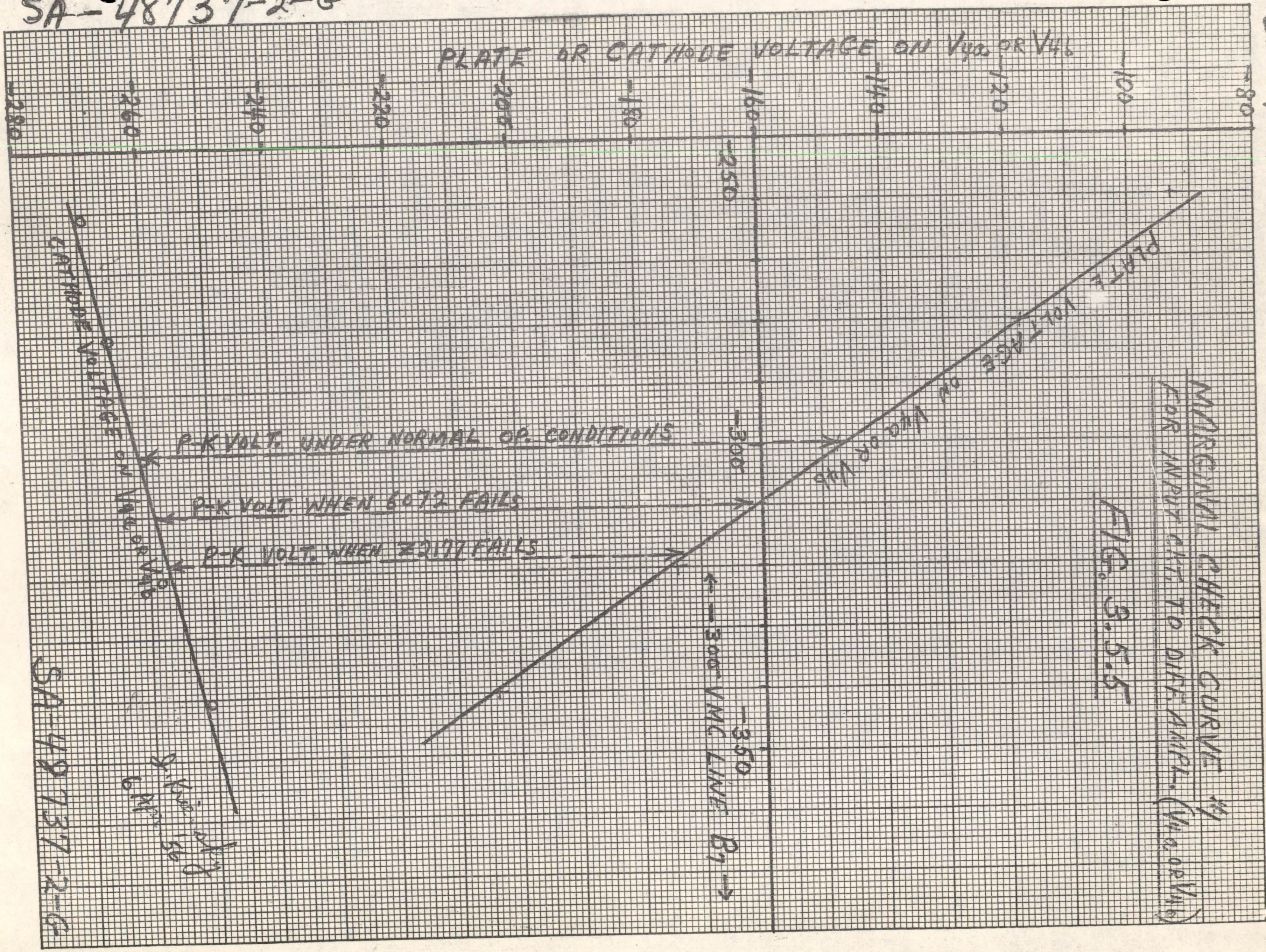


FIGURE 3.5.4
COMMON MODE
AMPLITUDE AND PHASE RESPONSE
OF
INPUT AND FEEDBACK CIRCUITS
TO
DIFFERENTIAL AMPLIFIER STAGE

SA-48737-2-G

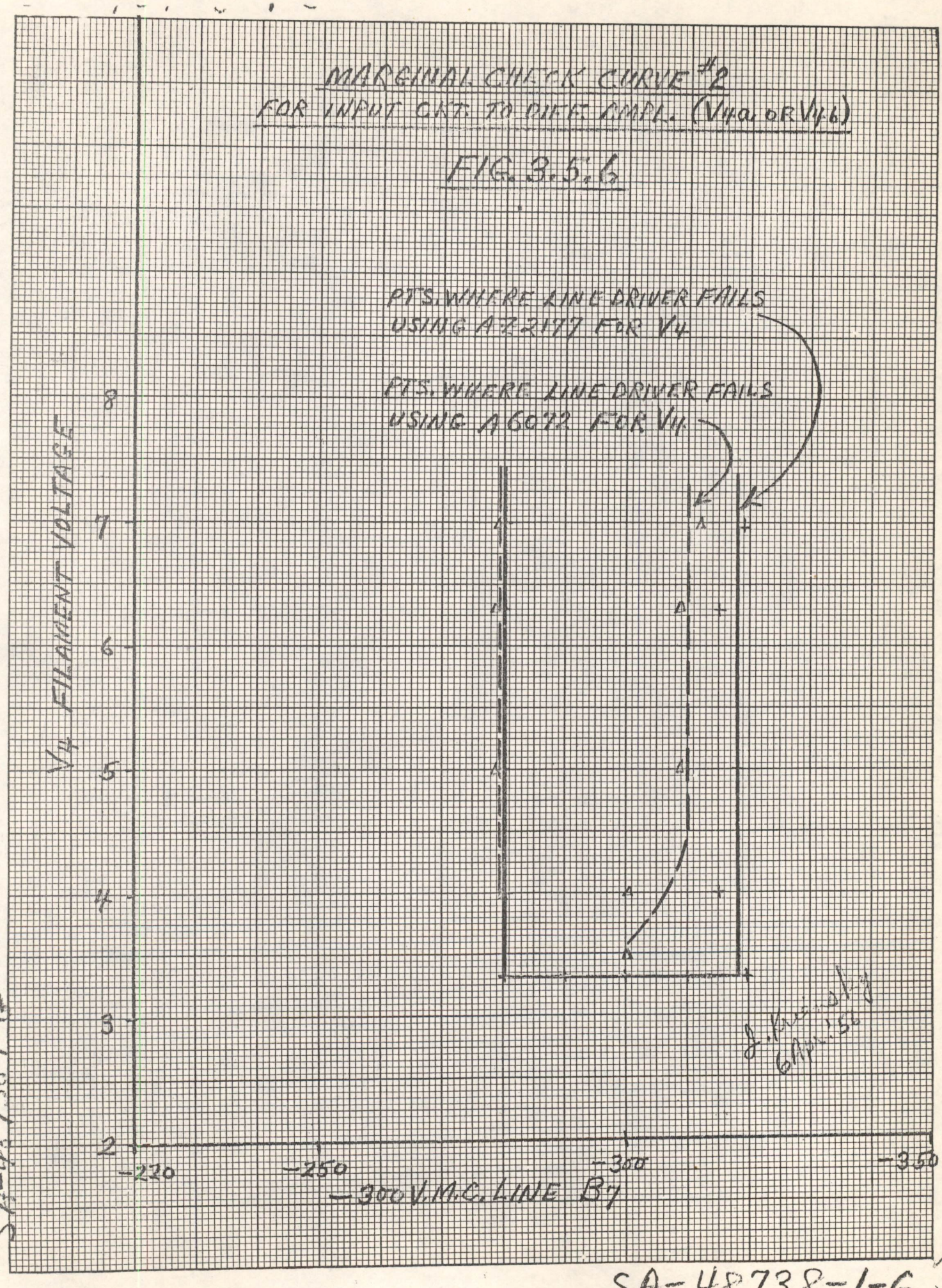


MARGINAL CHECK CURVE #7
FOR INPUT CKT. TO DIFF. AMPL. (V_{42} OR V_{46})

FIG. 3.5.5

MARGINAL CHECK CURVE #2
FOR INPUT CKT. TO DIFF. AMPL. (V_{7A} OR V_{7B})

FIG. 3.5.6



SA-48738-1-G

SA-48738-1-G

SA-61710

SEE CARD ASSEMBLY
300 6870
SLOT 19

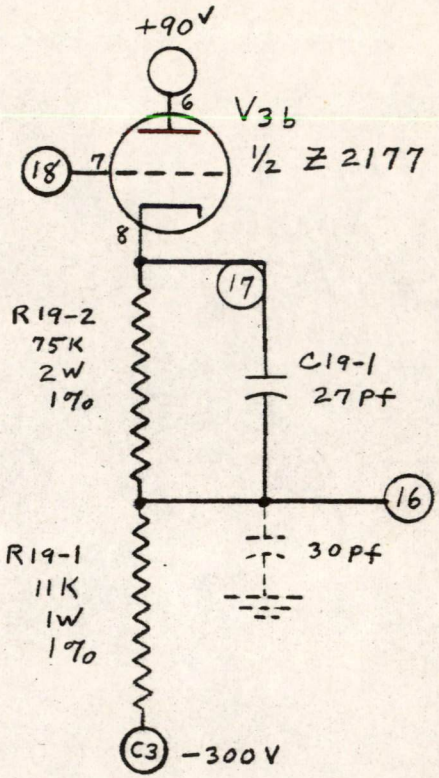


FIGURE 3.6.1

							HEZ	HEZ	HEZ		APPD.
							13/4/56	7/2/56	24/10/55		DATE
											CN#
-10	-9	-8	-7	-6	-5	-4	-3	-2	-1		CHG.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

REFERENCE DRIVER

SCALE:	DR. H.E. Zieman	SA-61710
ENG. H.E. Zieman	CK.	APPD.

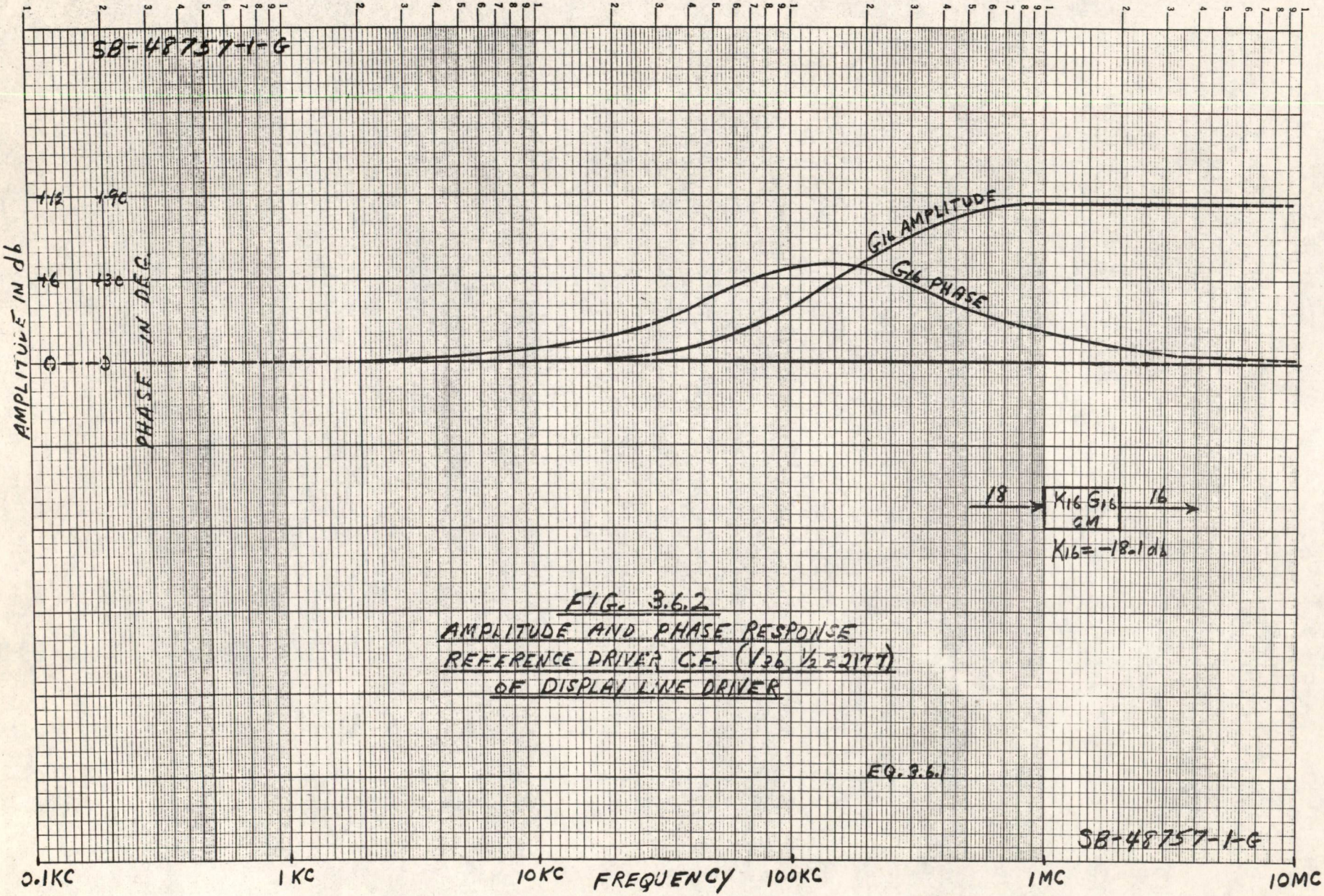


FIG. 3.6.2
AMPLITUDE AND PHASE RESPONSE
REFERENCE DRIVER C.F. (V_{36} ½ E2177)
OF DISPLAY LINE DRIVER

EQ. 3.6.1

SA-48735-G

MARGINAL CHECK CURVE FOR REFERENCE DRIVER C.F. V_{36} ($\frac{1}{2}$ Z 2177)

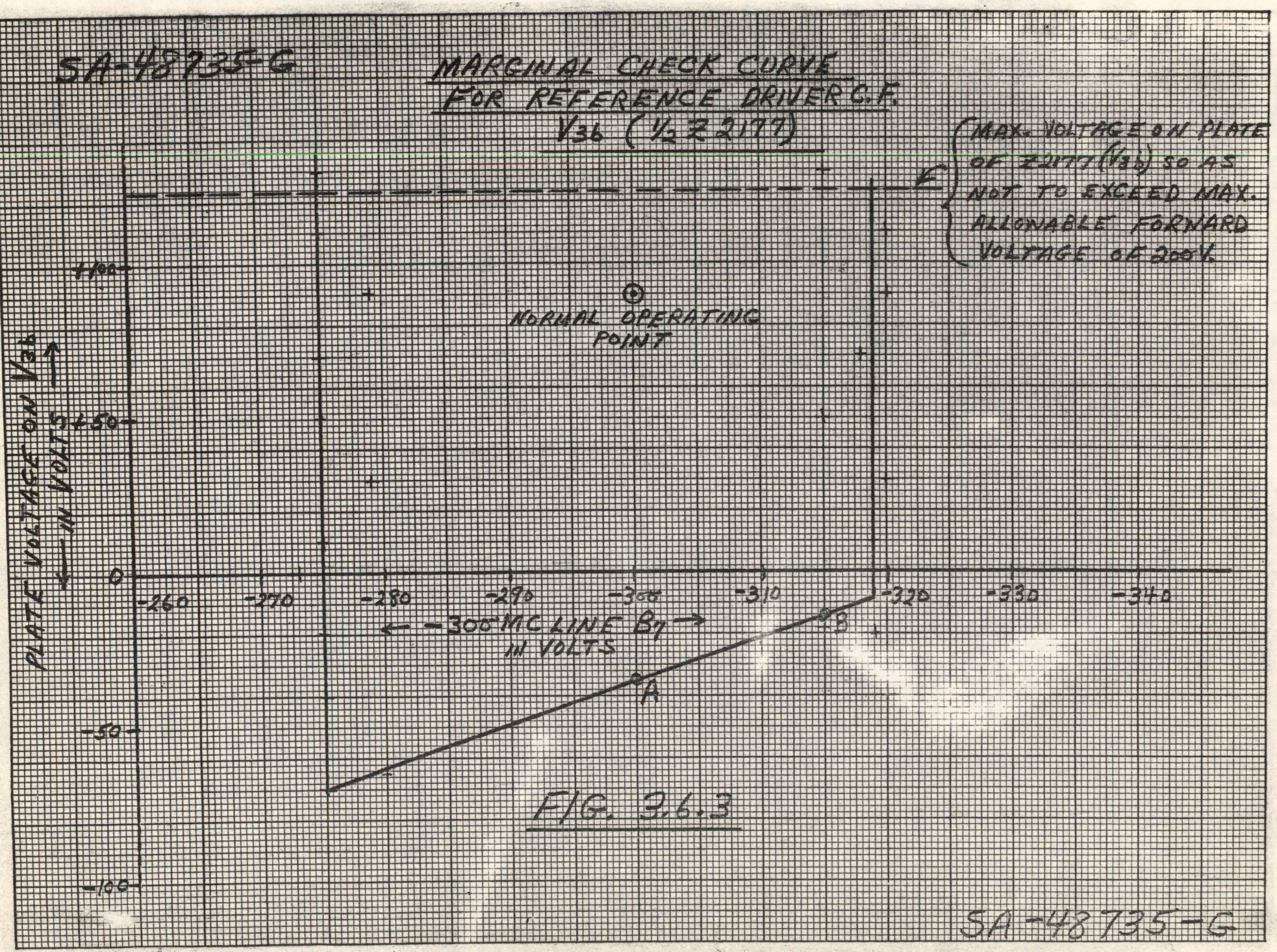
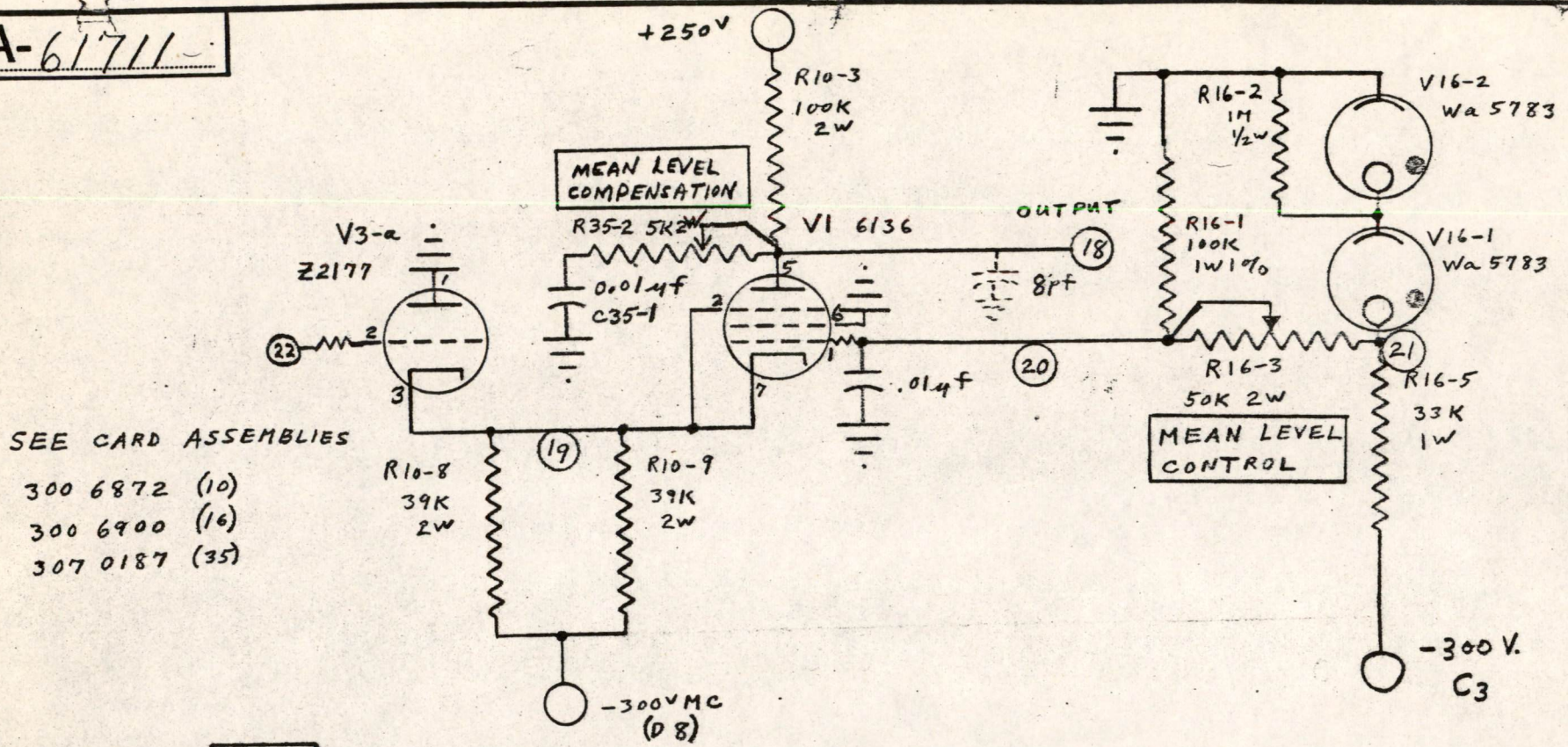


FIG. 3.6.3

SA-48735-G

SA-61711



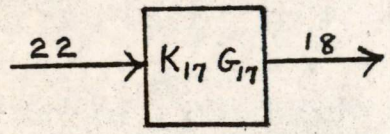


FIGURE 3.7.1

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3		13/4/56	HEZ
-2		7/2/56	HE2
-1		24/10/55	HE3

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REFERENCE AMPLIFIER

SCALE:	DR. H.E. Ziman	SA-61711
ENG. H.E. Ziman	CK.	APPD.

V

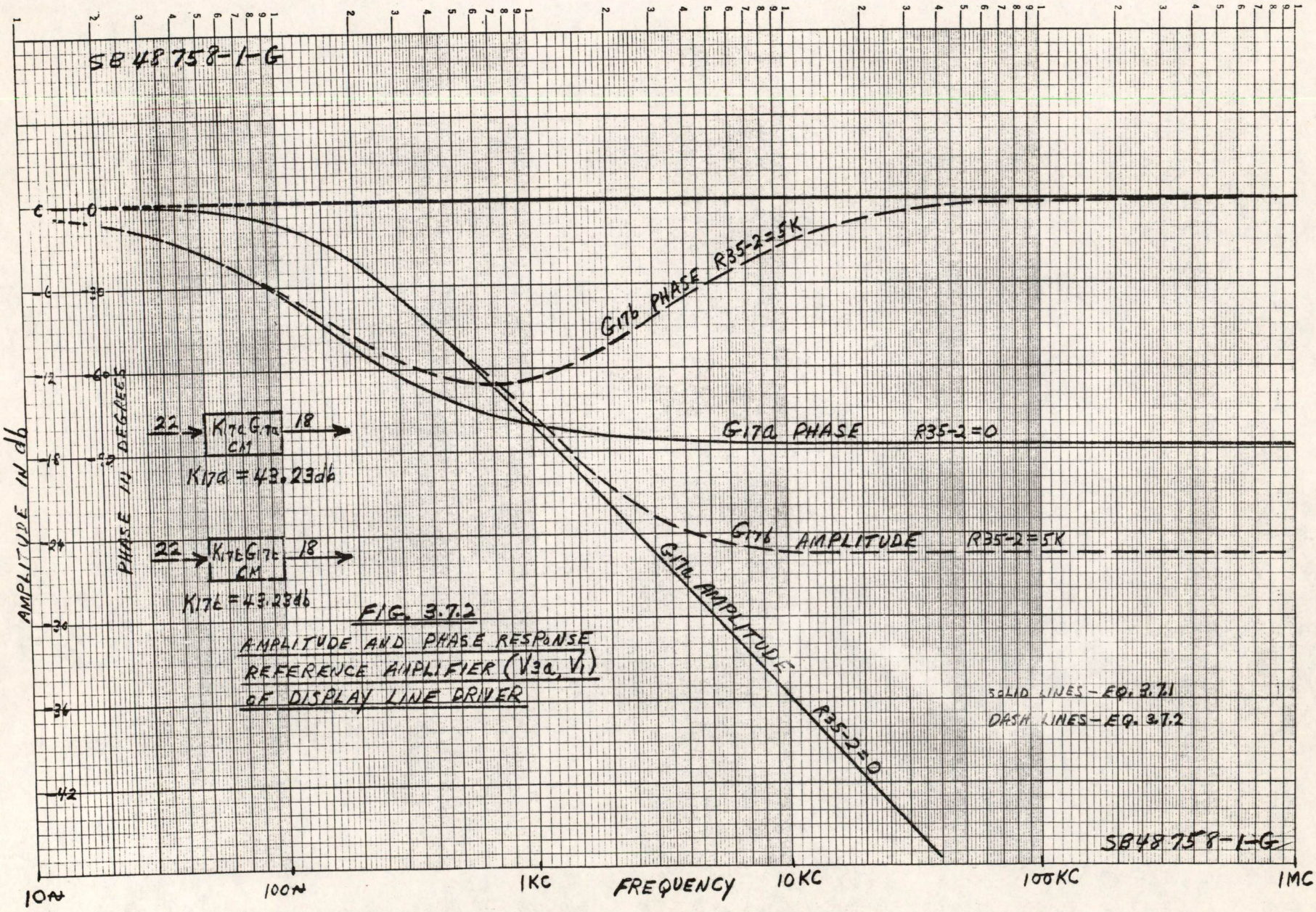


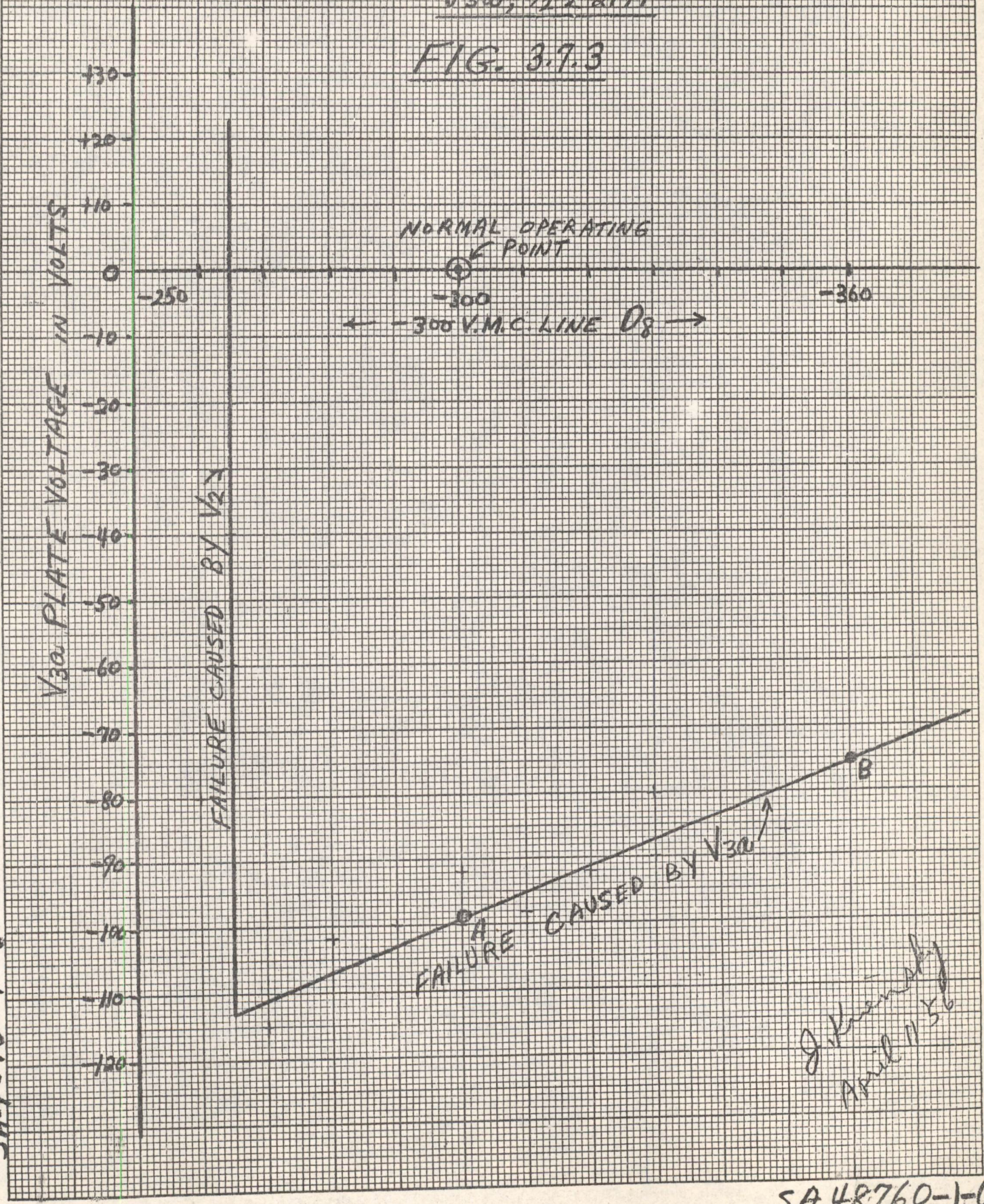
FIG. 3.7.2

AMPLITUDE AND PHASE RESPONSE REFERENCE AMPLIFIER (V_{3a}, V_1) OF DISPLAY LINE DRIVER

SA-48760-1-G

MARGINAL CHECK CURVE
PART OF REFERENCE AMPL.
V_{3a}, ½ Z 2171

FIG. 3.7.3



J. Kuenstler
April 11 56

SA-48760-1-G

SA 48760-1-G

SA-65906

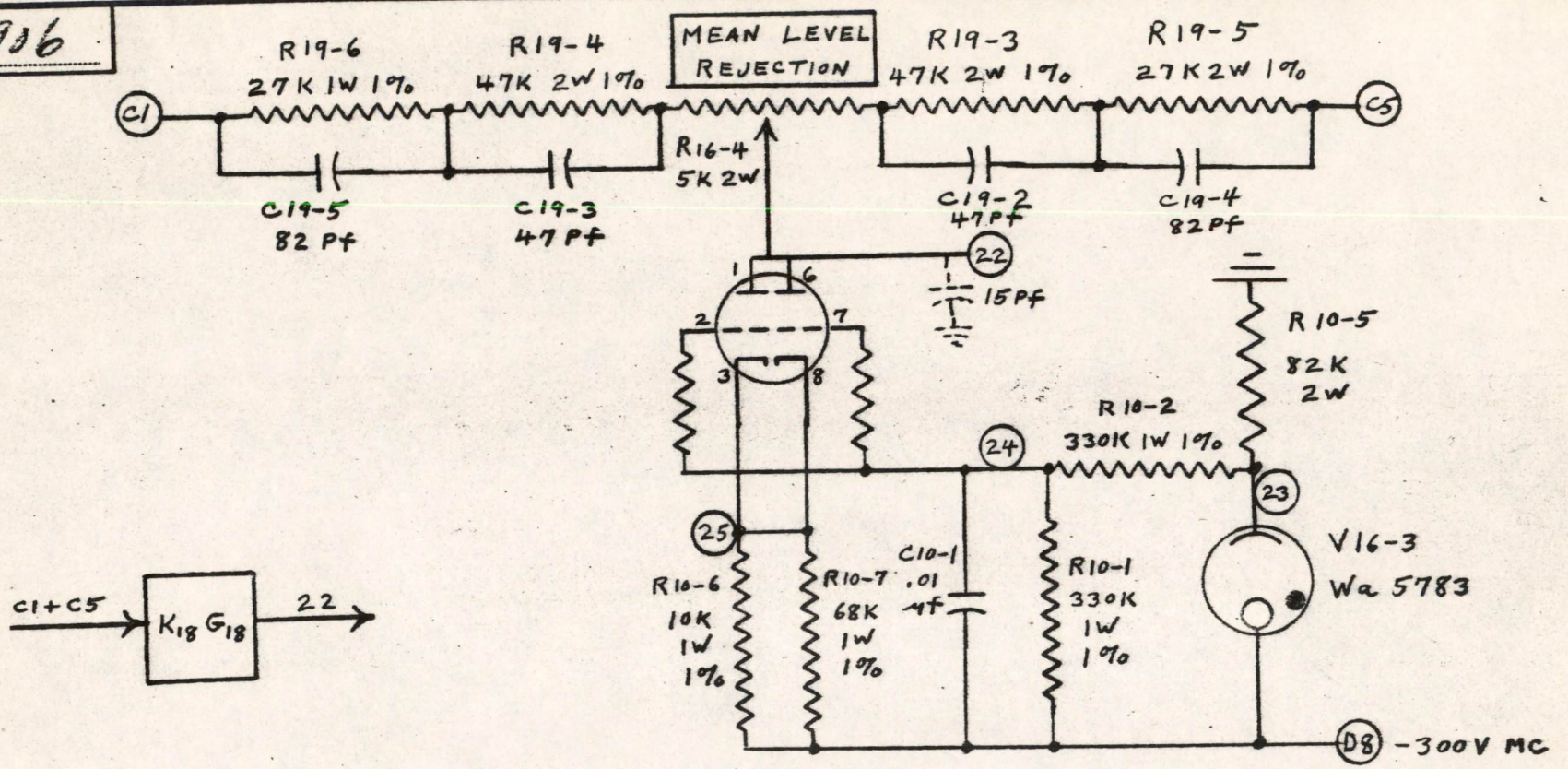


FIGURE 3.8.1

											APPD.
											DATE
											CN#
10	9	8	7	6	5	4	3	2	1		CHG.

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INPUT CIRCUIT TO REFERENCE AMPLIFIER

SCALE:	DR. H E Zieman	SA-65906
ENG. H.E. Zieman	CK.	APPD.

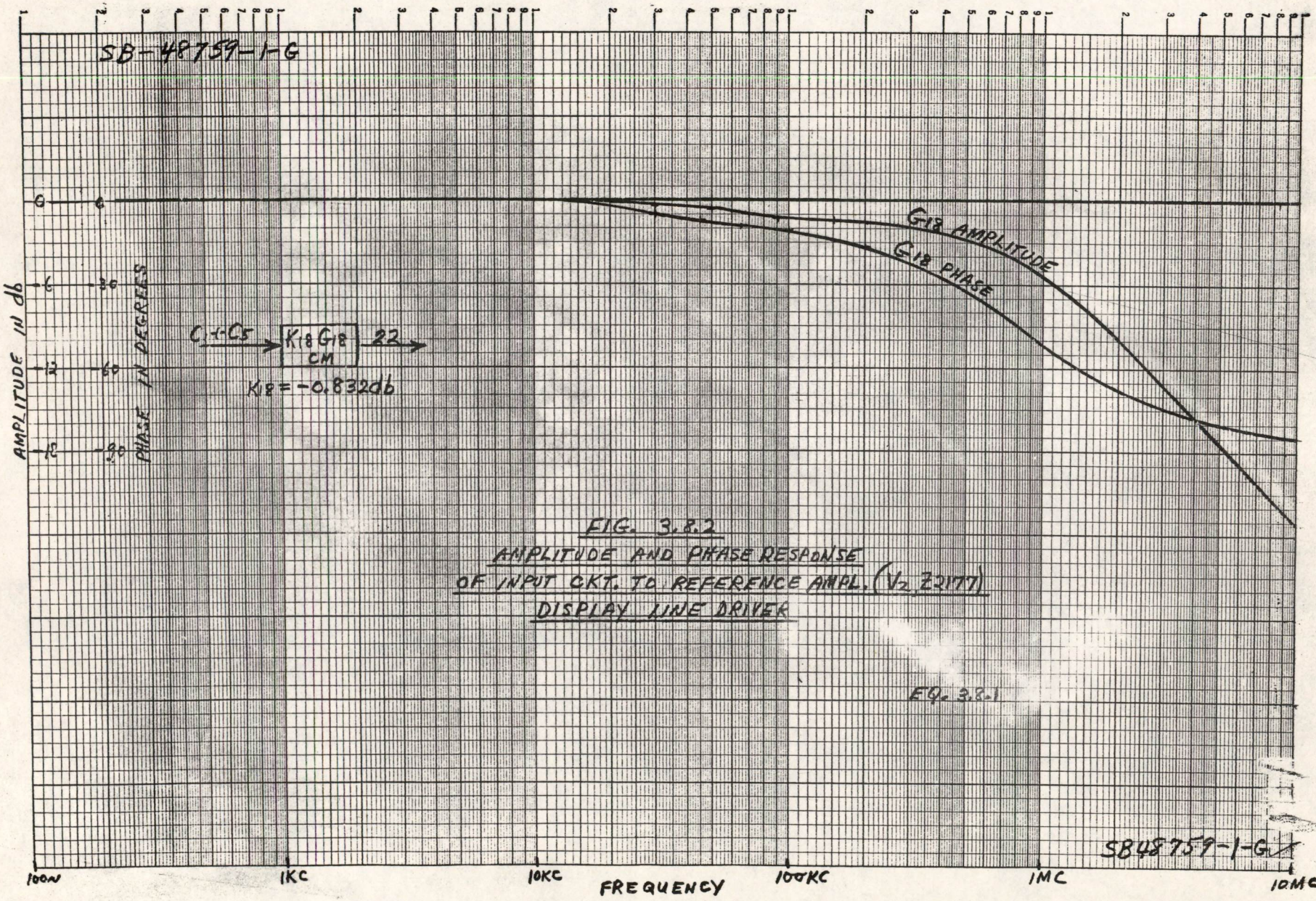
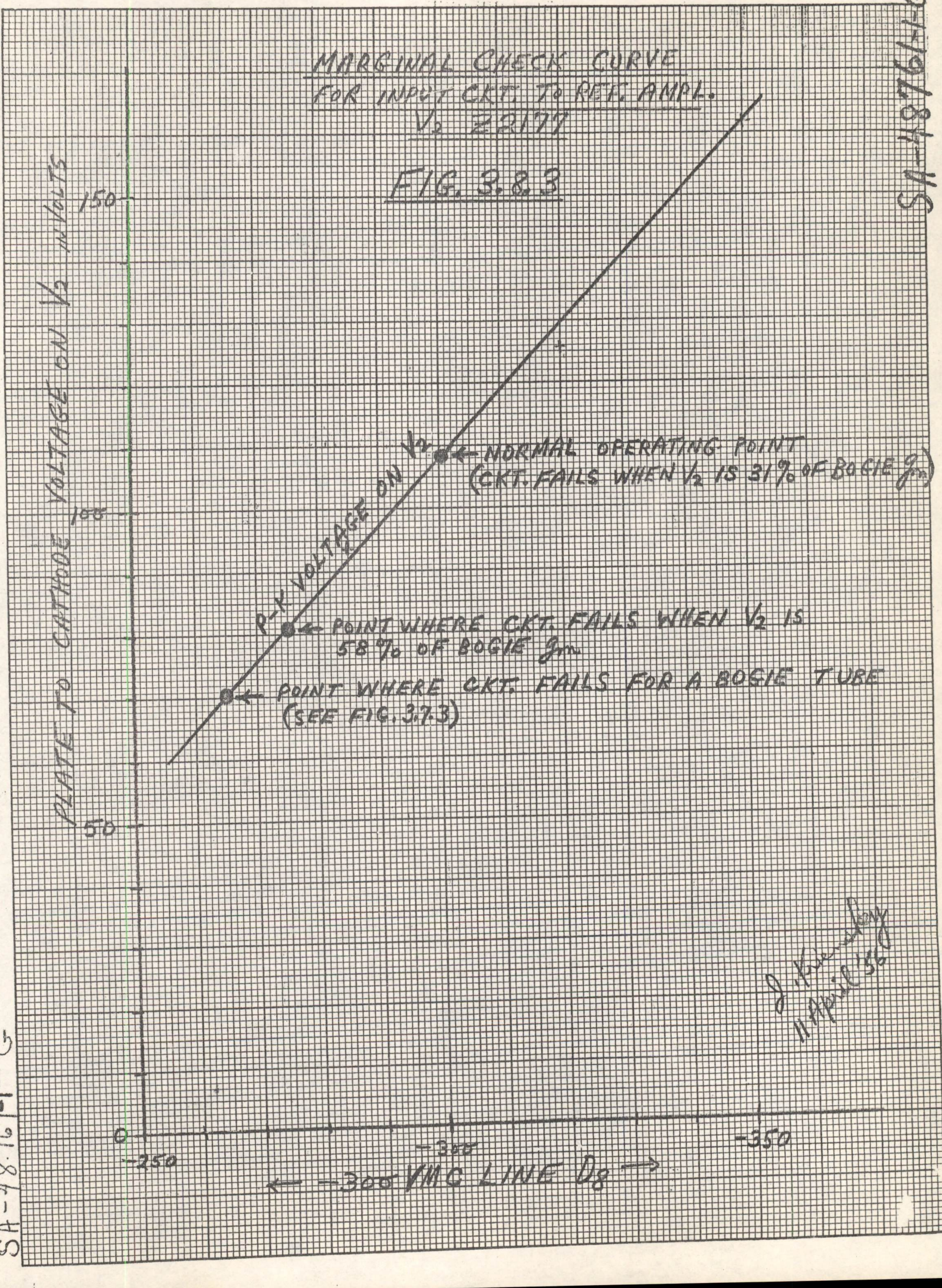


FIG. 3.8.2
AMPLITUDE AND PHASE RESPONSE
OF INPUT CKT. TO REFERENCE AMPL. (V_2 Z2177)
DISPLAY LINE DRIVER

Eq. 3.8-1


MARGINAL CHECK CURVE
FOR INPUT CKT. TO REF. AMPL.
V2 22177
FIG. 3.8.3
PLATE TO CATHODE VOLTAGE ON V2 IN VOLTS
150
100
50
0
-250
-300
-350
← -300 VMC LINE D8 →
P-K VOLTAGE ON V2
← NORMAL OPERATING POINT
(CKT. FAILS WHEN V2 IS 31% OF BOGIE gm)
← POINT WHERE CKT. FAILS WHEN V2 IS
58% OF BOGIE gm
← POINT WHERE CKT. FAILS FOR A BOGIE TUBE
(SEE FIG. 3.7.3)
11 April '56
SA-48761-G
SA-48761-G