Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: INFORMATION NEEDED FOR FINAL APPROVAL OF CIRCUITS

To: Distribution List Attached

From: A.W. Heineck

Date: December 29, 1953

INTRODUCTION: Complete up-to-date information should be assembled in a folder for each circuit under consideration for final approval. Final approval then means that the circuit, as described in the folder, is released for production. In the folder there should be

1) An up-to-date MRD circuit report which contains the following:

   A. Logical Definition

   B. Block Symbol

   C. Input Characteristics

   D. Output Characteristics

   E. Physical Layout

   F. Circuit Schematic

   G. Parts List

   H. Waveforms

   I. Power Requirements

   J. Marginal Checking Information

2) Supporting data which demonstrates the circuit's reliability.

   This data should be in the form of

   A. Margin Diagrams*

* J.W. Forrester: Memorandum M-1828, "Design and Tests of Electronic Circuits for Operating Safety Margins".

B. Transfer Characteristics

C. Final Design Notes

These items are discussed below and examples are given.

## 1.0 THE COMPLETE MRD REPORT

### A. Logical Definition (or Function)

The logical definition of a circuit is a brief statement which tells what the circuit can do logically, or functionally.

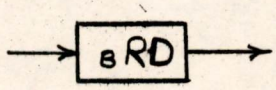
Example 1: Gate Circuit Model A -- The Gate Tube Circuit is a vacuum tube "AND" gate which has only two inputs. One input is a level, and the other is a narrow pulse.

Example 2: Register Driver Model A -- The Register Driver is used for power amplification of 0.1 μsec pulses.

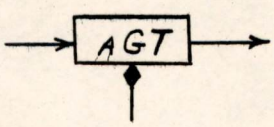
### B. Block Symbol

The block symbol is used to identify a circuit on block schematics. The circuit engineer should propose a symbol consistent with the note issued on Standard Terms and Symbols. See MRD Section 101, MD# 102.

Example 1: Register Driver Model B.




Example 2: Gate Tube Circuit Model A.




### C. Input Characteristics

The input characteristics include two main items

1) A complete description of the input signal (or range of input signals) for which the circuit will produce the specified output.

2) The load which this circuit places on the circuit driving it.

Input Signal Description

Example 1: Pulse Input

| | | |
|---|---|---|
| a) | Amplitude | 20 to 40 volts |
| b) | Width at Base | 0.08 to 0.12 μsec |
| c) | PRF | 0 to 2 mcps |
| d) | Polarity | positive |
| e) | DC Level | -15 volts |
| f) | Normal Shape and Allowable Distortion | |

The normal shape is a half sine wave as described above. The wave shape may vary from a triangle to a square as long as the width requirements are met. There is no limit on a negative overshoot, but the maximum allowable positive overshoot is 5 volts.

Example 2: Level Input

| | | |
|---|---|---|
| a) | Upper Level | +8 to +12 volts |
| b) | Lower Level | -27 to -30 volts |
| c) | Rise Time | $\leqq$ 0.3 μsec |
| d) | Fall Time | $\leqq$ 0.5 μsec |

Load Presented To Driver

Example 1: Suppressor of a Gate Tube Circuit

a) Input Capacitance: 15 μμf

b) When the control grid is pulsed and the d-c level applied to the suppressor is +10 volts, the positive conduction through the suppressor can be as high as 35 ma.

Example 2: For circuits with finite input resistance, the loading might be given as follows:

| | | | |
|---|---|---|---|
| Input level | > 5 volts | loading is | 100K to -150 v. |
| Input level | $\leqq$ 5 volts | loading is | 40K to +100 v. |

D. Output Characteristics

The output characteristics include

1) A complete description of the output pulse or level.

2) Delay caused by the circuit.

3) Load that can be driven.

Description Of The Output

Example 1: The description of the output pulse or level will be very similar to the examples given for the input pulse or level.

Delay Caused By Circuit

Example 1: Level Inverter -- The delay through the circuit is 0.1 μsec plus the time required for the signal to reach the switching levels of the circuit. The switch On level is -1 volt. The switch Off level is -4 volts.

Example 2: Gate Circuit -- The delay through the circuit is less than 0.03 μsec.

Loads That Can Be Driven

Example 1: Power Cathode Follower --

| | |
|---|---|
| Or current | 10 ma. |
| AND current | 25 ma. |
| capacity | 600 μμf |

Example 2: When a circuit is capable of driving many discrete loads under varying conditions, these loads should be tabulated somewhat as follows:

| Load That Can Be Driven | Terminating Resistors For RG 62U Coax 0 - 10 ft. | 11 - 30 ft. |
|---|---|---|
| 2 GT | 100 ohms | 150 ohms |
| 3 GT | 120 ohms | 180 ohms |
| 4 GT | 150 ohms | 220 ohms |

E. Physical Layout

This entry consists of a complete layout of the circuit. If the circuit is built on etched cards, a diagram of the back and front of each card is required. These diagrams are to show the position of each component on the card and all wiring, including the etched wiring. The components should be labeled with the same identification number that is used for the parts list and circuit schematic.

F. Circuit Schematic

All components on the circuit schematic should have an identification number and a value (or type). All other component informa-

tion such as tolerance, wattage, etc., will be contained in the parts list.

| | | | |
|---|---|---|---|
| Example 1: | Resistor | R1 | - 47K |
| | Capacitor | C7 | - 0.1 μf |
| | Inductor | L2 | - 27 μh |
| | Transformer | T1 | - 4:1 |
| | Diode | CR6 | - W |
| | Tube | V1 | - 5998 |

G. Parts List

The parts list consists of a table with the following information:

Resistors - Identification, quantity, value, voltage rating, tolerance, MRD Reference.

Capacitors - Identification, quantity, value, voltage rating, tolerance, MRD Reference.

Inductors - Identification, quantity, value, current rating, tolerance, MRD reference.

Transformers - Identification, quantity, material, turns ratio coupling (loose or tight), MRD reference.

Diodes - Identification, quantity, type, MRD reference.

Tubes - Identification, quantity, type, MRD reference.

Example:

| Identification | Quantity | Value (ohms) | Wattage (watts) | Accept. Tolerance | MRD Reference |
|---|---|---|---|---|---|
| Resistors | | | | | Sect. 122 |
| R1 | 1 | 470K | 1 | 5% | MD# 102 |
| R2, R3 | 2 | 56K | 1 | 5% | " " |
| R4, R5 | 2 | 20K | 1 | 5% | MD# 101 |

H. Waveforms

Pictures, or sketches, of the input and output waveforms should <u>not</u> be included if the waveform is the standard pulse described

in the introduction (Par. 1.01) of the circuits application section of the MRD book. A reference to 1.01 is sufficient. For all other waveforms the input pulse or level should be shown directly above the output pulse or level, both with the same time base.

I. Power Requirements

The power requirement entry has three items

1) Nominal operating voltages
2) Marginal checking voltages
3) Filament requirements

Nominal Operating Voltages

This section given the average current drain from each voltage source. If the current drain varies with PRF or other factors, a table should be used to show this information.

Example 1: Gate Tube Circuit Model A

| Voltage | Input Signal | Tube Condition | Average Current |
|---|---|---|---|
| 90 v. | 20 v. | on | 1.25 ma/mcps |
| " " | " " | off | 4.4 ma/mcps |
| " " | 40 v. | on | 9.4 ma/mcps |
| " " | " " | off | 16.0 ma/mcps |

Marginal Checking Voltage

This section gives the current drain from the marginal checking voltage source as the marginal checking voltage is varied.

Example 1:

| Voltage | Current |
|---|---|
| -75 v. | -0.3 ma |
| -150 v. | +2.6 ma |
| -225 v. | +5.5 ma |

Filament Requirements

A brief listing of the filament voltage and current requirements is sufficient. If any cathode is at some voltage other than the range of +15 to -30 volts, the average voltage, excursions, and duty factor should also be noted.

Example 1: Voltage 6.3 volts
Current 0.45 amps

Note: Cathode of V1-A normally at -110 volts is pulsed to -30 volts at a 10% max. duty factor.

J. Marginal Checking

The marginal checking entry consists of a brief statement which gives the voltage or voltages to be varried, the range of variation for a nominal circuit, and the effect of this variation upon the output.

Example 1: Gate Circuit Model A - Marginal checking shall be done by means of the +90 volt screen supply. A drop of 30 volts should be adequate to cause most circuits to fall below unity gain. A rise of 15 volts should pick up noise in most circuits.

2.0 SUPPORTING DATA ON RELIABILITY

In addition to the information needed for the MRD report, sufficient data should be presented to demonstrate the reliability of the circuit in question. This data should be in the form of

A) Margin Diagrams

B) Transfer Characteristics

C) Final Design Reports

and must be taken with the circuit assembled on etched cards and mounted in pluggable units, when the latter become available.

Inevitably, there will be circuits for which an infinite number of margin diagrams are available and others for which neither margin diagrams nor transfer characteristics are applicable. In these cases the engineer must use his judgment and present enough data to show reliability of the circuit.

A) Margin Diagrams

In general, the margin diagram will consist of a graph on which the percentage variation of a critical component is plotted as a function of the voltage variation necessary to cause circuit failure. See Fig. 1. These graphs should contain enough information to make them self-explanatory, and should demonstrate two things:

1) That the circuit as designed has adequate operating margins.

2) That the method of marginal checking described in the MRD report is effective in measuring deterioration of circuit components.

B. Transfer Characteristics

In general, the transfer characteristics will consist of a graph on which the output voltage amplitude is plotted as a function of the input voltage amplitude. See Fig. 2. Figure 2 is a typical transfer characteristic for the Gate tube circuit. The range of loads is covered by plotting transfer characteristics for the lightest load and for the heaviest load as given in the MRD report under output characteristics. For each load the marginal checking voltage should be used as a parameter.

C. Final Design Report

The final design report, such as an IBM--TR Note or an MIT--M Note, should contain all the circuit design information plus margin diagrams and transfer characteristics. Eventually, all the approved circuits should have in their folder an MRD report and a final design report. Until the final design report is ready, the transfer characteristics and margin diagrams will be sufficient.

NOTE: Please direct any questions to W. Jackman at IBM or R. Best at MIT.

Signed: A. W. Heineck
A. W. Heineck

AWH:cs

Drawings Attached:

SA-48501

SA-48495-1

Approved: J. F. Jacobs
J. F. Jacobs

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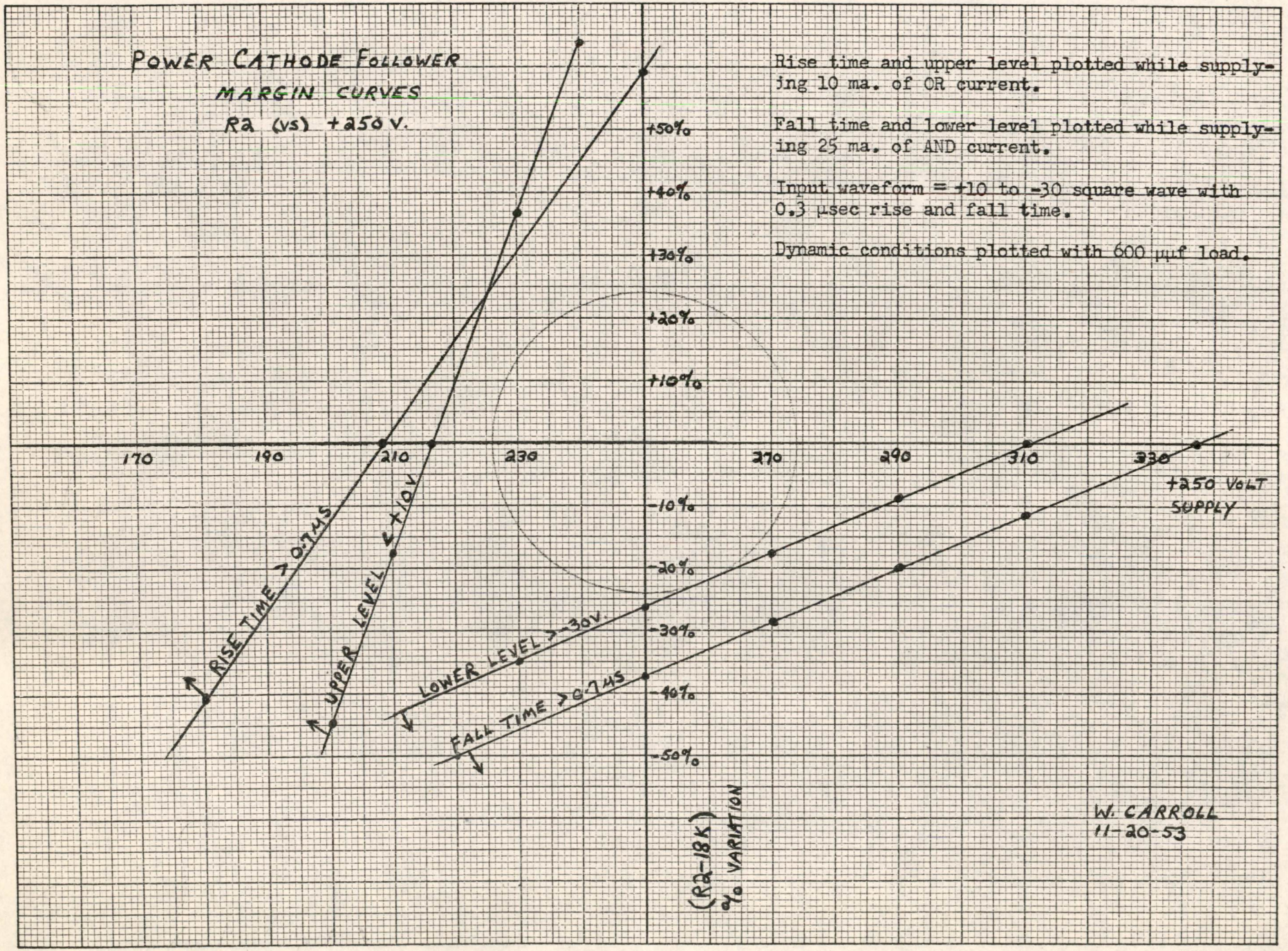
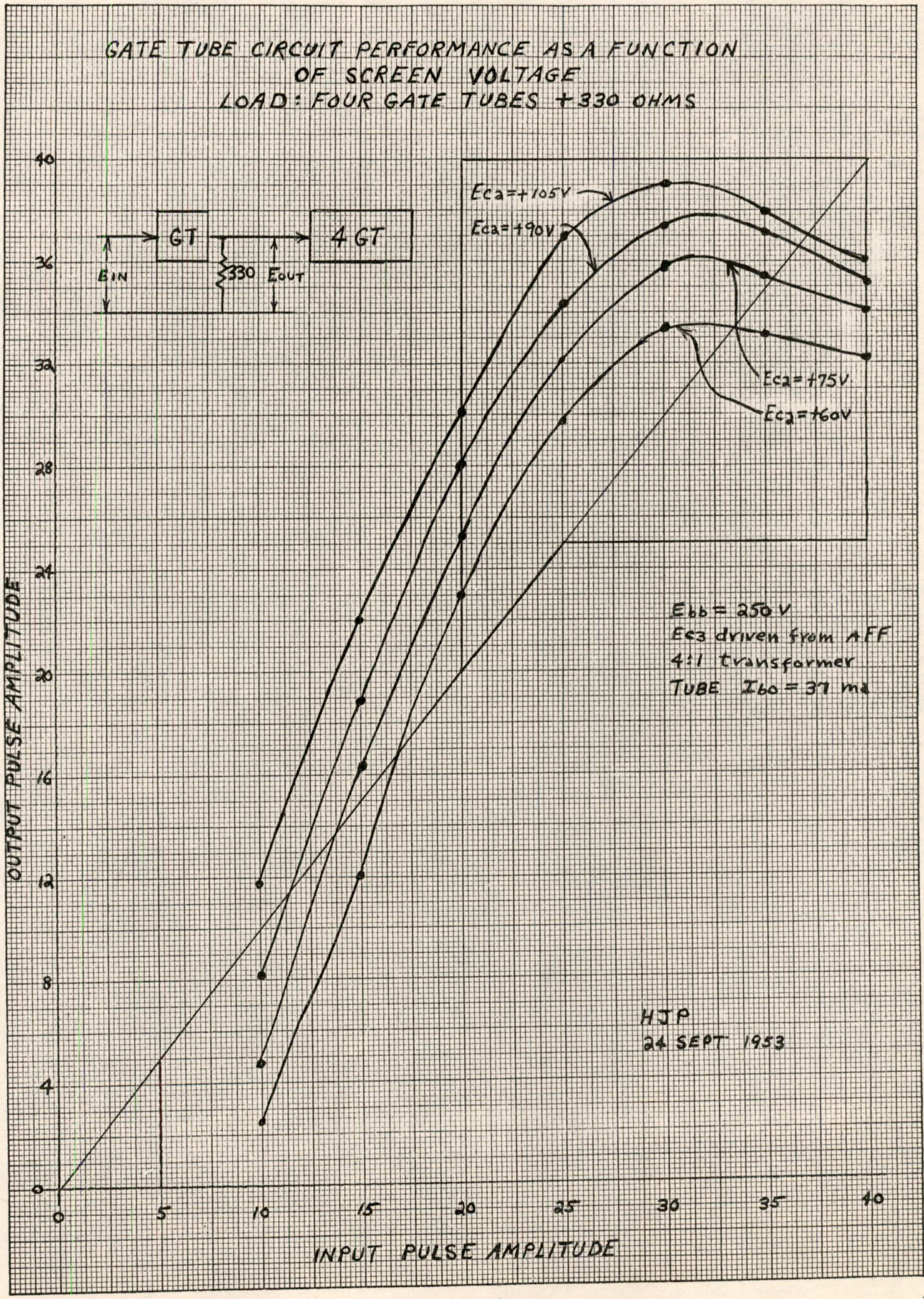



FIG 1

SA-48501-G




SA-48495-1-G

FIGURE 2

K. Olsen



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: MARGINAL CHECKING BREAKDOWN OF THE INSTRUCTION FRAME

To: N. H. Taylor

From: R. J. Pfaff

Date: January 6, 1954

Abstract: The philosophy and manner of the Instruction Frame marginal checking breakdown is given. A general description of the overall method of marginal checking the computer is contained in the Forward for those who may be unfamiliar with it.

## A. Forward

For the purposes of marginal checking, the central computer is divided into four "Equipment Groups": Arithmetic, In-Out, Program and Control, and Memory. These groups do not simply correspond with the physical frames. The table in Figure 1 shows what frames contribute to each Equipment Group. The circuits in each Equipment Group are broken down according to what voltages are used to marginal check them: +250, +150, +90, -150 or -300. A group of circuits designated according to Equipment Group and voltage is then broken into "Margin Groups" and finally, into even smaller "Logic Groups." Margin Groups are chiefly picked to separate circuits according to expected margins and occasionally to provide logical separation. Logic groups are picked to provide a logical breakdown for use in trouble location. There will be four Equipment Groups per central computer, a maximum of five Voltage Groups per Equipment Group, a maximum of six Margin Groups per Voltage Group, and a maximum of six Logic Groups per Margin Group. Programmed marginal checking will have access to any combination of Margin Groups for any given Equipment Group and voltage. It will have access to either half at a time or all the corresponding Logic Groups. This last point has not been completely settled.

## B. Conditions of the Problem

The Instruction Frame is entirely within the Program and Control Equipment Group. This report will only deal with that part of the Group having to do with the Instruction Frame.

Four voltages are used in this frame for marginal checking: +250 for power cathode followers, +150 for cathode followers, +90 for gates, and -150 for flip-flops, power cathode followers, and diode AND

circuits (cathode follower returns).

A few general criteria have been adhered to in making the breakdown:

1. Trouble Location of marginal checking failures must be possible without making use of involved programs or wholesale checks with a scope probe. This is accomplished by keeping the Logic groups comparatively small but doing routine checking on several at a time.

Undoubtedly, highly refined diagnostic programs will be available but, when they fail to work or to do the job completely, their very complexity will force the operator to turn to simpler programs and methods. The fine breakdown of the Logic Groups will be one of his tools

2. Low Margins due to cascading effect of margins must be avoided.

3. Circuits with expected significantly different margins must be separated.

4. The breakdown should be as straightforward and easy to understand as possible. One example--In some cases, for simplicity, the +150 breakdown corresponds to the -150 breakdown although it is not necessary on a logical basis.

5. Equipment is saved by providing no finer breakdown than appears reasonable or necessary.

6. A degree of safety should be provided by erring on the side of too much rather than too little and by anticipating what changes are likely to be required when actual machine margins are obtained.

Finally, it should be realized that some judgments regarding the breakdown are arbitrary. That is, many satisfactory solutions exist, these solutions differing in detail rather than in principle.

C. Cathode Followers and Diode Logic

It has been shown that cathode followers are best checked by lowering their plate voltage. When they are in cascade, whether or not there is diode logic between stages, each stage must have its plate voltage varied. This is because a stage should be removed well before its transfer characteristic under normal conditions has started to deteriorate. Hence, a lowering of input level would not accentuate the effect of a weakening tube until well past the proper time for that tube's removal. Diode OR circuits are checked by checking the cathode followers which drive them.

The back resistances of diodes in an AND circuit are checked by raising the cathode returns of the cathode followers driving them.

Figure 2 shows a typical AND circuit with inputs in a worst condition if CR1 is assumed to have a low back resistance. Unless the back current through CR1 exceeds the normal cathode current of CF4, the output voltage will remain approximately at its normal level, -30 volts, although the fall time of CF4 would be increased. If the normal cathode current of CF4 is 10 ma. and the leakage current of CR1 is 8 ma., the actual cathode current of CF4 will be approximately 2 ma. To detect this bad diode, one would raise the -150 return for CF4. This would, at first, raise the output level slightly, cutting off CF4. The point at which CF4 cuts off is directly related to the condition of CR1. After this point, the output voltage is proportional to the cathode return voltage and very quickly becomes intolerably high as the return voltage is raised, causing failure. If CR2 or CR3 were also doubtful, the effect would be accumulative. In practice, the cathode returns for CF1, CF2, CF3 and CF4 would be raised together a fixed amount and the worst combinations of inputs cycled through.

For illustration, consider Figure 3 to be a simplified version of the Class Cycle Matrix and the circled diode to have a low back resistance. The six lines from the cathode followers will be referred to as A,B,C, etc. For the circled diode to have any effect, line E must be at +10 volts. If line B is at +10, line C must be at -30, or vice-versa, so that one cathode follower is forced to take all the leakage current. Thus the flip-flops must be set for an I/O instruction (110) or a MISC instruction (000). The diode is "bad" if, when one of these classes is selected, spurious pulses are injected into the computer because the SHIFT line has climbed too high. Only the SHIFT line can climb; only the MISC and I/O class orders can cause it to climb.

To approach this question from the other end, how is it possible to detect and localize this bad diode? To detect that a bad diode exists, after the excursion is applied the program must try all classes and variations of orders -- all variations because it is to be expected that one variation of a class may work properly while another may not. Simultaneously, the program must look into all pertinent corners of the machine for the effects of spurious pulses. If said effect is detected, the machine will either halt or fail to carry out some positive action upon which further excursions are predicated (e.g. an Operate instruction directed to the Marginal Checking System). The operator's problem is to find out which CLASS line came up when it shouldn't have. Knowing this, his choice of the bad diode is reduced to one in three, which also happen to be in the same pluggable unit. The operator should have no trouble finding the line in question. Several methods are at his disposal, which, however, would require too much space here.

If the fall time of the output is critical, which is unlikely, the mere act of raising the return voltages could cause improper computer operation. In this case, some heavier thinking would have to go into the test programs.

Mr. Basic Remis has contributed much of the original thought

and work leading to the material given above.

D. Gates and Pulse Amplifiers

Gates are marginally checked by varying the screen voltage. Pulse amplifiers will not be checked directly but rather by the gate tubes which drive them. This is a valid method because in the operating regions in which we are interested 1) the transfer characteristic of the gate tube is very much a function of the screen voltage, and 2) the transfer characteristic of the pulse amplifier (all types included) adequately reflects the condition of the tube in the amplifier. Checking the pulse amplifiers in this way is desirable because it saves marginal checking equipment and speeds up routine checking.

E. Breakdown

Table I lists the lines to be brought out to the marginal checking terminals of the frame. The fact they are brought to this point does not necessarily mean that the marginal checking system will have access to each one individually. Fifty-seven lines are listed. With combination, something like 45 will be carried to the marginal checking distribution frame. Incidentally, it is expected that about 200 lines will be used to check the entire computer; 45 lines represent such a significant portion of the total because the Instruction Frame is the most complicated logically and hence the hardest to check.

Table II shows how the lines listed in Table I are to be used by the marginal checking system. Normally the system will check one full Margin Group at a time. In some cases only part of a Margin Group will be checked at a time. This is possible because programmed access to the Logic Groups will be provided. A number in parenthesis in front of the circuit description designates where this occurs.

The following abbreviations used in Tables I and II may unclear:

CF - 5965 Cathode Follower

PCF - 5998 Power Cathode Follower

7AK7-CF - 7AK7 Cathode Follower

Finally it should be emphasized that these tables cannot be considered final because 1) not everyone has had a chance to criticize and 2) information on some minor details has just recently become available.

Signed: R. J. Pfaff
R. J. Pfaff

Approved: R. L. Best
R. L. Best

DISTRIBUTION LIST

MIT

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Drawings attached:

SA-57470
SA-57471
SA-57472
SA-57473
SA-57474

SA-57470

# EXTENT OF MARGINAL CHECKING

## EQUIPMENT GROUPS

| MARGINAL CHECKING EQUIPMENT GROUP | CONTRIBUTING FRAMES |
|---|---|
| ARITHMETIC | RAE, LAE, PROGRAM |
| IN-OUT | RAE, LAE, PROGRAM SELECTION |
| PROGRAM + CONTROL | RAE, LAE, PROGRAM, INSTRUCTION |
| MEMORY | MEMORY #1<br>MEMORY #2 |

FIG. 1.

SA-57470

ROD
6 JAN 54

# REPRESENTATIVE "AND" CIRCUIT

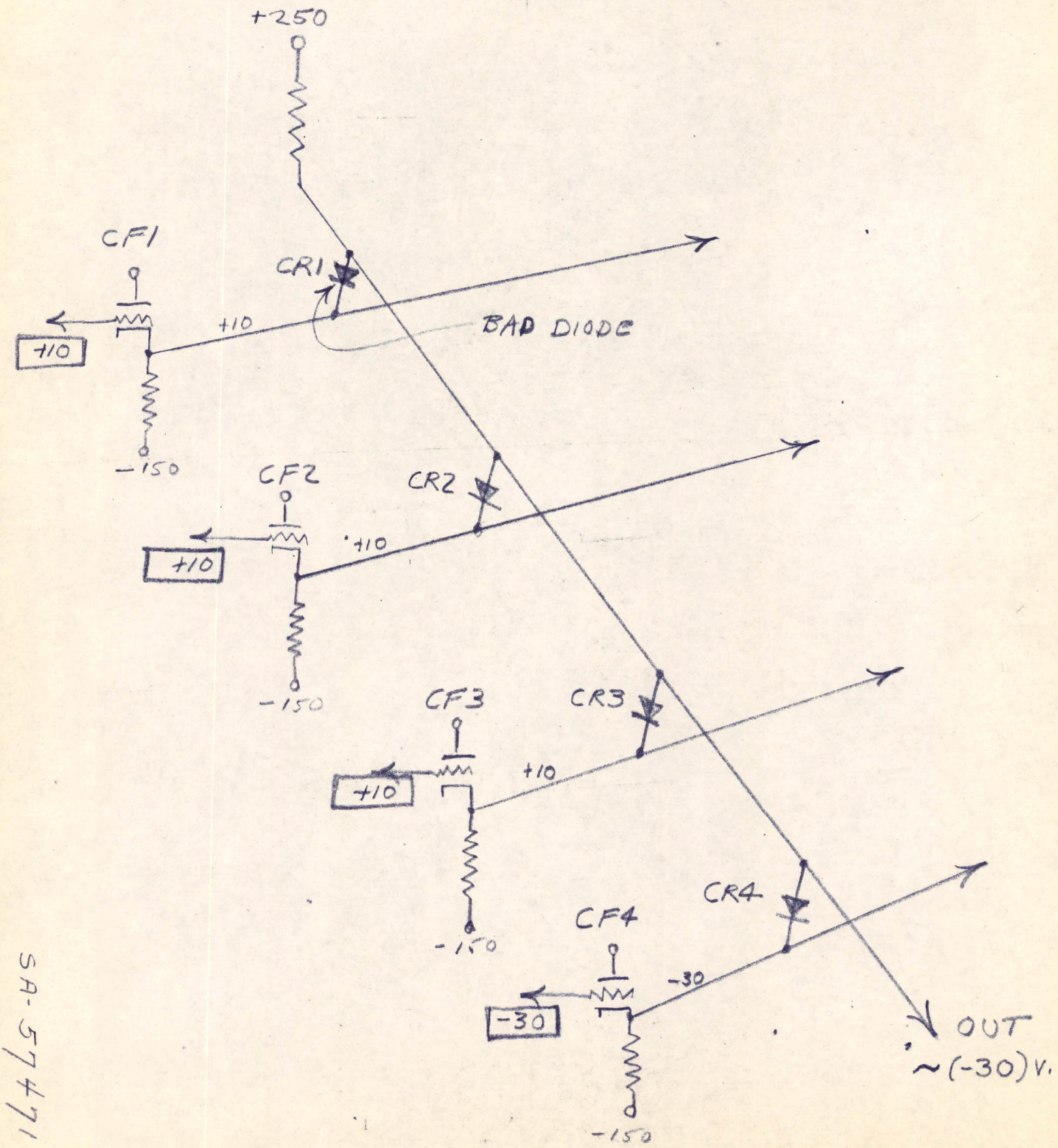


FIG. 2

SA-57471

SA-57471

# SIMPLIFIED CLASS-CYCLE MATRIX

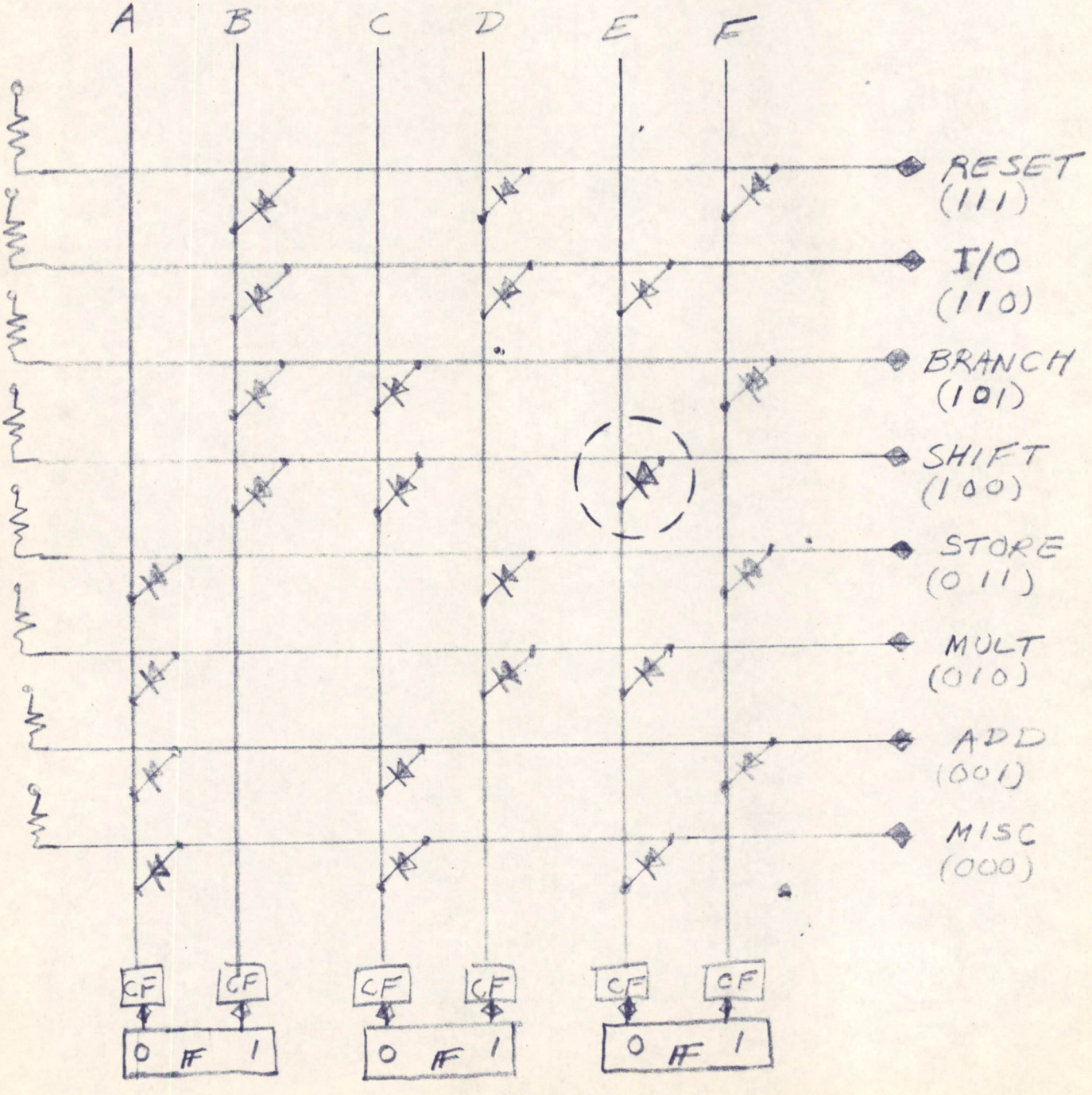


FIG. 3

SA-57472

RDF
6 JAN 54

6 JAN 54

SA-57473

TABLE I

LIST OF LINES BROUGHT OUT FROM INSTRUCTION FRAME



| Section Involved | No. of Lines | Voltage | Circuits Involved |
|---|---|---|---|
| Operation Reg | 5 | -150 | Class-Variation-Index FFs |
| | | +250 | Class PCFs |
| | | -150 | Class PCFs |
| | | +250 | Variation, Index PCFs |
| | | -150 | Variation, Index PCFs |
| Class Matrix Outputs (PCFs) | 8 | +250 | Branch Class |
| | | -150 | " " |
| | | +250 | Add, 1/O " |
| | | -150 | " " " |
| | | +250 | Store, Reset Class |
| | | -150 | " " " |
| | | +250 | Misc, Shift, Mult Class |
| | | -150 | " " " " |
| Variation, Index Matrix Outputs | 2 | +250 | |
| | | -150 | |
| Cycle Control | 3 | -150 | FFs |
| | | +150 | CF |
| | | -150 | CF |
| Instruction Matrices (CFs) | 8 | +150 | Branch Class |
| | | -150 | " " |
| | | +150 | Add,1/O " |
| | | -150 | " " " |
| | | +150 | Store, Reset Class |
| | | -150 | " " " |
| | | +150 | Misc, Shift, Mult Class |
| | | -150 | " " " " |

SA-57473

TABLE I (con't.)

LIST OF LINES BROUGHT OUT FROM INSTRUCTION FRAME



| Section Involved | No. of Lines | Voltage | Circuits Involved |
|---|---|---|---|
| Memory Select Matrix | 4 | -150 | FFs |
| | | + 90 | 7AK7-CF |
| | | -150 | " |
| | | +150 | CF |
| Command Generators (GTS) | 10 | + 90 | Branch, BR, Acc $A_1$ |
| | | + 90 | Acc $B_1$, Acc $B_2$ |
| | | + 90 | 1/O Control, Index |
| | | + 90 | AR, Adder |
| | | + 90 | SC Control #1, #2 |
| | | + 90 | Mem Control |
| | | + 90 | Acc $A_2$ |
| | | + 90 | Mem Buffer |
| | | + 90 | Prog Control #1, #2 |
| | | + 90 | Inst Control #1, #2, #4 |
| Time Pulse Distributor | 3 | -150 | FFs |
| | | +150 | CF |
| | | + 90 | Gates |
| Time Pulse Distributor Controls | 3 | -150 | FFs |
| | | +150 | CFs |
| | | + 90 | Gates |
| Clock | 1 | + 90 | |

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TABLE I (con't.)

LIST OF LINES BROUGHT OUT FROM INSTRUCTION FRAME



| Section Involved | No. of Lines | Voltage | Circuits Involved |
|---|---|---|---|
| Divide TPD | 3 | -150 | FFs |
| | | +150 | CFs |
| | | + 90 | Gates |
| Step Counter and Step Counter Controls | 7 | -150 | FFs |
| | | +250 | SC PCF |
| | | -150 | SC PCF |
| | | + 90 | 7AK7-CF SC Control |
| | | + 90 | Counting Gates |
| | | + 90 | " " |
| | | + 90 | Logic Gates |

SA-57473

TABLE II

INSTRUCTION CONTROL FRAME

Marginal Checking Voltage #250 Date 6 JAN 54 

| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| Prog & Control | 1 | A | Inst | Class PCF | Branch |
| | | B | | | Add, IO |
| | | C | | | Store, Reset |
| | | D | | | Misc, Shift, Mult |
| | 2 | A | | PCF | (1) Class Op |
| | | B | | | (1) Variation & Index Op |
| | | D | | | (2) Variation Matrix Output |
| | 3 | A | Inst | PCF | SC |

SA-57474

TABLE II (con't.)

Marginal Checking Voltage +150 Date 6 JAN 54 

| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| Prog & Control | 1 | A | Inst | Inst Matrix CF | Branch |
| | | B | | | Add, IO |
| | | C | | | Store, Reset |
| | | D | | | Misc, Shift, Mult |
| | 3 | A | | CF | TPD Control |
| | | | | | Cycle Control |
| | | | | | dv TPD |
| | | | | | SC Control |
| | | B | | | Memory Sel Matrix |
| | 4 | A | | CF | TPD |

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TABLE II (con't.)

Marginal Checking Voltage +90 Date 6 JAN 54 

| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| Prog & Control | 1 | A | Inst | Comm Gen | Branch, BR 2, Acc $A_1$ |
| | | B | | | Acc $B_1$, Acc $B_2$ |
| | | C | | | IO Control, IX Reg |
| | | D | | | AR, Adder |
| | | E | | | Se Control 1, Se Control 2 |
| | 2 | A | | Comm Gen | Mem Control |
| | | B | | | Acc $A_2$ |
| | | C | | | Mem Buff |
| | | D | | | Prog Control 1 |
| | | | | | Prog Control 2 |
| | | E | | | Inst Control 1 |
| | | | | | Inst Control 2 |
| | | | | | Inst Control 4 |
| | 3 | A | | Carry Gts | (1) Step Counter Odd Bits |
| | | D | | | (2) Step Counter Even Bits |
| | 4 | A | | Trans Gts | (1) Op-Adr R |
| | | B | | | (2) Clock |

SA-57474

TABLE II (con't.)

Marginal Checking Voltage +90 Date 6 JAN 54 

| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| | 5 | A | | Misc Gt | TPD Gates |
| | | B | | | Misc Control (e.g. SC) |
| | | | | | Divide TPD Gates |
| | | | | | TPD Control |
| | 6 | B | | 7AK7-CF | (1) SC Control |
| | | C | | 7AK7-CF | (2) Mem Sel Matrix |

SA-57474

TABLE II (con't.)

Marginal Checking Voltage -150 Date 6 JAN 54 Page 5

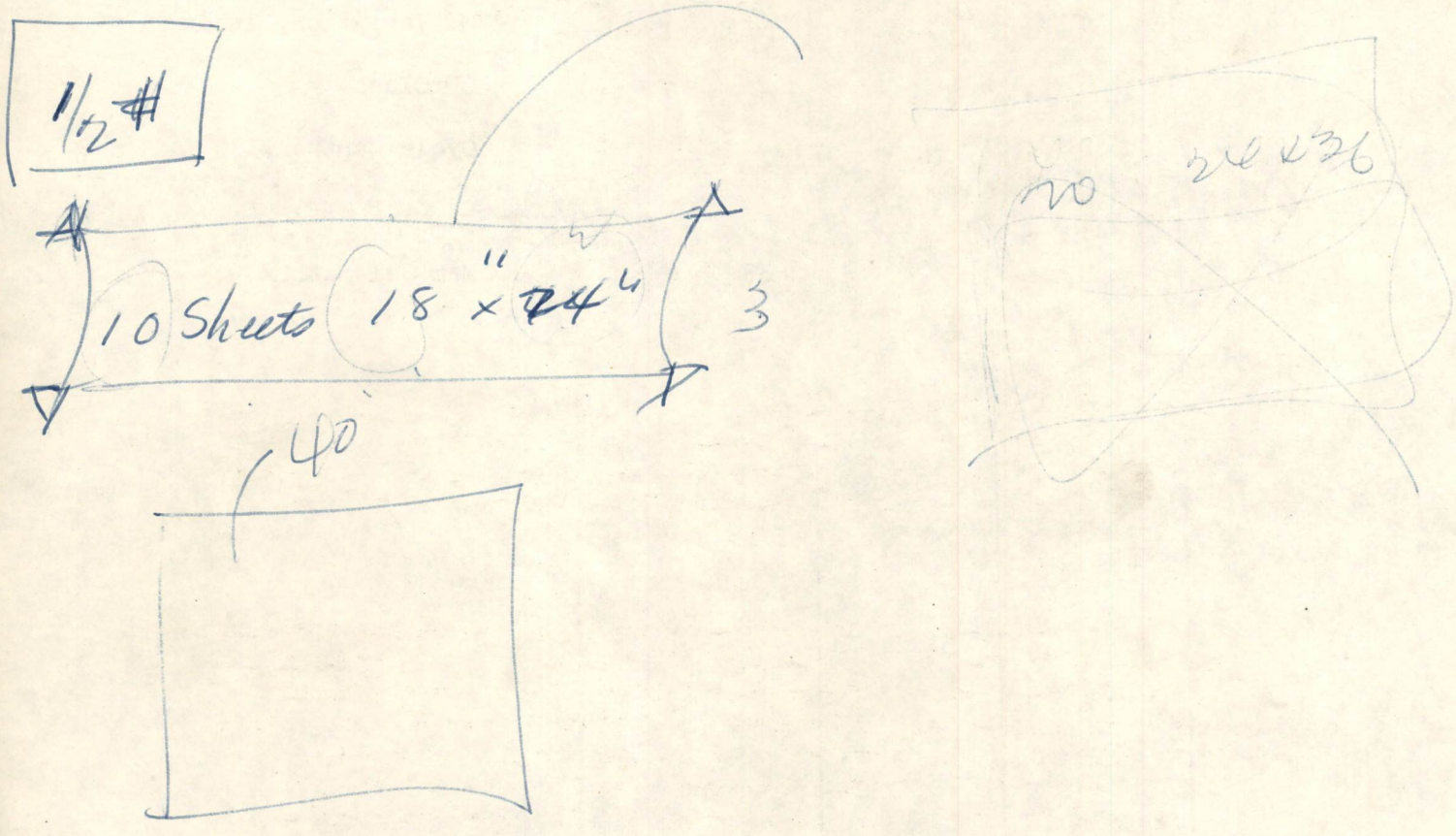
| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| Prog & Control | 1 | A | Inst | FF | Cycle Control |
| | | | | | TPD Control |
| | | | | | SC + SC Control |
| | | | | | TPD Divide |
| | | B | | | TPD |
| | | C | | | OP |
| | 2 | A | | PCF | Branch Class Output |
| | | B | | | Add " " |
| | | | | | IO " " |
| | | C | | | Store " " |
| | | | | | Reset " " |
| | | D | | | Misc " " |
| | | | | | Shift " " |
| | | | | | Mult " " |
| | | E | | | Variation Matrix Output |
| | | F | | | SC |
| | 3 | A | | Inst Matrix CF | Branch |
| | | B | | | Add, IO |
| | | C | | | Store, Reset |
| | | D | | | Misc, Shift, Mult |

SA-57474

TABLE II (con't.)

Marginal Checking Voltage -150 Date 6 JAN 54 Page 6

| Equipment Group | Margin Group | Logic Group | Frame | Circuit Type | Circuits |
|---|---|---|---|---|---|
| | 4 | A | | CF | OP Variation, Index |
| | | B | | | OP Class |
| | | D | | | Cycle Control, SC |
| | 5 | D | | FF | Mem Sel Matrix |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10 Sheets 18" x 24"
3
40
20 24 x 36

Olsen



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: MARGINAL CHECKING OF LOGICAL DIODE GATE CIRCUITS

To: N. H. Taylor

From: B. R. Remis

Date: February 10, 1954

Abstract: Included in this report are the methods for marginal checking diode "AND" circuits driven either by cathode followers or by "OR" circuits, diode "OR" circuits driven either by cathode followers or by "AND" circuits and diode matrix switches. Since the procedure is applicable only to circuits utilizing input levels, pulse diode circuits are not covered.

OBJECT: The object of a marginal check of diode circuits is: (a) to determine which diode gates in a system are causing marginal operation, and (b) to determine which diodes within the logical gate have low back resistances.

INTRODUCTION:

1. Definition of Margin: The voltage margin of a diode gate will be the permissible variation in the supply voltage of the circuit driving the diode gate before the output signal level of the diode gate changes sufficiently to cause inconsistent results. Margin is thus defined on a functional basis, rather than on the absolute value of the back resistance of any particular diode.

2. Cycling of Inputs: The conditions under which the marginal check will be made are those which present to the driving circuit the greatest load that occurs in normal operation. For an AND circuit this happens when the driven input under consideration is down at -30 and all other input lines are up to +10. An OR circuit presents a maximum load to its driving source when the driven input is up at +10, and all other input lines are down to -30.

To allow each driver in turn to handle the maximum load, the contents of the flip-flop register controlling the input levels of the diode gates should be cycled. This can be done either manually or by a suitable computer program.

3. Failure Indication: Failure can be detected by applying "checking pulses" to the control grids of the gate tubes controlled by the

diode gates. A pulse which passes an OFF gate tube or which is blocked by an ON gate tube can be used as an indication of failure. If the diode circuits do not control gate tubes, a voltmeter can be used to detect the change in output level.

4. Application of Marginal Checking Voltage: The marginal checking voltage is slowly varied out to a fixed excursion $\triangle E(max)$. If no error pulse is received from the checking gate tubes, the circuit is not marginal and no furthur information is recorded. If an error pulse was received, the procedure is repeated with reduced excursion until the circuit just operates without error. The marginal checking excursion at which this occurs is designated as $\triangle E$.

DIODE "AND" GATES DRIVEN BY CATHODE FOLLOWERS (figure 1)

1. Marginal Checking Voltage: A common negative return for all cathode followers driving the AND gate is brought out to a marginal checking supply.

2. Cathode Follower Drivers: The inputs to all cathode followers but one are held "up" at +10. The single "down" cathode follower draws I(AND)max from the diode gate. I(AND)max includes the diode back currents of the other n-1 inputs and the complete AND resistor load current. In figure 1, CF-1 is the "down" cathode follower.

3. Marginal Checking Procedure: The inputs are rapidly cycled so that each driver in turn becomes the "down" cathode follower. At the same time the marginal checking voltage, E(m.c.), is raised from -150 by the method mentioned above.

4. Failure Indication: Before failure the output level is held down to -30 volts by the single "down" cathode follower. As E(m.c.) is raised, less current is drawn from each of the cathode follower tubes. This does not affect the output of the "up" cathode followers, except for a minor increase in output due to a change in grid bias. However, if E(m.c.) + I(AND)max $R_K$ is greater than -30, no current is drawn from the "down" cathode follower, and the down cathode level will rise. Consequently, the diode gate output will rise. If this rise is large enough, a gate tube, normally held OFF by the diode AND circuit will pass a checking pulse to indicate that the circuit has failed. If gate tubes are not available, a voltmeter can be used to detect the rise in output level.

5. Evaluation of Margin: The presence of an error pulse indicates that one or more of the cathode follower drivers whose negative returns have been raised is accepting an I(AND)max sufficiently high to cause marginal operation. By proper grouping of cathode follower negative returns, AND gates in as large a section of the entire system as desired can be checked at one time. For example, if pluggable unit construction is used, it may be desired to locate the weak AND gates to within a particular pluggable unit. In that case one should lift together all

negative returns of cathode followers which drive AND gates in the pluggable unit in question.

If no error pulse was obtained the AND gates of the section tested are not marginal. If an error pulse was obtained for $\Delta E(max)$, the excursion, $\Delta E$, which barely allows errorless operation is recorded. $\Delta E$ is not affected by the driving cathode followers, since the only critical driver, the "down" cathode follower is cut off at the time of failure. It is dependent only upon I(AND)max, $R_k$, and the failure indication level ($\approx$ -15 if gate tubes were used). The numerical value of $\Delta E$ can therefore be designated as the "margin" of the AND gate in question.

To locate the particular diodes in an "n" input AND gate which have low back resistances, "n" static margins must be taken. Each margin is taken with the "down" level fixed at a particular input for the entire run. Since I(AND)max is composed of contributions from all diodes in the gate except the one whose input is held down, the correlation between margin on a particular line and condition of the diode on that line is an inverse one. That is, the poorest diode is the one whose line allowed the largest excursion of E(m.c.). Arranging the margins $|\Delta E|$, in order from highest to lowest will indicate the order of diode back resistances from lowest to highest. If no furthur data, other than whether $\Delta E(max)$ produced failure, is recorded, all that can be known about the relative conditions of the diodes within a gate is that the input lines for which error pulses were obtained do not contain the weakest diodes.

DIODE "OR" GATES DRIVEN BY CATHODE FOLLOWERS (figure 2)

1. Marginal Checking Voltage: A common positive return for all cathode followers driving the OR gate is brought out to a marginal checking supply.

2. Cathode Follower Drivers: The inputs to all cathode followers but one are held down to -30. The single "up" cathode follower supplies I(OR)max to the diode gate. I(OR)max includes the diode back current to the other n-1 inputs, the complete OR resistor load current, and $I(R_k)$, the current to the cathode resistor of the driving cathode follower. In figure 2 CF-1 is the "up" cathode follower.

3. Marginal Checking Procedure: The inputs are rapidly cycled so that each driver in turn becomes the "up" cathode follower. At the same time the positive returns of the driving cathode followers are lowered.

4. Failure Indication: Before failure the output level is held up to +10 by the single "up" cathode follower. As its plate voltage is lowered, the ability of the "up" cathode follower to supply the current demanded of it, I(OR)max, is weakened. If the "up" cathode follower is unable to maintain its +10 level, the output level of the OR gate will

fall to -30. If the output level eventually controls a gate tube, the OFF condition of this gate tube can be used as a failure indication. Otherwise a voltmeter can be used to detect the drop in output level.

5. Evaluation of Margin: The evaluation of $\triangle E$ is not as well defined as in the AND circuit case. Several factors other than diode back resistance have major affects on $\triangle E$: (1) the stiffness of the sources driving the follower grids, (2) the "age" of the cathode follower triodes, (3) the level the checking gate tube suppressors must fall to before pulses are rejected, and (4) the maximum tube current the "up" cathode follower is called upon to deliver. The condition of the OR gate, indicated by its back resistances, is reflected in $\triangle E$ only as a part of the current mentioned in (4). These factors partially obscure the effect of I(OR)max upon $\triangle E$. However, the factors most likely to change with time are the cathode follower triode characteristics and diode back currents. Information regarding the change of these two factors in a given circuit can be obtained by the change in $\triangle E$ from its nominal value.

A scheme similar to that outlined in the AND gate section can be used to isolate which OR gates, together with their drivers, in a large system are causing marginal operation. The absence of a checking pulse that should have passed thru an ON gate tube indicates that one or more of the cathode follower drivers whose plate voltage was lowered is sufficiently weak (or that the OR current it is called upon to deliver is sufficiently high), to cause marginal operation. By proper grouping of cathode follower plate returns, OR gates and their cathode follower drivers in as large a section of the entire system as desired can be checked at one time.

If an effort, similar to that outlined in the AND circuit section, is made to locate which diodes within a particular gate are poorest, certain simplifying assumptions must be made before the "static" margins are usable. One must assume that all of the above mentioned factors influencing the margin, with the exception of I(OR)max, are identical for all input lines to a given OR gate. If that is the case, the margins for each input line can be correlated with the back resistances of the diodes. Since I(OR)max is composed of contributions to all diodes in the gate except the one whose input is held up, the correlation is again an inverse one. That is, the poorest diode is the one whose input line allowed the largest excursion of E(m.c.). Arranging the margins, $|\triangle E|$, in order from highest to lowest will indicate the order of diode back resistances from lowest to highest.

If no furthur data, other than whether $\triangle E(max)$ produced failure, is recorded, all that can be known about the relative conditions of the diodes within a gate is that the input lines for which the checking pulse was blocked do not contain the weakest diodes.

DIODE "AND" GATES DRIVEN BY "OR" GATES (figure 4)

The OR gates (which are presumably driven by cathode followers) should be checked first using the methods outlined in the previous section. During this check all of the other inputs to the driven AND gate should be held at +10. This is necessary to permit any fall from +10 in the OR gate during the marginal check to be reflected as a fall in the output level of the AND gate. However, as soon as the OR gate output falls, all of the AND resistor load current and back currents through diodes of the other AND gate input lines flow down into $R_{or}$. This reduces the load current that the cathode followers driving the OR gate must supply and increases the margin of the OR gate circuit. This margin is the only realistic one to measure, however, since a failure in the OR gate which drives an AND gate does not make its presence felt unless the AND output is also affected. The AND gate diodes should then be checked as follows:

The -150 returns of the driving OR circuits are brought out to the marginal checking supply instead of the returns of the cathode followers.

The condition, whereby all of the inputs to the AND gate are held up at +10 and a single input is held down to -30, is still maintained. However, to facilitate the cycling process, the inputs to the cathode followers driving the OR circuit should be controlled as follows: All inputs to the driving OR gates but one in each OR gate are fixed at -30. The single unfixed input to each OR gate thus directly controls the output of the OR gate. The cathode follower driving that OR input may, as far as the cycling process is concerned, be treated as a direct cathode follower input to the AND gate. This allows the process to be carried out as before.

When failure occurs the single "down" input lines, (e.g., input $E_{a1}$ in figure 4), has become more positive than -30. Since the driving cathode follower (e.g., line $E_{o1}$ in figure 4) is down at -30, CR-01 is open. This corresponds to the statement in the cathode follower driven case that the "down" cathode follower is cut off at time of failure. Therefore, the simplified evaluation of margin, whereby $\Delta E$ depended only upon I(AND)max and $R_k$ hold for this case too. However $R_{or}$ replaces $R_k$.

A factor which presents a minor complication to the evaluation of $\Delta E$, is that not all of I(AND)max flows down through $R_{or}$. Some part of it flows down into the back resistances of the driving OR gate. However, since the OR gate has been previously checked (see first paragraph of this section) any decrease in $\Delta E$ from its nominal value is due primarily to the AND gate dioes. This method is therefore still a satisfactory marginal check for the AND gate.

With these exceptions the entire evaluation of margin outlined in the cathode follower driven case holds for this case too.

DIODE "OR" GATES DRIVEN BY "AND" GATES (figure 3)

The AND gates (which are presumably driven by cathode followers) should be checked first using the methods outlined in the section on AND

Gates Driven by Cathode Followers. During this check all of the other inputs to the driven OR gate should be held at -30. This is necessary to permit any rise from -30 in the AND gate during the marginal check to be reflected as a rise in the output level of the OR gate. However, as soon as the AND gate output rises all of the OR resistor load current and back currents through diodes of the other OR gate input lines are supplied from $R_{and}$. This reduces the load current that the cathode followers driving the AND gate must accept and increases the margin of the AND gate circuit. This margin is the only realistic one to measure, however, since a failure in the AND gate does not make its presence felt unless the OR output is also affected. The OR gates should then be checked as follows:

The +150 returns of the driving AND circuits are brought out to the marginal checking supply instead of the plate returns of the cathode followers.

The condition whereby all of the inputs to the OR gate are held down to -30, and a single input is held up at +10, is still maintained. However, to facilitate the cycling process, the inputs to the cathode followers driving the AND gates should be controlled as follows: All inputs to the driving AND gates but one in each AND gate are fixed at +10. The single unfixed input to each AND gate thus directly controls the output of the AND gate. The cathode follower driving that AND input may, as far as the cycling process is concerned, be treated as a direct cathode follower input to the OR gate. This allows the cycling process to be carried out as before.

When failure occurs the single "up" input line, (e.g., input $E_{01}$ in figure 3), has fallen below +10. Since the driving cathode follower (e.g., line $E_{A1}$ in figure 3), is up at +10, CR-A1 is open. This is an important difference from the case of the OR circuit directly driven by cathode followers. Now the driving source is effectively cut off from the OR circuit at the time of failure. Hence all the extraneous factors mentioned in the section on cathode follower driven OR circuits are absent in this case. Now $\Delta E$ depends only upon I(OR)max, Rand, and the failure indication level.

A factor which presents a minor complication to the evaluation $\Delta E$, is that not all of I(OR)max is supplied from Rand. Some part of it flows from the back resistances of the driving AND gate. However, since the AND gate has previously been checked (see first paragraph of this section) any decrease in $\Delta E$ from its nominal value is due primarily to the OR gate diodes. This method is therefore still a satisfactory marginal check for the OR gate.

By reasoning similar to that carried through in the cathode follower driven AND gate section, and driven OR gates, for as large a section of an entire system as desired, can be checked at one time. In addition the arranging in order of $|\Delta| E$, the margins on the +150 AND returns, in order from highest to lowest will indicate the order of diode back resistances from lowest to highest.

POSITIVE DIODE MATRIX (figure 5)

A positive matrix is defined as one for which the single selected

line is up, when all of the inputs to that line are up. Thus each output line consists of a separate AND gate. The class cycle matrix (figure 5) of the instruction frame will be used as an illustrative example. The problem of locating weak diodes in a matrix can be broken down into two simpler problems already discussed: (1) finding which AND gates of a system are marginal, and (2), finding which diodes within the marginal gate have low back resistance.

The marginal checking procedures are outlined in the section on Diode AND Gates Driven by Cathode Followers. For a matrix, the cycling process can be accomplished simply by adding "ones" to the contents of that portion of the flip-flop register which drives the matrix. In this manner, each driving cathode follower will at one time in the process handle I(AND)max. When the -150 returns of all driving cathode followers are raised together, failure will first occur at the output line of the most marginal AND gate. A rise in the output level of an unselected line is an indication of failure. If the gate tube in the command generator which passed an error pulse is known, the particular AND gate in the matrix selecting the class controlling that gate tube can be determined. Therefore, it is not necessary to store the contents of the flip-flop register at the time of failure to locate weak AND gates. It is also unnecessary to find which diodes within the gates of the class cycle matrix have low back resistance, since knowledge of the weak gate is sufficient to locate the pluggable unit to be replaced. However, when desired, the procedure for locating individual weak diodes in a matrix can be followed exactly as outlined in the section on AND gates driven by cathode followers.

## NEGATIVE DIODE MATRIX

A negative matrix is defined as a matrix for which the single selected line is down, when all of the inputs to that line are down. Thus each output line consists of a separate OR gate. The crystal matrix switch, Mod III of MTC, is an example of a negative matrix in the computer. The problem of locating weak diodes in a negative matrix can be broken down into two simpler problems already discussed: (1) finding which OR gates of a system are marginal, and (2) finding which diodes within the marginal gate have low back resistance.

The marginal checking procedures are outlined in the section on Diode OR Gates Driven by Cathode Followers. For a matrix, the cycling process can be accomplished simply by adding "ones" to the contents of the flip-flop register driving the matrix. In this manner each driving cathode follower will at one time in the process handle I(OR)max. When the positive plate returns of all driving cathode followers are lowered together, failure will first occur at the output line for which the combination of OR gate and driving cathode follower is most marginal. A fall in the output level of an unselected line is an indication of failure. Once again the output line which fails contains the marginal gate. Location of individual weak diodes in a matrix exactly follows the

outline in the section on OR Gates driven by Cathode Followers.

Signed Basil R. Remis
B. R. Remis

BRR:rmb

Approved R. L. Best
R. L. Best

Drawings Attached

A-57588
A-57589
A-57590
C-57777

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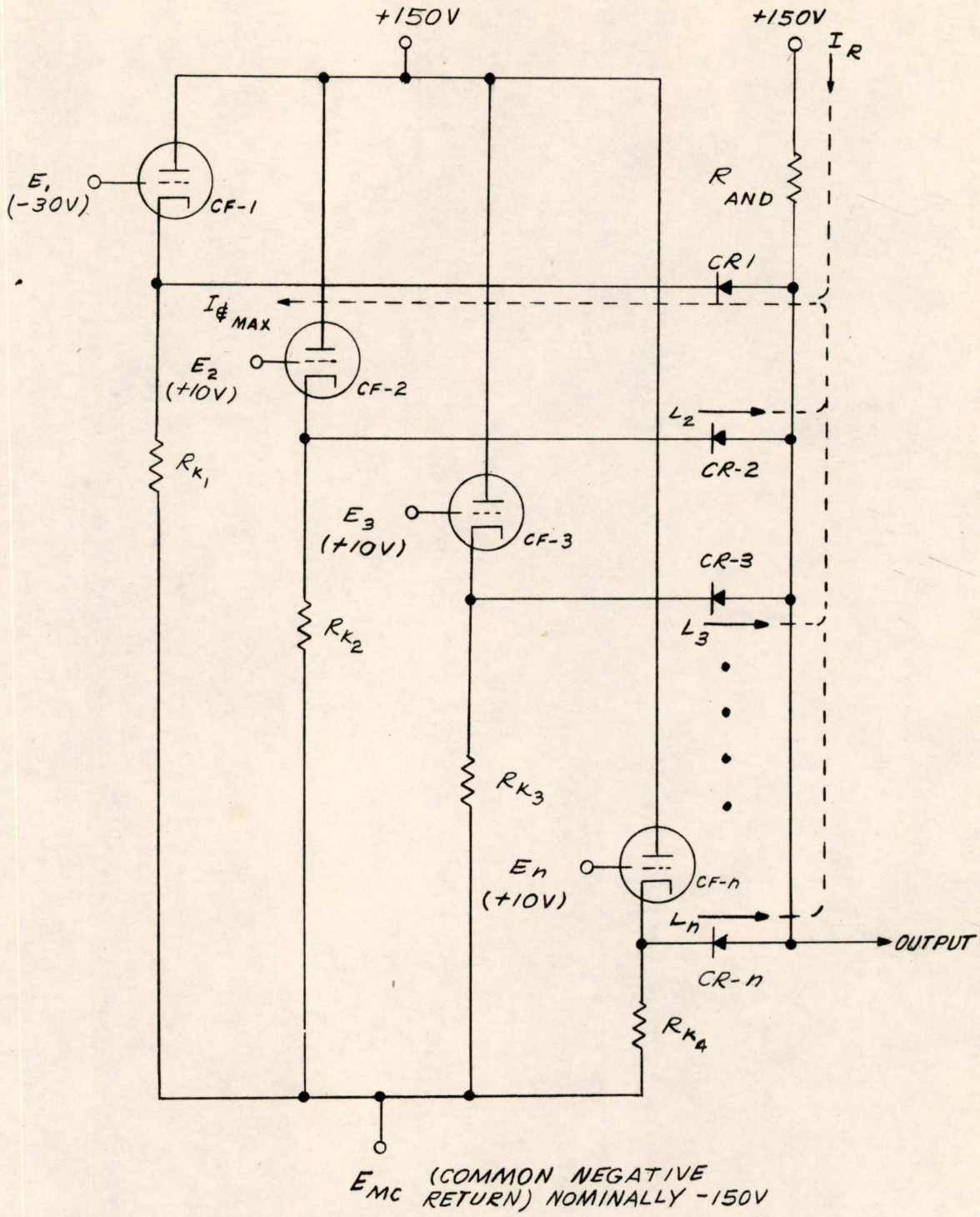


FIG. 1

DIODE "AND" GATE

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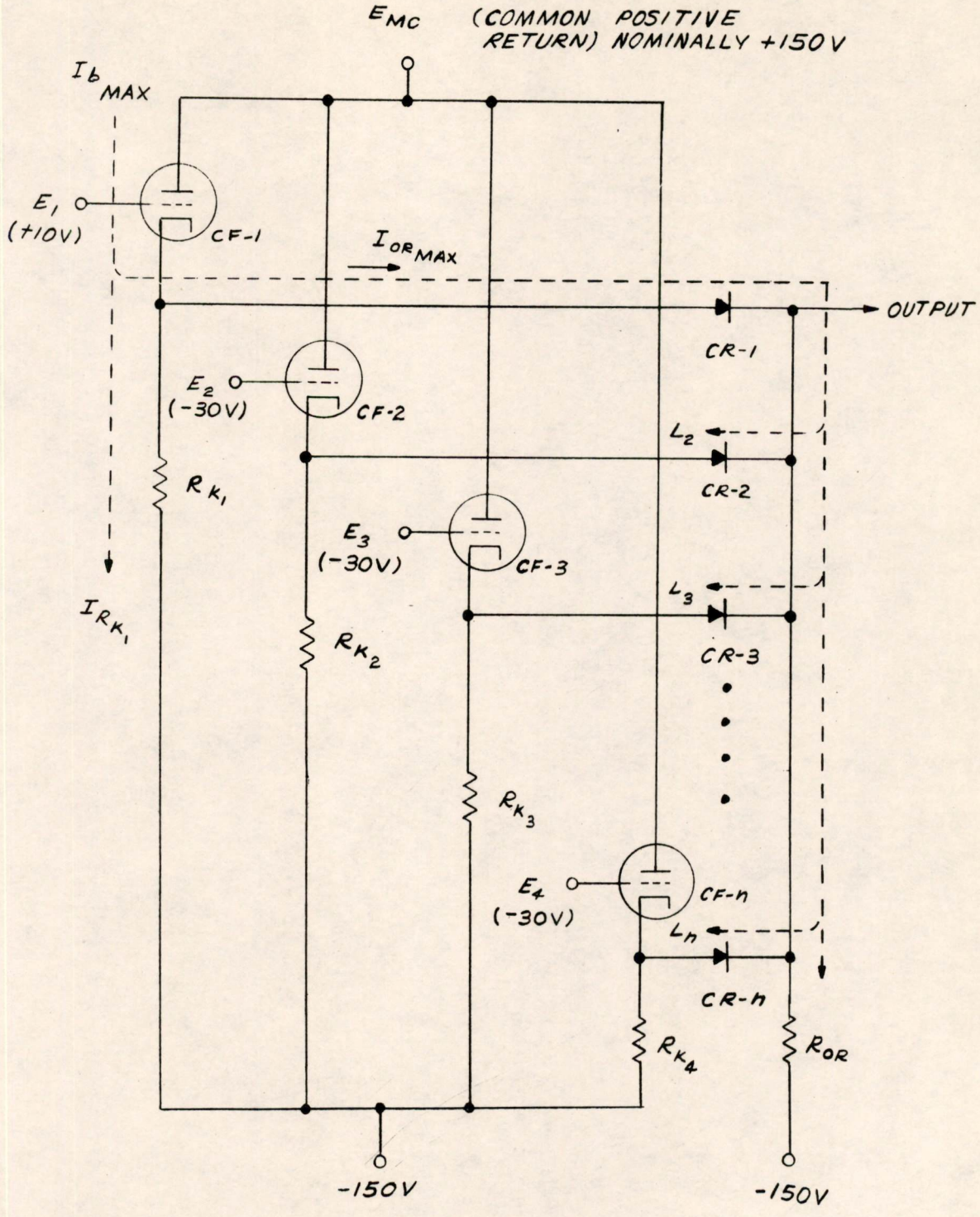


FIG. 2

DIODE "OR" GATE

A-57589

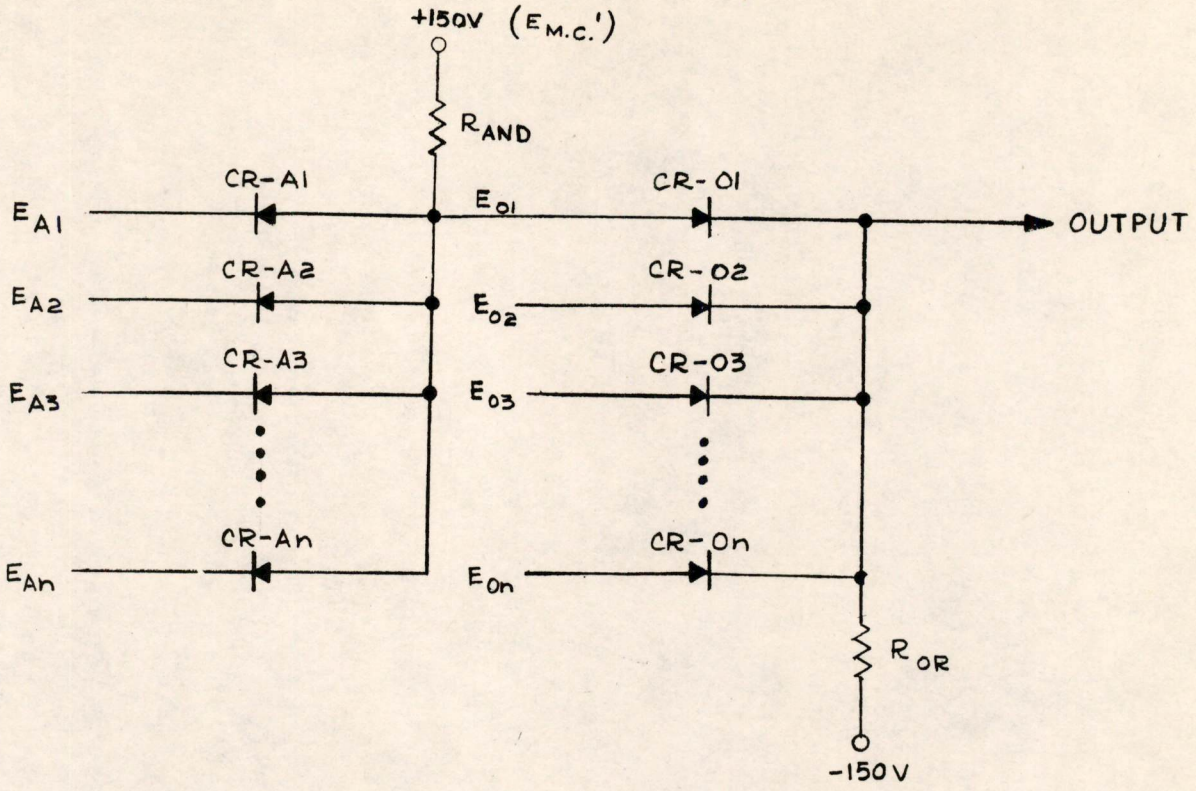


FIG. 3

"OR" GATE DRIVEN BY "AND" GATE

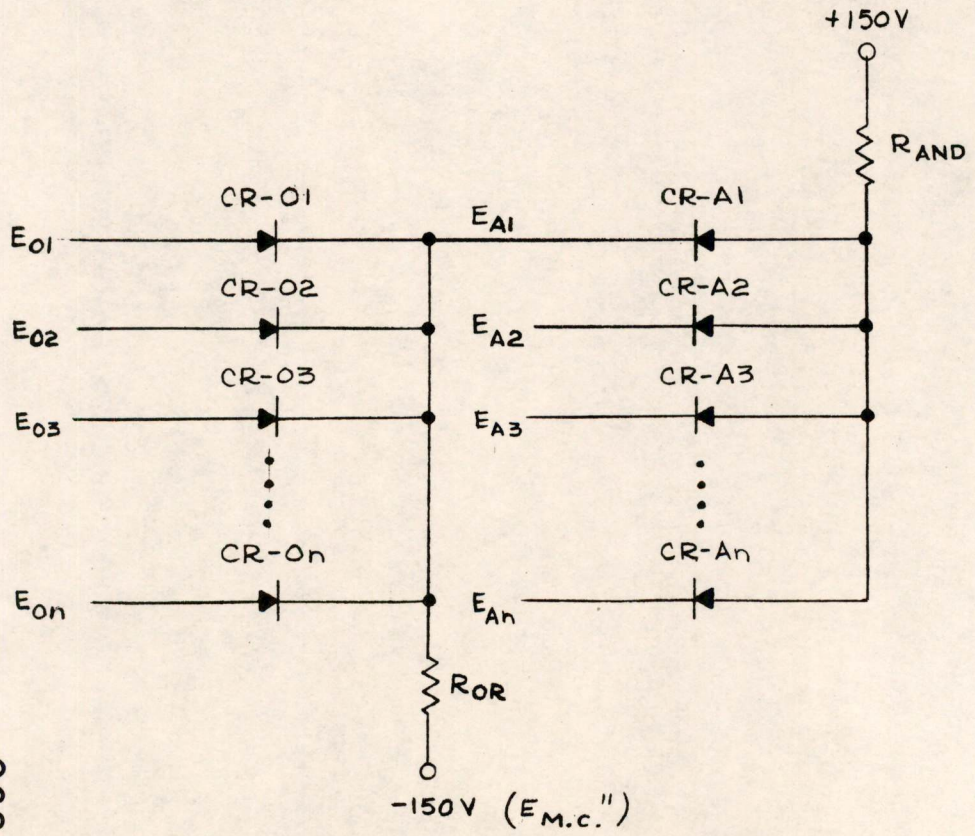


FIG. 4

"AND" GATE DRIVEN BY "OR" GATE

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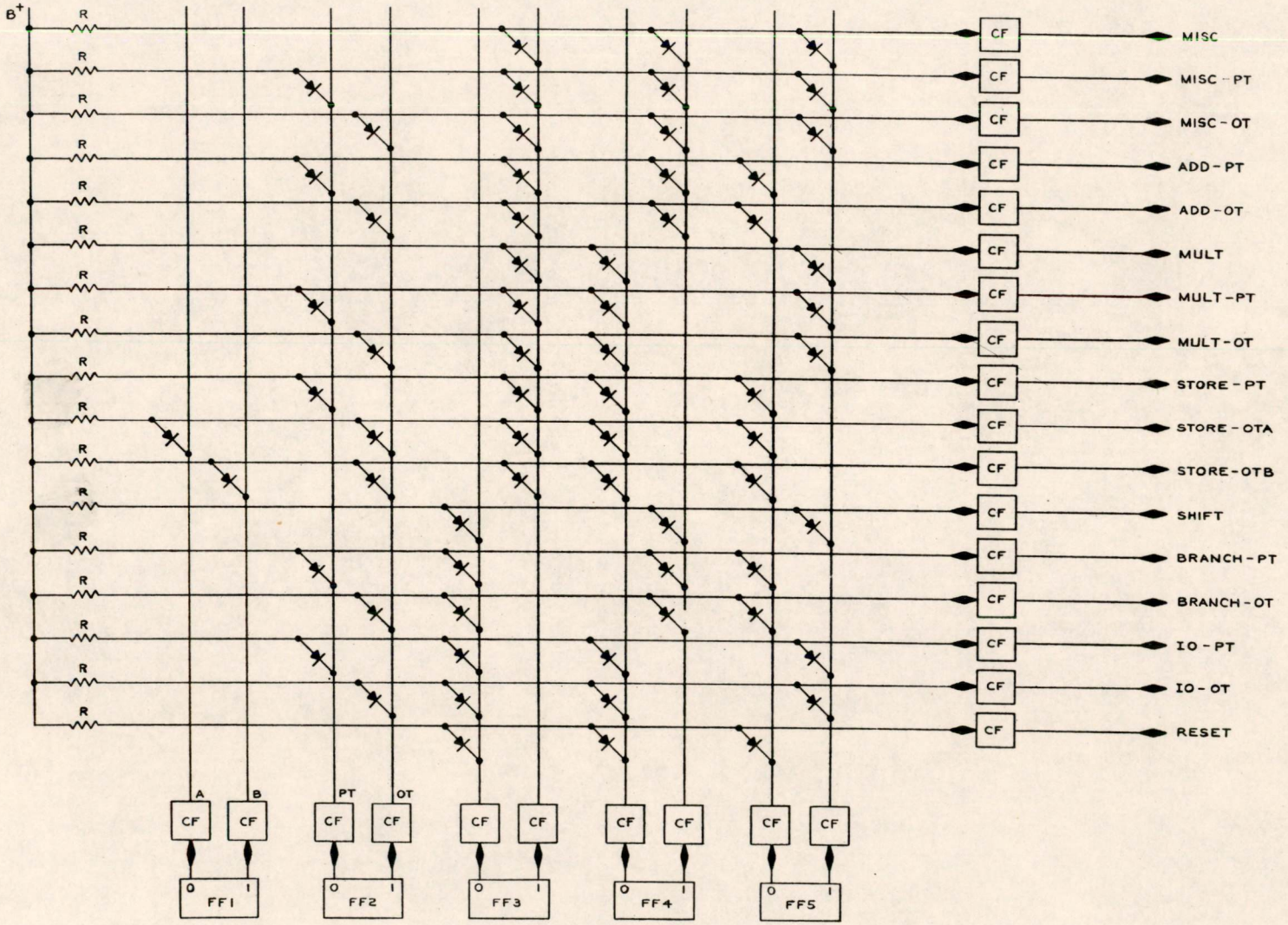


FIG. 5
CLASS CYCLE MATRIX

R. Best



Division 6 - Lincoln Laboratory
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SUBJECT: INTRODUCTION TO THE THEORY OF SEMICONDUCTORS VI, PROPERTIES OF HOLES AND ELECTRONS.

To: Transistor Group Distribution I

From: Donald J. Eckl

Date: 25 January 1954

Abstract: This is the sixth of a series of notes on the physics of semiconductors. In the previous note it was stated that when electrons left the valence band and moved to acceptor levels, holes were left in the valence band, and that these holes allowed increased conduction. This added conductivity was possible because valence electrons could now gain energy from an electric field and jump to the open levels at the top of the band. This would produce other empty levels to be filled and so on. It is possible to treat these empty levels or holes as positive particles with an effective mass $m_H^*$. The facts leading to this conclusion and the properties of these fictitious positively-charged particles are discussed in this note. Considerable attention is also paid to the properties of electrons moving in the top and bottom regions of the conduction band of a crystal. The idea of wave packets is developed in some detail.

## 6.0 Introduction. Conditions at the Top of an Energy Band.

The relation between the energy of an electron in a crystalline solid and its crystal momentum, $P = \pm h/\lambda$ where $\lambda$ is a wave length associated with the electron and h is Planck's constant, is depicted by the Brillouin zone plot shown in Figure 1. At lower energies the band energy approximates very closely the free-electron-type parabolic curve given by

$$E = E_o + \frac{P^2}{2m^*} \tag{6.0}$$

where $m^*$ is the effective mass of the electron for the energy band. The slope of this energy curve, as will be discussed in more detail later, gives the velocity of the electron in the crystal.

$$\therefore \quad \frac{dE}{dP} = \underline{v} = \frac{1}{m^*}\underline{P}. \tag{6.1}$$

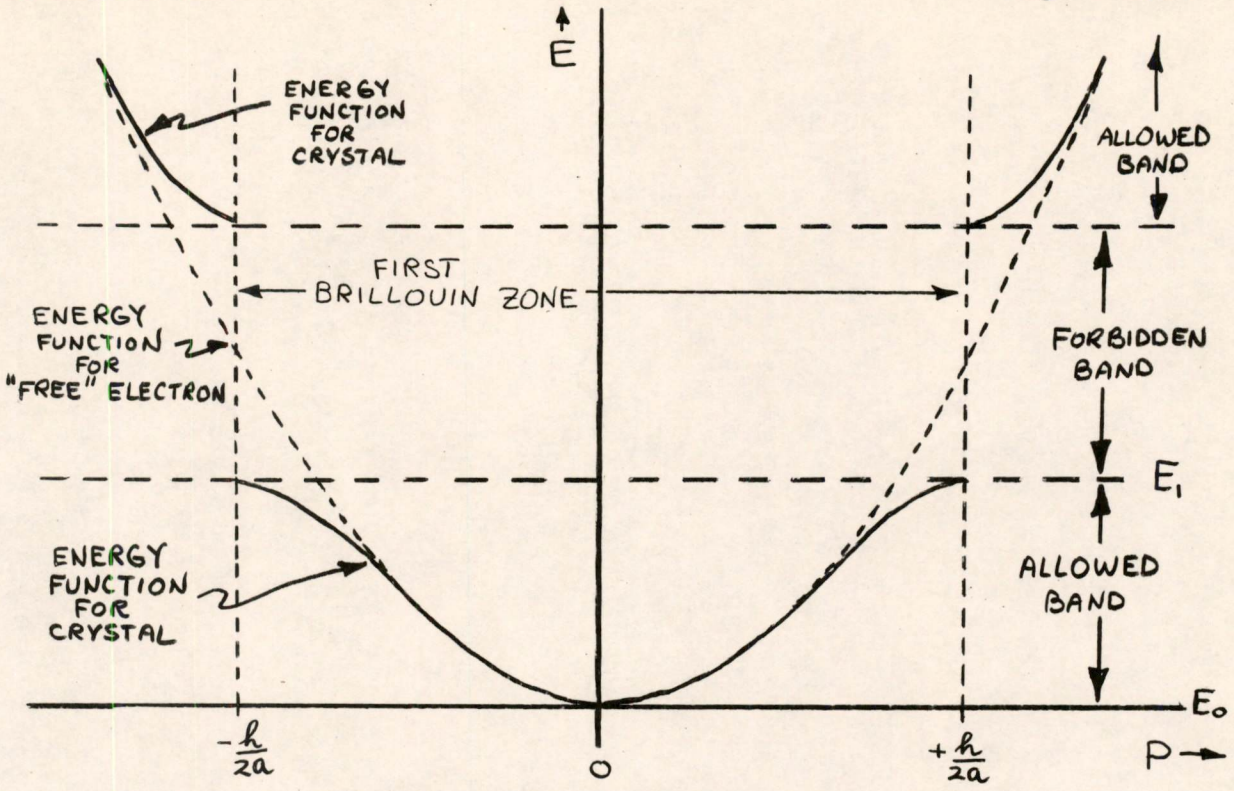


Figure 1. ALLOWED ENERGY BANDS

The second derivative gives the inverse of the effective mass of the electron in the crystal.

$$\frac{d^2E}{dP^2} = \frac{1}{m^*} \qquad (6.2)$$

As will be shown later dE/dP also gives the velocity for the true energy vs. momentum function. Equation (6.1) may be considered a definition of effective mass, $m^*$. A plot of the electron velocity $\underline{v}$ against crystal momentum $\underline{P}$ is given in Figure 2.

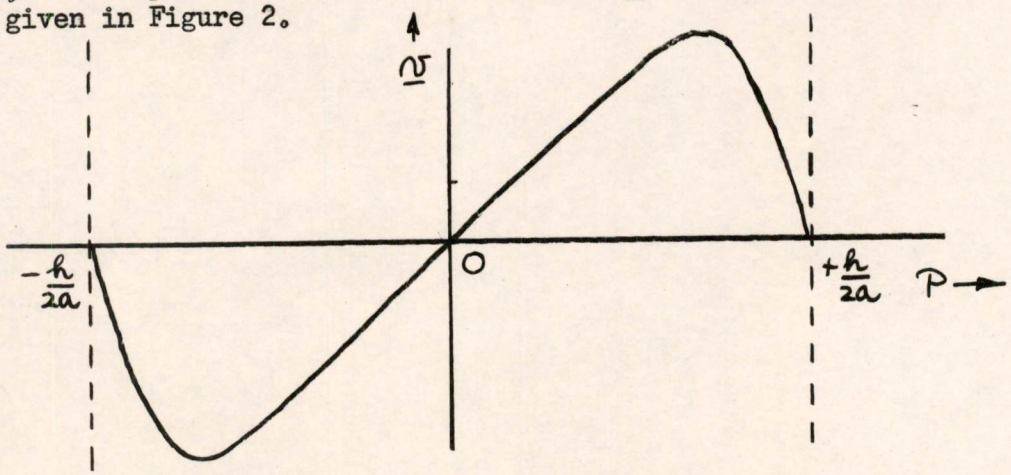


Figure 2. VELOCITY OF ELECTRON IN CRYSTAL

This curve shows the surprising (when viewed from a classical point of view) result that as its crystal momentum $\underline{P}$ increases the electron eventually slows down and has zero velocity when $\underline{P} = \pm h/2a$, the crystal momentum corresponding to the top of the energy band. Note also that the slope of this curve, which is the second derivative of the energy and therefore according to equation (6.2) the inverse of the effective mass, becomes negative at high values of $\underline{P}$. Therefore the electron exhibits a negative mass near the top of the allowed band!

## 6.1 Quantum View of the Electron.

Before discussing further this strange behavior of an electron in a crystal, it will be useful to review the quantum mechanical picture of the electron, which was introduced briefly in E-463, the first paper of this series. The electron, as it is visualized today, has a dual nature: it has the properties of both a particle and a wave. As a particle, the free electron has a mass of $9.11 \times 10^{-28}$ gram and a negative charge of $1.60 \times 10^{-19}$ coulomb. Experiments with a cathode ray tube[1] in a magnetic field provide the value of e/m for an electron, and Millikan's[2] oil-drop experiment gives the value of e. As a wave, the electron has a wave length of $\lambda = h/mv$. Insertion of the proper values[3] of m and h gives $\lambda = 7.2/v$ cms for a free electron. Davisson and Germer[4] performed experiments in 1927 which verified this result. Some indication of the wave lengths for free electrons of various energies is given in the table below:

| Energy | free-electron velocity | | wave length |
|---|---|---|---|
| $4.8 \times 10^{-6}$ e.v. | $1.3 \times 10^{5}$ cm/sec | (3000 MPH) | 6000 AU[5] |
| 1 electron-volt | $5.9 \times 10^{7}$ cm/sec | (370 mi/sec) | 12 AU |
| 140 e.v. | $7 \times 10^{8}$ cm/sec | (4000 mi/sec) | 1 AU |

For comparative purposes, although these are not electromagnetic waves, the first would fall in the middle of the visible light spectrum while the latter two would be in the X-ray spectrum as far as wave lengths are concerned.

The most satisfactory picture of an electron which we can form today is a mathematical one in accordance with the principles of the quantum mechanics. Thus the motion of an electron moving in a potential V(xyz) will be described in a statistical manner by the solution of the Schroedinger equation:

---

[1] Richtmyer and Kennard, "Introduction to Modern Physics" section 41.
[2] Richtmyer and Kennard, section 42.
[3] Planck's constant, $h = 6.6 \times 10^{-27}$ erg-sec.
[4] Richtmyer and Kennard, section 108.
[5] 1 Angstrom Unit (AU) = $10^{-8}$ cm.

$$\frac{h^2}{8\pi^2 m}\nabla^2\Psi - V\Psi = -i\frac{h}{2\pi}\frac{\partial\Psi}{\partial t}. \qquad (6.3)$$

where $\Psi$ is an eigen function, characteristic of the electron, for each allowed energy state (eigen value). This solution has the form

$$\Psi = c_k \psi_k(x,y,z) \exp\left(-\frac{2\pi i E_k t}{h}\right) \qquad (6.4)$$

where $c_k$ is an arbitrary complex constant and $\psi_k(x,y,z)$ is the solution of the Schroedinger amplitude equation for the Kth stationary state (eigen value) $E_k$:

$$\nabla^2\psi + \frac{8\pi^2 m}{h^2}(E - V)\psi = 0 \qquad (6.5)$$

The expression for $\Psi$ given in (6.4) represents the electron (in a manner of speaking). Note that it has the form

$$Ae^{-2\pi i \nu_k t} \qquad \text{where } \nu_k = E_k/h$$

which is a wave with a frequency $\nu_k$. Furthermore, the quantity

$$\psi\psi^* d\tau \qquad \text{where } \psi^* \text{ is the complex conjugate of } \psi$$

represents the probability that the electron will be found in a volume $d\tau$ of space. This means that an electron can only be found in a region where $\psi$ is non-vanishing.

An expression of basic import in our study of the motion of electrons is the Heisenberg uncertainty principle which can be expressed in one form as follows:

$$\Delta x \, \Delta p \geq \frac{h}{4\pi} \qquad (6.6)$$

where $\Delta x$ is the "uncertainty" in x and $\Delta p$ is the "uncertainty" in p. This expression states that we can never know both the position and the momentum of the electron with absolute certainty and, in fact, the product of the uncertainties or "spreads" in x and p can never be less than $h/4\pi$. This is a theoretical necessity and has nothing to do with our method of measurement. Consider for a moment the case of a free electron (moving in a potential V = 0). The general solution of the Schroedinger equation for this case is:

$$\Psi = A \exp\left\{2\pi i \sqrt{\frac{2mE}{h}}\, x - 2\pi i \frac{E}{h} t\right\} + B \exp\left\{-2\pi i \sqrt{\frac{2mE}{h}}\, x - 2\pi i \frac{E}{h} t\right\}. \tag{6.7}$$

Suppose we neglect the time-dependent part and consider the particular solution

$$\psi = Ae^{2\pi i \sqrt{\frac{2mE_o}{h}}\, x}$$

For this solution we know[6] that the momentum P is certainly $+\sqrt{2mE_o}$. Now if we calculate the distribution in x we obtain

$$\psi\psi^* = A^2, \text{ a constant independent of } x.$$

This is to be expected, since by specifying P exactly, we have made x indeterminate to agree with the uncertainty principle.

Suppose we now consider the case where

$$\psi = Ae^{2\pi i \sqrt{\frac{2mE_o}{h}}\, x} + Be^{-2\pi i \sqrt{\frac{2mE_o}{h}}\, x}. \tag{6.8}$$

In this case we obtain for the distribution in x

$$\psi\psi^* = A^2 + B^2 + 2AB \cos\left(\frac{2\pi}{h}\sqrt{2mE_o}\; x\right). \tag{6.9}$$

This is shown in Figure 3 below. Note that now the value of P is uncertain

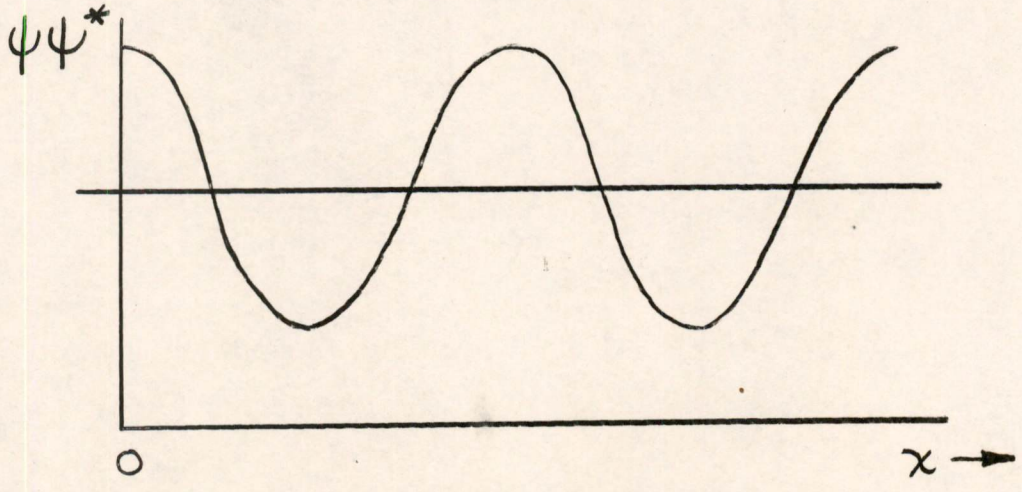


Figure 3. DISTRIBUTION IN X FOR FREE ELECTRON WITH MOMENTUM $\pm P_o$.

[6] Since the propagation constant is $2\pi x/\lambda$ and $P = h/\lambda$.

in that it may be either $+\sqrt{2mE}_o$ or $-\sqrt{2mE}_o$ with equal probability, and as a result we find x more exactly determined, there being most probable and least probable values.

6.2 Wave Packets.

The values of E allowed to the free electron are unrestricted. Therefore, for a free electron we can allow a wider range in the values of E and thus make P less certain, and as a result we will find that the value of x becomes more certain. We can eventually reach the point where $\Delta x \, \Delta P$ has the minimum value of $h/4\pi$ with both $\Delta x$ and $\Delta P$ small.

It is possible to choose wave functions $\psi$ which have a destructive interference, and hence have a resultant amplitude of zero, in all space except a single finite region. The group of waves occupying this finite region is called a wave packet or probability packet. The smallest possible wave packet, the minimum uncertainty packet with $\Delta x \, \Delta P = h/4\pi$, is sometimes referred to as a Kennard packet. Such a packet is the closest approach quantum mechanics can make to the classical particle with a known position and velocity. The electron in the lower part of the conduction band of a solid approximates a free electron and so can be represented by a wave packet.

The Schroedinger amplitude function for a Kennard packet in one dimension[7] has the form

$$\psi = \frac{A}{\sqrt[4]{2\pi \, \overline{\Delta x}^2}} \exp\left\{ - \frac{(x - \bar{x}_o)^2}{4\overline{\Delta x}^2} + \frac{2\pi i \, \bar{P}_o}{h} x \right\} \qquad (6.10)$$

where $\bar{x}_o$ and $\bar{P}_o$ are the most probable values of position and momentum and $\overline{\Delta x}$ is the range of x-values. The distribution in x is

$$\psi \psi^* = \frac{1}{\overline{\Delta x}\sqrt{2\pi}} \exp\left\{ - \frac{(x - \bar{x}_o)^2}{2\overline{\Delta x}^2} \right\} \qquad (6.11)$$

which is a Gaussian distribution centered around $\bar{x}_o$. For a Kennard packet

$$\overline{\Delta P} = \frac{h}{4\pi \overline{\Delta x}}$$

and the distribution in P is found by an analogous method to be:

---

[7] For reasons of simplicity this discussion and previous ones regarding the motion of an electron in a periodic potential have been carried out in one dimension. Extending the problem to three dimensions adds considerable complication but the results are essentially the same.

$$\frac{1}{\overline{\Delta P}\sqrt{2\pi}} \exp\left\{-\frac{(P-\bar{P}_o)^2}{2\overline{\Delta P}^2}\right\}. \qquad (6.12)$$

The form of a Kennard packet is shown in Figure 4 below.

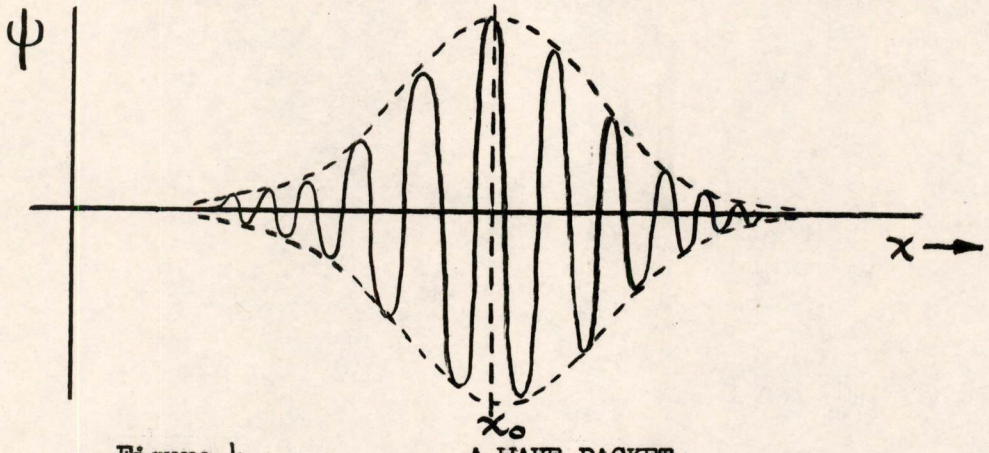


Figure 4. A WAVE PACKET

The distribution in x for such a wave packet is shown in Figure 5.

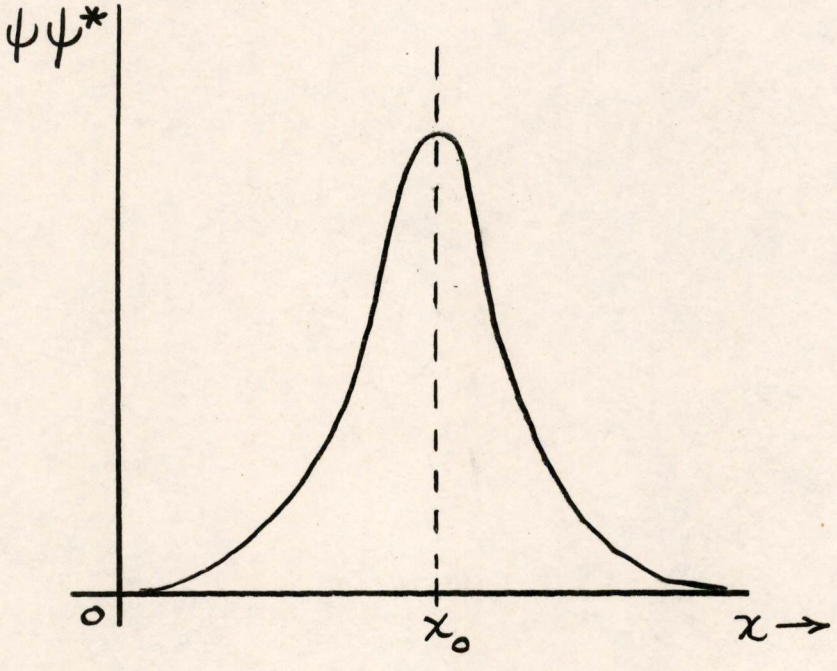


Figure 5. DISTRIBUTION IN X FOR WAVE PACKET

The introduction of wave packets brings up the question of group velocity. The velocity of the group of waves comprising such a packet is in general different from the phase velocity of the waves. The phase velocity $\nu\lambda$ is in this case given by E/P. The group velocity $v_g$, however, is given by the expression[8]

$$v_g = \frac{d\nu}{d(1/\lambda)} = 2\pi \frac{d\nu}{dk} = h \frac{d\nu}{dP} = \frac{dE}{dP} \tag{6.13}$$

This is the velocity used in discussing the electron in section 6.0 of this paper. In terms of the group velocity we can express the time-dependent $\Psi$-function for a Kennard packet as follows:

$$\bar{\Psi} = \frac{\exp\left\{-\frac{2\pi i \bar{P}_o^2}{2mh} t\right\}}{\sqrt[4]{2\pi}\sqrt{\Delta\bar{x} + i\Delta\bar{v}_g t}} \exp\left\{-\frac{\left[x - (\bar{x}_o + \bar{v}_{go} t)\right]^2}{4(\Delta\bar{x}^2 + i\Delta\bar{x}\Delta\bar{v}\, t)} + \frac{2\pi i \bar{P}_o}{h} x\right\}. \tag{6.14}$$

where $v_{go} = \frac{1}{m}\bar{P}_o$ and $\Delta\bar{v}_g = \frac{1}{m}\Delta\bar{P}$. Note that, while $\Delta x \Delta P$ can be made a minimum at some given time, say $t = 0$, as time goes on the packet will spread due to the range $\Delta v_g$ of velocities. The center of the packet is represented by the quantity

$$\bar{x}_o + \bar{v}_{go}\, t$$

so that the packet as a whole is moving with the group velocity $v_{go}$ while it spreads out. The variation of $\Delta\bar{x}$ with time is given by

$$\Delta\bar{x}^2 = \Delta\bar{v}_g^2 (t - t_o)^2 + \Delta\bar{x}_{min}^2 \tag{6.15}$$

where $t_o$ is the time at which $\Delta x$ is a minimum.

This Kennard packet is the closest approximation we can make to a classical particle at a point $x_o$ moving with a velocity $v_{go}$ at a time $t = 0$. The laws governing the motion of a wave packet in free space are identical to the classical laws governing the motion of a particle. A packet with energy E moving in an energy band of a solid will have a velocity given by[8]

$$\underline{v} = \frac{1}{h} \operatorname{grad}_P E. \tag{6.16}$$

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[8] This expression may sometimes be given as $d\nu/dk$. The difference depends on whether the k is defined by the term $e^{-ikx}$ (as above) or $e^{-2\pi ikx}$ in the wave equation.

The effect of a force on the momentum of such a packet is given by the vector relation[9].

$$\dot{\underline{P}} = - e\underline{E} - \frac{e}{c}\,\underline{v} \times \underline{H} \,. \tag{6.17}$$

where $\underline{E}$ and $\underline{H}$ are the electric and magnetic field vectors. The acceleration which a packet will experience under an applied force is

$$\frac{d\underline{v}}{dt} = \frac{d}{dt}\left(\frac{1}{h}\,\mathrm{grad}_p\ E\right) = \frac{1}{h}\,\mathrm{grad}_p \frac{dE}{dt} \,. \tag{6.18}$$

But the rate of change of energy under a force $\underline{F}$ is

$$\frac{dE}{dt} = \underline{F} \cdot \underline{v} \tag{6.19}$$

$$\therefore \quad \frac{d\underline{v}}{dt} = \frac{1}{h}\,\mathrm{grad}_p\left(\underline{F} \cdot \underline{v}\right) = \underline{F} \cdot \frac{1}{h}\,\mathrm{grad}_p\ \underline{v} = \underline{F} \cdot \frac{1}{h^2}\,\mathrm{grad}_p\,\mathrm{grad}_p\, E. \tag{6.20}$$

Since the acceleration is $\frac{1}{m}\underline{F}$, the reciprocal of the effective mass is

$$\frac{1}{m^*} = \frac{1}{h^2}\,\mathrm{grad}_p\,\mathrm{grad}_p\, E. \tag{6.21}$$

The operator "$\mathrm{grad}_p\ \mathrm{grad}_p$" is a second order tensor with 9 components so that in general the force and acceleration will not necessarily be in the same direction. This emphasizes that care should be taken in applying classical laws to "particles" in solids.

## 6.3 Bragg Reflections.

Before the discussion of the electron from the wave packet point of view, we had arrived at the startling conclusion that electrons near the top of an energy band behaved as though they had a negative mass -- i.e., for certain ranges of $P>0$, the velocity $\frac{1}{m}P$ became negative (see Figures 1 and 2). The wave nature of the electron discussed in the preceding section provides a reasonable explanation for this anomalous behavior.

At each plane of atoms in the crystal the electron wave $\Psi$ is partially reflected. In general these reflected waves will be out of phase. However, if the wave length is exactly 2a or twice the distance

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[9]The symbol E is used for energy while $\underline{E}$ is used for the electric field vector.

between the planes of atoms, the reflected waves from each plane will reenforce each other. That is, for

$$n\lambda = 2a \tag{6.22}$$

there will be a constructive interference for the reflected waves. As a result the incident waves will be reflected at each plane until the reflected intensity builds up to the incident intensity. There will then be two travelling waves of equal intensities, moving in opposite directions. This corresponds to a standing wave. Since $P = h/\lambda$, at the values of $P = \pm nh/2a$ the Bragg condition (6.22) is fulfilled. At these values of P there will be no travelling wave and no electron velocity. These are the points where the energy curve has its maxima and minima -- i.e., the points where the curve is multivalued and has its widest break from the free-electron curve (see figure 1). The multivalued energy arises from the possibility of two different standing waves, one with nodes and the other with loops at the atomic planes. The functions describing these waves are referred to as symmetric and antisymmetric, respectively.

A rigorous treatment of the problem shows that there is a finite range of P on either side of nh/2a over which reflections become highly probable. This causes the energy curve to deviate from the free-electron curve over this region. It is in this range that we find the net velocity decreasing as P increases, making the electron appear to have a negative mass.

## 6.4 Holes.

The contribution to current density in a crystal of volume V produced by a charge q moving with velocity $\underline{v}$ is given by

$$\left(\frac{q}{V}\right)\underline{v} \quad \text{coulombs per sq cm per sec.}$$

For the case of a full Brillouin zone or a full energy band there can be no net flow of current since all velocities have equal and opposite counterparts and there are no empty levels to which electrons can be excited. Suppose, following Shockley, we consider the current density contribution of an electron in a state s which has a velocity $\underline{v}_s$. This contribution plus that of all the other electrons must total zero for a filled band.

$$\therefore \sum_{\text{All } i \neq s} \left(\frac{-e}{V}\right)\underline{v}_i + \left(\frac{-e}{V}\right)\underline{v}_s = 0. \tag{6.23}$$

We can rewrite this to obtain

$$\sum_{\text{All } i \neq s} \left(\frac{-e}{V}\right)\underline{v}_i = \left(\frac{+e}{V}\right)\underline{v}_s \tag{6.24}$$

Therefore the current density contribution of the term on the left, which is a zone with one vacant state, is the same as that due to a particle with a charge + e moving in an empty zone with the velocity associated with the vacant state.

Now assume that we have an energy band of the type[10] shown in Figure 6.

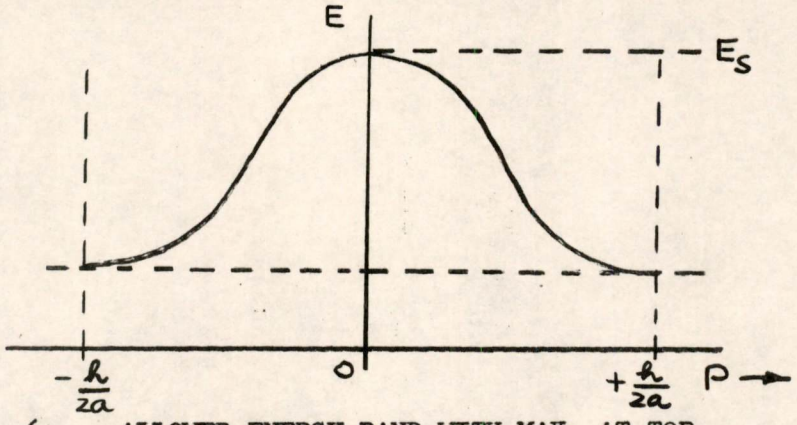


Figure 6. ALLOWED ENERGY BAND WITH MAX. AT TOP

The energy near the top of the band can be approximated by the expression

$$E = E_o - \frac{\underline{P}^2}{2m^*_H} \tag{6.25}$$

The velocity of a particle in this region is given by the group velocity

$$v_g = \frac{dE}{dP} = - \frac{\underline{P}}{m^*_H}$$

We have already seen that for the case of an isolated electron in one of the top states of the band, the application of an electric field causes the energy to decrease. However, we are now dealing with a hole. The state of minimum energy for a hole is the top state of a band, since all electrons will be in the lower states for minimum energy. Consider a hole at the top of the band in state s with energy $E_s$ and a velocity $\underline{v}_s = 0$. Suppose an electric field $\underline{E}$ is applied. Then the change in momentum is given by

$$\dot{\underline{P}} = e\underline{E}.$$

and

$$\dot{\underline{v}}_s = - \frac{1}{m^*_H} \dot{\underline{P}}.$$

---

[10] These arguments can also be developed for the case where the maxima occur at the edges of the zone.

The current density will then change as follows

$$\underline{\dot{J}} = \left(\frac{+e}{V}\right)\underline{\dot{v}_s} = \left(\frac{+e^2}{m^*_H}\right)\underline{E}. \tag{6.26}$$

Therefore, the power delivered to the hole from the field in time t will be

$$\underline{E}\cdot\underline{J} = \left(\frac{e}{m^*_H}\right)\underline{E}^2\, t. \tag{6.27}$$

Now if the effective mass is negative the power will be negative. But to gain momentum the hole must move downward in the energy band -- i.e., it must take energy from the field. Therefore, the effective mass of the hole must be positive.

As in the case of an electron, a hole can be represented by a wave packet. This packet actually serves to indicate the behavior of the electrons in the N-1 filled states.

## 6.5 Hall Effect.

At this point it will be helpful to discuss one important experimental justification for the depiction of holes as positive charge carriers. In 1878 E. H. Hall found that an e.m.f. can be induced across a strip of metal carrying an electric current by placing the strip in a magnetic field. For an isotropic crystal the direction and magnitude of the induced electrostatic field are given by the vector relation

$$\underline{E} = R\,\underline{J} \times \underline{H}\,. \quad \text{stat-volts} \tag{6.28}$$

where $\underline{J}$ is the current density, $\underline{H}$ is the magnetic field intensity, and R is the Hall constant of the material. It can be shown that in theory R for semiconductors should be given by the expression

$$R = \frac{3\pi}{8}\,\frac{1}{n\,q\,c} \quad \text{cm}^3/\text{stat-coulomb} \tag{6.29}$$

where n is the number of current-carrying particles per unit volume, q is the charge per particle, and c is $3 \times 10^{10}$. The sign of the charge is the same as the sign of the Hall constant.

Surprisingly, the Hall constant was found to be positive for a number of metals and semiconductors, although the conduction was known to be electronic. This was clarified by the theoretical prediction that holes should act like positive charge carriers. In fact, the explanation of this anomaly is one of the remarkable achievements of solid state theory.

Since there is a transverse electric field induced, the total electric field forms an angle $\Theta$ with the direction of current flow. This angle can be used to measure the Hall mobility from the expression (in practical units):

$$\mu_H = 10^8 \frac{\Theta}{H} \tag{6.30}$$

This mobility will not, in general, be equal to the mobility required in the expression for conductivity. In fact, the drift mobility depends on the square of the weighted average of $\tau$ (the mean free time between collisions for an electron) while the Hall mobility depends on the weighted average of $\tau^2$. As a result the Hall mobility is greater than the drift mobility by a factor[11] $3\pi/8$.

## 6.6 Mean Free Time of an Electron.

An electron (or hole) in a Brillouin zone can only occupy certain allowed energy states. If an electron gains or loses thermal energy, a transition from one state to another must occur. The average time between these transitions is called the mean free time. From a particle (or wave packet) point of view we can consider an electron in a given quantum state in the Brillouin zone as moving with a fixed velocity through the crystal. A transition occurs when this electron suffers a collision with another particle. The average time between such collisions is the mean free time $\tau$.

Suppose that an electron in state E has a probability A per unit time of undergoing a transition to another state. For a given state this probability is independent of the amount of time the electron has spent in the state. Therefore if there are N electrons in state E at time t, the number which will undergo a transition in the next interval of time dt is

$$dN = - N A \, dt. \tag{6.31}$$

This differential equation has the solution

$$N = N_o e^{- At} \tag{6.32}$$

where $N_o$ is the original number of electrons in state E. The form of this curve is shown in Figure 7.

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[11] Experiments show that this factor is actually too large to account for differences in the measured values. The "drift mobility" referred to here is the "microscopic" mobility of the electron. Conductivity mobilities may be less if trapping occurs.

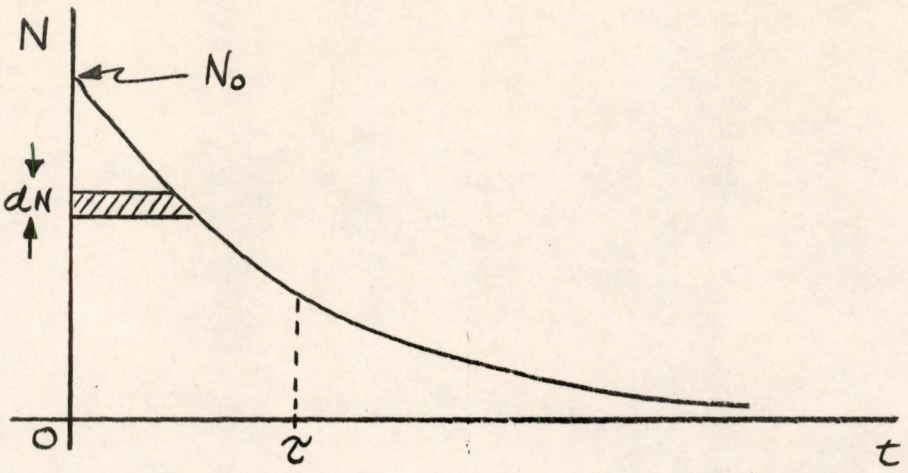


Figure 7. DECAY OF POPULATION OF STATE E.

The mean time that an electron will remain in state E is given by

$$\frac{1}{N_o}\int_o^\infty t\,dN = \frac{1}{N_o}\int_o^\infty t\,N\,A\,dt = \frac{A}{N_o}\int_o^\infty t\,N_o\,e^{-At}\,dt$$

$$= \frac{1}{A}\int_o^\infty At\,e^{-At}\,dAt = \frac{1}{A} \qquad (6.33)$$

The quantity $\frac{1}{A} = \tau$ is the <u>mean free time</u> for the electron in state E.

Now suppose a field E is applied to the electrons so that they acquire an acceleration $-(\frac{eE}{m})$ between collisions. The drift velocity can be calculated by determining the average distance covered by the electrons and dividing by $\tau$. The average distance will be the average of $\frac{1}{2}at^2$. The mean value of $t^2$ will be given by

$$\frac{1}{N_o}\int_o^\infty t^2 dN = \frac{1}{N_o}\int_o^\infty t^2 N A dt = \frac{A}{N_o}\int_o^\infty t^2 N_o e^{-At}\,dt$$

$$= \frac{1}{A^2}\int_o^\infty (At)^2\,e^{-At}\,dAt = \frac{2}{A^2} = 2\tau^2 \qquad (6.34)$$

The average distance or <u>mean free path</u> will be $a\tau^2$.

The <u>drift velocity</u> will be $\frac{a\tau^2}{\tau} = a\tau$.

6.7 Relaxation Time.

The mean free time which we have considered in the previous section is the value obtained in a pure solid where the electron scattering is due to thermal agitation of the atoms in the solid. Thermal vibrations of the atoms distort the periodic potential of the lattice and as a result the electronic wave functions and the momenta of the electrons change. If we consider a more general case and take into account the angle $\Theta$, which gives the new direction of the scattered or deflected electron relative to its original direction, we obtain a new value for $\tau$, which can be expressed in terms of our previous mean free time, here called $\tau_c$, by the relation

$$\tau = \frac{\tau_c}{(1 - \cos \Theta)_{avg}} \tag{6.35}$$

This $\tau$ is the relaxation time of the solid. It is the time constant for the exponential decay of a localized charge in the solid. It is this $\tau$ which must be used in the expressions for mobility. In the case of a pure solid where thermal vibrations produce the collisions, the direction of motion of the scattered electron after the collision is independent of its direction before the collision. As a result $(1 - \cos \Theta)_{avg}$ is unity and $\tau = \tau_c$. However, for impurity scattering (collisions with charged impurity ions) $\overline{\cos \Theta} \approx 1$ and $\tau \gg \tau_c$. If the mean free path for thermal vibrations is $\ell_T$ and for impurity scattering is $\ell_I$, then the resultant mean free path is given by

$$\frac{1}{\ell} = \frac{1}{\ell_T} + \frac{1}{\ell_I} \tag{6.36}$$

This means that for an impurity semiconductor, the mean free time as well as the concentration of carriers must be changed as the impurity concentration varies.

Signed: Donald J. Eckl
Donald J. Eckl

Approved: N. H. Taylor
N. H. Taylor

DJE:tl

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Memorandum M-2634


Richard S. DiNolfo
January 19, 1954

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: MULTI-COORDINATE SELECTION SYSTEMS FOR MAGNETIC-CORE STORAGE

STATEMENT OF THE PROBLEM

The purpose of this thesis is to consider the practicability of a magnetic-core memory system using more than three coordinates of selection and requiring selection ratios of less than 2 to 1.

HISTORY OF THE PROBLEM

When J. W. Forrester proposed the three-coordinate magnetic-core memory in the spring of 1950,[1] existing digital storage systems were utilizing either electrostatic storage tubes or devices requiring time and one space coordinate. The former resulted in bulky construction; the latter, in long access time.

It was the development of ferromagnetic materials with nearly rectangular hysteresis loops which made Forrester's proposal feasible. The basic element of a magnetic-core memory is a toroid of such a material with two remanent-flux states of opposite polarity used to arbitrarily represent the two digits (ZERO and ONE) of the binary system.

To understand the operation of a core memory, several facts about the hysteresis loop (Fig. 1) should be noted. If a core in the ONE state is excited with $I_m$ and the excitation is then removed, the core will "switch" to the ZERO state. Likewise, a core in the ZERO state can be switched to the ONE state by an excitation of $-I_m$. Excitations of $\pm \frac{I_m}{2}$ can at most change the flux state only slightly; except in a discussion of "noise" voltages the flux state can be considered unchanged.

Fig. 2 shows one digit of a three-coordinate array (i.e., there

is only one Z coordinate). As the core memory is used in Whirlwind I, the intersection of an excited X and Y plane selects a register, the word length of which is determined by the number of Z planes. The "read" operation consists of exciting the selected X and the selected Y plane with $\frac{I_m}{2}$ and observing the voltage induced in the "sense" winding of each digit (Z) plane. (The sense winding is one which goes through all the cores of a digit.) With this coincident-current type of readout, the following points should be noted:

1. Only one core in each Z plane is selected (excited with $I_m$); all others are either nonselected (no excitation) or half selected (excited with $\frac{I_m}{2}$). If the selection ratio is defined as the value of the excitation applied to the desired cores divided by the maximum excitation applied to any undesired cores, then the selection ratio is 2 to 1.

2. If a selected core is in the ONE state, a large voltage is induced in the sense winding, whereas a selected core in the ZERO state will induce only a small voltage; therefore, amplitude discrimination can be used to distinguish a ONE from a ZERO.

3. The read operation destroys the information if the core is in the ONE state and must therefore be followed by a "write" operation if the core is to be restored to its original state.

4. Half-selected cores induce unwanted voltages on the sense winding.[3]

The write which follows every read consists of exciting the selected X and the selected Y planes with $\frac{-I_m}{2}$ and in those digits where ZERO's are required exciting the Z plane with $\frac{I_m}{2}$. Therefore, the write

requires three coordinates, whereas the read requires two coordinates.

Two units employing the system described are now operating very reliably in Whirlwind I. Each unit consists of 1024 registers of 16-digit words and requires 144 vacuum-tube drivers to perform the selection.

PROPOSED SCHEME

The reliability of an electronic computer is to a large degree a function of the number of vacuum tubes. In a three-coordinate memory of the size described, the number of drivers is not excessive; however, with very large memories (see below), schemes to reduce the number of drivers are worth consideration. A means of doing this is to use N - coordinate systems ($N > 3$) with reduced selection ratios.[2]

Fig. 3 shows one digit plane of a possible system in which the read utilizes four coordinates and the write five. To read out of a register, the selected X coordinate, Y coordinate, and Z coordinate are excited with $\frac{I_m}{3}$ (this alone would fully select several registers, each of which lies on a different U coordinate), and all but one of the U coordinates is excited with $\frac{-I_m}{3}$ (of the registers fully selected by the X and Y and Z coordinates, only one remains selected).

For the write operation a fifth coordinate (V) is necessary to write ZERO in a digit. To write, the excitation on the X, Y, Z, and U coordinates is reversed, and in those digits where a ZERO is required the V coordinate is excited with $\frac{I_m}{3}$.

As an illustration of the reduction in drivers, consider a square digit plane of 256 cores on a side (65,536 registers). A tabulation for n digits is shown for both systems described.

| Three-Coordinate System | | Five-Coordinate System | |
|---|---|---|---|
| Read: | | Read: | |
| No. of X Drivers | 256 | No. of X Drivers | 16 |
| No. of Y Drivers | 256 | No. of Y Drivers | 16 |
| No. of Z Drivers | 0 | No. of Z Drivers | 16 |
| Write: | | No. of U Drivers | 16 |
| No. of X Drivers | 256 | No. of V Drivers | 0 |
| No. of Y Drivers | 256 | Write: | |
| No. of Z Drivers | n | No. of X Drivers | 16 |
| TOTAL | 1024+n | No. of Y Drivers | 16 |
| | | No. of Z Drivers | 16 |
| | | No. of U Drivers | 16 |
| | | No. of V Drivers | n |
| | | TOTAL | 128+n |

TABLE I

One drawback to increasing the number of coordinates is that the selection ratio decreases; consequently a core with a more rectangular hysteresis loop is needed (Maximum Selection Ratio = $\frac{N+1}{N-1}$ where N is the number of coordinates).[2] A more important drawback is the buildup of unwanted voltages from the partially excited cores. To illustrate this fact, the following derivation is made for the five-coordinate system described above.

Consider a square array $n^2 \times n^2$. Selection by the X and Y coordinates divides the array into three types of square arrays n x n, (i.e., a single array is excited with $\frac{2I_m}{3}$, 2 (n-1) arrays with $\frac{I_m}{3}$, and

$(n-1)^2$ arrays with 0 - Fig. 4). The final selection by the Z and U coordinates divides each n x n array into three types of cores, one with an additional $\frac{I_m}{3}$ excitation, 2(n-1) with no additional excitation, and $(n-1)^2$ with an additional $\frac{-I_m}{3}$. If it is assumed that the sense winding is wound as in the Whirlwind system[3], the following expression for the induced voltage applies:

$$V = 1\left[V_s - 2V_{2/3} \pm (n-2)\delta_{2/3} + V_{1/3} \pm \frac{n(n-2)}{2}\delta_{1/2}\right]$$
$$+2(n-1)\left[V_{2/3} - 2V_{1/3} \pm (n-2)\delta_{1/3}\right]$$
$$+(n-1)^2\left[V_{1/3} + V_{-1/3} \pm \frac{n(n-2)}{2}\delta_{-1/3}\right]$$

where

$V_s$ = the voltage output of the selected core;

$V_k$ = the voltage output of a core excited with $kI_m$;

$\delta_k$ = the difference between the average voltage output of the $kI_m$ - excited cores whose polarities on the sense winding are the same as that of the selected core and the average voltage output of the $kI_m$ - excited cores whose polarities on the sense winding are opposite to that of the selected core.

Simplifying

$$V = V_s + 2(n-2)V_{2/3} - (4n-5)V_{1/3} \pm n\delta_{2/3} \pm \frac{n^4-4n^3+12n^2-20n+12}{2}\delta_{1/3}$$

A similar expression can be obtained for the three-coordinate system.[4] $V = V_s - 2V_{1/2} \pm (n^2-2)\delta_{1/2}$

Using experimental data from single cores (General Ceramics type body MF1326-B, F-394 die size) and the two expressions given above,

the three-coordinate system can be compared with the five-coordinate system. For a 64 x 64 digit plane, the convergence ratio (ratio of largest possible ZERO readout to the smallest possible ONE readout) for the three-coordinate system is 2% whereas it increases to 14% for the five-coordinate system. However, it should be noted that the type of core used (the memory core now used in the three-coordinate system) is not necessarily a desirable type for the five-coordinate system. Any investigation to determine the practicability of such a system must include a study of the existing cores to determine which will operate most successfully at lower selection ratios.

PROPOSED PROCEDURE

The investigation will proceed as follows:

1. Investigation of cores

Single cores will be tested to determine which materials will allow a selection ratio smaller than the 2 to 1 ratio used now. Factors to be considered are excitation current, switching time, rectangularity of the hysteresis loop, and the relative sizes of the ONE, ZERO, and partially selected outputs.

2. Investigation of selection schemes

The general theory of selection will be reviewed and extended where possible, with special consideration given to a specific N-coordinate scheme to be decided upon after completion of Part 1 and consideration of the theoretical and practical problems involved. This will require an investigation of the number and complexity of the drivers necessary, the sensing problems, and the construction requirements.

EQUIPMENT NEEDS

The magnetic cores and the equipment necessary for testing the cores are available at the MIT Digital Computer Laboratory.

ESTIMATED DIVISION OF TIME

| | | |
|---|---|---|
| 1. | Preparation of proposal..... | 40 hours |
| 2. | Further study of literature..... | 40 hours |
| 3. | Experimental work and analysis..... | 150 hours |
| 4. | Correlation of results and formulation of deductions and conclusions..... | 100 hours |
| 5. | Preparation of thesis report..... | 70 hours |
| | TOTAL | 400 hours |

Signed: Richard S. DiNolfo
Richard S. DiNolfo

RSD/rb Date: January 19, 1954

Supervision Agreement

The problem described herein seems adequate for a Master's thesis. The undersigned agrees to supervise the research and evaluate the thesis.

Signed: William K. Linvill
William K. Linvill

Dudley A. Buck
Dudley A. Buck

Distribution List:

Group 62 - Staff
David R. Brown
James R. Freeman
Joseph H. McCusker

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2. Everett, R. R., "Selection Systems for Magnetic Core Storage," Engineering Note E-413 (August 7, 1951), MIT Servomechanisms Laboratory.

3. Guditz, E. A., "Delta $\Delta_s$ in Ceramic Array #1," Engineering Note E-488 (October 14, 1952), MIT Digital Computer Laboratory.

4. Freeman, J. R., "Pulse Response of Ferrite Memory Cores," Memorandum M-2568 (December 15, 1953), MIT Digital Computer Laboratory.

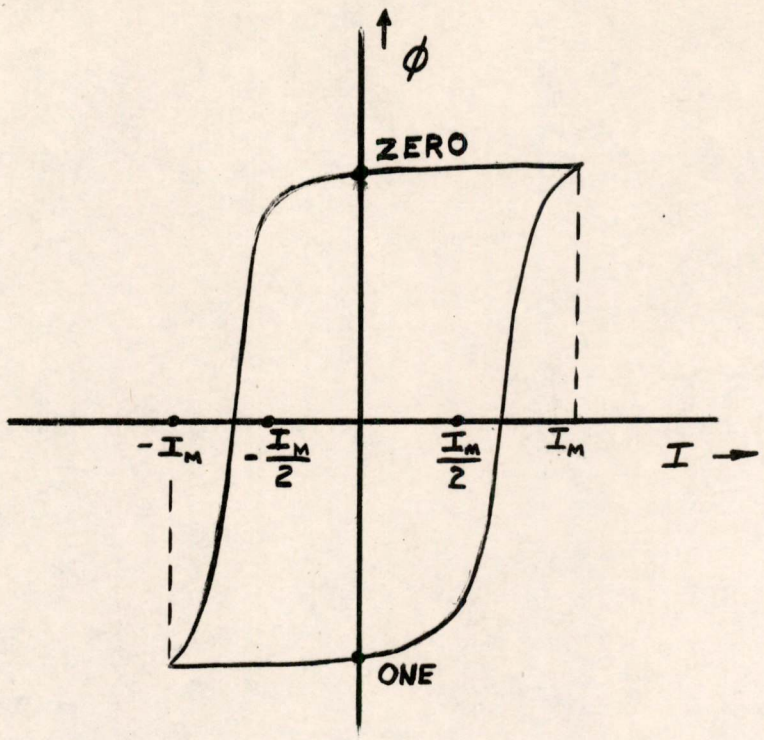
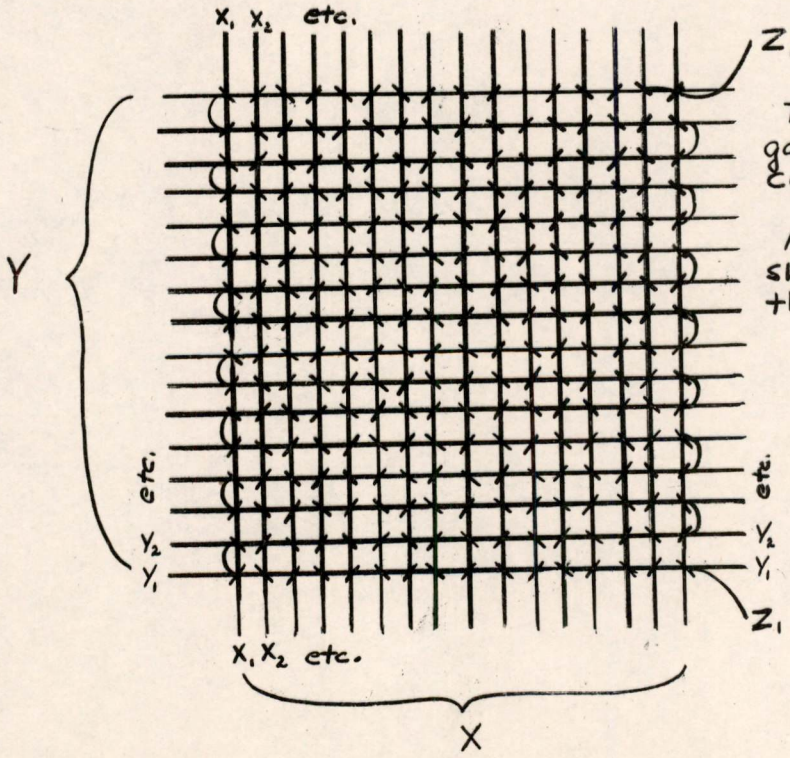


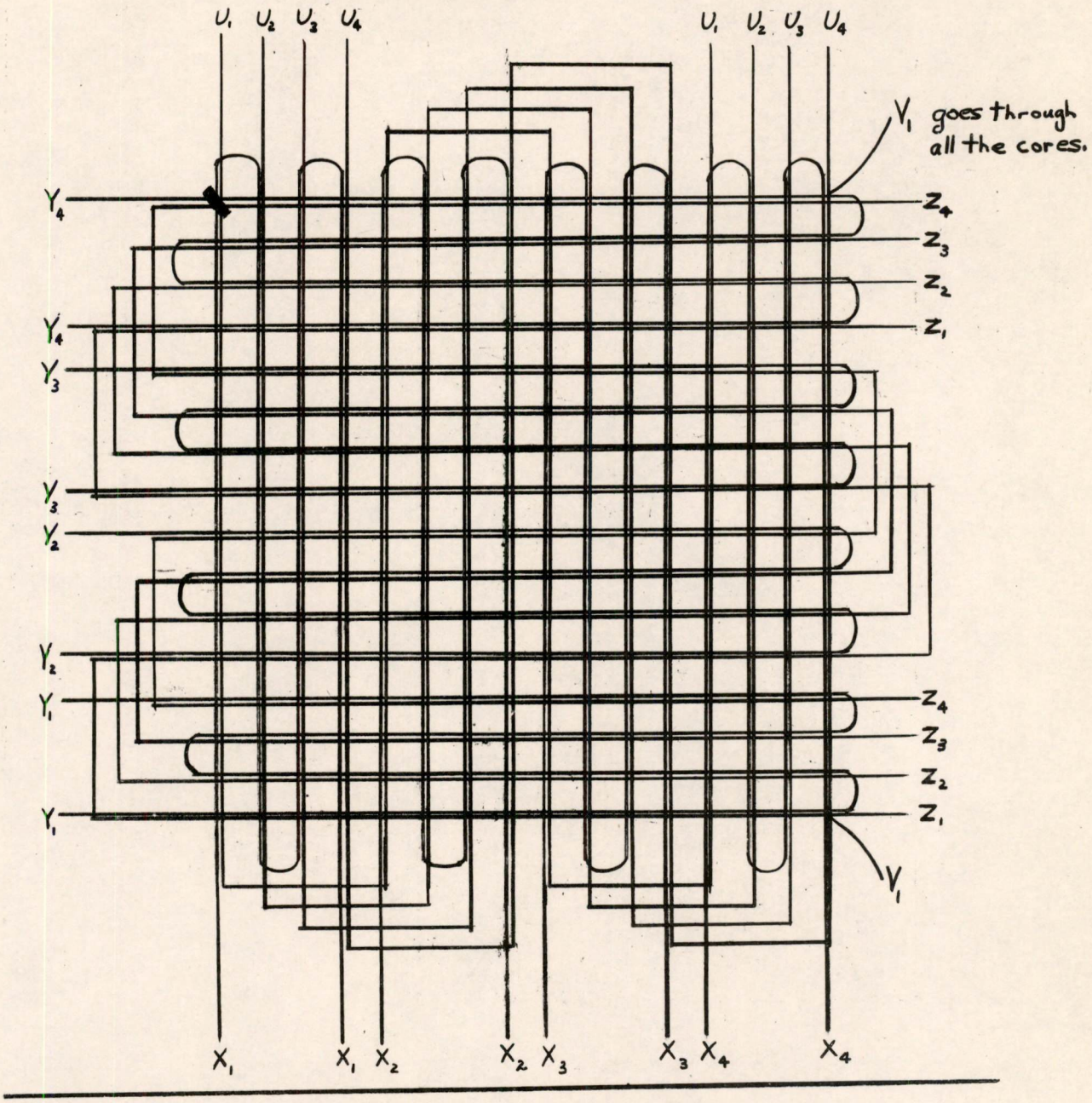

FIG. 1




The $Z_1$ coordinate goes through all the cores.

A "sense" winding which should go through all the cores is not shown.

FIG. 2


U1 U2 U3 U4
U1 U2 U3 U4
Y1 goes through all the cores.
Y4
Y4
Y3
Y3
Y2
Y2
Y1
Y1
Z4
Z3
Z2
Z1
Z4
Z3
Z2
Z1
Y1
X1
X1 X2
X2 X3
X3 X4
X4

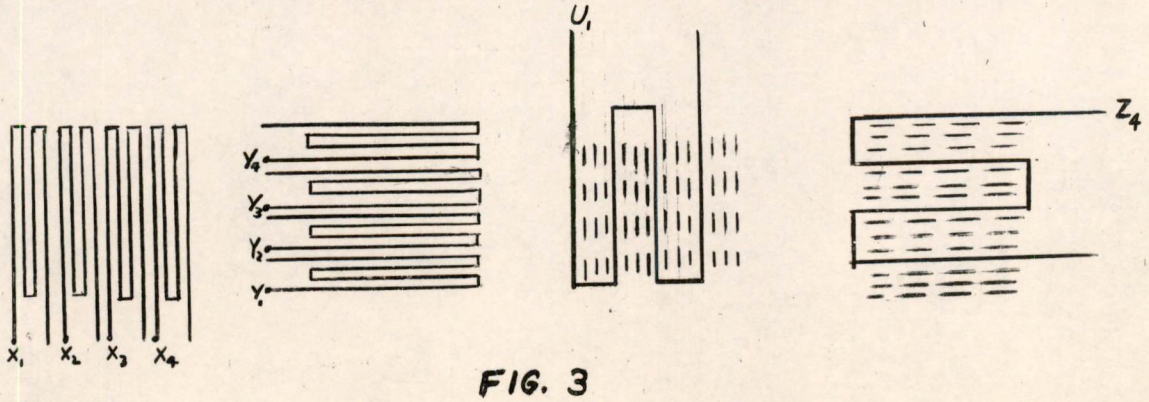
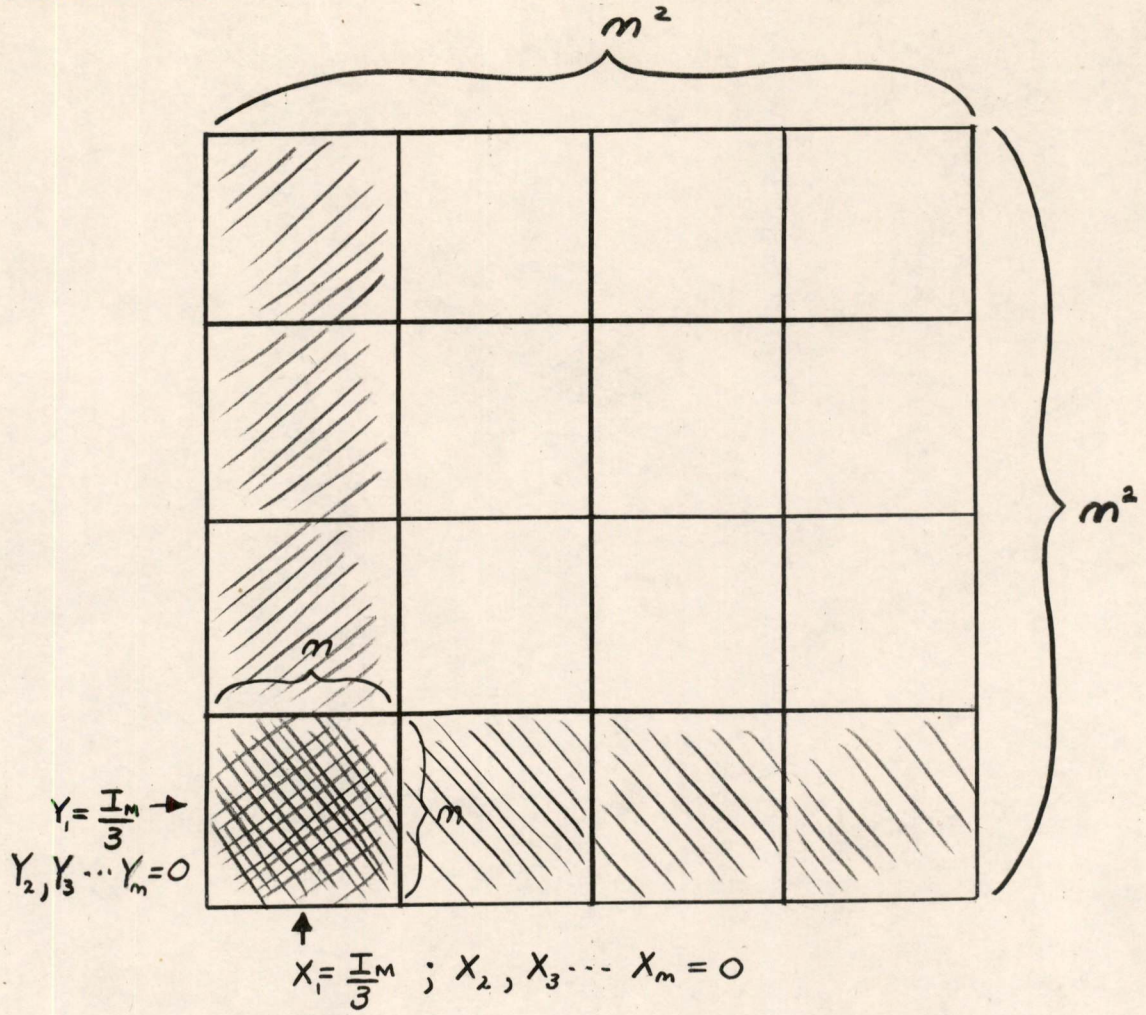

X1 X2 X3 X4
Y4
Y3
Y2
Y1
U1
Z4

FIG. 3


$m^2$
$m^2$
$m$
$m$
$Y_1 = \frac{I_M}{3}$
$Y_2, Y_3 \cdots Y_m = 0$
$X_1 = \frac{I_M}{3}$ ; $X_2, X_3 \cdots X_m = 0$

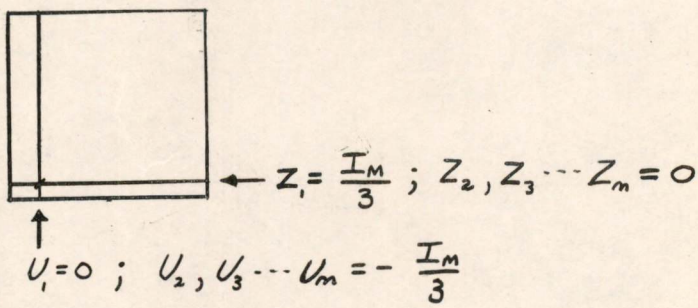

$Z_1 = \frac{I_M}{3}$ ; $Z_2, Z_3 \cdots Z_m = 0$
$U_1 = 0$ ; $U_2, U_3 \cdots U_m = -\frac{I_M}{3}$

FIG. 4

Olsen



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: COMPONENT TEST REPORT: PULSE TRANSFORMERS, HERMETICALLY SEALED, WITH FERRITE CORES

To: N. L. Taylor, IBM

From: R. J. Biagiotti

Date: January 18, 1954

References: IBM Test Number 5000-5021-97-123-82
MIT Job Number 015-M123

**********

Object: To evaluate potential reliability and suitability for use in AN/FSQ-7 equipment of pulse transformers built to IBM specifications.

Description of Material: Manufacturer: Sprague Electric Company

Part Numbers: IBM 5001-00001 (3:1 ratio)
IBM 5001-00003 (4:1 ratio)

Construction: According to IBM Engineering Specification 5001-43008

Conclusions: The transformers examined appear to be potentially unreliable due to the poor workmanship which went into their construction. These transformers do not meet requirements described in IBM Engineering Specification 5001-43008.

Procedures and Results:

Summary. The following tests were performed on the number of transformers indicated.

| Test | Number of Units | | |
|---|---|---|---|
| | 1:1 | 3:1 | 4:1 |
| Insulation Resistance | | 7 | 7 |
| Voltage Breakdown | | 8 | 8 |
| Pulse Breakdown | | 6 | 5 |
| Life Test | 6 | | |
| PRF Sensitivity | | 5 | 5 |
| Pulse Output Amplitude | | 5 | 5 |
| Visual Inspection | | 3 | 5 |
| Temperature Rise | | | 1 |

Procedure and Results: (continued)

INSULATION RESISTANCE

Procedure: Insulation resistance of 14 units, 7 of each type, was measured at temperatures ranging from room temperature (25° C) to 85° C at 500 volts d-c with a General Radio Type 1862-A Megohmmeter. Temperature was raised in 10° C steps, holding the transformers in an oven for one hour prior to resistance measurement. Resistance measurements were made one minute after voltage was applied.

Results: Resistances in Megohms x 1000.

| Temp. | Unit #1 | #2 | #3 | #4 | #5 | #6 | #7 |
|---|---|---|---|---|---|---|---|
| 3:1 Transformers | | | | | | | |
| | Winding-to-Winding Resistance | | | | | | |
| | Without Plastic Sleeve | | | | | With Plastic Sleeve | |
| Room | > 2000 | ∞ | > 2000 | ∞ | ∞ | > 2000 | > 2000 |
| 35° | 2000 | 2000 | 2000 | 1800 | 2000 | > 2000 | 2000 |
| 45° | 1500 | 2000 | 2000 | 2000 | 2000 | 2000 | 1500 |
| 55° | 900 | 1500 | 1200 | 1800 | 1200 | 1500 | 1500 |
| 65° | 600 | 800 | 900 | 2000 | 900 | 800 | 800 |
| 75° | 300 | 600 | 600 | 1500 | 550 | 500 | 520 |
| 85° | 150 | 220 | 220 | 900 | 190 | 140 | 210 |
| | Winding-to-Case Resistance | | | | | | |
| Room | > 2000 | ∞ | ∞ | ∞ | > 2000 | Above | |
| 35° | 2000 | 2000 | 2000 | 1800 | 2000 | | |
| 45° | 1800 | 2000 | 2000 | 2000 | 2000 | Range | |
| 55° | 1500 | 2000 | 1500 | 1800 | 1500 | | |
| 65° | 1000 | 2000 | 1000 | 1800 | 1500 | of | |
| 75° | 800 | 600 | 2000 | 1500 | 1500 | | |
| 85° | 500 | 1500 | 190 | 900 | 800 | Instrument | |
| 4:1 Transformers | | | | | | | |
| | Winding-to-Winding Resistance | | | | | | |
| Room | 2000 | > 2000 | > 2000 | > 2000 | > 2000 | > 2000 | > 2000 |
| 35° | 1800 | 1800 | 1000 | 2000 | 1800 | 2000 | 2000 |
| 45° | 1500 | 1800 | 700 | 1500 | 1200 | 1500 | 1800 |
| 55° | 850 | 650 | 600 | 1000 | 900 | 550 | 750 |
| 65° | 450 | 450 | 300 | 550 | 450 | 350 | 450 |
| 75° | 330 | 260 | 150 | 350 | 330 | 180 | 190 |
| 85° | 130 | 58 | 50 | 130 | 140 | 63 | 64 |
| | Winding-to-Case Resistance | | | | | | |
| Room | > 2000 | > 2000 | > 2000 | ∞ | > 2000 | Above | |
| 35° | 2000 | 2000 | 2000 | 2000 | 1800 | | |
| 45° | 2000 | 2000 | 1800 | 2000 | 1800 | Range | |
| 55° | 1500 | 1500 | 1800 | 1500 | 1800 | | |
| 65° | 1200 | 1200 | 1200 | 1200 | 1500 | of | |
| 75° | 1000 | 900 | 1000 | 1000 | 1000 | | |
| 85° | 800 | 800 | 800 | 700 | 800 | Instrument | |

The average winding-to-winding resistance is shown in Figure I.

Procedures and Results: (continued)

VOLTAGE BREAKDOWN

Procedure: Breakdown voltages were measured on 16 units with a hipot unit capable of applying 7600 volts d-c. The test was made between windings in all transformers. On four units, breakdown voltage was measured between the windings tied together and a piece of copper foil wrapped tightly around the outside of the plastic sleeve. On the other ten units voltage was applied between the windings together and the can.

Results:

Breakdown Voltages

| Type | Unit | Winding-to-Winding | Winding-to-Case |
|---|---|---|---|
| 3:1 | #1 | - | 6500 |
| | #2 | - | 6000 |
| | #3 | - | 4000 |
| | #4 | - | 7400 |
| | #5 | - | 5500 |
| | #6 | - | - |
| | #7 | 6800 | - |
| 4:1 | #1 | - | 6500 |
| | #2 | After 26 sec. at 7600 | 6500 |
| | #3 | After 6 sec. at 7600 | 6000 |
| | #4 | - | 5500 |
| | #5 | - | 6500 |
| | #6 | 7100 | - |
| | #7 | - | - |

Except where noted, transformers were held 30 seconds at 7600 V. without breakdown.

The breakdowns correlated with the insulation resistance measurements at elevated temperatures to the extent that all the transformers that broke down between the windings had insulation resistances below 100,000 megohms at 85° C, and the transformer which broke down between windings and case decreased in resistance by a factor of 10 when raised from 75° C to 85° C.

PULSE BREAKDOWN (Interturn)

Procedure: Eleven units were tested, 5 - 4:1 transformers and 6 - 3:1 transformers, by applying 0.1 microsecond pulses at a repetition frequency of 1 mc to the secondary and measuring the pulse amplitude at the primary with a Tektronix 514D Oscilloscope. The primary was terminated in 1500 ohms for the 4:1 transformers, and 1000 ohms for the 3:1 transformers.

Procedures and Results: (continued)

PULSE BREAKDOWN (continued)

Results: The maximum pulse output across the primary of the transformers was 280 volts for 4:1 transformers and 220 volts for 3:1 transformers. These were obtained with input pulses of 80 and 85 volts respectively. These limits were imposed by the equipment at hand, and not by the transformers. The pulse shape was good at these high voltages showing no indication of distortion due to saturation or inter-turn shorting. There was no decrease in transformation ratio as the pulses were increased. Negative overshoot was about 25% of the pulse maximum.

LIFE TEST

Although no life test was performed on the samples submitted, a test was made on six Sprague 1:1 transformers of similar construction from August 14 to September 4, 1953. The results of this test are presented herein.

Procedure: Initial insulation resistance of each transformer was measured at 500 volts d-c with one minute electrification with a General Radio 1862-A Megohmmeter. Transformers were soldered to turret lugs, and the mounting board assemblies were placed in a chamber maintained at 85° centigrade and 90-95 percent relative humidity for 500 hours. A d-c potential of 300 volts was maintained between windings. Insulation resistance was measured again, immediately after removal, and again after 24 hours at room temperature.

Results: No dielectric breakdowns occurred during the period of the test. The values of insulation resistance prevailing initially, and 24 hours after cessation of the test, are shown below:

| Unit # | Initial I.R. at 28° C | Final I.R. at 25° C |
|---|---|---|
| 1 | 2.0 million meg. | 2.0 million meg. |
| 2 | 1.6 " " | 1.5 " " |
| 3 | 2.0 " " | 2 + " " |
| 4 | 2.0 " " | 2.0 " " |
| 5 | 1.8 " " | 2.0 " " |
| 6 | 1.7 " " | 2 + " " |

PRF SENSITIVITY

Procedure: The sensitivity to pulse-repitition-frequency was measured on 10 units by applying bursts of 10 standard 0.1 microsecond pulses at a repitition frequency of 2 mc separated by an interval longer than three times the burst length. The bursts were observed on a Tektronix 513D Oscilloscope.

Results: All ten units showed a 10% decrease in pulse amplitude from first to last pulse.

Procedures and Results: (continued)

PULSE OUTPUT AMPLITUDE

Procedure: Output pulse amplitude of 10 units was measured using the test circuit on sheet 16 of IBM Engineering Specification No. 5001-43008. The input was modified so that a BNC connector could be used, and the output was modified to be used with a Coupling Unit (MIT Drawing A-52350) and a Tektronix 514D Oscilloscope. Calibration was provided by a recently calibrated Simpson Multimeter on the 0-50 volt d-c range.

Results: Using the test circuit the variation in output pulse amplitude within the sample used was small. The average, maximum, and minimum values are listed below.

| | 3:1 | 4:1 |
|---|---|---|
| Maximum | 16.5 volts | 18.0 volts |
| Average | 16.3 | 17.3 |
| Minimum | 16.1 | 16.8 |

TEMPERATURE RISE

Procedure: The temperature rise of the core and windings was measured by drilling a small hole in the case and placing a copper-constantan thermocouple against the core. A Leeds and Northrup #8657C potentiometer with internal reference junction was used to measure thermal emf. Currents ranging from 0 to 150 milliamperes d-c were passed through the primary winding.

Results: Core temperature increased less than 1° C with 150 milliamperes passing through the primary for 25 hours.

VISUAL INSPECTION

Procedure: Eight units were dissected by removing the outer can and melting the potting wax in an oven held at 100° C.

Results: Six of the eight transformers dissected had turns bunched or crossed. In all cases the primary was at fault. All five 4:1 transformers had the primary bunched and turns crossed, and one 4:1 transformer also had turns crossed on the secondary winding. Only one 3:1 transformer had turns crossed in any winding.

Five of the transformers had no slack in the lead from the winding to the soldered connection on the phenolic mounting board. In all cases the lead without slack came from under the core; one transformer had in addition a taut lead from the top of the core.

Five transformers had loose winding wire ends projecting from the soldered connection at the phenolic board where the winding is connected to the pigtail. These loose ends varied in length from 1/16 to 1/8 inch, approximately.

Procedures and Results: (continued)

VISUAL INSPECTION (continued)

Results: (continued)

Four transformers had bends or kinks in the windings. Three were 4:1 transformers and one was a 3:1 transformer.

In two transformers, one end of the Kraft paper can liner was charred. It appeared that the paper was charred in soldering the metal can to the ring around the glass end-seal.

There were two transformers in which the core insulating lacquer was chipped or blistered.

One transformer had a primary turn displaced about ninety degrees and a number of dark specks deposited upon the core near the secondary.

One transformer had no center post to support the core, which was fastened to the fibre board by transparent scotch tape.

The potting on all transformers was quite poor, containing many large blow-holes and air inclusions.

The marking system on the transformers was different; the 3:1 transformers had an orange band around the primary and black printing while the 4:1 transformers had only yellow printing.

Signed R. J. Biagiotti
(R. J. Biagiotti)

Approved B B Paine
(B. B. Paine)

Approved Hugh Wainwright
(Hugh Wainwright)

RJB:bbp:hw:mrs

cc: N. L. Taylor, IBM (20 copies)
H. Wainwright
C. W. Watt
Standards Office

Drawings attached:

A-57699 (Figure I)

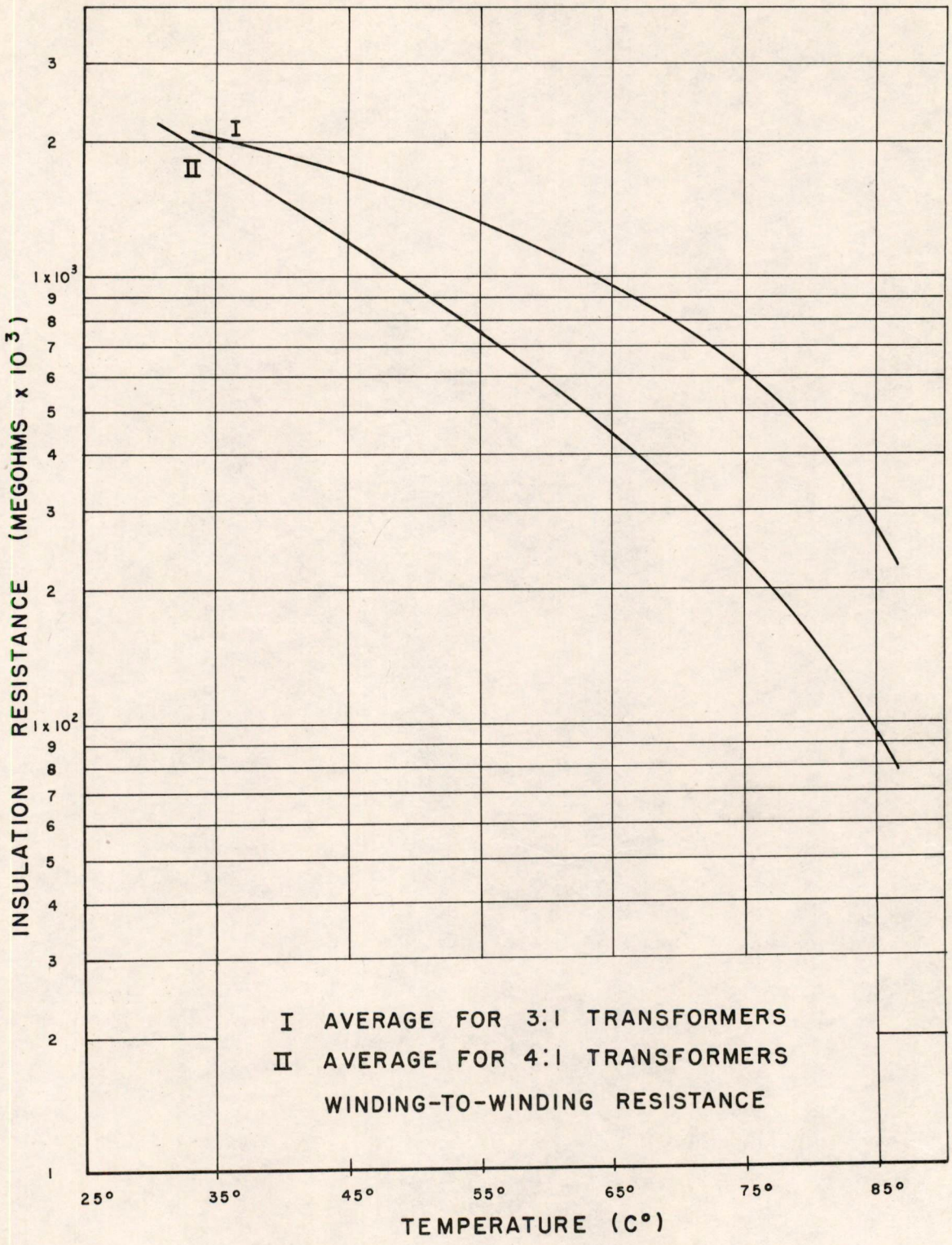



FIG. 1

SPRAGUE PULSE TRANSFORMER
INSULATION RESISTANCE

A-57699

R. Blad



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: REVERSE RECOVERY MEASUREMENTS OF DIODES

To: Transistor Distribution 3

From: Nolan T. Jones

Date: November 30, 1954

Approved: D. J. Eckl by N.T.J.

D. J. Eckl

Abstract: The "turn-off" or reverse-recovery characteristics of point, bonded and junction diodes are analyzed experimentally on the basis of Kingston's theory. The design of flexible and accurate measurement circuits is discussed and two general purpose circuits are described. The turn-off time, $\tau_2$, in planar-junction diodes is shown to fit the theory quite well. In such devices $\tau_2$ is a function of the ratio of the short-circuit reverse current to the forward current, $I_{RM/I_f}$, and the hole lifetime, $\tau_p$, with a noticeable decrease in $\tau_p$ at high forward currents. The $\tau_2$ of these diodes varies from about 3 $\tau_p$ to 0.1 $\tau_p$ over the range of $I_{RM/I_f}$ from 0.1 to 10. $\tau_p$ may be as low as 1 μsec in silicon-alloy junction diodes to larger than 50 μsec. in high-quality grown-junction diodes. $\tau_2$ in point and bonded diodes is shown to be a function of contact area or forward resistance, and reverse voltage as well as $I_{RM/I_f}$ and $\tau_p$, but the exact relationships depart from theory. In these devices $\tau_2$ is shown to be a linear function of forward current with back voltage constant. This slope is 0.02 μsec/ma $I_f$ for the Sylvania 1N34A and 0.1 μsec/ma $I_f$ for a Transitron T5 at 35 volts with 2000 ohms series resistance. $\tau_2$ in point diodes is nearly constant with increasing back voltage above about 20 volts with a constant series resistance of 2000 ohms. For constant $I_{RM/I_f}$ $\tau_2$ increases with increasing back voltage. $\tau_2$ is a direct function of the time that forward current flows,



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

$t_f$, prior to reverse-switching up to limiting values of $t_f$. $\tau_2$ becomes constant for $t_f$ above these limiting values. For planar-junction diodes the limiting value of $t_f$ is about 3 $\tau_p$ while in point and bonded diodes this limit is apparently related to the whisker contact area.

## 1.0 Introduction

The subject of reverse recovery of all types of both silicon and germanium diodes is currently receiving considerable attention among engineers in this laboratory and others. This interest is indicated by the several recent papers on the subject listed in the bibliography*. Special note should be made of Kingston's paper[1] since the work in this memorandum constitutes, in part, experimental verification of his theoretical treatment.

## 1.1 The Problem

A theorectically perfect diode from an applications standpoint would be a true bi-valued element, a short circuit in the forward direction and an open circuit in the back direction. In addition this diode would include no reactive characteristic components so that it would switch in zero time in either direction.

Practical diodes have many limitations. Two of these inherent in semi-conductor diodes are reverse- and forward-recovery times, transition periods during which the diode switches from one direction to the other. Forward-recovery, when the diode switches from the reverse to forward conduction state, will not be discussed in detail.

## 1.2 Circuit Description of Reverse-Recovery

The reverse-recovery characteristics of a given diode are the responses of that diode when it is switched from the forward to reverse conduction direction under the application of various circuit switching conditions. These may be described as follows:

1) Initial conditions: A forward current flowing.
2) Action: A reverse voltage applied to the diode through a fixed resistance.
3) Reaction: Diode current will be initially large with respect to the normal quiescent reverse current and will drop to that quiescent value in a characteristic time interval.

* Superscripts refer to numbered references in the bibliography.

In a junction diode the initial voltage drop during this interval is comparable to the forward drop immediately before switching. In the point-diode case the initial voltage drop is a sizeable fraction of the applied back voltage.

1.3 Physical Description of Reverse-Recovery

For forward voltage drops of 0.1 volt and higher[3] forward current in semi-conductor diodes is carried by minority carriers, holes flowing (or diffusing) from the p-region into the n-region and electrons flowing in the opposite direction. Due to the methods with which nearly all such diodes are constructed the lifetime of electrons in the more heavily doped p-region is much smaller than the lifetime of holes in the less heavily doped n-type material. For this reason the electron flow is often neglected in calculations of forward conduction in such diodes and related devices.

In a diode passing a forward current a large number of holes are flowing into the n-region. If the diode has been conducting in the forward direction for a time which is large with respect to the hole lifetime than the hole density reaches a steady-state distribution. When the diode is switched these minority carriers must disappear before the diode will reach its steady-state reverse characteristic. These "stored" holes may be removed by the initially large reverse current, and in point and bonded diodes by the reverse fields; or they may die by recombination with electrons. The reverse-recovery characteristics for high-quality junction diodes may be obtained as transient solutions to the diffusion equation with the steady-state forward-conduction hole distribution as the boundary condition. Special cases of this problem have been solved by Kingston[1] and others[4,5]. In point and bonded diodes reverse fields tend to speed the removal of the stored holes. In point diodes current multiplication, in the manner of point-transistor collectors, prolongs the current transient.

1.4 Other Names for Reverse-Recovery

As described above reverse-recovery is due to the storage of minority carriers. If the storage of electrons in the p-region is neglected then "minority-carrier storage" reduces to the popular term "hole storage". Since electron storage can be neglected in commercially avail-

able units this term is certainly valid.

The magnitude of the reverse current due to storage and the time required for it to reach a prescribed value are of interest to the circuit designer. This has led to the use of several terms, such as clean-up time, enhancement current, clearing time, switching time, etc. The term reverse-recovery is used here for clarity and generality.

## 2.0 Measurement Circuit Design

A representative diode switching circuit is illustrated in Figure 3.1a. Forward current is supplied to the diode by the current generator, $I_f$. Diode switching occurs when switch S is moved instantaneously to the right, applying a back voltage to the diode through a series resistance $R_s$, generally much smaller than the quiescent back resistance of the diode. Either the voltage across the diode or the current through it may be observed in each of the three circuits discussed in this section.

Another representative diode switching circuit is shown in Figure 3.1b. Battery $V_f$ supplies forward current to the diode through the series resistance $R_s$ with the switch arm S in the upper position. When S moves instantaneously to its lower contact the diode is switched. Nearly all switching applications of diodes may be reduced to a circuit of this form.

A third circuit, in which part of the series resistance is changed at the same time that switching conditions are applied to the diode, is shown in Figure 3.1c. This type of circuit is advantageous in measuring good point diodes, since it results in a scale change between forward and reverse currents.

Inspection of these representative circuits indicates a basic difference between circuit a and circuits b and c. The latter two are series circuits in which the back voltage is applied in series with the forward voltage supply, while circuit a is a shunt circuit, applying forward and reverse conditions to the diode alternately.

The Bell Labs variety of reverse-recovery measuring circuits [4,6,7] are of the shunt type, in which switching is accomplished with relays having mercury-wetted contacts. The IBM variety of circuit [7,8,9,10] is a series circuit in which part of the series resistance is switched

(Figure 3.1c above). In the series type, back voltage is generally supplied with pulse and square wave generators. The measuring circuits to be described and used in this work are of types b and c.

Use of either switching device has some disadvantages. The low repetition frequencies (under 100 cps) at which the special relays may operate produce faint traces at oscilloscopic sweep rates of the order of 0.1 microsecond per centimeter. However, they are certainly two orders of magnitude lower in cost than suitable generators, and rise times of a few millimicroseconds are achieveable. Since external batteries (or power supplies) and resistors control the switching conditions these relay circuits are flexible in this respect. Square wave and pulse generators have rise time and output magnitude limitations. However there are several units available that have outputs of tens of volts with rise times less than 50 millimicroseconds and are therefore suitable for many reverse-recovery measurements.

## 2.1 General Measurement Circuit

The general-purpose test circuit used in this work is shown in Figure 3.2. The forward current is supplied by battery $V_f$ to the diode through the series circuit consisting of the load resistor $R_L$ in series with the parallel combination of the generator internal resistance $R_g$ and the terminating resistor $R_t$. This total series loop resistance is designated $R_s$ in the manner of the illustrative circuits above. The diode current is measured as the drop across the load resistor at the terminal labelled $I_D$. A simple integrating circuit may be added as shown to obtain the integral of the diode current. However, accuracy and equipment manipulation problems eliminated the use of this integrator circuit. The net back voltage applied to the diode is the difference between the generator voltage at the terminating resistor and the forward voltage $V_f$. This net back voltage is abbreviated $V_r$.

## 2.2 Point Diode Measurement Circuit

Figure 3.3 shows the reverse recovery waveforms of a poor point diode and two types of junction diodes operating under identical switching conditions in the test circuit above. Since the waveform of the point diode is masked by the initial fall of the current waveform a small horizontal line denotes the negative current peak of this diode. The magni-

tude of this reverse recovery or storage "spike" in most point diodes is so small that it is barely distinguishable on this scale. For this reason a particularly poor point diode was used for this illustration and a special circuit must be used to measure good point diodes.

This test circuit is shown in Figure 3.4 and has the form of c of the illustrative switching circuits. Load switching is accomplished with diode $D_L$. $D_L$ may be vacuum diode[8] or specially selected silicon[9] or germanium diodes. The shunt capacity of vacuum diodes add to load capacity $C_L$, the effect of which will be discussed in the next few paragraphs. A semi-conductor diode in this position must have excellent reverse recovery characteristics, much better than any diodes to be tested in the circuit. A poor diode as $D_L$ reduces both the measured storage spike amplitude and the indicated turn-off time of the tested diode.[8]

Since the reverse-recovery transients have high-frequency components of the same order as the back voltage source, preservation of these components requires that the load capacity $C_L$ must not act as a bypass. In making measurements of this sort all time constants involved in the measurement must be critically chosen. The rise time capabilities of the driving generator and scope are largely matters of cost and availability of equipment while the allowable time constant of the load is a compromise including several factors. Scope sensitivity and signal swing require that the capacity reducing attenuator be small and $R_L$ be large, while exact reproduction of the waveform would require that the load time constant of $R_L$ and $C_L$ be very small. These considerations plus such others as desired switching conditions, measurement accuracy, and available components of the system, specify the measurement circuit. In the work reported here several combinations of equipment and circuits are used. The point diode test employs a Tektronix 105A square wave generator, a Tektronix 513D Scope (0.025 microsecond rise time response), an $R_L$ of 1800 ohms, the 2:1 attenuator shown in Figure 3.4, and a Sylvania type 5647 subminiature high-perveance diode for load switching. The load time-constant is 0.04 microsecond. In a circuit similar to the one above Aronson[9*] duplicated the reverse recovery waveforms of poor point and bonded diodes by shunting a Sylvania 1N34A diode with small

* This fact is not specifically reported in reference 9.

capacities. Therefore in order to minimize erroneous results, the capacity between diode test clips must be kept to an absolute minimum. A heavy copper capacitive shield between input and output was used to accomplish this. This is apparent in Figure 3.5, front and rear views of the point diode test circuit and front view of the general test circuit. Good VHF techniques must be used in the construction of these circuits. Grounds should be heavy bus wire; leads must be kept short; good components used, and components strategically located, as shown in Figure 3.5.

Figure 3.6 shows a typical point-diode reverse-recovery waveform using the standard circuit. The effect of $C_L$ on this waveform is shown in Figure 3.7. In the first case 120 mmfd was added in parallel with the load, and in the second 47 mmfd was added. Since the magnitude of the reverse-current transient and the time it takes to decay to a specified value are the quantities of interest in this measurement, the need to keep the load capacity minimized is obvious.*

3.0 Definitions of Terms

Figure 3.8 is the reverse-recovery current waveform for a grown-junction diode. During the first 10 microseconds the back resistance of the diode is of the same order as its forward resistance before switching, and the diode current is determined by the series circuit resistance and the back voltage source. Note that the reverse current during this phase is 21 ma. whereas the forward current was 10 ma. At $t = \tau_1$ the diode begins to open and the current tends to its normal quiescent value.

3.11 Reverse-Recovery Terms

Several useful definitions from Figure 3.8 and the above discussion are listed below:

$I_f$ = Diode forward current immediately before switching.

$t_f$ = The time that forward current flows.

$V_f$ = The supply voltage that furnishes forward current.

$V_r$ = The net back voltage applied to the diode.

$$V_r = V_{generator} + V_f$$

$R_s$ = The external series resistance in the reverse bias direction.

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* Although one popular test circuit has about 100 mmf. $C_L$.

$I_{RM}$ = The maximum available reverse current, a function of the circuitry external to the diode. $I_{RM} = \frac{V_r}{R_s}$

$\tau_1$ = Saturation time of the back voltage source, the flat portion of the waveform of Figure 3.7.

$\tau_2$ = Turn-off time. In the case of large area junction diodes this is defined as the time required for the transient reverse current* to decay to 10% of $I_{RM}$. In the case of point and bonded diodes this may be defined as the time for the transient reverse current to decay to 2% of $I_{RM}$. The definition used at any particular time will be clearly noted. The symbol is located arbitrarily on the waveform of Figure 3.8, actual location is in accordance with the definition used.

Storage spike = The maximum observed reverse current. In a large area junction diode this is $I_{RM}$. In point diodes it may be a measured quantity. In the point diode of Figure 3.3 the storage spike is 5 ma., in Figure 3.6 it is 0.8 ma.

$Q_s$ = Storage charge, the shaded area under the waveform of Figure 3.8. This is the charge that is removed in switching the diode.

$$Q_s = \int_0^T (i_r)\, dt$$, where $i_r$ is the transient reverse current and the upper time limit is taken sufficiently long for the transient to die out. This quantity is of interest when considering the energy required to switch the diode, but will not be discussed further here.

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* The reverse current of a diode will be considered to be composed of a steady-state or static component, plus a transient reverse-recovery or storage component that decays to zero.

3.2 Discussion of Turn-Off Time Definitions

The double definition of turn-off time is dictated by the nature of the switching characteristics for the different diodes. The definition to 10% of $I_{RM}$ for junction diodes is the same as that used by Kingston[1], and specifies the time for the diode's transient component of back resistance to reach a value of 9 times the circuit's series resistance $R_s$. This is insufficient for many applications, but a tighter definition would lead to larger errors in measurements in which it is already difficult to keep errors below the order of 10%. These additional errors would be introduced by the necessity of measuring time values from a waveform whose time rate of change is relatively small and by the problem of determining a small fraction of a large signal swing.

Point diodes and the special test circuit of Figure 3.4 invert the difficulties. Since the storage spike in good point diodes is often less than 10% of $I_{RM}$ the tighter definition must be used to get any significant measurements. The current scale change in the point diode test circuit makes it possible to obtain reasonably accurate measurements.

3.3 Discussion of Point-Diode Measurement Limitations

Theoretically, point diodes would have a characteristic waveform similar to the junction-diode waveform of Figure 3.8, but the times involved are such that $\tau_1$ may be the order of only a few millimicroseconds. To produce and observe such a waveform would require a switching source and an oscilloscope with rise time capabilities of the order of a millimicrosecond. Waltz[6] used equipment of this type in his experiment. Philosophically it might be desirable to use such equipment for these measurements. However, from two practical standpoints, availability of equipment and intended use of the results, a lesser compromise is sufficiently accurate. But the limits should be defined and kept in mind when considering the measurement results. In the test circuit of Section 2.2 the overall response of about 0.04 μsec. is as good or better than the rise times to be found in nearly all applications of these diodes in this laboratory, so it was considered adequate.

## 4.0 Relationships of Reverse Recovery Characteristics to Circuit and Diode Parameters

Summarizing the relevant parameters, the reverse-recovery dependent variables are saturation time $\tau_1$, turn-off time $\tau_2$, storage charge $Q_s$, and storage spike amplitude. The maximum power dissipated by the diode will be discussed in section 4.4. The internal diode variables are the hole lifetime, $\tau_p$, and the junction radius, a, if the junction is hemispherical. The independent circuit variables are $I_f$, $t_f$, $V_r$, $R_s$, and $I_{RM}$ (keeping in mind the relation between the last three). Circuit capacities and rise time of the $V_r$ source affect the results, but these may be minimized, as has been noted.

### 4.1 Theoretical Characteristics of Junction Diodes

In his solutions of three geometric types of junction diodes Kingston[1] performed simplifying normalizations that reduce the number of variables. These normalizations then led to transient solutions of the diffusion equation that describe the reverse-recovery characteristics of these diodes in terms of the following dimensionless ratios:

1) $T_1 = \frac{\tau_1}{\tau_p}$ 2) $T_2 = \frac{\tau_2 - \tau_1}{\tau_p}$

3) $\frac{I_{RM}}{I_f}$ 4) $A = \frac{a}{L_p}$ , where $L_p$ is hole diffusion in n type germanium and is determined by equation 5:

5) $L_p = \sqrt{D_p \tau_p}$ $D_p = 45$ cm$^2$/sec. the diffusion constant for holes.

Normalized turn-off time is seen to be:

6) $\frac{\tau_2}{\tau_p} = (T_1 + T_2)$

Kingston assumed that the minority carrier densities were sufficiently small that recombination was linear.

The three cases considered were a) planar, b) hemispherical semi-infinite diodes in which the thickness of the germanium block is much larger than a diffusion length, and c) the planar narrow base diode with the thickness much smaller than a diffusion length. These

models were intended to cover a) grown- and indium-alloy junction diodes, b) bonded diodes, and c) emitters of junction transistors. Subsequent measurements of the germanium wafers in the alloy junction and bonded diodes have shown that the diffusion lengths may be the same order as the thickness. Hence they will not strictly fit within the assumptions. However the errors are not large and are predictable as discussed later in this section.

Kingston's results are summarized graphically in Figure 3.9. $T_1$, $T_2$, and $(T_1 + T_2)$ are plotted for the wide base diode. At the lower $I_{RM}/I_f$ ratios recombination is the dominant factor, and the T functions are relatively large. At higher current ratios faster removal of the stored carriers by the reverse current decreases the T functions markedly. $T_1$ and $(T_1 + T_2)$ are also shown for the narrow base diode. At low $I_{RM}/I_f$ these curves are below the same curves for the wide base diodes, but at high current ratios these curves approach the wide base characteristics. $T_1$ is plotted for A = 0.1 and 0.01 for the hemispherical wide base diode. In a typical example:

$$7) \quad A = \frac{a}{L_p} = \frac{0.2 \text{ mil}}{10 \text{ mils}} = 0.02$$

The value of A might range from a maximum of 0.1 in a low-voltage, high current bonded diode to 0.001 in special bonded diodes or point diodes. The $T_2$ curve for the hemispherical case is the same as that of the planar case with the $I_{RM}/I_f$ axis multiplied by the factor $(A + 1)/A$.

The ratios of the wide-base $T_1$ and $(T_1 + T_2)$ to the narrow base functions at an $I_{RM}/I_f$ of 0.1 are approximately 1.5 and 3.0 respectively. When $I_{RM}/I_f$ is 10, the ratios are about 1.0 and 1.25. Therefore for planar diodes with base thicknesses nearly the same as the diffusion length the error introduced in using the wide base theoretical curves is problably not more than 30% at low $I_{RM}/I_f$ and negligibly small at high $I_{RM}/I_f$. In the hemispherical junction diodes with similar base thicknesses the error is even less because of the multiplication of $I_{RM}/I_f$ by $(A + 1)/A$.

A few general observations may be made at this time. The first and most obvious is that the reverse-recovery characteristics of any given junction diode should be a function only of the $I_{RM}/I_f$ ratio, within the assumption of linear recombination. Another is that a thin germanium wafer should lead to shorter turn-off times at lower current ratios, but nearly the same at high ratios. Since $(T_1 + T_2)$ is a function of the $I_{RM}/I_f$ ratio, the definition of equation 6 indicates that a reduction in $\tau_p$ results in a similar reduction in $\tau_2$ for the same $I_{RM}/I_f$. Most important is the dependence of the reverse-recovery characteristics of diodes with hemispherical junctions on the factor A.

4.2 Experimental Characteristics of Planar Grown-Junction Diodes

The range of $I_{RM}/I_f$ that would probably be encountered in normal circuit applications is from 0.1 to 10. This corresponds to a variation of $V_r$ from 0.1 $V_f$ to 10 $V_f$ in a circuit with constant $R_s$. Figure 3.10 is a summary of the turn-off time characteristics of a grown-junction diode under various switching conditions. Since the exact $\tau_p$ for the planar diodes measured in this and the next section were not known values of $\tau_p$ were determined at $I_{RM}/I_f = 1$. These values were reasonable for these devices and were used to plot the theoretical curves in the illustrations. The agreement between the experimental and the theoretical curves indicates that the reverse-recovery characteristics are indeed functions only of the current ratio. The decrease in $\tau_2$ at the higher forward currents shows that there is some reduction in lifetime due to large hole densities. If field effects were appreciable they would result in a bending of the experimental curves away from the theoretical curve toward lower values of $\tau_2$ at high current ratios. In addition, the higher $I_f$ curve for any $R_s$ would bend in the same direction away from the lower $I_f$ curve for the same $R_s$, since the former necessarily requires higher $V_r$ values. Figure 3.10 illustrates that field effects may be neglected, and $\tau_2$ is definitely a function only of $I_{RM}/I_f$ and $\tau_p$.

4.3 Experimental Characteristics of Planar Alloy-Junction Diodes

Figure 3.11 is a similar characteristic of a diffused- or alloy-junction diode. The lifetime in this diode is about 1/5 that in the grown-junction diode discussed above, so the time scale in Figure 3.11 is the same fraction of the time scale of $\tau_2$ of Figure 3.10. The theoretical

curves plotted are taken from the wide base case. This particular series of alloy diodes has been found to wafer thicknesses of the same order as the diffusion length, but the experimental agreement with the theoretical curve is good as illustrated.

Figure 3.12 is a set of reverse-recovery characteristics of a similar diode for various values of $I_f$. Here again the agreement with the theoretical wide base curve is good. The decrease in the $\tau_1$ and $\tau_2$ with increasing forward currents is more pronounced than the same effect in the grown junction diode above. Effective lifetimes for each of these curves of 13 μsec., 8.7 μsec., and 4.6 μsec., are obtained for $I_f$ = 0.75 ma., 6.1 ma., and 31 ma. respectively.

To summarize what can be expected in available planar junction diodes $\tau_2$ has been plotted for various $\tau_p$ over the range of $I_{RM}/I_f$ from 0.10 to 10 in Figure 3.13. The Western Electric[a] grown-junction diodes have lifetimes above 30 μsec. and as high as 80 μsec. The General Electric alloy diodes[b] range from 5 to 15 μsec. The Western Electric[c] and Texas Instruments[d] silicon alloy diodes have lifetimes of 1 to 3 μsec. Reverse-recovery in all these diodes is a function of $I_{RM}/I_f$ and $\tau_p$ with a reduction in $\tau_p$ due to high currents. Over the range of $I_{RM}/I_f$ from 0.1 to 10, $\tau_2$ varies from approximately 3 $\tau_p$ to 0.1 $\tau_p$.

4.4 The Effects of High Peak Powers Due to Reverse-Recovery

This discussion, while out of the logical sequence, it particularly pertinent to the use of the planar junction diodes. In these devices dissipation is normally a few tens of milliwatts when conducting in the forward direction. When the reverse voltage is applied and $I_{RM}$ flows, the dissipation remains low until $\tau_1$, then it increases, reaches a maximum, and decreases to its steady-state value at the applied $V_r$.

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a. Types 1N102 (1784), 1N101 (1786) and 1N83 (1787)

b. Types 1N91 (4JA1A1), 1N92 (4JA1A2), 1N93 and 1N94

c. Types 1N137 (1847), 1N138 (1821)

d. Type 601

This maximum will occur when the back resistance of the diode equals $R_s$, or when the diode current is $I_{RM}/2$ and diode voltage $V_r/2$.

$$8) \quad P_{max} = \left(\frac{I_{RM}}{2}\right)\left(\frac{V_r}{2}\right)$$

Since $$I_{RM} = \frac{V_r}{R_s},$$

$$9) \quad P_{max} = \frac{I_{RM}^2 R_s}{4} = \frac{V_r^2}{4R_s}$$

Example:

$I_f$ = 30 ma., $R_s$ = 200 ohms, $V_r$ = 60 volts, so that $I_{RM}$ = 300 ma., and $I_{RM}/I_f$ = 10. Then $P_{max}$ is found to be 4.5 watts.

Since the time that such a power is dissipated is very short, perhaps a few tenths of a microsecond, the average power rating of the diode might be exceeded by sizeable margin. Little information is available on the peak power ratings of most diodes, but several have been destroyed by peak dissipation in the order of a watt in the reverse-recovery work reported here. This must be examined carefully in high-current, high-voltage applications of these diodes. It should also be considered in the application of bonded and point diode with poor reverse-recovery characteristics.

## 4.5 Experimental Characteristics of Bonded and Point Diodes

The reverse-recovery characteristics of both the bonded and point diodes do not agree as well in detail with the theory as the planar junction diodes discussed above. When $\tau_2$ is plotted as function of $I_{RM}/I_f$ with constant $I_f$ the slope deviates from theory in the directions that field effects and carrier multiplication produce. Moreover, for a given $I_{RM}/I_f$ higher $I_f$ results in longer instead of shorter $\tau_2$ as con-

trasted to the opposite result in the planar junction diodes. However, there is general agreement with theory in that increasing $I_{RM}$ for a given $I_f$ reduces $\tau_2$, and $\tau_2$ is a function of the contact area (or junction radius).

The characteristics of point and bonded diodes are sufficiently similar to be included in the same section. For maximum clarity $\tau_2$ has been plotted as functions of $I_f$, $V_r$, and $R_s$ separately in Figures 3.14 through 3.17. Figure 3.14a illustrates the linear relationship of $\tau_2$ with $I_f$. The slope is 0.12 and 0.07 μs/ma for $V_r$ = 10 and 30v respectively. $R_s$ and $I_f$ are constant in Figure 3.14b with $V_r$ (and consequently $I_{RM}$ also) as the independent variable. It should be noted that $\tau_2$ tends to become constant at the high values of $V_r$ (and $I_{RM}$) and rises at low $V_r$.

Graphs of $\tau_2$ versus $V_r$ and $I_{RM}$ are separately presented in Figures 3.15 and 3.16 respectively. Figure 3.15 is a family of curves showing $\tau_2$ as a function $V_r$ at various values of $R_s$. To determine $\tau_2$ as a function of $I_{RM}$ with $V_r$ constant requires moving vertically along a line of constant $V_r$ on this family. If this is done at $V_r$ = 30 $\tau_2$ is found to be 0.09 μs for an $I_{RM}$ of 60 ma and 2.8 μs for 3.0 ma. Figure 3.16 is the same experimental data with $\tau_2$ plotted versus $I_{RM}$. Finding $\tau_2$ versus $V_r$ at constant $I_{RM}$ requires moving vertically along an $I_{RM}$ line on Figure 3.16. In this case $\tau_2$ increases as $V_r$ increases. The reason for this behavior is not clear but one possible cause is carrier multiplication at the junction. Collectors of Gold-bonded transistors[11] have current gain of the same order as point-contact transistors. The reverse-recovery characteristics of point diodes and point-contact collectors[2] as diodes and transistors are all similar to Figure 3.16. These two bits of information support the supposition that carrier multiplication is responsible for the increase in $\tau_2$ with increasing $V_r$, but they are certainly not conclusive.

Because of the fast recovery of good point diodes and the limitations of the test circuit complete characteristics as presented for the bonded diodes are not obtainable. Figure 3.17 illustrates the relationship of $\tau_2$ to $I_f$ in a point diode for constant $R_s$ (compare to Figure 3.14). The function of $\tau_2$ is of the form:

$$\tau_2 (I_f) = m I_f + b$$

where m is the slope of the characteristic and b is a constant. For the diode shown m is 0.014 and 0.021 μs/ma for $V_r$ = 30 and 10 volts respectively. The constant, b, is 0.09 μs for both curves. As indicated by the one point at $I_f$ = 0 and $V_r$ = 10, there is a small value of $\tau_2$ even when no forward current had been flowing. The possibility that this might be due to the diode or circuit capacity was eliminated because of the amplitude of the spike observed and its time constant. The explanation must then be that the applied field causes a small current flow due to residual thermally-generated carriers.

In the curves of $\tau_2$ versus $V_r$ in Figure 3.17b, a noteworthy fact is that $\tau_2$ becomes fairly constant at the higher values of $V_r$. There is a minor discrepancy between the same points in two curves. For instance $\tau_2$ at $I_f$ = 22.6 ma and $V_r$ = 10 volts is 0.41 μsec. in Figure 3.17a and 0.45 μsec. in Figure 3.17b. This must be attributed to experimental error but it does not affect the results significantly.

Average reverse-recovery measurements at four points in Figures 3.14 and 3.17 for a variety of diodes are tabulated in Table 3-I. The storage spike magnitude represents the minimum back resistance that the diode shows under these test conditions.

10) $$r_{min} = \frac{V_r}{\text{St. Sp.}} - 2000$$

This value of $r_{min}$ under condition A is found to be 23,000 ohms for the 1N90 at the top of the list and 780 ohms for the T5 at the bottom. Under condition D these values are 52,000 and 5,500 ohms.

Average reverse-recovery measurements under condition D of Table 3-I for all bonded and point diodes tested in this work are summarized in Table 3-II. More than one sample of some types of diode were received at different times. Such samples are listed independently and denoted by a letter in parenthesis after the type number. The variation between these samples may be great as it is for the Hughes 1N90. Sample A is top most on the list with an average $\tau_2$ of 0.03μs while sample B is more than half way down. Sample B included only three units, a poor statistical sample, but was included to illustrate this variation. All other samples of less than 5 units were not included in this table. One sample, Kemtron Type D357, has been in the laboratory for

Table 3-I: Reverse-Recovery of Point and Bonded Diodes

$R_s$ = 2000, $\tau_2$ defined to 2% of $I_{RM}$

| | A | | B | | C | | D | |
|---|---|---|---|---|---|---|---|---|
| $I_f$ | 15 ma. | | 5 ma. | | 5 ma. | | 15 ma. | |
| $V_r$ | 10 v. | | 10 v. | | 35 v. | | 35 v. | |
| Manufacturer and Type | St.Sp.[a] ma | $\tau_2$ μs | St.Sp. ma | $\tau_2$ μs | St.Sp. ma | $\tau_2$ μs | St.Sp. ma | $\tau_2$ μs |
| Hughes 1N90 | 0.40 | 0.24 | 0.20 | 0.14 | 0.38 | 0.07 | 0.65 | 0.16 |
| Sylvania 1N34A | 1.40 | 0.38 | 0.60 | 0.24 | 1.45 | 0.18 | 1.75 | 0.29 |
| Raytheon CK707 | 0.85 | 0.44 | 0.35 | 0.23 | 0.68 | 0.14 | 1.15 | 0.28 |
| Sylvania 1N38A | 0.95 | 0.48 | 0.42 | 0.25 | 0.75 | 0.19 | 1.35 | 0.34 |
| Hughes 1N55B | 0.75 | 0.50 | 0.40 | 0.28 | 0.82 | 0.21 | 1.25 | 0.35 |
| Hughes 1N116 | 0.95 | 0.52 | 0.45 | 0.30 | 1.25 | 0.22 | 1.10 | 0.31 |
| Hughes 1N67A | 1.85 | 0.60 | 1.0 | 0.34 | 1.45 | 0.24 | 2.45 | 0.39 |
| Hughes 1N118 | 2.8 | 0.75 | 1.25 | 0.35 | 2.0 | 0.27 | 3.6 | 0.60 |
| Hughes 1N117 | 2.8 | 0.77 | 1.3 | 0.39 | 1.90 | 0.28 | 3.6 | 0.54 |
| Amperex 1N38A | 1.70 | 1.35 | 0.85 | 0.7 | 1.25 | 0.34 | 2.1 | 0.75 |
| Radio Receptor 1N70 | 2.05 | 1.75 | 0.55 | 0.60 | 1.35 | 0.38 | 2.55 | 0.96 |
| Transitron 1N63* | 2.2 | 1.75 | 1.15 | 0.7 | 1.80 | 0.40 | 3.10 | 0.94 |
| Nation Union 1N108* | 2.9 | 2.1 | 2.25 | 1.0 | 3.30 | 0.52 | 5.35 | 1.19 |
| Transitron T5* | 3.6 | 2.80 | 1.95 | 1.45 | 2.80 | 0.74 | 4.65 | 1.65 |

* Bonded Types

[a] Storage Spike Magnitude

Table 3-II: Average Reverse-Recovery of All Samples of Point and Bonded Diodes

$R_s = 2000$, $\tau_2$ defined to 2% $I_{RM}$, $I_f \approx 15$ ma, $V_r \approx 35$ v

| Manufacturer | Type | No. Tested | Storage Spike ma | Turn-Off Time μs |
|---|---|---|---|---|
| Hughes | 1N90 (A)[a] | 7 | 0.22 | 0.03 |
| Sylvania | 1N34A (A) | 10 | 1.13 | 0.08 |
| Sylvania | 1N34A (B) | 70 | 0.59 | 0.09 |
| Hughes | 1N55B | 10 | 0.60 | 0.09 |
| Raytheon | CK707 | 8 | 0.84 | 0.13 |
| Kemtron | K34 | 9 | 0.75 | 0.14 |
| Kemtron | D357 | 6 | 0.76 | 0.15 |
| Hughes | 1N69 | 7 | 1.09 | 0.15 |
| Sylvania | 1N38A | 11 | 1.15 | 0.18 |
| Hughes | 1N68A (A) | 9 | 1.26 | 0.18 |
| Hughes | 1N116 | 20 | 1.79 | 0.18 |
| Hughes | 1N67A | 10 | 1.66 | 0.19 |
| Raytheon | CK713 | 10 | 1.02 | 0.20 |
| Sylvania | 1N57A | 6 | 1.28 | 0.21 |
| Hughes | 1N68A (C) | 19 | 1.99 | 0.22 |
| Hughes | 1N68A (B) | 30 | 1.28 | 0.28 |
| Hughes | H2060 | 20 | 2.04 | 0.29 |
| Amperex | 1N38 | 9 | 1.90 | 0.32 |
| Radio Recep. | 1N38 | 9 | 1.66 | 0.34 |
| Hughes | 1N90 (B) | 3 | 2.30 | 0.39 |
| Radio Recep. | 1N70 | 10 | 1.78 | 0.43 |
| Hughes | 1N96 | 8 | 3.50 | 0.43 |
| Hughes | 1N117 | 19 | 4.65 | 0.50 |
| Hughes | 1N118 | 20 | 5.53 | 0.58 |
| Transitron | T6[b] | 5 | 2.08 | 0.59 |
| Transitron | 1N63[b] | 5 | 2.71 | 0.60 |
| Transitron | T2[b] | 6 | 4.04 | 0.69 |
| Transitron | S77[b] | 5 | 3.41 | 0.90 |
| National Union | 1N108[b] | 7 | 3.62 | 1.11 |
| National Union | 1N175[b] | 9 | 5.24 | 1.65 |

[a] In some cases more than one sample lot of the same type of diode were received. The sample groups are indicated by a capital letter in parentheses.

[b] Bonded Types

several years but these particular diodes have not been used in equipment. Most of the testing represented in this table was repeated on the same diodes on three different occasions separated by periods of about three months. In these sets of tests the order of diode types remained the same, but differences in the tests gave different average values.

Correlation of average $\tau_2$ with forward resistance is shown in Figure 3.18. $V_{f10}$ is the forward voltage at 10 ma of static forward current. Reasonable interpretation of the ratings of similar diodes with respect to germanium resistivity and contact area gives good theoretical agreement with the results shown in Figure 3.18. These interpretations are 1) that a higher back voltage rating means higher resistivity and 2) that a higher forward current rating means larger contact area. For instance the difference between the NU 1N108 and 1N175 is a higher back voltage rating for the latter. Thus, the 1N175 should have higher $V_{f10}$ and $\tau_2$ and this is seen to be true in Figure 3.18. Comparison of the ratings of the Hughes 1N117 and 1N55 suggests that the contact area of the former should be larger, hence $V_{f10}$ would be smaller and $\tau_2$ larger. Microscopic examination of these diodes verifies the assumption and the location of the points supports the conclusions. Similar arguments hold for the Sylvania 1N34 and 1N38 and the Transitron diodes included in Figure 3.18.

Construction of small area bonded diodes, reported in Chapter VI of the thesis,[2] has indicated that the variation of $\tau_2$ with contact area is much less than predicted. For diodes with 2 mil. contact diameters the measured $\tau_2$ was about 10% of the theoretical value, with 0.5 mil. diameter the measured $\tau_2$ was about 30% of theoretical while with 0.2 mil. diameter the measured $\tau_2$ was 50% larger than the predicted turn-off time.

## 4.6 Reverse Recovery Buildup Time

The relationship of $\tau_2$ to the time in forward conduction, $t_f$, is illustrated in Figure 3.19. Units of each of the various constructional types are shown. The value of $t_f$ beyond which $\tau_2$ remains constant is the point where the hole density distribution has reached the steady state. Comparison of this $t_f$ to the values of $\tau_p$ for the planar junction diodes indicates that it is about 3 times $\tau_p$. Since $\tau_p$ is defined to the

1/e point of the steady-state hole density distribution then this $t_f$ is the time required for holes to diffuse to the $\frac{1}{e^3}$ point in the distribution. Since the steady-state hole-density distribution in the hemispherical case is a function that falls much more rapidly with distance (a = 0.1 or less) than the simple exponential of the planar case, the steady-state value of $t_f$ should be more closely related to the junction redius than $\tau_p$. Evidence of this is shown in Figure 3.19. Microscopic examination of the 1N116 and 1N68A reveals that the whisker-germanium contact area of the former is somewhat smaller. The static and reverse-recovery characteristics of the T5, a high forward conductance unit, indicate that it has a larger junction radius than the bonded 1N63 from the same manufacturer. The forward resistances of these units measured at 10 ma. is as follows: 1N116 No. 6 - 1.29 volts, 1N68A No. 1 - 1.00 volt, 1N63 No. 9 - 0.60 volts, and T5 No. 26 - 0.50 volt. This order of $V_{f10}$ is the same order as it is for increasing $\tau_2$ and steady-state $t_f$, although the 1N68A and 1N63 are very similar in both $\tau_2$ and $t_f$ in Figure 3.19.

This figure also indicates that the junction diodes might be usable in high speed circuitry in which $t_f$ is kept short. An example is an application in which the diode is normally reverse biased and required to pass occasional narrow forward pulses, provided diode capacity is not troublesome. A similar application of the point and bonded diodes would lead to substantial reduction in $\tau_2$.

## 5.0 Conclusions

In the course of this work it has become apparent that all diodes should be tested for reverse-recovery if there is any possibility that the application may be critical. Reverse-recovery has been the cause of numerous failures and some cases of improper operation of circuits in this laboratory. Unfortunately during the period of this period of this research, the trend in the "general stock" types of point diodes has been towards longer recovery times so that trouble may now be experienced where there was no difficulty a few months previous. The recovery time uniformity of these "general stock" point diodes has also decreased so that there is a greater percentage variation of recovery time within a given lot now than before. Furthermore new magnetic-core

and magnetic-drum circuits require the use of large-area point and bonded diodes that have inherently longer recovery times than the more common point diodes. To fill all needs a wide range of diodes is necessary; fast point diodes, medium-speed point and bonded diodes, and slow planar-junction diodes. But the recovery characteristics of any one diode type must be known and this information distributed to those engineers using these diodes. The recovery test circuits and measurements must be realistic. Quality control must be maintained so that all diodes within a given type will indeed fit the class of circuit operation for which that type is intended.

Several general statements may be made with respect to the effect of the reverse-recovery characteristics on the applications of point and bonded diodes. As forward conductance and/or back voltage ratings increase so does the recovery time tend to increase. From this standpoint then diodes should not be derated for applications, but should be used at their ratings, assuming that these ratings are realistic of course. The ideal application is one in which the diode is quiescently biased in the reverse direction and passes short forward current pulses. In other applications the recovery times may be minimized simply by keeping forward currents and impedance levels low.

Signed Nolan T. Jones
Nolan T. Jones

NTJ/ds

Distribution List:
Transistor Distribution 3 and the following:
B. B. Paine
K. E. McVicar
R. W. Hudson
J. V. Harrington

List of Illustrations:

Fig. 3.1 A-57159
Fig. 3.2 A-56055-1
Fig. 3.3 A-57690-1
Fig. 3.4 A-57078
Fig. 3.5 A-59106
Fig. 3.6 A-57147
Fig. 3.7 A-57146
Fig. 3.8 A-54949-1
Fig. 3.9 B-58441
Fig. 3.10 A-58779
Fig. 3.11 A-58440
Fig. 3.12 A-58778
Fig. 3.13 A-58539
Fig. 3.14 A-59276
Fig. 3.15 A-59277
Fig. 3.16 A-59278
Fig. 3.17 A-59279
Fig. 3.18 A-59104
Fig. 3.19 B-58781

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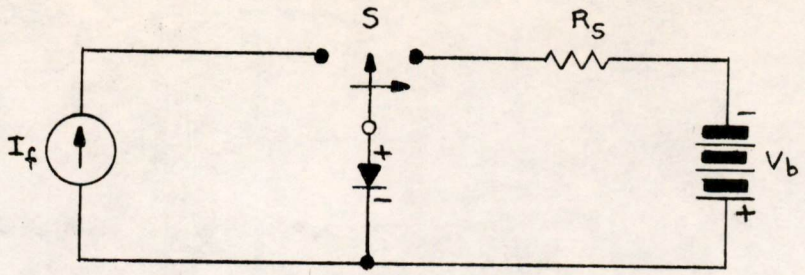
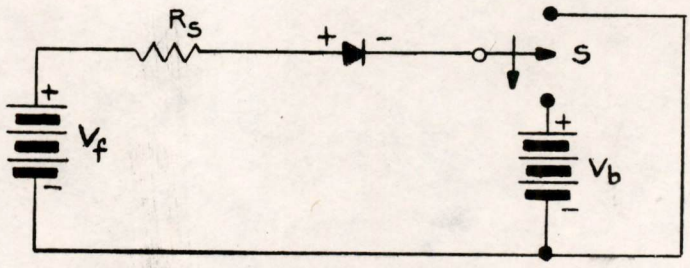
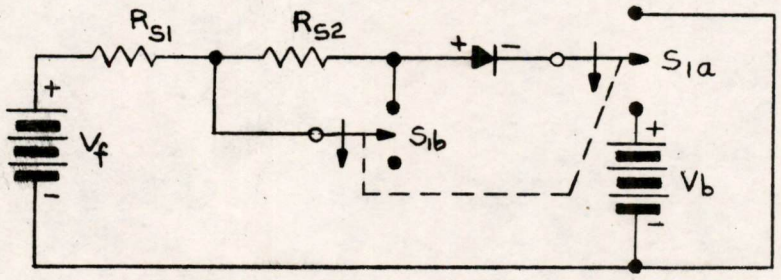
11. R. A. Langevin, "Gold Bonded Transistor Development Final Report," Transistor Products, Inc., (Jan. 8, 1954) Contract AF 19(604) - 814 Air Force Cambridge Research Center.




(a) REPRESENTATIVE CIRCUIT




(b) REALIZEABLE CIRCUIT



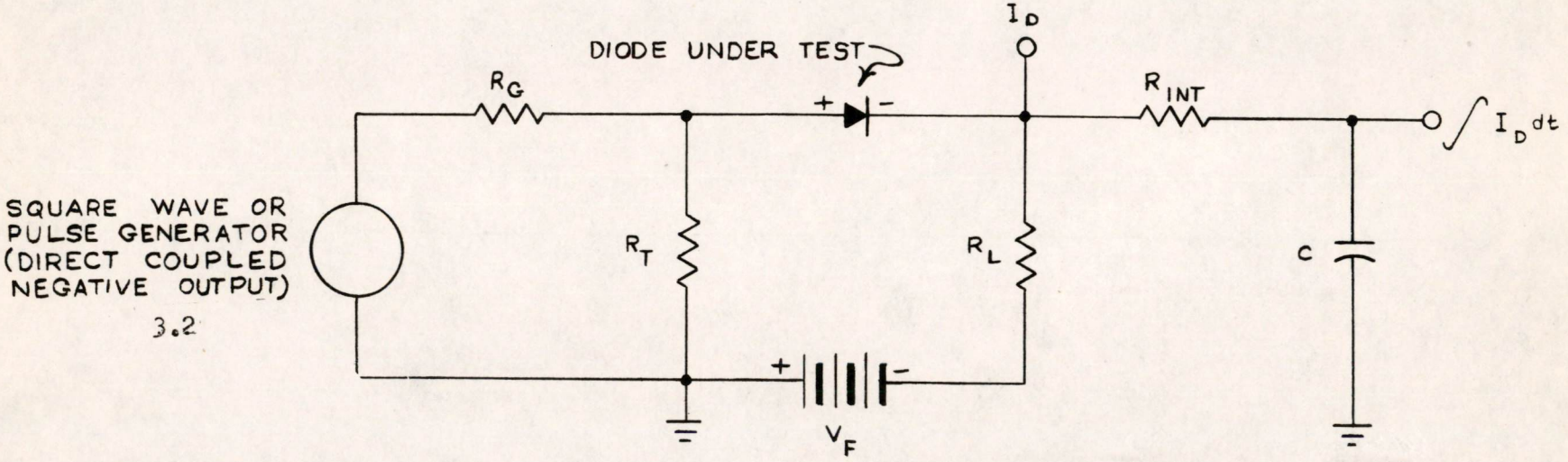

(c) REALIZEABLE CIRCUIT WITH SWITCHED LOOP RESISTANCE

A-57159

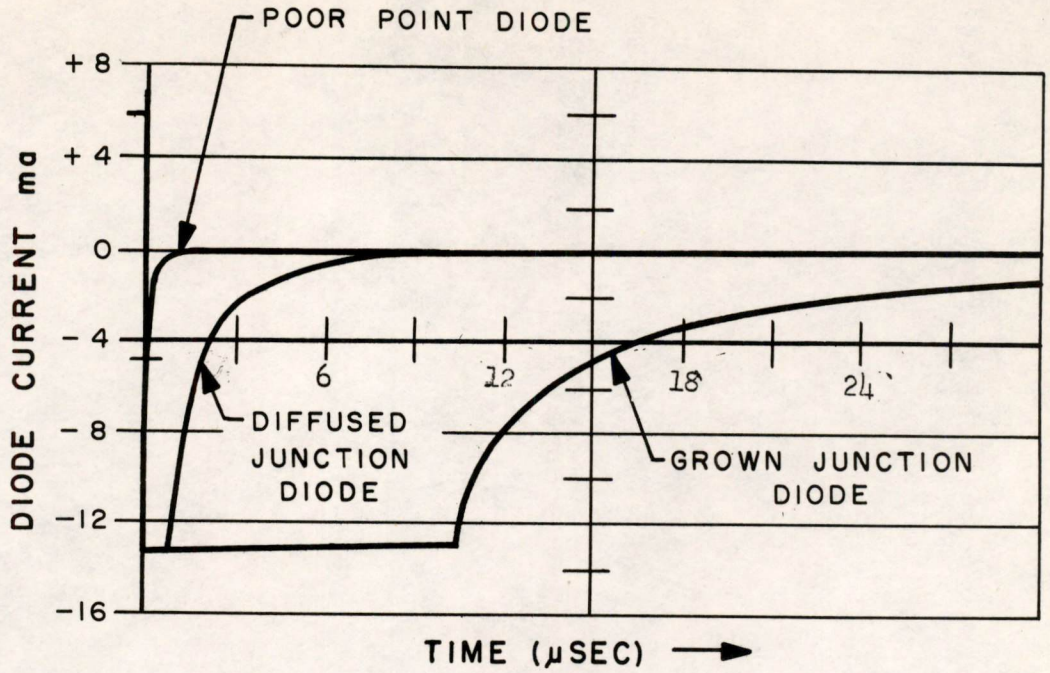
FIG. 3.1

DIODE SWITCHING CIRCUITS

A-56055-1




GENERAL DIODE REVERSE RECOVERY MEASUREMENT CIRCUIT




$I_F$ = 6 ma

$V_{BACK} \cong$ 14 V.

$R_S \cong$ 1000Ω

GROWN JCT. — WF 1784 NO. 4

DIFF. JCT. — GE IN92 NO. 4

POINT DIODE — HUGHES HD2017 NO. 1

Fig. 3.3

REVERSE RECOVERY OF JUNCTION AND POINT DIODES UNDER SAME SWITCHING CONDITIONS

A-57690-1

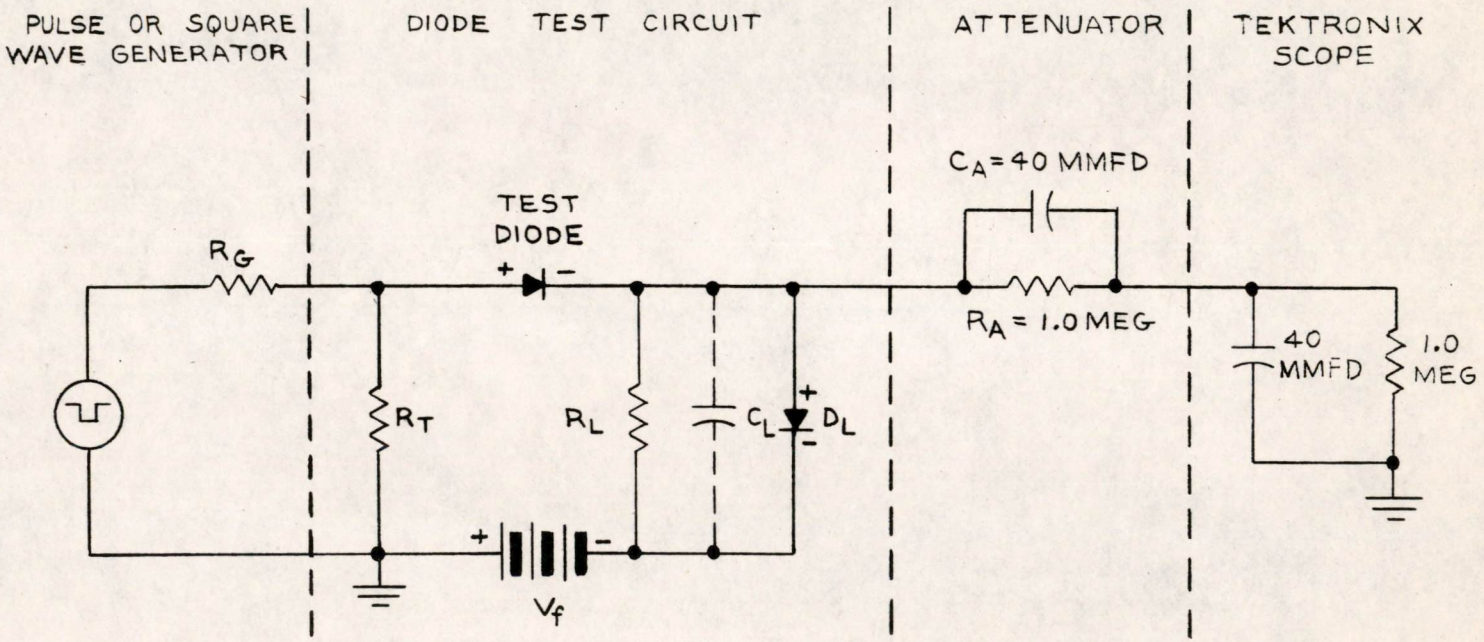
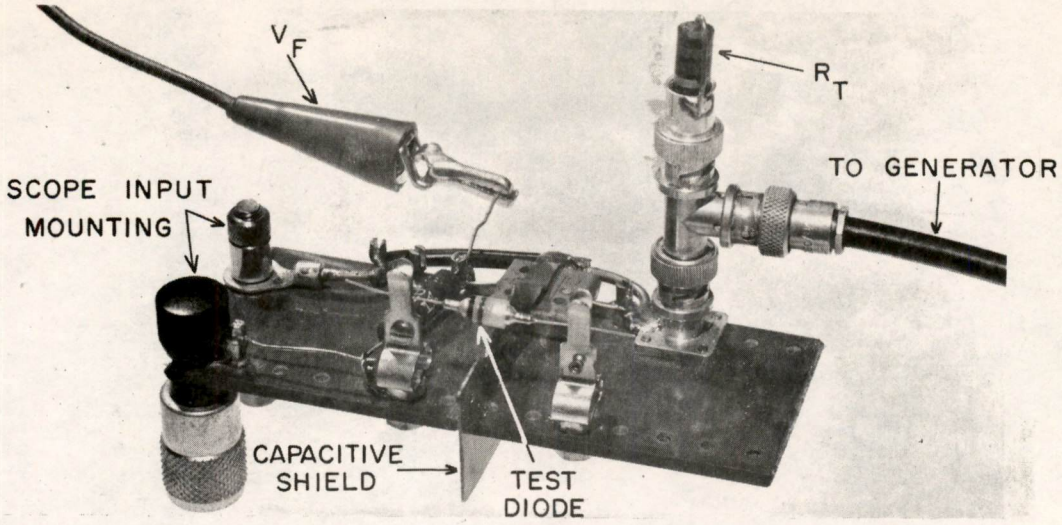
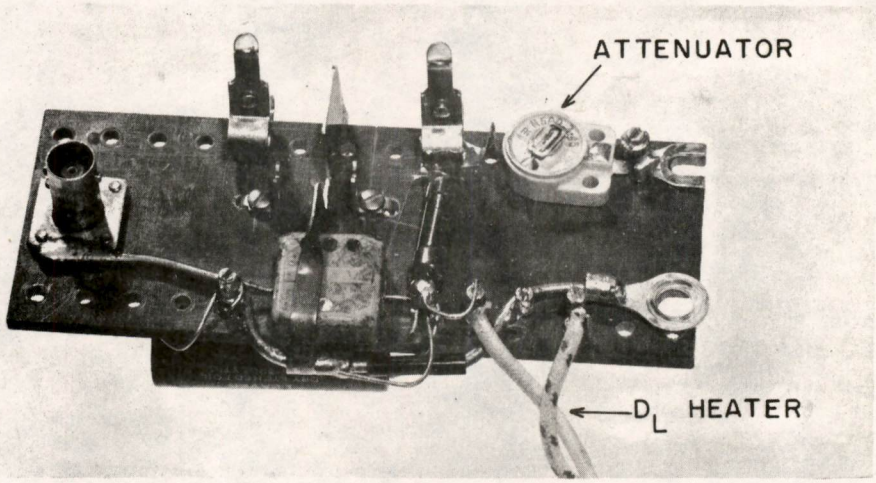



Fig. 3.4

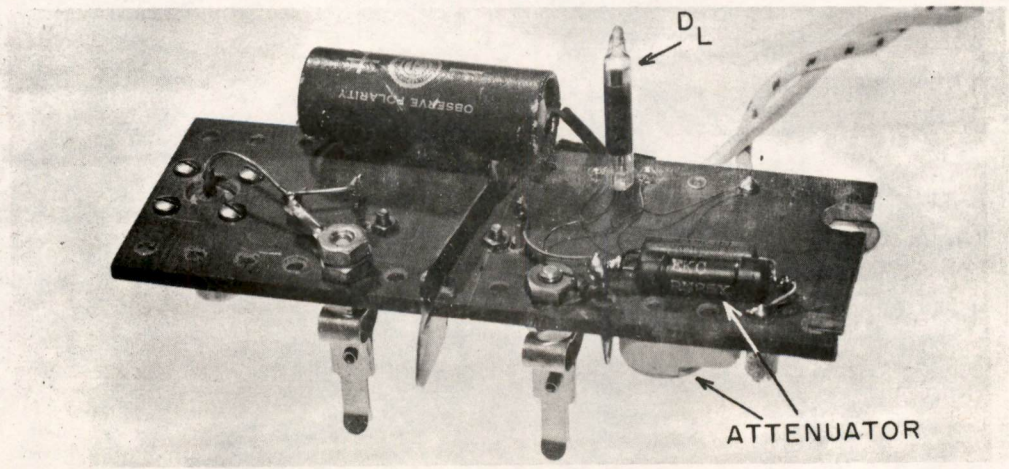
TEST CIRCUIT FOR POINT DIODE REVERSE RECOVERY MEASUREMENTS




a) GENERAL



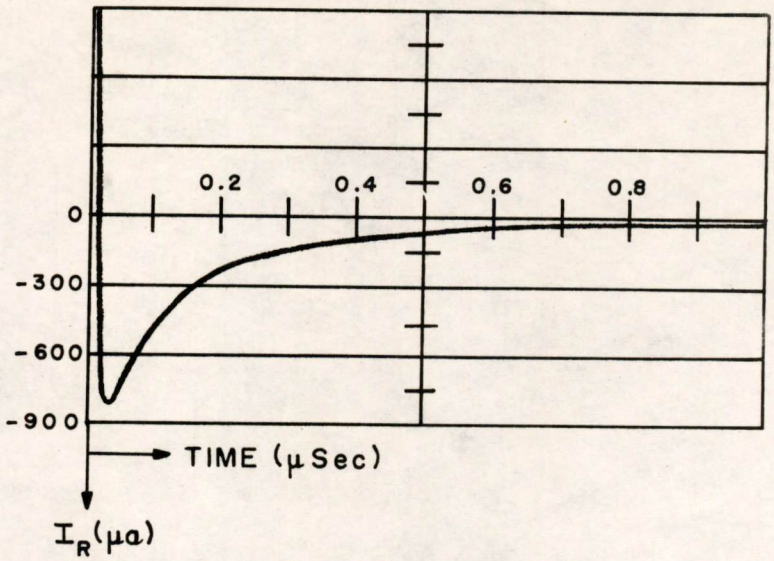

b) POINT DIODE (FRONT)




c) POINT DIODE (BACK)

FIG. 3.5

REVERSE RECOVERY MEASURING CIRCUITS



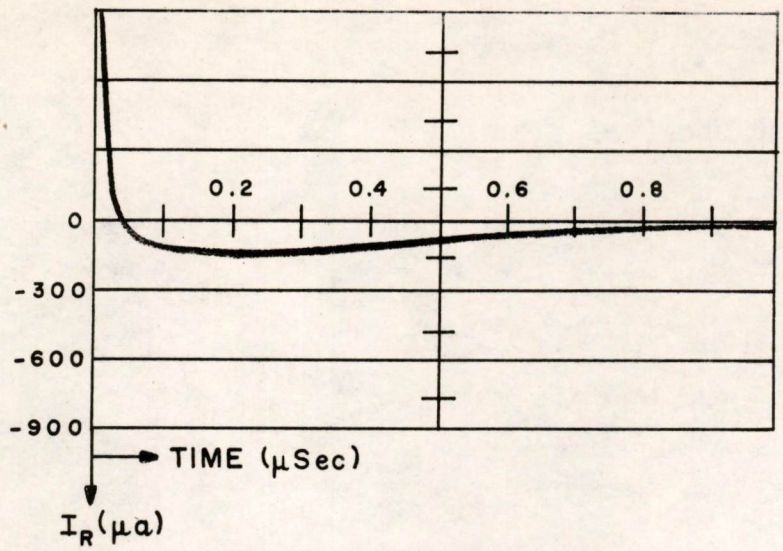

SYLVANIA IN38A $I_f$ = 24ma, $V_R$ = 30V, $R_s$ = 2K

Fig. 3.6

TYPICAL POINT DIODE

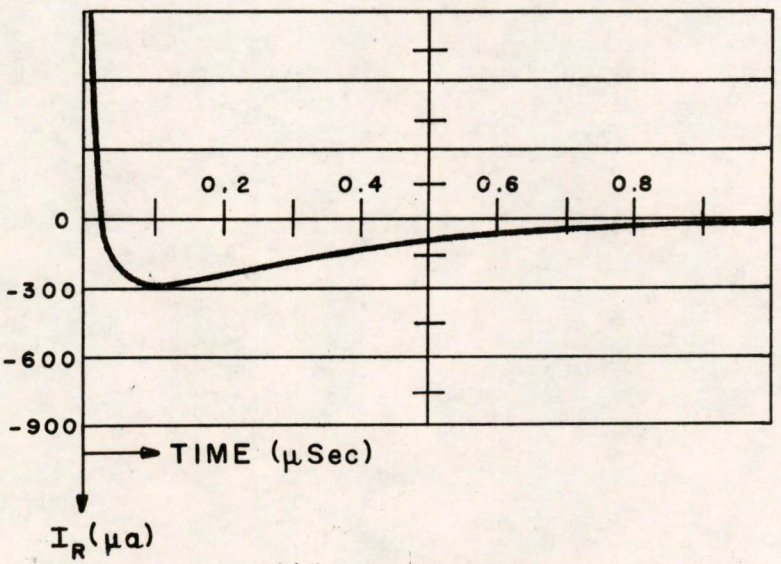
REVERSE RECOVERY WAVEFORM

A-57147




(a) $C_L$ = 120MMFD

SYLVANIA IN38A $I_f$ = 24 ma, $V_R$ = 30V, $R_s$ = 2K

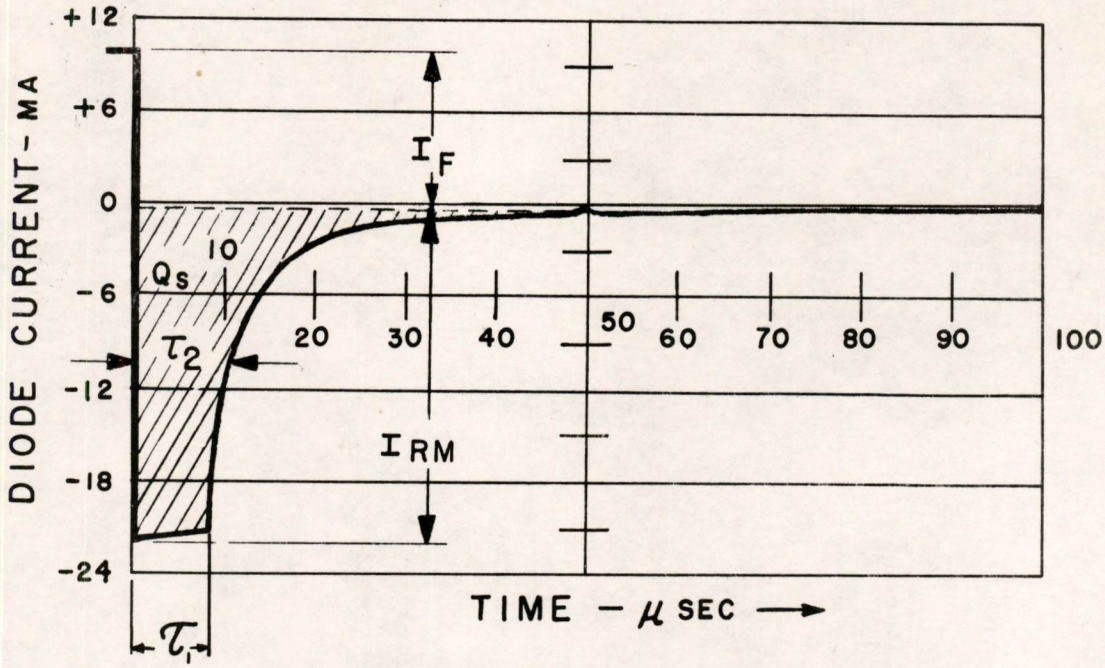



(b) $C_L$ = 47MMFD

FIG. 3.7

POINT DIODE REVERSE RECOVERY WAVEFORMS WITH SHUNT CAPACITY

A-57146




$I_F$ = 10 MA
$V_{BACK}$ = 12 V
$R_S$ = 600 Ω

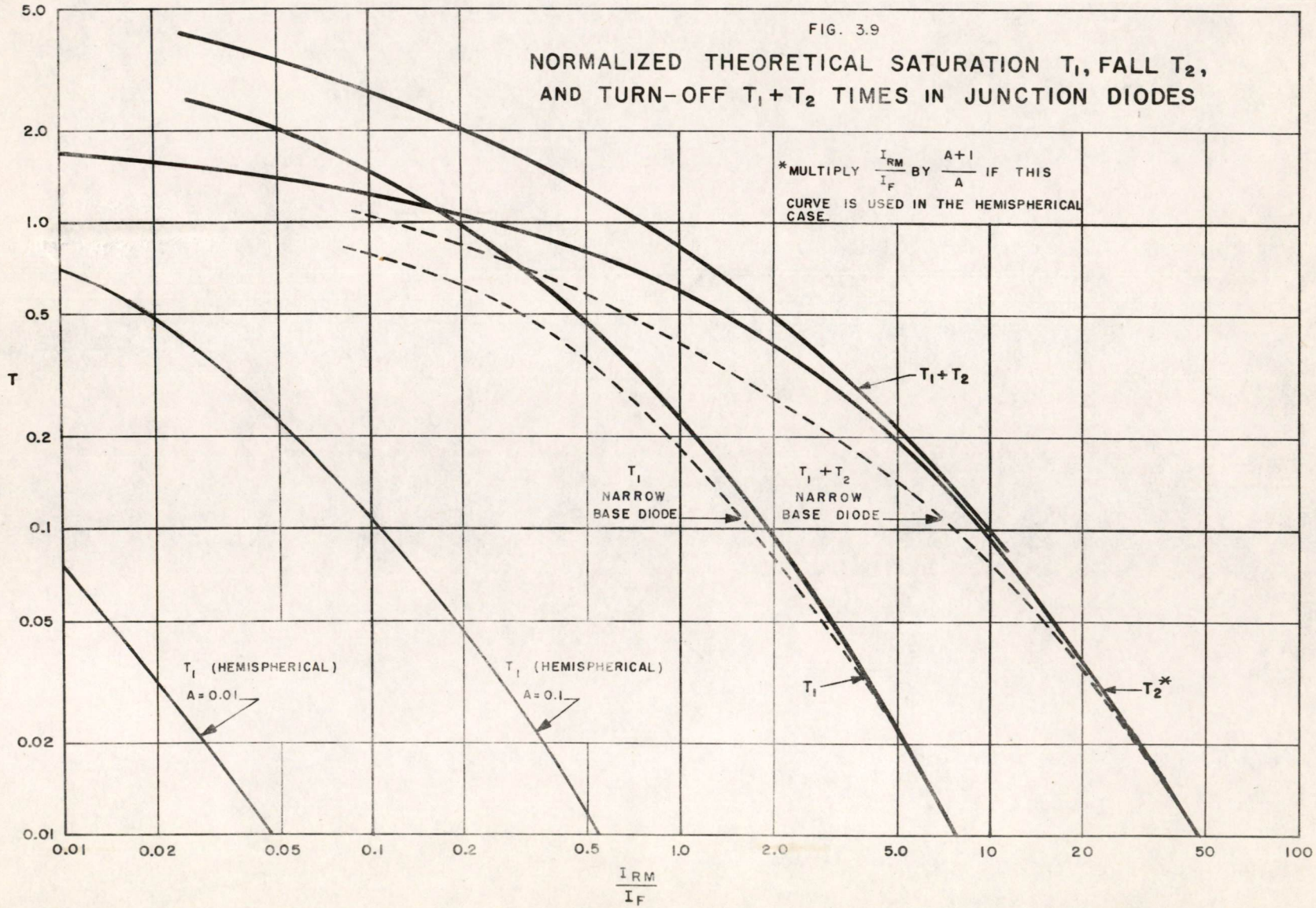
FIG. 3.8

REVERSE RECOVERY WAVEFORM OF A GERMANIUM JUNCTION DIODE (WESTERN ELECTRIC TYPE 1784 Nº 4)

A-54949-1

FIG. 3.9

NORMALIZED THEORETICAL SATURATION $T_1$, FALL $T_2$, AND TURN-OFF $T_1 + T_2$ TIMES IN JUNCTION DIODES



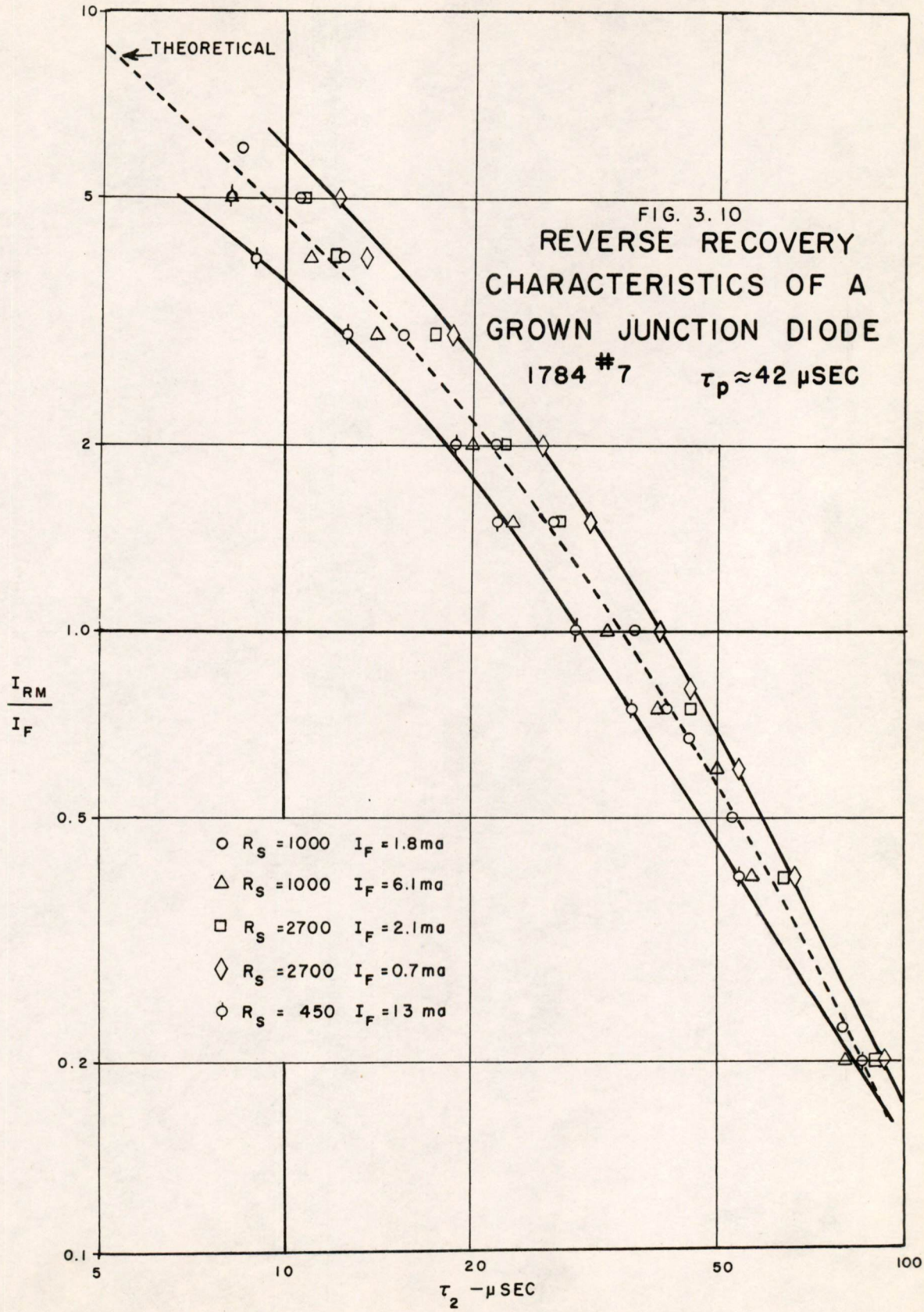



FIG. 3.10
REVERSE RECOVERY CHARACTERISTICS OF A GROWN JUNCTION DIODE
1784 #7 $\tau_p \approx 42$ μSEC

A-58779

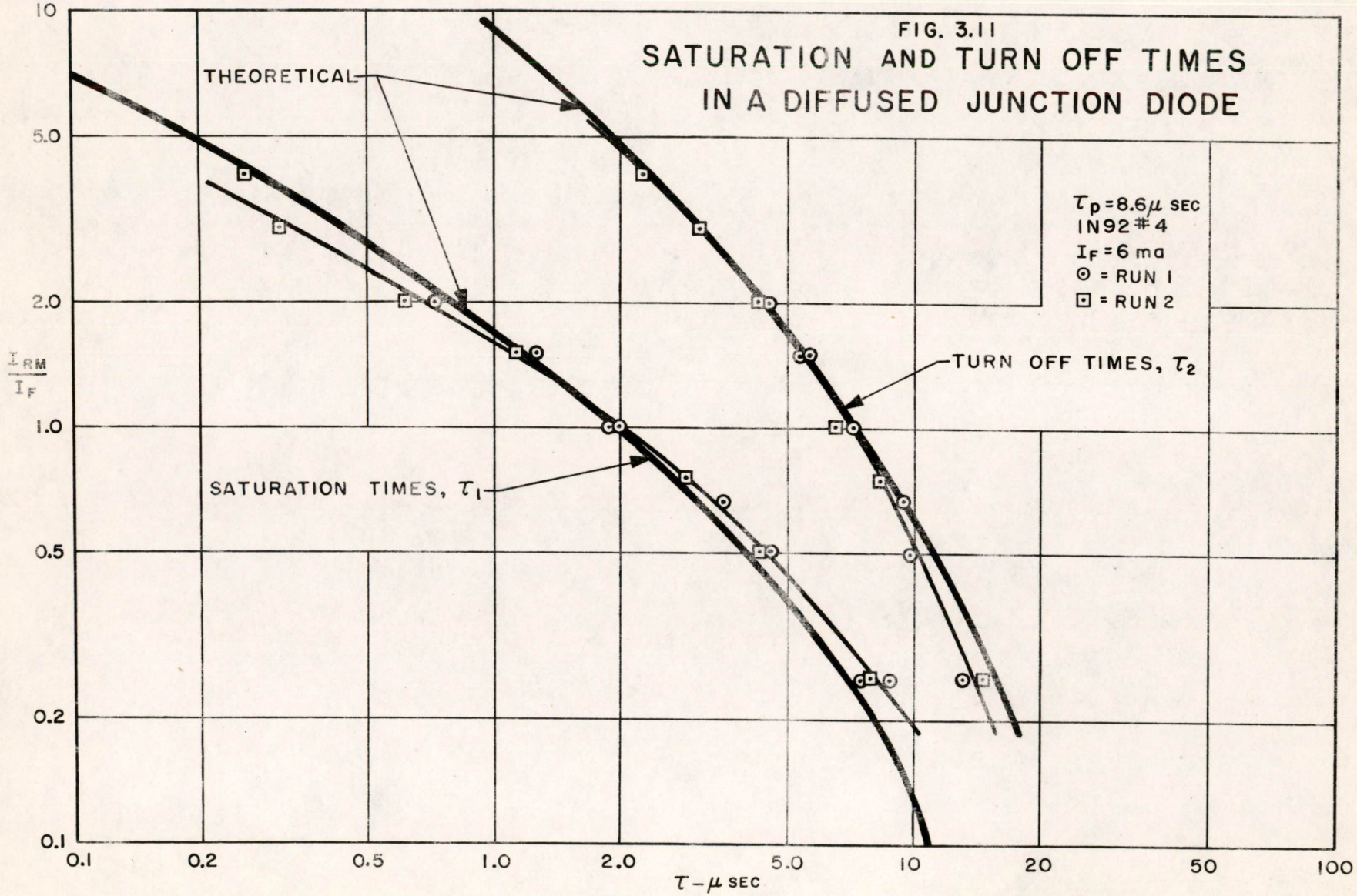


FIG. 3.11
SATURATION AND TURN OFF TIMES
IN A DIFFUSED JUNCTION DIODE
THEORETICAL
$\tau_p$ = 8.6μ sec
IN92 # 4
$I_F$ = 6 ma
⊙ = RUN 1
⊡ = RUN 2
TURN OFF TIMES, $\tau_2$
SATURATION TIMES, $\tau_1$
$\frac{I_{RM}}{I_F}$
10
5.0
2.0
1.0
0.5
0.2
0.1
0.1
0.2
0.5
1.0
2.0
5.0
10
20
50
100
τ – μ SEC

A-58778

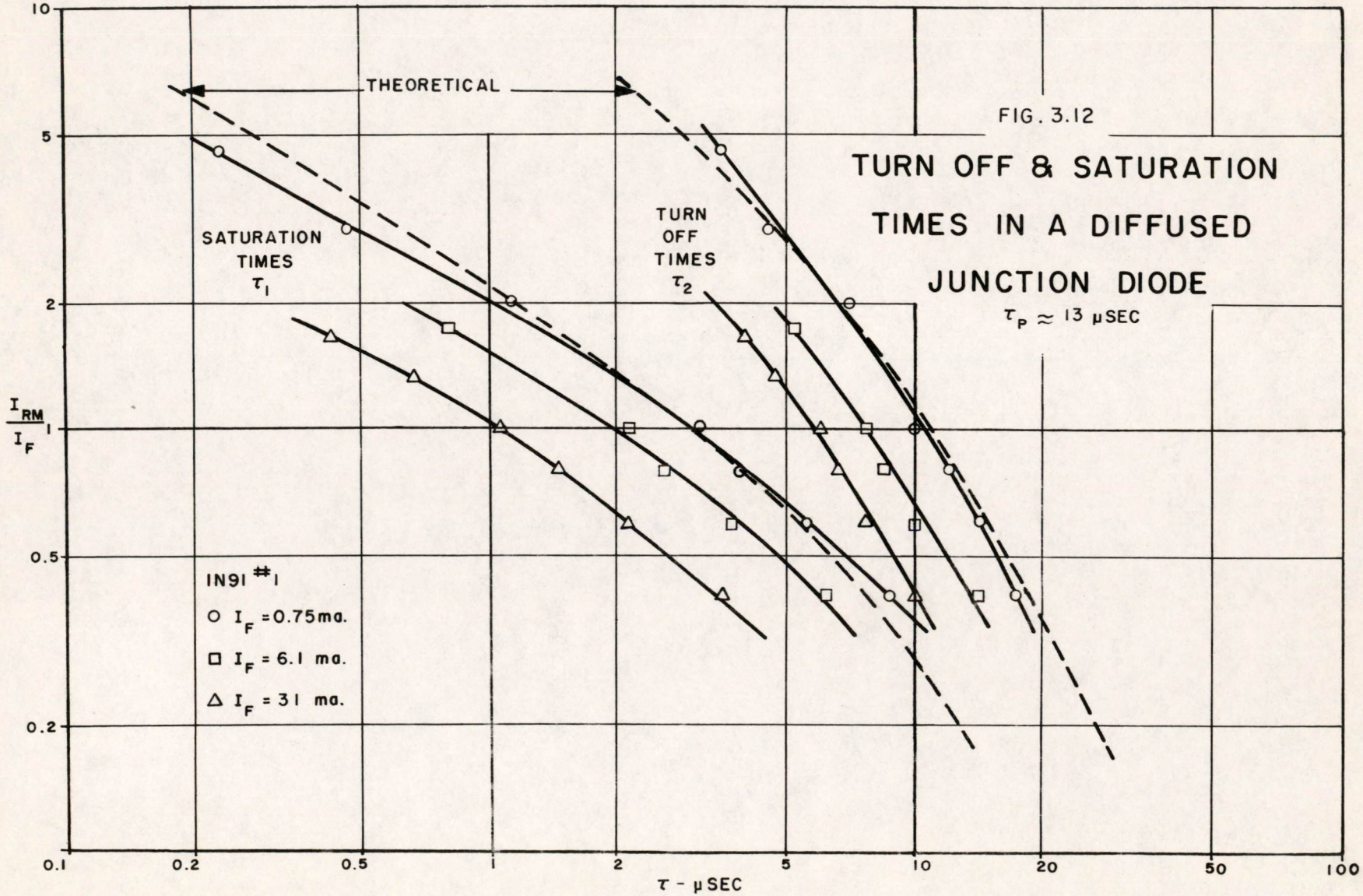



FIG. 3.12

TURN OFF & SATURATION TIMES IN A DIFFUSED JUNCTION DIODE

$\tau_P \approx 13$ μSEC

A-58539

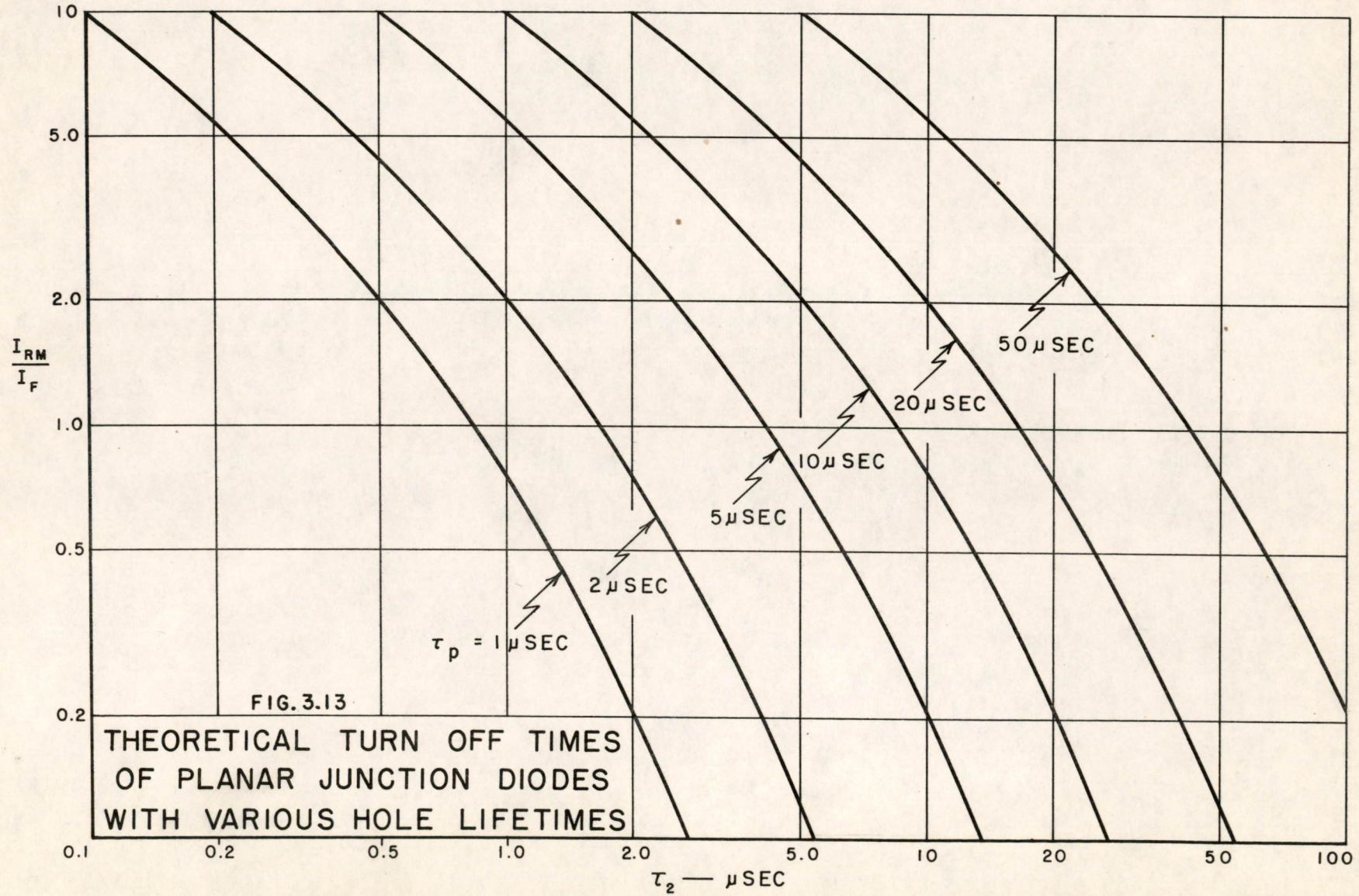
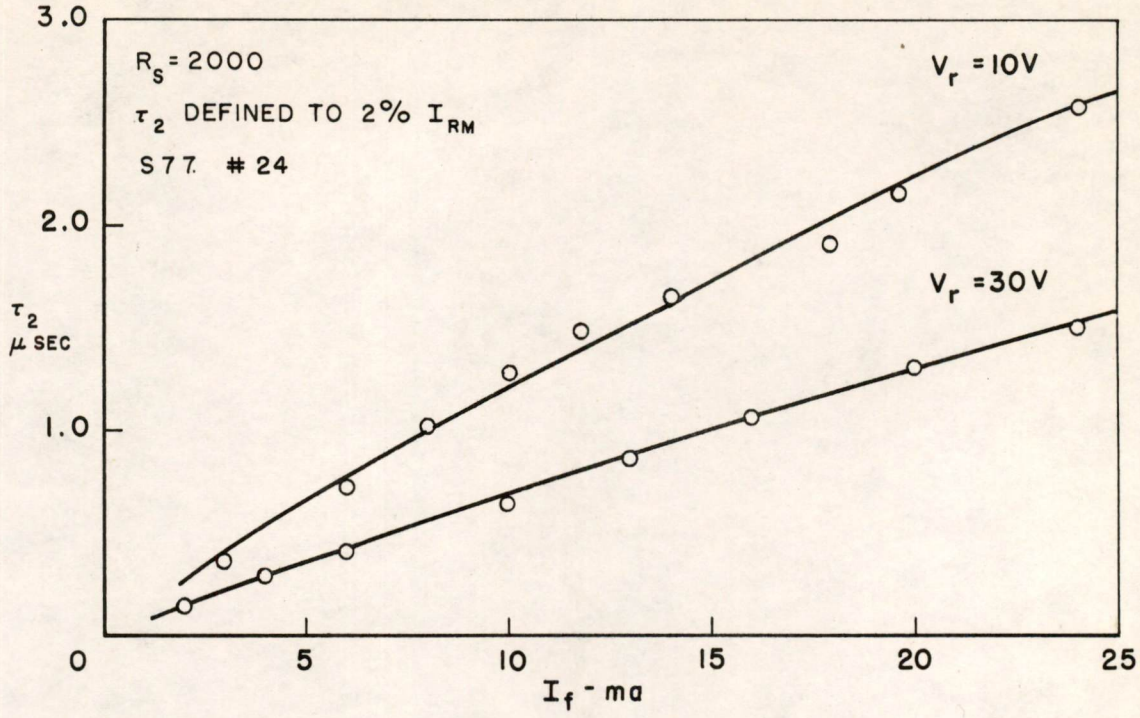



FIG. 3.13

THEORETICAL TURN OFF TIMES OF PLANAR JUNCTION DIODES WITH VARIOUS HOLE LIFETIMES



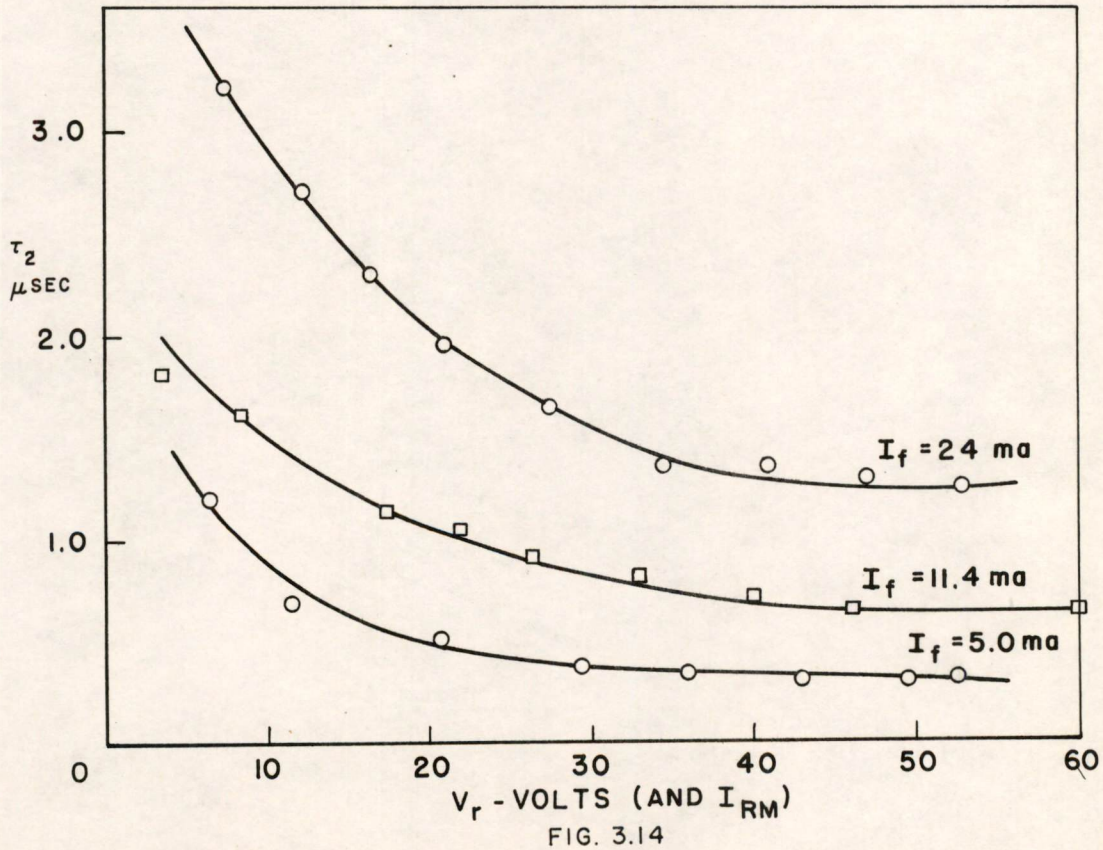




FIG. 3.14

REVERSE RECOVERY OF A BONDED DIODE $\tau_2$ vs. $I_f$ and $V_r$

A-59276

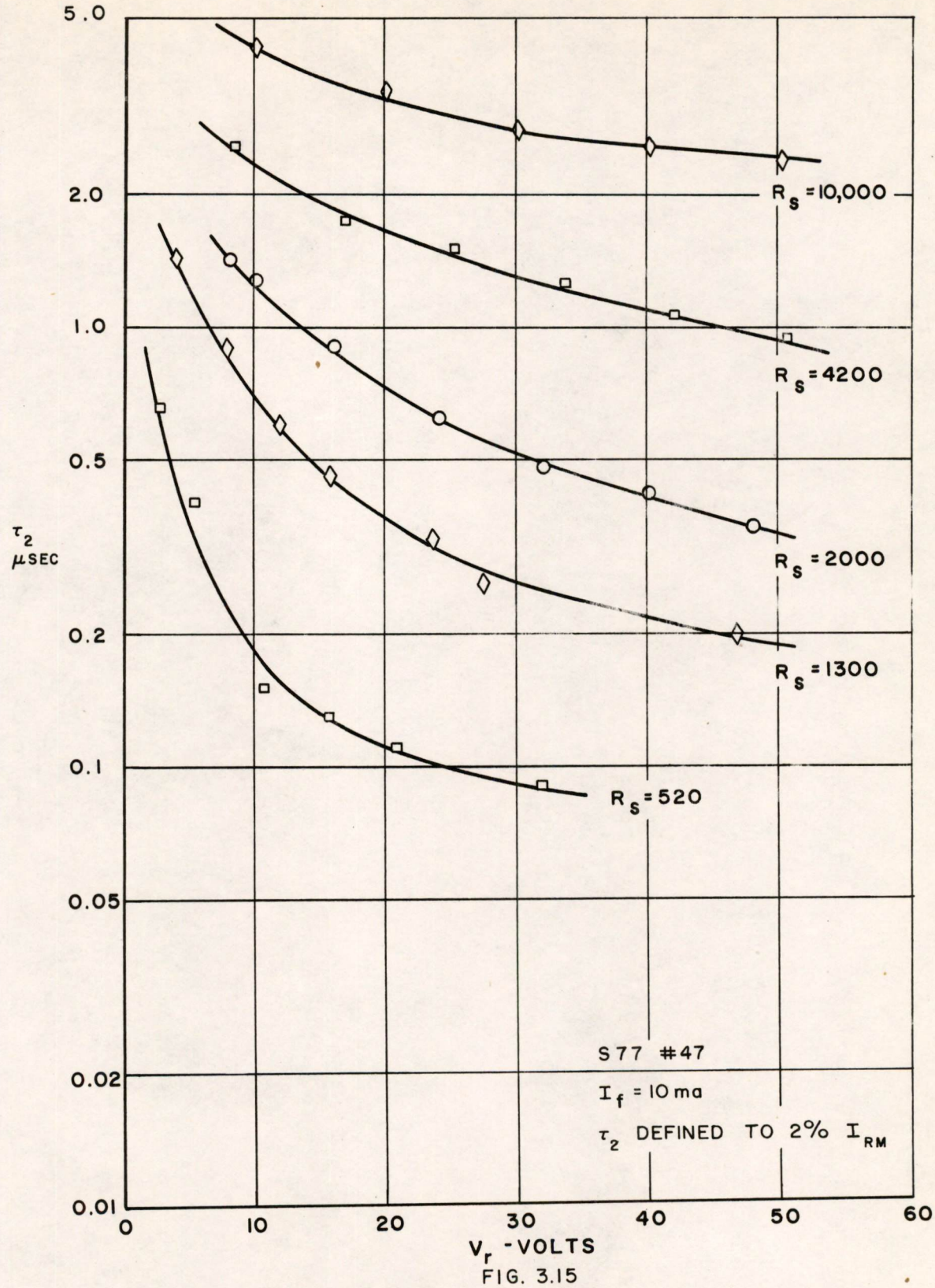



FIG. 3.15

REVERSE RECOVERY OF A BONDED DIODE

$\tau_2$ vs. $V_r$

A-59277

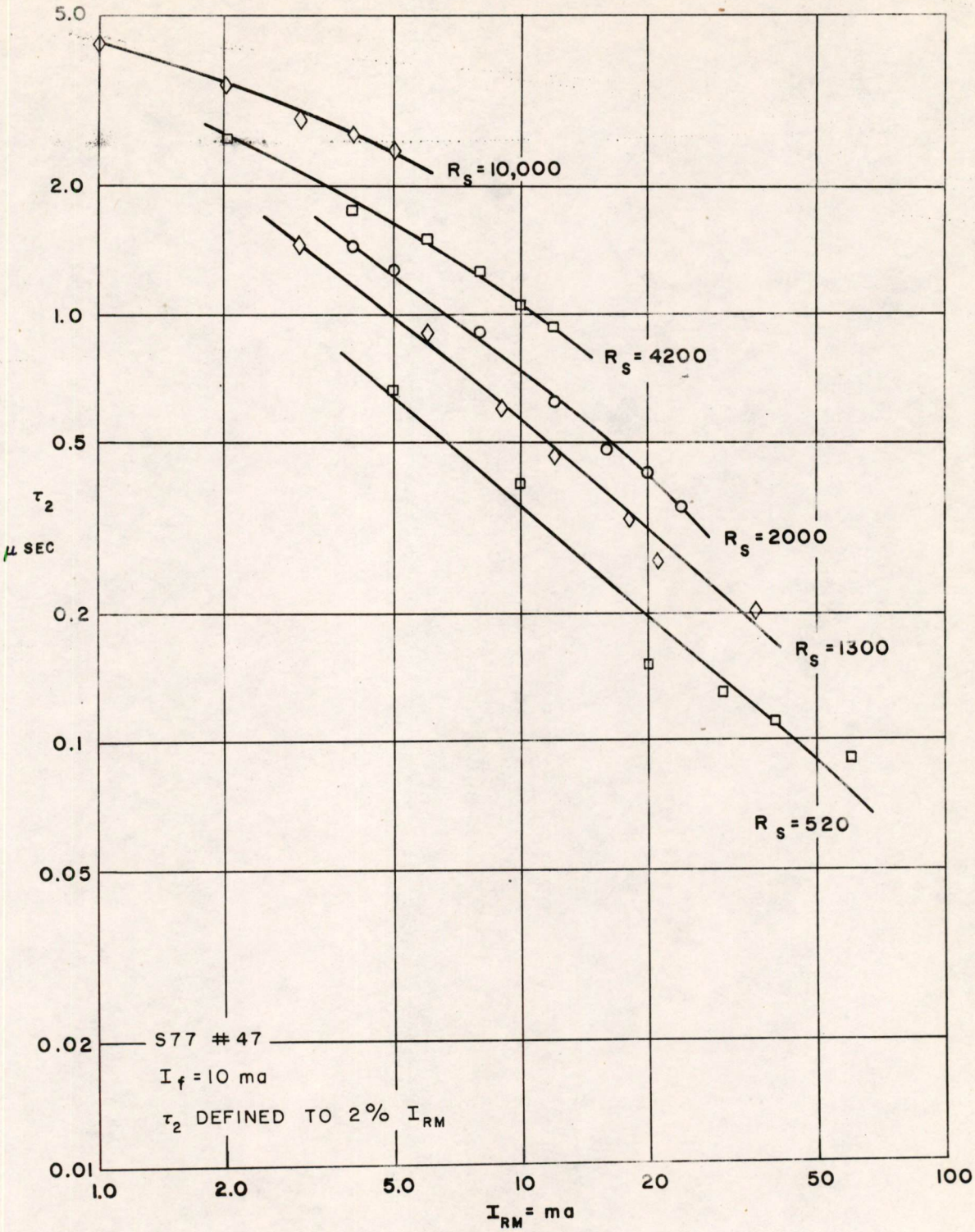
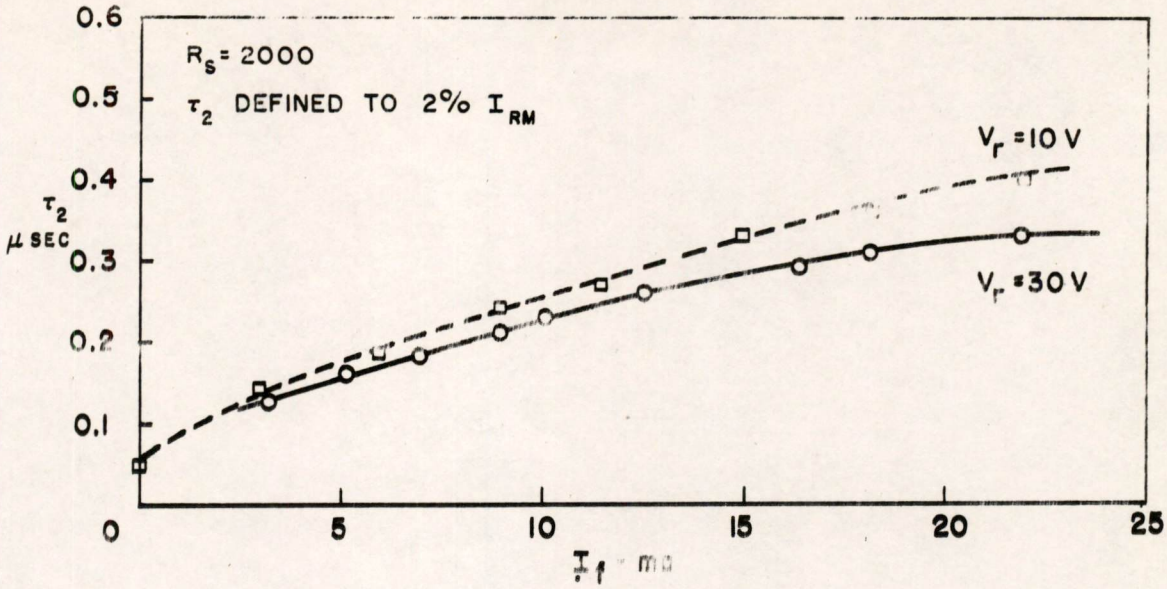



FIG. 3.16

REVERSE RECOVERY OF A BONDED DIODE

$\tau_2$ vs. $I_{RM}$

A-59278



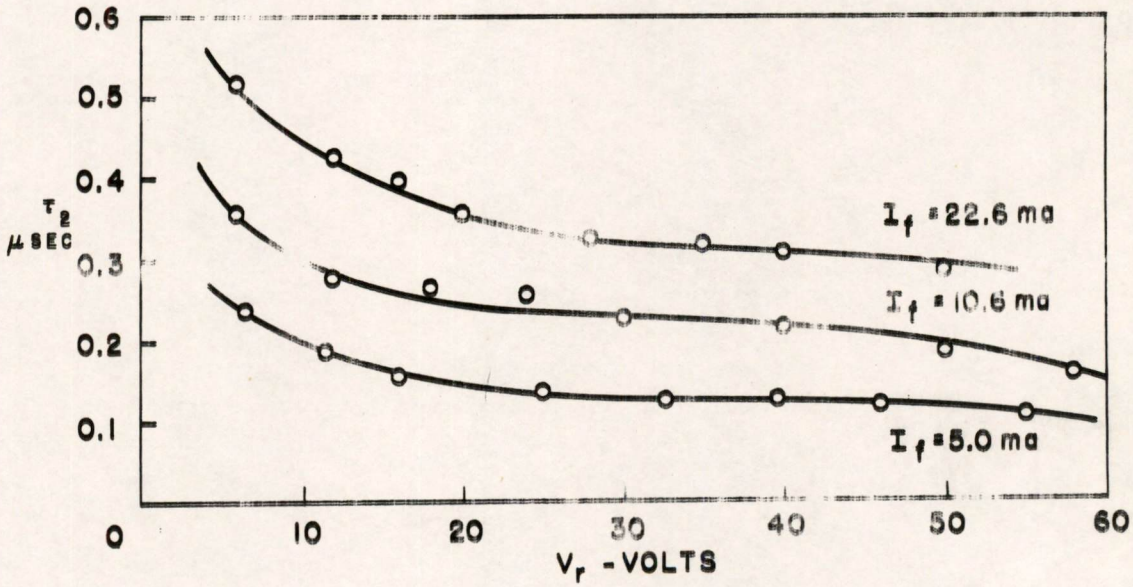




FIG. 3.17

# REVERSE RECOVERY OF A POINT DIODE

IN 34 A # 10

A-59279

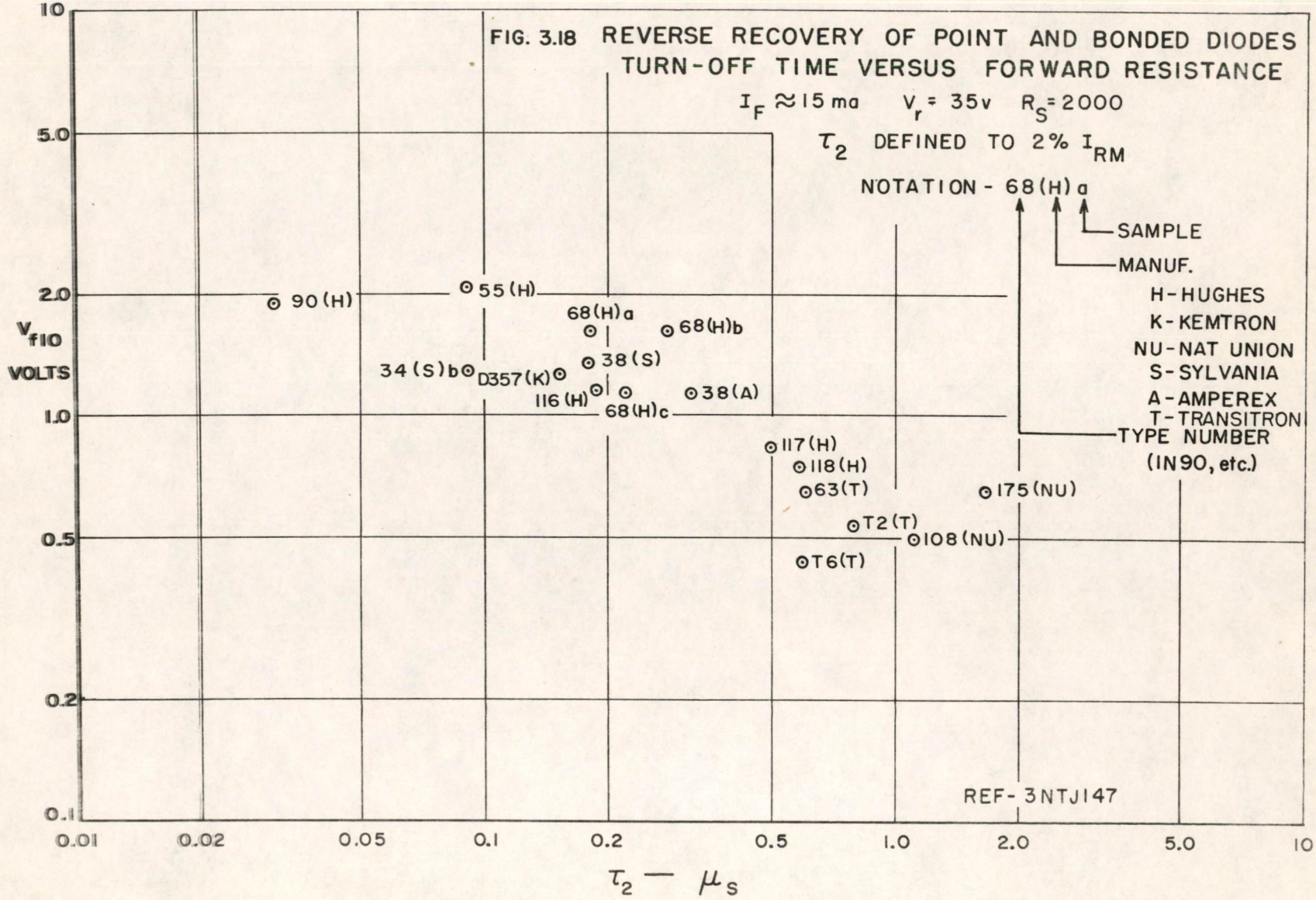


FIG. 3.18 REVERSE RECOVERY OF POINT AND BONDED DIODES
TURN-OFF TIME VERSUS FORWARD RESISTANCE
$I_F \approx 15$ ma $V_r = 35$v $R_S = 2000$
$\tau_2$ DEFINED TO 2% $I_{RM}$
NOTATION - 68(H)a
SAMPLE
MANUF.
H-HUGHES
K-KEMTRON
NU-NAT UNION
S-SYLVANIA
A-AMPEREX
T-TRANSITRON
TYPE NUMBER
(IN90, etc.)
$V_{f10}$ VOLTS
10
5.0
2.0
1.0
0.5
0.2
0.1
0.01
0.02
0.05
0.1
0.2
0.5
1.0
2.0
5.0
10
$\tau_2$ — $\mu_s$
90(H)
55(H)
68(H)a
68(H)b
38(S)
34(S)b
D357(K)
116(H)
68(H)c
38(A)
117(H)
118(H)
63(T)
T2(T)
108(NU)
T6(T)
175(NU)
REF- 3NTJ147

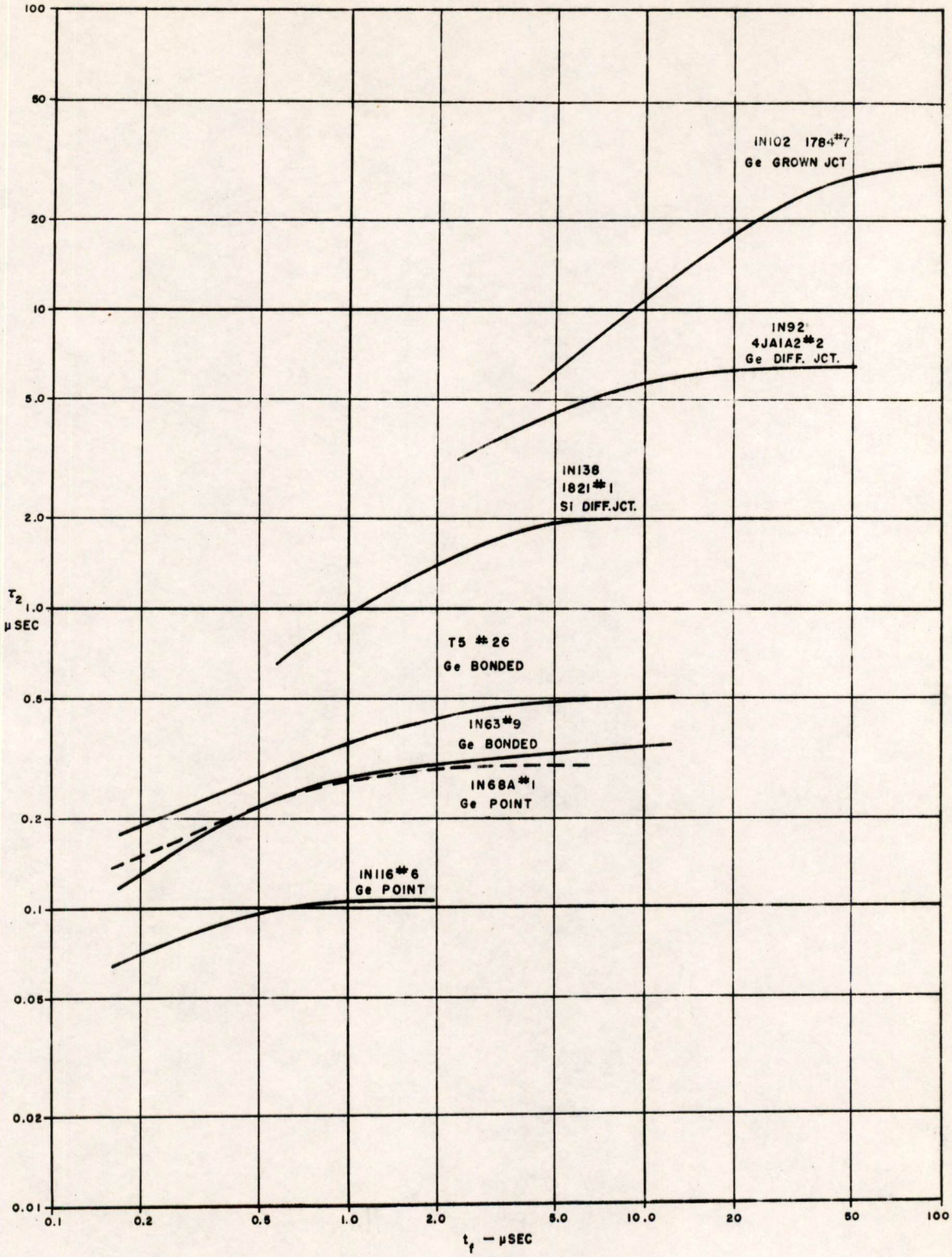



FIG. 3.19

REVERSE RECOVERY BUILDUP TIME IN DIODES

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: FERRITE SYNTHESIS II

To: D. R. Brown

From: F. E. Vinal

Date: February 17, 1954

Abstract: The systematic investigation of the $MgO-MnO-Fe_2O_3$ system for which preliminary results were reported in Memorandum M-2442, has been extended and verified. The patterns of loop squareness vs. composition have remained essentially unchanged, but one new region has been added to the interpretation diagram for the loop-squareness patterns. The tentative phase interpretation which was offered in M-2442 has been confirmed by microstructure studies and has been extended by considering the chemistry of memory-core constituents during heat cycling. A hypothesis is made that any magnetic ferrite phase containing small amounts of $Mn_3O_4$ in cubic solid solution is potentially square hysteresis-loop material. Magnetic measurements taken on the various compositions include coercive force and magnetic induction at saturation and at maximum loop-squareness conditions as well as flux reversal times at maximum loop-squareness. The magnetic measurements are plotted, using the above compositional hypothesis.

## I. HYSTERESIS LOOP SQUARENESS VS. COMPOSITION

A systematic investigation of the $MgO-MnO-Fe_2O_3$ system, which has thus far yielded the suitable ferrite memory cores, was undertaken to establish trends in the electrical and magnetic characteristics with changing composition. Progress in this investigation has been reported previously in Memorandum M-2442[1]. The observed trends have now been

1. Division 6 - Lincoln Laboratory, M. I. T., Cambridge, Mass.; Memorandum M-2442, Subject: Ferrite Synthesis, To: D. R. Brown, From: F. E. Vinal, September 15, 1953.

extended and verified.

The basic composition diagram which has been used to express the relationships of the raw-material constituents is shown in Figure 1. The compositions are given in terms of the three constituent oxides MgO, MnO, and $Fe_2O_3$. Using a ternary diagram for these three materials, obvious points of significance are the midpoints of the MgO-$Fe_2O_3$ side and the MnO-$Fe_2O_3$ side. These points represent the compounds magnesium ferrite, MgO·$Fe_2O_3$ and manganese ferrite, MnO·$Fe_2O_3$ respectively. A line joining these two compositions is the locus of all the possible combinations of MgO, MnO and $Fe_2O_3$ in which the basic formula for a spinel, $AB_2O_4$, is satisfied. The compositions on this line are all stoichiometric in character; that is, the sum of the bivalent oxides is chemically equivalent to the trivalent oxide. All other compositions in Figure 1 represent combinations which are not stoichiometric, and hence contain excesses or deficiencies of one or more constituent oxides. The specific compositions thus far investigated are indicated in Figure 2. Each of the approximately 160 compositions shown has been subjected to 8 or 10 variations in processing. The data presented are based therefore on approximately 1600 samples whose properties have been observed.

The maximum loop-squareness obtained for each composition has been plotted on the basic composition diagram and a contour "weather map" prepared, showing in Figure 3 the loop-squareness pattern vs. composition. The extended data have not substantially modified the similar pattern shown in M-2442. The significance of the "stoichiometry line" as a boundary of the good squareness region is apparent, as is the line connecting the MnO apex with the midpoint of the base, MgO·$Fe_2O_3$. Within the area defined by these two lines, squareness deteriorates as compositions of higher manganese content are prepared. Although no clear-cut boundary is observed in the MnO direction, it is expected that this boundary will clear-up with further work. A simplified diagram for the interpretation of the loop squareness data is shown in Figure 4. The interpretation of the phases, first suggested in M-2442, has now been confirmed by microstructural examination of specimens. Briefly, region A + B + C is single phase, homogenious material while regions D, E and F are two-phase regions. Area A, containing all of the very-good-to-good squareness

values, is a cubic spinel phase while regions B and C are areas of limited solid solution of MgO and $Fe_2O_3$, respectively, in the spinel phase. Fair-to-good loop squareness is possible in areas B and C but the usefulness of these compositions is limited by high firing temperatures and high values of coercive force. For good memory cores consideration may be limited to region A. The contours within region A are interesting because the best area appears, in general, to be in the region of high $MgO \cdot Fe_2O_3$ content, diverging toward the $MnO \cdot Fe_2O_3$ composition and the MnO apex. The deterioration of squareness in the upper central portion of region A is not fully understood, as verification of results in this area, now partially completed, indicate that with careful processing, values in this region may be improved. No improvement has been obtained for compositions close to the MnO apex.

Regions D, E and F are two-phase regions. The examination of suitable series of specimens by metallographic techniques shows clearly the increasing proportions of second phase as the boundaries of region A are crossed to the left and to the right. Region D lying to the left of region A shows a second phase of MgO appearing, at first as scattered grains in the spinel-phase matrix. Later, with increasing MgO content, the MgO may become the matrix and contain isolated grains of the spinel. These results might be expected because all compositions lying to the left of the center line in the composition diagram are so deficient in $Fe_2O_3$ that not even the MgO constituent alone may be satisfied. The granular appearance of the second-phase MgO is consistent with its cubic character. High electrical resistivity is known to be a characteristic in region D and creates some interest for applications where other qualities may be partially sacrificed to obtain high resistivity. Region E, in the lower right, is also a two-phase region but differs from D in that the second phase appears as lamellar sheets. Here the second phase is $\alpha$-$Fe_2O_3$ or haematite, whose growth as lamellar sheets is consistent with the hexagonal structure.

Region F, whose boundary with region A is not yet well defined, is of a more complex character. Microstructural examination of samples in region F has revealed twin-plane structures, containing what appears to be precipitates along the twin planes. The boundary between regions F

and A has been drawn somewhat arbitrarily on the basis of observed twin-plane formation and structural and energy considerations[2], although measurements of limits of good squareness with actual specimens do not at present conform to a straight line in this area. Microstructures illustrative of regions A, D, E, and F are shown in Figure 5.

## II. CHEMICAL CONSIDERATIONS ON SQUARE-LOOP FERRITES

In order to clarify the true nature of the system which yields the square-loop ferrites, the constituents and their chemical properties must be considered. As a start toward such clarification, consider again the pattern of loop-squareness *vs.* composition in Figure 3. As no high values of loop-squareness appear possible in the entire left half of the diagram, that portion may be eliminated from consideration of memory core ferrites. Similarly, the lower right one quarter is no longer of interest. The remaining quarter, in which all the good values of loop squareness have been observed, is still triangular in character, indicating a ternary system. This triangle, redrawn on an equilateral basis, would become a system-composition diagram specifically for the square-loop, memory-core ferrites. The constituents of this system as indicated from the apexes of the revised diagram are magnesium ferrite, $MgO \cdot Fe_2O_3$, manganese ferrite, $MnO \cdot Fe_2O_3$, and the manganese oxide constituent, $MnO$.

Consider first, the behavior of these three constituents individually during heat cycling, similar to that used in processing the ferrite memory cores. Magnesium ferrite is the most stable of the three. This ferrite, found in some quantity in chromite brick, is quite refractory and does not exhibit any tendency to oxidize at high temperatures. Confirmation of its stability has been obtained by thermal analysis. No thermochemical change is observed for $MgO \cdot Fe_2O_3$ between room temperature and 1400°C. At the upper limit of this temperature range there are indications of decreased stability with respect to oxygen loss[3]. The equilibrium partial pressure of oxygen has not been determined as a function of temperature but it is known to be significant in a region of 1400°C,

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2. Division 6 - Lincoln Laboratory, M.I.T., Cambridge, Mass., M-2473, "B-H Loop Squareness in the Magnesium Manganese Ferrites", To: D. R. Brown, From: J. B. Goodenough, October 22, 1953.

3. Roberts, H. S. and Merwin, H. E., "The System $MgO \cdot FeO \cdot Fe_2O_3$ in Air at One Atmosphere", American Journal of Science 21, 145 (1931).

and to become larger as the temperature is further increased. Analogy to the loss of oxygen from $Fe_2O_3$ at high temperatures is suggested[4,5]. Whether the oxygen loss from $MgO \cdot Fe_2O_3$ occurs directly from the undissociated compound or occurs from the $Fe_2O_3$ portion after a dissociation into constituent oxides, is not known but the net result will be the same and may be summarized in the equation:

$$3MgO \cdot Fe_2O_3 \xrightarrow[>1400^{\circ}C]{\Delta} 3MgO + 2Fe_3O_4 + 1/2\ O_2$$

It is therefore seen how "over firing" may affect the electrical and magnetic characteristics of memory cores. The $Fe_3O_4$ formed will readily join in the ferrite phase solid solution and, in very small quantities, perhaps the MgO also; in larger quantities, MgO would be expected to precipitate as a second phase. Changes in magnetic and electrical properties with high firing of $MgO \cdot Fe_2O_3$ may therefore be attributed to some combination of effects of the addition of $Fe_3O_4$ as a constituent and the presence of uncombined MgO. Considerable difficulty is experienced in the formation of suitable samples of $MgO \cdot Fe_2O_3$ because the refractory character of the substance requires sintering temperatures which reach into the range of oxygen instability. In memory core compositions whose sintering temperatures are somewhat reduced over those required for pure $MgO \cdot Fe_2O_3$, the $MgO \cdot Fe_2O_3$ constituent may be considerably stable and not easily susceptible to modification during a memory-core firing cycle in air.

The manganese ferrite constituent on the other hand presents quite a different picture during heat cycling in air. A number of articles[6,7,8] have described the results obtained when this material is heated

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4. Ralston, O. C., U. S. Bur. Mines Paper 296 (1929).
5. Darken, L. S. and Gurry, R. W., "The System Iron-Oxygen II, Equilibrium and Thermodynamics of Liquid Oxide and Other Phases", J. Am. Chem. Soc. 68, 798 (1946).
6. Hilpert, S., Wille, A. and Linder, A.; Z. Physik. Chem. (B) 18, 291 (1932).
7. Harvey, R. L., Hegyi, I. J., and Leverenz, H. W., "Ferromagnetic Spinels for Radio Frequencies", RCA Review 11, 321 (1950).
8. VanArkel, A. E., Verwey, E. J. W. and VanBruggen, M. G., "Ferrites I", Rec. trav. chim. 55, 331 (1936).

in air. All agree that the manganese oxidizes and a mixture of oxides results.

$$3MnO \cdot Fe_2O_3 \xrightarrow[air]{\Delta} Mn_3O_4 + 3Fe_2O_3$$

As neither of these oxides is magnetic, the production of a magnetic phase resulting from the heating of $MnO \cdot Fe_2O_3$ or the heating of an $Mn_3O_4 + Fe_2O_3$ oxide mixture, in air, must be explained by some other mechanism. A number of standard treatises[9] state that $Mn_3O_4$ breaks down further to MnO, i.e., Ephraim, p. 382, 2nd ed., states "MnO....is only stable at atmospheric oxygen pressure at a white heat, and can only be obtained from $Mn_3O_4$ if this temperature is reached." From this, a mechanism of high temperature reaction between MnO and $Fe_2O_3$ to form $MnO \cdot Fe_2O_3$, might be devised, followed by sintering and grain growth into a dense mass. Another possible mechanism might be based on the fact that $Mn_3O_4$ is expressed more correctly as $2MnO \cdot MnO_2$, differing basically from the structure of $Fe_3O_4$ or $FeO \cdot Fe_2O_3$. At high temperatures $Fe_2O_3$ may react with the MnO portion of $Mn_3O_4$ to form $MnO \cdot Fe_2O_3$, leaving $MnO_2$ which, being above 960°C, would convert to more $Mn_3O_4$ as

$$2MnO \cdot MnO_2 + 2Fe_2O_3 \xrightarrow[1300°C]{air} 2MnO \cdot Fe_2O_3 + MnO_2$$

$$MnO_2 \downarrow \rightarrow 1/3\ Mn_3O_4 + 1/3\ O_2 \uparrow$$

Again, sintering and grain growth of the $MnO \cdot Fe_2O_3$ to a dense mass is assumed. Which, if either, of these mechanisms is correct, is not known, but it is certain that a magnetic product is formed from high temperature treatment in air of $Mn_3O_4 + Fe_2O_3$, neither of which is alone magnetic. After the formation of this magnetic phase, which is assumed to be $MnO \cdot Fe_2O_3$, sintering and grain growth would restrict the access of air and tend to off-set reoxidation of the mass during cooling. Solid solution of a small amount of $MnO \cdot Fe_2O_3$ in a bulk of air-stable $MgO \cdot Fe_2O_3$ would greatly assist in desensitizing the manganese to reoxidation. In the study of memory core compositions it has been observed that compositions close to the $MnO \cdot Fe_2O_3$ point are much more sensitive to atmospheric oxidation than those whose composition is mostly $MgO \cdot Fe_2O_3$.

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9. See standard treatises on Inorganic Chemistry, i.e., Mellor, Treatise on Inorganic Chemistry; Ephraim, Inorganic Chemistry; etc.

Examination of the microstructure of a large core, basically a manganese-zinc ferrite, as is used in TV sweep voltage generation, shows the interior to be large, well-sintered, homogenious grains but the surface is two phase and poorly sintered. The two phase portion will follow cracks and flaws into the interior of the piece. In memory core applications the extent to which this oxidation process occurs is a function of the relative proportions of manganese ferrite and the other constituents, the compaction, the sintering and the temperature. An oxidized film on the exterior of a TV transformer core may well be insignificant, but the same film may constitute a high percentage of a memory core whose wall thickness is .015". Again, with manganese ferrite we must not ignore the loss of $O_2$ at very high temperatures from either the ferrite itself or the $Fe_2O_3$ oxidation product, with the consequent addition of $Fe_3O_4$ to the spinel phase.

It has been determined experimentally, that cooling from peak temperature in an inert (nitrogen) atmosphere yields a better memory core product than is obtained with air cooling. Closer examination of the effects of the inert atmosphere indicates that protection of a magnetic manganese ferrite against reoxidation is not the only possible effect. The oxygen instability and loss from $Fe_2O_3$ and ferrites at high temperatures will be affected by an inert atmosphere. In the case of uncombined $Fe_2O_3$ a nitrogen atmosphere would aid the conversion to $Fe_3O_4$ with respect to both rate and temperature of conversion. The $Fe_3O_4$, being a cubic spinel, would favor the formation of a single phase product and thus enhance the possibilities for loop squareness from that point of view. On the other hand, the effects of $Fe_3O_4$ as a constituent have not been ascertained in regard to the other electrical and magnetic properties of memory cores. It therefore is not clear, at this time, whether nitrogen cooling is entirely beneficial with respect to assisting in the conversion of $Fe_2O_3$ to $Fe_3O_4$. For the case of a ferrite such as $MgO \cdot Fe_2O_3$ showing oxygen loss at high temperature, the increased conversion of $Fe_2O_3$ to $Fe_3O_4$, by a nitrogen atmosphere, would inevitably increase the uncombined MgO content of the cooled ferrite. This would not be favorable to the production of good memory cores. Optimum processing conditions would therefore seem to require a compromise between high temperatures, favorable to the formation of a magnetic manganese ferrite and the sintering of

$MgO \cdot Fe_2O_3$, and somewhat lower temperatures, favoring oxygen stability in the ferrites. Using a nitrogen atmosphere for cooling accentuates the need for lower sintering temperatures.

The manganese oxide constituent also requires attention in heat cycling, primarily because it has been demonstrated that approximately the same result is obtained no matter which oxide of manganese is employed as a starting material, provided the variation in molar relationships among the oxides is placed on an equivalent basis for combination with $Fe_2O_3$. The oxides of manganese are the subject of considerable literature[9]. As they are heated in air they all are changed to cubic $Mn_3O_4$ above 1170°C.

1. $MnO \xrightarrow[air]{\Delta} (T)Mn_3O_4 \xrightarrow[air\text{-}1170^\circ C]{\Delta} (C)Mn_3O_4$

2. $Mn_2O_3 \xrightarrow[air\text{-}950^\circ C]{\Delta} (T)Mn_3O_4 \xrightarrow[air\text{-}1170^\circ C]{\Delta} (C)Mn_3O_4$

3. $(T)Mn_3O_4 \xrightarrow[air\text{-}1170^\circ C]{\Delta} (C)Mn_3O_4$

4. $MnO_2 \xrightarrow[air\text{-}650^\circ C]{\Delta} Mn_2O_3 \xrightarrow[air\text{-}950^\circ C]{\Delta} (T)Mn_3O_4 \xrightarrow[air\text{-}1170^\circ C]{\Delta} (C)Mn_3O_4$

In the sintering range for ferrites, in air, uncombined manganese oxide will be present as $(C)Mn_3O_4$ no matter what oxide of manganese was used as a starting material. Upon cooling through 1170°C, $Mn_3O_4$ reverts to the tetragonal form and so remains down to room temperature.

It appears, therefore, that starting with a mixture of $MgO \cdot Fe_2O_3$, $MnO \cdot Fe_2O_3$, and MnO, then raising the temperature in air to the sintering range for ferrites, the following are relatively stable forms which can co-exist: $MgO \cdot Fe_2O_3$, $(C)Mn_3O_4$, $\alpha$-$Fe_2O_3$, and $MnO \cdot Fe_2O_3$. The particular combination which will exist for a given starting mixture will depend principally on the relative proportions of the starting mixture. The forms stable at high temperature are all stable during cooling to room temperature except for the polymorphic change of $(C)Mn_3O_4$ to $(T)Mn_3O_4$ at 1170°C and reoxidation of $MnO \cdot Fe_2O_3$ at temperatures a little below white heat. If any sort of protection is provided against reoxidation of the $MnO \cdot Fe_2O_3$, it too will reach room temperature without change. Such protection may be provided by grain growth and sintering to a dense mass, nitrogen cooling atmosphere, solid solution of a small amount of $MnO \cdot Fe_2O_3$ in a bulk of an air-stable ferrite, quenching or some combination of these four methods. $Mn_3O_4$ in small amounts has been found to remain in cubic

solid solution with a spinel ferrite structure below 1170°C[10,11]. In predominant amounts, the tetragonality of the $Mn_3O_4$ shows its effect in the twin-plane structures of region F, Figure 4, where the twinning may be considered as a stress-relief mechanism in a tetragonal-cubic mixture.

The good values of loop-squareness have all been obtained with compositions of the general formula

| Mols | Constituent oxide |
|---|---|
| x | MgO |
| y | MnO |
| z | $Fe_2O_3$ |

where $z \geqq x$ but $z < x + y$.

This is interpreted to mean that the MgO must be satisfied by $Fe_2O_3$ and that the formation of $MgO \cdot Fe_2O_3$ occurs preferentially. After the formation of x mols of $MgO \cdot Fe_2O_3$, any $Fe_2O_3$ remaining may form (z - x) mols of $MnO \cdot Fe_2O_3$. Any uncombined MnO then remaining will be equal to y - (z - x) mols which, on heating, would convert to $\frac{y - (z - x)}{3}$ mols of $Mn_3O_4$. Assuming protection against oxidation of the $MnO \cdot Fe_2O_3$ by solid solution with $MgO \cdot Fe_2O_3$ or by other means, the final ferrite memory core should consist of a single phase cubic spinel solid solution of $MgO \cdot Fe_2O_3$ + $MnO \cdot Fe_2O_3$ + $Mn_3O_4$. In this composition it is assumed also that the $Mn_3O_4$ content is small compared to the total ferrite phase, so that the $Mn_3O_4$ will be sure to join the ferrite phase in cubic solid solution. Good loop-squareness has been observed for compositions which would be satisfied by a solid solution of $MgO \cdot Fe_2O_3$ and $Mn_3O_4$. It therefore appears that $MnO \cdot Fe_2O_3$ is not basic to loop-squareness but the $Mn_3O_4$ is a basic constituent.

From the above analysis, a hypothesis is made. The hypothesis is stated as follows:

> "Any magnetic ferrite plus $Mn_3O_4$, existing together as a single phase cubic spinel, is potentially a square hysteresis-loop material."

This hypothesis implies that the magnetic ferrite phase may be composed

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10. McMurdie, Sullivan and Mauer, Journal of Research of the National Bureau of Standards, 45, 35, (1950).

11. Romeijn, F. C., Phillips Technical Reports, 8, 304, (1953).

of a single ferrite or more than one ferrite, not all of which need be magnetic provided the overall blend is a magnetic ferrite phase.

## III. MAGNETIC MEASUREMENTS OF MEMORY CORES

For most of the memory core compositions detailed in Section I, measurements of the following magnetic properties have also been taken:

1. Coercive force at maximum loop-squareness conditions
2. Coercive force at saturation (30 Oersteds)
3. Magnetic Induction at maximum loop-squareness conditions
4. Magnetic Induction at saturation (30 Oersteds)
5. Flux reversal time at maximum loop-squareness conditions.

The handling of these data had proven troublesome until they were treated as a function of the composition, where the composition was expressed as a ratio of the total possible mols of the ferrite phase to the mols of the excess manganese oxide constituent, $Mn_3O_4$. Essentially the same curves would be obtained using MnO instead of $Mn_3O_4$ as the form of the excess manganese but this form would not exist after air firing of the powder compact.

Typical data are shown in Figures 6 to 9 for materials in which the amount of $Fe_2O_3$ was always chemically equivalent to the amount of MgO, hence the manganese content should all be present uncombined, as $Mn_3O_4$ in solid solution with the spinel phase. These samples are obtained by progressing up the centerline of Figure 4 toward the MnO apex from pure $MgO \cdot Fe_2O_3$ at the base. Figure 6 shows the loop-squareness values expressed as the squareness ratio[12]. In general terms, values of 0.80 to 0.85 are most suitable for memory core use. Figures 7 through 9 show the coercive force, magnetic induction and flux reversal time values respectively. While these data do not in any way prove the compositional hypothesis, the appearance of the curves lends support to the idea.

## IV. SUMMARY

The present state of the art regarding memory-cores and other square-loop ferrites may be summarized as follows:

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12. Division 6 - Lincoln Laboratory, M.I.T., Cambridge, Mass., "A Squareness Ratio for Coincident-Current Memory Cores", Engineering Note E-464, To: Group 63 Staff, From: D. R. Brown, July 17, 1952.

1. The most satisfactory compositions in the $MgO-MnO-Fe_2O_3$ system are known.

2. Explanations have been found for the failure of some compositions and the success of others.

3. A considerable understanding of reasons for the critical character of the required processing has been achieved.

4. It is now possible to recognize many of the significant chemical problems which must be solved to put loop-squareness on a sound scientific basis.

5. The present knowledge of square-loop ferrites, even though limited, would permit a logical start in the development of new square-loop materials, as needed, with pre-specified mangetic and electrical characteristics.

Signed F E Vinal
F. E. Vinal

Approved D R B
D. R. Brown

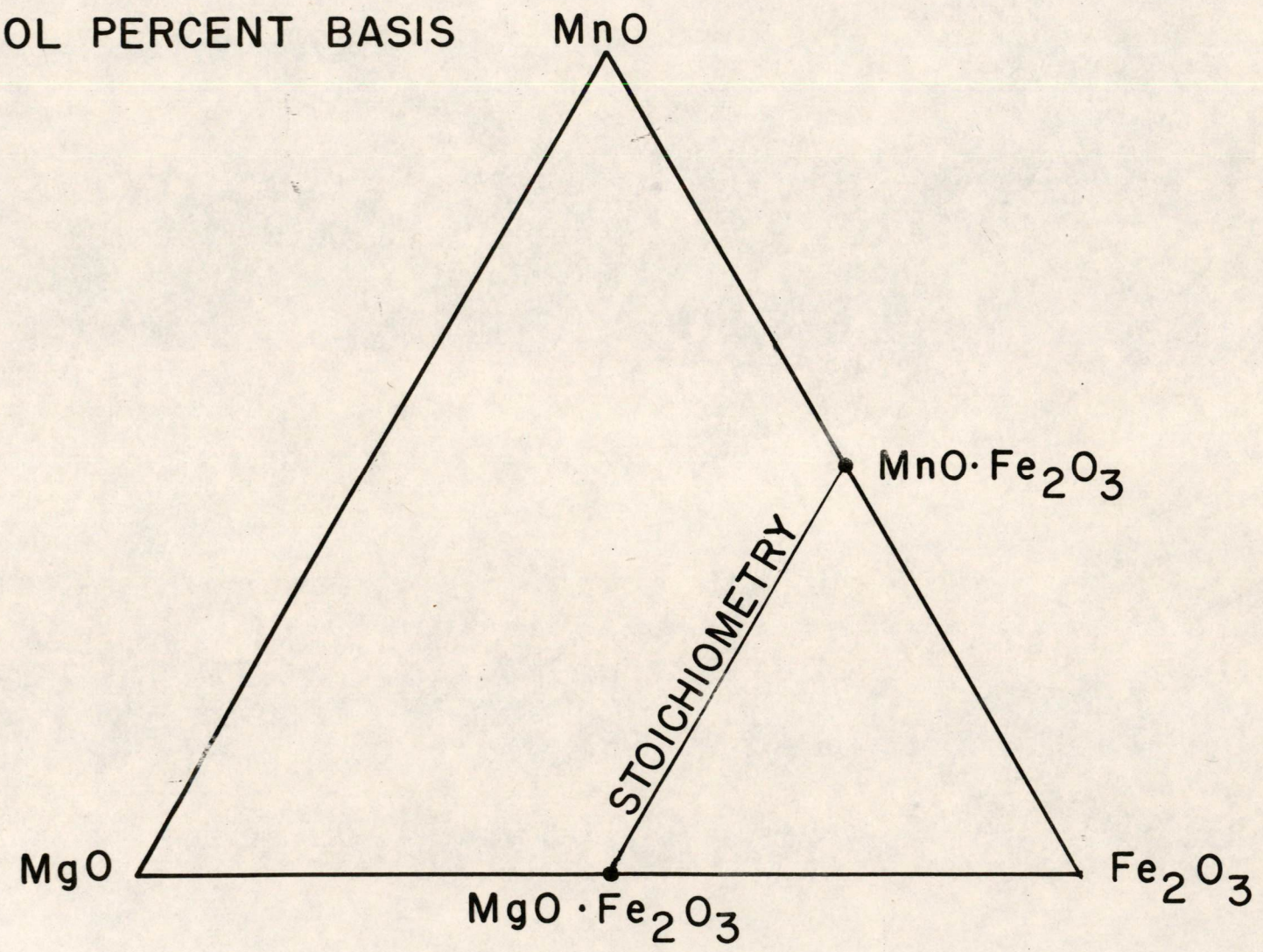
FEV/djd

Drawings Attached:
Figure 1 B-57066
Figure 2 B-56130-1
Figure 3 C-56411
Figure 4 B-56368-1
Figure 5 A-57953
Figure 6 B-57070
Figure 7 B-57062
Figure 8 B-57071
Figure 9 B-57061

cc: Group 63 Staff
Group 62 - N. H. Taylor and Section Leaders
Group 37 Staff
Group 35 - H. Priest, W. Z. Leavitt
IBM (Kromer)

B-57066

F-2153
SN-664




# FERRITE MEMORY CORE
# TERNARY COMPOSITION DIAGRAM

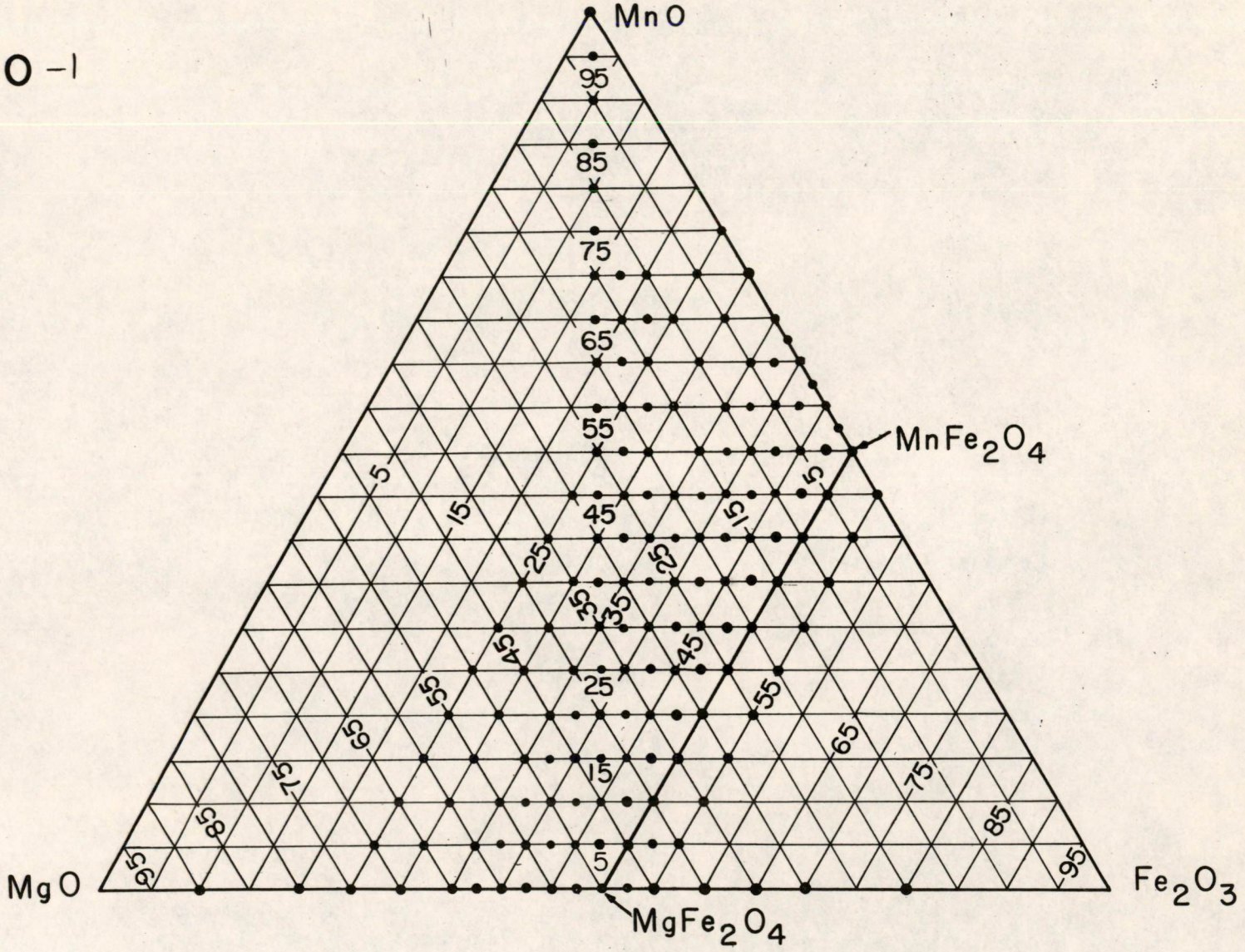
F16.1

B-56130-1

F-2146

SN-657

MN

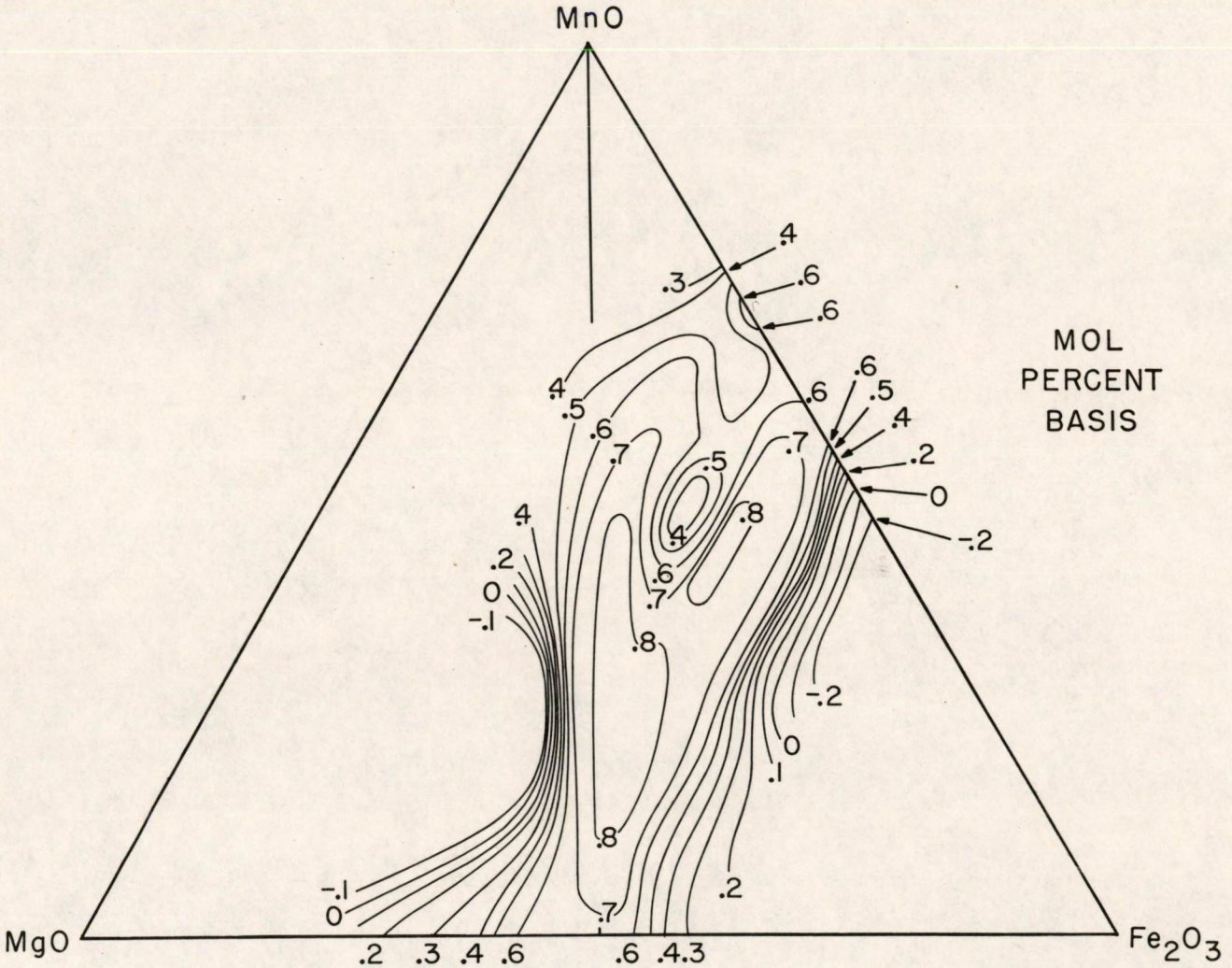



COMPOSITIONS INVESTIGATED IN THE

$MgO:MnO:Fe_2O_3$ OXIDE SYSTEM MOL PERCENT BASIS

FIG. 2

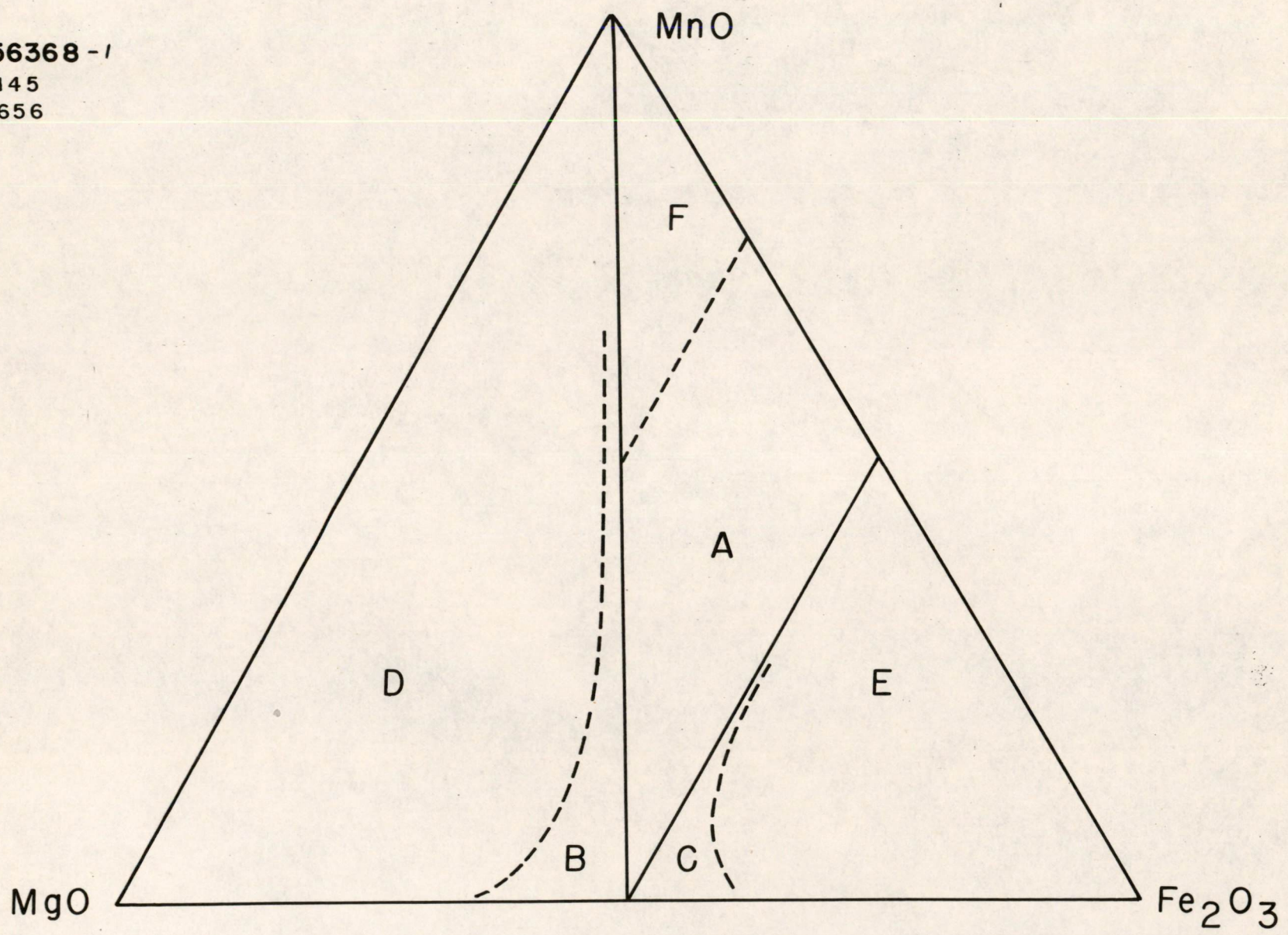
C-56411-1
F-2154
SN-665
MN




LOOP SQUARENESS VS. COMPOSITION FOR THE MgO · MnO · $Fe_2O_3$ SYSTEM

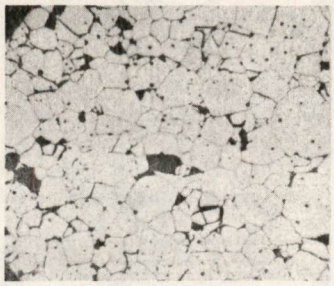
FIG. 3

B-56368-1
F-2145
SN-656
MN

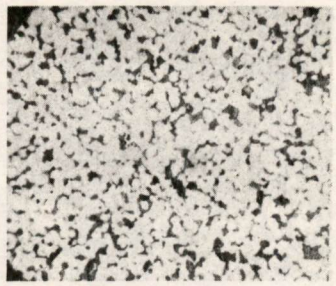



# INTERPRETATION OF HYSTERESIS-LOOP-SQUARENESS

FIG 4

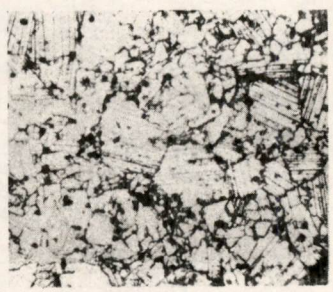


REGION A



REGION D

REGION E



REGION F

# MICROSTRUCTURES OF FERRITES IN THE $MgO \cdot MnO \cdot Fe_2O_3$ SYSTEM

A-57953

-57070
F-2152
SN-663
MN

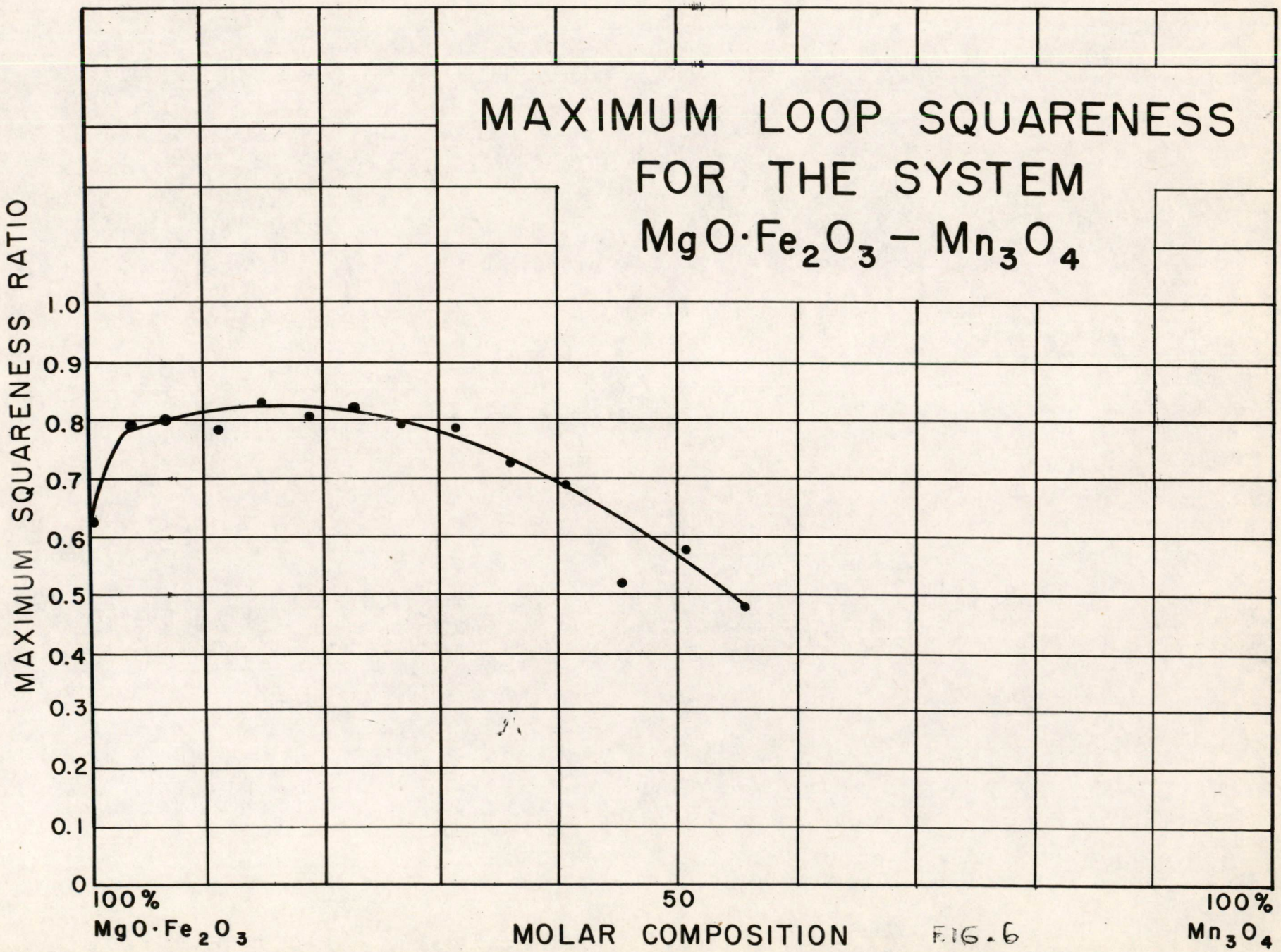



FIG. 6

B-57062
F-2151
SN-662
MN

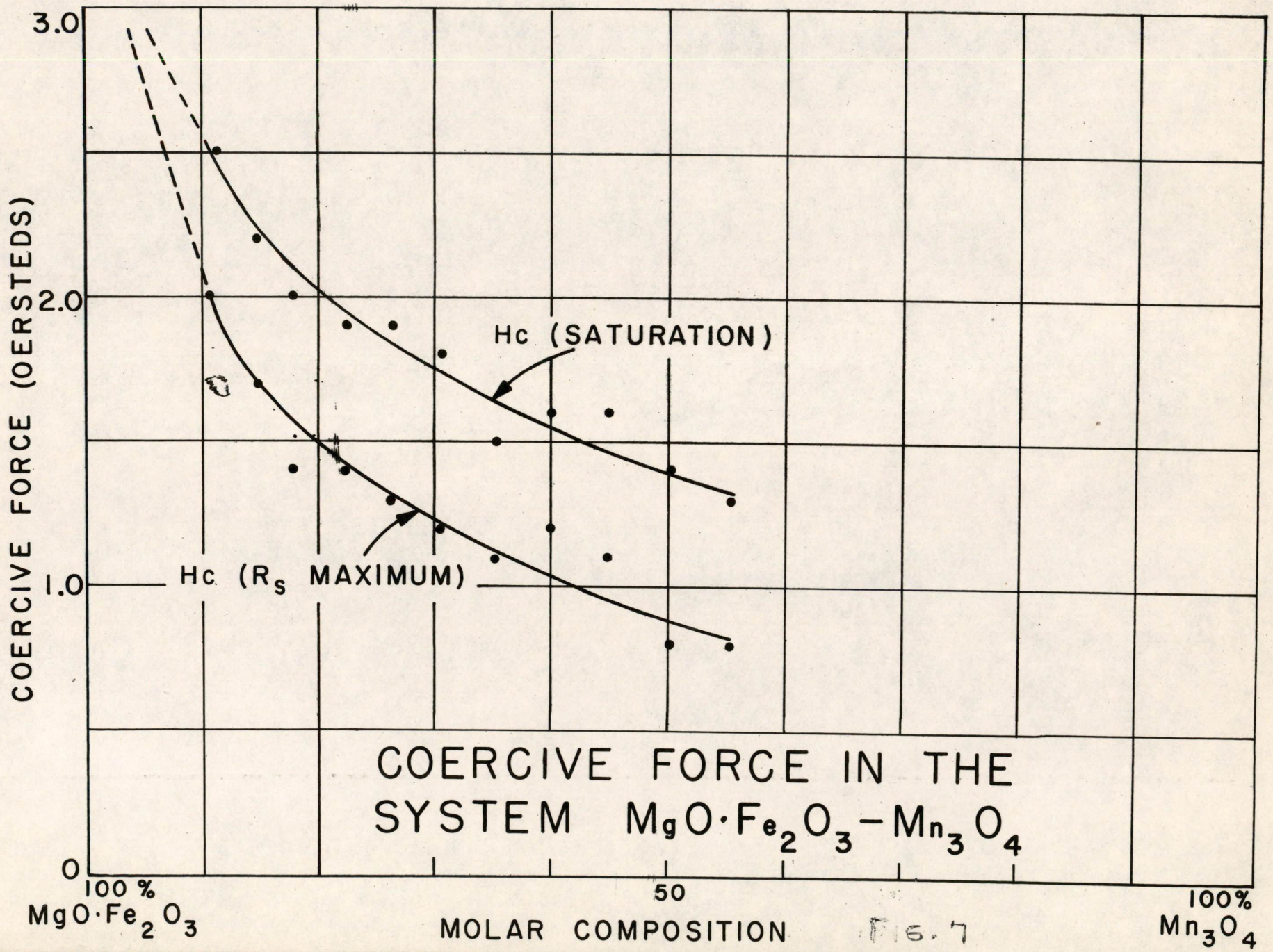



FIG. 7

B-57071
F-2149
SN-660
MN

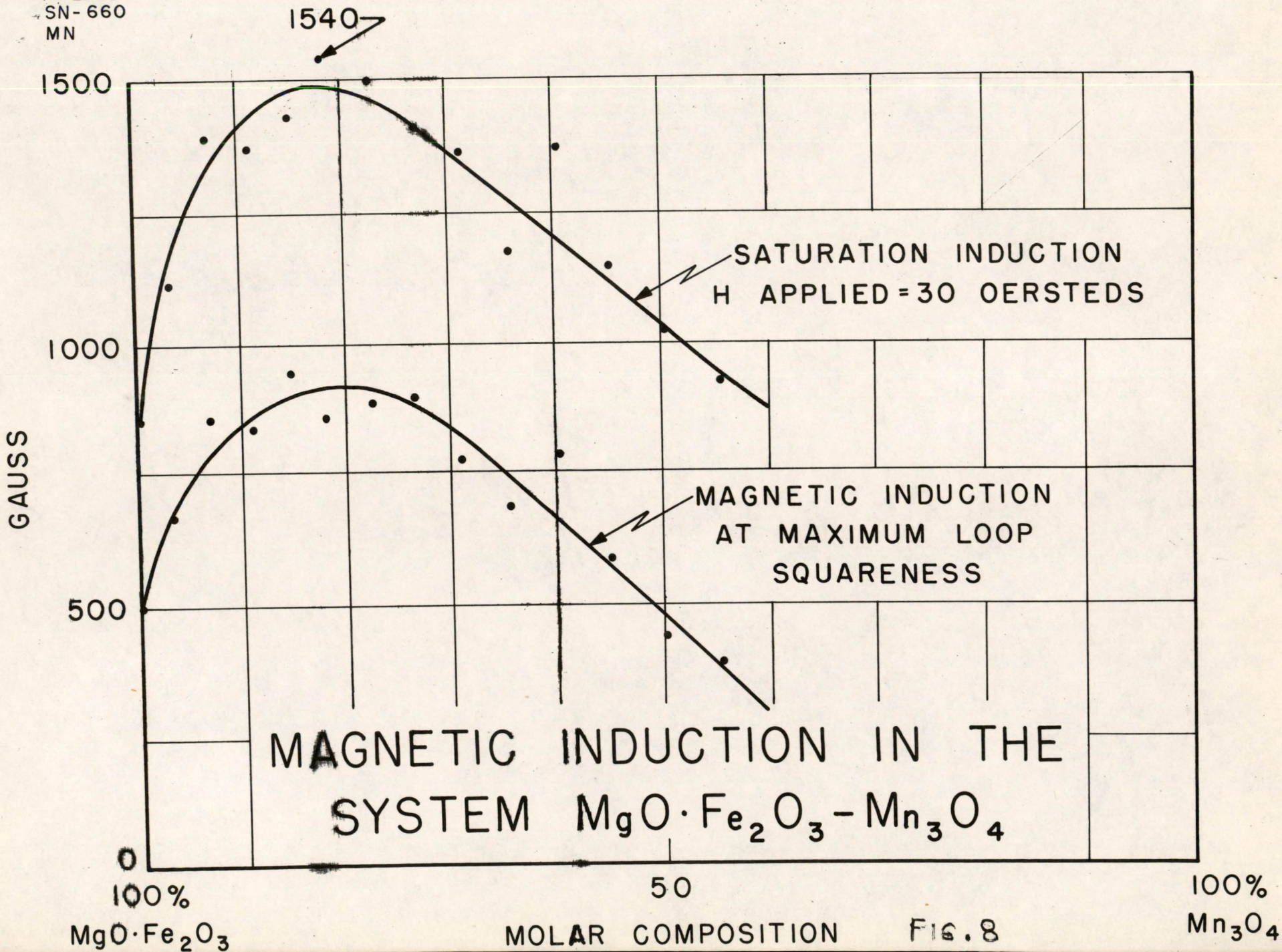



Fig. 8

B-57061
F-2147
SN-658
MN

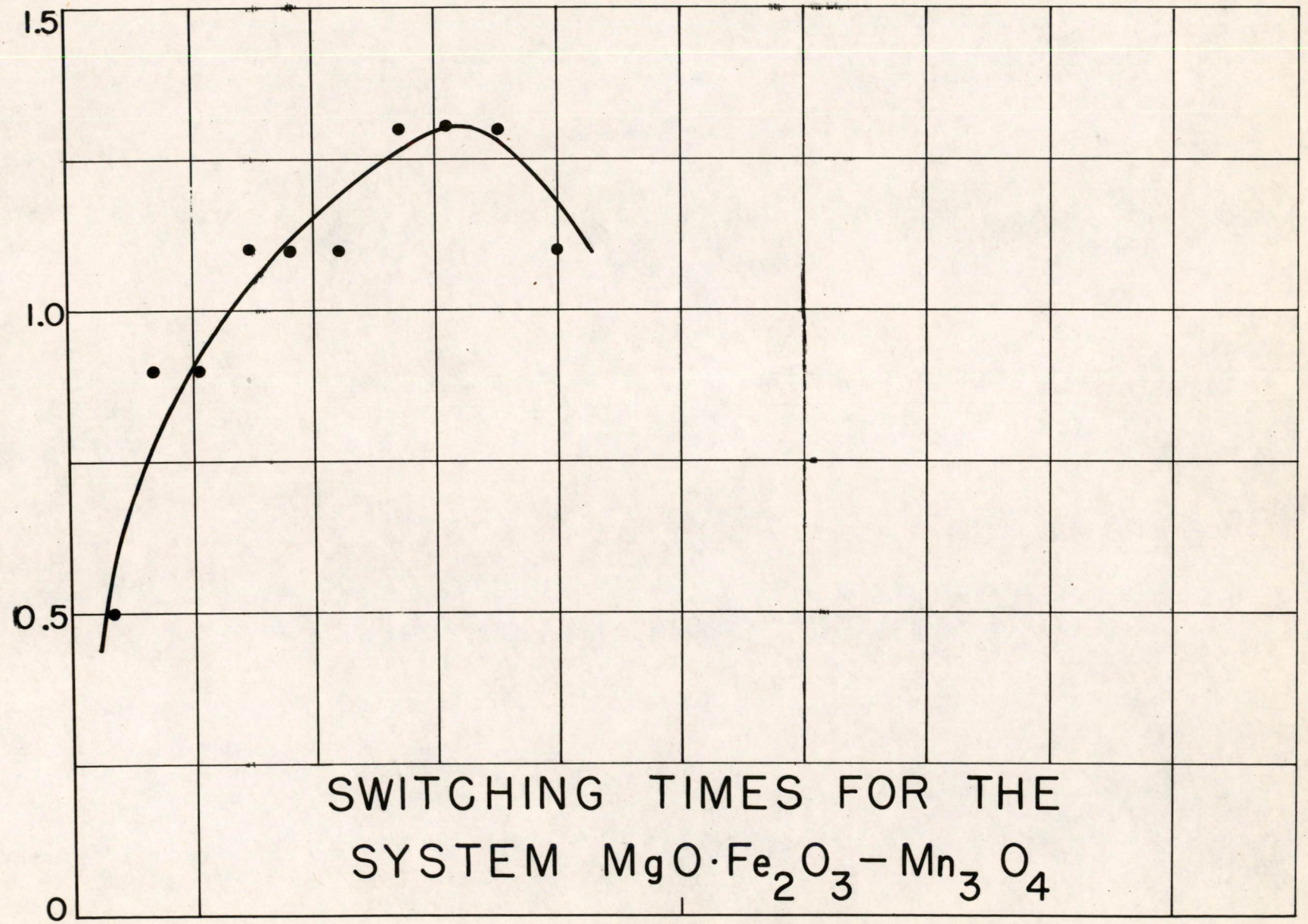



FIG. 9

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: DELAY CIRCUITS

To: N. H. Taylor

From: J. S. Gillette

Date: April 6, 1954

Abstract: A delay circuit has been developed which can delay standard 0.1 μsec pulses from 0.5 to 2 μsec when driven with a tetrode connected 7AK7 or 0.5 to 1.5 μsec when driven with a 7AK7 gate, both using a 1:1 transformer. These circuits may be used with pulse repetition rates up to 500 KC or the reciprocal of twice the nominal delay, whichever is smaller. For applications at a higher p.r.f., refer to the Basic Circuits Group. Marginal checking may be accomplished by varying the 90 volt supply.

## Introduction

The circuit consists of a 7AK7 tube, which is either gate connected or tetrode connected, driving a 1350 ohm distributed delay line through a 1:1 pulse transformer.* The delay line is terminated with a peaking inductance in parallel with a crystal damping diode. The d-c level is returned to -30 volts, instead of the usual -15 volts, so that any noise generated by the delay line is less likely to be fed through the output tube. Since the d-c level is at -30 volts, it cannot directly drive flip-flops. The load which can be driven is limited to one unit of load.

## The Delay Line

Most of the work covered in this report has concentrated on the application of high impedance distributed delay line: G.E. Cat. No. 5111891 DCL No. 211 5 1100. The line has a bandwidth of about two megacycles, which is quite small compared to the fundamental components of a 0.1 μsec pulse. The line tends to widen out the pulse and produces some noise just before the delayed pulse appears at the end of the line. The widening of the pulse can be attributed to both the amplitude distortion and phase distortion. The noise which precedes the pulse can be attributed to phase distortion and capacity feed through. It was found that the lines of shortest physical length per unit of delay produced the most feed through. These lines were either tightly wound or wound on a larger diameter core, both of which would have increased capacity from turn to turn. It actually appears that the more irregular-

*See Figs. 9 and 10

ly wound lines performed better.

## Circuit Design

The original delay circuit which appeared in the MRD Book (Section 131, MD 103, issue 1) had a noise output of about four volts and could only drive 30 μμfds of load. This was considered quite risky. It is conceivable that this noise could increase as diodes go bad. To eliminate this possibility, the line is now returned to -30 volts. This meant that the line must be driven harder to overcome the additional 15 volts of bias. To prevent the output from becoming too large when the input is 40 volts, a series grid-limiting resistor is used. It would seem desirable to use as much grid limiting as possible and take advantage of the amplitude standardization which results. However, as the grid resistor is increased, the pulse shape becomes distorted and the signal-to-noise ratio becomes worse. Also, the voltage across the damping diode becomes larger.

For the shortest lengths of delay, since the attenuation is less, all of the limiting cannot be done in the grid circuit. Therefore, Resistor $R_1$ is placed in series with the delay line when necessary. $R_1$ also performs the functions of partially terminating reflections on the line as they return toward the pulse transformer. $R_1$ also has some effect on the width of the pulse. The best compromise was found for various lengths of delays and the values of $R_1$ and $R_2$ are tabulated in Figure 11.

The diodes at the end of the line are needed to damp the peaking inductance. Two diodes are necessary to limit the voltage across any one diode to 50 volts peak.

A 39-ohm resistor is placed in series with the diodes to reduce the p.r.f. variation of output. When the diode forward resistance is low, the p.r.f. variation of output is greatest. This resistor was made as large as possible to limit p.r.f. variations but not large enough to allow the noise output to increase too much. With the diodes at end of life, with a 40-volt input, and with a hot tube the noise pulse will be less than two volts. A plot of the output noise vs the forward resistance is shown in Figure 12.

## Transfer Characteristics

The plots of input pulse amplitude vs output pulse amplitude for various screen voltages are shown in Figures 1 to 7. The output available for various screen voltages is indicative of the circuit margins. It should be noted that although the plots do not show points for each reading taken, they are drawn through the points taken and are

not an artist's conception.

The plots of pulse width input vs pulse width output are not complete, but the points taken are taken under various conditions that indicate that the pulse widths are within specifications under the most adverse conditions. Typical data is tabulated in Figure 8.

The amplitude of the pulse will not vary with p.r.f more than ±10% under the most adverse conditions. For some lengths of delay, the amplitude variation will not exceed ±2%. The largest variations occur at the critical frequencies where the p.r.f. is a submultiple of the delay time. The variation is shown with each amplitude plot.

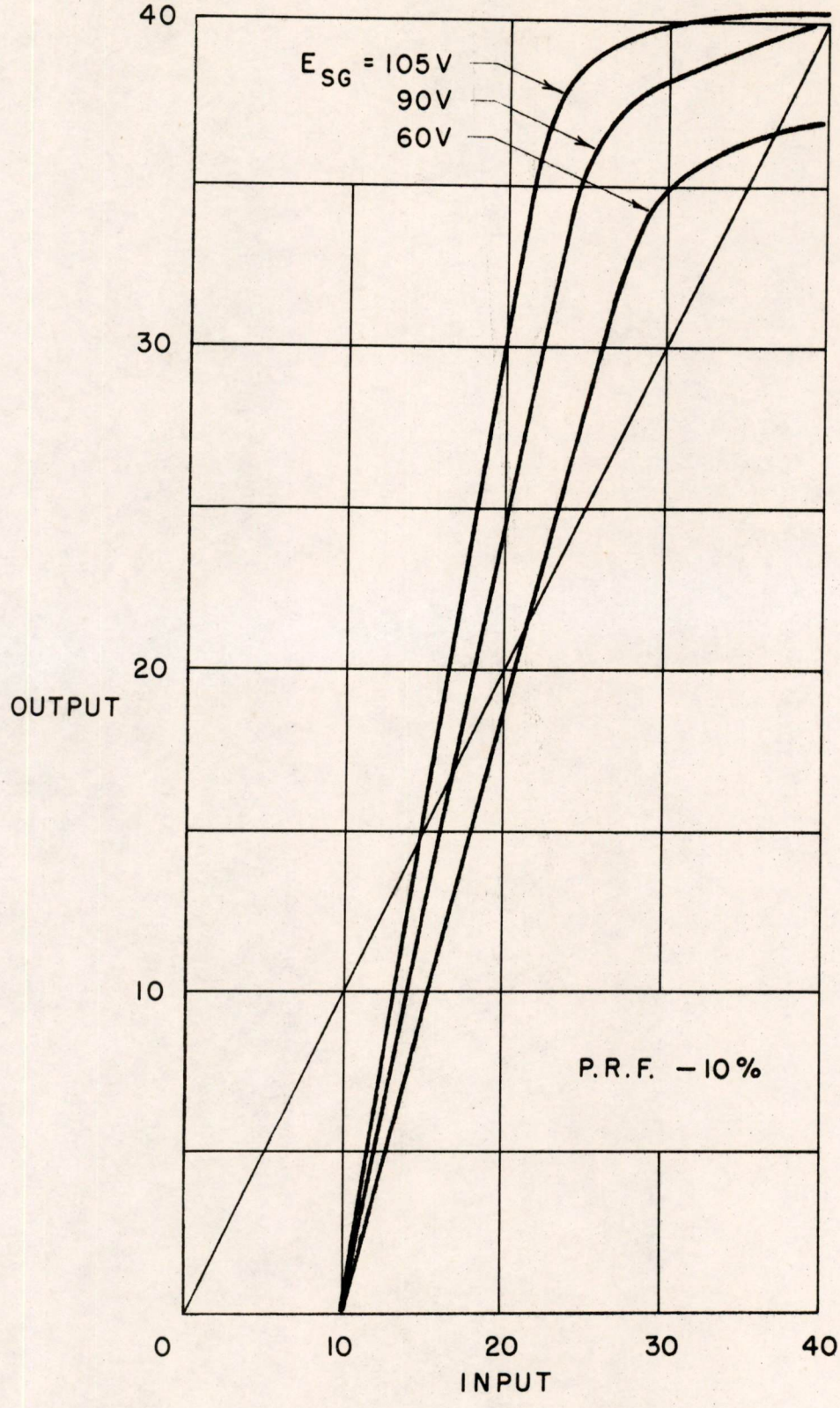
Signed: Jack S Gillette
J. Gillette

Approved: R L Best
R. Best

JSG:ts:meo

Drawings Attached

| | |
|---|---|
| A-57792 | A-57798 |
| 57793 | 57799 |
| 57794 | 57800 |
| 57795 | 57801 |
| 57796 | 57802 |
| 57797 | |




A-57792

*FIG. 1*

TRANSFER PLOT FOR TETRODE-CONNECTED 2.0 μSEC DELAY CIRCUIT

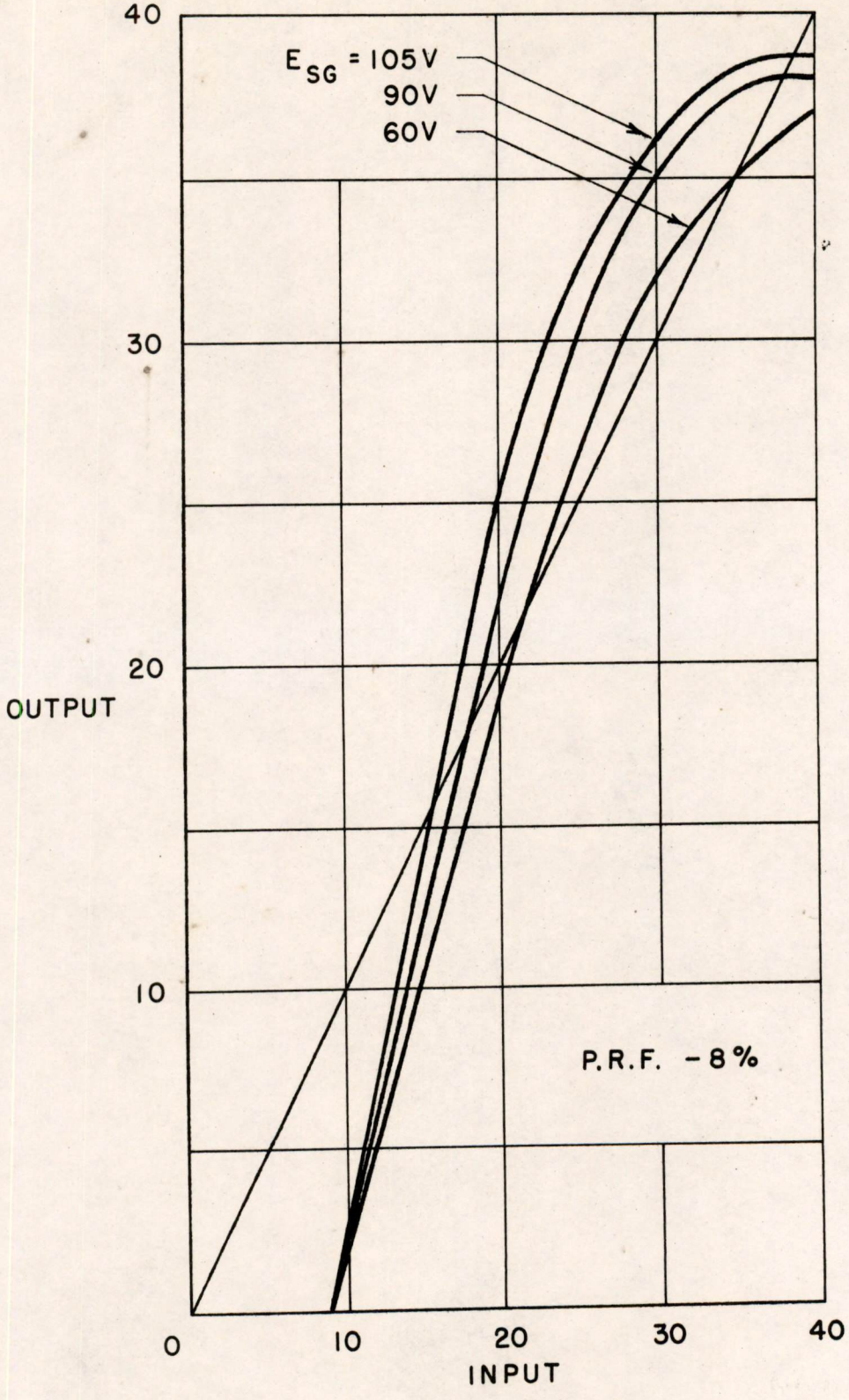
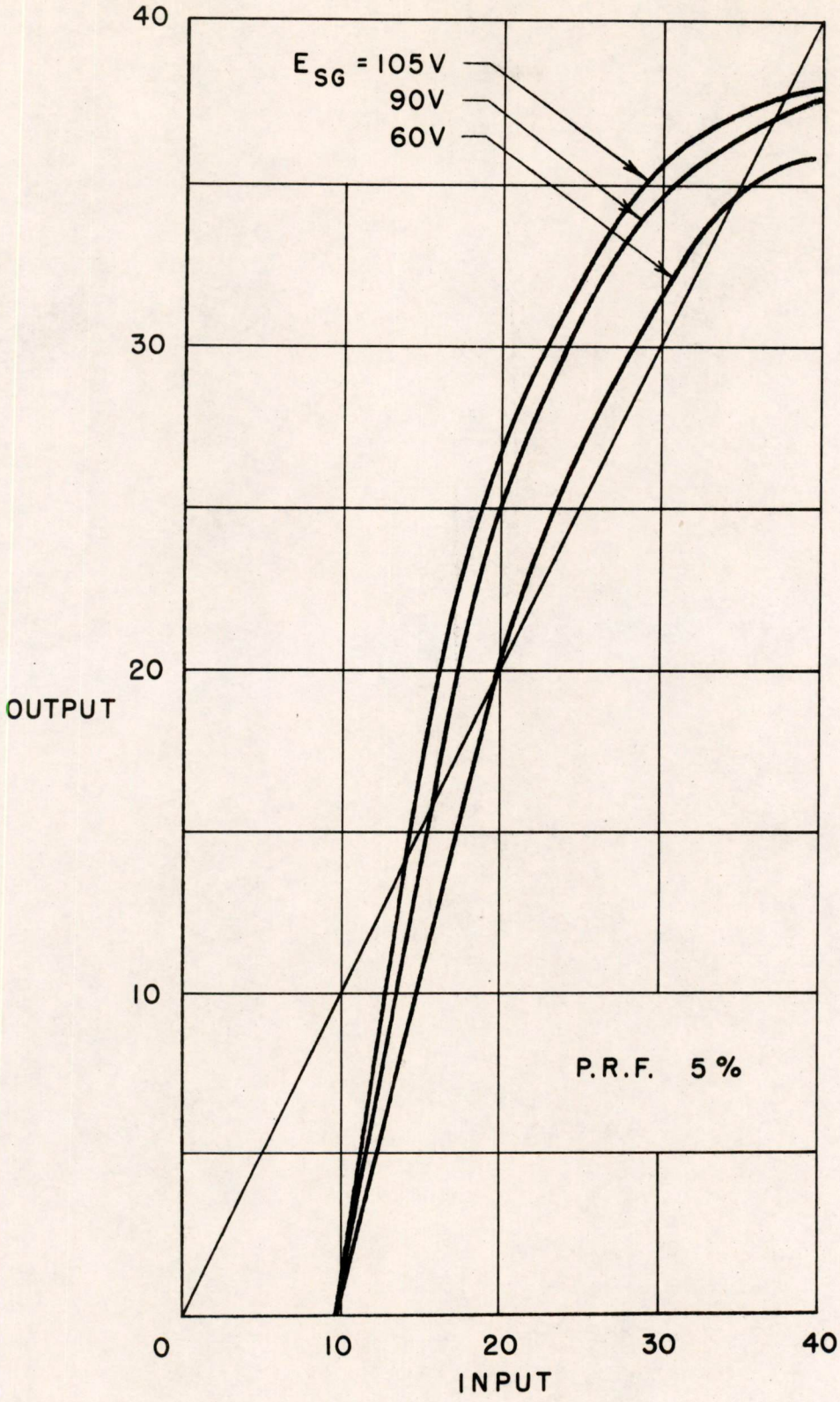



FIG. 2

TRANSFER PLOT FOR TETRODE-CONNECTED 1.5 μSEC DELAY CIRCUIT

A-57793




A-57794

*FIG. 3*

TRANSFER PLOT FOR TETRODE-CONNECTED 1.0 μSEC DELAY CIRCUIT

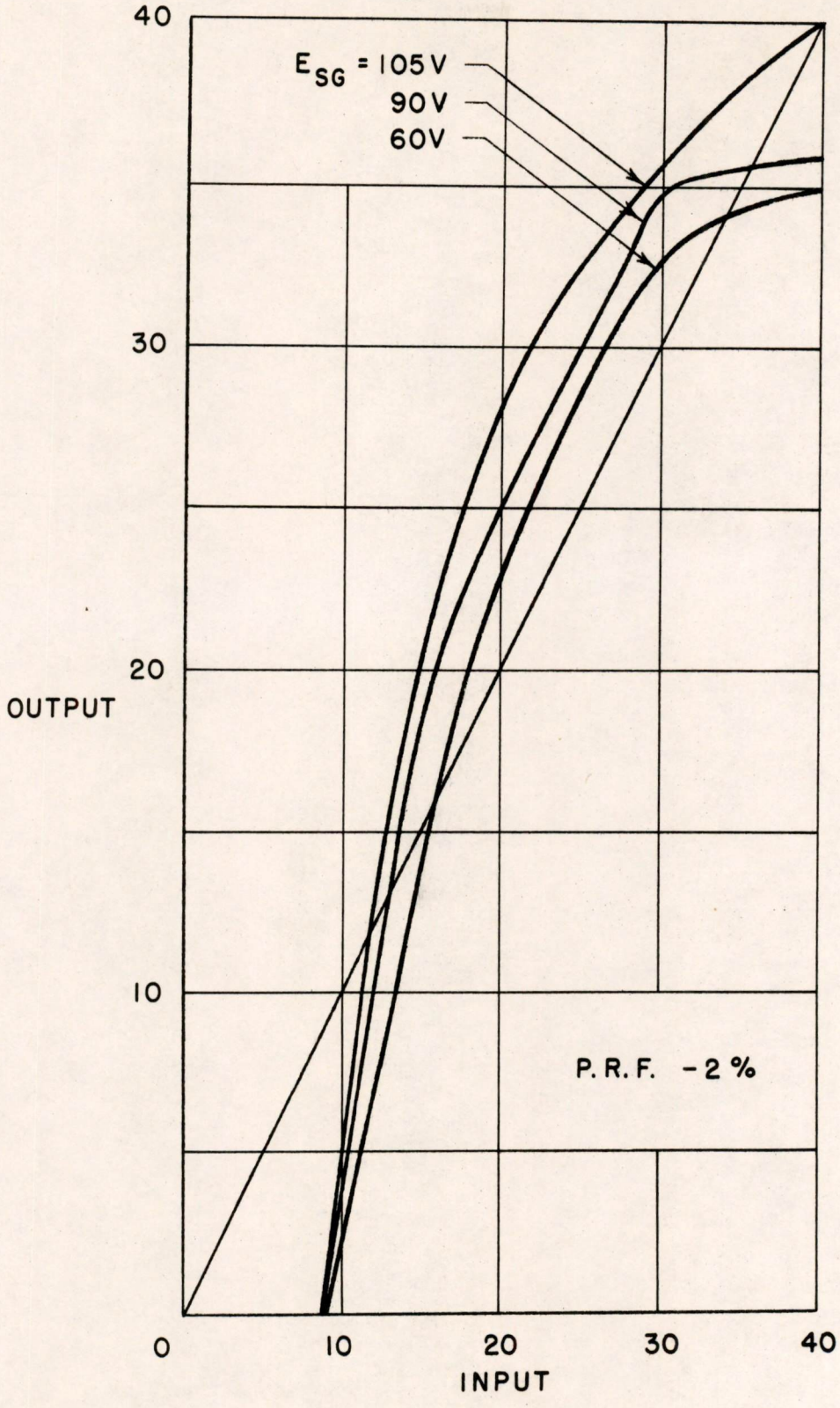



FIG. 4

TRANSFER PLOT FOR TETRODE-CONNECTED 0.5 μSEC DELAY CIRCUIT

A-57795

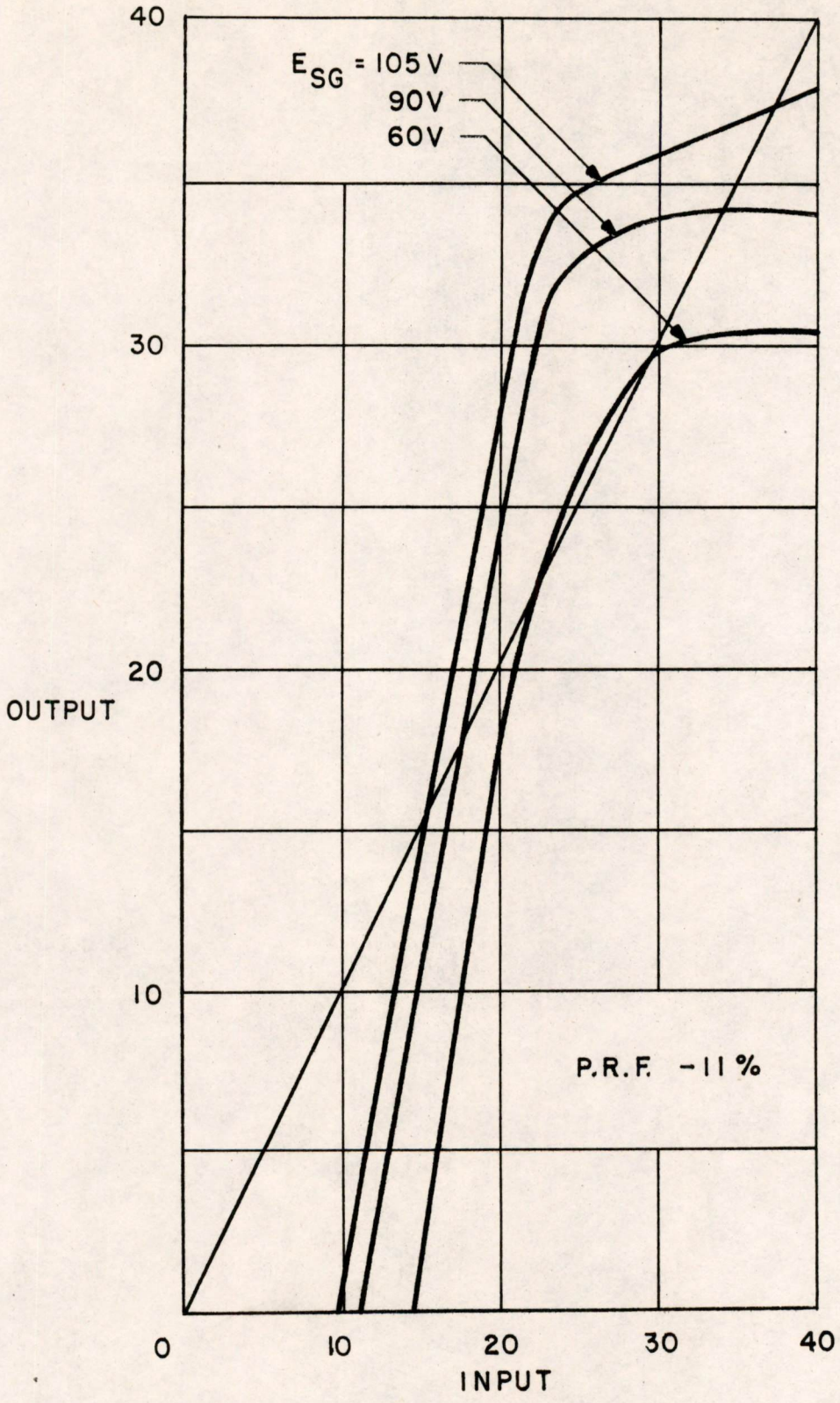



FIG. 5

TRANSFER PLOT FOR GATE-CONNECTED 1.5 μSEC DELAY CIRCUIT

A-57796

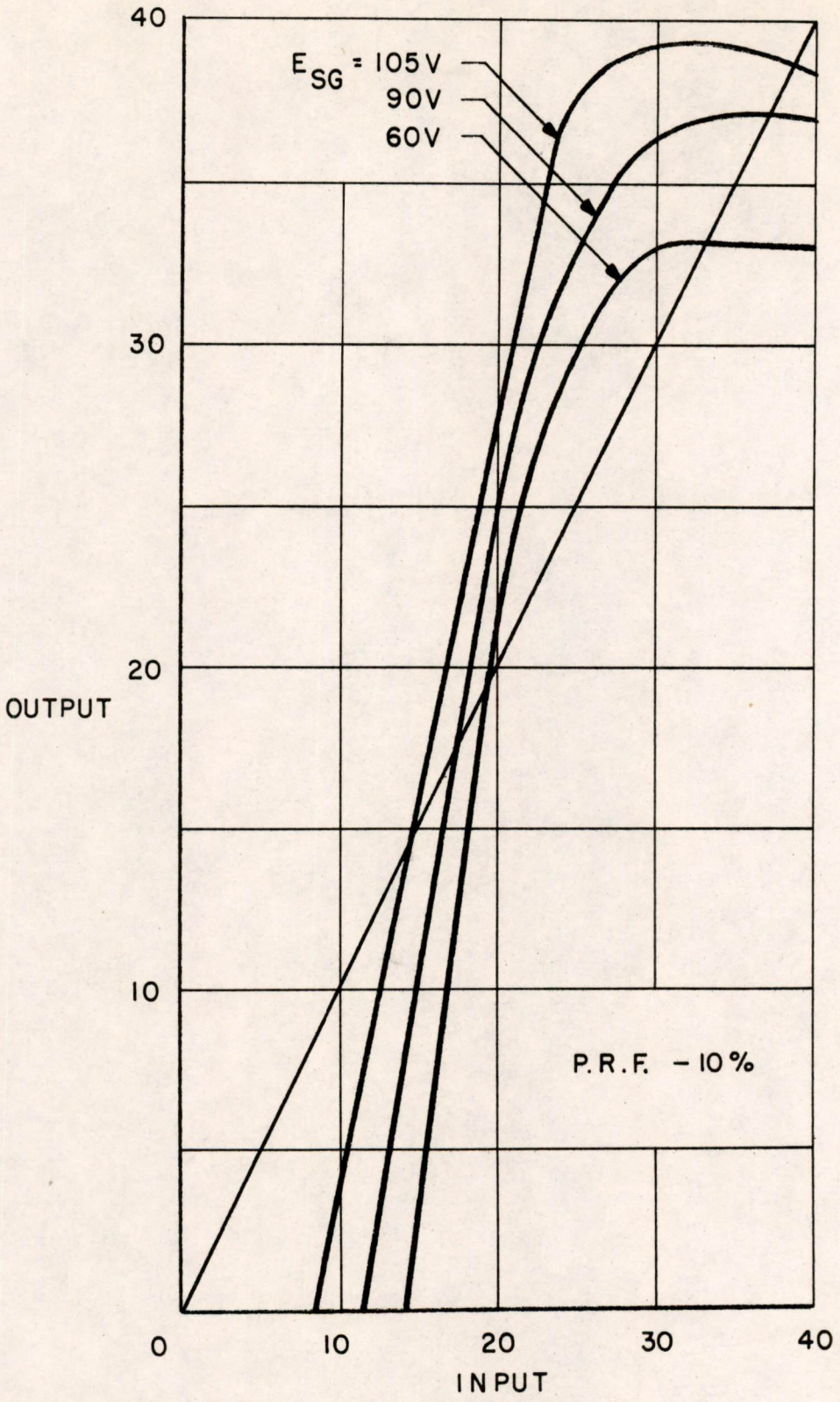



FIG. 6

TRANSFER PLOT FOR GATE-CONNECTED
1.0 μSEC DELAY CIRCUIT

A-57797

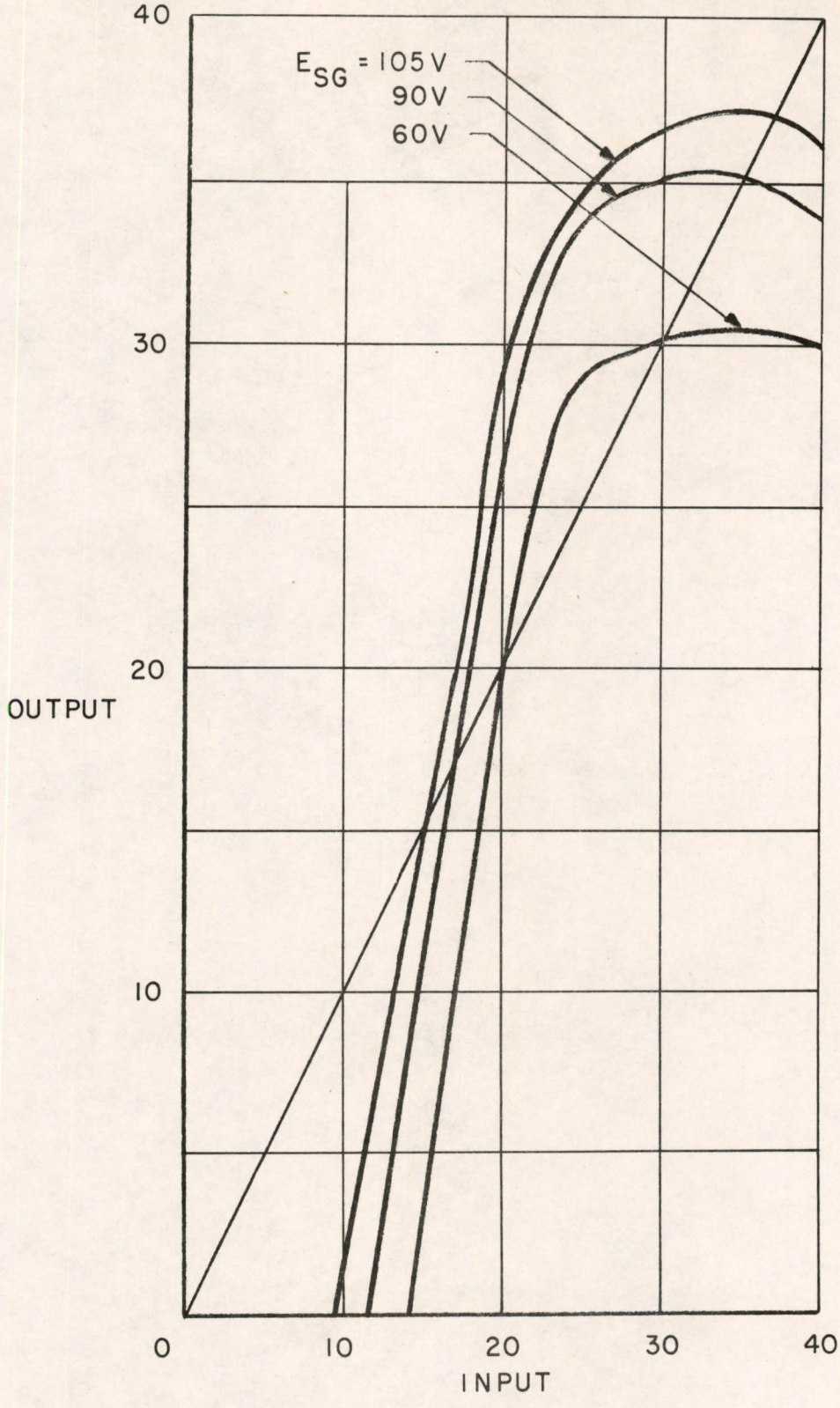



FIG. 7

TRANSFER PLOT FOR GATE-CONNECTED
0.5 μSEC DELAY CIRCUIT

A-57798

1/2 microsecond tetrode connected

Width Transfer Data

| Input | Screen | Output Width |
|---|---|---|
| 20 v.<br>0.1 μsec | | |
| | 90 v. | 0.09- |
| | 60 v. | 0.08+ |
| | 105 v. | 0.09 |
| 40 v.<br>0.1 μsec | | |
| | 90 v. | 0.095 |
| | 60 v. | 0.095- |
| | 105 v. | 0.095 |
| 20 v.<br>0.08 μsec | | |
| | 90 v. | 0.08+ |
| | 60 v. | 0.08 |
| | 105 v. | 0.085 |
| 40 v.<br>0.12 μsec | | |
| | 90 v. | 0.1 |
| | 60 v. | 0.1- |
| | 105 v. | 0.1+ |

Fig. 8

Jan. 25, 1954
J. S. Gillette

A-57799-1
MN

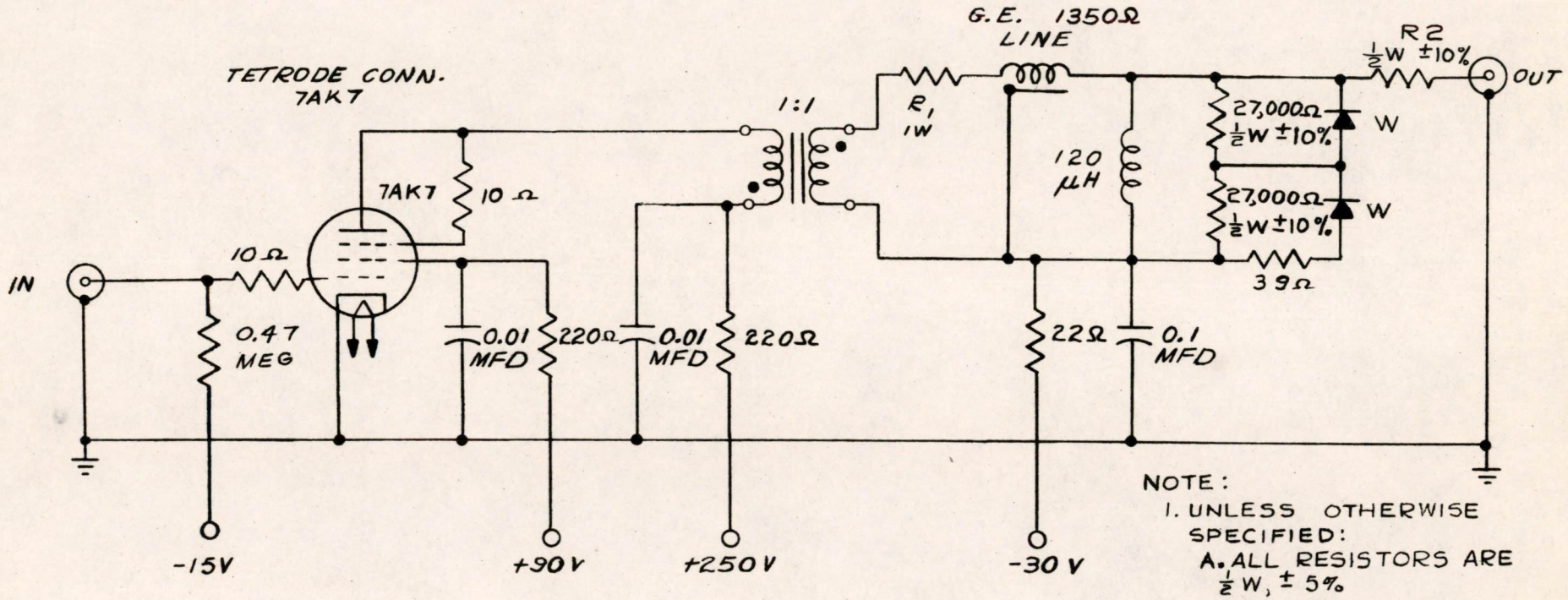



FIG. 9

CIRCUIT SCHEMATIC,
DELAY SCHEMATIC (TETRODE CONN.)

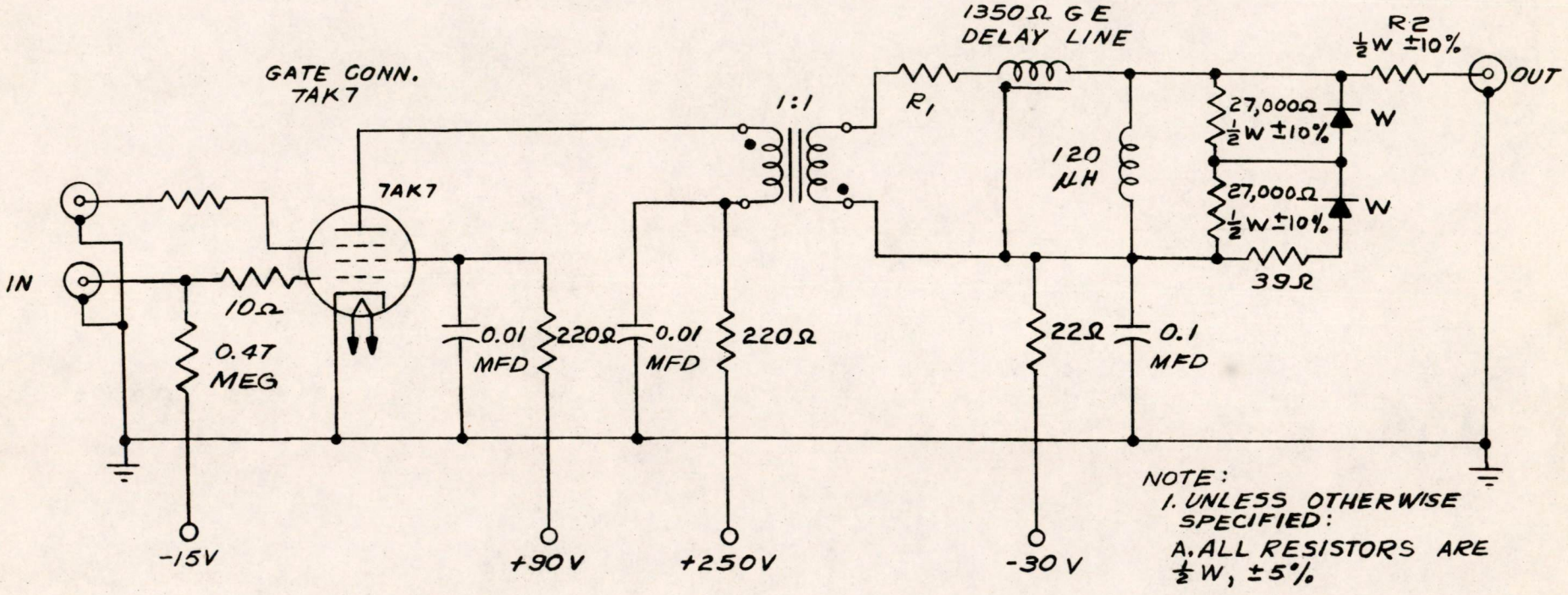
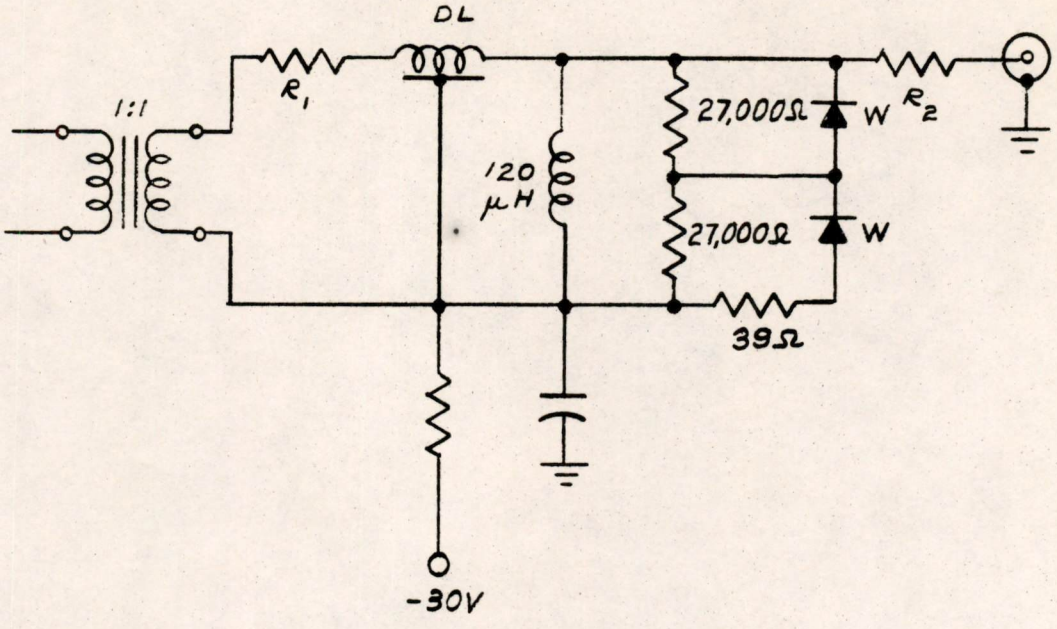



FIG. 10

CIRCUIT SCHEMATIC,

DELAY CIRCUIT - GATE CONNECTED




| DRIVER | DELAY | $R_1$ | $R_2$ |
|---|---|---|---|
| GATE | 0.5 | 470Ω | 0 |
| GATE | 1.0 | 0 | 0 |
| GATE | 1.5 | 0 | 0 |
| PULSE AMP | 0.5 | 820 Ω | 270 Ω |
| PULSE AMP | 1.0 | 560 Ω | 270 Ω |
| PULSE AMP | 1.5 | 270 Ω | 270 Ω |
| PULSE AMP | 2.0 | 0 | 0 |

FIG. 11

DELAY CIRCUIT — RESISTOR VALUES

A-57801

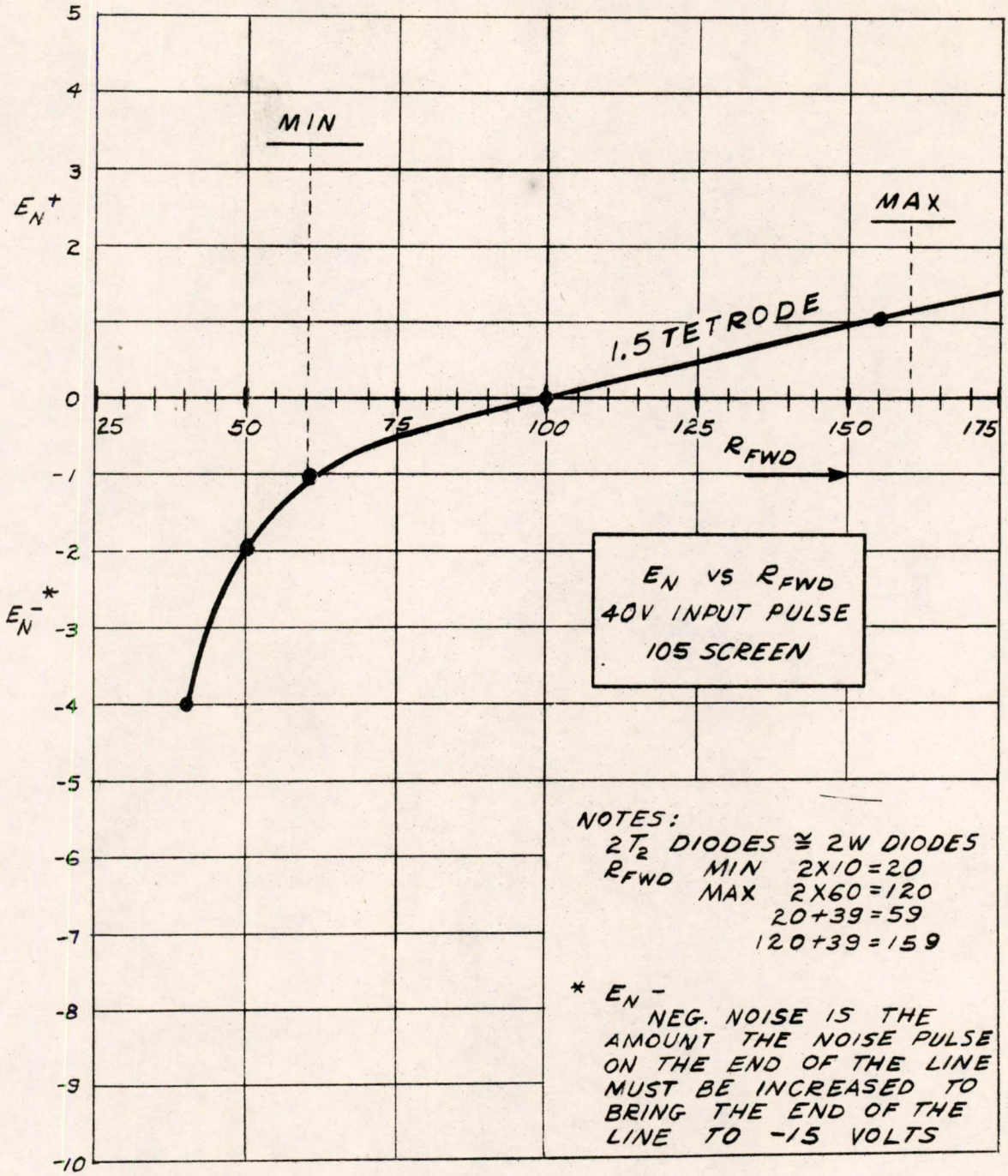



FIG. 12

DELAY LINE CIRCUIT NOISE OUT vs $R_{FWD}$

A-57802

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: Z-2177 Development Meeting on March 1 and 2, 1954

To: N. H. Taylor and Those Listed

From: S. Twicken

Date: March 22, 1954

Abstract: After production of several lots of different characteristics, Lot K has been decided upon as the one desired. The specification was reviewed and corrected and most sources of disagreement resolved. Many limits remain open; larger quantities of tubes are needed to determine them.

## 1.0 Introduction

A trip was made on March 1 and 2, 1954, to the General Electric Company at Owensboro, Kentucky, primarily to decide on design objectives in regard to tube characteristics and secondarily to review the specification and clarify several problems. The following people attended the meeting:

| MIT | IBM | GE |
|---|---|---|
| T. F. Clough | E. J. Breiding | C. E. Albrecht |
| H. B. Frost | F. A. Ordemann | F. M. Carter |
| S. Twicken | G. O. Mc Cabe | C. D. Cillie |
| | | C. W. Hamaker |
| | | C. Hopper, Jr. |
| | | W. T. Millis |
| | | W. U. Shipley |
| | | J. Somerville |

## 2.0 Format of Specification

The format of the specification conforms generally to MIL specs. The question of complete conformity was brought up, since there has been some misunderstanding as to whether the Z-2177 is a military tube in the sense that the military may want it for other applications. This matter will be clarified by a letter from Ordemann to GE to the effect that the tube is not a military tube (in the sense above) and that the specifications need not necessarily conform to military specifications.

## 3.0 Concurrence on Design Objectives

As a result of the meeting of January 11 and 12, 1954, GE has produced a third lot, Lot O, with higher current and lower $\mu$ than previous lots (at 100V. $E_b$, $I_b$/200 $\mu$aIc approximately 20ma and $\mu$ at the Class A point about 36). A comparison of the three lots in actual circuits by the Basic Circuits Groups at MIT and IBM showed Lot K to be preferred because of more symmetrical margins, current within the present maximum rating, and higher $\mu$ than Lot O. Lot L proved to be unsatisfactory in the low speed flip-flop because of its low plate current. Accordingly, mutual agreement was reached that the design objectives for the Z-2177 are to be the characteristics of Lot K whose salient points (nominal values) are plate current (at 100V. plate voltage and 200$\mu$a grid current) of approximately 17ma; 150 $\mu$a cutoff at 150V plate voltage of approximately -4.5V; and $\mu$ of about 44.

## 4.0 Desired Characteristic Curves

A request was made that GE provide the following characteristic curves in addition to normal triode curves:

1) On the $i_b$ vs. $e_b$ family, a curve at constant $i_c$ of 200 $\mu$a and 1ma, and constant $e_c$ of + 1V.
2) $i_c$ vs. $e_c$ for several values of $e_b$: 50V, 100V, 150 V.
3) $i_b$ vs. $e_b$ (for pulsed applications) with $i_b$ to about 150ma and $e_c$ to about +6V. These specific values will depend on results of pulse tests now underway.

## 5.0 Review of Z-2177 Specification

### 5.1 Maximum Plate Voltage

At present the maximum d-c plate voltage is given as 200V and the maximum peak voltage as 500V. The desire on the part of some circuit designers to use higher d-c voltages has resulted in questioning of the basis of these ratings. In addition to this, MIL E-IB 3.5.1.1 allows the use of twice the rated d-c for a supply voltage. This double rating comes from the Class A amplifier use. The tube is controlled at 180V on life test. Frost disapproves of increasing the 200V d-c value because of the increased probability of gas arcs. Millis disapproves of exceeding 400V peak (twice the rated d-c value). In view of the 180V control point, the consensus was that the 200V maximum d-c rating should stand. Ordemann will look into the circuit applications, especially the relay driver, to determine which circuits will exceed a 400V maximum peak rating. A decision on the maximum peak

5.1 Maximum Plate Voltage (continued)

plate voltage will be deferred until such time as factual life data can be obtained at higher plate voltages, and the circuit requirements are known.

5.2 Carton Drop

Delete AQL and Inspection Level since the MIL reference states the percent of allowable defectives. Reference to the notes will be changed from Note #5 to Note #7.

5.3 Glass Strain

Delete AQL and Inspection Level since the MIL reference states sample size and percent defectives.

5.4 Mechanical Inspection

5.4.1 Appearance of Pins

In Section 2.4.2.4E of spec add "Discoloration shall not be a cause for rejection."

5.4.2 Conducting Particles

In Section 2.4.2.5 of the spec, presence of conducting particles in the bulb is given as a cause for rejection. Since there is no known means of determining the conductivity of particles, this section of the spec is open to question. Based on the fact that GE has shipped large numbers of 5844's to IBM with this clause in the spec without any difficulty, the decision was made to leave it in the Z-2177 spec. It should be noted that this only defers action on the problem until such time as a lot rejection is attempted on the basis of conducting particles in the bulb.

5.4.3 Getter Flash

In Section 2.4.2.7E, getter flash extending below the top supporting mica is given as a basis for rejection. Some instances have been observed by GE where light streamers of getter have extended to or below the top supporting mica between the snubbers of the getter flash mica. This could be a cause for rejection without being a source of difficulty. In view of the presence of a getter flash mica and the 1,000 megohm electrode-insulation resistance minimum, it was decided to delete Section 2.4.2.7E from the spec.

5.4.4 Inspection Level for Mechanical Inspection

The inspection level will be determined after consultation with John Brock of IBM, one of the authors of the inspection format. An ambiguity in the introductory paragraph will be resolved.

5.5 Acceptance Tests

5.5.1 Title

Delete reference to Note #19 in title of Section 2.5.1.

5.5.2 Intermittent Short

The characteristics of the shorts tester will be removed from "conditions" and incorporated into Note #7. The AQL will remain open. GE reported that the 5,000 tubes of Lot K met a 0.4% AQL for shorts. If they have been tested on the high-speed short tester, this is exceptionally good.

5.5.3 Heater-Cathode Leakage

Delete URLM.

5.5.4 Plate Current at 200 μa Grid Current

Add LRLM and URLM.

5.5.5 Cutoff Voltage

The maximum value was decreased from -8.0V to -7.5V.

5.5.6 Contact Potential

Delete minimum and bogie. Add 2.5% AQL.

5.5.7 Pulse Emission

Add provision for an AQL.

5.5.8 $\mu$, $G_m$, & $r_p$

Delete the specification for plate resistance. The spec for $\mu$ will have provision for a minimum, LRLM, bogie, URLM, and maximum with an AQL of 6.5%. The spec for $G_m$ will have provision for a minimum, LRLM, bogie, URLM, and maximum with an AQL of 2.5%. The MIT suggestion that $\mu$ and $G_m$ be measured at fixed current rather than fixed voltage remians open. Distribution curves of the 5965 taken both ways show a narrower $G_m$ distribution at fixed current, which is

5.5.8 $\mu$, $G_m$, & $r_p$ (continued)

to be expected, and a wider $\mu$ distribution at fixed current. Pending an investigation of what each of the two tests means in terms of product control, the fixed voltage test (180V, -2V) will be continued.

5.5.9 Plate Current (3) (Cathode Activity Test)

Heater voltage will be dropped from 6.3V to 5.7V rather than 5.5V in order that GE will not find it necessary to increase cathode temperature to meet the $\Delta I_b$ spec. In addition, the Class A test point (180V, -2V) will be used rather than the fixed grid current point and a change in $G_m$ will be measured rather than a change in plate current. This involves an entire revision of the test. Breiding will check it with John Geisler.

5.5.10 Noise and Microphonics

GE questions the 2.5% AQL as being too tight for a tube not designed to be low in microphonics. Test conditions and limits also remain open.

5.5.11 Capacitances

Delete all LRLM's and URLM's.

5.6 Life Tests

5.6.1 Stability

Change Note #13 to read "During the 100-hour period, $OI_b$ must not differ from its initial value by more than 5% of bogie." Add Note #19 to conditions; this note to state that this test is continuous.

5.6.2 Zero Bias Life Test End Points

Delete bogie for $OI_b$ and bogie and minimum for $-I_c$.

5.6.3 Cutoff Life Test

Delete minimum spec for interface impedance.

5.6.4 Regular Life Test (Class A)

Change end point from plate current (2) to $G_m$.

5.6.5 Grid Emission Life Test

GE maintains internally a 63-hour grid emission life test at 7.5V. Therefore, a separate life test need not appear on the

5.6.5 Grid Emission Life Test (continued)

spec, but end points on regular 500-hour life test will remain.

5.6.6 10,000-Hour Life Tests

Zero Bias Life Test: Add minimum for $OI_b$. Delete minimum for $-I_c$.

Cutoff Life Test: Delete minimum for interface impedance and change pulse emission limit from maximum to minimum.

Regular Life Test: Change plate current (2) to $G_m$.

## 6.0 Review of Life Tests (GE)

### 6.1 Pulse Emission Life Test

No change after 500 hours on any of the three tests being run at 100, 150, and 200ma cathode current.

### 6.2 Stability

Of four groups of 50 tubes each considerable difficulty was experienced with one group ($\Delta I_b$ greater than 5%).

### 6.3 Zero-Bias Life (Positive Grid Current)

At 1,000 hours the positive-grid plate current average has dropped from 16.6ma average to 14.0. The contact potential maximum increased 0.16V at 500 hours and decreased 0.5V at 1,000 hours. No other changes of note.

### 6.4 Regular Life (Class A)

At 750 hours the positive-grid plate current decreased from 17.1ma average to 15.2ma average with a narrower range between minimum and maximum. At 500 hours there was no interface or grid emission.

### 6.5 Cutoff Life

No change at 700 hours.

### 6.6 Special High Dissipation Life Test

GE has been running a life test under Class A conditions with dissipation of 2.5 watts per plate. At 4,000 hours there is no major change in any of the characteristics. Only one tube shows interface and this of 5 and 10 ohms. There is no grid emission and the lowest insulation resistance is 200 megohms.

## 7.0 Inoperative Control

GE has no objection to including inoperative control on stabilization. The current procedure for 5-star tubes is a test for inoperatives after 46 hours of stabilization. The lot must meet 2% limit or is restabilized for 46 more hours at which time it must meet a 1.5% limit. If this is exceeded, a third restabilizing is permitted after which a 1.0% limit must be met. If the 1.0% limit for inoperatives is exceeded after the third period, the lot is scrapped. An identical procedure would be followed for the Z-2177. However, GE feels that the 2.0, 1.5, and 1.0% limits may be too tight, since the high-speed shorts tester will be used. They will accumulate data on future lots to determine what the limits shall be. It is understood, but nevertheless included for the record that if a lot passes the first test at 46 hours, GE is free to process the tubes for a longer period in order to meet the stability life test requirements of a maximum change in current of 5%.

## 8.0 Life-Test Sample Size

A fixed sample size of 20 tubes per lot (one week's production) will be taken with a fixed number of allowable defects per characteristic depending upon the survival rate desired. In the event of failure to pass, there is provision for a second sample of 40 tubes.

## 9.0 Development Status

Now that tubes of various characteristics have been made and evaluated and the characteristics of Lot K decided upon, GE will make at least 5 lots of about 200 tubes each to these characteristics to determine reproducibility and product spread. Two thousand tubes will be made after that, 1,000 for IBM on the contract and 1,000 for MIT on a separate outstanding order. It should be noted that the 5,000 tubes produced late last year were made to the Lot K characteristics and should yield considerable information although the mechanical design was not that of the final tube. Breiding of IBM will make a trip to Owensboro about the end of March to discuss progress on the sample lots, and a general meeting has been set up for April 26 to fill in as many of the undetermined limits as possible.

Signed S. Twicken
S. Twicken

Approved H B Frost
H. B. Frost

ST:EJM

## Distribution List

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R. S. Fallows
H. B. Frost
P. Youtz
A. Zacharias

IBM

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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: CORE MEMORY USING EXTERNAL BIT SELECTION*

To: N. H. Taylor

From: J. Raffel

Date: March 18, 1954

Abstract: A memory system in which the memory function (remanence) and the selection function (nonlinearity) are performed in separate cores may have the following advantages over the present (coincident-current) system:

1) Much broader tolerances on core acceptability

2) Reduced noise out of the memory array

3) Larger signals out of memory

4) Shorter memory cycle time

Some of the costs may be:

1) Two or three times as many cores required

2) More complex construction problems

## 1. Statement of the Problem

Consider the problem of using switch cores to perform the selection function for a magnetic core memory completely external to the memory cores themselves.

## 2. The Functions This Selection System Must Perform

It must be capable of subjecting any memory core in a selected register to either of two cycles:

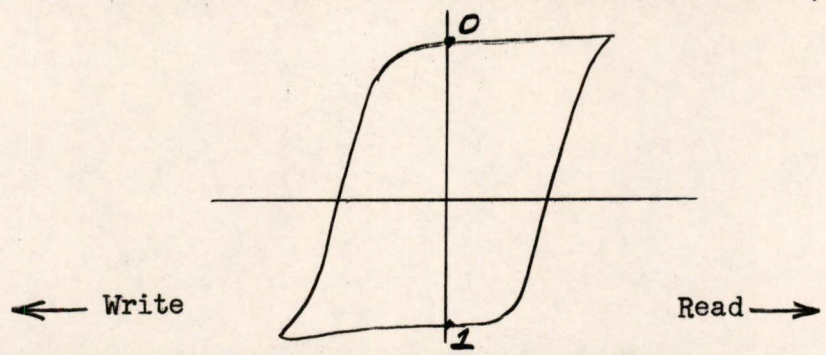
Read, Write ZERO ($R\text{-}W_0$)

Read, Write ONE ($R\text{-}W_1$)

without exciting any other cores in the array.

* This note is a section of a thesis to be finished shortly which will deal with the general problem of register selection.

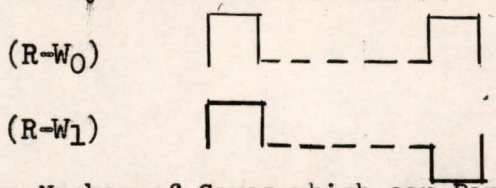
(A ZERO and a ONE are represented in the usual manner as shown on the hysteresis loop below along with Read and Write polarities.)




3. The Necessary and Sufficient Conditions Imposed on the Excitations which the Switch Cores are to Provide to the Memory Cores.

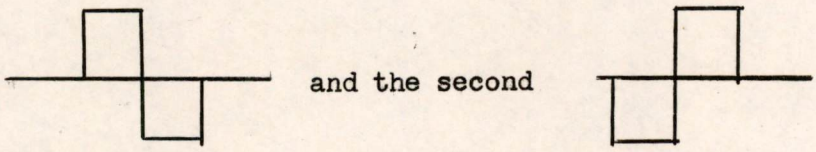
For cycle R-W0 it is only necessary that we have a sequence which has a first pulse plus and a last pulse plus.

For cycle R-W1 we require a first pulse plus and a last pulse minus. These two cycles are shown below.

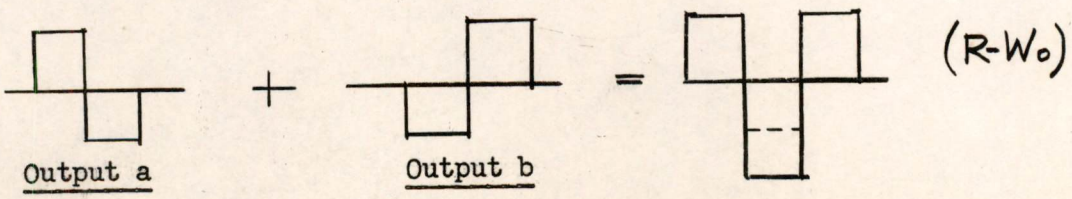



4. The Minimum Number of Cores which can Perform the Switching Function Outlined Above.

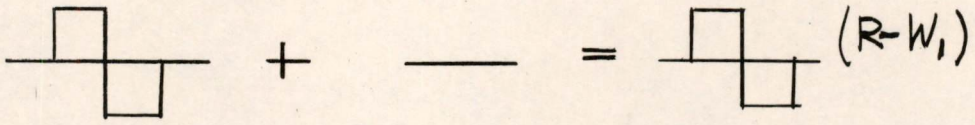
We recall that a switch core must be reset to its original flux state before the start of a new cycle; this is a natural for R-W1 cycle. However, the R-W0 cycle cannot come from a single core; it could, though, come from the properly combined outputs of two switch cores, the first of which produced:




We then have all we need to obtain the two cycles desired as shown below.




(If we overlap for minimum time)




Output a

It is also evident from above that the minimum number of switch cores needed is one core per register to supply Output a, (all the cores in the register receive it) and one core per bit to supply Output b, (each core in the register may or may not receive this depending on whether a ONE or a ZERO is being written).

## 5. Operating Characteristics

By completely separating the switching and memory functions the cores are no longer restricted to the critical requirements on driving current and hysteresis-loop squareness imposed by coincident-current operation. The hysteresis loop required for a coincident-current memory is shown in Fig. 1. The loops required of the switch core and memory cores in the proposed system are shown in Figs. 2 and 3 respectively. The main requirement of the switch core is that it be saturable, of the memory core that it have two distinct remanent-flux states.

In addition to reducing the core uniformity requirements this system makes possible increased signal outputs, shorter cycle times and reduced noise.

## 6. Physical Realization

The main problem in constructing a memory of this sort is the increased wiring complexity which results from driving each memory core individually rather than from common lines. This requires small coupling loops linking pairs of cores and these may be difficult to fabricate unless done perhaps by machine. One possible configuration is shown in Fig. 4. On one side of a phenolic board are wired switch cores having X, Y, and Z windings as in conventional memory digit plane. Each core is also connected to a corresponding memory core on the other side of the board by a small loop or staple. All the memory cores on a single digit plane have a common sense winding. This takes care of the memory core and the switch core which supplies ouput b described above. All we require now is a single core per register to supply output a. The output of this switch would then go down a line linking all the memory cores in a register successively. From a construction point of view it might be simpler to use one core per bit for output a. The construction of the two switch planes now required per digit would be identical and might lead to simpler winding although more cores are used.

## 7. Conclusion

This system offers many advantages over the conventional coincident-current method. Its main drawback is construction complexity. Experimental work to obtain a quantitative evaluation in terms of cycle time, core material requirements, etc., would be desirable, since it may find use in some special memory application and if construction difficulties were overcome, as central memory unit for a computer.

Signed: J. Raffel
J. Raffel

Approved:
W. N. Papian

JR/rb

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Group 63 Staff
N. L. Daggett

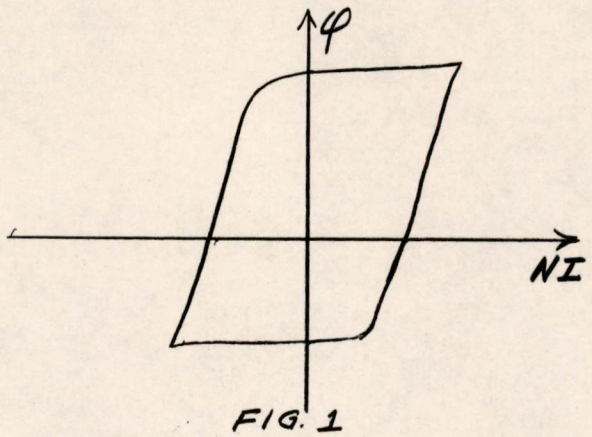



FIG. 1

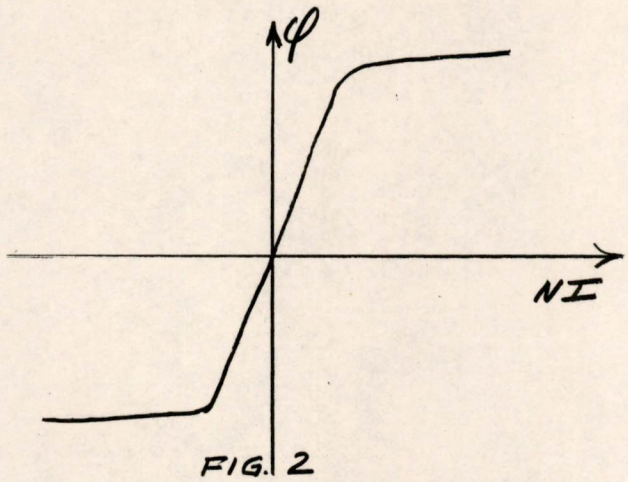



FIG. 2

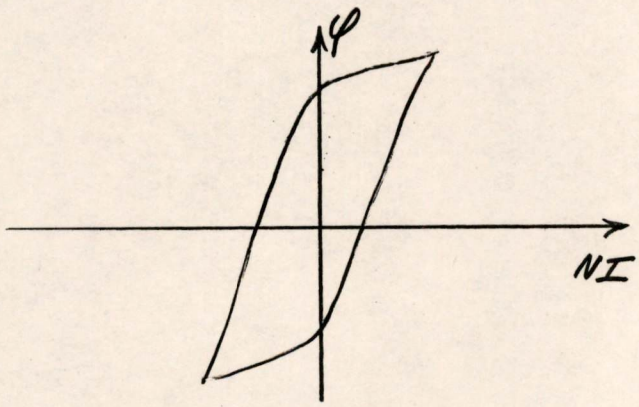
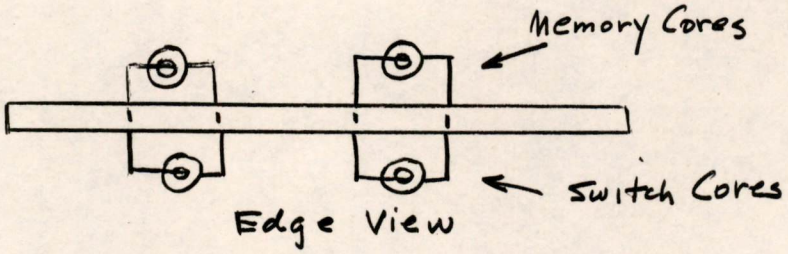
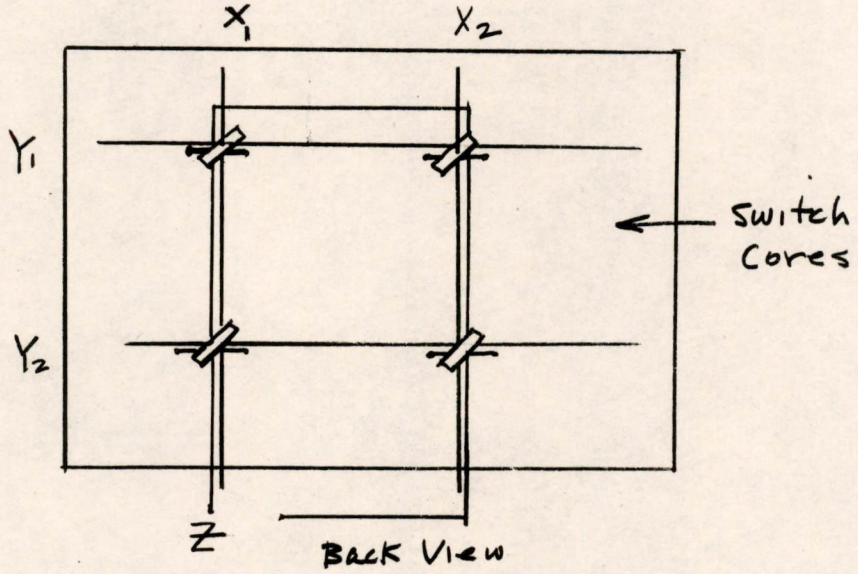



FIG. 3


Memory Cores
Switch Cores
Edge View


X1
X2
Y1
Y2
Switch Cores
Z
Back View

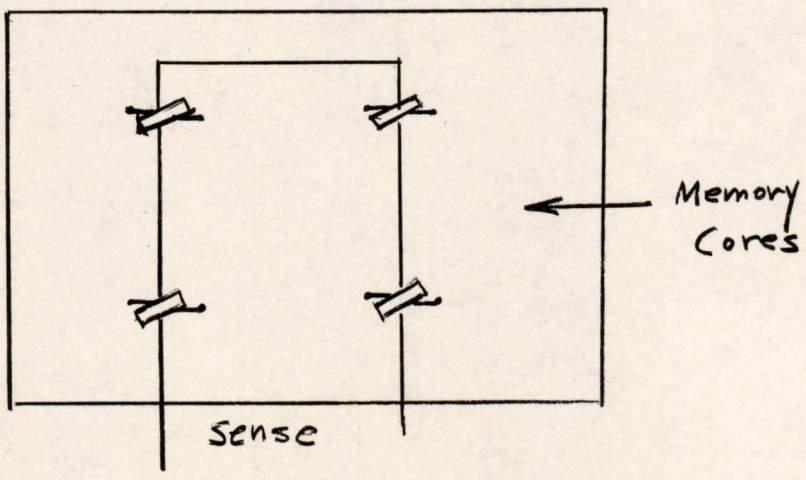

Memory Cores
Sense

FIG. 4

H. Anderson

4.2.0



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: AIRPLANE TRANSPORTATION BETWEEN BEDFORD AND POUGHKEEPSIE

To: All Division 6 Group Leaders, Section Leaders & Group 62 Staff

From: A. P. Kromer

Date: September 24, 1954

Approved: R. R. Everett

Abstract: Close coordination of reservations for travel on the IBM airplane and chartered planes is required to avoid confusion and secure maximum use from the service. No staff member should independently arrange for charter of an airplane.

Use of the airplane for transportation between Bedford and Poughkeepsie has proved a considerable convenience to members of the laboratory. In order to continue to receive full benefit from this service, all Lincoln personnel are asked to conform to the procedures indicated below. Such action is intended to avoid misunderstandings or confusion regarding passenger lists for specific flights and to avoid delaying departure of flights, while at the same time providing service for the maximum number of people. Please refer to 6M-2747 and 6M-2747, Supplement 1, for additional information regarding this subject.

## I. TRAVEL BY IBM AIRPLANE

### A. Procedure at Lincoln Laboratory

Requests for reservations on the Tuesday and Thursday flights should be made by telephoning ext. 128 (Mrs. Dorothy Roberts) providing the desired information to her. This includes name, date, time of flight, person to be visited, business to be discussed, personal weight, home telephone number and weight of any baggage in excess of a briefcase. Such requests should be made as early as possible and in any event not later than noon on the date preceding the flight. However, all last minute changes should be made known to Mrs. Roberts. (Note: Last minute changes in plans after close of the laboratory at 5:30 on the date preceding the flight should be telephoned to the Lincoln Laboratory guard desk, Le 9-3370, ext. 397, with a request that this information be given to the pilot of the IBM plane upon arrival by means of a telephone call to the manager's office at the airport, Le 9-2550, or by a message via the Lincoln courier who meets the plane to pick up the mail pouch.)



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

B. Procedure at Poughkeepsie

While requests for return flights from Poughkeepsie should also be given to Mrs. Roberts as indicated above, some confusion has existed on these flights because of changes in plans which occur after personnel have arrived at Poughkeepsie. Therefore, it is asked that all personnel reconfirm their return flight reservations with Miss J. Badami at ext. 205H prior to noon on the day of the return flight. Such reconfirmation should also include information concerning the IBM location from which transportation is desired to the Duchess County Airport. Any change in plans regarding return flights after arrival in Poughkeepsie should also be given to Miss Badami as early as possible. If two Lincoln Laboratory members agree to swap reservations with each other, this information should also be telephoned to Miss Badami so that the proper names will appear on the passenger list given to the pilot. This has been the cause of some confusion and has delayed some flights in the past. (Note: Any last minute or emergency changes in information that occur concerning flights originating in Poughkeepsie can be telephoned to the CAA Control Tower, Poughkeepsie 2707 or 1505, with a request that this information be given to the pilot of the IBM plane.)

## II. TRAVEL BY CHARTER PLANE

The IBM plane may be supplemented by other planes on a charter basis if insufficient space is available on the IBM plane and/or on days when it does not operate to Bedford. Charter of such planes is handled by the Lincoln Travel Office (Jean Friberg, ext. 375) under certain conditions approved by DDL. No Staff member should charter an airplane. If, when at Poughkeepsie, space for a return flight on the IBM plane unexpectedly is not available and charter plane service to Bedford is desired, a request for such service must be given to the Travel Office by phone to have them secure approval of a Group Leader or the DDL Office. After such approval the Travel Office will arrange for charter of an airplane. Any arrangements other than the type outlined above must be avoided as it will cause considerable difficulty over payment of bills resulting from the charter of airplanes by any agency other than the Lincoln Travel Office.

## III. GENERAL INFORMATION

Ground transportation at Poughkeepsie is normally provided by IBM. If it is necessary to use taxi service, this should be paid for by the Staff member and recovered by means of a regular travel voucher. Any unusual costs for transportation from home to the Bedford Airport will likewise be considered as a recoverable item of expense on a travel voucher.

Since a round trip in a single day is not regarded as travel in the usual sense, vouchers should not be submitted except for expenses mentioned above.

Any IBM personnel visiting here who desires information concerning departure time of flights, or other data regarding return flights from Boston to Poughkeepsie should be advised to contact Mrs. Roberts, ext. 128, who is kept informed of the status of flights to Poughkeepsie.

Election of the means of travel between Lexington and Poughkeepsie is at the option of the individual. Availability of the airplane should not be construed as preventing travel by auto or train for those who desire it.

Signed: A. P. Kromer

APK/mo

cc: H. W. Fitzpatrick
Jean Friberg

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRAVEL IN IBM AIRPLANE

To: All Division 6 Group Leaders, Section Leaders & Group 62 Staff

From: A. P. Kromer

Date: July 9, 1954

All persons wishing transportation to Poughkeepsie by plane should make requests to Miss Betty Osenton, Ext. 128 or 129 (Building B-121) as early as possible so that a passenger list for the IBM plane can be prepared and forwarded to them by noon on the day preceding the flight and so arrangements for charter of other planes can be made if required.

Since IBM requires complete information at noon on the Monday and Wednesday for flights on the following days so that the pilot and ground transportation can be properly advised, last minute changes in plans and requests to travel on the IBM plane represent an imposition on a number of people and should be avoided.

Everyones cooperation in this matter will make the plane service of most use to all.

The present schedule for flights is as follows:

Tuesday and Thursdays

| Flight # | Departure | Arrival |
|---|---|---|
| 1 | 7:00 AM Poughkeepsie | 8:10 AM Bedford |
| 2 | 8:15 AM Bedford | 9:30 AM Poughkeepsie |
| 3 | 4:45 PM Poughkeepsie | 5:50 PM Bedford |
| 4 | 6:00 PM Bedford | 7:15 PM Poughkeepsie |

Departure at Poughkeepsie is from Duchess County Airport.

Departure at Bedford is from Hanscom Field Civilian Terminal (not Air Force Base Ops.).

Note: On certain occasions special arrangements for a flight by IBM on Wednesdays can be made - several days advance notice is required for such arrangements however.

Please refer to the original Memorandum M-2747 dated March 26, 1954, for additional information regarding number of people, insurance, baggage, etc. in connection with travel in the IBM plane.

Signed A. P. Kromer

Approved N. H. Taylor

APK:mo

Olsen Antenna



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SILVER MIGRATION DISCUSSIONS AT SQUIER SIGNAL LABORATORY AND BELL TELEPHONE LABORATORIES

To: N. H. Taylor

From: B. B. Paine and C. W. Watt

Date: March 29, 1954

Abstract: The following report summarizes all the information that Division 6 and IBM have been able to collect on silver migration. It was written by J. B. Little of IBM with some contribution by B. B. Paine of Division 6.

## REPORT ON SILVER MIGRATION

The words "Silver Migration" are occurring with increasing frequency lately, particularly in association with printed circuits. Project High, spurred on by reports from M.I.T., has been especially concerned as to whether long term deleterious effects might occur in circuits built up on boards with printed wiring.

At the request of John Coombs of Project High and through arrangements made by B. B. Paine of M.I.T., an attempt has been made to track down available information on silver migration by contacting groups at the Squier Signal Laboratory at Fort Monmouth, N. J. and the Bell Telephone Laboratories in New York City, on January 27 and 28, 1954.

At Squier Signal Laboratory discussions with Messrs. E. M. Beekman, H. M. Gade, R. A. Gerhold, S. G. Bassler indicated that silver migration, as a problem, was known to exist; but that no quantitative and very little qualitative data were available. It was generally agreed that some difficulties with electronic equipment could be attributed to silver migration as long ago as World War II. Failures in equipment were commonly associated with surface leakage effects on moulded phenolic parts with silver inserts. Subsequent tests have shown that this surface leakage may develop on a wide variety of insulating materials when a d-c voltage is maintained between silver contacts on these materials, particularly in the presence of high humidity.

No specific information concerning voltages, spacings, base materials, humidity conditions, etc. was available, although some tests on copper-clad phenol-paper laminate are being initiated. Also, no sample parts or examples of failures due to silver migration were available or known to exist locally.

At the Bell Telephone Laboratories a conference was held with Messrs. G. H. Downes, G. T. Kohman, J. M. Wilson, and K. G. Compton of B.T.L., Messrs. B. B. Paine and A. L. Loeb of M.I.T. and J. B. Little of I.B.M. in attendance.

Mr. Downes produced a voluminous report which contained specimens of failures due to silver migration. These specimens were thin sheets of phenol laminate, similar to stock commonly used for printed wiring, which had been clamped between sets of silver plated brass contacts which form parts of "step-by-step" switches used in telephone central offices. There was considerable blackening and discoloration directly under the silver on the surface of the phenolic, and in most cases, a discoloration through the volume of the material in the region of the silver plated contacts, causing actual conductive paths through the insulator.

This discoloration, which apparently occurs when moisture and d-c potential coexist in the region of silver electrodes, is the first indication of a progressive deterioration of the surface and volume resistivity of the base material. Usually progressing from the anode to the cathode, the silver bearing discoloration migrates across or through the space between electrodes causing eventual breakdown. In the examples shown, the potential difference was 48 volts across approximately .015" thick material. With normal humidity variations, failures were occurring in four years. Equipment in high humidity areas tended to fail earlier than similar equipment in low humidity areas.

Silver migration is not limited to phenol plastics or laminates. The volume effects are more commonly found in cellulose filled materials. Mr. Kohman showed photographs of several dozen ceramic rods with silver-coated ends. These test rods, about an inch long, had been exposed to 97% relative humidity with several hundred volts between the metal ends. All the surfaces showed silver migration patterns developing. There were many types of ceramic bodies under test and the results were quite varied. Actual times were not given, but it was implied that noticeable effects could be observed in the matter of weeks at these high humidities.

As far as the particular problem of the "step-by-step" telephone equipment was concerned, it was solved by replacing the phenol laminate by an acetobutyrate material known as Tenite #2 and eliminating silver in the region where the contact touches the plastic. To sum up the available information, the following points appear to be important:

1. Silver migration has been observed and has caused equipment failure.

2. Under average temperature and humidity conditions failures have occurred in operating equipment in about three to four years.

3. The effect appears to be peculiar to silver; at least is more marked and progresses faster with silver than with other commonly used materials such as copper, tin, etc.

4. The effect is enhanced by high humidity, intimacy of contact between the silver and the insulator, and by increased potential.

5. The presence of chlorides, fluorides, amines, etc., seems to accelerate the silver migration effect.

6. The effect is most probably associated with electrolysis, but the details of the explanation on this basis are not clear. However, the fact that silver occurs commonly in the singly ionized state may be a significant factor in leading to an explanation of why silver is more deleterious than gold or copper.

On the basis of the above information it seems reasonable to insist upon the following: do not use silver or silver alloys in intimate contact with common insulating materials in the presence of d-c potentials if normal humidity variations exist and long operating life is required.

ADDENDUM

"Whisker growth" was discussed briefly at Bell Telephone Laboratories by Mr. Compton. This effect has been observed only on the surfaces of Cadmium, Tin, and Zinc when these metals are unalloyed. The term "whisker growth" is truly descriptive since spines or whiskers, from 1/2 to 4 microns thick and of surprising length, grow out of the surface of the metals. No applied potentials are necessary for this effect. The whiskers will grow through chromated and varnished finishes. Equipment troubles have been traced to circuit changes produced by these metallic spined bridging across normally insulating paths. This effect should not be confused with silver migration. It occurs in air, not in or along the surface of solid insulators.

These whiskers, curiously, are said to be examples of perfect structure in that their strength approaches theoretical limits and far exceeds measured values for the same metals in normal bulk form.

REFERENCES ON SILVER MIGRATION

1. "The Case of Reliability versus Defective Components et al" by R. M. C. Greenidge, Bell Telephone Laboratories, Inc., New York City. Presented at Electronics Symposium in

1. (continued)

Pasadena, California in Spring of 1953. Silver Migration, as such, is not discussed, but examples and photographs are given which show electrical breakdown due to conducting growths comprised of silver in one form or another.

2. "Phenolic Dielectric Breakdown in W W I" by B. B. Paine, Digital Computer Laboratory, M.I.T., Cambridge, Mass. Internal Memorandum M-1829. Dated February 6, 1953. The possibility of Silver Migration causing breakdown between turret lugs on phenolic panels in W.W.I. is discussed. Bell System experience with same effect in 1936 is related.

3. "Silver Migration in Electronic Equipment" by G. H. Downes, Bell Telephone Laboratories, Inc., New York City. Private Communication to Mr. C. W. Watt, M.I.T. Dated December 14, 1953. This is a re-write of a memorandum by Mr. Watt on the above subject. It is expected to be published soon and presents a brief, but concise picture of failures in Whirlwind I Computer at M.I.T. and Bell Telephone experience in switching equipment.

4. "Silver Migration in Electronic Equipment"
Internal Information Bulletin No. 212., Squier Signal Laboratory, Components and Materials Branch, Fort Monmouth, New Jersey. Dated December 23, 1953. This is essentially an elaboration of information covered by the other references.

5. "Silver Migration in Electronic Equipment" by B. B. Paine for the Lincoln Laboratory Standards Committee, M.I.T., Cambridge, Mass. Internal Memorandum LS-15. Dated November 17, 1953. A summary of equipment failures due to the migration of silver ions through insulation in the presence of d-c potential and moisture.

6. "Use of Silver in Etched-Wiring Cards" by A. L. Loeb and B. B. Paine, Division 6 - Lincoln Laboratory, M.I.T., Cambridge, Mass. Internal Memorandum M-2669. Dated February 3, 1954. Findings of a brief study of the conditions which contribute to the migration of silver in laminated plastic materials.

Signed by: J. B. Little

Issued at MIT by: B B Paine
(B. B. Paine)

Approved for MIT by: C W Watt
(C. W. Watt)

JBL/bbp/cww/mrs

cc: W. H. Ayer R. W. Hudson
J. D. Bassett A. P. Kromer
Lincoln Laboratory Standards Committee

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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: CORE DRIVERS - MODEL V AND MODEL VI
Applications, Limitations, and Modifications

To: David R. Brown

From: J. D. Childress

Date: April 1, 1954

Abstract: (This memorandum supersedes Engineering Note E-523.[1]) The Model V and Model VI Core Drivers are standard test units which generate rectangular wave current pulses of variable amplitude, rise time, and duration. Model V supplies pulses negative-going from ground; Model VI, positive-going from ground.

## 1.0 Specifications

### 1.1. Dimensions:

5-1/4 x 5 x 19 inches for rack mounting.

### 1.2. Circuits:

Monostable multivibrator (5965)
Inverter-amplifier (1/2 - 5687)
Clamper (1/2 - 6AL5)
Cathode Follower (1/2 - 5687)
Current Amplifier (4 - 6CD6's)

### 1.3. Input:

Standard 0.1 μsec pulses, -13 to -30 volts

### 1.4. Output:

Shape - rectangular
Rise time - less than 0.15 μsec, and 0.2 μsec to 1 μsec in two overlapping ranges
Duration - less than 1 μsec to greater than 40 μsecs[2]
Amplitude - variable from 0 to 1.2 amps
Output impedance - greater than 100 Ω for Model V and less than 10 Ω for Model VI

---

1. Boyd, Harold W., "Core Drivers - Model V and Model VI," MIT Digital Computer Laboratory Engineering Note E-523, February 10, 1953.

2. See Section 2.1.

1.5. Duty Factor:

Less than 40 percent or less than $\frac{40}{\text{output current in amps}}$ percent, whichever is smaller[3]

1.6. Power Requirements: (approximate during pulse)

| Voltage | Model V | Model VI |
|---|---|---|
| +150 volts | 0 | 0.07 to 2.0 amps |
| -150 volts | 0.03 to 2.0 amps | 0 |
| -300 volts | 0.04 amps | 0.04 amps |
| 6.3 volts, AD | 11.5 amps | 11.5 amps |

Use separate filament supplies, center tap floating, for each type driver.

## 2.0 Operation

The Core Drivers (schematics C-52170 - Model V and C-52643 - Model VI, Figures 1 and 2, respectively) are shown in block diagram in Figure 3. The drivers have five stages--monostable multivibrator, inverter-amplifier, clamper, cathode follower, and current amplifiers.

2.1. Monostable Multivibrator:

The monostable multivibrator is labeled "monostable" and "bistable" because of the two options in the use of the stage. In "monostable" operation, the duration of the negative gate output to the inverter amplifier is determined by the network of C-2 (C-3), R-2, and CR-3 and is variable by the Duration Coarse and Duration Fine controls from less than 1 μsec to greater than 40 μsecs; in "bistable" operation, the duration is fixed at greater than 40 μsecs. The duration of the gate from the multivibrator determines the duration of the output current pulse.

The multivibrator is set by a standard 0.1 μsec pulse, amplitude -13 to -30 volts, into J1-set and can be cleared in both "monostable" and "bistable" operation by a standard 0.1 μsec pulse, amplitude -13 to -30 volts, into J2-clear.

It is recommended that the Core Drivers be operated in the "monostable" mode whenever the duty factor is less than 40 percent. For use with a "clear" input, the Duration Coarse and Duration Fine controls are set for a pulse duration slightly greater than desired; then the multivibrator is "cleared" by a delayed pulse into J2-clear. The delay of the "clear" trigger is adjusted for exactly the pulse duration desired.

---

3. See Section 2.1. and 2.5.

The duty factor of the multivibrator is less than 75 percent in "bistable" operation, less than 40 percent in "monostable" operation.

2.2. Inverter-amplifier:

The negative gate from the multivibrator cuts off the normally conducting inverter-amplifier. The plate of the tube rises with a time constant depending on the plate to ground capacitance and the plate load resistance. The rise time of the plate of the inverter-amplifier determines the rise time of the output current pulse. With the Rise Time Coarse set on "short", the rise time of the output pulse is less than 0.15 μsec, but is not variable with this setting; with the Rise Time Coarse set on either "medium" or "long", the rise time can be varied with the Rise Time Fine control from less than 0.2 μsec to greater than 1 μsec in overlapping ranges.

Since the latest changes (6052 and 6118), the inverter-amplifier stages of the two drivers differ. The plate load resistor has been decreased and a small inductance added in this stage of the Model VI to decrease the rise time of the output pulse. Also, in the Model VI the voltage on the plate with the tube conducting has been lowered so that the output tubes are held cut off even when their cathodes are driven 70 volts negative.

2.3. Clamper:

The plate of the inverter-amplifier rises to be clamped to a level determined by the setting of the Amplitude control (R-20). This clamping controls the amplitude of the output current pulse; the amplitude is variable from 0 to greater than 1.2 amps, the upper limit depending on the quality of 6CD6's.

There is a 0.25 μsec condenser from the center arm of R-20 to ground (C-11) in Model V, C-14 in Model VI). This condenser lowers the effective impednace of the clamp voltage to give the output waveform in Figure 4a. Without the condenser, the waveform is shown in Figure 4b. The break in the rise (indicated by the arrow) is the point at which the diode begins to clamp; the further rise is caused by the clamp current affecting the clamp voltage.

The addition of the condenser to the center arm of R-20 has made the circuit pulse duration sensitive and prf sensitive. For long pulse durations, the clamp current causes the clamp voltage to rise, thereby increasing the output current--see Figure 4c. The time constant of the circuit is such that the current pulse changes less than 0.25 percent per microsecond duration. As the prf is increased, the average value of the clamp voltage increases; therefore the current pulse amplitude increases. For the burst of high prf pulses, the current pulses "grow" along the sequence--see Figure 4d.

2.4. Cathode Follower:

The cathode follower is used to match impedance between the inverter-amplifier and the current amplifier.

2.5. Current Amplifier:

Four 6CD6's connected in parallel form the current amplifier (pentode amplifier in the Model V and pentode cathode follower in the Model VI). The maximum amplitude of the output pulse is greater than 1.2 amps, even with marginal tubes.

The current output of the Core Drivers is limited by the screen dissipation of the 6CD6's. The maximum duty factor for four 6CD6's in the output stage is given:

$$\text{Duty factor} = \frac{40}{\text{output current in amps}} \text{ percent.}$$

A Screen Current Warning lamp gives a rough indication of the screen dissipation; for rated operation, this lamp should not glow. Note that the duty factor of the driver as a whole depends on the duty factors of both the multivibrator[4] and the current amplifier and is equal to the smaller of the two, see Figure 5.

The output impedance of the current amplifier is a function of the current pulse amplitude and of the external load impedance. For an external load impedance of less than 100Ω (including 50-Ω current measuring resistor) and output current less than 1.2 amps, the output impedance of the Model V is greater than 100Ω; of the Model VI, less than 10 Ω. Note that for smaller currents, the Model V becomes more like a current source; the Model VI, more like a voltage source.

3.0 Applications, Limitations, and Modifications

The Core Drivers are designed particularly for the application of ferrite memory core testing. The stringent specifications for this application are as follows:

Shape - rectangular with top "flat" within 0.5 percent, no overshoots
Rise Time - 0.2 μsec, smooth with a sharp break at the top
Duration - 2 to 3 μsec
PRF - less than 20 kc
Amplitude - less than 1.2 amps

The Core Drivers have faults and limitations as discussed in Section 2. For use in other applications, modifications may be necessary. A number of possible requirements for other applications and the proper modifications are listed below.

1. Decrease rise time to about 0.06 μsec - reduce plate load resistor of inverter-amplifier and/or add small inductor.

2. Long pulse duration without "droop" - increase the value of the condenser in the clamp circuit or, if the rise shape is not too important, remove it.

3. Increase output current amplitude - raise the clamp voltage or remove the condenser in the clamp circuit to increase the output of a single driver to about 2 amps.

4. Improve current source characteristics of the Model VI - change C-14 so that it is connected between the clamp voltage and the cathodes of the 6CD6's in the current amplifier. A second method is to remove C-14, replace R-37 with a 10,000 Ω potentiometer (rheostat connected), and tie the junction of R-37 and R-20 to the cathodes of the 6CD6's. With this change, R-37 (pot) would have to be adjusted for zero steady current (driver not triggered) output.

5. Improve life characteristics of the Model VI - bias the filament power supply at -90 volts or bring out separately the filaments of the 5687 and bias them at -200 volts. This is recommended for experimental or test assemblies in which Model VI's are used for long periods of time.

## 4.0 Conclusions

The Core Drivers work quite well in the application for which they are designed. They still have faults and idiosyncracies and must be modified for other uses.

The Model V is a better driver than the Model VI and is to be used instead of the Model VI whenever possible.

Signed James D Childress
James D. Childress

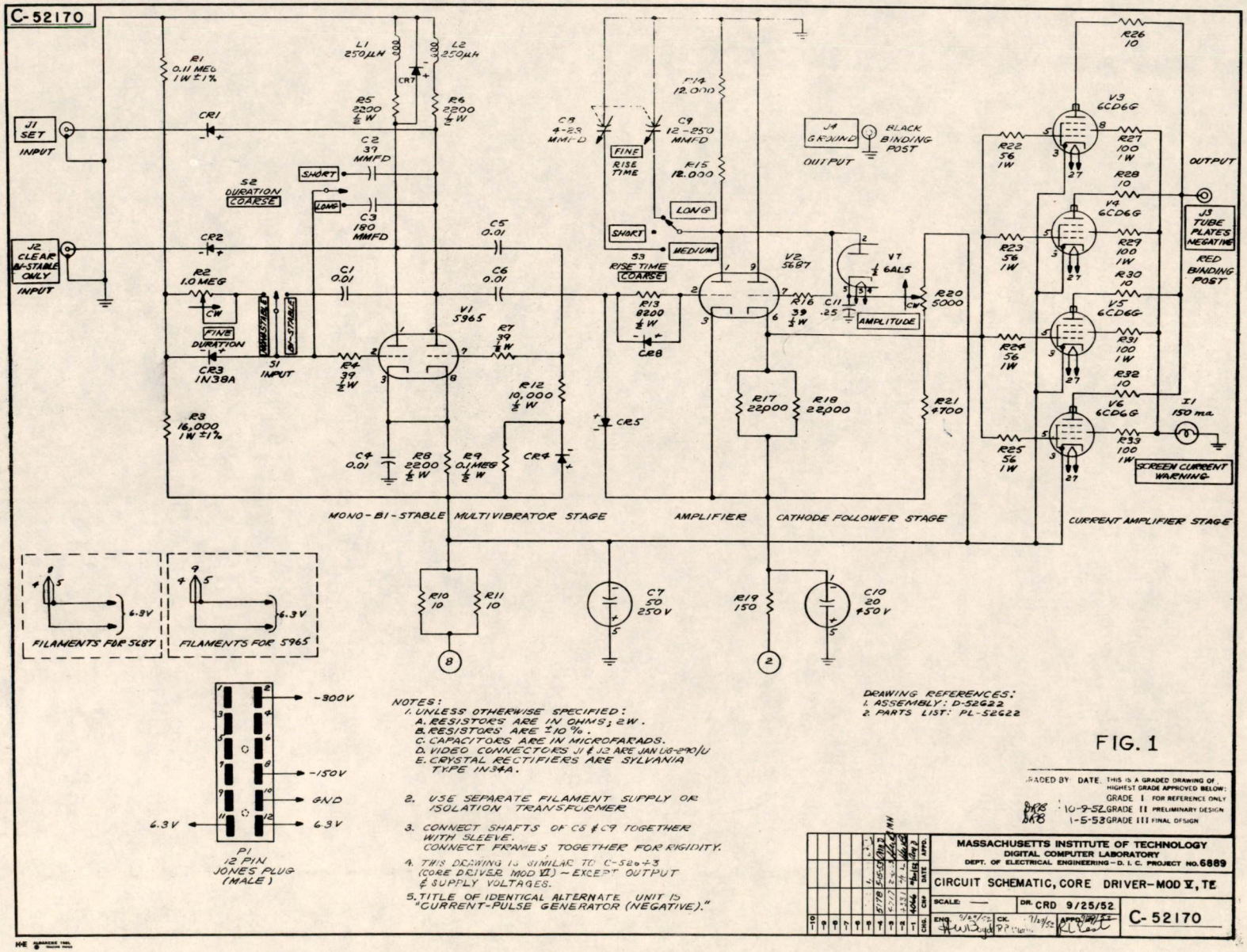
Approved DRB
David R. Brown

JDC/jk

Drawings attached:

| | |
|---|---|
| Figure 1 | C-52170 |
| Figure 2 | C-52643 |
| Figure 3 | B-58376 |
| Figure 4 | A-58374 |
| Figure 5 | A-58375 |

cc: Test Equipment Committee
Group 63 Staff
Magnetic Memory Section - Group 62




NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, 2W.
   B. RESISTORS ARE ±10%.
   C. CAPACITORS ARE IN MICROFARADS.
   D. VIDEO CONNECTORS J1 & J2 ARE JAN UG-290/U
   E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. USE SEPARATE FILAMENT SUPPLY OR ISOLATION TRANSFORMER
3. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE. CONNECT FRAMES TOGETHER FOR RIGIDITY.
4. THIS DRAWING IS SIMILAR TO C-52043 (CORE DRIVER MOD VI) - EXCEPT OUTPUT & SUPPLY VOLTAGES.
5. TITLE OF IDENTICAL ALTERNATE UNIT IS "CURRENT-PULSE GENERATOR (NEGATIVE)."

DRAWING REFERENCES:
1. ASSEMBLY: D-52G22
2. PARTS LIST: PL-52G22

FIG. 1

GRADED BY DATE. THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
DRB 10-9-52 GRADE II PRELIMINARY DESIGN
DRB 1-5-53 GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, CORE DRIVER - MOD V, TE

SCALE: —  DR. CRD 9/25/52  C-52170

ENG. 9/29/52  CK. 10/9/52  APPD.

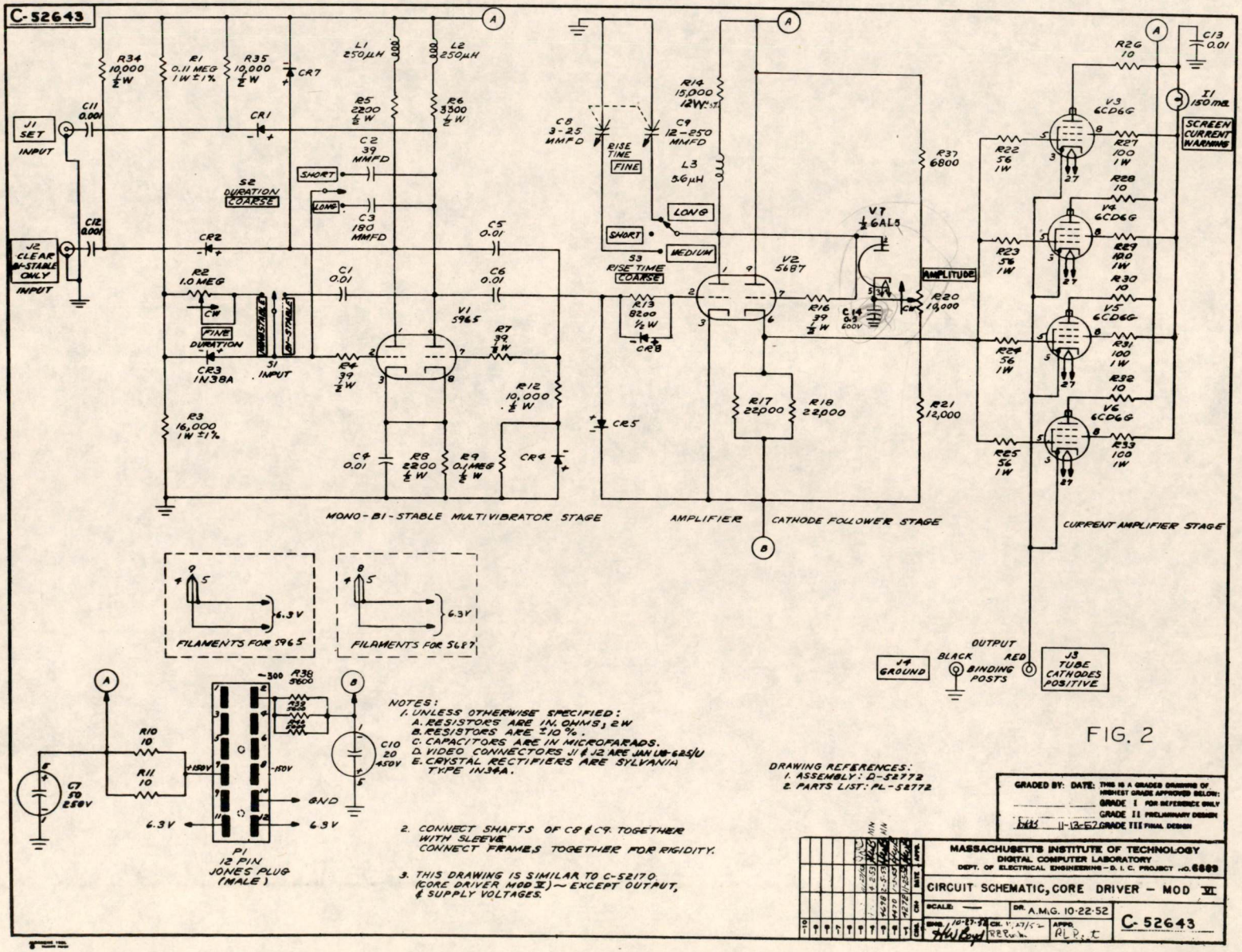



FIG. 2

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, 2 W
   B. RESISTORS ARE ±10 %.
   C. CAPACITORS ARE IN MICROFARADS.
   D. VIDEO CONNECTORS J1 & J2 ARE JAN UG-625/U
   E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE. CONNECT FRAMES TOGETHER FOR RIGIDITY.
3. THIS DRAWING IS SIMILAR TO C-52170 (CORE DRIVER MOD IX) — EXCEPT OUTPUT, & SUPPLY VOLTAGES.

DRAWING REFERENCES:
1. ASSEMBLY: D-52772
2. PARTS LIST: PL-52772

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
11-13-57 GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D.I.C. PROJECT NO. 6869

CIRCUIT SCHEMATIC, CORE DRIVER — MOD VI

SCALE: — DR. A.M.G. 10-22-52 CH. 11-27-57 APPD. RLP, t

C-52643

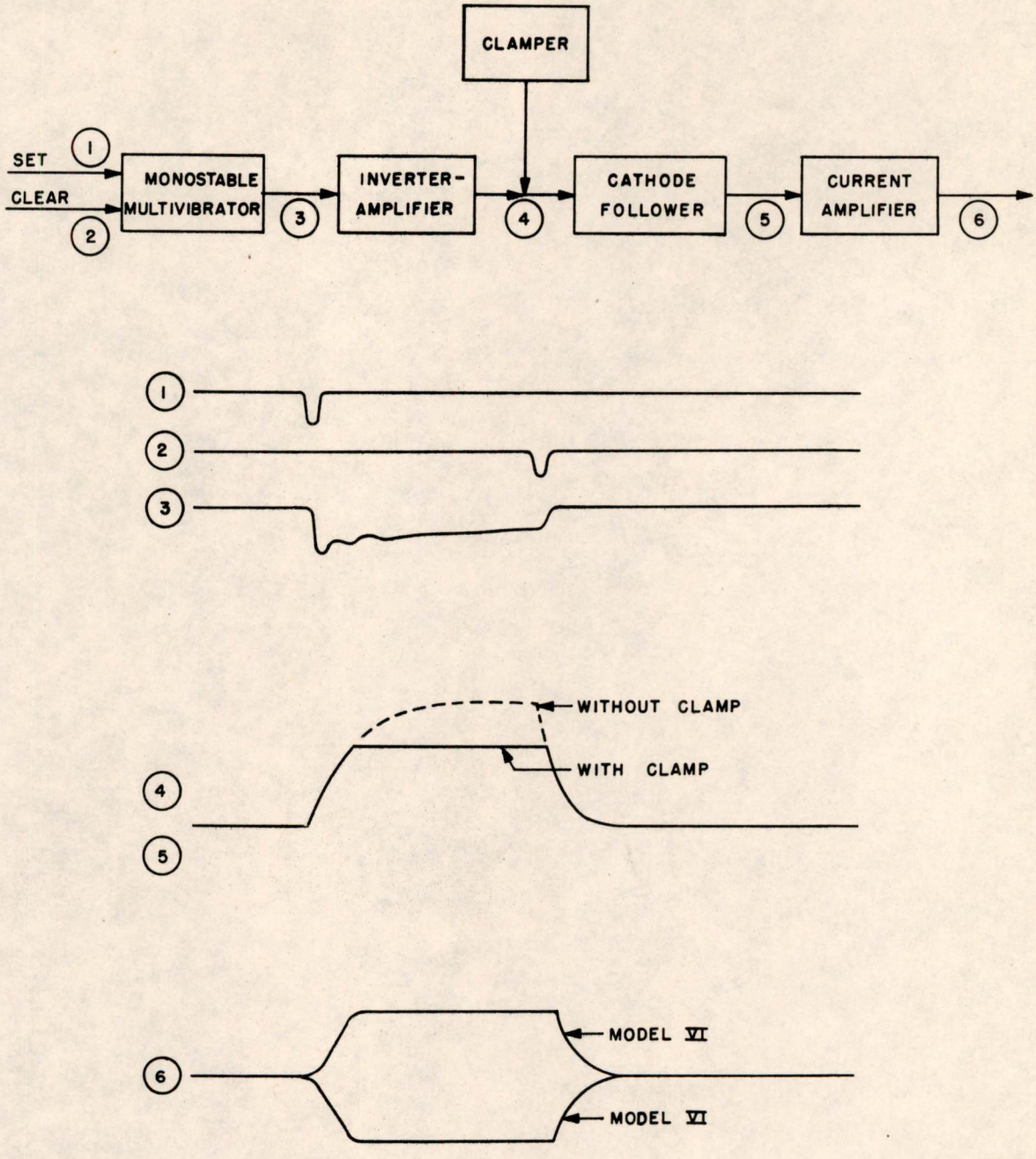
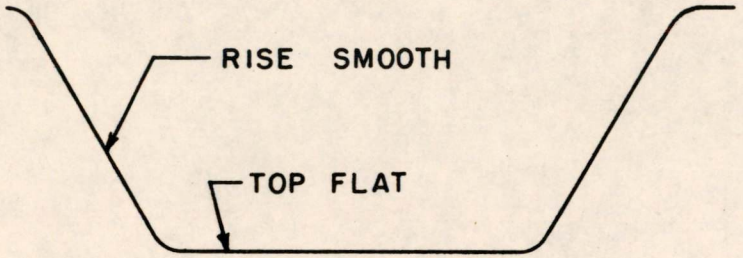


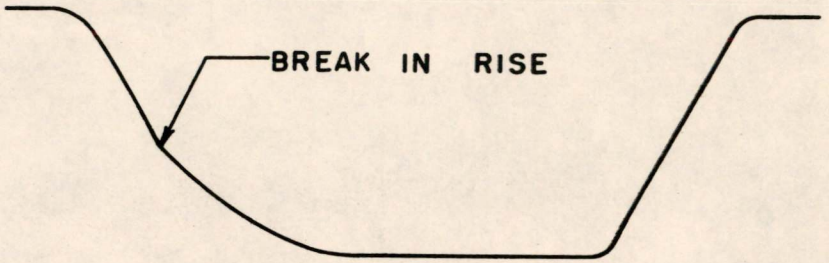

FIG. 3

BLOCK DIAGRAM AND WAVEFORMS
OF THE CORE DRIVERS

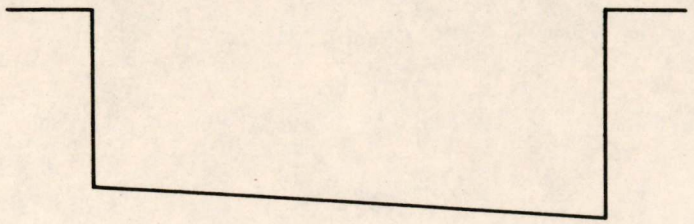
A-58374




A.
WITH CONDENSOR
IN CLAMP CIRCUIT

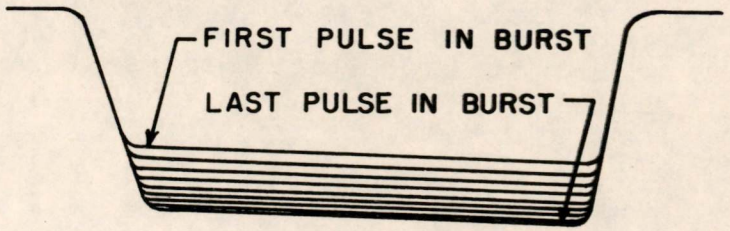



B.
WITHOUT CONDENSOR
IN CLAMP CIRCUIT



C.

LONG PULSE DURATION




D.
BURST OF
HIGH PRF PULSE

FIG. 4

OUTPUT WAVEFORMS

A-58375

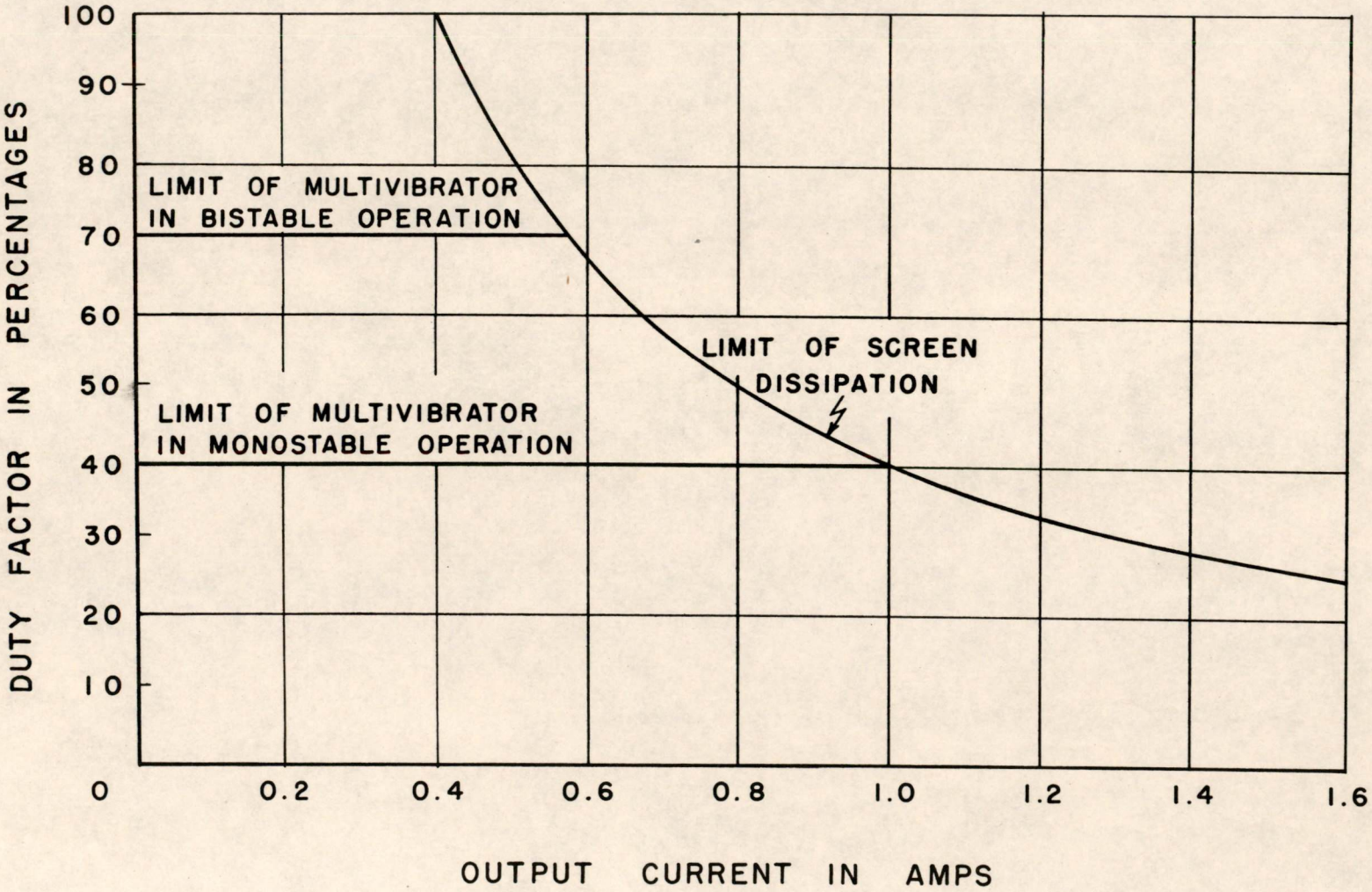



FIG. 5

DUTY FACTOR

Sydney Bradspies

April 6, 1954

## MASTER'S THESIS PROPOSAL

TITLE: A Magnetic-Core Memory With External Selection

### BRIEF STATEMENT OF THE PROBLEM

The purpose of this thesis investigation is to design, build, and evaluate the operation of a magnetic-core memory in which selection is external to the actual memory cores.

### HISTORY OF THE PROBLEM:

For several years the Digital Computer Laboratory at MIT has worked on the problems of storing binary information in a three-dimensional magnetic-core memory.[1,2] In the course of these studies, it was found that the major requirement for the cores to be used is that they have rectangular hysteresis loops (Fig. 1).

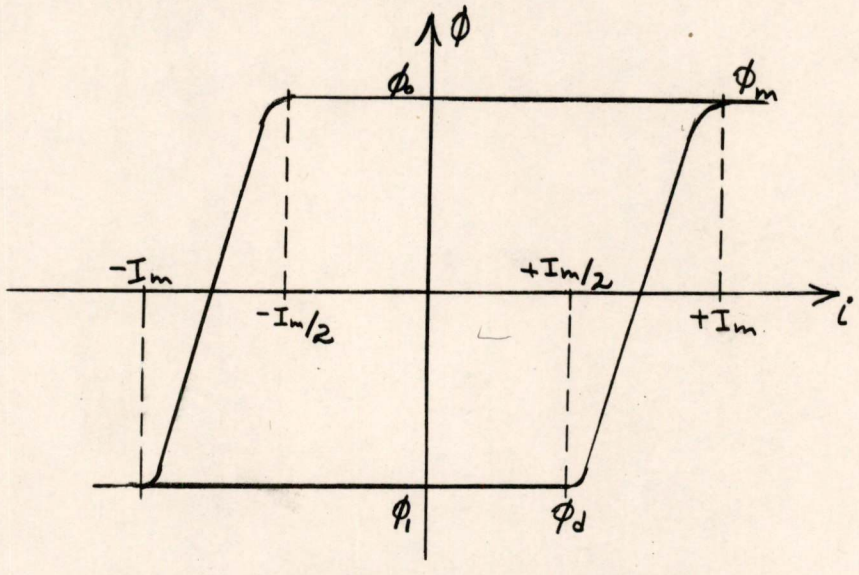



Fig. 1 A typical hysteresis loop for a magnetic-memory core

When there is no current driving a core, with such a hysteresis loop, it is in equilibrium at point $\phi_1$ or at point $\phi_0$, depending upon its previous history. By convention, the flux position $\phi_0$ is called ZERO, and $\phi_1$ is called ONE.

---

[1, 2] Superscripts refer to similarly numbered items in the Bibliography.

A simple 9-core (3 x 3) portion of a large memory plane (Fig. 2) clarifies operation of the coincident-current magnetic memory.

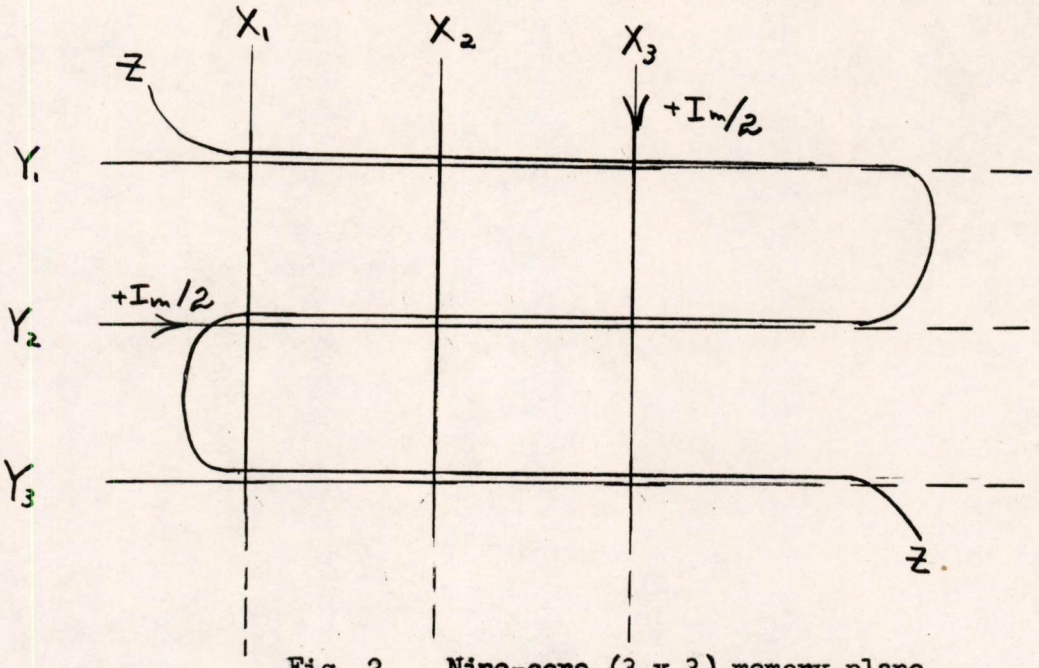



Fig. 2 Nine-core (3 x 3) memory plane.

At the intersection of each X and Y line there is a magnetic core. Both a Z (inhibiting winding used for writing ZEROS) winding and a sensing winding (used for reading out of the memory, and not shown so as to prevent confusion in the diagram) are threaded through each core.

The "read" operation passes $+I_m/2$ through the selected X and Y co-ordinates, exciting the selected core by $+I_m$. If the core holds a ONE, its flux state is reversed, and a large voltage is induced in the sensing winding. If, on the other hand, the core holds a ZERO, there is a relatively small change of flux in the core, and little voltage is induced, provided that the ratio $\phi_0/\phi_m \cong 1$ (Fig. 1). The read operation is destructive; that is, when reading has been accomplished, the core holds a ZERO, regardless of its original contents.

A number of cores lie on either the selected X co-ordinate or the selected Y co-ordinate. These cores are excited by $+I_m/2$ (that is, they are half selected). At the time of the read operation the information held by these cores is of no interest; furthermore the information that they hold should not be destroyed. For these reasons, the half selected-cores should not even be partially switched. As a consequence (referring to Fig. 1), the ratio $\phi_d/\phi_1$ has to be close to unity.

These, then, are the requirements for a core in a coincident-current magnetic memory -- the ratios $\phi_0/\phi_m$ and $\phi_d/\phi_1$ must each be

close to unity. By symmetry $\phi_0 = -\phi_1$. Therefore these conditions may be combined and restated: $|\phi_d/\phi_m|$ must be close to unity if the memory is to operate with a minimum of output signal from half-selected cores and from the selected core (if it holds a ZERO) and with a certainty that information is not being destroyed. The ratio $|\phi_d/\phi_m|$ is called the squareness ratio,[3] and it is in general somewhat less than unity.

"Writing" is accomplished in one of the following manners:

To write a ONE, pass currents of $-I_m/2$ down the chosen X and Y co-ordinates.

To write a ZERO, pass currents of $-I_m/2$ down the chosen X and Y co-ordinates, and a current of $+I_m/2$ through the Z (inhibiting) winding.

Block diagrams of the write operations may be found in the literature.[4,5]

The core performs two functions in the coincident-current magnetic memory just described: primarily it stores information, but its rectangular hysteresis loop also provides the nonlinearity which discriminates between $I_m$ and $I_m/2$, needed for selection. Because the core must be used for selection, it must have a rectangular hysteresis loop with $|\phi_d/\phi_m| \cong 1$, and the magnitudes of the switching currents are severely limited because $I_m/2$ must not even partially select a core.

For a given switched core, the change of flux is independent of the switching time, $\tau$, and the voltage induced in the sensing winding is inversely proportional to $\tau$. Thus, shortening $\tau$ increases the output voltage and also increases the speed of the memory. It has been shown[3] that $\tau$ is inversely proportional to the exciting current. The exciting current in the present memory is limited, however, by coincident-current restrictions, significantly limiting the operating speed of the memory.

PROPOSED SCHEME:

A system that did not use the memory cores for selection would avoid the restrictions on exciting current (which could be made very large, thereby reducing $\tau$ significantly) and it would reduce rectangularity requirements on the hysteresis loop of the cores. Such a system has been proposed by J. Raffel.[6]

In this memory system, switch cores A and B (Fig. 3) are used for selection. Memory core M is used solely for retention of information. This system requires 3 cores for each bit of information as compared to 1 core in the present memory. However, the rectangularity requirements placed on these cores are far more lenient than the requirements on the present cores.

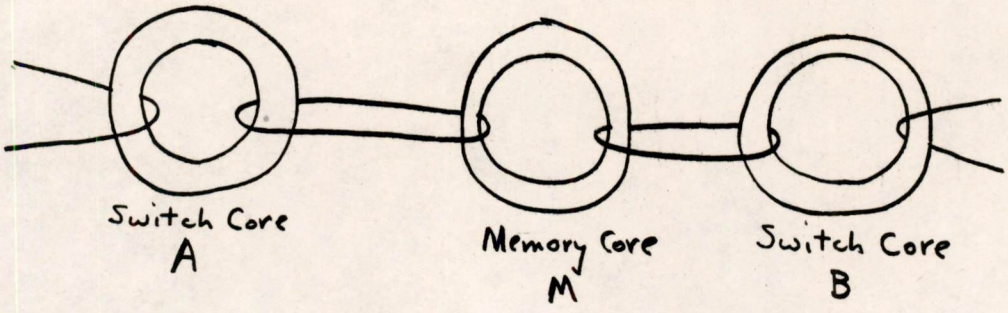



Fig. 3 Wiring necessary for one bit of information.

It is only necessary that switch cores A and B have nonlinear $\phi$-i curves (Fig. 4) and that memory core M have some remanence (Fig. 5).

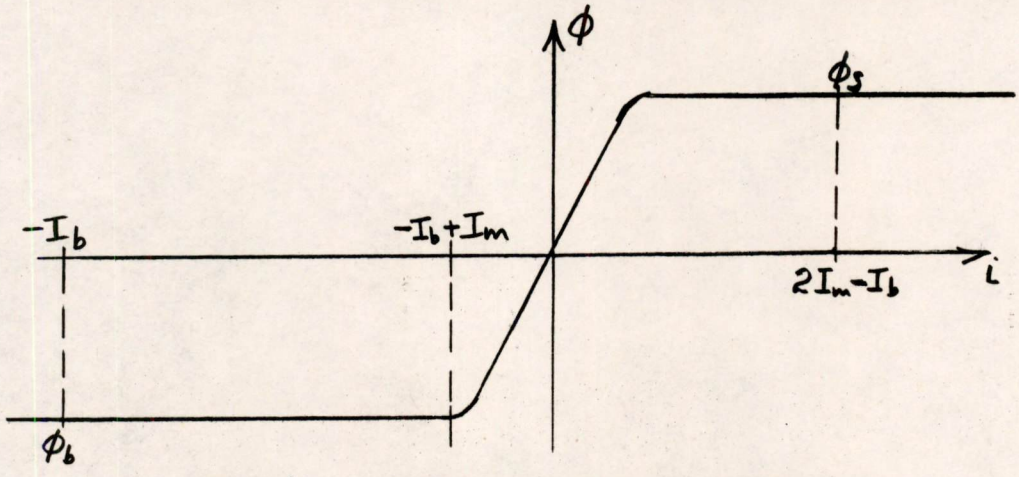



Fig. 4 Switch-core characteristics.

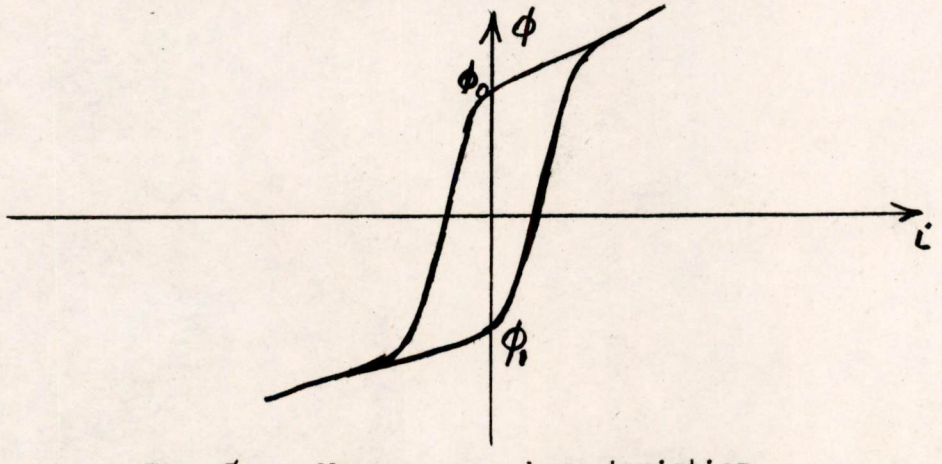



Fig. 5 Memory-core characteristics.

Let us now consider the operation of a 9-core (3 x 3) memory plane (Fig. 6), flanked by two 9-core switch planes.

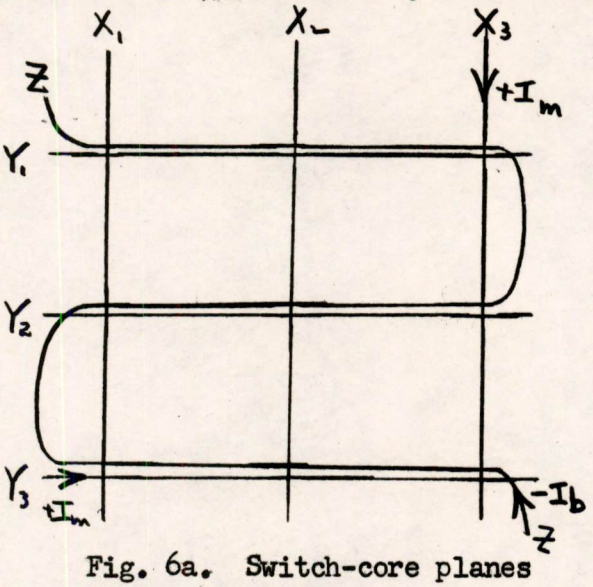



Fig. 6a. Switch-core planes (Plane A or B). Top view.

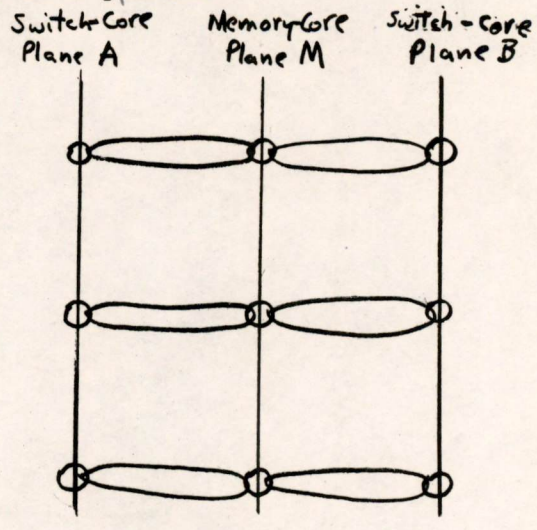



Fig. 6b. Side view of 9-bit memory

Switch-plane A is for the read operation, and switch-plane B for writing. The Z-winding (Fig. 6a) carries bias currents, $-I_b$ in plane A (Fig. 4) and $+I_b$ in plane B.

The read operation sends currents $+I_m$ along the selected X and Y co-ordinates. The selected switch core in the A plane is switched from $\phi_b$ to $\phi_s$ (Fig. 4). When the excitation of lines X and Y is stopped, switch core A reverts to $\phi_b$. The output of switch core A (Fig. 7) is coupled to the memory core M, and so the information is read out and destroyed. At the completion of the read cycle, the selected memory core holds a ONE.

If ONE is to be written in core M, switch core B is left unexcited following a reading.

If ZERO is to be written, $-I_m$ is passed along the selected X and Y co-ordinates in switch-core plane B (the Z-winding of plane B carries a bias current of $+I_b$). The output of switch core B (Fig. 8) leaves memory core M in the ZERO state.

Certain advantages may be expected from this system, in comparison to the present coincident-current-memory system:

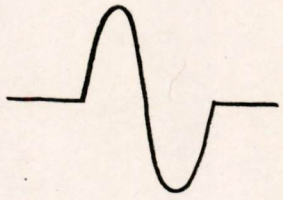


Fig. 7 Read output of switch core A.

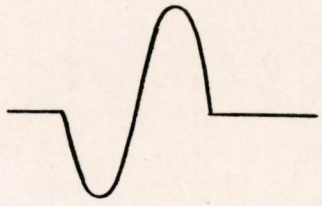


Fig. 8 Write-ZERO output of switch core B.

1. Faster switching (by an amount not yet determined) becaused the switch cores can be excited by very large currents. The only restriction is that $-I_b + I_m$ (Fig. 4) must not pass the knee of the Ø-i curve. Thus the larger $I_b$ is, the harder the core may be driven and the more rapidly it will switch.

2. Larger output ONEs because the voltage output is inversely proportional to the switching time.

3. The hysteresis-loop requirements on the various cores are relaxed as is evidenced by comparing Figs. 4 and 5 to Fig. 1.

There are, however, some disadvantages immediately obvious in the proposed system:

1. The coupling necessary between the cores of planes A, B, and M is such that difficulties in construction may be expected.

2. For a word n digits in length, at least 2n + 1 cores are required (1 A core, n B cores and n M cores). The present system requires only n cores.

## PROPOSED PROCEDURE

### 1. Determine the Magnetic Properties of Cores

Metallic and ferrite cores with various types of hysteresis loops will be tested. The operating characteristics of these cores will be determined and compared to ascertain how poor the cores may be and still be satisfactory for the proposed memory. The relative sizes of the switch and memory cores will be ascertained. Limits on core uniformity must also be determined.

2. Determine the Operation of the Memory

Investigations will be made into the requirements to be placed on the loop of wire coupling the memory core to the switch core. Operating characteristics will be found for various resistance values of this loop. Also to be determined is the number of times this loop should be wrapped around both the switch and memory cores.

Signal-to-noise ratios are extremely important and will be established for various schemes of wiring and for different cores.

3. Operation of Experimental Model

The switching logic for a simple 3-dimensional memory will be designed. The memory will be built and tested. Its operating characteristics -- switching time, outputs and core requirements -- will be compared to those of the present magnetic core memory.

EQUIPMENT NEEDS

The magnetic cores and the equipment necessary for testing the cores are available at the MIT Digital Computer Laboratory.

ESTIMATED DIVISION OF TIME:

| | | |
|---|---|---|
| 1. | Preparation of Proposal | 50 hours |
| 2. | Further study of Literature | 30 hours |
| 3. | Experimental Work and Analysis | 200 hours |
| 4. | Correlation of Results and Formulation of Conclusions | 50 hours |
| 5. | Preparation of Thesis Report | 70 hours |
| 6. | Total | 400 hours |

SIGNATURE AND DATE

Signed: Sydney Bradspies
Sydney Bradspies

Date: April 7, 1954

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

Approved: William K. Linvill
William K. Linvill
Associate Professor of
Electrical Engineering

SB:cs

## BIBLIOGRAPHY

1. J.W. Forrester, "Digital Information Storage in Three Dimensions Using Magnetic Cores," R-187 (May 16, 1950), MIT Digital Computer Laboratory Report.

2. W.N. Papian, "A Coincident Current Memory Unit," R-192 (September 8, 1950), MIT Digital Computer Laboratory Report.

3. J.B. Goodenough, N. Menyuk, "Nucleation of Domains of Reverse Magnetization and Switching Characteristics of Magnetic Materials," E-532 (March 9, 1953) MIT Digital Computer Laboratory Engineering Note.

4. K.H. Olsen, "A Magnetic-Matrix Switch and Its Incorporation into a Coincident-Current Memory," R-211 (June 6, 1952), MIT Digital Computer Laboratory Report.

5. B. Widrowitz, "The 16 x 16 Metallic-Core Memory Array, Model I," R-216 (September 25, 1952), MIT Digital Computer Laboratory Report.

6. J. Raffel, "Core Memory Using External Bit Selection," M-2736 (March 18, 1954), MIT Digital Computer Laboratory Memorandum.

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: JUNCTION-TRANSISTOR MAGNETIC CORE DRIVERS

TO: The Transistor Section - Distribution 2

FROM: Stanley Oken

DATE: 20 March 1954

ABSTRACT: A transistorized core driver, employing one point-contact and one junction transistor, which can drive the equivalent of about 200 metallic magnetic memory cores in series is discussed in detail. A current output of 12 ma with a rise time of 0.3 μsec can be obtained from this circuit. The note begins with a discussion of the relative merits of point-contact and junction type transistors as core drivers. This is followed by an analysis of the grounded-emitter connection of the junction transistor. Next, the transistorized core driver circuit is presented and discussed in detail, including input and output characteristics, design criteria, and voltage margins. Finally the current and voltage outputs from the driver when it is driving the equivalent of a memory plane are shown. The note terminates with a paragraph on the future prospects for this type of driver.

## 1. A COMPARISON OF POINT-CONTACT AND JUNCTION TRANSISTORS AS CORE DRIVERS

The transistor core-driver for fast switching magnetic cores must possess sufficient power handling capacity, a fast rise time or high-frequency response, and a high output impedance.

Although the point-contact transistor has a higher frequency response than present junction transistors, its power handling capacity and output impedance level are much smaller.

Due to its extremely high output impedance the junction transistor is inherently a better current source than a point-contact transistor. The output impedance of a junction transistor is in the range of 500 KΩ to 1 MΩ while that of the point-contact transistor is only about 20 KΩ.

At the present time most transistor manufacturers are concentrating on the production of junction transistors with a higher frequency response. Other work is directed toward the development of power junction transistors. The ideal core driver for a coincident current memory requires a combination of the two characteristics.

## 1.1 POWER LIMITATIONS

Above a temperature of about 60 - 80° C. germanium will act as though it were intrinsic, i.e., the donor and acceptor type impurities which were added to control the conductivity of the germanium material, will no longer exert an appreciable effect. Thus the power-handling capacity of a transistor is governed by the temperature of the p-n junction. As the temperature depends largely upon the current density in the junction area, the larger the contact area the greater the power and current rating of the unit will be.

In the point-contact transistor the contact area is governed by the cat whisker electrodes which are very small. The power rating on this unit is therefore relatively low and it does not appear to be an easy matter to increase it.

The contact area in a junction transistor depends upon the area of the bulk of germanium which can always be increased. Therefore, the future in large power handling transistors lies with the junction transistor, and in fact, some transistors have already been developed which can handle several watts of power. However, due to the large junction areas in these units the collector capacitance has been greatly increased, and thus they have a very poor frequency response, i.e., $f_{co}$ lies in the audio range.

A transistor found to be acceptable is a low-power commercially-built npn transistor with $f_{co} \cong 2$ mc, which has been modified to allow a larger collector power dissipation. It will be discussed later in the paper.

## 1.2 FREQUENCY RESPONSE

The higher frequency response of point-contact transistors as compared to junction transistors is mainly due to three effects. These are:

1) The mechanism through which the minority carriers flow from the emitter to the collector.

2) The spacing between the emitter and collector electrodes.

3) The collector capacitance.

In the point-contact transistor the distance that the minority carriers must traverse is very small since the two terminals are only about 0.002" apart. Furthermore, the carriers move mainly under the influence of an electric field at the points. This field produces a relatively fast movement of the carriers and a resultant high frequency response. The small collector capacitance of this unit also contributes to its good frequency response.

In the junction transistor the applied field has very little effect on the flow of carriers in the base region and so the flow is mainly due to a diffusion of the minority carriers in the germanium. This in itself would limit the frequency response of the unit, for the process of diffusion is a relatively slow one. Aside from the above consideration, the physical structure of the unit, i.e. the width of the base region, as well as its large collector capacitance are detrimental to a high frequency unit. If one is willing to accept small power dissipations the junction areas can be made smaller and an $f_{co}$ in the order of two megacycles can be achieved.

## 2. THE GROUNDED-EMITTER CONNECTION OF THE JUNCTION TRANSISTOR

Since $\alpha_e$ for a junction transistor is less than unity, the first circuit which was evaluated was the grounded-emitter connection which affords a large current gain. The standard equivalent circuit for the grounded-emitter connection is shown in Fig. 1A. Another useful equivalent circuit for the grounded-emitter connection can be derived by the usual methods employed in network synthesis.

Any two terminal-pair network can be represented by the following equilibrium equations: (Fig. 1B)

$$V_1 = I_1 Z_{11} + I_2 Z_{12} \tag{1}$$

$$V_2 = I_1 Z_{21} + I_2 Z_{22} \tag{2}$$

By adding and subtracting $I_1 Z_{12}$ in equation 2) we obtain

$$V_2 - I_1 (Z_{21} - Z_{12}) = I_1 Z_{12} + I_2 Z_{22} \tag{3}$$

An equivalent circuit which can be represented by equations 1) and 3) is shown in Fig. 1C. In this diagram the $I_1 (Z_{21} - Z_{12})$ voltage source has been converted to a current source. From the usual grounded-emitter equivalent circuit, Figure 1A, the values of the open-circuit transfer impedances, which are required for the equivalent circuit of Fig. 1C, can be obtained as follows:

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2 = 0} = r_b + r_e \tag{4}$$

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1 = 0} = r_e \tag{5}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2 = 0} = r_e - \alpha_e r_c \tag{6}$$

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1 = 0} = r_e + r_c (1 - \alpha_e) \tag{7}$$

When these values are substituted into the equivalent circuit of Fig. 1C and $V_1$, $I_1$, $V_2$, $I_2$ are replaced by $V_b$, $I_b$, $V_c$, $I_c$ respectively, the circuit in Fig. 1D is obtained.

## 2.1 THE TRANSFER FUNCTION OF GROUNDED-EMITTER CIRCUIT

The usefulness of the circuit of Fig. 1D is readily demonstrated when the transfer function of the circuit is calculated. This equivalent circuit permits us to compute the transfer function $I_c/I_b$ without regard to any internal current such as $I_e$. It should be noted here that the dependent current source is expressed in terms of the input current $I_b$ not the emitter current.

If such factors as collector capacitance and transit time are to be included in the calculation, $r_c$ becomes paralleled by the collector capacitance and

$$\alpha_e = \frac{\alpha_o}{1 + \tau s} = \frac{\alpha_o}{1 + j\frac{f}{f_o}} \tag{8}$$

where $\alpha_o$ is the current gain, in the grounded-base connection at low frequencies, and $f_{co}$ is the cut-off frequency of the unit in the base connection.

If both effects are included the result will be so complicated algebraically that it will be of no practical use. For a more or less qualitative result the collector capacitance will be neglected. This assumption is valid for very low load impedances. In our case the result will be on the optimistic side. The exact calculation is given in the appendix. The result is

$$I_c(t) = +\frac{\alpha_o I_b}{(1-\alpha_o)}\left\{1 - \left[1 + \frac{r_e(1-\alpha_o)}{\alpha_o r_c}\right]e^{-\frac{(1-\alpha_o)}{\tau}t}\right\} \tag{9}$$

There are three things to note in this equation. First, there is a current gain of $\alpha_o/(1-\alpha_o)$ which can be very large if $\alpha_o$ is very close to unity. The time constant of the circuit has now become $\tau/(1-\alpha_o)$. The latter was to be expected for the gain-bandwidth product for the base connection must be the same for any other connection of the transistor. The third fact is that there is a small initial jump opposite to the direction in which $I_c$ will finally flow. This is due to direct feed-through from the source since the dependent current generator has not yet had time to respond to the input signal. The waveform is given in Fig. 2.

If we assume that $f_{co}$ = 2 mc in the grounded-base connection and $\alpha_o$ = 0.9, then for the grounded-emitter circuit $f_{co}$ = 0.2 mc and the equivalent time constant is about $0.8 \times 10^{-6}$ seconds. Then since the rise time is 2.2 time constants, the rise time in the grounded-emitter connection would be 1.7 μsec. This is a conservative estimate as mentioned previously, since the collector capacitance has been neglected.

The effect of the rise time of the driving current pulse on the output of the switching metallic cores[1] is shown in Fig. 3. From these pictures it is obvious that if we want a good ratio of "1" to "0" output at the sensing time, the rise time should be kept less than 1 μsec. The grounded-emitter circuit cannot satisfy this requirement when operated in the active region and must, therefore, be ruled out for the magnetic core driver. One can decrease the rise time by driving the collector into a saturated condition. This procedure actually involves taking a small part of a large exponential. It yields a decrease in effective rise time with a subsequent loss in gain. The rise time can be greatly reduced by this method but the resulting circuit will not be useable as a core driver. This is the case because the circuit will now act like a voltage source rather than a current source, since the current output is taken when the transistor is in the low impedance saturated state. This type of circuit may find applications in magnetic stepping registers or pulse circuits in general, where a gain in current is desired and the driver may approximate a voltage source without any disadvantages.

## 3. THE GROUNDED-BASE CONNECTION

Although the current gain in the grounded-base connection of a junction transistor is slightly less than unity, the frequency response is satisfactory for driving cores since rise times of the order of 0.2 μsec are obtainable from some commercial transistors. Unfortunately, these high-frequency transistors usually have power ratings of about 50 mw. In order to safely dissipate, say, 240 mw at the collector of the transistor, the unit must be cooled in some manner to keep the junction temperature down. One way to accomplish the cooling is to place the transistor in a glass enclosure and fill the space in the enclosure with silicon oil type DC550.[2] A transistor modified in the above manner was obtained from S. Schwartz. It is a Germanium Products n-p-n Junction transistor type 2520 K, with the following characteristics:

$$f_{co} = 2 \text{ mc}$$

$$r_{cr} = 1.09 \text{ m}\Omega$$

$$\alpha_o = 0.98$$

$$C_c = 13 \text{ } \mu\mu\text{f} \quad (Vc = 4.5v)$$

## 4. THE TRANSISTORIZED MAGNETIC CORE DRIVER CIRCUIT

The core driver which was developed on the basis of the above considerations consists of a voltage-source type input stage driving a

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[1] Magnetics Inc. Mo-Permalloy Core, 1/4 mil, 1/8" width, 1/8" diam, 5 wraps

[2] J. G. Mavroides and S. Schwartz - Lincoln Laboratory Technical Memorandum No. 38 - "Half Watt Power Transistors Obtained by Modifying Commercial Transistors." Sept. 16, 1953

current-source type output stage. The input stage is a single-transistor flip-flop which supplies a large current at a low impedance (it goes into the saturated region). The output stage converts the low impedance to a high impedance with only a slight loss of current. A circuit schematic diagram of the driver is given in Fig. 4A. The two pulse transformers shown are used to switch the circuit to the state specified in the diagram. When the point contact flip-flop is in the "on" (saturated) condition, diode $d_1$ and the emitter diode of the npn transistor are in the reverse direction. Thus there is no current supplied to the cores. If the first stage is driven "off" by applying a negative pulse at the emitter, both diodes switch to the forward conducting state. The collector voltage of the flip-flop is clamped to $V_4$ and the base voltage to $V_2$. Since the emitter of the npn transistor is in the forward direction at this time, it is in this state of the flip-flop that the driving current is sent through the core winding.

The clamping of the collector voltage to the value $V_4$ serves several purposes. The clamping action makes the current in the emitter of the second stage almost independent of the transistor in the first stage. The transistor in the first stage must just be capable of changing states. Also, since we would like the output current of the driver to be relatively large, this large current must be supplied by the flip-flop. This, in turn, means that large voltages must be employed. As the clamping of the collector voltage reduces the collector power dissipation in the "off" condition, it in effect permits us to use large voltages and yet not exceed the power ratings on the transistor.

### 4.1 DESIGN CRITERIA FOR FLIP-FLOP

The equivalent circuit of the driver is shown in Fig. 4B. In the design of the flip-flop stage of the core driver, there are three main points to be considered. These are:

1) In order to obtain a stable point in the "on" condition $\alpha_e \; I_{e\ "on"} > I_{c\ "on"}$

$$\text{or} \quad \alpha_e > \frac{I_{c\ "on"}}{I_{e\ "on"}} \tag{10}$$

The circuit must therefore be designed for a minimum $\alpha_e$. This limit is chosen from practical considerations to be $\alpha_{e\ "on"} \cong 1.9$.

2) The amount of saturation should be not excessive. The saturation current is the net current flowing through the internal collector diode[3], when the transistor is in the saturated region. Thus:

$$\alpha_e \; I_{e\ "on"} - I_{c\ "on"} = I_{sat.} \tag{11}$$

---

[3]The diode mentioned is the equivalent collector diode in the T-equivalent circuit for a transistor.

It has been shown experimentally that the "hole storage" time[4] increases with the magnitude of $I_{sat.}$ and with the length of time in saturation. Large hole storage effects necessitate using larger and/or wider triggering pulses to switch the flip-flop to the "off" state.

Furtherfore, since the rise time of the output current depends upon the length of time it takes the flip-flop to switch from the "on" to the "off" condition, a large amount of hole storage would be detrimental to a good rise time.

3) The desired current output must be specified. This current will be

$$I_o = \frac{V_3 - V_4}{R_2 + d_2 f} \qquad (12)$$

It should again be noted that the current is independent of the parameters of the transistor in the flip-flop.

## 4.2 THE $V_e$-$I_e$ CHARACTERISTIC OF THE FLIP-FLOP

The $V_e$-$I_e$ characteristic of the flip-flop shown in Fig. 5, can be determined by the ensuing procedure. A variable current source, $I_e$, is assumed to be applied at the emitter terminals. The break points in the $V_e$-$I_e$ characteristic are then determined by the values of $I_e$ at which the different diodes in the equivalent circuit are forced to change their state. In order to find these values of $I_e$, the circuit is cut across the diode or diode-and-battery combination of immediate interest. A Thevenin's equivalent circuit is then obtained for the remainder of the circuit looking from the cut terminals. When the resultant current is zero the diode is just about to switch; this condition therefore specifies a value of $I_e$.

The internal emitter resistance can be neglected when calculating the values of emitter current because it is in series with the current source $I_e$. However, it should be included when the value of $V_e$ at a break point is sought.

It can be seen in Fig. 5 that the trigger voltages, based on the dc conditions, which are required to flip the circuit to the "on" position (~1.5 v) and to the "off" position (~8 v) are quite different. If a negative bias voltage is used in the emitter circuit, the emitter load line, (which is now the line $V_e=0$), will be effectively shifted downward in voltage. Thus the trigger requirements will be more nearly equal. The input requirements have not been stressed in the note because the problem of using the driver with a diode matrix has not been tackled yet. This will require bias batteries and perhaps a resistance in the

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[4] "Hole storage" is the effect which causes a delay when the transistor is pulsed so as to switch the unit from the saturated condition to the "off" condition.

emitter circuit, so that the trigger requirements and the "off" and "on" position points will be different.

It should also be noted that since the slope in the "on" condition depends mainly on $R_1$ and $R_2$ it cannot be changed inasmuch as other considerations specify the value of these parameters. This will be discussed later.

## 4.3 THE $V_c$ - $I_c$ CHARACTERISTICS OF THE FLIP-FLOP

The collector characteristic is derived in the following manner. With a value of $I_e$ specified from the $V_e$ - $I_e$ characteristics, $I_c$ and then $V_c$ can be found by using Thevinen's equivalent circuit for the current sources.

From Fig. 6 and the equation for $V_{c1}$, it is obvious that the maximum power dissipation is determined largely by $V_4$, which should therefore be limited in magnitude to about 10 v.

The calculated voltages at the point where the transistor switches to the "on" state, ($V_{c3}$), and at the stable point in the "on" condition are not strictly correct. In order to make a good approximation to the actual voltages at these points $r_b$ cannot be neglected, for if it is $V_{c3} = 0$. This we know is not true. In this region the usual equivalent circuit does not hold since the values of $V_c$ obtained experimentally are about 1.5 volts lower than that calculated. One method used to overcome this difficulty is that of replacing the dependent current source and collector resistance by a constant voltage source.[5] The value of this voltage is naturally dependent upon the value of $V_{c34}$ for the transistor, but it will normally be about V =-1.5 volts. Experimentally, it can be seen that in the saturation region the value of $r_b$ is much smaller than that in the active region. From the usual equivalent circuit it can be shown that the voltage $V_c$ "on" should be more positive than $V_{c3}$. The above facts, coupled with the fact that the actual measured voltage $V_c$ "on" varies with different transistors from 2 - 3.5 volts, make the following assumptions desirable:

1) The equivalent battery should be 1.5 v

2) $r_{b\ act} = 300\Omega$

3) $r_{b\ sat} = 100\Omega$

The maximum power dissipation is seen from Fig. 6 to be about 100 mw. As this occurs only for a short period of time, this power dissipation is not harmful to the transistor. The power dissipation in the "on" condition is also very important, since the flip-flop remains in this position except when an output pulse of current is desired. As explained previously, the calculated value of $V_c$ "on" is not too accurate.

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[5] This method was first used by Arthur W. Lo in "Transistor Trigger Circuits" Proc. IRE Nov. 52, p. 153.

[6] $V_{c34}$ is the collector to base voltage with $I_e$ = 3 ma and $I_c$ = - 4 ma.

Thus, the power dissipation in the "on" state varies with different transistors. When actual measurements were made on the circuit, the power dissipation at this point for several different transistors was found to be in the 30 - 50 mw range.

### 4.4 NUMERICAL VALUES FOR CIRCUIT PARAMETERS

The desired output current is about 12 ma. From collector power dissipation considerations, $V_4$ is chosen to be 10 v. $V_1$ and $V_3$ are conveniently chosen to be $V_1 = 40$ v and $V_3 = 50$ v. With larger voltages the power dissipation in the "on" condition will be excessive, since a larger value of $I_{c\ "on"}$ will be obtained. With these values and equation 12, section 4.1, the value of $R_2$ is calculated to be 3.2 K.

A value of $V_2 = 2$ v is chosen as a compromise between stability and input pulse height. A smaller value would mean the circuit might trigger with noise while a larger value would necessitate a large input trigger pulse.

The next value to be specified is that of $R_1$. Its magnitude is chosen as a compromise between stability and hole storage effects. As pointed out previously in equation 10), the requirement for a stable state in the "on" condition is

$$\alpha_e I_{e\ "on"} + I_{c\ "on"} > 0.$$

But, the larger the magnitude of the left-hand side of the inequality, the longer the hole storage time will be. The circuit was designed for a value of about $\alpha_e = 1.9$. This value seemed to be the best one experimentally. With this value of $\alpha_e$ the value of $R_1$ is found to be 5.5K.

### 4.5 TRANSISTOR SPECIFICATIONS FOR THE FLIP-FLOP STAGE OF THE DRIVER

The specifications for the point-contact transistor which is to be used in the flip-flop stage are:

1) $\alpha_e > 1.9$.

2) The value of $V_{c34}$ should be limited to a maximum of about - 1.5 v since $|V_{c\ "on"}|$ increases as $|V_{c34}|$ increases. A larger $|V_{c34}|$ therefore means that there will be a larger collector dissipation in the "on" condition.

3) The storage coefficient[7] should be about 0.5 or less so that hole storage will not adversely effect the switching of the flip-flop.

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[7] Storage Coefficient = $\frac{\text{Turn-off-Time}}{(\alpha_e - 1)}$

4) The rise time of the transistor should be about 0.2 μsec if trigger pulses with small widths are desirable.

## 5. COLLECTOR OPERATING PATH FOR THE OUTPUT STAGE

The idealized collector operating path of the output stage is given in Fig. 7. The circuit normally sits at point A. When a current, with a trapazoidal waveshape, is applied to the emitter, i.e., when the flip-flop is pulsed to the "off" state, a large back voltage ($V_b = L_{eq}\frac{di}{dt}$) is developed across the cores. When the output current reaches its maximum value, $I_{co} = \alpha_e I_{e1}$, the voltage across the inductance jumps to zero and the equivalent impedance of the cores is just the d.c. resistance of the windings. The path followed is thus ABCD. At the end of the input pulse, i.e., when the flip-flop is triggered to the "on" condition, the emitter current decreases linearly to zero. The operating path is similar to the initial path but the back voltage is in the opposite direction. The operating path is now DEFA. Since $I_{c_{max}} \left[V_{c2} + V_4\right]$ is set as close to the maximum power rating is as deemed safe, the return path leads to excessive power dissipations. This problem will be further discussed in section 7, when the equivalent circuit for the cores is considered.

### 5.1 THE OUTPUT IMPEDANCE OF THE DRIVER

The output impedance of the final driver stage is a good indication of the ability of the driver to act like a current source. The output impedance of the transistor ($r_{co}$) was measured and found to be about 1 mΩ. Figure 8 illustrates the ability of the driver to act as a current source. The load used here was a 330 ohm resistor, and the voltage across it was taken as a measure of the output current. The two waves shown in the picture were obtained at $V_{cc}$ = 25 v and $V_{cc}$ = 4 v. The change in current with the two values of $V_{cc}$ was only 1 ma in a normal value of 12 ma. It should be noted here that a back voltage of 21 volts can be tolerated with only a 1 ma change in the output current.

### 5.2 SPECIFICATIONS FOR THE JUNCTION TRANSISTOR

As mentioned previously, in order to obtain a current output from the driver which has a fast enough rise time to be useful and which is at a high impedance level, the junction transistor must be operated in the grounded-base connection and in the active region. This, in turn, means that the transistor must be able to safely dissipate a large amount of power. The specifications for a junction transistor in this circuit are as follows:

1) $f_{co} \geq 1$ mc. This indicates that a rise time of 0.5 μsec is desired.

2) About 250 mw collector dissipation. This value will vary with the back voltage expected across the core. Since in section 5.1 it was shown that the back voltage can be a maximum of 21 v, and the current supplied is 12 ma, the power dissipation required is specified.

3) $\alpha_e \geq 0.9$. The value of $\alpha_e$ specifies the current loss in the output stage. Lower values of $\alpha_e$ can be used if the flip-flop stage is redesigned to give a little larger current output.

## 6. VOLTAGE MARGINS OF THE CORE DRIVER

The variation of transistor parameters in the flip-flop stage of the driver has very little effect on the output current as long as the circuit still changes state. This is due to the fact that the transistor is acting as a switch. The d-c voltages actually determine the current supplied to the second stage. These voltages must therefore be regulated.

The current output will not vary with the d-c voltage on the collector of the output stage because, as shown previously, the driver is a good current source.

With an input pulse of 12 v amplitude and about 0.25 μsec width, the following margins can be expected. (It must be noted that only one power junction transistor was available and only about 10 point-contact transistors were tried.)

$$V_1 = 40 \begin{matrix} +6 \\ -5 \end{matrix} \text{ volts}$$

$$V_2 = 2 \begin{matrix} +4 \\ -1.5 \end{matrix} \text{ volts}$$

$$V_3 = 50 \begin{matrix} +2.5 \\ -2.5 \end{matrix} \text{ volts}$$

$$V_4 = 10 \begin{matrix} +2.5 \\ -2.5 \end{matrix} \text{ volts}$$

When $V_1$ or $V_2$ exceeds the range of voltages shown, the circuit will not trigger. The nominal $V_3$ and $V_4$ voltages can be other than specified and the circuit will still operate. The range of voltages for $V_3$ and $V_4$ was determined by the stipulation that the current output not vary more than 1 ma from the nominal value of 12 ma.

## 7. THE EQUIVALENT CIRCUIT FOR THE CORES

The problem of deriving an equivalent circuit for the cores to be driven now presents itself. The output voltage from one core with a "non selection"[8] pulse of current through it is shown in Fig. 9. Since the driver can withstand a back voltage of about 21 v and the output voltage from one core is about 0.12 v, 180 non-selected cores in series can be driven. By using a current pulse with a longer rise time, the initial spike can be reduced to about 0.1 v and thus 200 cores can probably be driven.

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[8] A "non selection" pulse is the pulse obtained from only one driver in a coincident current memory system.

An equivalent circuit of the cores is shown in the dotted box in Fig. 10. The inductance L and resistor $R_3$ are used to give the initial spike and its decay time. Resistor $R_2$ is a resistor, which will have to be added to damp out the oscillations, while the diode and resistor $R_1$ are used to clamp the collector voltage to its nominal value of 25 v. Without this diode, the back voltage developed across the cores will make the collector voltage very large and thus the power dissipation will be exceeded. Resistor $R_1$ can be employed to make a compromise between the clamping action and the fall time of the current wave. With the diode included in the circuit, the operating path in the $V_c$ - $I_c$ characteristic of Fig. 7 is modified. It is now ABCDGA. The effect of including the diode in this circuit is shown in Fig. 11. It would be of very little practical value to determine specific values for these components since this is not an exact equivalent circuit of the cores. When the memory is built the final values can be determined.

## 8. REQUIRED POWER RATING OF THE TRANSISTOR WITH THE NUMBER OF CORES TO BE DRIVEN SPECIFIED

The power rating required of the junction transistor in the final core-driver stage can be approximated in the following manner:

1) From the value of coercive force ($H_m$) for the core, and its physical dimensions, the ampere-turns (NI) which must be supplied by each driver are specified. Each driver supplies half the ampere-turns required to bring the core to a magnetization, equal to $H_m$.

2) The current $I_o$ is then specified. This, in turn, determines the turns $N_o$ required on each winding.

3) The output voltage per core per turn, $V_p$, is determined experimentally with the above ampere turns applied.

4) The power rating of the transistor must be approximately

$$P = C N_o V_p I_o$$

where C = the number of cores to be driven in series.

## 9. FUTURE PROSPECTS

Through the use of complementary symmetry,[9] i.e., n-p-n and p-n-p junction transistors, it should be possible to design a driver which can "read" and "write" information on only one winding. This would save about one half of the windings on the core. The driver would consist of two of the above type drivers, one with a p-n-p output stage, the other

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[9] "Symmetrical Properties of Transistors and Their Applications", by G. C. Sziklai Proc. IRE June 1953 p. 717-24.

with an n-p-n stage (as discussed in this note). Since the cores are in the collector circuit of both drivers, each driver will act like a current source when driving the cores. A circuit schematic of the proposed driver is shown in Fig. 12. When the flip-flop voltages are larger in magnitude than the corresponding battery in the output stage of the drivers, a pulse of current is sent through the cores in the direction indicated in the diagram.

Signed Stanley Oken
Stanley Oken

Approved Donald J. Eckl
Donald J. Eckl

SO/er

Drawings

| | | |
|---|---|---|
| A-58306 | Fig. | 1A, 1B |
| A-58307 | " | 1C, 1D |
| A-58308 | " | 2 |
| A-58312 | " | 3 |
| A-58309 | " | 4A, 4B |
| C-58316 | " | 5 |
| C-58358 | " | 6 |
| A-58310 | " | 7 |
| A-58313 | " | 8 |
| A-58315 | " | 9, 10 |
| A-58314 | " | 11 |
| A-58311 | " | 12 |

## APPENDIX I

## CALCULATION OF COLLECTOR CURRENT RESPONSE FOR GROUNDED-EMITTER JUNCTION TRANSISTOR

The grounded-emitter equivalent circuit is shown in Fig. 1D. Assume that a load $R_L$ and a voltage source $V_{cc}$ are connected to the collector in order to make an operable circuit.

Let the driving pulse be a current step $I_b$ at the base. Since we are interested only in the variational output current, $V_{cc}$ is shorted out. Then, taking a Thevinen's equivalent circuit for the network to the left of terminals A - B, and for the dependent current source and collector resistance, we obtain the transient solution as:

$$I_c(s) = \frac{I_b(s)(\alpha_e r_c - r_e)}{[r_e + R_L + r_c(1 - \alpha_e)]} \tag{1}$$

with the substitutions:[10]

a) $I_b(s) = L[I_b(t)] = \frac{I_b}{s}$

b) $\alpha_e = \frac{\alpha_o}{1 + \tau s}$

equation (1) becomes:

$$I_c(s) = \frac{\frac{I_b}{(r_e + r_c + R_L)\tau}\left[(\alpha_o r_c - r_e) - r_e \tau s\right]}{s\left[s + \frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + R_L + r_c)\tau}\right]} \tag{2}$$

This transform can be simplified by the method of partial fractions to:

$$I_c(s) = + \frac{I_b}{(r_e + r_c + R_L)\tau}\left[\frac{K_o}{s} + \frac{K_1}{s + B}\right] \tag{3}$$

where $B = \frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + r_c + R_L)\tau}$

[10] L = Laplace transform

$$K_o = \frac{\left[\alpha_o r_c - r_e\right]\left[r_e + r_c + R_L\right]\tau}{\left[r_e + R_L + r_c (1 - \alpha_o)\right]}$$

$$K_1 = \frac{\left[(\alpha_o r_c - r_e) + r_e\tau\right]\left[\frac{r_e + R_L + r_c (1 - \alpha_o)}{(r_e + r_c + R_L)\tau}\right]}{\left[\frac{r_e + R_L + r_c (1 - \alpha_o)}{(r_e + r_c + R_L)\tau}\right]}$$

Substituting in the values of $K_o$ and $K_1$ into equation (3) and assuming $r_c \gg r_e + R_L$ (this is valid in the active region), we obtain as a final result:

$$I_c(s) = \frac{I_b \alpha_o}{(1 - \alpha_o)}\left\{1 - \left[1 + \frac{r_e (1 - \alpha_o)}{\alpha_o r_c}\right] e^{-\frac{(1 - \alpha_o)}{\tau} t}\right\}$$

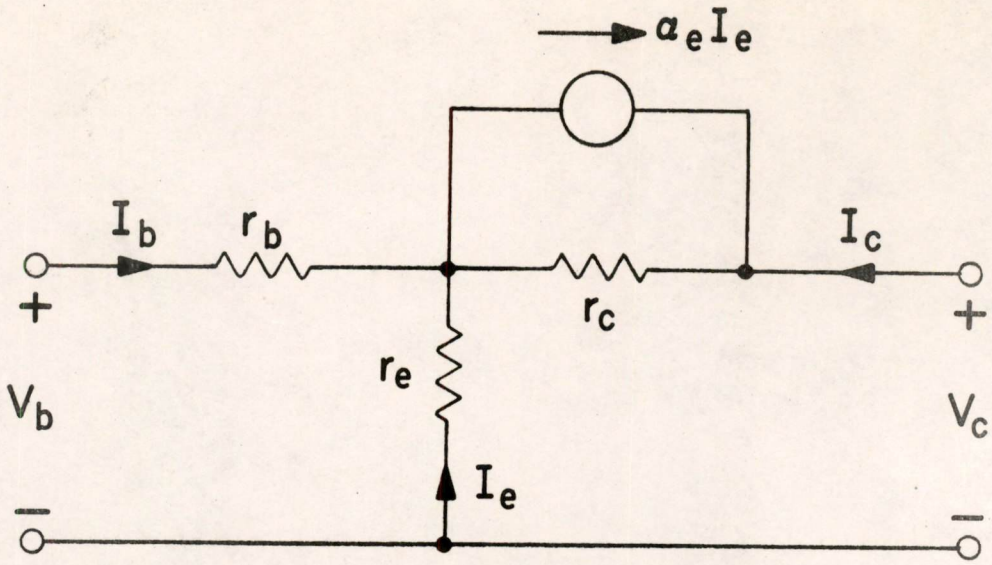



FIG. 1A
STANDARD EQUIVALENT CIRCUIT
FOR A TRANSISTOR IN THE
GROUNDED-EMITTER CONNECTION

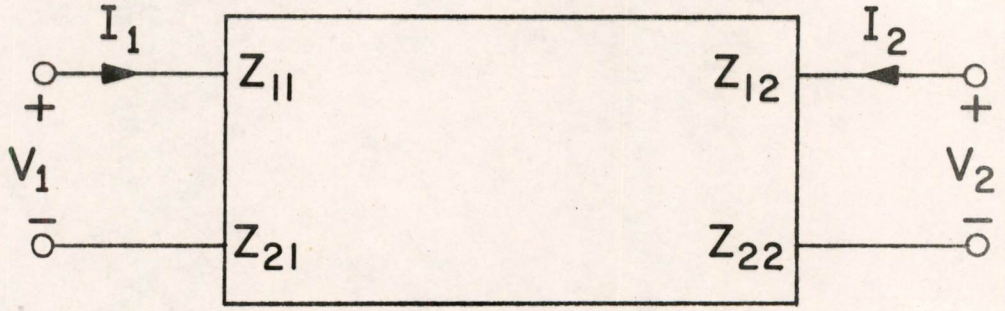



FIG. 1B
A GENERAL REPRESENTATION OF A
TWO TERMINAL PAIR NETWORK

A-58306

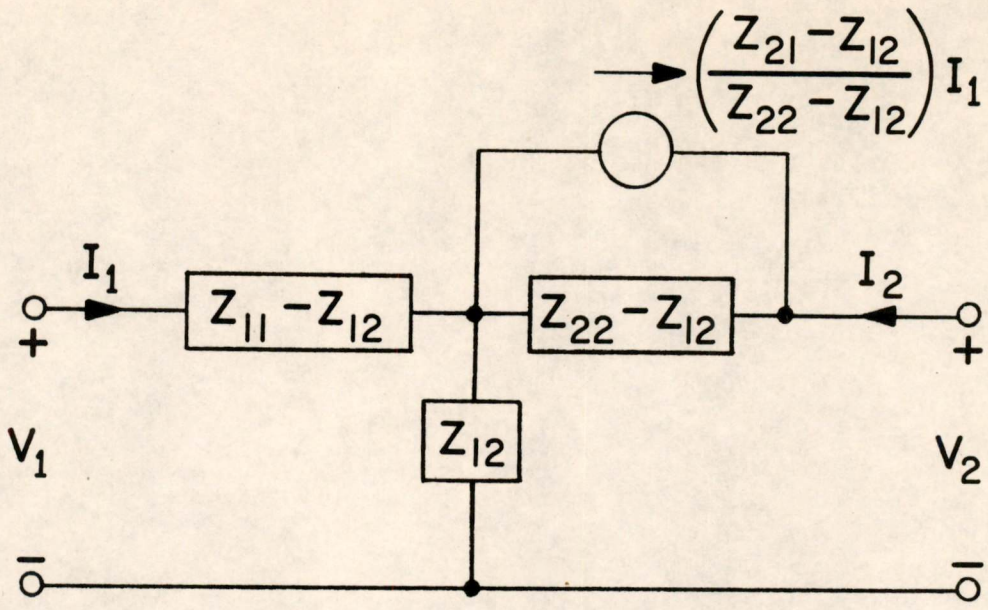



FIG. 18C

AN EQUIVALENT CIRCUIT
USEFUL FOR TRANSISTORS

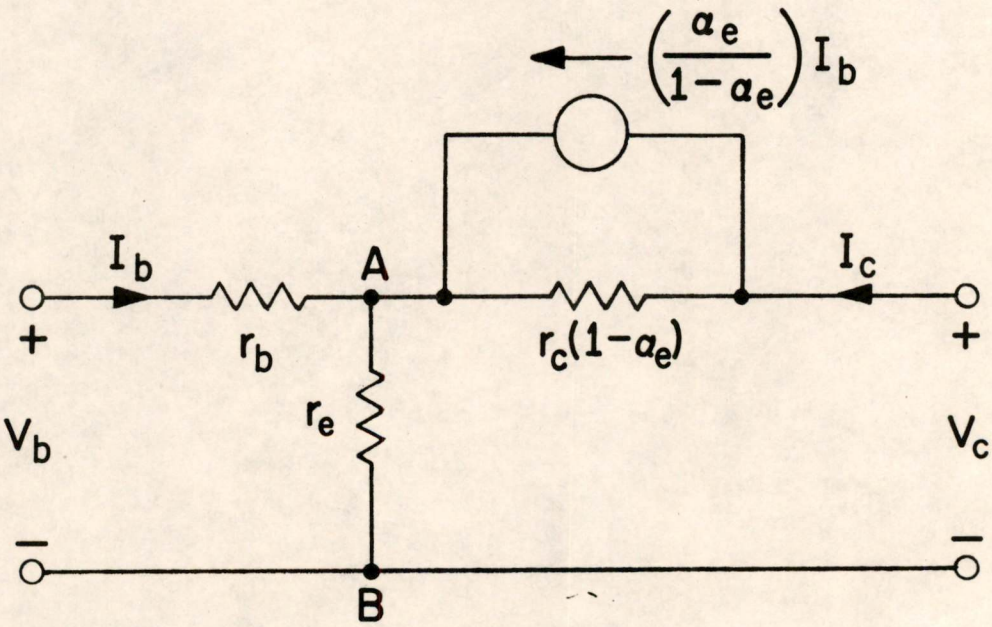



FIG. 18D

ANOTHER GROUNDED-EMITTER
EQUIVALENT CIRCUIT

A-58307

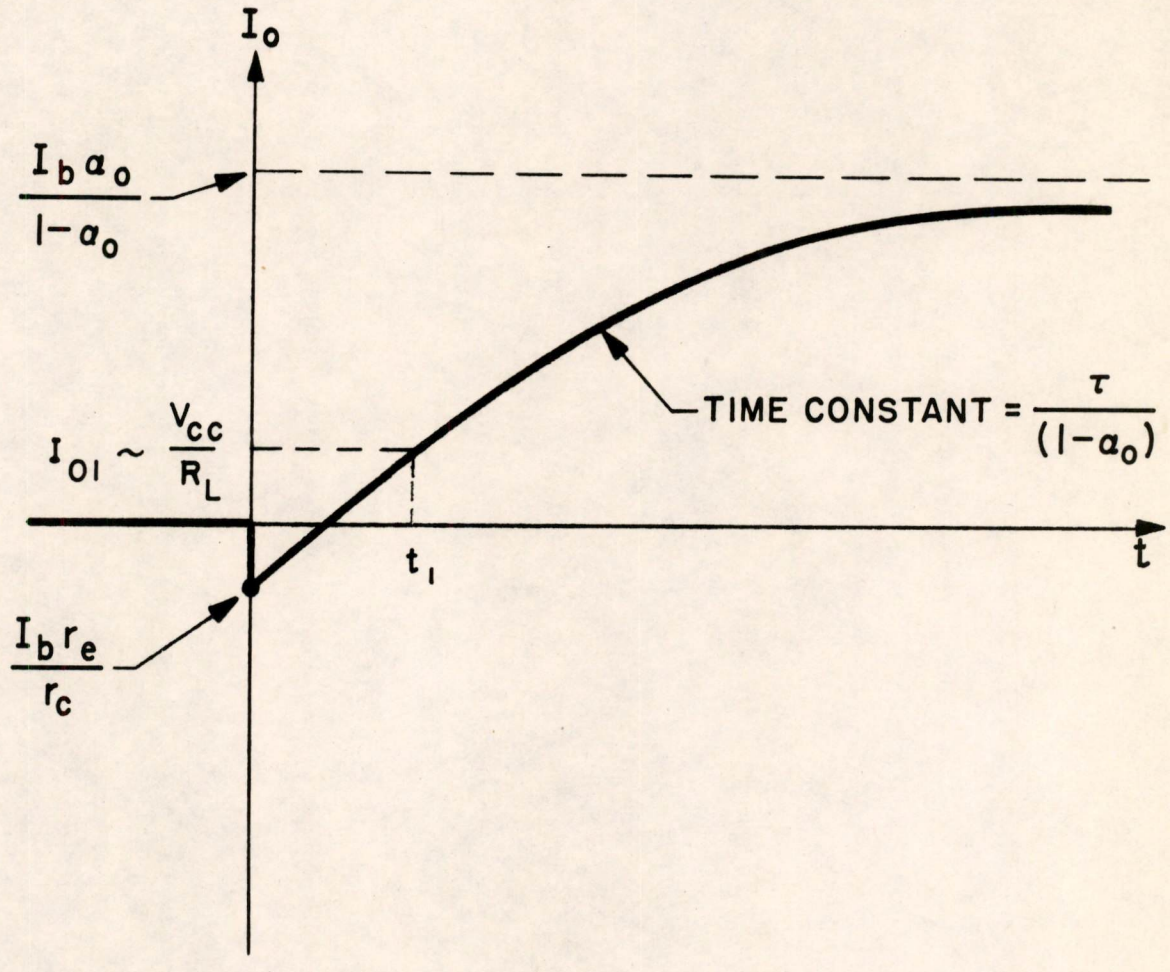
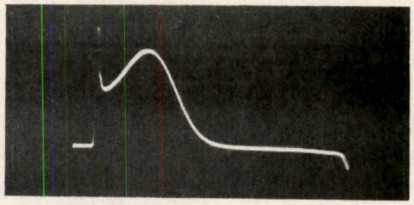
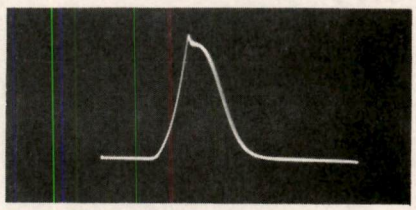



FIG. 19
THE OUTPUT CURRENT FROM
GROUNDED-EMITTER CONNECTION

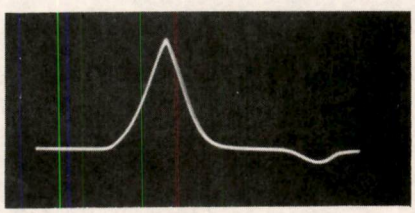
A-58308-1
MN



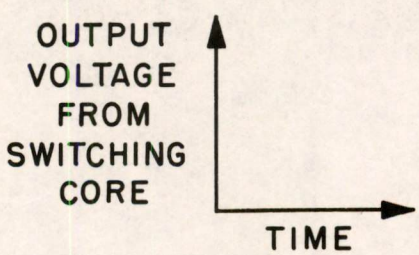
RISE TIME = 0.18 μsec
OF
DRIVING PULSE



RISE TIME = 1.0 μsec
OF
DRIVING PULSE



RISE TIME = 1.6 μsec
OF
DRIVING PULSE




TEN TURN SENSING WINDING
0.2 AMPERE TURNS

SCALES:
TIME: 1.0 μsec / div
VOLT: 0.17 V / div

FIG. 20

THE EFFECT OF RISE TIME OF CURRENT PULSE ON OUTPUT FROM MAGNETIC CORES

A-58312

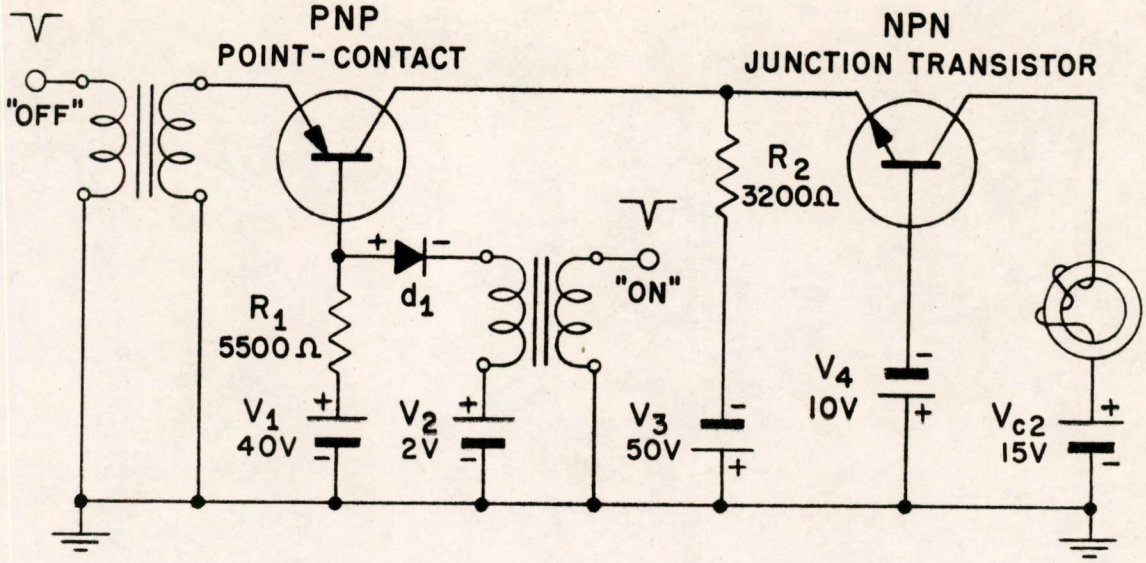



FIG. 4A

SCHEMATIC DIAGRAM OF CORE DRIVER

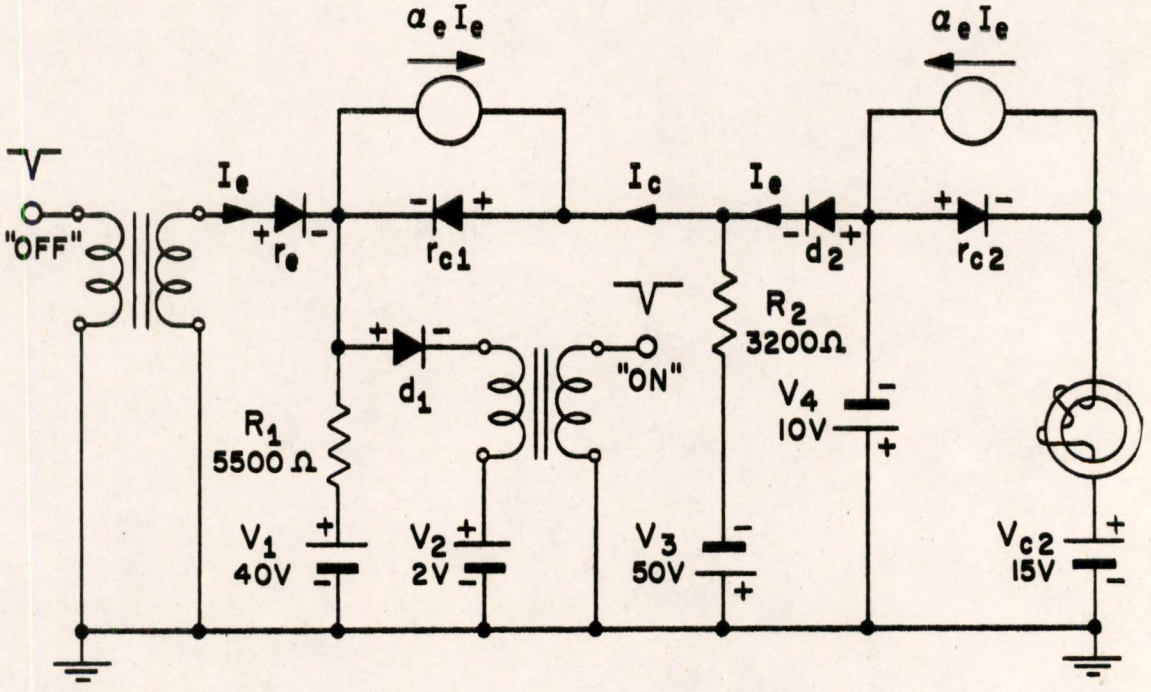
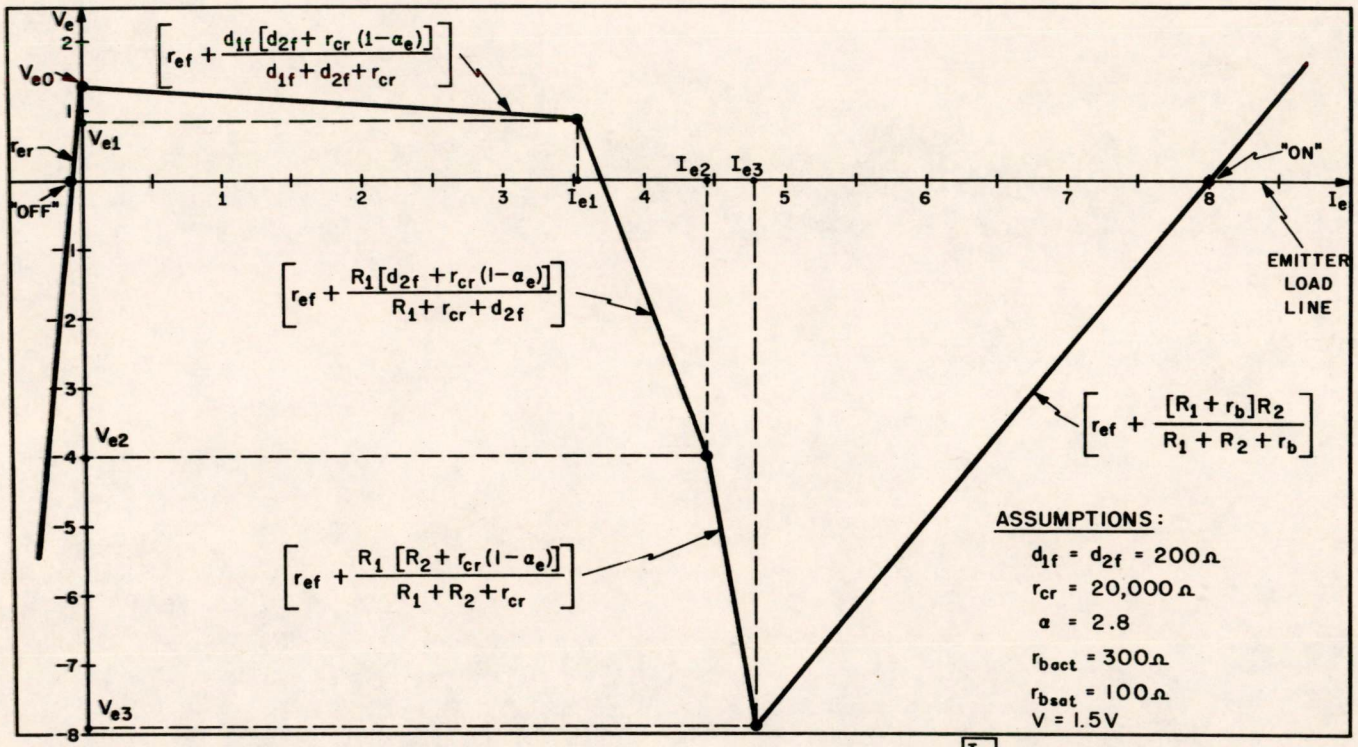



FIG. 4B

EQUIVALENT CIRCUIT OF CORE DRIVER

C-58316 - 1
MN




$V_e$

$$V_{e0} = \frac{V_2(r_{cr}+d_{2f}) - V_4 d_{1f}}{d_{1f}+d_{2f}+r_{cr}} = 1.4\ V$$

$$V_{e1} = I_{e1}\left[r_{ef} + \frac{d_{1f}[d_{2f}+r_{cr}(1-\alpha_e)]}{d_{1f}+d_{2f}+r_{cr}}\right] + V_{e0} = 0.8\ V$$

$$V_{e2} = I_{e2}\left[r_{ef} + \frac{R_1[R_2+r_{cr}(1-\alpha_e)]}{R_1+R_2+r_{cr}}\right] + \left[\frac{V_1[R_2+r_{cr}] - V_3R_1}{R_1+R_2+r_{cr}}\right] = -4V$$

$$V_{e3} = I_{e3}\left[r_{ef} + \frac{R_1R_2}{R_1+R_2}\right] + \frac{V_1R_2}{R_1+R_2} - \frac{V_3R_1}{R_1+R_2} = -7.9V$$

$$V_{e"ON"} = 0V$$

$I_e$

$$I_{e0} = 0\ ma$$

$$I_{e1} = \frac{\left[\frac{V_1}{R_1} - \frac{V_4}{d_{2f}+r_{cr}} - \frac{V_2[R_1+r_{cr}+d_{2f}]}{R_1[r_{cr}+d_{2f}]}\right]}{\left[\frac{r_{cr}[\alpha_e-1]-d_{2f}}{r_{cr}+d_{2f}}\right]} = 3.6\ ma$$

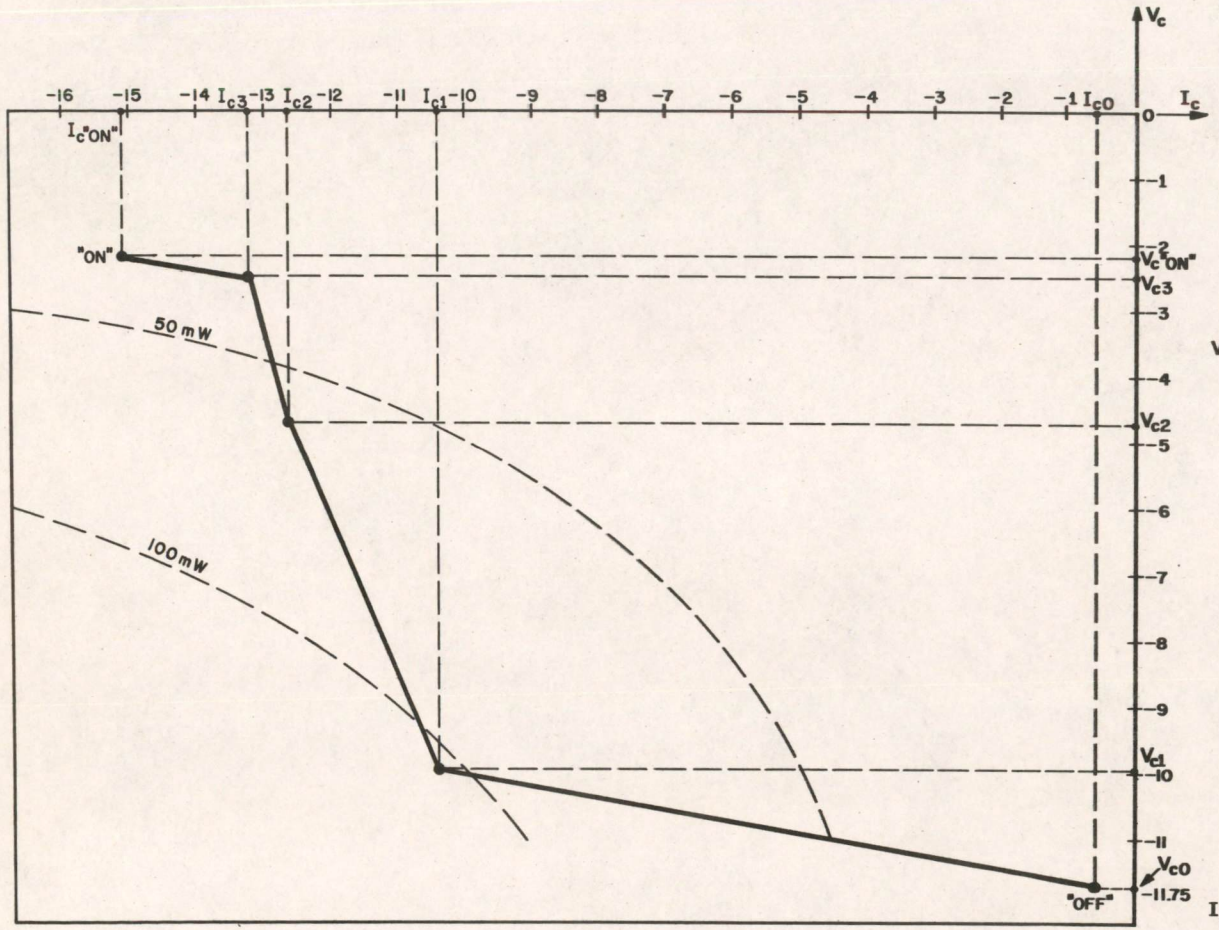
$$I_{e2} = \frac{\left[\frac{V_3}{R_2} - \frac{[R_1+r_{cr}+R_2]V_4}{R_2[R_1+r_{cr}]} - \frac{V_1}{R_1+r_{cr}}\right]}{\left[\frac{R_1+\alpha_e r_{cr}}{R_1+r_{cr}}\right]} = 4.4\ ma$$

$$I_{e3} = \frac{V_1+V_3}{[R_2\alpha_e + R_1[\alpha_e-1]]} = 4.8\ ma$$

$$I_{e"ON"} = \frac{[V_3+V][R_1+r_b] - V_1R_2}{r_{ef}[R_1+R_2+r_b] + [R_1+r_b]R_2} = 8.1\ ma$$

FIG. 23
EMITTER "N" CURVE FOR FLIP-FLOP

C-58358




$$V_c$$

$$V_{c0} = I_{c0} r_{cr} = -\frac{[V_2 + V_4] r_{cr}}{d_{1f} + d_{2f} + r_{cr}} = -11.7 \text{ V}$$

$$V_{c1} = -[V_2 + V_4 + I_{c1} d_{2f}] = -9.9 \text{ V}$$

$$V_{c2} = -[V_4 + V_1 + I_{e2} R_1 + I_{c2} R_1] = -4.6 \text{ V}$$

$$V_{c3} = r_b [I_{e3} + I_{c3}] = -2.5 \text{ V}$$

$$V_{c"ON"} = -[V - [I_{e"ON"} + I_{c"ON"}]\, r_b] = -2.2 \text{ V}$$

$$I_c$$

$$I_{c0} = -\frac{[V_2 + V_4]}{d_{1f} + d_{2f} + r_{cr}} = -0.6 \text{ ma}$$

$$I_{c1} = -\frac{[V_2 + V_4 + \alpha_e I_{e1} r_{cr}]}{r_{cr} + d_{2f}} = -10.4 \text{ ma}$$

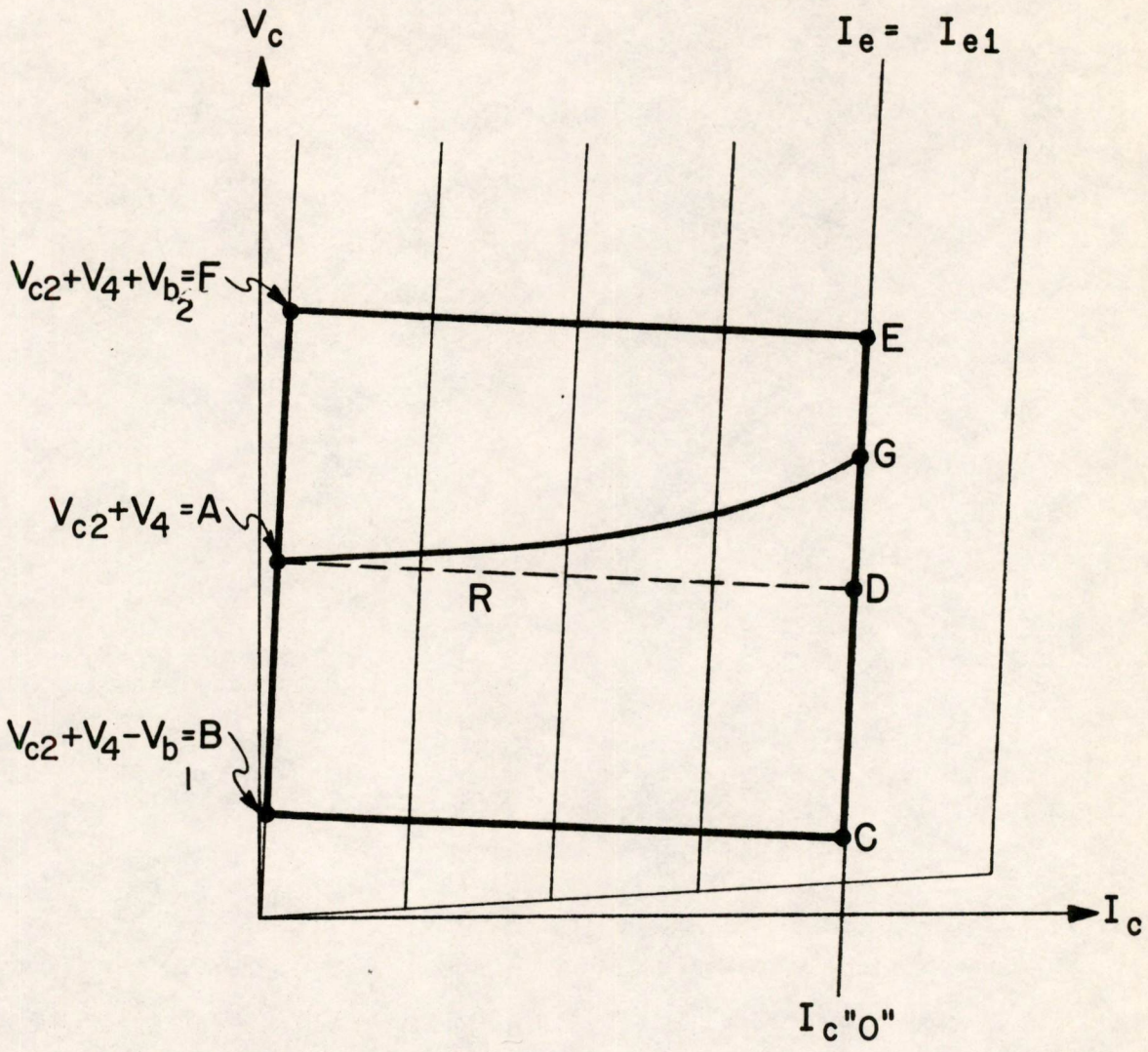
$$I_{c2} = -\frac{[V_4 + V_1 + I_{e2}[R_1 + \alpha_e r_{cr}]]}{R_1 + r_{cr}} = -12.7 \text{ ma}$$

$$I_{c3} = -\frac{[V_3 + V_1 + I_{e3}[R_1 + r_b]]}{R_1 + R_2 + r_b} = -13.3 \text{ ma}$$

$$I_{c"ON"} = -\left[\frac{V_1 + V_3 + I_{e"ON"}[R_1 + r_b] - V}{R_1 + R_2 + r_b}\right] = -15.3 \text{ ma}$$

FIG. 6

$V_c - I_c$ CHARACTERISTIC FOR FLIP-FLOP




$V_{b_1}$ = BACK VOLTAGE ACROSS THE CORES

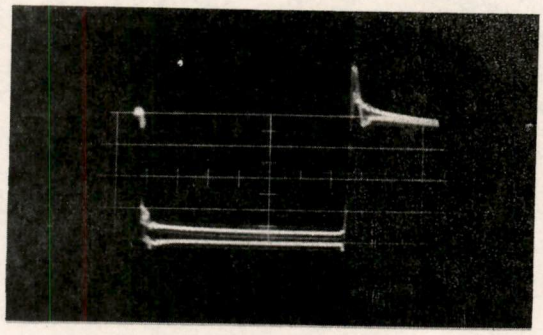
R = RESISTANCE OF WIRE

$V_{b_2}$ = BACK VOLTAGE ON CORES MAINLY DUE TO WINDING INDUCTANCE

FIG. 25

THE IDEAL $V_c - I_c$ OPERATING CHARACTERISTIC FOR THE OUTPUT STAGE OF CORE DRIVER

A-58310-1
MN



SCALES:

TIME = 1.0 usec / div

CURRENT = 3.0 ma / div

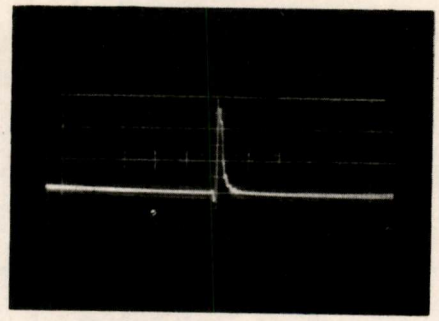
LARGER CURVE $V_{cc}$ = 25 VOLTS

SMALLER CURVE $V_{cc}$ = 4 VOLTS

FIG. 26

CHANGE IN CURRENT OUTPUT WITH THE COLLECTOR VOLTAGE OF THE OUTPUT STAGE

A-58313 m-1



SCALES:

TIME = 1.0 μsec / div

VOLTS = 0.05 V / div

SENSING WINDING = 8 TURNS

FIG. 27

OUTPUT FROM CORE WITH "$I_m$" / 2 CURRENT INPUT

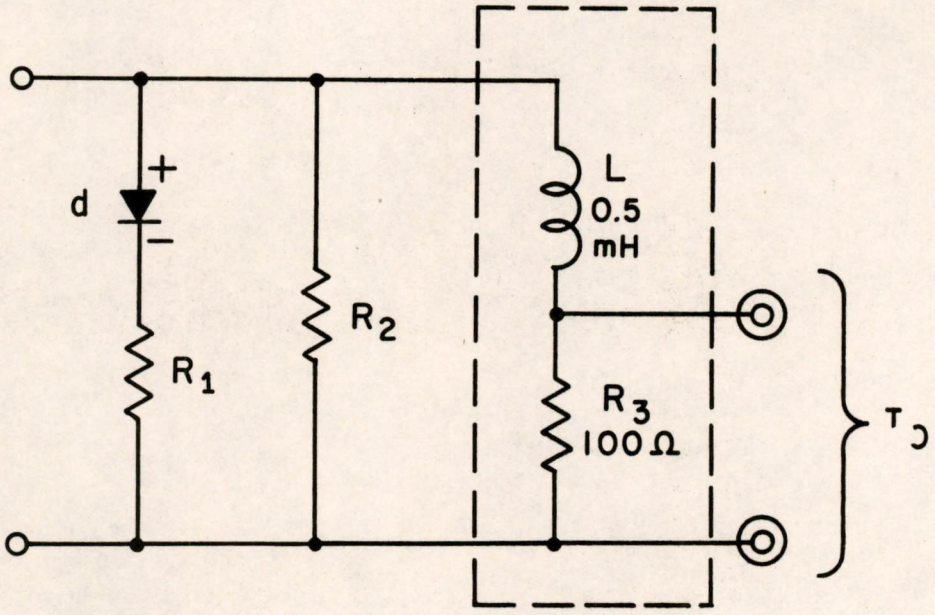
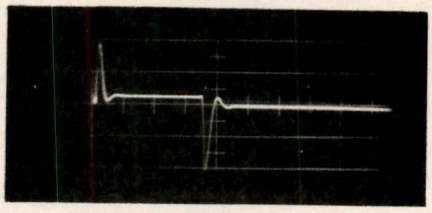
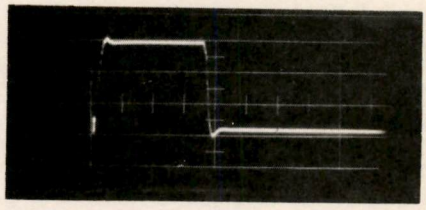
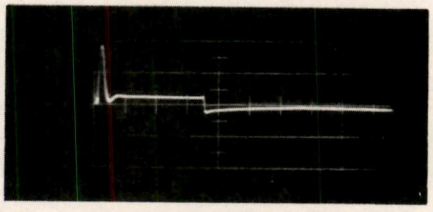
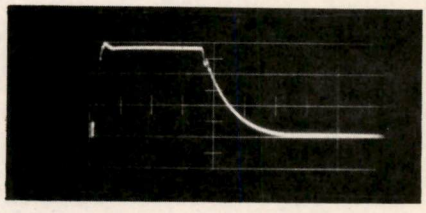
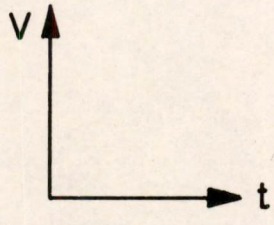



FIG. 28

AN EQUIVALENT CIRCUIT FOR THE CORES

A-58315-1

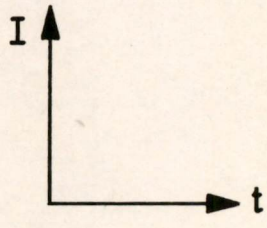
| VOLTAGE OUTPUT | PARAMETERS | CURRENT OUTPUT |
|---|---|---|
|  | DIODE = OUT<br>$R_1$ = OUT<br>$R_2$ = 2600 Ω |  |
|  | DIODE = IN<br>$R_1$ = OUT<br>$R_2$ = 2600 Ω |  |




SCALES :

VOLTS = 8 V/ div

TIME = 2.0 μsec/ div




SCALES :

CURRENT = 4.4 ma/ div

TIME = 2.0 μsec / div

FIG. 29

OUTPUT FROM DRIVER WITH EQUIVALENT "MEMORY PLANE" LOAD

A-58314-1

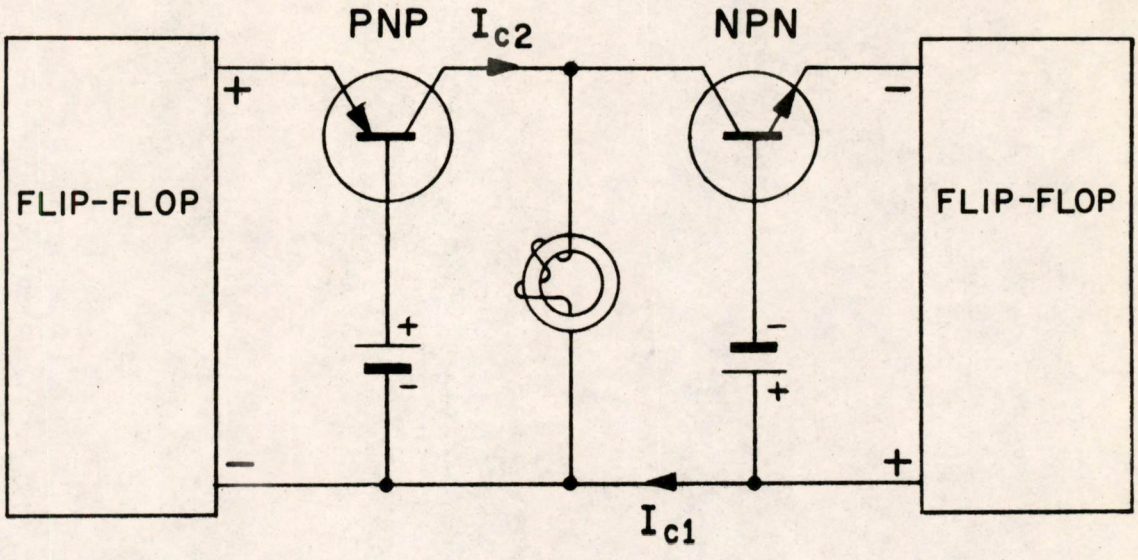



FIG. 12
A SCHEMATIC DIAGRAM OF THE
PROPOSED READ-WRITE DRIVER

A-58311

K. H. Olsen

INTERNAL DISTRIBUTION ONLY



Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: TRIP REPORT: Trip to IRE, Bell Telephone Laboratories, Glenco, Naval Ordnance Laboratory, Professor Pulvari, Cavitron, Mullard, RCA, and NSA, March 23-31, 1954.

To: D. R. Brown

From: Dudley A. Buck

Date: April 13, 1954

Abstract: A trip was made to various laboratories investigating ferroelectric and ferromagnetic materials for information storage and switching. Information is listed by topics.

## Ferroelectrics

Walter Merz of Bell Telephone Laboratories has made important contributions to an understanding of the switching mechanism in ferroelectric single crystals of barium titanate. He calculates that 180° domain walls in ferroelectrics are much narrower than in ferromagnetic materials--of the order of two or three lattice constants rather than several hundred. This is due to the small exchange energy (the equivalent of which is dipole-dipole interaction in ferroelectrics) and much higher anisotropy. Domain-wall thickness is of the order of the square root of the exchange parameter divided by the anisotropy. For this reason, 180° walls do not tend to move broadside through the material. Large numbers of dagger-shaped spikes of reverse polarization pierce the ferroelectric from electrode to electrode during switching. Formation rate of these domains of reverse polarization is a function of the temperature and applied electric field. At room temperature, very low fields applied for long periods of time eventually switch the polarization. This may mean that large numbers of half-amplitude disturb pulses will eventually switch a ferroelectric.

I saw a new batch of barium titanate crystals being removed from the growth furnace. Excess fluoride flux is poured off immediately so that its solidification does not strain the new crystals. These crystals grow in thin plates, twinned, and in a background of little cubic crystals, which modification also grows at the temperature they use but at a slower rate.

Reid Anderson of Bell Labs. has several 16 x 16 ferroelectric storage arrays in toggle-switch operation. Switching times are slow because of high-resistance evaporated electrodes. On the present matrices, the row and column stripes are 4 mils wide. The sheets are 2 mils thick and an electric polarizing process is used to make them essentially c-domain plates. Pulvari says they polish their plates down to a uniform 2 mils.

Lee Johnson of Glenco has performed an experiment in which he switches a ferroelectric by dipping it in a hot bath, above the Curie temperature. Switching time of the order of seconds is exhibited and with a double-hump switching voltage at the condenser terminals. As the temperature of the bath is increased, the second hump gets larger and comes in closer to the origin. This experiment may shed some light on the switching mechanism proposed by Merz. I put the two men in touch with one another.

Pulvari has a new theory to account for the slow velocity of switching in ferroelectrics. Computed velocity, electrode to electrode, is about 300 meters per second, slower than even acoustical waves in the medium. His theory treats the statistics of the titanium atom jumping from one stable point to another in the lattice at any given temperature. Reams of numerical analysis have yielded velocities of the correct order and also have predicted coercive forces of the observed magnitude. Pulvari has a 10 x 10 matrix of individually selected condensers made from recrystallized ceramic sheets. His apparatus steps through the matrix at relay speeds, reading and writing in each individual cell. He plans to leave this development for the present and continue work on his ferroelectric-tape recorder.

Metallic-Core Fabrication

I visited the Naval Ordnance Laboratory, White Oaks, Maryland, to see the pulse-test equipment of Van Sant and Burnside. They are testing magnetic cores for magnetic-amplifier and switching circuits by observing current waveforms due to an applied voltage step. The step is generated by a hand-operated mercury relay and a battery, and measurements are made from scope photographs.

At the same Laboratory, I saw the two rolling mills, the Rohn and the Sendzimir, for making ultra-thin metallic tapes; vacuum melting and casting furnaces; and a hot-rolling mil. In one place, they have all the necessary equipment for compounding, melting, casting, rolling, wrapping, and annealing magnetic cores.

I had a very brief progress report on the work of the Corona group. They have been able to eliminate hydrogen annealing of their evaporated mo-Permalloy cores by using a heated substrate. Effectively, they are annealing as they deposit the core.

I found out that the electroplated-core project at Battelle Memorial Foundation is sponsored by the Michigan Bumper Corporation. RCA has volunteered to evaluate the square-loop material they are making.

Ultrasonic Machine Tool

We have been working with the Raytheon Ultrasonic Machine Tool for sometime on a loan basis and are now considering the purchase of one. I made a comparison shopping visit to Cavitron and International Electric

(Mullard Distributors). Mullard has no machine for cutting and will not quote on one. Cavitron has a machine equal in every respect to the Raytheon machine but somewhat more expensive. I made a sample cut with the Cavitron equipment. It will satisfy our requirements.

Signed Dudley A. Buck
Dudley A. Buck

Approved DRB
David R. Brown

DAB/jk

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