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B-191

Digital Computer Laboratory
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Cambridge, Massachusetts

SUBJECT: ENERGY DISSIPATION IN SQUARE LOOP FERROMAGNETIC MATERIALS WITH SPECIFIC APPLICATION TO SWITCH CORES

To: David R. Brown

From: N. Menyuk

Date: May 12, 1953

Abstract: A determination is made of the energy dissipation in a square loop ferromagnetic material due to domain wall motion. These energy losses are separated into three terms, representing the relaxation loss, the eddy current loss, and the hysteresis loss. The order of magnitude of the energy loss per cycle is found for an F-262 ferrite and a 140 wrap 4-79 molybdenum permalloy core. From the values thus determined, the power loss of these cores is calculated for a frequency of 100 kilocycles, assuming a semi-infinite step function input. The calculated order of magnitude is in agreement with the experimental results for a ferrite; no data is available for the metallic cores. The results indicate that external cooling will be needed for switch core matrices operated at this frequency. A number of reasons are given to show that metallic cores should be preferable to ferrites as switch cores.

A high speed multiposition switch can be made using ferromagnetic cores, ¹, ², and a number of these switch-core matrices are operating successfully at the present time. However, J. Mitchell has noted that when these cores are operated at frequencies in excess of 5 kilocycles they heat up and, with increasing frequency, soon lose their ability to operate as a switching device. This is not surprising since the successful operation of a ferromagnetic toroid is limited by the shape of the hysteresis loop (see reference 1) and this loop is a function of the temperature.

1. Olsen, K. H., "A Magnetic-Matrix Switch and its Incorporation into a Coincident Current Memory," Digital Computer Laboratory Report R-211 (1952).
2. Katz, A. and Guditz, E. A., "Switch Core Analysis, I" Digital Computer Laboratory, Engineering Note #500 (1952).

The heating problem is a serious one since the switch cores, when used in a computer, will operate at a frequency of the order of 100 kilocycles. It is therefore important that the factors which contribute to the temperature rise be understood. This note investigates the energy dissipated by a core on reversing its magnetization and, on the basis of the results obtained, determines the power loss at 100 kilocycles.

Energy Losses

In the calculations which follow the hysteresis loop is assumed to be square and the input signal is assumed to be a sequence of semi-infinite step functions. This corresponds to a cyclic input of the form shown in figure 1.

Upon reversing the magnetization of a ferromagnetic material the equation of motion of a domain wall is given approximately by the equation³

$$\beta \vec{v} = 2(\vec{H} - \vec{H}_0) \cdot \vec{I}_s \quad (1)$$

wherein β is the damping factor, \vec{v} the velocity of the domain wall, \vec{H} the applied field, \vec{H}_0 the threshold field, which is closely related to the coercive field, and \vec{I}_s is the saturation magnetization. The damping factor β is the sum of two factors

$$\beta = \beta_e + \beta_r \quad (2)$$

where β_e is the damping factor due to eddy current effects and β_r is the damping factor due to relaxation effects. Equation 1 can therefore be rewritten as

$$\beta_e \vec{v} + \beta_r \vec{v} + 2\vec{H}_0 \cdot \vec{I}_s = 2\vec{H} \cdot \vec{I}_s \quad (3)$$

In equation 3

- $2\vec{H} \cdot \vec{I}_s$ is the energy/unit volume supplied by external field \vec{H} .
- $\beta_e \vec{v}$ is the energy/unit volume dissipated as eddy current losses.
- $\beta_r \vec{v}$ is the energy/unit volume dissipated as relaxation losses.
- $2\vec{H}_0 \cdot \vec{I}_s$ is the energy/unit volume dissipated as hysteresis losses.

3. Goodenough, J. B. and Menyuk, N., "Nucleation of Domains of Reverse Magnetization and Switching Characteristics of Magnetic Materials," Digital Computer Laboratory, Engineering Note #532 (1953).

Eddy Current Loss

The value of β_e , as given in reference 3, page 26, is

$$\beta_e = \frac{64\pi^2 I_s^2}{\rho_e c^2 \langle \cos\theta \rangle} \langle r \rangle \ln \frac{R_m}{\langle r \rangle} \quad (4)$$

where R_m is half the thickness of the ferromagnetic material, ρ_e is the resistivity of the material, $\langle r \rangle$ is the effective value of the radius of the base of a cone of reverse magnetization as seen on a plane through the material, and $\langle \cos\theta \rangle$ is the effective value of the cosine of the angle between the normal to this plane and the direction of magnetization within the domain (see figure 2). The wall velocity v and $\frac{d\langle r \rangle}{dt}$ are related by

$$v = \frac{1}{\langle \cos\theta \rangle} \frac{d\langle r \rangle}{dt}$$

therefore,

$$\beta_e v = \frac{\beta_e}{\langle \cos\theta \rangle} \frac{d\langle r \rangle}{dt} = \text{Eddy current loss} = \frac{64\pi^2 I_s^2}{\rho_e c^2 \langle \cos^2\theta \rangle} \langle r \rangle \frac{d\langle r \rangle}{dt} \ln \frac{R_m}{\langle r \rangle} \quad (5)$$

The switching time τ is the time required for the core to completely reverse its magnetization direction, and in this time the domain wall is assumed to travel a distance ρ . On integrating equation 5 over the proper limits one finds

$$\text{Eddy current loss} = \begin{cases} \frac{16\pi^2 I_s^2 R_m^2}{\rho_e c^2 \langle \cos^2\theta \rangle} & \text{for } R_m \leq \rho \langle \cos\theta_2 \rangle \quad (6a) \\ \frac{16\pi^2 I_s^2 \rho^2}{\rho_e c^2} \left\{ 2 \ln \frac{R_m}{\rho \langle \cos\theta \rangle} + 1 \right\} & \text{for } R_m > \rho \langle \cos\theta_2 \rangle \quad (6b) \end{cases}$$

The eddy current loss in ferrites is negligible because of the high resistivity of these materials. In metallic cores this is no longer the case. For thin ribbon metallic cores of the dimensions used in this laboratory (1/8 mil and 1/4 mil) $R_m < \rho \langle \cos\theta_2 \rangle$ and equation 6a is applicable.

Relaxation Loss

The value of β_r given in reference 3, page 25, is

$$\beta_r = \frac{2 I_s^2 \Delta}{(\Delta^2 + I_s^2 \tau^2)} \sqrt{\frac{K}{A}} \quad (7)$$

where Δ is the relaxation frequency, γ the magneto-mechanical ratio, K the anisotropy constant, and A the exchange constant. Therefore,

$$\text{Relaxation Loss} = \frac{2I_s^2 \Delta}{(\Delta^2 + I_s^2 \gamma^2) \langle \cos \theta \rangle} \sqrt{\frac{K}{A}} \frac{d\langle r \rangle}{dt} \quad (8)$$

and on integrating one finds

$$\text{Relaxation Loss} = \frac{2I_s^2 \Delta \rho}{\tau (\Delta^2 + I_s^2 \gamma^2)} \sqrt{\frac{K}{A}} \quad (9)$$

Hysteresis Loss

The hysteresis loss, as given earlier, is $2H_0 \cdot I_s$ or $2H_0 I_s \langle \cos \theta \rangle$. H_0 is the value of the magnetic field at which domain wall motion ceases. It is obtained experimentally as described in reference 3, page 28. This value is based on the assumption of a square hysteresis loop.

Total Loss

The total energy loss per unit volume in the course of a single magnetization reversal is thus

$$\frac{E}{V} = \frac{16\pi^2 I_s^2 R_m^2}{\tau \rho_s c^2 \langle \cos^2 \theta \rangle} + \frac{2I_s^2 \Delta \rho}{\tau (\Delta^2 + I_s^2 \gamma^2)} \sqrt{\frac{K}{A}} + 2H_0 I_s \langle \cos \theta \rangle \quad (10)$$

where equation 6a has been used for the eddy current loss. Since a full cycle represents two reversals, the energy loss per cycle will be twice the value given above.

Comparison with Experiment

Ferrite Core

At present, the General Ceramic ferrite core MF-1312B is being used in switch core matrices. Many of the factors which appear in equation 10 are unknown for this material. However, reasonable values can be obtained from a knowledge of these values for similar materials, and the order of magnitude obtained can then be checked with experimental results. In ferrites the eddy current effect is neglected.

The ferrite MF-1312B has $I_s \approx 155$ gauss and $H_0 \approx 0.5$ oersteds. The distance $\rho \approx 5 \times 10^{-3}$ cm, $\langle \cos \theta \rangle \approx 1$, $\gamma = 2 \times 10^7$ (gauss-sec) $^{-1}$. The relaxation frequency $\Delta \approx 10^8$ sec $^{-1}$ and $\sqrt{\frac{K}{A}} \approx 10^5$ cm $^{-1}$. The switching time τ is taken as 1.1×10^{-6} seconds, which is the experimental value. Substituting these values,

$$\text{Relaxation loss} = \frac{4I_s^2 \Lambda \rho}{\tau (\Lambda^2 + I_s^2 \rho^2)} \sqrt{\frac{K}{A}} \approx 450 \text{ ergs/cm}^3/\text{cycle}$$

$$\text{Hysteresis loss} = 4H_0 I_s \langle \cos \theta \rangle \approx 300 \text{ ergs/cm}^3/\text{cycle}.$$

The volume of these F-262 cores is 0.145 cm^3 . The relaxation loss/core/cycle is therefore ≈ 62 ergs and the hysteresis loss/core/cycle is 44 ergs.

The experimental value of the hysteresis energy loss, as obtained from a measurement of the static hysteresis loop area, was found to be 75 ergs. The discrepancy between the calculated and experimental results can arise from our assumption of a perfectly square hysteresis loop. Actually, the loop is only approximately square, and increases in size with increasing input. Also, the experimental value of H_0 was taken from a single core, and it was not one of the cores used in obtaining the energy loss data. Since H_0 can vary by as much as 20% between supposedly similar cores, this leads to a large uncertainty in the calculated result.

The total energy loss per core per cycle has been found experimentally to be 162 ergs as compared with our calculated value of approximately 106 ergs. Thus the calculated relaxation loss of 62 ergs compares quite well with the experimental value of 87 ergs.

Metallic Core

A 1/4 mil 140 wrap 4-79 molybdenum permalloy core has recently been obtained by A. Katz for possible use as a switch core. The parameter constants, as given on page 29 of reference 3 are: $I_s \approx 700$ gauss, $\rho_s = 6 \times 10^{-17}$ asu-cm, $\sqrt{\frac{K}{A}} = 1.05 \text{ cm}^{-1}$, $\Lambda = 2 \times 10^8 \text{ sec}^{-1}$, $\rho = 5 \times 10^{-3}$, $\langle \cos \theta \rangle \approx 1$, and $\gamma = 2 \times 10^7 (\text{gauss-sec})^{-1}$. Since this is 1/4 mil material, $R_m = 3.2 \times 10^{-4} \text{ cm}$, and the switching time τ is again taken as $1.1 \times 10^{-6} \text{ sec}$. The switching time can be chosen arbitrarily as it is dependent upon the amplitude of the applied field. This value was chosen in order to obtain results which can be compared meaningfully with the results obtained for the ferrite MF-1312B. H_0 is 0.14 oersteds.

$$\text{Eddy Current loss} = \frac{32\pi^2 I_s^2 R_m^2}{\tau \rho_s c^2 \langle \cos \theta \rangle} \approx 36 \text{ ergs/cm}^2/\text{cycle}$$

$$\text{Relaxation loss} = \frac{4I_s^2 \Lambda \rho}{\tau (\Lambda^2 + I_s^2 \rho^2)} \sqrt{\frac{K}{A}} \approx 900 \text{ ergs/cm}^3/\text{cycle}$$

$$\text{Hysteresis loss} = 4H_0I_0\langle\cos\theta\rangle \approx 392 \text{ ergs/cm}^3/\text{cycle}$$

The total volume of this core is 0.13 cm³. The calculated energy loss per core per cycle is therefore approximately 170 ergs.

No experimental values of energy losses are available as yet for comparison purposes.

Conclusions

The magnitude of the energy losses discussed above leads to a large power dissipation at high frequencies. At 100,000 cycles/second the calculated power loss for the MF-1326B and the metallic-ribbon core is about 1.1 and 1.7 watts per core respectively. Furthermore, in view of the parameters involved, it is highly unlikely that these figures will be decreased in order of magnitude. An external cooling system will therefore be needed in conjunction with a switch core matrix operating at high frequencies. Within this limitation, let us compare the relative merits of the metallic and ferrite cores as switch-matrix components.

1. Hysteresis loop - The hysteresis loop of the MF-1326B ferrite core is less square than that of the 140 wrap 1/4 mil 4-79 molybdenum permalloy core, as shown in figure 3. The pulse characteristics of the metallic core should therefore be preferable to that of the ferrite and should reduce the need for any "tailoring" of the input signal with its resultant complication of the electronic circuit.
2. Heating - As shown above, the metallic core dissipates 1.7 watts at 100kc. as compared to 1.1 watts for the ferrite core. However, in view of the assumptions made in these calculations, the difference is not necessarily significant. Furthermore, since the saturation magnetization is almost five times as great in the metallic core as in the ferrite, the output per metallic core should be considerably greater than the output per ferrite core. At present, seven ferrite cores are needed for each switch-matrix component to obtain the desired output. Since fewer metallic cores will be needed, the heat generated per component will probably be lower using metallic cores.
3. Surface Area-Volume Ratio - For efficient cooling it is desirable to have as large a surface area to volume ratio as possible. This ratio is rather poor in both the F-262 size ferrite core now in use and the 140 wrap metallic core which has been received. This ratio can be increased in the metallic core by widening the core and decreasing the number of wraps, maintaining the same

volume. It would probably be more difficult to effect a large improvement in this ratio with a ferrite.

4. Temperature Sensitivity - Since molybdenum permalloy has a higher Curie temperature ($\sim 460^{\circ}\text{C}.$) than the ferrites ($\sim 300^{\circ}\text{C}.$), the metallic core hysteresis loops should be somewhat less sensitive to small temperature changes in the vicinity of room temperature than the ferrites.

Applied Field Value - The $1/4$ mil molybdenum permalloy core has a smaller value of H_0 than the MF-1326B ferrite. In addition, the switching coefficient S_w , where $S_w = (H-H_0)\tau$, is also smaller for the metallic core. The figures are: $S_w = 6.4 \times 10^{-7}$ oersted-second for $1/4$ mil 4-79 molybdenum permalloy, and $S_w = 10.2 \times 10^{-7}$ oersted-second for MF-1312B.

A metallic switch-core matrix designed to operate at the same speed as the ferrite switch therefore requires a smaller magnetic field. Thus, when using metallic cores, a smaller current amplitude will be required of the electronic equipment used in conjunction with the matrix. This may permit a simplification of the circuitry.

Recommendation

The above considerations all indicate that the metallic switch core matrix is preferable to a ferritic switch core matrix. Future experimentation along this direction should therefore be emphasized. In particular, wider cores should be used to increase the surface area.

Acknowledgment

The writer wishes to thank A. Katz for bringing the problem to his attention and for supplying all the experimental information pertaining to switch cores. Useful discussions pertaining to this problem were held with J. B. Goodenough, P. K. Baltzer and A. Katz.

Signed

Norman Menyuk
N. Menyuk

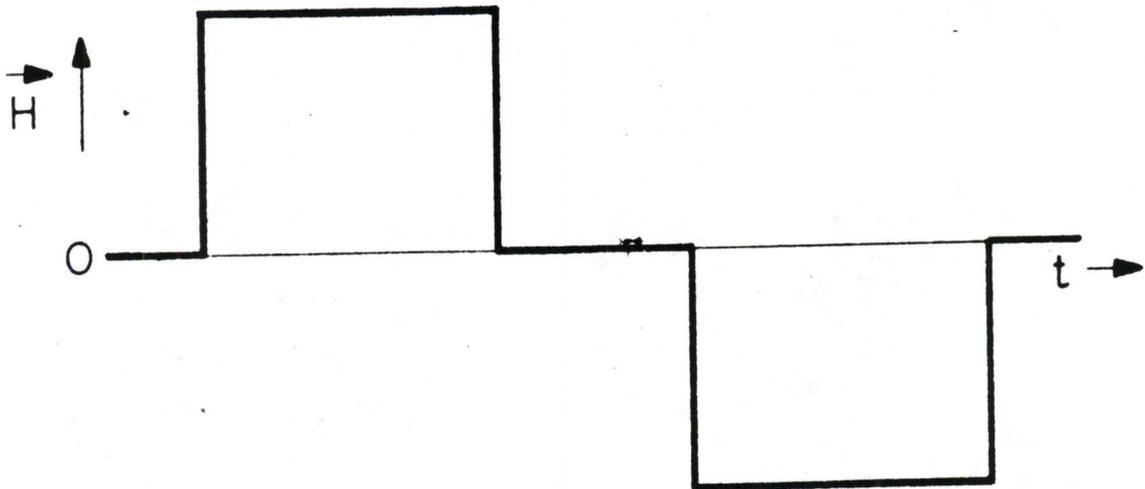
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D. R. Brown

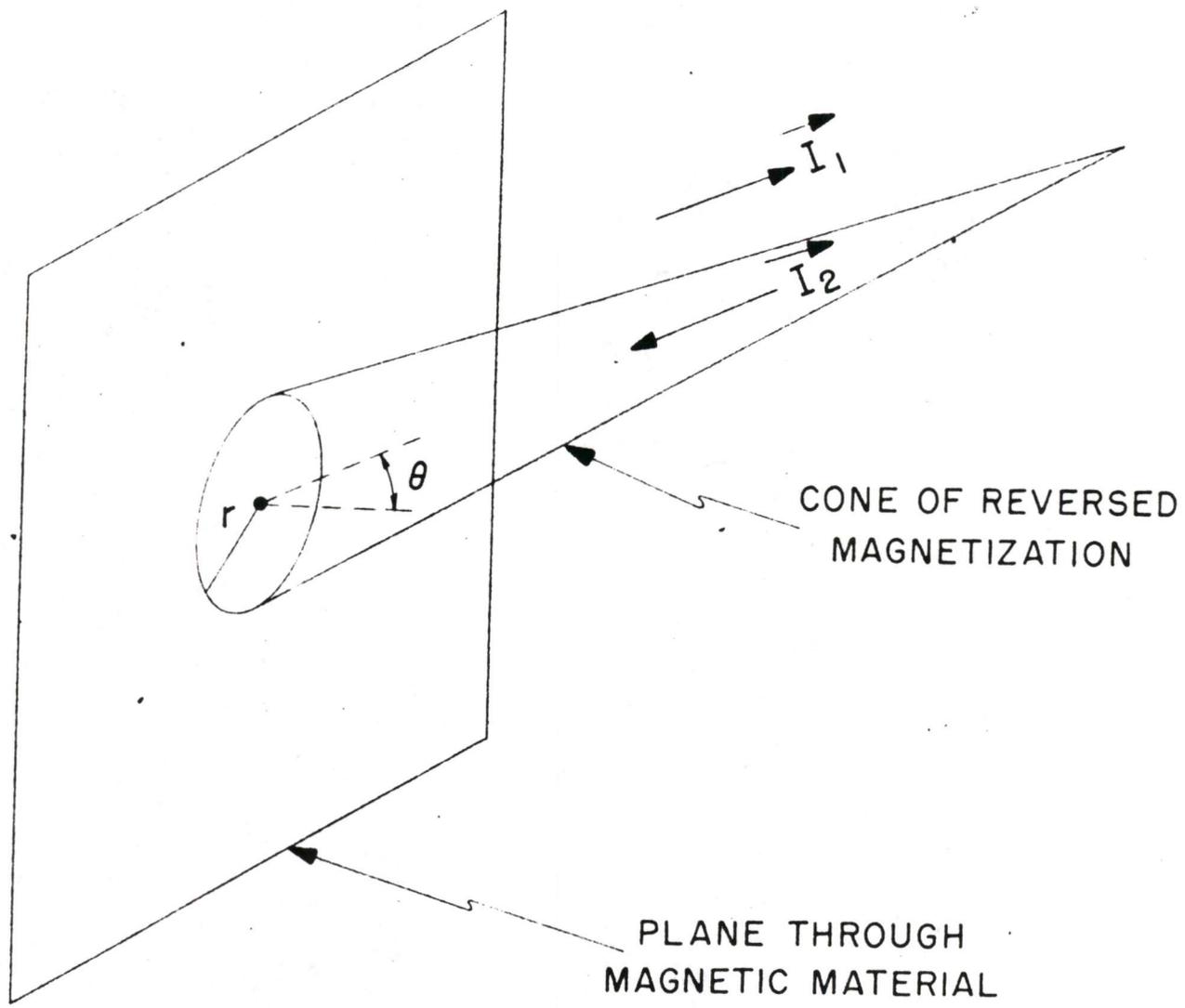
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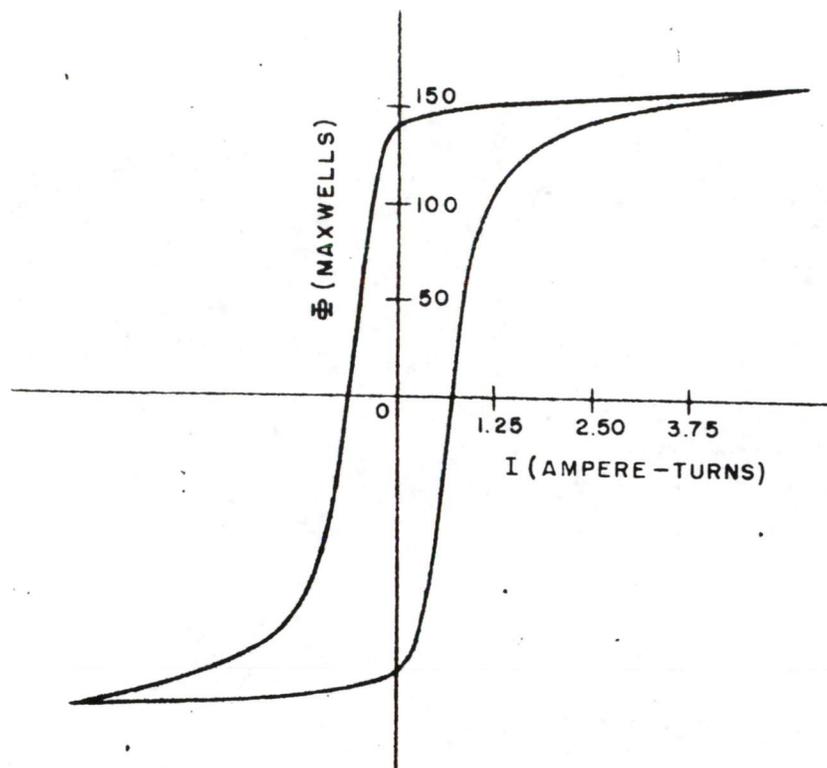
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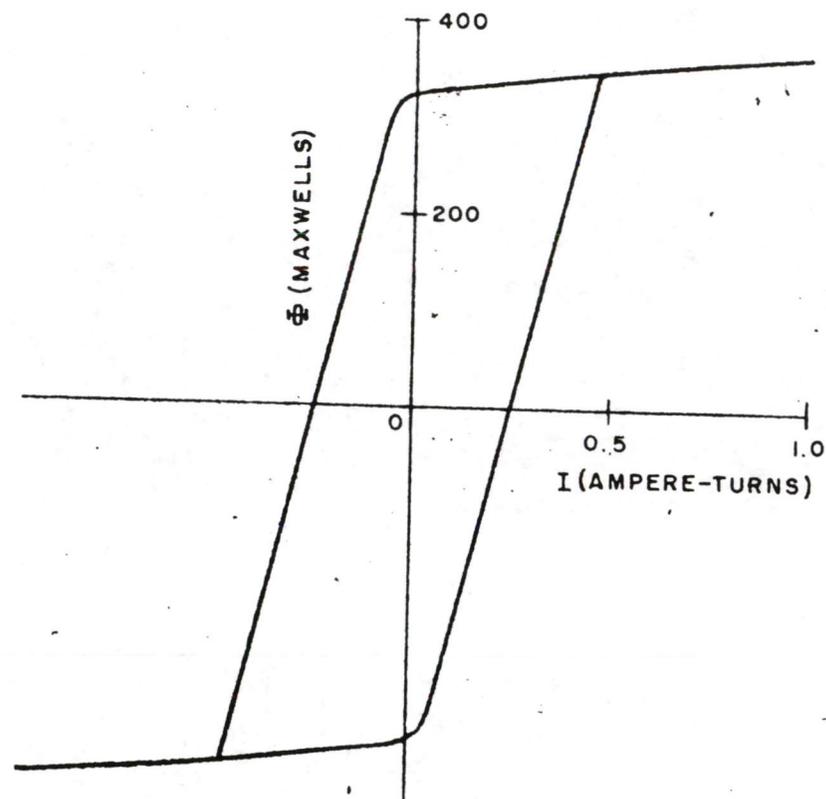
ASSUMED CORE SIGNAL INPUT



REGION OF REVERSE MAGNETIZATION



(a) STATIC HYSTERESIS LOOP OF AN MF 1312 B FERRITE CORE.



(b) 60 CYCLE HYSTERESIS LOOP OF A 140 WRAP $\frac{1}{4}$ MIL 4-79 MO-PERMALLOY CORE.

H. Olsen

6889
Memorandum M-2162

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Digital Computer Laboratory
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Subject: WWII MEMORY ADDRESS SELECTION SYSTEMS - P. B. No. 62
To: N. H. Taylor
From: J. L. Mitchell
Date: May 6, 1953

Abstract: This note contains a survey of the existing memory-address selection systems as well as a survey of some of the more promising new systems that have been proposed.

The function of the memory-address selection system is to take the memory address from the memory-address register and either read from or write into the selected memory register. In order to do this, two pieces of equipment are needed: a translator and a set of current drivers. The translator takes the output of the memory-address register flip-flops, converts from the base 2 to the base 64, and thus selects the proper driver. The selected X driver and the selected Y driver drive the X and Y selection "planes" with the currents necessary to read from and write into the memory.

Basically there are two types of translators and two methods of driving that will be considered. The two types of translators are the crystal-matrix and the magnetic-core matrix. The two methods of driving are driving a selection "plane" directly from the plate of a vacuum tube and driving a selection "plane" from the secondary of a magnetic device. The subsequent discussion will describe some of the combinations which have been proposed. Throughout this note we will talk about a 4096-register memory.

Following the description of the various systems, there are two charts: a chart, Figure 4, listing the equipment needed for each system and a chart, Figure 5, showing some of the advantages, disadvantages, and other peculiarities of each system.

Equipment counts, Figure 4, include all the equipment needed to operate the entire memory-address selection system. In the tube counts, the tubes will be separated into five types, as follows:

1. Memory drivers. These tubes drive the X and Y selection "planes" directly and must supply rectangular 500-ma current pulses about 1.5 μ secs long at a duty cycle of something less than 50%.
2. Pulse-transformer drivers. These tubes drive the memory through current step-up pulse transformers and probably will have to supply 100-ma pulses 1.5 μ secs long at something under a 50% duty factor.
3. Magnetic-core matrix drivers. These tubes drive the magnetic-core matrix and probably will have to supply the same sort of pulses as the memory drivers, or slightly greater.
4. Buffer amplifier tubes (including crystal matrix drivers).
5. Gate tubes.

A. Crystal-Matrix Translator with Vacuum-Tube Drivers

In order to select and drive one of the selection planes, we need a 64-position crystal matrix, 128 drivers and their associated buffer amplifiers, and read and write switches to gate the drivers on. Figure 1 shows a block diagram of the system. The outputs of the six flip-flops are run through buffer amplifiers into the crystal matrix. Each of the 64 outputs of the matrix goes to two buffer amplifiers which are normally-on tubes. The selected pair of buffers is cut off by the matrix, and as a result they tend to gate a read and a write driver on. However, all the read-driver cathodes are connected to ground through a common resistor, the voltage drop across this resistor being determined by the read switch. This voltage drop is adjusted so the driver tubes that have been gated will not turn on until the read switch is pulsed. When the switch is pulsed, the drop across the read resistor is decreased, causing the read driver to conduct and send $1/2 I_m$ to the selection "plane." The write operation is performed in the same manner. Each driver used to drive a memory plane would contain one tube of the "memory driver" size. The buffer amplifiers used with these drivers would also consist of one tube. The read and write switches would each be made up of five memory-driver tubes in parallel, a buffer amplifier tube, and a gate tube.

This scheme could be varied in a number of ways, one way being to gate the buffers in place of the drivers. Crystal diode gates could be placed in the input lines to the buffers and used to control the read and write operation and thus eliminate the read and write switches. This would eliminate about 25 tubes and add 256 crystals to the system.

B. Crystal-Matrix Translator with Pulse-Transformer Drive

This system is similar to the system described under part "A"; the difference is that pulse transformers have been added to the system. The memory planes are driven by three-winding, current step-up, pulse transformers which might give a current gain of about five.

C. Magnetic-Matrix Translator and Driver

To select and drive the selection "planes" along each coordinate axis, a 64-position magnetic-matrix translator and driver and 14 vacuum-tube drivers and their associated buffer amplifiers are needed, as shown in Figure 2. The switch is set up by the 12 drivers controlled by the address flip-flops; then, during read time, the read driver is turned on and causes the selected core to switch and produce a current pulse which drives the selection "plane." The write operation is carried on in a similar manner; this operation both resets the switch and supplies the write pulse to the memory. All the driver tubes would be of the "magnetic-matrix driver" type. A one-tube buffer amplifier could be used between each flip-flop output and driver; however, the read and write buffer amplifiers would need about six tubes each for pulse shaping and current regulation. There are several variations which can be made on this basic scheme, but none of them makes an appreciable change in the tube count or operation.

A good deal of work is being done on the analysis of the switch, and the feeling is that there is a fair chance that a satisfactory switch can be built in the near future.

D. Magnetic-Matrix Translator with Vacuum-Tube or Pulse-Transformer Drive

Another possible system has been suggested which uses a magnetic-matrix in place of a crystal matrix. Each core in the switch has two output windings, one going to the grid of the write driver and the other to the grid of the read driver. The secondary windings on the switch cores have a large number of turns and give enough voltage out to drive the grids of the driver tubes directly, eliminating the need for buffer amplifiers. The equipment needed to drive the switch would probably consist of single-tube drivers and a single-tube buffer amplifier for each switch driver.

E. 4096-Position Magnetic-Core Translator and Driver

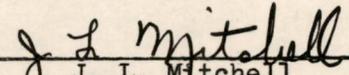
This system would use a 4096-position magnetic-core "switch," with each output of the switch driving one register of memory cores. Register selection within the memory would be on a one-coordinate basis (not using coincident currents). There are

several ways a switch like this could be built; for instance, it could be built using the same principles that are used in present matrix switches; this seems, as yet, infeasible. Another way to build the switch is described in M-2110 by K. Olsen. The equipment needed for this switch when it is, in turn, driven by crystal matrices and vacuum tubes is shown in Figure 4.

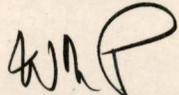
F. Crystal-and-Transformer Matrix Translator and Drive

In order to select and drive one selection "plane", this system requires two 8-position crystal matrices, 24 drivers and their associated buffer amplifiers and gates, and an array, or matrix, of 64 pulse transformers connected as shown in Figure 3. Selection of a selection "plane" is accomplished by obtaining coincidence between the read and write drivers connected to crystal matrix number one and the condition drivers connected to crystal matrix number two. The condition drivers are on during both the read and write operation, and the read and write drivers are gated on for their respective operations. The diodes in the primaries of the transformers are necessary to prevent "back" circuits in the transformer matrix. The drivers are all one-tube units, as are the buffer amplifiers and gates. IBM is building up an experimental system of this type at High Street.

Signed


J. L. Mitchell

Approved


W. N. Papian

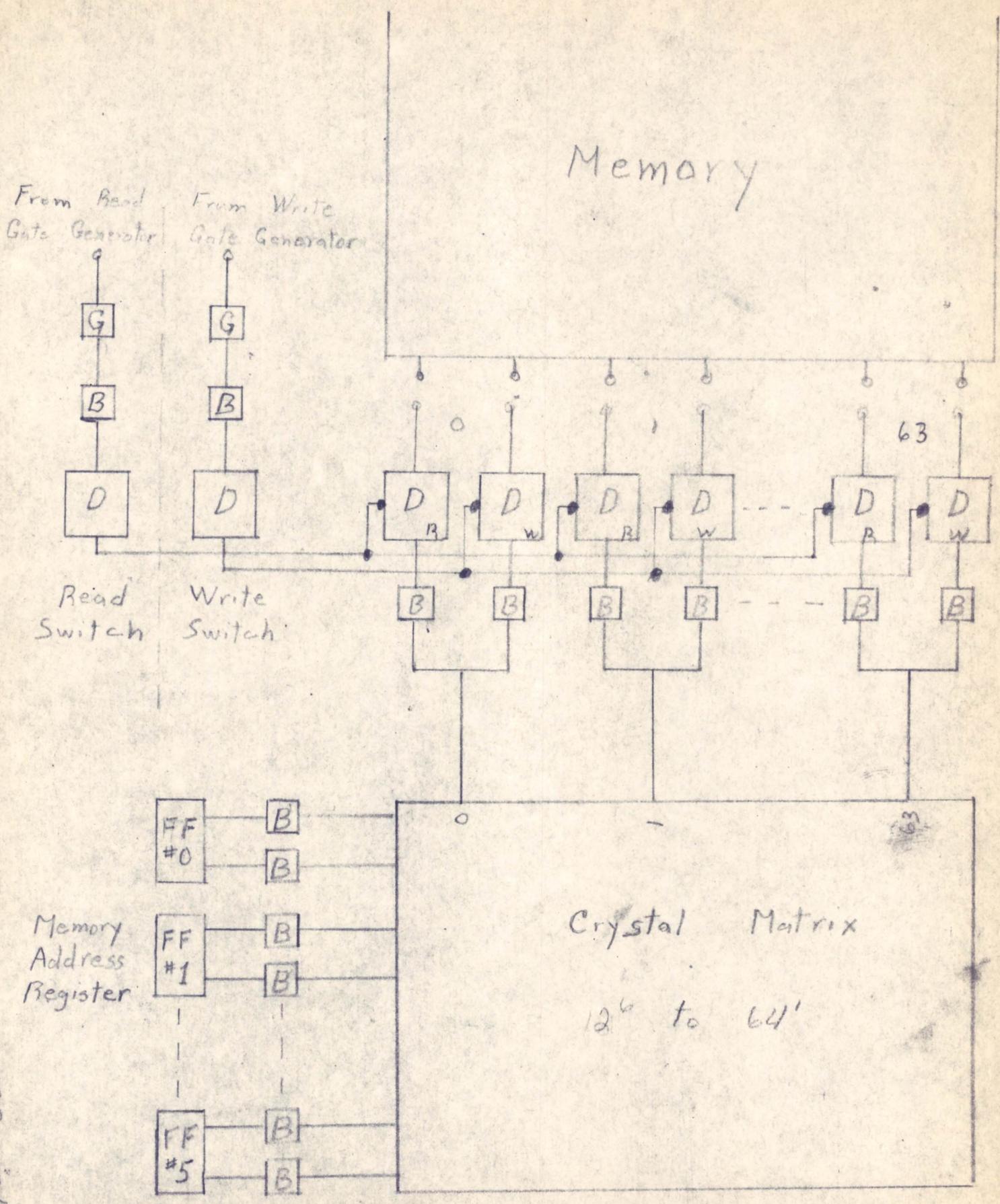
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cc: D. R. Brown, Mag. Mem. Section,
N. Edwards, D. Shansky.
J. McCusker,
R. Nelson,

Drawings attached:

Figure 1, SA-54789-2
Figure 2, SA-54790-1
Figure 3, SA-54791-3
Figure 4, SA-54911
Figure 5, SB-54912

SA-54789-2

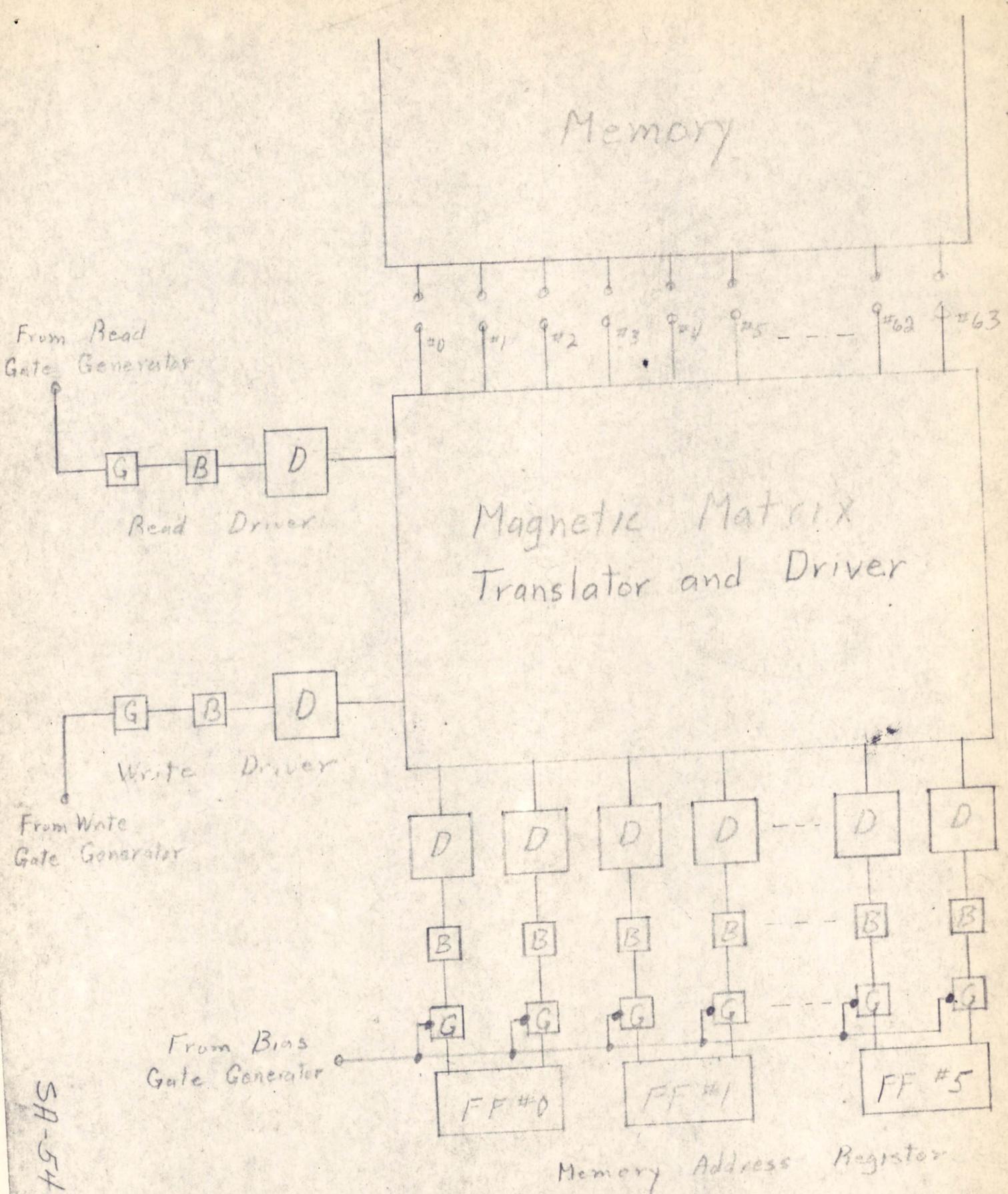


Crystal - Matrix Translator with Vacuum - Tube Drive
figure #1

810 Max. Total
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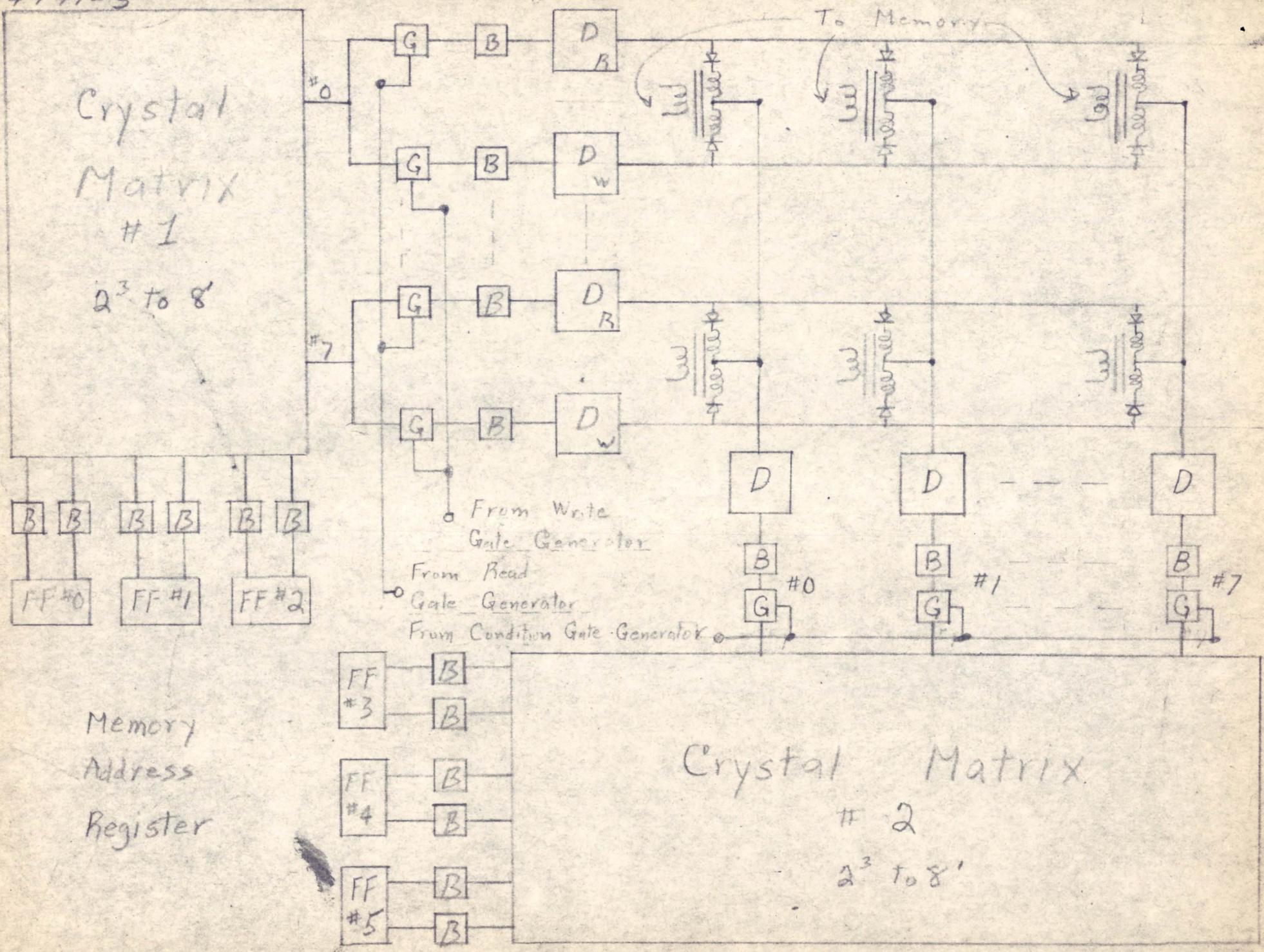
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Magnetic - Matrix Translator and Driver
 figure #2

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Crystal and Transformer Matrix Translator and Drive
 Figure # 3 SA-54791-3

88 Matrix 4-22-53

Equipment Count
 For
Memory Address
Selection Systems
 4096 registers
 figure 4

J. J. Mitchell 4-28-53

	A	B	C	D	D'	E	F
Crystal-Matrix Translator, Vacuum-Tube Drive							
Crystal-Matrix Translator, Pulse-Transformer Drive							
Magnetic-Matrix Translator and Driver							
Magnetic-Matrix Translator, Vacuum- Tube Drive							
Magnetic-Matrix Translator, Pulse- Transformer Drive							
4096-Position Magnetic-Core Translator and Drive							
Crystal and-Transformer Matrix Translator and Drive							

Memory-Driver Tubes	276	-	-	256	-	-	-
Pulse-Transformer Driver Tubes	-	276	-	-	256	-	48
Magnetic-Matrix Driver-Tubes	-	-	28	28	28	207	-
Buffer Amplifier Tubes	284	284	48	28	28	219	72
Gate Tubes	4	4	28	28	28	3	48
<u>Total Tubes</u>	564	564	104	340	340	429	168
Crystal Diodes	768	768	-	-	-	768	352
Pulse Transformers	-	128	-	-	128	-	128
Switch Cores	-	-	128	128	128	4096	-

	A Crystal-Matrix Translator, Vacuum-Tube Drive	B Crystal-Matrix Translator, Pulse-Transformer Drive	C Magnetic-Matrix Translator, and Driver	D Magnetic-Matrix Translator, Vacuum-Tube Drive	D' Magnetic-Matrix Translator, Pulse-Transformer Drive	E 4096-Position Magnetic-Core Translator and Drive	F Crystal-and- Transformer Matrix Translator and Drive
Experience with System	A rather large amount of experience has been acquired; more than any other system	Experience with components, but none with system	Some experience with 16 position switches driving a 16x16 memory	None	None	None	None
Output Current Shape and Line-to-Line Regulation	Good; common cathode resistor gives regulation	Could be obtained by feedback around transformers, precision transformers, or vernier adjustments on drivers	Input must be shaped to get desired output. Line-to-line regulation may be difficult	See A	See B	Requirement on current pulses are not as strict as in other systems	See B
PRF Sensitivity	None	Read pulse must immediately be followed by a write pulse	Some trouble may be encountered due to asymmetrical operation on B-H loop	Less trouble than C	See B	Same as C but probably less critical	See B
Number of Drive Wires in a Memory Selection Plane	2	1	1	2	1	Different winding mode.	2
Memory Array Impedance	Not critical	Should be low to keep back-voltage down	Not too critical	Not critical	See B	Not critical	Must be very low to keep back-voltage on diodes down
Memory Fabrication Ease	Standard	Standard	Standard	Standard	Standard	Memory easier to build	Standard
Signal-to-Noise Ratio in Memory Output	Standard	Standard	Standard	Standard	Standard	Better because no cores are disturbed during read time	Standard
Memory Core Specifications	Standard	Standard	Standard	Standard	Standard	Can be relaxed	Standard
Quality of Driver Tubes Available	A very reliable tube not yet found	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown
Dynamic Load on Driver (effect of cores switching)	0-32 cores out of 2048 being driven can switch	See A	See A	See A	See A	0-32 cores out of 32 being driven can switch	See A
Miscellaneous Comments			Uses fewer components than any other system	Requirements on switch core are reduced.	See D		Diodes in transformer primary are not desirable. Electronics of this system is more complicated than any other system

R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: TWO METHODS OF REDUCING DELTA NOISE AS TRIED ON
MEMORY TEST SETUPS I AND II

To: Norman H. Taylor

From: Saul Fine

Date: May 22, 1953

Abstract: A large l_D/δ value is desired for error-free magnetic-core memory operation. Improved operation can be attained by reducing the system delta to a small magnitude. This is accomplished by half-selecting all the cores in the memory plane with a post-write disturb pulse. With this method Memory Plane 1 was capable of holding a "worst" type pattern.

Another method of improving operation is to delay either the x or y coordinate drivers. This effectively separates the delta noise of both coordinate lines and reduces the magnitude of delta noise at the sensing point to one half. Both methods require added operation time.

A. Discussion of the Problem

1. Effects of l_D/δ on magnetic memory operation.

The ratio of disturbed ONE (l_D) to delta (δ) is a factor that tends to limit the size and usefulness of a magnetic-core memory. This ratio, a function of core material and production methods, should be as large as possible in order to maintain error-free operation. The driving current limits or margins are dependent on this ratio, especially when operating with a large magnetomotive force, as delta is a rapidly-rising exponential at high driving currents*.

2. Delta noise.

A definition of delta has been outlined in Engineering Note E-488 by E. A. Guditz, D.C.L. The magnitude of delta is a function of the previous history of the cores. Figure 1 is a typical hysteresis loop of a ferromagnetic core. The half-selected ONE (HSL)

* "Driving Current Margins in Memory Test Setup I", S. Fine
Engineering Note E-531, D.C.L., March 6, 1953.

output of a core is largest in magnitude if the core had previously been undisturbed (HSl_0). This is point A on Fig. 1. After one or more disturbances in the read direction the remanent flux moves to point C and the magnitude of the HSl output is very much smaller (HSl_1). However, if the disturbed core is now half-selected in the write direction, the remanent flux changes from point C to point B. The half-selected ONE readout (HSl_1^1) now is larger in magnitude. Similarly, a half-selected core holding ZERO will produce a larger output if it had been disturbed in the write direction (point D) than if it had been disturbed in the read direction (point E). Delta is defined as the difference in the half-selected outputs of a core holding ONE and a core holding ZERO; this indicates that the amount of delta noise depends on the previous history of the cores.

The sensing winding output signal is the sum of all the voltages on the winding. This includes either a disturbed ONE or disturbed ZERO plus the various magnitudes of delta. The polarity of the deltas might be such that they reduce the size of a ONE or increase the size of a ZERO. The obvious thing to do is to reduce the system delta to as small a value as possible. $\delta_1 = (HSl_1 - HSO_1)$ cannot be reduced any further so $\delta_0 = (HSl_0 - HSO_1)$ and $\delta_1^1 = (HSl_1^1 - HSO_1)$, the larger and more troublesome magnitudes, must be reduced through some means. This is especially true for large memory planes where many δ_1^1 can add to cause an error.

B. Post-Write Pulse

1. Method of applying Post-write pulse.

The magnitude of delta can be reduced to δ_1 in amplitude by disturbing all the undisturbed cores and all those cores with remanent flux at point B or D (Fig. 1) through the application of a half-amplitude current pulse in the read direction. This pulse can be conveniently applied to the z-plane winding. It must be applied after the write pulse, before reading, and has been called a "post-write disturb pulse." This post-write pulse puts all cores at remanent flux points C or E, so the next readout will produce delta noise that is small in magnitude and improved memory plane operation will be attained.

Experimental observations have shown that the half-selected output of a core rises to a peak value rapidly and reduces to a small magnitude at approximately $2/3$ the switching time of the core. Therefore, the duration of the half-amplitude disturb pulse need be only $1/2$ to $1/3$ that of the read pulse.

The core-switching time of memory plane 1 is 12μ seconds at normal current. It was found that a post-write disturb pulse of 6μ second duration was sufficient to reduce δ_0 and δ_1' to δ_1 in magnitude. In memory plane 6, whose core-switching time is 8μ seconds, a post-write disturb pulse of 4μ seconds duration was found sufficient.

This added pulse increases the overall cycle time, thus limiting the PRF at which the memory can operate. It is felt that improved operation resulting from the added disturb pulse is more necessary than the increase in PRF.

2. Operation of memory plane 1.

The cores used in memory plane 1 are Magnetics, Inc., Molybdenum-Permalloy, $1/4$ -mil thick, 5 wraps. From tests made, the peak value of l_D/δ_0 is 11 and of l_D/δ_1 is 180. δ_0 is approximately 15 times the amplitude of δ_1 . The memory plane was unable to hold certain "worst" patterns. These are patterns in which the selected core held a ONE with an output polarity opposite to the HSI outputs along the selected lines or a pattern in which the selected core held ZERO with an output polarity the same as HSI. In either case, the ONE output was reduced in amplitude and the ZERO output increased.

By applying a post-write disturb pulse to the entire z-plane winding in the read direction, the abnormally large δ_0 was reduced to the magnitude of δ_1 , and the memory plane was able to hold the "worst" patterns. The current margins were increased from zero (the memory would not operate without the added pulse) to $\pm 13\%$ of a normal driving current of 240 ma. Therefore, in memory plane 1 the post-write disturb pulse was the difference between operating satisfactorily or not operating at all. (See Fig. 2-a). Another difficulty in operation of this plane is that the signal levels are low - in the order of 6-10 millivolts. Noise due to coupling or line transients can easily be of a magnitude that will cause an error in operation.

According to present standards, the cores used in this plane are poor. There has been considerable improvement in core manufacturing in the meantime, with resulting improvement in operation of succeeding arrays.

3. Operation of memory plane 6.

Memory plane 6 consists of 256 moly-permalloy cores, $1/8$ -mil thick, 10 wraps, made by Magnetics, Inc. The outputs of these cores are much improved over plane 1, both in ONE amplitude and in switching time. The average value of l_D/δ_0 was measured at 270, with normal

driving current of 180 ma. I_D/δ_1 was measured at 5500. This indicates that both the HSI disturbed and undisturbed outputs are much less than the disturbed ONE output. From this fact it is to be expected that memory plane 6 operation should be greatly improved over that of plane 1. This has been verified in that the memory will hold the "worst" type of pattern with satisfactory results.

Because the magnitude of δ and δ^1 is small enough so as not to be troublesome the post-write disturb pulse has little effect on operation. (See Fig. 2-b). This memory plane has been operating satisfactorily using both 2-to-1 and 3-to-1 selection without the post-write disturb pulse.

4. Memory Test Setup II.

Memory plane 2, a 16 x 16 array using ceramic cores type 1118, was the first of the two planes used in Memory Test Setup II. A driving current of three amperes was used to switch the cores. At this current the ratio I_D/δ_0 was measured at 30 and I_D/δ_1 measured at 385. The ratios are considerably less than those of plane 6, and, as expected, discrimination between ONE and ZERO was not quite as good, although no exceptional operating difficulties were experienced during the operation of this plane. This is partly due to the large signal outputs obtained from high driving currents. The signal output is large enough to override any noise developed in the array.

The array can hold the "worst" type of pattern without difficulty and without using a post-write disturb pulse. Its use, however, does result in some improvement in ONE-to-ZERO discrimination. (See Fig. 3-a).

The other plane used in this setup was a 16 x 16 array of ferrite-cores type 1326B. At a driving current of 1 ampere, the ratio I_D/δ_0 was measured at 68 and I_D/δ_1 at 1200. The ONE-to-ZERO discrimination is very good in this plane. This is to be expected because of the large ONE-to-delta ratio. The memory can hold the "worst" type patterns without using the post-write disturb pulse. (See Fig. 3-b). Its effect, however, is to improve ONE-ZERO discrimination slightly, and it will probably be incorporated in larger memory planes using this type of core. Whether the amount of improvement in operation will warrant the reduction in PRF because of the time consumed by the added disturb pulse will be determined later.

Other Methods of Improving Operation1. Y driver delay

In using memory plane 1, it was found that by delaying either the Y or X driver a few microseconds, considerable improvement in operation was attained. Effectively this reduced the delta magnitude at the sensing point by separating the delta outputs of the selected row from the delta outputs of the selected column.

The half-selected output of a core rises to a maximum value and then decays to a low value in about $2/3$ of the core-switching time. By delaying the Y-column driving current, the half-selected outputs along the X row will have passed their peak value and will be approaching a minimum value before the half-selected outputs of the Y column appear on the sensing winding. Therefore, at the point of sensing only one-half of the unwanted delta outputs will have a magnitude large enough to add to or subtract from the output of the selected core. This greatly improves the ONE-ZERO discrimination, the ability to hold a "worst" pattern, and the driving current margins. Memory plane #1 was able to hold a "worst" type pattern with but a 2- μ second delay in Y driver current. Somewhat better operation was observed with a delay of 4- μ seconds. Increasing the Y driving current delay further, did not result in any additional improvement in operation. Similar results were obtained by delaying the X driver current instead of the Y. Figure 4 shows the sensed output of plane #1 with a 2- μ second and a 4- μ second delay in Y driver current. The plane was holding a "worst" type of pattern. Without a delay in the Y driver this plane was unable to hold the "worst" pattern.

2. Increasing Y driver rise time

Increasing the rise time of the Y driver is essentially delaying the Y driver current. This results in a separation of X and Y deltas, so that at the sensing point the ONE-ZERO discrimination is improved. The improvement in operation for a given increase in Y-driver rise time was found to be the same as that attained by delaying the Y-driver current by this same amount of time. Increasing the X-driver rise time instead of the Y resulted in a similar improvement in operation.

A further improvement in operation was attained by incorporating the Z-plane winding post-write disturb pulse along with an increase in Y-driver rise time. Figure 4-b shows the effects of this last method on the memory plane operation. All photographs were taken with memory plane #1 holding the "worst" type pattern. The first photo is the sensed output without a half-amplitude disturb pulse and with equal X- and Y-driver rise times but with a post-write disturb pulse. The last two photos are with a post-write disturb pulse and with increased Y-driver rise time.

It should be remembered, however, that all of the operational improvement methods explained in this paper result in increased operation time and therefore a reduced pulse-repetition frequency. In using any one of the three methods explained, the increase in overall operation time for a similar improvement in operation will be approximately the same. However, using a half-amplitude disturb pulse along with an increase in Y-driver rise time will result in a much longer overall operation time. The type of core used, i.e., the l_D/δ ratio and the core switching time, and the application of the memory plane will be determining factors in which method is to be used.

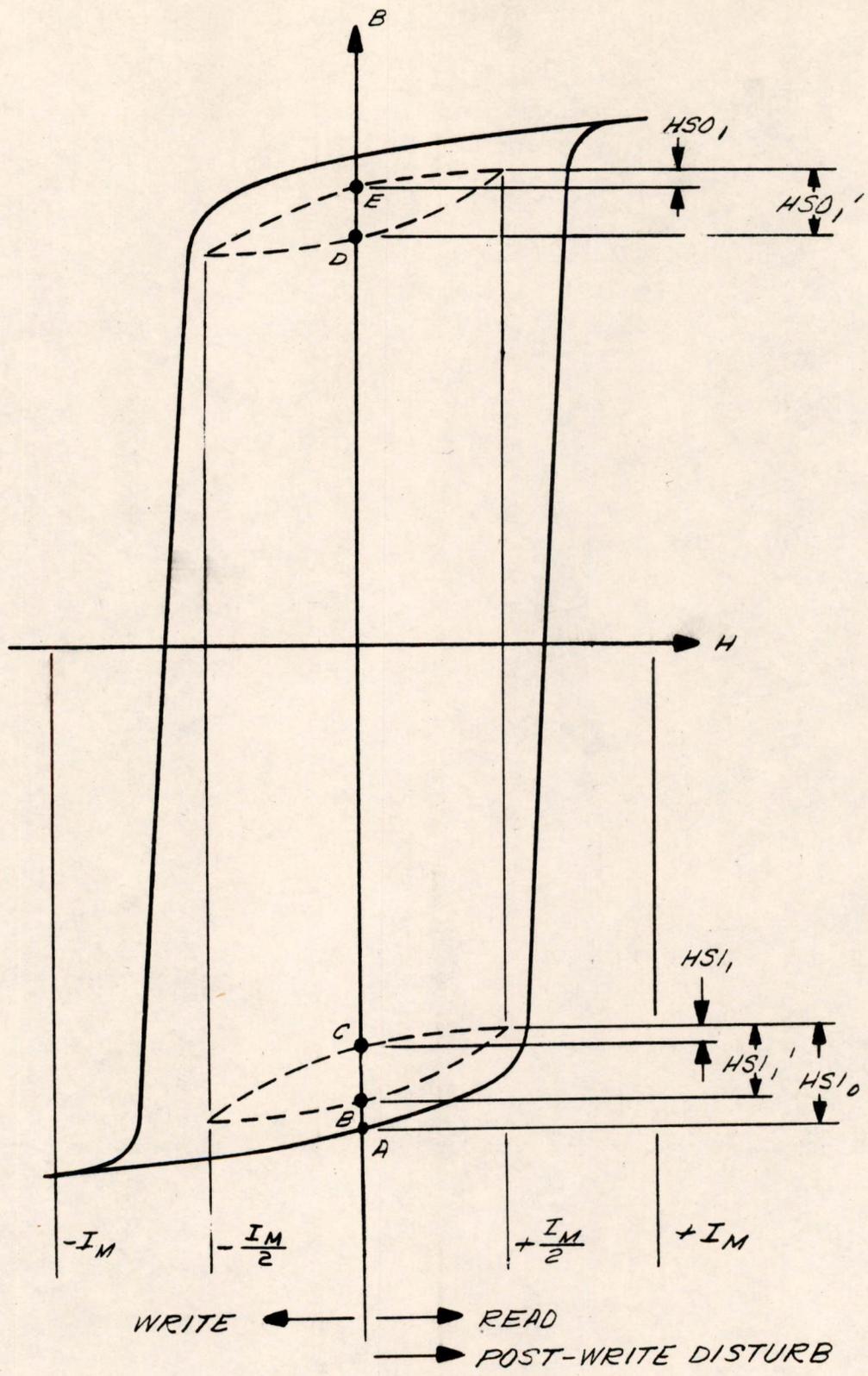
Signed S. Fine
S. Fine

Approved W. N. Papian
W. N. Papian

SF:jrt

Drawings attached: A-54971
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A-55196
A-55195

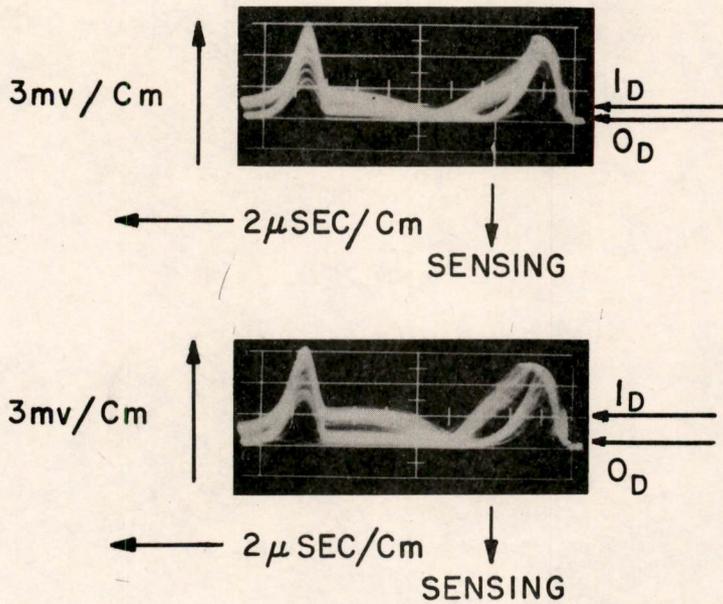
cc: D. R. Brown
J. McGusker
Magnetic Memory Section
Nate Edwards (IBM)



A-54971

FIG. 1

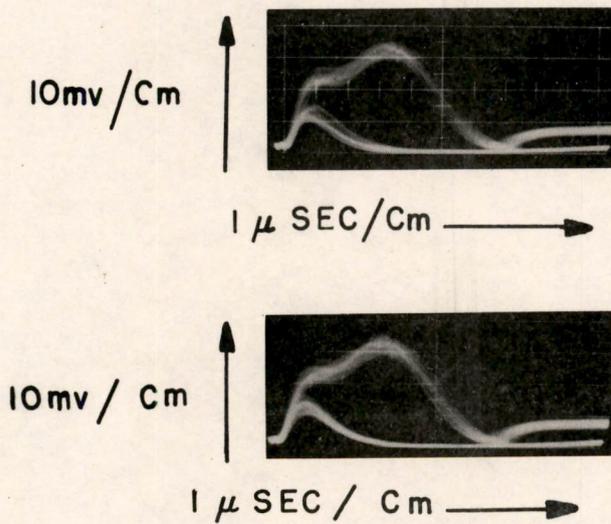
A "RECTANGULAR" HYSTERESIS LOOP



MEMORY PLANE 1
 SENSING AMPLIFIER OUTPUTS.
 $I_m = 280$ ma.
 ARRAY HOLDING "WORST"
 PATTERN WITHOUT USING
 POST-WRITE DISTURB PULSE.

SENSING AT 5.0μ SEC.
 $I_z = 140$ ma.
 WITH POST-WRITE DISTURB
 PULSE APPLIED TO Z PLANE
 WINDING.

(a)

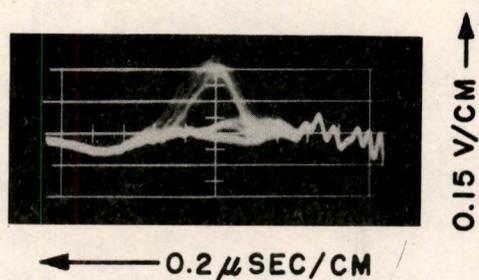


MEMORY PLANE 6
 SENSING AMPLIFIER OUTPUTS.
 $I_m = 200$ ma.
 ARRAY HOLDING "WORST"
 PATTERN WITHOUT USING
 POST-WRITE DISTURB PULSE.

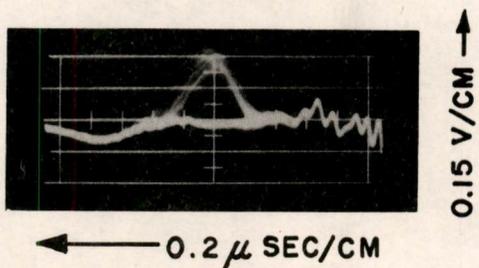
SENSING AT 3.5μ SEC.
 $I_z = 100$ ma.
 WITH POST-WRITE DISTURB
 PULSE APPLIED TO Z PLANE
 WINDING.

(b)

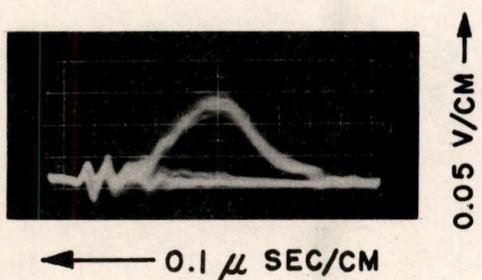
FIG. 2
 SENSED OUTPUT OF MEMORY PLANES 1 AND 6



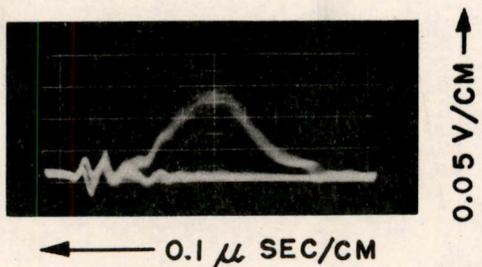
(a) MEMORY PLANE 2
 SENSING WINDING OUTPUT.
 $I_m = 3.6$ AMPERES.
 "WORST" PATTERN WITHOUT
 POST-WRITE DISTURB PULSE.



WITH POST-WRITE DISTURB
 PULSE APPLIED TO THE
 Z PLANE WINDING.

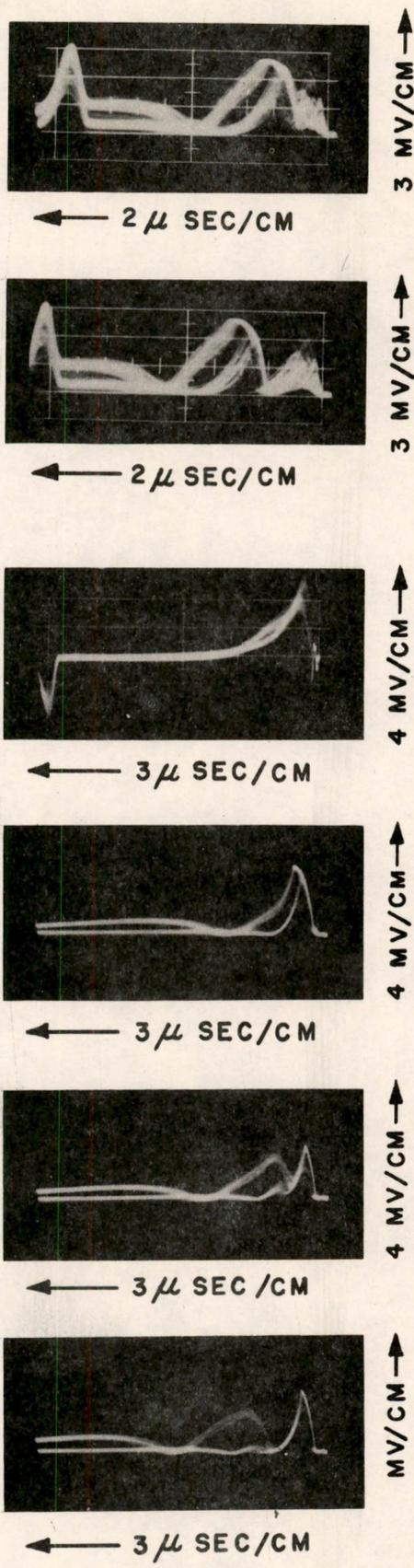


(b) MEMORY PLANE 4
 SENSING WINDING OUTPUT
 $I_m = 1$ AMP.
 ARRAY HOLDING "WORST"
 PATTERN WITHOUT POST-WRITE
 DISTURB PULSE.



WITH POST-WRITE DISTURB
 PULSE APPLIED TO THE
 Z PLANE WINDING.
 $I_z = 500$ mA

FIG. 3
 SENSED OUTPUT OF
 MEMORY PLANES 2 AND 4



(a) MEMORY PLANE 1

SENSING AMPLIFIER OUTPUTS.
 NO POST-WRITE DISTURB PULSE.
 Y DRIVER DELAYED $2 \mu \text{ SEC}$
 AFTER X DRIVER.
 $I_m = 280 \text{ ma.}$
 ARRAY HOLDING "WORST" PATTERN.

Y DRIVER DELAYED $4 \mu \text{ SEC}$
 AFTER X DRIVER.

(b) MEMORY PLANE 1

SENSING AMPLIFIER OUTPUTS.
 $I_m = 280 \text{ ma}$
 NO POST-WRITE DISTURB PULSE.
 $\frac{1}{2} \mu \text{ SEC}$ RISE TIME ON X AND
 Y DRIVERS
 ARRAY HOLDING "WORST" PATTERN.

POST-WRITE DISTURB PULSE
 APPLIED.
 $\frac{1}{2} \mu \text{ SEC}$ RISE TIME ON X AND
 Y DRIVERS.

POST-WRITE DISTURB PULSE
 APPLIED.
 X DRIVER RISE TIME = $\frac{1}{2} \mu \text{ SEC.}$
 Y DRIVER RISE TIME = $3 \mu \text{ SEC.}$

POST-WRITE DISTURB PULSE
 APPLIED.
 X DRIVER RISE TIME = $\frac{1}{2} \mu \text{ SEC.}$
 Y DRIVER RISE TIME = $6 \mu \text{ SEC.}$

FIG. 4
 MEMORY PLANE 1 OUTPUT

R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: READOUT AND DIGIT-PLANE DRIVING SYSTEMS - P.B. No. 62
To: Norman H. Taylor
From: W. Canty and S. Fine
Date: May 28, 1953

Abstract: This note contains a survey of the existing readout and digit-plane driving systems as well as a survey of some of the more promising new systems that are proposed. Preliminary block diagrams with weak and strong points of each system are also included.

Introduction

In order to make an evaluation of readout and digit-plane driving systems, certain basic assumptions have been made to establish a starting point of this investigation. They are:

1. Storage Medium - it is assumed that small ferrite rings approximately 0.090 inches O.D., 0.060 inches I.D., and 0.030 inches thick will be used as the storage medium.
2. Selection System - it is assumed that the memory will be of the coincident-current single-turn type using digit-plane winding currents for inhibition of write-current pulses, and using 2:1 current ratios.
3. Readout System - it is assumed that the readout system will be destructive. Cores holding a ONE will induce a voltage pulse in a sense winding, threaded through cores in each memory plane, when interrogated by a read current pulse of essentially the same shape and amplitude as the write pulses.

READOUT SYSTEMS

Proposed Readout Schemes

1. Single Sensing Winding (Fig. 1-A)

This scheme is the present system of read-write using one sensing winding and one sensing amplifier per plane. The output of the sensing amplifier is to be a positive-going pulse applied to the negatively-biased suppressor grid of a gate tube. A strobing pulse will determine the point of sampling.

The present MTC sensing amplifier consists of 5 tubes: 3 stages of amplification, a phase inverter, and a cathode follower. The amplifier gain is from 250 to 1000. Rise time is approximately 0.3 μ second and bandwidth is 2 mcps.

If specially-designed pulse transformers were available, the sensing amplifier design might be reduced to two stages of amplification and a cathode follower.

2. Multiple Sensing Windings (Fig. 1-B)

This is the same scheme as (1) except that the sensing winding is divided into N number of sections with one sensing amplifier for each section. This requires N times as many sensing amplifiers and tubes as scheme 1. Considering equal size planes, the delta noise per sensing amplifier would be reduced over that in scheme 1 by a factor of 1 over the square root of the number of sections.

3. Post-Write Disturb (Fig. 2-A)

This consists of scheme 1 or 2 with an added post-write disturb pulse. The post-write pulse can be generated by the digit-plane driver or by a separate driver. The duration of the post-write pulse is from 1/2 to 2/3 of the switching time. This results in a much-improved signal ratio.

If the digit-plane driver is used for post-writing, no added tubes or components in the memory system are required. The addition of the extra pulse, of course, increases the overall memory cycle time by that amount.

4. Staggered Read (Fig. 2-B)

The start of the read pulse is staggered, i.e., the read pulse on one coordinate line is delayed. This will result in having the half-selected core outputs along one coordinate line reach a maximum and decay to a small magnitude well before the point of sensing. Effectively, this reduces the delta noise to one-half that of scheme 1.

A negligible amount of additional tubes or components are required in the memory system. The memory cycle time will be increased by approximately one-half the switching time of the core and the information readout time will be increased by a factor of 2.

5. Same-Polarity Double-Read and Compare (Fig. 3-A)

This method requires a double read pulse. The first readout is delayed and then compared with a second readout in a difference amplifier. If the same noise is read out both times, they should cancel, leaving only a ONE for a core holding ONE or nothing for a core holding ZERO. A post-write disturb pulse is necessary to assure that each core produces the same half-selected output during both readouts. This results in an increased memory cycle time of over 1.6 times that of scheme 1 while the information readout time is increased at least 4 times.

6. Opposite-Polarity Double-Read and Compare (Fig. 3-B)

This method is similar to scheme 5 except that the second read pulse is opposite in polarity to the first. This allows the use of a magnetic-matrix switch or transformer driver. The first read is delayed, inverted and compared with the second read in the same manner as described in scheme 5. The rewrite may be as in scheme 1 unless magnetic-core drivers are used, in which case another pair of opposite-polarity pulses must be used. The memory cycle time is thus increased over scheme 1 by a factor of at least 1.5 for vacuum-tube drivers, or 2 for magnetic-core drivers. The information readout time is increased by a factor of at least 4.

In order to have the delta noise equal during first and second read pulses, it will be necessary to half-select all cores in a write direction prior to the readout. This further increases the overall operation time.

With the addition of integration in this sensing scheme it becomes essentially that being used at R.C.A. Laboratories. Using the integral of the outputs means that all "closed-path" noises will be cancelled out.

7. Single Read with Delay (Fig. 4-A)

If the rise and fall time of the read current pulse are equal, the $d\Phi/dt$ producing both delta noise and air-flux noise will be almost equal in magnitude and opposite in polarity at the start and finish of the read pulse. This noise can be cancelled by proper delay and comparison in a difference amplifier. A post-write pulse is necessary so that the core's history will assure more complete noise cancellation. The overall time added to the present read-write-post-write disturb system is approximately 1/3 the duration of the read gate while the information readout time may be about 3 times larger.

8. Combination of Scheme 3 with Others (Fig. 4-B)

The post-write pulse has the pronounced effect of reducing the delta noise in the sensing winding and may be incorporated with other methods in reducing the overall delta-noise outputs. Schemes 3 and 4 would be a good delta noise-reducing combination. A disadvantage, though, would be the increase in memory-cycle time. The post-write pulse is also necessary with schemes 5 and 7 in order to assure better noise cancellation.

DIGIT PLANE DRIVERS

The Problem

The insertion of binary information into the memory registers of WWII necessitates the use of inhibition pulses supplied to a digit-plane winding of each plane in the memory where a ZERO is to be written. These pulses are approximately the same amplitude and shape as the x and y selection-plane currents. They are applied during the application of x and y write current pulses and nullify the effect of these pulses on the core at the x-y intersection. MTC experience has indicated the usefulness of a post-write disturb pulse, that is a pulse applied to the digit-plane winding of every memory plane, of the same amplitude and approximately the same shape as the inhibition pulse. A convenient

time to apply this pulse is immediately after the memory write time. The post-write disturb pulse is effective in reducing the "delta" noise in large arrays when certain configurations of ONES and ZEROS are stored.

Theoretical studies of noise in large arrays predict that a reduction in noise can also be accomplished by using the post-write disturb pulse only on those planes into which a ONE has been written. This reduction of noise is of the same order as that which is obtained by using a post-write disturb pulse at the end of each memory read-write cycle irrespective of whether a ONE or a ZERO is written. The use of post-write disturb pulses only in those planes into which a ONE has been written lends itself nicely to some of the digit-plane driving schemes to be mentioned in this report since it would be difficult (in these cases) to supply a post-write disturb pulse immediately after an inhibition pulse. The problem as to whether or not a post-write disturb pulse is to be used or whether a "partial" post-write disturb or a "full" post-write disturb system is to be used is largely dependent on the nature of the memory cores and the sensing scheme to be used, therefore the relative merits of each system will not be discussed further.

Drawing once more from MTC experience we can list the tentative specifications for a WWII digit plane driver:

I_m	300 - 500 ma
Rise Time	0.3 - 0.6 μ second
Current Regulation	\pm 5%
Overshoot or Ripple on Top of Pulse	\pm 5%
Inhibit Pulse Duration	approx. 2 μ seconds
Post-Write Disturb Pulse Duration	approx. 1.5 μ second
Interval between Inhibit and Post-Write Disturb Pulses	may be as small as 0 μ second
Memory Cycle Time	5 - 10 μ seconds

It may be possible to allow digit-plane currents to vary much more than \pm 5% as stated above. In MTC while a "complemented checkerboard pattern" (so called worst possible pattern) was being interrogated, the digit-plane driver currents could be varied in any one of 3 digits (these were the only ones tried) \pm 30% from the normal operating current without causing an error. While this test was by no means conclusive it indicates that the above specification on current regulation may be too strict. Further study will be needed in this matter.

The problem at hand is to outline digit-plane driving schemes which will meet the above specifications and to list the advantages and disadvantages of each.

The Proposed Systems

To supply memory plane inhibition and possible post-write disturb pulses in WWII, four schemes are hereforth proposed:

A. Utilizing digit-plane drivers of the type currently used in MTC. Inhibition and post-write pulse currents would flow through a digit-plane winding in the plane directly coupled to the plate circuit of the output driver stage. This requires that the driver output tubes pass peak currents of approximately 0.5 ampere. A schematic diagram of such a driver which meets the tentative specifications above is shown in Fig. 6. A block diagram of such a system is given in Fig. 7. Advantages and disadvantages of this scheme are given in Fig. 11.

B. Utilizing a digit-plane driver of the same type used in part A with the exception that the plate circuit of the output stage is transformer coupled to the digit-plane winding of the memory plane. Since better transfer of energy to the digit-plane winding is attained, a saving of one of the output tubes in the circuit of figure 1 can be realized. Advantages and disadvantages of this system are given in Fig. 11.

C. Essentially the scheme described in part B with diodes in transformer secondary. An objection to the scheme proposed in part B is that the negative overshoot on the secondary of the pulse transformer is objectionable when applied to a driving line of a memory. Also if an attempt is made to keep the amplitude of this overshoot small by adjusting transformer parameters a long time is taken for the overshoot to disappear completely and the transformer is PRF sensitive. A means of overcoming either of these two faults might be to place a diode either in series or parallel with the transformer secondary. Advantages and disadvantages of this system are given in Fig. 11.

D. Utilizing switch cores. No experience has been gained with this type system, therefore a more detailed explanation will be given. Switch cores of the type now under investigation for use in x and y selection-plane driver systems could be used here. A block diagram is shown in Fig. 8 and a timing diagram in Fig. 9 while a schematic diagram of the system is shown in Fig. 10. The operation of the system is as follows: Control Pulses are (see Fig. 9) applied from a current source. The first pulse which occurs during the memory write time causes the switching of unbiased cores and a resulting inhibition pulse is applied to each digit plane where a ZERO is to be written. A removal of bias on all cores during the Post-Write Disturb time allows a second positive pulse in the control winding to switch cores not previously switched and thus a post-write disturb pulse is applied to those digit planes into which a ONE was just written. A negative pulse applied to the control winding resets all switch cores to their original state. A junction diode in the output line

of each core prevents the reset pulse of each core from being applied to the digit-plane winding of the memory planes. Advantages and disadvantages of this system are listed in Fig. 11.

Signed

W. J. Canty

 W. J. Canty

S. Fine

S. Fine

Approved

W. N. Papian

W. N. Papian

WJC/SF:jrt

Drawings Attached: SA 37479
 SA 37480
 SA 37481
 SA 37482
 SA 37483
 SA 37484

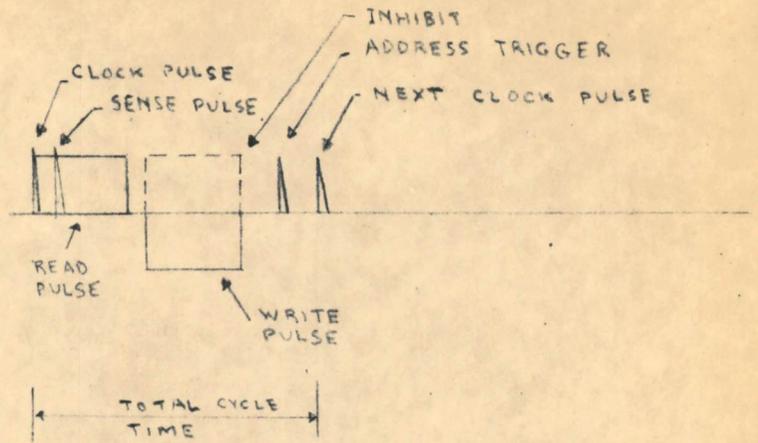
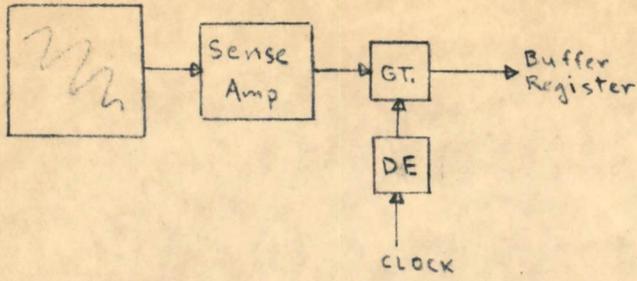
SA 54918-2
 SA 55146
 SA 55147
 SA 55148
 Figure 11

Distribution List:

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 R. A. Nelson
 D. Shansky
 Magnetic Memory Section

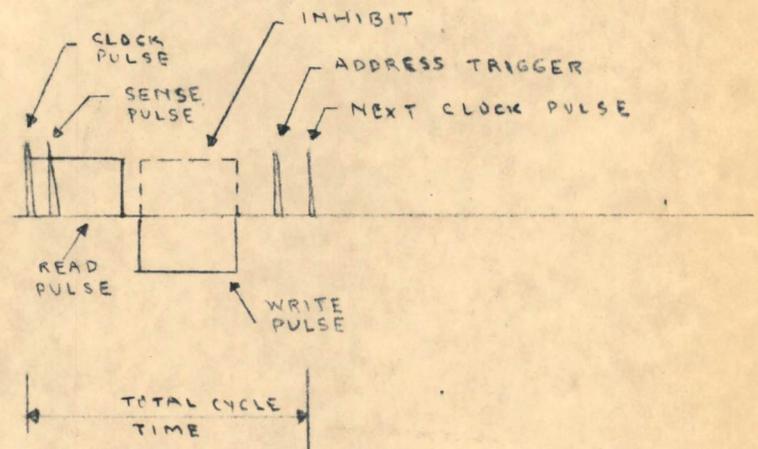
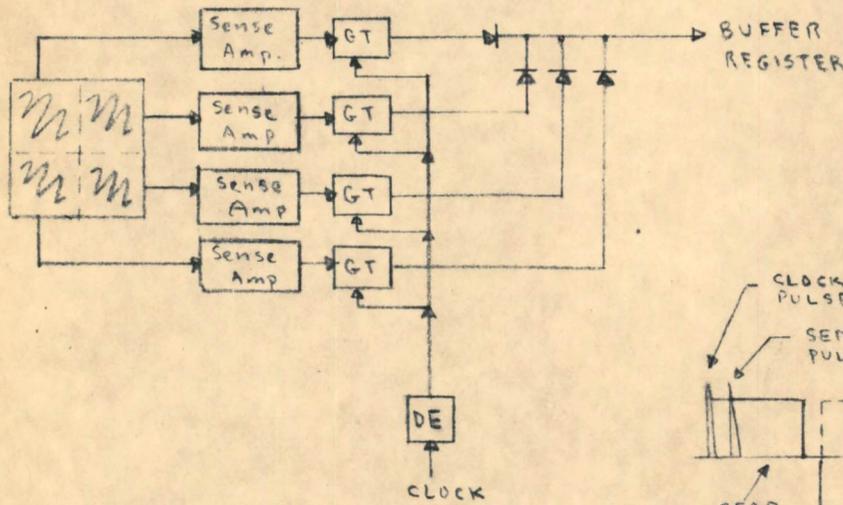
Scheme 1

FIGURE 1-A



Scheme 2

FIGURE 1-B



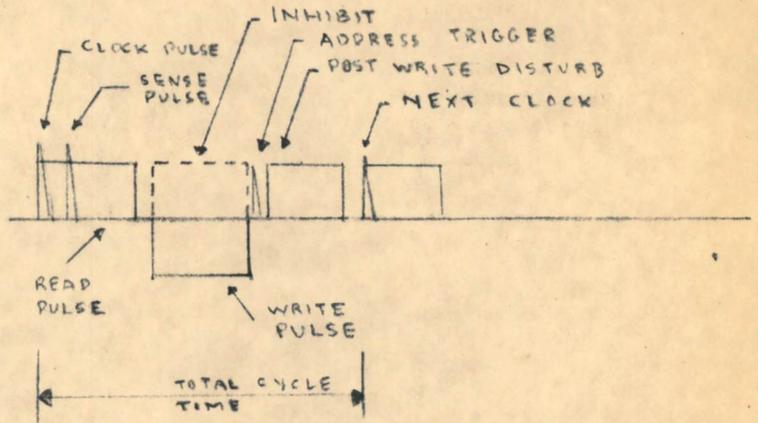
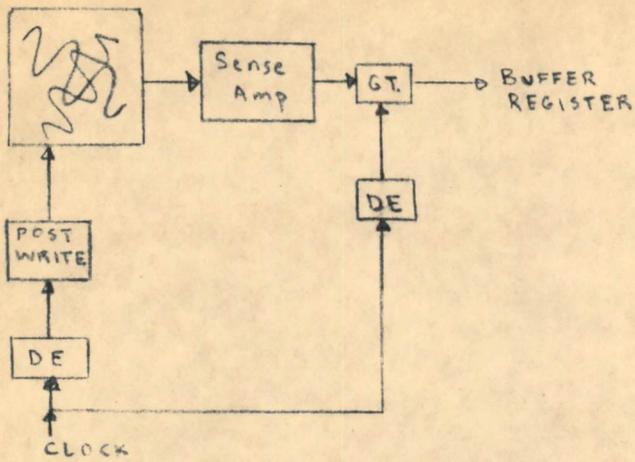
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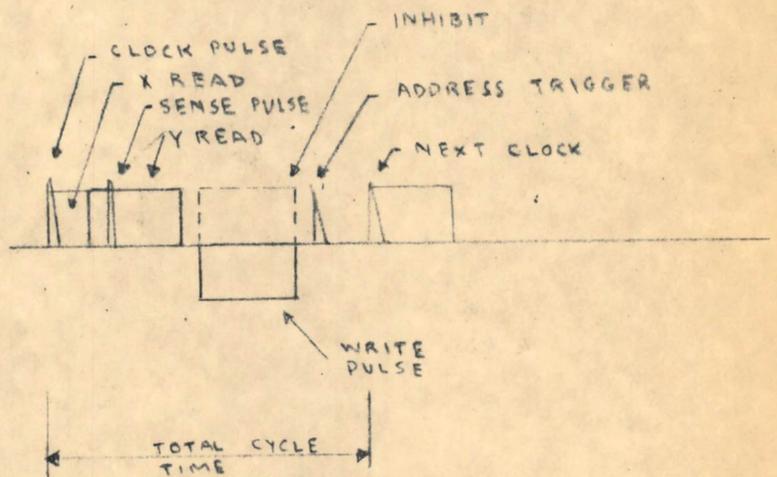
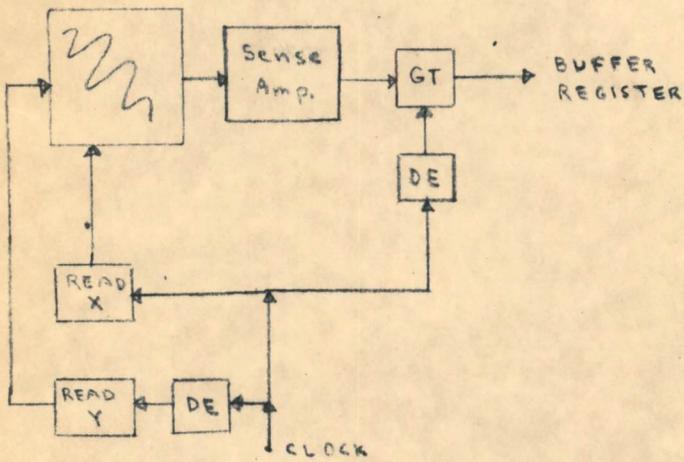
FIGURE 2-A

Scheme 3



Scheme 4

FIGURE 2-B



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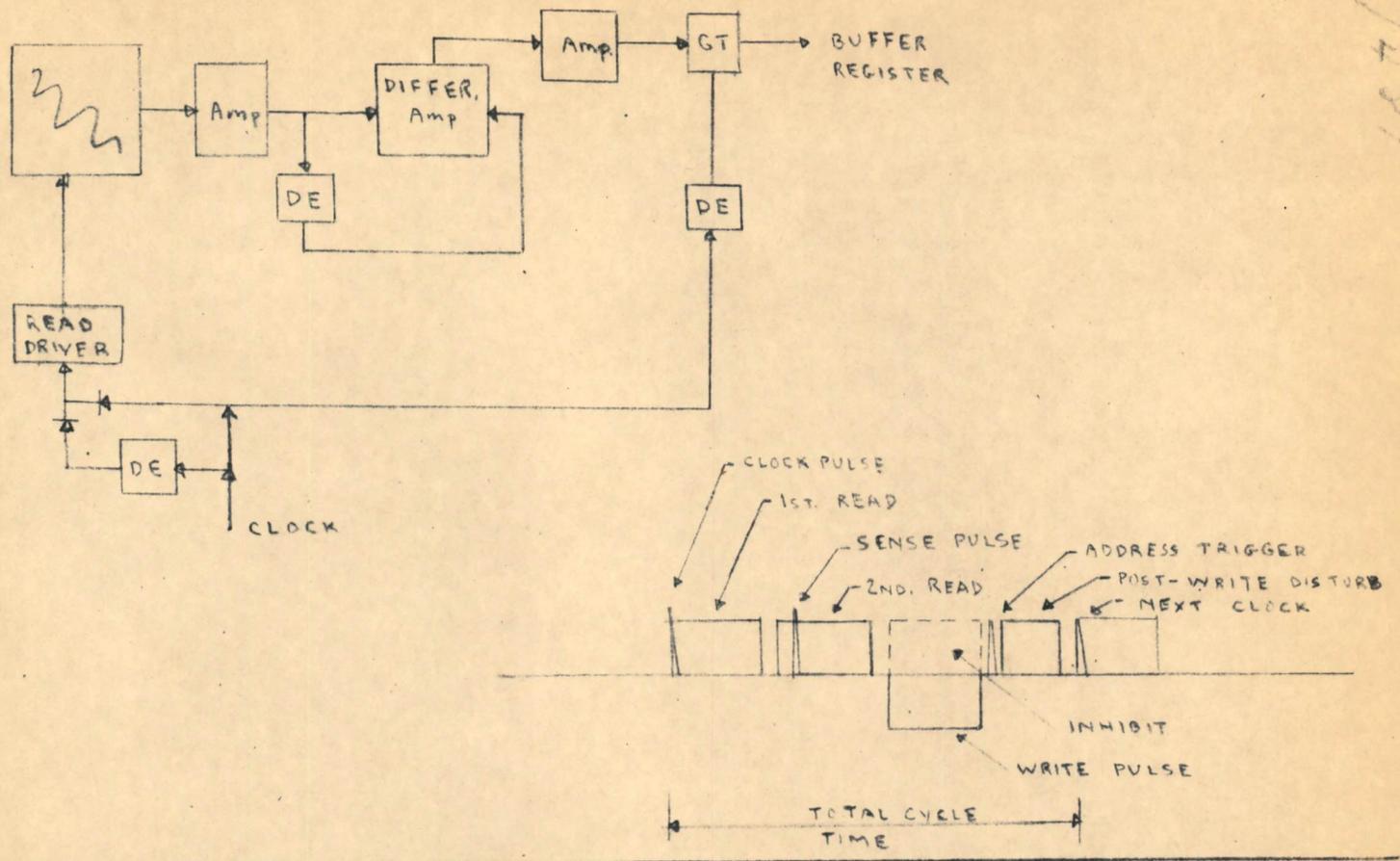
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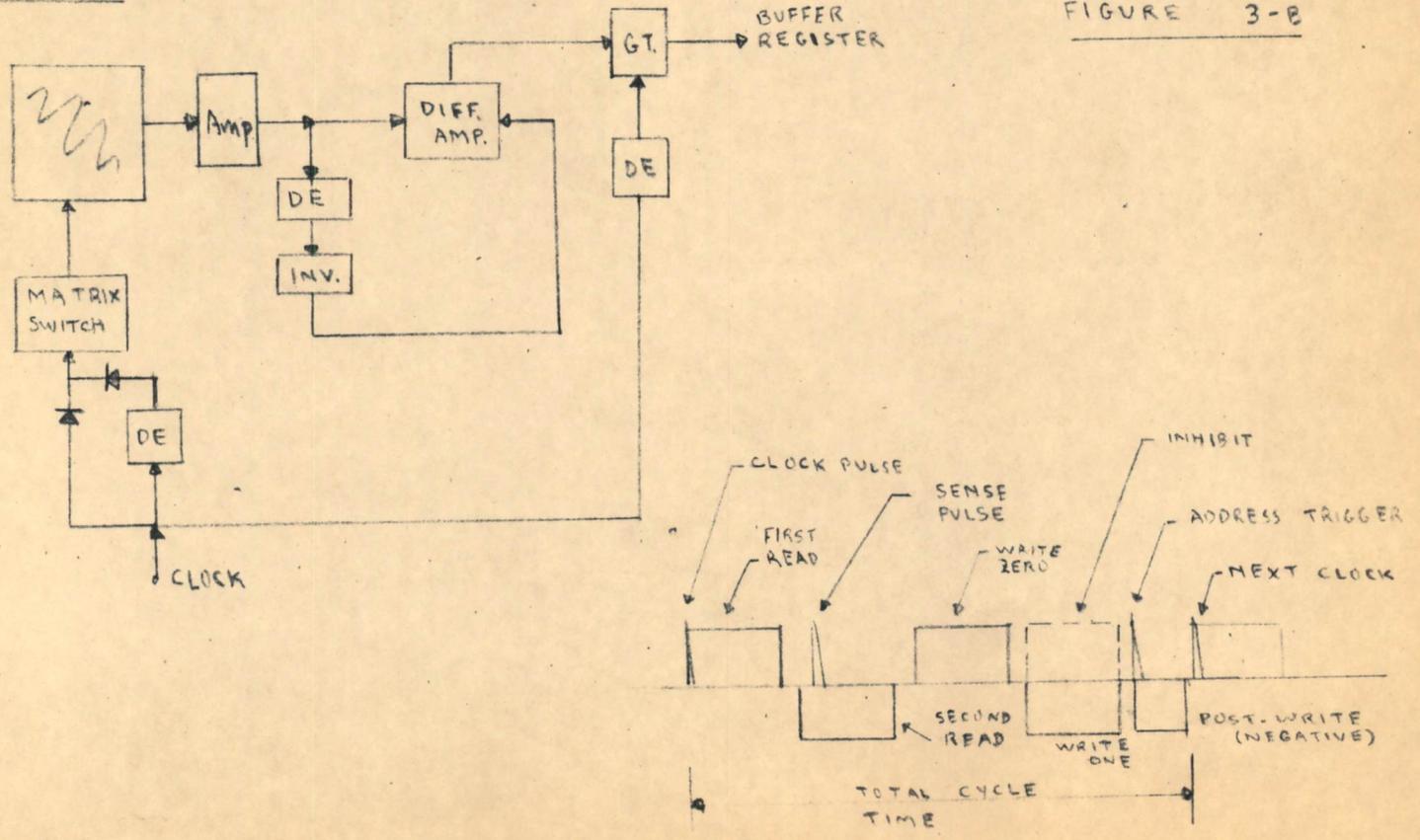
FIGURE 3-A

Scheme 5



Scheme 6

FIGURE 3-B



SA 37481

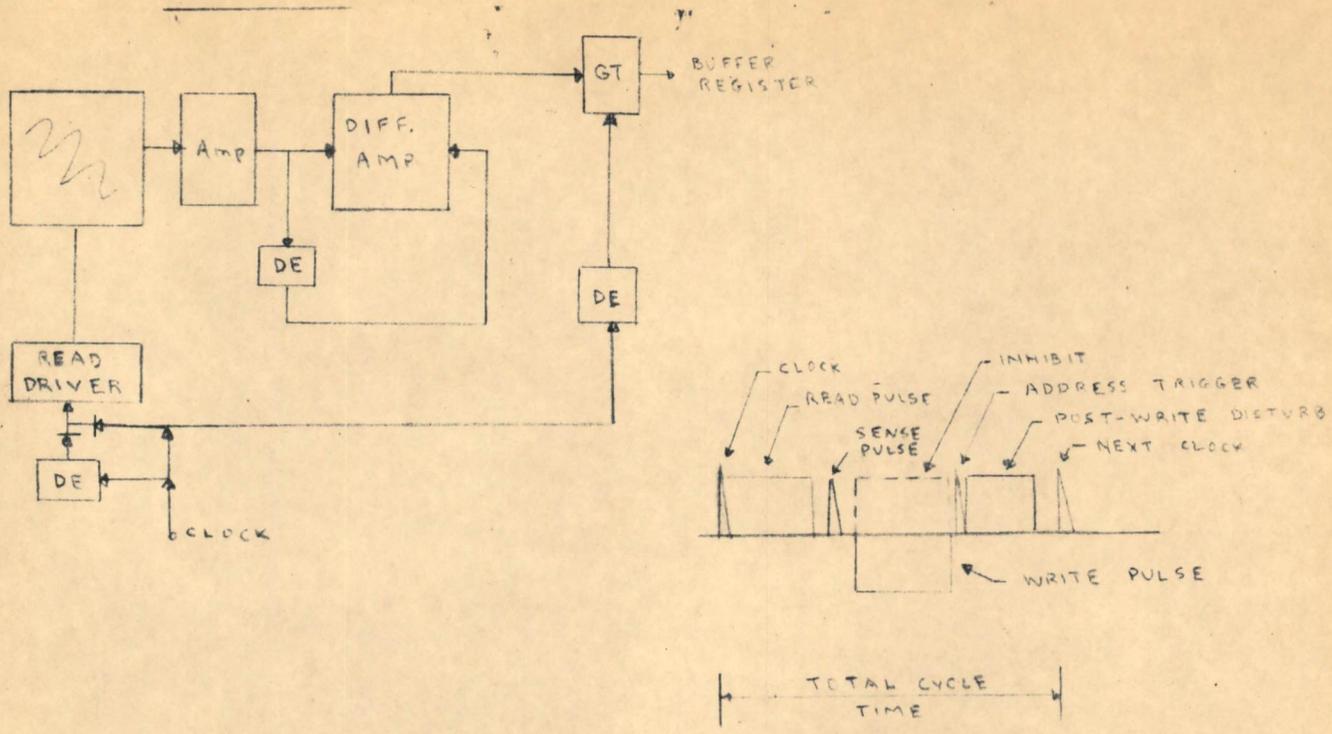
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SA-37482

Scheme 7

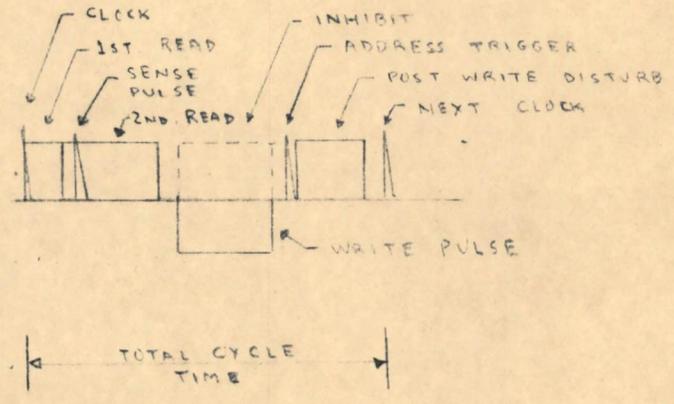
FIGURE 4-A



Scheme 8

FIGURE 4-B

SAME AS SCHEMES 3 AND 4.



SA-37482

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SA 374 23

MR = Memory Register

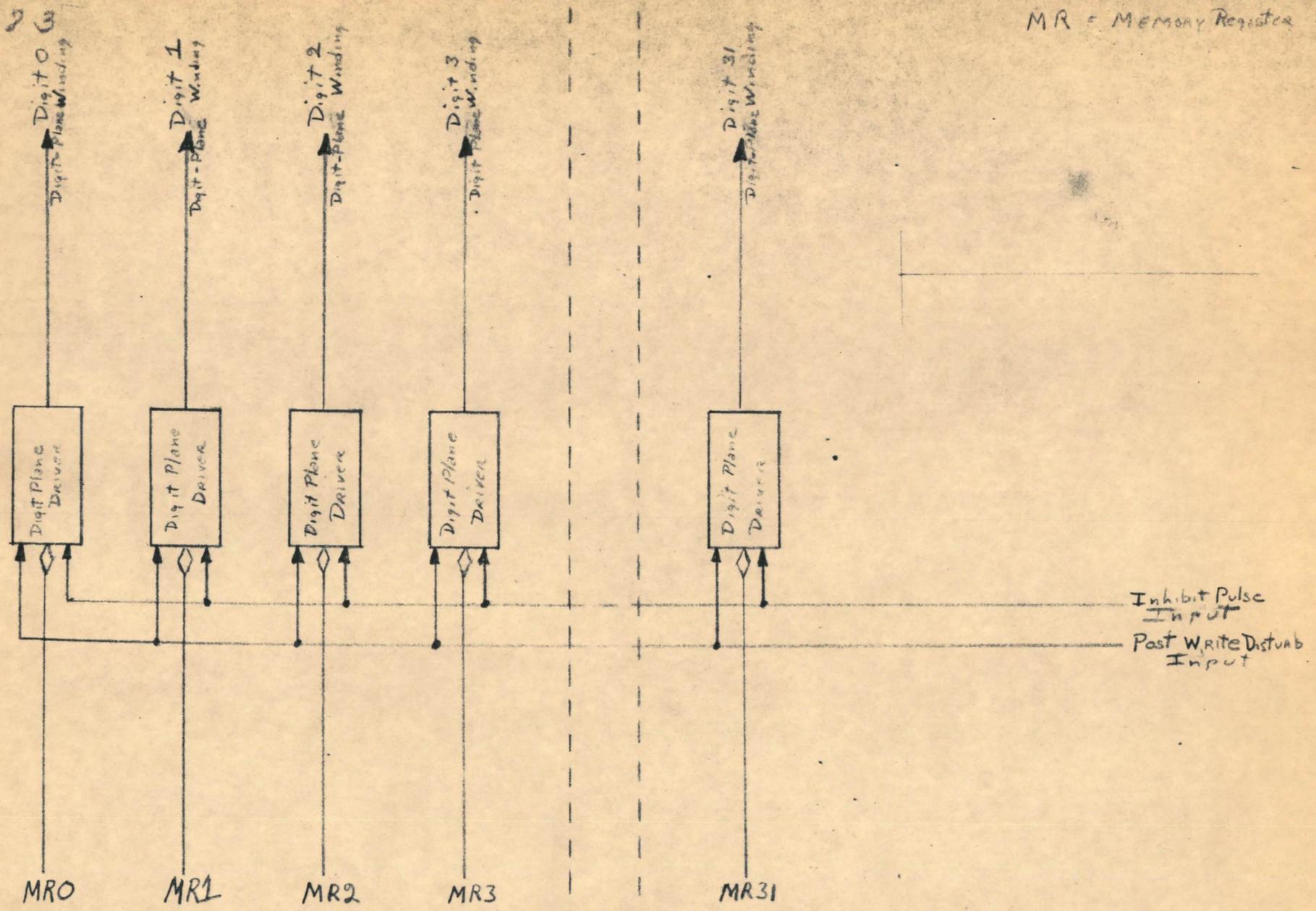


Fig. 7 SA-374 23
 Block Diagram: Digit-Plane Driving Schemes A, B, & C.

W.J. Canty, May 19, 1953

SA 37484

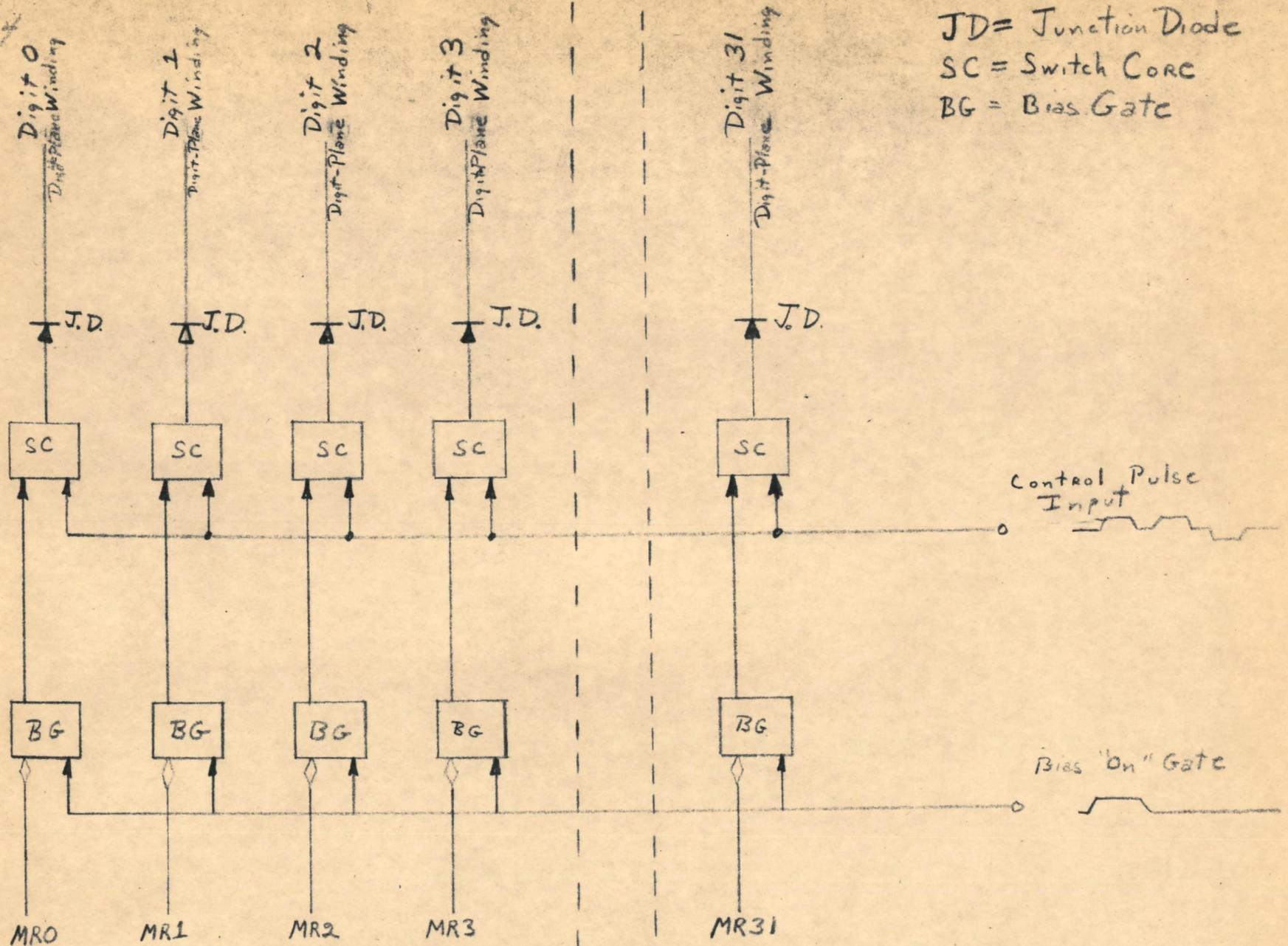


Fig. 8 SA-37484
Block Diagram: Digit-Plane
Driving Scheme D.
W.J. Canty, May 19, 1953

JUN 4 '53 AM



SA-55146

FIGURE 5

	SCHEME 1	SCHEME 2	SCHEME 3	SCHEME 4	SCHEME 5	SCHEME 6	SCHEME 7	SCHEME 8
	READ-WRITE	MULTIPLE WINDINGS	POST-WRITE	DELAYED READ	READ-READ WRITE	DOUBLE READ-WRITE	READ-DELAY WRITE	COMBINATION 3 AND 4
TOTAL CYCLE TIME	2/3 OF SCHEME 3	SAME AS 1	SPECS. REQUIRE < 6 USEC.	SAME AS 3	4/3 TIMES SCHEME 3	3/2 TO 2 TIME SCHEME 3	7/6 TIMES SCHEME 3	SAME AS 7
DELTA-NOISE REDUCTION	NONE	$\frac{2}{N}$ SECTIONS THAT OF 1	CONSIDERABLE	1/2 THAT OF 1	NEARLY COMPLETE	NEARLY COMPLETE	NEARLY COMPLETE	MORE THAN 2 OR 3
AIR-FLUX NOISE REDUCTION	NONE	SAME AS ABOVE	NONE	SAME AS ABOVE	COMPLETE	COMPLETE	COMPLETE	SAME AS 4
DRIVERS TO BE USED	ANY TYPE	ANY TYPE	ANY TYPE	ANY TYPE	VACUUM TUBE ONLY	ANY TYPE	ANY TYPE	ANY TYPE
EXPERIENCE	EXTENSIVE	NONE	EXTENSIVE	SOME	SOME	NONE	SOME	SOME
EFFECTIVE CORE UNIFORMITY	CRITICAL FACTOR	SAME AS 1	LESS THAN 1	SAME AS 1	NOT AS CRITICAL AS OTHERS	SAME AS 5	SAME AS 5	SAME AS 3
POST-WRITE DISTURB NEEDED	NO	NO	YES	NO	YES	YES (Neg)	YES	YES
NUMBER OF TUBES REQUIRED	32 TIMES NUMBER IN ONE AMP. (160)	N TIMES SCHEME 1	SAME AS 1	SAME AS 1	SCHEME 1 PLUS 2 64 (224)	SAME AS 5	SAME AS 5	SAME AS 1
ADDED LOGIC (COMPARED TO SCHEME 3)	LESS	LESS		YES	YES	YES	YES	YES
ADDED COMPONENTS (COMPARED TO SCHEME 3)	NO	N-TIMES MORE		NO	YES	YES	YES	YES
INFORMATION READOUT TIME (COMPARED TO SCHEME 3)	SAME AS SCHEME 3	SAME AS SCHEME 3		TWICE THAT OF SCHEME 3	4 TIMES THAT OF SCHEME 3	4 TIMES THAT OF SCHEME 3	3 TIMES THAT OF SCHEME 3	SAME AS SCHEME 4

SA-55146

Timing Diagram: Digit-Plane Driving Scheme D.

SA-55147

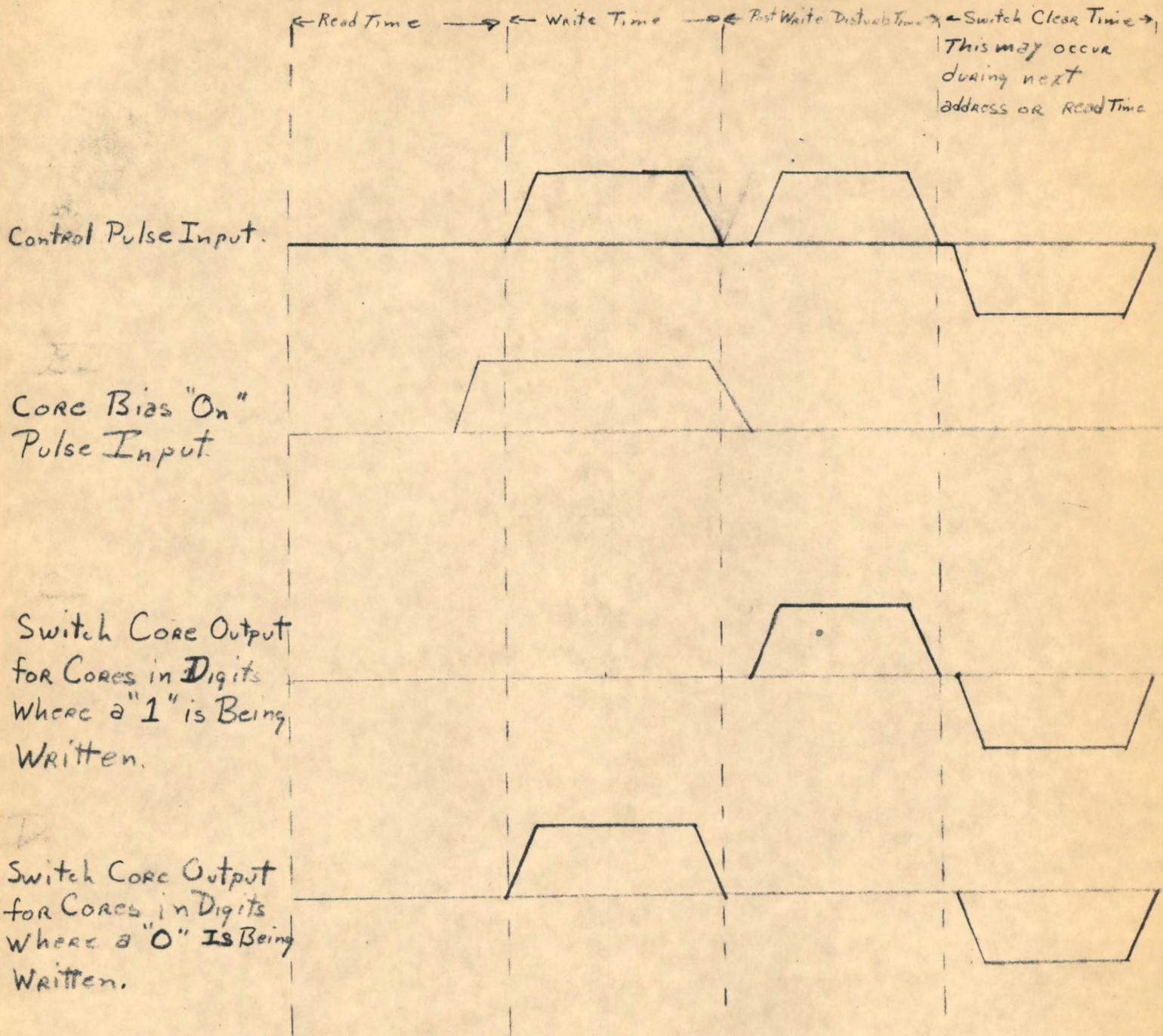


Fig. 9

W.J. Canty

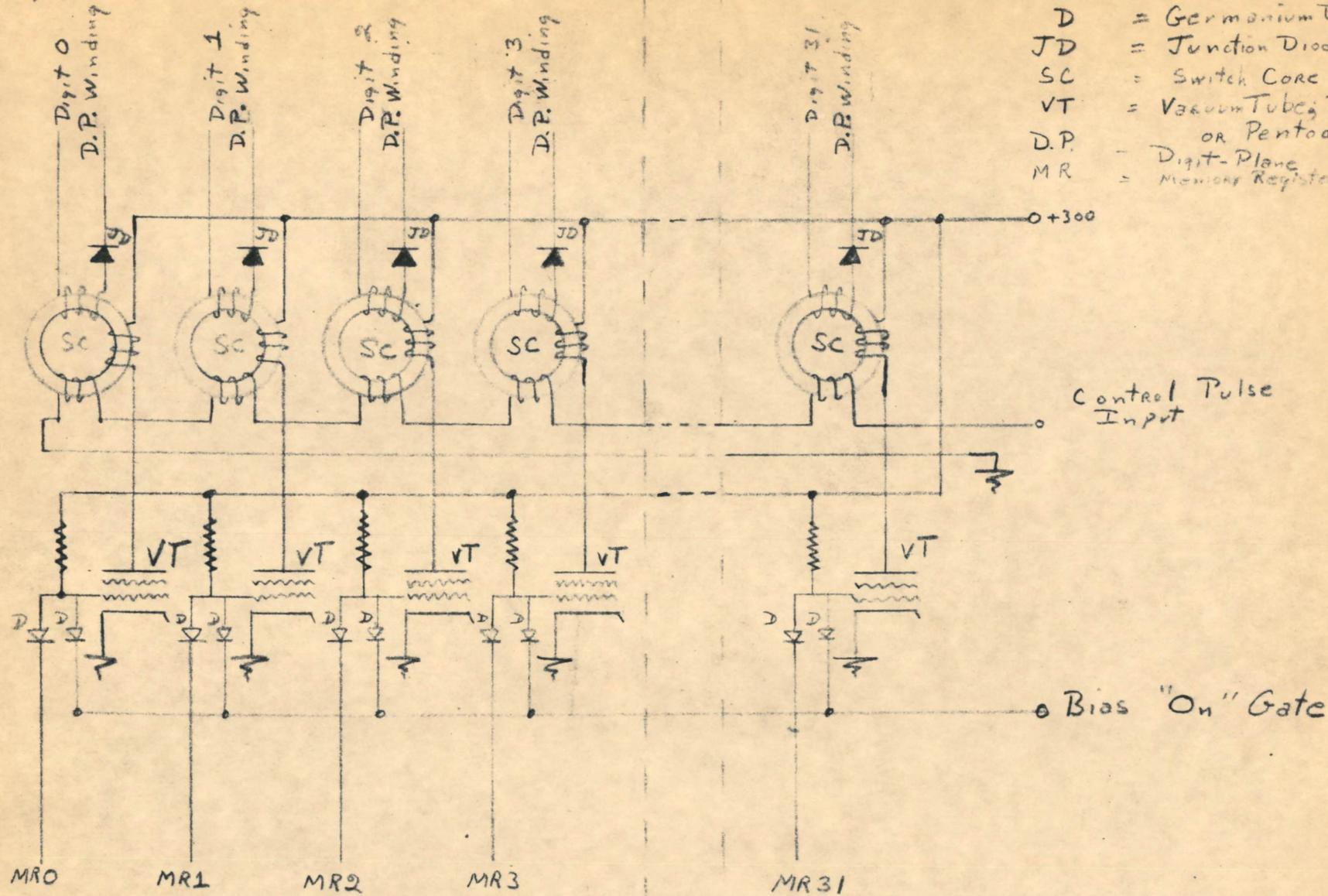
May 19, 1953

SA-55147

JUN 4 53 AM



SA-55148



- D = Germanium Diode
- JD = Junction Diode
- SC = Switch Core
- VT = Vacuum Tube, Tetrode or Pentode
- D.P. = Digit-Plane
- MR = Memory Register

SA-55148

Fig. 10
Schematic Diagram: Digit-Plane
Driving Scheme D.

W. J. Canty, May 19, 1953

FIGURE 11

	A Direct-Coupled Drivers	B Transformer- Coupled Drivers	C Transformer- Coupled Drivers with Diodes in Secondary	D Switch-Core Drivers
Experience with the system	Much experience with this system	None	None	None
Experience with components	Same as above	Fair: A little work has been gained on transformers. More work is needed. Driving circuits appear to be conventional	Fair: Same as B. Almost no work has been done with junction diodes	Fair: Experience has been gained from research on switch cores for x and y plane drivers. Almost no work done on junction diodes.
Output pulse shape	Good-can be controlled	Good	Same as B.	Can be made good by doctoring Control Pulse shape
Overshoot	Same as above	Unknown-depends on design of transformer	Same as B.	Good
Current regulation	Same as above	Appears might be good	Same as B.	Same as B
Line to line regulation	Same as above	Same as A	Same as A	Fair: may have to be controlled by selecting cores
Recovery time	Good	Poor-core must be given long time in which to recover if overshoot is to be kept small	Unknown-hoped that transformer parameters can be adjusted to give fast recovery	Good
PRF Sensitivity	Good	Subject to above	Subject to above	Good-except cores may need forced cooling to dissipate heat caused by core losses
Signal to noise ratio	∞	∞	∞	Unknown
Effect of load	Minimized by circuitry	Same as A	Same as A	Unknown
Sensing schemes not compatible with	None	No. 3 (questionable)	Same as B	None
No. of tubes per digit	5-6	4-5	4-5 plus 1 junction diode	1-2 plus 1 junction diode
No. tubes in control circuit	0	0	0	5-7
Difficulty of fabrication	Requires 32 sub-chasses for Z-plane drivers	Same as A	Same as A	Cores may be mounted on single frame Less components, faster assembly time

FIGURE 11 (CONTINUED)

	A Direct Coupled Drivers	B Transformer- Coupled Drivers	C Transformer- Coupled Drivers with Diodes in Secondary	D Switch-Core Drivers
Availability of tubes	Investigation of tube types for this use is now going on	Same as A	Same as A	Unknown
Availability of other components	Good	Good-except transformers unknown	Good-except transformers and junction diodes unknown	Good-switch cores in small quanti- ties appear to be available. Junc- tion diodes un- known.
Type of Post- Write Disturb System-compa- tible with	Any	Partial Post- Write Disturb No Post-Write Disturb	No Post-Write Disturb. Partial Post-Write Dis- turb. Probably. Full Post-Write Disturb	Same as B

Alsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: MEETING ON WWII TUBES, MAY 22, 1953

To: N. H. Taylor

From: R. S. Fallows

Date: May 29, 1953

Abstract: Certain basic circuits utilize the 7AK7 tube outside its normal operating range. A discussion of these applications and the plans to get needed tube data is covered here.

INTRODUCTION

The meeting of May 22nd between MIT and IBM circuit and tube people covered only one tube -- the 7AK7. The basic circuits involving this tube were reviewed, certain important tube characteristics were identified as essential to circuit development work, and a preliminary specification for this tube was discussed.

Present at the meeting were D. J. Crawford, H. J. Geisler of IBM and R. L. Best, H. B. Frost, H. J. Platt, S. Twicken, P. Youtz, R. S. Fallows and S. Thompson of MIT.

It was decided that characteristic information is of first priority. Both MIT and IBM will investigate suppressor grid current in the positive-grid region. Sylvania has been asked to obtain complete curves over the contemplated operating voltage ranges.

BASIC CIRCUITS

Four circuit applications were listed as contemplated uses for the 7AK7 tube. All of these operate the tube with its suppressor grid positive.

1. Low impedance, .1 μ sec pulse
Supply Voltages: $E_b = +250$ V, $E_{c3} = +10$ V, $E_{c2} = +90$ V,
 $E_{c1} = -15$ V.

Grid signal: 0.1 μ sec pulse
30 V amplitude
2 MC rep. rate

Plate load: 3:1 transformer driving 100 ohms to produce a
30 volt signal

(It was noted that screen dissipation may limit the rep. rate to less than 2 MC.)

2. Medium impedance, .1 μ sec pulse
 Supply voltages: $E_b = +150$ V, $E_{c3} = +10$ V, $E_{c2} = +90$ V,
 $E_{c3} = -15$ V
 Grid signal: 0.1 μ sec pulses
 30 V amplitude
 2 MC rep. rate
 Plate load: 1:1 transformer driving 1000 ohms to produce a
 30 volt signal.
3. Memory switch gating
 Supply voltages: $E_b = 150$ to 250 V, $E_{c3} = +10$ V, $E_{c2} = +90$ V,
 $E_{c3} = -15$ V
 Grid signal: 2 μ sec square pulse
 20 V amplitude
 30% duty factor
 Plate load: 4 - 10 K ohm resistance shunted by 15 μ f signal
 to have 40 volt amplitude with .3 μ sec rise time.
4. In-out and control gating
 Supply voltages: $E_b = +250$ V, $E_{c3} = +10$ V, $E_{c2} = +90$ V,
 $E_{c3} = -15$ V
 Grid signal: 0.5 μ sec pulse
 30 V amplitude
 Plate load: Transformer driving 100 to 1000 ohms

REQUIRED CURVES

Since basic circuit design work is still in process on the above applications, certain characteristic curves would be valuable in determining the best operating regions. Such problems as supply loading and operating margins are now a matter of circuit experimentation and results may not be typical of all tubes. In particular, the load presented by the suppressor grid when the control grid is pulsed positive may require additional cathode followers between flip-flops and gate tubes.

The following curves were listed as being of value:

$I_b, I_{c1}, I_{c2}, I_{c3}$ vs. E_b (0 to 250 V) for $E_{c1} = -15$ V to +15 V,
 $\Delta E_{c1} = 5$ V;

$E_{c3} = -15$ V to +15 V, $\Delta E_{c3} = 5$ V;

$E_{c2} = 50, 85, 90, 95, 130$ V.

It was agreed that the E_{c2} family is of interest from the point of view of marginal checking only and is of less value at present than are the E_{c1} and E_{c3} families. The curves of I_{c3} for $E_{c3} = +5$ V and $+10$ V are of particular interest. Both MIT and IBM will obtain these curves in the next week.

Roger Slinkman was contacted at Sylvania, Emporium, Pennsylvania. He indicated that the required curves can be obtained by Sylvania. This is very fortunate since neither MIT nor IBM has the required facilities.

Negotiations were started, by letter from H. B. Frost dated May 22, to have these curves obtained.

PROPOSED OBJECTIVE SPECIFICATION REVIEW

H. B. Frost presented a proposal specification for the 7AK7 modified for WWII. This specification, dated May 22, will be revised in consultation with H. J. Geisler at a later date.

LIFE TESTS

Certain life tests are indicated if the 7AK7 is to be used in the basic circuits discussed above. It was agreed that work on these tests should be postponed until the basic circuits are more firmly established.

Signed: Richard S. Fallows

Richard S. Fallows

RSF:mt

Approved: Arthur P. Kromer

Arthur P. Kromer

CC:

IBM

D. J. Crawford
H. J. Geisler
J. A. Goetz
N. P. Edwards

MIT

R. L. Best
H. B. Frost
H. J. Platt
S. Twicken
P. Youtz
A. P. Kromer
S. Thompson

W. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: MARGINAL CHECKING AND TROUBLE LOCATION

To: N. H. Taylor, J. M. Coombs

From: R. S. Fallows

Date: June 1, 1953

Abstract: A committee has been formed to work on marginal checking and trouble location for WWII. Their first meeting is reported.

Introduction

The purpose of this memo is to document the formation of a committee to investigate the methods of marginal checking and trouble location to be used in the WWII computer. The committee consists of I. Aronson, R. Fallows, and R. Pfaff of MIT and P. Beeby and L. Walters of IBM.

This committee met for the first time on May 27th and formulated the following initial program.

Scope of Activity

The mission of the committee is to investigate the problems associated with marginal checking and trouble location as they apply to the WWII computer and to reach a first proposal for a complete maintenance system. It was agreed that certain equipment involved in the physical part of the system will affect the physical design of the computer and should receive first attention of the committee.

It is assumed that the time required for routine preventive maintenance must be kept to a practical minimum. Therefore, automatic marginal checking coupled with check programs will form the core of the maintenance system.

The committee will start with the present logical design and basic circuits. By way of reasonable restriction, they will not recommend changes in logic or circuitry unless they are of great value in servicing.

It is expected that the present investigation will be restricted to the following:

1. The main frame of the computer, including control.
2. High-speed memory
3. Power supplies
4. The marginal checking equipment itself

Purpose of Marginal Checking and Trouble Location

There are three major objectives to be accomplished by the marginal checking and trouble location system.

1. Determine the reliability of the entire computer at least once a day.
2. Provide for the logging of the operating condition of all circuits, in logical groups, to accumulate data on deteriorating components.
3. Facilitate location and isolation of faulty components.

Equipment and Methods to be Considered

The following physical or logical devices were listed as having a possible place in the marginal checking and trouble location system.

1. Voltage variation
2. Check register (either a special register or a computer register)
3. Test storage
4. Indicator lights (and camera)
5. Display scope
6. Audio indicator
7. Manual controls on the maintenance console
8. Memory parity check

9. Flip-flop complement lines
10. Diagnostic programs
11. Reliability programs
12. Line-at-a-time recording (card, tape, printer, etc.)
13. Cyclic program control (with delayed stop and automatic restart)
14. Control bit (for use with diagnostic programs)
15. Sense instruction
16. Identity check or branch-on-zero instruction
17. Check instruction (wave of 1's or 0's)

Proposed Initial Program

In order to arrive at some needed early decisions on the marginal checking equipment to be used with WWII, the committee decided to restrict their attention, at first, to certain areas which affect the physical design of the computer. These areas are the following:

1. Voltage variation
2. Test storage
3. Indicator lights
4. Check register
5. Flip-flop complement lines
6. Manual controls on the maintenance console
7. Power supply
8. Check programs or orders as they affect 1 thru 6

It was agreed that recommendations on all of these subjects are desirable as early as possible. However, for a first aim, items 1 and 8 are probably as much as we should

expect to cover in the next month.

Announcement

By this memo, we the committee invite any and all parties who have information or recommendations relative to the subject under investigation that they communicate with a member of the committee in the near future -- before our proposal is submitted.

Signed: *R. Fallows*
Richard S. Fallows

Approved: *AP Kromer*
Arthur P. Kromer

RSF:tl

cc:

IBM

MIT

M. M. Astrahan
P. Beeby
J. M. Coombs
R. P. Crago
D. J. Crawford
N. P. Edwards
H. Ross
L. Walters

H. Fahnstock
I. Aronson
J. Gano
R. Pfaff

A. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MEMORY TEST COMPUTER TOGGLE-SWITCH STORAGE AND TOGGLE-SWITCH STORAGE SWITCH

To: MTC Engineers

From: John D. Crane

Date: May 29, 1953

Abstract: Toggle-Switch Storage in MTC provides 32 registers of storage with a capacity of 16 binary digits per register. Selection of a register is accomplished by use of a 32 position Toggle-Switch Storage Switch.

It is possible to substitute a live register (Flip-Flop Storage) for any of the 32 registers.

A digit schematic of Toggle-Switch Storage, MTC, and the associated gates, flip-flops, and cathode followers is shown in SD-55005.

Toggle-Switch Storage Switch

It is the function of the storage switch to select the register of storage contained in the address section of the A-Register.

The Toggle-Switch Storage Switch consists of a 32-position diode-matrix switch driven by 10 cathode followers and 5 flip-flops. The address to be selected is read into the Toggle-Switch Storage flip-flops from 5 gates connected to the A-Register ONE bus. These 5 flip-flops are connected to 10 cathode followers which drive the 32-position diode-matrix switch. The output levels of the flip-flop are 0 and -40 volts. From the output of the cathode followers, the d.c. levels are applied to the inputs of the 32-position switch whose outputs are 31 non-selected lines (-35 volts), and one selected line (+2 volts). Registers are numbered 0 through 31. Register 31 is selected when all 5 flip-flops are in the ONE position. See SD-55005. Flip-flop FFO is the least significant digit.

Toggle-Switch Storage

Toggle-Switch Storage provides 32 registers of storage. Information stored in the toggle switches can be set or changed by setting the switches, which are accessible to the operator at the console.

Toggle-Switch Storage is located in the Toggle-Switch Storage panel which contains toggle switches, crystal diodes, and cathode followers. See SD-55005. All toggle switches are DPDT's and all crystals are 1N38A's.

From the outputs of the 32-position switch, lines are connected to the inputs of 32 Toggle-Switch Storage cathode followers. The d.c. levels are shifted by the cathode followers so the selected line is +6 to +8 volts and the non-selected lines are -28 to -30 volts. This variation in output voltages results from a difference in load when many toggle switches are changed. Two typical input lines are shown as line 16 and line 31 on SD-55005.

Following the cathode followers, the first switch in the line, S 16, chooses either the Toggle-Switch Storage Register or the live register. If S 16 is in the NO position, the live register is substituted in place of a Toggle-Switch Storage Register by applying the +6 to +8 volt d.c. level to the live-register detection gate.

Placing S 16 in the NC position allows the +6 to +8 volt d.c. level of the selected register to be applied to the grid of cathode followers (digits 0 through 15) whose associated toggle switches (S0 through S15) are closed. Any cathode follower not having access to this +6 to +8 volt level will have its grid at the -28 to -30 volt level, so a binary number can be placed in a register by controlling d.c. levels with toggle switches. Crystal diodes are placed in series with each switch to isolate the selected line from the 31 non-selected lines.

The input to the cathode followers is either +6 to +8 volts or -28 to -30 volts, depending on the position of the toggle switch between the grid of the cathode follower and the selected line. Toggle switch out-gates, which receive their suppressor grid voltage from the outputs of these cathode followers (digits 0 through 15), are connected to the A-Register to provide the means for getting information from Toggle-Switch Storage to the A-Register.

For each set of 8 registers, one crystal diode is placed in series with each of the digit outputs. These diodes are shown in the circuit schematic for Toggle-Switch Storage, MTC, E-54259, but they are not included in the digit schematic, SD-55005. Their main function is to increase the back resistance seen by the cathode follower which is at +6 to +8 volts.

Signed John D. Crane
John D. Crane

Approved Kenneth H. Olsen
Kenneth H. Olsen

JDC:jrt

Drawing attached: SD-55005

Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

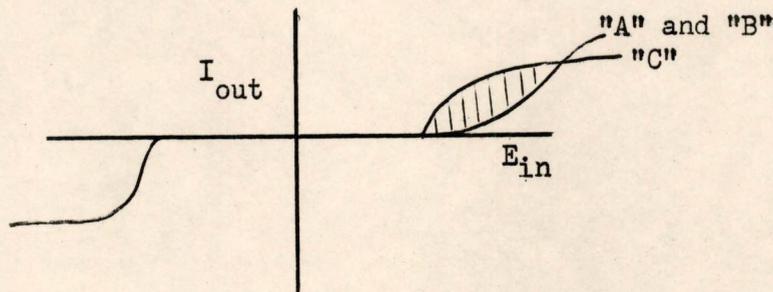
SUBJECT: WWII BASIC CIRCUITS - LOW SPEED LEVEL INVERTER (16)

To: N. H. Taylor, A. H. Nelson, Group 62 Section Chiefs,
Vellum to D. Crawford at I.B.M. via A. P. Kromer

From: J. S. Gillette

Date: June 1, 1953

I have investigated three possible cathode clamping circuits which may be used with low speed level inverters and amplifiers. These circuits are shown on the attached drawing No. A55181. Circuits "A" and "B" are similar in operation. Circuit "C" was selected on the basis of its transfer characteristic. (See sketch below).



The design margins are being obtained and will be studied. The total rise and delay time and the total fall and delay time is of the order of one microsecond. This circuit should be capable of delivering three milliamps of "And" current and three milliamps of "Or" current. The value of the output stage's cathode resistor can be varied to change the distribution of available output current between the "And" and "Or" conditions.

A tentative schematic is included with this report.

Signed

J. S. Gillette

J. S. Gillette

Approved

R. L. Best

R. L. Best

JSG:jrt

Attached drawings: A55181
A55182

Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: ESTIMATED PARTS LIST FOR SCOPE DEFLECTION AMPLIFIER

To: N. H. Taylor, R. A. Nelson, Group 62 Section Chiefs,
and vellum copies to D. J. Crawford and W. Triest at
IBM via A. P. Kromer.

From: Henry E. Zieman

Date: 5 June 1953

Since a specific CRT has not yet been decided on, definite amplifiers have not yet been designed. For magnetic deflection, an amplifier similar to SB53854 will be used with each of the 715C tubes replaced by two 4 x 150 A. For electrostatic deflection (K1187P-) the amplifier will be similar to the magnetic deflection amplifier with the deflection coils replaced by plate resistors which go to a high B+ (1250V). For a dual deflection tube (EX 4566 P7M), the same amplifier mentioned above will be used for positioning the spot magnetically, and a simpler a-c coupled amplifier using 5965 tubes throughout will be used for writing electrostatically.

Two amplifiers will be used in each scope (one vertical and one horizontal). At present it is planned to use a total of 75 scopes, making a total of 150 amplifiers.

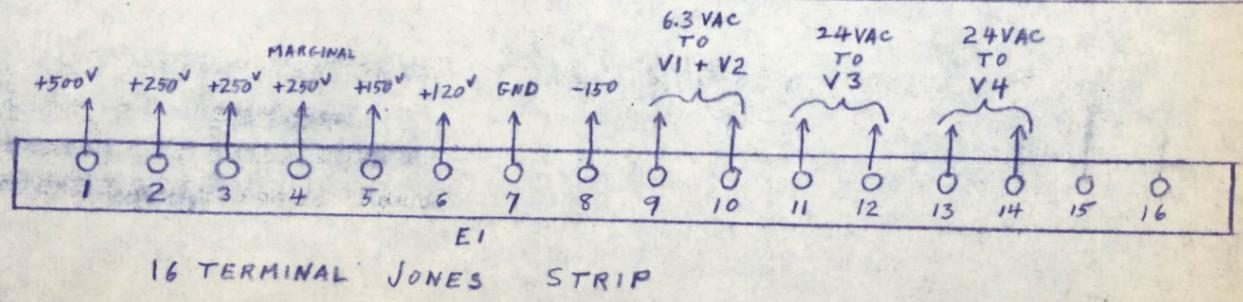
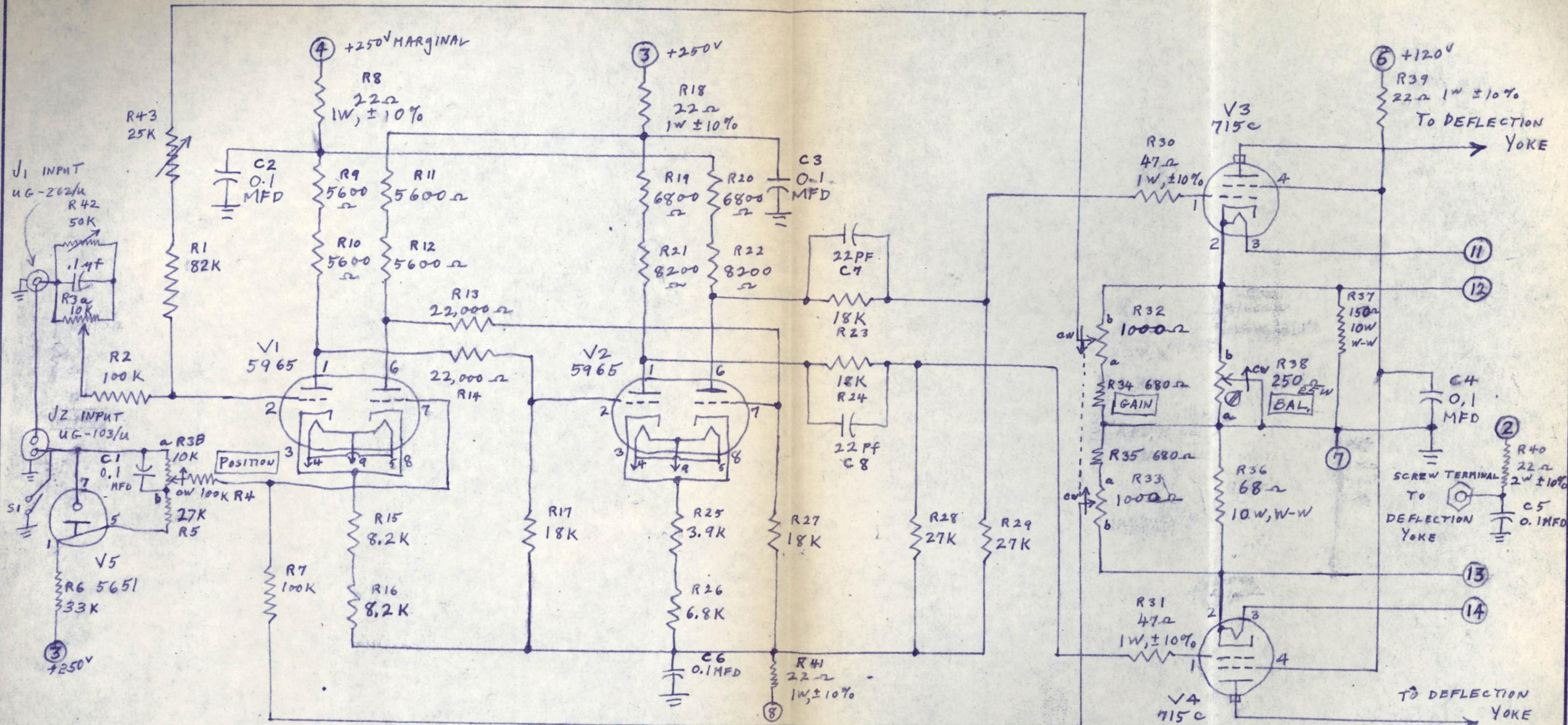
Signed Henry E. Zieman
Henry E. Zieman

Approved R. L. Best
Richard L. Best
Section Leader

Approved N. H. Taylor
Norman H. Taylor
Group Leader

Drawing attached: SB 53854
HEZ:gn

SB-53854



10	9	8	7	6	5	4	3	2	1
CHG.	HE Ziman	DATE	12/2/53	APPD.	HE Ziman	CN#			

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
 DIGITAL COMPUTER LABORATORY
 DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO.

Deflection Amplifier, Scope Unit, WWI

SCALE: DR. *HE Ziman*

ENG. *HE Ziman* CK. APPD. **SB-53854**

H. Olsen

Memorandum M-2218

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SPECIFICATIONS ON IMPROVED INTENSIFICATION AMPLIFIER

To: N. H. Taylor, R. A. Nelson, Group 62 Section Chiefs,
and vellum copies to D. J. Crawford and W. Triest at
IBM via A. P. Kromer

From: Henry E. Zieman

Date: 5 June 1953

Figure SB-55242 is a schematic of a new intensification amplifier which incorporates the new High-Speed Flip Flop (see E-543) to improve the reliability of the present system. Since a new display tube has not yet been decided on, the output voltages of this circuit are expected to be similar to that of the present system. When a new tube is finally decided on, the output of this circuit will have to be modified to fulfill the requirements of the new tube.

One of these units will be required for each scope and at present it is planned to have 75 scopes.

Signed: *Henry E. Zieman*
Henry E. Zieman

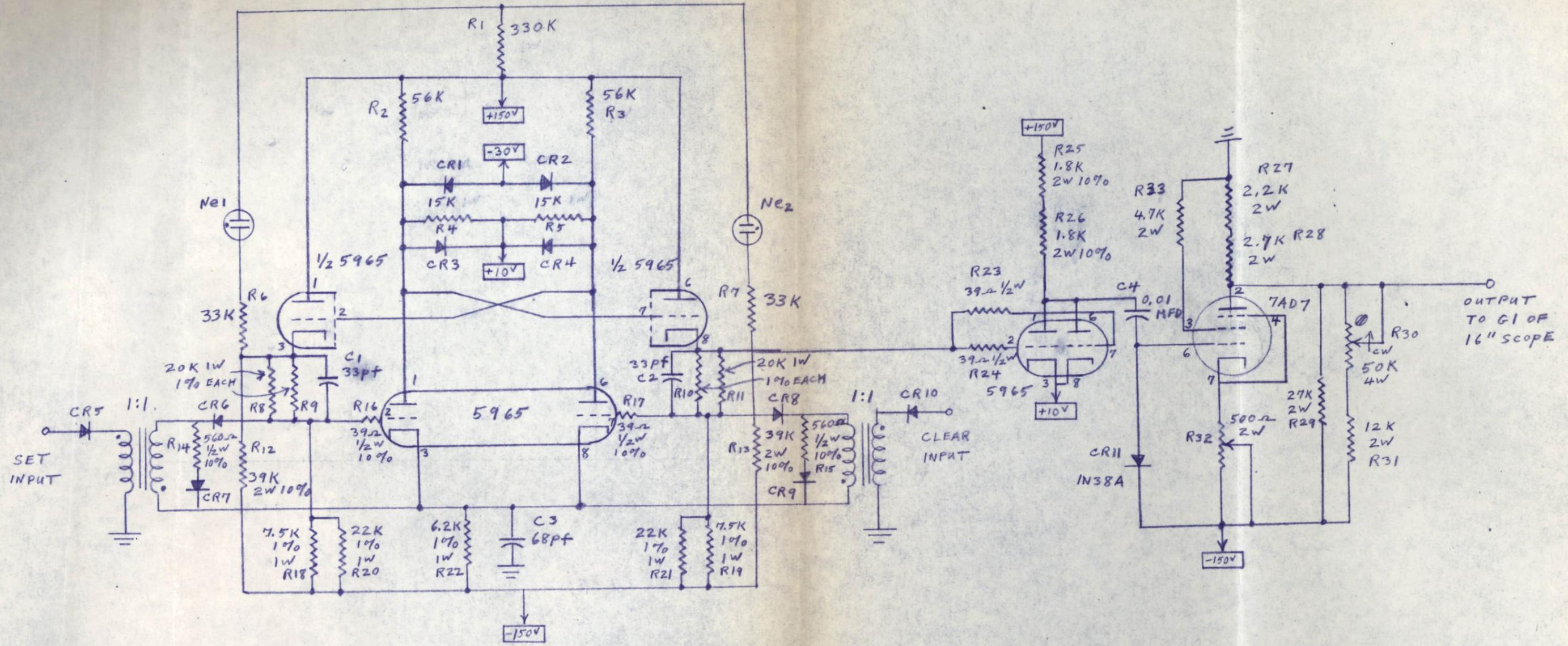
Approved: *R. L. Best*
Richard L. Best
Section Leader

Approved: *N. H. Taylor*
Norman H. Taylor
Group Leader

HEZ:tl

Drawing Attached: SB-55242

B-55242



NOTE:
 1. ALL CRYSTALS ARE IN34A
 2. NEON BULBS ARE 1/25 W
 3. ALL RESISTORS ARE 1W 10% UNLESS SPECIFIED

						MASSACHUSETTS INSTITUTE OF TECHNOLOGY DIGITAL COMPUTER LABORATORY DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO.		
						INTENSIFICATION AMPLIFIER		
						SCALE:	DR. <i>H. E. Zeman</i>	
						ENG. <i>H. E. Zeman</i>	CK.	APPD.
						SB-55242		

R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: TESTING OF INDIVIDUAL CORES IN MTC MEMORY PLANES

To: N. H. Taylor

From: A. D. Hughes

Date: June 16, 1953

Abstract: The 32 x 32 magnetic-core memory planes for MTC were constructed from cores tested and sorted on a production basis. To obviate the possibility of defective cores, each core was retested after it had been wired into a memory plane. A device was constructed to enable the operator to send current pulses through each core in a plane and observe the output. The necessary test equipment was arranged to provide the pulses and allow measurement of the outputs.

No defective cores were found. The test showed that the limits of output voltage at the sensing time used were $\pm 17\%$. Five cores with outputs outside of these limits were replaced. Taking into account that the variable factors inherent in testing and equipment are $\pm 5\%$, the cores in each plane are within approximately $\pm 20\%$ limits.

Definition of Terms

The magnetic memory for MTC consists of 17 memory planes. Each plane has 1024 magnetic cores wired at the intersections of 32 pairs of vertical wires and 32 pairs of horizontal wires (see Memorandum M-2225, "The Construction of Memory Planes for MTC Memory," E. A. Guditz, June 10, 1953). These vertical and horizontal wires are called the x and y windings, respectively. The completed plane also includes both a sense winding and a Z-plane winding, each of which passes through each core.

The tester being described is called the plane tester. The tester used to select cores for the planes is called the production tester.

Reason for Test

Least completed planes mistakenly include defective cores rejected by the production tester or cores damaged in construction, it was decided to retest the individual cores in each memory plane after completion of the x and y windings.

Defective cores could then easily be replaced before the Z-plane and sense windings were added. A retest also gave the limits of the ONE-disturbed output voltages or the percent difference between the highest and lowest cores in the plane. (An incidental result here was a correlation of plane-tester outputs with those of the production tester.)

Actual testing of the planes showed three common errors in construction of the x and y windings:

1. Any cores out of proper 90° angle with their neighbors;
2. Failure of any x or y wire to go through any core;
3. Improper connection of the pair of x or y windings to the correct terminals.

Such errors were easily corrected before addition of the Z-plane or sense windings.

Method of Test (see Fig. 1)

Testing each core in the array was accomplished by using the x windings for driving and the y windings for sensing. One y winding was connected to a scope so that the ONE-disturbed output of any of the 32 cores on that winding could be observed. The driving current was then connected to all the x windings in succession, until each of the 32 cores on the y winding had been tested. The sensing connection was then moved to the next y winding, and the procedure repeated until the output of every core in the array had been measured. Only one of the pair of x windings need be used for the driving current since the current drivers supply both negative and positive pulses over the same wire. Using only one of the x windings for the driving current considerably speeds the testing procedure, since a rig was devised which makes it very easy for an operator to shift the driving current quickly from one x wire to the next. The device (Fig.1) provides a spring wire which can be moved to make contact with any of the x windings on one set of terminals. The other connection at the opposite side of the plane is a common wire connecting all of the x terminals. The movable spring-wire connection and the common wire are connected to the source of driving current. The sensing or output connection merely connects the ends of one given y winding into a coaxial cable, which is fed into the scope. The device provides a means of testing the plane using one of the pairs of x windings and one of the pairs of y windings which pass through each core. So that the others of the pairs of x and y wires may be used, the test device is reversed and the plane retested. Although one test is sufficient to detect a bad core, the second test gives a double check and completes a test of all the x and y wires of the plane for possible construction errors. The entire test can be completed in about 2 hours.

Test Setup (see Fig. 2)

To drive the cores, a train of pulses which simulates actual operating conditions is used. The positive pulses are provided by two Mod. VI core drivers and the negative pulses by two Mod. V drivers. The logic used to drive the system is the same physically as that used with the production tester. (An Engineering Note by J. W. Schallerer which will describe the Production Tester is being written.) Calibration of the current amplitude is provided by a 60-cycle a-c/d-c chopper calibrator mounted with the test setup. The current which drives the cores goes through a 1%, 10-ohm resistor. The voltage across the resistor is then fed to the current calibrator. Calibration of the scope for reading the output voltage is provided by the same calibrator used with the production tester, which gives a continuous 200-millivolt, 400-cycle, square wave. Fig. 2 shows two cables on input 1 at the scope, one for voltage calibration and the other for current calibration. Actually, either one or the other is connected, but not both. Since the scope is easily calibrated, the test operator can read the output of each core directly from the scope face, which is marked off with the proper division lines.

Also included with the test setup is a delay-line panel which provides a pulse to intensify the output disturbed-ONE pulse at the desired read time. The d-c voltage for the test setup is provided by a regulated power supply. This is to insure, in particular, no drift of the current drivers.

Driving Current

Most of the test was designed to be consistent with the production tests, since, in effect, it was desired to show that no really bad cores had been passed by the production tester. However, since the production tester uses a semi-infinite current-pulse length, it was decided that a pulse length closer to the one MTC would use would give a better test. The read and write driving currents used, including the disturb pulses, were 1.5 microseconds in length, measured from 10% of the maximum at the rise to 10% of the maximum at the fall. At the beginning of the test it was not known exactly what pulse length would be used for MTC. It was decided, however, that a 1.5-microsecond pulse length was probably the minimum that could be used. Since then, a 2-microsecond pulse length was decided on for MTC, but the tests were continued at 1.5 microseconds, for consistency. The current rise time used for the tests was the same as that used for the production tester, 0.2 microseconds.

The current amplitude used was the same that was used with the production tester, 920 milliamps for read and write pulses and 460 milliamps for half-selected pulses. This seemed to be optimum driving current and gave consistent results.

Output

The output for each core in the plane was displayed on the scope. Five important traces were observed, disturbed ONE, disturbed ZERO, write ONE, half-selected ONE, and half-selected ZERO. The traces which were significant for the tests were the disturbed ONE and disturbed ZERO. The disturbed ZERO was found to

have decayed to zero at sensing time for all cores tested. The disturbed-ONE output was measured at the same sensing time for all cores. The sensing time was determined by taking the average peak time for a large sample of cores. This turned out to be 0.52 microseconds after the read driving current pulse had reached 10% of its full value. The delay-line panel mentioned above was used to intensify the disturbed-ONE trace on the scope at 0.52 microseconds for easy reading.

Results

It was found early in the tests that the variation between the lowest and the highest disturbed-ONE output for a given plane was about 34% at its minimum. It was decided that +17% would comprise the basis for acceptance of cores in a given plane. That is, any cores whose output at sensing time was outside of the limits prescribed were considered bad cores. The average output per core was 0.115 volts. The acceptable limits, then, were 0.095 volts and 0.135 volts. Cores replaced were as follows:

<u>Plane</u>	<u>Core Output</u>	<u>Next Closest Core in Plane</u>
6	0.093 volts	0.097 volts
9	0.092	0.097
10	0.138	0.135
10	0.093	0.098
10	0.096	0.098

The 0.096-volt core in Plane 10 was replaced since it happened to be on the same x winding as the 0.093-volt core.

It should be emphasized that there were no cores in all 17 planes tested which were actually bad cores, mistakenly placed in the planes. Those cores which were replaced, were found to be satisfactory, although marginal, when retested on the production tester. As mentioned above, important results of the tests were the detection of errors of construction in building the arrays. About one third of the planes tested had such a construction error.

The production tester accepted cores between 0.105 volts and 0.125 volts whereas the plane tester found the range to be 0.095 volts to 0.135 volts. The difference was probably due to several factors, one of which was the difference in driving-current pulse lengths. Another was a difference in sensing time (0.67 microseconds for the production tester, 0.52 microseconds for the plane tester).

A third factor was the noise in the plane being tested and general difference in physical setups between the plane tester and production tester.

Validity of Results

Each plane was considered as a separate unit. Core outputs in any given plane were tested for spread for that plane alone. Since MTC has a separate sensing amplifier with variable gain for each plane, considering each plane separately seemed to be a valid criterion. Differences in core outputs throughout a given plane, regardless of distribution, were disregarded, providing the outputs fell within the desired limits. The time and effort involved and the variation in availability of large numbers of cores prevented the construction of planes with an even distribution of core outputs or putting cores of closest outputs in the same planes.

Control of parameters involved in driving current was as close as practicable. However, variations in results were inevitable due to such variations in parameters. The greatest cause of error resulted from variations in amplitude of driving current. A 5% change in driving-current amplitude will produce approximately a 25% change in output. Considering all the parameters, i.e., rise time, pulse width, and amplitude of driving current, plus variations in the oscilloscope and the calibrators, the worst variation in core outputs in any given plane would be approximately +20%.

Conclusions

1. The most distinct advantage of testing a plane before Z-plane and sense windings are added is in incovering construction errors when correcting such errors is simple.
2. It is believed that the test will definitely show any cores which are bad.
3. The quality of the present core-selection system was good enough so that no bad cores were found in 17 planes, of 17,408 cores selected as good.
4. The cores in each memory plane at the driving currents used for the tests have a worst-output variation of approximately +20%.
5. The plane tester performed the function for which it was designed. Further improvements and tests would overlap core production tests and tests given the planes before their use in MTC.

Signed A. D. Hughes

A. D. Hughes

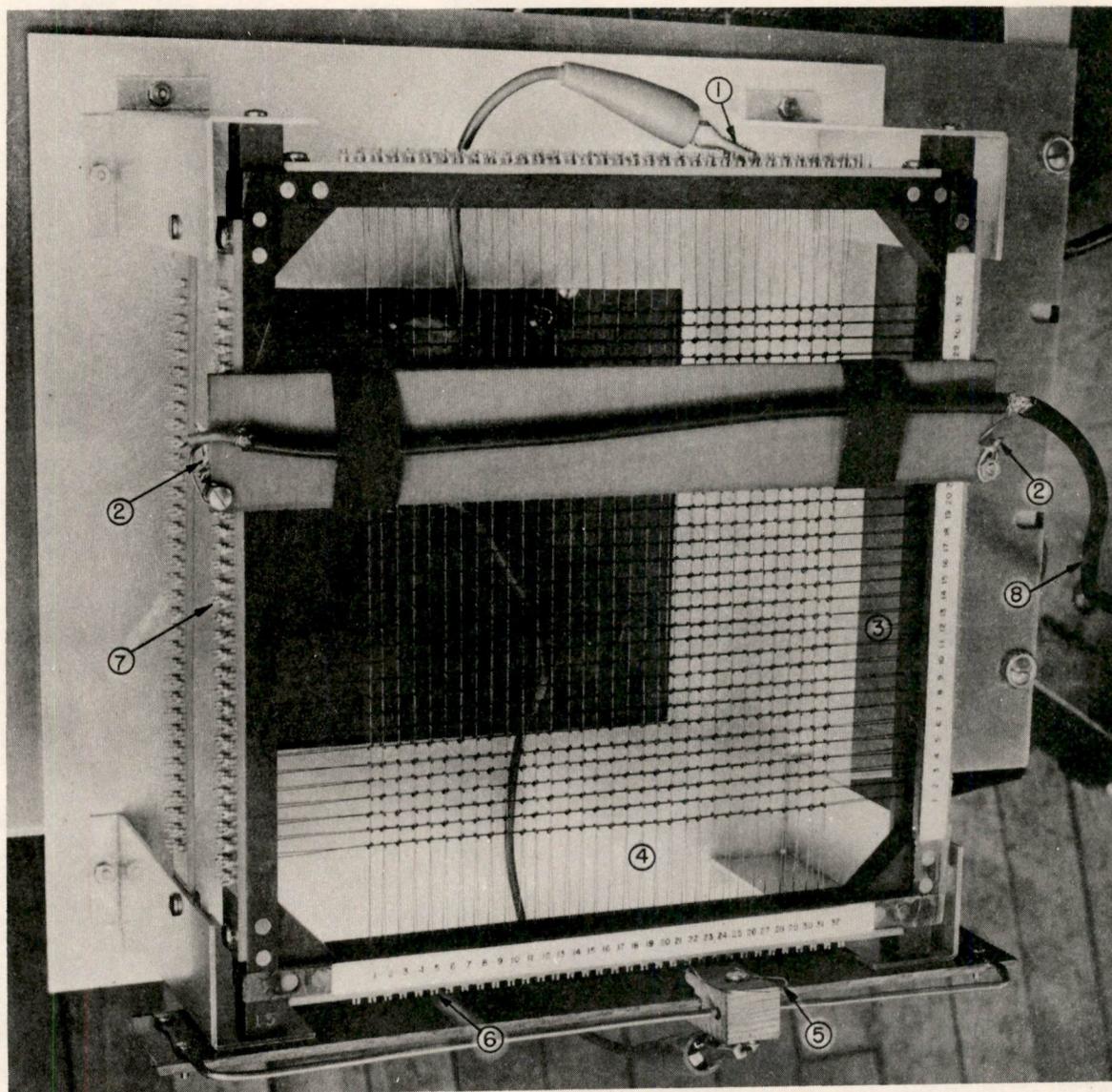
Approved W. N. Papian

W. N. Papian

ADH:jrt

cc: Magnetic Memory Section
 J. H. McCusker
 J. W. Schallarer
 N. Edwards
 R. Horn

Attached drawings: A-55166
 A-55167

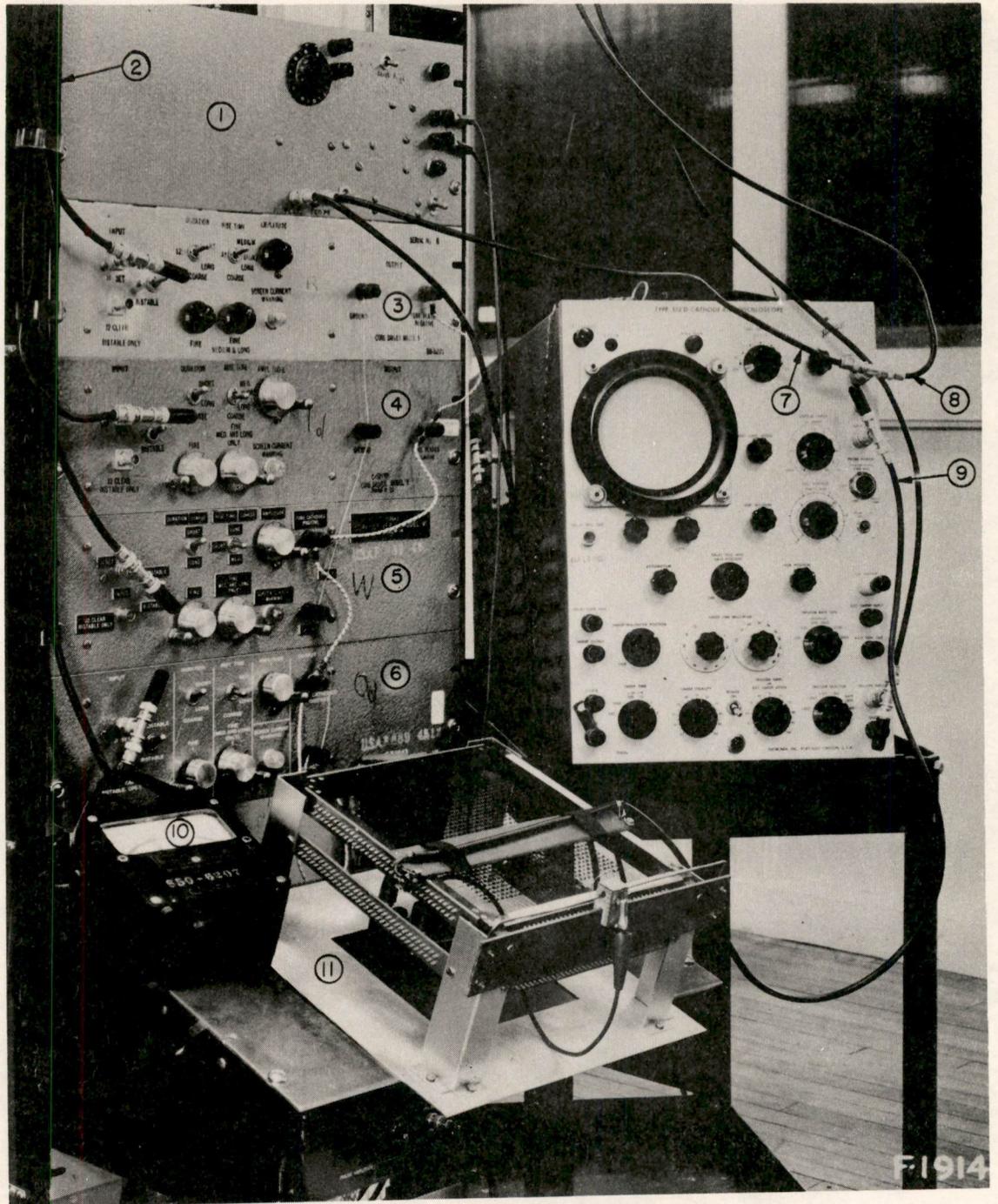


- | | |
|---|---|
| ① DRIVING CURRENT CONNECTION
TO COMMON OF X WINDING
TERMINALS | ⑤ MOVABLE SPRING WIRE
FOR X WINDING DRIVING
CURRENT |
| ② SENSING CONNECTIONS TO
Y WINDINGS | ⑥ X WINDING TERMINALS |
| ③ Y WINDINGS | ⑦ Y WINDING TERMINALS |
| ④ X WINDINGS | ⑧ TO SCOPE FOR OUTPUT
MEASUREMENT |

FIG. 1

M.T.C. PLANE ON TEST DEVICE

A-55166
F-1915



- ① CURRENT CALIBRATOR
- ② CABLES FROM PRODUCTION TESTER LOGIC
- ③ READ CURRENT DRIVER
- ④ HALF AMPLITUDE READ CURRENT DRIVER
- ⑤ WRITE CURRENT DRIVER
- ⑥ HALF AMPLITUDE WRITE CURRENT DRIVER
- ⑦ CURRENT CALIBRATION SIGNAL
- ⑧ VOLTAGE CALIBRATION SIGNAL
- ⑨ OUTPUT SIGNAL
- ⑩ VOLTMETER FOR CURRENT CALIBRATION
- ⑪ MEMORY PLANE ON TEST DEVICE

FIG. 2

M.T.C. MEMORY PLANE TEST SETUP

A-55167

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: A MAGNETIC CORE TEST STORAGE

To: N. H. Taylor

From: K. H. Olsen

Date: June 15, 1953

Abstract: The toggle-switch test storage units in WWI and MTC use large numbers of crystal diodes and vacuum tubes. A much simpler unit might be possible using a modified magnetic matrix switch which will both select the words and isolate the outputs. Only one core per word will be needed.

The WWI-MTC Toggle-Switch Storage

In the WWI and MTC toggle-switch storage units, crystal diodes are used both to select the words and isolate the outputs. In the MTC units, there are over 700 crystal diodes and 60 cathode followers.

Magnetic Test Storage

The proposed test storage consists of a magnetic matrix switch, the type described in R 211. A four-word unit is illustrated in the accompanying drawing. The selection flip flops with their buffers saturate all but the selected core. During the readout operation the driver pulses all the cores; the one which is not saturated switches and a voltage is induced across all its windings. Each digit output is in series with one output winding on each core. Each output winding can, however, be bypassed by a toggle switch which is in one position to represent a "zero" and in the other to represent a "one". Induced pulses will, therefore, come from a given digit only if the toggle switch for that digit of the selected word is in the "one" position.

Both selection and isolation are accomplished using only one core per word of storage. Each core will have a large number of windings but the cores can be large with many turns in the driving windings because operation of test storage need not be fast.

Signed


Kenneth H. Olsen

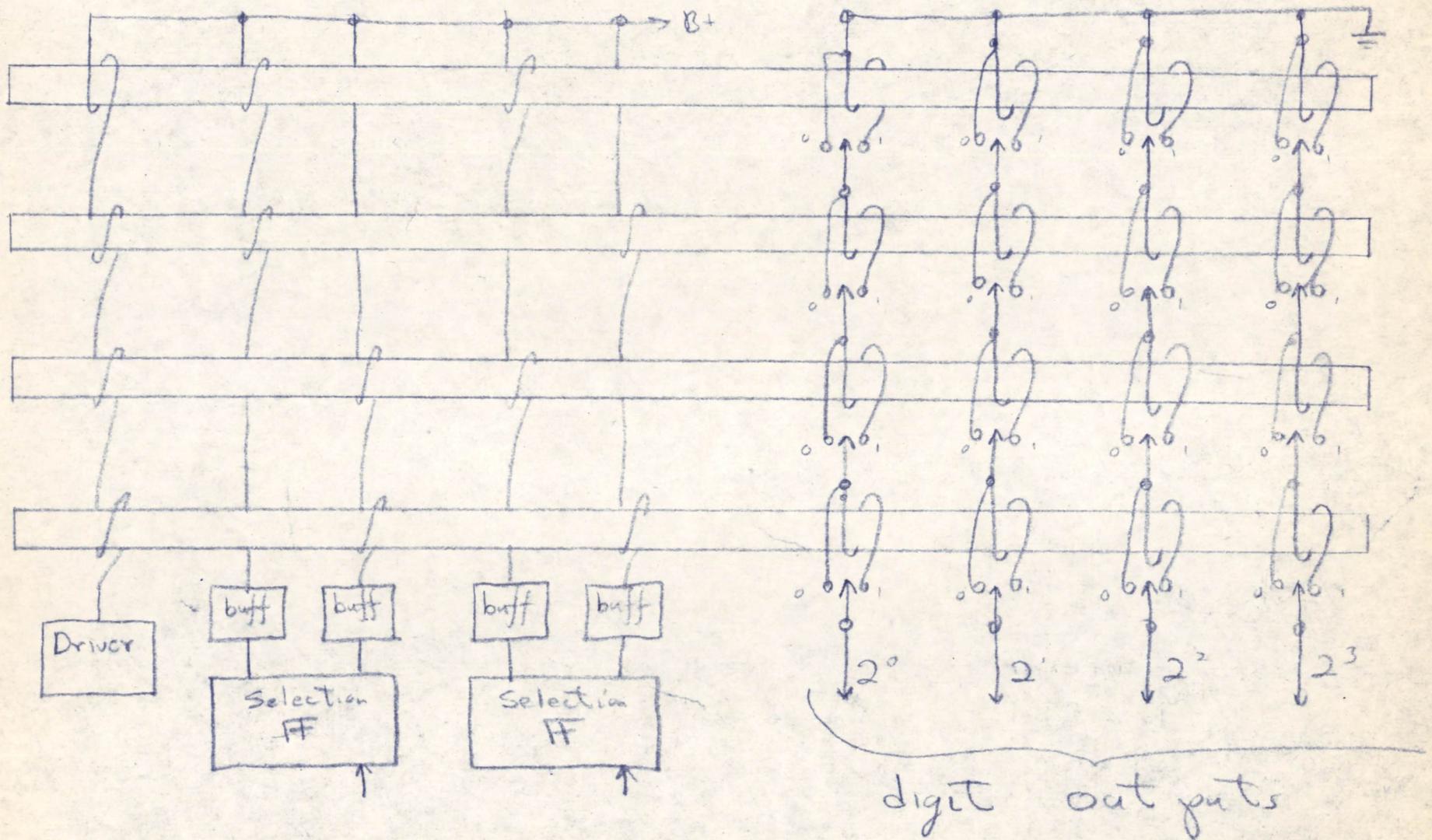
KHO:hpm

Attached:

Drawing No. SA-55295

cc: R. R. Everett - W3-413
H. Ross - I.B.M.
D. Crawford - I.B.M.

SA-55295



A 4 Word Test Storage Using Magnetic Cores for Selection and Isolation

SA-55295 ✓

H. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: BENDIX RED BANK DIVISION TUBE PLANT

TO: N. H. Taylor

FROM: R. S. Fallows

DATE: June 15, 1953

ABSTRACT: As a result of J. W. Forrester's recommendation to Mr. M. A. Babb of Bendix and Mr. J. A. Goetz of IBM that there may be a place for Bendix in the tube development activity of Project Lincoln, contact has been established and an engineering evaluation has been made.

Introduction

I attended a meeting in Poughkeepsie on June 9th at which M. A. Babb, W. C. Coldwell, R. R. Meijer and W. C. Wyman of Bendix presented the Red Bank Division's position. J. A. Goetz and H. J. Geisler of IBM presented the WWII tube problems and discussed the project procurement status. The Bendix position is briefly stated as follows:

1. Bendix Management issued a request to the Red Bank Division (possibly other divisions also) that an effort should be made to get into the Lincoln Project activities as soon as possible.
2. The Tube Plant of the Red Bank Division is a job shop for developing and making high-quality special-purpose tubes.
3. They would be interested in a development contract, development followed by limited production (up to 20,000 tubes per month), or, simply, limited production in the capacity of a second source of supply. However, they prefer development jobs.
4. They appear to be ready to start work immediately, since their facilities are just being completed and are not yet filled.

The meeting at Poughkeepsie made it clear that Bendix could fit into the WWII tube development program. Thus, it was followed by a visit to Red Bank to inspect facilities and evaluate the Bendix engineering and production potential.

Plant and Facilities

On June 12th, H. John Geisler, H. Bonnell Frost, Pat Youtz and I visited the tube plant near Red Bank, N. J. A more complete appraisal of the facilities and manpower at Bendix can be obtained from Frost or Youtz.

The plant is small compared to most tube plants. Mr. Babb (Plant Manager, Electron Tubes) explained their plans for revising the layout and expanding the plant as business builds up. He pointed out that the work in Red Bank Division to date has been directed toward building an organization with experience in doing the most difficult tube jobs in the industry. For example, they have redesigned and are producing the 2K50 (K-band low voltage, local oscillator) and the 2C51 (a difficult miniature twin-triode).

The tube group of Bendix moved from Teterboro, N.J. to Eatontown, N.J., about a year ago. The facilities are still incomplete, but the plant is a working unit. Emphasis has been on gas tubes, microwave tubes, and high-reliability tubes (power supply and receiving types) with emphasis on hard glass, rugged designs, and good early-life reliability. One feature of their designs is a heater insulated with ceramic tubulations, which they feel has virtually eliminated the problem of heater-cathode shorts.

In general, we were impressed with every feature of the Red Bank Division's tube plant.

The organization is built around a few key people in each department. These key people all appear to be expert in their specialty. In particular, Mr. John H. Wyman, who is Chief Project Engineer on receiving type tubes, is a very capable all-around tube engineer.

The working group seems to be built of mature, conscientious people who have been trained in the attitude and methods needed in assembling and processing first-quality tubes. There was no hurry or casualness apparent anywhere in the plant.

The equipment in each department includes the best that is available. The people know how to use this equipment and what its limitations are.

The working areas are the cleanest I have seen outside a laboratory -- in fact, they compare well with many laboratories. The practices followed in each department were in accord with the best that could be recommended.

General Discussion

We discussed the 5965, 7AK7, and core-driver tubes. Specs for the WWII versions of the first two tubes were left at Bendix (for information only). Bendix wants our business on almost any terms, but the terms on which they would like to work are of particular interest. Mr. Wyman expressed their desires as follows:

1. Bendix would like to start with a development contract for any of these tubes.
2. This is a somewhat new field to them and they can not guarantee results; however, they would give the job their best effort.
3. By working very closely with MIT and IBM tube engineers, they think that, if the necessary knowledge is available within our three organizations, they can come as close to satisfying our requirements as is possible. (This presents an ideal relationship which, I think, no other company has wanted to establish.)

Mr. Wyman's estimate of the time involved to develop one of these tubes sounds a bit optimistic. He quoted two to three months to study the problems and work up several designs, perhaps two to three months to try several designs, and about four months to make up dies and tools, giving a total of less than a year. He pointed out, however, that he had not studied our specs carefully and that our life test requirements might increase development time considerably.

We specifically asked if Bendix would consider production only as second source for the 7AK7. Mr. Babb said, "We have been told to get into the Lincoln Project wherever we can fit." Mr. Wyman estimated that Bendix could get into business producing an established design (with tool designs and parts available from the prime manufacturer) in five to six months on a "crash" basis if necessary.

With reference to long life operation of tubes, Mr. Wyman said that bulb temperature is a prime factor. He said that he thought 4 watts total dissipation for a tube like the 5965 is a safe rating only if air cooling keeps the bulb temperature to 80° C maximum.

Conclusions

The electron tube plant of Bendix Red Bank Division is an ideal contender for consideration in the development of long-life high-reliability tubes for computer use. They should also be viewed as a very promising producer of such tubes in quantities up to 20,000 per month. However, it is difficult to see how they fit into the WWII tube program at this time.

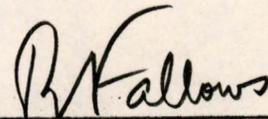
They could be considered as a second bidder on the improved 7AK7. However, it should be pointed out that Sylvania is in a preferred position since they developed the original tube and have made it for several years. Also, we have a certain moral obligation to Sylvania because of their long devotion to our unprofitable cause.

In the case of the improved 5965, we are already well involved with G.E. who have experience with the original tube. We do not have time to start further discussions with Bendix. Also, I have the impression that Frost and Youtz consider R.C.A. at least equal to Bendix with reference to this tube.

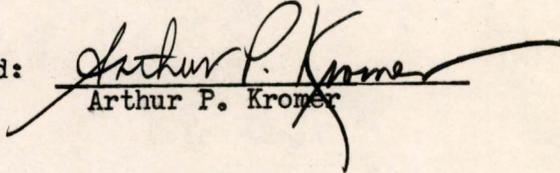
It may turn out that Bendix could be considered for development of the core-driver tube. However, we can not spell out the exact requirements at this time, and we will certainly have to spell out our requirements in terms of a tube which is already being produced by someone.

We left Bendix with the understanding that we will report our evaluation to the planning and procurement people at MIT and IBM. They, in turn, will contact Bendix. We predicted that this would occur in about two weeks.

Signed:


Richard S. Fallows

Approved:


Arthur P. Kromer

RSF:smmt

CC: H. B. Frost
P. Youtz

Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: JOINT MEETING ON PACKAGING OF WWII

To: N.H. Taylor

From: W.H. Ayer

Date: June 17, 1953

PRESENT

IBM

M.M. Astrahan
P.A. Beeby
P.P. Crago
D.J. Crawford
N.P. Edwards
W.F. Hughes
J. Montgomery
H. Ross
B.L. Sarahan
D.B. Thompson

MIT

Irving Aronson
W.H. Ayer
S. Best
S.H. Dodd
R.R. Everett
J.F. Jacobs
A.P. Kromer
K. Olson
R.J. Pfaff
N. Taylor
C.W. Watt

The meeting was opened by Harold Ross of IBM who presented the latest recommendation for the number of types of pluggable units and the types of tubes in each. A combination of six and nine tube units was broken down into five different types as follows:

<u>Type</u>	<u>No. of Circuit Types</u>				<u>Estimated No. used</u> <u>in central machine</u>
A	1-FF	2-GT	1-CF	1 Spare	160
B	1-FF	1-GT	2-CF	1 Spare	80
C	1-FF	3-GT	3-CF	1 Spare	80
D		6-GT			
E		9-GT			

These five units are used to make up all the registers except those that count such as the adder, program counter, address register and I/O control counter. The requirement of a spare gate tube and a spare socket in each digit of each register is satisfied and the redundancy of components made necessary by the use of only five pluggable units is held to 15%. The meeting voted to accept this proposal and to allow the mechanical design group to proceed with the design of a six and a nine tube pluggable unit.

J. Montgomery presented sketches of a new pluggable unit design, and demonstrated a sample frame containing two pluggable units. A discussion of the redesigned 701 plug that will be used touched on the following features: sequencing, locking, contact life and contact spacing. A comparison with the Amphenol Blue Ribbon connector showed that both plugs can be made to do the job with equally good results, providing the time and money are available for tooling. It was decided that a new 701 type design would be used on the pluggable units since it meets all the requirements and will probably be available much sooner. It also has the advantage of a self contained locking scheme.

A discussion of the method of component mounting to be used in the pluggable units resulted in the following voluntary assignments. H. Ross and D. Crawford will inform J. Montgomery of their decision regarding the inclusion of the 2 watt 1% resistor in the high speed flip flop circuit or its replacement by two 1 watt 1% resistors. D. Thompson will make up as many sample pluggable units as necessary to establish standard physical layouts for the basic circuits.

J. Montgomery followed up his discussion of the pluggable units with a brief description of the proposed bay design, including the location of air ducts, pluggable units, and power distribution equipment. It was agreed that each vertical stack of pluggable units would contain units of only one size, either 6 tube or 9 tube. Agreement was also reached on the bay size, which will be one pluggable unit wide. Two bay sizes will be produced, for six and nine tube units. These will be permanently assembled in any order desired, on a base or skid that will be approximately six feet long.

H. Ross presented the current thinking on the physical breakdown of the central machine. Seven main cabinets will be used as follows:

1. Left arithmetic element
2. Right " "
3. Control
4. Program Control
5. Maintenance and control console
6. Memory #1
7. Memory #2 (IF DESIRED)

He also presented diagrams showing a suggested arrangement of the registers within the frames and the number of connecting cables.

Signed: W.H. Ayer

W.H. Ayer

Approved: A.P. Kramer

A.P. Kramer

P. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: TESTS OF SOME MAGNETIC-MATRIX SWITCH OPERATING MODES

To: N. H. Taylor

From: J. L. Mitchell, R. S. DiNolfo

Date: June 17, 1953

Abstract: There are two independent questions that must be answered when choosing a switch operating mode:

1. Should the "set" and "reset" windings take part in the selection operation?
2. Should the "bias" drivers be gated?

The tube counts indicate the "set" and "reset" windings should not take part in the selection operation. The duty factor requirements on the "bias" driver indicate the "bias" drivers should be gated. The experimental results obtained from two different operating modes show that the tube count should determine the operating mode.

Introduction

The magnetic matrix switch is being considered as a device to select and drive the "selection" planes in a magnetic-core memory, its main advantage being that it greatly reduces the number of tubes and other components required in a memory-address selection system. This advantage stems from the fact that the magnetic-matrix switch performs two jobs: it translates the address from the base 2 to the selection-coordinates^{base} and it drives the memory selection planes with the desired current pulses. The fact that the switch is a dual-purpose device enables us to make tremendous savings in equipment over systems that use separate translators and drivers. For example a system using a crystal-matrix translator and vacuum-tube drivers requires 564 tubes and 768 crystals to operate a 4096-register memory, while a magnetic-matrix switch system requires only 104 tubes and 128 switch cores to drive the same memory.

A "n" position magnetic-matrix switch is made up of "n" magnetic cores threaded with three types of windings as shown in Fig. 1. There are a number of "bias" windings which, when excited, select the desired core by biasing off all but the selected core. In addition, there is a "set" winding and a "reset" winding; driving the set winding switches the selected core

and causes this core to produce a voltage pulse; driving the "reset" winding resets the selected core to its original state.

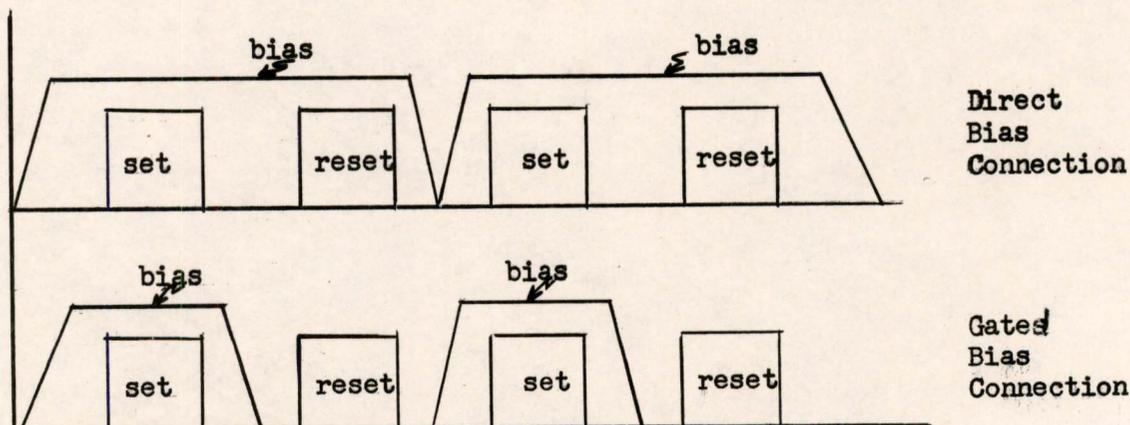
There are many different modes in which a magnetic matrix switch can operate; however, in this note only a few of these modes will be considered. In the discussion of the modes of operation, two independent questions arise:

1. Should the "set" and "reset" windings take part in the selection of the core?

The "set" and "reset" winding configurations can be arranged so that the only function of these windings is driving the selected core (the selection operation is performed by the "bias" windings); the winding configuration can be arranged so that these windings not only drive the selected core, but also take part in its selection.

2. Should the "bias" drivers be gated?

The "bias" drivers can be connected directly to the outputs of the address flip-flops, or gate tubes may be interposed between the flip-flops and the drivers. By adding the gate tubes the duty cycle of the "bias" drivers can be reduced. A timing diagram showing the switch input pulse sequence for the two types of "bias" driver operations is shown below.



Timing Diagram for Switch Input Pulses

Description of Operating Modes

In the first mode of operation to be considered the switch has a "set" winding, a "reset" winding, and a full set of "bias" windings as shown in Fig. 1. The "set" and "reset" windings pass through all the cores and do not take part in the selection of the desired switch core.

In the second mode of operation the switch has two "set" windings, (which now take part in the selection process), a "reset" winding, and a set of "bias" windings minus two as shown in Fig. 2. Each "set" winding goes through half the cores, and the high-order selection is done by pulsing only one of the "set" windings. The highest-order address flip-flop determines which "set" winding is pulsed. The "reset" winding is the same as the previous case.

In the third mode of operation the switch has a "set" winding, and a full set of "bias" windings, as shown in Fig. 3. The "set" winding goes through all the cores and does not do any of the selection. One pair of "bias" windings does double duty, that is they supply both the "bias" and the "reset" pulse to the memory. This is possible because there is only one core in the switch that has to be reset. This core is always on the "bias" winding that is connected to the nonselected side of the flip-flop; in other words, the core is on the one of a pair of "bias" windings that was not driven during the set operation.

In the fourth mode of operation the switch has two "set" windings and a full set of "bias" windings minus two as shown in Fig. 4. The "set" operation is the same as in system number 2 and "reset" operation is the same as in the system number 3, described above.

The "bias" drivers can be connected directly to the memory-address flip-flops or they can be gated with any of the four above-mentioned systems. If the "bias" drivers are connected directly to the flip-flops the drivers must be able to operate at a 100% duty cycle; but, if gate tubes are interposed, the duty cycle can be reduced, and as a result the driver-tube specifications can be relaxed.

Estimated Tube Counts

The tube and winding counts shown in Fig. 5 are made on the following assumptions:

1. The gate tubes are independent units and are counted as such.
2. The "bias" winding drivers would be made up of two tubes, a buffer amplifier and a driver.
3. The "set" and "reset" drivers would be made up of 7 tubes, a 6-tube buffer amplifier and a driver tube. The large number of tubes is necessary for pulse shaping and current regulation.

After looking at Fig. 5, it is clear that no saving in the number of driving tubes is made by using one of the more sophisticated driving systems. The only saving is in the number of windings on the switch core, the maximum saving being two windings. The gates added between the address flip-flops and the "bias" drivers increase the total number of tubes required, but on the other hand, the duty cycle of the "bias" driving tubes will be reduced from 100% to about 50%.

Test Results

Memory Test Setup IV was built up so that a switch could be tested under two different modes of operation. The system consisted of two 16-position magnetic-matrix switches made up of MF 1118, F262 cores which drove a 256-register, 2-digit memory made up of MF 1326 B, F291 cores. Each switch selected and drove the "selection" planes along one co-ordinate axis. This switch was set up so that it could be operated with one "set" and one "reset" winding with the "bias" drivers connected directly to the flip-flops as shown in Fig. 1, or it could be operated with two "set" windings and combined "bias" and "reset" windings, with gate tubes controlling the "bias" drivers as shown in Fig. 4. The switch was driven with similar driving functions for both modes of operation, and every effort was made to keep the conditions similar for both modes of operation.

The first test made was a comparison of the selected and non-selected outputs of the switch core under the two different modes of switch-core operation. There was very little difference in the output pulse shapes from the selected switch core when the operation mode was changed. The slight differences could be attributed to the fact that the driver was working into different impedances depending on whether the driving winding passed through all the switch cores or one-half the cores. The outputs from the non-selected cores showed very little difference for the two modes. In both cases the largest non-selected output was about 9% of the selected output. As a whole, the non-selected outputs of the system shown in Fig. 1 were slightly smaller than those of the other system, but the difference was very small and could very well be attributed to measurement errors.

Various patterns were placed in the memory planes and the spreads of the outputs from the memory were compared under the two modes of switch operation. The outputs were observed with all "one"s in the memory, with all "zero"s in the memory, and with the "pairs checkerboard" pattern in the memory. The spreads were approximately the same for the three patterns for both operating modes. The post-write disturb pulse was removed and the output with the "pairs checkerboard" pattern in the memory was observed. Here again, no difference was detected in the output spread from the memory when the driving mode was changed. The effect of load changes on the output of the switch core was very small and did not change when the mode of operation changed. The test data was documented by R. S. DiNolfo in notebook #2.

Conclusions

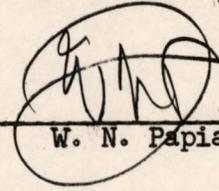
To minimize the number of tubes required to operate the switch, there should be one "set" winding, one "reset" winding, and a full set of "bias" windings. The "bias" drivers should probably be gated in spite of the fact that the gated system used 12 gate tubes that are not needed in the direct-connected systems; this allows the driver duty cycle to be reduced by a factor of about one half, a considerable reduction when the driver tube must supply 400 ma.

In the actual operation of the two systems that were tested, we were not able to detect any significant difference in the characteristics of the two systems. The outputs of the switch and the operation of the memory were similar for both modes of operation. As a result, it seems that the winding and tube count should be used to determine the operating mode.

Signed


J. L. Mitchell
R. S. DiNolfo

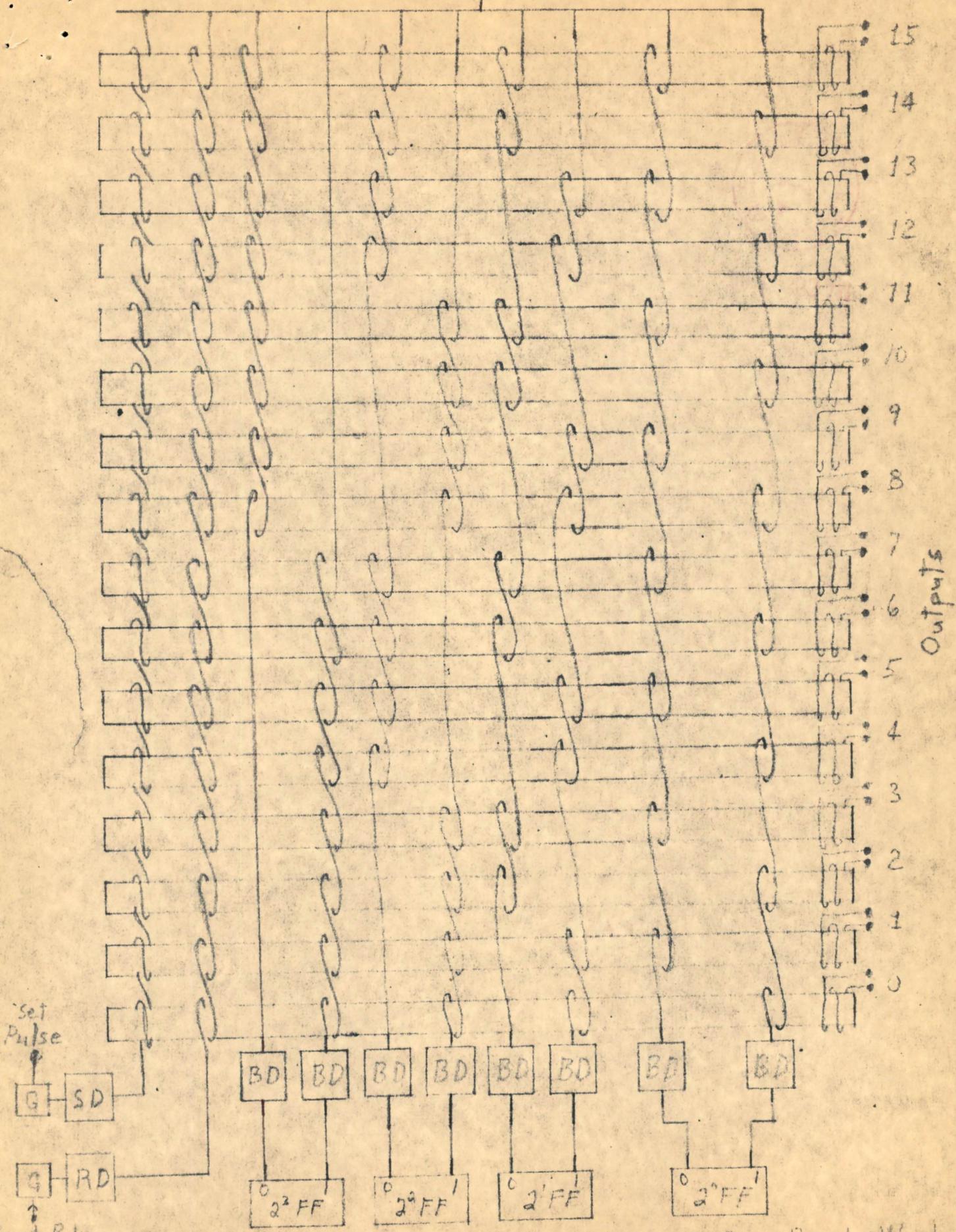
Approved


W. N. Papian

JLM/RSD:jrt

cc: Magnetic Memory Section
D. R. Brown
J. McCusker
N. Edwards (IBM)
D. Shansky

Drawings attached: SA 55290
SA 55291
SA 55292
SA 55293
SA 55294



Outputs

Set Pulse

G SD

G RD

Reset Pulse

Magnetic Matrix

Switch Driver

with One Set Bias Driver

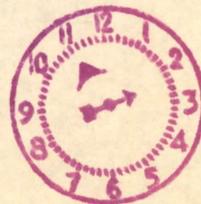
and One Reset Winding; Connections

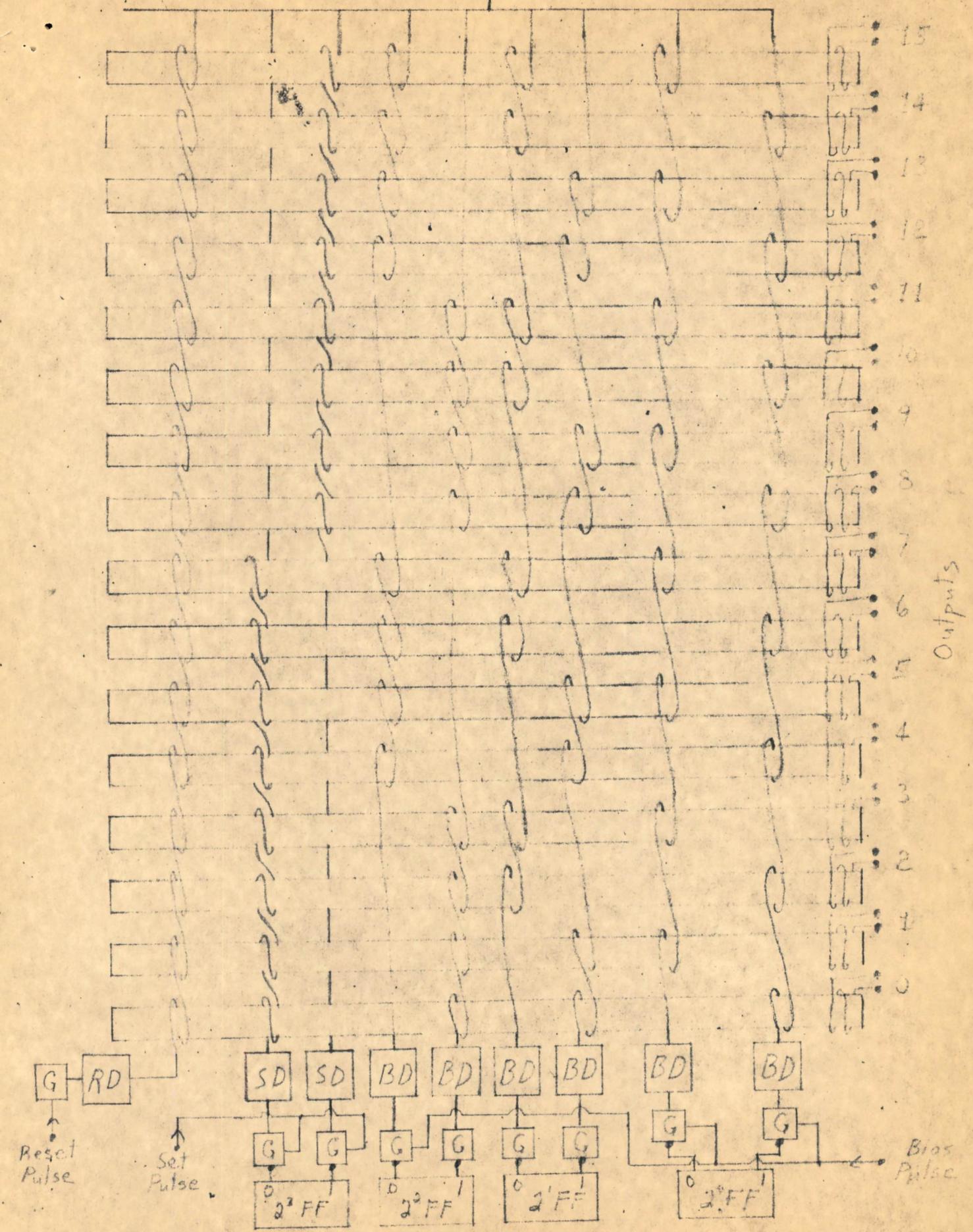
figure 1

gsmith 5-21-53

SA-55290

JUL 1 '53 AM

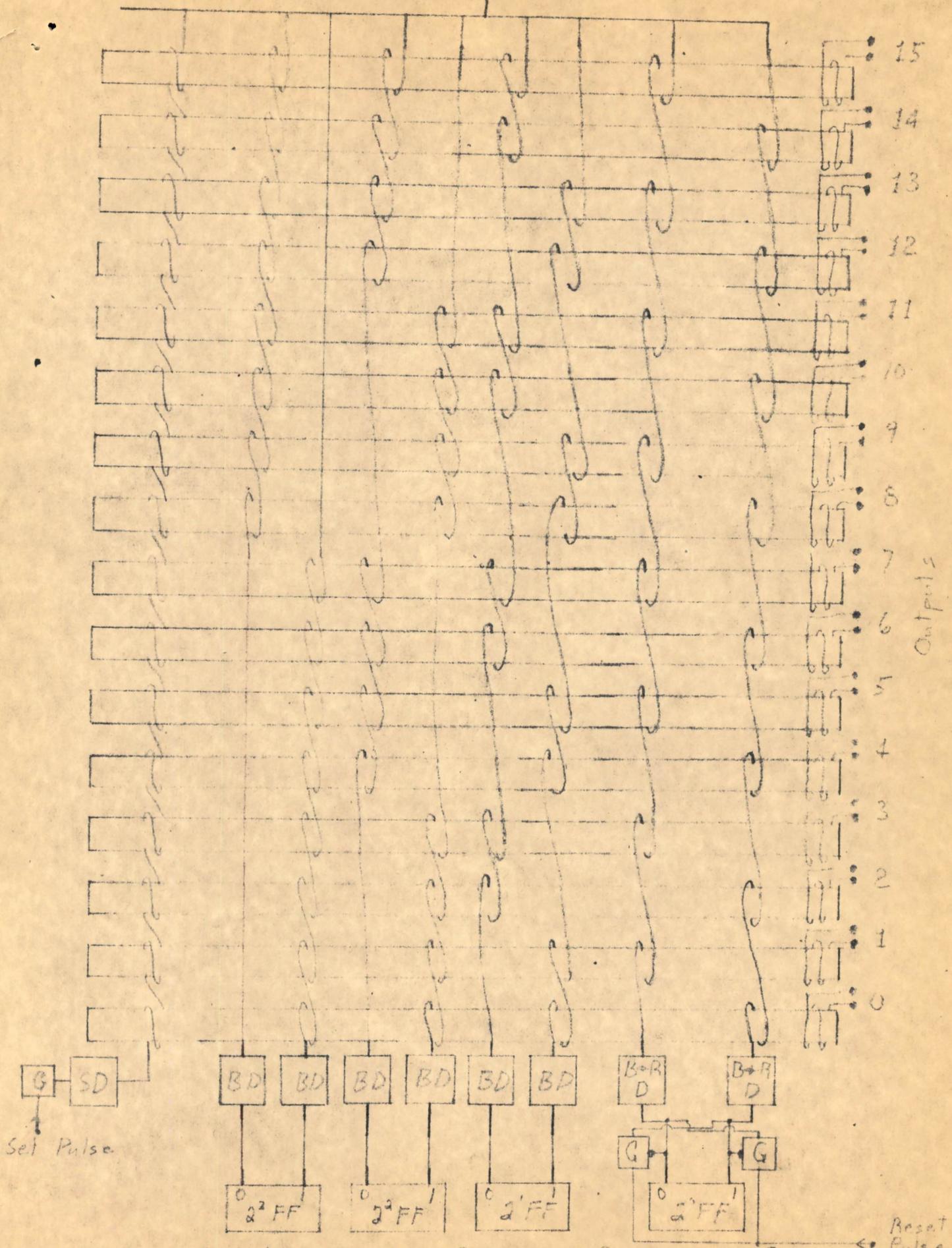




Outputs

16825-45

Magnetic Matrix Switch with Two Set and One Reset Winding;
 Gated Bias Driver Connections
 Figure # 2
 J. L. Mitchell
 5-21-53



SA-55392

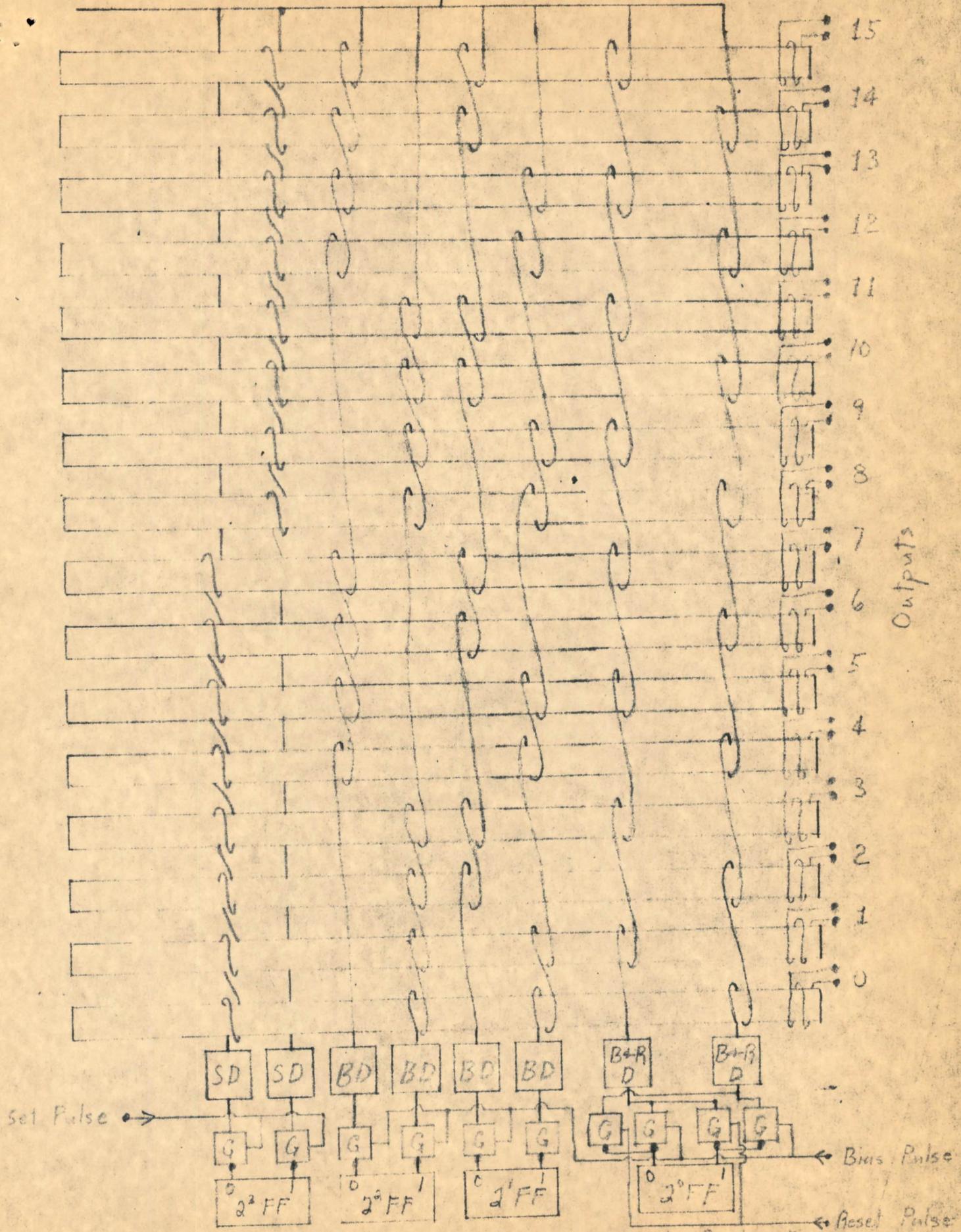
Magnetic Matrix Switch with One Set and Combination Bias and Reset Windings; Direct Bias Driver Connections figure #3

Reset Pulse
J. Mitchell
5-21-53

JUL 1 '53 AM



SA-55293



SA-55293

Magnetic Matrix Switch with Two Set Windings and Combination Bias and Reset Windings; Gated Bias Driver Connections
 Figure #4
 J. L. Muth 5-21-51

SA-55294

Winding and Tube Countfor a 64 position magnetic matrix switch
figure #5

Type of Bias Driver Connection to Address Flip-flops	Number of Windings on Each Core				Total Number of Windings on Entire Switch	Tube Count			
	Bias Winding	Set Windings	Reset Windings	Combination Bias and Reset Windings		Bias Driver Tubes	Set & Reset Driver Tubes	Gate Tubes	Total Tubes
direct	6	1	1	-	14	24	14	2	40
direct	5	1	1	-	13	20	21	3	44
direct	5	1		1	13	20	21	3	44
direct	4	1		1	12	16	28	4	48
gated	6	1	1		14	24	14	14	52
gated	5	1	1		13	20	21	13	54
gated	5	1		1	13	20	21	15	56
gated	4	1		1	12	16	28	17	58

J. J. Mitchell
5-21-53
SA-55294

Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: SENSING THE SLOPE OF MAGNETIC MEMORY OUTPUT

To: William N. Papiian

From: Kenneth H. Olsen

Date: June 19, 1953

Abstract: In the MTC memory, the amplitude of the output voltage is sensed to tell if it is a "one" or a "zero". If the slope of the output is sensed, the "one" to "zero" ratio may be greater.

In M. T. C. the amplitude of the output voltage of the coincident-current magnetic memory is sampled at a fixed time. Pulses above a fixed level are considered "ones" and those below are considered "zeros". Sensing may be more straight forward if, instead of the amplitudes, the slopes of the output pulses are sampled because at a fixed time the slope of a "zero" is negative while that of a "one" is positive.

A voltage proportional to the slope can be obtained by differentiating the output of the memory but this attenuates the amplitude of the signal significantly and accentuates the noise. If this signal is only "partly differentiated", the difference in slope may still be discernible without a great loss in amplitude. If a capacitor is put across the "differentiator", it will filter out some of the noise and may help the circuit recover quickly.

Figure 1 shows the output signals from a memory core in an experimental set-up. The "zeros" are made unusually large to exaggerate the effect of noise. When the signal is put through the network of Figure 3, the output is as shown in Figure 2.

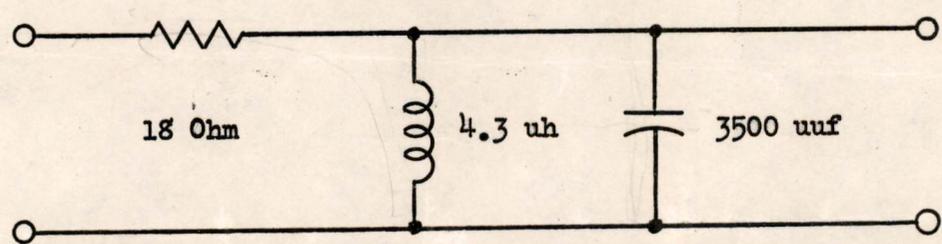
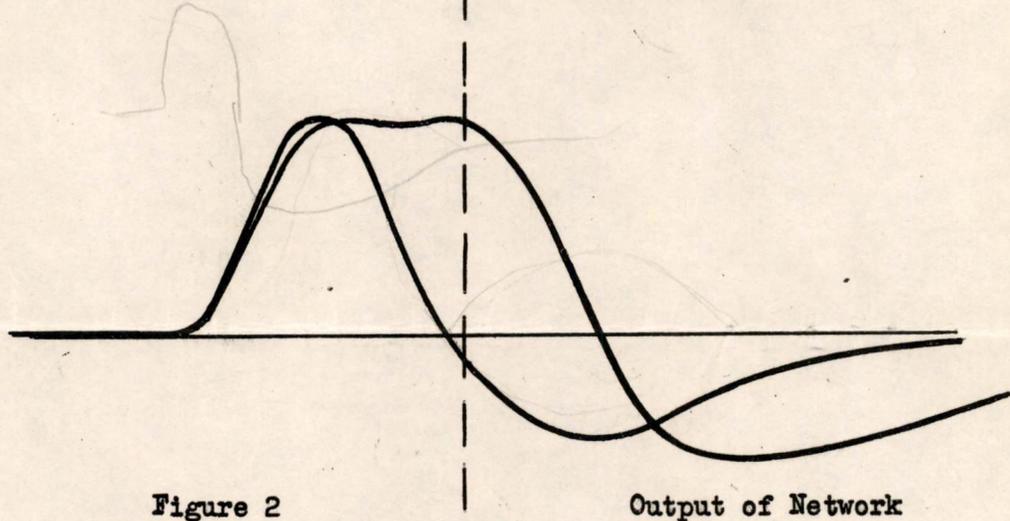
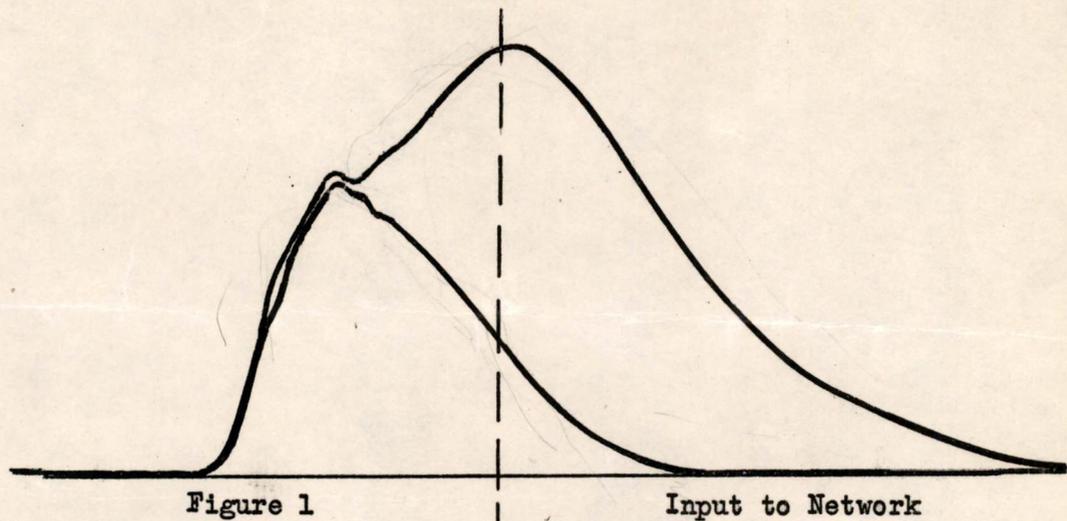
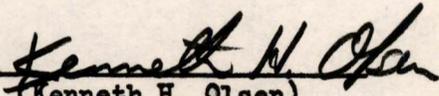


Figure 3 Network

Sensing Amplifier "Differentiator"

It can be seen that even with this large "zero" there is a time when the "one" is positive and the "zero" is negative. With smaller "zeros" there is a much greater time when this difference is evident.

Signed


(Kenneth H. Olsen)

KHO:hpm

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: MTC PARITY CHECKING SYSTEM

To: MTC Engineers

From: Philip R. Bagley

Date: June 25, 1953

Abstract: Each 16-digit word stored in magnetic memory has associated with it an extra digit, termed a parity digit. This parity digit, generated at the time the word is stored, is 0 if the stored word has an odd number of 1's, or 1 if it has an even number of 1's. When the word is read out of memory, there must be parity--that is, equality--between the previous "1" count as stored in the parity digit, and a new count made at the time of read-out. Otherwise a parity alarm will occur.

Fundamental Parity Checking Scheme

The parity count, often referred to simply as parity, of a binary word in MTC, is odd or even according to whether the sum of the digits--i.e., the number of 1's--in the word is odd or even. A binary parity digit may be used to indicate the parity count of a binary word. Parity digits of 1 and 0 may be associated with numbers whose parity counts are even and odd, respectively, or vice versa. From the logical standpoint, the choice is entirely arbitrary. Engineering considerations, however, dictate that words of even parity should have a parity digit of 1, and conversely, and that words of odd parity should have a parity digit of 0. This convention was chosen so that if the magnetic memory should fail entirely, or be accidentally turned off, the apparent contents of any register--i.e., all zeros--would have the wrong parity digit. A word of 16 zeros should have a parity digit of 1, but if no 1's can be obtained from the magnetic memory, the parity digit will appear to be a zero also, and the computer alarm circuits will register a parity alarm.

When a 16-digit binary word is stored in magnetic memory, a parity digit chosen according to the established convention is stored with it. When the word is read out of memory, the parity of the word is checked against its associated parity digit. If the check fails, a parity alarm is given, which normally stops the computer. If a single digit of a stored word or its parity digit is in error--i.e., has been changed from a 1 to a 0, or from a 0 to a 1,--the parity alarm will occur. It may be observed that the parity alarm will occur for any odd number of errors, but not for any even number of errors. Because the probability of a single error is usually small, the probability of a double error is usually negligible. If this were not the case, a more elaborate technique for checking would have to be used, such as is available in the identity check instruction, id.

Since Panel Storage has no provision for storing a parity digit with each word, the parity generating and checking circuits are automatically by-passed when dealing with Panel Storage.

Generating the Appropriate Parity Digit

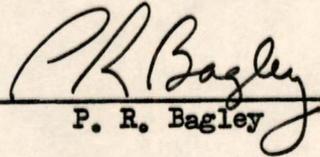
Preparatory to storing a word in the memory for the first time the proper parity digit must be generated. This is done in the memory buffer, or "A", register. The A-Register Flip-Flops (0-15) which hold the 16-digit word are connected to a network of gate tubes which will pass a pulse if the parity count of the 16-digit word in AR 0 through 15 is even. AR16, the parity digit position, is initially clear. If a pulse (called Parity Count) gets through the parity gates, AR16 is set to a 1. At the end of this process, AR16 holds the proper parity digit and the word is ready to be stored in the memory.

Parity Checking

Whenever a word is read out of magnetic memory to the A-Register, a parity check is performed upon it. If there is not parity (equality) between the count of the word read out and the parity digit's record of the count of the word originally stored, a parity alarm pulse is given which will stop the computer unless the pulse has been suppressed by a manual switch.

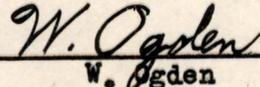
The mechanics of the check are as follows: the word from storage is read into the 17 digits of the A-Register. The 17th digit ("digit 16"), besides going into AR16, is also read in on the complement line of the Parity flip-flop, which initially holds a zero. Hence at this instant, the Parity FF holds the parity digit read from storage. A "parity count" pulse is given after the read. If the parity digit was a "1" and if the parity count pulse passes all the way through the parity gates, it will go to the complement input of the Parity FF, thus clearing it again. (The passed pulse will set AR16 if this is not already set, but AR16 does not enter directly into the checking operation). If the parity digit was "0", and if no pulse is passed by the parity count gates, the Parity FF will likewise finish clear. If, however, the parity digit and the count gates do not agree, only one pulse will arrive to complement the Parity FF. A succeeding "parity check" pulse will pass through the gate on the "1" side of the Parity FF and cause a parity alarm.

Signed:



P. R. Bagley

Approved:



W. Ogden

Approved:



N. H. Taylor

PRB:hpm

cc: W. J. Canty
E. A. Guditz
J. L. Mitchell
W. N. Papian

Drawing attached: SA-37488

H. V. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROJECT GRIND MEETING OF JUNE 25, 1953 (Second Day)

To: AN/FSQ-7 Planning Group

From: A. P. Kromer, R. P. Mayer

Date: June 29, 1953

Abstract: At this meeting marginal checking, power supplies and magnetic memory were discussed. It was generally agreed that more work remains to be done on marginal checking and power supplies before decisions can be made, and that the memory section was more firmly established.

Members

Present:	I. Aronson*	MIT	J.F. Jacobs	MIT
	M.M. Astrahan	IBM	A.P. Kromer	MIT
	P.A. Beeby*	IBM	R.P. Mayer	MIT
	R.L. Best	MIT	J.L. Mitchell**	MIT
	D.R. Brown**	MIT	Moyer*	IBM
	W.J. Canty**	MIT	W. Ogden**	MIT
	J.M. Coombs	IBM	K.H. Olsen	MIT
	R.P. Crago	IBM	W.N. Papian**	MIT
	D.J. Crawford	IBM	R.J. Pfaff	MIT
	N.L. Daggett	MIT	M.J. Raffensperger	IBM
	N.P. Edwards	IBM	E.S. Rich	MIT
	R.R. Everett	MIT	H.D. Ross	IBM
	R.S. Fallows*	MIT	G.F. Sandy*	MIT
	R.G. Farmer*	MIT	N.H. Taylor	MIT
	W. Fitzgerald*	IBM	L. Walters*	IBM
	J.J. Gano*	MIT	W. Whittenberg**	IBM

I. Marginal Checking

Memorandum M-2202 states the existence and function of the marginal checking group. Although further study need be made by this group, it is desirable at the moment to obtain some idea of how to break down marginal checking lines so that electronic design of the logical progress can proceed and so the power supplies can be worked out.

* Present at Marginal Checking and Power Supply discussion only.

** Present at Memory discussion only.

It was agreed that no mechanical marginal checking will be built in.

The capacity of the marginal checking generator must be such that it can carry any circuit to failure although this capacity may not be used in most cases.

It was generally agreed that no more than two hours a day will be available for process of marginal checking itself. The basic philosophy should be that "if a part starts to deteriorate or is different from other circuits, it should be replaced."

Whole circuits must be marginal checked. (This may be done by varying the voltage on adjacent circuits in some cases.)

It is not necessary to locate an error more precisely than to the pluggable unit containing it.

All procedures and variable voltage lines must be manually controllable through simple circuits and any automatic equipment decided on later can make use of the same lines. Someone must study the methods of setting excursion limits for use in automatic (or manual) operation. It must be possible to service and repair all marginal checking equipment without interrupting computer operation.

Marginal checking lines will be arranged and grouped roughly as follows: (an illustrative example will be presented next week).

(1) A single line will connect to all circuits, in a unique logical section, which have the same supply voltage and approximately the same percentage margin. A "unique" logical section is to be defined in such a way that each pluggable unit being checked should be fed by and fed into ones which are not being checked (it is suspected that no more than 170 lines will be needed in the central computer including magnetic memory).

(2) All lines, having the same supply voltage and the same percentage margin, in a physical frame (gross logical division) can be varied together.

(3) All lines having the same supply voltage and same percentage margin, in the whole computer can be varied together (perhaps by varying power supply). It should be mentioned that Norm Daggett thinks this type of control would be excellent.

A marginal checking procedure using the above arrangement of lines was suggested as follows:

- (a) With a check program running, marginal check all group lines (see (3) above) to see if any of this is wrong. Log any trouble and proceed to (b).
- (b) If a failure occurs in one such group, split that group into subgroups (see (2) above) and vary each subgroup. Log the trouble and proceed to (c).

- (c) Depending on the particular frame discovered to be in trouble, insert a diagnostic program and/or split the faulty subgroup into individual lines (see (1) above) and vary each one.
- (d) Replace the faulty pluggable unit or log trouble to be fixed later.

Automatic equipment for any and all of the above procedure should not be provided unless it is sufficiently simple.

Automatic or manual procedures must not cause unreliable nor electronic damage nor serious logical damage (writing between pockets on the drum, etc.).

It was agreed that further investigations should be carried on in connection with diagnostic programs and techniques for automatically logging troubles and margins. Study of the application of marginal checking to power supplies and air conditioning equipment should be made.

II. Memory

The memory section was discussed next. It is fairly well established that magnetic memory will contain 4,096 registers, 33 bits each (including one parity bit) in a 64 x 64 x 33 core array using a 2:1 current ratio selection scheme.

It was definitely decided that everything should have sufficient capacity so that a complete second memory can be added later without redesigning of logic, air conditioning, power supply, room space, etc., although a second memory may not actually be built for sometime.

A memory cycle was proposed which required $7 \frac{3}{4}$ microseconds for a complete read-write time from one strobe to the next. It was agreed that every attempt should be made to obtain a faster memory cycle. It may be possible to make memory cycle faster due to the following details which could be possible eliminated: a post write disturb pulse requires $\frac{1}{4}$ to $\frac{3}{4}$ microsecond longer than the memory address register setup time depending on how the M. Adr. Reg. is read into. It is possible that a post write disturb is not necessary or that it can be made no longer than the M. Adr. Reg. setup time. $\frac{1}{2}$ microsecond is used for staggering the read pulses in order to reduce noise. An additional $\frac{1}{2}$ microsecond is used for staggering write pulses if at somewhere drivers are used in the system which uses stagger read. Stagger read might be omitted if 4 sensing lines per plane are used instead of the 2 which were proposed at the meeting; but this would probably require extra sensing amplifiers adding 528 cathodes to the system unless low level gates could be used. Such techniques will be investigated.

MIT will check to see if cores must be tested specially to make use of the stagger read system.

The sensing amplifier will use a balanced input and amplifier, full wave rectification taking place immediately preceding strobing gate.

It was agreed that people should concentrate on developing transformer driving systems. A crystal translator (matrix switch) will control cathode drivers which drive the driving transformers. IBM will study the 6146 and 7AK7 tubes as transformer drivers and MIT will study the 5998 tube (a direct vacuum tube driver without transformers). It was generally decided that a few spare planes should be wired into the memory array for emergency use. Perhaps the complete memory cube will be pluggable but independent planes will definitely not be pluggable. Perhaps 2 planes will be sewn together as one assembly but probably not more than 2 (although investigation is being made on the possibility of sewing the whole cube). The cube will probably be about 1' x 1' x 2 1/2'. It took 2 man weeks to wire an MTC plane, so careful production schedules must be made immediately.

The memory cube must be air conditioned to + a few degrees Centigrade. This will probably require a separate low velocity recirculating system with thermostatic control of injection of cool air from the main system.

III. Power Supplies

This was the first major discussion of power supplies and few decisions were reached although some major decisions and ordering action are required soon, since power supply equipment is required very early in the installation period. It was decided that there will be a diesel generator unit provided for XDI for practice with such a device. Details will be decided later. The water cooling portion of the air conditioning system will be broken into several sections or units (perhaps 4) for reliability.

Rotating machines will be used between the line and all power supply regulator units in order to isolate the system from transients at the power source and within the AN/FSQ-7 Central. At least 1 spare machine will be provided. The motor and generator sections of each machine must be separate in order to prevent capacitative coupling of large transients. A 208 volt system was suggested (120 volts, 3 phase, 4 wire).

In general, any standby power unit should be able to take over within one minute of power failure.

Filaments will cycle up (when starting) from some voltage (not necessarily Zero) to a final voltage which will be regulated. They will be cycled off except in an emergency when another supply is going to be flipped on.

Estimated requirements for AC power needed for computer and associated equipment is 200-250 KVA with approximately 100-150 KVA for air conditioning, lights, etc.

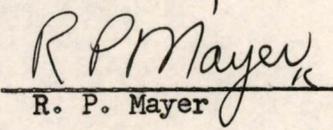
The DC should be regulated to roughly 0.3% for any type of load variation or to within about 2% if all types of variations were cumulative in the worst way. (The following types of variations were mentioned: 95% steady change of load, 80% transient change, 98% change at any frequency, ripple and immediate drift). Estimated voltage requirements are -450, -300, +250, + 150, +90, -30, +15. High voltage for scopes might be by way of low voltage high frequency system. The estimated DC power requirements totals about 56 KVA.

The logic and planning group should help define power supply number of units to use, number of standby units, etc. All this depends on methods of operating during breakdown, methods of marginal checking, etc.

The method of sequence power on and off must be designed to prevent writing undesirable information on the drum or between slots on the drum even when emergency cut-off drops everything considerably (emergency cut-off probably should not drop air conditioning system).

It must be possible to apply power to any large logical block without disturbing power supply to the rest of the system.

Signed


A. P. Kromer
R. P. Mayer

APK/RPM:jrt

Sured

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: EQUATION OF MOTION FOR A CYLINDRICAL 180° DOMAIN WALL

To: Group 63 Staff

From: P. K. Baltzer

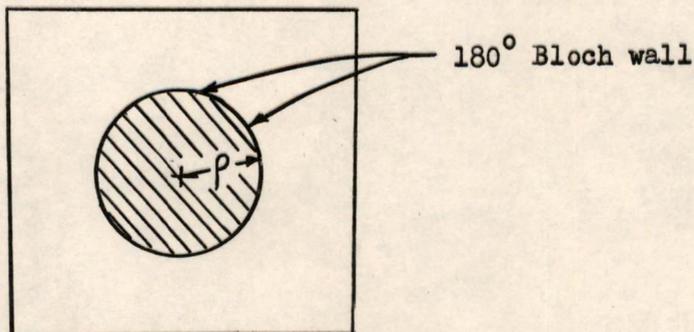
Date: July 30, 1953

Abstract: The equation of motion for a cylindrical domain wall has been derived utilizing the Lagrangian formulation. Additional terms enter the equation of motion for a cylindrical wall that do not appear in that for a planar wall.

The motion of planar 180° domain walls have been investigated by J. K. Galt, where the equation of motion is $m\ddot{z} + \beta\dot{z} + \alpha z = 2I_s H$ for a unit area of 180° Bloch Wall. m = equivalent mass per unit area, β is the damping coefficient, α is the stiffness coefficient and z is the linear displacement of the wall. I_s is the saturation magnetization and H is the applied field.

To derive the equation of motion for a cylindrical wall, the Lagrangian formulation is used. The Lagrangian = $\mathcal{L} = T - V$; where T is the kinetic energy of system and V is the total potential energy. The dissipation function is $G(\dot{\rho})$ where ρ is the radial displacement of wall. The equation of motion is:

$$\frac{d}{dt} \left(\frac{\partial \mathcal{L}}{\partial \dot{\rho}} \right) + \frac{\partial G}{\partial \dot{\rho}} - \frac{\partial \mathcal{L}}{\partial \rho} = 0.$$



Cross Section of a Unit Area of Material

Note: Saturation magnetization of shaded domain is perpendicular to paper and toward reader, and that for the unshaded domain is away from reader.

1. J. K. Galt, J. Andrus, and H. G. Hopper, "Motion of Domain Walls in Ferrite Crystals," Rev. Mod. Phys., vol. 25, p. 93, (Jan. 1953).

Wall motion is considered for a wall of the configuration shown where the domain enclosed by the wall is magnetized in opposition to that outside, and is ℓ units long. The applied field will be parallel to the domains, favoring one of the two directions, thus causing the wall to move radially in such a direction as to enlarge the domain magnetized in the direction of the applied field.

The kinetic energy is

$$T = \frac{(2\pi\rho\ell)m\dot{\rho}^2}{2}$$

The total potential energy is

$$\begin{aligned} V &= E_{\text{mutual}} + E_{\text{wall}} + E_{\text{magnetostatic}} \\ &= (1 - \pi\rho^2)\ell 2HI_s + (2\pi\rho\ell)\sigma_w + \frac{(2\pi\rho\ell)d\rho^2}{2} \end{aligned}$$

and the dissipative function is;

$$G(\dot{\rho}) = \frac{(2\pi\rho\ell)\beta\dot{\rho}^2}{2}$$

where σ_w is the wall energy per unit area, all other constants being the same as those in the equation of motion used for a planar wall.

Hence substituting these values in the equation of motion;

$$\frac{d}{dt} \left(\frac{\partial \mathcal{L}}{\partial \dot{\rho}} \right) + \frac{\partial G}{\partial \dot{\rho}} - \frac{\partial \mathcal{L}}{\partial \rho} = 0$$

one obtains for the motion of a cylindrical 180° Bloch wall (per unit wall area);

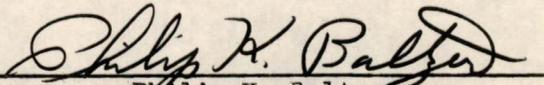
$$m\dot{\rho} + \frac{m\dot{\rho}^2}{2\rho} + \beta\dot{\rho} + \frac{3}{2}d\rho + \frac{\sigma_w}{\rho} = 2HI_s$$

the equation of motion for a planar wall being

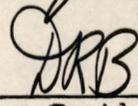
$$m\ddot{z} + \beta\dot{z} + \alpha z = 2HI_s$$

In general since $m \sim 10^{-10}$, the normal inertial term can be neglected. For low fields where $\dot{\phi}$ would not be excessively large, the additional inertial term can also be neglected. However the additional non-linear term, $\frac{Q_w}{\rho}$, is of the same order as the driving force and cannot be neglected in calculations involving the motion of a cylindrical wall. This term enters here since the total wall area, and thus also the total wall energy, varies as the wall moves.

Signed


Philip K. Baltzer

Approved



David R. Brown

PKB/jk

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MTC BOOTSTRAP TYPE PROGRAMS

To: Norman H. Taylor

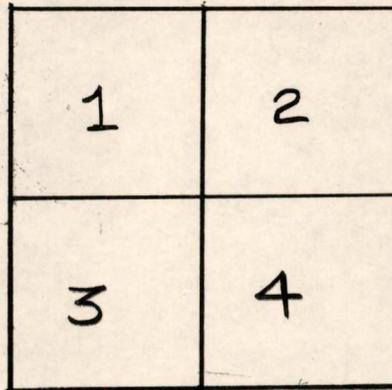
From: H. E. Anderson

Date: July 6, 1953

Abstract: There have been three bootstrap type programs written and tested on MTC. The general characteristics of these are described in this note.

- MP-27 (Inchworm) This program starts from toggle switch storage and moves through magnetic memory in steps of 16 registers. The program spends full time pulling itself through the magnetic memory and when it has reached the end it starts over in toggle switch storage, all automatically. Much of the memory data that has been taken was taken with this program because it has semi random references to magnetic memory and because of its convenience since it can be made to regenerate itself automatically after an alarm has occurred. The only checking involved in the program is the parity checking and the fact that the program would probably destroy itself if an error occurred.
- MP-29 (Bootstrap) This program must be read into the magnetic memory. It then divides the magnetic memory into two parts. When the program is being operated in the first part it is testing the second part of the memory by storing all 1's in each register of the second part and then checking to see that every register reads out all 1's. The checking is done by means of the identity check instruction, which checks all digits. This program has been used for life tests. It operates entirely in magnetic memory and will probably destroy itself if an error occurs. For this reason it is not desirable for marginal checking of the memory.
- MP-36 (Worst Bootstrap) This program is the most recent of this series. It is similar to MP-29 except that it divides the magnetic memory into geometric quarters. When the program is running in the first quarter it is testing the diagonally opposite quarter by placing the checkerboard pattern in the three quarters which do not contain the program.

This procedure is necessary in order to have available a full row and column of the checkerboard pattern. In the diagram below the program would be in section 1. The checkerboard pattern would be stored in sections 2, 3, and 4. The section being tested would be section 4. The testing is done by means of the double complement technique.



After testing of section 4 is completed the program would move itself to section 4 and test section 1, etc. Eventually this program will have checked all four quarters.

Signed

H. E. Anderson
H. E. Anderson

Approved

W. Ogden
W. Ogden

HEA:jrt

H. Olsen

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PULSE DELAY REPEATER, P.B. #7

To: N. H. Taylor

From: Julius Woolf

Date: July 8, 1953

The pulse delay repeater consists of a buffer amplifier which drives a 400-ohm .5 μ sec delay line. The delay line in turn senses a gate tube. (See Figs. 1,2) The gate tube's output is fed back to the input of the buffer amplifier through a mixing circuit.

An initiating pulse, greater than 20 volts, is required to start the pulse delay repeater. It was observed that the output pulse stabilized at 30 volts. If the input pulse is under 30 volts the first few pulses will build up in a progression dependent on the loop gain at each point. (See Fig. 2) When an output pulse of 30 volts is reached, the buffer amplifier operates on the non-linear portion of the $i_p - e_p$ curve and limits the output amplitude.

With an increase in resistor R-8 the diodes, CR-2,3 can be removed which will result in a slightly greater output.

This 2 mcps clock appears to be stable with regard to load and voltage variations. (See Figs. 3,4,5)

The WWI 2 mcps clock, (See drawing E-32333-7) in comparison, uses four tubes. This is an increase of two tubes, and related parts over the delay line pulse repeater. The WWI clock consists of a 6SN7 cathode-coupled oscillator, a 7AD7 inverter, a 6L6 peaker, and a 6L6 buffer output tube.

Signed *Julius Woolf*
Julius Woolf

JW/cs

cc: R.A. Nelson
Group 62 Section
Chiefs
H. Ross,
D. Crawford }
D. Hart }

IBM

Approved *R L Best*
R. L. Best

Approved *NHT*
N. H. Taylor

Attached Drawings: A-48457 A-48458 A-55360

B-55360

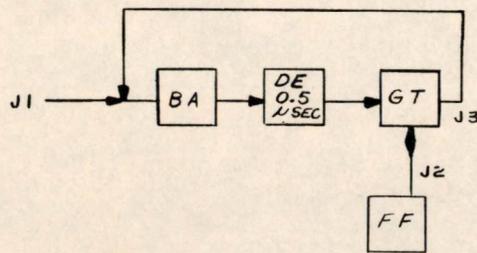


FIG. 1

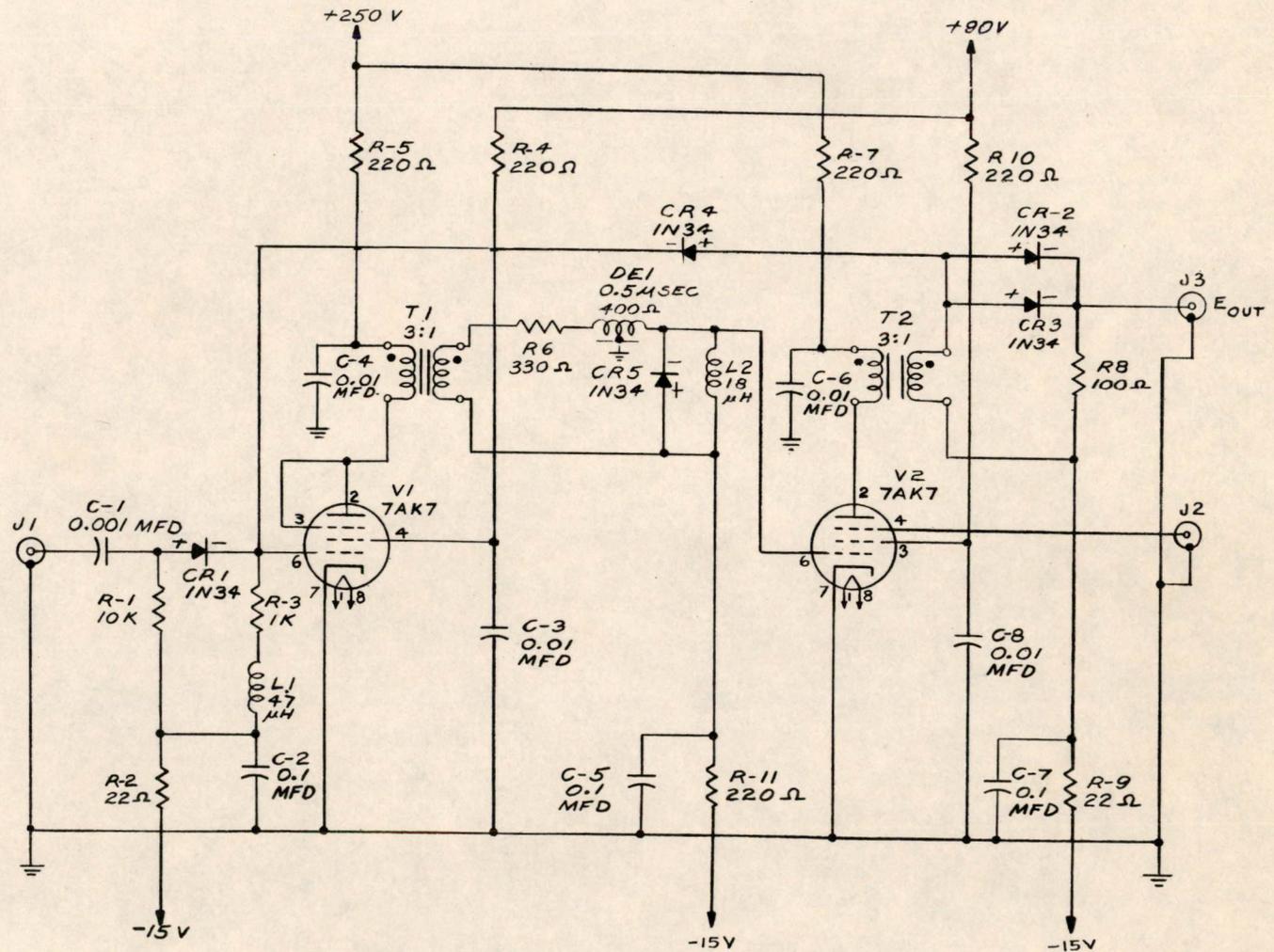


FIG. 2
CIRCUIT SCHEMATIC
PULSE DELAY REPEATER

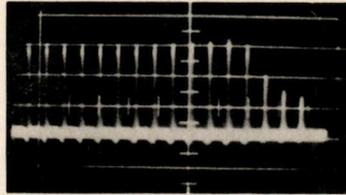
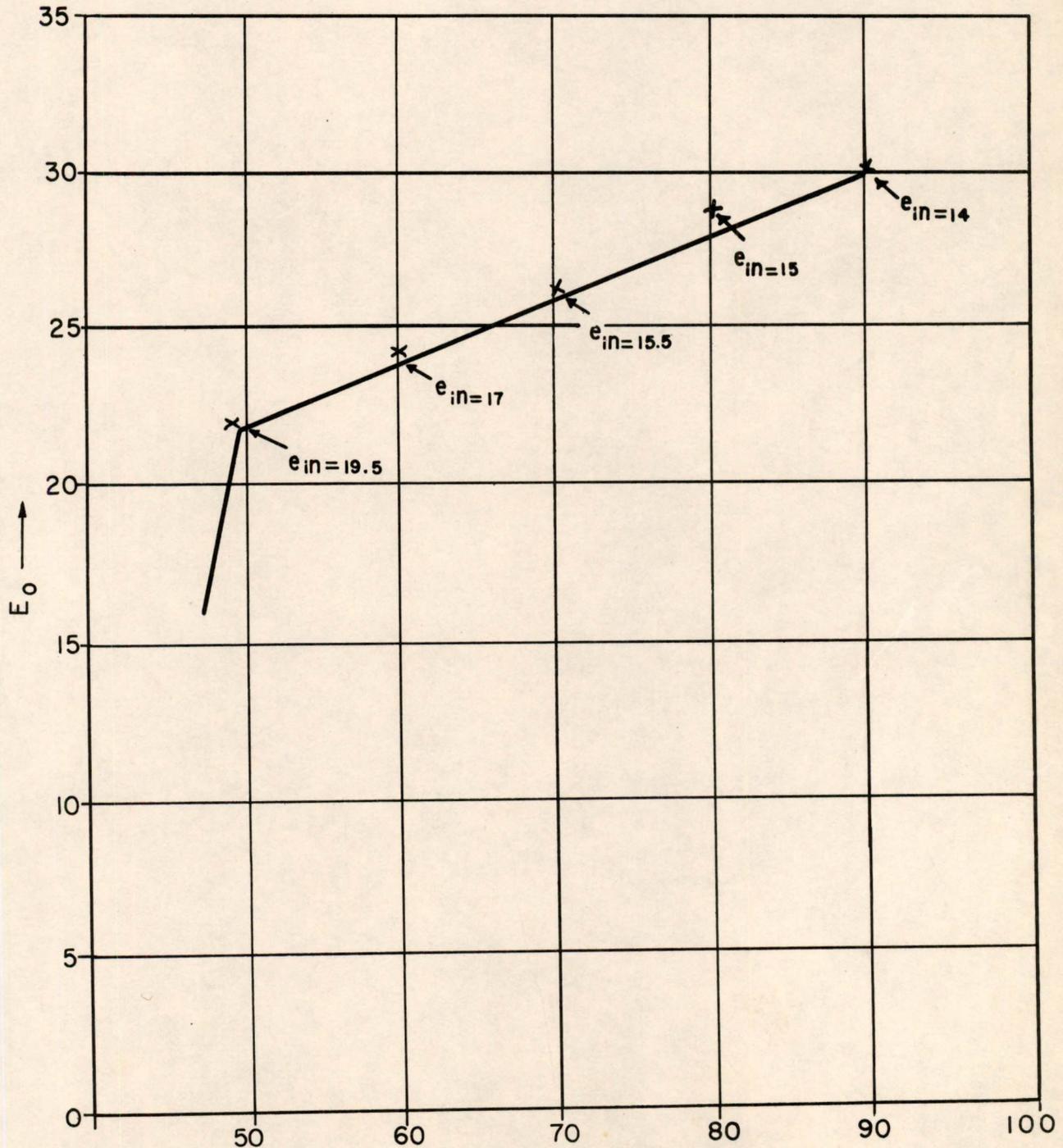


FIG. 3
 $1 \mu \text{ sec./cm}$ SWEEP



$E_c - 2$
 FIG. 4

OUTPUT VS SCREEN VOLTAGE V-2

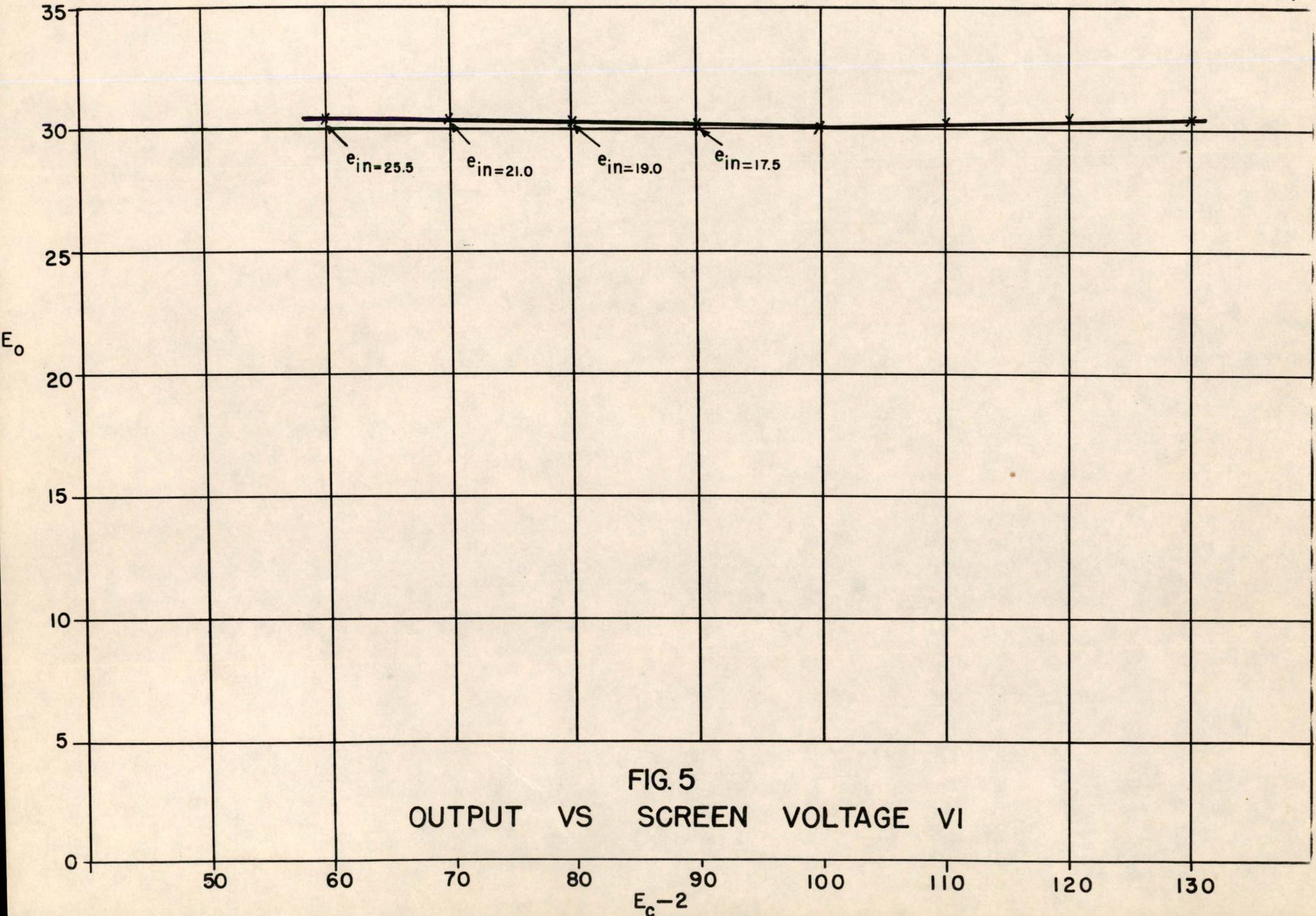


FIG. 5
OUTPUT VS SCREEN VOLTAGE VI

R. Beck

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROPOSAL FOR REDUCING THE NUMBER OF TUBES USED IN DRIVING A
MAGNETIC MATRIX SWITCH

To: N. H. Taylor

From: J. Raffel

Date: July 9, 1953

Abstract: A scheme is outlined which eliminates roughly half the bias drivers used in present models of the magnetic matrix switch. It calls for an increase of about 50% in the number of wires passing through a core in the switch.

The usual scheme for driving a magnetic matrix switch (shown in Fig. 1) having 2^n cores and the same number of output windings, calls for $2n$ separate bias windings, one set winding and one reset winding. An alternate scheme calls for $2(n-1)$ bias windings, 2 set windings and 1 reset winding. In this note we will refer only to the first scheme above. The results can be applied equally well to the alternate scheme. In either case the bias windings occur in pairs; one pair per digit flip-flop. Of the pair, one is activated by the "1" side of the flip-flop and the other by the "0" side. These windings will be referred to as the "1" and "0" windings respectively in this report.

A given flip-flop performs the logical function of selecting one of the two windings associated with it. Each of these windings threads half of the cores. In Fig. 1 for instance the "0" winding of the 2 flip-flop threads cores 4, 5, 6, 7 and the "1" winding cores 0, 1, 2, 3. The pairs of windings associated with the other flip-flops are made to divide the cores into halves also, but each division is made in a different way. For example the 2^1 flip-flop (Fig. 1) is seen to divide the cores in half by alternate groups of two. This arrangement of windings leaves only one core in the matrix unbiased for each setting of the flip-flops, all other cores being subjected to at least one unit and as many as "n" units of bias.

The modification of the above conventional magnetic matrix switch which is proposed is based essentially on the fact that all of the information in a flip-flop is contained in either of its two sides. Our process of selection could, for instance, be made to depend only on the condition of the "1" side of the flip-flop. Suppose we make the "0" winding of a particular flip-flop independent of the condition of the "0" side of the flip-flop, and instead have it automatically pulsed whenever the switch is to be operated.

In order to have this flip-flop produce an effect equivalent to that in the usual switch we must have the "1" winding, when it is selected:

- a) perform its usual function of biasing half the cores,
- b) perform the additional function of cancelling the effects of the automatic "0" bias on the other half of the cores.

This cancellation is readily accomplished by having the "1" winding in addition to biasing its half of the cores in the matrix, send its current in the opposite direction through the other half. Fig. 2 shows a diagram of the proposed scheme.

Let us examine the 2^2 flip-flop and its associated windings. The "0" winding automatically biases cores 4-7. If the "0" side of the flip-flop is on, the "1" winding is not pulsed and we have the desired result. If the "1" side of the flip-flop is on, the "1" winding is pulsed. This means that cores 0-3 are biased and cores 4-7 receive current which tends to cancel the automatic bias of the "0" winding. We therefore have cores 0-3 biased and 4-7 unbiased, which is the desired result. The other digit flip-flops and windings may be seen to operate similarly.

The total number of bias drivers used in this system becomes n "1" bias drivers, one "0" bias driver where the usual magnetic matrix switch has n "1" bias drivers, and n "0" bias drivers. For a large switch this proposed design cuts the number of tubes approximately in half.

The main disadvantage of this system is that it requires the cancellation of currents within a core. Added noise on non-selected cores or possibly unequal outputs for different selected cores may result from differences in currents assumed to be cancelling. It also requires an increase of something less than 50% in the total number of turns on the switch.

An incidental advantage is that the buffers which are normally turned on by the flip-flops and which actually drive the "0" and "1" windings need not be gated drivers in order to be off during the period when the switch is not in use. Since there are no buffers hanging on the "0" side of the flip-flop we can simply set all the flip-flops to the "0" side during the periods when the switch is inoperative.

Signed

J. Raffel
 J. Raffel

Approved

W.N. Papian

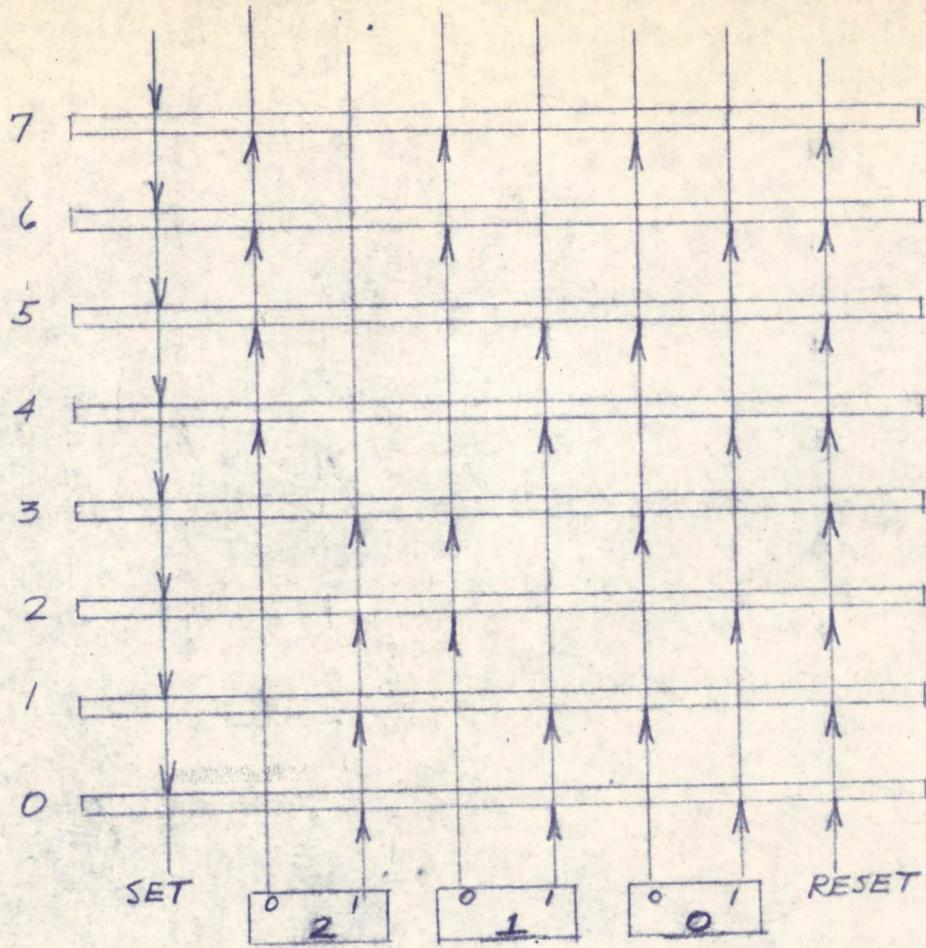
W.N. Papian

JR:jrt

cc: Magnetic Memory Section
 D.R. Brown
 Nate Edwards (IBM)
 K.H. Olsen

Attached drawings: SA 55534
 SA 55535

SA-55534



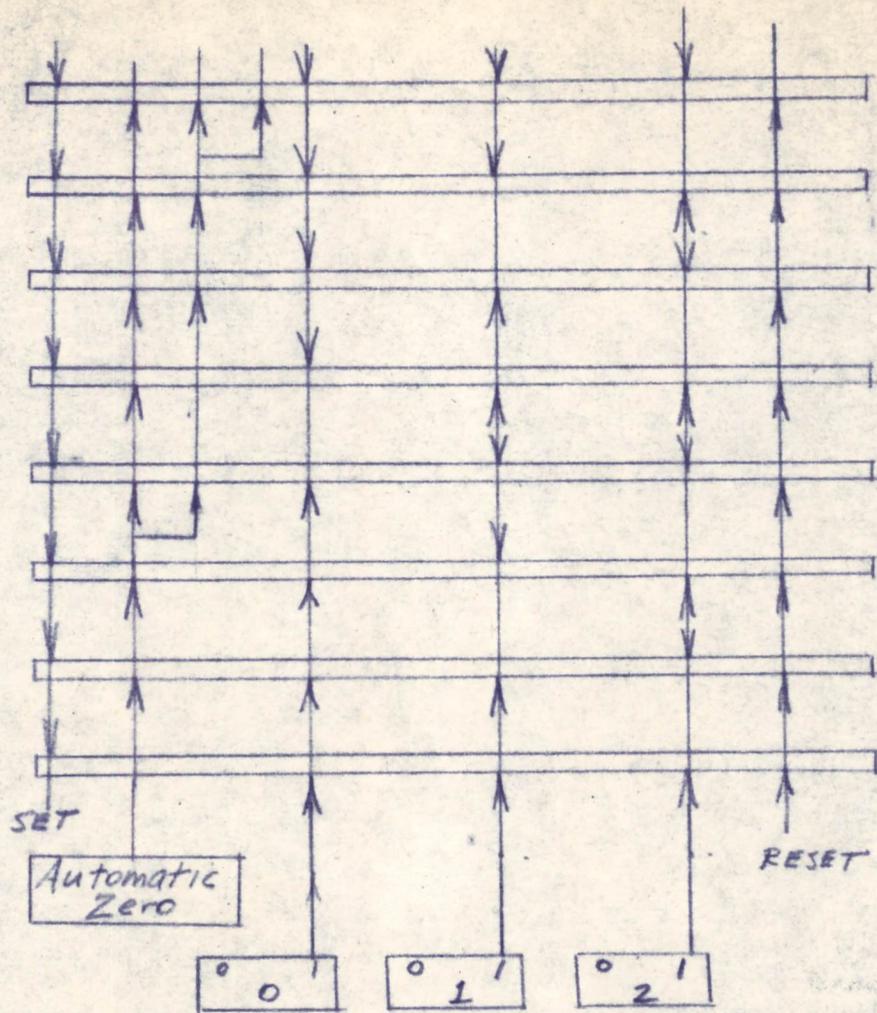
An arrow pointing up indicates current passing through core so as to bias it off.
 An arrow pointing down indicates opposite current direction.

Schematic of Olsen Switch

Fig. 1

SA-55534

SA-55535



Proposed Scheme For Reduction of Tubes In Olsen Switch

Fig. 2

SA-55535

Allen

Digital Computer Laboratory
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SUBJECT: PROPOSED SENSE WINDING FOR A 64 x 64 MEMORY PLANE

To: W. N. Papiian

From: W. J. Canty

Date: July 23, 1953

Investigation of the optimum sense winding geometry of a 64 x 64 memory plane indicates the following:

1. If a single sense winding per plane is to be used the present MTC type geometry should be used.
2. If multiple sense windings are to be used, the best geometry is one in which an equal number of cores in each sense loop is distributed along each of the X and Y coordinate lines.

To enumerate on the second conclusion:

A multiple sense winding geometry has been proposed which consists of dividing the memory plane into four equal parts as shown in Fig. 1.

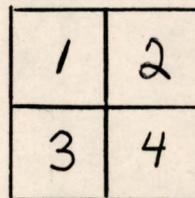


Fig. 1

The MTC type sense winding is to be wound into each section. An analysis of this type of geometry indicates that the expected $\overline{\delta}$ noise in the sense winding containing the addressed core will be 1/2 of that expected from a plane using a single sense winding.

If the memory sense winding was divided into 2 sections per plane as shown in Fig. 2 it is seen that the expected delta noise in the sense winding containing the addressed core will be 1/2 of that from a plane using a single sense winding.

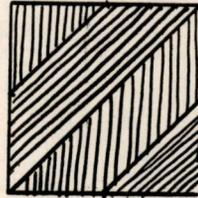
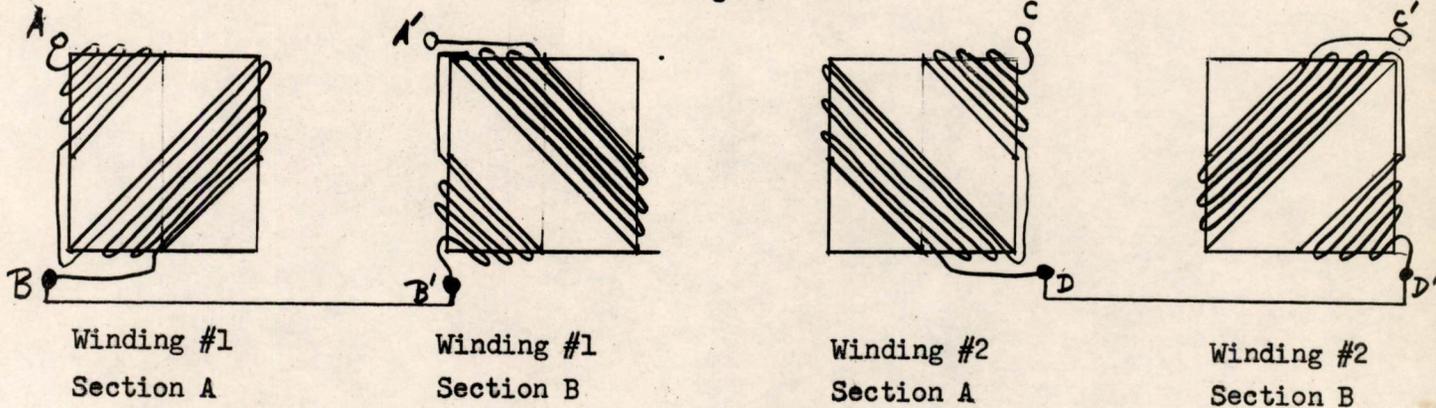


Fig. 2

Thus by using a sense geometry as shown in Fig. 2 only two sense amplifiers per plane would be required whereas four sense amplifiers per plane would be required with the geometry of Fig. 1 and yet the expected delta noise would be the same from both.

The proposed method of winding the sense winding is shown in Fig. 3. This type of winding has the air-flux-pickup cancelling qualities of the MTC Type array.

Fig. 3



Signed: Wm. J. Canty

Approved: William H. Taylor

WJC/rmb
 cc: N. H. Taylor
 Group 62 Section Chiefs
 Magnetic Memory Section
 Group 63 Section Chiefs
 D. R. Brown

H. Olsen

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: RESULTS OF TRANSISTOR LIFE TESTS, JUNE 1952 TO APRIL 1953

To: N. H. Taylor

From: D. J. Eckl

Date: July 28, 1953

Abstract: This note describes the reaction of a limited number of transistors, manufactured over a year ago, to a series of a-c, d-c, and shelf life tests. The tests ran for approximately 5000 hours. The number of transistors which were available for the tests is too small to make meaningful calculations of expected life from the data obtained. The transistors employed were the Bell 1698, GE G11A, and a few RCA TA-165. The Bell transistors in general withstood the tests far better than the other types. This is not surprising since Bell had been producing transistors for a much longer period of time. The GE and RCA transistors used were from initial (or nearly so) experimental production runs.

The tests involved a total of 91 transistors, not counting the immersion tests, and there were 14 failures. In the a-c tests there were 3 failures in 29 transistors during 5000 hours of operation. In the d-c tests there were 5 failures in 32 transistors. The shelf life tests produced 1 failure in 15, and the elevated temperature test 5 failures in 15 at 60° C (140° F). All 15 transistors in the water immersion test failed. These results are good when it is remembered that: 1) many of the tests were intended to be destructive tests, not tests under normal conditions; and 2) many of the transistors used were by necessity of somewhat poor quality.

1.0 Introduction

As soon as transistors became available in quantities, the question of their life in circuits became of interest. Small signal A. F. amplifiers were among the first applications and life tests were started on circuits of this type. Figure 1 illustrates tests used to obtain life data described by Mr. E. Shower on a visit to this laboratory. The small signal A.F. amplifier shown in Figure 1a was the basis

of this test. Normal dissipation was set at 140 mw. End of life was defined as the point where the power gain dropped 3 db. A large number of amplifiers were operated in an accelerated life test at 200, 250, and 350 mw and the average life was calculated from the number of survivors after a given time as shown in Figure 1b. Using this data, the half life for 140 mw dissipation was obtained from the extrapolated curve shown in Figure 1c. The result gave a life expectancy of about 70,000 hours.

A recent article¹ in the IRE based on 20,000 hours of operation, indicates that the half life should be somewhat in excess of 70,000 hours.

In contrast to this highly satisfactory picture there were scattered reports in the spring of 1952 of shelf lives of only a few months. The difficulty was attributed to humidity and presumably moisture penetration of the plastic impregnation.

As a result of this and other problems and in particular in the face of conflicting claims, it was felt that life-test data should be obtained in this laboratory. Modest tests were started in the summer of 1952. At this time, there were two serious obstacles to the operation of satisfactory life tests: 1) Lack of sufficient number of transistors which could be allocated to such tests; 2) Somewhat poor quality of those units which were available. Nonetheless, tests were started and the results of 5000 hours of these initial tests are presented below:

2.0 A-C or Dynamic Life Tests

There were 3 dynamic tests which involved the active operation of the transistor. The blocking oscillator and pulse amplifier tests were expected to take a heavy toll. The counter test was intended to give some idea of life in normal operation.

2.1 Blocking Oscillator Test

This test employed 5 Bell 1698 and 5 GE G11A transistors in the circuit of Figure 2. It was intended to be a destructive test since blocking oscillators of this type had a reputation for producing transistor failures. The test was introduced to show the effects of high emitter and collector peak currents on transistors. The waveforms produced by the blocking oscillator are shown in Figure 3. The test was run for 5500 hours with only 1 failure² which occurred abruptly at 4000 hours. A list of parameters before and after is given below:

¹ Morton, J.A., "Present Status of Transistor Development", Proc. IRE 40, 1314, 1952.

² Since some of the transistors which were of necessity used in the test did not meet our specifications (see M-1800), the definition of failure is somewhat doubtful. It was decided to assume that a failure occurred if a parameter changed by 50%. In most cases when a unit does fail, a change of this magnitude will suddenly occur.

Blocking Oscillator life test data:

Bell 1698 Transistors: 5500 hours 1 failure

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
B-212	2.8	2.9	20	19	0.9	0.8
B-235	2.2	2.6	21	18	1.2	1.0
B-245	3.1	3.2	29	27	1.1	1.3
B-262	2.7	2.9	21	19	1.0	0.9
B-195	3.7	2.0	23	30	0.6	2.2

Failed at 4000 hrs.

GE G11A Transistors: 5500 hours no failures

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
W-15	2.4	2.3	19	15	0.9	1.0
W-24	3.5	3.6	23	20	1.2	0.9
T-55	4.3	3.8	< 15	12	0.7	0.8
V-78	2.7	2.9	33	23	1.5	1.2
U-46	3.5	3.5	41	25	0.7	0.7

The trend in these parameters over the duration of the test is shown in Figures 4 and 5. Some of the other tests show less change. The only significant result is a decrease in average r_{co} of about 2K for the Bell units and 6K for the GE units.

2.2 Pulse Amplifier Test

The pulse amplifier life test used 5 Bell and 5 GE transistors in the circuit of Figure 6. This test was designed to drive the collector heavily into saturation. The driver circuit shown in Figure 7

³ I and F stand for Initial and Final, respectively

operated at a 100 kc/sec repetition rate and produced a pulse 1 μ sec wide and 45 volts in amplitude. This produced an emitter current of 4.5 ma and a collector current of 8 ma. The pulse output at the collector was 15 volts. The test ran for 5300 hours with no failures. The parameter values before and after the test are tabulated below:

Pulse Amplifier life test data:

Bell 1698 Transistors: 4800 hours.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
B-110	3.0	3.2	20	16	0.9	0.8
B-127	2.7	2.8	23	17	1.1	1.0
B-123	1.9	2.3	44	36	1.7	1.4
B-122	2.6	2.5	23	17	1.1	1.4
B-92	3.0	3.1	21	17	0.9	1.0

GE GL1A Transistors: 4800 hours.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
Y-78	2.0	2.1	23	16	1.3	1.2
U-23	3.0	2.6	33	25	1.3	1.4
W-66	2.0	1.8	17	9	3.0	1.8
Z-29	2.5	2.4	18	16	1.0	1.0
V-82	3.0	3.0	31	15	1.0	0.9

The only significant change was a decrease in average r_{co} of 6K for the Bell 1698 transistors and 8K for the GE GL1A transistors.

2.3 Three-Stage Counter Life Test

The three-stage Jacobs counter⁴ shown in Figure 8 was operated for 5200 hours to test transistor life in counter circuits.

⁴ Jacobs, J.F., "A High-Speed Counter Employing Transistors", Digital Computer Laboratory Report, R-214.

There were 3 flip-flop circuits using a total of 6 transistors. No failures occurred in these circuits. In addition, one amplifier and two gate stages were used. The amplifier failed at 2600 hours and one of the gates failed at 1400 hours. Replacements for each lasted until the end of the test. The counter was driven at 200 kc/sec by the vacuum tube blocking oscillator shown in Figure 9. A tabulation of the parameter data for this test follows:

3 FF stages:

Bell 1698 Transistors: 5200 hours; no failures.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
B-239	2.5	2.5	23	20	1.0	1.0
B-224	3.0	3.0	20	19	1.0	0.9
B-201	2.9	3.0	19	17	0.9	0.9
B-288	3.3	3.4	20	16	0.8	0.8
B-207	3.0	3.0	14	13	1.0	1.0
B-232	3.1	3.1	17	14	1.0	1.2

1 Amplifier stage: 5200 hours.

Bell 1698 Transistor; Transistor Products 2C.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
B-291	2.6	2.3	31	16	1.8	3.0	Failed to operate at 2600 hours.
C-332	4.0	4.0	40	28	0.8	0.8	Replacement; operated 2600 hours.

2 Gate stages: 5200 hours.

Bell 1698 Transistors:

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
B-248	3.5	3.6	23	19	0.8	0.8	
B-191	3.5	2.3	17	25	0.6	6.2	Failed at 1400 hrs.
B-146	4.6	4.2	19	19	1.0	1.1	Replacement; operated 3800 hours.

Both transistors which were used in the pulse amplifier showed a large decrease in r_{co} . This circuit was originally intended to stretch a 0.1 μ sec pulse and the 0.2 μ sec pulse provided by the driver may have been too wide. The flip-flop circuits showed a change in r_{co} of about 2K with other parameters unchanged. If this rate is assumed to be constant, it would take some 25,000 hours for r_{co} to reach 9K, the minimum for the circuit.

3.0 D-C or Static Life Tests

Three static life tests, in which d-c voltages were applied to determine the effect of certain operating points on the life of the transistor, were set up. These included a cut-off test, a saturation test, and a maximum dissipation test.

3.1 The Cut-Off Life Test

This test was operated for 5500 hours with 9 transistors: 5 Bells and 4 GE's. The circuit is shown in Figure 10a. Two RCA TA-165's, which did not become available until after the start of the tests, were operated for 3700 hours. One G11A failed at 550 hours. The approximate ratings for the test were:

collector current	1 ma.
emitter current	10 μ a.
collector dissipation	24 mw.
emitter dissipation	60 μ w.

The initial and final parameter values are given on the next page:

Cut-off life test data:

Bell 1698 Transistors: 5500 hours; no failures.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
B-55	2.9	2.6	26	22	1.0	1.8
B-285	2.7	2.7	22	22	1.0	1.0
B-218	3.2	3.2	24	20	0.8	0.8
B-266	3.1	3.1	19	17	1.1	1.0
B-66	2.6	2.6	24	20	1.4	1.4

GE G11A: 5500 hours; 1 failure.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
W-11	3.0	2.1	24	22	1.7	1.6
V-85	2.4	1.7	15	15	2.3	2.6
V-91	2.7	2.2	16	16	1.3	1.5
T-73	2.5	1.0	24	40	1.1	8.3

failed at 550 hours

RCA TA-165: 3700 hours; no failures.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
5521	2.5	2.4	42	36	1.6	1.5
5528	3.6	3.4	60	50	1.1	1.2

In the case of the Bell units the main change was an average drop of about 3K in r_{co} . The GE units showed a drop in α , the average value going from 2.7 to 2.0. The RCA units had an average decrease in r_{co} of about 8K.

3.2 The Saturation Life Test

This test was operated for 5500 hours with no failures. The circuit is shown in Figure 10b. The approximate ratings on the test were:

collector current	9.2 ma
emitter current	9.2 ma
collector dissipation	15 mw
emitter dissipation	5.5 mw

The parameter data follow:

Saturation life test data:

Bell 1698 Transistors: 5500 hours; no failures.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
B-251	2.4	2.7	19	14	0.9	0.7
B-276	2.4	2.9	22	15	1.5	1.4
B-65	2.3	2.5	23	17	1.4	1.4
B-80	3.3	2.4	21	15	0.9	1.1
B-229	2.4	2.6	16	11	1.2	1.1

GE GL1A transistors: 5500 hours; no failures

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)	
	I	F	I	F	I	F
T-51	2.5	2.4	25	15	1.4	1.3
U-31	1.6	1.6	<15	10	2.4	1.8
W-30	2.2	1.7	<15	11	3.2	3.0
W-59	3.0	2.0	<15	15	1.8	1.8
Z-25	1.9	2.0	29	15	1.9	1.7

The average r_{co} for the 1698 transistors decreased 6K. α increased about 0.3 in all cases except one, where it dropped 0.9. In the case of the GE units the data is less exact, but r_{co} decreased.

3.3 The 120 mw Dissipation Test

This test was set to give approximately 120 mw dissipation in the collector of the transistor, as shown in Figure 10c. There were 11 transistors in the test which lasted 5300 hours. There were 4 definite failures: 1 Bell at 500 hours; 2 GE's at 500 hours; and 1 RCA at 500 hours. All of these had an excessively low r_{co} , which is associated with excessive power dissipation or "overforming". In the case of the other units r_{co} also changed considerably, making these borderline failure cases. In almost every case the major change took place in the first 500 hours and no further change occurred. Apparently the drop in r_{co} brought the transistor out of the excessive dissipation range.

The ratings for the test were:

collector current ~ 5 ma
 emitter current ~ 1.3 ma
 collector dissipation 120 mw

The parameter data follows: All these units remained in the test for the full time. After the "failure" at the time noted, no further significant change took place.

120 mw dissipation life test data:

Bell 1698 Transistors: 5300 hours

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
B-271	2.5	2.9	17	9	1.4	1.0	failed at 500 hours
B-242	2.1	2.5	40	21	2.4	1.8	
B-61	2.6	2.6	26	13	1.0	0.9	
B-177	3.2	3.3	30	15	0.7	0.6	

GE G11A: 5300 hours

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
V-22	2.5	2.5	25	11	1.4	1.4	failed at 500 hours
U-25	1.4	1.5	19	12	3.4	1.2	
T-81	1.4	1.4	24	16	2.0	2.0	
U-84	3.2	2.3	<15	8	1.0	1.0	
T-34	2.5	2.8	25	12	1.1	1.0	failed at 500 hours

RCA TA-165: 5300 hours

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
5549	2.2	2.7	23	19	1.2	1.0	
5663-A	2.2	1.4	38	23	1.8	>10	failed at 500 hours

The collector dissipation of 120 mw used in this test is apparently high, although this is about the maximum quoted for the experimental transistors made at the time of the test. Some transistors now available commercially (RCA 2N32) have a 50 mw maximum rated collector dissipation.

4.0 Shelf Life Tests

Two tests of this type were made, one at normal temperature and the second at 60°C.

4.1 Room Temperature Shelf Life Test

The main purpose of this test was to show the effects of ordinary humidity on stored transistors. The test lasted for 7000 hours from June '52 to April '53 and therefore covered a wide range of temperature and humidity conditions. Figure 11 shows temperature and humidity readings from September '52 on. No data was available previous to this time. The parameter data follow:

Normal temperature shelf life test data:

Bell 1698 Transistors: 7000 hours; 1 failure.

<u>Transistor</u>	α		r_{co} (K ohms)		V_{c34} (volts)		
	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>	
B-202	2.6	2.4	27	24	1.4	1.4	
B-210	2.7	2.7	24	22	1.4	1.1	
B-214	2.7	2.6	21	16	1.4	1.4	
B-223	2.5	1.9	24	18	1.7	7.8	failed within
B-228	2.9	3.0	24	23	1.3	1.0	1000 hours

GE G11A: 7000 hours; no failures.

<u>Transistor</u>	α		r_{co} (K ohms)		V_{c34} (volts)		
	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>	
T-42	1.8	1.6	12	14	2.0	2.8	removed after 3000 hours
U-17	1.8	1.8	17	16	1.2	1.2	
U-53	1.5	1.4	26	20	1.9	2.1	
Y-16	2.0	1.9	50	50	1.9	2.0	
Z-44	2.7	2.4	36	31	1.3	1.3	

RCA TA-165: 5200 hours; no failures.

<u>Transistor</u>	α		r_{co} (K ohms)		V_{c34} (volts)	
	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>	<u>I</u>	<u>F</u>
5331	2.0	2.5	30	40	1.6	1.3
5344	2.3	2.5	17	17	1.5	0.9
5356	2.5	2.9	23	28	1.3	1.0
5405	2.2	2.2	23	25	1.3	1.2
5424	2.2	2.0	25	30	2.3	2.1

The trend here again seems to be a decrease in r_{co} of 2 to 3K in the case of the Bell and GE units. However, the RCA transistors show an average increase of 4K in r_{co} .

4.2 Elevated Temperature Shelf Life Test

The shelf life of transistors at a temperature of 60°C (140°F) was also measured. Failures were considerably higher than in the case of the tests at normal room temperatures. A list of the data follows:

Elevated temperature shelf life data (60°C)

Bell 1698 Transistors: 5600 hours; 1 failure.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
B-203	2.8	2.4	22	21	0.9	1.0	
B-217	2.6	1.0	47	52	1.9	1.0	failed at 200 hours
B-225	3.6	3.0	22	27	0.9	1.1	
B-213	2.5	2.2	23	16	1.7	2.8	
B-282	2.2	1.8	<15	12	1.2	1.2	

GE G11A: 5600 hours; 2 failures.

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
T-69	1.6	1.3	46	39	1.5	8.0	failed at 2900 hours
U-61	2.1	2.0	19	23	1.5	3.4	failed at 3700 hours
U-80	2.3	2.2	18	17	1.3	1.2	

RCA TA-165: 3800 hours; 2 failures

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
5707	2.3	2.2	40	39	2.0	7.2	failed at 3800 hours
5711	2.5	2.7	40	32	1.6	1.5	
5704	2.5	2.9	36	34	0.4	1.5	
5705	2.5	2.3	60	41	0.8	9.4	failed at 3800 hours
5717	2.7	3.4	60	45	2.3	2.1	
5719	2.4	2.0	28	28	1.5	1.8	
5721	2.7	2.9	46	40	2.2	2.0	

The Bell units showed a slight decrease in α and no definite trend in the r_{co} change. The one G11 which did not fail showed little change. The RCA units showed a slight increase in α and an average drop of 6K in r_{co} .

4.3 Water Immersion Life Test

This test was intended to be an extreme humidity test and was expected to be hard on transistors. All units in the test failed, showing that the transistors tested were not moisture proof. At the start of the test the curve tracer was not available, and checks were made by measuring d-c parameter values. Failure was therefore considered to occur when a significant change occurred in the parameters or when drift became too serious to make measurements. However, it seems likely that actual circuit failure would occur before this. The result of moisture is to produce hysteresis in the characteristic curves as shown in Figures 12, 13, and 14, which show all transistors before and after the test. These curves also tend to drift considerably. The parameter data for this test and the time of failure are given on the figures.

5.0 Summary

The table on page 14 gives an overall picture of the test and its results. In general these results were better than expected. The transistors which were available were not the best quality and some had previously undergone the rigors of thermal testing. The tests were intended to be severe yet the majority of the transistors were not seriously affected. The most prevalent change was a decrease in the value of r_{co} .

RCA TA-165: 3800 hours; 2 failures

Transistor	α		r_{co} (K ohms)		V_{c34} (volts)		
	I	F	I	F	I	F	
5707	2.3	2.2	40	39	2.0	7.2	failed at 3800 hours
5711	2.5	2.7	40	32	1.6	1.5	
5704	2.5	2.9	36	34	0.4	1.5	
5705	2.5	2.3	60	41	0.8	9.4	failed at 3800 hours
5717	2.7	3.4	60	45	2.3	2.1	
5719	2.4	2.0	28	28	1.5	1.8	
5721	2.7	2.9	46	40	2.2	2.0	

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5.0 Summary

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Type of Test	Transistor Type	Test Hours	No. Units	No. Fail.	Avg. Time at Failure	Significant Change **	α	r_{co}	V_{c34}
Blocking Osc.	Bell 1698	5500	5	1	4000	- -2K			N O
	GE G11A	5500	5	0	----	- -6K			
Pulse Ampl.	Bell 1698	4800	5	0	----	- -6K			A P P R E C I A B L E
	GE G11A	4800	5	0	----	- -8K			
Counter: FF AMP GT	Bell 1698	5200	6	0	----	- -2K			C I A B L E
	Bell 1698	5200	1	1	2600	- ----			
	Bell 1698	5200	2	1	1400	- ----			
Cutoff	Bell 1698	5500	5	0	----	- -3K			C H A N G E
	GE G11A	5500	4	1	550	- .7 ----			
	RCA TA165	3700	2	0	----	- -8K			
Saturation	Bell 1698	5500	5	0	----	- -6K			C H A N G E
	GE G11A	5500	5	0	----	- ----			
120 mw	Bell 1698	5300	4	1	500	- -16K			C H A N G E
	GE G11A	5300	5	2	500	- -8K			
	RCA TA165	3500	2	1	500	- ----			
Shelf Life	Bell 1698	7000	5	1	1000	- -3K			C H A N G E
	GE G11A	7000	5	0	----	- -2K			
	RCA TA165	5200	5	0	----	- +4K			
El. Temp.	Bell 1698	5600	5	1	200	- ----			C H A N G E
	GE G11A	5600	3	2	3300	- ----			
	RCA TA165	3800	7	2	3800	- -6K			
Immer- sion	Bell 1698	----	5	5	1600*				C H A N G E
	GE G11A	----	5	5	1000*				
	RCA TA165	----	5	5	2200*				

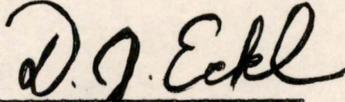
106 29

* These times are probably high since failure was based on d-c point measurements
 ** This does not include units which have failed.

This is normally expected when operating conditions are exceeded, but in some cases where ratings were not exceeded the same result was observed. There was very little change in other parameters.

There were two serious difficulties involved in the tests. The number of satisfactory transistors was not sufficient to make a good statistical analysis of results. The test equipment available during most of the tests did not allow as full a study of the transistors as desirable. In particular, the curve tracer was not in operation at that time.

Signed:


Donald J. Eckl

Approved:

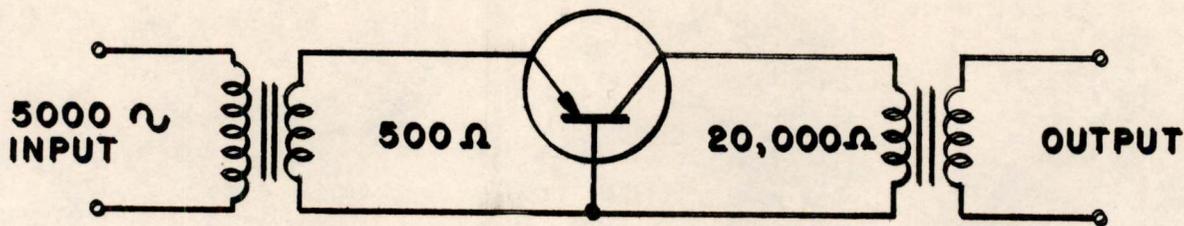

Norman H. Taylor

DJE:tl

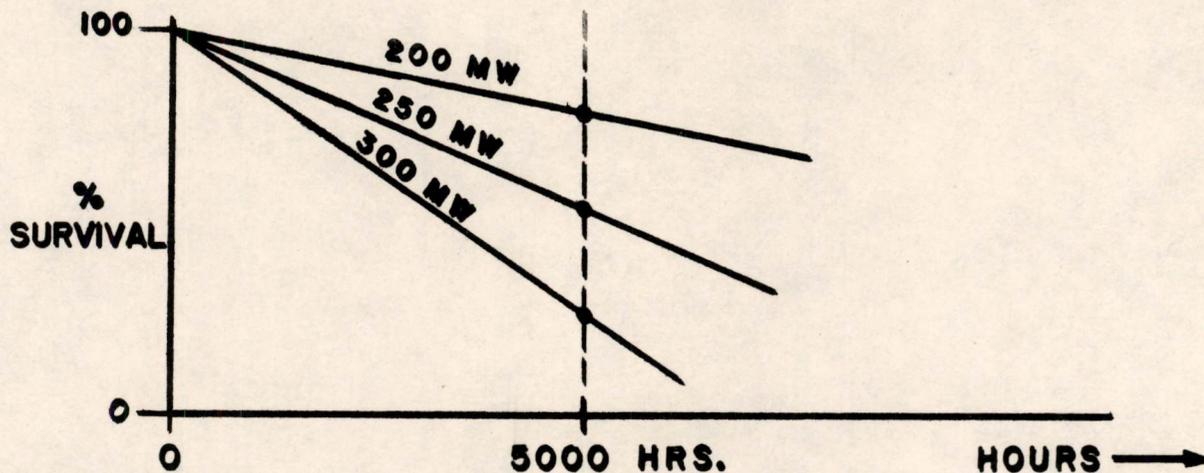
Distribution 2

Drawing Nos:

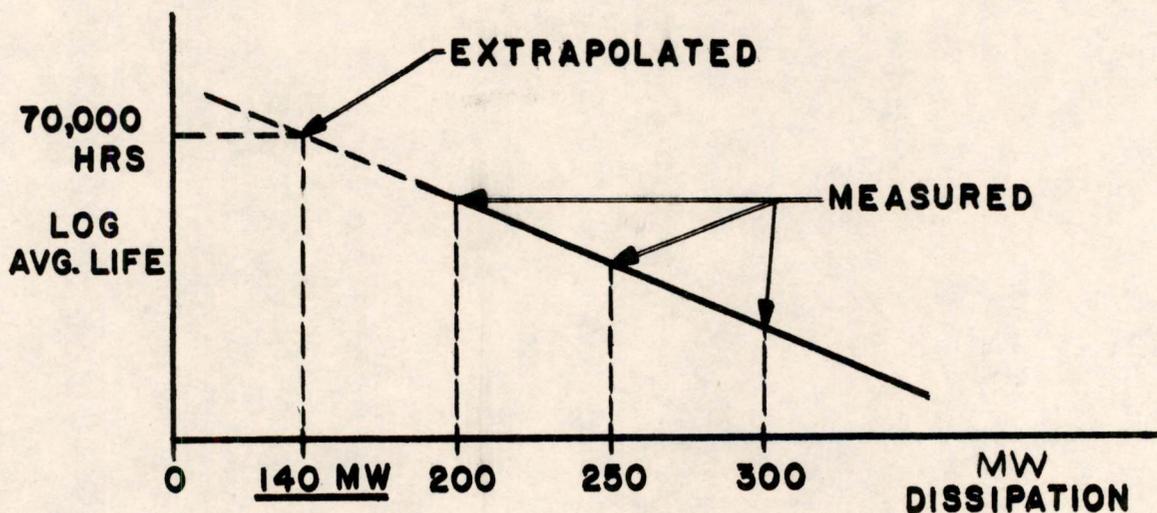
A-55546	C-51509
A-55550	A-55555
A-55547	A-55720
A-55525	A-55721
A-55527	A-55724
A-55548	A-55722
A-55549	A-55723



a) A.F. AMPLIFIER TEST CIRCUIT



b) PERCENTAGE OF ORIGINAL TRANSISTORS SURVIVING AS A FUNCTION OF TIME



c) AVERAGE LIFE AS A FUNCTION OF DISSIPATION

A-55546

FIG. 1
A METHOD FOR ESTIMATING TRANSISTOR LIFE

A - 55550

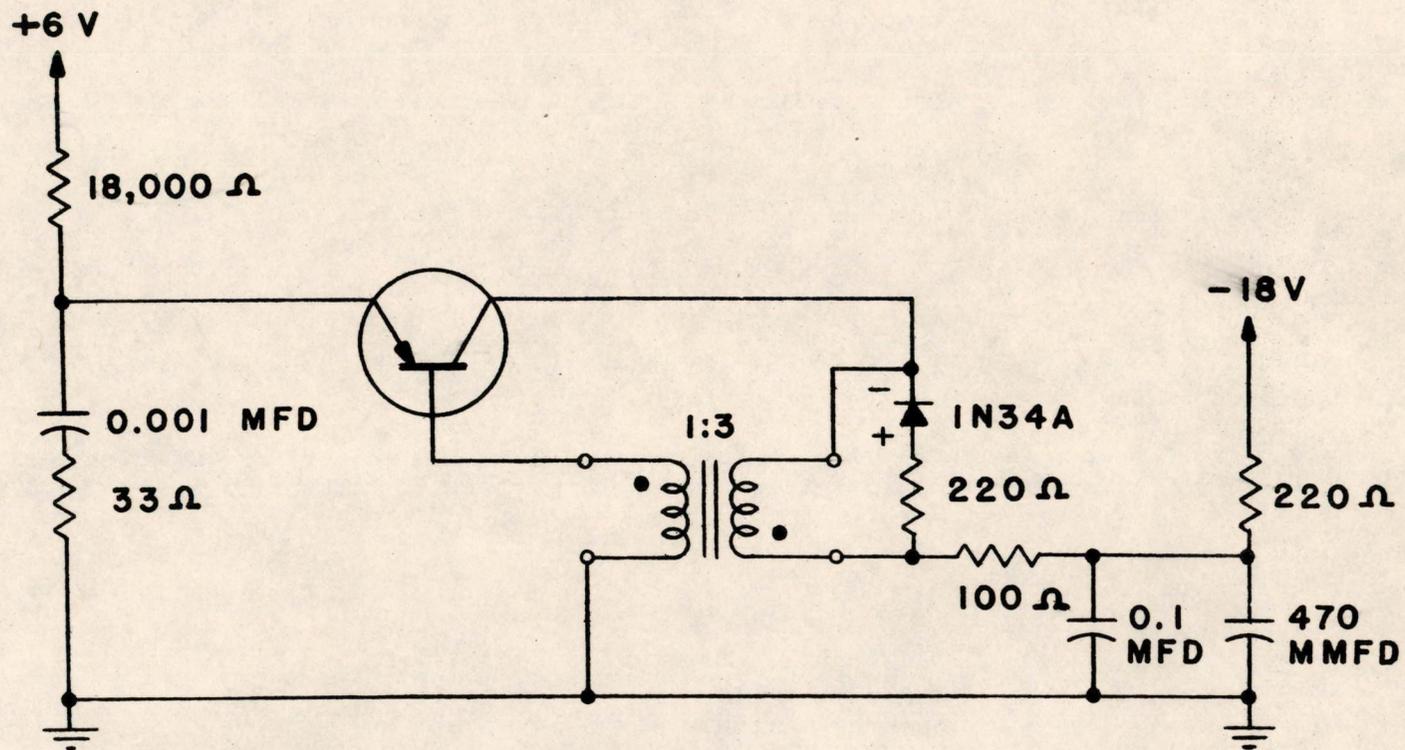
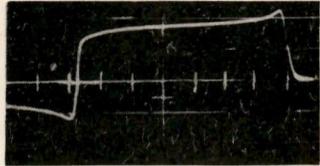


FIG. 2
BLOCKING OSCILLATOR

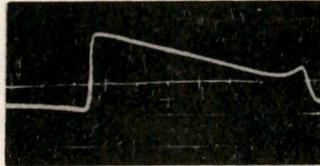
B-195



PULSE WIDTH
1.4 μ sec

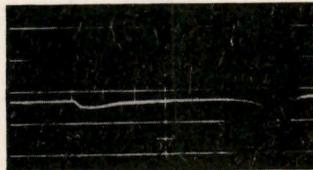
a) COLLECTOR VOLTAGE
PEAK = 12 VOLTS

B-195



b) COLLECTOR CURRENT
PEAK = 13 ma

B-195



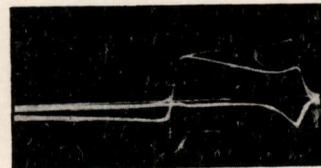
c) EMITTER CURRENT
PEAK = 21 ma

←
TIME

B-262



0 HOURS



5700 HOURS

d) INITIAL AND FINAL TEST PHOTOGRAPHS FOR B-262
 $I_e = 18$ ma PEAK; $I_c = 9$ ma PEAK; WIDTH = 0.8 μ sec

A-55547

FIG. 3
BLOCKING OSCILLATOR WAVEFORMS

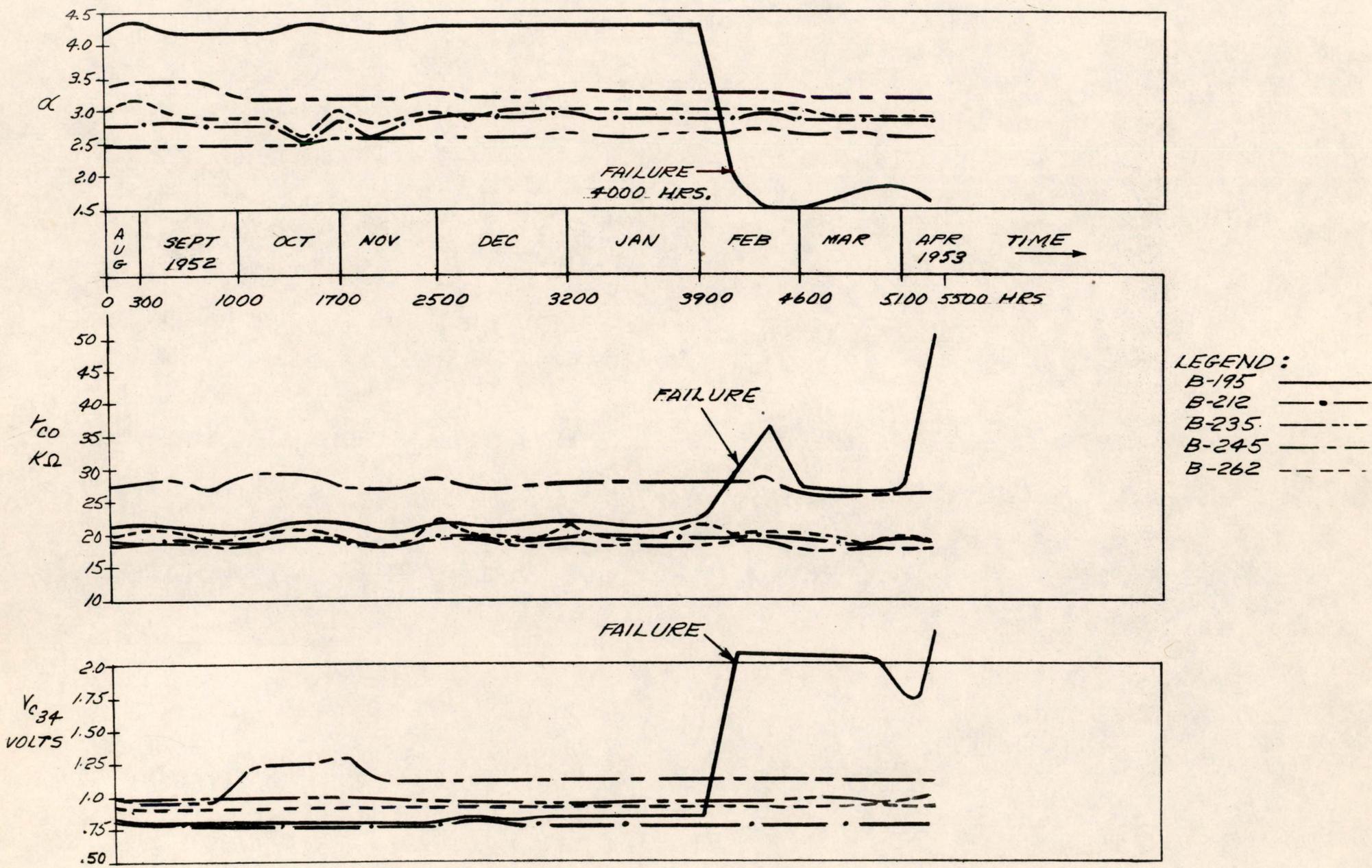


FIG. 4
BLOCKING OSCILLATOR LIFE TESTS - BELL 1698 TRANSISTORS

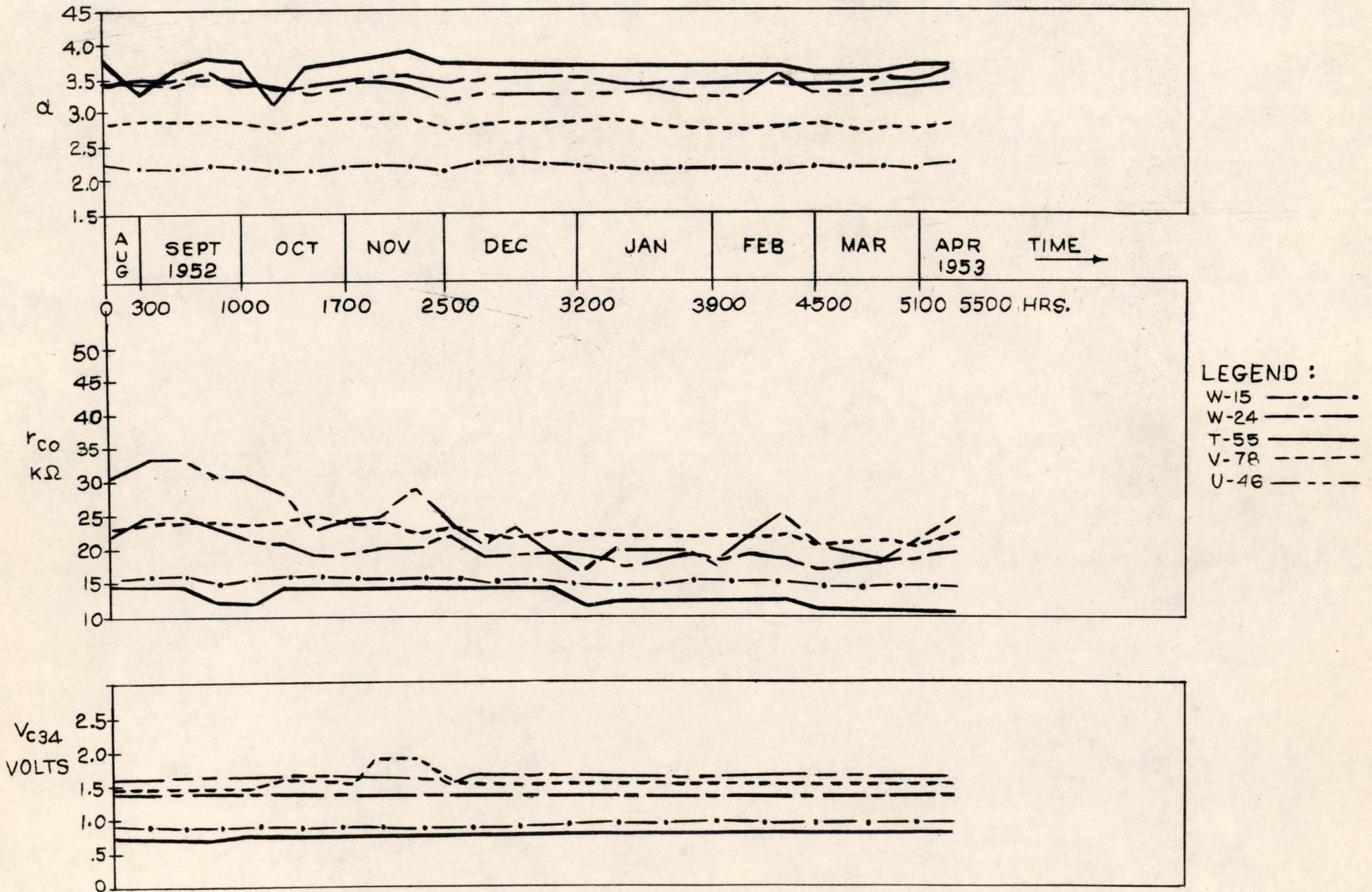


FIG. 5

BLOCKING OSCILLATOR LIFE TESTS-GE G11A TRANSISTORS

A-55548

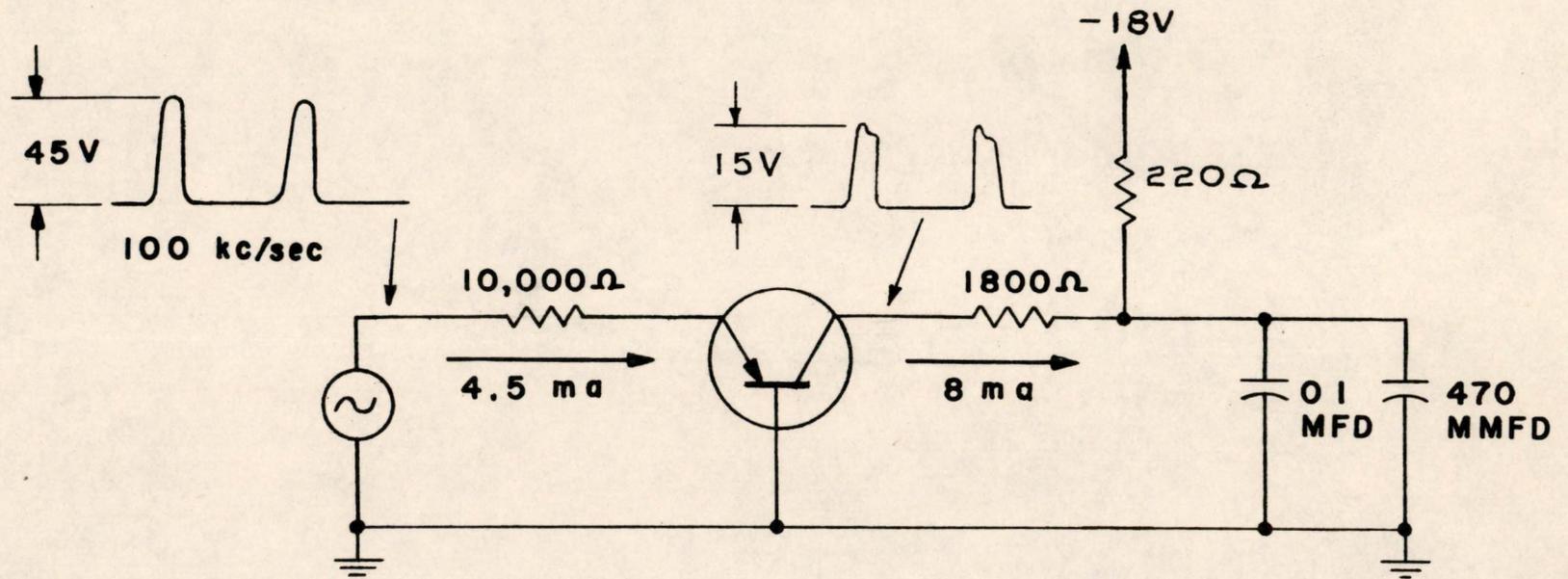
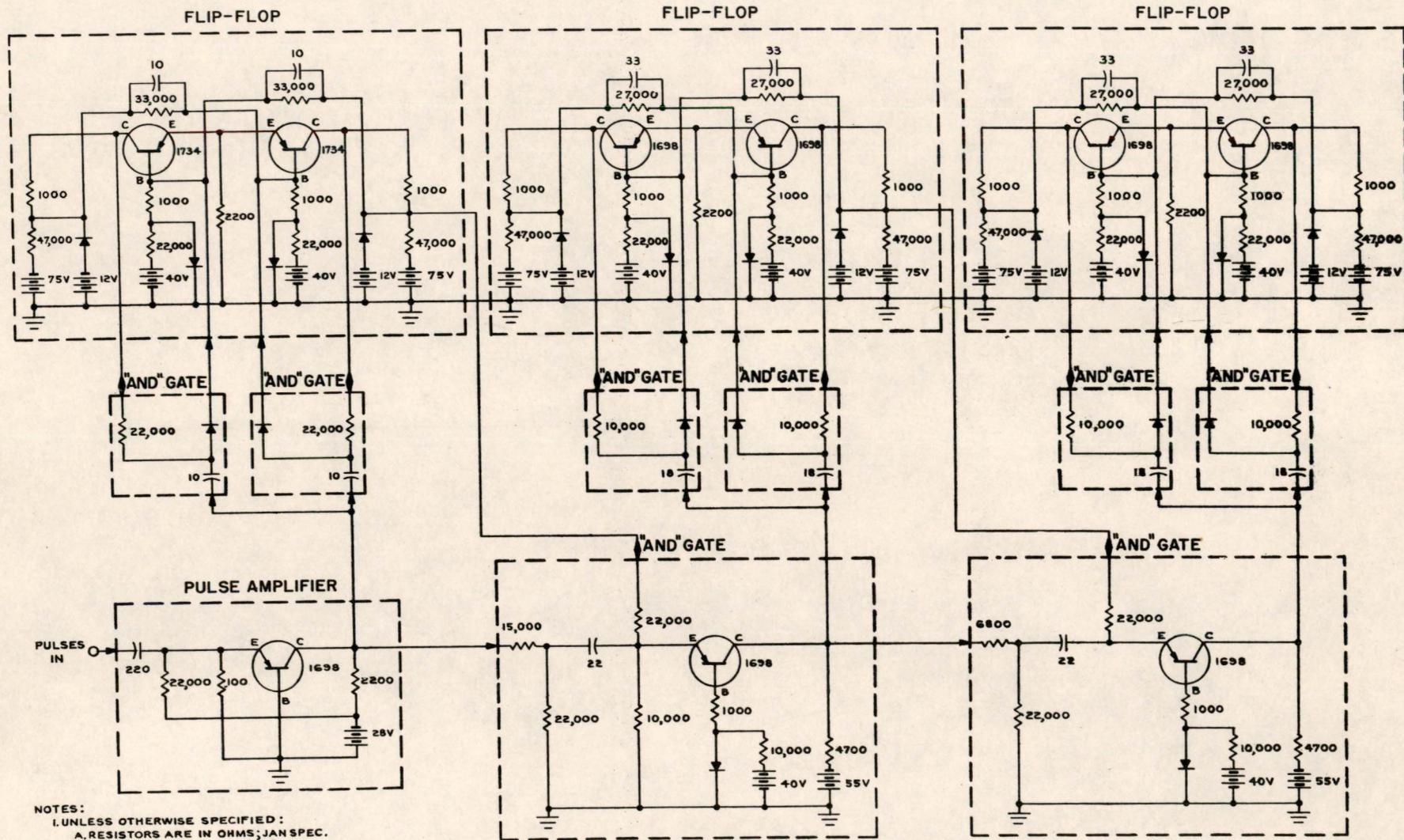


FIG. 6
PULSE AMPLIFIER



NOTES:
 I. UNLESS OTHERWISE SPECIFIED:
 A. RESISTORS ARE IN OHMS; JAN SPEC. COMPOSITION TYPE, 1W, ±10%.
 B. CAPACITORS ARE IN MICROMICROFARADS; JAN SPEC., MICA, ±5%.
 C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN38A.

FIG. 5

CIRCUIT SCHEMATIC, THREE STAGE TRANSISTOR COUNTER

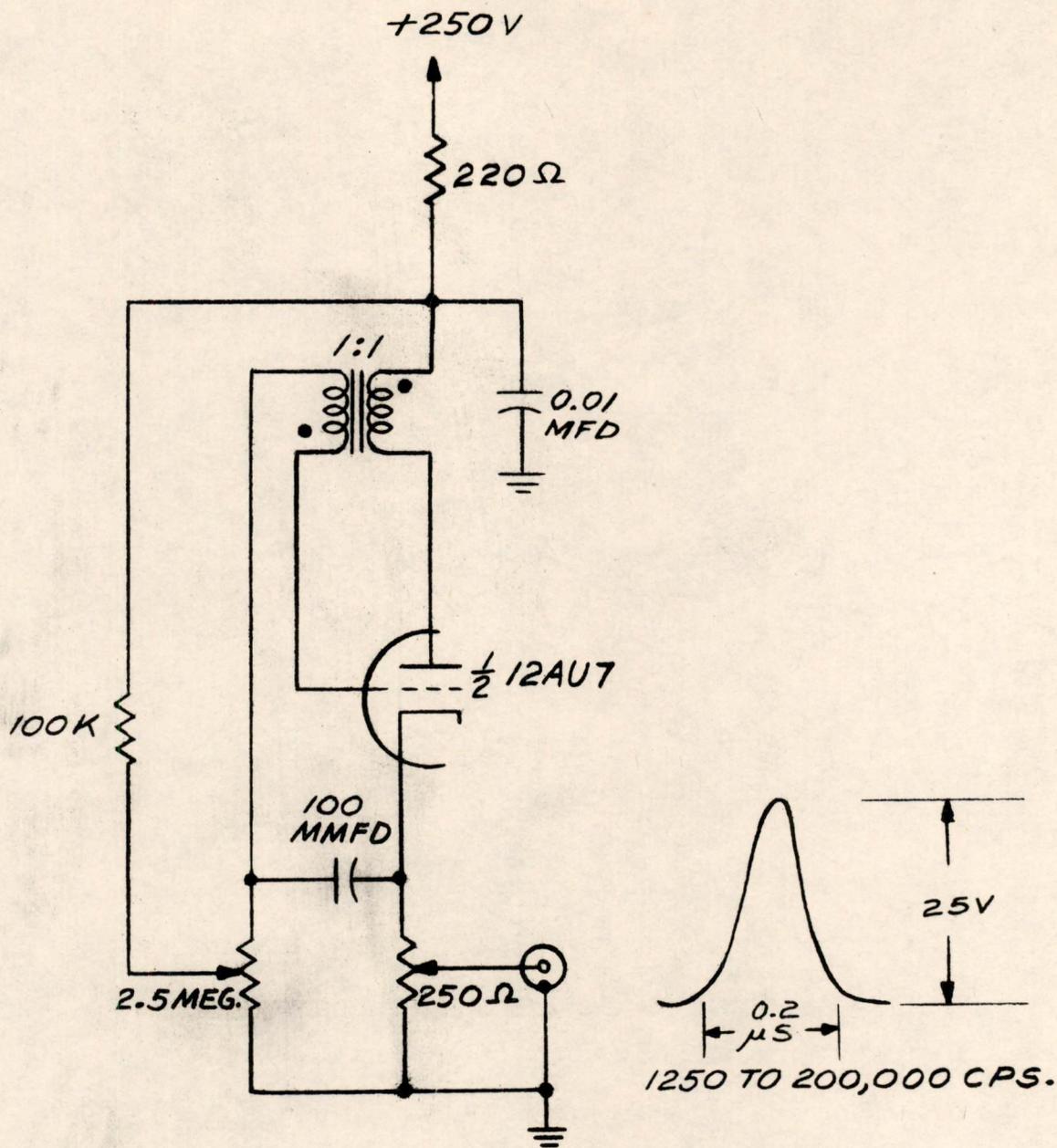
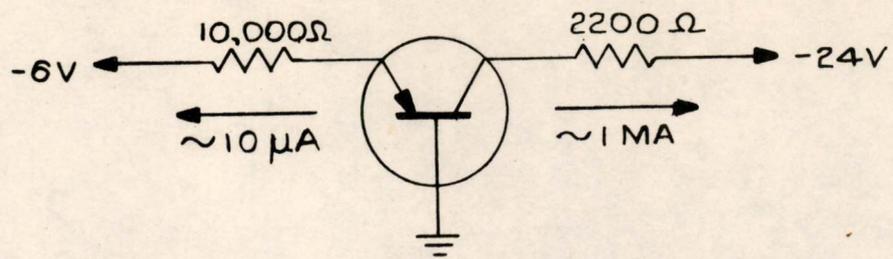
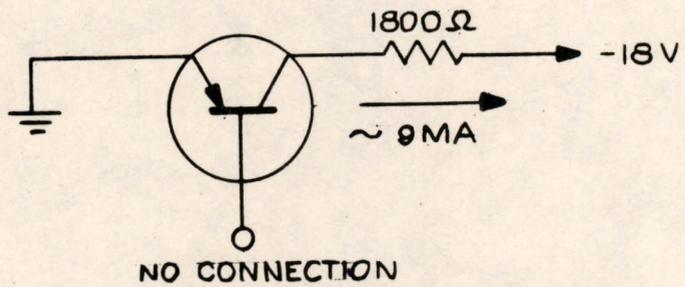


FIG. 9
DRIVER FOR 3-STAGE COUNTER

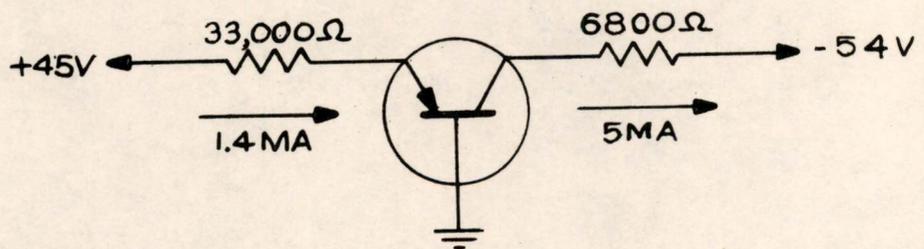
A-55555



a) CUT-OFF LIFE TEST



b) SATURATION LIFE TEST



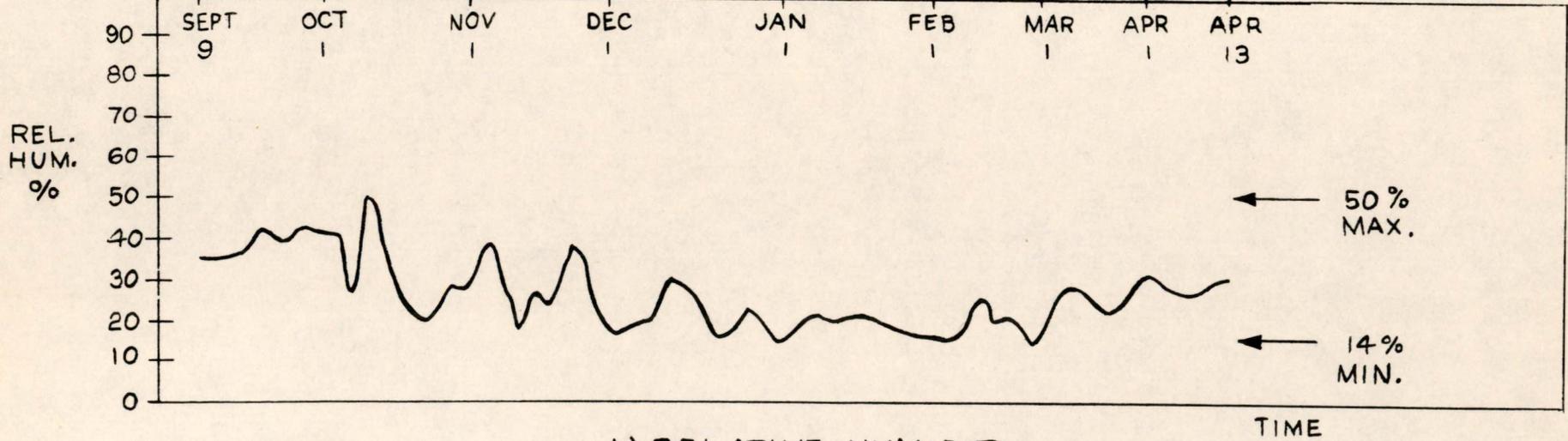
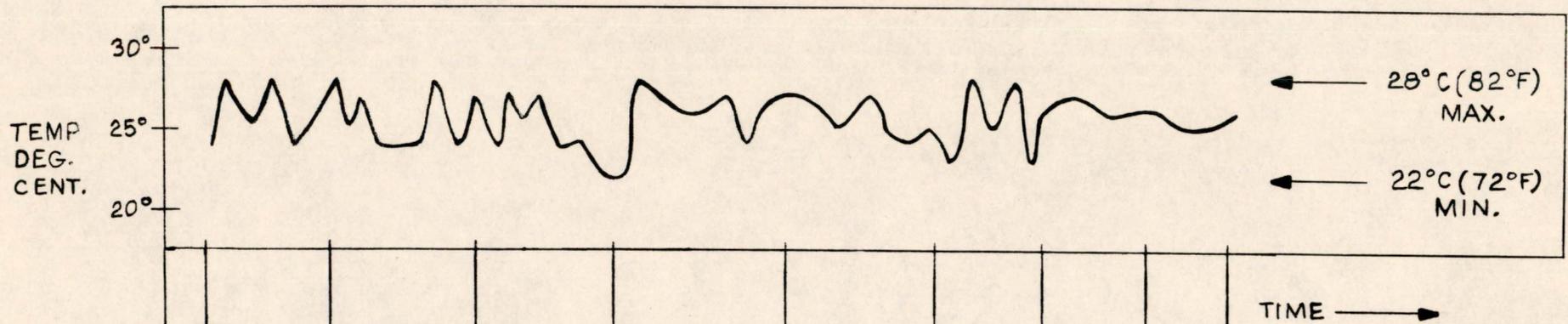
c) 120 MW DISSIPATION TEST

FIG. 10

DC LIFE TESTS

A-55721

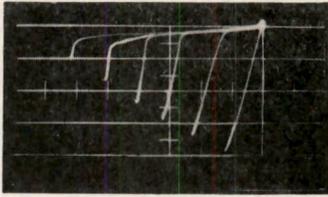
a) AMBIENT TEMPERATURE



b) RELATIVE HUMIDITY

FIG. 11

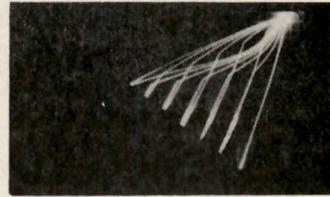
ORIGINAL



B-184

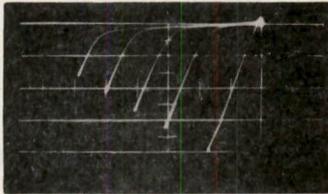
α 2.2
 r_{CO} 34K
 V_{C34} 2.7V

AFTER FAILURE



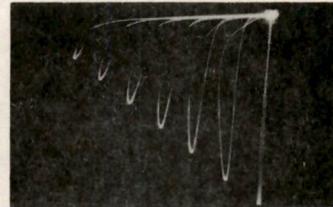
FAILED* AT

1100 HRS.

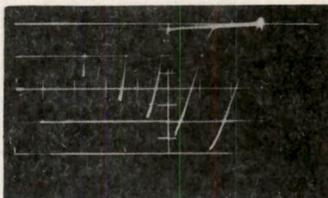


B-187

α 2.8
 r_{CO} 23K
 V_{C34} 1.0V

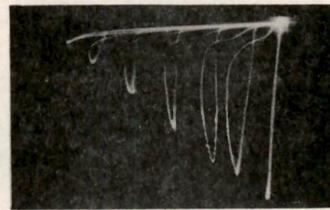


1400 HRS.

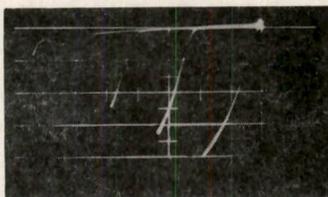


B-198

α 2.5
 r_{CO} 22K
 V_{C34} 1.3V

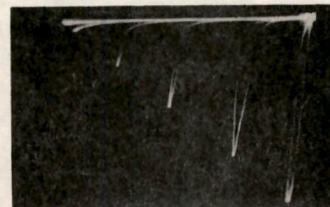


2800 HRS.

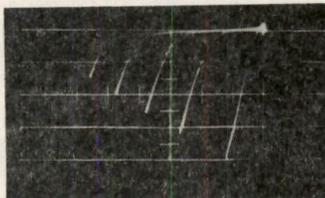


B-221

α 3.6
 r_{CO} 24K
 V_{C34} 0.9V

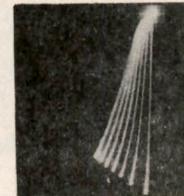


2000 HRS.



B-215

α 2.7
 r_{CO} 24K
 V_{C34} 1.0V



600 HRS.
FAILED AT 600HRS. WITH
 $\alpha=6.4, r_{CO} < 15K.$
ON CONTINUED IMMERSION
CHANGED TO CONDITION AT
LEFT AT 3000 HRS.

* THESE TIMES ARE PROBABLY HIGH. SEE TEXT.

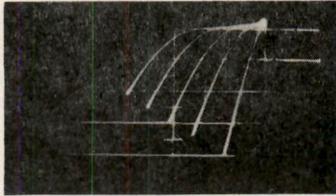
FIG. 12

IMMERSION LIFE TEST

BELL 1698 TRANSISTORS

(STARTED JUNE 52)

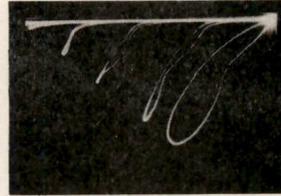
ORIGINAL



G-673
(T-67)

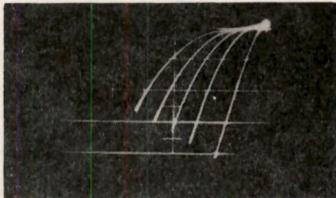
α 2.1
 r_{CO} 24K
 V_{C34} 2.2V

AFTER
FAILURE



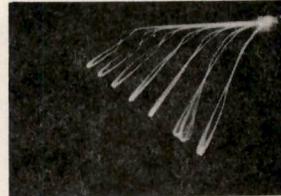
FAILED* AT

500 HRS.

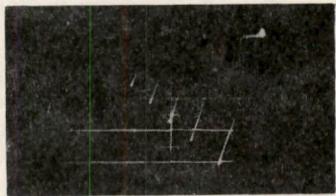


G-674
(T-98)

α 1.5
 r_{CO} 19K
 V_{C34} 4.1V

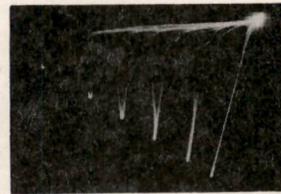


1300 HRS.



G-675
(T-59)

α 2.0
 r_{CO} 27K
 V_{C34} 3.6V



1000 HRS.



G-763
(V-8)

α 2.8
 r_{CO} 9K
 V_{C34} 1.9V



1000 HRS.



G-773
(W-98)

α 1.9
 r_{CO} 25K
 V_{C34} 1.4V



1000 HRS.

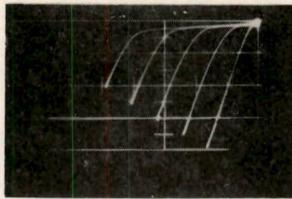
* THESE TIMES ARE PROBABLY HIGH. SEE TEXT.

FIG. 13

IMMERSION LIFE TEST

GE G11A TRANSISTORS
(STARTED JUNE 52)

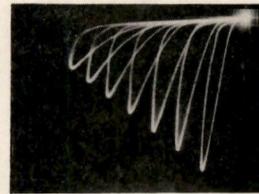
ORIGINAL



R-722
(R5221)

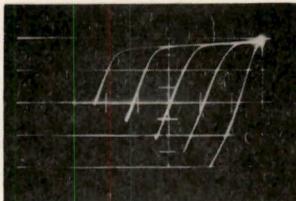
α 1.8
 r_{CO} 17K
 V_{C34} 1.3V

AFTER
FAILURE



FAILED*AT

1300 HRS.

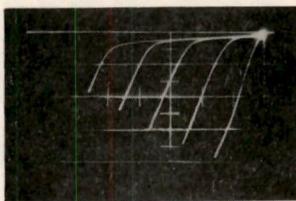


R-723
(R5413)

α 2.1
 r_{CO} 26K
 V_{C34} 1.5V

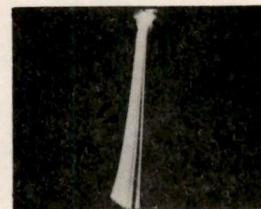


3300 HRS.

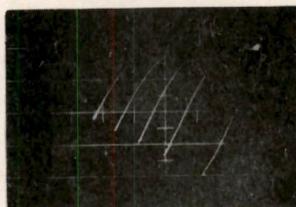


R-724
(R5420)

α 2.2
 r_{CO} 23K
 V_{C34} 1.4V

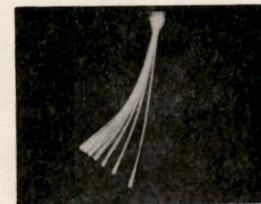


3100 HRS.

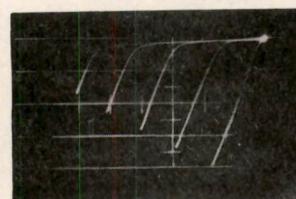


R-725
(R5492)

α 2.4
 r_{CO} 32K
 V_{C34} 1.1V

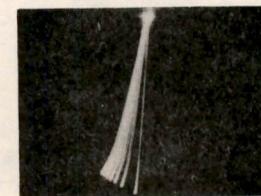


1600 HRS.



R-726
(R5520)

α 2.6
 r_{CO} 2.6K
 V_{C34} 1.2V



1600 HRS.

*THESE TIMES ARE PROBABLY HIGH. SEE TEXT.

FIG. 14

IMMERSION LIFE TEST
RCA TA 165 TRANSISTORS
(STARTED JUNE 52)

R. Bush

Division VI - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SWITCH-CORE DESIGN AND POWER LOSS

To: N. H. Taylor

From: J. Raffel

Date: August 7, 1953

Abstract: Criteria for the design of switch cores to be used in a magnetic-matrix switch are established. Core loss is shown to depend only on the average value of net ampere-turns excitation if certain assumptions are made about memory requirements and switch construction. Temperature effects on core output are discussed, and the problem of heat dissipation is considered. Comparison of 2 ferrite and 1 metallic core materials show the latter superior, and specifications are given for a metallic core which should be capable of driving a magnetic memory without cooling although such operation would probably be marginal under the worst possible operating conditions.

Introduction

The principal problem in the design of a magnetic-matrix switch has been essentially that of designing a saturable core transformer to provide a current pulse specified in shape and amplitude into a specified load. The latest 32-position switches represent the results of efforts in this direction.

Of late it has become necessary to recall that the core in the matrix switch is really a device for distributing blocks of energy, often at very high repetition rates; that the losses in the core are considerable; and that heating is a problem of great importance, since magnetic cores are in general temperature-sensitive components.

I. Excitation and Core Output

The voltage output from a core is a function of the flux in the core and the net ampere-turns linking it. Two voltage waveforms of interest are shown in Figures 1 and 2 with the corresponding excitations which produce them. The first corresponds to driving with a current source (the case of a memory core, for instance). The second corresponds to a voltage-source drive which might be used to produce a flat-topped pulse from a switch core. (This assumes perfect coupling which is approached in most square-looped materials.)

The total energy loss in a core being switched is expressed by:

$$W = \int_0^T NI_{net} \cdot v dt \quad (1)$$

where $v = \frac{d\phi}{dt}$ is the rate of change of flux in the core and T is the switching time.

For constant i or constant v, the two cases considered above, this reduces to

$$W = NI_{net} \cdot \Delta \bar{\Phi} \quad (2)$$

where $\Delta \bar{\Phi}$ is the total flux change of the core switching and NI_{net} is the time-average value of NI_{net} . The d-c hysteresis loop for a square-loop material is shown in Figure 3. We recall that the change in flux is given by the area of the voltage pulse on a single turn linking the core. It is immediately apparent from an examination of Figures 1 and 2 that the d-c loop does not give an accurate account of the operating point of the core under pulsed conditions. If it did, the time response could, of course, be predicted from the shape of the input current pulse and the d-c loop alone.

It is also clear that the energy loss of a core switching under pulsed conditions is not given by the area of the d-c loop, but rather by the area of the appropriate pulsed loops drawn roughly in Figures 5 and 6 for constant current and constant voltage drives, respectively. (In drawing these it was assumed that there was no flux change on the rising edge of the current pulse.) The added energy may be thought of as going into relaxation and eddy-current losses.

For rise times used in the magnetic-matrix switch the assumptions made above are well justified; at worst they give a slightly exaggerated estimate of the energy loss in the core.

II. Switch as Used with Memory

The requirements for a memory of the coincident-current type using MF-1326, F-291, cores are:

- 1) $I_2 \approx 1/2$ amp;
- 2) $R_2 \approx 64$ ohms;
- 3) Driving-current shape as shown in Figure 4

These conditions are imposed because:

- 1) The current amplitude must be half that necessary to switch a core;
- 2) The resistive termination must be such that the back voltage of 32 memory cores switching will be small compared to the total voltage across the secondary of the switch core. The back voltage for 1 memory core is about 0.1 volt; for 32 cores, 3.2 volts. If we assume that a change in secondary current of less than 10% due to back voltage is required, then:

$$I_2 R_2 \approx 10 \times 3.2 \text{ volts}$$

$$R_2 \approx \frac{32}{I/2} = 64 \text{ ohms}$$

It is possible that this estimate of $I_2 R_2$ may be too low since it would allow for a 10% dip in the current pulse from the switch core. For a 2% change, for instance, the switch-core output would require 150 volts or a terminating resistance of 300 ohms.

Two switch cores must be pulsed each time a memory address is to be selected. Since one core must supply pulses to all memory cores with the same x (or y) address, it is possible that a single switch core may be required to produce outputs many times in succession for certain programs. If we assume a total read-write cycle of 10 microseconds, a single switch core may be operating at a prf of 100 kc for a considerable period of time. In any case, conservative design demands that such a contingency be provided for.

III. Switch-Core Design

In switch-core design, three relations governing core operation must be kept clearly in mind. We can formulate them as follows:

$$N_2 \Delta \bar{\Phi} = I_2 R_2 T \quad (3)$$

$$\Delta \bar{\Phi} = f(N_1 I_1) \quad (4)$$

$$T = g(N_{\text{net}}) \quad (5)$$

where

T is the output-pulse length;

R_2 is the secondary resistance;

$N_{\text{net}} = N_1 I_1 - N_2 I_2$ (capitals indicate time-average values).

Equation 3 is merely a particular example (for a square pulse) of the general equation which states that the area of the secondary voltage pulse equals the number of secondary flux linkages.

It is important to note that $I_2 R_2$, and T are usually specified beforehand in switch design; therefore the product $N_2 \Delta \bar{\Phi}$ is fixed and represents a prime design criterion.

Equation 4 states that the total flux change depends only on the input ampere-turns. This is true only if the secondary pulse is allowed to go to completion before the input current pulse has ended. The functional relationship is best expressed graphically. The curve is much the same in shape as the familiar magnetization curve for iron except that the entire curve is shifted by a constant amount along the NI axis. This shift is an indication of the square-loop characteristic of the material. Its shape of course depends

on the particular square-loop material being used. Curves for MF-1312, F-262, for MF-1131, F-262, and for mo-Permalloy 4-79 1/4 mil, 1/4-inch wrap are shown in Figure 7. In order to eliminate inequalities in output due to pulse-sequence sensitivity arising from unequal biases on different cores, the switch is generally designed to operate in the saturated region of the $\Delta \bar{\Phi}$ vs $N_1 I_1$ curve.

Equation 5 says that the switching time T depends on the net ampere-turns linking the core. This expression, unfortunately, is the one most difficult to evaluate explicitly. In order to obtain this data, the core with its secondary open-circuited is excited with a low-impedance source. This yields a flat-top voltage pulse on the secondary and the driving current gives a direct measure of NI_{net} .

We can use the three equations above (with their corresponding graphs) and certain constraints imposed by memory-driving requirements to outline the steps to be followed in designing a switch from any given core material. If it is assumed that $N_1 I_1$ is limited by tube and construction restraints to some maximum value and that I_2 , R_2 , and T are constants fixed by the memory, the design procedure is as follows:

1. Determine NI_{net} for the value of T required;
2. Find N_2 from the equation $N_2 = \frac{N_1 I_1 - NI_{net}}{I_2}$ where all of the quantities on the right side of the equation are now fixed;
3. Determine the $\Delta \bar{\Phi}$ required from $\Delta \bar{\Phi} = \frac{I_2 R_2 T}{N_2}$;
4. Calculate the height of the core needed to supply the necessary $\Delta \bar{\Phi}$ from the magnetization curve for the material.

For these assumptions, then, switch-core design and the consequent power loss are fixed. Core loss may now be expressed as a function of NI_{net} alone using the results obtained above.

$$\begin{aligned} W &= NI_{net} \cdot \Delta \bar{\Phi} \\ &= NI_{net} \frac{I_2^2 R_2 T}{N_1 I_1 - NI_{net}} \end{aligned} \quad (6)$$

This last equation shows that core loss depends only on NI_{net} and that its variation with NI_{net} is more than linear since NI_{net} appears with a minus sign in the denominator of the second factor.

It was stated above that the design was completely fixed once we assumed a fixed value of $N_1 I_1$ which was the largest physically obtainable. This was done, since increasing $N_1 I_1$ to its maximum tends to decrease core loss as shown by Equation 6, above. It may be desirable to reduce $N_1 I_1$ in order to place less of a load on the driver tubes. Such reduction will cause

the losses to increase, and some kind of compromise between high driving current and high core loss will have to be made. At present, heating seems to be the predominant difficulty so that maximum driving ampere-turns will be used in subsequent calculations in this memorandum.

IV. Core Loss

Temperature effects on core output

Tests on different materials show the same general effects of temperature on output waveform as shown in Figure 8. It is important to note that variation in output with changes in temperature is not a discontinuous phenomenon but occurs throughout a large range of temperatures. In the range from -20 C to 100 C, pulse amplitude increases and switching time decreases fairly linearly with incremental increases in temperature. It seems reasonable to define workable temperature limits in terms of the greatest difference in core temperature which can be tolerated in a switch. We will call this temperature ΔU and note that it should be no less than the difference between the maximum core temperature (core being pulsed at 100 kc) and the ambient temperature. The allowable ΔU will be determined by how much variation in output waveform we can tolerate and will depend on the core material used. We arbitrarily limit variations in core output to switching-time change no greater than 0.2 microsecond (out of total length of 2.5) and amplitude change less than 3%.

Heat dissipation in core

Once the maximum power loss in the core has been determined as well as the allowable temperature rise and the area of the core, it is convenient to formulate a measure of the required amount of heat to be dissipated per degree centigrade per unit surface area of material. We denote this required coefficient of heat transfer by h ; the defining equation is:

$$h = \frac{Q}{A\Delta U}$$

where Q is the maximum power (at 100 kc);
 A is the free surface area; and
 ΔU is the allowable temperature rise.

The results of cooling tests in still air and with small-fan cooling are shown in the curves of Figure 8. They indicate that maximum values of h obtainable with still air are about 0.025 watts per in² per degree centigrade; with a concentrated blast of air from a small fan, an h of 0.14 watts per in² per degree centigrade.

It is apparent from the above analysis that the problem of heat dissipation is a direct function of the material used. The two most important factors are NI_{net} (which alone determines core loss) and ΔU (the allowable temperature rise in a core), both of which vary greatly for different materials. A third factor whose effect is not quite so easy to estimate is the flux per unit volume of material. In order to make a reasonable comparison between

different core materials it is necessary to assume that any core material could be redistributed so that the over-all dimensions would be comparable for different materials. It is also necessary to assume some maximum fixed height of core material (imposed probably by wiring restrictions). Otherwise the material could always be stretched out to give enough area to provide the necessary dissipation. If all the materials then are of the same height, the flux per unit volume for each will determine the required outside diameters for each, assuming the inside diameters are unchanged. This outside diameter will then give a measure of the free surface area for cooling for each material. The assumption is made that cooling in the switch only takes place at the surface lying on the outside diameter.

When considering heat dissipation from a core the tacit assumption has been made that there was no temperature gradient within the core and that cooling was merely governed by the equation:

$$Q = hA\Delta T$$

However, it is clear that the larger the difference between inside and outside diameters the less valid this assumption of uniform core temperature. It would therefore seem desirable to include in any comparison of materials a measure of the difference between inside and outside diameters which will be denoted by "L". For this comparison, L is not measured on the original core but rather on the "redistributed" core obtained by making cores of equal height and required total flux with inside diameter unchanged. The results of this comparison between three materials on the basis of h and L appear in Figure 10 in tabulated form. A maximum core height of 2 inches is assumed. Maximum N_1I_1 is assumed to be about 4.0 ampere-turns.

The table indicates clearly the advantage of metallic cores over ferrites from the point of view of power-dissipation problems. Other properties which make it particularly desirable for switch-core applications are squareness of loop and saturability of the $\Delta \Phi$ vs NI curve which lead to reduced noise and greater uniformity of output, respectively. The results tabulated in Figure 10 show that the metallic core will require about 1/10 the cooling of the ferrite core. It also shows that with simple fan cooling a mo-Perm core having the following specifications should be capable of driving a memory without significant change in output due to core heating:

Tape width	2 inches
Inside radius	3/32 inch
Outside radius	0.128 inch
Material	4-79, 1/4 mil

With natural convection (still-air cooling) such a core would still produce outputs with less than 0.3 microsecond variation in pulse length and less than 3% change in amplitude.

V. Conclusions

A search for new materials should follow along the lines suggested by the analysis given above, the main criteria being fast switching time (low net ampere-turns for a given switching time), insensitivity of output to temperature change, and high flux per unit volume of core material.

The mo-Perm 4-79 had values equal to or better than any other cores tested for these three factors. These values are .75 ampere-turns for 2.5 micro-seconds switching time (from open-circuit test), 90 C allowable temperature rise, and about 30,000 maxwells per cubic inch.

It is important to realize that the energy dissipated in the core is directly proportional to the output power (Equation 6) and that as a result the losses go up directly with the terminating resistance on the secondary. The heat-dissipation problem will become more and more serious, therefore, as the current regulation is improved through higher secondary resistance. Recent tests with linear transformers indicate that extremely good regulation may be required in which case the core loss could be increased by a significant factor.

Signed: _____

J. Raffel
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Approved: _____

W. N. Papian
W. N. Papian

JIR/rb

cc: Group 63 - Staff
A. P. Kromer - (IBM)
Magnetic Memory Section - Staff
D. Shansky

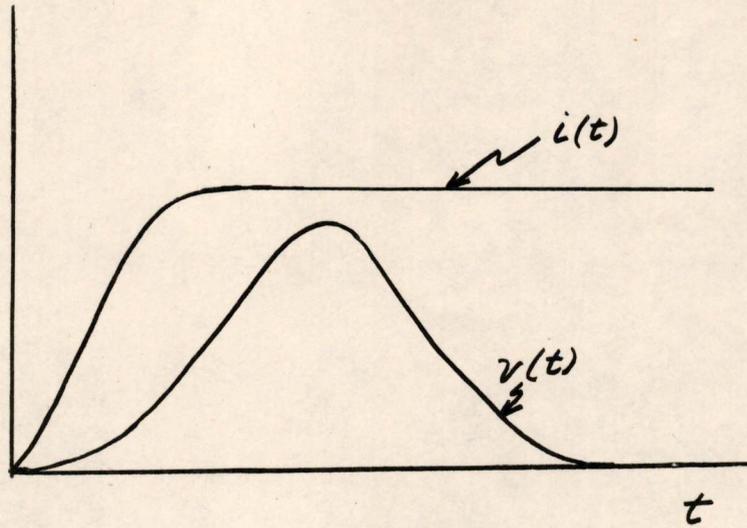


FIG. 1
EXCITATION AND OUTPUT
CURRENT-SOURCE DRIVE

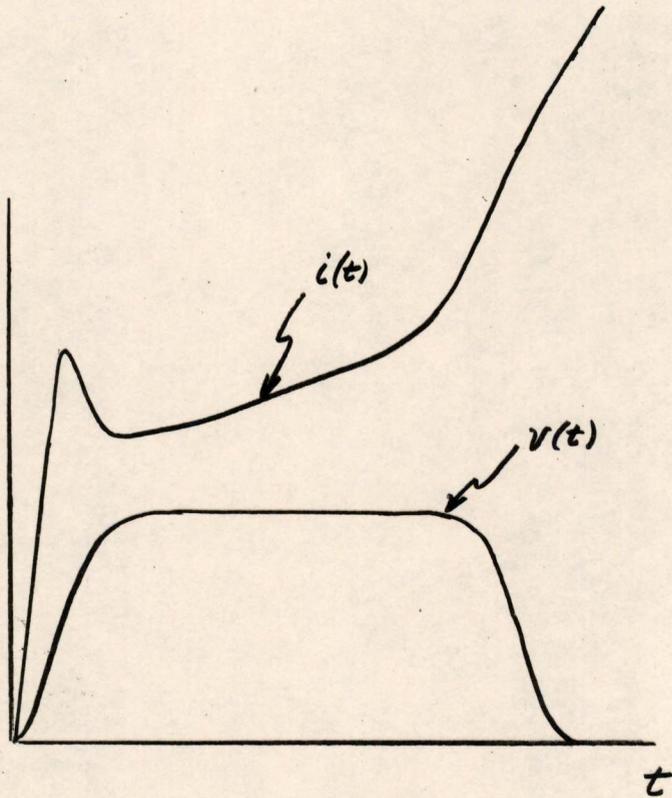


FIG. 2
EXCITATION AND OUTPUT
VOLTAGE-SOURCE DRIVE

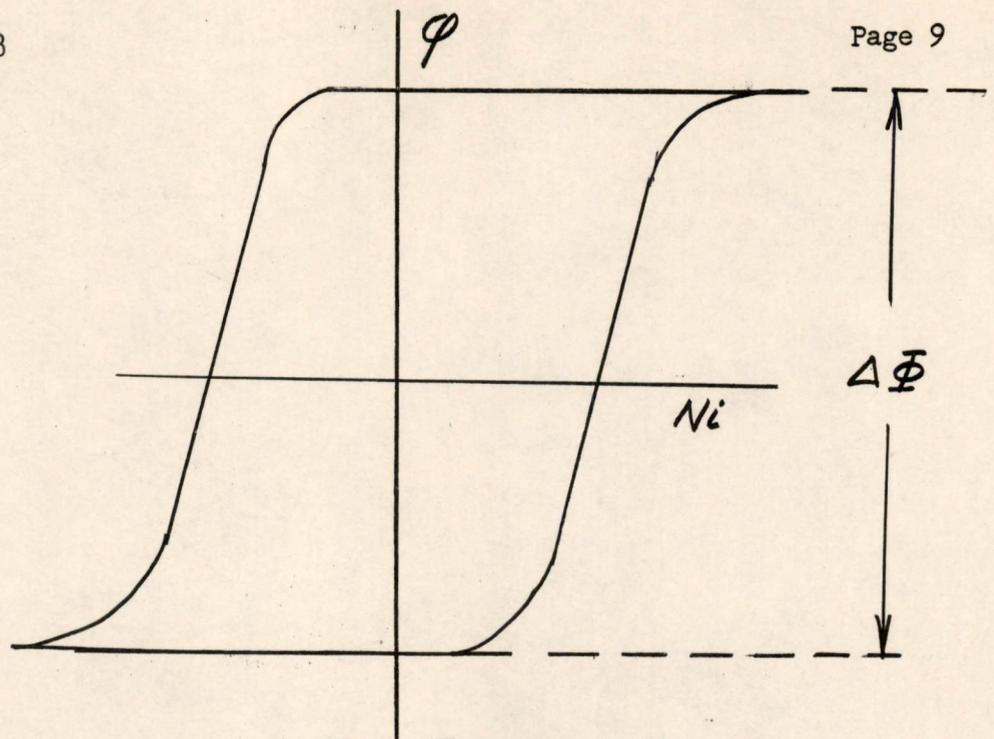


FIG. 3

A "RECTANGULAR" d-c HYSTERESIS LOOP

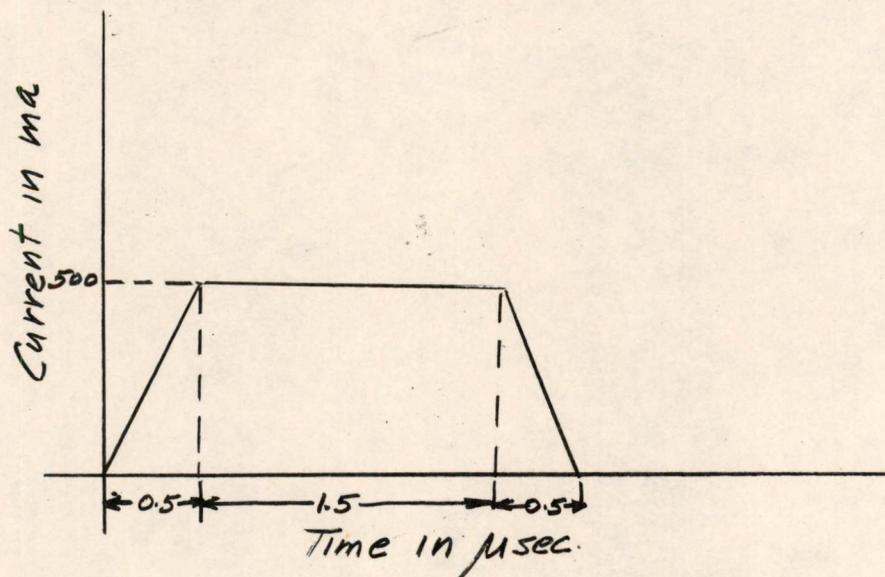


FIG. 4

CURRENT PULSE DESIRED FROM SWITCH CORE

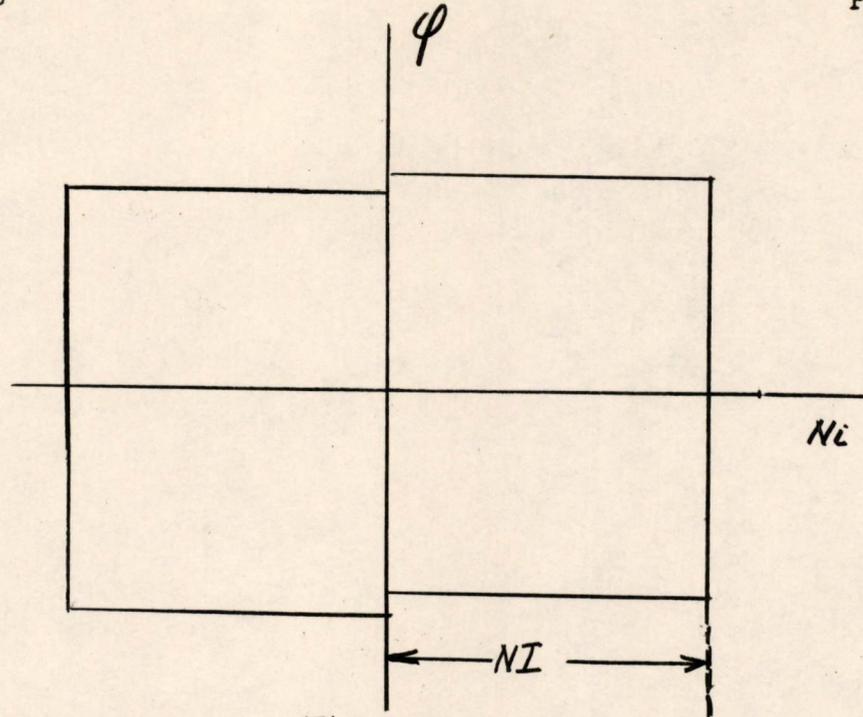


FIG. 5
PULSED LOOP
CONSTANT CURRENT EXCITATION

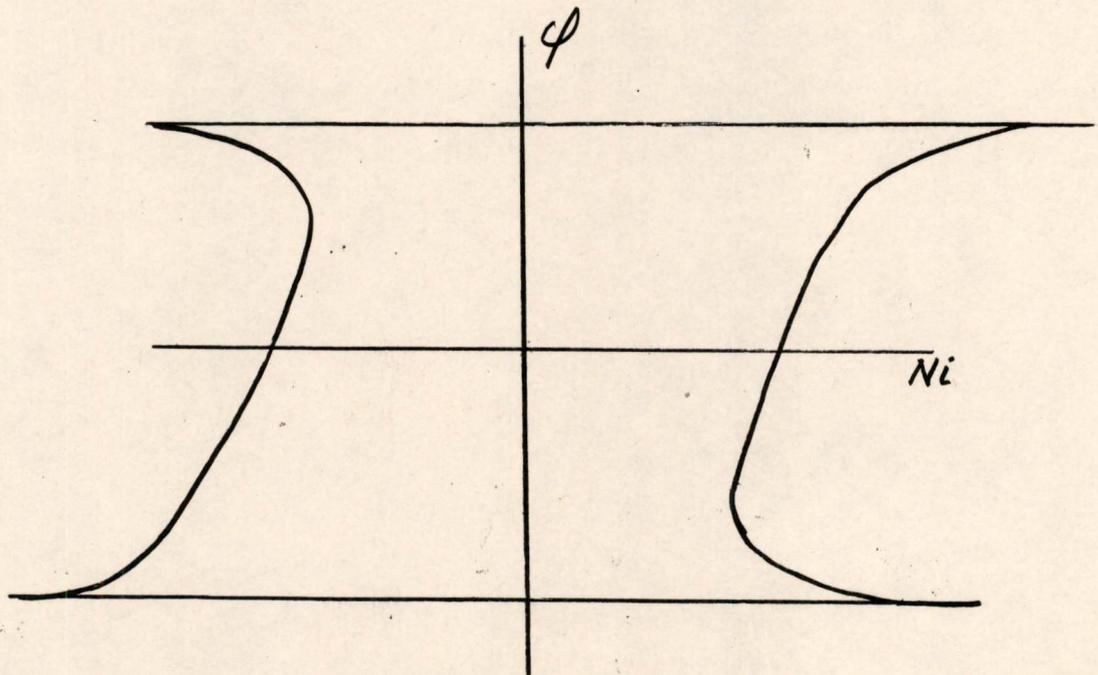


FIG. 6
PULSED LOOP
CONSTANT VOLTAGE EXCITATION

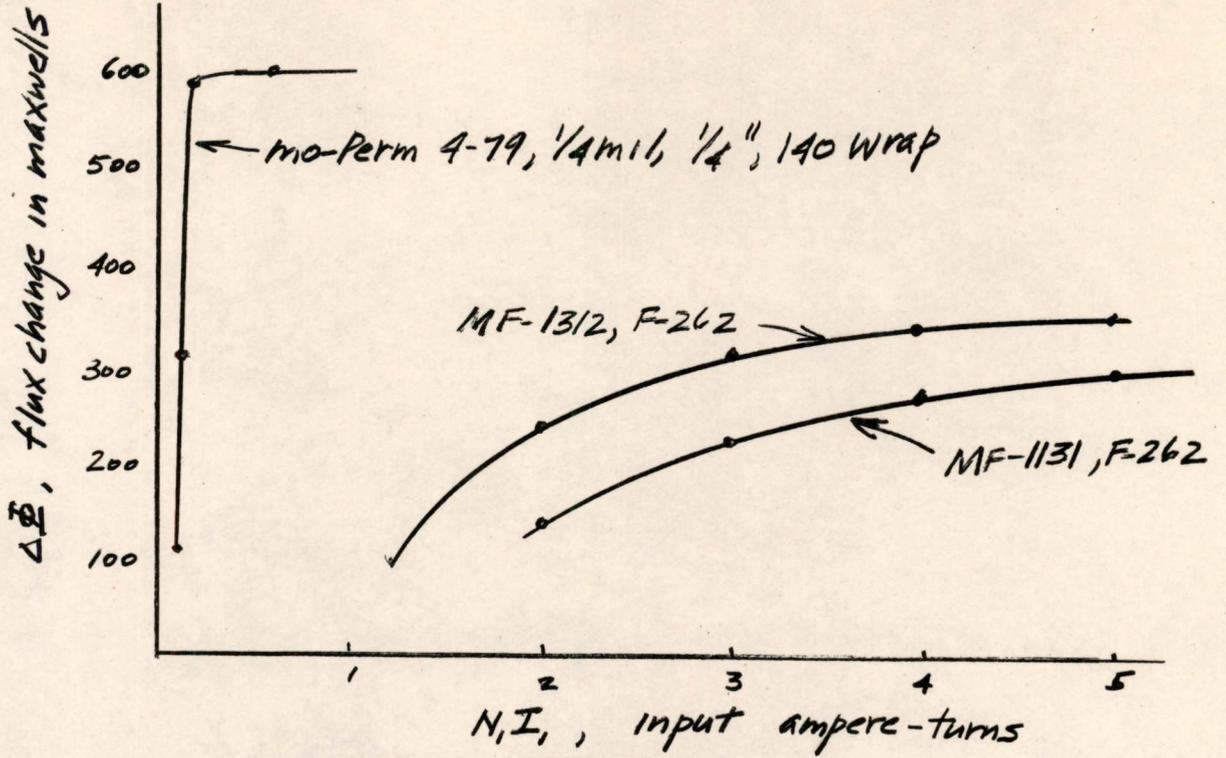


FIG. 7
FLUX CHANGE VS. AMPERE-TURNS
FOR THREE MATERIALS

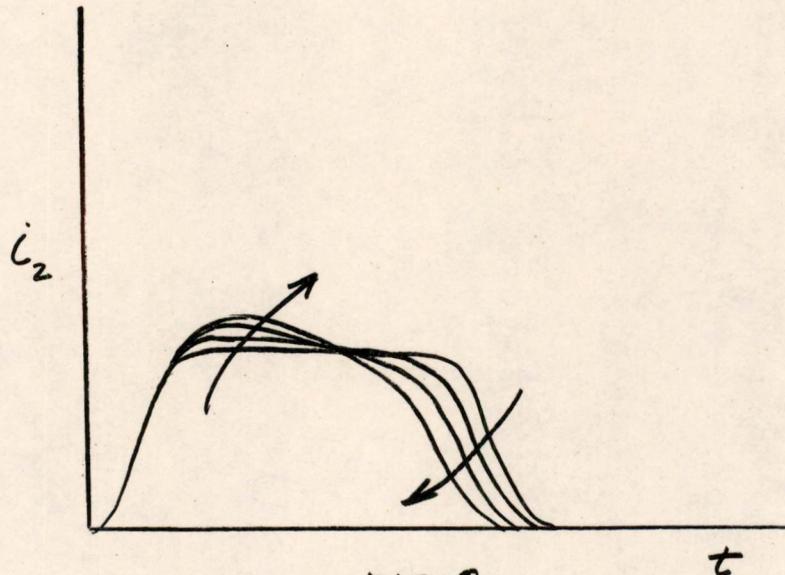


FIG. 8
EFFECT OF TEMPERATURE
ON SWITCH-CORE OUTPUT
(arrow indicates increasing temperature)

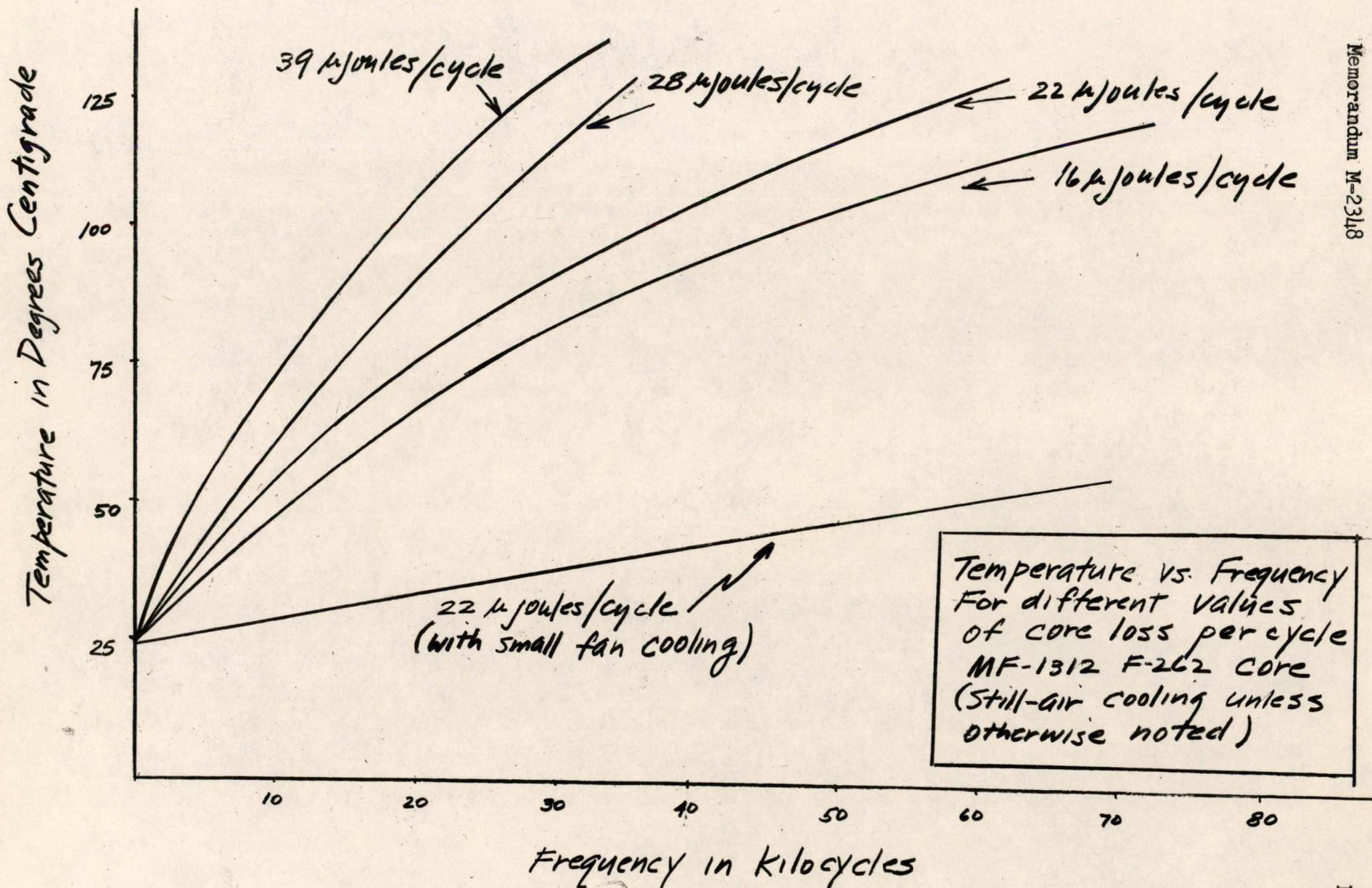


FIG. 9
TEMPERATURE RISE DUE TO CORE LOSS

Core	NI_{NET} amp- turns	N_2 turns	$\Delta \Phi$ maxwells	Flux per Unit Vol. maxwells per cubic inch	r_0 inches	L inches	ΔU Degrees Centigrade	Surface Area in. ²	Loss per cycle μ joules per cycle	h watts per degree C. per in. ²
MF-1131 F-262	2.7	3	2,500	26,600	.154	.06	35	1.94	156	.23
MF-1312 F-262	2.3	3	2,500	33,000	.143	.049	20	1.8	145	.40
mo-Perm 4-79 1/4 mil, 1/4" 140 wrap	.75	6	1,250	31,500	.123	.029	90	1.55	22.5	.016

FIG 10

DESIGN CALCULATIONS FOR SWITCH CORES OF THREE MATERIALS,
IN TABULAR FORM

Olsen

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: DURATION AND RESISTANCE OF SHORTS IN THE TUBE TYPES 6145 AND 5965

To: J. W. Forrester

From: S. Twicken

Date: August 14, 1953

ABSTRACT: Vacuum tube shorts are caused generally either by loose particles or by some mechanical defect. The laboratory shorts tester is capable of detecting a cathode to control grid dead short in about 1 μ second and one of 100K ohms in about 8 μ seconds. Like shorts between other electrodes require a somewhat longer duration for detection. A special test to determine distribution curves of duration and resistance of shorts in the 6145 and 5965 was performed. The laboratory shorts detector appears capable of definitely picking up 90 per cent of the flicker shorts observed with 4 per cent marginal and 6 per cent incapable of detection. This 6 per cent probably does not constitute a potential source of trouble.

INTRODUCTION

Vacuum tube shorts are caused generally either by loose particles, usually lint converted to carbon during processing, or by some kind of mechanical or structural defect such as enlarged holes in the supporting mica spacers which allow movement of electrodes, deformed elements which reduce nominal spacings, or poor welds. Under shock or vibration the lint particles may move about shorting the tube elements, or there may be actual movement or deflection of electrodes which cause them to short one another, or both. As herein used, a "short" exists without any applied shock. A "tap short" is induced by impact and continues for at least some tenths of seconds after the impact. A "flicker short" is one which is induced by impact but which lasts no more than several milliseconds. Shorts must also be defined in terms of their resistance. In addition the intensity of impact must be specified as part of the description of a short.

Tap and dead shorts are of no exceptional concern in measurements since they can usually be detected by any equipment designed to detect the shorter duration flicker shorts. Flicker shorts have been observed ranging in resistance from zero ohms to a megohm or more and in duration from 3 to 1000 microseconds or more. Ideally the minimum acceptable resistance should be determined by the minimum resistance which gives unreliable circuit operation e.g., a grid to cathode flicker short of 5 megohms will not cause anywhere near the trouble of one of 5000 ohms. This criterion is, of course, not practically feasible when circuit applications are varied. The problem of minimum duration is of the same nature.

THE LABORATORY SHORT TESTER

The detector currently in use on the Model II Tube Tester, the design of which is due in large part to H.B. Frost, detects resistances up to about 3 megohms in 3-4 milliseconds and a dead short in a few microseconds. Its resistance-time characteristic for cathode to control grid shorts is shown in Figure 1. The characteristic for shorts between other elements is displaced upward somewhat so that a suppressor grid to plate short of one megohm can be detected in 100 microseconds while a dead short between those electrodes can be detected in about 2 microseconds.

The method of detection is shown in Figure 2. A string of 2D21 thyratrons is hung on a voltage divider between ground and a negative supply voltage, the grids of the thyratrons being about 14 volts more negative than the cathodes and normally cut-off. There is a 60 volt difference in potential between adjacent electrodes of the tube under test. A hypothetical short is shown between cathode and control grid. The current through this resistance makes the grid bias of V1 less negative due to the voltage drop across the parallel combinations of resistors in the grid circuit and if this current is high enough (short resistance low enough), V1 will fire and the neon light in its plate circuit will indicate a cathode to control grid short. Similarly, a short between any two electrodes will cause the thyatron of the more negative electrode to fire.

The tube under test, in a horizontal position, is rotated about its longitudinal axis by a reversible motor whose direction of rotation is changed every 360° by a cam on its shaft. During one test cycle the tube makes a 360° rotation clockwise and then returns to its initial position. While the tube is rotating, it is automatically tapped about every 90° of rotation by a solenoid tapper. Thus, on the shorts test, the tube is tapped eight times. The intensity of impact is variable and is set at about 50g as measured with a Gulston A-314 accelerometer. The indicating circuits are of the lock-in type, i.e., once a thyatron has fired and a neon light indicating a short is turned on, it will remain on until the foot switch initiating the cycle is released by the operator.

SPECIAL TEST METHOD

A program was recently undertaken to determine the distribution of short duration and resistance in two common tube types, the 6145 and 5965: first, to discover whether any troublesome shorts are incapable of detection by the current equipment; and second, to obtain much needed information on these distributions. The tubes were tapped manually with a reasonable facsimile of a MIL- approved tapper.¹ This consists of a 6 inch long rod with a cork head which is swung through an arc of 2 inches. With manual tapping, the intensity was not as uniform as that of the automatic tapper and was greater. The circuit schematic for this test is shown in Figure 3. A short between control grid and any other electrode produces across the 1K load resistor a voltage which is fed into the scope and used to trigger the sweep. A Polaroid Land camera was used to record the results. It was not possible to photograph every short because of the randomness of occurrence of some shorts,

1

Military Specification MIL-E-1B, Amend. 1

especially those caused by moving lint. It was necessary to cause the tube to short a sufficient number of times for the scope sweep speed to be set to an appropriate value. The camera was then closed up, the shutter opened and the tube tapped until a short occurred, a short being indicated by the switching over of a 2^6 counter whose input came from the "Gate Output" of the scope.

TEST DATA

Lot 1:

A lot of 179 6145's rejected by the automatic tapper for shorts was tested by this method. Seventy-one tubes showed tap or dead shorts while flicker shorts in twenty-three tubes were recorded on film. Unfortunately, the number of tubes which shorted only once or twice and could not be photographed was not recorded. As measured by the accelerometer previously mentioned, the tubes were given an impulse of about 50-60 g. lasting 500 μ seconds. Distribution curves of duration and resistance of the shorts are shown in Figures 4 and 5. In the case of tubes with multiple shorts only the one of longest duration is plotted, since the shorts indicator should be able to detect the longest short produced by any given tube. All signals definitely attributable to tube flicker shorts were of 10 μ sec. duration or longer, with the median about 100 μ sec. The median of the resistance distribution is about 100K ohms. Sixty-five per cent of the shorts fall between 30 and 300 μ sec. duration. Tubes with tap or dead shorts sometimes show spikes of a few tenths of microseconds on impact. Since the shop equipment will not detect shorts of less than one μ second duration, it is important to note that these short spikes were found only in tubes which had been picked up as dead or tap shorts.

Lot 2:

Ninety-three 6145's which had passed the shop test were tested. Results are shown in Table I.

TABLE I

No shorts	79
Shorted once	1
Tap shorts	5
Flicker shorts	<u>8</u>
Total	93
% showing no shorts	80%

Distribution curves of duration and resistance of the flicker shorts are shown in Figures 6 and 7.

In view of the randomness of some shorts and the increased acceleration on this test, the figure of 80 per cent exhibiting no shorts is felt to be fairly good. The thirteen tap and flicker shorts on retest on the automatic tapper showed only four failures.

Lot 3:

One hundred and ten 5965's rejected for shorts at incoming inspection were tested. Results are shown in Table II.

TABLE II

No shorts	45
Tap shorts	15
Shorted once	16
Flicker shorts	29
Dead shorts	<u>5</u>
Total	110

Distribution curves of duration and resistance of these shorts are shown in Figures 8 and 9. The intensity of tapping on this test was about 150 g. The short of least duration observed was 9 μ seconds with the exception of one tube showing spikes of a few tenths of microseconds. There is some question as to whether this one was in fact a short or only socket noise as was experienced with some other tubes.

The median here again is about 100 μ sec. Seventy-one per cent of the shorts fall between 30 and 300 μ seconds which is quite similar to the 6145 distribution (Fig. 4) wherein 65 per cent of the shorts fall between the same duration limits.

Lot 4:

Twelve 5965's were tested as a separate lot, seven of which had failed at initial test for shorts and five for low plate current. Of the seven rejected for shorts, four were found and recorded on film. Of the five rejected for low current, one shorted once, one showed an intermittent tap short, and one showed a flicker short. It should be noted again, however, that the intensity of tapping on this manual test was higher than that on the automatic tapper by about 50 per cent.

Lot 5:

Ninety-nine 5965's which had been passed by the automatic tapper were tested. Results are shown in Table III.

TABLE III

No shorts	90
Flicker shorts	5
Tap shorts	<u>4</u>
Total	99
% showing no shorts	91%

Again in view of the randomness of the nature of some shorts and the increased acceleration on the manual test, this figure of 91 per cent is felt to be rather good.

CONCLUSION

Of sixty-five flicker shorts whose resistance and duration were recorded, only four lie below the curve of Figure 1 in the region where they are theoretically incapable of detection by the tester; three additional shorts are marginal. Resistance and duration of these four shorts are shown in Table IV.

TABLE IV

<u>Resistance (Approx.)</u>	<u>Duration</u>
0.8 mehogm	25 μ sec.
1 "	10 "
1 "	10 "
0.16 "	3 "

The intermittent-short detector is capable of detecting about 90 per cent of the flicker shorts observed with about four per cent marginal and six per cent incapable of detection. Whether this six per cent represents a potential source of trouble is open to considerable question.

The distribution curves of short duration are quite similar for the two types tested. For dimensional comparison, the cathode to control grid spacing of both tubes is about five mils while the control grid to plate spacing of the 5965 is about 11 mils and the control to screen grid spacing of the 6145 is about 14 mils.

Only four flicker shorts were observed with a resistance higher than 750K ohms. This compares quite favorably with a recommendation by the Armour Research Foundation² to set 750K ohms as the maximum value to be considered a short. On the other hand, they recommend in the same report setting 100 microseconds as the minimum duration to eliminate false indications of shorts, caused by extraneous transients in the system. This is not borne out by our tests on the 6145 and 5965 which show about 55 per cent of all flicker shorts lasting less than 100 microseconds. This discrepancy may have been caused by the difference in impulse length, 500 μ seconds in these tests but one millisecond in the Armour test.

Signed

S. Twicken

S. Twicken

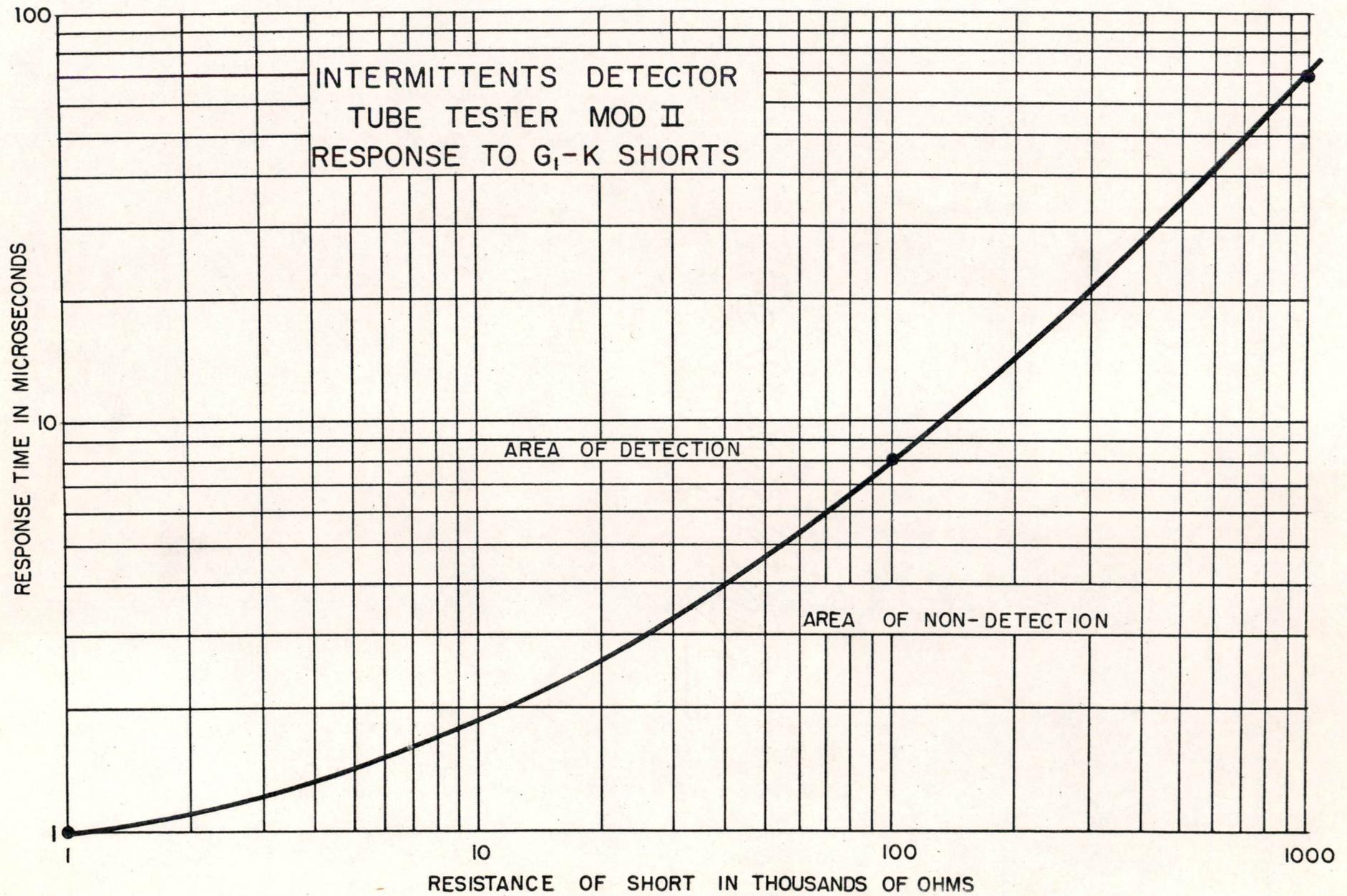
Approved

H. Wainwright

H. Wainwright

Encs: A 55385 (Fig.1)
 A 55386 (Fig.2)
 A 55387 (Fig.3)
 A 48440 (Fig.4)
 A 48436 (Fig.5)
 A 48437 (Fig.6)
 A 55433 (Fig.7)
 A 48439 (Fig.8)
 A 48438 (Fig.9)

² Armour Research Foundation, Project No. 90-568E, Report No. 88



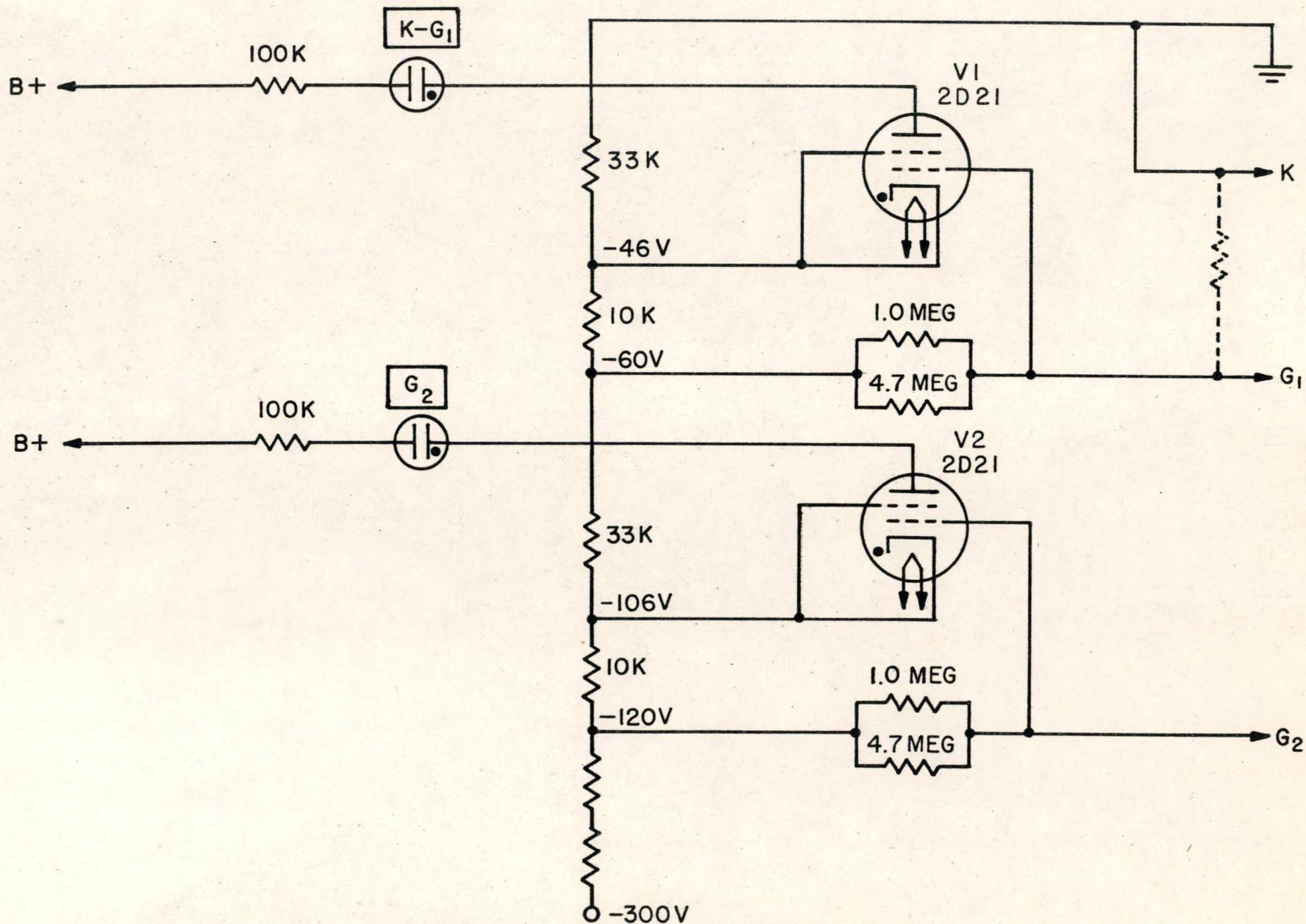


FIG.2

METHOD OF SHORT DETECTION

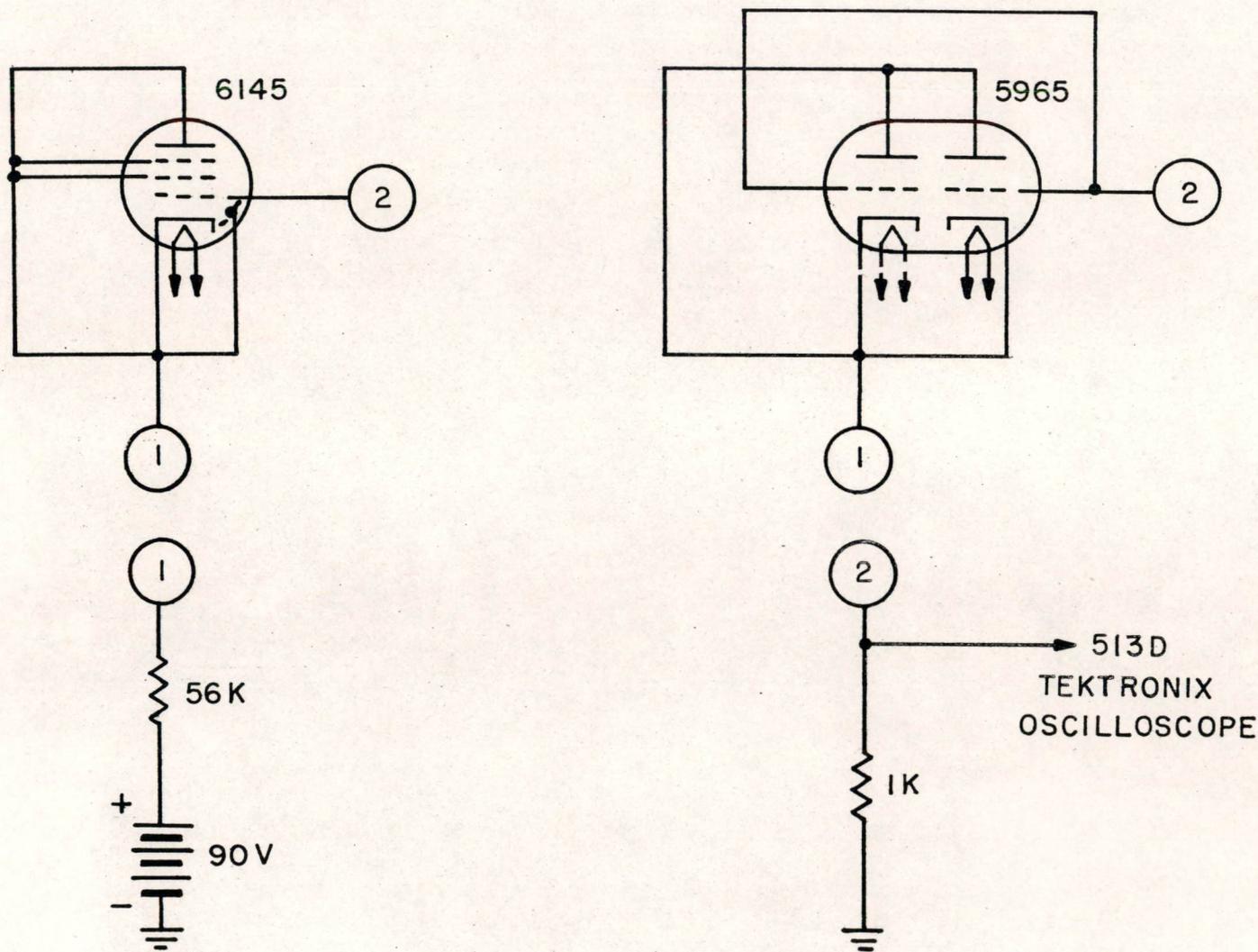


FIG. 3.
SPECIAL TEST CIRCUIT

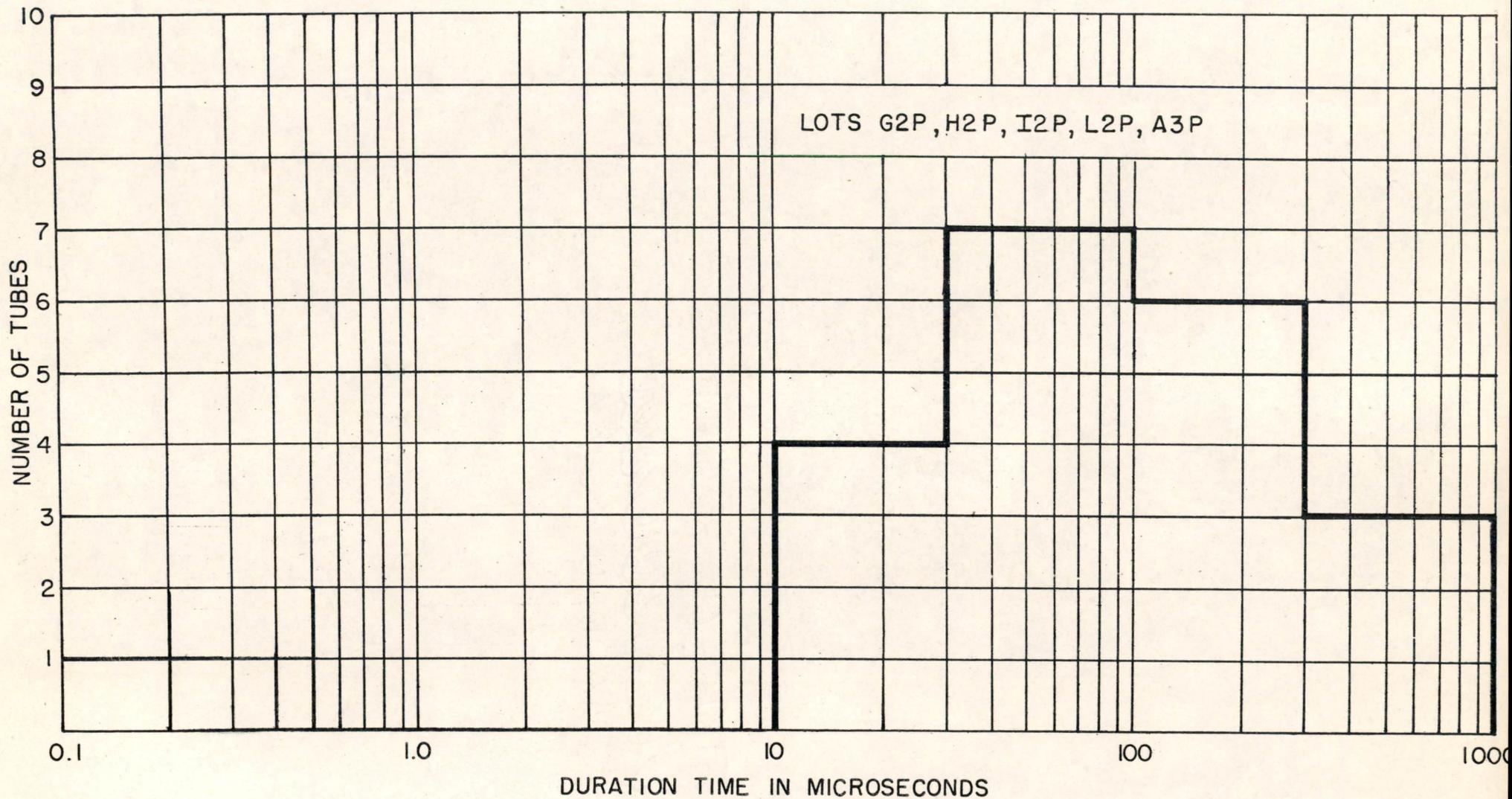


FIG. 4
DISTRIBUTION CURVE
6145 REJECTS - DURATION OF LONGEST SHORT

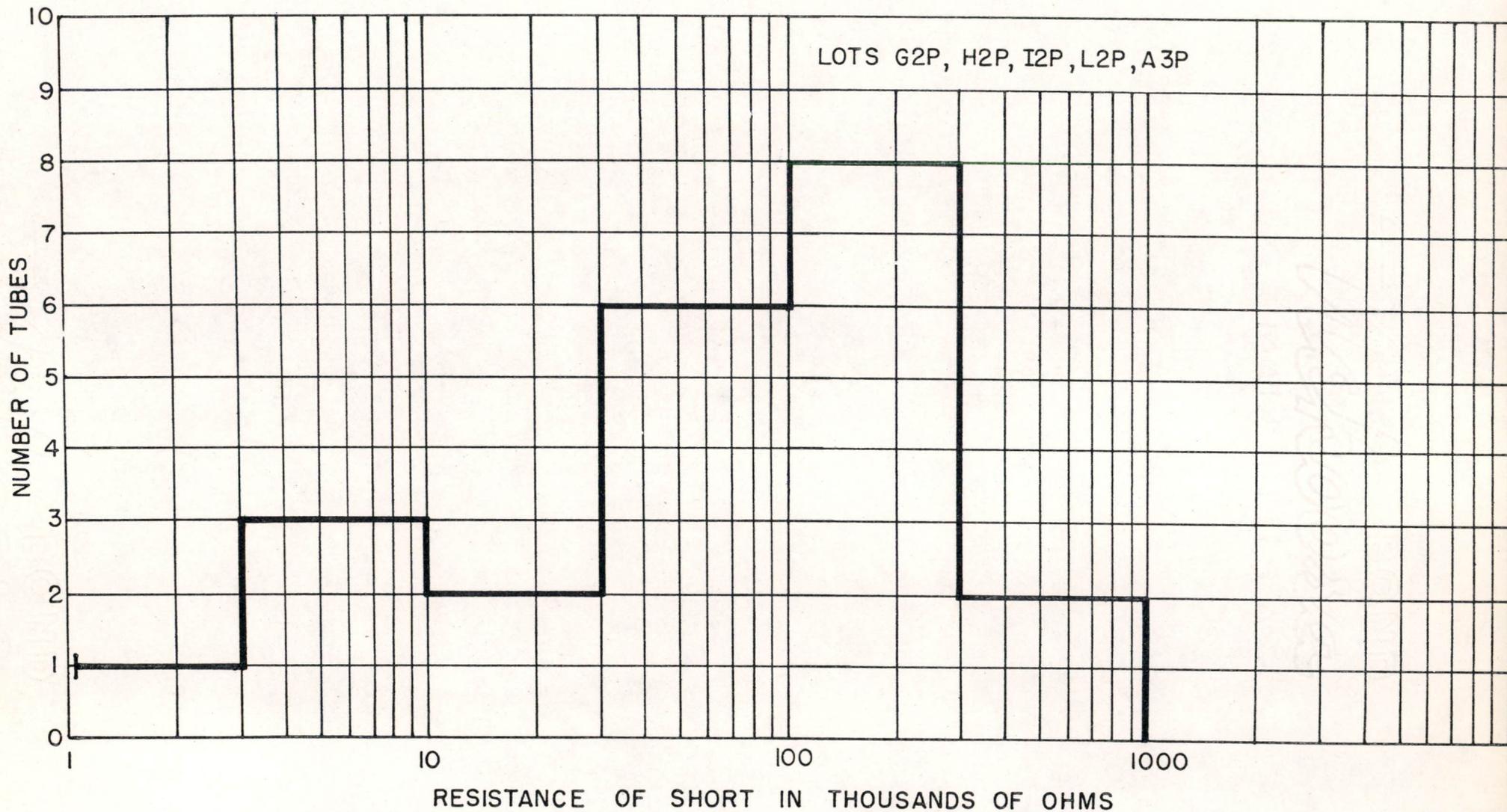


FIG. 5
DISTRIBUTION CURVE
6145 REJECTS - MINIMUM RESISTANCE OF LONGEST SHORT

A-48437

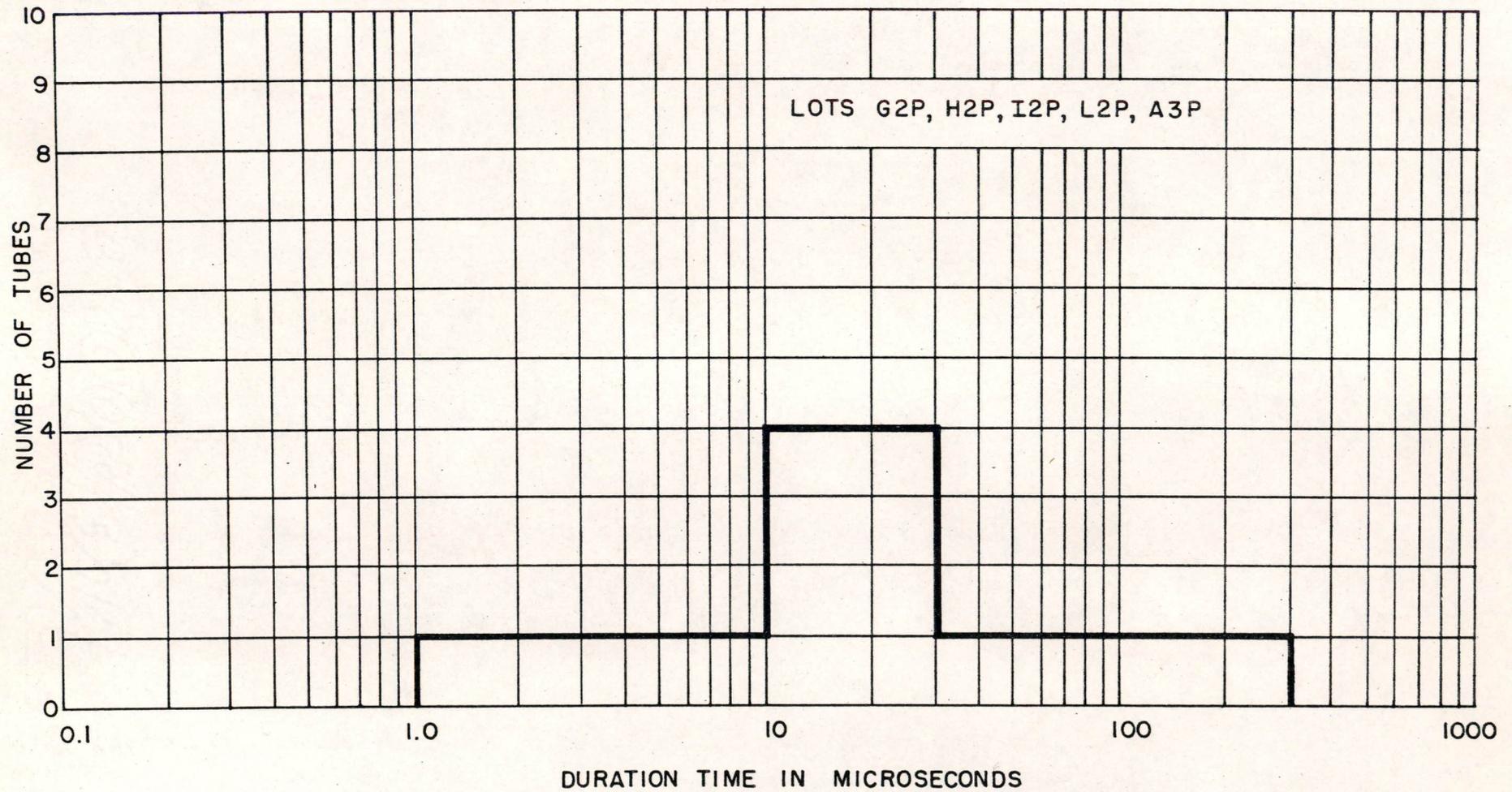
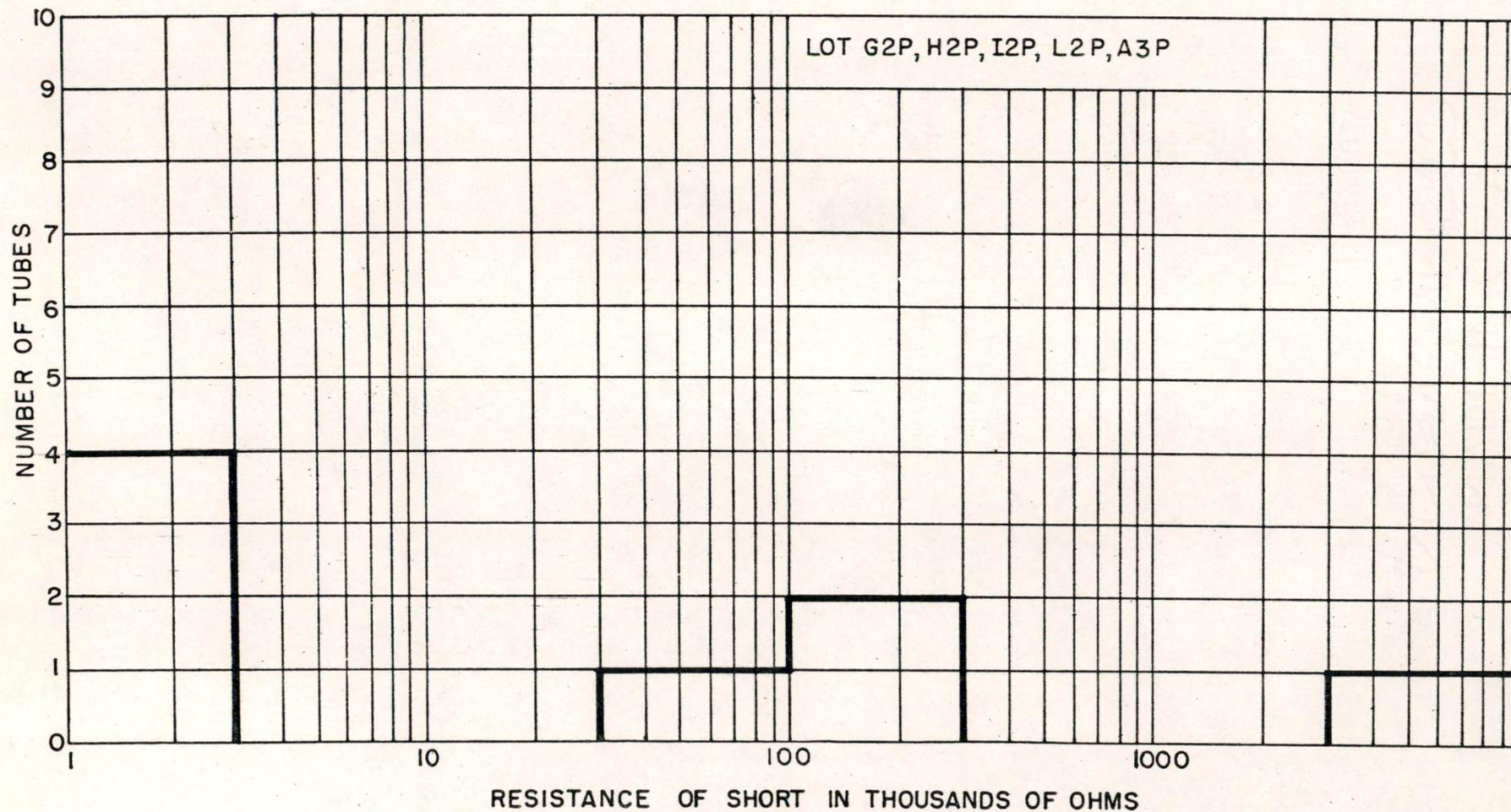


FIG. 6
DISTRIBUTION CURVE
6145 ACCEPTED TUBES - DURATION OF LONGEST SHORT

A-55433



DISTRIBUTION CURVE
6145 ACCEPTED TUBES - MINIMUM RESISTANCE OF LONGEST SHORT

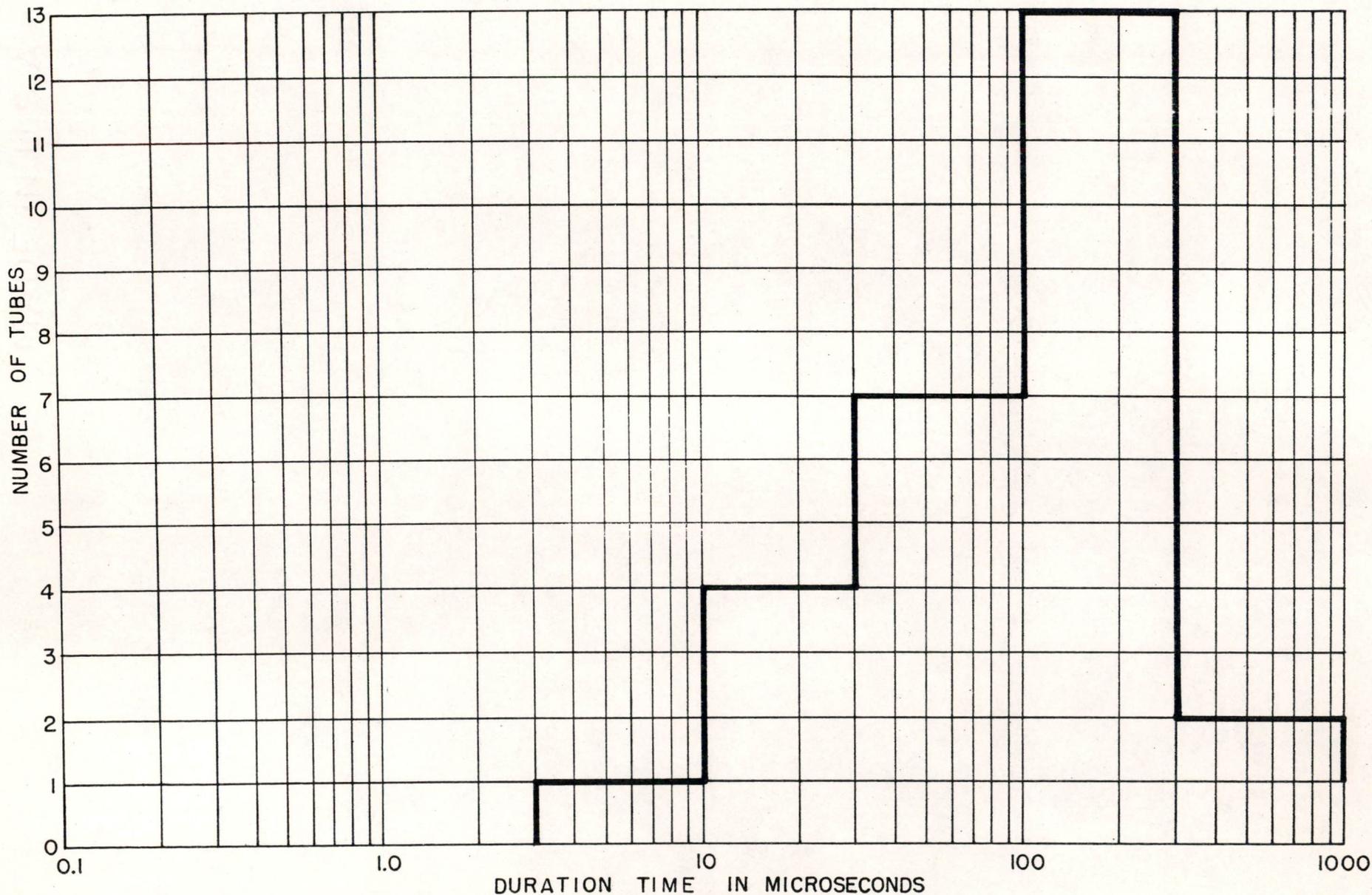


FIG.7 DISTRIBUTION CURVE
5965 REJECTS - DURATION OF LONGEST SHORT

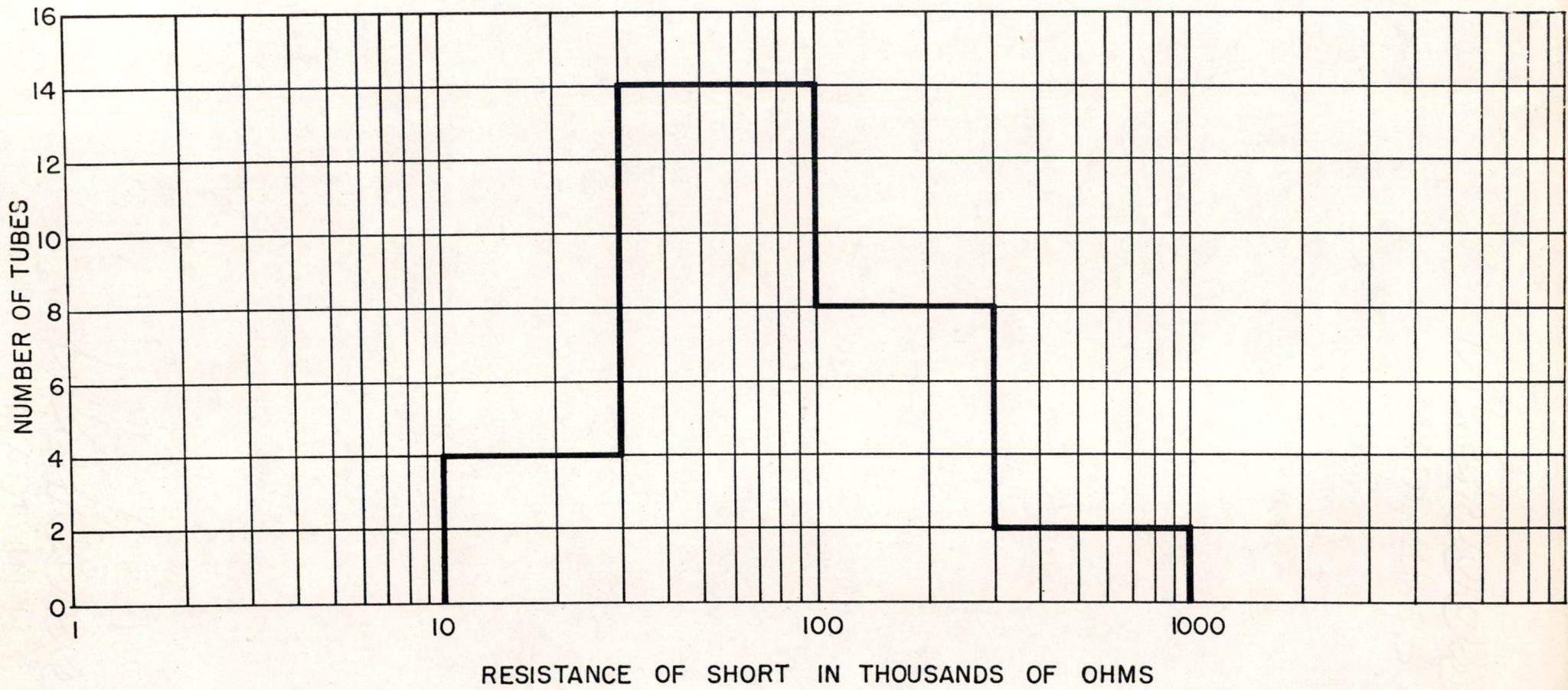


FIG. 8
DISTRIBUTION CURVE
5965 REJECTS - MINIMUM RESISTANCE OF LONGEST SHORT

file Falcorie

Division VI - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: SENSING WINDING GEOMETRY

To: N. H. Taylor

From: J. Raffel

Date: August 6, 1953

Abstract: The difference between the minimum wanted output (a system ONE) and the maximum unwanted output (a system ZERO) is the same for a winding which threads the cores so that each half of the memory plane has a different polarity as it is for one in which all the outputs add.

Introduction

This memorandum concerns itself with the analysis of the signal and noise in the present sensing winding and in a proposed winding, and will not consider other associated factors such as plane construction, sense amplifier design, etc.

Present Sensing Winding

When the first magnetic memory planes were being designed, before any detailed work had been done to determine the exact nature of the half-selected outputs which might appear in an array, the assumption was made that these voltages were approximately uniform and independent of the previous history of the core. This led quite naturally to a sensing winding geometry which tended to have the half-selected outputs cancel. This was accomplished by having the winding thread the cores in a diagonal fashion so that cores in two halves of the plane were threaded in opposite directions. The wiring scheme is shown in Figure 1. With this type of winding it turns out that all but two half-selected outputs are of canceling polarities.

Since the construction of these first planes a good deal of information has been obtained about the types of half-selected outputs which can appear on the sense winding. The original assumption of equal outputs from all half-selected cores is no longer justified. It is logical therefore to reconsider the problem of sensing winding geometry. The term "canceling" will be used to describe the present winding and "additive" will be used to describe that proposed which will thread the cores in such a way that all the outputs appear with the same polarity on the winding.

The following definitions will be used below:
(All definitions are for values at stroke time)

- h_1 the maximum output possible from a half-selected core.
 h_0 the minimum output possible from a half-selected core.
 s_1 the minimum output from a selected core containing a ONE.
 s_0 the maximum output from a selected core containing a ZERO.
 $ZERO_{max}$ the maximum sensing winding voltage when a core containing a ZERO is selected.
 ONE_{min} the minimum sensing winding voltage when a core containing a ONE is selected.
 $\delta = (h_1 - h_0)$
 $D = ONE_{min} - ZERO_{max}$

For an $n \times n$ memory containing n^2 cores the following results may be seen to hold:

Canceling

$$ONE_{min} = s_1 - 2h_1 - (n-2)\delta$$

$$ZERO_{max} = s_0 - 2h_2 + (n-2)\delta$$

$$D = s_1 - s_0 - 2(n-1)\delta$$

For additive

$$ONE_{min} = s_1 + 2(n-1)h_2$$

$$ZERO_{max} = s_0 + 2(n-1)h_1$$

$$D = s_1 - s_0 - 2(n-1)\delta$$

The difference between the minimum wanted output and the maximum unwanted output is the usable signal, D. Since this difference is seen to be the same for the two systems, it would seem that a re-evaluation of the canceling winding is needed to determine if it really buys anything, especially since plane construction and amplifier design are affected so strongly by the sensing winding geometry.

Signed: J. Raffel
J. Raffel

Approved: W. N. Papian
W. N. Papian

JR/rb

cc: Group 63 - Staff
A. P. Kromer - (IBM)
Magnetic Memory Section - Staff

Drawing: A-51628

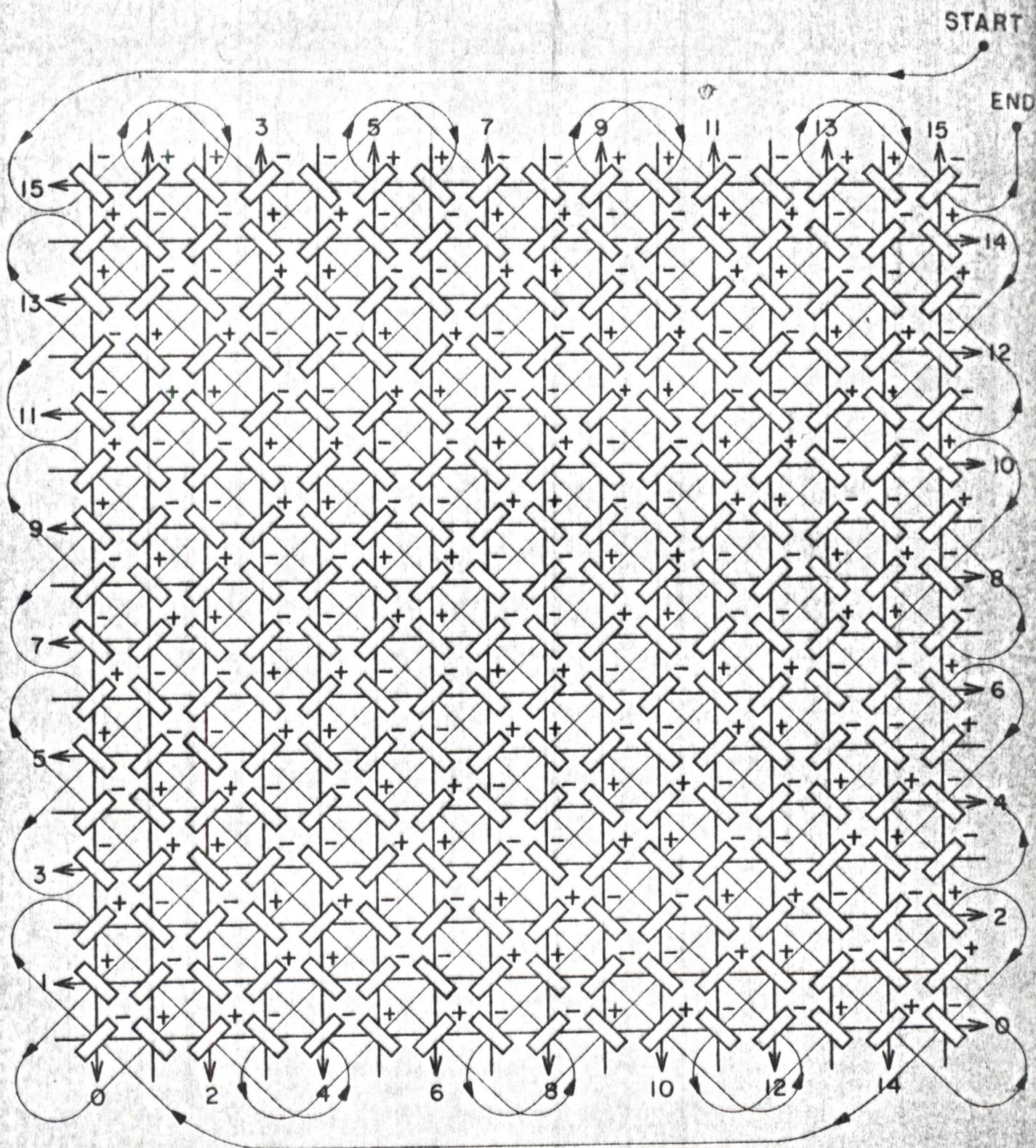


FIG. 1
WINDING GEOMETRY-CERAMIC ARRAY #1

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

APR 5 1962

SUBJECT: TESTING THE MAGNETIC-CORE MEMORY SYSTEM IN A COMPUTER

To: N. H. Taylor

From: B. Widrow

Date: September 18, 1953

Abstract: A working memory has a "safe" operating region in a multidimensional space whose coordinates consist of the significant operating parameters of the memory. Errors occur only with excursions of the operating point outside the safe volume; such excursions result from failure of the surrounding equipment to remain perfectly stable. The optimum operating point is determined by the nominal settings of all the parameters which permit operation with a minimum of errors. Reliability is then defined as the ratio of the number of memory cycles to the number of errors. This is, to a very close approximation, the reciprocal of the probability of the operating point to drift from its optimum setting into the region outside the safe volume.

The specific problems of finding an optimum point and evaluating the reliability of the 32 x 32 MTC memory have been facilitated by reduction of the number of significant variables to two: the driving current and the common bias of the sensing gate tubes. Optimum conditions were 475-ma X, Y, and Z driving currents ($1/2 I_m$) and -30-v gate-tube bias. Since the probability distributions of the variables are not known, reliability can only be evaluated by optimizing the adjustments of the system and maintaining count of its errors.

I. General Problem

A system affected by n parameters will in general operate as long as these variables are set to correspond to some point within a "safe" volume in an n -dimension space whose coordinates are these parameters. If the system is a computer memory, the shape of the operable volume in the n -dimension space will depend upon the computer's program. This volume will henceforth be called a "shmoo."

Memory-test programs are usually cyclic and do not work on "live" incoming data. This type of program always "does the same thing" to the memory. A practical program dealing with input data that may be

continuously changing is, from the memory's point of view, like a very large number of programs. The word program will now be considered from the memory's point of view, so that it refers to a given information pattern stored and acted upon at certain PRF's.

The surface of a shmoo for a given program may be obtained by varying a parameter between the lower and upper bounds over which operation is possible, while the other variables are fixed. This is repeated for many values of the "fixed" variables. Then a new parameter is picked as the one to be varied over operation limits, and the process is repeated.

Two shmoos corresponding to two programs will most probably overlap in the n-dimension space and share a common volume. If a volume exists that is common not only to two shmoos but to every possible shmoo, then the memory is a working memory. Operation within the common volume is error free. Errors occur only upon transient excursions of the operating point outside the common volume; such excursions result from failure of the surrounding equipment to remain perfectly stable.

Let us define the nominal optimum operating point as that point in the n-dimension space at which, for the given surrounding equipment, a minimum number of errors occur on a long-term basis (allowing many programs to be worked). The problem is to find this point and, at this point, to determine the reliability of the memory. The stability of the surrounding equipment and the tolerances of the memory itself are both involved in this problem.

A. Experimental variables

If the memory operation is a function of only two variables, a two-dimensional shmoo may be simply obtained for a given program. If operation depends upon 3 variables and data is taken for 5 points of each variable, 5 two-dimensional shmoos are needed. If, on the other hand, operation depends upon n variables and each is varied over 5 points, $5^{(n-2)}$ two-dimensional shmoos are needed to specify the operating space for each program.

Among the variables affecting the 32 x 32 MTC memory are the X and Y read-and-write driving-current magnitudes (128 of them); digit-plane driving-current magnitudes (17 of them); rise time and pulse duration of these currents; strobe time; sensing-amplifier gains (17 of them); sensing-gate-tube bias; and temperature. Hence the total number of variables lies between 10 and 170 depending upon how one weighs and counts. At any rate, $5^{(n-2)}$ experiments per program for an almost infinite number of programs is staggering.

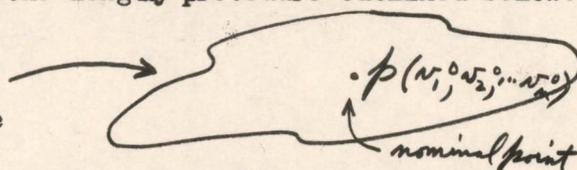
B. Optimum settings and reliability

Assume for a while that the information concerning these variables is available. How can it be used to determine an optimum operating point in multidimensional space and to allow the calculation of

a figure of reliability?

It will be assumed that the number of errors made on a long-term average basis will be proportional to the number of excursions of the operating point outside the common volume. This assumption, that errors are just as likely to occur as a result of crossing the safe surface at one point as at any other, must be made in the absence of specific prior knowledge of the programs (and their respective shmoos) to be handled by the computer. Each parameter may be described statistically in terms of a probability distribution that peaks at the nominal setting. For given settings of the n parameters, the probability of the operating point being at a given point in the n-dimensional space is the product of the n distribution amplitudes. This over-all probability function, a scalar field, is the joint probability of the n independent parameters. The problem of finding an optimum point is one of maximizing the probability that the operating point will be within the safe volume. The surface of the safe volume may be approximated by some equation while the distributions of the parameters may be approximated by analytic functions. The maximizing done on a formal basis will only require differential calculus, but will involve the lengthy procedure outlined below.

"safe" n-dimensional volume
in space whose coordinates
are the independent variable



$P(v_1 - v_1^0) P(v_2 - v_2^0) \dots P(v_n - v_n^0)$ is the probability of the operating point being at any point $p(v_1, v_2, \dots, v_n)$ when the variables are nominally set at $v_1^0, v_2^0, \dots, v_n^0$.

The probability of being within the safe volume is:

$$P \equiv \int \dots \int P(v_1 - v_1^0) P(v_2 - v_2^0) \dots P(v_n - v_n^0) dv_1 dv_2 \dots dv_n$$

P is only a function of $v_1^0, v_2^0, \dots, v_n^0$ and is to be maximized. The optimum point is now found from the simultaneous equations:

$$\frac{\partial P}{\partial v_1} = 0 \quad ; \quad \frac{\partial P}{\partial v_2} = 0 \quad ; \quad \dots \quad ; \quad \frac{\partial P}{\partial v_n} = 0$$

A more practical and no less precise procedure is that of trial and error. Here again knowledge of the n-dimension shmoos and of the statistics of the parameters is necessary. How a trial and error process may be instrumented in the absence of such precise knowledge will be considered below.

II. An Engineering Answer for the 32 x 32 MTC Memory

A. Finding optimum point

1. Reduction of number of variables.

To make the first important reduction, let all the driving currents be identical in magnitude ($1/2 I_m$) and let this magnitude

be a single variable. The X and Y currents should be identical by symmetry, and a limited amount of experimental data shows that the Z current magnitudes are best when they are the same as for X and Y. This is not sufficient, however, to justify the lumping of all currents into a single variable. It is necessary in addition to show that all the currents simultaneously undergo the same transient excursions from the nominal $1/2 I_m$. The X and Y currents would exhibit this as a result of power supply transients. However, the Z driver circuits are not the same as the X and Y circuits and so would not experience the same transients. Also, variations may exist among the Z driver units and among the X and Y driver outputs due to driving-tube differences. Actually the currents do not behave as a single variable. Although the biggest strain on the memory comes from read-and-write driver currents wandering in opposite directions, the circuitry is such that this possibility is remote; the next biggest strain comes from all drivers drifting in the same direction. Assuming a single driving-current magnitude thus leads to an approach that is nearly the most conservative.

The memory performance varies considerably with temperature. This will not be considered as a variable, however, because it is fixed by the temperature of the air-conditioned memory space.

The 17 sensing-amplifier gains will not be considered as experimental variables. They are not quantities that could fluctuate rapidly; their sensitivity to power-supply fluctuation gives only second-order gain variations. These gains are subject to long-term variation, however, but this would doubtless be eliminated by system tune-up at sufficiently close time intervals. If shmooos are taken and the gain (all 17 identical) noted, the shmoo that will result from a different gain can be simply calculated from the first shmoo if one knows the gate-tube threshold. It follows at any rate that complete information is obtainable from data taken at fixed gain settings.

Operation of the memory depends upon current-gate durations only when these gate widths are less than the time necessary to switch the memory cores. The read-and-write gate durations may be eliminated as variables if they are made sufficiently long.

As long as the current gates are of sufficient durations, rise time on write is not important. Experiment shows also that varying the read rise time between 0.5 and 1 μ sec has no effect upon margins. Hence it is no longer necessary to consider rise time as a variable.

2. Observe properties of remaining variables.

There are three remaining variables: driving-current magnitude, strobe time, and gate-tube bias. The significance of the single driving-current magnitude has already been discussed. Next to be considered are the special characteristics of strobe time.

All times are measured with respect to some start pulse which initiates the read gate into the read switch. The time of

strobing is fixed relative to this pulse by delay-line amplifiers. The strobe time could be pin-pointed if it were not for the fact that, for the particular driving circuits used, the time after the start pulse when the X and Y read currents begin flowing in the selected memory lines depends fairly critically on power-supply voltages. The strobe time turned out to be a significant variable whose value hardly needed to be changed over wide variations of the other variables. For each driving-current magnitude of an experimental run, the strobe time was adjusted to give maximum bias limits. This procedure lead to the result that the strobe time needed only to be increased by $0.05 \mu\text{sec}$ as the driving currents were lowered from 500 ma to 350 ma. The strobe time was set at $1.20 \mu\text{sec}$ with read current - rise times at $0.5 \mu\text{sec}$ thereafter.

The gate-tube bias is the last remaining variable. Gate-tube bias limits give a measure of the size of the smallest ONES and the largest ZEROS. The differences between these limits, very significant quantities, are the differences between the ONES and ZEROS outputs and are proportional to sense-amplifier gain.

3. Two-dimensional reduction.

Now the problem of finding the optimum operating point is two dimensional. For a given program, let the bias limits be plotted against driving-current magnitude where the strobe time has been optimized. This gives a single two-dimensional shmoo per program (See Fig. 1). When a sufficient number of shmoo's have been taken for the various programs, the overlap region may be found, as shown in Fig. 2.

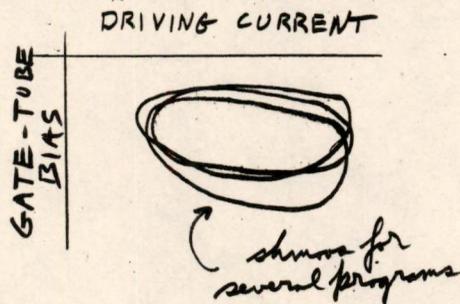


Fig. 1

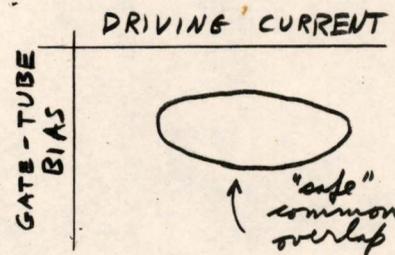


Fig. 2

The two-dimensional safe-overlap region together with the characteristics of the driving currents and gate-tube bias are sufficient to determine the optimum point. The gate-tube-bias probability distribution should not only include the variations in the bias potential applied to the gate tubes but also should take account of any stray noises appearing on the outputs of the sensing amplifiers that are generated within the sensing amplifiers. These distributions may be measured but not very simply. They may best be estimated and at the same time the optimum point should be selected. The decision as to where to operate for a minimum of errors is not difficult in two dimensions and can be made with as close an accuracy as the shmoo's can be measured in the first place.

B. Reliability

Reliability may be conveniently defined as the number of operations divided by the number of errors. This is a statistical measure — a long-term average. Reliability is then the ratio of the probability of the operating point being inside the safe volume to the probability of the point being outside the safe volume. This is very nearly the reciprocal of the probability of being outside the safe volume.

In a reliable system such as a magnetic-core memory, it may be assumed that appreciable simultaneous excursions of two or more variables from their nominal settings is a very much rarer situation than that of a single variable deviating from nominal. Therefore, not much conservatism will be lost if it is assumed that excursions of the variables are mutually exclusive events. From the optimum point, each of the parameters may be varied separately over finite ranges before the system fails. The error probability is then the sum of the probabilities of each variable being outside its safe range. The reciprocal of this sum is the reliability. These probabilities are difficult to obtain, but a feeling for the system reliability may be achieved from knowledge of the allowable ranges of the variables at the optimum point. These ranges at least give a basis for critical comparison of various magnetic-memory systems and of the merits of the various adjustments of a given system.

III. Experimental Determination for the 32 x 32 Memory in MTC

The procedures described above will be illustrated for the 32 x 32 magnetic-memory installation in the Memory Test Computer.

Fig. 3 shows two shmoo's taken on the MTC memory-test programs MP11 and MP28-2 (the "inchworm"). MP11 places all ONES or all ZEROS in a memory plane and operates on the memory at a low PRF. Most of the computer time is spent in toggle-switch storage and the arithmetic element. This program placed less strain on the memory system than the high-speed program MP28-2 which had about the poorest margins of all those tried. The safe overlap region for the 32 x 32 memory in MTC was roughly the shape of the shmoo of MP28-2. The placing of the optimum point was easy here because the tolerable ranges of both current and bias were maximum and balanced at the same point. For this special case, no knowledge of the variations in current and bias was necessary because the best operating point biaswise also turned out to be the best operating point currentwise.

At the optimum operating point, if each variable is allowed to change while the others are fixed, the reliability of the memory alone is indicated by the following tolerances:

Driving currents	±15% at 475 milliamperes	} 85 F
Gate-tube bias	±30% at -30 volts	
Strobe time	±15% (+0.2 μsec) at 1.20 μsec	
Read-rise time	Noncritical 0.5 - 1.0 μsec	

As yet, the probability distributions of these variables have not been measured. Monitoring these variables for deviations may give information leading to equipment changes with subsequent improvement in reliability. The reliability may only be measured at present by keeping count of errors made over known numbers of memory cycles.

Only observations of the existing system have been considered thus far. Some recommendations may be made now for improving the 32 x 32 MTC memory installation. The time when the X and Y driving currents begin flowing in the memory lines after the initial cycle start pulse depends fairly critically upon the -300-v supply. Reducing this sensitivity will improve reliability. It is believed that the margins on all programs could be made as good, if not better, than those of MPL1 by improving the filtering and shielding in the sensing circuits and making changes in the sensing amplifiers to reduce PRF sensitivities. Photographs of voltage waveforms on the sensing windings show that the sizes of ONES and ZEROS changed negligibly with program. Delta noise is not a serious problem here, and hence operating margins should not be greatly affected by the nature of the program.

A considerable amount of experimental work was done by R. L. West and F. R. Durgin of IBM. Their results are given in the IBM report "An Experimental Evaluation of the MTC Memory System" and justify many of the simplifications made here in arriving at a practical solution to the memory-adjustment and evaluation problem.

Signed: Bernard Widrow
B. Widrow

Approved: W.N. Papian
W.N. Papian

BW/rb

CC: Group 63 Leader & Section Chiefs
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Magnetic Memory Section
MTC Section
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N. Daggett
Wm. Linvill
R.R. Everett

SA-48466-G

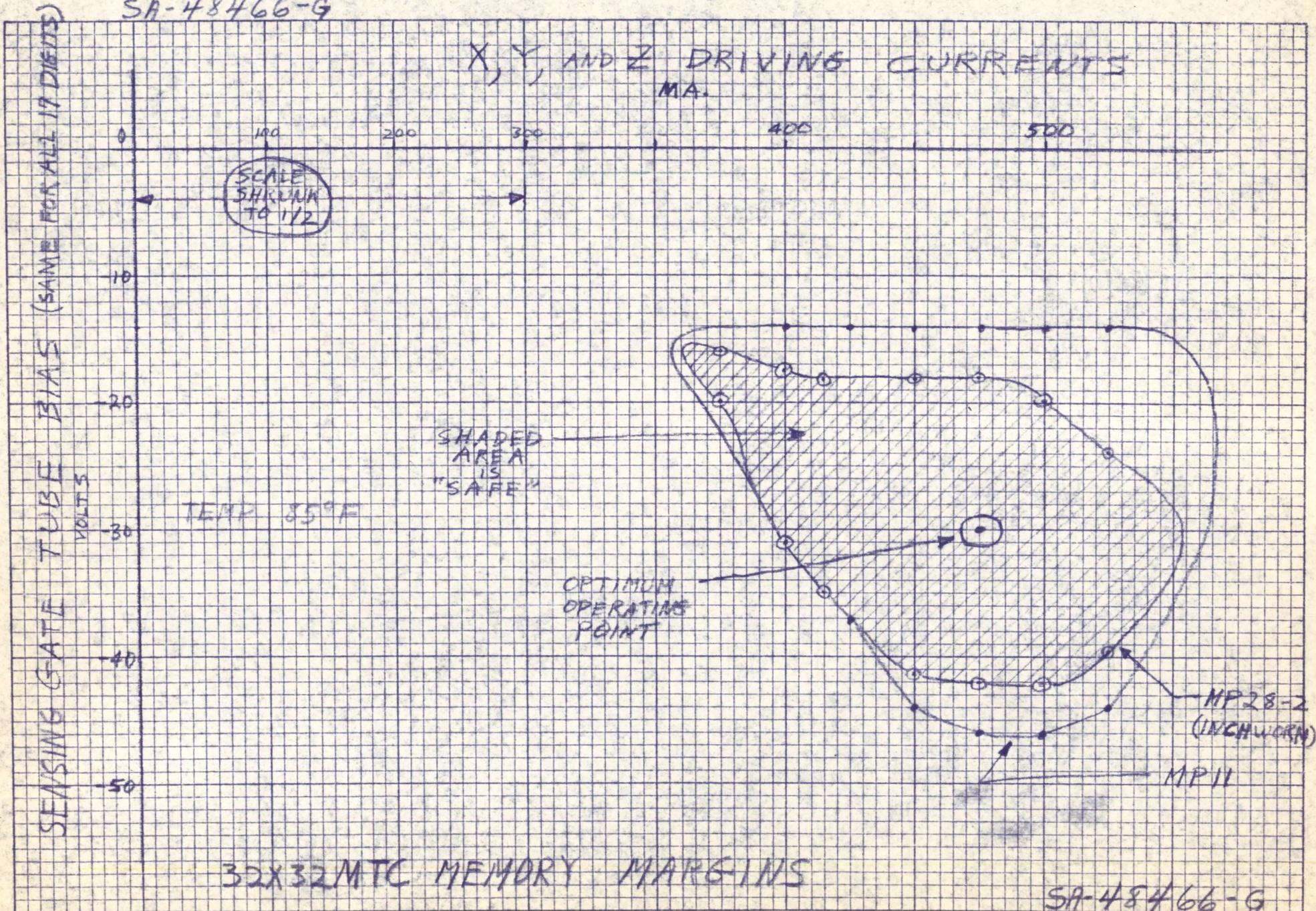


FIGURE 3

Olsen

Memorandum M-2408

Page 1 of 3

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: CLAMPED LOW-SPEED FLIP-FLOP FOR XD-1

To: N. H. Taylor

From: H. W. Boyd

Date: September 15, 1953

Abstract: This M-note is intended to describe, by the presentation of characteristic curves and marginal checking curves, the operating characteristics of the clamped low-speed flip-flop. This flip-flop, possesses those characteristics which should allow its use as an all-purpose low-speed flip-flop for XD-1.

1.0 General Characteristics and Applications

This flip-flop was designed to drive 2 ma of "AND" and "OR" current, and extremely large capacitive loads. As are all circuits for XD-1, this unit is capable of operating within specifications with 50k back resistance diodes and 65% unbalanced tubes (+25, -40%).

As the total rise time (delay + rise time) is larger than the total fall time, it is the determining factor in the flip-flop's total transition time. The total rise time R_t (including a constant 0.1 μ second delay) can be calculated for any capacitive load by

$$R_t = 1.0 + \frac{C \text{ load } (\mu\text{f})}{80\mu\text{f}} \mu\text{sec.}$$

This assumes 50k diodes.

The maximum capacitive unbalanced load that can be reliably driven is 320 pf (μf) on either or both outputs.

The input is specified by:

pulse width	0.8 to 0.12 μ sec.
amplitude	20 to 40 volts
polarity	positive (or negative by reversing input xformer and mixing diodes)

The only limit on the magnitude of a negative overshoot at the input is that of the input diodes back-voltage. The maximum allowable positive overshoot is 10 volts during that 0.3 μ sec immediately following the trigger. The maximum allowable noise at the input is 5 volts (positive). When driving gate-tubes that are to be sensed by 0.1 μ sec pulses, favorable gate-tube transfer characteristics* can be obtained by padding the flip-flop output to 160pf for each gate-tube to be sensed at any one time. The padding consisting of gate-tubes and/or additional capacitance. The flip-flop has inherent delays suitable for counting.

When driving gate-tubes that are to be sensed by larger pulses (around 1.0 μ sec.), each gate-tube thus sensed should contain a 4.7k isolating resistor at the suppressor grid. When the number of such gates approaches around 4 the suppressor resistance may be neglected and only the total capacitance considered in computing rise time.

2.0 PRF Response

Figure 1 and 2 show the prf response characteristics of the flip-flop. Figure 1 shows the effect of varying pulse width and prf, under the most adverse conditions. These being complementing the flip-flop at a continuous pulse repetition frequency. Figure 2, taken with 0.1 μ sec. pulse widths, shows the effect of capacitive load on the input prf response.

3.0 Output Waveform

Figure 3, "Output Waveform Characteristics," was taken with a 40 volt 0.12 μ sec. input. In this figure are plotted the variations in total rise, total fall, upper delay, and lower delay times with variable balanced capacitive load up to 320 μ fds per side. The rise time curve is extended to 10,000 μ fds in Figure 4. Also in Figure 3 is plotted the total rise time curve obtained with the most critical diode at a 50k back resistance.

4.0 Maximum Safe-Loading

Figure 4 indicates the maximum loads that the flip-flop can drive. The flip-flop can drive an infinite capacitance on one side, but a maximum capacitance of 3500 pf on both sides. These marginal checking curves were taken at an input of 30 volts. The maximum safe load of the flip-flop, allowing about a 25% reduction in margins, and hence tolerances, is 320 pf on one side, 640 pf total.

5.0 Reliable Input-range and Loading

Figures 5 and 6 allow an approximate determination of the reliable input trigger ranges and allowable reduction in margins caused by loading.

Figure 5 shows how margins are affected by the input trigger amplitude, while Figure 6 shows how the most critical component's tolerances vary with trigger input. Both curves suggest a linear relationship between margins and tolerance. Note that at an input of 20 volts the most critical

* The same as with the High-Speed Flip-Flop in counting applications.

component has a nominal, no-load tolerance of about 17%. A full-load reduction in margins of about 25% should yield a minimum tolerance of about 12%, a not too severe reduction.

6.0 Gate-tube Transfer Characteristics (0.1 μ sec.)

The gate tube transfer characteristics of a 0.1 μ sec. gate-tube when driven by the Low-Speed Flip-Flop are the same as when driven by the High-Speed Flip-Flop in a counting application. (Low-speed flip-flop output padded to 160 pf.) The low-speed flip-flop delayed sensing characteristics are identical to its coincident sensing (counting) characteristics.

7.0 Tolerances and Marginal Checking

Figure 7 is a plot of the variations in critical voltages with unbalanced low I_b tube sides. The critical voltages are the "on" tube's grid voltage, E_{g1} , the "off" tube's grid voltage, E_{g2} ; the cathode voltage, E_k , and the lower output voltage level, E_o' . One tube side was held at 25% above bogie I_b while the other was varied below bogie. The below bogie tubes were not simulated, but were actual low I_b 5965's. A plot of the variations in margins vs. low unbalanced tubes is shown in Figure 8.

The rest of the marginal checking curves, Figure 9 thru 11, are self-explanatory. However, I might add that OS on the curves means marginal checking on the opposite side of the flip-flop from which the component is located, while SS is for the same side.

Signed: _____

H. W. Boyd

Approved: _____

R. L. Best, Section Leader

Approved: _____

N. H. Taylor, Group Leader

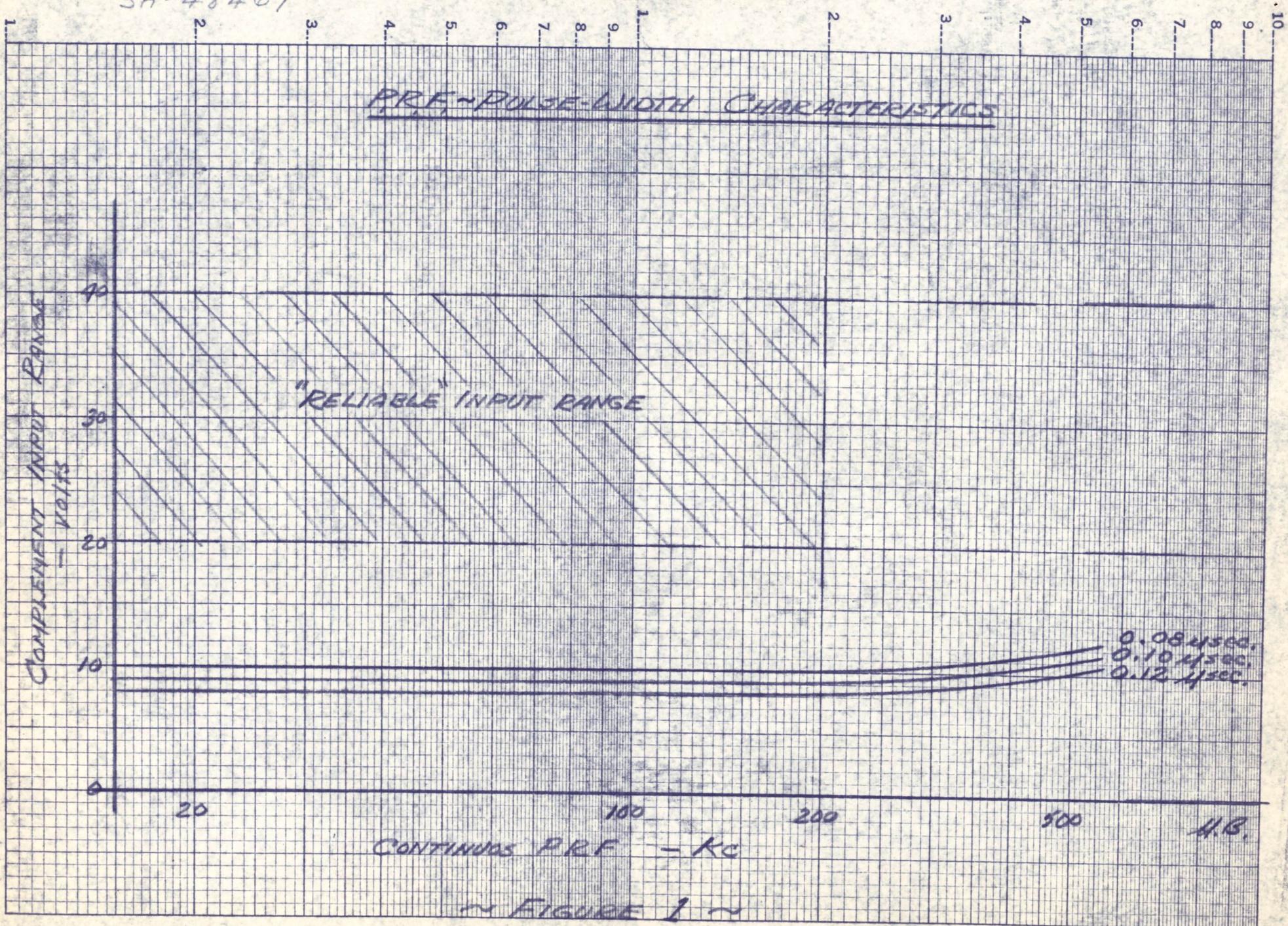
HWB/rb

cc: Basic Circuits
 D.J. Crawford (IBM)
 D. Dossin "
 N. Jackman "
 R. Neinburg "
 R. Randles "
 J. Sanders "

Drawings attached:

SA-56282
 SA-48467 thru 48477 (Fig.1 - 11)

SA-48467

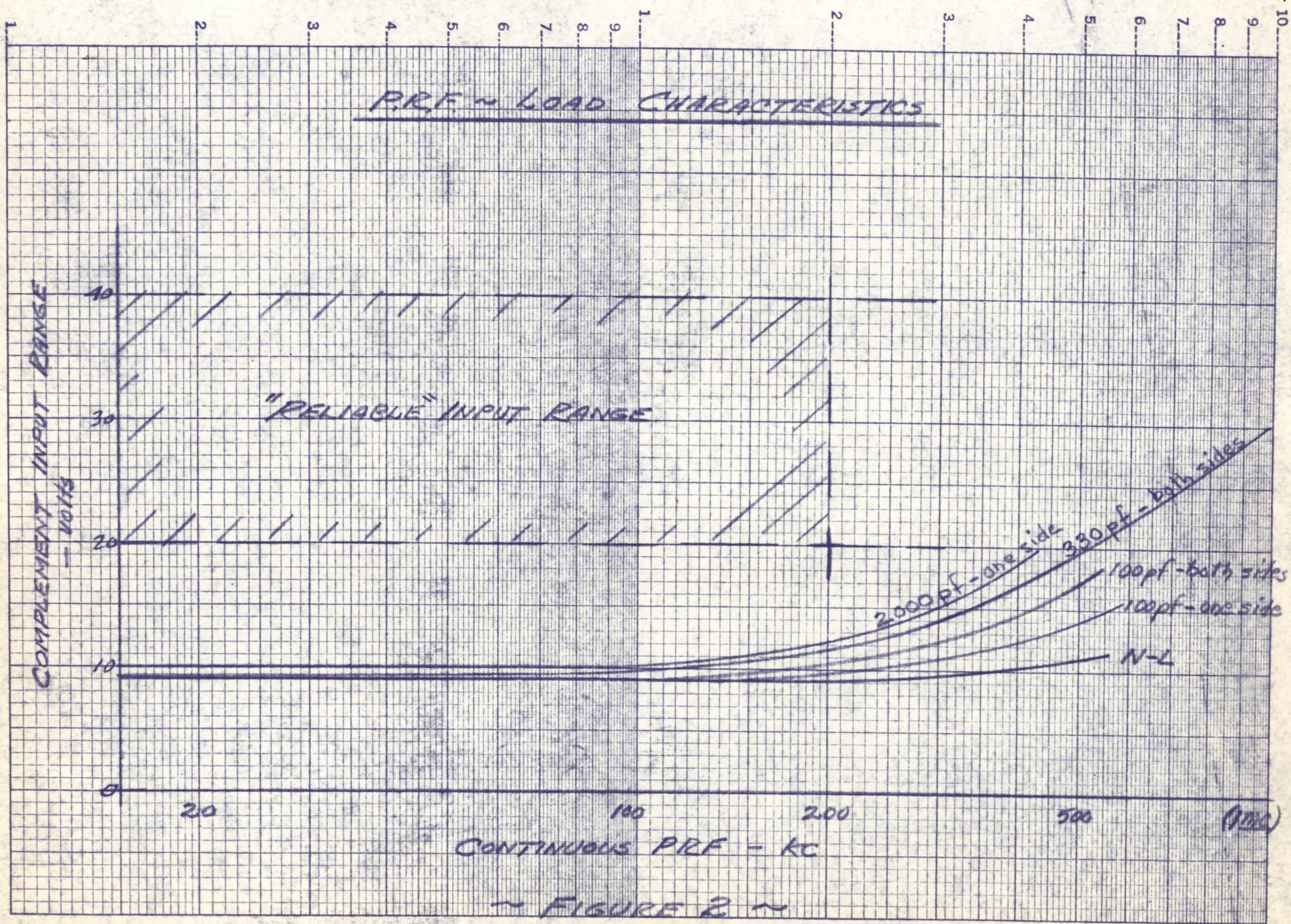


CONTINUOUS PRF - Kc

~ FIGURE 1 ~

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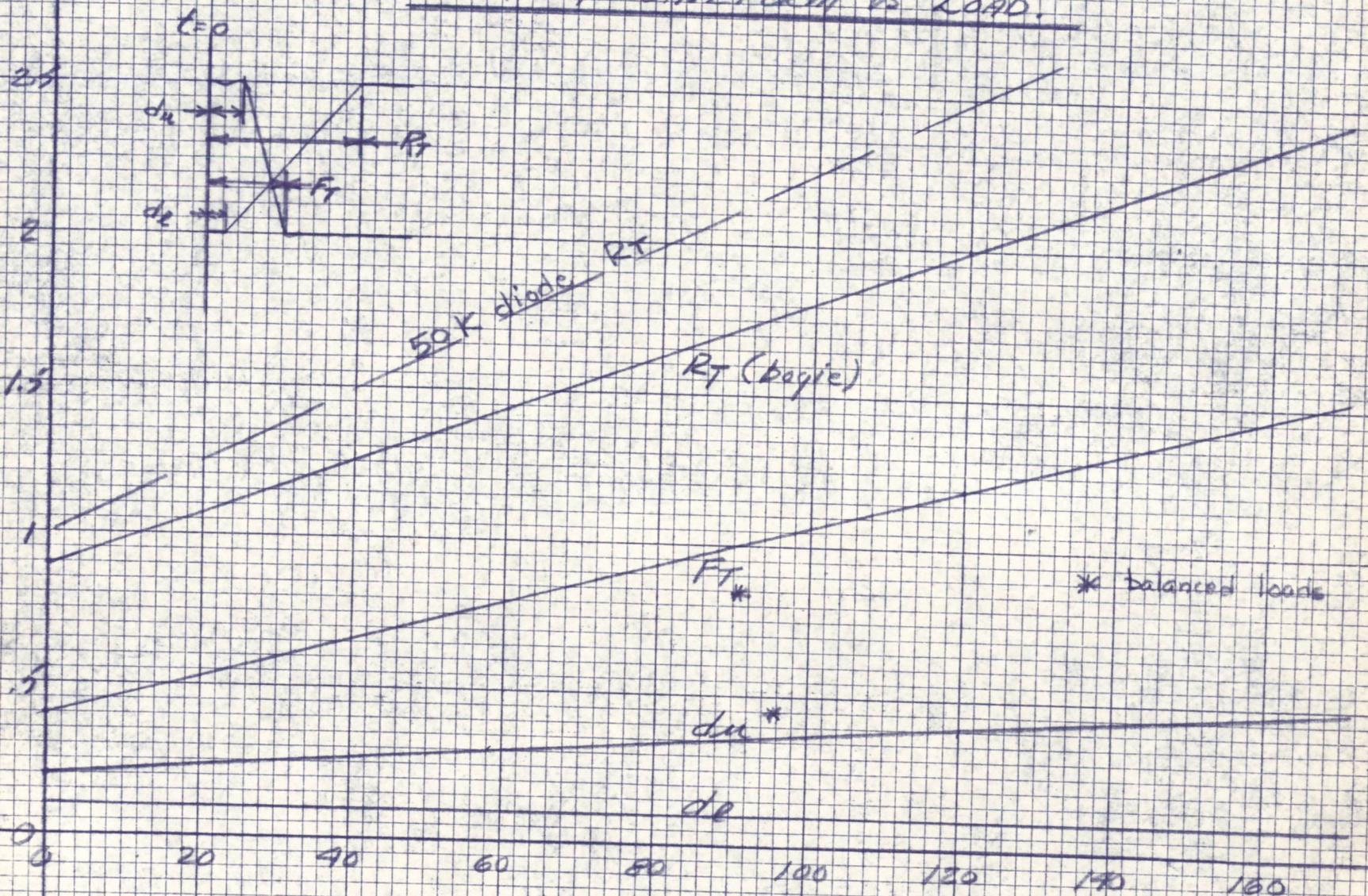
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SA-48468

OUTPUT WAVEFORM VS LOAD.

WAVEFORM TIME SCALE = 4 sec.

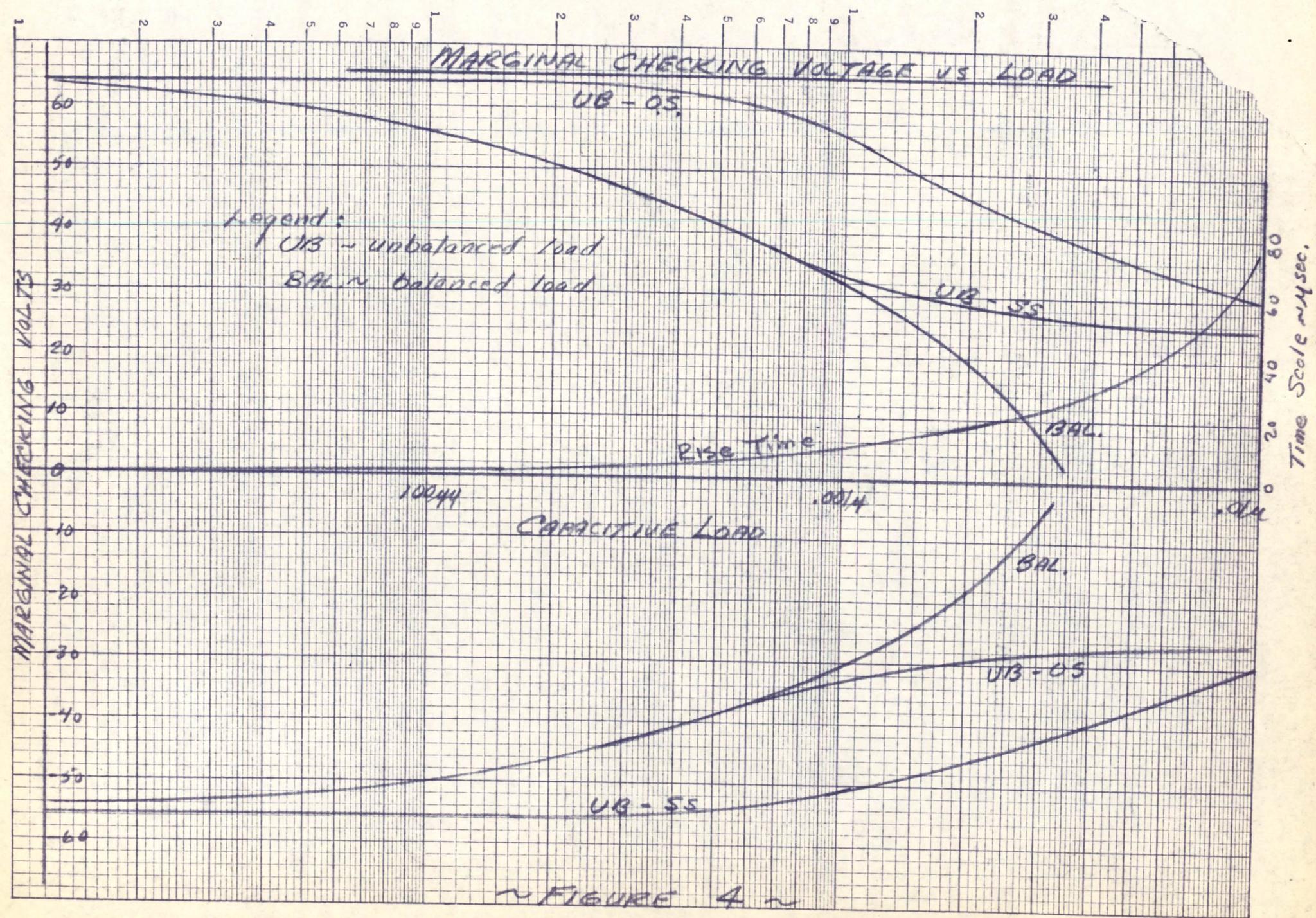


CAPACITIVE LOAD - 44 f/s

~ FIGURE 3 ~

A-48470

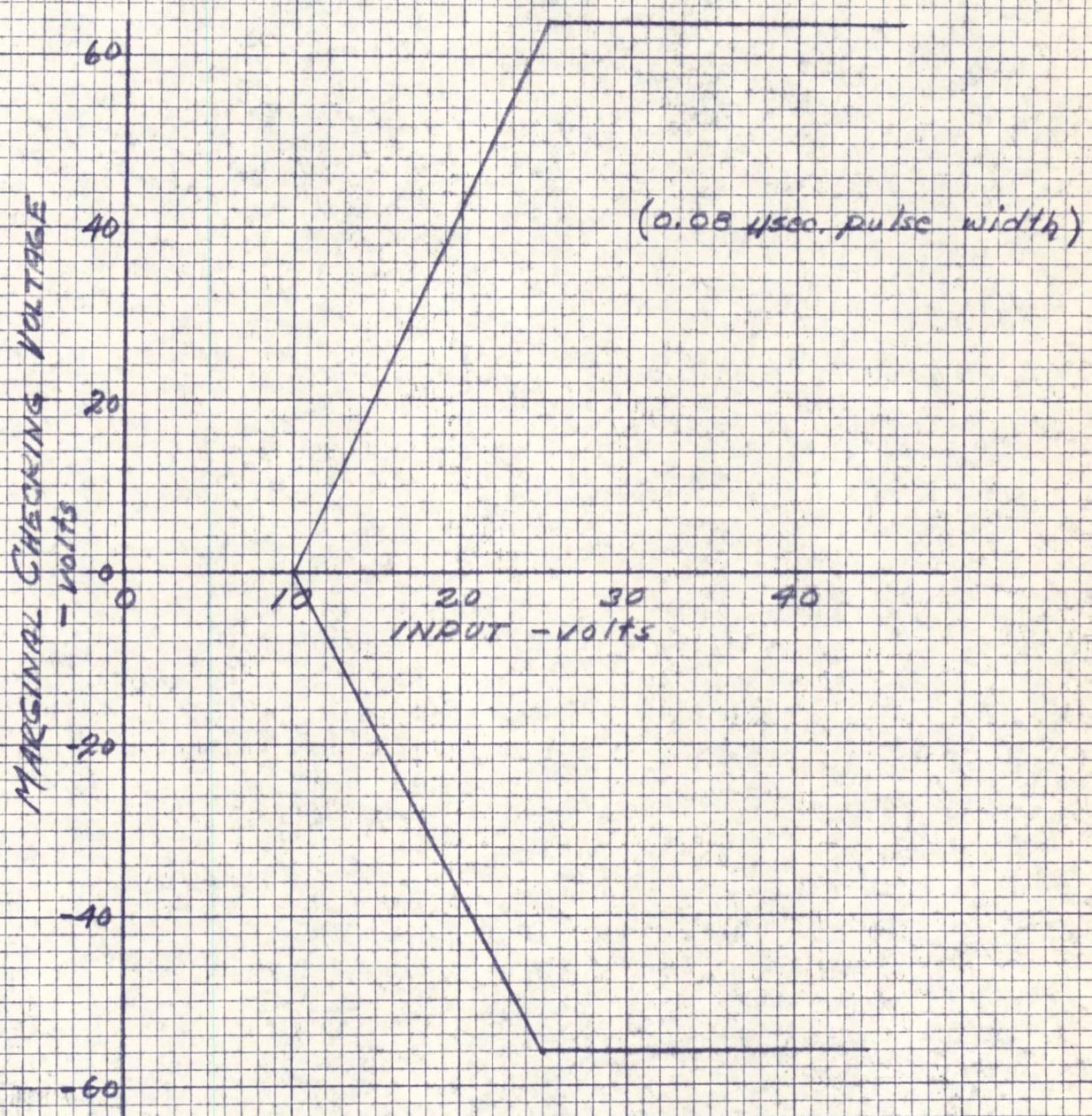
359-71G KEUFFEL & ESSER CO.
Semi-Logarithmic, 3 Cycles X 10 to the inch,
5th lines accented.
MADE IN U.S.A.



~ FIGURE 4 ~

SA-48471 ✓

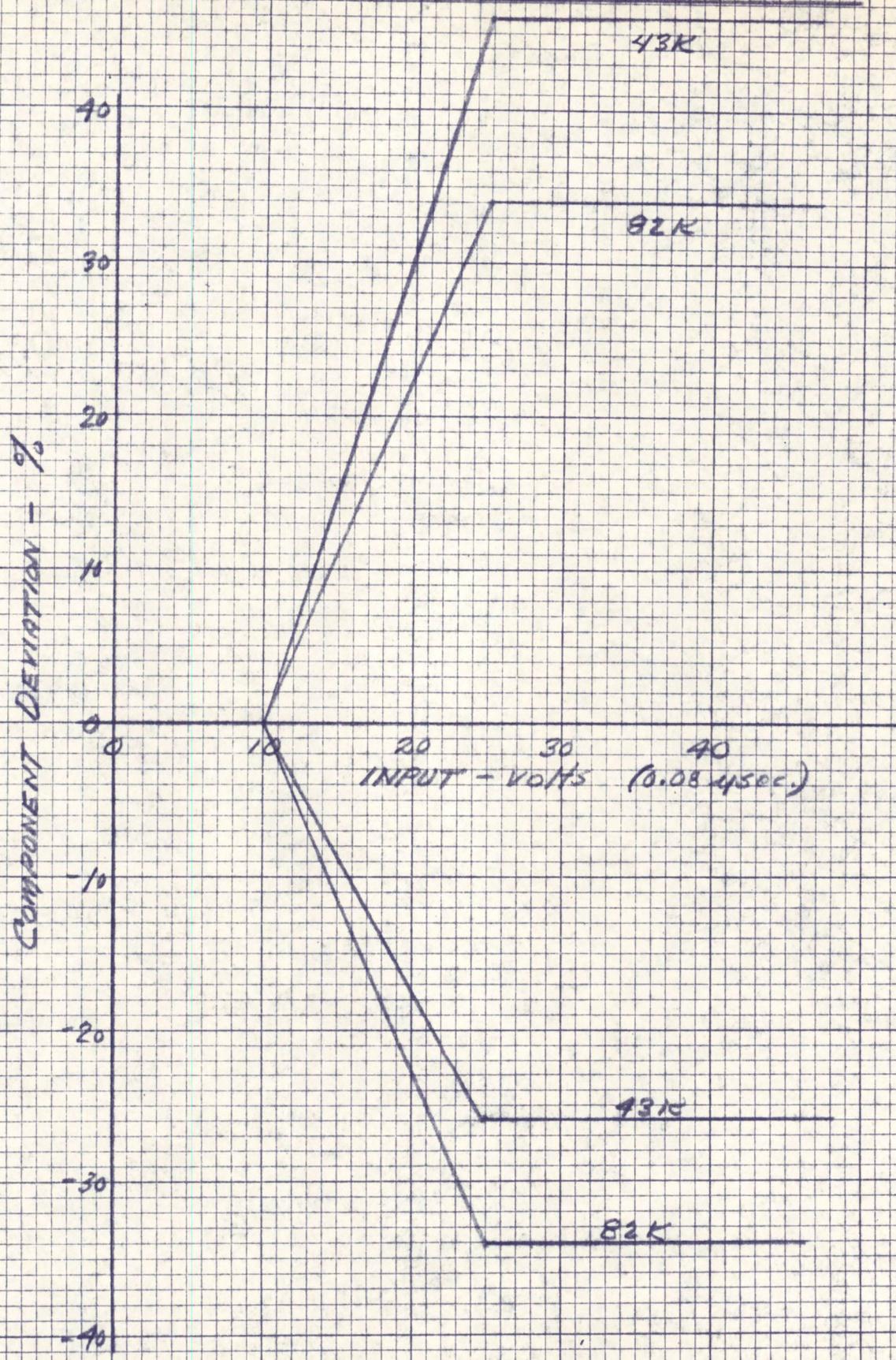
MARGINAL CHECK VS. INPUT



~ FIGURE 5 ~

SA-48471

DIVIDER TOLERANCES VS INPUT



INPUT - VOLTS (0.0845sec.)

~ FIGURE 6 ~

359-5C KEUFFEL & ESSER CO.
10 X 10 to the inch.
MADE IN U. S. A.

SA-48472

SA-48472

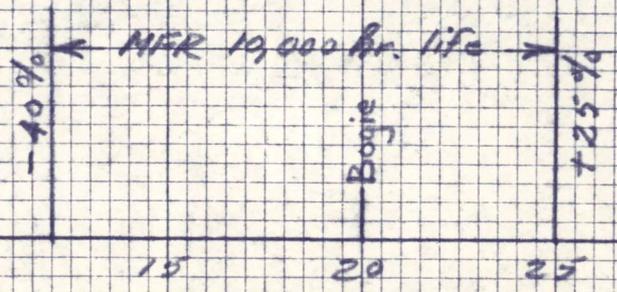
SA-48473

359-5G KEUFFEL & ESSER CO.
10 x 10 to the inch.
MADE IN U.S.A.

LOW I_b TUBE CHARACTERISTICS

VOLTAGE SCALE - VOLTS

100
80
60
40
20
0

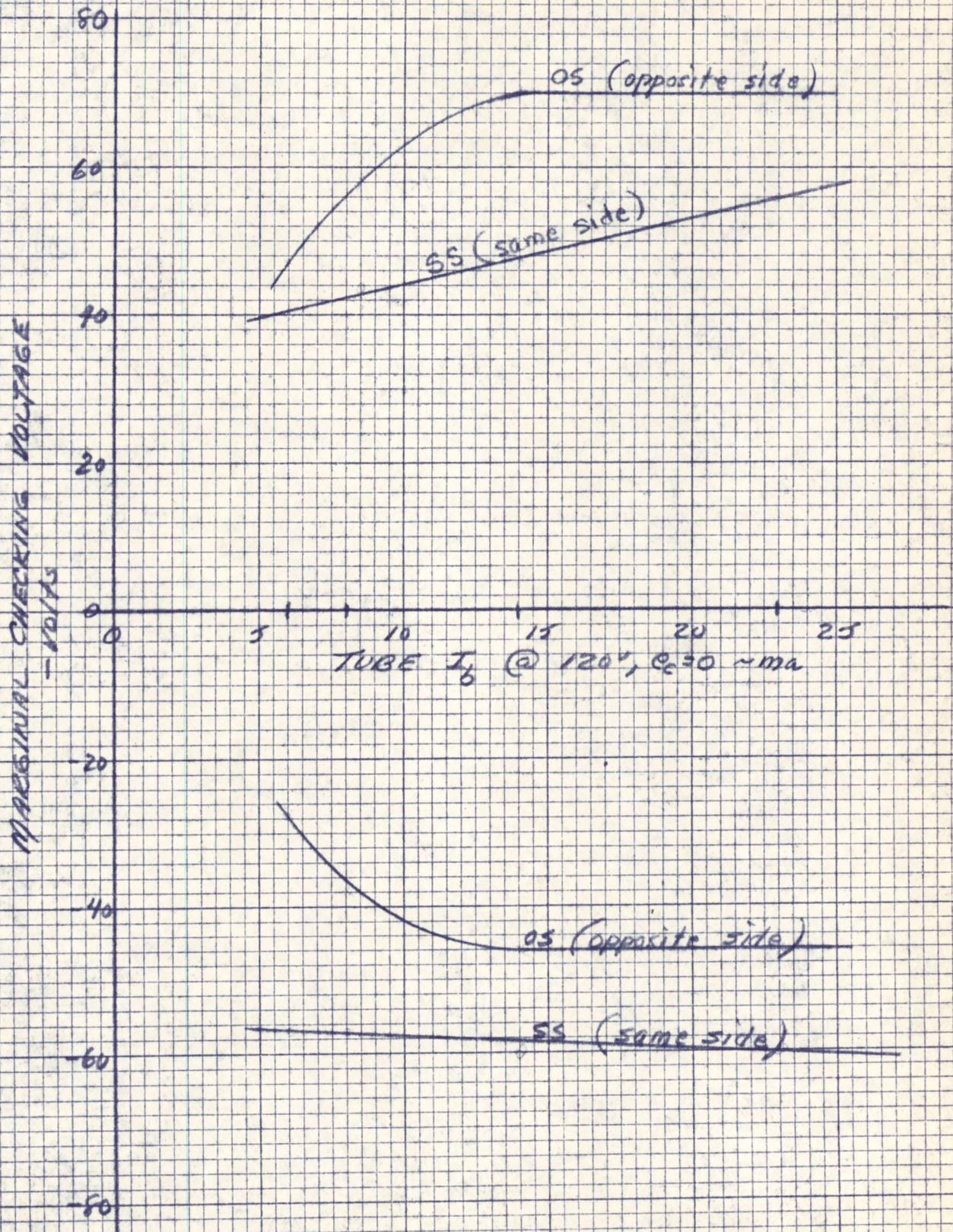


TUBE I_b (ma) @ $120^\circ E_k$ and $E_g = 0$, in test ckt.

~ FIGURE 7 ~

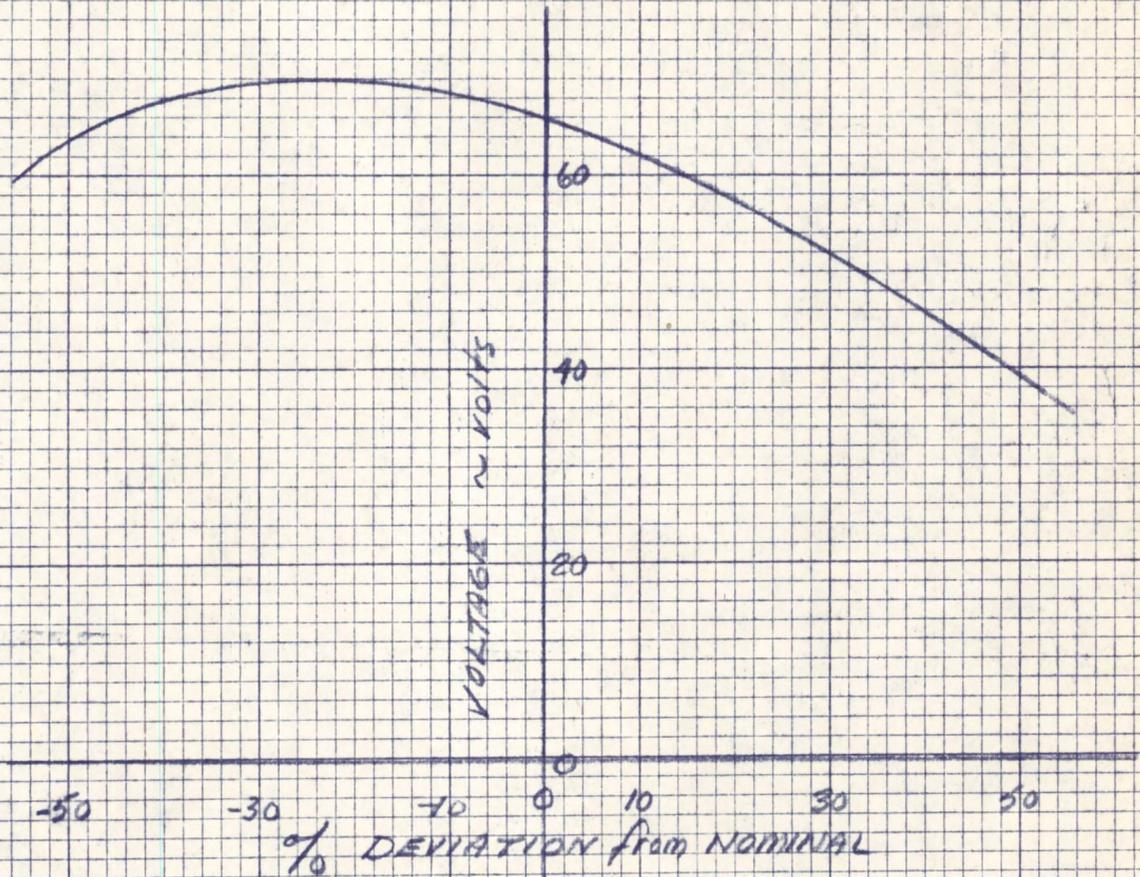
SA-48473

MARGINAL CHECKING TUBES



~ FIGURE 8 ~

MARGINAL CHECKING the CATHODE RESISTOR



MARGINAL CHECKING

20

40

60

~ FIGURE 9 ~

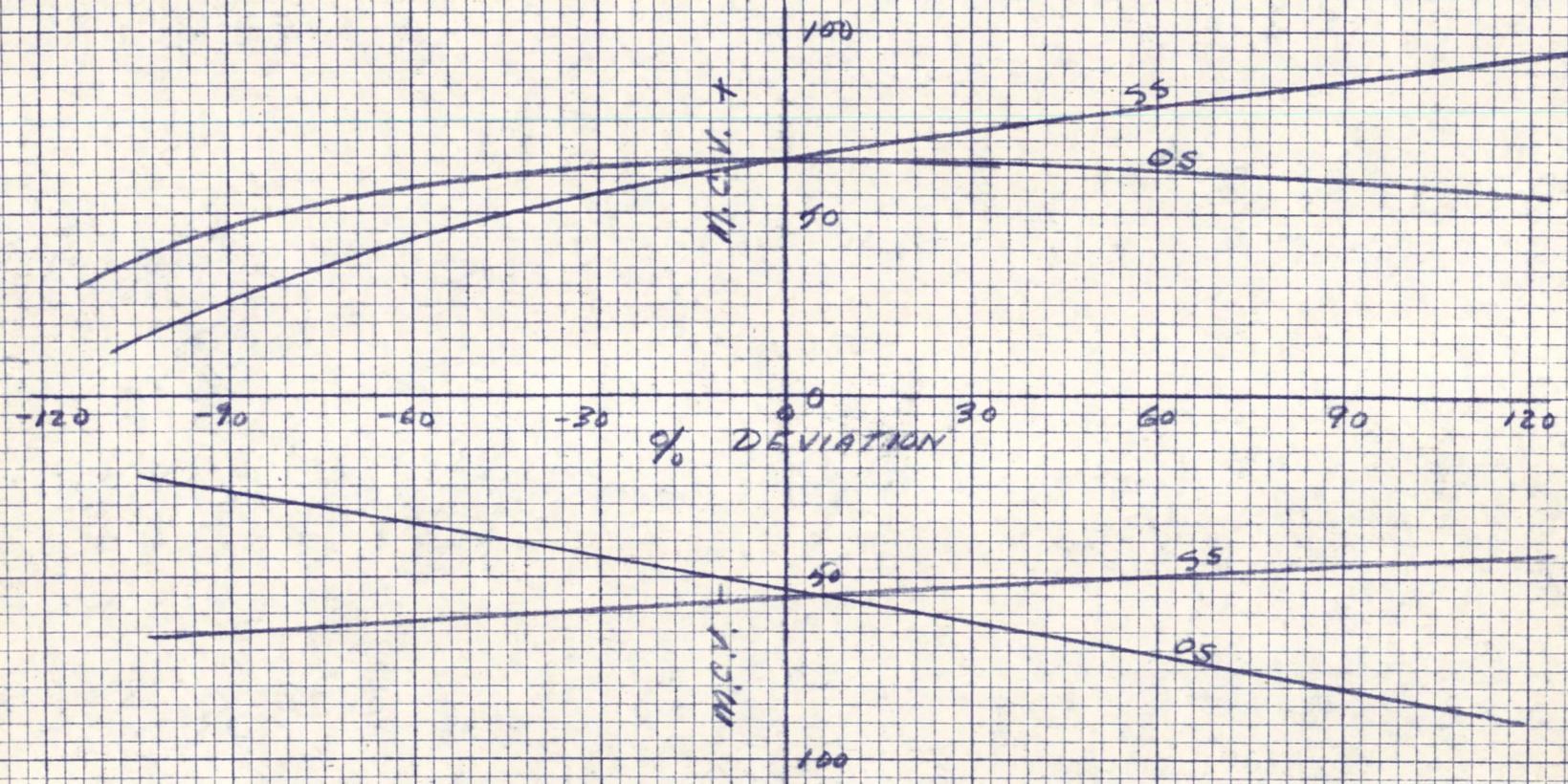
SA 48475

SA 48475

SA-48476

359-5G KEUFFEL & ESSER CO.
10 x 10 to the inch.
MADE IN U.S.A.

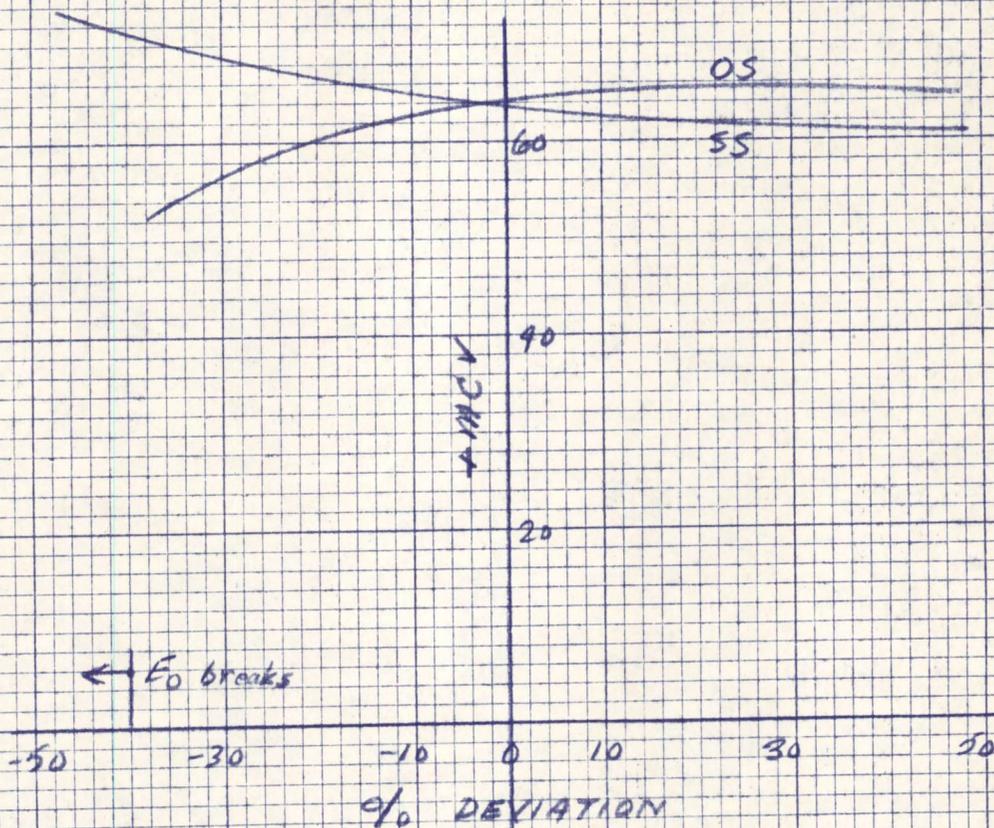
MARGINAL CHECKING the 3.9K PLATE RESISTOR



~ FIGURE 10 ~

SA-48476

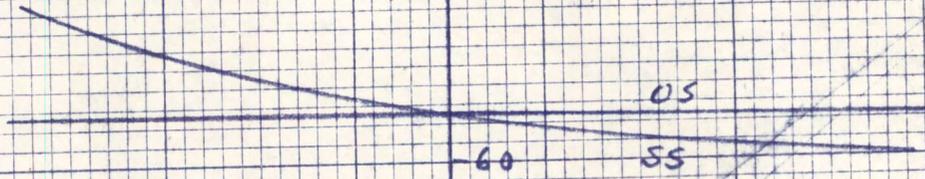
MARGINAL CHECKING the 15K PLATE RESISTOR



← E0 breaks

% DEVIATION

-MCMV



~ FIGURE 11 ~