Memorandum No. M-61

To: J. W. Forrester

From: Warren S. Loud

Subject: Discussion of Numerical Methods

Date: March 17, 1947

Digital Computation and Numerical Methods as a New Field of Mathematics

With the advent of high-speed digital computing equipment, the need for more study of numerical methods becomes apparent. Many questions of a mathematical nature arise when an attempt is made to employ this new machinery.

Two main aspects of the theory present themselves. First there is the question of errors. A numerical solution of an analytic problem will be in error because the numerical method is discrete and not continuous, and because any numerical expression is only an approximation to a quantity which is not rational with a small denominator. The two kinds of errors are called truncation errors and round-off errors respectively. The study of errors is of utmost importance. No confidence can be place in a numerical result unless an estimate of its error is available. A numerical solution of a process can be badly in error yet no clue to its error might be in evidence.

A second aspect of the theory is the question of numerical methods used with physical problems without an intervening differential equation. It would be of interest to know just how numerical methods can be used directly with physical or engineering problems.

Ideas for a Course in Numerical Methods

I. Background

At first sight numerical methods appear to be merely a tool for understanding and treatment of mathematical subjects. This is not entirely true, for numerical computation and its accompanying problems form a proper field of pure mathematics. Indeed one can look at the problem from two points of view, that of using numerical methods to learn more about other fields of mathematics or that of using the other fields of mathematics to learn more about numerical methods. However, since numerical methods do have much application to other branches of mathematics and also to engineering, it is advisable to obtain as broad a background as possible in the application of numerical methods to these other fields. There is a three-fold objective here. First, it is well to know the material so that places where numerical methods are of use at present can be known. Second, a wide acquaintance with related fields is desirable if new results within them are to be found by numerical methods. Third, it is well to have as many tools as possible for advancing the art of computational methods.

II. Specific Topics

Mathematical fields which would be studied include:

A. Algebraic and transcendental equations.

B. Differential Equations both ordinary and partial.

C. Integral Equations.

D. General Computations.

Discussion

A. Under algebraic equations we might emphasize the field of simultaneous linear equations in large numbers of unknowns. In general, iterative procedures should be emphasized in this field in view of the nature of high-speed computers currently being developed.

B. Ordinary Differential Equations

Numerical methods to date have not been helpful in the theory of differential equations because the time involved to obtain sufficient information to generalize from particular solutions has been prohibitive. With the new machines it is to be anticipated that sufficient particular information can be gathered in a reasonable time so that generalizations can be drawn. This can be considered a reason for study of this field over and above the desire to solve equations which cannot be solved in terms of elementary functions.

Partial Differential Equations

The statements made under ordinary differential equations apply here but with more force. Partial differential equations are more difficult to solve. Nevertheless many physical problems are currently phrased in terms of partial differential equations. Also since the theory is so much more limited, it will be important to have means for gaining new knowledge.

C. Integral Equations

Integral equations have been used more in recent years in physical problems. It would seem that here is a place where numerical methods could be widely used.

D. General Computations

There are problems in existence today which do not yield to analytical solution. Such problems arise in the theory of design of optical systems. Numerical methods are absolutely necessary in such problems. In addition matrix calculations can be studied from the point of view of high-speed machines.

III. Mathematical Methods Used

A. Relaxation Methods

B. Iteration Methods

C. General Numerical Methods

Relaxationsmethods are a recently developed tool finding much use in numerical work with engineering problems.

Interation procedures are given a special place because it appears that they will be of highest importance with high-speed machines. They represent an essentially simple process repeated many times.

In addition general numerical methods as described in books like Scarborough would be considered.

Under numerical methods in general, two remarks should be made. First, there needs to be an assembly of pertinent material. Much valuable literature on the subject is not collected in books, and it is often not available in English. Second, numerical methods should be examined with the thought in mind that they are to be used with high-speed machines. Present-day methods are designed for desk calculator speeds or slower. As a consequence, they are complicated, calling for reasoning and judgment on the part of the

operator. For high-speed machines, simpler repetitive methods should be considered. The high-speeds permit so many steps to be taken that the accuracy is still increased.

IV. Errors

Numerical methods introduce errors. Such errors are important, since it is necessary to know how close to the true solution a numerical solution lies. They fall in general into two classes, truncation errors and round-off errors. Truncation errors are those due to the fact that a numerical process is different from an analytical process. Such errors can be studied by analytical methods. Round-off errors are due to the necessary rounding off of each numerical step. This introduces errors which are of a random nature and difficult to analyze.

New Mathematical Results which can be Obtained by Numerical Methods

At the present time it is difficult to state just what new mathematical results can be obtained with high-speed machines. An opportunity for mathematical experiment presents itself. The technique of generalizations from particular experimental results so long used in science can be greatly extended in mathematics. Much work of this nature ought to be done.

As an example of results which can be obtained the theory of partial differential equations is in need of particular results that more generalizations may be drawn. There will also be an opportunity to study long-time iteration procedures in general. Iteration procedures have not been studied much in the past because they converge slowly if at all. However with high-speed

machines the slowness of convergence is not of importance and the properties of such procedures can be studied.

Many theorems in mathematics are of such a general nature that their use in specific cases is not possible. With machines of the type considered more concrete information can be obtained from these general theorems. For example, an existence theorem in order to be general often gives too restricted a result. It should be possible to obtain more comprehensive results in particular cases with such methods.

Warren S. Loud

Warren S. Loud

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DATA STORAGE - JWF - 4-47

MEMORANDUM NO. M-70

SERVOMECHANISMS LABORATORY
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Staff Members

FROM: Jay W. Forrester

SUBJECT: Data Storage in Three Dimensions

DATE: April 29, 1947

6345
Page 1 of 6 pages

Illustrations:

A-30363 A-30491
A-30488 A-30492
A-30489 A-30493
A-30490

The storage of operating instructions and numerical data is perhaps the most important and difficult operation in large scale digital computers. Large scale computers have in the past been made impractical by lack of satisfactory data storage means. Electrostatic storage tubes show satisfactory promise of operating as storage devices for the Whirlwind series of computers. It is, however, clear that storage tubes do not represent the ultimate in data storage devices. If other promising storage methods can be discovered they will be studied for evaluation. The storage method outlined below shows some promise and will be investigated to determine its possibilities. Glow discharges which might permit 3-dimensional storage arrays as outlined below are now being investigated as a thesis subject by Mr. Markel. The outcome of his work should indicate the lines for future study if additional work is shown to be desirable.

The concept of digital storage has passed from that of a vacuum tube, namely, the storing of a piece of information in a flip-flop circuit to surface storage where a single circuit controls many points of information on an area. This method of storing on an area as used in our electrostatic tube and the RCA Selectron still falls far short of effective use of the volume occupied by the storage equipment. Efficient storage will be possible only if points can be closely spaced in a 3-dimensional volume. Storage in a volume can be readily imagined if a suitable form of non-linear impedance having a double valued current-voltage characteristic is available. Such an impedance might support two different values of conduction current at a given operating voltage.

Examples of such an impedance characteristic are provided by the ordinary gas discharge tube and also by the germanium crystal rectifier in the reverse current direction. The gas discharge requires a voltage to

initiate conduction which is higher than that required to maintain current flow. The reverse current characteristic of the germanium crystal rectifier is shown in drawing No. A-30363. Operation of a storage system using a double valued impedance is most simply explained for 2-dimensional storage before proceeding to the 3-dimensional system.

Consider drawing No. A-30488. Illustrated are two sets of conductors crossing one another. Imagine a double valued impedance element tied between each crossover point of the two sets of conductors. Let the impedance characteristics of each of these elements be as shown in A-30363. As typical operating voltages for the impedance, assume that V_m is the breakdown voltage between the first and second stable operating points, identified on the drawing as currents I_1 and I_2. Identify the transition voltage from the second to the first operating states as the extinction voltage V_e. The normal operating voltage V_0 is capable of sustaining either current I_1 or I_2.

Suppose that the storage junction at the point 43' is to be placed in conducting condition I_2. All lines 1 to 6 are normally at 0 volts and all lines 1' through 6' are normally at V_0 volts. The voltage on 3' is raised and the voltage of line 4 is lowered by an equal amount until their difference exceeds voltage V_m. This is above the breakdown voltage and conduction will be in the region "C". Voltages at 4 and 3' can then be returned to normal with assurance that the impedance between line 4 and 3' is in the second conducting state. In the above operation, all other impedance elements either continued to operate at voltage V_0 or if connected to either line 4 or line 3' were raised half way between voltage V_0 and V_m. Either way, the unselected impedance elements would have remained in their respective operating regions adjacent to current I_1 or current I_2.

Current conduction in the region I_1 is established by a similar process wherein the voltage 3' is lowered and the voltage on line 4 raised by an equal amount until their difference is less than the voltage V_e.

The information stored at the non-linear impedance point can be read by noting the current change at line 4 caused by a voltage pulse at line 3'. An impedance in state I_1 will conduct only a small change in current in response to a voltage pulse compared to the change in current which will be conducted by an impedance in state I_2.

Three-Dimensional Glow Discharge Storage

It should be possible to develop a useful double valued impedance storage cell as a low pressure gas glow discharge. In drawing No. A-30489 is shown a typical static current versus voltage relationship for a gas

discharge from 0 current into the region of arc conduction. Current is plotted on a logarithmic scale. It will be noted, as in drawing A-30363, that two stable operating currents can exist, one prior to breakdown of the glow discharge which represents an extremely small current with little current change as voltage changes and one in the abnormal discharge region where current is relatively high and where current change is great with a change in voltage. The normal discharge region is one of essentially constant voltage with varying current. In this region the cathode area is not entirely covered by the glow discharge. After the cathode is entirely covered by the glow discharge conduction exhibits the characteristics of the abnormal discharge region where a positive resistance characteristic predominates. For a glow discharge storage cell, the normal discharge region should be shortened as much as possible through the use of small cathode areas. Such a static discharge curve might exhibit the characteristics of drawing No. A-30490. Operation at current I_1 and I_2 and at voltages between V_e and V_m would be as described earlier. It would be necessary to design the glow discharge electrodes in such a manner that the positive resistance characteristic in the region of I_2 would stabilize current glow without a series resistor.

Consider now a possible physical arrangement of glow discharge gaps and a selecting system for switching to the proper storage cell. If a glow discharge is used for storage then a gas breakdown system might well be used to switch the incoming lines, for writing, and for reading. Suitable switching must be incorporated inside the tube to reduce the number of external lines and the number of vacuum seals. Consider a switching system and 3-dimensional storage matrix as shown in drawing No. A-30491. The matrix consists of a 2-dimensional array of parallel wires extending through perforated plates. In addition to passing through the storage plates the 2-dimensional array of wires also passes through clearance gaps in the horizontal and vertical selecting bars and in the collector plate. Glow discharges may be established at each of these intersections between storage wires and the plates and bars.

The schematic diagram in drawing No. A-30492 shows the arrangement of gas discharge gaps involved in a single selection and operating process. Gap A exists between a vertical selection bar and the storage wire. Gap B is between a horizontal selecting bar and the storage wire. Gap C lies between the collector plate and the storage wire, while Gap D is between the storage wire and the storage plate. Gap E is between the storage plate and the outgoing lead to this plate while Gap F is between the storage plate and the common control wire to all storage plates. The following table shows a compatible set of gap characteristics.

Table

Gap	Ignite Voltage	Operate Voltage	Extinguish Voltage
A	V_e	V_e	V_e
B	V_e	V_e	V_e
C	$2V_e$	V_e	V_e
D	$3V_e$	$2V_e$	V_e
E	V_e	V_e	V_e
F	$2V_e$	V_e	V_e

Gaps A, B, and E show voltage regulator characteristics with constant voltage drop over a wide current range. Gaps C and F show a relatively high breakdown voltage but with a large cathode area which does not reach the abnormal glow region in operation. Gap D is the storage gap previously described which exhibits a high breakdown voltage and an operating point in the abnormal glow region. All gaps operating in the normal region are stabilized by current limitation at the abnormal glow gap D. Drawing No. A-30493 shows the three shapes of glow discharge characteristics at the six gaps.

Drawing No. A-30492 shows normal holding voltages at the various electrodes with arrows showing electron flow paths during standby conditions. A potential difference of $2V_e$ exists across gap D which may be in either the conducting or non-conducting state. Consider the following sequences of switching and controlling operation.

1. Selection

Selection of a storage gap is done in such a manner that the controlled voltage V_4 on the collector plate and voltage V_7 on the common wire can be used for establishing either the conducting or non-conducting state at the gap or to read the state of the gap. The following steps are required:

a. Reduce V_6 to voltage $2V_e$ and raise V_7 to 3.5V.

Result: Gap E extinguishes. Voltage V_5 drops. Gap F fires when V_5 equals $1.5V_e$. Voltage across D has dropped

to $1.5V_e$ but does not alter its on or off condition. After breakdown of gap F, V_5 rises to $2.5V_e$ bringing drop across all gaps D in this plate to $2.5V_e$.

b. Reduce V_7 from $3.5V_e$ to $3.0V_e$.

Result: V_5 returns to $2.0V_e$.

c. Raise V_1 and V_2 from $-V_e$ to 0. Reduce V_4 from $-0.5V_e$ to $-1.5V_e$.

Result: Gap A and B extinguish (probably only one was originally on). V_3 rises to $0.5V_e$. Gap C breaks down and is the only conducting gap in the collector plate. This operation disconnects the storage wire from gaps A and B and connects it to the collector plate through gap C.

d. Raise V_4 to $-V_e$.

Result: V_3 is now at 0 volts under the control of V_4 and V_7. Only the gap C for the particular storage wire under consideration and the gap F for the particular storage plate under consideration are fired. No other C or F type gaps are conducting. All other storage wires and storage plates are controlled by their respective V_1, V_2, and V_6 voltages.

2. Gap Control

Switching is now complete and the sequence can be followed to write 0, write 1, or read at the gap selected. By a corresponding process to steps a through d the line V_4 and V_7 could have been connected to any other storage gap. Voltages at operating points are now as follows:

$$V_4 = -V_e, \quad V_3 = 0, \quad V_5 = 2V_e, \quad V_7 = 3V_e$$

a. Assume the digit 1 is to be written corresponding to conduction at gap D. Reduce V_4 to less than $-1.5V_e$. Raise V_7 to more than $3.5V_e$.

Result: Voltage across gap B is above $3.0V_e$ and breakdown will occur. The maximum voltage across any other gap D is $2.5V_e$ and other gaps will not be ignited.

b. Assume that the digit 0 is to be written corresponding to no conduction at gap D. Raise V_4 above $-0.5V_e$. Reduce V_7 below $2.5V_e$.

Result: Voltage across D is below V_e and the gap will be extinguished. The minimum voltage on any other storage gap will be $1.5V_e$ so that other conducting states will not be affected.

c. Assume as the third possibility that the condition of gap D is to be read. Hold V_4 at $-V_e$. Raise V_7 from $3V_e$ to $3.5V_e$.

Result: If D is conducting there will be a large current increase through gap D which can be observed as an increase of current to the collector plate. If gap D is not conducting little current increase will occur at the collector plate.

The storage and switching system described above requires discharged gaps which can be constructed to meet specified breakdown and extinction voltages and which exhibit extreme stability in these voltage characteristics.

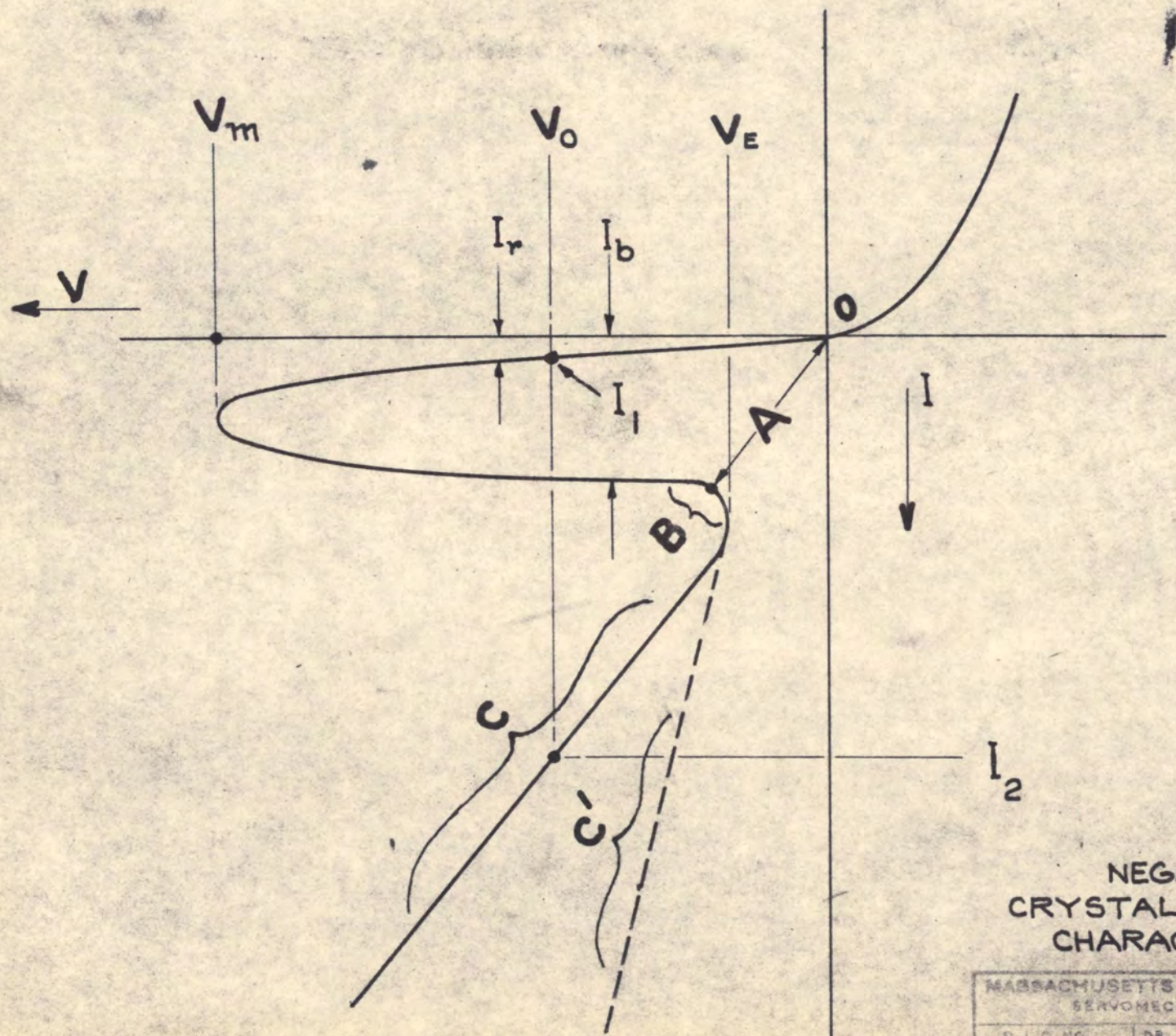
Firing and deionizing time must be short and the pulse impedance of a gap must be low. The above discussions have been carried out in terms of the static glow discharge characteristic. This static characteristic is known not to hold under pulse conditions but it is anticipated that similar curves, differing in numerical values, will prevail.

Until additional information is collected and until tests with especially designed gaps have been completed, it will be impossible to evaluate the promise shown by the system outlined above. The major problems seem to be the short operating times required and the problem of obtaining uniformity in gaseous discharge performance.

Advantages of the system are rather obvious. Storage sensity will be high since storage is in a volume rather than in individual circuits or on a surface. Mechanical assembly will be relatively easy except for the problems involved in obtaining accurate gap tolerances and performance. The system inherently includes most of the switching as well as the storage function. The number of seals necessary to be brought through the glass are practical and amount to the cube root of the number of storage gaps plus the two control wires. In construction the storage volume might take the form of parallel metal plates perforated for passage of the storage wires with these plates interleeved by ceramic barriers to confine the glow discharge to the individual gap structure. Work on this storage method will be assigned low priority until it reaches the stage where evaluation is possible.

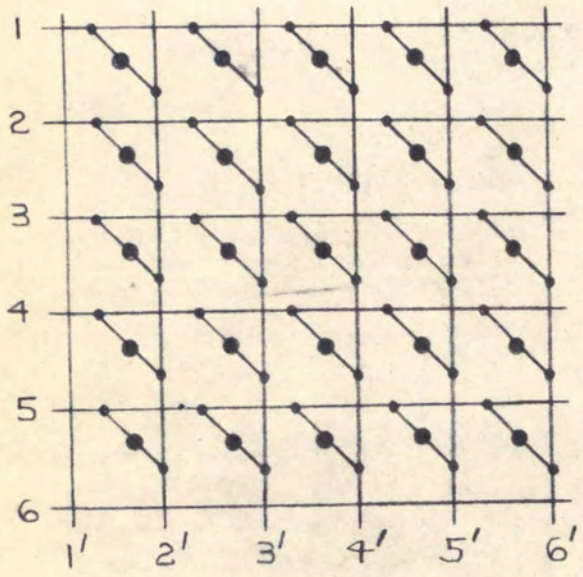
JWF:vh

A-30363



NEGATIVE
CRYSTAL RECTIFIER
CHARACTERISTICS

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. C. NO. 6345	DR	CK
ENG. JWF 3/11/47	APP.	A-30363



VOLTAGES FOR OPERATION

OPERATION	VOLTAGE ON ONE OF LINES 1 THRU 6	VOLTAGE ON ONE OF LINES 1' THRU 6'
SUSTAIN	0	V_0
ESTABLISH CONDUCTION (CURRENT STATE I_2)	$< -\frac{V_0 - V_m}{2}$	$> V_0 + \frac{V_m - V_0}{2}$
EXTINGUISH (CURRENT STATE I_1)	$> \frac{V_0 - V_\ell}{2}$	$< V_0 - \frac{V_0 - V_\ell}{2}$
READ	0	$> V_0$

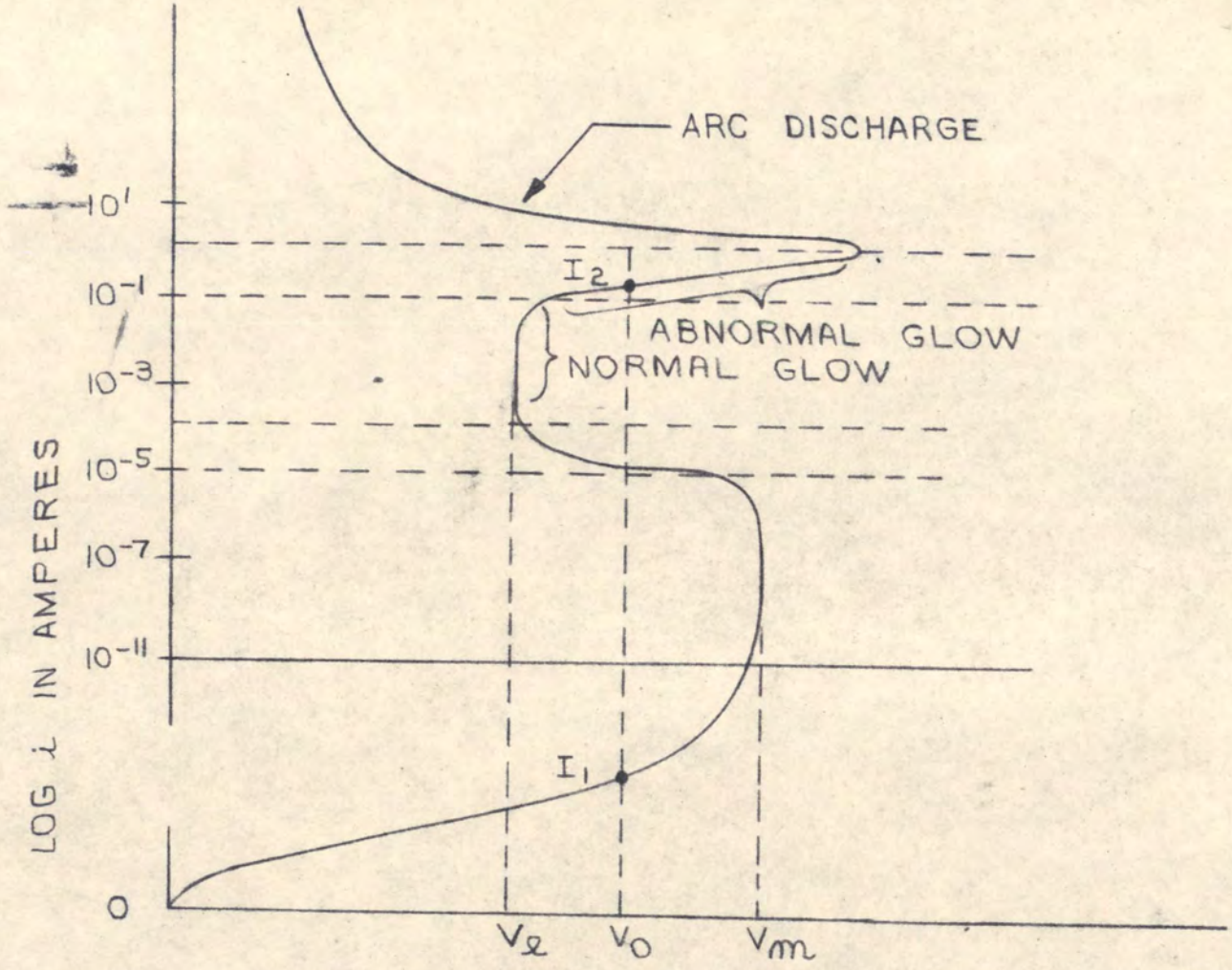
SEE A-30363 FOR SYMBOLS

↖ = DOUBLE VALUED IMPEDANCE

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

TWO-DIMENSIONAL STORAGE ARRAY
USING DOUBLE-VALUED IMPEDANCE ELEMENTS

SCALE:	DR. D.L.O. 5-6-47	**A-30488**
ENG. J.F. 5/9/47	CK. JWF 5-7-47	APP'D



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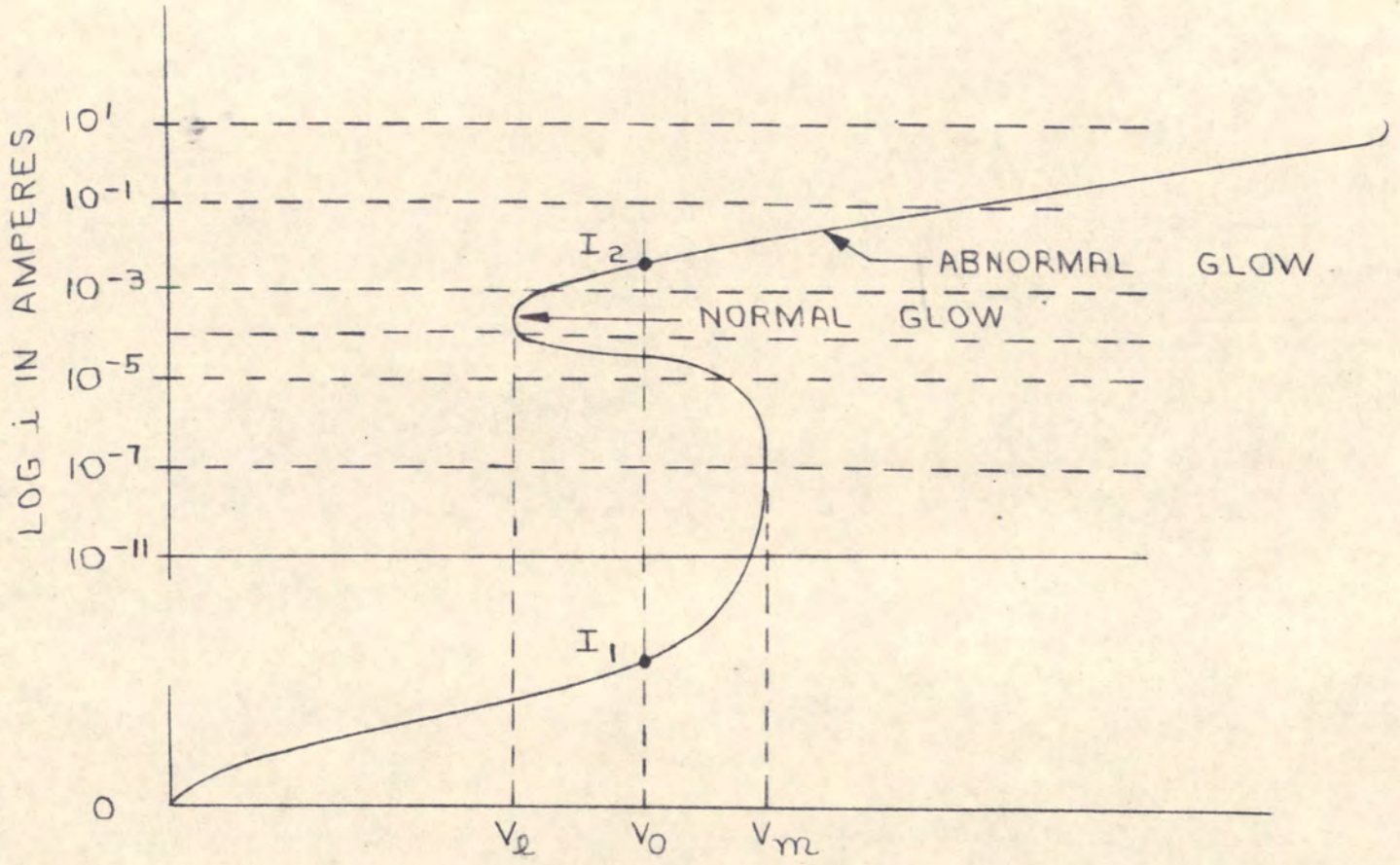
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

GLOW CHARACTERISTICS FROM TEXT WITH ADDITIONS

SCALE:	DR. D.L.O. 5-6-47	
ENG. 5/9/47	CK. 5.7-47	APP.

A-30489



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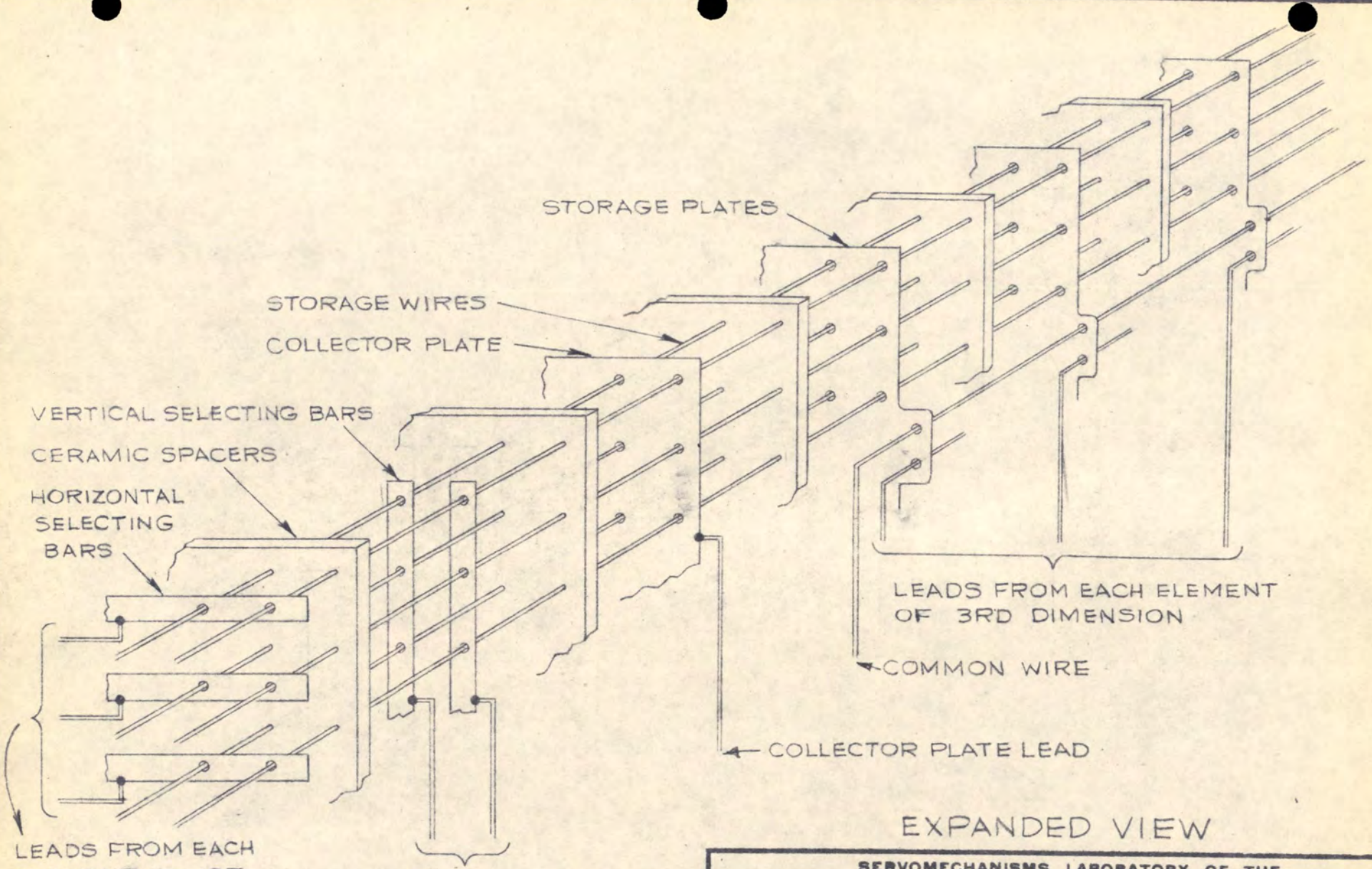
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

IDEAL STORAGE - CELL CHARACTERISTICS

SCALE:	DR. D.L.O. 5-6-47	A-30490
ENG. 5/9/47	CK. 5-7-47	APP.

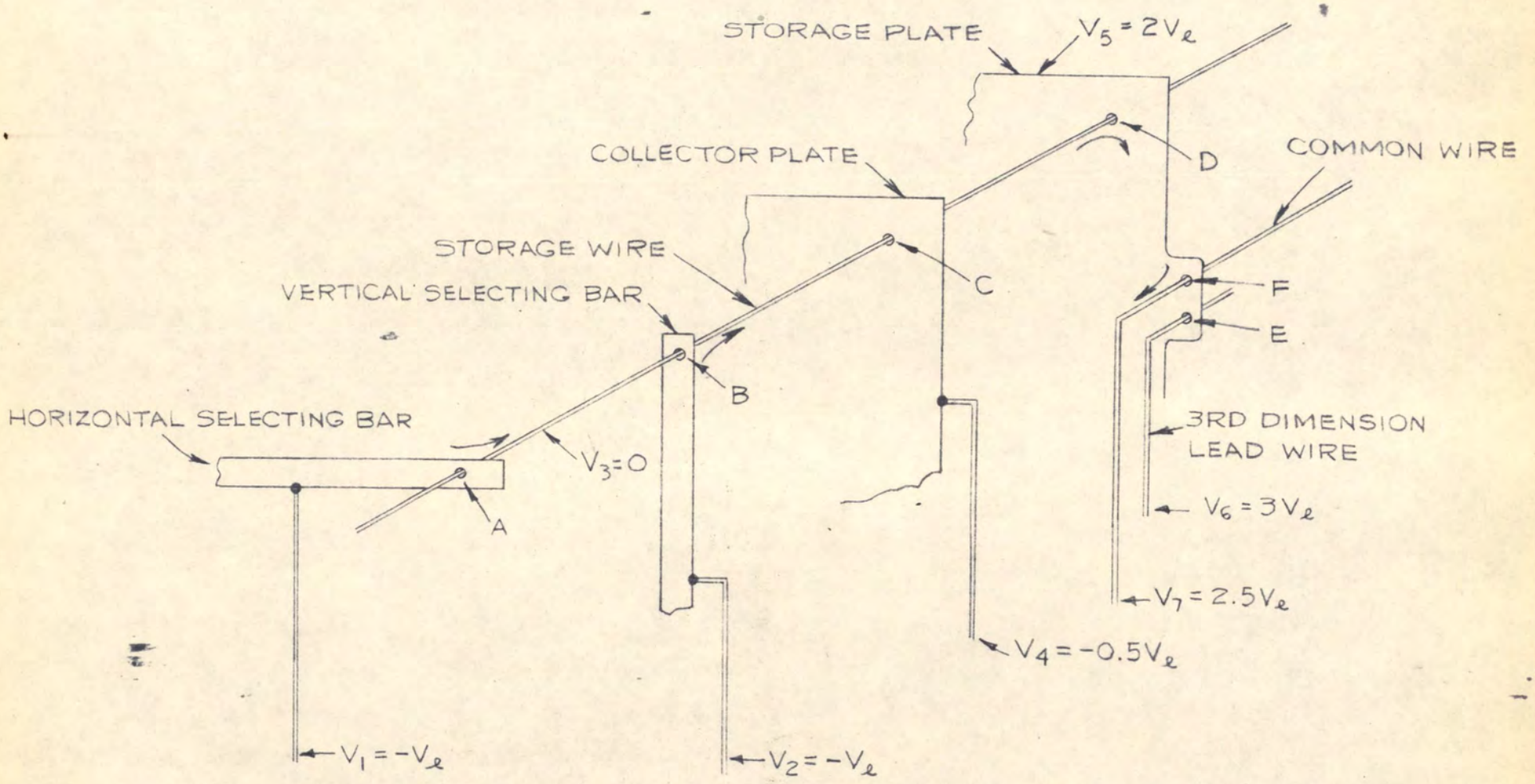


EXPANDED VIEW

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

3-DIMENSIONAL STORAGE

SCALE: NONE	DR. F. Brunswick 5-6-47	A-30491
ENG. 5/9/47	CK JWA 5-7-47	APP.



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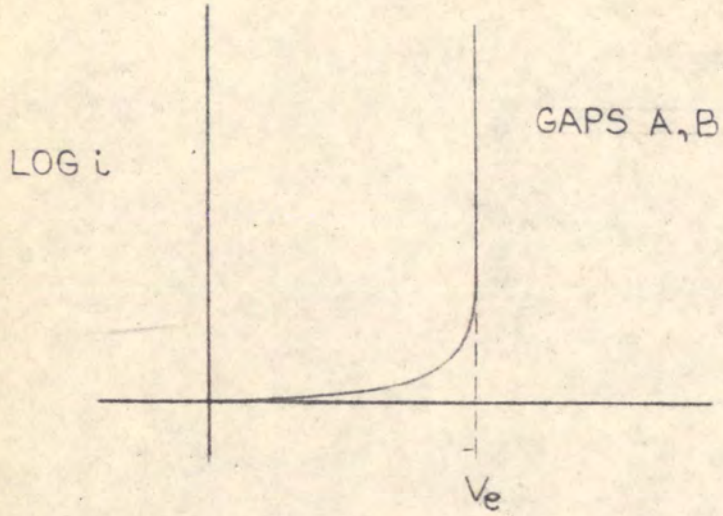
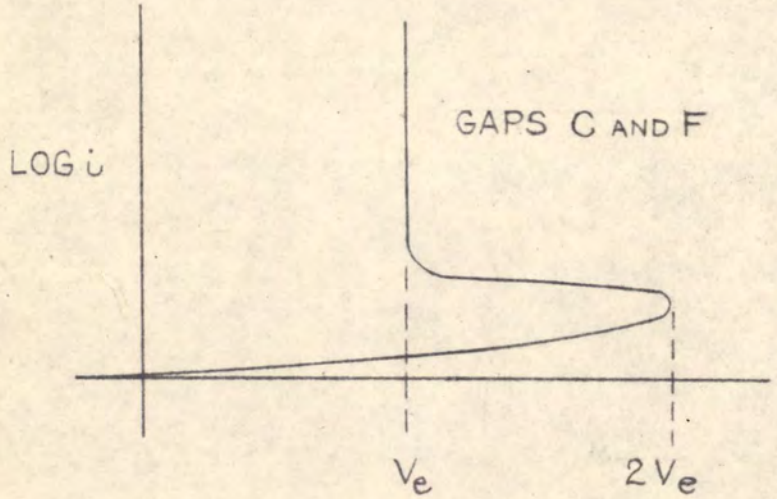
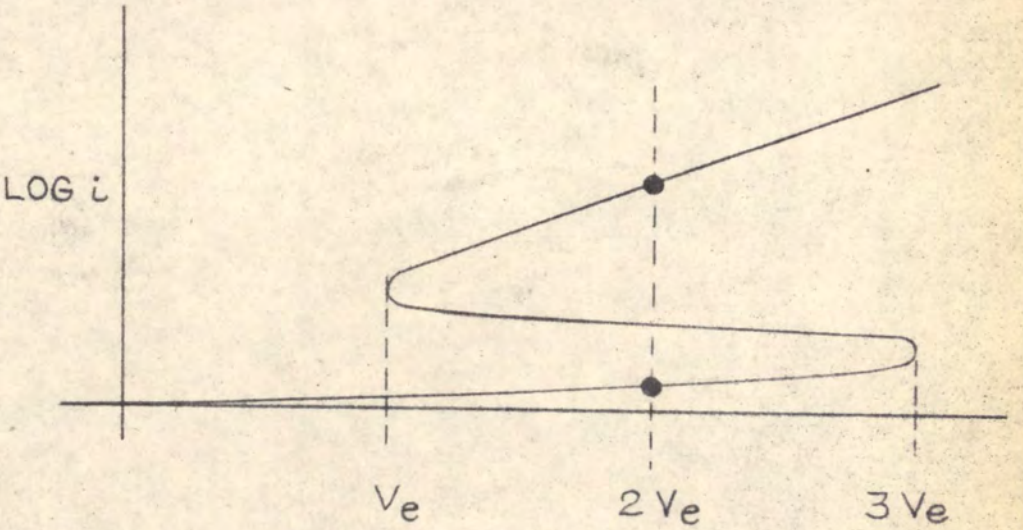
SCHEMATIC OF STORAGE GAPS

SCALE: NONE	DR. F Brunswick 5-6-47	A- 30492
ENG. 5/9/47	CK. 5.7.47	APP.

A-30493







SERVOMECHANISMS LABORATORY OF THE
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DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

COMPOSITE OF GAP CHARACTERISTICS

SCALE:	DR. F. WOLSKY 5-6-47	
ENG. 5/9/47	CK. 5.7.47	APP.

A-30493

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MATHEMATICAL WORK OF PROJECT WHIRLWIND

To: Jay W. Forrester

From: Philip Franklin

Date: November 12, 1947

I. The Mathematics Program

The projected Whirlwind high-speed electronic digital computer, from the mathematical point of view, has several objectives. One aim is to solve the equations of motion for aircraft and so serve as the computing element of an aircraft analyzer. A more general objective is the solution of other problems of engineering interest, particularly in the field of dynamics and ordinary differential equations.

The mathematical studies in the past have related to the specific equations to be solved, some tests of existing numerical methods, and attempts to anticipate possible difficulties with a view to prescribing how to meet them. At present a study of known methods of solving simultaneous linear equations and differential equations is under way, with a view to the coding of such methods for the computer. These studies will be extended to other types of problems, such as those listed in Section III.

II. Studies Already Completed

A survey of numerical methods made by Dr. Loud and his associates, summarized in Memorandum M-61 (Vol. 8), revealed as subjects of major importance the solution of linear simultaneous equations, and the solution of ordinary differential equations.

For the solution of linear simultaneous equations, elimination methods, iteration methods, relaxation methods, matrix methods, and the method of steepest descent have all been considered and expositions of these methods studied. For some of these, codes are in process of preparation.

The errors inherent in solving systems of equations of very high order, when all of the coefficients have random errors, has been pointed out.

A number of solutions have been carried out for simple differential equations to provide case histories of accumulated round-off and truncation errors. These indicate the objections to numerical integration over a large

number of cycles without some check, such as the use of the energy integral for conservative systems. The possibility of filtering out frequencies corresponding to computational instability terms has also been considered.

A method of using Fourier Transforms to estimate the best value of a function or its derivative (the message) when its values over a long range are known only to within certain random errors (noise) was presented to the group. Later studies indicated this as having restricted application to computation because of the rare occurrence of data with truly random errors.

Last year several conferences were held at M. I. T. on digital computation. Some were sessions of the Electrical Engineering Department seminar, but were well attended by representatives of the Mathematics Department and Project Whirlwind. Another series of smaller conferences were attended by some electrical engineers, including Professors Hazen and Y. W. Lee, as well as several members of the Center of Analysis. The mathematicians present included Professors Phillips, Martin, Wiener, Franklin, Wallman, and Thomas.

In addition to these men, several other M. I. T. staff members have shown an interest in electronic computers, and a willingness to give advice when problems in their special fields are considered. Thus, if shock waves are under consideration, advice can be obtained from Professors Tsien or Lin or Dr. Kopal, who are all familiar with this field. For elasticity problems and their theory Professor Reissner, for statistical and meteorological applications Professor Wadsworth, and for general numerical computation Professors Hitchcock, Crout, and Hildebrand are available.

The many members of the M. I. T. Mathematics Department who are interested in numerical computation contribute much information about recent developments through informal discussions.

In addition, the staff members of the project have attended meetings at Princeton, Philadelphia, New Haven, and Cambridge at which computing methods were discussed. And the group has followed recent developments in the theory of codes and numerical computation at Princeton, Harvard, the University of Pennsylvania, and elsewhere.

III. Plan for Future Investigations

Certain problems of interest to applied scientists and engineers can be most conveniently solved by numerical methods. Classified mathematically, the principal types are as follows:

1. Solution of ordinary differential equations with given initial conditions.

2. Solution of parabolic and hyperbolic partial differential equations, obtaining the characteristics curves as in 1.

3. Solution of systems of linear simultaneous equations.

4. Solution of ordinary differential equations with boundary conditions at more than one point.

5. Solution of elliptic partial differential equations for various types of conditions on the boundary of a region.

6. Solution of non-linear simultaneous equations.

7. Least square solutions of overdetermined systems of the types of 3 and 6.

8. Solution of integral equations.

9. Tabulation of functions.

While the relative advantages of different methods may change in the transition from hand or desk calculations to high-speed machines, it is improbable that any radically new mathematical principles will come into play. Much past and recent experience bears this out.

Thus, the methods used by Aiken in computing tables, or by the Watson Laboratory in checking the moon's motion, bear strong resemblance to those long known to astronomers; and except for the use of conditional orders the methods used for elementary functions, such as those coded for the A.R.C. by Booth and Britten, would have been used by Babbage in the nineteenth century if he had completed his analytical engine.

Again, the report on linear equations by Bargmann, Montgomery, and von Neumann recommends as the two best methods an iteration rule, stated by Hotelling, which amounts to an application of Newton's method of approximation, or an elimination method which is that used by most computers in such forms as those of Doolittle or Crout.

And except for minor details of technique, the differential analyzer uses mathematical methods differing little from those used by Kelvin in evaluating special integrals with his globe disk and cylinder integrator.

This suggests that the first attack with the computer on the problems listed above should be by processes close to the traditional ones. Of course, two special points to be covered in taking over existing methods are the coding of complete instructions to remove any human judgment, and keeping the high speed from letting us carry the computations beyond their range of validity.

The present thinking on procedures for the various types of problems is as follows:

1. Ordinary Differential Equations, One Point Conditions

For systems of ordinary differential equations, some method using second differences or their equivalent such as the

Runge-Kutta method or the Moulton (Adams, Kriloff) method. This last may be used in the form set up by Ford, which uses linear combinations of the numbers instead of differences. After several steps have been taken, the results can be checked and improved by a Simpson's rule calculation which would have a smaller round-off error than the result obtained step by step.

2. Characteristics of Partial Differential Equations

Most of the procedure is as in 1, the new feature being the cut-off due to an initial boundary or the meeting of some conditional bounding condition like that for shock waves.

3. Linear Algebraic Equations

For systems in 20 or fewer variables, an elimination method can be used and coded with about 80 orders. The matrix iteration procedure $F_{k+1} = F(2-AF_k)$ to obtain A^{-1}, the limit of F_k, may be useful for more variables or where a system must be solved for several right members. A steepest-descent method on the sum of the squares of the residuals may be useful for a large number of variables.

In many applications where numerous variables are met, the system is loosely coupled in the sense that effects in one place affect values at a distance only slightly. Here much of the difficulty of treating a large matrix with all values equally in error disappears.

Systems with determinants near zero will have to be recognized as such at some stage of the solution process, and the recognition used as a halt signal.

4. Ordinary Differential Equations, Boundary Conditions

This situation will be met by reduction to an integral equation, by an expansion in known functions whose co-efficients are found by solving linear equations (Ritz, Galerkin, Fourier), or from solutions found as in 1. For conditions at two points we use a family of solutions starting from one point, and interpolate to meet the conditions at the second point. For linear differential equations with conditions at several points, we may use a linear combination of independent solutions found numerically, evaluating the constants by solving a system of linear algebraic equations.

5. Elliptic Partial Differential Equations

Linear partial differential equations of elliptic type are reduced to difference equations on nets. In a two-dimensional problem, if our machine eventually used say 64 points on a square

it might be advantageous to get a first approximation for a 4 x 4 grid by solving simultaneous equations, then interpolating on this for a first approximation on an 8 x 8 grid, which could be improved by some successive approximation scheme or relaxation method. Relaxation methods by machine have the difficulty of requiring a large number of comparison orders.

WWI will probably be able to work two-dimensional grids of fairly fine dimensions, but possibly only crude three-dimensional grids, like those now used by hand in two-dimensional problems.

6. Non-Linear Algebraic Equations

Iteration procedures are usually successful. The code would have to make possible the insertion of an approximation at different points in a loop, only continuing if the successive values clustered after a few tries.

7. Least Squares

Gauss procedure reduces this to 6 and 3.

8. Integral Equations

Approximation of the kernel by a degenerate one reduces linear integral equations to 3, or we can express the solution as a linear combination of known or determined functions as described under 4 above.

9. Functions

Our machine will probably tabulate functions only for its own use. Functions will be inserted either through discrete values and an interpolation program, or by using polynomials that approximate the functions in restricted ranges and calculating the polynomials.

In some cases the approximating polynomials may be found by approximating some higher derivative and integrating.

In addition to general methods, several aspects of the specific application of the computer to the analysis and control problem will be considered. Thus, the detailed equations and constants for different types of service and air-borne craft will be investigated.

Some preliminary studies of the mathematics of correlating statistically, at information centers, data from radar stations will be continued.

IV. The Practical Estimate of Error

While existence theorems are nice to have when they can be obtained,

much numerical work proceeds successfully without them. For example astronomers guessed right on semi-convergent asymptotic series before they were understood by the purists. Series with coefficients obtained by numerical methods are used to predict the moon's position years in advance, but the stability of the system of sun, earth, and moon under the known initial conditions has never been established with complete mathematical rigor. Many of the iteration processes used to find roots of equations can either converge or diverge rapidly. By comparing, say, a fourth and a fifth approximation, and sensing the size of the discrepancy, our machine will recognize the process as finished, promising for further approximations, or useless for computation because of divergence or excessively slow convergence.

A large percentage of recent numerical computation for partial differential equations has no other justification than that the results seem to converge. Undoubtedly many WWI and WWII solutions will use such evidence, for lack of anything better.

Because of the labor of making codes, high-speed machines will be chiefly used for whole fields of solutions. A certain amount of experiment on the machine may be needed at the start, but once verified for a few cases, the method will extend to the whole field.

Similar considerations apply to formulas for the size of the error. These are seldom used literally, because if rigorous they are apt to be much too pessimistic in practice. At best such formulas are merely useful to prove convergence; a comparison of successive values then estimates the error.

In many problems the stability of the method of solution can be predicted in advance, and a large number of solutions differing slightly are to be found. Here the smooth character of the results is a reasonable protection against excessive errors at any place.

In other cases, some form of a successive approximation method will be used. When the process succeeds, the clustering of the approximations serves both to check the results and to provide an estimate of the closeness of approximation.

When the successive approximation method fails, some order to test the closeness of approximations after some set number of steps will lead either to a halt signal or to an alternative procedure. Thus in a loop process the alternative may be another starting point in the loop. In a step-by-step process the alternative may be the use of smaller steps.

In many solutions of ordinary differential equations by the Moulton method, the use of a Simpson's rule integration over large intervals may prevent the piling up of round-off errors.

V. The Influence of Mathematics on the Design of WWI

The specifications for WWI were set up with the aim of providing a prototype capable of performing all the operations desired from a computer, on a scale large enough to be applied to many typical situations, and sufficiently limited to be constructable in reasonable time. However, within this last limitation, it was found feasible to provide for greater speed and storage capacity than any existing digital computer possesses.

The types of desired mathematical operations are fairly well known: namely, the four fundamental arithmetic operations, and certain logical operations such as shifting, digit transfers, subprogramming, and conditional subprogramming. From these fundamental elements any finite combination of computational processes can be built up.

The mathematician's requirement is that these operations be performed either directly, or by combination of other operations. Thus division or square rooting can be either built in as special operations, or carried out by a subprogram. The present plans call for a built-in division unit, and the possibility of including a few special orders which would enable the operator to call for any particular subprogram, as that for square root.

Considerable study of binary arithmetic and the conversion problem showed the feasibility and advantage of having the computer work in binary arithmetic but translate data and outputs from or into the decimal notation.

A guiding principle of the WWI specifications has been maximum flexibility. This will simplify the extension to larger models, and will increase the effective power of the computer, for example by allowing an arbitrary distribution of the storage capacity between numbers and orders.

Beyond the fundamental questions just mentioned, and verification that the computer has sufficient speed and capacity for certain specific problems such as that of aircraft control, mathematical considerations can have little effect on the basic design.

With regard to overall capacity of later models, experience with WWI and theoretical considerations can only dictate ratios of components, rather than absolute size. For the size at any stage will always be limited by economic and engineering factors. Any machine is certain to have just a little less capacity than that required for some desired applications. For WWII, sufficient capacity for the aircraft problem seems to be the only fixed requirement; that is, it should have sufficient speed and capacity to be used as a computing link in the aircraft analyzer.

Philip Franklin

Philip Franklin

PF:hcs

4-104
4-138 Bl. Cons Bl. Child

6345
Memorandum M-1058

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: STAFF INDOCTRINATION PROGRAM

To: New Staff Members

From: J.C. Proctor

Date: July 5, 1950

In order to assist new staff members in becoming familiar with our project and its organization, a two week program of selected reading, with discussions by various members of the staff, has been arranged. The program will, in general, be as follows, with whatever modifications may be necessary to fit individual requirements.

INDOCTRINATION PROGRAM

FIRST DAY

J.W. Forrester — Welcome to the Project and Discussion of Computers and their future role in Science, etc.

Reading:

R-142 Talk delivered by J.W. Forrester at U.C.L.A., Modern Calculating Machinery and Numerical Methods Symposium, July 1948.

R-154 OUTLOOK FOR ELECTRONIC DIGITAL COMPUTERS--SCOPE OF THE ENGINEERING INVOLVED, J.W. Forrester.

R-166 DIGITAL COMPUTERS AS INFORMATION PROCESSING SYSTEMS, J.W. Forrester.

R-115 PROJECT 6345 ELECTRONIC DIGITAL COMPUTERS, J.W. Forrester.

R-116 PROJECT 6345 ELECTRONIC DIGITAL COMPUTERS, J.W. Forrester.

SR-2 Volumes 1, 2, and 3.

SECOND DAY

H. Fahnestock The History of Whirlwind I

Assorted Reading on the History of Computers:
(Most of this material is in the Vail Library. Check with the Project Librarian, Rm. 217, for any of this material she may have).

PROCEEDINGS OF A SYMPOSIUM ON LARGE-SCALE DIGITAL CALCULATING MACHINERY, Annals of the Computation Laboratory of Harvard University, Vol. XVI. Vail

HISTORY AND DEVELOPMENT OF METHODS USED IN AUTOMATIC-SEQUENCE-CONTROLLED COMPUTING MACHINES, D.J. Crawford, E.E. Seminar, January 1947. Vail

A HISTORICAL SURVEY OF DIGITAL COMPUTING MACHINES, D.R. Hartree, Proceedings of the Royal Society, A, 195, 265-271 (1948). Central

~~BABBAGE'S CALCULATING ENGINES, H.P. Babbage.~~ unavailable

AMA--AN EPOCH IN TELEPHONE ACCOUNTING, Bell Laboratories Record, 27, 2-4 (1949). Vail

AIEE Technical Paper, 50-42 (1949). Whirl

THIRD MORNING

R-Formal
E-Eng. Notes
M-Memo
A-Admin
C-Confer.

John Proctor Non-Technical Discussions of Personnel Matters, Laboratory Procedures, etc.

Reading: Security
Memorandums A-55, A-58, A-92, A-94, A-107.

Organization of Project: Personnel
A-62.

Personnel Policies
The Institute publication POLICIES AND PROCEDURES, and A-72--OFF HOURS WORK.

Drafting
A-43, A-46, A-46-A, A-83, and MECHANICAL DRAFTING STANDARDS. PRINT ROOM FILE

Stockroom
Electrical and mechanical supplies, tools, instruments, etc.--THE STANDARDS BOOK.

Purchasing
A-88.

THIRD MORNING (Continued)

Fire Drills
A-99.

Reports, Memoranda, and Typing
A-78, A-45, A-61, A-90-2, A-104, A-42-2.

Production Control
A-81

THIRD AFTERNOON

R. Mayer Binary Arithmetic 130

Reading: R-90 THE BINARY SYSTEM OF NUMBERS, M. Florencourt.

FOURTH DAY

R.R. Everett Block Diagrams

Reading: M-62 THE PROJECT WHIRLWIND PROGRAM OF ELECTRONIC DIGITAL COMPUTATION, J.W. Forrester.

M-63 DIGITAL COMPUTING MACHINE LOGIC, R.R. Everett.

M-76 DIGITAL COMPUTERS IN SCIENCE, J.W. Forrester.

R-127 WWI COMPUTER BLOCK DIAGRAMS, R.R. Everett & F.E. Swain.

FIFTH DAY

S. Dodd Storage Tubes

Reading: E-149 HISTORY OF STORAGE TUBE PROGRAM, S. Dodd. (Contains other references)

R-153 ELECTROSTATIC STORAGE TUBES FOR DIGITAL COMPUTERS AND OTHER INFORMATION PROCESSING SYSTEMS, J.W. Forrester.

SIXTH DAY

E. Rich, J.A. O'Brien Electronics

Reading: Basic Circuits

R-109 GATE CIRCUITS, D.R. Brown, December 17, 1946.

SIXTH DAY (Continued)

R-113 FLIP-FLOP CIRCUITS, J.J. O'Brien, March 19, 1947.
E-104 BASIC CIRCUIT REVISIONS
E-144 BASIC CIRCUIT REVISIONS

Gate Tubes
M-103 GATE TUBE DEVELOPMENT
E-137 PERFORMANCE OF CHAINS OF GATES
E-139 7AK7 CHARACTERISTICS

Vacuum Tube Life
R-139 VACUUM TUBE LIFE, Dave Brown, June 1, 1948.

Matrix Switch
R-123 32 POSITION SWITCH, J.A. O'Brien, July 15, 1947.

Crystals
E-128 CRYSTAL RECTIFIERS FOR WWI

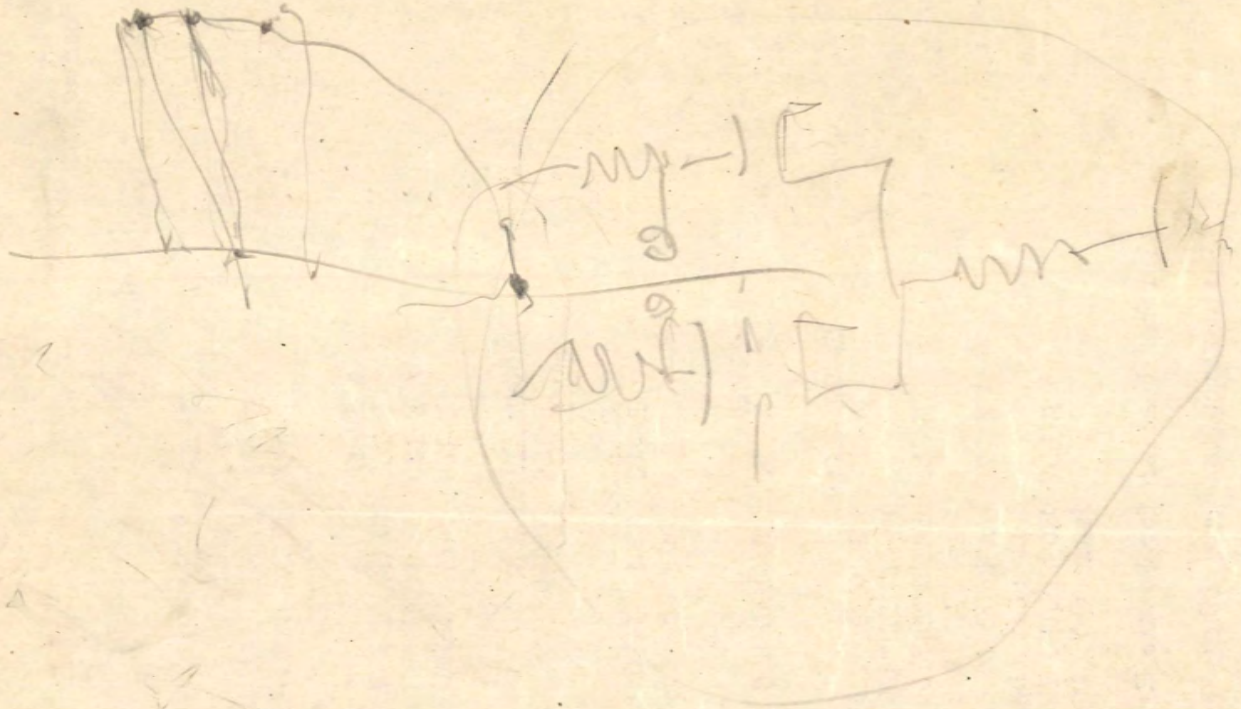
Miscellaneous
M-77 USE OF D.C. RESTORER CIRCUITS AS A MEANS OF ELEMENTARY D.C. COUPLING
M-555 DEMONSTRATION OF TRANSISTOR AT BTL, E. Rich, July 27, 1948.
E-77 BLACKOUT IN 6AS6 AND SR1030 GATE TUBES, R.L. Best, December 1, 1947.
M-207 DECOUPLING IN WW CIRCUITS, Harry Kenosian, January 7, 1948.

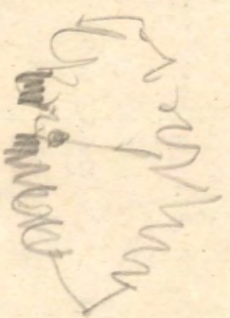
Further Reading for Future Reference:

Basic Circuits	Gate Tubes	Vacuum Tube Life	Pulse Transformers
E-95	E-61	E-109	R-122
E-114	E-73	E-110	E-138
E-115	E-132	E-112	
M-306	E-137	M-361	
M-329			
M-566			

Switching	Crystals	Miscellaneous
R-141	R-106	E-59
Thesis--MULTIPLE CHANNEL SWITCHING, D.R. Brown.	R-111	E-76
		E-81
Thesis--HIGH SPEED PULSE RECORDING IN MAGNETIC TAPE, E. Rich, May 20, 1948.		E-92.
		E-103

$\int_0^{\pi} f x \, dx \rightarrow \sum$ P(0) 40





SEVENTH DAY

R. Mayer Block Diagrams

Reading: M-64* MATHEMATICAL PROBLEMS OF HIGH-SPEED DIGITAL COMPUTATION, W.S. Loud.
M-66* HIGH-SPEED DIGITAL-COMPUTER CIRCUITS, D.R. Brown.
M-69 DIGITAL COMPUTER BLOCK DIAGRAMS, R.R. Everett.
R-127 WWI COMPUTER BLOCK DIAGRAMS, R.R. Everett & F.E. Swain.

*Read over lightly only

EIGHTH DAY

R. Rathbone Test Equipment

Reading: R-143 SPECIFICATIONS FOR STANDARD TEST EQUIPMENT
R-78 STANDARD TEST EQUIPMENT PROGRAM
R-145, R-171 REGISTER PANEL
E-121 GATE AND DELAY UNIT
R-144 VARIABLE-FREQUENCY CLOCK-PULSE GENERATOR
R-146, M-440 CODER
E-126 SCOPE SYNCHRONIZER
R-147 PULSE STANDARDIZER
R-159 PULSE MIXER
R-164 VIDEO AMPLIFIER & CATHODE FOLLOWER PROBE
E-303 VOLTAGE CALIBRATOR
E-293 EVALUATION OF STANDARD TEST EQUIPMENT
R-182 NEW DEVELOPMENTS IN PULSE CIRCUIT TEST EQUIPMENT
R-161 WWI TEST CONTROL

NINTH DAY

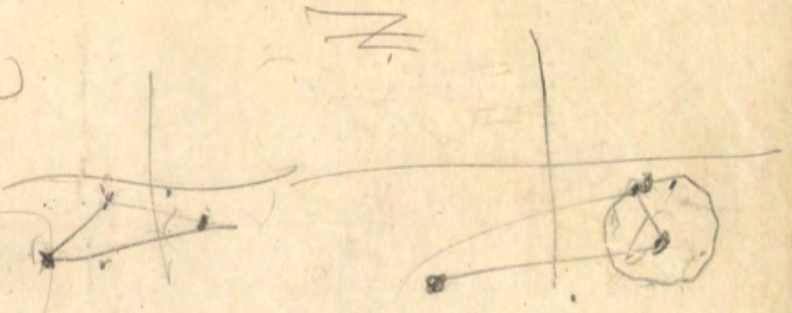
C.W. Adams Mathematics

Reading: M-160 MATHEMATICAL WORK OF PROJECT WHIRLWIND
M-61 DISCUSSION OF NUMERICAL FUNCTIONS
M-176 METHODS OF NUMERICAL INTEGRATION OF ORDINARY DIFFERENTIAL EQUATIONS
C-50 to C-57 RUNGE-KUTTA METHOD OF NUMERICAL INTEGRATION
C-60 RUNGE-KUTTA METHOD FOR SOLVING ORDINARY DIFFERENTIAL EQUATIONS AND ITS VARIATIONS
C-99 RUNGE-KUTTA METHOD APPLIED TO A SIMPLIFIED PROBLEM

Signed J.C. Proctor
J.C. Proctor

JCP:nkh

$\frac{r_1}{r_2}$ const



$$w = \frac{az+b}{cz+d}$$

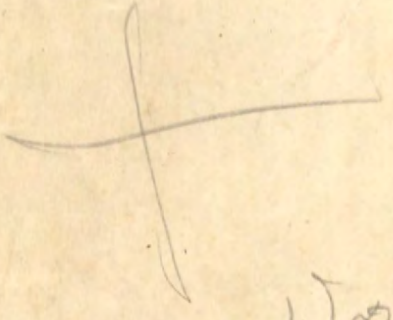
$$w_\infty = \frac{z_\infty - z_0}{z - z_\infty}$$

$w = f(z)$

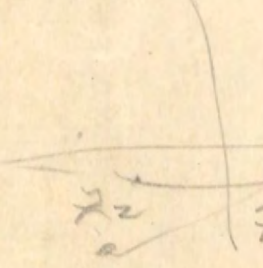
$z = f(w)$

$w_\infty = w_\otimes$

$z_1 = f(w_1)$



$$\frac{w_\infty - w_1}{w_2 - w_1} = \frac{z_\infty - z_2}{z_\infty - z_1}$$



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Best

6345
Memorandum M-1129

R. L. Best

November 20, 1950

MASTER'S THESIS PROPOSAL

TITLE: A Direct-Coupled Amplifier for Magnetically Deflecting an Oscillograph Tube.

BRIEF STATEMENT OF THE PROBLEM:

The problem is to design and build an amplifier to drive the deflection yoke of a K1048-P7 tube, which is a 16 inch magnetically deflected oscillograph tube, having a 54 degree total deflection angle. Desired rise time of current in the yoke is 10 microseconds, with 5% linearity, and 1% stability. The input signal will be the output of a digital-to-analogue converter in the range between 0 and -1.5 volts. Since the signal will be arbitrary and non-repeating, the entire amplifier must be direct coupled.

HISTORY OF THE PROBLEM UP TO THE PRESENT TIME:

The problem arises from the need for a display oscilloscope for general use in the Whirlwind computer. One display that this system should handle involves showing a series of points at random positions, each point to be intensified approximately once every 15 seconds. This call for a long persistance phosphor, P7 having been selected. One of the digital-to-analog decoders that will feed

information to this unit is non-holding; that is, it holds the information fed to it for only a fixed amount of time, after which it clears itself. Since it is desired to use this same decoder for displaying solutions that may come at a much higher repetition rate, the intensification time must be as short as possible, and still be able to get 15 second persistance. Dumont recommends a 1000-microsecond intensification time for 15-30 seconds persistance with a 10-inch electrostatic tube; tests here with a Dumont 304-H oscilloscope indicate that an intensification time of 100 microseconds will suffice, with some sacrifice in spot size. A magnetically focused and deflected tube, however, would be able to give the required persistance with a 10-microsecond intensification time, since very high beam currents are possible with this construction.

The Radar Lab of the Air Force Cambridge Research Lab was consulted at this point, and they agreed to make a deflection yoke for this project, suitable for any of the standard magnetically deflected tubes that have a 54 degree or less total deflection angle.

Their estimated figures were 12 millihenries inductance, and 150 milliamps for full deflection from center to edge (or from edge to edge if two coils in push-pull are used). To make an approximation of how much time it might take to establish deflection, the following equation is useful:

$$\frac{di}{dt} = \frac{V}{L}$$

Substituting sample values of V = 400 volts, which would be an easily obtainable drop across the coil from a 500 volt supply, which is available, and L = 12 mh, di/dt = 42 m.a./usec. The coil resistance will be the order of 100 ohms, and 150 m.a. would cause only 15 volts drop across it. This is small enough compared to the 400 volts applied for this approximation to neglect it. According to this it should theoretically take 150 ÷ 42 = 3.6 microseconds to establish deflection. Push-pull deflection drive will be used, in order to force the current to change as rapidly as possible in either direction. Estimating 10 microseconds to establish stable deflection, and 10 more to intensify, leaves a 20-microsecond interval to work with. This is the maximum consecutive amount of time that Whirlwind can conveniently allow, the way the controls now are; therefore, one specification on the amplifier shall be that it shall establish deflection in 10 microseconds.

Considering the uses to which the display scope will be put, a 5% linearity and 1% stability will be adequate. It is desirable to use pentodes in the output stage, to take advantage of their higher gain and plate resistance, both of which will be an advantage in forcing large current changes through an inductance. The linearity requirement makes some type of feedback necessary; feedback is also indicated from the speed requirement, to shorten the coil's effective time constant. The deflection yoke has not as yet been received, so it is not known what the coupling between the pair of coils is. If this coupling is

tight, the feedback amplifier may be counted on to damp any oscillations better than if the coupling is loose, particularly if they are driven by a class AB stage. Damping resistors may need to be added. Any feedback used must have a d-c path in it -- this makes it awkward to measure coil current by means of the drop across a resistor in series with the coil, which will be at a d-c level of the order of +500 volts. A more convenient method would be to insert cathode resistors in the output tubes, and use the drop across them as a measure of total load current. Non-linearities introduced by screen current will be small enough so that it will still be possible to meet the 5% linearity desired, since the total screen current is only of the order of 5-10% of the plate current in most good pentodes, when the plate voltage is higher than the screen voltage. Only during a transient is the plate voltage apt to be lower than the screen voltage, but the plate voltage will always be high as the point of stability is reached.

A cathode resistor in an output tube gives a voltage proportional to the total load current, the total load consisting of the coil in parallel with shunt capacitance, and possibly some shunt resistance for damping. It is desirable to obtain a voltage for feedback use which is only proportional to coil current. This may be done by inserting in the feedback path a network which is the dual of the coil network. Thus, the feedback amplifier generates the waveform needed to make the coil current change to its new value as rapidly as possible.

The problem of phase inversion arises in a push-pull amplifier such as this, and it is complicated by the feedback question. One way would be to phase invert at low signal level, near the input, and trust that the small signals used would allow this to be done linearly. Once the two-out-of-phase signals are obtained, each is fed to a single-ended amplifier, each amplifier driving one set of deflection coils, and each amplifier being stabilized in itself. Such a method necessarily restricts both amplifiers to be class A in operation. In order to guard against either output stage being cut off at maximum deflection, the total current drawn by the two output amplifiers would be a minimum of about 160 m.a., assuming a differential current of 150 m.a. for full deflection. The dissipation resulting from 500 volts and 0.16 amps is 80 watts for the pair of output tubes, again assuming negligible coil resistance. That considerable wattage could be reduced somewhat if the output stage could be arranged to be class AB. Class AB could be realized if a single feedback signal could be obtained that would be proportional to the difference of the coil currents. This can be accomplished by the following method: Two signals are obtained by the method described in the preceding paragraph, which would be proportional to the deflection coil currents. One of these is fed to a phase inverter, the output of which is mixed in a resistor mixer with the other one. The resultant is a voltage proportional to the difference of the plate currents, and is a single-ended signal that may be compared

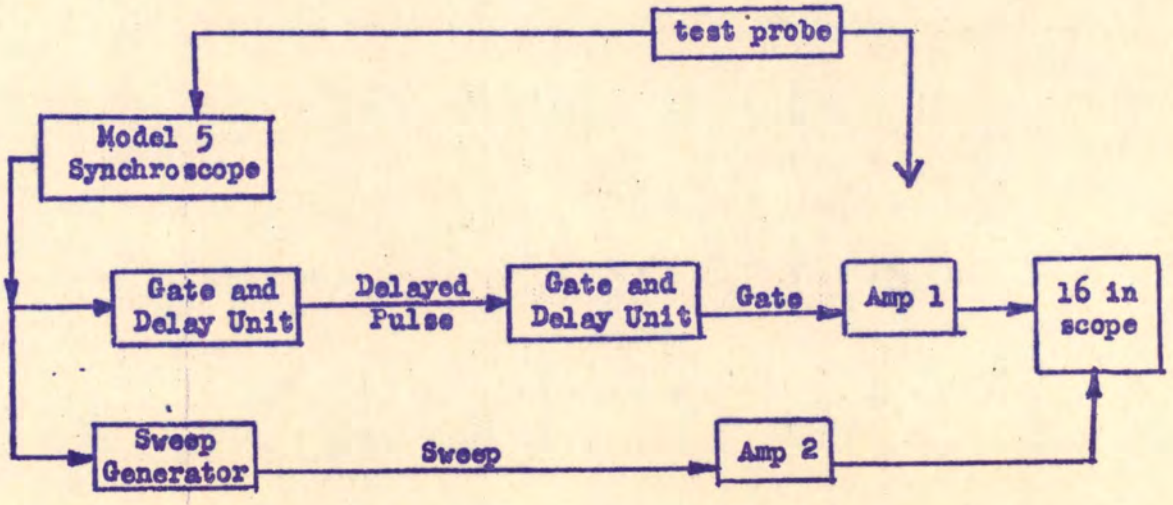
with the single-ended input signal. A phase inverter feeds the pair of output tubes, and class AB operation may be realized. There will be considerably less dissipation for any but full deflection conditions, and the most important quantity is being directly stabilized; the differential coil current.

Following, then, is the proposed solution: The output stage will be push-pull, using pentodes. Cathode resistors in each half of this stage will generate voltages proportional to their respective plate currents. These voltages will be fed to networks which are the dual of the coil networks, their output being voltages proportional to the actual deflection currents. One of these voltages will be inverted and mixed with the other voltage, the resultant being proportional to the difference of the plate currents, and being used as a feedback signal to compare with the input voltage. When more than three stages are closed in a loop, it is very difficult to prevent oscillations at frequencies where the feedback becomes in phase -- to avoid this, it probably will be necessary to precede the above amplifier with a pre-amplifier, to boost the incoming voltage from a swing of 1.5 volts to something larger, of the order of 15 to 30 volts. The pre-amplifier may be also stabilized with feedback, and probably will contain the gain and centering controls. All of the above will be for one co-ordinate of deflection only; and must be duplicated for the other co-ordinate.

PROPOSED PROCEDURE:

Equipment Needs

The accompanying block diagram indicates the needed equipment, and the probable method of connection. The Model 5 Synchroscope and the two Gate and Delay Units are readily available from project Whirlwind, where the work is to be done. The Sweep Generator will be built especially for this thesis, and can be quite simple, since a sweep of only 1.5 volts amplitude is required. It would only be used in the later stages of testing, after any major troubles are remedied in the amplifiers. Amplifiers 1 and 2 are to be identical, and are the subject of this thesis. This block diagram shows a gate being fed to one amplifier, and a sweep to the other, so that the transient response of amplifier 1 may be observed on the 16 inch cathode ray tube. A sweep calibrator is available so that data may be taken from the observed deflections of amplifier 1, and re-plotted on a real time base, if necessary. Other equipment such as voltmeters, soldering irons, power supplies, etc., and also technician help are readily available from Whirlwind.



Probable Procedure

The first step will be to draw up a circuit for the Sweep Generator described above, and to give it to the shop for construction. In that way, it won't be the cause of any delay later. The 16 inch cathode ray tube and a high voltage power supply to be used with it have been ordered. The deflection yoke is completed, and will be delivered to us shortly; the other test equipment has already been assembled.

The next step is to arrive at an amplifier design, following the general procedure outlined in the last paragraph of the section on history, above. An analysis of the resulting circuit will be made to determine its stability and gain, and therewith perhaps to modify the design somewhat.

A circuit will be given to the shop for construction before the previous step is complete, even though the above mentioned analysis may bring about some changes, merely to avoid being delayed, waiting for it all to be built later.

One completed amplifier at a time will be tested with the deflection yoke on the 16 inch tube, observing waveforms with the aid of the Model 5 Synchroscope. When satisfactory operation appears to have been achieved, the system shown in the block diagram on page 7 will be connected. Final testing of the system may then be carried out, with a sweep being applied to the horizontal amplifier, and a gate to

the vertical amplifier, to observe the transient response of the system. The function of the two amplifiers may easily be interchanged for a final check.

ESTIMATED DIVISION OF TIME:

Preparation of proposal	60 hours
Further study of the literature	30 hours
Experimental work and analysis	140 hours
Correlation of results and formulations of deduction and conclusions	50 hours
Preparation of thesis report	80 hours
Total	360 hours

SIGNATURE AND DATE:

Richard L. Best

Richard L. Best
November 20, 1950

SUPERVISION AGREEMENT:

This problem appears adequate for a Master's research, and the undersigned is willing to supervise the research and evaluate the thesis.

C. R. Wieser

C. R. Wieser

Approved:

T. S. Gray

T. S. Gray
Associate Prof. of E.E.

RLB:ks

K. H. Olsen
September 21, 1951

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

1. TITLE: A MULTI-POSITION MAGNETIC SWITCH AND ITS INCORPORATION INTO A MAGNETIC MEMORY

2. BRIEF STATEMENT OF THE PROBLEM

Considerable research has been carried on with core materials suitable for a multi-dimensional magnetic memory. However, in its present development the memory is expensive because of the complex method of switching with a crystal matrix and driving with hard tubes. It is herein proposed that a magnetic switch will significantly simplify the memory unit. The switch may have many other uses such as selecting recording heads on a magnetic drum or a tape recorder. It might also be used in many places where relays are now used such as decoding "flexowriter" tape where it could drive the typewriter keys directly. Techniques developed might be used to build arithmetic tables, so that arithmetic operations with binary numbers could be carried out almost instantly.

3. BRIEF HISTORY OF THE PROBLEM

The practical application of a magnetic core as a "gating" device dates back to the use of a large saturable reactor as the antenna-keying switch on one of the early radio-transmitting alternators as developed by E. F. W. Alexanderson in the late 1900's.[1] Since then

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1. E. F. W. Alexanderson, "Transatlantic Radio Communication", Trans. A.I.E.E., Vol. 38, p. 1269, 1919.

saturable reactors have been used in many similar applications. Recently their use as high-speed low-power gates has been partially investigated by laboratories interested in their application to digital-computer circuits.[1,2]

The idea of storing digital information in a magnetic-core array of two or more dimensions was first proposed in 1949 by J. W. Forrester, Director of the Digital Computer Laboratory at M.I.T.[3] At that time the most serious problem was the lack of a core material with a sufficiently rectangular hysteresis loop that could be switched fast enough to be of use in a high-speed computer. Intensive research has been carried out and a master's thesis written on this subject by W. N. Papian.[4] Although considerable improvement is expected in the future, core materials are now available which can be incorporated into a memory. Of particular interest are the ceramic cores which can be switched in a fraction of a micro-second.

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1. Harvard University Computation Laboratory, Progress Report 5 (Summer of 1949), Investigations for Design of Digital Calculating Machinery.

2. James G. Miles, "Saturable Core Reactors as Digital Computer Elements". A Report of the Engineering Research Associates. Contract NObsr 42001, 17 June, 1949.

3. J. W. Forrester, "Digital Information in Three Dimensions Using Magnetic Cores," Project Whirlwind, Report R-187, (May 16, 1951), M.I.T. Servomechanisms Laboratory.

4. W. N. Papian, "A Coincident-Current Magnetic Memory Unit," Project Whirlwind, Report R-192, (September 8, 1950), M.I.T. Servomechanisms Laboratory.

The problem to be considered in this thesis will be divided into two parts: the development of a suitable switch and the incorporation of the switch into a working memory.

Because the switch is an integral part of the memory and because the mode of operation of the memory with the switch will be different from that originally proposed, the second part of the problem will be a large part of the thesis. It is difficult to realize now what problems will be found when such a large number of interacting elements are tightly coupled together.

4. DESCRIPTION OF SWITCH

The magnetic switch is very much like the crystal matrix switch which is now in common use particularly in digital computers. One of 2^n output terminals can be selected by n inputs, each operating a flip-flop or a two-position switch. In the crystal matrix switch this selecting is done by arranging crystals from the flip-flop outputs to the switch terminals in a binary scheme so that all but one terminal is drawn negative (Fig. 1). The terminal not drawn negative is the one selected by the binary number set up in the flip-flops.

The equivalent magnetic switch (Fig. 2) has a core or a saturable transformer for each switch terminal. On each core there are n control windings connected to the flip-flops as the crystals were in the crystal switch. The output of one flip-flop is enough to saturate a core so with this connection all but one core will be saturated.

Each core also has an output winding and an input winding as in a transformer. All the input windings are driven in series but only the unsaturated core will pass a signal to the output winding. This signal can be a square wave as will be used in the memory or a sine wave for power switching.

5. DESCRIPTION OF MEMORY UNIT

The memory will be made up of an array of small cores or rings of a magnetic material which has a rectangular hysteresis loop. When the residual magnetization of a core is in one direction the core is said to be holding a ONE, and when in the other direction it is said to hold a ZERO. The contents of a core is "read out" by driving current through a winding on the core in such a way as to drive the core to the ZERO position. If the core is already in the ZERO position there will be very little change in flux, but if the core is in the ONE position there will be a large change in flux and a voltage will be induced in a sensing winding on the core. The information in a core is of course destroyed and it has to be "rewritten."

Each core in the array has one winding in series with a line from each of two or more co-ordinates (see Fig.3). In the original scheme, a selected core is switched from one position to another when a measured current is applied to each of the windings of that core so that the sum is enough to switch the core. Many other cores also have current in one winding, but this is not enough to switch them. This

nessitates carefully regulated current sources and very rectangular hysteresis loops. However, when the array is driven from the magnetic switch, a considerably greater current can be used in each line because every non-selected core is kept from switching by the saturated switch core it sees on the other co-ordinate or co-ordinates. Eliminating the necessity of many critically adjusted current sources simplifies the problem significantly, and the increased current will speed up the switching.

6. PROPOSED PROCEDURE

A 16x16 memory array of ceramic cores using the magnetic switch will be built and the problems investigated. Study will be made of the reliability of the system and the deterioration of the information in a single core as information is read out of and written into neighboring cores. Provision will be made in the equipment to display the output of the cores as an array of spots on an oscilloscope.

Every time the core is cycled about the hysteresis loop an amount of energy equal to the area of the hysteresis loop is dissipated in the core. The frequency at which cores can be switched will be limited by the temperature rise in the core due to this and other losses. Apparatus will be built to switch several test cores for a long period of time to investigate this problem.

7. EQUIPMENT NEEDS

Equipment for the proposed system for testing the complete memory (Fig. 4) is under construction or readily available at the Digital Computer Laboratory.

Cores have been already ordered for the 16x16 array, and more are procurable as needed.

8. ESTIMATED DIVISION OF TIME

a.	Preparation of Proposal	40 hours
b.	Experimental Work and Analysis	240 hours
c.	Correlation of Results and Formulation of Deductions and Conclusions	40 hours
d.	Preparation of Thesis Report	80 hours
e.	TOTAL	400 hours

9. SIGNATURE AND DATE

Kenneth H. Olsen
Kenneth H. Olsen,
September 21, 1951

10. SUPERVISION AGREEMENT

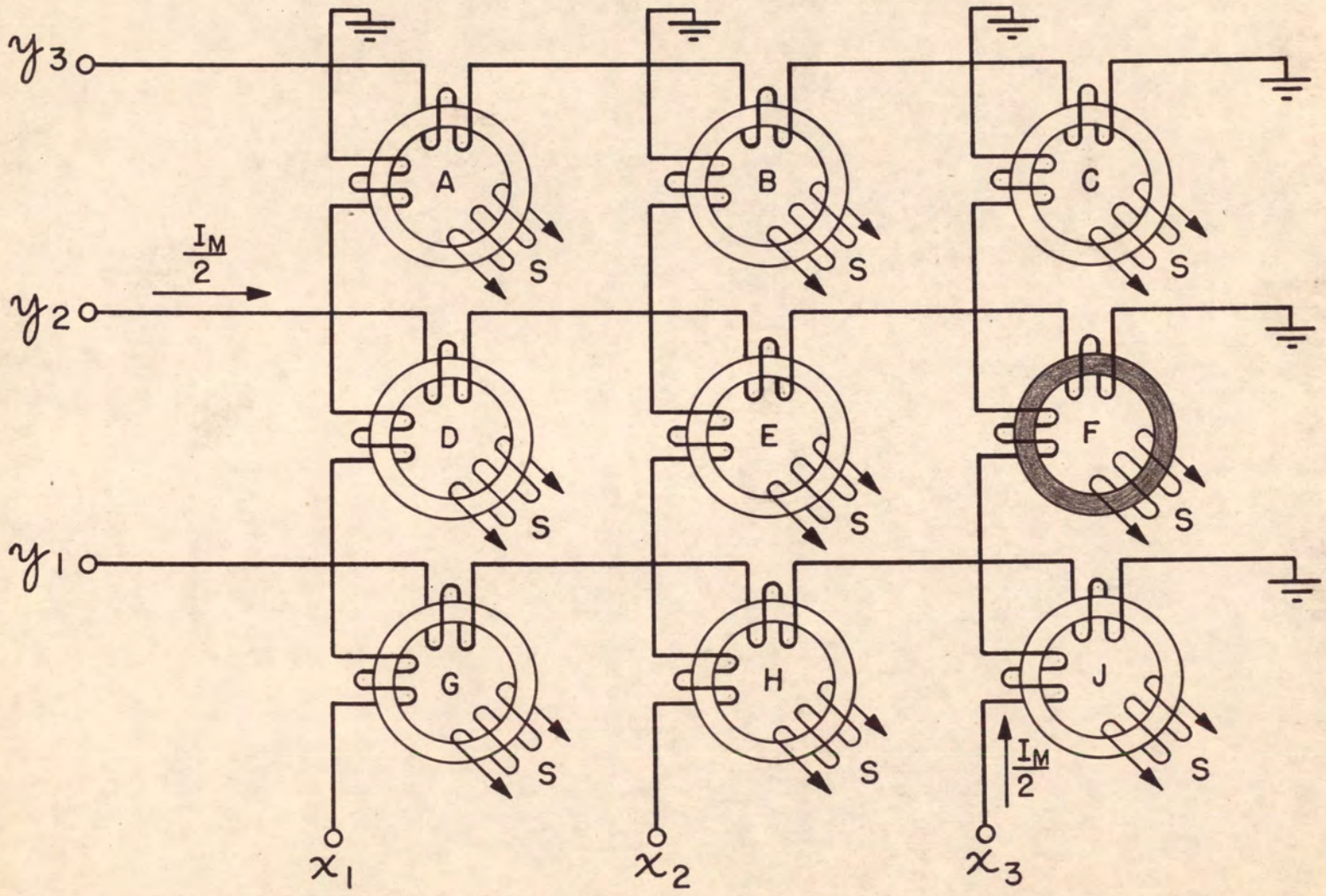
The problem described here seems adequate for a Master's research. The undersigned agrees to supervise the research and evaluate the thesis.

Robert R. Everett

KHO:kst

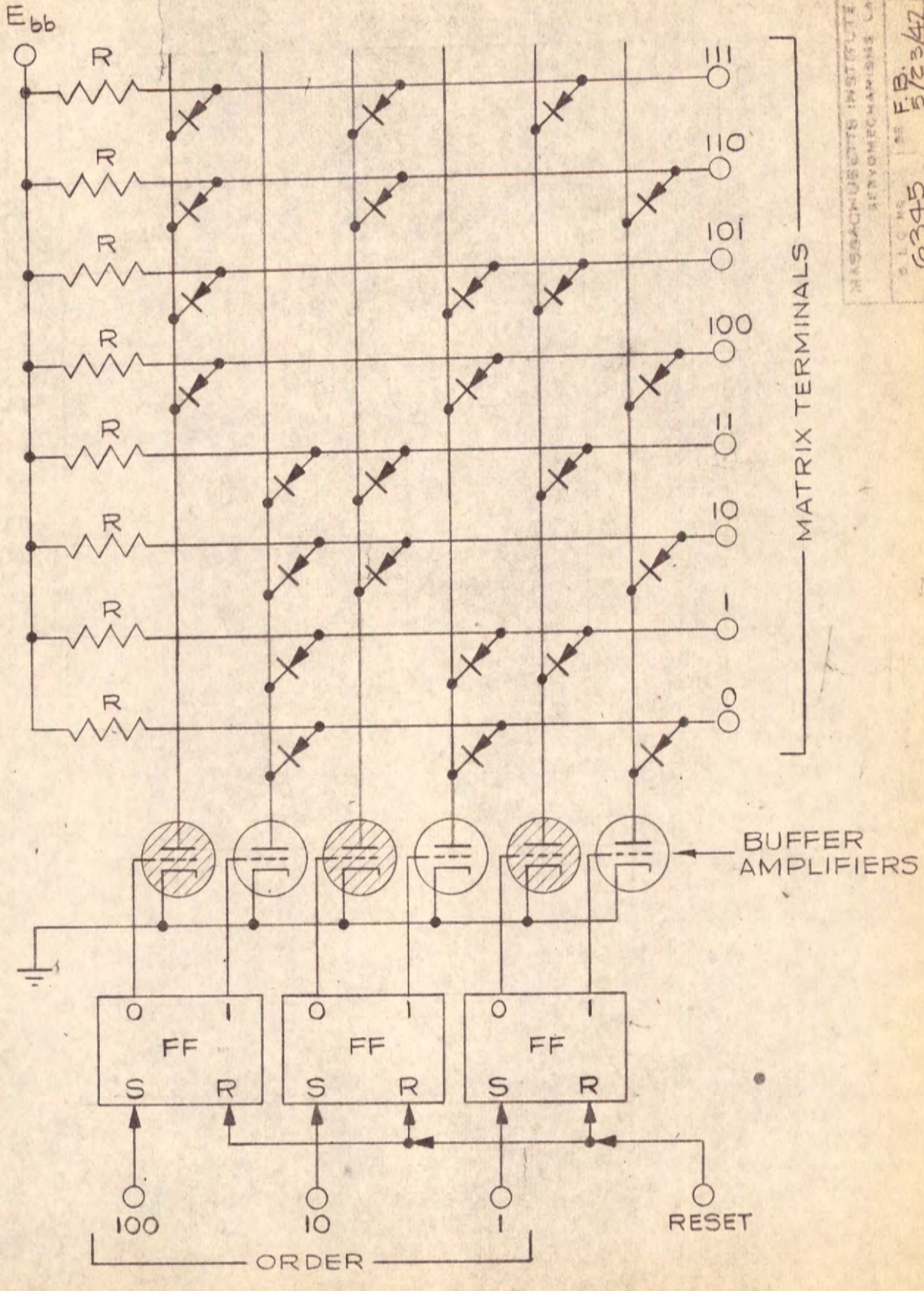
Drawings Attached:

A-30527	Figure 1
SA-50348	Figure 2
A-36656	Figure 3
SB-50349	Figure 4



A TWO-DIMENSIONAL ARRAY OF CORES

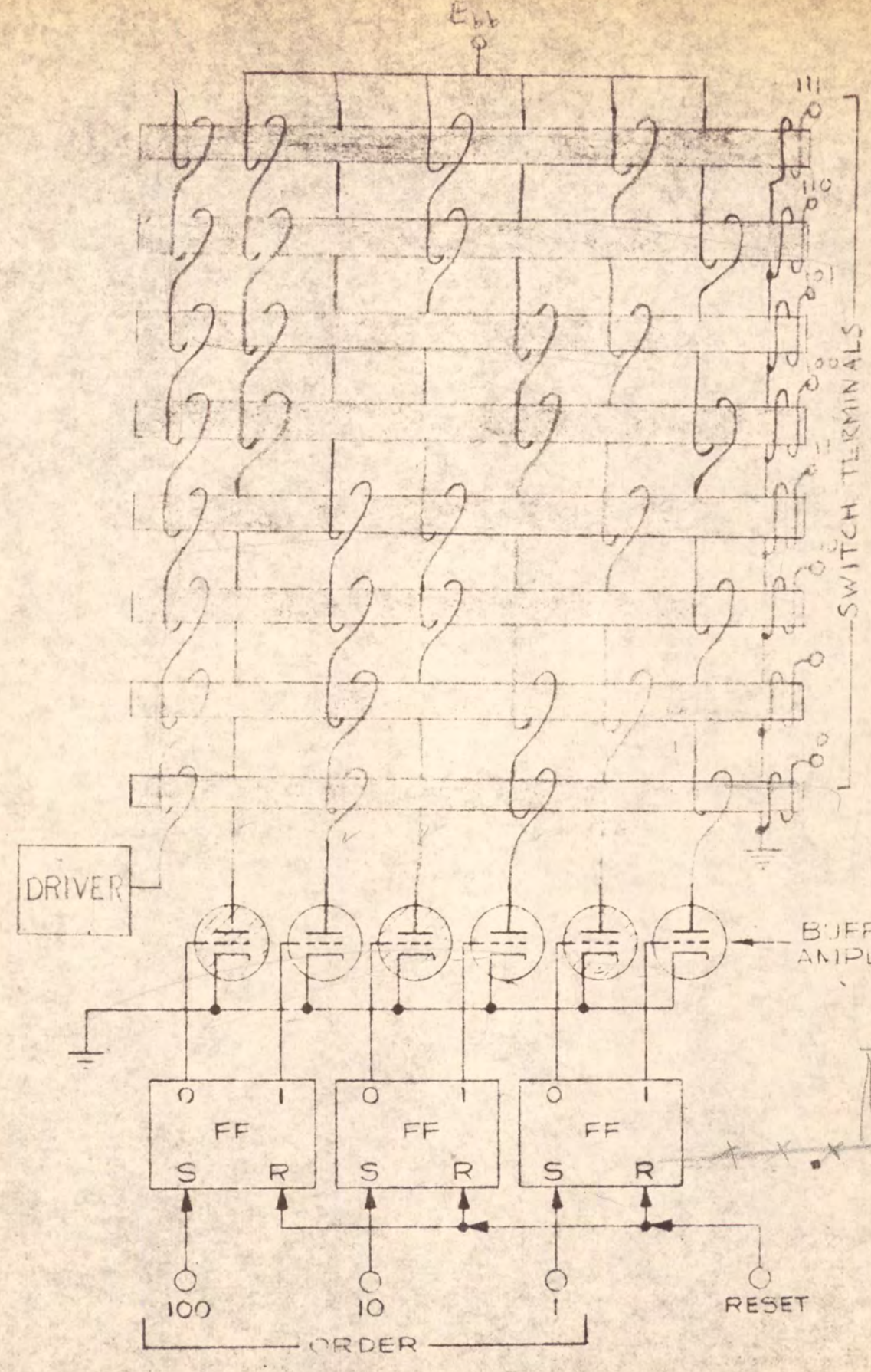
FIG. 8



CRYSTAL-MATRIX SWITCH REDRAWN

FIG. 1

A-30527



8-POSITION MAGNETIC SWITCH

FIG. 2

SB-50349

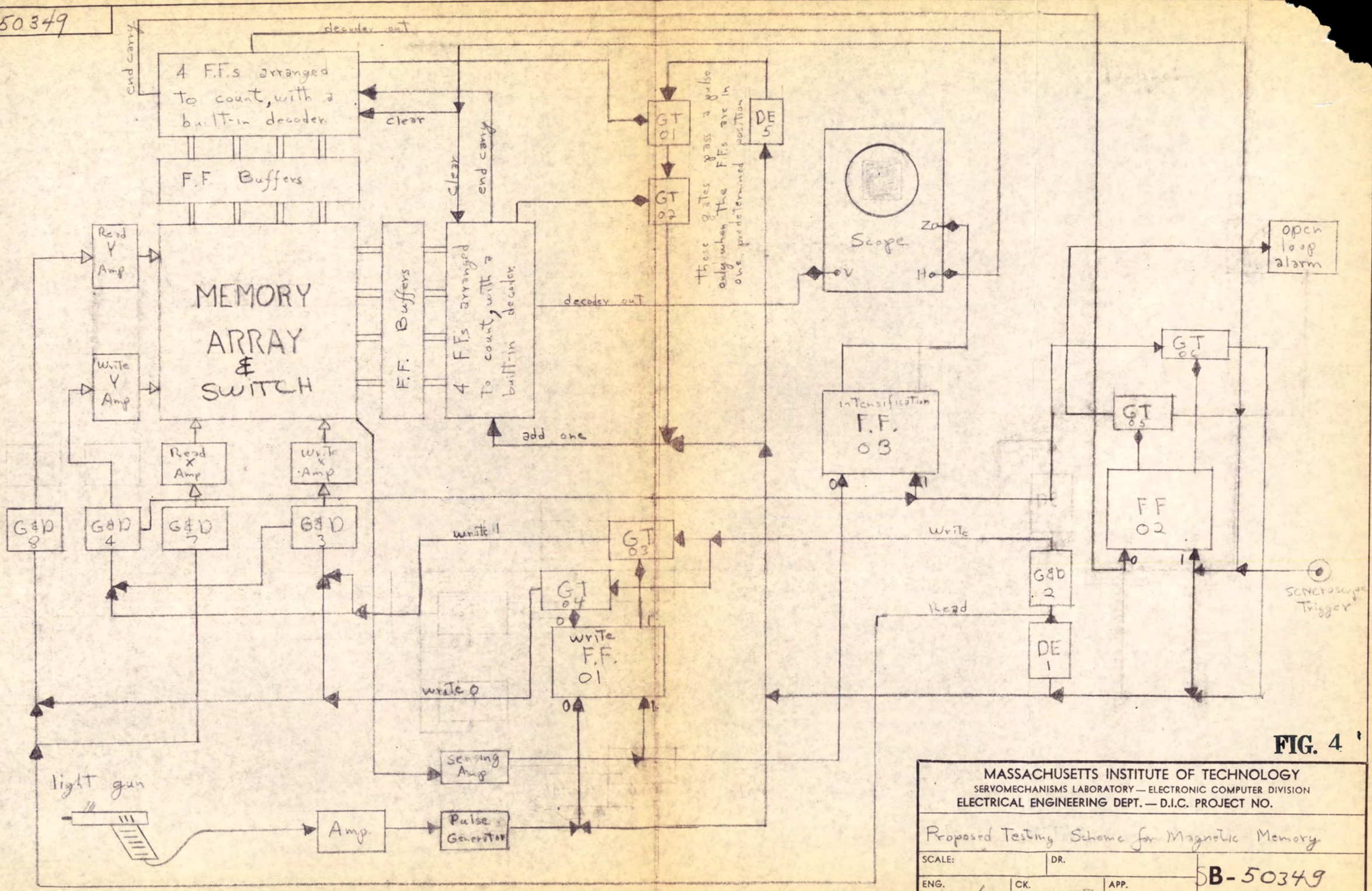


FIG. 4

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY — ELECTRONIC COMPUTER DIVISION
ELECTRICAL ENGINEERING DEPT. — D.I.C. PROJECT NO.

Proposed Testing Scheme for Magnetic Memory

SCALE:	DR.	SB-50349
ENG. K. Olsen	CK. Sept 20 1951	APP.

R. Best

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: INTERNAL DOCUMENTS ON FERROMAGNETIC AND FERROELECTRIC CORES

To: Group 62 and 63 Staff

From: Jean C. Kresser

Date: January 18, 1952, Revised June 1, 1953

Abstract: A list of Reports, Engineering Notes, and Memoranda on various aspects of the ferromagnetic-core and ferroelectric-slab activity is presented.

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** Classified Memorandum

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M-2160	Energy Dissipation in Square-Loop Ferromagnetic Materials with Specific Application to Switch Cores	5-12-53	N. Menyuk
M-2162	WWII Address Selection Systems P.B. No. 61	5-6-53	J. L. Mitchell
M-2167	First-Order Cancellation Residue in Rectangular Memory Arrays	5-15-53	D. A. Buck
M-2186	Two Methods of Reducing Delta Noise	5-22-53	S. Fine
M-2195	Further Work on Nondestructive Read System	5-27-53	W. I. Frank
M-2197	Read-Out and Digit Plane Driving Systems P.B. No. 62	5-28-53	W. J. Canty S. Fine

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Collections

Group 63 Seminar on Magnetism		A. Loeb N. Menyuk

Memoranda covering Lectures I to L and Appendices I to VII have been released to date.

Signed Jean C. Kresser
Jean C. Kresser

Approved DRB
David R. Brown

Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

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E-548	Preliminary Report -- Temperature Effects in MTC-Type Ferrite Cores	6-26-53	J. D. Childress
E-559	A Free Energy Model for the Hysteresis Loop	6-16-53	A. L. Loeb

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M-2240	A Magnetic Core Test Storage	6-15-53	K. Olsen
M-2248	Tests of Some Magnetic-Matrix Switch Operating Modes	6-17-53	J. L. Mitchell R. S. DiNolfo
M-2254	Sensing the Slope of Magnetic Memory Output	6-19-53	K. Olsen
M-2275	Equation of Motion for a Cylindrical 180° Domain Wall	7-30-53	P. Baltzer
M-2291	Proposal for Reducing the Number of Tubes Used in Driving a Magnetic Matrix Switch	7-9-53	J. Raffel
M-2314	Readout-Noise Reduction in a Magnetic-Core Memory	7-23-53	S. Fine
M-2316	Proposed Sense Winding for a 64 x 64 Memory Plane	7-23-53	W. Canty
M-2319	Procedure for Handling Cores During Testing Program	7-23-53	J. Schallerer

	Title	Date	Author
Memoranda (continued)			
*M-2332	West Coast Trip, July, 1953	7-31-53	D. A. Buck
M-2348	Switch-Core Design and Power Loss	8-7-53	J. Raffel
M-2383	Testing the Magnetic-Core Memory System in a Computer	9-18-53	B. Widro
M-2384	A Large Planar Switch for Register Selection in a Magnetic-Core Memory (M.S. Thesis Proposal)	8-31-53	J. Raffel
M-2398	Trip to Linde Corp., Tonawanda, N. Y., 8-17-53, to Discuss Growth and Procurement of Ferrite Single Crystals	9-8-53	D. A. Buck
M-2412	An Analytical Review of Neél's Molecular Field Theory of Ferri- and Ferromagnetism	9-16-53	A. L. Loeb
M-2420	Interpretation of Memory-Core Specifications	9-22-53	D. R. Brown
M-2442	Ferrite Synthesis	9-15-53	F. E. Vinal
M-2473	B-H Loop Squareness in the Magnesium-Manganese	10-22-53	J. B. Goodenough
M-2514	The Incorporation of a Magnetic Matrix Switch into a Multiplanar Coincident-Current Magnetic Memory (M.S. Thesis Proposal)	11-12-53	A. D. Hughes
M-2568	Pulse Response of Ferrite Memory Cores	12-15-53	J. R. Freeman
M-2598	Transformer Drive for a Coincident-Current Magnetic Memory (M.S. Thesis Proposal)	1-5-54	E. K. Gates
M-2602	Stress Effects in Ferrites and Generalization of Switching Coefficient for Non-Square Materials	1-6-54	N. Menyuk
M-2629	Trip Report to Bell Labs., Murray Hill, New Jersey, January 6, 1954	1-14-54	J. B. Goodenough
M-2634	Multi-Coordinate Selection Systems for Magnetic-Core Storage	1-19-53	R. DiNolfo

	Title	Date	Author
Memoranda (continued)			
M-2649	Graphical Summary of Core Data in the $MgO-Fe_2O_3-MnO$ System	1-25-54	J. B. Goodenough
M-2674	A Comparison Between Square-Loop Metals and Ferrites for High-Speed Pulsed Operation	2-4-54	D. R. Brown D. A. Buck N. Menyuk
M-2692	Ferrite Synthesis, II	2-11-54	F. E. Vinal
M-2736	Core Memory Using External Bit Selection	3-18-54	J. Raffel

Title	Date	Author

Collections

Group 63 Seminar on Magnetism — A. L. Loeb, N. Menyuk

Memoranda covering the Introduction and Lectures I to LV and Appendices I to VII have been released for the academic year 1952-53.

Memorandum covering Lecture I of Vol. 2 has been released to date.

Signed Jean C. Kresser
Jean C. Kresser

Approved DRB
David R. Brown

K. H. Olsen
B-063

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: DOCUMENTS ON MAGNETIC CORE WORK

To: Group 63 Staff

From: Joan M. Sullivan

Date: July 16, 1956

Approved: William N. Papian

Abstract: A partial list of Reports, Theses, Engineering Notes, Articles, and Memoranda on various aspects of the magnetic-core activity is presented.

	Title	Date	Author
Reports			
6R-187	Digital Information Storage in Three Dimensions Using Magnetic Cores	5-16-50	J. W. Forrester
6R-192	A Coincident-Current Magnetic Memory Unit (S.M. Thesis)	9-8-50	W. N. Papian
6R-211	A Magnetic Matrix Switch and Its Incorporation Into a Coincident-Current Memory (S.M. Thesis)	6-6-52	K. H. Olsen
6R-216	The 16-by-16 Metallic-Core Memory Array Model I	9-25-52	B. Widrow
6R-217	Design of Low-Power Pulse Transformers Using Ferrite Cores (S.M. Thesis)	8-29-52	R. D. Robinson
6R-234	Switch for Register Selection in a Magnetic Core Memory (S.M. Thesis)	5-24-54	J. I. Raffel
6R-235	Multi-Coordinate Selection Systems for Magnetic-Core Storage (S.M. Thesis)	8-23-54	R. S. DiNolfo

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

	Title	Date	Author
Reports	(continued)		
6R-236	Magnetostriction in Ferrites Possessing a Square Hysteresis Loop (S.M. Thesis)	1-17-55	P. K. Baltzer

	Title	Date	Author
Theses	(not in report form)		
	A Magnetic Flip-Flop	5-16-52	R. J. Pfaff
	An Investigation of Magnetic Core Stepping Registers for Digital Computers	8-22-52	R. C. Sims
	Rectangular Hysteresis Loop Materials in a Nondestructive Read System	5-25-53	W. I. Frank
	An RF Readout System for a Coincident-Current Magnetic-Core Memory	5-25-53	B. Widrow
	High-Speed Magnetic Pulse Control Circuits for Computer Applications	5-25-53	H. K. Rising
	Magnetic Amplifiers with High Carrier Frequency	5-25-53	A. L. Pugh, III
	A Study of Single-Pulse Ferrite-Core Stepping Registers	8-31-53	J. B. Ricketts, Jr.
	Temperature Behavior of Ferrites	1-18-54	L. F. Silva
	A Differential Thermal Analysis Study of Synthesized Magnesium Ferrite, Manganese Ferrite, and Magnesium-Manganese Ferrite	1-18-54	R. A. Maglio
	A Carry-Matrix Counter	5-24-54	G. Lampke
	Transformer Drive for a Coincident-Current Magnetic Memory	8-23-54	E. K. Gates
	Magnetic Drum Writing Circuits Using Magnetic Cores	8-23-54	H. Henegar
	The Incorporation of a Magnetic Matrix Switch into a Multiplanar Coincident-Current Magnetic Memory	8-23-54	A. Hughes
	A Magnetic-Core Memory with External Selection	1-17-55	S. Bradspies

	Title	Date	Author
Theses	(continued)		
	A Transistorized Amplifier-Discriminator for Core Memory Output	5-23-55	F. W. Sarles, Jr.
	A Transistor Selection System for A Magnetic-Core Memory	1-56	G. A. Davidson
	The Application of Transistors to Multiposition Selection Switches	5-24-56	P. G. Griffith
	A Magnetic-Core Test Storage	6-19-56	J. N. Ackley

	Title	Date	Author
Engineering Notes			
6E-406	Preliminary Tests on the Four-Core Magnetic Memory Array	6-18-51	W. N. Papian
6E-413	Selection Systems for Magnetic-Core Storage	8-7-51	R. R. Everett
6E-422	Rectangular-Loop Magnetic Core Materials	9-4-51	W. N. Papian
6E-438	Binary Counting with Magnetic Cores	12-6-51	D. A. Buck
6E-454-1	Nondestructive Sensing of Magnetic Cores	3-24-53	D. A. Buck
6E-464	A Squareness Ratio for Coincident-Current Memory Cores	7-16-52	D. R. Brown
6E-470	Paper on Ferromagnetic and Ferroelectric Memory Devices	8-6-52	W. N. Papian
6E-472	The Mirror: A Proposed Simplified Symbol for Magnetic Circuits	8-14-52	R. P. Mayer
6E-475	A Magnetic-Core Gate and Its Application in a Stepping Register	10-30-52	G. R. Briggs
6E-477	Magnetic and Dielectric Amplifiers	8-28-52	D. A. Buck
6E-488	$Delta_{ns}$ in Ceramic Array #1	10-14-52	E. A. Guditz
6E-491	Hysteresis Loop Characteristics of MF-1118 for Different Temperatures	10-16-52	C. Morrison
6E-495	Test Procedure for Ferrite Pulse Transformers, I	11-5-52	E. K. Gates
6E-496	Instructions and Specifications for the Manufacture of 3:1 and 1:1, 0.1 Microsecond Pulse Transformers on Ferrite-Ring Cores	11-3-52	R. E. Hunt
6E-500	Switch Core Analysis I	11-4-52	A. Katz E. A. Guditz
6E-512	A Method for Acceptance Testing of Ferrite Core Production Lots	12-4-52	P. K. Baltzer

	Title	Date	Author
Engineering Notes (continued)			
6E-518	New Metallic Cores from Magnetic Metals	1-2-53	A. D. Hughes
6E-519	General Ceramics Materials MF-1348B and MF-1359B	1-5-53	B. Smulowicz
6E-523	Core Drivers--Model V and VI	2-10-53	H. Boyd
6E-529	Matrix Driving with Unidirectional Pulses	2-25-53	D. A. Buck
6E-530	Magnetic Materials for High-Speed Pulse Circuits	2-27-53	D. R. Brown
6E-531	Driving Current Margins on Memory Test Setup I	3-6-53	S. Fine
6E-532	Nucleation of Domains of Reverse Magnetization & Switching Characteristics of Magnetic Materials	3-9-53	J. B. Goodenough N. Menyuk
6E-533	Effect of Current Pulse Duration on the Pulse Response of MTC Memory Cores	3-10-53	P. K. Baltzer
6E-539	An Approach to a Rationale in Ferrite Synthesis: Evaluation of Magnetic Moments	4-28-53	L. Gold
6E-540	A Fast-Core Tube Register	4-27-53	K. H. Olsen R. Pfaff
6E-544	Circuit for Measuring Switch Time, Rise Time, etc., (Switch-Time Comparator)	5-11-53	B. Gurley
6E-545	Dependence of Coercivity and Stress Hysteresis on Nucleation of Domains of Reverse Magnetization	5-14-53	J. B. Goodenough
6E-548	Preliminary Report--Temperature Effects in MTC-type Ferrite Cores	6-26-53	J. D. Childress
6E-559	A Free Energy Model for the Hysteresis Loop	6-16-53	A. L. Loeb

	Title	Date	Author
Engineering Notes (continued)			
6E-563	Specifications for a Ferrite Memory Core	6-30-53	D. R. Brown

Note: This series discontinued under date of July 28, 1954.

	Title	Date	Author
Memoranda			
6M-1371	Magnetic Core Activity	1-15-52	W. N. Papian
6M-1381	Magnetic-Core Memory Matrix Analysis (Effect of Driver Impedance)	1-24-52	D. A. Buck
6M-1490	Procedure for Receiving Magnetic Cores	5-16-52	D. R. Brown
6M-1529	Conference on Magnetic Core Switching Phenomena	6-16-52	A. Katz
6M-1582	High-Speed Magnetic Pulse Control Circuits for Computers (Thesis Proposal)	8-6-52	H. K. Rising
6M-1650	The Effect of Size of Metal Cores on Pulse and Hysteresis Measurements	9-25-52	R. F. Jenney
6M-1664	Conference on Thin Evaporated Metal Films	10-6-52	A. L. Loeb
6M-1676	Polishing Specimens of Ferrites	10-14-52	F. E. Vinal
6M-1681	Uniformity Tests on Ferrite Cores	10-21-52	J. H. McCusker
6M-1741	Metallographic Studies of Ferrites	12-4-52	D. R. Brown
6M-1767	An RF Readout System for a Coincident-Current Magnetic-Core Memory (Thesis Proposal)	12-19-52	B. Widrow
6M-1785	Testing of Magnetic Cores	1-7-53	A. D. Hughes
6M-1806	Pulse Tests of the RCA Victor Ferrite, XF-96	1-22-53	B. Smulowicz
6M-1811	Coordinate Conversion with Memory-Core Matrix	1-27-53	D. McCann
6M-1830	MF-1326-B, F-291, Life Test No. 1--Initial Tests	2-6-53	J. R. Freeman
6M-1883	Magnetic-Core Matrix Switch Adder	3-9-53	C. J. Schultz
6M-1893	Hysteresis Test Results from Five New Glenco Ferroelectric Materials	3-10-53	C. D. Morrison

	Title	Date	Author
Memoranda	(continued)		
6M-1929	AD HOC Conference on $FeNi_3$	3-25-53	D. A. Buck J. B. Goodenough A. L. Loeb N. Menyuk
6M-1943	Testing Cores for WWII	3-30-53	J. McCusker
6M-1957	Procedure for Preparing and Stripping Wires for MTC Memory Planes	4-6-53	E. A. Guditz
6M-1987	First Note on Pulse Transformers for Memory Drivers	5-27-53	F. Durgin E. K. Gates
6M-1989	MF-1326-B, F-291, Life Test No. 2	4-21-53	J. R. Freeman
6M-2110	A Linear Selection Magnetic Memory Using an Anti-Coincident Current Switch	5-8-53	K. H. Olsen
6M-2160	Energy Dissipation in Square-Loop Ferromagnetic Materials with Specific Application to Switch Cores	5-12-53	N. Menyuk
6M-2162	WWI Address Selection Systems, P.B. No. 61	5-6-53	J. L. Mitchell
6M-2167	First-Order Cancellation Residue in Rectangular Memory Arrays	5-15-53	D. A. Buck
6M-2186	Two Methods of Reducing Delta Noise	5-22-53	S. Fine
6M-2195	Further Work on Nondestructive Read System	5-27-53	W. I. Frank
6M-2197	Read-Out and Digit Plane Driving Systems, P.B. No. 62	5-28-53	W. J. Canty S. Fine
6M-2219	Testing of Individual Cores in MTC Memory Planes	6-16-53	A. D. Hughes
6M-2225	The Construction of Memory Planes for the MTC Memory	6-10-53	E. A. Guditz
6M-2240	A Magnetic Core Test Storage	6-15-53	K. Olsen

	Title	Date	Author
Memoranda (continued)			
6M-2248	Tests of Some Magnetic-Matrix Switch Operating Modes	6-17-53	J. L. Mitchell R. S. DiNolfo
6M-2254	Sensing the Slope of Magnetic Memory Output	6-19-53	K. H. Olsen
6M-2275	Equation of Motion for a Cylindrical 180° Domain Wall	7-30-53	P. K. Baltzer
6M-2291	Proposal for Reducing the Number of Tubes Used in Driving a Magnetic Matrix Switch	7-9-53	J. I. Raffel
6M-2314	Readout-Noise Reduction in a Magnetic-Core Memory	7-23-53	S. Fine
6M-2316	Proposed Sense Winding for a 64 x 64 Memory Plane	7-23-53	W. J. Canty
6M-2319	Procedure for Handling Cores During Testing Program	7-23-53	W. J. Schallerer
6M-2348	Switch-Core Design and Power Loss	8-7-53	J. I. Raffel
6M-2351	Sensing Winding Geometry	8-6-53	J. I. Raffel S. Bradspies
6M-2383	Testing the Magnetic-Core Memory System in a Computer	9-18-53	B. Widrow
6M-2384	A Large Planar Switch for Register Selection in a Magnetic-Core Memory (Thesis Proposal)	8-31-53	J. I. Raffel
6M-2412	An Analytical Review of Néel's Molecular Field Theory of Ferri- and Ferromagnetism	9-16-53	A. L. Loeb
6M-2420	Interpretation of Memory-Core Specifications	9-22-53	D. R. Brown
6M-2442	Ferrite Synthesis	9-15-53	F. E. Vinal
6M-2473	B-H Loop Squareness in the Magnesium-Manganese Ferrites	10-22-53	J. B. Goodenough

	Title	Date	Author
Memoranda	(continued)		
6M-2474	A Theory of Ionic Ordering, Tetragonal-Phase Formation, Magnetic Exchange, and Lamellar Precipitation Due to Covalent Forces in Spinels	5-7-54	J. B. Goodenough A. L. Loeb
6M-2514	The Incorporation of a Magnetic Matrix Switch into a Multiplanar Coincident-Current Magnetic Memory (Thesis Proposal)	11-12-53	A. D. Hughes
6M-2568-1	Pulse Response of Ferrite Memory Cores	9-20-54	J. R. Freeman
6M-2598	Transformer Drive for a Coincident-Current Magnetic Memory (Thesis Proposal)	1-5-54	E. K. Gates
6M-2602	Stress Effects in Ferrites and Generalization of Switching Coefficient for Non-Square Materials	1-6-54	N. Menyuk
6M-2634	Multi-Coordinate Selection Systems for Magnetic-Core Storage	1-19-54	R. S. DiNolfo
6M-2649	Graphical Summary of Core Data in the $MgO-Fe_2O_3-MnO$ System	1-25-54	J. B. Goodenough
6M-2674	A Comparison Between Square-Loop Metals and Ferrites for High-Speed Pulsed Operation	2-4-54	D. R. Brown D. A. Buck N. Menyuk
6M-2692	Ferrite Synthesis, II	2-11-54	F. E. Vinal
6M-2736	Core Memory Using External Bit Selection	3-18-54	J. I. Raffel
6M-2755	Core Drivers--Model V and Model VI Applications, Limitations, and Modifications	5-1-54	J. D. Childress
6M-2762	A Magnetic-Core Memory with External Selection (Thesis Proposal)	4-6-54	S. Bradspies

	Title	Date	Author
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6M-2803	Magnetic-Core Shift Register Evaluator	5-3-54	C. J. Schultz
6M-2804	Effects of Tape Thickness and Temperature on Flux Reversal of 4-79 Molybdenum Permalloy	5-3-54	N. Menyuk
6M-2839	One One or the Other	5-28-54	R. P. Mayer W. N. Papian
6M-2840	Test Results on the DCL Memory Plane	5-28-54	E. A. Guditz
6M-2873	Basis for Release of Ferrite Memory Core Specifications	6-17-54	D. R. Brown
6M-2880	Evaluation of Ferroxcube Cores	6-28-54	P. A. Fergus
6M-2919	Sensing Winding Geometry and Information Patterns	7-22-54	J. I. Raffel
6M-2943	X-Ray Equipment for Magnetic Research	7-29-54	D. Tuomi F. E. Vinal
6M-2945	Current Calibrator (Chopper Model)	8-10-54	J. D. Childress
6M-2969	Tentative Cathode Estimates for 256^2 x 33 and 128^2 x 33 Core Memories	8-6-54	W. J. Canty J. L. Mitchell
6M-3005	Bondeze Magnetic Wire for Memory Plane Construction	8-27-54	A. Bowen E. A. Guditz
6M-3035	An Investigation of Some Parameters which Influence the Magnetic Characteristics of Ferrites	9-20-54	P. K. Baltzer
6M-3059	Thoughts on Incremental Permeability	9-17-54	J. B. Goodenough
6M-3097	Description of Memory Test Setup IV	10-11-54	E. A. Guditz
6M-3107	High-Speed Core Driver	10-21-54	S. Bradspies
6M-3185	A Theory of Pervoskite-Type Manganites (La,M(II), MnO_3)	11-30-54	J. B. Goodenough

	Title	Date	Author
Memoranda	(continued)		
6M-3215	Conference on Ferrimagnetism	11-12-54	J. B. Goodenough P. K. Baltzer F. E. Vinal
6M-3252	Paramagnetic Behavior of Ferrites Containing two Kinds of Magnetic Ions	1-17-55	N. Menyuk
6M-3316	Transistor Circuits for Driving Coincident-Current Memories	1-21-55	K. H. Olsen
6M-3390	Memory Plane Margins: DCL-2-720 Cores vs S-1 Cores	2-21-55	J. L. Mitchell
6M-3417	A Transistorized Amplifier Discriminator for Core Memory Output Sensing (Thesis Proposal)	3-7-55	F. W. Sarles, Jr.
6M-3505	Experiments on a Three-Core Cell for High-Speed Memoires	-----	J. I. Raffel S. Bradspies
6M-3526	X-Y Tests on Memory Plane Units	4-11-55	J. W. Schallerer
6M-3530	Improved Memory Cores Produced in Lincoln Laboratory	4-13-55	F. E. Vinal
6M-3654	Procedure for Stripping Wires for 64 x 64 Memory Plane Modules	6-7-55	E. A. Guditz
6M-3699	Specifications for 64^2 Memory Plane Module Frame	6-20-55	E. A. Guditz L. B. Smith
6M-3717	A Transistor Selection System for a Magnetic-Core Memory (Thesis Proposal)	6-27-55	G. A. Davidson
6M-3805	Mod. III Current Calibrator	8-9-55	R. A. Pacl
6M-3820	EMAR: An Experimental Memory Address Register	8-10-55	W. A. Clark
6M-3856	Pulse Transformer Amplifier	9-7-55	M. M. Cerier
6M-4064	Remarks on Domain Patterns Recently Found in BiMn and SiFe Alloys	12-27-55	J. B. Goodenough
6M-4089	Geometry of Magnetic Memory Elements	1-18-56	J. D. Childress

	Title	Date	Author
Memoranda (continued)			
6M-4137	Memory Core Heating by Switching at High Frequencies	1-31-56	J. D. Childress
6M-4153	The Noise Problem in the Coincident-Current Memory Matrix	2-13-56	J. D. Childress
6M-4218	A Sequential-Access Three-Microsecond Core Memory	3-8-56	R. L. Best T. H. Meisling
6M-4298	Proposed Research Program on Thin Film	4-17-56	A. L. Loeb
6M-4328	The Influence of Chemistry on B-H Loop Shape, Coercivity, and Flux-Reversal Time in Ferrites	5-16-56	J. B. Goodenough
6M-4362	Magnetization Reversal in Thin Films	6-4-56	D. O. Smith

Title	Author
Collections	
Group 63 Seminar on Magnetism Memoranda covering the Introduction and Lectures I to LV and Appendices I to VII have been released for the academic year 1952-1953.	A. L. Loeb N. Menyuk
Memorandum covering Lecture I of Vol. 2 has been released. Seminar was discontinued after Lecture I of Vol. 2.	

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Goodenough, John B., and Loeb, Arthur L., "Semicovalence and Anisotropy in Magnetic Oxides," to be presented at October meeting of the American Institute of Electrical Engineers, Boston, Massachusetts, and later published in the Conference Proceedings.

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SUBJECT: MAGNETIC-CORE MEMORY MATRIX ANALYSIS (EFFECT OF DRIVER IMPEDANCE)

To: Kenneth H. Olsen

From: Dudley A. Buck

Date: January 24, 1952

Abstract: The following analysis of a magnetic-core memory shows the extent to which the quiescent internal impedance of the row and column drivers affects the selection ratio.

Consider a square N by N matrix of identical magnetic cores (Fig. 1a). Having selected a row and a column, the matrix can be redrawn (Fig. 1b) as it is seen looking between the selected row and the selected column. One core, the selected core, links the selected row and column. From the selected row one core links each of the (N-1) unused columns and from the selected column one core links each of the (N-1) unused rows. In addition, each of the (N-1) unused rows is linked to each of the (N-1) unused columns (dashed lines).

Whatever the currents in the unused rows, they will, by symmetry, be identical. We can therefore connect them in series for this analysis (Fig. 1c). Similarly, we can connect the unused columns in series.

The final step (Fig. 1d) is to slide together cores which link the same pair of wires giving a composite reduction of the matrix into four cores; core A is the selected core, cores B are the cores lying along the selected row and column but not at the intersection, and C represents all other cores in the matrix. If core A has a cross-sectional area A, cores B each have area (N-1)A and core C has area $(N-1)^2A$.

$$1 + 2(N-1) + (N-1)^2 = N^2$$

let:

H_A = magnetic field acting on core A
H_B = magnetic field acting on cores B
H_C = magnetic field acting on core C
i_1 = current in selected row and column
i_2 = current induced in unused rows and columns
ℓ = mean magnetic path (circumference) of all cores
Single-turn coupling throughout

From Fig. 1d,

$$H_A = \frac{2i_1}{\ell}$$

$$H_B = \frac{i_1 - i_2}{\ell}$$

$$H_C = \frac{2i_2}{\ell}$$

We will now consider two driving condition extremes; the first is one in which the quiescent internal impedance of the row and column drivers is infinite and the second is one in which the quiescent internal impedance of the row and column drivers is zero. We will define the selection ratio as

$$H_A : H_B \text{ if } H_B > H_C$$
$$H_A : H_C \text{ if } H_B < H_C$$

Infinite Quiescent Internal Impedance Row and Column Drivers

In this condition, no induced currents are allowed to flow in the unused rows and columns.

Therefore:

$$i_2 = 0$$

$$H_A = \frac{2i_1}{\ell}$$

$$H_B = \frac{i_1}{\ell}$$

$$H_C = 0$$

In this driving condition, the selection ratio, $H_A : H_B$, is 2:1 regardless of matrix size.

Zero Quiescent Internal Impedance Row and Column Drivers

The current induced in the unused rows and columns, i_2, is due to a voltage produced by flux changes in cores B. This current is limited only by a voltage of opposite polarity produced by flux changes in core C. Since the loop is assumed to have zero impedance, these voltages, and therefore the changes in flux, must be equal.

$$\frac{d\phi_B}{dt} = \frac{d\phi_C}{dt}$$

but:

$$\frac{d\phi_B}{dt} = \mu_B (N-1) A \frac{dH_B}{dt}$$

$$\frac{d\phi_C}{dt} = \mu_C (N-1)^2 A \frac{dH_C}{dt}$$

Assuming $\mu_B = \mu_C$, and equating these two, we have:

$$\frac{dH_B}{dt} = (N-1) \frac{dH_C}{dt}$$

Assume that H_B and H_C both start from zero. At any time, T, then:

$$H_B = (N-1) H_C$$

We see that for any size matrix, $H_B > H_C$, and the selection ratio therefore is $H_A : H_B$

From:

$$H_B = (N-1) H_C$$

$$H_B = \frac{i_1 - i_2}{\ell}$$

$$H_C = \frac{2i_2}{\ell}$$

We can write:

$$\frac{i_1 - i_2}{\ell} = (N-1)\left(\frac{2i_2}{\ell}\right)$$

$$i_1 = (2N-1) i_2$$

And:

$$H_B = \left(\frac{2N-2}{2N-1}\right) \frac{i_1}{\ell}$$

$$H_A = \frac{2i_1}{\ell}$$

And the selection ratio, $H_A : H_B$, equals $\frac{2N-1}{N-1} : 1$

We see that the selection ratio in this driving condition is a function of the matrix size. Tabulated below is $\frac{2N-1}{N-1} : 1$ for several values of N:

N	Selection Ratio $\frac{2N-1}{N-1}$:1
2	3.00:1
3	2.50:1
4	2.33:1
5	2.25:1
6	2.20:1
7	2.16:1
8	2.14:1
16	2.06:1

Summary

For drivers with infinite quiescent internal impedance, the selection ratio is always 2:1. For drivers with zero quiescent internal impedance, the selection ratio is always better than 2:1 and it depends upon the matrix size. It can be as high as 3:1 for a 2 by 2 matrix but it drops off rapidly as the matrix size increases. For a 16 by 16 matrix, the selection ratio varies but 3% as the quiescent internal impedance of the drivers is varied over the entire range from zero to infinity.

SIGNED Dudley A. Buck
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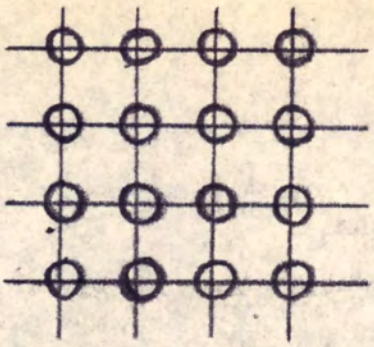
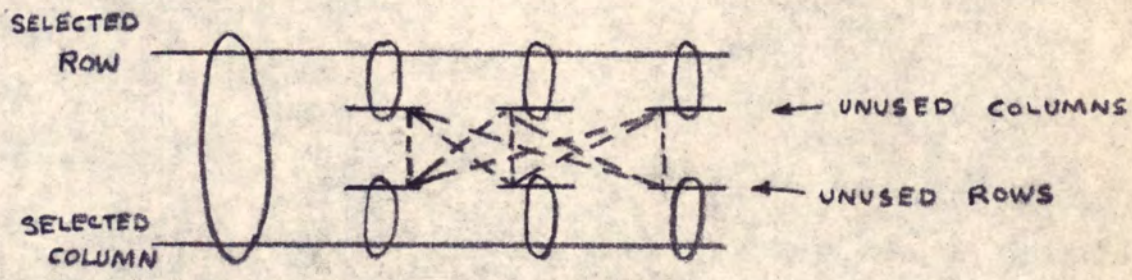
APPROVED WNP
W. N. Papian

DAB/cp

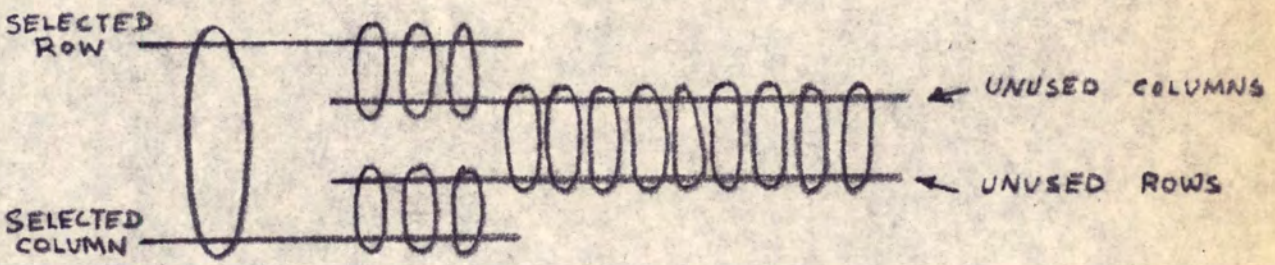
Drawing: SA-50769



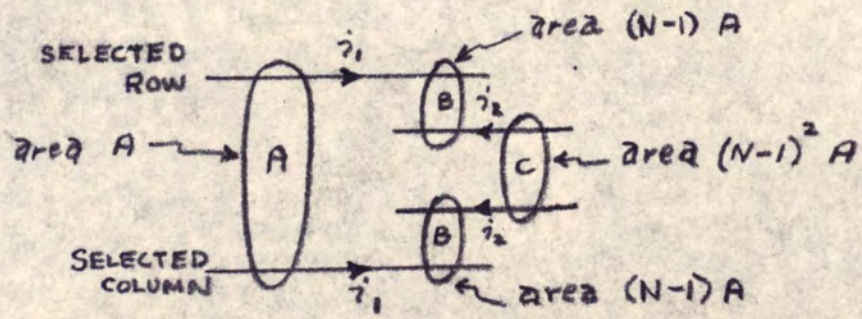
a) N x N MATRIX



b) MATRIX REDRAWN



c) UNUSED ROWS AND COLUMNS JOINED



d) COMPOSITE REDUCTION

FIG. 1. MAGNETIC MATRIX REDUCTION

SA-50769

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: SAMPLE PROBLEMS FOR APPLICANTS FOR EMPLOYMENT

To: C. R. Wieser

From: D. R. Israel

Date: February 11, 1952

The following are some problems which might be used in determining whether an applicant is interested and suited for the type of work done in the Applications Group of Project 6889.

Problem 1. Assume that you are offered two jobs. Job A has a salary of $1200 a year with an annual raise of $200. Job B starts with a semi-annual salary of $600 and has a semi-annual raise of $50. Which job would you choose?

Problem 2. Assume that you have been given a set of 64 cards. On one side of each card is written a number between 0 and 1000. The cards are then put into numerical sequence and are laid out in a row, face down. On one of these cards the number 230 has been written. The job at hand is to find this card, but in doing this only the minimum number of cards must be turned face up. What is the minimum number of cards which must be turned face up before you can guarantee to find the desired card? Can you generalize your answer in the case where there are n cards?

Problem 3. Assume that you have a rectangular surface measuring 90" x 33". We wish to cover this surface completely using rectangular pieces of paper 9" x 5". What number of these pieces of paper will

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

be needed to cover the surface, and how much paper, if any, must be wasted in cutting these pieces of paper so that the area covered it exactly 90" x 33" and no papers are overlapped? If a piece of paper is cut in several pieces, only one of the pieces may be used.

Problem 4. The rate of climb of a jet aircraft decreases with altitude. Assume that this variation is linear and that the rate of climb at sea level is 8,000 ft. per minute, while at 50,000 ft. it is 1,000 ft. per minute. Derive a formula which will enable you to determine the time that it will take the aircraft to reach any altitude up to 50,000 ft. If the performance figures given above are accurate to only about 10%, can the required expression, giving time as a function of altitude, be replaced by a simple approximation if the maximum altitude in which we are interested is limited to 20,000 ft.? If there is such a suitable approximation, can you estimate its approximate error at 20,000 ft.?

Problem 5. Assume that you are asked to consider the problem of directing and aiming anti-aircraft guns on a naval vessel. The naval vessel will be maneuvering and will be firing at maneuvering aircraft. What are the important factors and pieces of information about which knowledge would be necessary in considering the computational aspects of the problem?

Problem 6. The sequence of numbers, 0, 1, 2, 5, 6, 7, 0, 1, 2, 5, 6, 7, ... is generated by the expression $x_{n+1} = (x_n^2 + 1)_{\text{mod } 10}$. Given the sequence of numbers 1,3,7,5,1,3,7,5,.....1,3,7,5,.....can you derive an equation for generating this sequence? Can you do the same for the following sequence: 2,3,7,43,1807,.....?

Problem 7. Assume that Figure 1 below represents a network of cross streets. The section shown is six blocks by six blocks. The blocks are all of equal length, L. What is the length of the shortest path(s) between a and b?

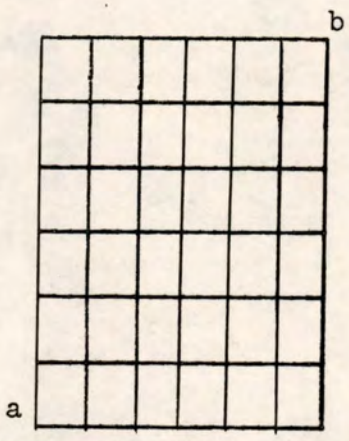


Figure 1

In Figure 1 assume that motion to the right is indicated as +H, motion to the left as -H; motion up as +V, motion down as -V. With this notation, any path between a and b can be specified as a sequence of H's and V's with appropriate algebraic signs. For example, the path +H,+H,+H,+H,+H,+H,+V,+V,+V,+V,+V,+V specifies the path from a to b going around the outside of the network horizontally to the right and then up. Assume that a number of these paths are available on paper or have been punched out on cards or paper tape. It is then desired to use a machine to pick out the shortest path(s) between a and b. Among the properties which it is possible to give this machine are those of addition, subtraction, multiplication, division, or the recognition of a negative number. Of the above properties, which should the machine have? (Assume that there is at least one path of length 12L.

In Figure 2 how many different (distinct) paths are there between a and b? Any one path must not retrace any section of itself.

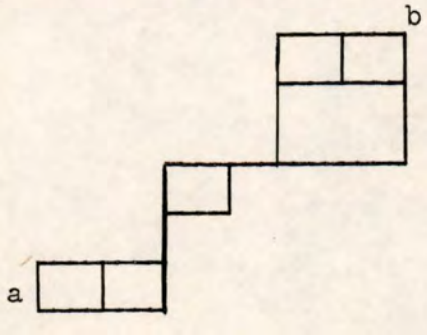


Figure 2

Problem 8. Assume that you are given a list of 100 angles. The angles are all positive and are measured in degrees between 0° and 360°, but the angles are not listed in any special numerical order. It is desired to find all those consecutive pairs of angles in this list which have an angular separation whose magnitude is less than 5°. Assume that this is to be done by a machine whose arithmetic capabilities consist of addition, subtraction, the taking of magnitudes, and the determination of positive and negative results. No comparison is desired between the first and the last (hundredth) angle. Write the necessary expression(s) using the angles θ_i and θ_{i+1} and only the machine capabilities mentioned above. As an example, if we wished to find whether angle θ_{i+1} were arithmetically greater than angle θ_i, we would form the expression:

$$p = \theta_{i+1} - \theta_i$$

If p were positive, θ_{i+1} would be greater than θ_i; if p were negative, θ_{i+1} would be smaller than θ_i. For purposes of the problem at hand, we can consider a zero difference as being positive.

Problem 9. Assume that a computing machine were to be used to operate the traffic lights in a metropolis so as to expedite the flow of traffic; that is, depending upon the results of its computation or other activity, the computer will be able to turn any traffic light in the city either red or green. Make a list of the different types of information which you would need in studying this problem, and also a list of the information which would be needed by the computer in carrying out the problem. Discuss the means whereby this latter information might be gathered; that is, from what sources.

Problem 10. On the next two pages are given flow diagrams for forming the expression

$$ax^3 + bx^2 + cx + d$$

Each line in these flow diagrams represents a single operation, either that of multiplication, addition, or the saving of an intermediate result for later use. Flow Diagram A and Flow Diagram B form the expression

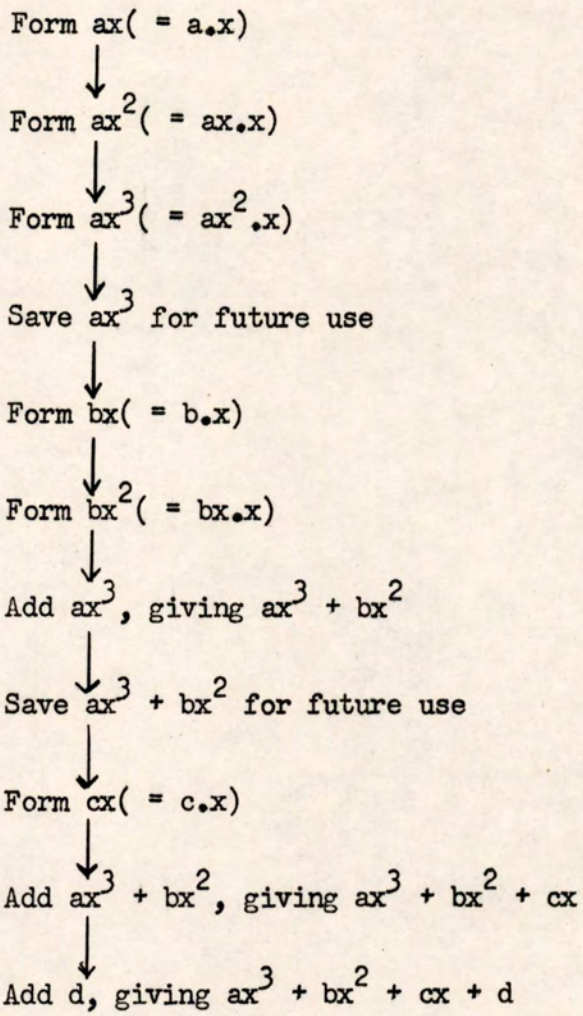
$$ax^3 + bx^2 + cx + d$$

in two different ways; Flow Diagram A requires 11 steps while B requires 9 steps. Draw a third flow diagram for forming the same function but requiring fewer steps. (Each step requires a single computer operation and the fewer the number of steps, the faster the solution of the problem.)

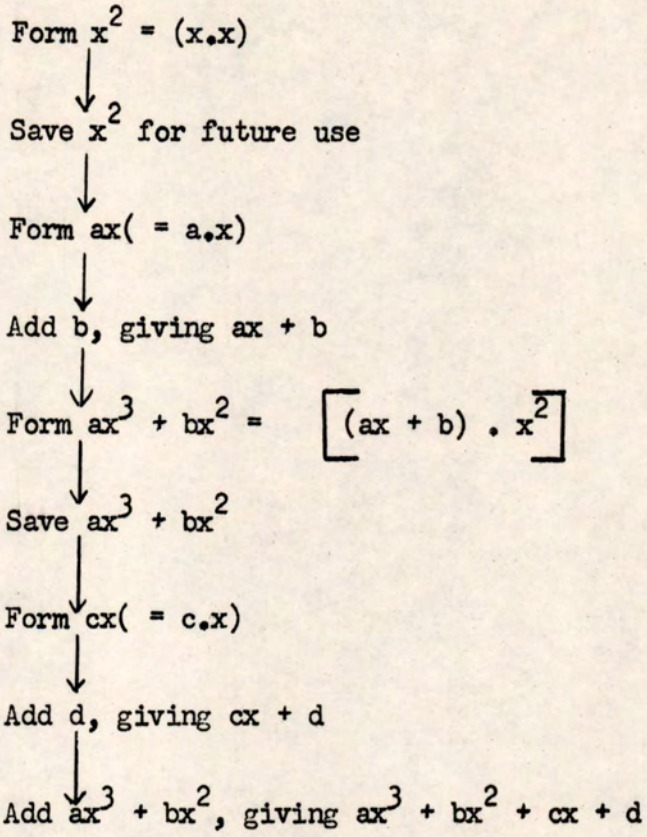
Problem 11. Assume that a different positive number is written on each of three pieces of paper. One of these pieces of paper goes into Box #1, another into Box #2, and a third into Box #3. Assume that a Box #4 is initially empty. On page 9 is a flow diagram for manipulating upon the contents of these boxes. The notation used is as follows:

c(2)	means the contents of Box #2,
$\Longrightarrow$	means place into,
c(2) $\Longrightarrow$ 4	means place the contents of Box #2 into Box #4,
c(4) - c(2)	means subtract the numerical value of the contents of Box #2 from the numerical value of the contents of Box #4.

Flow Diagram A



Flow Diagram B

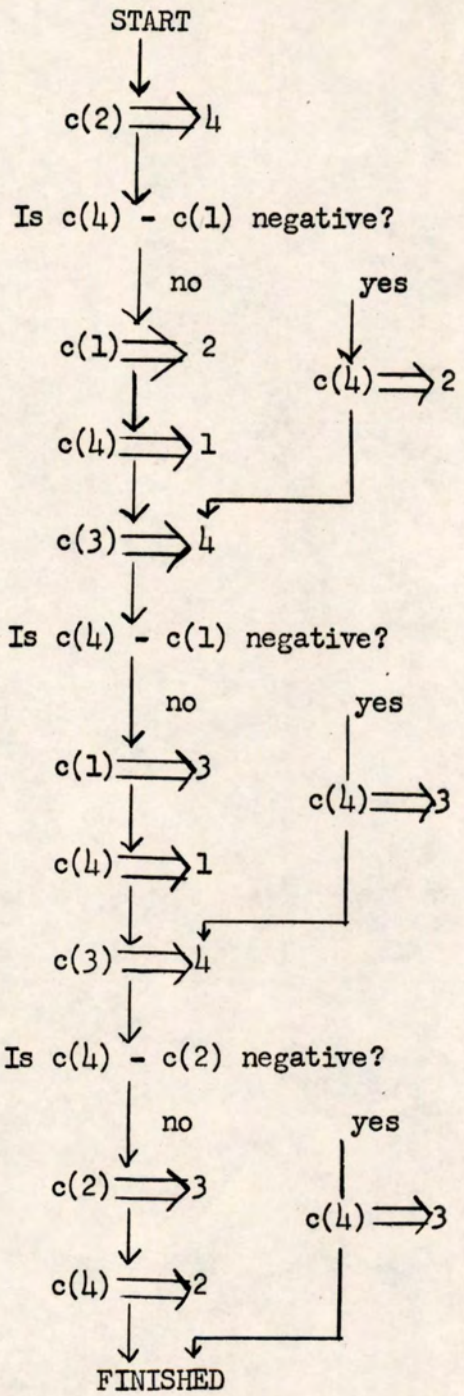


In this problem, assume that a zero resulting from a subtraction is a negative number. After studying the flow diagram, describe the resulting action and the relationship of the numerical value of the final contents of Boxes #1, #2, and #3. Describe what happens if two or more of the papers have the same number.

Signed David R. Israel
David R. Israel

Approved C. R. Wieser
C.R. Wieser

Flow Diagram



Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: STABILIZED TRANSISTOR AS A FOUR TERMINAL NON-LINEAR NETWORK*

To: Transistor Group

From: John F. Jacobs

Date: March 6, 1952

Abstract: This memorandum outlines a method for describing the characteristics of a transistor with base stabilization. The method consists of plotting the linearized emitter and collector characteristics for the stabilized transistor treating the whole unit as a four terminal network. On these linearized characteristics the locus of the points at which the various diodes (emitter, collector, and base) switch is clearly presented. Several experimental checks are made which indicate the closeness of the linear approximation to the actual characteristics.

1.0 The Stabilized Transistor Circuit Element

The circuit shown in Fig. 1 occurs so often in transistor trigger** applications that it is profitable to study it in detail. It differs from the unstabilized transistor in that an external resistance, R_b, a switching diode, r_{bd}, and a biasing network, V_{bs} and R_{bs}, are inserted in the base circuit.

When the large signal equivalent circuit for the transistor*** and a Thevinins equivalent circuit of the base diode and its biasing network are substituted in Fig. 1, the circuit, Fig. 2, results.

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* This memorandum is part of a thesis progress report. See S. M. Thesis Proposal M-1353.

** A trigger circuit is one which is characterized by a negative resistance characteristic and usually exhibits more than one stable state.

*** Alder, Richard B. Large Signal Equivalent Circuit for Transistor Static Characteristics, R.L.E. Transistor Group, August 30, 1951. (Revised October 2, 1951)

Representative magnitudes of the equivalent large signal circuit parameters are given in the Table 1 so that the following derivations can be simplified by dropping insignificant quantities:

Table 1

Parameter	Typical Value (Ohms)
r_{ef}	100
r_{er}	200,000
r_{cf}	80
r_{cr}	20,000
r_{bdf}	100
r_{bdr}	500,000
r_b	200
R_{bs}	10,000 - 30,000
R_b	1000 - 3000
α_e	$\begin{cases} 2.5 & I_e > 0 \\ 0 & I_e < 0 \end{cases}$

1.1 Conditions Under Which the Base Diode Switches

When the base diode is about to switch, the voltage across it and the current through it are both zero. Under this condition

$$I_e + I_c = -\frac{V_{bs}}{R_{bs}} \qquad (1)$$

When: $$I_e + I_c < -\frac{V_{bs}}{R_{bs}} \qquad (2)$$

The base diode must be open because point (a), Fig. 1, is negative with respect to ground.

When: $$I_e + I_c > -\frac{V_{bs}}{R_{bs}} \qquad (3)$$

The base diode is closed because point (a) is positive with respect to ground.

1.2 The Collector Characteristics of the Stabilized Transistor Circuit Element

The stabilized transistor circuit element is treated in this section as one treats a transistor, and the collector characteristic (V_c as a function of I_c with I_e a parameter) is found in the same way.

For the plot of the collector characteristic, the collector loop equation is written*. It is:

$$V_c = I_e (R_b' + \alpha_e r_c) + I_c (R_b' + r_c) + V_b \qquad (4)$$

Where $$R_b' \triangleq r_b + R_b + \frac{r_{bd} R_{bs}}{r_{bd} + R_{bs}}$$

And $$V_b \triangleq V_{bs} \frac{r_{bd}}{r_{bd} + R_{bs}}$$

1.21 Locus of Points at Which the Base Diode Switches

When equation 1 is substituted into equation 4, an expression for V_c as a function of I_c is obtained. This is the locus of the points at which the base diode switches:

$$V_c = I_c r_c (1 - \alpha_e) = \frac{V_{bs}}{R_{bs}} (R_b' + \alpha_e r_c) + V_b \qquad (5)$$

Three distinct regions are apparent when one studies Equation 5. These regions are dependent upon the positions of the base and collector diode. The condition at which the base diode switches is explained above, while the collector diode switches when $I_c = -\alpha_e I_e$.

Region 1: $I_e < 0$; $V_c < 0$.

In this region $\alpha_e = 0$; $r_c = r_{cr}$

---

* For the current generator, $\alpha_e I_e$, and the collector diode, substitute the Thevinins equivalent circuit before writing the loop equations.

Then:

$$V_c = I_c r_{cr} - \frac{V_{bs}}{R_{bs}} (R_b') + V_b$$

Or when one substitutes for R_b' and V_b as defined above:

$$V_c \cong I_c r_{cr} - \frac{V_{bs}}{R_{bs}} (R_b + r_b) \qquad (5a)$$

Note that when $I_e = 0$ the point at which the diode switches is (from Equation 1)

$$I_c = - \frac{V_{bs}}{R_{bs}} \qquad (5b)$$

and substituting 5b in 5a:

$$V_c = - \frac{V_{bs}}{R_{bs}} (R_b + r_b + r_{cr}) \cong - \frac{V_{bs}}{R_{bs}} r_{cr} \qquad (5c)$$

Region 2: $I_e > 0$; $0 > V_c$; $I_c < -\alpha_e I_e$.

In this region:

$\alpha_e > 0$; $r_c = r_{cr}$;

and:

$$V_c = I_c r_{cr} (1 - \alpha_e) - \frac{V_{bs}}{R_{bs}} (R_b + r_b + \alpha_e r_{cr}) \qquad (5d)$$

The value of V_c is also found at the point where the collector diode switches; that is, where:

$$I_c = -\alpha_e I_e \qquad (a)$$

When this equation is substituted into (4) one obtains:

$$V_c = I_c \left[1 - \frac{1}{\alpha_e}\right] \left[R_b'\right] + V_{bs} \frac{r_{bd}}{r_{bd} + R_{bs}} \qquad (b)$$

The point of intersection of (b) with (5d) is:

$$I_c = - \frac{V_{bs}}{R_{bs}} \left[\frac{\alpha_e}{\alpha_e - 1}\right] \qquad (5e)$$

$$V_c = - \frac{V_{bs}}{R_{bs}} (R_b + r_b) \qquad (5f)$$

Region 3: $I_e > 0$; $V_c < 0$; $I_c > - \alpha_e I_e$.

In this region:

$\alpha_e > 0$ and $r_c = r_{cf}$

Then:

$$V_c = I_c r_{cf} (1 - \alpha_e) - \frac{V_{bs}}{R_{bs}} (R_b + r_b + \alpha_e r_{cf}) \qquad (5g)$$

Thus, the locus of the points at which the base diode switches is established by means of the equations 5a, 5d, and 5g, or it can be determined by means of the four check points developed in the text 5b, 5c, 5e, 5f, and the intercepts of 5g and 5a. This locus is sketched in Fig. 3. The four points are numbered 1, 2, 3, and 4. Equations 5b and 5c determine check point 2, and equations 5e and 5f determine point 1. The intercept of 5a determines point 3, while the intercept of 5g determines point 4.

For example: Let the parameter values in Table 1 apply. Let $R_{bs} = 20{,}000$ and $R_b = 1000$. Let $V_{bs} = 20V$. Find the locus of the points at which the base diode switches.

(5a) Intercept $= - \frac{V_{bs}}{R_{bs}} (R_b + r_b) = - \frac{20}{20{,}000} (1200) = - 1.2$ Volts

(5b) $I_c = - \frac{V_{bs}}{R_{bs}} = - \frac{20}{20{,}000} = -1$ Mil

(5c) $V_c = - \frac{V_{bs}}{R_{bs}} (R_b + r_b + r_{cr}) = -10^{-3}(21{,}200) = -21.2$ Volts

(5e) $I_c = - \frac{V_{bs}}{R_{bs}} \times \frac{\alpha_e}{\alpha_e - 1} = -10^{-3} \times \frac{2.5}{1.5} = -1.66$ Mils

(5f) $V_c = - \frac{V_{bs}}{R_{bs}} (R_b + r_b) = -10^{-3} \times 1200 = - 1.2$ Volts

(5g) Intercept $= - \frac{V_{bs}}{R_{bs}} (R_b + r_b + \alpha_e r_{cf}) = -10^{-3} \times 1400 = -1.4$ Volts

1.22 Plot of the Linearized Collector Characteristics

Equation 4,

$$V_c = I_e (R_b' + \alpha_e r_c) + I_c (R_b' + r_c) + V_b \qquad (4)$$

is the equation which is used to plot the collector characteristics. The left half of this current-voltage plane can be divided into 6 regions in each of which one can modify 4 in such a way that the linearized plot is simplified.

Region 1: $I_e < 0$; $V_c < 0$; $I_e + I_c > -\frac{V_{bs}}{R_{bs}}$.

In this region:

$$\alpha_e = 0 \quad ; \quad r_c = r_{cr} \quad ; \quad r_{bd} = r_{bdf}.$$

With simplification by neglecting insignificant terms, Equation 4 becomes:

$$V_c \cong I_e (R_b + r_b + r_{bdf}) + I_c (R_b + r_{cr}) \qquad (4a)$$

Region 2: $I_e > 0$; $V_c < 0$; $I_e + I_c > -\frac{V_{bs}}{R_{bs}}$; $I_c < -\alpha_e I_e$.

In this region:

$$\alpha_e > 0 \quad ; \quad r_c = r_{cr} \quad ; \quad r_{bd} = r_{bdf}.$$

Neglecting insignificant terms, Equation 4 becomes:

$$V_c \cong I_e (\alpha_e r_{cr}) + I_c (R_b + r_{cr}) \qquad (4b)$$

Region 3: $I_e > 0$; $V_c < 0$; $I_c > -\alpha_e I_e$; $I_e + I_c > -\frac{V_{bs}}{R_{bs}}$

In this region:

$$\alpha_e > 0 \quad ; \quad r_c = r_{cf} \quad ; \quad r_{bd} = r_{bdf}.$$

Neglecting insignificant terms, Equation 4 becomes:

$$V_c \cong I_e (R_b + r_b + r_{bdf} + \alpha_e r_{cf}) + I_c (R_b + r_b + r_{bdf} + r_{cf}) \qquad (4c)$$

Region 4: $I_e < 0$; $V_e < 0$; $I_c < -\alpha_e I_e$; $I_e + I_c < -\frac{V_{bs}}{R_{bs}}$.

In this region:

$\alpha_e = 0$; $r_c = r_{cr}$; $r_{bd} = r_{bdr}$.

Neglecting insignificant terms, Equation 4 becomes:

$$V_c \cong I_e (R_{bs} + R_b) + I_c (R_{bs} + r_{cr}) + V_{bs} \qquad (4d)$$

Region 5: $I_e > 0$; $I_c < -\alpha_e I_e$; $I_e + I_c < -\frac{V_{bs}}{R_{bs}}$; $V_c < 0$.

In this region:

$r_c = r_{cr}$; $\alpha_e > 0$; $r_{bd} = r_{bdr}$.

Neglecting insifnificant terms, Equation 4 becomes:

$$V_c = I_e (R_{bs} + \alpha_e r_{cr}) + I_c (R_{bs} + r_{cr}) + V_{bs} \qquad (4e)$$

Region 6: $I_e > 0$; $I_c > -\alpha_e I_e$; $I_e + I_c < -\frac{V_{bs}}{R_{bs}}$; $V_c < 0$.

In this region:

$r_c = r_{cf}$; $\alpha_e > 0$; $r_{bd} = r_{bdr}$.

Neglecting insignificant terms, Equation 4 becomes:

$$V_c = I_e (R_{bs} + R_b) + (R_b + R_{bs}) I_c + V_{bs} \qquad (4f)$$

The diagram, Fig. 4, shows Equation 4 plotted in the six regions. The values of the parameters used in the previous example were used for this plot.

1.23 Experimental Check of the Results Predicted From 1.22

The circuit shown in Fig. 5 was built* and the collector family was determined experimentally. A General Electric G11A and a Bell 1698 were used which have the parameter values shown on

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* John F. Jacobs and Nolan T. Jones, Standardized Transistor Parameter Measurements, E-441, January 3, 1952.

Figures 6 and 7. Figures 6 and 7 show the calculated and experimentally determined characteristics shown on the same graph.

1.3 Linearized Emitter Characteristic of Stabilized Transistor Element

For the emitter characteristic (I_e as a function of V_e with I_c as a parameter) the emitter loop voltage equation is written:

$$V_e = I_e (r_e + R_b') + I_c (R_b') + V_b$$

Where

$$R_b' \triangleq R_b + r_b + \frac{r_{bd} R_{bs}}{r_{bd}+R_{bs}}$$

$$V_b \triangleq V_{bs} \frac{r_{bd}}{r_{bd}+R_{bs}} \qquad (6)$$

1.31 Locus of Points at Which the Base Diode Switches

If Equation 1 is substituted into Equation 6, one obtains

$$V_e = I_e r_e - \frac{V_{bs}}{R_{bs}} (r_b+R_b) \qquad (7)$$

This is the locus of the point at which the base diode switches. Two distinct regions are evident:

Region 1 $I_e < 0$

$$V_e = I_e r_{er} - \frac{V_{bs}}{R_{bs}} (r_b+R_b) \qquad (7a)$$

Region 2 $I_e > 0$

$$V_e = I_e r_{ef} - \frac{V_{bs}}{R_{bs}} (r_b+R_b) \qquad (7b)$$

This locus is shown in Fig. 8. This figure is drawn using the parameter values of the previous example.

1.32 Plot of Linearized Emitter Characteristic for Stabilized Transistor Element

Four district regions are evident. These are mapped on Fig. 8.

Region 1 $I_e < 0$; $I_e + I_c > -\frac{V_{bs}}{R_{bs}}$

In this region $r_e = r_{er}$; $r_{bd} = r_{bdf}$

when the insignificant terms are neglected in Equation 6.

$$V_e = I_e r_{er} + I_c (r_b + R_b + r_{bdf}) \qquad (6a)$$

Region 2 $I_e > 0$; $I_e + I_c > -\frac{V_{bs}}{R_{bs}}$.

In this region $r_e = r_{ef}$; $r_{bd} = r_{bdf}$,

and neglecting insignificant terms 6 becomes

$$V_e = I_e (r_{ef} + R_b + r_b + r_{bdf}) + I_c (R_b + r_b + r_{bdf}) \qquad (6b)$$

Region 3 $I_e > 0$; $I_e + I_c < -\frac{V_{bs}}{R_{bs}}$.

In this region $r_e = r_{ef}$; $r_{bd} = r_{bdr}$,

and :

$$V_e = I_e (R_{bs} + R_b) + I_c (R_b + R_{bs}) + V_{bs} \qquad (6c)$$

Region 4 $I_e < 0$ $I_e + I_c < -\frac{V_{bs}}{R_{bs}}$.

In this region $r_e = r_{er}$; $r_{bd} = r_{bdr}$,

and:

$$V_e = I_e r_{er} + I_c (R_{bs} + R_b) + V_{bs} \qquad (6d)$$

For the typical example which has been carried along throughout this discussion, the plot of 6a to 6d appears in Fig. 9.

1.33 Locus on the Collector Characteristic where the Collector Diode Switches

The collector diode switches when:

$$I_c = -\alpha_e I_e \quad (I_e > 0) \tag{a}$$

If (a) is substituted into Equation 6, one obtains:

$$V_e = I_e \left(r_e + R_b' (1 - \alpha_e) \right) + \frac{V_{bs} r_{bd}}{r_{bd} + R_{bs}} \tag{b}$$

Three regions are apparent:

Region 1 $I_e < 0; \quad I_e > -I_c \frac{-V_{bs}}{R_{bs}}$,

$$V_e \cong I_e (r_{er} + R_b') \cong I_e r_{er} \tag{c}$$

Region 2 $I_e > 0; \quad I_e > -I_c \frac{-V_{bs}}{R_{bs}}$,

$$V_e \cong I_e (r_{ef} + R_b + r_b + r_{bdf}) (1 - \alpha_e) \tag{d}$$

Region 3 $I_e > 0 \qquad I_e < -I_c \frac{-V_{bs}}{R_{bs}}$

$$V_e = I_e r_{ef} + (R_{bs} + R_b) (1 - \alpha_e) + V_{bs} \tag{e}$$

This locus is sketched on Fig. 9.

1.34 Experimental Check of Results Predicted from 1.3

The circuit Fig. 10* was set up and the emitter family was plotted experimentally for a General Electric G-11A transistor. Calculated and plotted values appear in Fig. 11.

---

* The pentode was necessary to maintain the constant collector currents.

1.4 Conclusion

1.41 Simplicity of Plotting the Characteristics

When the parameter values are known, one can approximate the collector characteristics by calculating (7) points*, and the emitter characteristic by calculating (2) points and (3) slopes.**

1.42 Comparison of the Stabilized and Unstabilized Transistor Characteristics

The most significant thing about the base stabilized characteristics is that the slopes and spacings of the constant parameter lines are made somewhat independent of the transistor parameter values. This is especially true of the slopes and spacings of the constant collector current lines on the emitter characteristics. To a lesser extent, it is true on the collector characteristics. Thus, the linearized equivalent circuit is a better approximation for the stabilized transistor circuit than it is for the transistor itself. The approximation is best when R_b and R_{bs} are large and α_e in the transistor is quite constant.

The addition of the base stabilization circuit has the effect of reducing the effective α value in the region where the base diode is open. This is shown as follows. For the unstabilized transistor:

$$\alpha = \frac{r_b + \alpha_e r_c}{r_c + r_b} = \frac{\Delta I_c}{\Delta I_e} \qquad V_c = \text{constant}$$

or in the region where the collector diode is open $r_{cr} >> r_b$

so, $$\alpha \cong \alpha_e$$

when the base stabilization circuit is added from Equation 4

$$\alpha_s = \frac{\Delta I_c}{\Delta I_e} \qquad V_c = \text{constant}$$

$$V_c = \frac{R_b' + \alpha_e r_c}{R_b' + r_c}$$

---

* Further assumptions would lead to a four point approximation which would be satisfactory for most purposes. These points are (1), (2), (5), and (7).

** This can be simplified if one assumes that r_{ef} is very small.

when the base and collector diodes are open $R_b' \cong R_{bs}$ which is about the value of r_{cr} so;

$$\alpha_s = \frac{R_{bs} + \alpha_e r_{cr}}{R_{bs} + r_{cr}}$$

and the ratio of α to α_s is

$$\frac{\alpha}{\alpha_s} \cong \frac{\frac{R_{bs}}{\alpha_e} + r_{cr}}{R_{bs} + R_{cr}}$$

These approximations can be used to space the constant emitter current lines in Figure 4. In fact, this is the simplest way to space these lines.

Signed: John F Jacobs
(John Jacobs)

Approved: Norman H. Taylor
(Norman H. Taylor)

JJ:ak/rdf

Illustrations:

Figure 1 - SA-50963-1
Figure 2 - SA-50963-1
Figure 3 - SA-50964
Figure 4 - SA-50965
Figure 5 - SA-50966
Figure 6 - SA-48306-G
Figure 7 - SA-48307-G-1
Figure 8 - SA-50967
Figure 9 - SA-50968
Figure 10 - SA-50969
Figure 11 - SA-48308-G

cc: Standard Trans. Dist. (15)

Stabilized Transistor Circuit

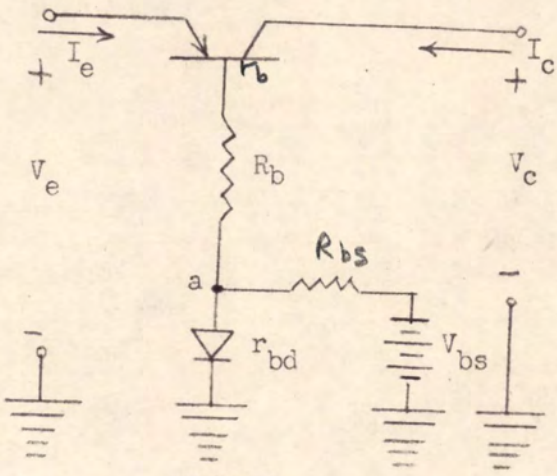
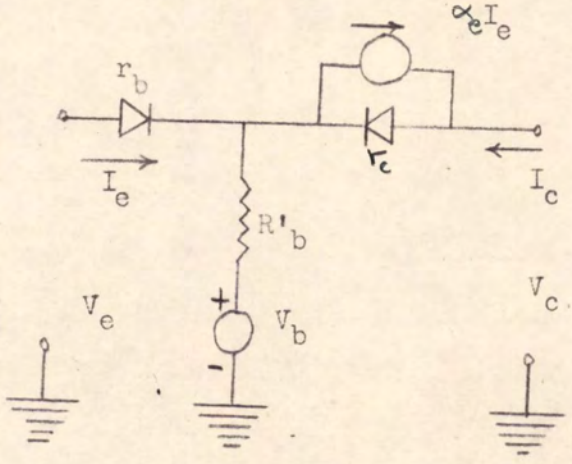


FIGURE1



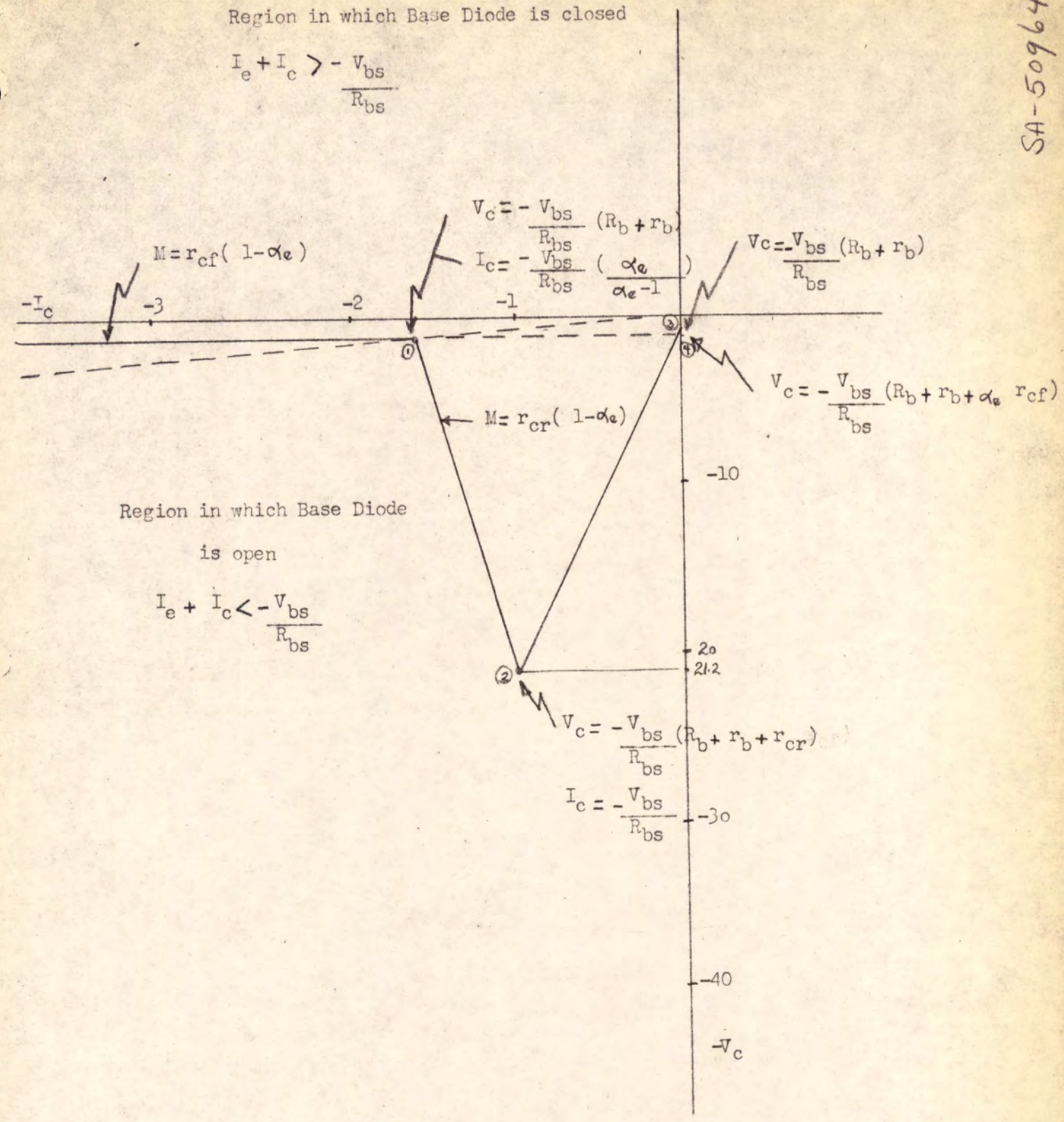
$r_c = r_{cr}$ (reverse)

$r_c = r_{cf}$ (forward)

Equivalent Circuit

FIGURE 2

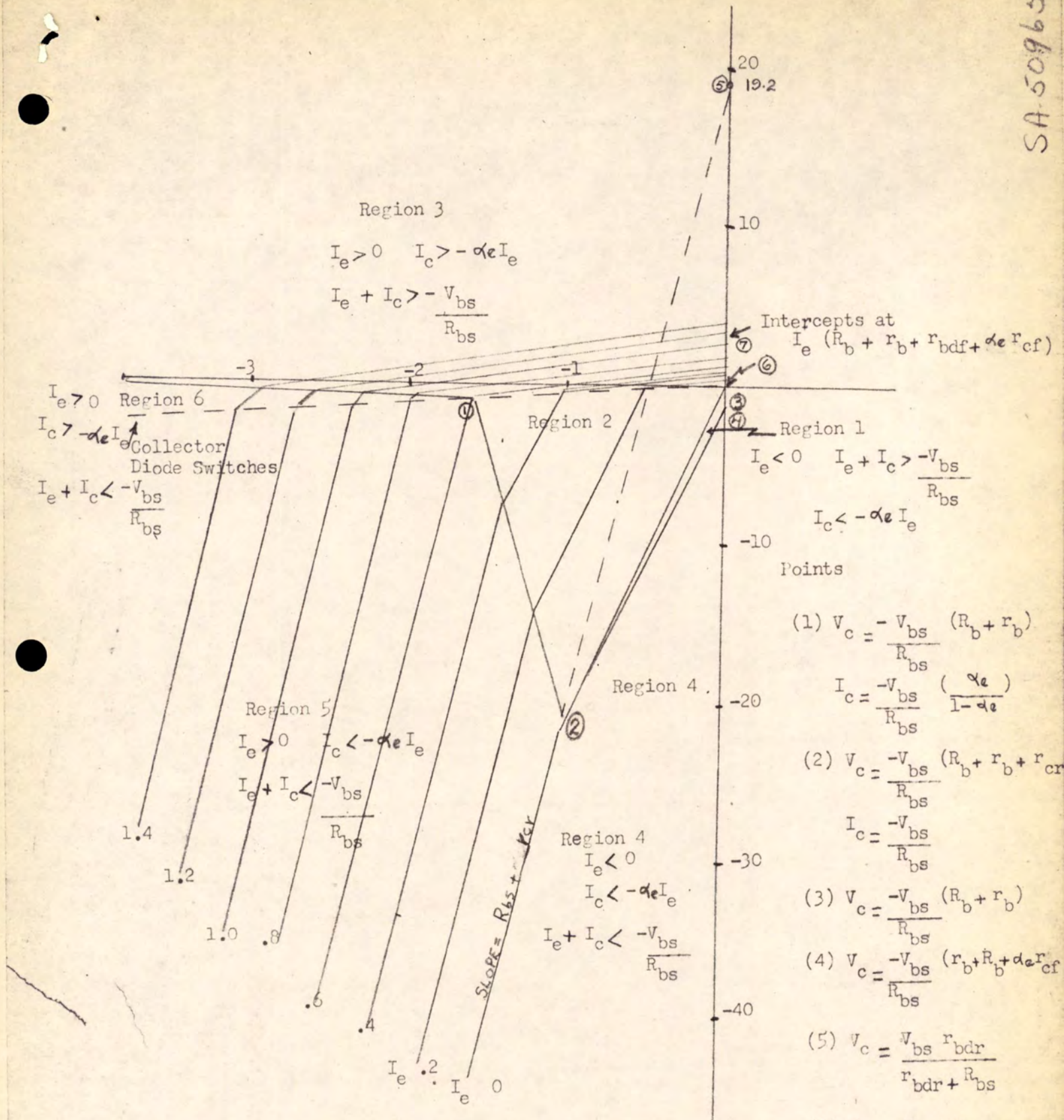
SA-50



Four point method for showing locus of Base Diode switch

FIGURE 3

SA-50964



Liniarized Collector Family From 7 Points

FIGURE 4

SA-50965

SA-50965

Circuit For Taking Collector Characteristics

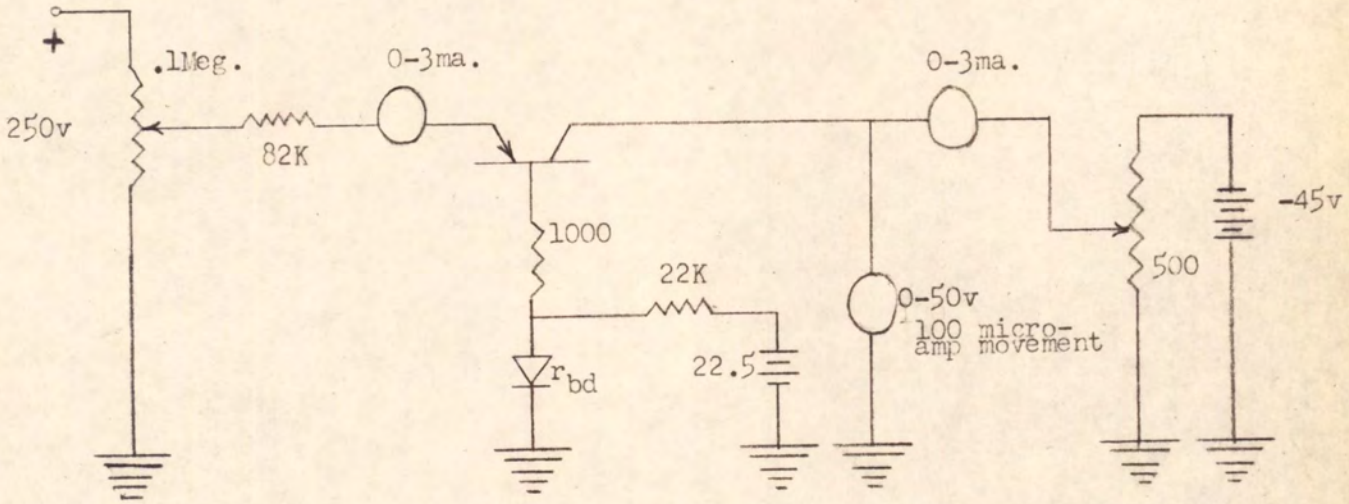


FIGURE 5

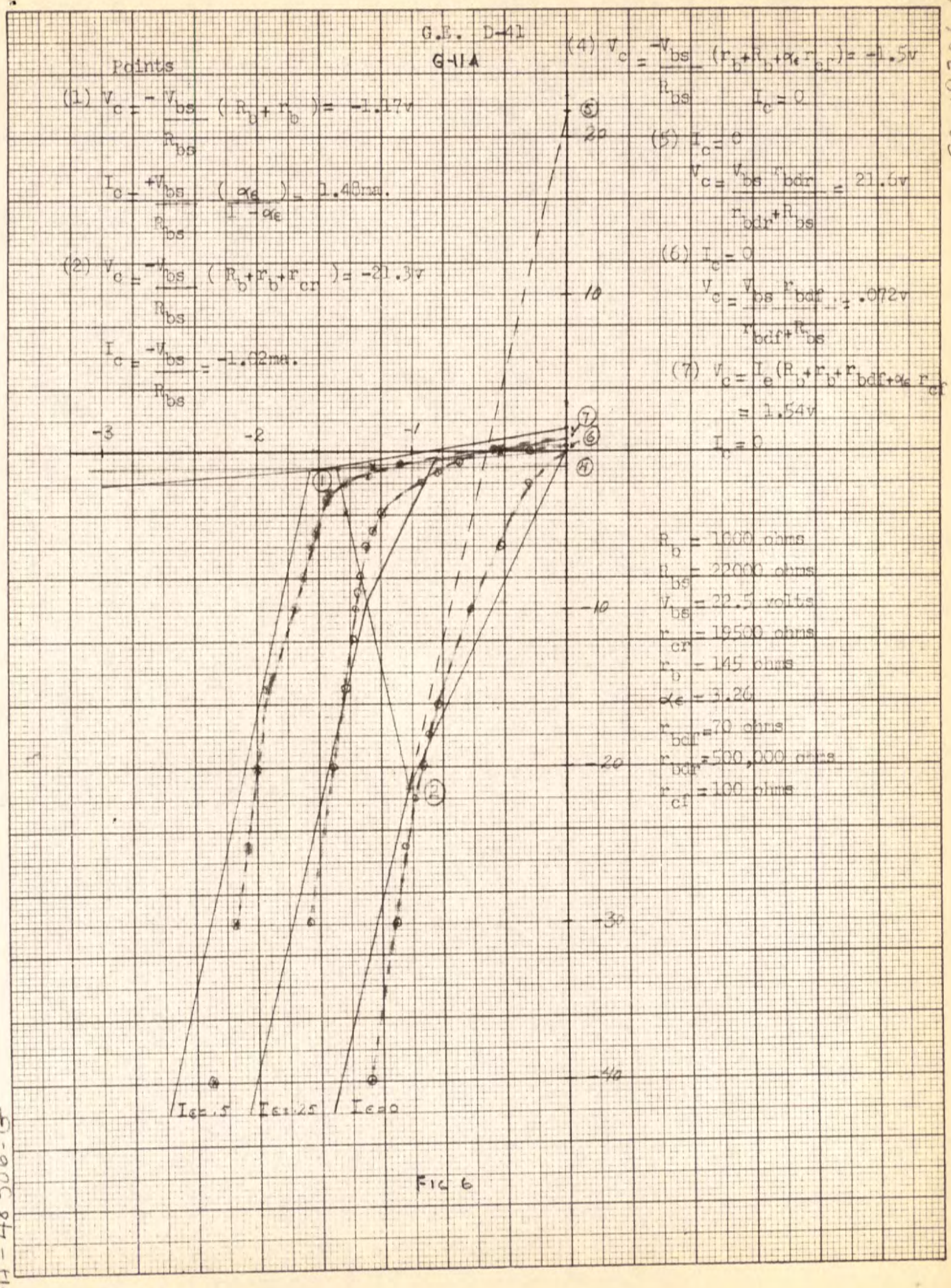


Fig 6

SA-48306-G

Bell Labs 1698
D2218

Points

(1) $V_c = \frac{-V_{bs}}{R_{bs}} (R_b + r_b) = -1.4v$

$I_c = \frac{-V_{bs}}{R_{bs}} \left(\frac{\alpha_c}{1-\alpha_c} \right) = -1.8ma.$

(2) $V_c = \frac{-V_{bs}}{R_{bs}} (R_b + r_b + r_{cr}) = -29.2v$

$I_c = \frac{-V_{bs}}{R_{bs}} = -1.02ma.$

(3)

(5) $I_e = 0$

$V_c = V_{bs} \frac{r_{bdr}}{r_{bdr} + R_{bs}} = 21.6v$

(6) $I_e = 0$

$V_c = V_{bs} \frac{r_{bdf}}{r_{bdf} + R_{bs}} = .072v$

(4) $V_c = \frac{-V_{bs}}{R_{bs}} (r_b + R_b + \alpha_c r_{cf}) = 3.74v$

(7) $V_c = I_e (R_b + r_b + r_{bdf} + \alpha_c r_{cf}) = 1.87v$

$R_b = 1000$ ohms
$R_{bs} = 22000$ ohms
$V_{bs} = 22.5$ volts
$r_{cr} = 20,000$ ohms
$r_b = 365$ ohms
$\alpha_c = 2.30$
$r_{bdf} = 70$ ohms
$r_{bdr} = 500,000$ ohms
$r_{cf} = 100$ ohms

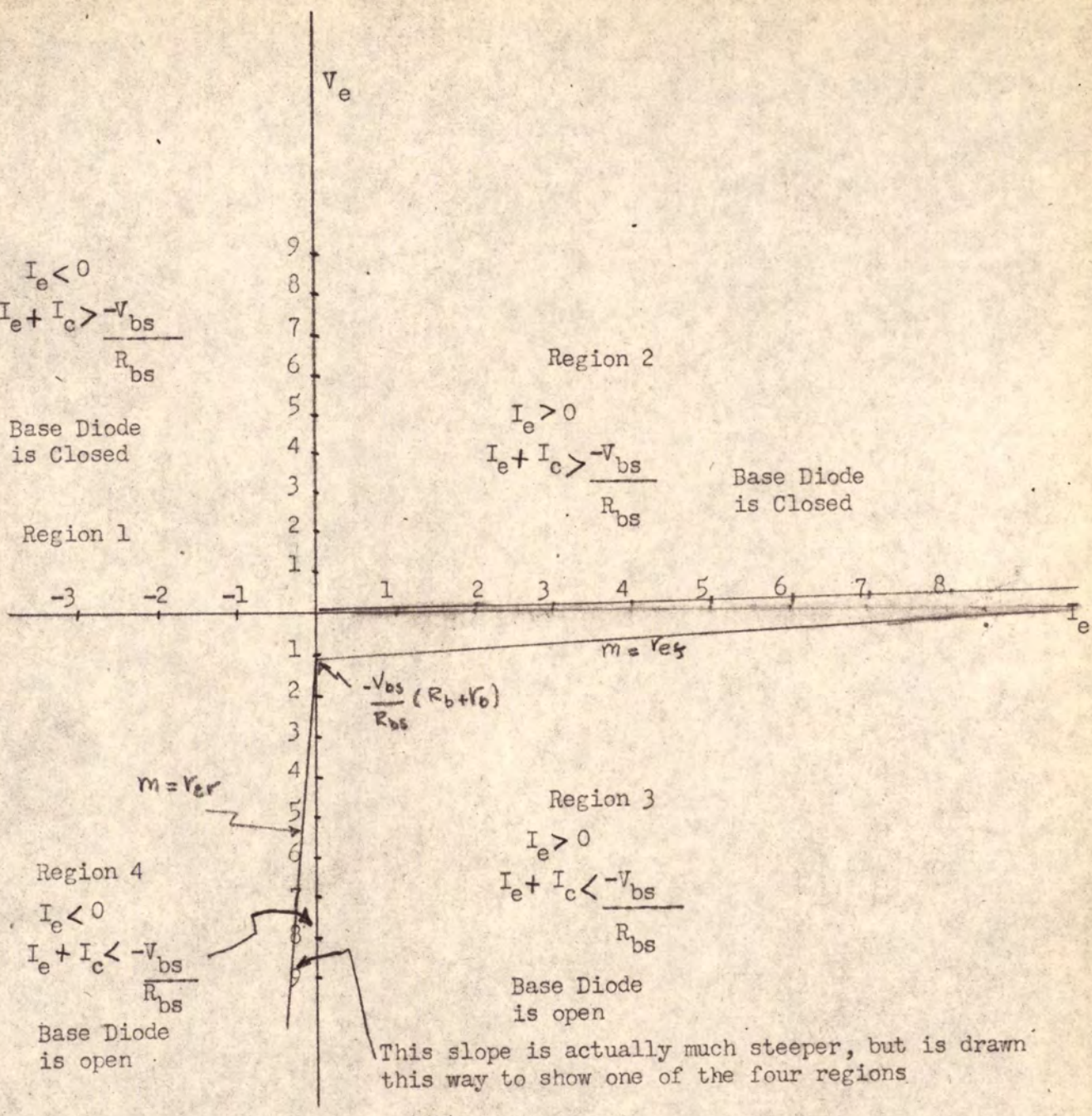
-10
-20
-30
-40

$I_e = 1ma.$ $I_e = .5ma.$ $I_e = 0$

FIGURE 7

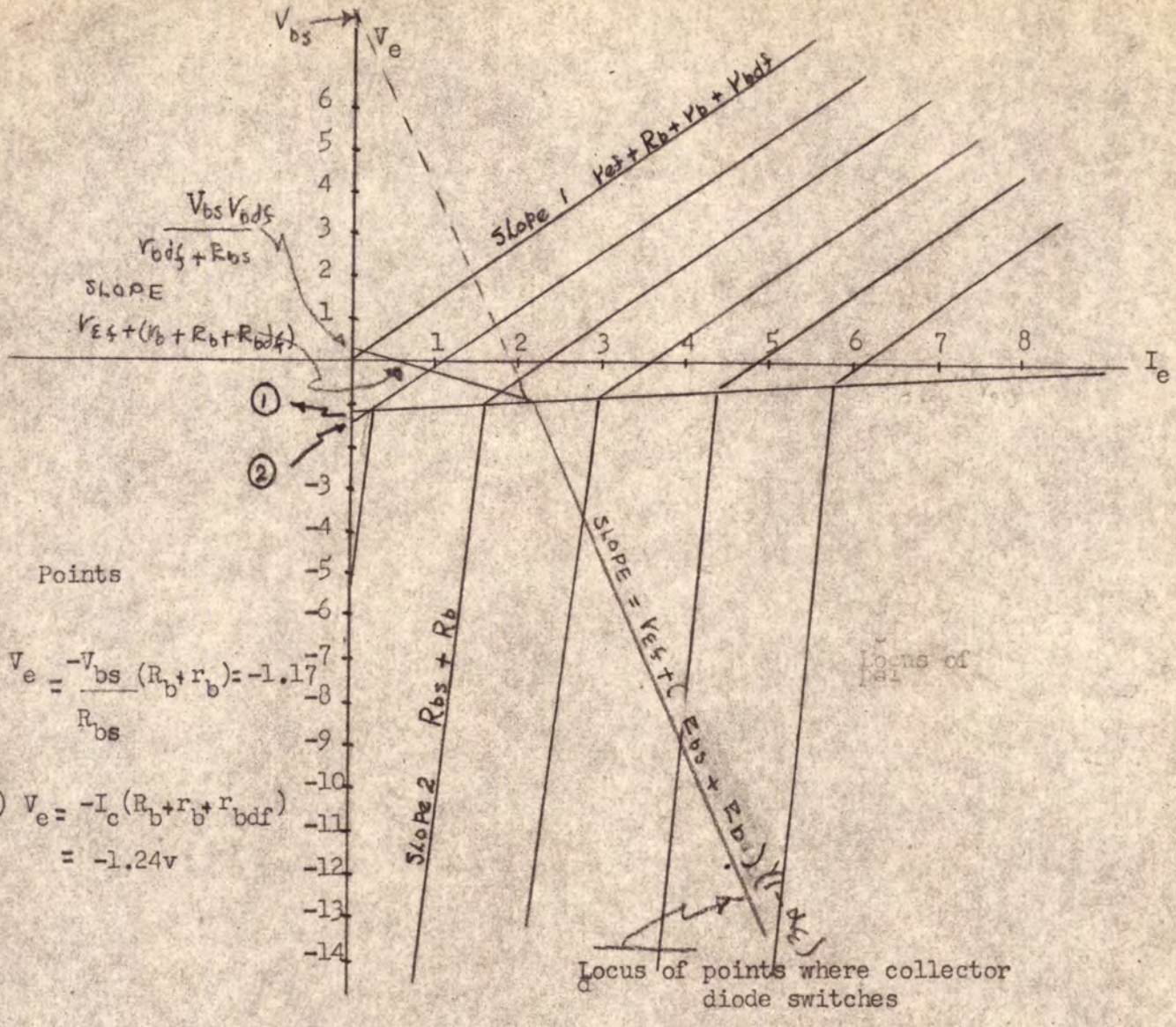
359-12G KEUFFEL & ESSER CO.
10 X 10 to the ½ inch, 5th lines accented.
MADE IN U.S.A.

SA-48307-G-1



One Point And Two Slopes For Plotting Switch Locus

FIGURE 8



Liniarized Emitter Family From Two Points And Two Slopes

FIGURE 9

Circuit For Taking Emitter Characteristics

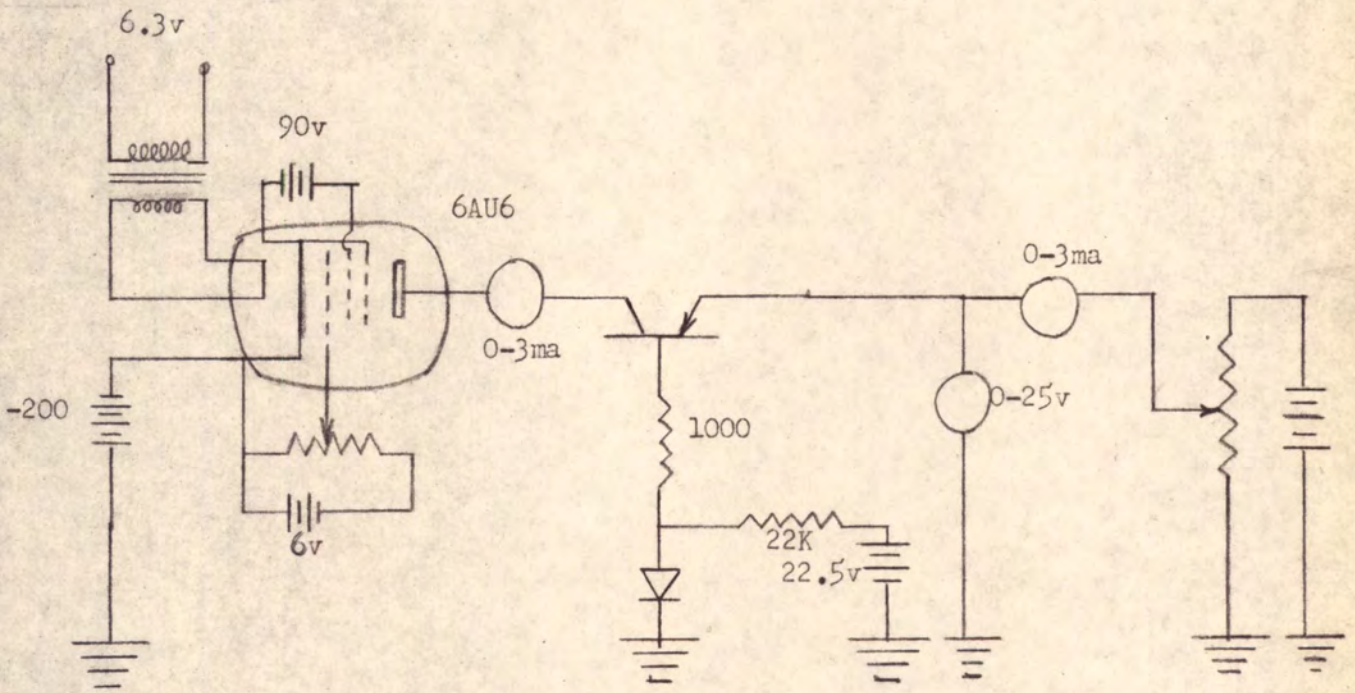
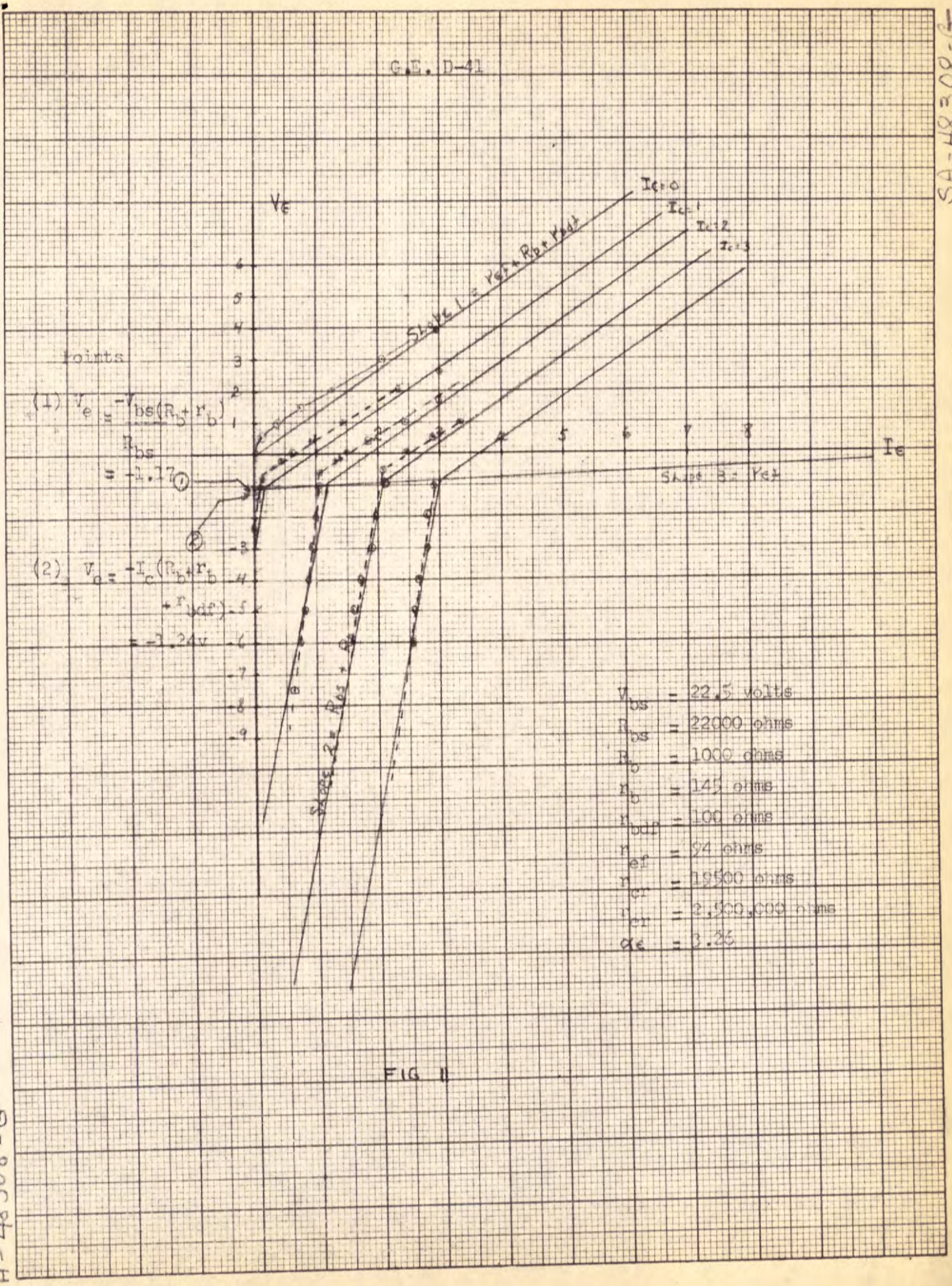


FIGURE 10

SA-50969

G.E. D-41



Points

(1) $V_e = -\frac{V_{bs}(R_b + r_b)}{R_{bs}}$

$= +4.17$ ①

(2) $V_e = +I_c(R_b + r_b + r_{bdf})$

$= -3.24$ ②

$V_{bs} = 22.5$ volts

$R_{bs} = 22000$ ohms

$R_b = 1000$ ohms

$r_b = 145$ ohms

$r_{bdf} = 100$ ohms

$r_{ef} = 24$ ohms

$r_{cr} = 19500$ ohms

$r_{cr} = 2,500,000$ ohms

$\alpha_e = 3.25$

FIG 11

SA-48308-GT

SA-48308-GT

R. Beck

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Cambridge, Massachusetts

SUBJECT: LINEARIZED CHARACTERISTICS OF A BASE FED, GROUNDED EMITTER TRANSISTOR

To: Transistor Group

From: John F. Jacobs and W. A. Klein

Date: April 3, 1952

Abstract: The linearized input and output characteristics of a grounded emitter transistor are derived.

3.1 The grounded emitter transistor

In this note, as in M-1400, the transistor circuit is treated as a four-terminal network and the input and output characteristics are plotted. The input or base characteristic is a plot of input voltage, V_b, as a function of the input current, I_b, with the output current, I_c, as a parameter. The output or collector characteristic is a plot of the output voltage, V_c, as a function of the output current, I_c, with the input current, I_b, as a parameter. The circuit under investigation and its large signal equivalent are shown in Figure 1.

3.2 The base characteristics

The base loop equation is:

$$1) \quad V_b = I_b(r_b + \bar{R}_e) + I_c(\bar{R}_e)$$

where $\bar{R}_e \triangleq r_e + R_e$ and, for later use, $\bar{R}_{er} \triangleq r_{er} + R_e$, $\bar{R}_{ef} \triangleq r_{ef} + R_e$.

3.21 Locus of points at which the emitter diode switches

Examination of equation 1) shows that the emitter diode, r_e, is the only two-valued resistance which must be considered when one plots the base characteristic. The emitter diode is in the act of switching when the current through $\bar{R}_e$ and the voltage across $\bar{R}_e$ are zero. This leads one directly to:

$$2a) \quad V_b = I_b r_b$$

as the locus of points on the V_b-I_b plane at which the emitter diode switches, and to

$$2b) \quad I_b = -I_c$$

for locating the particular point on this locus at which switching occurs for a given value of I_c.

3.22 Regions in which the emitter diode is open and closed

When:

$$V_b > I_b r_b \quad \text{or} \quad I_b > -I_c$$

the voltage across $\overline{R}_e$ must be greater than zero and the emitter diode is open.

When:

$$V_b < I_b r_b \quad \text{or} \quad I_b < -I_c$$

the voltage across $\overline{R}_e$ must be less than zero and the emitter diode is closed.

3.23 Typical Base Characteristic

As an example, consider the transistor D-51, which is a G11A. This transistor has the following large signal equivalent circuit values, as measured by the methods outlined in E-441:

$$r_{ef} = 120\ \Omega$$
$$r_{er} = 5\ \text{meg.}\ \Omega$$
$$r_b = 200\ \Omega$$
$$r_{cf} = 100\ \Omega$$
$$r_{cr} = 20{,}000\ \Omega$$
$$\alpha = 2.4$$

and let $R_e = 1{,}000\ \Omega$

In the region where the emitter diode is closed, equation 1) becomes:

1a) $V_b = I_b(r_b + r_{ef} + R_e) + I_c(r_{ef} + R_e)$

Substituting the above values in this equation, one obtains:

$$V_b = I_b(200+120+1000) + I_c(120+1000)$$

1b) $V_b = I_b(1320) + I_c(1120)$

In the region where the emitter diode is open, equation 1) becomes:

1c) $V_b = I_b(r_b + r_{er} + R_e) + I_c(r_{er} + R_e)$

Substituting the typical values into 1c), one obtains:

1d) $V_b = I_b(5 \times 10^6) + I_c(5 \times 10^6)$

Using 1b) and 1c) and equation 2a) one can plot the input characteristics of the grounded emitter transistor. This plot appears in Figure 2.

3.24 How to plot the base characteristics

The simplest way to plot these curves is to proceed as follows:

a) Define the factor Γ:

$$3)\quad \Gamma \triangleq \left.\frac{\partial I_c}{\partial I_b}\right|_{V_b}$$

From equation 1) we find:

$$3a)\quad \Gamma \doteq \frac{\bar{R}_e}{r_b + \bar{R}_e}$$

When the emitter diode is open:

$$3b)\quad \Gamma \cong \frac{\bar{R}_{er}}{\bar{R}_{er}} = 1$$

When the emitter diode is closed:

$$3c)\quad \Gamma = \frac{r_{ef} + R_e}{r_b + r_{ef} + R_e}$$

b) Draw the locus of the points at which the emitter diode switches (equation 2a)

c) Draw the line representing $I_c = 0$ when the emitter diode is open. The line is almost a vertical one.

d) Draw the line representing $I_c = 0$ when the emitter diode is closed (slope is $r_b + R_e + r_{ef}$).

e) Space the lines according to 3b) or 3c).

3.25 Locus of points where the collector diode closes

The collector diode closes when:

$$4)\quad I_c = -\alpha_e I_e$$

If one substitutes this equation along with the relationship

$$5)\quad I_e = -I_c - I_b$$

into 1), one finds that:

$$6)\quad V_b = I_b\left[r_b + \frac{\bar{R}_e}{1-\alpha_e}\right]$$

When the emitter diode is open this is:

$$6a)\quad V_b = I_b\left[r_b + r_{ef} + R_e\right] \cong I_b r_{er}$$

For our example, this is:

$$V_b \cong I_b \, 5 \times 10^6$$

When the emitter diode is closed this is:

$$6b) \quad V_b = I_b \left[r_b + \frac{r_{ef} + R_e}{1 - \alpha_e} \right]$$

For our example:

$$V_b = I_b \left[200 + \frac{120 + 1000}{1 - 2.4} \right]$$

$$= I_b \, (-600)$$

3.26 The actual base characteristics

Actual base characteristics for D51 with R_e=1K are plotted in Figure 3 and compared there with the predicted curves.

3.3 The collector characteristics

3.31 Analytical derivation

The collector loop equation is

$$7) \quad V_c = I_c \left[r_c (1 - \alpha_e) + \bar{R}_e \right] + I_b (\bar{R}_e - \alpha_e r_c)$$

where $\alpha_e = 0$ if $I_e = -I_c - I_b < 0$

An attempt to discover regions of the V_c-I_c plane in which the conditions of the various diodes are constant proves fruitless. Instead, the following approach is used:

For

$I_e > 0 \quad (I_c + I_b < 0)$	$I_e < 0 \quad (I_c + I_b > 0)$
equation 7) becomes:	
7a) $V_c = I_c (r_c + r_{ef} + R_e - \alpha_e r_c) + I_b (r_{ef} + R_e - \alpha_e r_c)$	7b) $V_c = I_c (r_c + r_{er} + R_e) + I_b (r_{er} + R_e)$
CASE I: $I_b = 0$	
Then $I_c < 0$	Then $I_c > 0$
and 7a) becomes:	and 7b) becomes:
$V_c = (r_c + r_{ef} + R_e - \alpha_e r_c) I_c$	$V_c = (r_c + r_{er} + R_e) I_c$

$(I_e > 0)$	$(I_e < 0)$
The current through the collector diode is $I_c + \alpha_e I_e$. Since $I_b = 0$, $I_e = -I_c$. Then $I_c + \alpha_e I_e = (1-\alpha_e) I_c$. Since $\alpha_e > 1$, $1-\alpha_e < 0$. Thus: $(1-\alpha_e) I_c > 0$	The current through the collector diode is I_c, which is > 0. Therefore, $r_c = r_{cf}$ and the $V_c - I_c$ relation is (for $I_c > 0$):
Therefore, $r_c = r_{cf}$, and the $V_c - I_c$ relation is (for $I_c < 0$):	
8a) $V_c = \left[r_{cf}(1-\alpha_e) + r_{ef} + R_e \right] I_c$	8b) $V_c = \left[r_{cf} + r_{er} + R_e \right] I_c$

CASE II: $I_b > 0$

Then $I_c < -I_b < 0$	Then $I_c > -I_b$
and 7a) is	and 7b) is
$V_c = I_c \left[r_c(1-\alpha_e) + r_{ef} + R_e \right] + I_b (r_{ef} + R_e - \alpha_e r_c)$	$V_c = I_c (r_c + r_{er} + R_e) + I_b (r_{er} + R_e)$
The collector switches when:	
$I_c + \alpha_e I_e = 0$	$I_c = 0$
Substituting $I_e = -I_b - I_c$ and solving: $I_c = \frac{\alpha_e}{1-\alpha_e} I_b < -I_b < 0$	
$r_c = r_{cf}$ when $I_c + \alpha_e I_e > 0$, that is when $I_c < \frac{\alpha_e}{1-\alpha_e} I_b$	$r_c = r_{cf}$ when $I_c > 0$
$r_c = r_{cr}$ when $I_c + \alpha_e I_e < 0$, that is when $I_c > \frac{\alpha_e}{1-\alpha_e} I_b$	$r_c = r_{cr}$ when $I_c > 0$

$(I_e > 0)$	$(I_e < 0)$

Thus the V_c-I_c relation is:

for $I_c < \frac{\alpha_e}{1-\alpha_e} I_b$:	for $-I_b < I_c < 0$:
9a) $V_c = I_c\left[r_{cf}(1-\alpha_e)+r_{ef}+R_e\right] + I_b\left[r_{ef}+R_e-\alpha_e r_{cf}\right]$	9c) $V_c = I_c(r_{cr}+r_{er}+R_e) + I_b(r_{er}+R_e)$
for $\frac{\alpha_e}{1-\alpha_e} I_b < I_c < -I_b$:	for $I_c > 0$:
9b) $V_c = I_c\left[r_{cr}(1-\alpha_e)+r_{ef}+R_e\right] + I_b(r_{ef}+R_e-\alpha_e r_{cr})$	9d) $V_c = I_c(r_{cf}+r_{er}+R_e) + I_b(r_{er}+R_e)$

CASE III: $I_b < 0$

Then $I_c < -I_b > 0$	Then $I_c > -I_b > 0$

The collector switches when:

$I_c + \alpha_e I_e = 0$	$I_c = 0$

Substituting $I_e = -I_b - I_c$

and solving:

$I_c = \frac{\alpha_e}{1-\alpha_e} I_b > -I_b > 0$

$r_c = r_{cf}$ when $I_c < \frac{\alpha_e}{1-\alpha_e} I_b$	$r_c = r_{cf}$ when $I_c > 0$
$r_c = r_{cr}$ when $I_c > \frac{\alpha_e}{1-\alpha_e} I_b$	$r_c = r_{cr}$ when $I_c < 0$
But, in this case,	But, in this case,
$I_c < -I_b < \frac{\alpha_e}{1-\alpha_e} I_b$	$I_c > -I_b > 0$
Therefore, $r_c = r_{cf}$ for $I_c < -I_b$.	Therefore, $r_c = r_{cf}$ for $I_c > -I_b$.

Thus the V_c-I_c relation is:

for $I_c < -I_b$	for $I_c > -I_b$
10a) $V_c = I_c\left[r_{cf}(1-\alpha_e)+r_{ef}+R_e\right] + I_b\left[r_{ef}+R_e-\alpha_e r_{cf}\right]$	10b) $V_c = I_c(r_{cf}+r_{er}+R_e) + I_b(r_{er}+R_e)$

3.32 A systematic procedure for plotting the collector characteristics

The expressions for all points and slopes are as follows:

Case I: $I_b = 0$ See Figure 3 and equations 8a) and 8b).

Slopes: $I_c > 0$: $\bar{R}_{er} + r_{cf} \cong \bar{R}_{er}$

$I_c < 0$: $\bar{R}_{ef} - r_{ef}(\alpha_e - 1) \cong R_e$

Case II: $I_b > 0$ See Figure 4 and equations 9a), b), c), d).

Slopes: (0)-(1) $r_{cf} + \bar{R}_{er} \cong \bar{R}_{er}$

(1)-(2) $r_{cr} + \bar{R}_{er}$

(2)-(3) $\bar{R}_{ef} - (\alpha_e - 1) r_{cr}$

(3)-(4) $\bar{R}_{ef} - (\alpha_e - 1) r_{cf} \cong R_e$

Points:

(1) $I_{c1} = 0$, $V_{c1} = I_b \bar{R}_{er}$

(2) $I_{c2} = -I_b$, $V_{c2} = -I_b r_{cr}$

(3) $I_{c3} = \frac{\alpha_e}{1-\alpha_e} I_b$, $V_{c3} = \frac{\bar{R}_{ef}}{1-\alpha_e} I_b$

Case III: $I_b < 0$ See Figure 5 and equations 10a) and 10b).

Slopes: (0)-(1) $r_{cf} + \bar{R}_{er} \cong \bar{R}_{er}$

(1)-(2) $\bar{R}_{ef} - (\alpha_e - 1) r_{cf} \cong R_e$

Point: (1) $I_{c1} = -I_b$, $V_{c1} = -I_b r_{cf}$

For cases I and III, the indicated slopes and point are necessary for the plot. For case II, all slopes and points need not be calculated for making a plot. Generally V_{c1} will be of no interest and, furthermore, so large that it will not be within the scale range used. Also, line (0)-(1) is of no particular interest, while the slope of line (2)-(3) need not be calculated if points (2) and (3) have been found. Thus, in case II, all that is needed is: slopes of (1)-(2) and (3)-(4), and points (2) and (3).

3.33 Loci of switching points

Case II: $I_b > 0$ See figure 4 and section 3.32, Case II.

Locus of point (1): (collector switching)

$I_c = 0$

Locus of point (2): (emitter switching)

$$\text{slope} = \frac{V_{c2}}{I_{c2}} = r_{cr}$$

Locus of point (3): (collector switching)

$$\text{slope} = \frac{V_{c3}}{I_{c3}} = \frac{\bar{R}_{ef}}{\alpha_e}$$

Case III: $I_b < 0$ See Figure 5 and section 3.32, Case III.

Locus of point (1): (emitter switching)

$$\text{slope} = \frac{V_{c1}}{I_{c1}} = r_{cf}$$

3.34 Predicted and actual collector characteristics:

The predicted characteristics:

As in section 3.23, some collector characteristics are calculated and displayed for transistor #D51. The procedure of 3.32 is used. The results are displayed graphically as dotted lines in Figure 7.

Case I: $I_b = 0$

Slopes: $I_c > 0$: $\bar{R}_{er} = R_e + r_{er} = 5M + 1K \cong 5$ Megohms

$I_c < 0$: $R_e = 1K$

Case II: $I_b > 0$

I_b \ Point or Slope	(1)	(2)		(3)		(1)-(2)	(3)-(4)
	V_{c1}	I_{c2}	V_{c2}	I_{c3}	V_{c3}		
1 ma	5000 volts	-1 ma	-20 vts	-1.7 ma	-.86 vts	5 MΩ	1K

Case III: $I_b < 0$

I_b \ Point or Slope	(1)		(0)-(1)	(1)-(2)
	I_{c1}	V_{c1}		
-1 ma	1 ma	0.1 vt	5 MΩ	1K

The actual characteristics:

The results of a dynamic plot of some collector characteristics

for transistor D-51 with R_e=1K also appear in Figure 7. The discrepancy between the predicted and observed results in the steep positive slope portion of the I_b=1ma curve is very likely due to the I_b supply not acting as a constant current source.

Signed John F Jacobs
John F. Jacobs

Signed William A. Klein
William A. Klein

Approved Norman H. Taylor
Norman H. Taylor

JFJ:WAK/jk

Drawings Attached:
Fig. 1 - A-51133
Fig. 2 - A-51134
Fig. 3 - A-51176
Figs. 4 & 5 - A-51135
Fig. 6 - A-51136
Fig. 7 - A-51177

Standard Trans. Dist. (32)

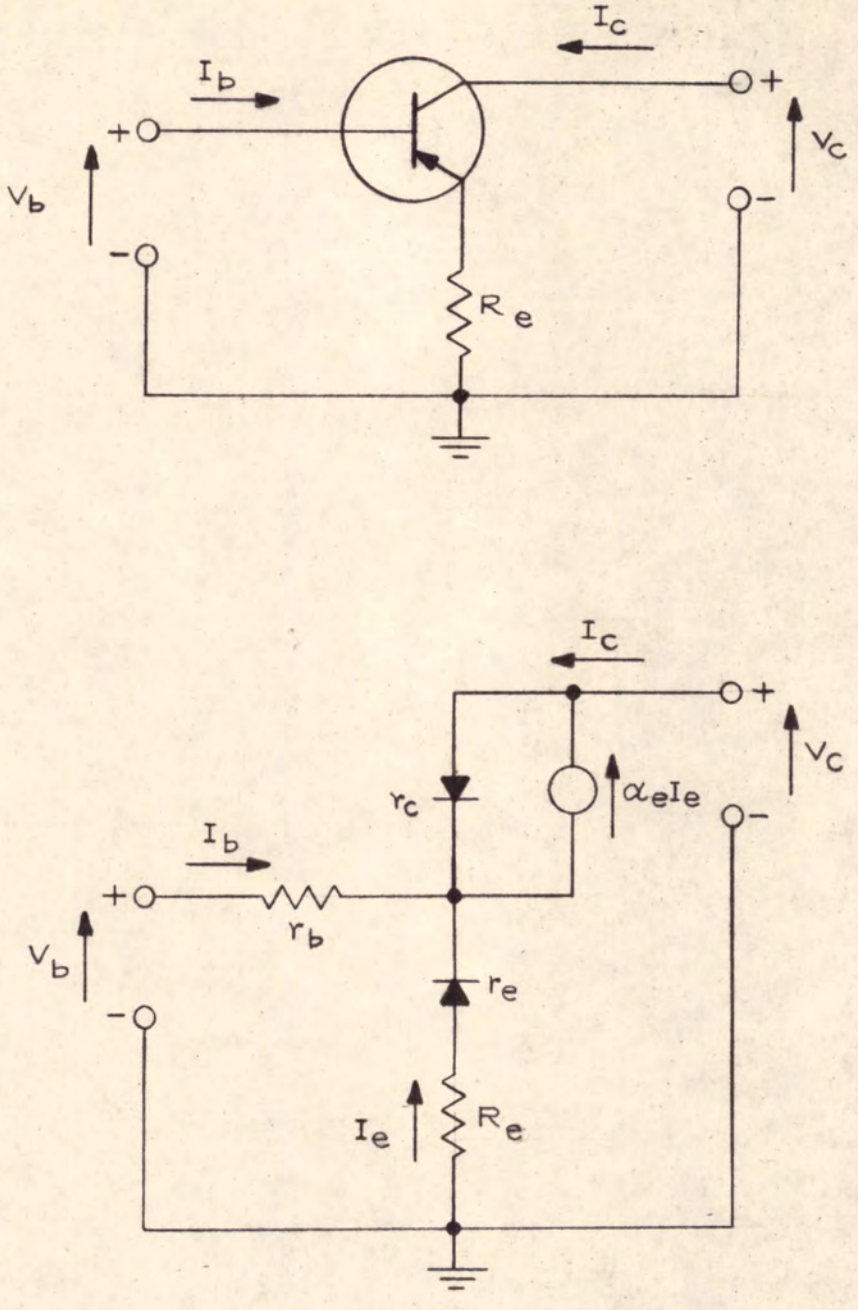


FIG. 1

GROUNDED EMITTER AND EQUIVALENT CIRCUIT

A-51133

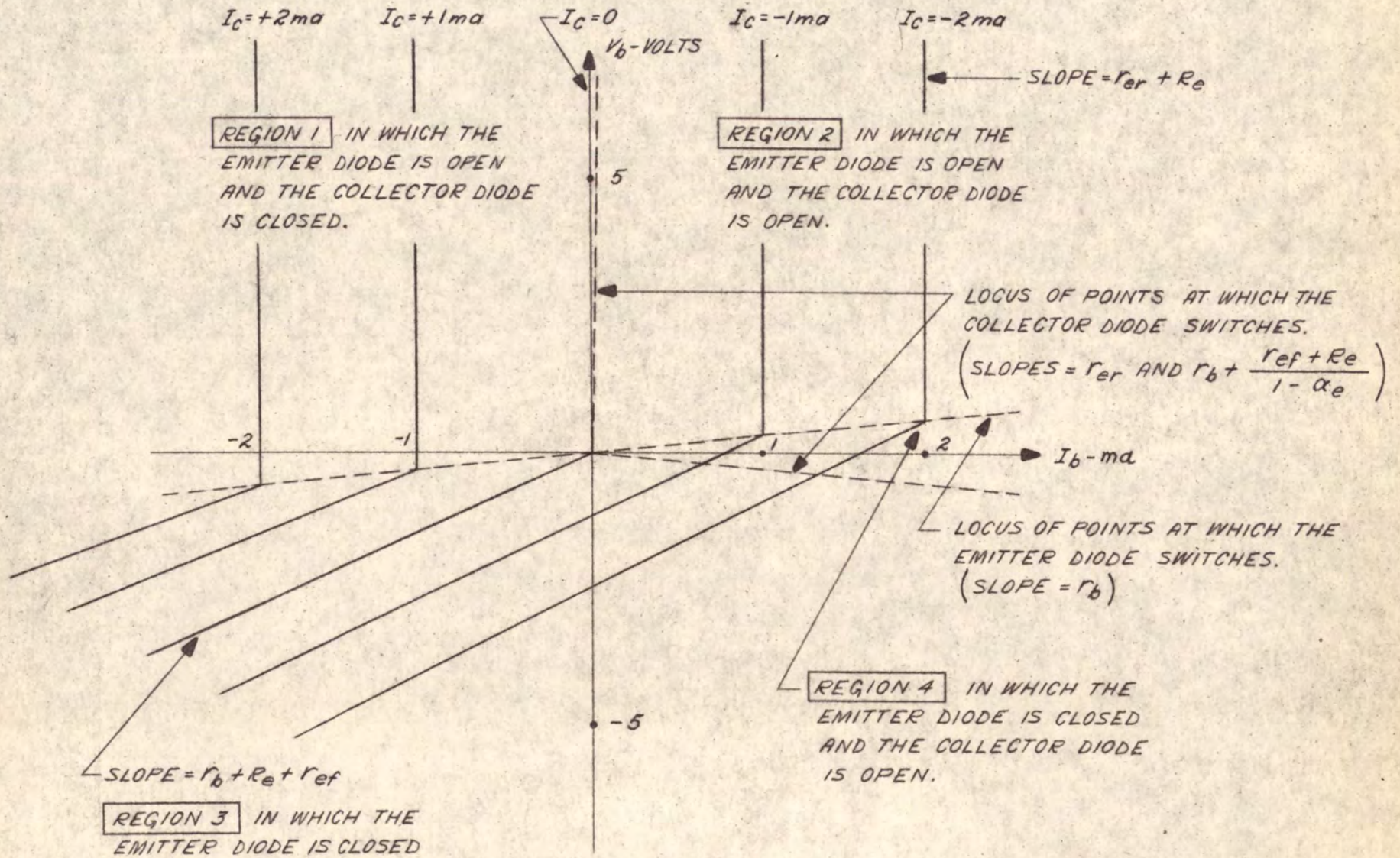


FIG. 2

BASE CHARACTERISTICS

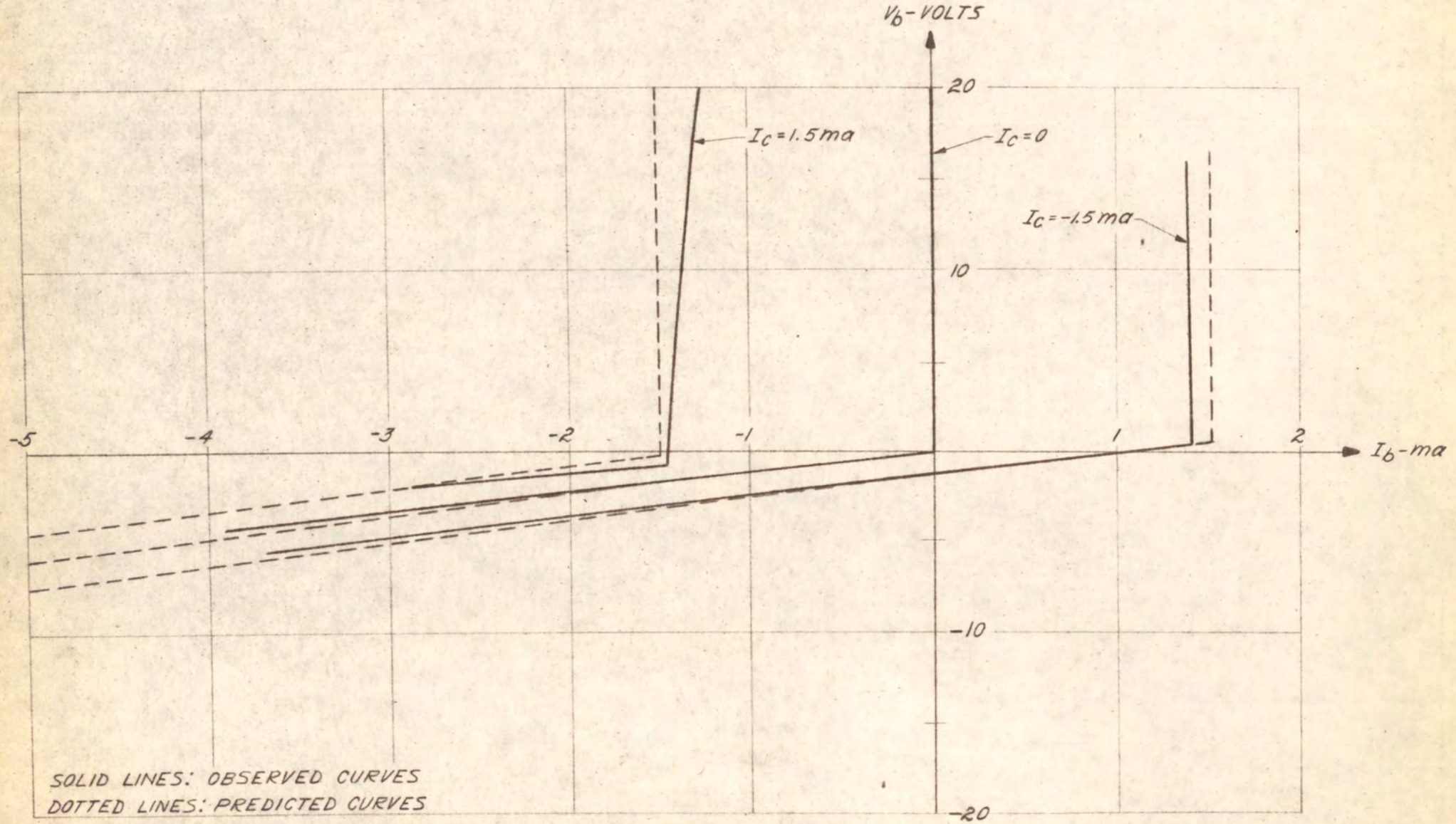


FIG. 3

COMPARISON OF PREDICTED AND OBSERVED BASE CHARACTERISTICS

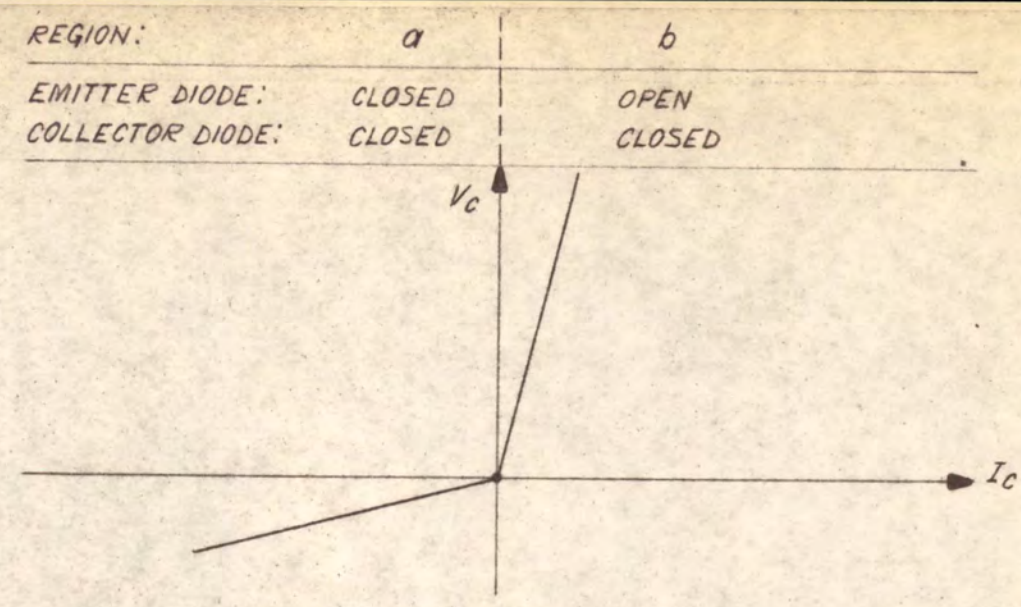


FIG. 4

COLLECTOR CHARACTERISTIC FOR $I_b = 0$

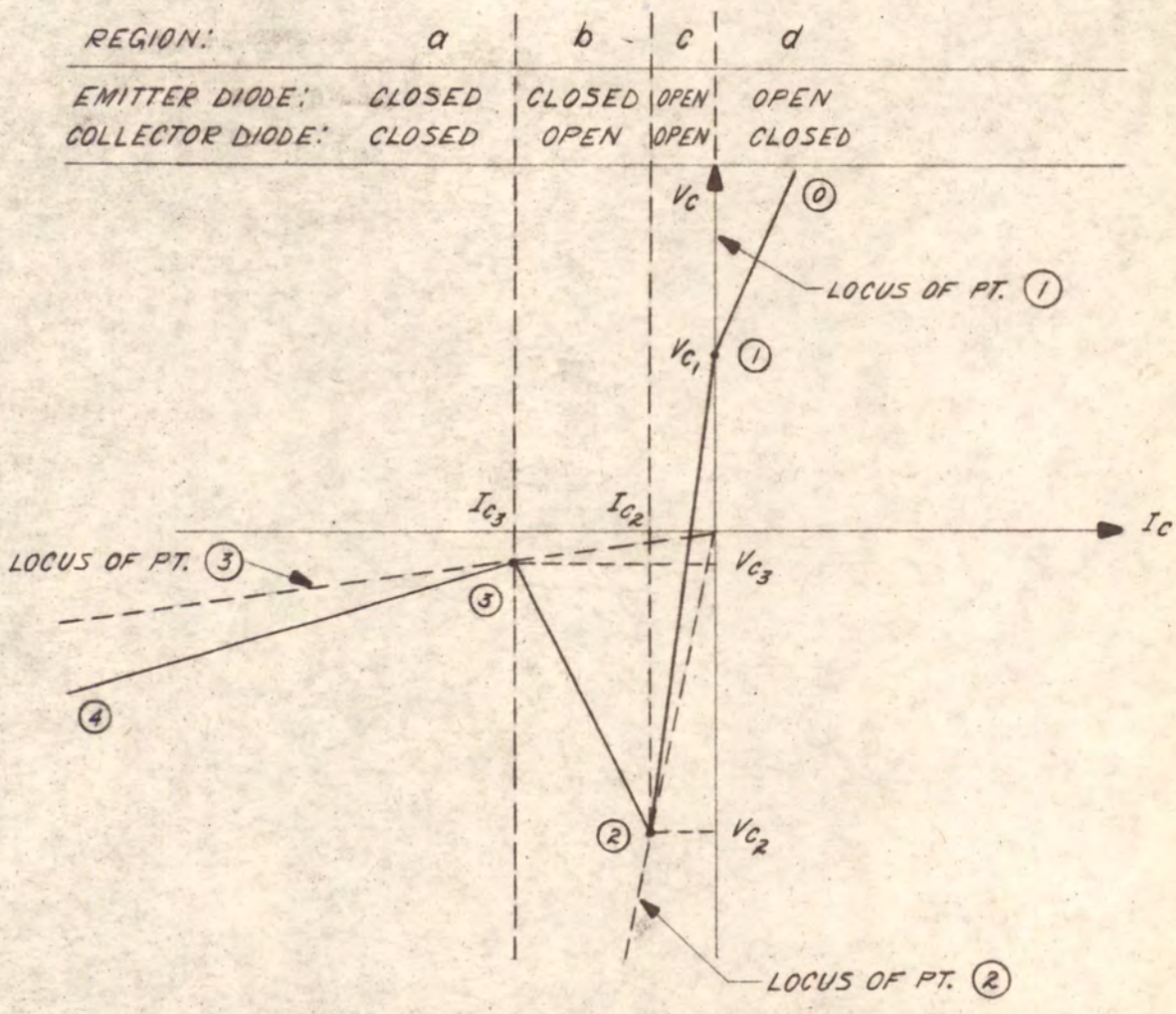


FIG. 5

COLLECTOR CHARACTERISTIC FOR $I_b > 0$

A-51135

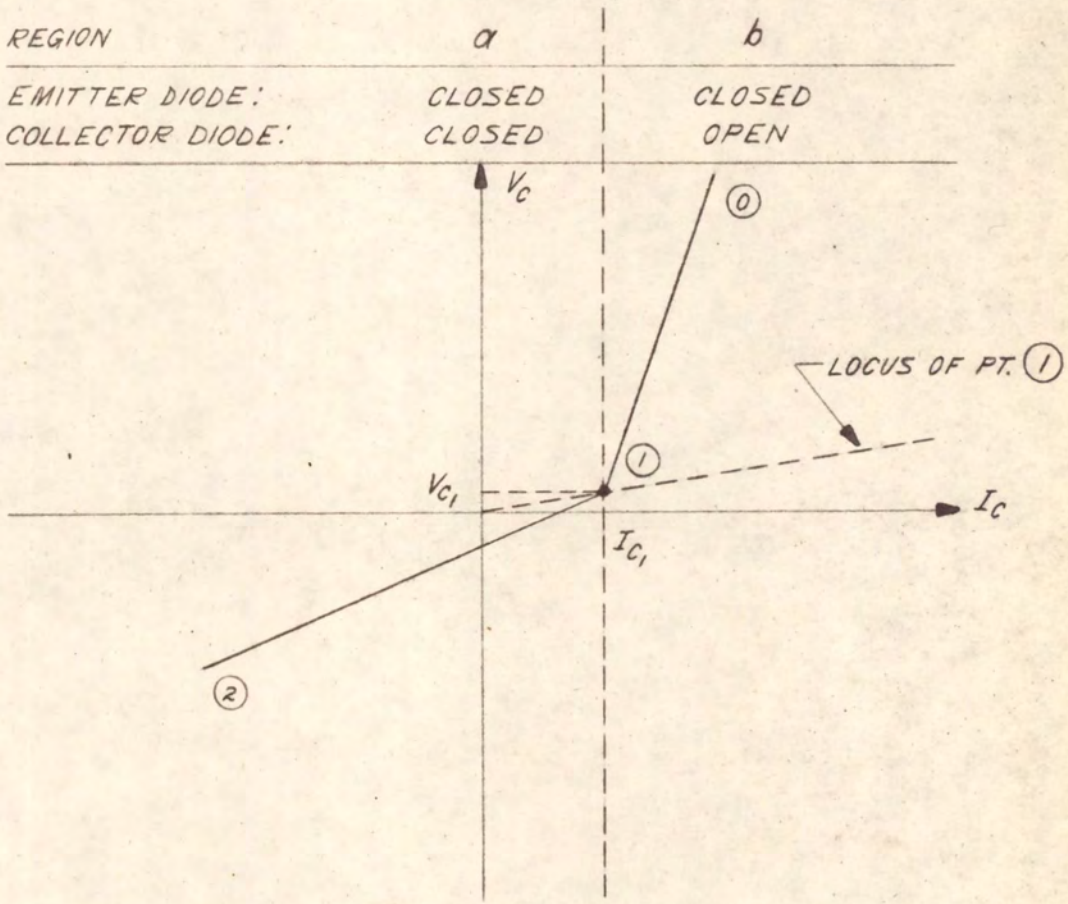


FIG. 6

COLLECTOR CHARACTERISTIC FOR $I_b < 0$

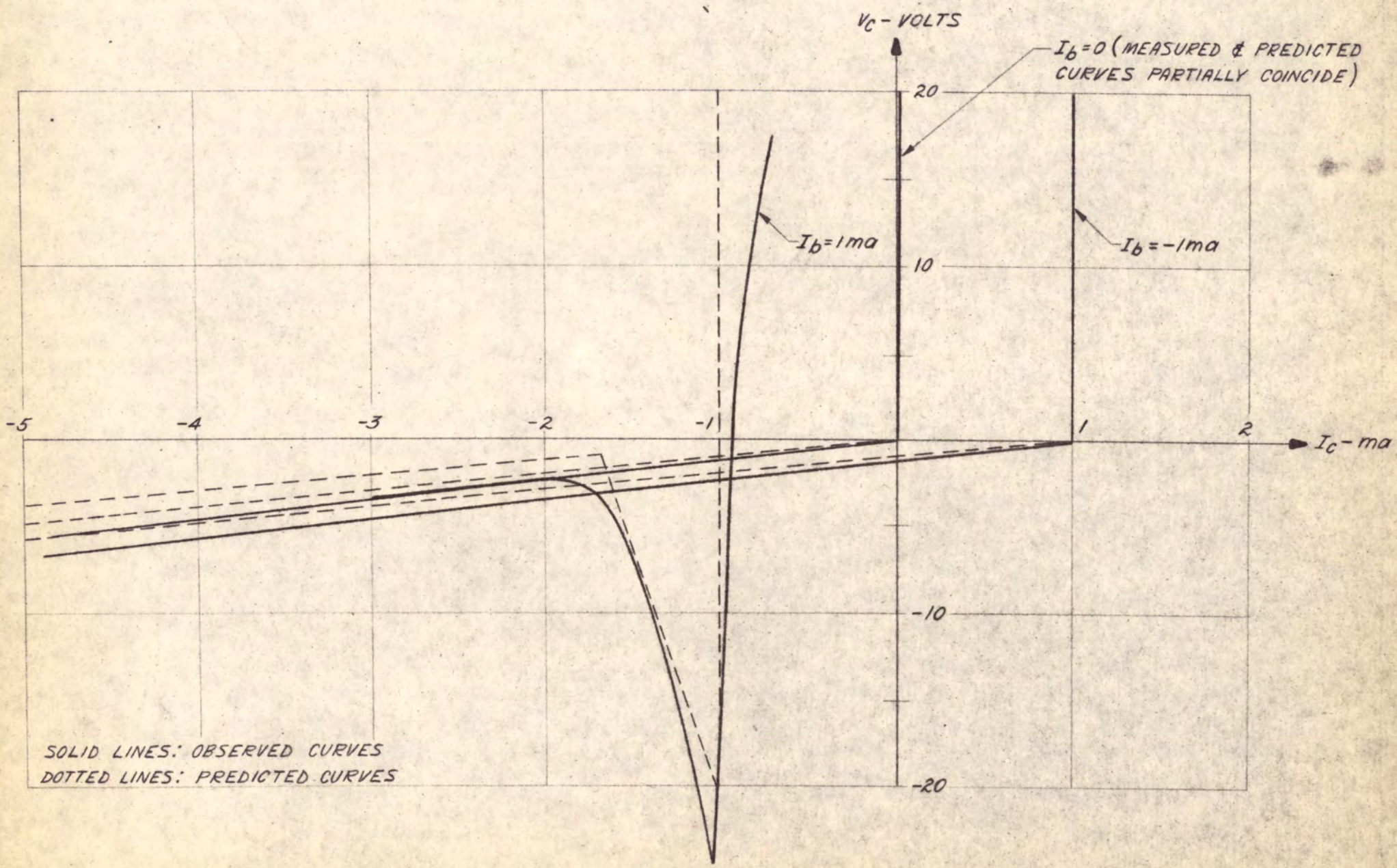


FIG. 7

COMPARISON OF PREDICTED AND OBSERVED COLLECTOR CHARACTERISTICS

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROCEDURE FOR RECEIVING MAGNETIC CORES

To: Group 63

From: David R. Brown

Date: May 16, 1952

Abstract: Two procedures are outlined. The first is for the receipt of one or a small number of cores submitted for evaluation. The second is for the case of a lot of cores where the particular body has previously been evaluated.

EVALUATION

1. Enter information in receiving record, magnetic-materials looseleaf notebook.

2. Tag each core. If more than one core with the same composition and processing is received, serial number the cores with color coding paints.

3. Label a container for core No. 1. This is to be used for the hysteresis test. Place the other cores in a separate, labeled container.

4. Make the hysteresis test on core No. 1, filling out form DL-439 as completely as possible. Be sure to measure the core before it is wound. Keep the tag on the core.

5. If the core looks promising and is suitable for pulse tests, make the pulse test. Use core No. 2, unless only one core has been received. For coincident-current memory application, use forms DL-435 and DL-446.

6. Place all data and curves in the magnetic-materials looseleaf notebook.

7. Place the cores, in containers, in the magnetic-materials storage cabinet.

ACCEPTANCE

1. Enter information in receiving record, magnetic-materials looseleaf notebook.

2. Label a container and place the lot in it. Select samples from the lot, tag and serial number them.

3. Pulse test the samples. For coincident-current memory application, use forms DL-435 and DL-446.

4. Accept or reject the lot.

Signed David R. Brown
David R. Brown

DRB/fes

Olsen-W

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: SIGNED TERNARY ARITHMETIC

To: J. W. Forrester

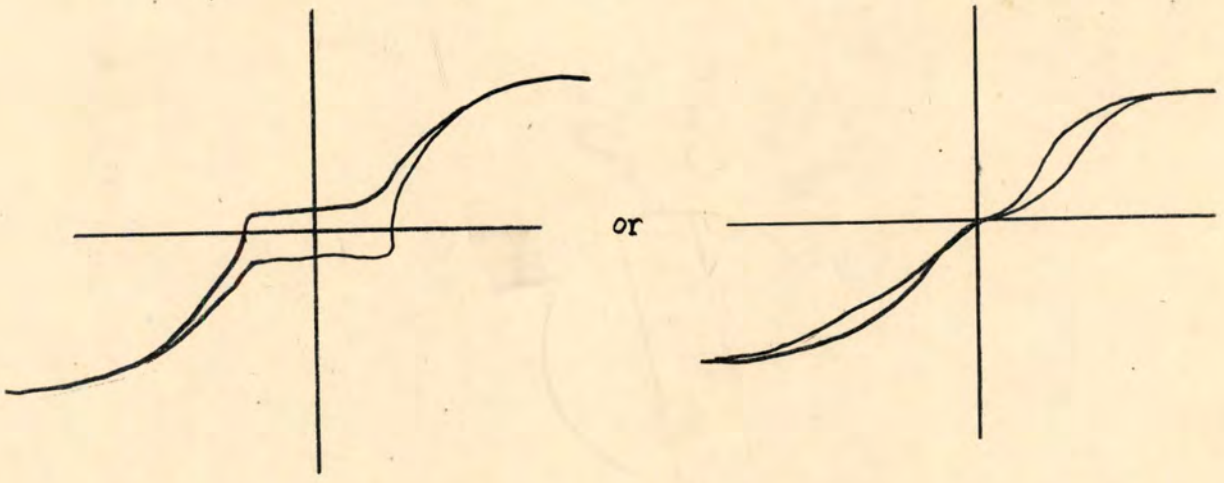
From: H. R. J. Grosch

Date: May 22, 1952

Introduction

Large digital calculating machines have been built to exploit the various advantages of pure decimal, binary-coded decimal, biquinary, and pure binary arithmetics. The availability of high-speed electromechanical and electronic elements having two stable states has been largely responsible for the swing away from the decimal number system.

Now we find ourselves increasingly interested in ferromagnetic and ferroelectric storage elements. There is a good possibility that these can be jockeyed into more than two stable, or better, "insensitive", states. Papian has shown me some B-H curves having the general forms



Such a material may be thought of as having three stable states. I have been interested for some years in the possibilities of a rather special sort of ternary arithmetic. This report is intended to give a resumé of its properties, and to advocate detailed consideration of its use in Whirlwind II.

Definitions

A real number is conventionally represented by a sequence of symbols.

$$A_4A_3A_2A_1A_0 \cdot A_{-1}A_{-2}A_{-3}$$

This is defined as having the value

$$A_4n_4 + A_3n_3 + A_2n_2 + A_1n_1 + A_0n_0 + A_{-1}n_{-1} + A_{-2}n_{-2} + A_{-3}n_{-3}$$

where the n's are the radices of the system. A convenient arithmetic requires that the A's and n's be rational numbers and that the representation possible therewith be both complete and unique over the real number field: that is, that every real number give rise to one and only one sequence of A's (not necessarily closed at the right, of course). The term "convenient" should be understood as referring to use on digital machines, which have a built-in prejudice in favor of the rational numbers. Unless at least one of the A's or n's is negative, it will be necessary to prefix the sequence with a minus sign to get over into the left half of the real number axis. No complementation convention can be adopted to get around this if a long repetition of arithmetic operations such as multiplication is required to yield answers consistent with the system.

The simplest forms of representation arise when all the A's are integers, and when the n's are monotonic non-decreasing. The radix point is placed to the right of an A (called A_0) whose corresponding base number n_0 is ± 1. Still more simplicity is gained when the n's are products of powers of a few integers. The abacus uses powers of two and five:

$$n_0 = 1$$

$n_1 = 5$ $\qquad$ $n_{-1} = 2^{-1}$

$n_2 = 2.5$ $\qquad$ $n_{-2} = 2^{-1} \cdot 5^{-1}$

$n_3 = 2.5^2$ $\qquad$ $n_{-3} = 2^{-2} \cdot 5^{-1}$

$n_4 = 2^2.5^2$ $\qquad$ $n_{-4} = 2^{-2} \cdot 5^{-2}$

etc. $\qquad$ etc.

This is also used in Bell and IBM relay calculators; it is called biquinary arithmetic. The A_i are either 0 or $\pm$ 1 for odd i, or from 0 to $\pm$ 4 for even i.

Finally, one may adopt a single positive integer radix r, so that $n_i = r^1$ and $A_i = 0, 1, \ldots, r-1$. The values $r = 2$ and $r = 10$ give

rise to the conventional binary and decimal systems, and r = 8 is familiar as an output system for "base two" machines. The unit base r = 1 is a degenerate counting system which cannot represent fractional numbers between -1 and +1, and in which many other features of the positional notation, such as rounding, become meaningless.

In conventional ternary arithmetic r = 3, $n_i = 3^i$, A_i = 0, 1, or 2. There are interesting possibilities, however, in using A_i = -1, 0, and +1; this "signed ternary" system fulfills the conditions of completeness and uniqueness, and possesses several properties which can be very useful in a large computer and which are not present in conventional positive-symbol arithmetics.

To simplify the writing of signed ternary numbers, special symbols can be helpful:

Λ ("lam") ≡ + 1

0 ("oh") ≡ 0

V ("vee") ≡ - 1

Thus ΛVV0.0V = +27-9-3-1/9 = +14 8/9 (decimal),

and V0.0VVΛVVVΛ000 = -3-1/9-1/27 + 1/81 - 1/243 - 1/729 - 1/2187 + 1/6561
= -3.14159.....

In the signed ternary system defined above, there are exactly 3^p different combinations of p symbols $A_{p-1}.....A_3A_2A_1A_0$. A demonstration that the system is unique will therefore prove completeness, or vice versa. By ordering all possible sequences of symbols, and by noticing that

$$\Lambda\Lambda\Lambda\Lambda\Lambda\ ..... = \sum_{i=0}^{p-1} 3^i = 1/2(3^p - 1),$$ either one of these proofs can

be carried out.

Finally, it may prove amusing to recall the old mathematical recreation of finding the minimum number of (integer) weights which, when placed in either pan of a balance, will weigh any (integer) unknown up to a certain limit. There is a perfect correspondence with signed ternary arithmetic!

Arithmetic

For practical two-quantity addition the following tables are required:

1. If there is a carry Λ from previous position,

		ADDEND		
		Λ	0	V
AUGEND	Λ	Λ 0	Λ V	0 Λ
	0	Λ V	0 Λ	0 0
	V	0 Λ	0 0	0 V

Right-hand symbol is digit of sum.
Left-hand symbol is carry to left position.

2. If the carry from previous position is 0,

	Λ	0	V
Λ	Λ V	0 Λ	0 0
0	0 Λ	0 0	0 V
V	0 0	0 V	V Λ

3. If the carry is V,

	Λ	0	V
Λ	0 Λ	0 0	0 V
0	0 0	0 V	V Λ
V	0 V	V Λ	V 0

A practical addition example looks like this:

VO.OVVΛVVVΛ (-3.1416.....)
ΛΛ.ΛΛΛΛΛΛΛΛ (+4.4999.....)
0Λ.Λ0ΛV00ΛV (+1.3583.....)

Subtraction will almost always be accomplished by complementing the subtrahend and adding. Complementation is performed by changing all

Λ's to V's and vice versa.

Multiplication is accomplished by shifting, complementation, and addition in a way very similar to multiplication in pure binary. No over-and-over addition is required. If the current digit of the multiplier is Λ , the multiplicand is added; if 0, ignored; if V, subtracted (complemented and then added); the partial product is then shifted one position to the right and the next digit of the multiplier examined in like manner.

ΛV0Λ.	+ 19
V0ΛV	- 2.78....
VΛ0V	
ΛV0Λ	
0000	
VΛ0V	
VΛ00Λ.ΛV	- 52.78....

In case single-digit multiplication is required, the table is as follows:

$$\Lambda \times \Lambda = V \times V = \Lambda$$

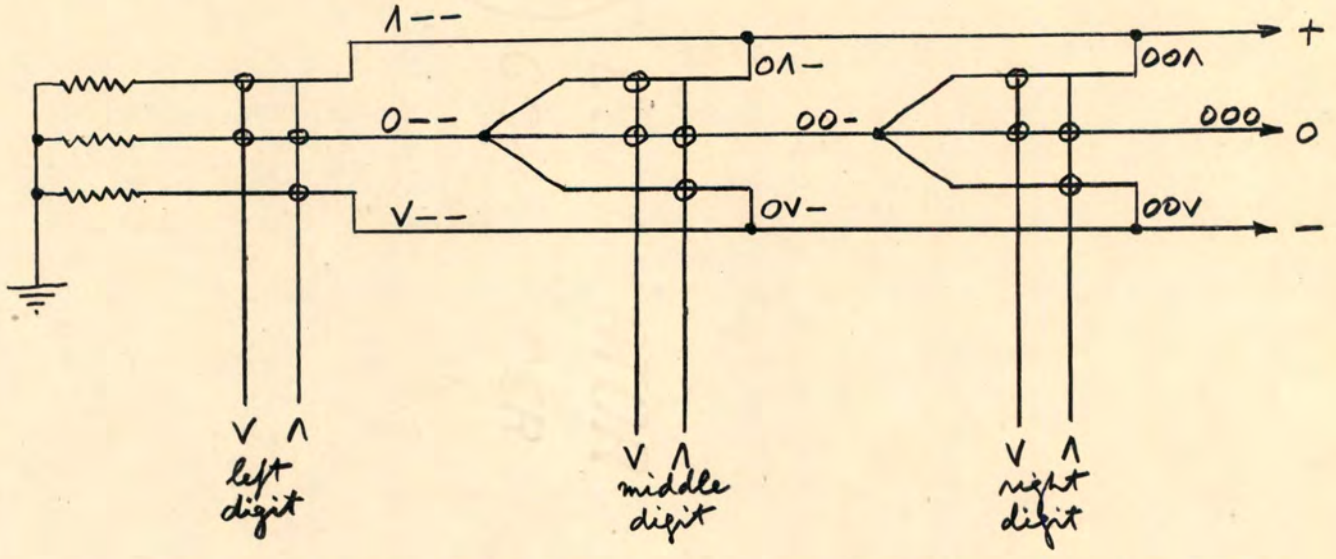
$$\Lambda \times 0 = 0 \times \Lambda = 0 \times 0 = V \times 0 = 0 \times V = 0$$

$$\Lambda \times V = V \times \Lambda = V$$

The arithmetic of division is by no means so easy. In fact, it probably would not be too pessimistic to say that the introduction of signed symbols makes most arithmetic operations simpler at the expense of more complicated division. Since division occurs so infrequently, there is a temptation not to build it into a machine; this temptation is very strong in the present signed ternary case.

One elementary but wasteful method of division is to start at the extreme left quotient position (assuming as usual that the dividend and divisor have been suitably positioned). This exposes the fundamental difficulty of signed-symbol division clearly: is the divisor to be added or subtracted? Once the process has started correctly, so that the remainder tends toward zero, an alternation of adding and subtracting will be sufficient; the catch is to choose the first "direction" correctly.

In order to transform signed ternary to conventional binary or decimal output, some sort of sign determination is required. In a fast machine this determination should be parallel, and by determining successively the signs of the dividend and division we can set up the start of the division process. One diode network capable of doing the sign determination requires four diodes per digit, but this can probably be reduced to three cores if a long string of cores can be made to flip domino-fashion. The diode array for three digits is



In a two- , three- , or four-address machine two of these networks would be required.

Given the sign of the dividend and of the division, a simple logical combination embodies the rule: if the two signs agree, start by subtracting (complementing and adding) the divisor; if they disagree, start by adding. Shift the divisor one position to the right and "reverse" (add instead of subtract, or subtract instead of add) whenever the remainder changes sign. In detail, then,

V1.V1 = V0.1V (-2 7/9)

(+19) 1V01. | V100V1.1V (-52 7/9)

1V01 (+5)

001V1.1V (+4 2/9)

V101 (-19)

01V10.1V (-14 7/9)

1V01 (+6 1/3)

00V01.VV (-8 4/9)

1V01 (+6 1/3)

001V1.01 (-2 1/9)

1V01 (+6 1/3)

001V1.1V (+4 2/9)

V101 (-2 1/9)

0011V.01 (+2 1/9)

V101 (-2 1/9)

00000.00

It will be evident that for randomly distributed n-digit quotients 2n additions and subtractions will be required, three times as many as the irreducible minimum 2/3 n. Undoubtedly much simpler processes can be evolved.

Given the arithmetic operations and a sign-determining network, and reserving three ternary digits to represent a decimal digit, transformation into and out of the conventional decimal system poses no special problems. After the sign of the number is determined and stored, the number is complemented to positive form if necessary. Three signed ternary digits cover the range -13 to +13 decimal, and only 0 to +9 decimal is required.

Advantages

It may be easily shown that three is the most economical radix of all single-integer-radix systems. If two elements can store a binary digit, and three a ternary digit, the ratio of equipment is 1.500 and the ratio of information stored is $\log_2 3$ or 1.585. Comparing quaternary and ternary on the same basis, one finds an equipment ratio of 1.333 and an information ratio of $\log_3 4$ or 1.262. This argument of economy applies to components such as tubes, diodes, and electromechanical gadgets. If core materials with three "insensitive" states are feasible, the gain of 1.585 in information stored compares with an equipment ratio not much over 1.000 for a large memory.

Is it really true that the outside world is best represented by dichotomies? Computing machines are basically logical, the argument runs, and the logic of the real universe is two-valued. My idea, on the contrary, is that computing machines operate on the basis of a logic concerned not with the real world, but rather with a special representation of the world by rational real numbers. And there are three relationships between pairs of rational numbers: X less than Y, X greater than Y, and X equal to Y. Putting it another way, zero is a member of the class of rational real numbers but is not a member of either the positive or negative subclass. Thus there is some real support for the theory that, while computer arithmetic may be done in any radix system, computer logic is basically ternary.

In real-time control applications the original conversion from continuous to digital representation is the place where the special representation by rational real numbers is introduced. There is of course no reason why the fundamental counters or other transformation devices cannot be ternary, with the same favorable equipment ratio as the central computer. As for the transmission of digital information, there is little doubt that more data can be transmitted over a given channel. Consider the old system of transmitting sixteen binary digits, frequency multiplexed, over a single phone line. If a single frequency is reserved for a fundamental continuous reference sine wave, the other fifteen frequencies can be phase-compared

with this reference to give signed ternary digits: in phase represents Λ, 180° out of phase represents V, absence of signal represents 0. These fifteen ternary digits are equivalent to 23.77 bits, a gain of 48.6 per cent. It may be useful here to give the following tabulation:

1 binary digit (bit) = 0.631 stits = 0.301 dits

1 signed ternary digit (stit) = 1.585 bits = 0.477 dits

1 decimal digit (dit) = 3.322 bits = 2.096 stits

So much for what might be called the philosophical advantages of the signed ternary system. There are even more attractive arithmetical advantages. One, which has been mentioned earlier, is the elimination of a special "sign" representation. This makes it unnecessary to decide whether to shift the sign when shifting the rest of the number. In a sense, the left non-zero digit may be thought of as the sign, and this is convenient for the operator or customer. There is no longer any difference between a "negative" number (that is, a positive number with minus sign prefixed) and a complement: also there is no such thing as an end-around carry, and no difference between "nines"and "tens" (or rather, twos and threes) complements.

These advantages would accrue to any practicable signed radix system where zero is near the center of the ordered set of symbols A. Signed ternary, however, is the largest radix which will permit multiplication to be done without over-and-over addition.

Since the base of the system is an odd number, the representation of 1/2 is a repeating ternary - that is, 1/2 is not one of the class of rational real numbers representable by a finite computer. This has inconveniences, but it eliminates the problem of ambiguous rounding. In the decimal system, for instance, one rounds 6.49 to 6 and 6.51 to 7, but what does one do with 6.50? Adding 0.50 will often introduce a statistical bias and render error estimates based on random rounding errors unsatisfactorily optimistic.

In fact, signed ternary arithmetic completely eliminates the operation of rounding: rounding and dropping are identical operations. Thus ΛΛ.VV(+ 3 5/9) rounds to ΛΛ (+ 4) by dropping the last two digits; Λ0.ΛΛ (+ 3 4/9) rounds to Λ0 (+ 3) similarly. Any leftmost portion of a number is therefore the correctly rounded less-accurate representation of that number, a profound advantage in floating-point calculations.

Conclusion

This short introduction to the features of signed ternary arithmetic glosses over many points of interest. There has been no attempt to tie in three-valued logic, nor has there been any attempt to point out the possible advantages of ternary-coded decimal, nonary, or other bastard form

The next stage is obviously a discussion of hardware: core circuitry, ring-of-three counter elements (flip-o-flops?), magnetic tape storage, and so on.

H. R. J. Grosch

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HRJG:ajg