H. E. Anderson
B-147



Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A PROPOSAL FOR TRAINING YOUNGSTERS IN DIGITAL COMPUTING TECHNIQUES

To: Distribution List

From: R. P. Mayer

Date: 18 September 1956

Approved: K. E. McVicar

Abstract: The current and predicted shortage of people familiar with and trained in computer techniques may be alleviated by beginning training at the elementary school level. It is demonstrated that the average 12-year old youngster can learn basic concepts of digital computers if inexpensive models, properly prepared instruction manuals, and technical magazines designed for his age level, are made available.

The basic philosophy of inexpensive construction of computer components is outlined and demonstrated with working models made of cardboard and common pins.

This is a preprint of a paper presented at the Association for Computing Machinery Conference in Los Angeles on 29 August 1956.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The proposal outlined here is based on three premises: (1) That the digital computing field needs, and will continue to need, not only more people who are capable of designing and programming digital computers, but more people who understand the basic limitations and potential uses of digital computers; (2) that the computer industry should take an active interest in providing a basic computer training to the largest number of people, in addition to more extensive training to those who show an interest in designing and programming computers; and (3) that the typical 12-year-old youngster has the interest, skill and basic knowledge necessary to build and understand simple working models of practically anything.

Consider a typical 12-year old: You would not be surprised to learn that he's been flying gliders for years, has probably built at least one rubber-powered stick model airplane, and is wondering whether he should spend his allowance on a more fancy model. At this age, he can take his bike apart and put it together again, diagnose and often correct a short circuit on his friend's electric train, build a bridge with his Erector set, and can develop and print pictures taken with his own box camera. He knows the difference between a rocket and a jet, alternating current and direct current, telescopes and microscopes, and between a gasoline engine and a diesel. For a small sum of money - often less than $20 - he can buy himself a working model of any of these things, plus a subscription to a magazine which will keep him informed of progress in the real devices, in the models, and in ways of using and improving the models. It is not surprising to find such youngsters entering the aeronautics, automotive, and electronics industries.

But when it comes to digital computers, our youngster is rather out of luck. He can buy a 4-digit decimal adder for a dollar; but this is hardly inspiring. The cheapest drum storage he could get costs more than his father's automobile.

It becomes apparent that our youngster needs a well-rounded computer package consisting of three parts: (1) a full line of cheap, standardized, general-purpose, digital computers in plan, kit, and assembled forms; (2) a full line of simple instruction manuals; and (3) one or more magazines, sponsored by the computer industry and designed especially for youngsters, covering coded programs for new and interesting problems, discussion of ways of making improvements and modifications to the models, etc.

Given the models and manuals, as described below, the magazine should be clearly written and profusely illustrated. It should stimulate continuing interest in computers by informing the youngsters about new full-scale computers and new problems being handled by them, and by providing a way for the youngster to exchange ideas on logical changes in the models and their in-out devices; on uses of the model around the house, in schoolwork, and for games; and on programming and mathematical tricks.

Each kit or model would include a complete instruction manual especially designed for that kit. General instruction manuals on construction, logic, coding, mathematics, and applications should also be made available. It is proposed that these manuals should be not only very easy for youngsters to understand, but should be exciting, too, even for those who dislike arithmetic and mathematics, and that they should represent the computer as a powerful tool which can be used in many fields, rather than as an end in itself.

The manuals will be easy to understand if care has been taken to explain the simple relationships between basic elements which the youngster is sure to know. Youngsters are normally not taught calculus until after they understand arithmetic and algebra. But with a calculator at their fingertips, capable of doing the arithmetic automatically, such a sequence of training may not be necessary. For example, it should be easy for them to understand a well-designed description of basic relationships which will train them how to use their computer to solve problems normally handled only by advanced calculus. Remember, we teach six-year-olds how to use numbers without teaching them advanced number theory.

The magazines and manuals discussed above are based on the availability of cheap, interesting computer models. These should be made in standardized sections which can be bought separately and pieced together to form an increasingly useful computing system. Each section should cost no more than $5 with several basic demonstration sections at $1 each or less. Typical sections might include: (1) A 32-register, 8-bit, 4-instruction, display-screen-output basic computer; (2) a 1,024-register, 8-bit storage; (3) a 32-instruction control; (4) an 8-bit multiply-divide arithmetic element; (5) analog and digital inputs; (6) analog and digital outputs. Two storage and arithmetic sections would be required to provide a full 16-bit machine. Thus, a typical full-scale model with eight sections would cost about the same as a bicycle. The speed of such a machine might easily be faster than ten instructions per second.

The design goals mentioned above can be met by adhering to several basic principles:

First, the computer should be mechanical. Basic computer techniques can be easily observed on functioning mechanical parts. Parts can be easily and cheaply made by youngsters out of paper, or mass-produced as plastic or metal stampings. For example, $3.40 buys enough pins for 1,024 8-bit registers. Second, the computer should be binary. The ease of making such parts outweighs the necessity for teaching the binary system to the youngster, who will learn it readily enough.

Third, all action should be positive and should not depend on friction, inertia, or springs. This allows the parts to work at any speed - as slowly as you wish for demonstrations, and as fast as you wish, limited only by the strength of the materials and of the drive motor. The use of springs tends to increase the forces required to drive the device. The use of positive action allows several steps to be performed on the same input pulse, perhaps allowing a complete single-address instruction to be performed on each input pulse.

Fourth, and finally, the parts should be made as small and light as possible, consistent with strength, manufacturing tolerances, and ease of repair of observation. Lighter parts have less inertia and can be driven faster or with less power.

A number of experimental models of logical circuits built according to these principles will now be discussed.

Figure 1 shows an 8-bit register cut from paper. Each bit operates as a toggle element whose spring is formed by bending the central strip of paper into a Z-shape. This violation of the no-spring principle might be justified if a large memory can be made so simply. The selection of a given register would be done by moving the register to the left. Read-in would be accomplished by moving a digit bus (not shown) upward or downward. Read-out would be accomplished by allowing the tab of each bit to engage a light-weight output bus. Note that read-out would not tend to disturb the setting of the toggle.

Figure 2 shows a more reliable, but more costly, 8-bit register. Each bit is represented by a pivoted arm whose position is locked by tabs on the locking bar. Selection, read-in, and read-out are accomplished simply by moving the register to the right. Both ends of each pivoted arm would then come in contact with two halves of a corresponding digit bus (not shown) so that the arm and the bus would be forced to the same angle: If the locking bar is moved forward with the register then a positive read-out takes place, but if the locking bar is not moved forward, then a positive read-in takes place.

Figure 3 shows three such registers mounted in their frame. This is the state of progress on a demonstration model which will consist of thirty-two 8-bit registers, a selection counter, and a Charactron-style output display made of cardboard and bits of mirror. It will be used to test the speed and reliability of a small system and the feasibility of sectional, expandable construction.

Figure 4 shows one type of AND circuit. The "secondary flip-flop" assumes the position of the "primary flip-flop" only when the circuit is not being operated. While the circuit is being operated, the "primary flip-flop" may be altered as much as desired without affecting the output signals.

Figure 5 shows an adaptation of this basic AND circuit to form a one-stage binary counter. The primary flip-flop is set and cleared by the output pulses, thus causing it to be complemented on each input pulse. The primary flip-flop is locked while the secondary flip-flop is sensing it.

Figure 6 shows a model of this binary counter cut from 3 x 5 card stock, pivoted with common pins, and connected to a drive motor. A cover plate holds the parts together. This model has been run at 40 cycles per second, for over an hour at no load. Only slight wear is evident in the counter itself, operating margins have deteriorated only slightly, and it looks like it might last another hour or more.

These are typical of the inexpensive computer elements which can be used to intrigue and train the 12-year old, who, by the time he graduates from high school will be able to perform many of the tasks for which graduate engineers are now employed.

When you consider the remarkable interest in computers that would be generated by the ready availability of a computer, and of instruction in its use, to any 12-year old, the computer industry should be happy to provide whatever moral, technical, and financial support is necessary to provide the most reliable and workable standardized models, the most eagerly read manuals, and the most interesting magazines.

How long will it be before a teenager appears at the local airport complete with radio-controlled model airplane, acoustical tracker, and computer-controlled stunt patterns?

Signed: R. P. Mayer
R. P. Mayer

RPM:hpm

Attachments:

Drawing A-66192-1
[illegible] A-67510

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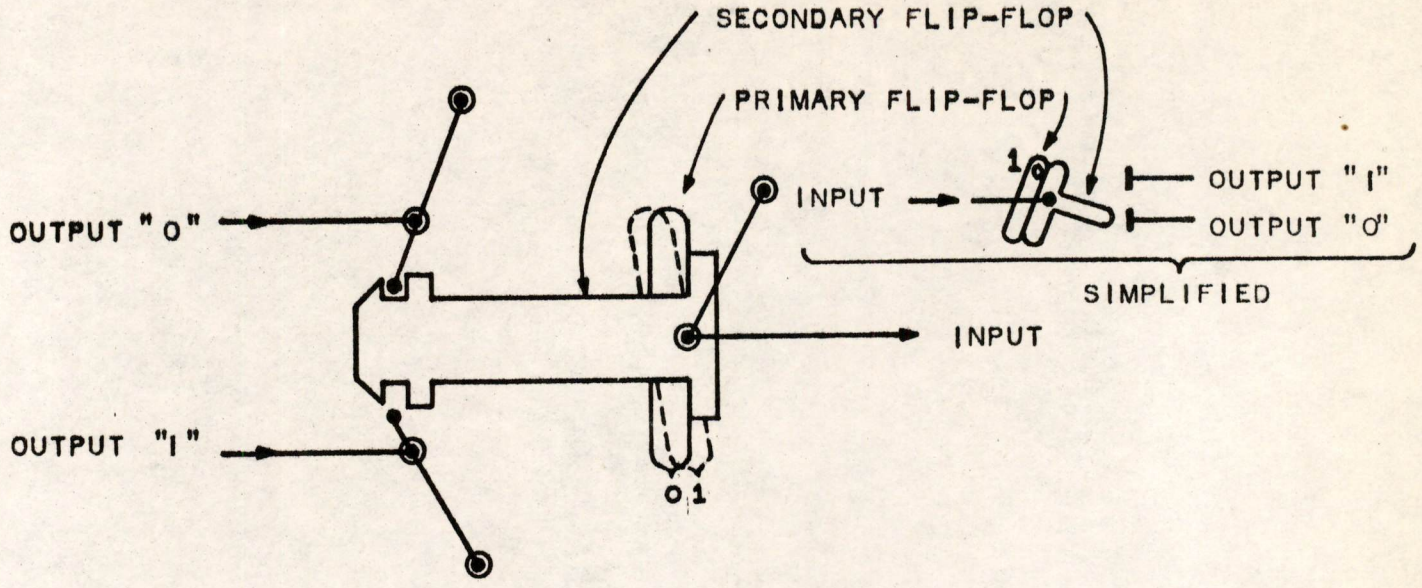
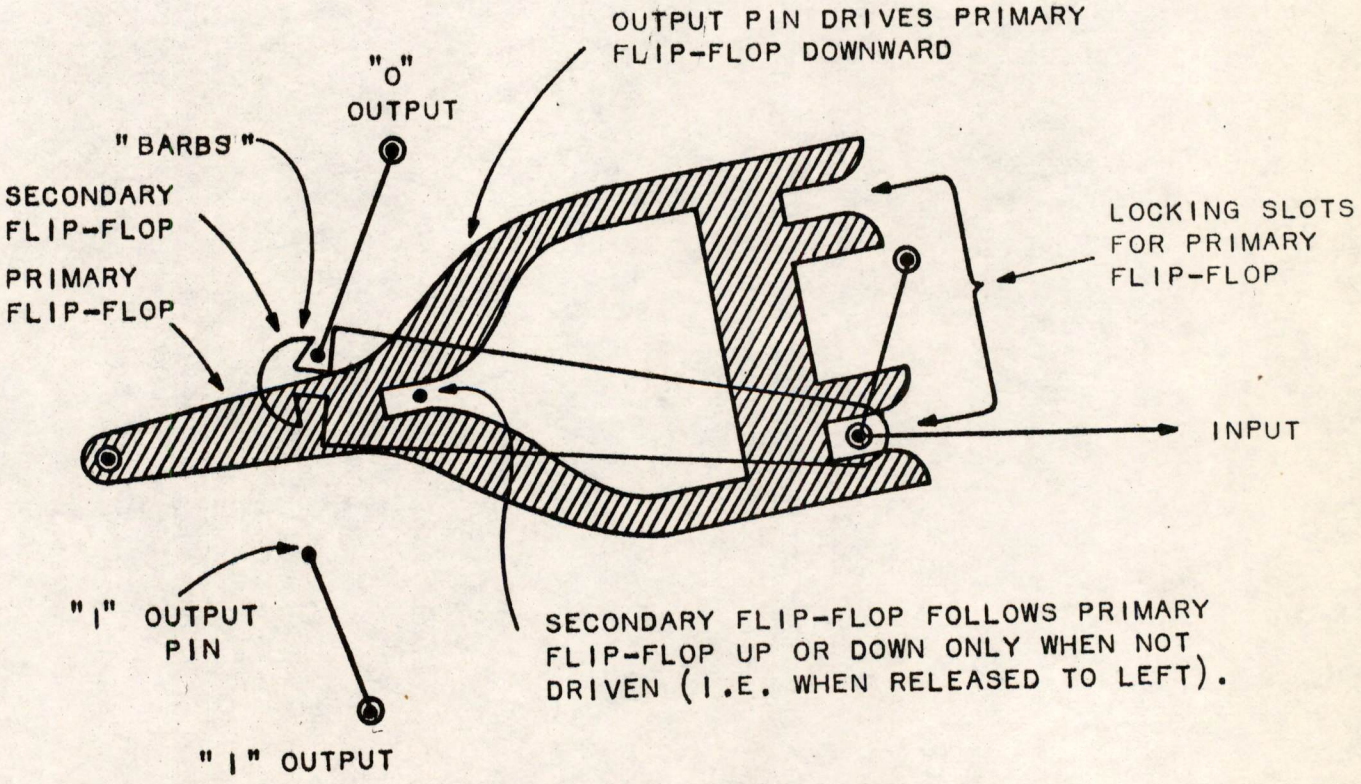
ALL PERSONS LISTED ABOVE ARE TO RECEIVE COMPLETE MEMO




BASIC "AND" CIRCUIT




BINARY COUNTER

A- 67510

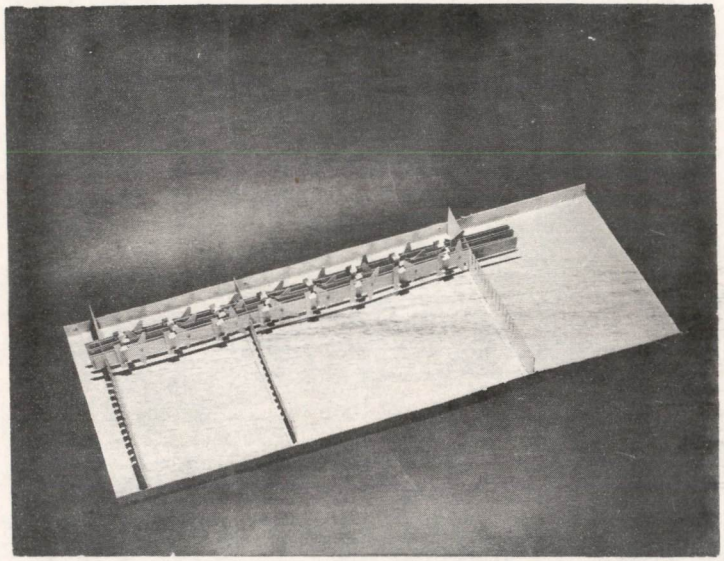


Fig. 3 Three 8-Bit Registers Mounted In Their Frames

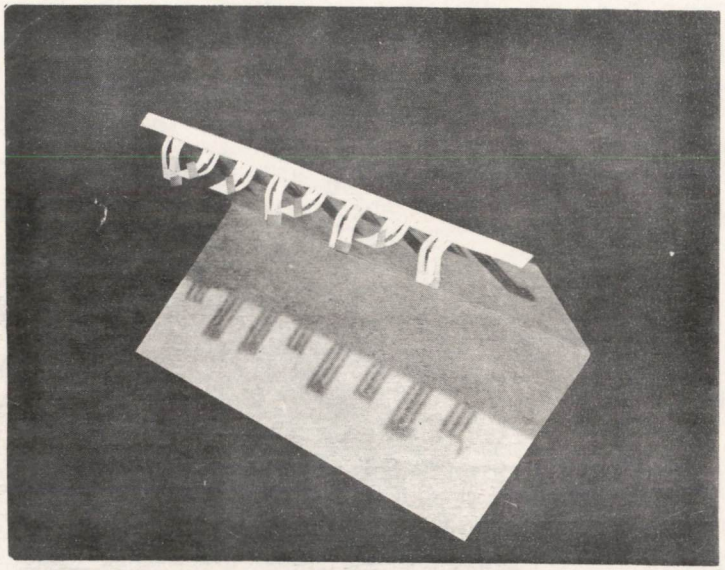


Fig. 1 An 8-Bit Register Cut From Paper.

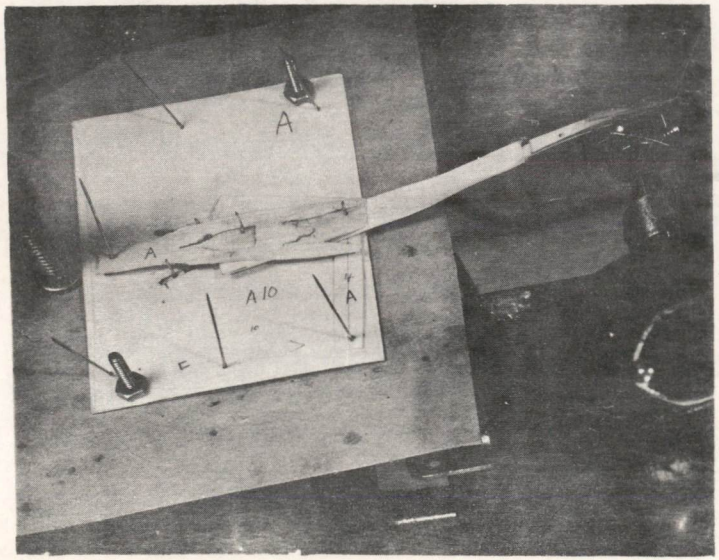



Fig. 6 Binary Counter Cut From 3x5 Card Stock.

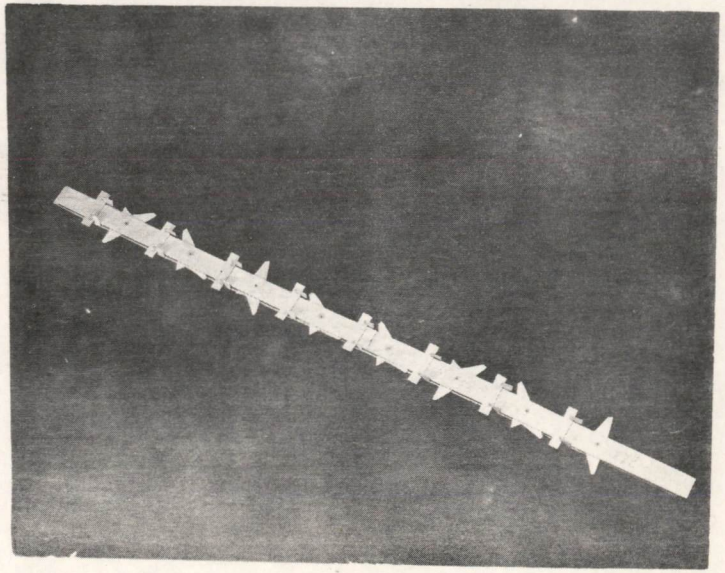


Fig. 2 A More Reliable, But More Costly, 8-Bit Register.

R. L. Best

Memorandum 6M-4713



Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: Lincoln TX-2 Computer

To: R. R. Everett

From: K. H. Olsen and W. A. Clark

Date: September 25, 1956

Approved: W. N. Papian

Abstract: The Lincoln TX-2 computer will be a full-scale computer of great flexibility utilizing 5-mc transistor circuits and a very large internal store. The computer is a binary, parallel, single-address machine with two separate magnetic-core memories and a 36-bit word length. It will have wide-spread application to SAGE-related studies, and longer term uses in fundamental research and development in advanced data-processing systems.

Distribution:

Division VI - Division Heads and Group Leaders
Group 63 Section Chiefs



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## INTRODUCTION

Construction of the Lincoln TX-2 computer is the next step in the Group 63 program for the study and development of advanced digital-computer systems. Like the TX-0, its precursor in this development program, the TX-2 will use 5-mc transistor circuits (though in an improved form) and the 256 x 256 magnetic-core memory. Unlike the TX-0, which is a skeletal machine of near-minimum complexity, the TX-2 will be a full-scale computer of great power and flexibility.

Parallelism of operation is significantly greater in the TX-2 design than in existing computer systems. This increased parallelism, or ability to carry out many diverse operations simultaneously, is an important advance in the computer field. It will give the TX-2 a peak operating rate which is nearly four times that of the AN/FSQ-7 for certain programs.

Table I summarizes the important characteristics of the TX-2.

## APPLICATION

Operation as well as the development of the Lincoln TX-2 computer will further the goals of the Laboratory. The following outline, which does not attempt to describe the topics in detail, lists some of the applications of the TX-2 in the areas of SAGE-related studies and in non-programmatic research and development.

I. SAGE-Related Shorter Term Applications

A. Hardware evaluation and development

1. New display equipment
2. New memories
3. Packaging and circuit experiments
4. Special input-output devices

B. Simulation of SAGE Equipment

(Special data-processing equipment suggested for use between radar, or radar nets, and central computer)

C. Self-Evaluation of TX-2 System

1. Multiple program-counter logic
2. Parallelism of arithmetic elements
3. Memory heirarchies

II. Long-Term Research and Development



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

II. Longer Term Research and Development

A. Improving communication between human and machine

1. Speech recognition
2. The coding language study
3. Computer-aided problem formulation
4. Electroencephalography experiments

B. Shifting higher level processes from human to machine

1. Perception model study
2. Machine learning study
3. Automatic management of computing installation

C. Computer system theory

1. Formulation of computer models
2. Simulation of advanced systems
3. Neuron network studies

## SCHEDULE

The attached time schedule indicates a "delivery" time about a year from now.

Below is a rough estimate of the costs which will have to be met from the Division VI Extraordinary Budget for fiscal 1957.

TX-2

Extraordinary Costs

| | | |
|---|---|---|
| Frame and console | (ordered) | $ 2,600. |
| Plug-in unit parts | (ordered) | 3,000 |
| Etched boards | | 30,000 |
| Plug-in assemblies | | 37,500 |
| SBT Transistors | (ordered) | 52,500 |
| SBT Transistors | | 82,500 |
| SBTT Transistors | | 20,000 |
| Condensors | | 2,400 |
| Plugs & sockets | | 8,700 |
| Misc. parts | | 15,000 |
| | TOTAL | $ 254,200 |

Personnel (full time)

| | |
|---|---|
| Logical design | 2 staff |
| System design and assembly | 3 staff, 1 STP, 10 technicians |

TABLE I

TX-2 Characteristics

| | |
|---|---|
| Type | Binary, parallel, single-address |
| Word length | 36 bits (fracturable under program control to 2 18-bit words or 4 9-bit words) |
| Storage (coincident-current magnetic-core arrays 7μs cycle time or less) | Mem. 1: 65,536 37-bit words (36+ parity bit)<br>Mem. 2: 4,096 37-bit words (36+ parity bit)<br>(expandable to 65,536 words)<br><br>Mem. 1 and mem. 2 operate simultaneously and independently. |
| Indexing system (magnetic-core array, 1μs access time) | 64 18-bit index registers |
| Input-output | Initially - 2 paper tape-readers<br>2 auto. typewriters<br>2 c.r.t. display systems<br>2 magnetic-tape transports<br><br>System easily expanded and extremely flexible. All devices may be concurrently operated. |
| Operating speeds (peak rates for typical instructions) | Additions/sec. 150,000 (36-bit words)<br>300,000 (18-bit words)<br>600,000 (9-bit words)<br><br>Multiplications/sec.<br>100,000 (36-bit words)<br>300,000 (18-bit words)<br>600,000 (9-bit words) |

Attachment:
Drawing - B-67527

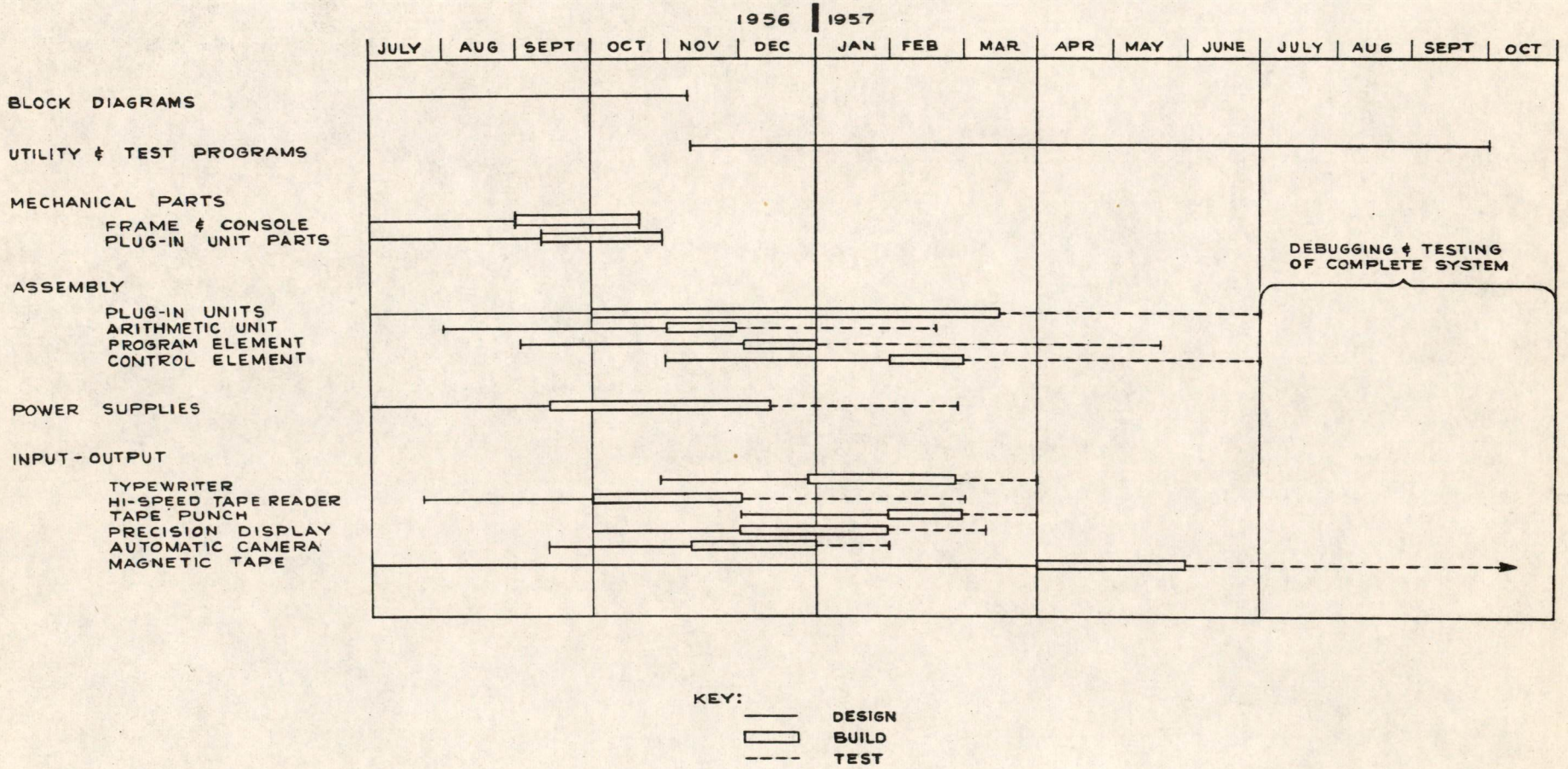
Signed W. A. Clark

K. H. Olsen

WAC:KHO:mk

B-67527

# TX-2 TIME SCHEDULE



S. C. Olsen



Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: RESULTS OF INVESTIGATIONS TO IMPROVE RELIABILITY OF THE MTC TAPE SYSTEM

To: J. A. O'Brien

From: T. C. Stockebrand

Date: 5 November 1956

Approved: H. L. Ziegler
H. L. Ziegler

Abstract: Difficulties have been encountered by MTC and XD-1 with their tape systems. An investigation has been made to determine the sources of error. Findings are as follows:

1. Apparently coupling between the write busses and read busses of the Tape Adapter Frame caused some errors. This situation has been cleared up with an IBM engineering change.

2. Pickup of an extra bit after a "one" preceded by a long burst of zeros occurred. A transistor gate at the input of the preamp to "gate out" these transients allowed changes to improve signal fidelity.

3. The tape reels seem to warp with time and abuse and thus cause chafing at the tape edges. The consequent wrinkles in the outside tracks produce errors. Tape reel holes and/or reel clamping mechanisms apparently are not controlled closely enough with the result that operators sometimes bend the reels in forcing them on the machine.

4. Some errors arise from the vagaries of the tape head environment. Preliminary results indicate that most errors arising from this environment are due to gradual build up of oxides on the heads or on the tape and not due to appreciable deterioration of the magnetic image on the tape. Checking of each machine for excessive wearing of tape due to rough head surfaces; regular cleaning of heads; proper reading programs; and the selection of a new type of tape, may allow ten times more error-free passes of a given piece of tape over the heads. In a rather restrictive situation we have achieved 60,000 readable passes using a hi-output tape similar to Whirlwind's, but with a lubricated binder.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

MTC PROGRAM USED TO CHECK TAPES:

Tests on the MTC tapes have been carried out with the aid of a computer program designed to be simple yet create conditions which are difficult for the tape drives. The program alternately writes, backspaces, then verifies what has been written. The same word is written repeatedly to form a record of any desired length. The composition of this word can be changed at will. The program is difficult for the tape system because the sync track channel must be operative very soon after the transition from write to read status (about 6 milli-seconds). The program cycle time is less than one hundred milli-seconds (if the record length is short) so that the delayed-sweep feature of the 545 Scope can be used to examine any waveform during the whole cycle of operation of the program. This program was used for all the tests of MTC's tapes.

NOISE BURSTS:

Each tape drive contains seven preamplifiers (one for each channel) to amplify the 30 mv (peak-to-peak) signal read from the tape to a 20v (peak-to-peak) signal for use by the Tape Adapter Frame. Illustrated in the bottom two sections of Figure 1, are the outputs of two sample preamplifiers before any modifications were made of the system. Figure 2 is an enlarged view of one section of the curves in Figure 1 -- the signal during the actual reading. A close look at the middle picture in Figure 2 will show that noise bursts exist between the information pulses. It was found that these small bursts occurred at the same time as did the transitions between the various "word ring" conditions of the tape control as reading progressed. D.C. levels of the write busses are free to change during read time and do so during the transitions between "word ring" conditions (especially at the end of WR #1 time). Apparently coupling exists between the write and read busses and the noise bursts are a result of this coupling. IBM found that some errors could be eliminated by preventing the write-buss levels from changing during "word ring #1" time. We tried the same correction. This eliminated our errors from this source, though it did not remove all the noise bursts. Since then IBM has developed an official engineering change to clamp all write busses during read time. This circuit should eliminate the rest of the noise bursts.

OVERSHOOTS:

When the spikes had been eliminated as a source of error in MTC, a second type of error showed up. This was bit pickup immediately following an isolated "one" preceded by a long burst of zeros. Examination of the signal presented to the clipping stage showed that an overshoot occurred after any pulse. This was in some cases large enough to be recorded as a bit. Figure 2 shows the overshoot phenomenon at the preamp outputs and Figure 5 shows it as the clipper input-though the pulses are not far enough apart to show the full effect of the overshoot. (This condition of bit pick-up after isolated "ones" had been noted in XD-1 but their solution was simply to raise the clip level and accept the decreased

minimum signal margins).

Checking signals through the amplifiers showed that the overshoot phenomenon was not present on the tape but did exist at the input to the clipper in the Tape Adapter Frame (at the clipper, 10V P-P overshoot was present in 75V P-P signal). The amplifiers apparently did not have good enough low frequency response to pass the signal effectively. About half of the overshoot was introduced by the RC coupling between the preamp and its output cathode follower. The rest came from the Tape Adapter Frame amplifier coupling circuits. As a test the RC time constant of the coupling circuit in the preamp was increased but then the "DC" level shifts attendant to the unblocking of the amplifier at read-write transitions caused trouble.

During write time (and especially at the change from write to read status after write-forward-before-backspace) the transients produced at the read-write head by the write drivers blocked the preamplifier to such an extent that it took up to 30 milli-seconds to recover. The output voltage level was still changing long after the backspace read signals came through. When the coupling time constant was increased as noted above, this slowly changing voltage was coupled to the succeeding amplifier and caused errors. Various schemes were tried to either eliminate the blocking of the amplifier or to get it to unblock in a hurry. Simply changing the values of components already in the circuit did not help. Diode limiters of several types were tried at the input to try to keep the signal amplitude below that which would saturate the amplifiers-but diodes do not work well at the low signal levels (30mv) involved. Several types of gates were proposed but they introduced more transients than they eliminated. Finally Dick Best, of Group 63, suggested a transistor gate at the input of the amplifier. An RC network was added to ensure that the transistor stayed on during the collapse of the field around the write heads. (Since this transient occurred last it was the most troublesome one, though not the biggest.) Figure 3 shows the final design.

The results are shown in Figure 4 which indicates the voltages at the preamp input grid before and after these modifications. The write transients have been made the same order of magnitude as the read pulses. They could have been made smaller by increasing the 12K series resistor (see Figure 3), but this would make the gate circuit more dependent on transistor variations and drift of cut-off current. With this modification of the input, the amplifier no longer "blocks". The coupling capacitor at the output can now be increased 50% in value to 0.0022 μf since it need not attenuate the long term "unblocking" transient, and the overshoot is reduced to about half its former value.

SELECT TRANSISTION:

A problem exists in the tape adapter frame because the signal from the tape drive occurs in combination with the 10 volt "selection transient" visible about half way across Figure 1. This transient should not be coupled to the clipping stage, but the signal, of course, should be passed. The coupling time constants in the TAF were not

long enough to pass the signal portion of the waveform presented to them without re-introducing the overshoot phenomenon in the signal. The time constants could not be increased, however, without coupling the "selection transient " portion thru to an excessive degree. Now, however, because of the added transistor gate the selection transient is a smooth exponential (see top, Figure 1), instead of the exponential plus the "unblocking transient" (see middle, Figure 1). Therefore, the coupling capacitors can be increased to reduce signal overshoot without causing corresponding increase in size of the transient at the clipper input. The delay which determines when the character register can be set up may have to be lengthened somewhat since the transient, though of small amplitude, lasts longer.

RESULTS:

When work was started on this project a data plot was made to show the effects of various gain settings and clip level voltages with respect to errors. It should be understood that changing the gain of the preamplifiers, while it is a convenient handle, does not duplicate the conditions imposed by a low output tape on the one hand, or an excessively noisy tape on the other. This is because the gain control operates by changing the amount of feedback and therefore has radical effects on the bandwidth of the amplifier. However, the results of similar tests under similar conditions are of significance and, if interpreted with discretion, indicate the progress made. Figure 6 is a plot of the area of failure on a graph of amplitude against clip level both before and after the modification. The gain control was set so that the average signal amplitude peak-to-peak was that indicated on the ordinate. The recommended 20 or 21 volts (P-P) seems to be the best from the point of view of S/N ratio and saturation of amplifiers. The figure shows that now one clip level can be found for which any setting of the gain control will produce error-free operation. This was not possible before. More important it allows us to pick a clip level for best operation. This level is around 8.5 volts.

Knowing that the signal into the clipping stage is a nominal 37.5 volts and that there is about 3 volts bias from grid to cathode of the clipping stage, we can deduce that the changes made have allowed us to reduce the clipping to the point that signal of about 15% of normal amplitude will operate the character register instead of the 25-30% minimum formerly required. These figures indicate that a definite improvement in reliability is to be expected. Figure 8 shows the improvement, graphically.

To calculate an ideal clip setting we note, first, that IBM allows a 49% reduction of signal strength anywhere on good tape. Oxide build up on the head reduces signal amplitude by causing increased tape-to-head separation. The signal amplitude frequently drops as much as 50% for this reason and then abruptly returns to nearly full amplitude when the oxide build-up is knocked off the head thru abrasion. Therefore, intermittent variations from full amplitude to 25% amplitude (50% due to oxide build-up, 50% more due to allowable drop-out), can and do occur in normal operation. Secondly, erased tape can

produce noise up to 10% of normal signal. Thus, considering noise and amplitude changes, it would be mandatory to have the clip level below 25% of signal and above 11% of signal. Since we would like to set it as low as possible to allow for oxide buildup and/or wearout of heads, but still be above the noise, and since there is always some noise, 15-20 percent of the normal signal amplitude would seem a reasonable value for the clip level. Thus, if the system accepts 20% signals, instead of 30%, many common error producing situations are eliminated. IBM tape gave us about 2,500 error-free passes when tested on unmodified drives with our particular wearout program. With the modifications, but before suppressing all the write busses, we averaged about 4,500 error-free passes. With good maintenance we should be able to achieve 6,000 error-free passes consistently.

MECHANICAL TROUBLES:

During the course of our investigations, periodic errors occurred which were traceable to crinkles and waves in the edges of the tape. These were apparently caused by warped reels which dragged the edge of the tape and chafed it. It was discovered that very few reels were free from warp. Observations of operators using the machine led to the conclusion that most reels, if they do not warp normally with age, will become warped because of the necessity of forcing the reels onto some of the drives. This can always be done in such a way as to prevent warpage but many times an excessive amount of care must be exercised. It is thought that perhaps the reels or the hubs are not controlled closely enough in diameter. Also, replacements are not readily available.

SUMMARY:

To Summarize:

1. A transistor gate was added at preamp inputs.
2. The preamp output coupling capacitor was then increased to .0022.
3. The TAF coupling capacitors were changed from .0015 to .0022.
4. The clip level could then be reduced with consequent decrease in size of minimum readable signal.

T. C. Stockebrand

TCS:sc

Attachments:
B-67612 Fig. 1, 2, 4, 5, & 7.

## DISTRIBUTION LIST

Division 6

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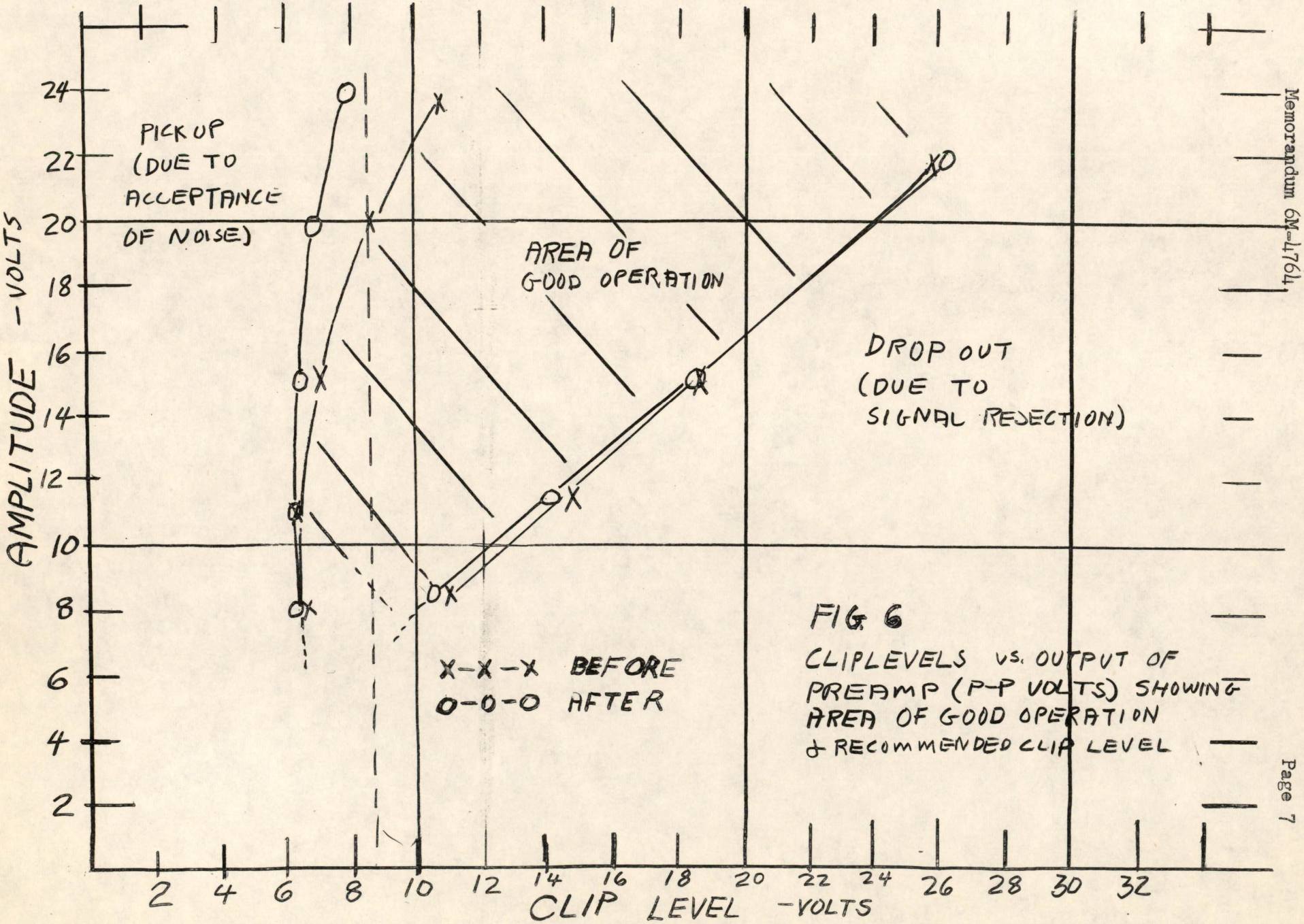
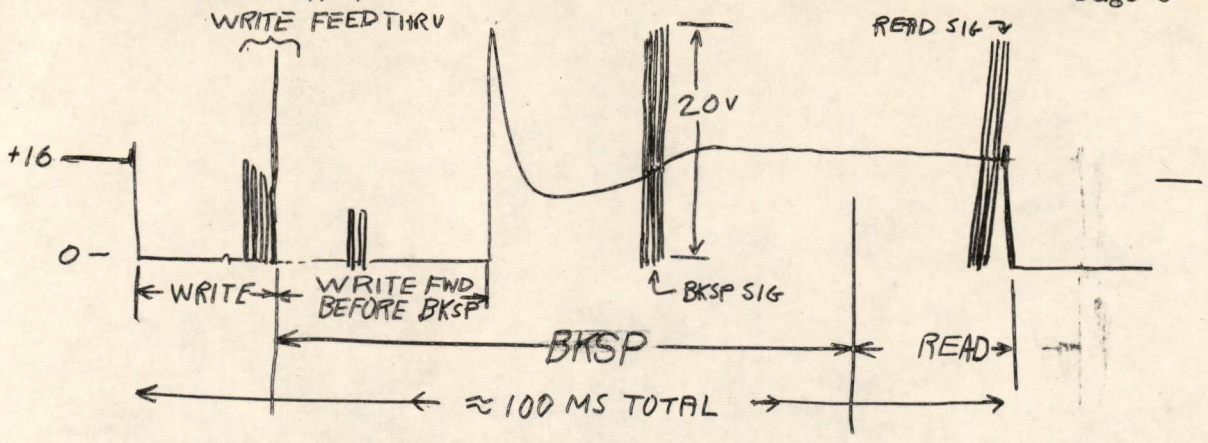



FIG 6

CLIPLEVELS VS. OUTPUT OF PREAMP (P-P VOLTS) SHOWING AREA OF GOOD OPERATION & RECOMMENDED CLIP LEVEL




1A = FIG 1 DIAGRAMATICALLY

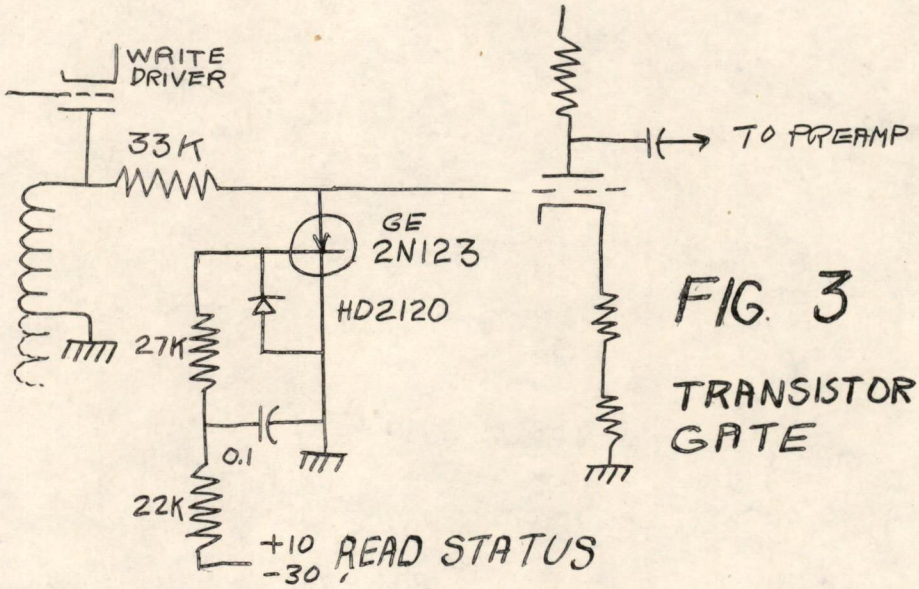


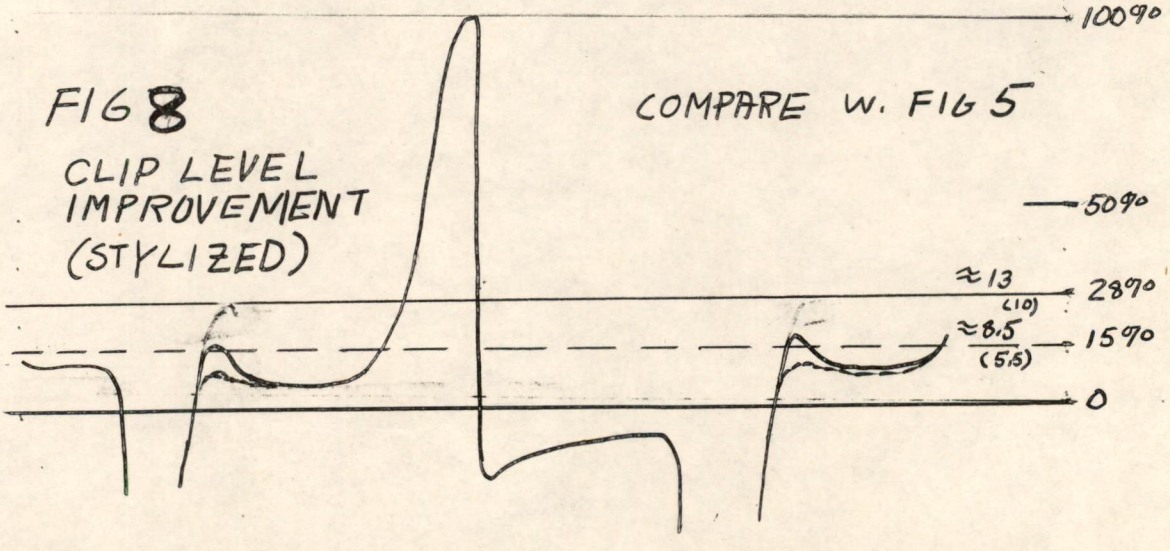

FIG. 3

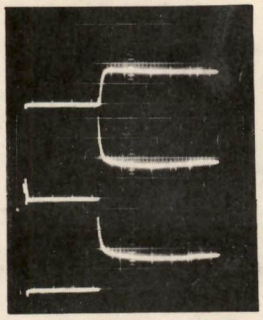
TRANSISTOR GATE

FIG 8

CLIP LEVEL IMPROVEMENT (STYLIZED)

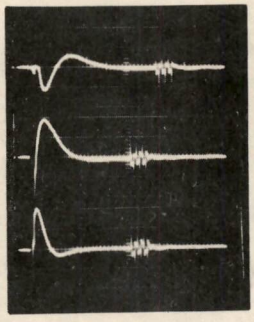
COMPARE W. FIG 5





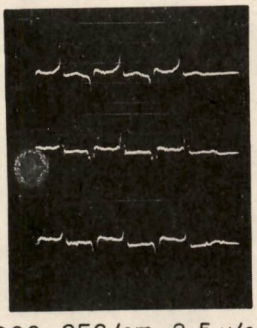

10 v/cm 10 ms/cm
GROUND ON BOTTOM LINE

FIG. 1
PREAMP OUTPUT




100 v/cm 1 ms/cm
SHOWING WRITE-READ TRANSIENT
AND BACKSPACE SIGNAL

FIG. 5
CLIPPER INPUT



200μSEC/cm 2.5 v/cm
(SIGNAL 20V P-P)

FIG. 2
PREAMP OUTPUT
DURING BACKSPACE

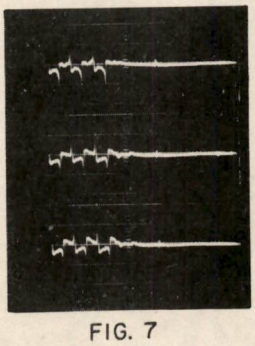
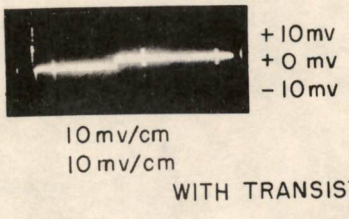
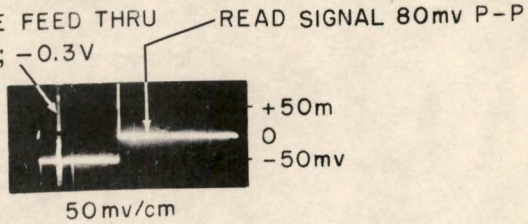



FIG. 7
CLIPPER INPUT
BACKSPACE SIGNAL




10 mv/cm
10 mv/cm
WITH TRANSISTOR




50 mv/cm
10 mv/cm
WITHOUT TRANSISTOR

FIG. 4
INPUT GRID

B-67612

K. H. Olsen
B-062

Memorandum 6M-4774

Sheet 1 of 22 sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: MAGNETIC AMPLIFIERS (Magnetic Materials and Saturable Reactors)

To: Distribution List

From: S. T. Coffin

Date: 12 December 1956

Approved: J. J. Gano

J. J. Gano

Abstract: Magnetic amplifiers make use of the non-linear characteristics of magnetic cores to obtain power amplification, and offer high reliability and large power-handling capability, making them adaptable to certain computer system applications such as switching circuits and power control. The analysis of magnetic amplifier circuits involves a study of the properties of magnetic core materials, the use of certain simplifying assumptions, and application of basic electrical principles to a step-by-step solution of the various voltage and current waveforms involved. Investigation of some simple saturable reactor circuits yields basic formulas and relations useful in more complex circuits. The ordinary parallel-connected and series-connected saturable reactor circuits, which are described in detail, offer moderate power gain and linear transfer characteristics. Descriptions of other circuits and specific applications will be issued as supplements.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## 1.0 Introduction

Magnetic amplifiers are devices which make use of the non-linear characteristics of certain magnetic core materials to obtain amplification of power, and in their simplest form they consist merely of turns of wire wound on suitable magnetic cores. There are many applications where magnetic amplifiers are preferrable to other types of amplifiers because of their advantages of simplicity, high reliability, low cost, and large power handling capability. In addition, a particular magnetic amplifier design may be used over a wide range of voltage, current, and power rating by scaling core size, wire size, and number of turns up or down. They are especially desirable in systems where high reliability is demanded; and in particular, they are useful in digital computer systems for certain switching circuit and power control applications. Magnetic amplifiers have been used in regulated power supplies, line voltage regulators, alternator and d-c generator field control, motor speed control, light-dimming and indicator lamp operation, logical switching circuits, instrumentation and metering; and a great variety of uses appear possible.

Although the field of magnetic amplifiers has undergone rapid development in recent years with the improvement of core materials and semiconductor rectifiers, factors retarding their application have been the cumbersomeness of their circuit analysis and the small number of people familiar with them. The difficulty in analysis arises from the non-linear nature of the magnetic core. Rectifiers are often used, and add to the non-linearity. Since magnetic amplifiers depend upon a periodically varying power source for their operation, it is common practice to make certain simplifying assumptions which enable the operation of the circuit over one cycle to be broken up into a series of linear intervals which can be attacked analytically, and then pieced together to describe one cycle of operation. Often, the characteristics of the circuit being studied are obvious after the waveforms of the various voltages and currents have been determined, hence the emphasis in this series of papers is on graphical representation of quantities rather than on involved mathematics.

The characteristics of various magnetic core materials are first considered briefly. Then, a few simple circuits are analyzed to illustrate various basic ideas. The parallel-connected and series-connected saturable reactor circuits are considered in some detail. The next paper will cover external feedback in saturable reactor circuits. This will lead to the self-saturating magnetic amplifier. One installment will cover the half-wave flux reset circuit and its use as a switching circuit, while another will be devoted to polyphase magnetic amplifiers and their application in regulated d-c power supplies.

## 2.0 Saturable Cores

### 2.1 Core Materials

All magnetic amplifiers make use of saturable magnetic cores in some way or other. The properties of magnetic cores are often represented by a graph of the hysteresis loop of their core material. Figure 1 shows the 60 cycle hysteresis loops of a few common magnetic amplifier core materials. A typical value of lamination thickness has been selected for each material, and some of the different trade names under which these materials are sold are listed. One type of ferrite core has been included for the sake of comparison.

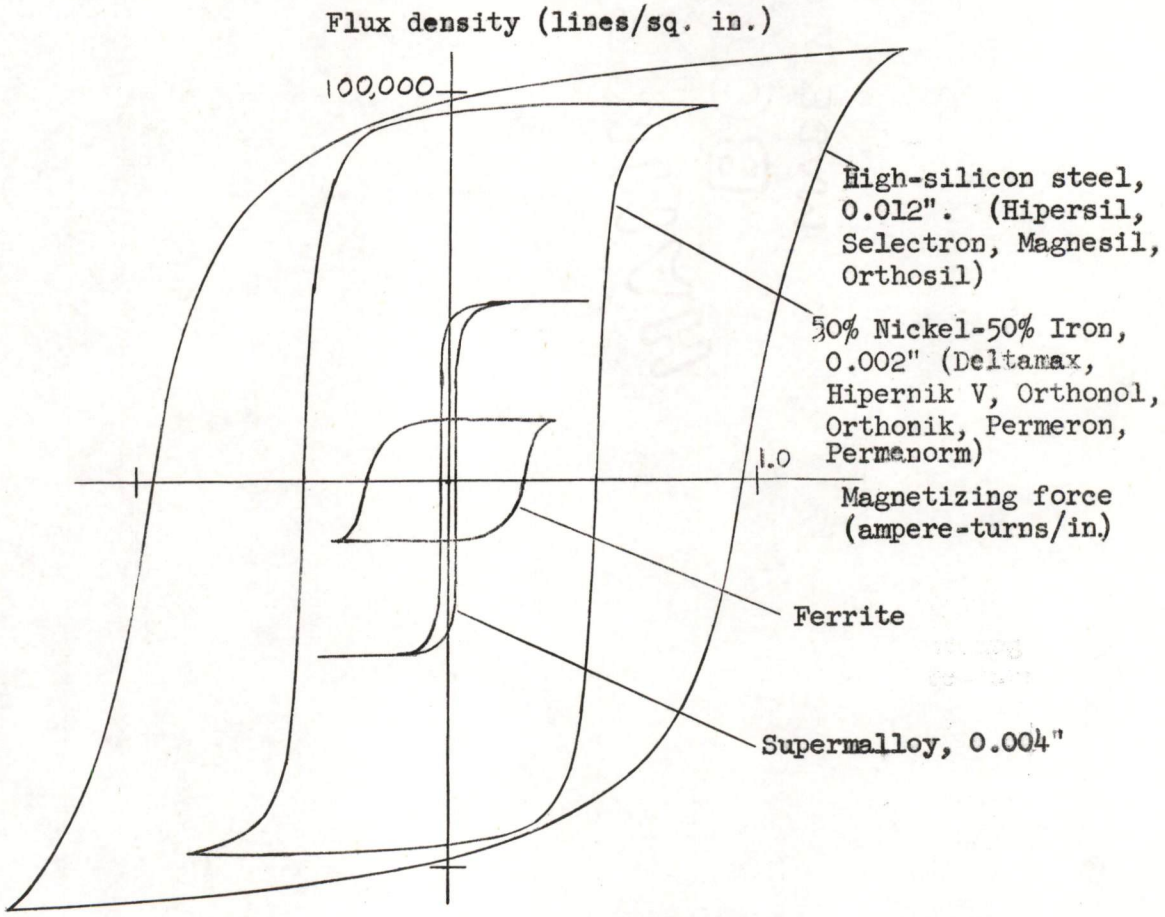



Figure 1, Core Materials

In the above figure, flux density is plotted in lines per square inch and magnetizing force in ampere-turns per inch to simplify subsequent calculations. Since flux density is often given in guasses, and magnetizing force in oersteds, the following conversion formulas are useful:

1 gauss = 6.45 lines/sq. in.

1 oersted = 2.02 ampere-turns/in.

The high-silicon steel material contains 4 percent silicon, and is cold-rolled to produce a high degree of grain orientation resulting in one easy direction of magnetization parallel to the direction of rolling. It is commonly used for handling large amounts of power. It is inexpensive and rugged, but has a wide hysteresis loop.

The 50 percent nickel-50 percent iron material is widely used in small, high performance magnetic amplifiers. It is medium priced and has excellent magnetic properties, but is temperature and strain sensitive. It is cold-rolled to produce grain orientation, resulting in two directions of easy magnetization. A similar material, sold as Nicaloi, Hipernik, Conpernik, and 48 Alloy, is not grain-oriented, and is sometimes used in the form of punched, stacked laminations.

65-Permalloy, not shown in Fig. 1, is a nickel-iron alloy containing 65 percent nickel. It is not grain oriented and has a hysteresis loop somewhat shorter and narrower than 50 percent nickel-50 percent iron.

Supermalloy and Molypermalloy are alloys of nickel, iron, and molybdenum. They have extremely narrow hysteresis loops, but are quite expensive and have low saturation flux density. They are used mostly in low power, high frequency applications.

Ferrites are used only at very high frequencies, often in pulse-operated circuits. Their characteristics vary with chemical composition and treatment, but their saturation flux density is always low.

Other less commonly used materials are Mumetal, Sinimax, Monimax, Permendur, and Supermendur.

The hysteresis loop of a particular core material varies so greatly under different conditions that the loops shown in Fig. 1 are of little use to the designer and are shown merely to compare the different materials. Some of the factors which affect the shape of the hysteresis loop are the frequency, magnitude, and waveshape of the applied voltage and the lamination thickness of the material. Most of these affect the width of the hysteresis loop but do not affect the saturation flux density. Catalogs are available which contain much useful information concerning different core materials.*

---

* Core Catalogs:

Magnetics, Inc., catalog TWC-100.
Westinghouse Electric Co., bulletins 44-550 and 44-750.
Arnold Engineering Co., bulletin TC-101A.

## 2.2 Core Geometry

Cores made of these saturable materials are available in a variety of different shapes and sizes. Given the dimensions of a core of a certain material, its characteristics are found by calculating the effective cross-sectional area and mean length of the magnetic path. The effective cross-sectional area is found by multiplying the actual core cross-sectional area by the stacking factor. This factor takes into account the insulation and air gap between laminations. Typical values are:

| Lamination Thickness | Stacking Factor |
|---|---|
| 0.012" | .95 |
| 0.004 | .90 |
| 0.002 | .85 |
| 0.001 | .80 |

The mean length of magnetic path in a toroidal core may be found by taking the average of inside and outside core circumference.

effective area = actual area x stacking factor

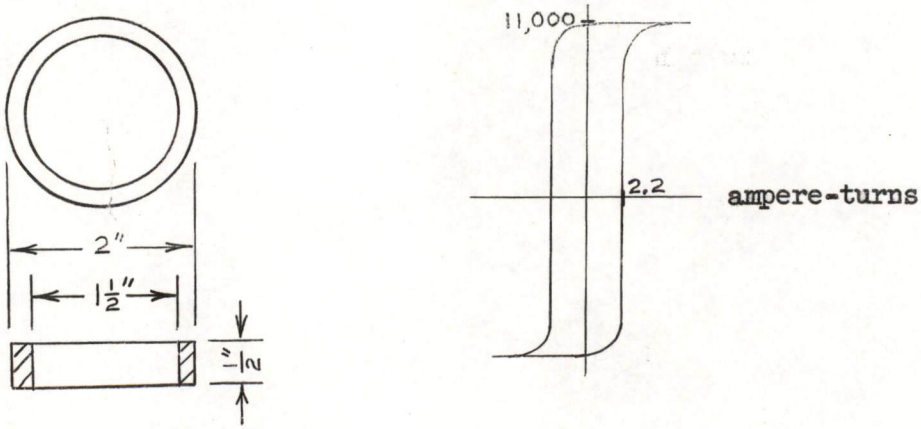
mean circumference = $\frac{1}{2}$(inside circumference + outside circumference)

These calculations allow the hysteresis loop to be plotted in terms of lines of flux and ampere-turns, using the following relations:

lines of flux = flux density x effective area

ampere-turns = mean circumference x ampere-turns per inch

For example, the core shown in Figure 2 would have the characteristics shown on the right.




Material: Deltamax, 0.002"

Fig. 2, Core Characteristic

Calculations for Fig. 2:

effective area = $\frac{1}{2}$" x $\frac{1}{4}$" x .85 = 0.11 sq. in.

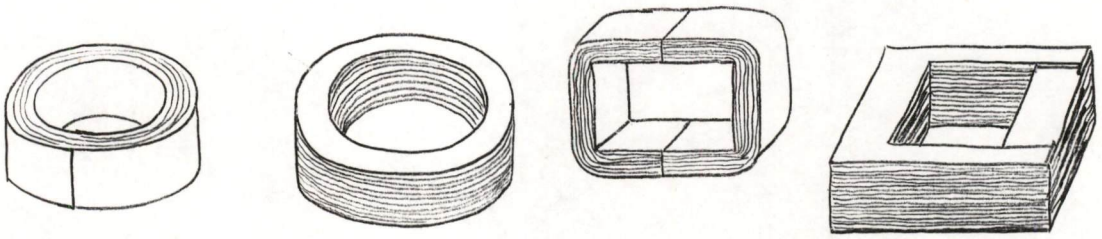
mean circumference = $\frac{1}{2}(\pi \times 1\frac{1}{2}" + \pi \times 2") = 5.5"$

and, using hysteresis loop in Fig. 1,

saturation flux $\phi_s$ = 100,000 lines/sq.in. x 0.11 sq.in. = 11,000 lines

magnetizing MMF = 0.4 ampere-turns/in. x 5.5" = 2.2 ampere-turns

Although saturable cores are usually made of a continuous strip of material rolled into the toroidal form shown in Fig. 2, other configurations shown in Fig. 3 are suitable for certain applications.



Wound Toroid Stamped Ring C Type D-U Type

Fig. 3, Core Types

The wound toroidal core combines the advantages of uniform cross-section, no appreciable air gap, and proper orientation of the grain of the metal along the direction of easiest magnetization. Some of the other types have the advantage of lower cost and easier winding and mounting.

It is important that the ratio of inside to outside diameter be as near <u>one</u> as possible. Otherwise, the inside layers, having a shorter circumference, will saturate first, causing a rounding-off of the knee of the hysteresis loop. This ratio is called the core ratio. The core of Fig. 2 has a core ratio of 0.75.

$$\text{core ratio} = \frac{\text{I.D}}{\text{O.D}}$$

It will become apparent that the most desirable core is one that has a tall, narrow, rectangular hysteresis loop--in other words, large saturation flux, small magnetizing force, high permeability in the unsaturated region and low permeability in the saturated region, and a sharp transition between the two regions.

## 3.0 The Half Wave Saturable Reactor

### 3.1 Basic Single Core Saturable Reactor

A simple saturable reactor circuit consisting of a saturable core wound with a number of turns of wire and connected in series with an a-c voltage source and resistive load is shown in Fig. 4.

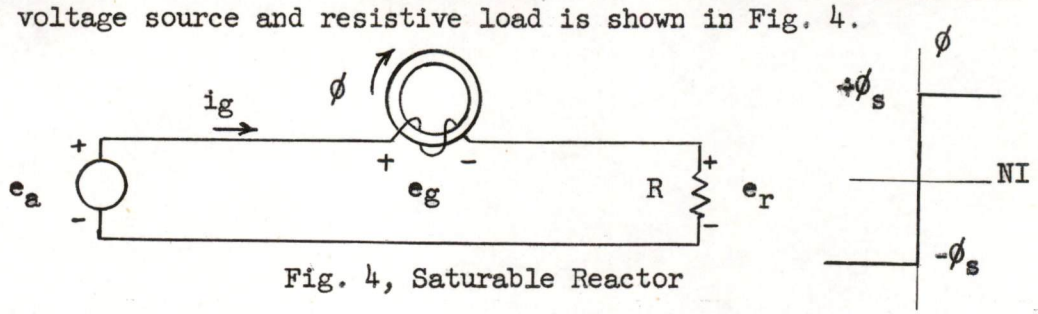



Fig. 4, Saturable Reactor

It is convenient when analysing certain saturable reactor circuits to consider that the windings have zero resistance and that the saturable core has the idealized hysteresis loop consisting of three straight lines as shown. In the saturated regions, represented by the two horizontal lines, the reactor has zero inductance. In these regions the flux is constant, so no voltage may be induced in the winding. In the unsaturated region, represented by the vertical line, the reactor has infinite inductance and no current flows when voltage is applied across the winding, or if there is more than one winding on the core, the net ampere-turns of all the windings must be zero. Thus the saturable reactor (abbreviated SR) behaves as a short circuit when saturated and an open circuit when unsaturated. The winding of the core is appropriately called a gate winding.

If the applied voltage is small enough in the circuit of Fig. 4 so that the core remains unsaturated at all times, then no current will flow in the circuit and the voltage induced in the SR will be equal and opposite to the applied voltage. The maximum voltage that the core may absorb without saturating may be found from the familiar Faraday's Law:

$$e_a = -10^{-8} N_g \frac{d\phi}{dt} \qquad (1)$$

where $e_a$ is instantaneous applied voltage,

$N_g$ is number of turns on gate winding,

$\phi$ is lines of flux.

Rewriting Faraday's Law in its integral form:

$$\int e_a = -10^{-8} N_g \phi \qquad (2)$$

If the applied voltage is a periodic a-c voltage, then from the preceding equation the following expression may be derived:

$$E_a = 2 \times 10^{-8} N_g \phi f \qquad (3)$$

where E is the average rectified value of applied voltage,

$\phi$ is the peak-to-peak flux,

f is the frequency of the applied voltage.

This simple equation is often useful in magnetic amplifier design. Thus, the core of Fig. 2 wound with 4000 turns will absorb 106 volts at 60 cycles before saturating.

$$Ea = 2 \times 10^{-8} \times 4000 \times 22{,}000 \times 60 = 106$$

Note: for reasons that will become apparent, it will be convenient to deal with average rectified values of voltage and current rather than rms values. Throughout this paper, capital letter (E, I) refer to average rectified values unless otherwise noted, and small letters (e,i) refer to instantaneous values.

If the applied voltage is increased beyond the saturation voltage $\phi_s$, part of the applied voltage will appear across the resistive load, and the resulting waveforms are shown in Fig. 5.

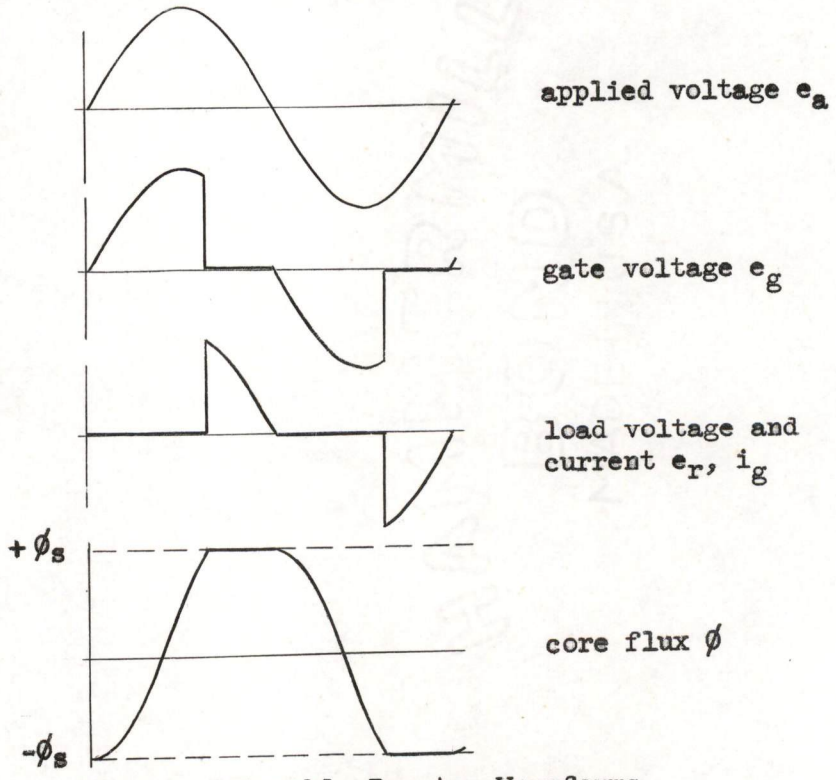



Fig. 5, Saturable Reactor Waveforms

In order to calculate the voltage across the load, one may write:

load voltage = applied voltage - voltage absorbed by SR

or $$E_r = E_a - 2 \times 10^{-8} N_g (2\phi_s) f \qquad (4)$$

The reason for dealing with average values of voltage is now obvious. Faraday's Law states that the SR absorbs a constant volt-time area, or a constant average voltage, from the applied voltage waveform as its flux changes from one saturated region to the other. Fig. 6 shows the effect of varying the applied voltage. The SR absorbs a constant volt-time area (shaded) while the remainder of the applied voltage waveforms (not shaded) appears across the load.

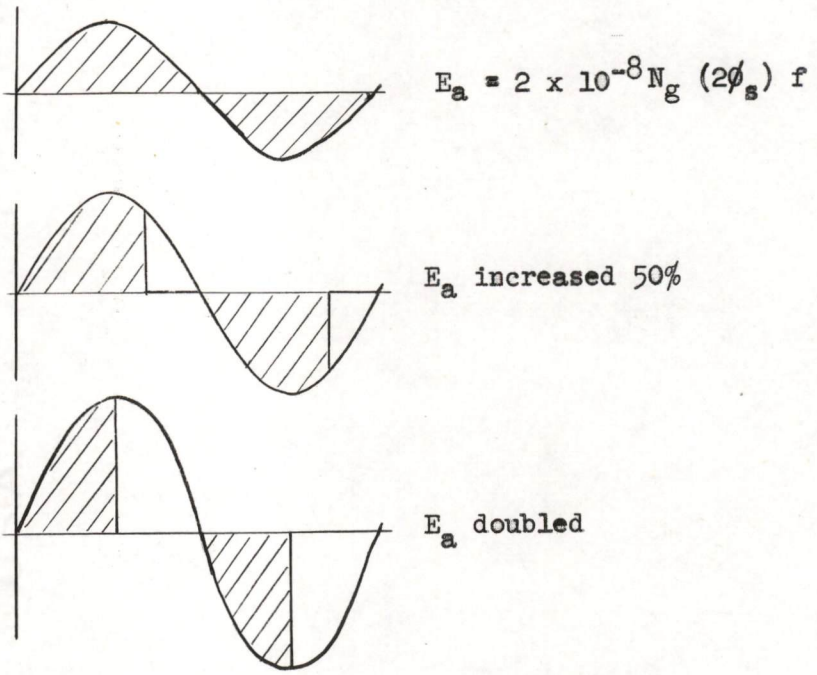



Fig. 6, Effect of Varying Applied Voltage

The relation between applied voltage and load voltage is shown in Fig. 7. Many devices, including constant-voltage transformers and magnetic voltage references, depend upon this non-linear relationship for their operation.

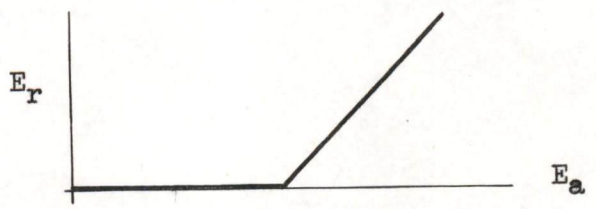



Fig. 7, Output Characteristic

### 3.2 Single Core With Control Winding

In the preceding circuit, the input voltage was varied. In most magnetic amplifier circuits, however, the input voltage is constant and the load voltage is controlled by a second winding on the saturable core. The saturable reactor circuit with this control winding added is shown in Fig. 8.

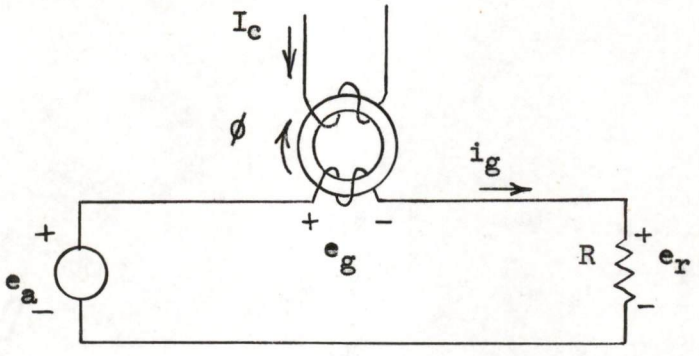



Fig. 8, Saturable Reactor With Control Winding

The applied a-c voltage is again made just equal to the saturating voltage of the SR, so that with no control current flowing, no voltage appears across the load. If a d-c control current is now made to flow in the direction indicated, the SR is driven into its positive saturation region during a portion of each cycle, and the resulting waveforms are shown in Fig. 9.

As in all magnetic amplifier circuits, the cycle can be considered as broken into different modes of operation, depending on whether or not the SR is saturated. When the SR is unsaturated, the net ampere-turns must be zero, and the following relation applies:

$$N_g\, i_g + N_c\, I_c = 0 \qquad (5)$$

This means that during these periods, since the control current is assumed constant, the gate current must also be constant, of opposite polarity, and related to the control current by the turns ratio $N_c/N_g$.

When operating in the saturated mode, the gate voltage is zero, and the equation for the loop voltage reduces to:

$$e_a = i_g\, R \qquad (6)$$

One other basic rule illustrated by this circuit is that the gate voltage, when averaged over a complete cycle of steady-state operation, must be zero. Furthermore, since there are no batteries or diodes in the load circuit of Fig. 8, the current in this circuit and the load voltage can have no d-c component either.

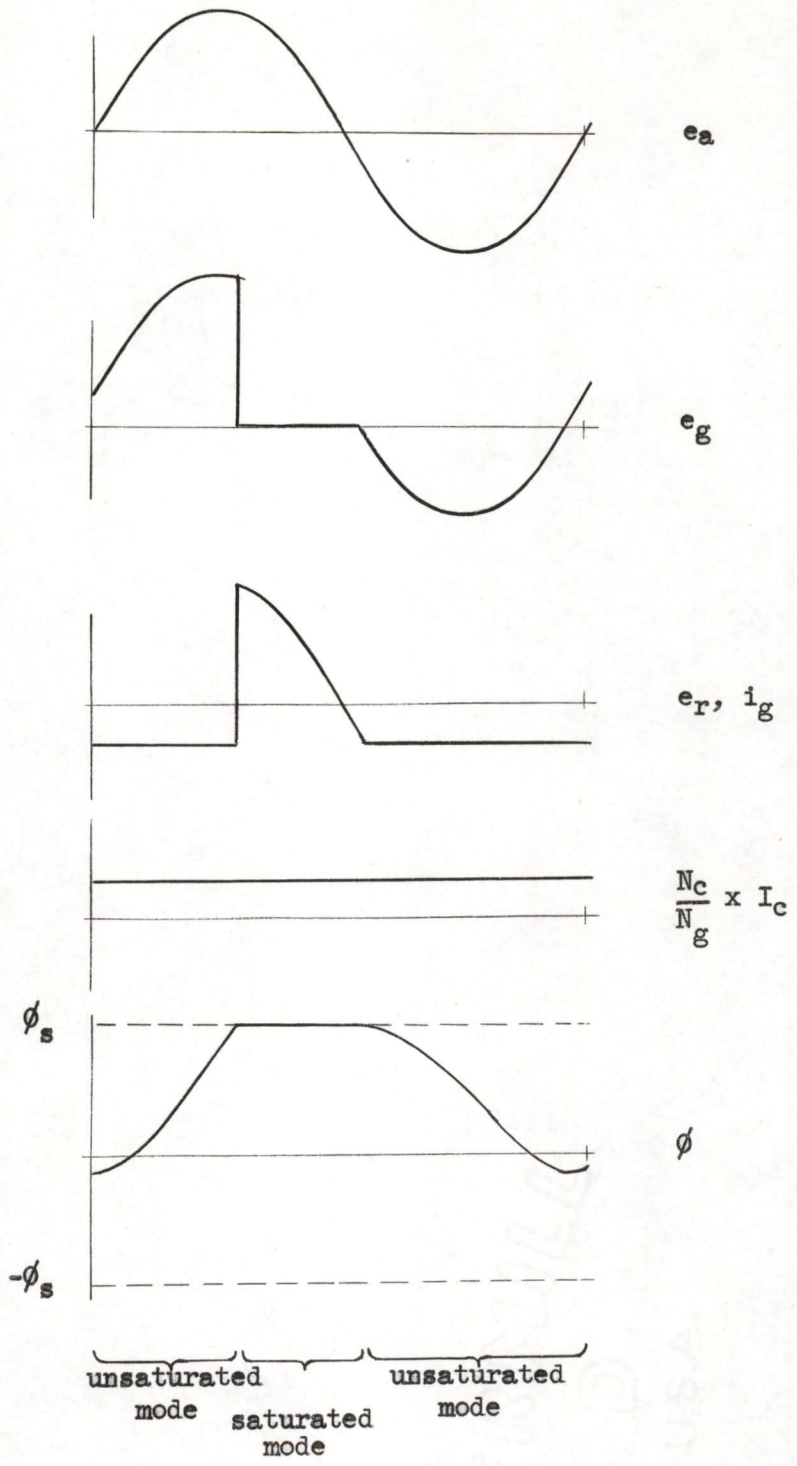


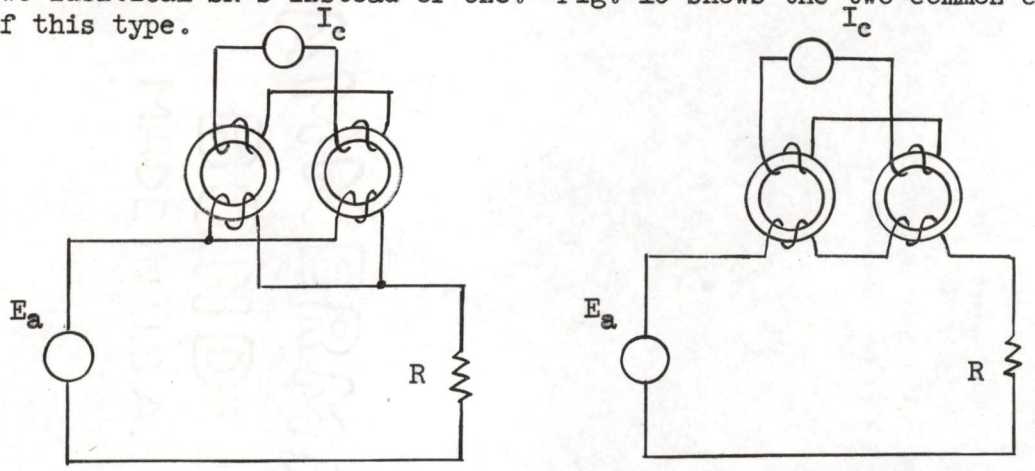

Fig. 9, Waveforms of Saturable Reactor with Control Winding

The circuit of Fig. 8 has one disadvantage which makes it impractical. It was assumed that a steady d-c current was flowing in the control winding. But the changing flux will induce a voltage in the control winding which, unless the control current source has infinite impedance, will cause an a-c component of current to flow in the control circuit. If the control circuit has zero impedance, then the SR behaves as a transformer with a shorted secondary and presents no impedance in the circuit at any time. If resistance is inserted in the control circuit, then the power dissipated in it is such that the circuit can have no power gain. A large choke could be used to solve this problem, but a better solution will be presented. Hence, this circuit is not used.

## 4.0 Full-Wave Saturable Reactors

### 4.1 Basic Full Wave Circuits

The disadvantage of the preceding circuit is overcome by using two identical SR's instead of one. Fig. 10 shows the two common circuits of this type.




Parallel-Connected SR  Series-Connected SR

Fig. 10, Full Wave Circuits

### 4.2 Parallel-Connected SR

Considering the parallel-connected circuit first, assume that the applied a-c voltage is again selected such that it equals the saturating voltage of either SR. The circuit is redrawn in Fig. 11 with voltage polarities and current and flux directions indicated.

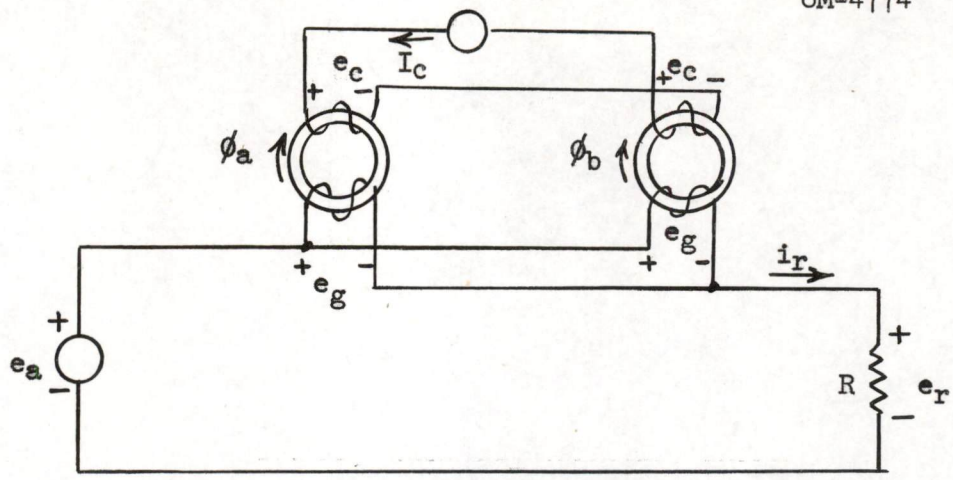



Fig. 11, Parallel-Connected Circuit

Since the two gate windings are connected in parallel, their instantaneous voltages $e_g$ are always equal. Furthermore, since the instantaneous gate voltage $e_g$ and control voltage $e_c$ of each SR are related to the rate-of-change of flux by the equations:

$$e_g = -10^{-8} N_g \frac{d\phi}{dt}$$

and

$$e_c = -10^{-8} N_c \frac{d\phi}{dt}$$

it follows that

$$e_c = \frac{N_c}{N_g} e_g \qquad (7)$$

This useful relation applies to nearly all magnetic amplifier circuits.

It follows that the instantaneous voltages of the two control windings are always equal. They are connected with their voltages opposing, so that the net voltage across the control current source is always zero. This, then, is the advantage of the full wave circuit—no net voltage is induced in the control circuit, so that regardless of how low the impedance of the control current source, no objectionable short-circuiting current flows.

Because of the similarity in connections of the gate and control windings, a simplification of the circuit is possible. Instead of having the d-c control current flow in a separate winding, the circuit has been redrawn in Fig. 12 with the d-c control current flowing in the loop of the gate winding circuit. Although this is not usually convenient in practice, it simplifies the analysis, and is perfectly valid. The imaginary d-c loop current is made equal to the original control current multiplied by the turns ratio $N_c/N_g$.

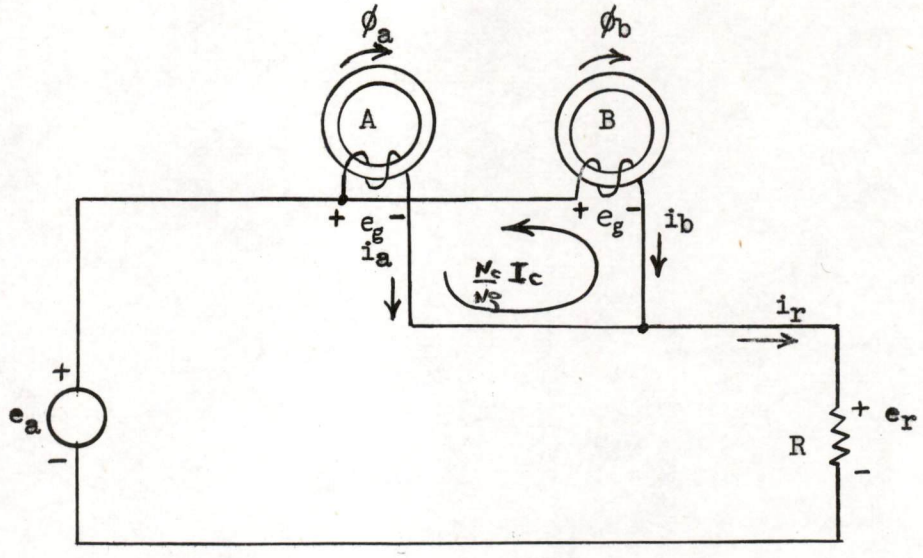



Fig. 12, Simplified Circuit

Now assume a d-c control current flowing in the direction indicated. This causes core A to saturate in the direction of positive flux at some point in the positive half-cycle of applied voltage, and core B saturates one-half cycle later in the direction of negative flux. The resulting waveforms are shown in Fig. 13. Since the operation of each SR is confined to one of its saturated regions, the gate current of each SR is unidirectional. The average value of this current must be the imaginary d-c control current which was assumed to be flowing in the gate circuit. It can be seen that the load current is the sum of the two gate currents:

$$I_r = I_a + I_b$$

but

$$I_a = I_b = \frac{N_c}{N_g} I_c$$

therefore

$$I_r = \frac{2N_c}{N_g} I_c \qquad (8)$$

This is the equation for the steady-state transfer characteristic of the parallel-connected SR. This direct proportion between control current and output current is the most important feature of the circuit, making it useful in current-measuring instruments and current-limiting devices as well as for conventional amplification of power.

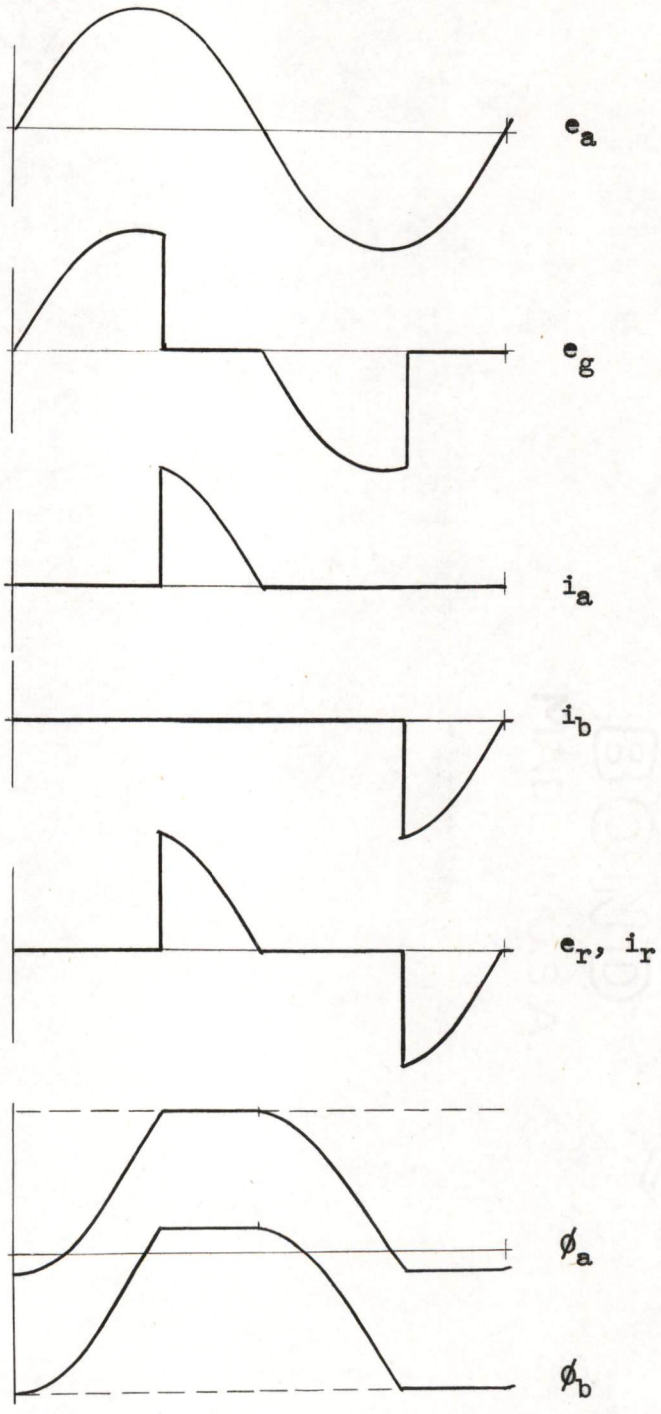



Fig. 13, Waveforms of Parallel- Connected SR

Fig. 14 shows the theoretical and actual transfer characteristic of the circuit. The behaviour of the circuit is similar for either polarity of control current. A point is reached at the end of the proportional region where the SR's are completely saturated, the entire applied voltage is impressed across the load, and the load current cannot increase further. The load current at this point is determined by the value of load resistance, and therefore the flat regions are called the resistance-limited regions.

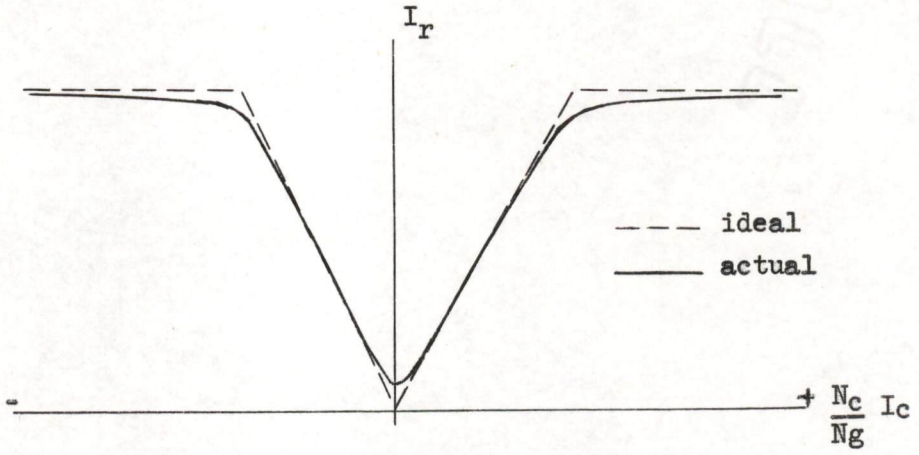



Fig. 14, Characteristic of Parallel-Connected SR

In an actual circuit, the load current does not decrease to zero because a small magnetizing current flows even when the cores are unsaturated. The entire applied voltage never appears across the load because the cores always have a slight inductance when saturated. In a well balanced design, the load resistance should be small compared to the unsaturated impedance of the reactors and large compared to the saturated impedance.

## 4.3 Series-Connected SR

The operation of the series-connected SR is similar in many respects to the parallel-connected SR. One difference is that, since the gate windings are connected in series, the entire load current must flow through each of them but only half of the applied voltage must be absorbed by each SR. Therefore, for a circuit the equivalent of the parallel-connected SR, the series-connected SR would use half as many turns of larger wire in the gate winding.

Another difference is that the impedance in the control circuit of the series-connected SR has a considerable effect on the operation of the circuit. In this analysis, it is assumed that the control circuit has zero source impedance. The circuit is shown in Fig. 15 with voltage polarities and current and flux directions indicated.

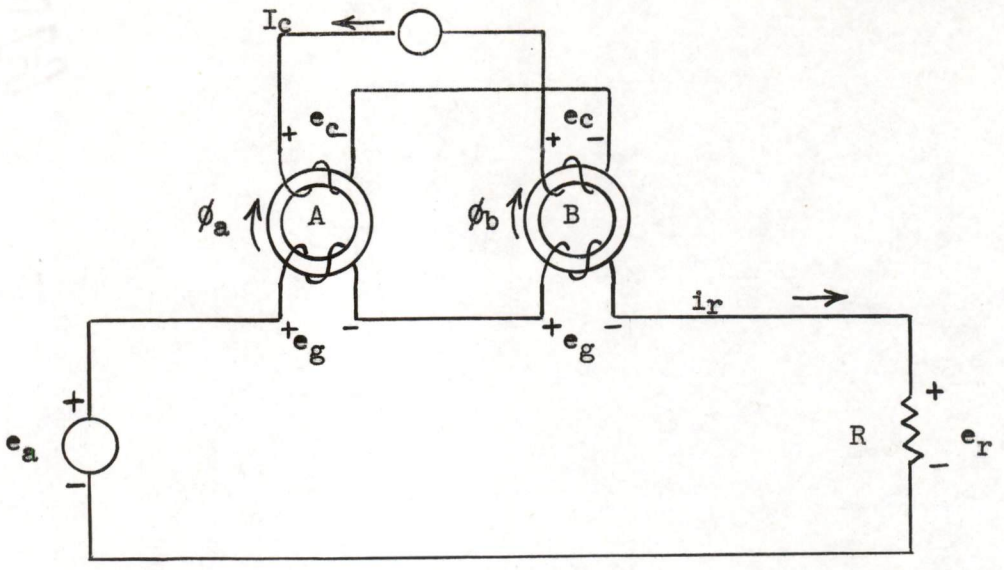



Fig. 15, Series-Connected Circuit

Since the two control windings are connected in a closed loop in which it has been assumed there are no external voltages (zero control current source impedance), the instantaneous voltage $e_c$ of the two control windings must be equal at all times. It follows that the instantaneous voltages of the two gate windings must also be equal at all times, because:

$$e_c = \frac{N_c}{N_g} e_g$$

Now assume a d-c control current flowing in the direction indicated, causing core A to saturate in the direction of positive flux at some point in the positive half-cycle of applied voltage, similar to the parallel-connected SR. When core A saturates, the voltage across both its gate and control windings must decrease to zero. When this happens, the control circuit acts as a short circuit to core B, so its gate and control winding voltages must decrease to zero also. With no voltage across either gate winding, the applied voltage is impressed across the load for the remainder of the positive half-cycle of applied voltage. During this period, since core B is unsaturated, the net ampere-turns on it must be zero. Therefore, during this period the instantaneous control current is:

$$i_c = \frac{N_g}{N_c} i_r$$

During the periods that neither core is saturated, no current can flow in either control or gate circuit, since any current or combination of currents would violate the rule of zero net ampere-turns.

During a portion of the next half-cycle, a similar action takes place with core B saturating, and the control circuit again passes a current proportional to the load current. The resulting waveforms are shown in Fig. 16.

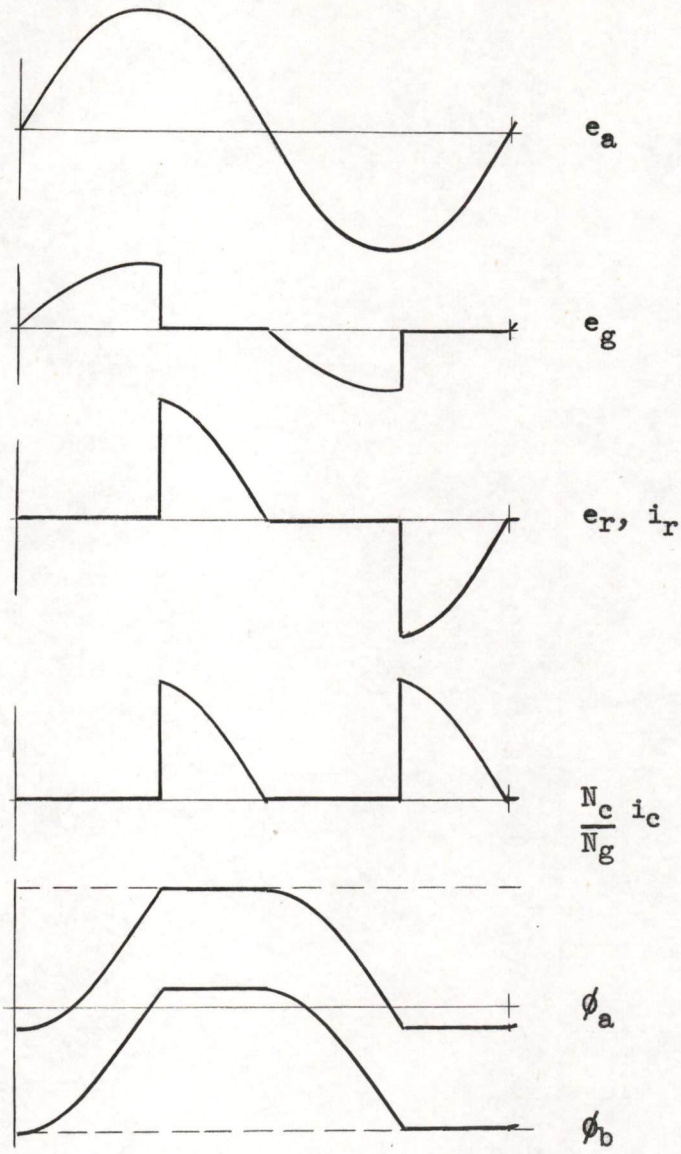



Fig. 16, Waveforms of Series-Connected SR

From inspection, it can be seen that:

$$I_r = \frac{N_c}{N_g} I_c \qquad (9)$$

This expression is the same as that for the parallel-connected SR except for the factor of 2 missing. It can be seen that the characteristics and waveforms of the two circuits are alike in many respects.

## 4.4 Power Gain

Both full-wave circuits described would have infinite power gain with the assumption made of zero winding resistance. Taking the control winding resistance into consideration but neglecting the gate winding resistance the power gain may be defined roughly as the change in output power divided by the change in control circuit dissipation over the range from zero to maximum output. At zero output, the control circuit current and power dissipation are also zero. At maximum output, the load dissipation is:

$$(1.1\ I_r)^2\ R$$

where the factor 1.1 is necessary to convert from average to rms values assuming sinusoidal applied voltage.

The control circuit dissipation is:

$$(1.1\ I_c)^2\ R_c$$

where $R_c$ is the total control circuit resistance. The power gain is therefore:

$$\frac{(1.1\ I_r)^2\ R}{(1.1\ I_c)^2\ R_c}$$

For the parallel-connected SR, using equation (8), this simplifies to:

$$\text{Power gain} = \frac{1}{4}\left(\frac{N_c}{N_g}\right)^2 \frac{R}{R_c} \qquad (10)$$

and for the series-connected SR:

$$\text{Power gain} = \left(\frac{N_c}{N_g}\right)^2 \frac{R}{R_c} \qquad (11)$$

Power gains of around 100 to 1000 are common.

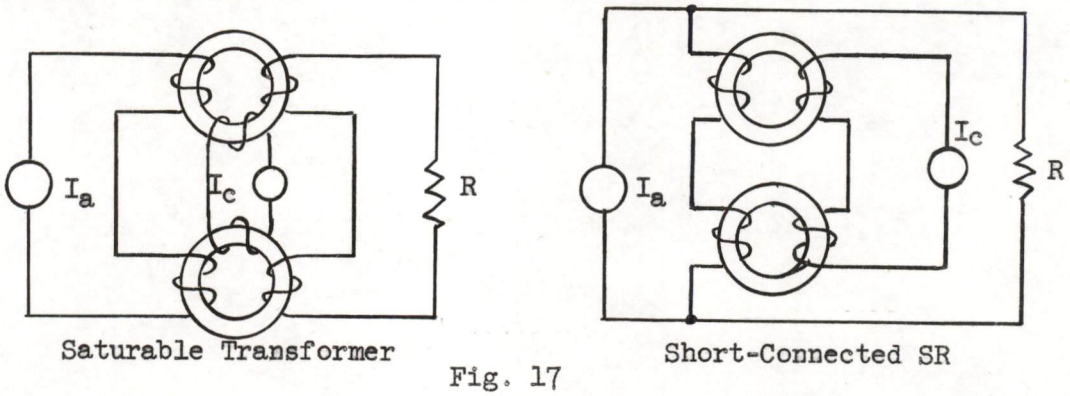
This treatment of full-wave SR's has been simplified in the extreme. Many assumptions have been made which are not always reasonable. Persons desiring a more rigorous and detailed analysis of these circuits are referred to Magnetic Amplifiers, by H. F. Storm.*

---

* H. F. Storm, Magnetic Amplifiers, Wiley, 1955.

## 5.0 Saturable Transformers and Shunt-Connected Saturable Reactors

Up to this point, a zero impedance source of applied voltage has been assumed. If the power source has high impedance (i.e. a current source) then the previously described SR circuits fail to function, and a saturable transformer or shunt-connected SR is used. Fig. 17 shows a common circuit for these two devices.




Saturable Transformer  Short-Connected SR

Fig. 17

The saturable transformer has the advantage that the load is isolated from the power source, and the load may be matched to the power source by selecting the proper turns ratio for the transformer. The shunt-connected SR, on the other hand, has higher efficiency, especially in applications where the output power is on most of the time. An early memorandum by D. A. Buck contains an informative discussion of these circuits.*

## 6.0 Power Rating of SR's

An interesting problem is the selection of the proper core to handle a given amount of power. For the most efficient design, the core window should be as full of windings as possible, and the windings should be operated near the rated temperature of the insulation. If too small a core is selected, difficulty will be encountered in winding or the temperature rise may be excessive, and if too large a core is used, an inefficient and uneconomical design is the result. A conservative rule of thumb is that 60 percent of the window area of a toroidal core can be wound conveniently, and that a current density of 1000 ampere-turns per square inch is possible in the windings. If half the useable winding space is used for control windings and the other half for gate windings, then the rms current rating of the gate winding is:

$$I_{rms} = 300 \frac{W}{N_g}$$

where W is the core window area in sq. in.

---

* D. A. Buck, Magnetic and Dielectric Amplifiers, E-477, July 28, 1952.

The volt-ampere rating of a single SR may be defined as the product of the saturating voltage and rms current rating of the gate winding. Therefore, using the preceding equation and equation (3), the volt-ampere rating is:

$$VA = 2 \times 10^{-8} N_g (2\phi_s) f \times 300 \frac{W}{N_g}$$

or

$$VA = 1.2 \times 10^{-5} \phi_s f W$$

The actual output power of a SR circuit depends upon the particular circuit used and the waveforms of the various voltages and currents. Of course, the figures used in the above equations are very rough. Other considerations often result in the selection of a core which is operated well below its power capacity.

## 7.0 Construction

Two common methods of assembling full wave SR's are shown in Fig 17.

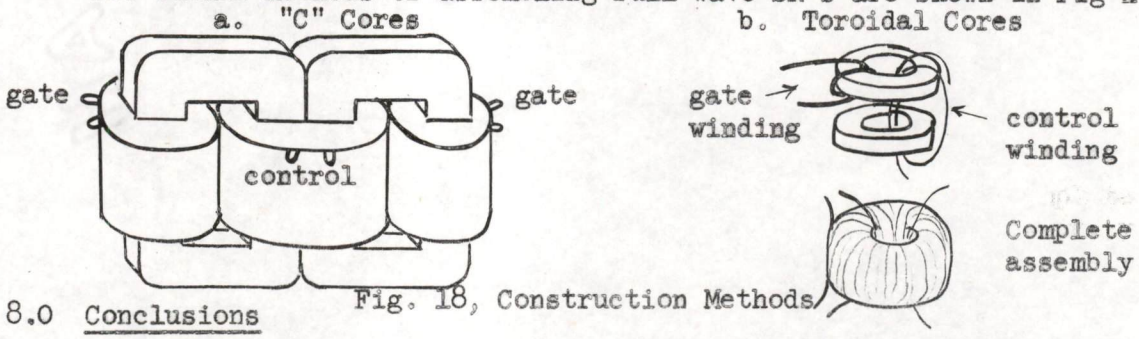



Fig. 18, Construction Methods

## 8.0 Conclusions

Saturable reactors provide linear transfer characteristics and moderate power gain. The average rectified output current is proportional to the control current and is relatively unaffected by changes of supply voltage, supply frequency, or load resistance. D-c outputs may be obtained by using a bridge rectifier. Multiple control windings allow the output to be proportional to the sum of several control signals. Some possible applications are: motor speed control, regulated power supplies, indicator light operation, relay operation, and alarm circuits. The first supplement will cover SR's with feedback, and self-saturating magnetic amplifiers.

S. T. Coffin

S. T. Coffin

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$KE = \frac{1}{2} m r^2 \omega^2$

$F = ma = m\omega^2 R$

$\frac{\omega^2 R \uparrow}{\omega^2 r^2 \downarrow} =$

R. L. Best

B077

Memorandum 6M-4774, S1

Sheet 1 of 6 Sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

**SUBJECT:** MAGNETIC AMPLIFIERS (Transient Response and Feedback in Saturable Reactors)

**To:** Distribution List

**From:** S. T. Coffin

**Date:** 4 February 1957

**Approved:** R. J. Callahan
R. J. Callahan

Abstract: The transient response of the ordinary saturable reactor is poor because of the inductive nature of the control circuit. The transient response can be improved by inserting control circuit resistance, but the power gain is reduced proportionally. The product of power gain times bandwidth remains constant and is determined only by the supply frequency. This product may be increased, however, by using feedback. It is also possible to obtain snap-action by using sufficient feedback. The disadvantages of feedback are increased complexity of the circuit and less linear operation. The case of unity feedback is of special importance because of its high dynamic gain, and because of its similarity to the more common self-saturating magnetic amplifier.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## 9.0 Transient Response of the Saturable Reactor

One of the most serious disadvantages of saturable reactors is their limited transient response, or in other words, their low cut-off frequency. The reason for this is the inductive nature of the control circuit. If the control voltage is changed abruptly, the control current, and hence the load current, will follow an exponential curve. Fig. 19 shows the transient response waveform of a typical saturable reactor.

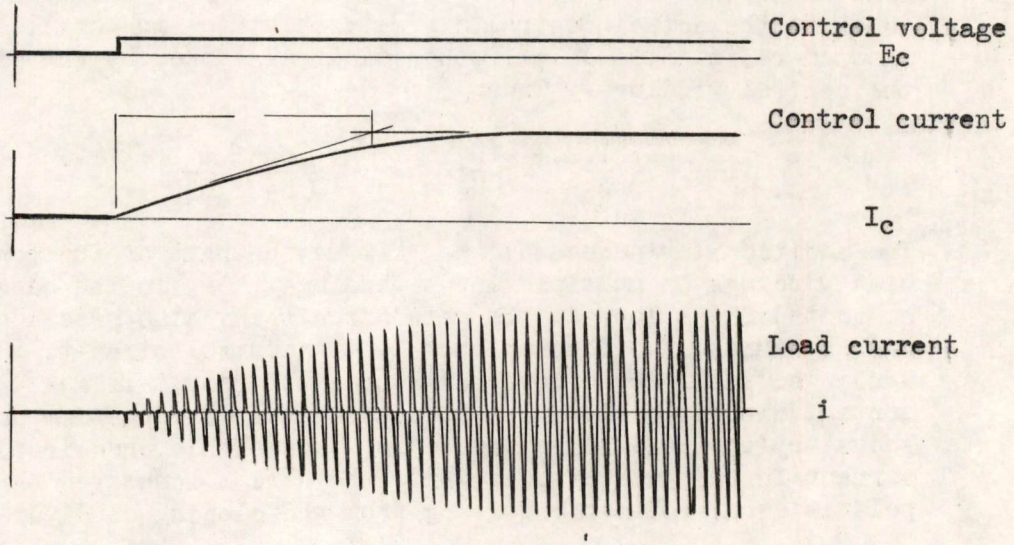



Fig. 19, Transient Response

The time constant T is determined by the equivalent control circuit resistance $R_c'$ and inductance L.

$$T = \frac{L}{R_c'} \qquad (13)$$

The equivalent circuit for the control current is shown in Fig. 20.

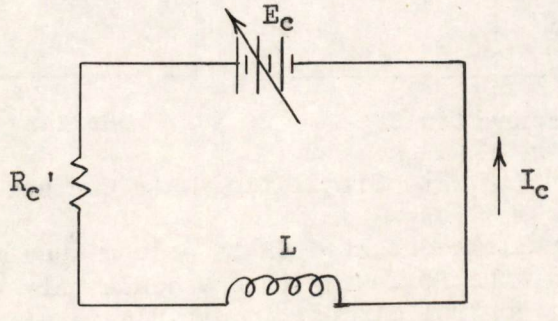


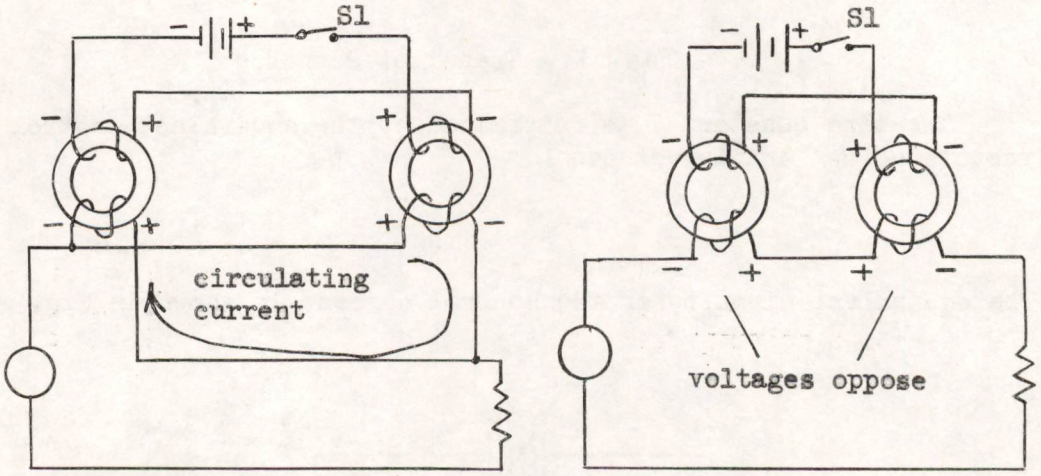

Fig. 20, Control Equivalent Circuit

It will be recalled that in Sections 4.2 and 4.3 of the original memorandum the control circuit resistance was assumed zero, but in Section 4.4 it was shown that zero control circuit resistance would produce infinite power gain. Now it can be observed that zero control circuit resistance would also result in an infinitely long time constant. But in practice, of course, there is always some resistance in the control circuit and the power gain and time constant are both finite.

The time constant my be found by evaluating $R_c'$ and L. The equivalent resistance seen by the control circuit of a saturable reactor is equal to the actual control circuit resistance in parallel with the reflected resistances of all other windings linked by the same flux as the control windings. Thus:

$$\frac{1}{R_c'} = \frac{1}{R_c} + \left(\frac{N_1}{N_c}\right)^2 \frac{1}{R_1} + \left(\frac{N_2}{N_c}\right)^2 \frac{1}{R_2} + \cdots \qquad (14)$$

The additional windings $N_1$, $N_2$, ... may be part of the control such as bias windings or multiple input windings. Or, in the case of the parallel-connected SR, a loop in the gate circuit may also pass a circulating current which is reflected back to the control circuit. Since the gate windings usually have low resistance, the result is a low equivalent control circuit resistance and consequently a long time constant. Fig. 21 shows why the parallel-connected SR passes this undesirable circulating current in the gate circuit while the series-connected SR does not. The polarities of voltage resulting from the closing of S1 are indicated.




Parallel-connected SR  Series-connected SR

Fig. 21, Circulating Gate Current

Since the parallel-connected SR is seldom used when response time is a consideration, the following theory deals only with the series-connected SR. The control circuit inductance is defined by the following expression:

$$L = 10^{-8} N_c \frac{d\phi'}{dI_c} \text{ henries} \qquad (15)$$

The net flux $\phi'$ linking the control windings is the difference of $\phi_a$ and $\phi_b$ as defined in Fig. 15.

$$\phi' = \phi_a - \phi_b \tag{16}$$

In order to determine the relation between $\phi'$ and control current $I_c$, the flux waveform of Fig. 16 of the original memorandum has been redrawn in Fig. 22.

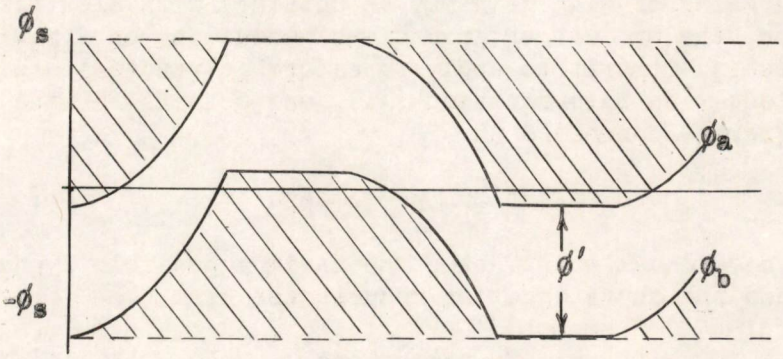



Fig. 22, Flux Waveform

It can be seen that for steady-state operation, $\phi'$ is constant. Furthermore, the peak-to-peak values of $\phi_a$ and $\phi_b$, and therefore the gate voltages, decrease linearly as $\phi'$ increases; so that at maximum output, the gate voltages are both zero and:

$$\phi' = 2\phi_s \tag{17}$$

Under this condition, the entire applied a-c voltage appears across the load, and:

$$E_a = E_r \tag{18}$$

where $E_r = I_r R$,

and $I_r = \frac{N_c}{N_g} I_c$

It has been assumed that the reactors are designed such that each gate winding is capable of absorbing half the applied voltage, that is:

$$\frac{1}{2} E_a = 2 \times 10^{-8} N_g (2\phi_s) f \tag{19}$$

Combining these equations, one obtains a linear relation between $\phi'$ and $I_c$:

$$\frac{\phi'}{I_c} = \frac{R}{4 \times 10^{-8} N_g f} \frac{N_c}{N_g} \tag{20}$$

Substituting into equation (15)

$$L = \left(\frac{N_c}{N_g}\right)^2 \frac{R}{4f} \tag{21}$$

The time constant of the control circuit is therefore:

$$T = \frac{1}{4f}\left(\frac{N_c}{N_g}\right)^2 \frac{R}{R_c'} \quad \text{seconds} \tag{22}$$

This equation shows that, other things being constant, the response time can be decreased by increasing the control circuit resistance. But adding control circuit resistance increases the control circuit dissipation and therefore decreases the power gain. Thus, fast response may be obtained by sacrificing gain, or high gain may be obtained with slow response. For this reason, the product of gain times bandwidth, or dynamic gain, is a useful figure of merit to apply to saturable reactors. Dividing the preceding equation into equation (11), one obtains for the dynamic gain D of the series-connected SR:

$$D = 4f \frac{R_c'}{R_c} \text{ per second} \tag{23}$$

If $R_c'$ can be made equal to $R_c$, then the maximum possible dynamic gain is obtained, and the above equation reduces to:

$$D = 4f \text{ per second} \tag{24}$$

This remarkably simple equation shows that only the frequency of the a-c power source ultimately limits the dynamic gain of the SR. If the dynamic gain is expressed in terms of cycles of the a-c source, equation (24) becomes merely:

$$D = 4 \text{ per cycle} \tag{25}$$

If the gate winding resistance, which has been neglected in these derivations, is taken into account, the actual dynamic gain available in a practical SR is slightly less than that given by the above equation.

Since the speed of response can be increased at the expense of power gain merely by increasing the control circuit resistance, large values of external resistance are sometimes inserted in the control circuit for this purpose. When this is done, the SR operates in a different mode from that described in Section 4.3, the output waveform becoming rectangular instead of sinusoidal as $R_c$ is made large compared to the equivalent load resistance, that is:

$$R_c \gg \left(\frac{N_c}{N_g}\right)^2 R \tag{26}$$

In this mode, the response time is practically zero since the control circuit supplies power to the load through transformer action, but the power gain is much less than unity. It will be shown in a later paper how this principle is used in a fast d-c voltage monitor.

## 10.0 Feedback in Saturable Reactors

### 10.1 Steady-State Operation

In certain applications, there are advantages to be gained by using feedback in SR circuits. The output current cannot be fed directly back into the control circuit, since the output is a-c and the control is d-c. But, if a bridge rectifier is added in the output circuit of a full wave SR, in theory a current waveform is obtained which is not only proportional to the control current but also identical in shape. If the rectified output current is now fed back by means of a second control winding $N_f$, the control characteristic of the SR may be altered considerably. One method of doing this is shown in Fig. 23. The load R may be connected in either the a-c or d-c side of the bridge.

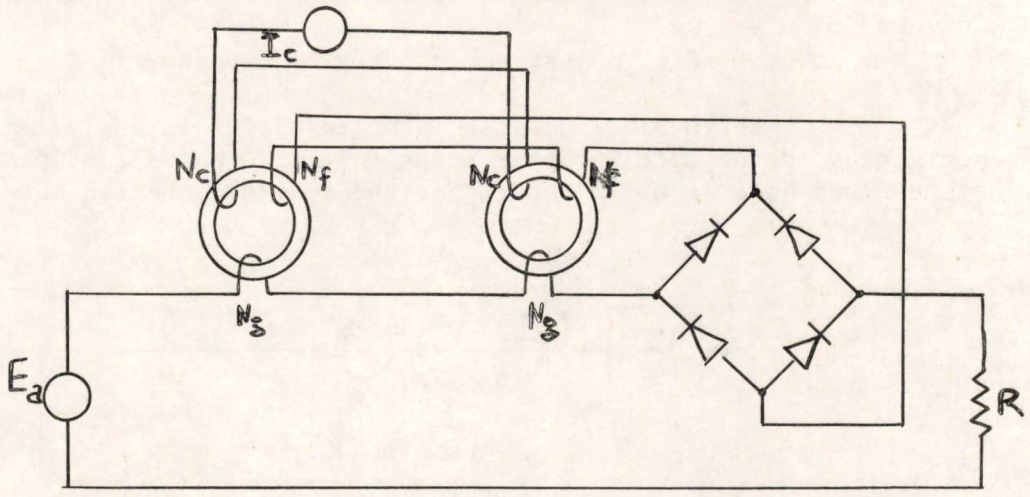



Fig. 23, Feedback

The steady-state effect of feedback in an amplifier may be analyzed by a simple graphical method shown in Fig. 24. The characteristic of the amplifier without feedback is first drawn. Then a "load line" is drawn, the slope of which corresponds to the amount of feedback. In order to obtain the new characteristic, the control current fed back, represented by the load line, is subtracted from the original control current. The effect is to shear the control characteristic to one side.

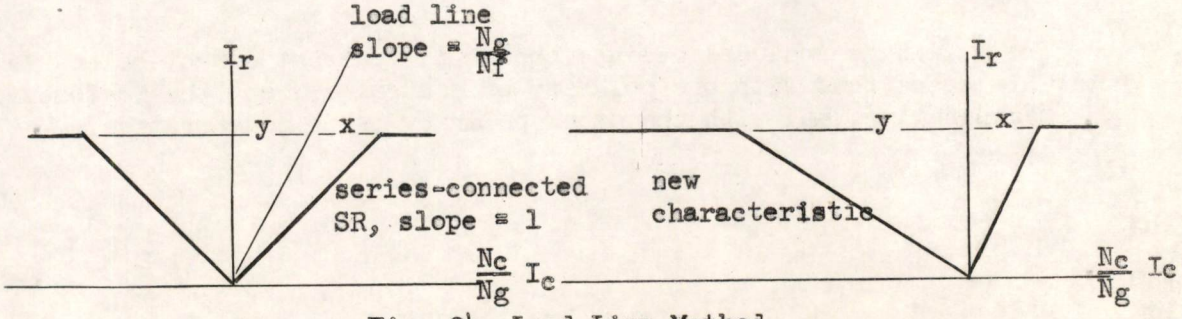



Fig. 24, Load Line Method

The effect of varying the amount of feedback is shown in Fig. 26. If, in the case of the series-connected SR, $N_f$ is made equal to $N_g$, then a theoretically infinite gain is obtained; and if the amount of feedback is further increased, the SR has the snap-action characteristic of a switching circuit.

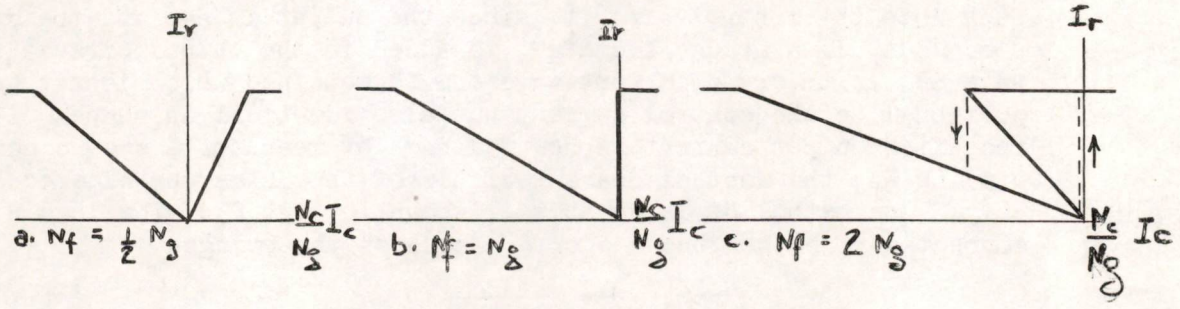



Fig. 25, Effect of Varying Feedback

A servo block diagram is often useful in analyzing circuits containing one or more feedback loops. Fig. 26 shows a simple steady-state block diagram of this sort for the series-connected SR.

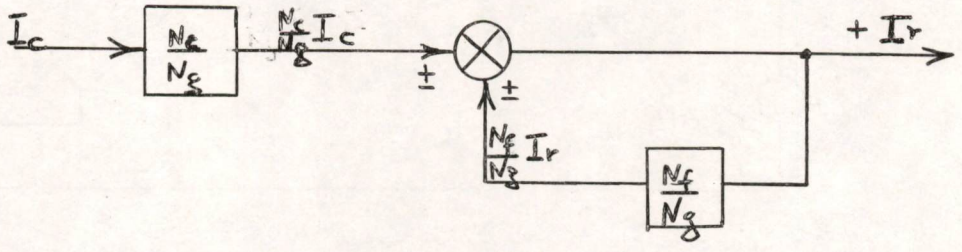



Fig. 26, Block Diagram of Series-Connected SR with Feedback

Using this block diagram, the closed-loop equation for the output current as a function of control current may be written by inspection:

$$I_r = \pm\left(\frac{N_c}{N_g} I_c + \frac{N_f}{N_g} I_r\right)$$

or

$$I_r = \frac{N}{\pm N_g - N_f} I_c \qquad (27)$$

The $\pm$ sign is included because the output current cannot be negative. This means that with one polarity of control current the feedback is regenerative, and with the other polarity it is degenerative.

## 10.2 Transient Response

An analysis of the transient response of the SR with feedback follows the same procedure as was given for the circuit without feedback but is slightly more involved. It can easily be shown, however, that the dynamic gain can be improved by using feedback. Consider the case where sufficient feedback is added to double the ampere-turn gain of the SR, ($N_f = 1/2N_g$). Now, only half as much control current is required to obtain full output current. This means that, for the same control voltage, the control circuit resistance may be doubled by adding external resistance. Thus, the control circuit dissipation is halved and the power gain doubled. The equivalent control circuit resistance is doubled, and the equivalent inductance is also doubled, since half the control current produces the same change of flux. The time constant therefore remains the same, and the dynamic gain has been doubled. In fact, if the ampere-turn gain is increased by a factor A using feedback, the dynamic gain is also increased by A and becomes:

$$D = 4A \quad \text{per cycle} \tag{28}$$

This increase in dynamic gain is one of the principle reasons for using feedback.

One other important feature of SR's with feedback is that the control time constant is not the same for either polarity of control voltage transient. In the preceding discussion of dynamic gain, it was assumed that the feedback circuit did not decrease the effective resistance of a circulating current in the feedback circuit. However, one polarity of control voltage will cause a circulating current in the feedback circuit which is reflected back into the control circuit causing a low equivalent resistance, as shown in Fig. 27.

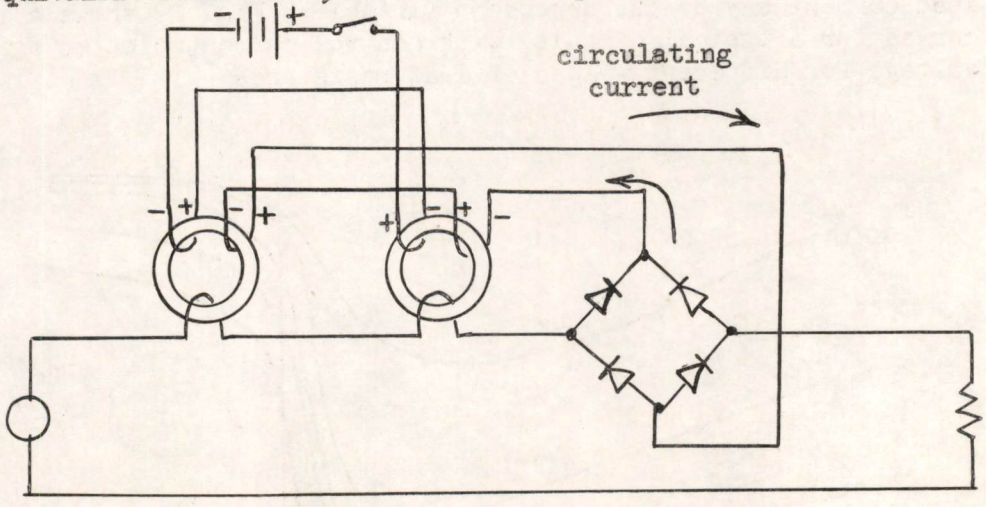



Fig. 27, Feedback Circulating Current

For control voltage transients of opposite polarity, this circulating current is blocked by the rectifiers.

## 10.3 Unity Feedback

The case of unity feedback in SR's is of special importance. It has been shown that the gain theoretically becomes infinite when $N_f = N_g$. In practice, the gain is never infinite because of the non-ideal characteristics of the cores and rectifiers. While these deviations from the ideal are hardly noticable in the characteristics of SR's without feedback, their effect becomes more pronounced as the feedback is increased. Fig 28 shows the actual characteristic (greatly exaggerated) of an SR with unity feedback derived by the load line method.

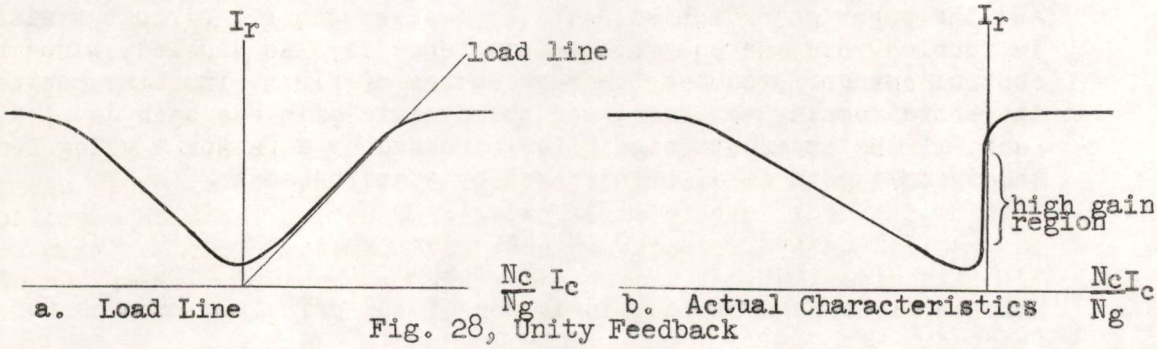



Fig. 28, Unity Feedback

The characteristics are no longer linear over a wide range, and the gain is greatest over only a portion of the regenerative region. In this region rectifier reverse current and core magnetizing current are the principle factors which limit the gain. Since these factors vary non-linearly with both load voltage and load current, an accurate analytical analysis of the circuit might be quite difficult. Consequently, the characteristics of the SR with unity feedback are often obtained experimentally and plotted as a family of curves. Either load voltage or load current may be the dependent variable. Fig. 29 shows a family of curves for a typical circuit, with control current plotted against load voltage for different values of load resistance.

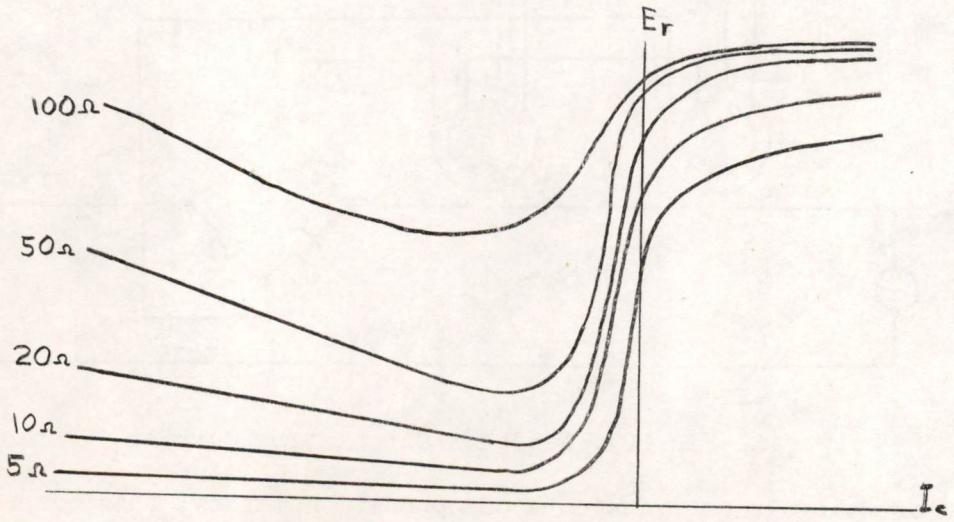



Fig. 29, Control Characteristics with Unity Feedback

## 11.0 Conclusions

The principle dynamic characteristics of the ordinary SR are slow transient response and limited dynamic gain. Higher power frequencies are often used to obtain improved performance, and often make possible savings of size and cost also. To obtain best transient response, circulating currents must be suppressed in all circuits coupled to the control windings, and the control resistance must be made as high as possible.

Feedback alters the control characteristics, and can be used to improve the dynamic gain by several orders of magnitude. The effect of the non-ideal characteristics of the components becomes more pronounced in the regenerative region as the feedback is increased, and drift becomes more of a problem. However, since the amount of feedback is determined by a turns-ratio, there is little danger of drift causing instability as it may in other types of positive feedback amplifiers. The case of unity feedback has been given special consideration because of its similarity to the self-saturating magnetic amplifier, which will be described in the second supplement.

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S. T. Coffin

B 077 R.L. Best

Memorandum 6M-4774, S2

Sheet 1 of 12 Sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

**SUBJECT:** MAGNETIC AMPLIFIERS (Self-Saturating Magnetic Amplifiers)

**To:** Distribution List

**From:** S. T. Coffin

**Date:** 3 April 1957

**Approved:** R. J. Callahan
R. J. Callahan

**Abstract:** The self-saturating magnetic amplifier may be considered as a simplified version of the saturable reactor with unity feedback. The high dynamic gain is accomplished by placing a rectifier in series with each gate winding. The half-wave circuit consists of only one core and one rectifier. The full wave circuits operate in a similar manner as the half-wave circuit, but have lower control circuit losses. They may have either a d-c or a-c load, and require two cores. Highest gain is obtained by using cores with high permeability and rectifiers with low leakage current. The a-c flux reset circuit accomplishes high gain and fast response by using an a-c voltage and rectifier in the control circuit. The circuit schematics, waveforms, and control characteristics of the various circuits are shown.

Included in the appendix are calculations for the design and performance of a typical magnetic amplifier, a list of abbreviations used, and a table of the more important properties of the various circuits.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## 12.0 Derivation of Self-Saturating Magnetic Amplifier

The saturable reactor with unity feedback has been described in the preceding supplement. Although this circuit has many desirable features, it is seldom used. A somewhat different circuit accomplishes the same results with fewer rectifiers and without the need for feedback windings. Fig. 30 shows how the self-saturating magnetic amplifier is derived from the saturable reactor. The saturable reactor with unity feedback is shown in Fig. 30a. Arrows indicate the direction of flow of load current and resulting MMF during the positive half-cycle of a-c supply voltage. It can be seen that the gate and feedback windings on core A aid each other and may therefore be replaced by one winding having twice as many turns. On core B, the two windings oppose each other and behave as a short circuit. The resulting equivalent circuit for this half cycle is shown in Fig. 30b. The two rectifiers in series have been replaced by one rectifier. This is the basic half-wave self-saturating circuit.

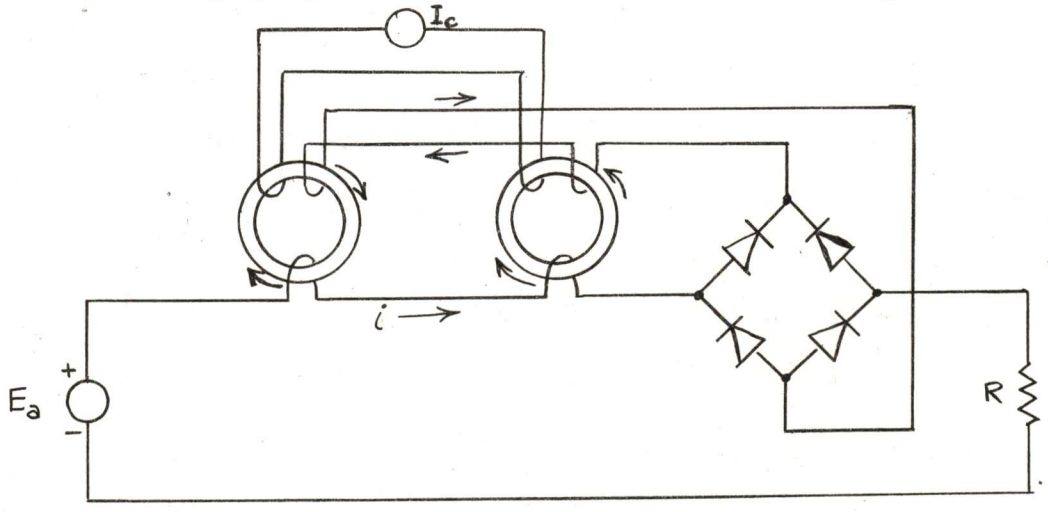


Fig. 30a, Saturable Reactor with Feedback

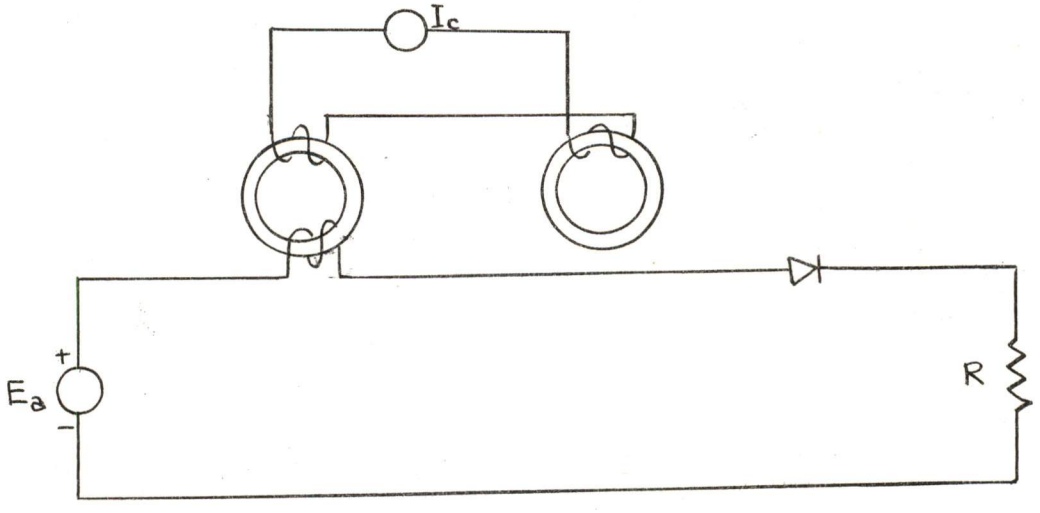


Fig. 30b, Equivalent Circuit

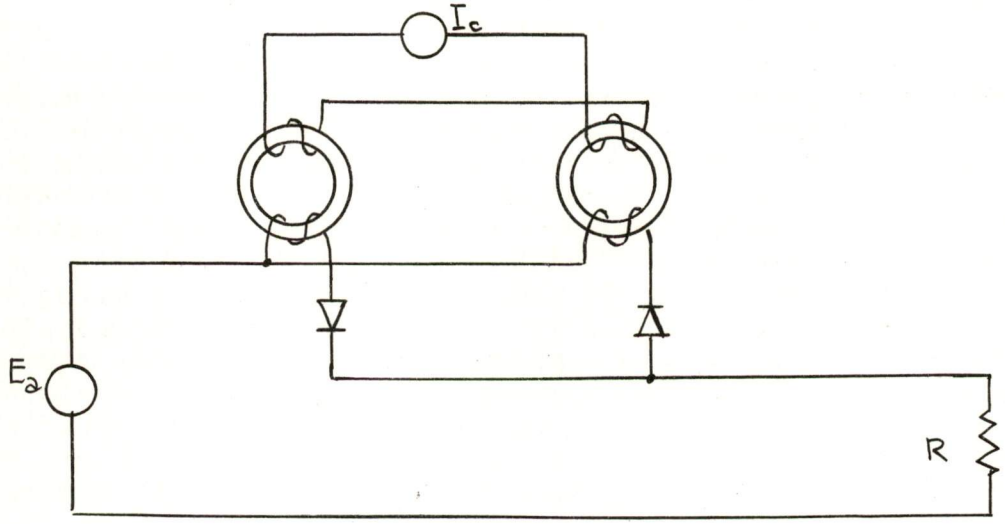


Fig. 30c, A-C Self-Saturating Circuit

A similar equivalent circuit is obtained for the next half-cycle of a-c supply voltage. Fig. 30c shows the two half-wave circuits combined to form the full-wave a-c self-saturating circuit, corresponding to the SR circuit of Fig. 30a.

## 13.0 Half-Wave Self-Saturating Circuit

### 13.1 Operation of the Half-Wave Self-Saturating Circuit

Since the theory of operation of all the self-saturating circuits is basically the same, only the half-wave circuit, because of its simplicity, will be described in detail. The circuit is shown in Fig. 31 with polarities indicated.

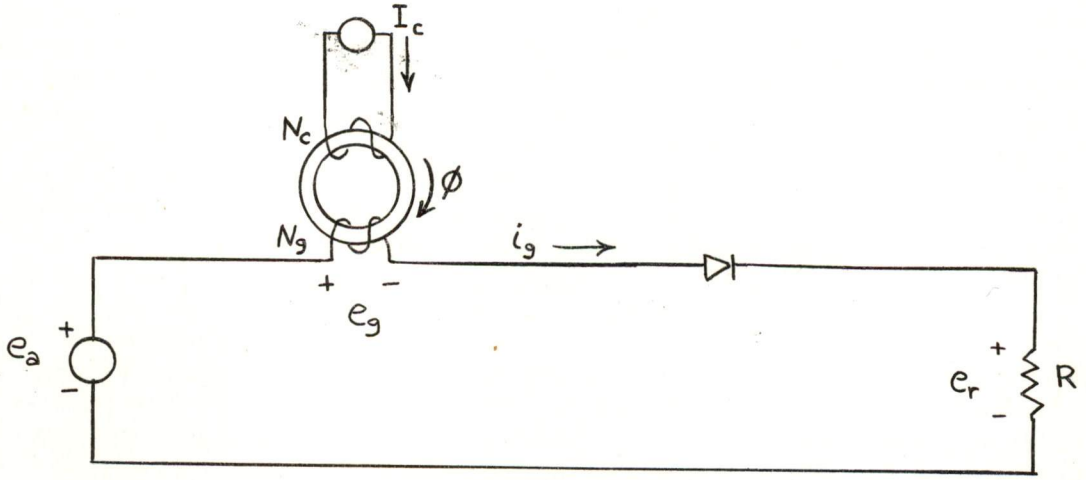


Fig. 31, Half-Wave Circuit

The control is assumed to be a high impedance current source. The operation of the circuit can be understood most easily by first considering what happens during the negative, or non-conducting, half-cycle of supply voltage. During the period that there is an inverse voltage across the rectifier, no current flows in the gate windings; and the only MMF present is that of the control winding. In order to analyze the situation, the exact nature of the hysteresis loop must be considered. The assumed hysteresis loop is shown in Fig. 32.

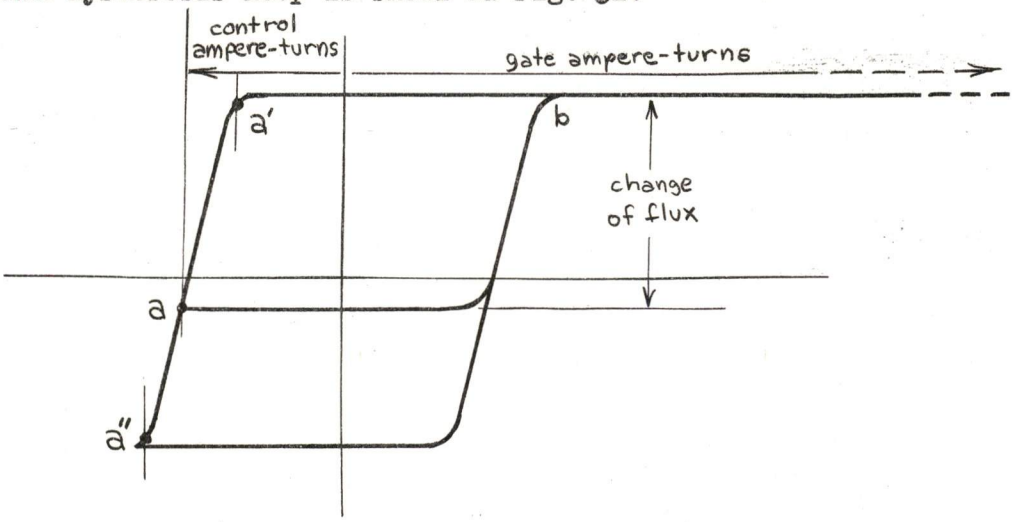


Fig. 32, Hysteresis Loop

The control and gate windings are connected such that their MMF's are opposing. During the conducting portion of the previous cycle, operation of the core was along the right-hand saturated arm of the hysteresis loop, and at the end of the conduction period, operation took place toward the left along the top of the loop. Now, with no gate MMF, and a certain control MMF indicated by the arrow at top, operation proceeds down the left-hand side of the loop to point a. When the a-c supply voltage begins its positive half-cycle, voltage is impressed across the gate winding, a small magnetizing current flows, and the flux begins to increase toward saturation. When the flux reaches saturation at point b, the gate voltage collapses and the applied voltage is impressed across the load. At the end of the positive half-cycle of supply voltage, the gate current approaches zero and the flux is again reset to point a by the control ampere-turns. The average voltage absorbed by the core is, of course, proportional to the change of flux.

If the control ampere-turns are reduced to an amount a ', there is no flux change and no voltage is absorbed by the core. A further decrease or change of polarity of the control ampere-turns has no effect on the output. With no control current, the core remains saturated at all times, hence the name "self-saturating." If the control ampere-turns are increased to an amount a", then the entire

hysteresis loop of the core is traversed and the load voltage is a minimum. Assume, as in the case of the saturable reactors, that the core is designed to absorb just the full supply voltage, that is:

$$E_a = 2 \times 10^{-8} N_g (2\phi_s) f$$

Then the average load voltage is varied from zero to 1/2 $E_a$ as the control ampere-turns are decreased from a" to a'. The resulting control characteristic, which has a shape similar to one side of the hysteresis loop, is shown in Fig. 33.

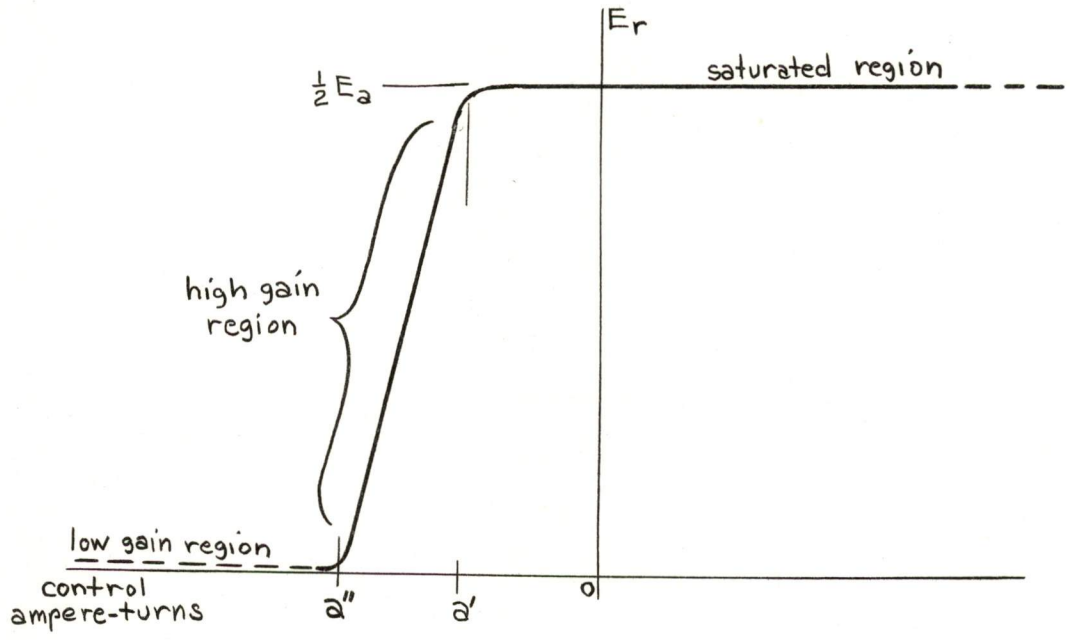


Fig. 33, Control Characteristic of Half-Wave Circuit

The waveforms for the half-wave circuit are shown in Fig. 34.

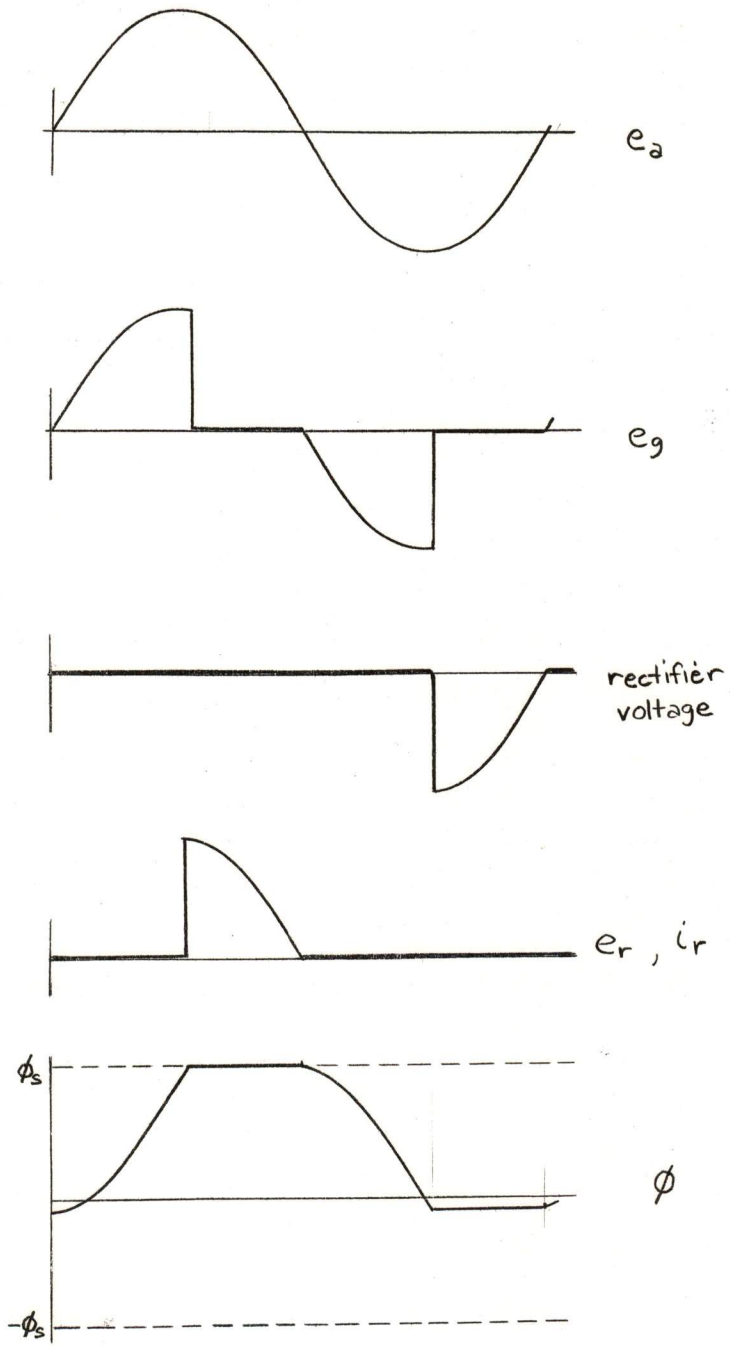


Fig. 34, Waveforms of Half-Wave Circuit

## 13.2 Gain of Half-Wave Circuit

### 13.2.1 Nature of Hysteresis Loop

The gain of the circuit depends to a great extent on the characteristics of the core, in particular on the slope of the descending side of the hysteresis loop from a' to a". If this slope is known, the gain may be expressed in volts per ampere by determining the amount of control current required to traverse from a' to a" on the hysteresis loop, and calculating the corresponding change in output voltage. But the hysteresis loop that the core describes in this circuit may be quite different from the d-c or sinusoidal excitation hysteresis loops which are ordinarily published, and also depends on the core shape as well as material. It is really the locus of the points a' to a" that is important rather than the actual shape of the loop. This is illustrated in Fig. 35, which shows the actual hysteresis loops traced by a deltamax core in a self-saturating circuit for different values of control current.

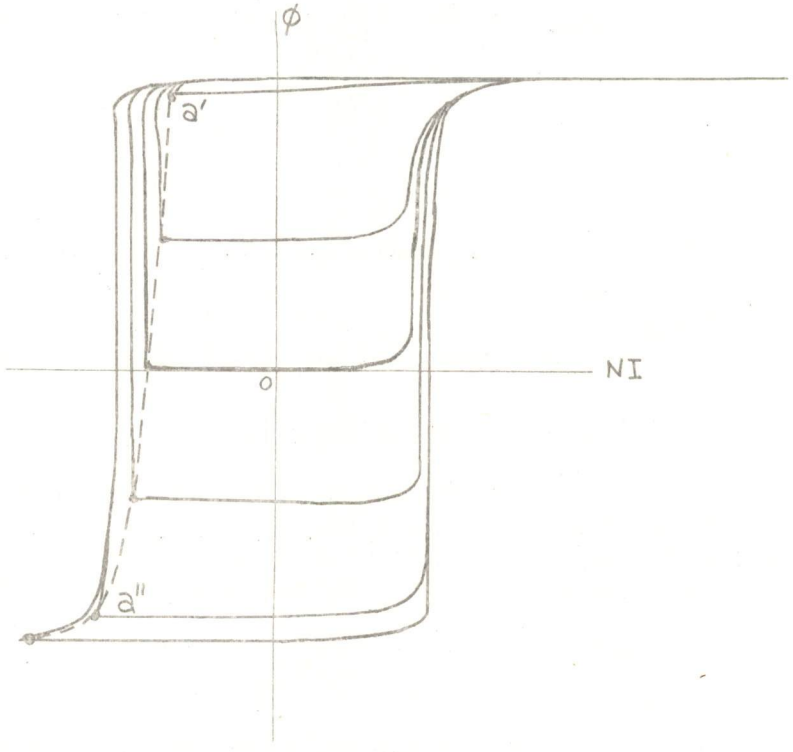


Fig. 35, Minor Hysteresis Loops of Deltamax Core

The locus of the points a' to a" is indicated by the broken line. This line shows that the gain is much less than would have been calculated from the major hysteresis loop alone. This undesirable effect is caused by the eddy currents and other phenomena in the core material.

### 13.2.2 Rectifier Leakage Current

Rectifier leakage current also has an important effect on the gain of the circuit. Zero leakage current has been assumed up to this point. If the control current is made large enough to produce zero output (a"), then there is no reverse voltage across the rectifier and hence no leakage current. If the control current is now reduced, the output voltage and rectifier inverse voltage and leakage current increase. But the leakage current flows in such a direction as to oppose the decrease in control current. Hence its action is degenerative and reduces the gain. For this reason, silicon rectifiers are desirable because of their low leakage. Selenium rectifiers are to be avoided in this circuit, not only because their high leakage current reduces gain, but their variation in leakage current as they age causes drift of the control characteristics. Rectifier capacitance also has a degenerative effect. Fig. 36 shows the effect of rectifier leakage current on the control characteristic.

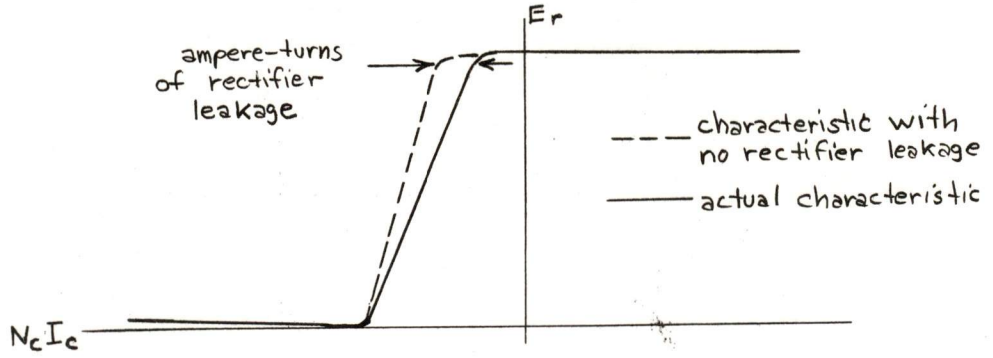


Fig. 36, Effect of Rectifier Leakage Current

### 13.2.3 Calculating the Gain

Once the exact nature of the dynamic hysteresis loops of the core and the rectifier leakage current are known, the calculation of the control characteristic may be made. The change in output voltage from minimum to maximum output may be calculated by the equation:

$$\Delta E_r = 10^{-8} N_g (2\phi_s) f$$

The control ampere-turns required to traverse from minimum to maximum output may be found by adding the ampere-turns a"-a' of Fig. 33 and the rectifier leakage ampere-turns of Fig. 36. The gain may be expressed as the ratio of these quantities in volts per ampere-turn. A sample calculation is given in the appendix. Often a more important quantity is the power gain. The maximum possible power gain for a half-wave self-saturating circuit is relatively low for the same reason as in the half-wave SR—a large control circuit impedance is required to block a-c components of current. Hence, the full-wave circuits are more commonly used.

## 14.0 Full-Wave Self-Saturating Circuits

### 14.1 Circuit Configuration

The three basic full-wave self-saturating circuits and their corresponding waveforms are shown in the following figures. They all may be considered as combinations of two half-wave circuits, and their operation is very similar to that of the half-wave circuit. The principle differences are that load current flows every half-cycle, and only second and higher harmonic voltages are induced in the control circuit. Similar to saturable reactors, the solution of the circuit depends upon the control source impedance. A constant current control is assumed. If the control source has zero impedance, the operation of the circuits are somewhat different but the resulting control characteristics turn out to be nearly the same.

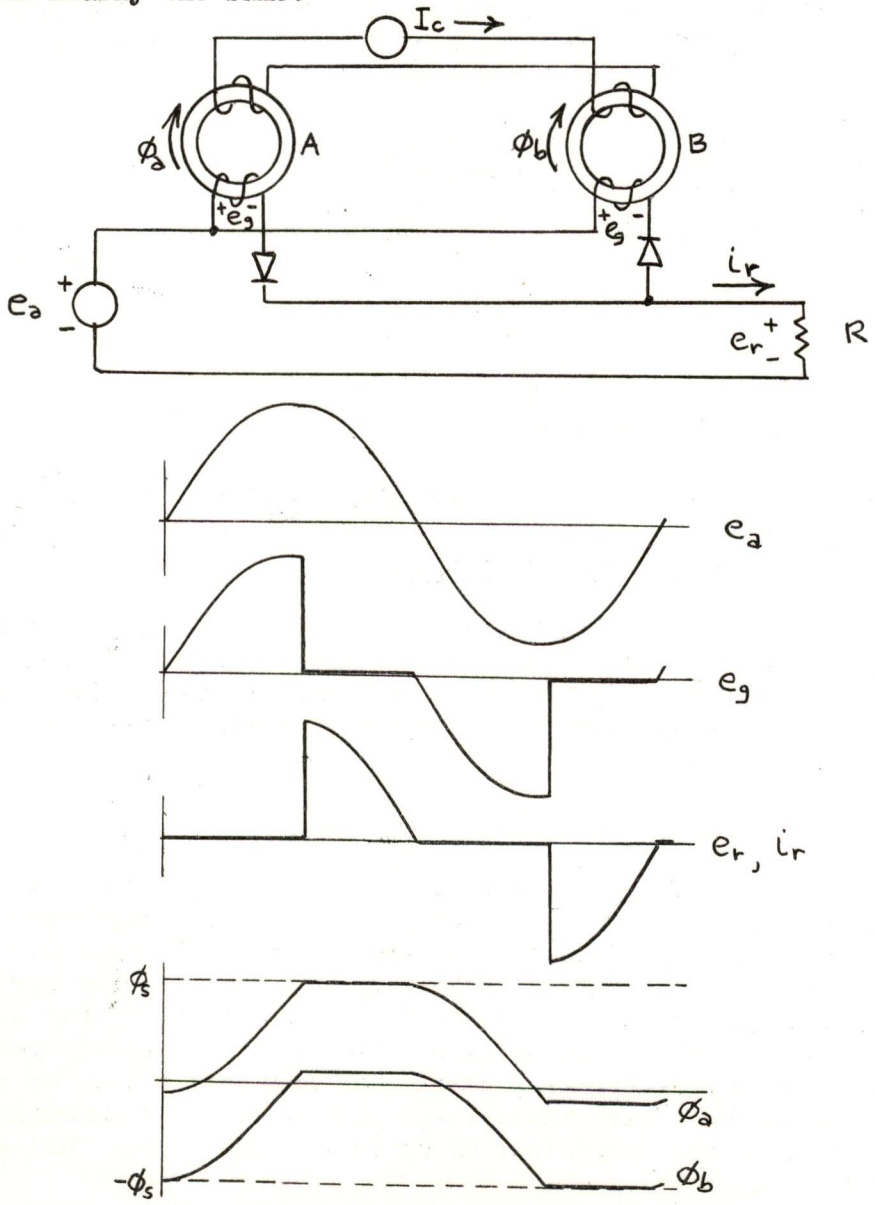


Fig. 37, A-C Self-Saturating Circuit

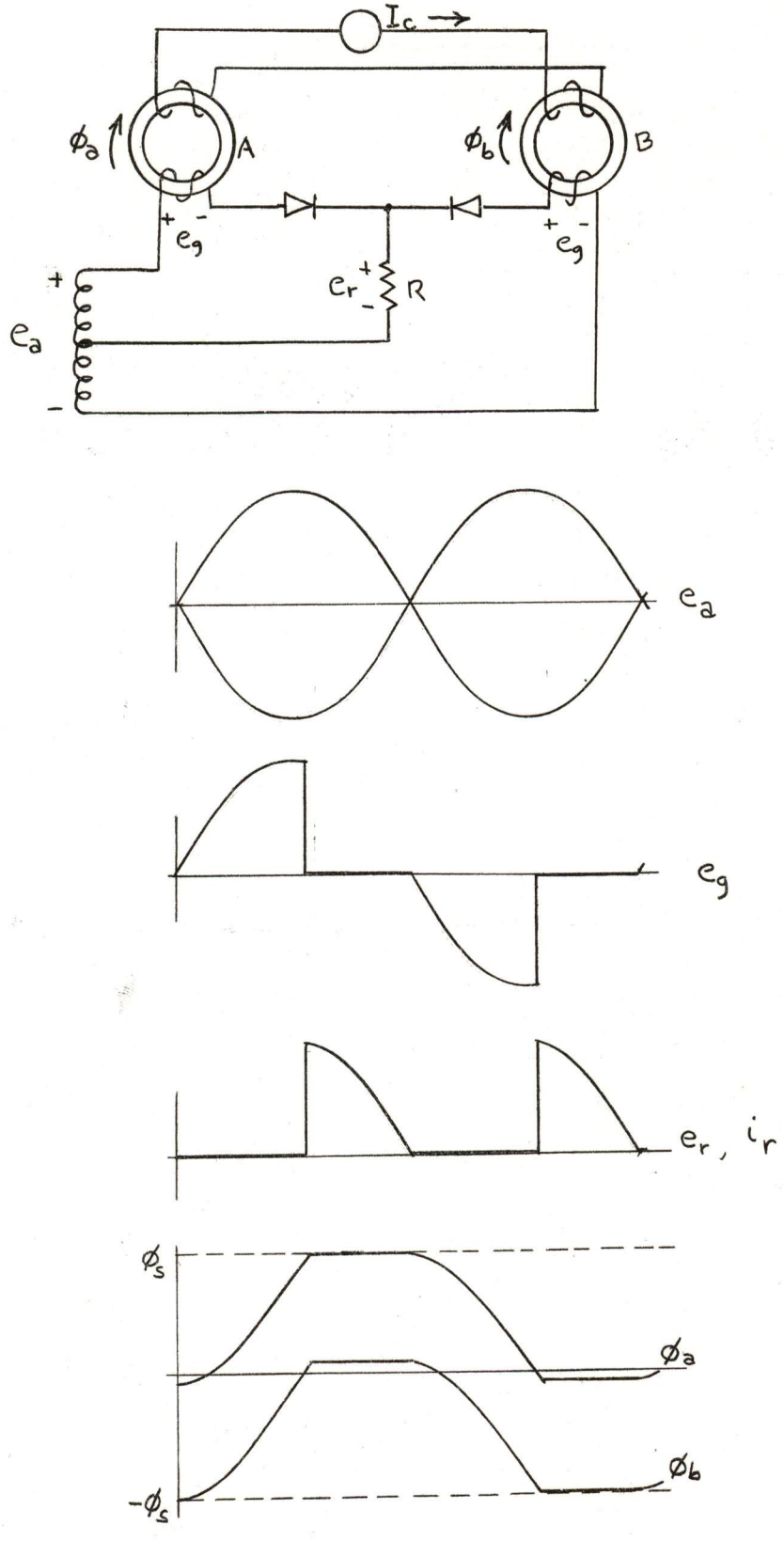


Fig. 38, Center-Tap Self-Saturating Circuit

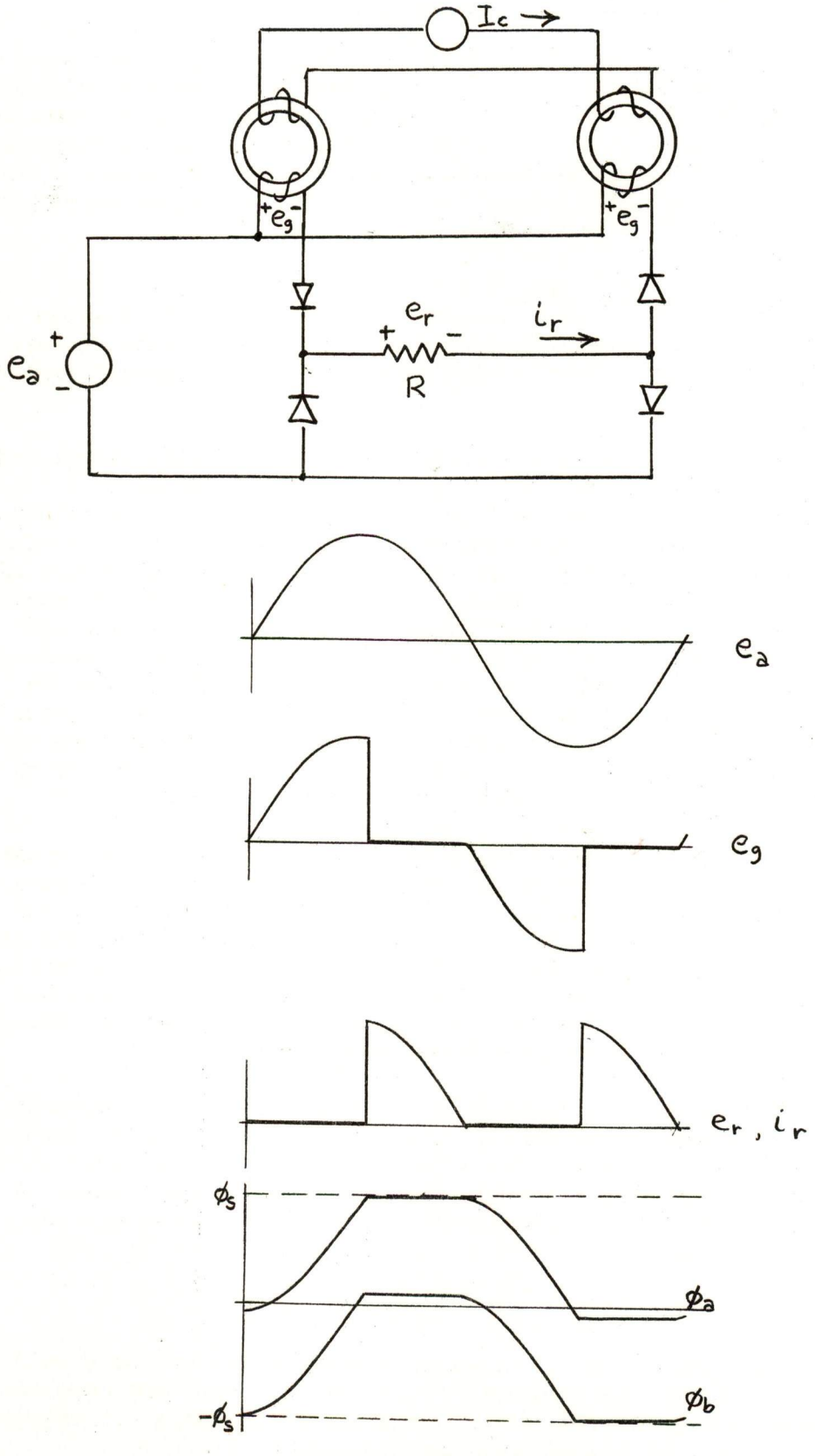


Fig. 39, Bridge Self-Saturating Circuit

## 14.2 Gain and Transient Response

The volts per ampere-turn gain of any of the full-wave circuits described may be calculated in the same manner as was outlined for the half-wave circuit. The change in output voltage from minimum to maximum is obtained directly from Faraday's Law, and the corresponding control ampere-turns are obtained from the appropriate dynamic hysteresis loop of the core, also taking into account the leakage ampere-turns of the rectifiers if it is appreciable.

The power gain may be defined in various ways. One method is to take the change in load dissipation from minimum to maximum output and divide by the maximum control circuit dissipation, which occurs at minimum output. This is very simple once the control characteristic has been determined.

Calculation of the transient response is also simple, since the method described in section 9.0 still applies. The control circuit inductance is found by equation (15), where the total change in flux is again $2\phi_s$; and the corresponding change in control current is found as described above. The equivalent control circuit resistance is also found by methods already described. Similar to the saturable reactor with feedback, an objectionable circulating current flows with one polarity of control voltage, increasing the time constant. Examination of Figs. 37, 38, and 39 will show that this current flows when the output is turned off. It is most severe in the case of the a-c circuit since it encounters only the resistance of the two gate windings and the forward resistance of the two rectifiers, whereas in the two d-c circuits it must also flow through the load.

An objectionable feature of self-saturating magnetic amplifiers is that the response time is limited to not less than approximately one-half cycle of the a-c supply. The flux in each core is "reset" during the negative half-cycle of a-c supply voltage, and the core is "fired" during the next positive half-cycle. Thus there is a "dead time" between the time of application of a control signal and the time that there is any effect on the output. The only way to reduce this time appreciably is to use higher power frequency.

The power gain divided by the time constant, or dynamic gain, is again a useful figure of merit. Similar to the saturable reactor with feedback, the quality of the cores and rectifiers, as well as the power frequency, determines the maximum obtainable dynamic gain. A sample calculation of the performance of a typical self-saturating circuit is given in the appendix.

## 15.0 A-C Flux Reset Circuit

One other common circuit closely related to the ordinary self-saturating circuits is the a-c flux reset circuit. It was mentioned that the half-wave self-saturating circuit had the disadvantage of requiring

a large impedance in the control circuit to block a-c components of current. A low impedance control circuit would effectively short-circuit the core. A method of overcoming this problem is shown in Fig. 40. The a-c voltage $e_a$ and a rectifier have been added to the control circuit. The a-c voltage is of such a polarity as to cause an inverse voltage across the control circuit rectifier during the positive or conducting half-cycle of a-c supply voltage.

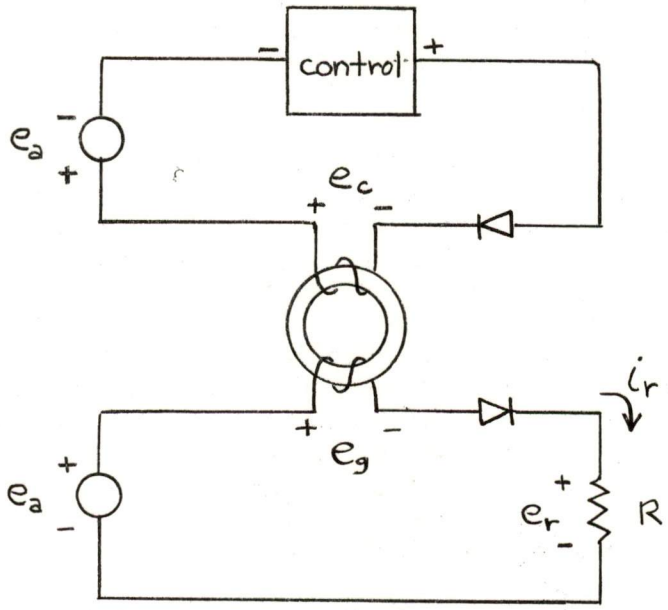


Fig. 40, A-C Flux Reset Circuit

Assume the gate and control windings have the same number of turns. If the control is a short circuit, then the full voltage Ea will be applied to the control winding during the negative half-cycle and the flux will be completely reset. During the following half-cycle the entire a-c supply voltage will be absorbed by the gate winding and the output will be zero. But if the control is an open-circuit, then the core remains saturated at all times and maximum output is obtained. Any passive circuit element that will absorb a controllable amount of the a-c voltage in the control circuit can be used to control the output, such as a variable resistance, variable a-c voltage, or variable d-c bias. Fig. 41 shows the waveforms obtained when a half-wave a-c voltage is used as the control.

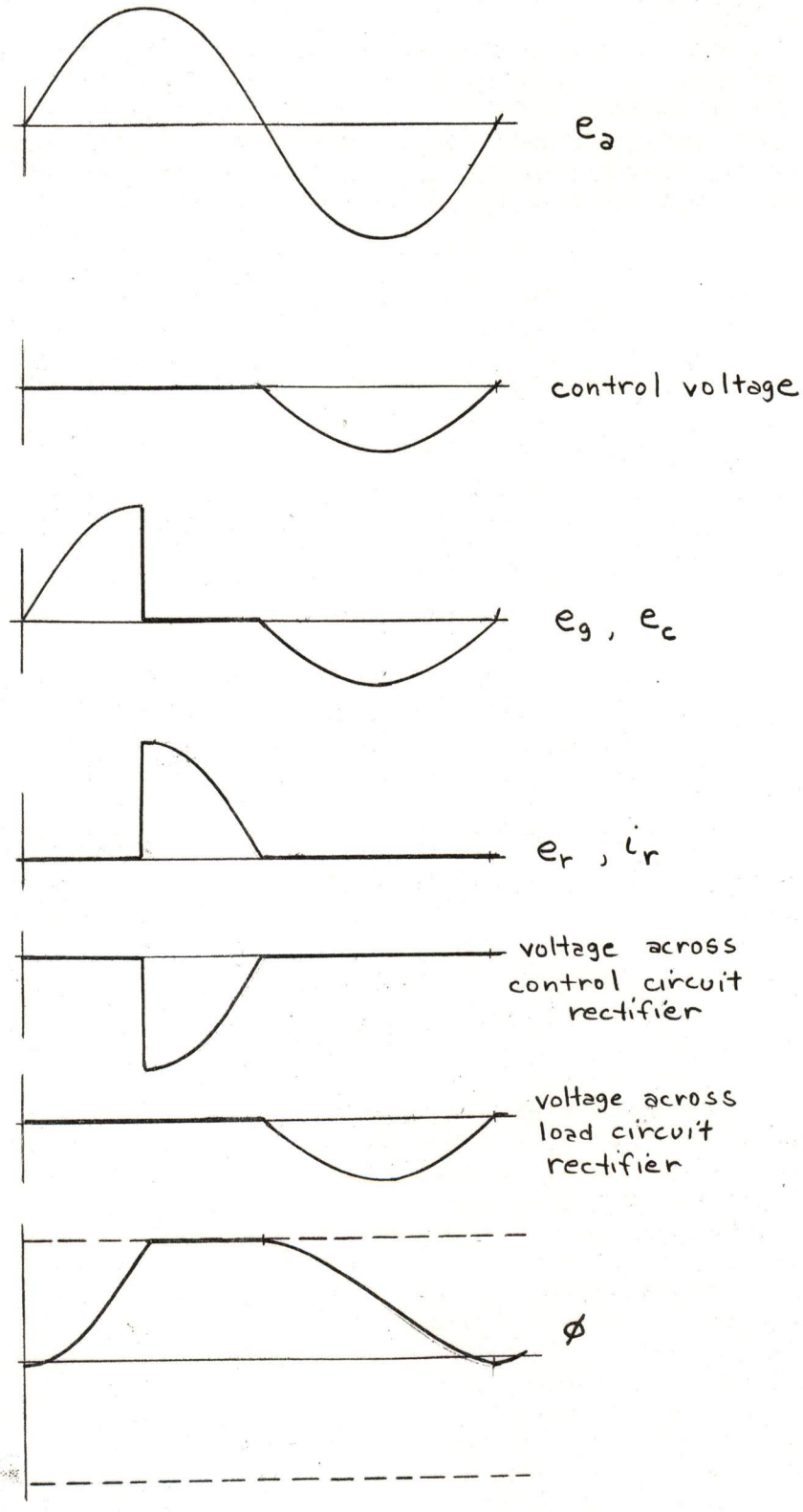


Fig. 41, Waveforms of A-C Flux Reset Circuit with Half-wave A-C Control Voltage

Advantages of this circuit over the ordinary self-saturating circuits are:

1. The voltage gain is independent of the core characteristics and depends entirely upon the turns ratio.

2. The control does not exhibit an inductive time constant and the response is therefore inherently half-cycle.

3. The power gain can be made high by using core materials with low hysteresis losses. The control power corresponds to the area of the hysteresis loop.

4. Only one core and power rectifier are required.

Disadvantages are:

1. Multiple control windings cannot be used in the usual way to obtain the sum of several isolated inputs.

2. Except for a-c voltage control, poor linearity is obtained between input and output.

3. The rectifier in the control circuit can introduce drift of the control characteristics, and also makes it necessary that the signal voltage be large compared to the forward voltage drop of the rectifier.

A more complete description of this circuit may be found in a paper by R. A. Ramey.*

## 16.0 Conclusions

The self-saturating magnetic amplifier achieves the high dynamic gain of the saturable reactor with feedback simply by having a rectifier in series with each gate winding. The example in the appendix shows a gain of 26,000 per second with a control requirement of 17 volts and 8.5 ma., using average quality silicon rectifiers, the poorest of core materials, and the lowest of power frequencies. A 150 mw. transistor can drive this circuit easily. A future paper will describe how this combination of a transistor driving a magnetic amplifier has been used with success in regulated d-c power supplies.

Included in the appendix are calculations for a typical magnetic amplifier, a list of abbreviations used, and a table of the more important properties of the various circuits which have been discussed.

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* R. A. Ramey, On the Control of Magnetic Amplifiers, AIEE Transactions, volume 79, 1951.

STC:smm
Attachments: Appendix A
Table A
Table B

S. T. Coffin

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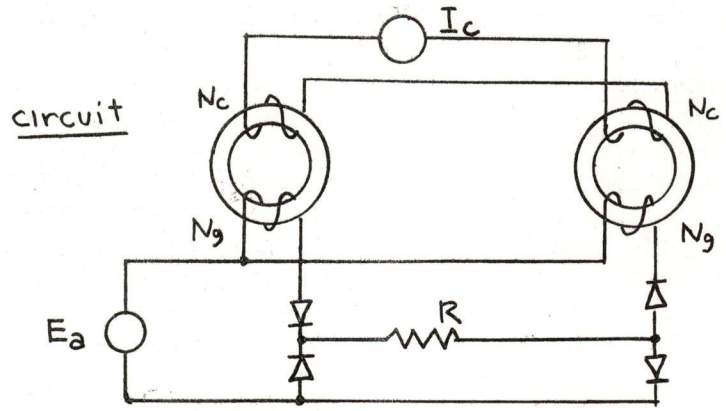
## Appendix A

### I. Sample Calculations for a Bridge Self-Saturating Magnetic Amplifier




Given: $E_a$ = 100 volts, 60 cycles
R = 20 ohms
maximum output required = 4 amps
full load dissipation = $(4)^2$ x 20
= 320 watts

Core

cores chosen: Arnold #5468-L12 selectron, 12 mil.

I.D. = 2.5 in.
O.D. = 3.5 in.
height = 1.0 in.
thickness = .5 in.

cross sectional area = .5 x 1.0
= .5 sq. in.

effective area = .5 x .95 (sect. 22)
= .48 sq. in.

saturation flux density = 100,000 lines/sq. in. (Fig. 1)

saturation flux $\phi_s$ = 100,000 x .48
= 48,000 lines

window area W = $\pi$ x $(1.25)^2$
= 4.9 sq. in.

volt-ampere rating of core = $1.2 \times 10^{-5}$ x 48,000 x 60 x 4.9 (sect. 60)
= 170 volt-amperes

Gate Winding

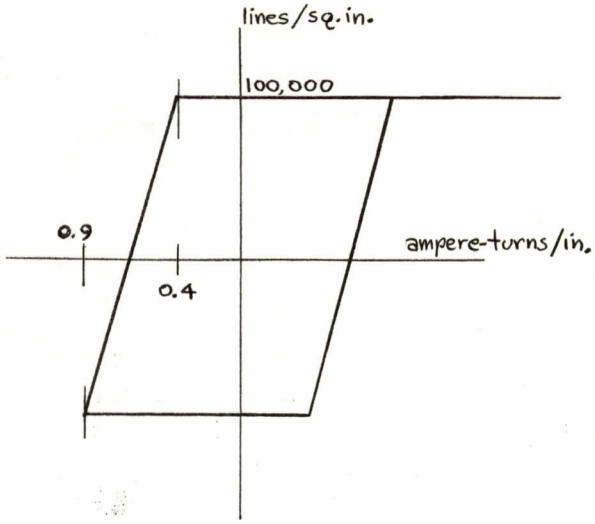
$$\text{gate turns } N_g = \frac{100}{2 \times 10^{-8} \times 2 \times 48{,}000 \times 60} \quad \text{(sect. 3.1)}$$

$$= 870 \text{ turns}$$

Control Characteristics

assumed hysteresis loop of core material:

(based on experimental data as indicated in Fig. 35)




mean core circumference = $\pi \times 3$
= 9.4 in.

a' = 0.4 x 9.4 (Fig. 32)
= 3.8 ampere-turns

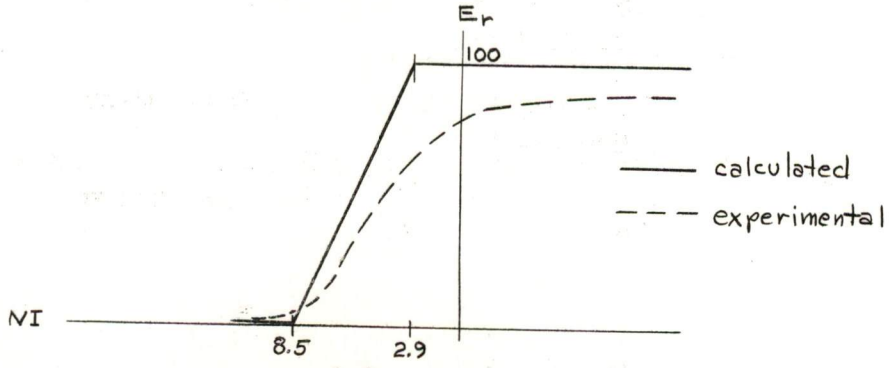
a" = 0.9 x 9.4 (Fig. 32)
= 8.5 ampere-turns

rectifier chosen: Sarkes Tarzian 10 LF silicon rectifier

leakage current = .001 amps (approx.)
rectifier leakage ampere-turns = .001 x 870 (Fig. 36)
= .9 ampere-turns

control ampere-turns for max. output = 3.8 - .9
= 2.9 ampere-turns

resulting control characteristic:



Note: The experimental results show a maximum output voltage lower than the calculated value because of core saturated inductance and gate winding resistance which were neglected in the calculations. In practice, therefore, the applied a-c voltage must be made somewhat larger than the maximum output voltage required.

Gain

control turns $N_c$ chosen: 1000 turns #24 wire
resistance of each control winding = 1000 x .3 ft/turn x 0.26 ohms/ft
= 7.8 ohms

total control winding resistance = 7.8 x 2
= 15.6 ohms

maximum control current required = 8.5/1000
= .0085 amps

control winding dissipation = $(.0085)^2$ x 15.6
= .0011 watts

maximum power gain = 320/.0011 (Sect. 14.2)
= 290,000

Transient Response

control circuit inductance L = $10^{-8}$ x 1000 x $\frac{96,000}{.0056}$ (Equation 15)
= 170 henries

time constant T = 170/15.6
= 11 sec.

dynamic gain = 290,000/11
= 26,000 per sec.

assume 2000 ohms inserted in control circuit to improve transient response.

T = 170/2015
= .085 sec.

control dissipation = $(.0085)^2$ x 2015
= .145 watts

## II. Abbreviations Used

| Symbol | Meaning | Page |
|---|---|---|
| A | ampere-turn gain | 27 |
| a | control ampere-turns | 32 |
| a' | control ampere-turns at upper knee | 32 |
| a" | control ampere-turns at lower knee | 32 |
| b | point of saturation | 32 |
| D | dynamic gain | 24 |
| $E_a$ | average applied a-c voltage | 7 |
| $E_c$ | average control voltage | 21 |
| $E_r$ | average load voltage | 8 |
| $e_a$ | instantaneous applied a-c voltage | 6 |
| $e_c$ | instantaneous control winding voltage | 12 |
| $e_g$ | instantaneous gate winding voltage | 6 |
| $e_r$ | instantaneous load voltage | 6 |
| f | frequency of applied a-c voltage | 7 |
| $I_a$ | average applied a-c current | 19 |
| $I_a$ | average current in gate A | 13 |
| $I_b$ | average current in gate B | 13 |
| $I_c$ | average control current | 9 |
| $I_r$ | average load current | 13 |
| $i_a$ | instantaneous current in gate A | 13 |
| $i_b$ | instantaneous current in gate B | 13 |
| $i_c$ | instantaneous control current | 16 |
| $i_g$ | instantaneous gate current | 6 |
| $i_r$ | instantaneous load current | 12 |
| I.D. | inside diameter | 5 |
| L | control circuit inductance | 21 |
| MMF | magnetomotive force | 5 |
| $N_c$ | control winding turns | 9 |
| $N_f$ | feedback winding turns | 25 |
| $N_g$ | gate winding turns | 6 |
| NI | ampere-turns | 6 |
| O.D. | outside diameter | 5 |
| R | load resistance | 6 |
| $R_c$ | control circuit resistance | 18 |
| $R_c'$ | equivalent control circuit resistance | 21 |
| SR | saturable reactor | 6 |
| T | control time constant | 21 |
| VA | volt-amperes | 20 |
| W | core window area | 19 |
| $\phi$ | flux | 6 |
| $\phi_a$ | flux in core A | 12 |
| $\phi_b$ | flux in core B | 12 |
| $\phi_s$ | saturation flux | 5 |
| $\phi'$ | net flux linking control windings | 23 |

III. Properties of Magnetic Amplifier Circuits

TABLE A: Circuits Without Rectifiers

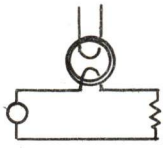
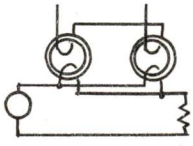
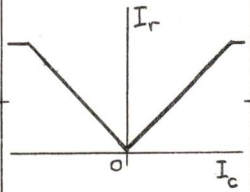
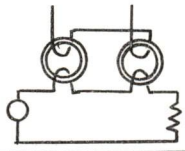
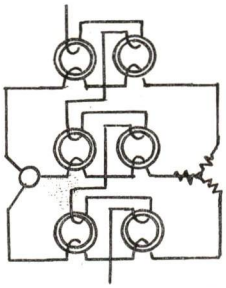
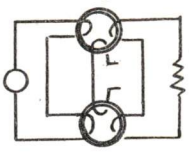
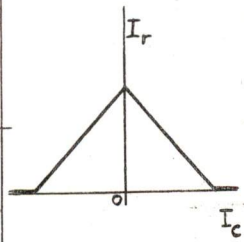
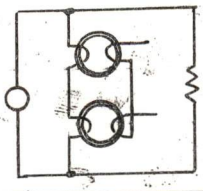
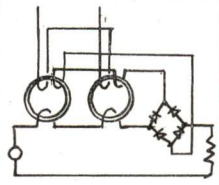
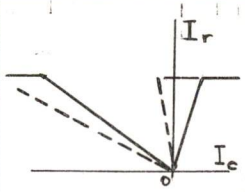
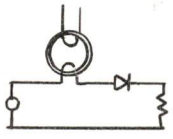
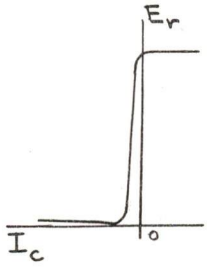
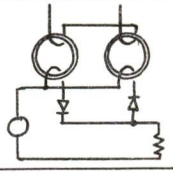
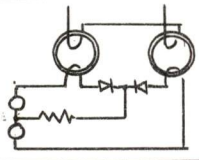
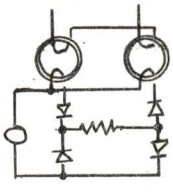
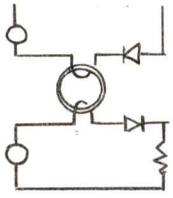
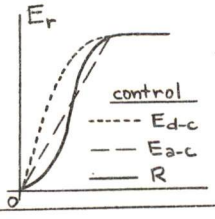
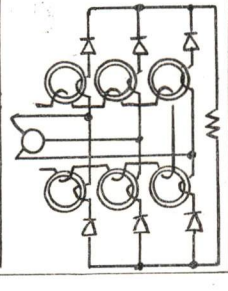
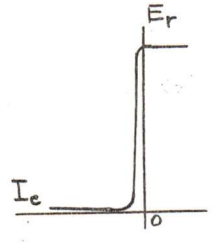
| TYPE | CIRCUIT | CONTROL CHARACTERISTIC | COMMENTS |
|---|---|---|---|
| Half-Wave SR |  | | very low power gain |
| Single-Phase Full-Wave SR | | | linear control characteristic, moderate power gain, high output impedance |
| Parallel |  |   | no induced voltage in control circuit, poor transient response |
| Series |  | | better transient response, large second harmonic induced in control circuit |
| Three-Phase SR |  | | used for large loads |
| Saturable Transformer |  |   | used with high impedance power source, permits load matching |
| Shunt-Connected SR |  | | used with high impedance power source, has higher efficiency than saturable transformer |

TABLE B: Circuits Containing Rectifiers

| TYPE | CIRCUIT | CONTROL CHARACTERISTIC | COMMENTS |
|---|---|---|---|
| SR with Feedback |  |   | improved dynamic gain, less linear characteristics, a-c or d-c output |
| Single-Phase, Self-Saturating Magnetic Amplifier | | | higher dynamic gain, simple circuitry, low output impedance |
| Half-wave |  |   | high impedance control required |
| A-C |  | | used for a-c load |
| Center-tap |  | | for d-c load, center-tapped transformer required, inefficient use of transformer |
| Bridge |  | | uses twice as many rectifiers as a-c circuit, but inverse voltage is halved, more efficient use of transformer |
| A-C Flux Reset |  |   | high gain with one core, half-cycle response time |
| Three Phase D-C Bridge Self-Saturating Magnetic Amplifier |  |   | lower ripple, faster response, used for large d-c loads |

K. Olsen
B-063



Division 6 – Lincoln Laboratory
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SUBJECT: A Transistorized Sensing Amplifier for the 256 X 256 Core Memory

To: W. N. Papian

From: S. Bradspies

Date: November 16, 1956

Approved: R. L. Best
R. L. Best

Abstract: A transistorized sensing amplifier, suitable for use in conjunction with a 256 X 256 magnetic core memory plane has been designed. This plane will be equipped with four sensing windings, each of which feeds an independent amplifier input. The circuit rectifies the bi-polarity pulses, and mixes the four inputs so that there is only one output per plane. The output is a negative 10 ma pulse that feeds a 160 Ω cable.

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## I Introduction:

Ever since the introduction of magnetic core memory devices to the digital computers at M.I.T. - Whirlwind I and MTC - the problem of supplying the information held by this memory to the computer has not been solved to everyone's satisfaction. [1, 2, 3, 4, 5]

It has been found impossible to ground either end of the sensing winding because of the presence of common mode signals.[3] This has led to the necessity for using a difference amplifier input.

The memory plane may display a variety of undesirable output pulses (Fig.1) in addition to the signal it is supposed to amplify. These signals may be listed:

a. ONE -- is the signal that is to be amplified and fed to the computer. It is nominally 50 millivolts high and 1 microsecond wide in the 256 X 256 memory.

b. ZERO -- is a signal that should not be present in the output. The absense of an output from the sense amplifier at the time of interrogation is taken to be ZERO. When a single core holding a ZERO is selected, its output is very small. However, in an n x n memory plane, there are 2 (n-1) partially selected cores and the noises produced by these cores may combine with the output of the selected core to produce a substantial output pulse. It is necessary that the sense amplifier be able to distinguish between the ONE and ZERO outputs, either in time or amplitude.

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1. Laspina, C.A. "Basic Circuits - Sensing Amplifiers", M.I.T. Digital Computer Laboratory Memorandum, M - 1969, 10 April, 1953.

2. Laspina, C.A. "Basic Circuits - Sensing Amplifier, Preliminary Specifications, PB#20", M.I.T. Digital Computer Laboratory Memorandum, M-2274, 3 July, 1953.

3. Sarles, F.W.Jr. "A Transistorized Amplifier - Discriminator for Core Memory Output Sensing", S.M.Thesis Proposal, M.I.T. Lincoln Laboratory Memorandum 6M-3417, 7 March 1955.

4. Sarles, F.W.Jr. "A Transistorized Amplifier-Discriminator for Core Memory Output Sensing", S.M.Thesis, M.I.T. Department of Electrical Engineering, May 1955.

5. Zopatti, R.C. Private Communications

c. Inhibit Noise -- is caused when the digit plane winding is pulsed during the writing of a ZERO. When the inhibit current is applied, every core in the plane is partially selected. It has been found that in the worst case, for a 64 X 64 plane, that the signal is about 1 volt in amplitude. The amplifier must not be so disturbed by this large pulse that it is unable to respond correctly to a signal that is applied about 1.0 microsecond following the completion of the inhibit.

d. Common Mode Signals -- are probably caused by capacitive coupling between the drive lines and the sensing winding. It is expected that these signals (which raise both ends of the sense winding together) may be as large as 10 volts per 64 X 64 plane. These common signals must be totally rejected.

In connection with items c and d above, reference was made to disturbances caused by a single 64 X 64 plane ( or module). If the 256 X 256 plane was treated as a unit (with one sensing winding and one digit plane winding), then the noise pulses would be greatly increased. Fig. 2a demonstrates that during the read operation $2(n-1) = 2(256-1) = 510$ cores receive half select excitations. In a 64 X 64 plane, only $2(64-1) = 126$ cores are disturbed during read. It is seen, then, that if a single sense winding is used for the large plane, the noise is increased by a factor of 4.05. It is essential, therefore, that the sense winding be split so that a minimum of noise due to partial selects is found on any one sensing winding. If the winding is distributed as shown in Fig.2b (no sense winding passes through any two modules that are on the same vertical or horizontal line), this condition will be met, and a maximum of 128 partially selected cores will be sensed by any one sense winding. Furthermore, due to the fact that the sensing winding acts as a delay line, shortening the length of it, cuts the delay, and restricts the time interval during which an information pulse may arrive.

Experiments have demonstrated that it is not possible to use a single digit plane winding per plane. There are to be four of these windings per plane, and they will be connected as shown in Fig.2c. The memory will be operated in a manner that excites only the required digit winding when a ZERO is to be written. The other three digit drivers will be held off. The primary reason for this is to cut the ringing on the X and Y driving lines, and on the sensing windings due to capacitive coupling between these leads and the inhibit leads. This permits a large reduction in the memory cycle time (to less than 6 μsec). Of course, this operation aids the sensing amplifier because of the reduction in the sizes of the inhibit pulses to those seen by 64 X 64 planes.

It is found that a memory plane can put out a long chain of unipolarity pulses, followed immediately by pulses of the opposite

polarity. It is essential that the amplifier not be so prf sensitive that these kinds of pulse sequences cause a misreading of information.

## II Preliminary Considerations

One of the major requirements of the sensing amplifier is speed. It must be able to respond quickly and to recover quickly. These conditions lead to the necessity for using fast transistors, and Philco Surface Barriers (SBT's) -- which are used throughout the TX-0 computer-- are the best commercially available transistors in this respect.

If the amplifier is to perform satisfactorily, it is necessary that it be capable of recovery from the peculiar signals (mentioned above) that may be applied to it. Consequently, the sensing amplifier has about 1 microsecond in which to recover from a four volt inhibit pulse, and it must not be allowed to give false outputs when it is excited by a string of unipolarity pulses. Actually, a direct coupled amplifier would be ideal for this particular application. But this is not possible in the present application for reasons to be discussed below.

In order to permit the difference amplifier to operate most satisfactorily, it is necessary to have the circuit impedances adjusted in an attempt to block common signals and to aid difference signals. These ideals can be realized by use of either choke or transformer coupling, if the coil polarities are as shown in Fig. 3.

The circuit pictured in Fig. 3a works well in all respects save one. It fails to effectively eliminatethe common mode signal. On the other hand, the circuit pictured in Fig. 3b behaves as well as that which is choke coupled, and it also eliminates common mode signals to a large extent.

For the best results the choke, or transformer, should be wound as shown in Fig. 4. If the choke is used, windings c and d are eliminated. In order to achieve the proper coil polarities, leads 2 and 3 are connected to form the center tap of the primary. If the coupling element is a transformer, leads 6 and 7 are also joined to form the secondary center tap.

The two circuits of Fig. 3 may be analyzed, approximately, by drawing the simplified linearized equivalent circuits. These are shown in Fig. 5. In these equivalent circuits the following assumptions are made:

1.) Both halves of circuits are identically balanced;

2.) Grounded base current gain of each transistor is $\alpha$;

3.) Base resistance is $r_b$;

4.) Emitter resistance is $r_e$;

5.) Collector resistance is infinite;

6.) $Z_5$ is a non-linear impedance such as a diode -- low in one direction and high in the other direction;

7.) Mutual coupling between primary windingsis $M_1$;

8.) Mutual coupling between secondary windings is $M_2$;

9.) Mutual coupling between any primary winding and any secondary winding is $M_{12}$;

10.) Sensing winding impedence is negligible.

Fig. 5a shows the equivalent circuit for the choke coupled case when a common mode signal $V_{cm}$, is applied. The output voltage is

$$V_{out\,cm} = -\frac{2\alpha V_{cm} Z_6 R_d (L_1 - M_1)s}{\left[R_d + Z_5 + 2Z_6\right]\left[R_p + (L_1 - M_1)s\right]\left[R_3 + r_e + r_b(1-\alpha)\right]}$$

$$\cong -\frac{2\alpha V_{cm} Z_6 R_d (L_1 - M_1)s}{R_3\left[R_d + Z_5 + 2Z_6\right]\left[R_p + (L_1 - M_1)s\right]} \qquad (1)$$

in which

$$R_p = \frac{R_d(Z_5 + 2Z_6)}{R_d + Z_5 + 2Z_6}.$$

It is observed that the only way in which the common mode signal can be eliminated is to have $M_1 = L_1$. In actual practice this is not possible, and so one must be content to allow some common mode to pass. Some help is achieved by allowing $R_3$ to be very large. However, there is a limit to this, for the supply voltage must be increased proportionally.

Fig. 5b shows the equivalent circuit that is presented to a difference signal. It is assumed that the capacitor across the resistors $R_3$ effectively shorts the emitters together.

It is found that

$$V_{out\,s} = -\frac{\alpha V_s R_d Z_6\left[R_d + (L_1 - M_1)s\right]\left[L_1 + M_1\right]s}{2\left[r_e + r_b(1-\alpha)\right]\left[R_d + Z_5 + Z_6\right]\left[(R_L + L_1 s)(R_d + L_1 s) - (M_1 s)^2\right]} \qquad (2)$$

in which

$$R_L = \frac{R_d(Z_5 + Z_6)}{R_d + Z_5 + Z_6}.$$

The gain in this circuit is greater for the difference signal than it is for the common signal, but one cannot assume that the common signal is negligible.

Fig. 5c shows the equivalent circuit for a common mode signal in a transformer coupled circuit. The output is found to be

$$V_{out\,cm} = 0. \tag{3}$$

This is due to the fact that the net current in the primaries of the transformer is zero, and there can be no signal coupled through to the secondary. In actual practice, however, it is found that some signal may be transmitted by capacitive coupling between the leads of the primaries and secondaries. In order to minimize this capacity, the primaries and secondaries are isolated from each other to as great an extent as possible, as shown in Fig. 4. Another manner in which common mode may get through is if the circuit elements are not balanced. One percent resistors are used in attempt to minimize this. However, no attempt will be made to balance the transistors. It has been found that even with badly unbalanced transistors, common mode signals are not passed by the amplifier.

Fig. 5d shows the equivalent circuit when a difference signal is applied to the transformer coupled circuit. The output is

$$V_{out_s} = -\frac{\alpha V_s R_d Z_b M_{12} S}{\left[r_e + r_b(1-\alpha)\right]\left[L_2 S + Z_b + Z_d\right)(R_d + L_1 S + M_1 S) - 2(M_{12} S)^2\right]}. \tag{4}$$

These results show the vast superiority of the system that uses a transformer rather than a choke as a coupling element. The output signal is somewhat smaller in the latter case than it was before, but this drawback is of little consequence when the advantage gained by the loss of common mode signal is considered.

One problem that must be solved in connection with the transformer is whether to use a long time constant or a short time constant. In the following discussion, it will be assumed that inhibit pulses always come in pairs, one negative and one positive. In the case of a long time constant circuit, the effect of these inhibit pulses will not be bothersome (only insofar as the a.c. coupling is concerned). If a short time constant is used, the inhibits will cause trouble.

In order to understand how various time constants affect recovery, a simplified analysis shows how an inductor shunted by resistance reacts to a square current pulse. Fig. 6 shows the output voltage for three different time constants. It is to be noted that the shorter the time constant is made, the larger the negative overshoot is, but the more rapid is the recovery. However, it is apparent that when the long time constant is used, the circuit is immediately ready to respond almost fully to another positive current pulse. For shorter

time constants, some time must be allowed to elapse before a full output will be obtained.

It is now possible to discuss the various chains of memory outputs that might possibly occur, and to determine how the output is affected by various time constants. In fig. 1, it is observed that the length of time between two successive reads is six microseconds, and that the time between the end of the second inhibit and the beginning of the next read is from 0.5 to 1.0 microseconds.

From Fig. 7 (in which the non-linear operation of the input difference stage is shown), it is noted that due to the fact that pulses are considerably widened by a short time constant circuit, (Fig.7b), it may be difficult to distinguish between a ONE and a ZERO, if the information pulse closely follows an inhibit pulse because the information pulses ride on the overshoot of the inhibit pulse.

If a long time constant circuit is used, (Fig.7c), the overshoots are very small, but the circuit must wait a long time in order to completely recover. The pulses are not deformed, but after a long series of unipolarity pulses, the base line shifts in order that the net area may be zero. The inhibits do not cause any additional trouble, because the net area of a pair of bipolarity inhibit pulses is zero. The base line shift is caused solely by the unipolarity ONEs. The ONEs are present only for 1 microsecond out of a period of 6 microseconds, and so the base line will move not more than 16.6% the height of a ONE. The problem caused by this difficulty can be discussed fairly simply. Assume that a long burst of positive ONEs (the finish of which is shown in Fig.7), have been supplied by the memory. Assume the worst possible case occurs, and that each ONE occupies one microsecond out of the six microsecond cycle time. If all the ONEs were 50 millivolt pulses, the base line at the transformer will have decayed to -8.3 millivolts. The result is that any positive ONE will have a net effective input amplitude of 50-8.3 = 41.7 millivolts. Any negative ZERO, of 10 millivolts amplitude (for example), will display a net effective input amplitude of 10+8.3=18.3 millivolts. Thus, the ratio of signal to noise has decayed from

$$\frac{50}{10} = 5.0, \text{ to } \frac{41.7}{18.3} = 2.3.$$

The remainder of the circuit can be designed so as to compensate for this annoyance.

Nothing can be done to rectify the damage caused by a short time constant.

In the actual circuit, a compromise solution was reached and an intermediate time constant was used.

## III The Circuit

The complete circuit diagram is shown in Fig. 8. Although the input stage was discussed in some detail in the previous section, there are several additional remarks that may be made concerning it.

In the input difference stage, large resistors and large power supplies are used in series with the transistors. The result is that slight differences in transistor characteristics do not noticeably alter the quiescent conditions in the circuit. If it is assumed that the two transistors used in the difference stage are identical, then the quiescent circuit may be represented as in Fig. 9.

The equations that describe this system are:

$$300 = I_e(.216+68) + V_{ec} + (I_1+I_e)(33+.216), \text{ and}$$

$$150 = .160\,I_1 + 1.3(I_1+I_b) + (I_1+I_e)(33+.216).$$

These equations may be rewritten as follows:

$$300 + V_{ce} = 101.4\,I_e + 33.2\,I_1 \qquad (5)$$

$$150 - 1.3I_b = 33.2\,I_e + 34.7\,I_1 . \qquad (6)$$

It is reasonable to assume that $V_{ce}$ and $1.3I_b$ are much smaller than 300 and 150 respectively, and they may be neglected. It is then found that $I_e = 2.26$ ma and $I_1 = 2.18$ ma. The collector to base voltage in the quiescent state is $-1.3\,(I_1+I_b)$ volts. Therefore, this voltage is just about -3 volts, and to a very great extent is independent of the transistor that is used. The only contribution that a transistor makes to its own collector-to-base voltage is its base current through a 1.3k resistor with its emitter current at 2.26 ma. Even if $\alpha$ of the transistor is as low as 0.9, the base current is only about 0.2ma, and this is small compared to $I_1$.

Fig. 10, then, shows the quiescent operating point of either of the two input transistors. The collector-to-base voltage is about -3 volts and the emitter current is about 2.26 ma. A variation in transistor characteristics will only result in a change in the base current, and this results in only a slight variation of collector-to-base voltage. Fig. 10 shows that in the neighborhood of the operating point, the transistor characteristics do not vary when the collector voltage is altered.

If the input transistors are identical, and are operated linearly, it is found that the output current is

$$i_{out} = -\frac{V_s\, z_m\,(\alpha r_c - z_e)}{[r_b(r_c - \alpha r_e + z_e + z_L) + z_e(r_c + z_L)][z_{sw} + z_m]} \qquad (7)$$

where Vs is the input difference signal; $\frac{1}{Z_{11}} = \frac{1}{2}\left(\frac{1}{R_1} + \frac{1}{R_4} + \frac{1}{Z_{in}}\right)$

(refer to Figs. 3b and 5d) and

$$Z_{in} = r_b + \frac{Z_e(r_e + Z_L)}{r_e(1-\alpha) + Z_e + Z_L} \quad ;$$

Ze is the impedance in the emitter of one transistor; $Z_{SW}$ is the impedance of the sense winding; and $Z_L$ is the equivalent load that a transistor sees. In order to achieve a maximum output, it is noted from equation (7) that minimizing $Z_e$ will be of great benefit. Thus a large capacitor is used to shunt the two 68k resistors that feed the emitters. Because of the need for large capacity and extremely small physical size, it was necessary to use subminiature aluminum electrolytic capacitors. In order to insure uniform operation for positive and negative pulses, it was necessary to use two 5μf capacitors in series, back to back. When the signal is applied, the capacitor is essentially a short circuit, and $Z_e$ reduces to $r_e$. During the quiescent operation the two emitters are isolated from each other, and the current drawn by one does not affect the other.

The impedance that the capacitors face is about

$$2\left[r_e + (1.3 + r_b)(1-\alpha)\right] \qquad \text{kilohms.}$$

It has been found for SBT's that at 2.26 ma of emitter current $r_e \cong 11.5\ \Omega$ and that $r_b \cong 350\ \Omega$. If transistors with $\alpha = 0.95$ are used, then the capacitors see an impedance of about 188 ohms. The time constant then is about 470 microseconds, and this is relatively long. Even if the transistors have α's as high as 0.99, the time constant is 140 μsec, and this is still quite long.

The output impedance of a common emitter transistor stage is about 10 kilohms. So far as a difference signal is concerned, there are 2 of these transistors in series, and they are shunted by the two damping resistors in series. Therefore, the output impedance is

$$\frac{(2\times 10)\times(2\times 6.8)}{(2\times 10)+(2\times 6.8)} = 8.1\ \text{k}\Omega$$

The impedance seen past the secondary is either infinite (when the emitter followers are off); or $(\beta_{EF}+1)$ $Z_{in}$ Q104 (where $\beta_{EF}=\beta$ for the on emitter follower) when one of the emitter followers is on, and the following stage, Q104 is still on; or $(\beta_{EF}+1)82\text{k}\Omega$, when one of the emitter followers conducts and Q104 is off. The first and last regions (those of very high impedance) last for a long time. The middle region, during which the transformer sees the relatively low impedance

$$(\beta_{EF}+1)\, Z_{in\,Q104} = (\beta_{EF}+1)\left(r_e + r_b(1-\alpha)\right)\Big|_{Q104}$$

lasts only for a very short period of time. Hence, for the major portion of the cycle, the impedance seen by the secondary is very much greater than the output impedance and may be neglected.

Fig. 11 shows a 60 cycle hysteresis loop for the transformer core. This core is manufactured by Arnold Engineering Co., and is a plastic encased, permalloy core, number 5340-S1. The loops shown are a minor loop on which the core operates, and the saturation loop. This data was taken with a single turn on the core.

It was found that no more than about 0.35 ma flowed through the primary of the transformer in the actual circuit when a difference signal was applied (whether the signal was 100 mv or 1.0 volts). Since there are 60 turns, the exciting force is 21 ma-turns. I have, therefore, assumed that the minor loop on which the core operates has a maximum excitation of about 21 ma-turns. The corresponding peak flux was 33.3 Maxwells. Because of the fact that the remanent flux is 30% of the maximum flux, the linearized inductance of the coil with a single turn is

$$L = \frac{1.3\,\Phi_m}{I} \times 10^{-8} = \frac{1.3 \times 33.3 \times 10^{-8}}{21 \times 10^{-3}} = 20.6\,\mu h.$$

When 60 turns are used, as in the sense amplifier, the inductance is

$$(60)^2 (20.6)\,\mu h = 74\,mh.$$

The transformer time constant is $\frac{L}{R} = \frac{74}{8.1}\,\mu sec = 9.2\,\mu sec$. This time is considerably shorter than that of the capacitor circuit, and so the transformer time constant controls the circuit behavior. Apparently from the tests that have been run on this circuit thus far, the time constant is long enough to assure satisfactory performance.

A decrease in the number of turns on the transformer would result in several disadvantages. The signals coupled through to the remainder of the amplifier would be decreased, due to the lessening of the magnetizing inductance. Furthermore, the time constant would be decreased, and this is highly undesirable.

An increase in the number of turns apparently does not aid the circuit operation materially. This may be because of the corresponding increase in wiring capacity shunting the primary and the secondary.

The operation of the remainder of the circuit is fairly straight-forward. The eight emitter followers, (Q3 and Q4), whose bases are connected to the transformers (Fig. 8) are biased slightly off. An applied difference signal on one of the four sensing windings results in the application of a pulse to one of the transformers. The base of one of its two transistors rises, and it is further cut-off. However, the other transistor has its base lowered, and if the signal is large enough, this transistor is turned on. The bias level can be adjusted by varying the 50k pot. All eight emitters fall with the one that has been switched. It is seen, therefore, that the memory output that controls the sense amplifier behavior is the largest output, and consequently a ONE will control the sense amplifier even if it is mixed with low level noise.

In this one section of the circuit, the operations of rectification, mixing and slicing have been accomplished. It is found that the sense amplifier output completely switches when the memory plane output varies by 1.1 millivolts. Below this level, there is no output; above it, a full 10 ma pulse.

The transistor Q104 is normally on. When one of the emitter followers is switched on, Q104 goes off. Its collector falls towards -30, turning Q103, which is normally held off, to the saturated state. Its collector rises, turning Q102 and Q100 off. Q102 then saturates Q101. With Q100 off, and Q101 saturated, the circuit output drops to -3 volts.

When the pulse at the input has ended, the cycle is reversed -- Q104 again goes on turning Q103 off. Q102 and Q100 are saturated; Q101 is shut off, and the output rises to ground potential.

Inhibit pulses turn out no larger than ONEs because of the fact that signals are limited by saturation and cutoff.

The resistors in this section of the circuit are chosen so that with minimum acceptable transistors and maximum allowable variation in the undesirable direction of resistance values, the circuit continues to operate satisfactorily.

The operation of the cable driver (consisting of transistors Q100 and Q101) deserves some comment. The cable driver consists of these two transistors connected in series, and the output is taken from the junction of the emitter of Q101 and the collector of Q100. Under standby conditions Q100 is saturated and Q101 is off. The output impedance is very low, and the output level is at ground potential. A pulse at the input to the sense amplifier turns Q100 off, but saturates Q101. (The circuit parameters are adjusted so that when an intermediate sized signal is applied, both Q100 and Q101 are off. If this were not done, it would be possible to saturate both transistors simultaneously, and this would result in the destruction of at least one of the transistors.) Consequently, the output drops to -3 volts, and the output impedance remains at a very low level.

The load that is to be driven is about 50 feet of 160-ohm cable. Because it is not feasible to terminate the cable at the far end, it is necessary to do so at the driving end. Therefore, a 130 ohm resistor is placed in series with the load and the output impedance is probably very close to 160 ohms. The figure of 130 ohms was determined by trying various values of terminations, and choosing that which gave the most satisfactory results.

## IV Results

There is, in this circuit, one result that is both theoretically and actually somewhat disturbing. This is the fact that if the different sensing amplifier input channels (of which there are four per memory plane) are not matched, then their gain characteristics will not be identical. There is only one variable element per sense amplifier - the clipping level potentiometer, R118 (Fig.8), and this cannot possibly be adjusted to satisfy all channels. Suppose the gain of channel A is greater than the gain of channel B, and R118 is set to just pass a 30 millivolt signal applied to channel A. It may then be found that perhaps a 35 mv signal in channel B will be blocked, because it is not amplified as strongly as a signal in A.

In the circuit, this is found to be the case, but it is possible to correct this mistake to a large extent.

In an effort to limit the differences between the various stages, 1% resistors are used exclusively in all channels. With this restriction in force, it is found that the gain of a channel depends upon the characteristics of the transistors and of the transformer used. If a detailed examination was made, it would probably be discovered that the results also depend on the individual resistors in the circuit.

In almost every case of excessive unbalance detected so far, it has been possible to satisfactorily equalize channels by juggling transformers - that is, place strong transformers in weak channels, and vice versa.

The variation of results as the transistors of an input stage are varied, is clearly shown in the following tables of data. In each case the negative voltage signal at the secondary of the transformers is measured for a 50 mv difference input signal. By connecting all four channels in parallel at their inputs, it is ascertained that the same voltage signal is applied to each. Three runs were taken. Sensing amplifier number 9 was used. The results are shown in Table 1.

TABLE 1.

| | Channel | Transistors | α | Negative Output (volts) at transformer Secondary for 50 mv. Input |
|---|---|---|---|---|
| Run 1 | 1 | A108 | 0.962 | 1.28 |
| | | A109 | .950 | |
| | 2 | A81 | .972 | 1.08 |
| | | A75 | .972 | |
| | 3 | A74 | .969 | 1.30 |
| | | A107 | .968 | |
| | 4 | A73 | .956 | 1.35 |
| | | A82 | .962 | |
| Run 2 | 1 | A108 | .962 | 1.35 |
| | | A109 | .950 | |
| | 2 | A81 | .972 | 1.10 |
| | | A75 | .972 | |
| | 3 | 3863 | .919 | 1.25 |
| | | 3866 | .918 | |
| | 4 | 9209 | .979 | 1.30 |
| | | 9215 | .978 | |
| Run 3 | 1 | A81 | .972 | 1.19 |
| | | A75 | .972 | |
| | 2 | A108 | .962 | 1.22 |
| | | A109 | .950 | |
| | 3 | 3863 | .919 | 1.25 |
| | | 3886 | .918 | |
| | 4 | 9209 | .979 | 1.28 |
| | | 9215 | .978 | |

These three runs should not be compared to each other numerically because of the fact that the data were not taken under the same conditions (e.g. the "50 mv" input in run 1 may not have been the same size as the "50 mv" input in run 3). But it is valid, and very interesting, to compare the magnitude obtained within the various runs.

Run 1 demonstrates the fact that the gain of a channel does not vary linearly with the transistor α's. For instance, channel 2

has the strongest transistors, and yet it is the weakest channel; but channel 4, the strongest, has a pair of intermediate gain transistors. It is also noted that channels 1, 3 and 4 are about equivalent.

Run 2 differs from the first run in that channel 3 now has very low $\alpha$ transistors and channel 4 has very high $\alpha$ transistors. It is noted that 3 is weakened just a bit relative to 4. But the really interesting fact is that 4 is weakened relative to 1. This tends to indicate that channel 4 has been significantly weakened when its transistors were replaced by supposedly better transistors. Channel 2 is still the weakest by a good margin.

Run 3 is the same as the second run, except that the transistors in channels 1 and 2 have been interchanged. The result is that the gain of channel 1 has fallen below that of channel 2. This virtually assures us that although transistors A75 and A81 have very high $\alpha$'s, they are poorer than A108 and A109. It also proves that the gain of a channel depends to a large extent upon all of the characteristics of the transistors used, and not merely $\alpha$, as shown in equation (4). That is,

$$V_{out} = -Z \frac{\alpha V_s}{r_e + r_b(1-\alpha)} \qquad (8)$$

It is apparent, therefore that not only $\alpha$, but $r_e$ and $r_b$ are very important parameters in determining the voltage gain of a common emitter transistor amplifier.

Fig. 12 shows the negative pulses at the transformer secondaries corresponding to the conditions of Run 1. This demonstrates that channels 1, 3 and 4 are about equal, while channel 2 is relatively weak.

In passing, it should be pointed out that the pulse size at these points is completely independent of the setting of the clipping level potentiometer. In Fig. 13, the effect of the different gains upon the output pulse is shown. It is observed that the pulse widths at the base of the outputsare as follows:

| | |
|---|---|
| Channel 1 | 0.95μsec |
| Channel 2 | 0.90μsec |
| Channel 3 | 0.99μsec |
| Channel 4 | 0.96μsec |

Run 1 yielded the most widely divergent results, and the complete data from this run is plotted in Fig. 14. From the slopes of these linear curves (they are linear because the signals are not large enough to drive the transistors into non-linear operation), it is observed that the difference in gains between the extreme cases is about 20%.

When the results shown in Fig. 12, 13, and 14 are observed, it is realized that great differences in channel gains do not yield very widely diverging results at the outputs.

It has been found for this circuit that the bias at the emitters of the emitter followers is several hundred millivolts positive. It is observed to a very close approximation, that when the d.c. level of the base voltage drops to ground potential, the corresponding transistor will begin to conduct. Consequently, by use of Fig. 14, it is possible to set the clipping level to any predetermined input level by adjusting R118 to give the proper voltage at the bases of the emitter followers. Because of the different gains achieved in different channels, it will be necessary to accept a compromise solution, however. For instance, assume that it is desired to set the clipping level at 30 mv. Fig.14 shows that, on the average a negative 750 mv pulse is obtained at the transformer secondary when a difference signal of 30 mv is applied at the input. Therefore, the bias point should be adjusted to +750mv. It will then be found that channel 2 will clip at 34 mv, and that channel 4 will clip at 28 mv.

An examination of the transfer characteristics of the complete sensing amplifier (from difference input signal to the output across a 160Ω terminating resistor) leads to the data tabulated below for a nominal clipping level of 30 mv.

This data is for channel 3 of sensing amplifier number 9. The input transistors are A74 and A107.

TABLE 2

| Difference Input Signal mv | Output Voltage Volts | Output Pulse Width μsec | Negative Signal at Transformer Secondary Volts |
|---|---|---|---|
| 100 | 1.55 | 0.95 | -- |
| 90 | 1.55 | 0.92 | -- |
| 80 | 1.55 | 0.86 | -- |
| 70 | 1.55 | 0.82 | -- |
| 60 | 1.55 | 0.77 | -- |
| 50 | 1.55 | 0.67 | -- |
| 40 | 1.55 | 0.50 | -- |
| 30+ | 1.55 | 0.18 | 0.89 |
| 30- | 0 | 0 | 0.86 |
| 20 | 0 | 0 | -- |
| 10 | 0 | 0 | -- |
| 0 | 0 | 0 | -- |

Channel 3 is about the same as channel 4 (Fig.12 and 13) and so the gain from input to transformer secondary is about 27. Thus, in the

active region (around 30 mv of input), the gain of the complete amplifier

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta V_{transformer\ secondary}}{\Delta V_{in}} \times \frac{\Delta V_{out}}{\Delta V_{trans\ sec}} = 27 \times \frac{1.55}{.03} = 1400.$$

That is, in the active region, the amplifier voltage gain is about 1400. Thus, in order to switch the amplifier from no output to full 1.55 volt output, a change of about 1.1 millivolts at the input is required.

These data are plotted in Fig.15. It is noted, that although the pulse height experiences a very sharp cutoff, the output pulse width depends upon the input signal to a very large extent. (The width of the input pulse remains fixed at about 1.0μsec). The reason for this is obvious: as the pulse height is reduced, clipping occurs at higher, and narrower points on the input waveform.

Figures 16 show the pulses obtained at various places in the sensing amplifier when a 50 mv ONE is applied to the input, and Figures 17 show the pulses at the same points when a 20 mv ZERO is applied. It should be noted that in each of these cases, the cycle time is about 4.5 μsec (the length of time between the beginning of the first ONE, and the beginning of the second ONE).

At the input (Fig.16A and B), the ONEs are about 50 mv high and the inhibit pulses are about 800 mv. However, due to the non-linear characteristic of the difference stage, the ONE is amplified more strongly than the inhibit pulse, and the difference signal at the transformer primary consists of 2-volt ONEs, and 6-volt inhibits (Fig.16C). The transformer is a 2 to 1 step down, and consequently the signals at either side of the transformer secondary are about 1 volt and 3 volts, respectively (Fig.16D). (It should be noted that the negative inhibit pulse cannot go far below ground because of the clamping action of the forward biased emitter follower transistor. This accounts for the peculiar shape of the large negative pulse.)

At the emitter follower output (Fig.16E), all pulses are negative. Some portion of the signal at the transformer is lost because the emitter followers are biased off. Hence the ratio of inhibit pulse to ONE signal has been increased. But, as is shown in Fig. 17E, this operation allows for the discrimination against ZEROs.

It is noted that all outputs of Q104 (Fig.16F) - ONEs and inhibits alike - are now the same size. This is caused by the fact that Q104 is turned off even by the small ONE pulse. The notches that are found in this waveform at a level of about $+0.22 - 0.3 \cong -0.1$ volts are caused by the saturation of Q103, the following stage. The output of Q104 is clamped at about -0.4 volts by the conducting base-to-emitter diode of Q103. It is possible for the base to go more negative than the emitter because it is connected directly to the -30 volt supply.

The output of Q103 (Fig.16G) is basically the same as the output of Q104, except that it is greatly amplified, and it is inverted. The pulses are clamped at about ground because when Q103 is saturated its collector-to-emitter voltage is very low, the input to Q102 (Fig.16H) is slightly peaked at its front edge, because the coupling capacitor, C107, is somewhat too large. At any rate, these pulses are large enough to shut Q102 off.

The input to Q100 (Fig.16I) has a slow rise, because its coupling capacitor, C101 is too small. Although this rise time can be greatly improved by adding 100μμf to C101, the affect on the output is unnoticeable. The reason is that Q100 is turned off long before the slow rise takes effect.

The output of Q102 (Fig.16J) (which is fed directly to Q101) is a negative-going square wave that turns Q101 full on. The pulse is able to sink lower than -3 volts because the emitter of Q101 falls to -3 volts, and the base is a little negative relative to the emitter.

The sensing amplifier output (Fig.16K)shows the typical well-defined negative-going 1.55 volt, 10ma pulses that are approximately the same shape for all input pulses that exceed the switching threshold.

Figures 17 show the results obtained when a signal that is below the cutoff level is applied. It is noted that the inhibits appear at the output just as they did in the previous case, but that the information signals are blocked.

Fig.18 demonstrates that the sensing amplifier delay is about 0.3 μsec as measured from the peak of the input pulse to the center point of the output pulse. This result is true, no matter where the clipping level is set, and it is independent of the input pulse amplitude of course.

Fig.19 traces chains of some 1430 unipolarity pulses through the amplifier. These pulses are spaced 6 μsec apart. The points of observation are the same as those used for Figs.16 and 17. It should be noted that the only spot at which there is any prf sensitivity is at the input to the amplifier. The pulse generator is prf sensitive; the sense amplifier obviously is not sensitive at any spot. Fig.19K demonstrates the almost negligible voltage buildup across the emitter-coupling capacitors of the difference stage.

The fact that no common mode signal should appear at the output was discussed earlier in this note. Fig.20 shows the results obtained when a large common signal is applied to the amplifier. With no load, the signal was ±65 volts; the sensing amplifier cut this signal to ±30 volts. There is no output from the amplifier due to either the positive or negative going common signal. The disturbances that are seen at this output (Fig.20B, 20D) are caused by pick-up due to radiation; it is not an output that feeds through the amplifier in the

normal manner. This is proven by the fact that the output obtained for positive and negative common signals are obviously merely the negatives of each other, and that the output amplitude varies directly with the input amplitude. It was found that even if the input transistors were very badly mis-matched, the results are the same. Thus, it would seem as though this amplifier is capable of eliminating common mode signals to a very large extent.

Some time ago D. H. Ellis took data concerning the successful operation of a 256 X 256 magnetic core memory plane as a function of strobe time and bias voltage of the sensing amplifier. This is plotted in Fig. 21. It is to be noted that area of safe and successful operation is the innermost enclosed area (shaded). A ONE fails when the bias is so large that the ONE signal is not passed by the amplifier. A ZERO fails when the bias is so low that the ZERO signal is passed by the amplifier.

A large amount of data has now been accumulated using 20 memory planes and 20 amplifiers. The results, so far as the amplifiers are concerned, have been very gratifying.

The graphs, Fig.22 through 25, show marginal checking data for the sensing amplifier when it drives a load of 50 feet of 160 ohm cable, terminated by 2.2 kilohms in parallel with 47 μμf. The shaded areas show the regions of safe operation. If the supply voltages stray beyond the boundaries shown, it may be expected that either: (1) ZEROs will be passed as ONEs because the amplifier is always in the "switched" condition; or (2) 40 mv ONEs will be blocked because they are not strong enough to switch the amplifier.

Fig.22 shows the plot of the voltage applied to resistor R111 as a function of the voltage applied to the resistors R105 and R107.

Fig.23 shows the variation of the voltage applied to R109 as a function of the voltage applied to R105, R107 and R111.

Fig.24 shows the variation of the voltage applied to R101 as a function of the voltage applied to R105, R107 and R111.

Fig.25 shows the variation of the voltage applied to R108 as a function of the voltage applied to R105, R107 and R111.

In each of these cases a variation of 30% in any voltage cannot possibly cause a failure.

In the actual circuit there are two +150 marginal check voltages. One is applied to R110 and the other to R104 (these resistors are merely decoupling resistors). The -30 volt marginal checking line is applied solely to R109. (See Fig.8) The resistor R104 is connected directly to resistors R105, R107 and R111. Hence, by varying the voltage to R104 and that to R109, a plot that is similar to Fig.23 is obtained.

The other marginal checking voltages (that applied to R110) can be used in two ways: (1) it can be lowered or raised in order to insure that all clipping level potentiometers (R118 and R138) are set to the same value; and (2) it can be used to vary the clipping levels of all amplifiers simultaneously in order to determine which amplifier or plane is weakest.

- - - - - - - - -

It is now intended that this circuit will be used as the sensing amplifier in the TDCM. Because this memory is only 64 X 64, it will only be necessary to employ one input channel. This will ease the restrictions on uniformity of components in the difference stage. There is no difficulty expected with this circuit. There are also several changes of components in the new circuit.

Sydney Bradspies

SB:rs

Sydney Bradspies

Drawings:

| | | | |
|---|---|---|---|
| Fig. 1 | A-68254 | Fig.14 | A-68508 |
| Fig. 2 | B-68255 | Fig.15 | A-68473 |
| Fig. 3 | B-68256 | Fig.16 | B-68402 |
| Fig. 4 | A-66352-1 | Fig.17 | B-68403 |
| Fig. 5 | C-68401 | Fig.18 | A-68262 |
| Fig. 6 | A-68531 | Fig.19 | B-68645 |
| Fig. 7 | B-68846 | Fig.20 | A-68593 |
| Fig. 8 | D-65501-1 | Fig.21 | A-68644 |
| Fig. 9 | A-68426 | Fig.22 | A-68717 |
| Fig.10 | A-68847 | Fig.23 | B-68719 |
| Fig.11 | A-68253 | Fig.24 | A-68718 |
| Fig.12 | B-68252 | Fig.25 | B-68720 |
| Fig.13 | A-68592 | | |

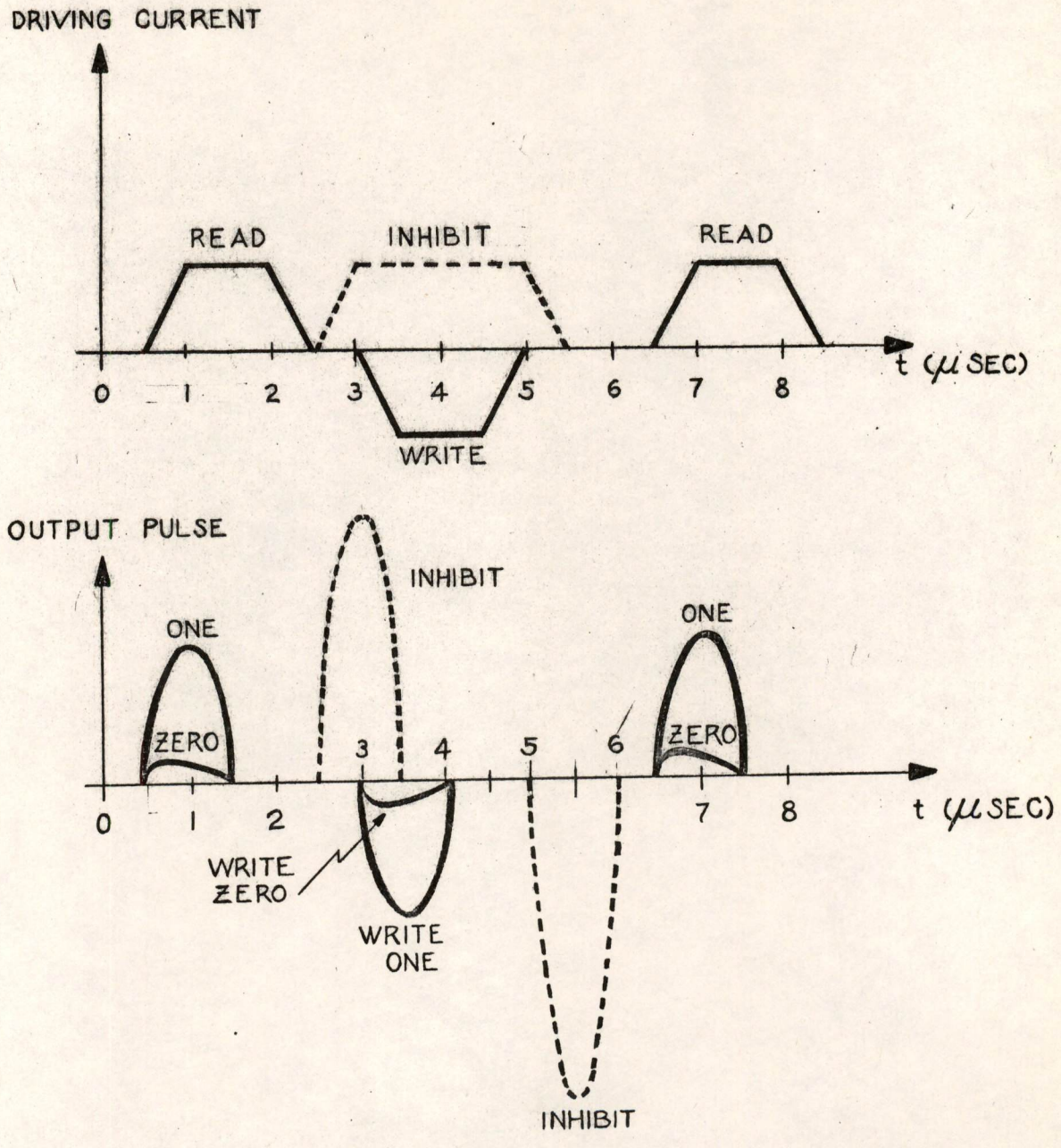
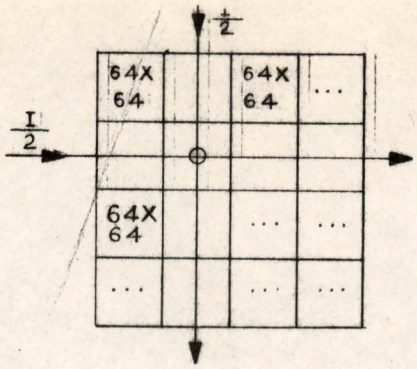


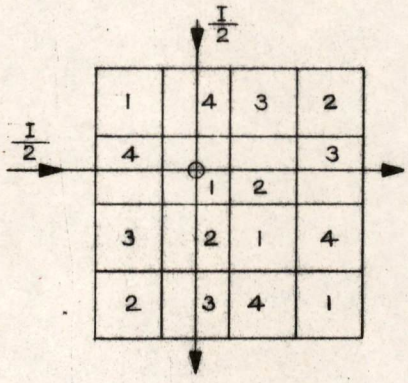

FIG. 1

DRIVING CURRENTS AND OUTPUT PULSES FOR MEMORY PLANES

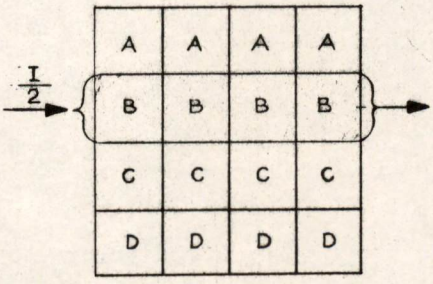
A-68254




a) PLANE CONNECTED WITH SINGLE SENSE WINDING AND SINGLE DIGIT WINDING



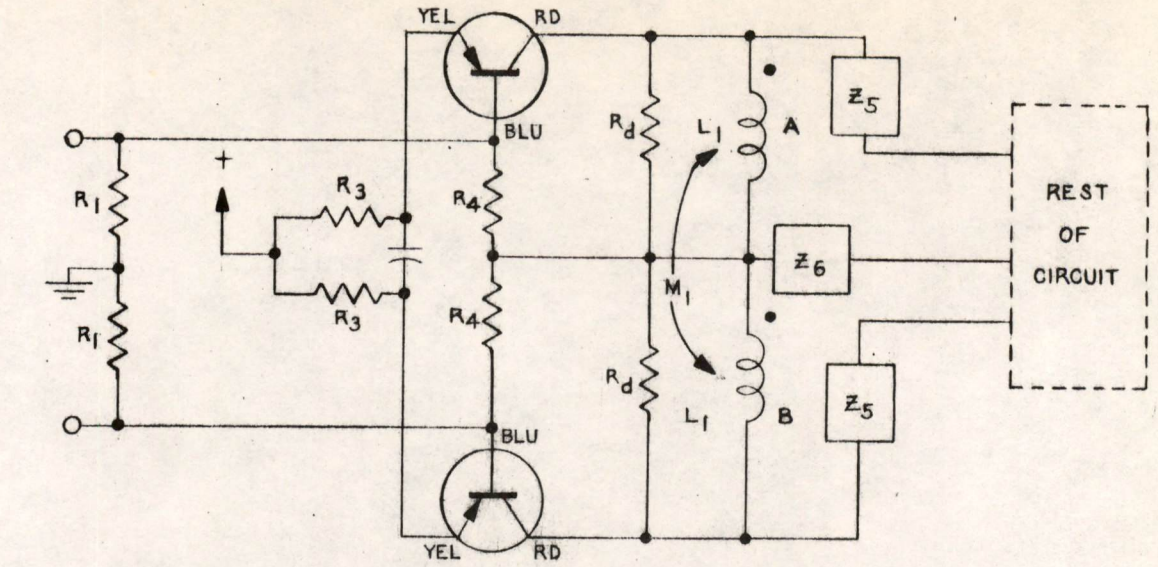

b) METHOD OF CONNECTING FROM SENSE WINDINGS – 1, 2, 3, AND 4 – SO AS TO MINIMIZE NOISE CONTRIBUTIONS OF PARTIALLY SELECTED CORES



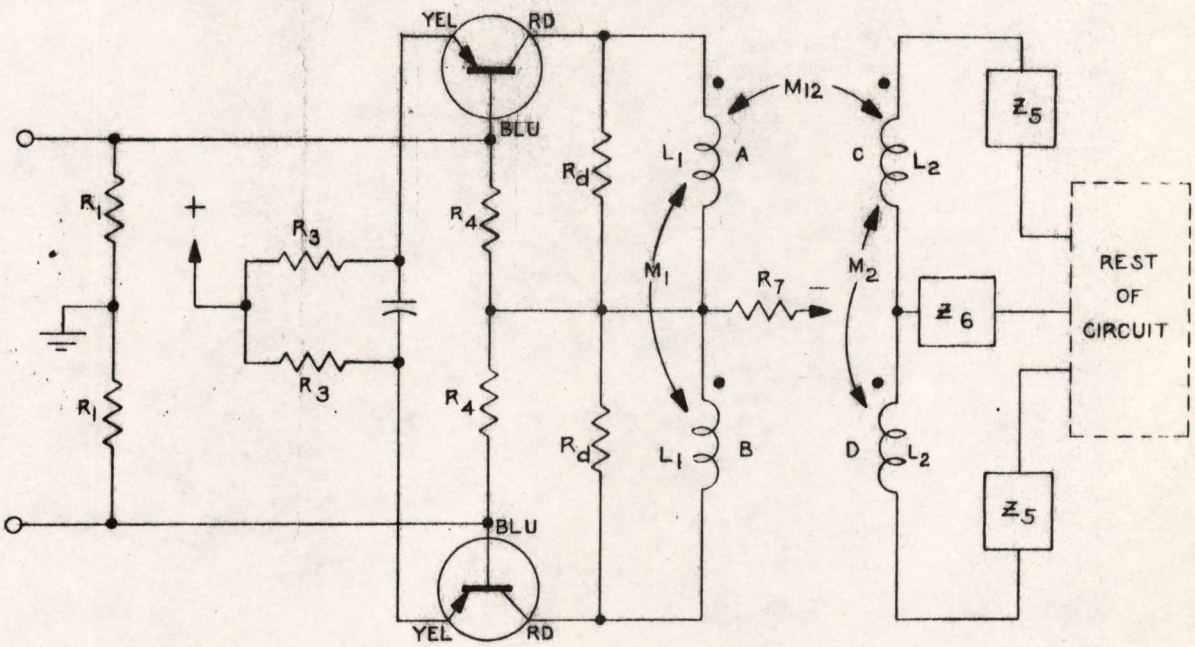

c) METHOD OF CONNECTING FOUR DIGIT WINDINGS – A, B, C AND D.

FIG. 2

256 × 256 PLANE BROKEN INTO 16 64 × 64 MODULES, WITH SENSING WINDING AND DIGIT PLANE WINDING CONNECTED IN VARIOUS WAYS.




a) CHOKE COUPLING




b) TRANSFORMER COUPLING

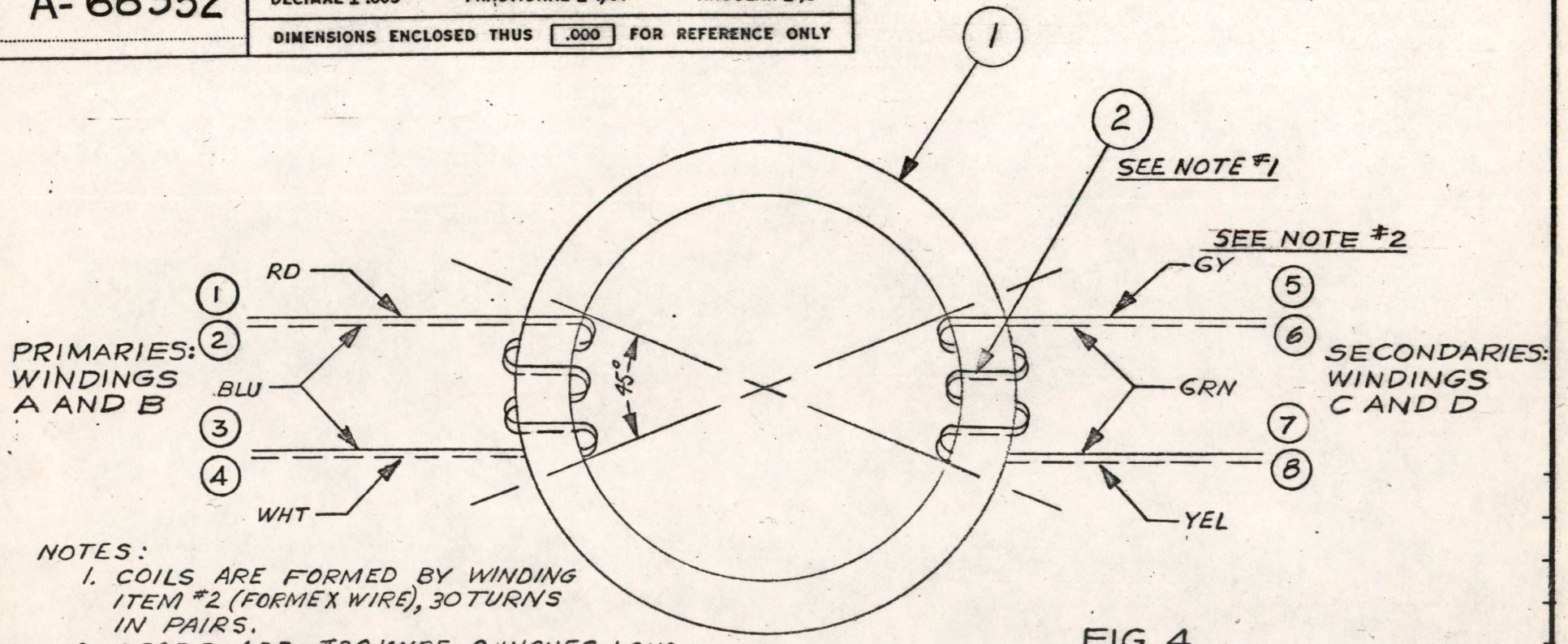
FIG. 3

TWO METHODS OF COUPLING FROM INPUT DIFFERENCE AMPLIFIER TO REMAINDER OF CIRCUIT

B-68256

A-66352

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY




NOTES:
1. COILS ARE FORMED BY WINDING ITEM #2 (FORMEX WIRE), 30 TURNS IN PAIRS.
2. LEADS ARE #20 WIRE 2 INCHES LONG IN SPECIFIED COLORS.

FIG. 4
METHOD OF WINDING TRANSFORMER FOR CIRCUIT PICTURED IN FIG. 3b

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE: Prel. 19 OCT 56

| ITEM | MATERIAL - DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| 2 | FORMEX MAGNET WIRE, #32 AWG G.E. | | AS REQD |
| 1 | PERMALLOY CORE PLASTIC ENCASED ARNOLD ENGINEERING CO. | 5340-S1 | 1 |

| CHG. | CN# | DATE | APPD. |
|---|---|---|---|
| -1 | 8354 | 11-28-56 | |

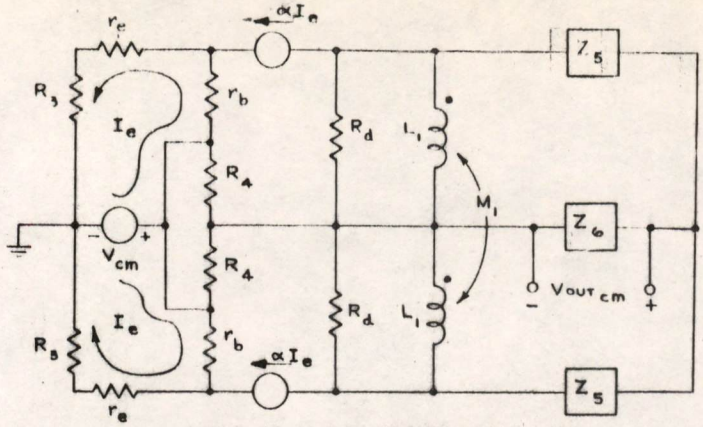
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

TRANSFORMER, SENSING AMPLIFIER

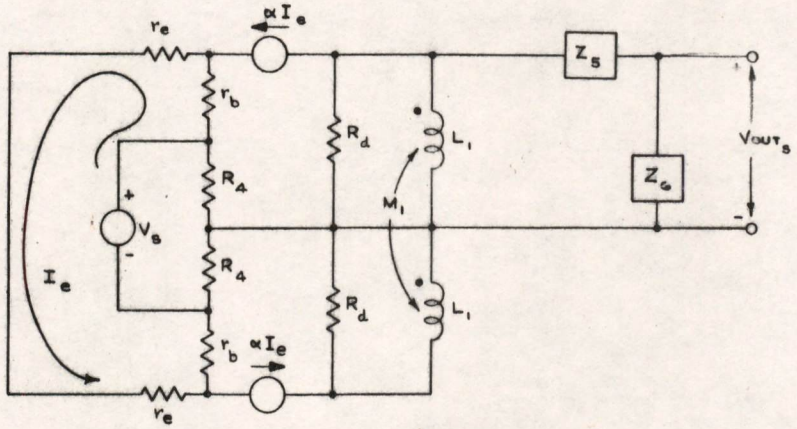
SCALE: NONE
DR. A.O. Annetti 5-28-56
ENG. 6-5-56
CK. 6/5/56
APPD.

A-66352

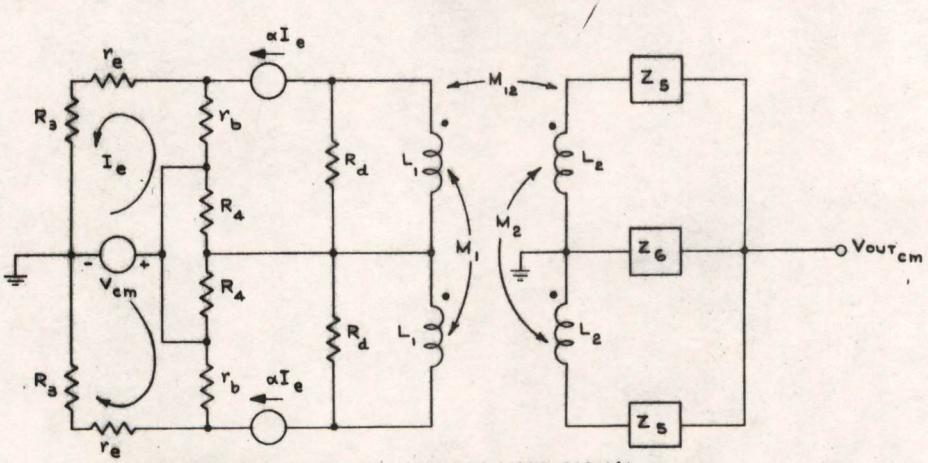
8M-7-54-Boston Blue Print



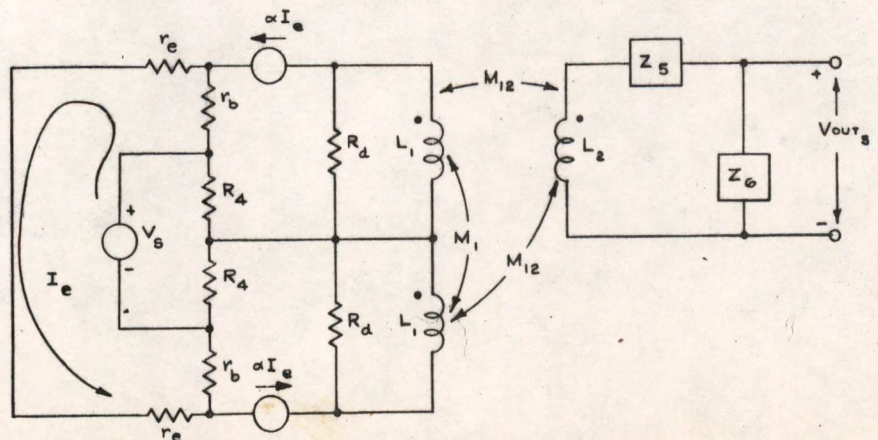

a. CHOKE COUPLING, COMMON MODE SIGNAL




b. CHOKE COUPLING, DIFFERENCE SIGNAL




c. TRANSFORMER COUPLING, COMMON MODE SIGNAL

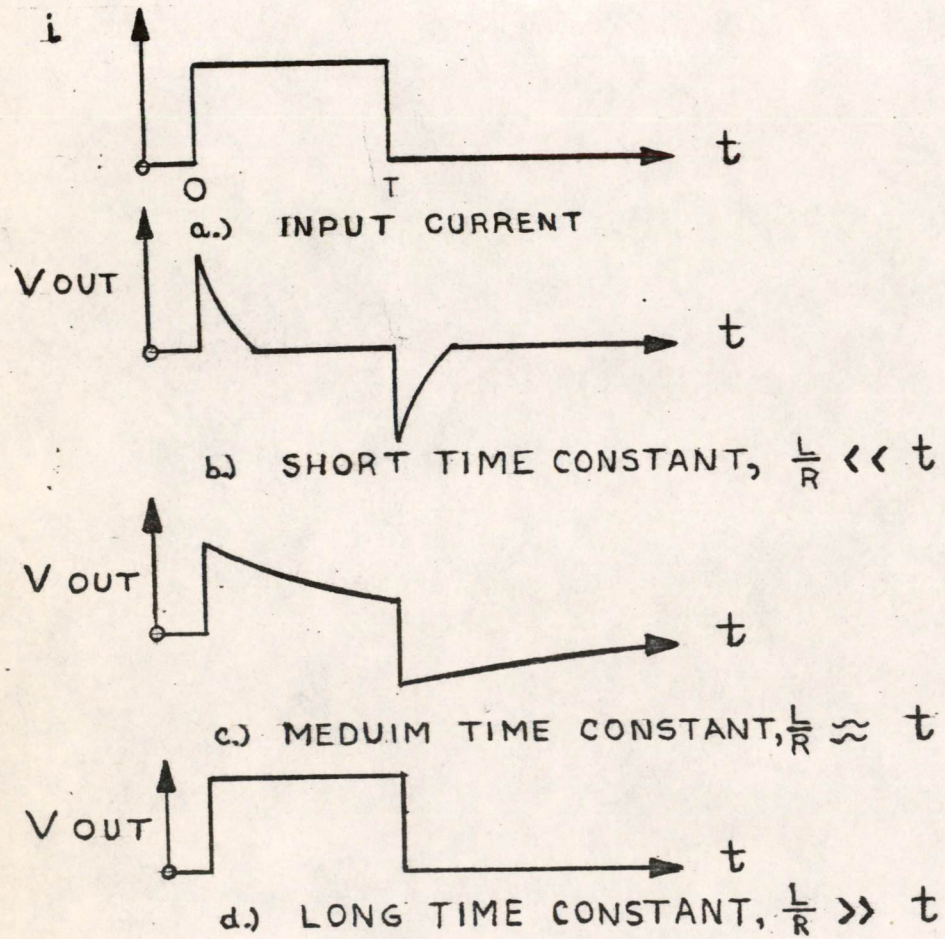



d. TRANSFORMER COUPLING, DIFFERENCE SIGNAL

FIG. 5

LINEARIZED AND BALANCED EQUIVALENT CIRCUITS FOR FIG. 3

C-68401



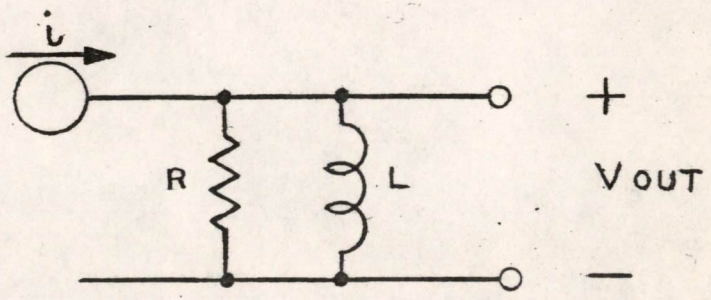
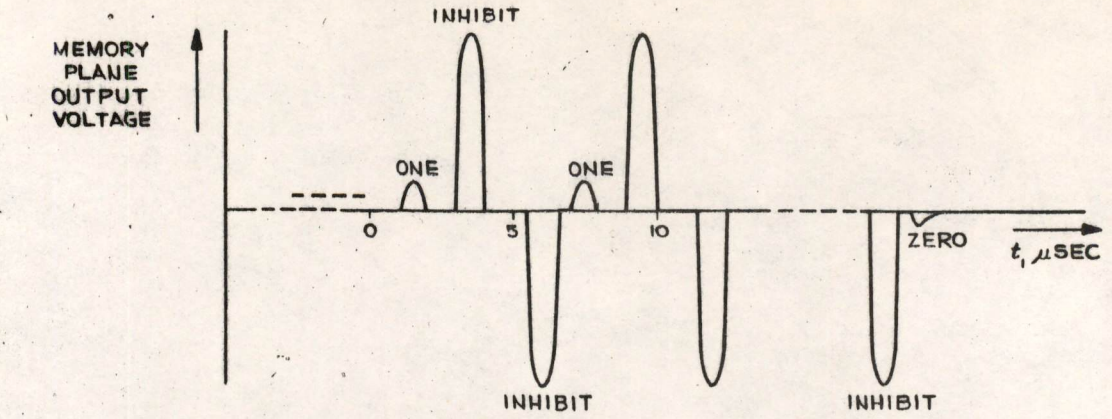
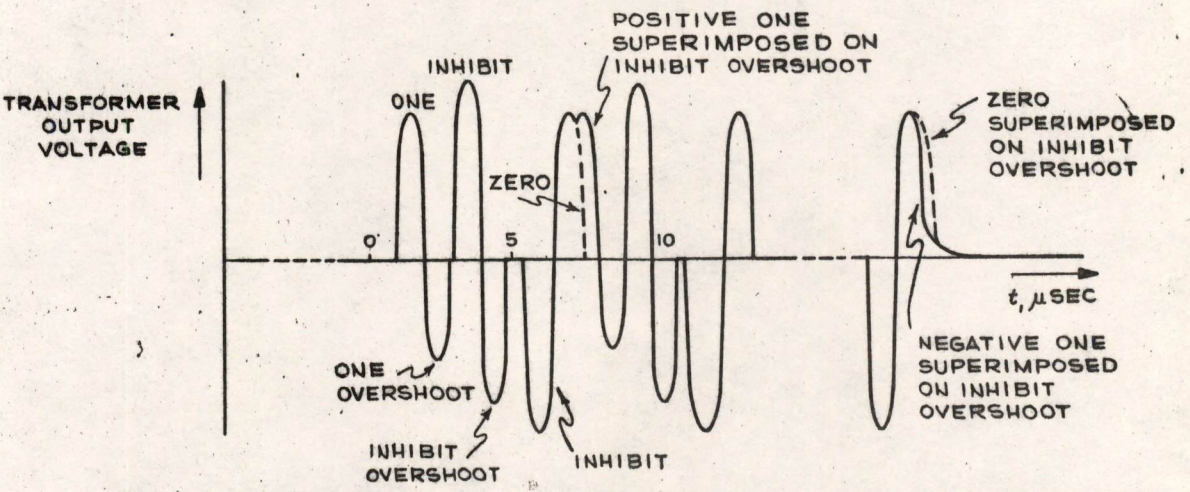




FIG 6

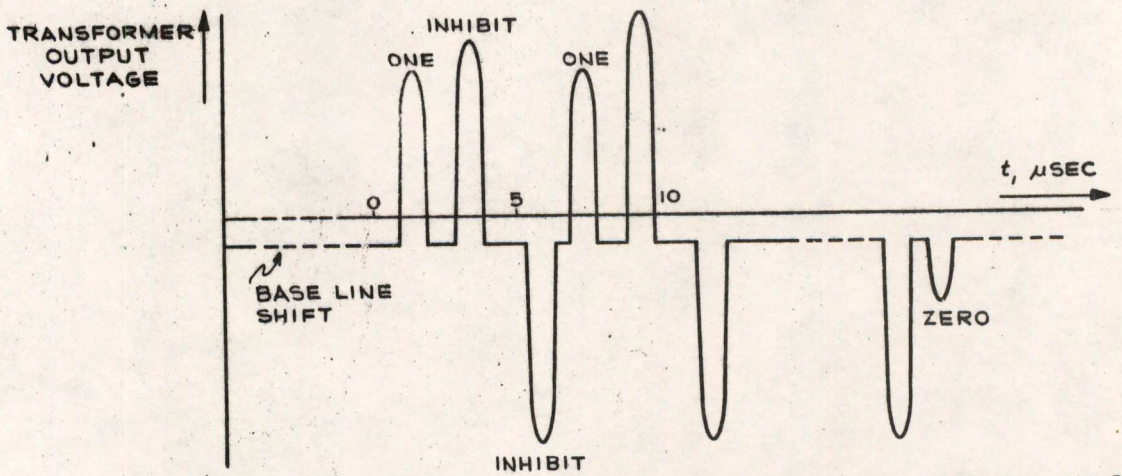
OUTPUTS OBTAINED FOR VARIOUS TIME CONSTANTS WHEN CURRENT SOURCE FEEDS PARALLEL RL CIRCUIT




a) SENSING AMPLIFIER INPUT




b) SHORT TIME CONSTANT TRANSFORMER – NON-LINEAR GAIN OF INPUT STAGE EXPLAINS GROWTH OF ONE's RELATIVE TO INHIBITS




c) LONG TIME CONSTANT TRANSFORMER – NON-LINEAR GAIN OF INPUT STAGE EXPLAINS GROWTH OF ONE's RELATIVE TO INHIBITS

FIG. 7

EFFCTS CAUSED BY A CHAIN OF UNIPOLARITY (POSITIVE) ONE's, INTERSPERSED WITH INHIBIT PULSES. THESE SHOW DIFFICULTIES THAT ARE ENCOUNTERED BOTH WITH SHORT AND LONG TIME CONSTANT TRANSFORMERS.

B-68846

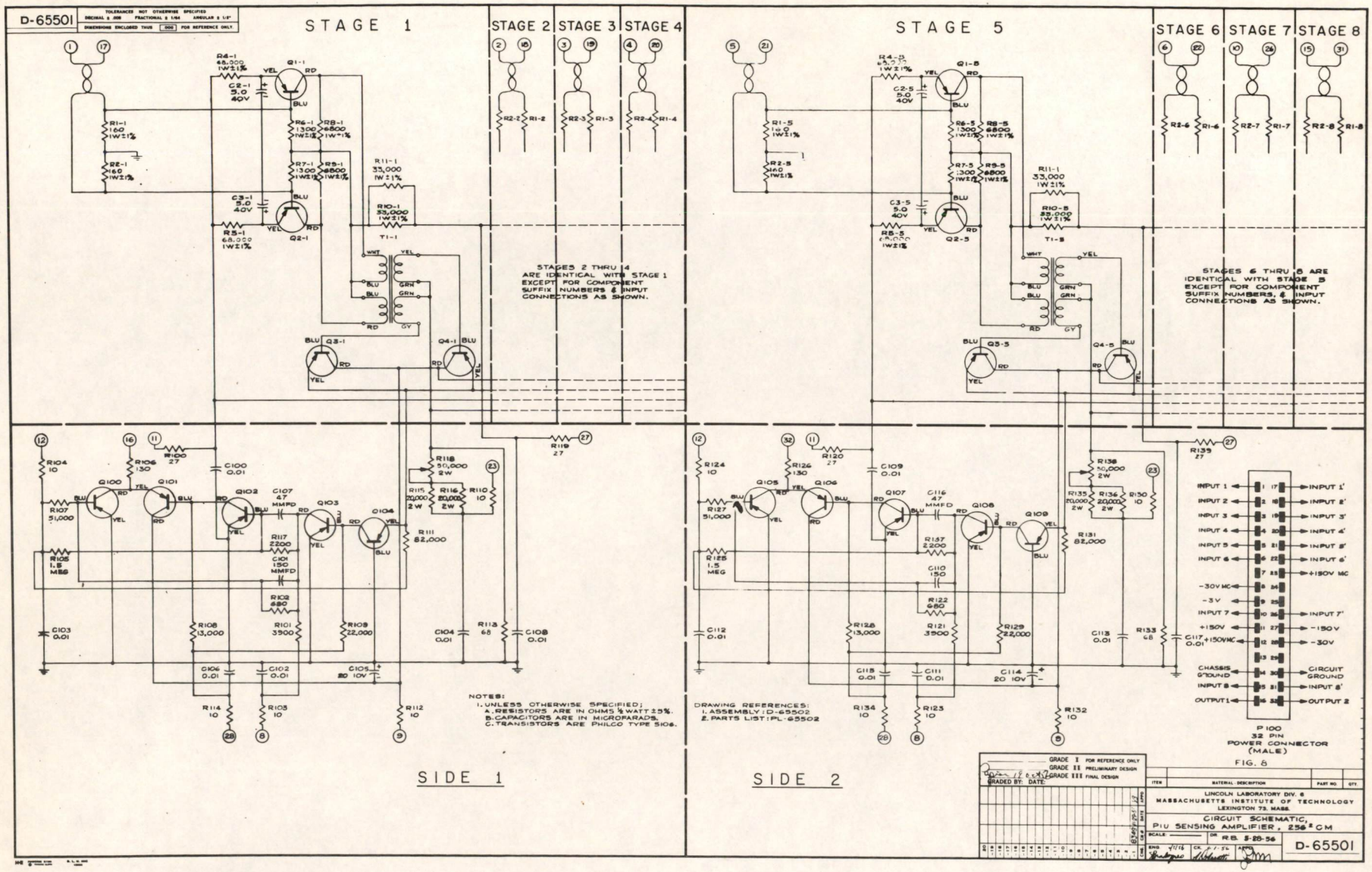

D-65501
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
STAGE 6
STAGE 7
STAGE 8
STAGES 2 THRU 4 ARE IDENTICAL WITH STAGE 1 EXCEPT FOR COMPONENT SUFFIX NUMBERS & INPUT CONNECTIONS AS SHOWN.
STAGES 6 THRU 8 ARE IDENTICAL WITH STAGE 5 EXCEPT FOR COMPONENT SUFFIX NUMBERS, & INPUT CONNECTIONS AS SHOWN.
NOTES:
1. UNLESS OTHERWISE SPECIFIED;
A. RESISTORS ARE IN OHMS ½ WATT ±5%.
B. CAPACITORS ARE IN MICROFARADS.
C. TRANSISTORS ARE PHILCO TYPE 2106.
DRAWING REFERENCES:
1. ASSEMBLY: D-65502
2. PARTS LIST: PL-65502
INPUT 1
INPUT 2
INPUT 3
INPUT 4
INPUT 5
INPUT 6
-30V MC
-3V
INPUT 7
+15OV
+150V MC
CHASSIS GROUND
INPUT 8
OUTPUT 1
INPUT 1'
INPUT 2'
INPUT 3'
INPUT 4'
INPUT 5'
INPUT 6'
+150V MC
INPUT 7'
-150V
-30V
CIRCUIT GROUND
INPUT 8'
OUTPUT 2
P100
32 PIN
POWER CONNECTOR
(MALE)
SIDE 1
SIDE 2
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.
CIRCUIT SCHEMATIC,
PIU SENSING AMPLIFIER, 256 ϕ CM
D-65501

FIG. 8

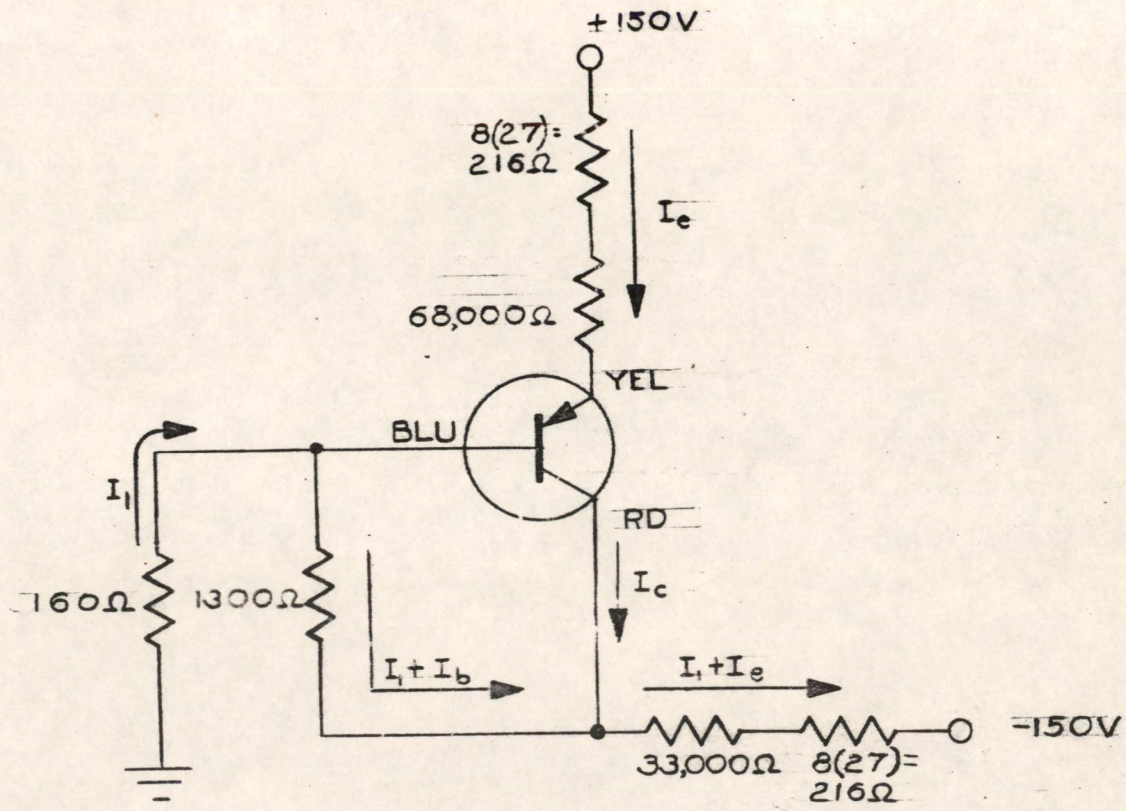



FIG. 9

D.C. OPERATION OF DIFFERENCE STAGE,
ASSUMING THAT INPUT TRANSISTORS ARE IDENTICAL

TRANSISTOR #48 BY M. PETERSON - DEC. 1954

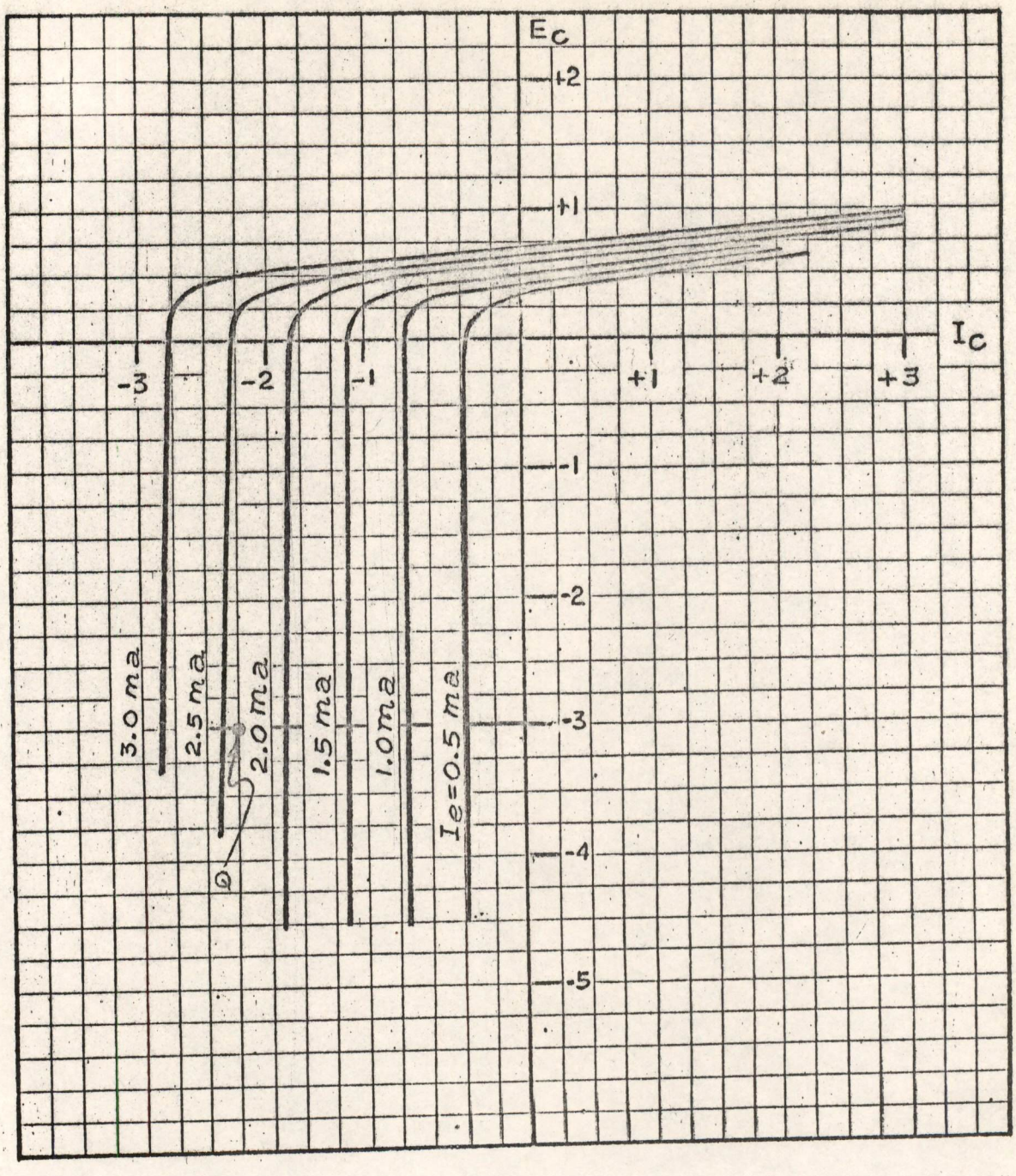
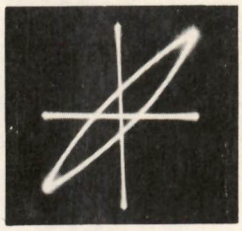



FIG. 10

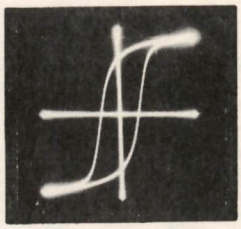
OPERATING POINT
OF DIFFERENCE STAGE TRANSISTORS AT Q

TYPICAL SBT CHARACTERISTICS GROUNDED BASE
$I_C$ vs $E_C$

A-68847



DRIVING CURRENT = 21 ma
MAXIMUM FLUX = 33.3 maxwells



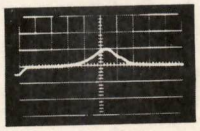
SATURATION LOOP
DRIVING CURRENT = 500 ma
SATURATION FLUX = 560 maxwells

FIG. 11

60 CYCLE HYSTERESIS LOOP OF TRANSFORMER CORE - PLASTIC ENCASED, PERMALLOY CORE, NUMBER 5340-SI MANUFACTURED BY ARNOLD ENGINEERING CO. ONE TURN (N=1) IS USED.

A-68253

INPUT DIFFERENCE SIGNAL

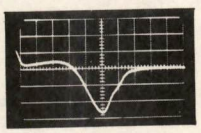


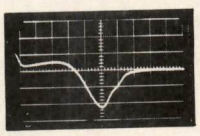
50 mV/cm

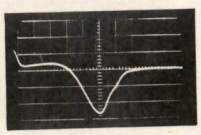
0.5 μSEC/cm

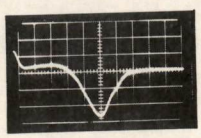
TRANSFORMER SECONDARIES

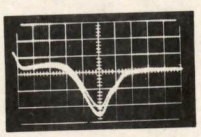
| | DIFFERENCE STAGE TRANSISTOR | α |
|---|---|---|
| CHANNEL 1 | A108 | 0.962 |
| | A109 | 0.950 |
| CHANNEL 2 | A81 | 0.972 |
| | A75 | 0.972 |
| CHANNEL 3 | A74 | 0.969 |
| | A107 | 0.968 |
| CHANNEL 4 | A73 | 0.956 |
| | A82 | 0.962 |











COMPOSITE OF FOUR CHANNELS

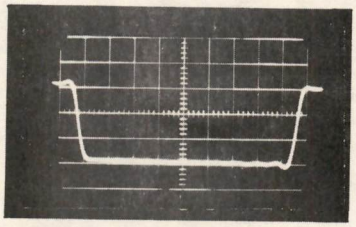
500 mV/cm

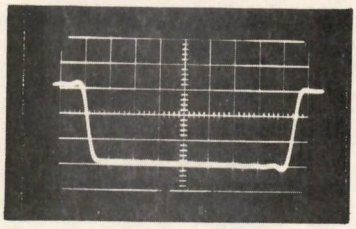
0.5 μSEC/cm

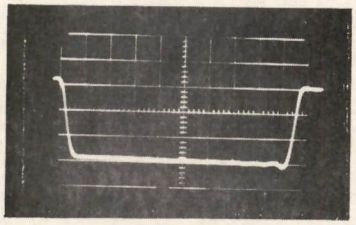
FIG 12

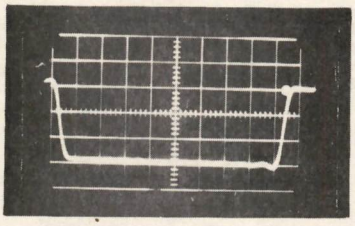
NEGATIVE PULSES AT TRANSFORMER SECONDARIES WHEN ALL INPUTS ARE CONNECTED IN PARALLEL. THIS SHOWS EFFECT OF DIFFERENT GAINS IN VARIOUS CHANNELS UPON THE SIZES OF PULSES APPLIED TO EMITTER FOLLOWERS. SENSING AMPLIFIER #9

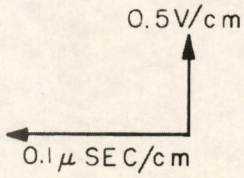
B-68252












| | DIFFERENCE STAGE TRANSISTORS | α |
|---|---|---|
| CHANNEL 1 | A108 | 0.962 |
| | A109 | 0.950 |
| CHANNEL 2 | A81 | 0.972 |
| | A75 | 0.972 |
| CHANNEL 3 | A74 | 0.969 |
| | A107 | 0.968 |
| CHANNEL 4 | A73 | 0.956 |
| | A82 | 0.962 |

FIG. 13

OUTPUT PULSES FROM DIFFERENT CHANNELS OF SENSING AMPLIFIER #9 FOR 50mV INPUT PULSES. THIS DEMONSTRATES THE EFFECT OF UNEQUAL GAINS IN DIFFERENT CHANNELS. RESISTIVE LOAD = 160Ω

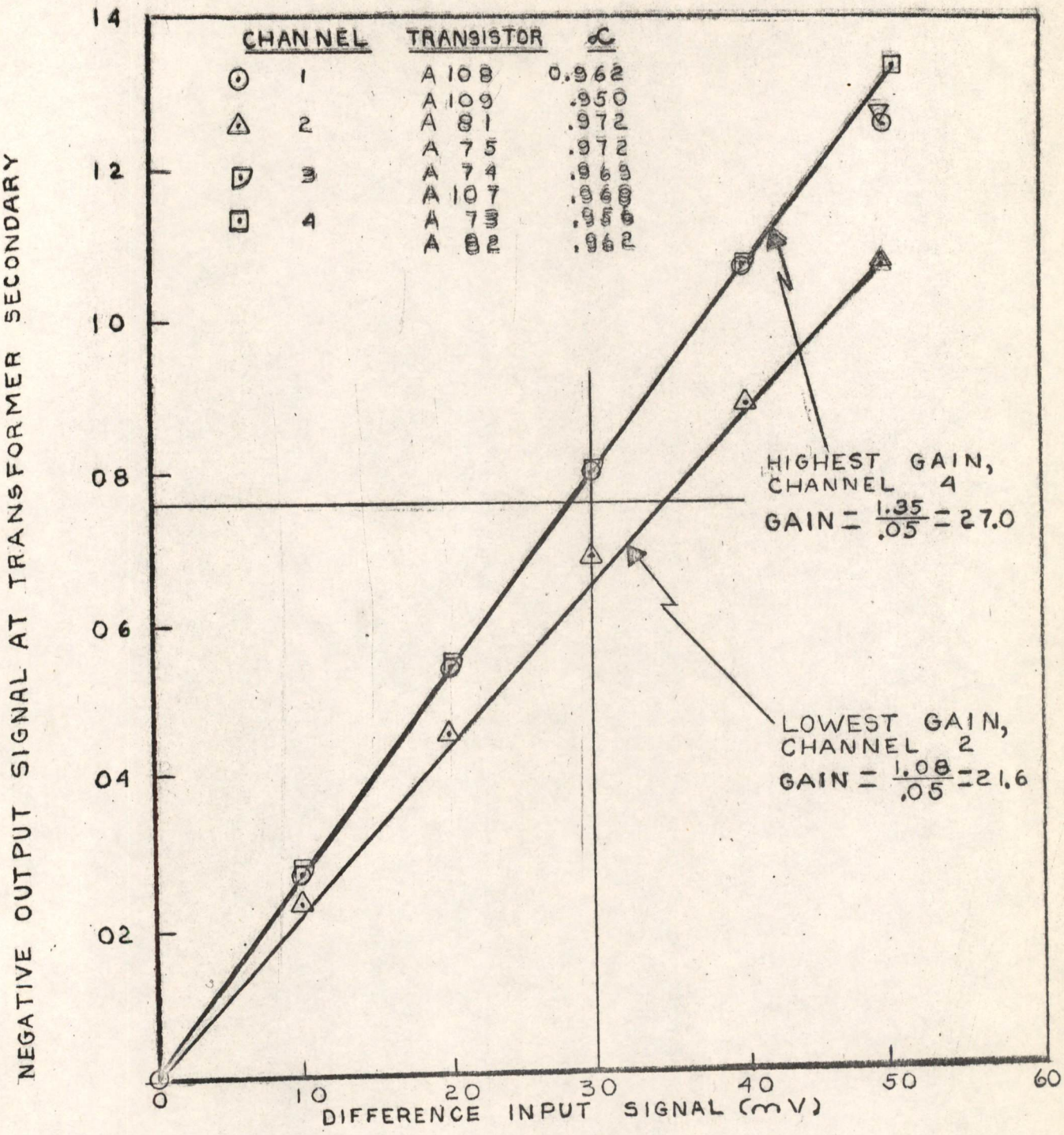



FIG 14

NEGATIVE SIGNAL AT TRANSFORMER SECONDARY AS A FUNCTION OF DIFFERENCE INPUT SIGNAL FOR THE DATA OF RUN 1

SENSING AMPLIFIER#9

A-68508

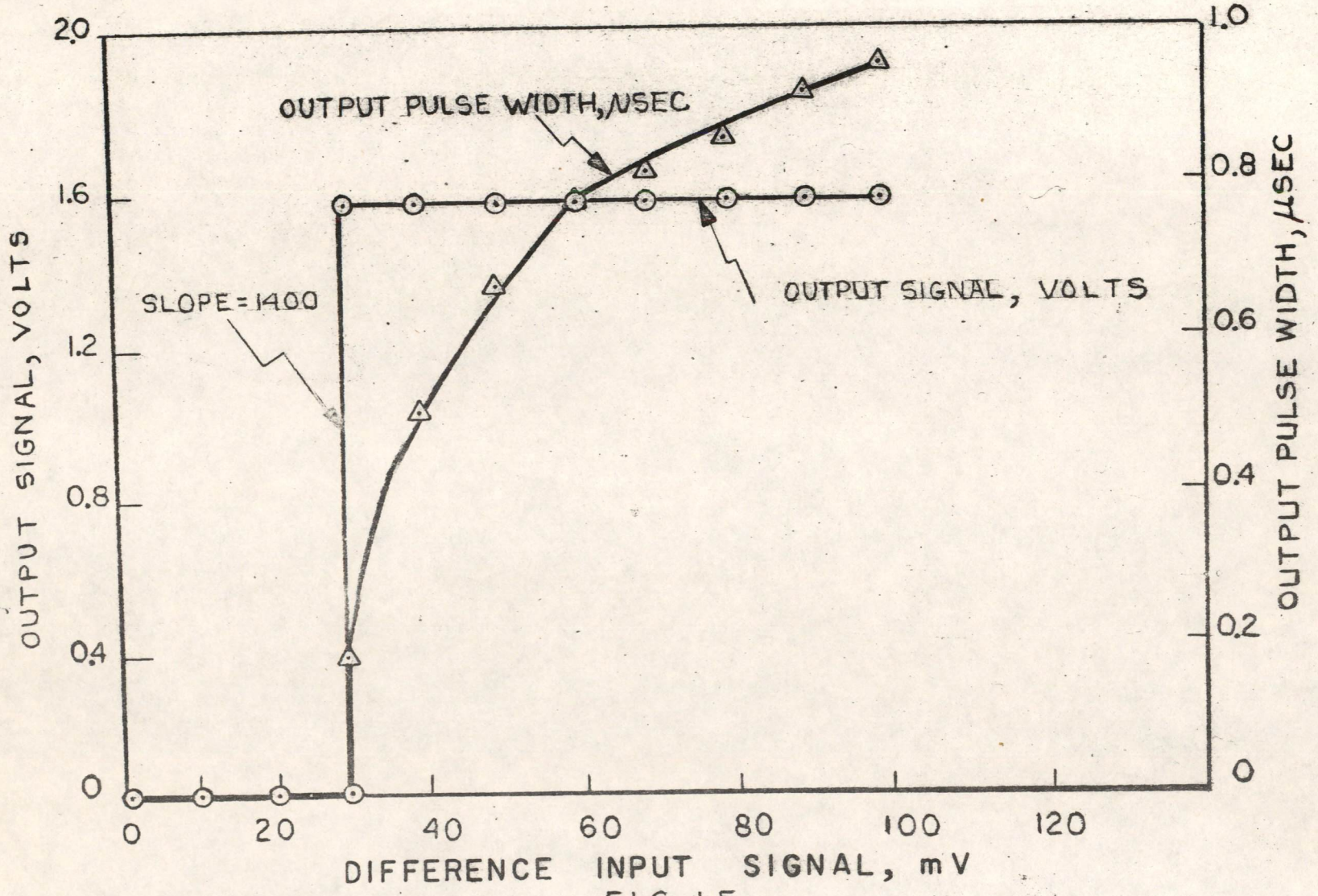
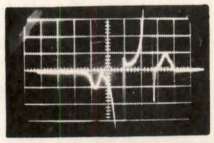



FIG. 15

TRANSFER CHARACTERISTIC OF TYPICAL SENSING AMPLIFIER

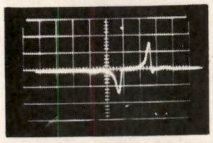
RESISTIVE LOAD = 160 Ω

SENSING AMPLIFIER # 9, CHANNEL 3



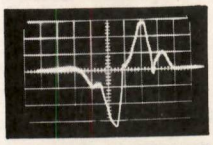
A. INPUT DIFFERENCE SIGNAL

50 mV/cm
1.0 μSEC/cm



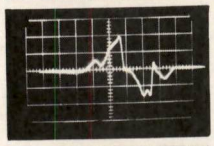
B. INPUT DIFFERENCE SIGNAL

500mV/cm
1.0 μSEC/cm



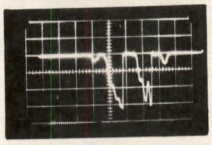
C. DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

2V/cm
1.0 μSEC/cm



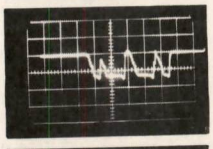
D. SIGNAL AT ONE SIDE OF TRANSFORMER SECONDARY (D.C. LEVEL = +0.73 VOLTS)

2V/cm
1.0 μSEC/cm



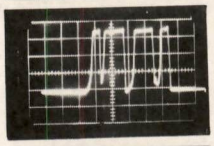
E. SIGNAL AT EMITTER FOLLOWER OUTPUT (D.C. LEVEL = +0.25 VOLTS)

1V/cm
1.0 μSEC/cm

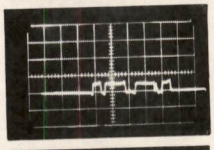


F. OUTPUT OF Q104 (D.C. LEVEL = +0.22 VOLTS)

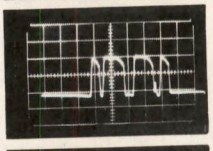
500mV/cm
1.0 μSEC/cm



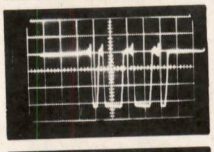
G. OUTPUT OF Q103 (D.C. LEVEL = -3.6 VOLTS)



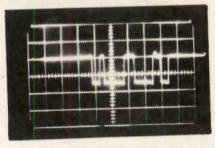
H. INPUT TO Q102 (D.C. LEVEL = -0.40 VOLTS)



I. INPUT TO Q100 (D.C. LEVEL = -0.43 VOLTS)



J. OUTPUT OF Q102 (D.C. LEVEL = -0.04 VOLTS)



K. SENSE AMPLIFIER OUTPUT, ACROSS 160Ω (D.C. LEVEL = GROUND)

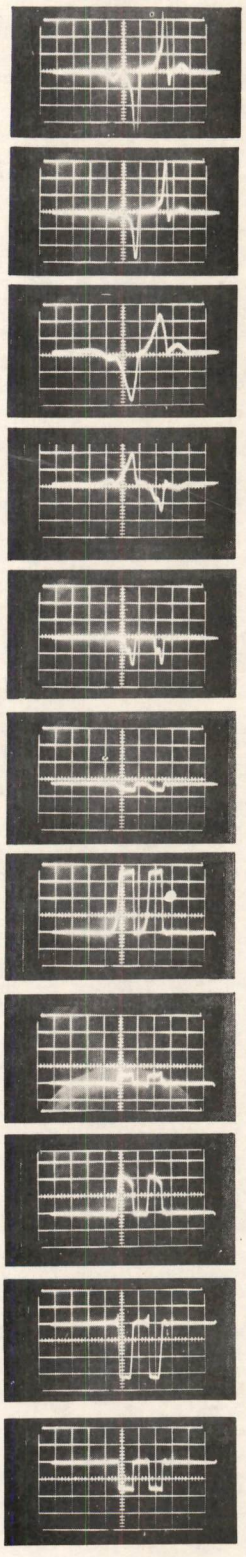
1V/cm
1.0 μSEC/cm

ORDER OF PULSES IS ONE, INHIBIT, INHIBIT, ONE

FIG. 16

TRACE SIGNAL THROUGH CIRCUIT.
INPUT ONE IS 50mV IN AMPLITUDE. CLIPPING LEVEL IS SET AT 30 mV.
SENSE AMPLIFIER #9, CHANNEL 3. CYCLE TIME ≅ 4.5 μSEC. RESISTIVE LOAD = 160Ω.

B-68402



A. INPUT DIFFERENCE SIGNAL

50 mV/cm
1.0 μSEC/cm

B. INPUT DIFFERENCE SIGNAL

100 mV/cm
1.0 μSEC/cm

C. DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

2 V/cm
1.0 μSEC/cm

D. SIGNAL AT ONE SIDE OF TRANSFORMER SECONDARY (D.C. LEVEL = +0.73 VOLTS)

2 V/cm
1.0 μSEC/cm

E. SIGNAL AT EMITTER FOLLOWER OUTPUT (D.C. LEVEL = +0.25 VOLTS)

1 V/cm
1.0 μSEC/cm

F. OUTPUT OF Q104 (D.C. LEVEL = +0.22 VOLTS)

500 mV/cm
1.0 μSEC/cm

G. OUTPUT OF Q103 (D.C. LEVEL = -3.6 VOLTS)

H. INPUT TO Q102 (D.C. LEVEL = -0.40 VOLTS)

I. INPUT TO Q100 (D.C. LEVEL = -0.43 VOLTS)

J. OUTPUT OF Q102 (D.C. LEVEL = -0.04 VOLTS)

K. SENSE AMPLIFIER OUTPUT, ACROSS 160Ω (D.C. LEVEL = GROUND)

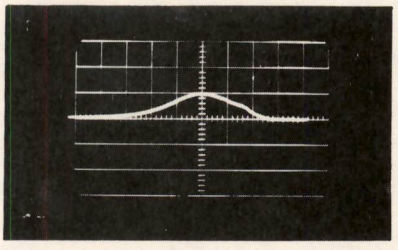
1 V/cm
1.0 μSEC/cm

ORDER OF PULSES IS ZERO, INHIBIT, INHIBIT, ZERO

FIG. 17

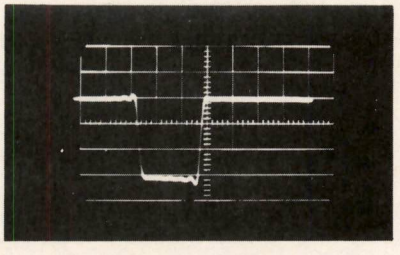
TRACE SIGNAL THROUGH CIRCUIT,
INPUT ZERO IS 20mV IN AMPLITUDE. CLIPPING LEVEL IS SET AT 30 mV.
SENSE AMPLIFIER #9, CHANNEL 3. CYCLE TIME ≅ 4.5 μSEC. RESISTIVE LOAD = 160Ω

B-68403



DIFFERENCE INPUT
50 mV/cm

0.2 μSEC/cm



OUTPUT ACROSS 160 Ω
500 mV/cm

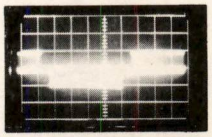
0.2 μ SEC/cm

FIG 18

THE DELAY OF A PULSE PASSING THROUGH THE SENSING AMPLIFIER

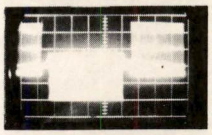
SENSING AMPLIFIER # 9, CHANNEL 3. CLIPPING LEVEL ≅ 30mV. DELAY ≅ 0.3 μ SEC. RESISTIVE LOAD = 160 Ω

A 68262



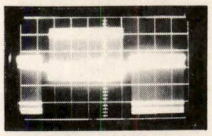
a) DIFFERENCE INPUT SIGNALS

50mV/cm
2000 μSEC/cm



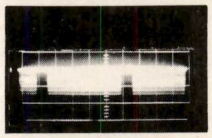
b) DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

1V/cm
2000 μSEC/cm



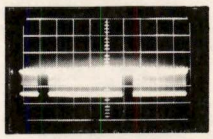
c) SIGNALS AT ONE SIDE OF TRANSFORMER SECONDARY

500mV/cm
2000 μSEC/cm



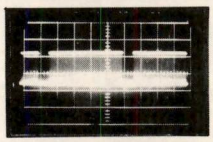
d) SIGNALS AT EMITTER FOLLOWER OUTPUT

500mV/cm
2000 μSEC/cm



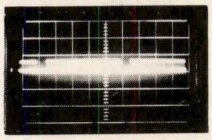
e) OUTPUT OF Q104

500mV/cm
2000 μSEC/cm



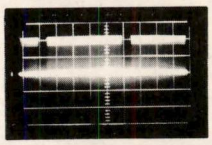
f) OUTPUT OF Q103

2V/cm
2000 μSEC/cm



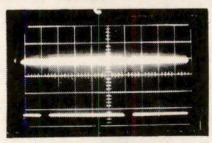
g) INPUT TO Q102

1V/cm
2000 μSEC/cm



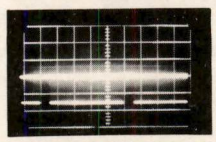
h) INPUT TO Q100

1V/cm
2000 μSEC/cm



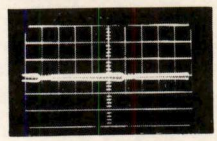
i) OUTPUT OF Q102

1V/cm
2000 μSEC/cm



j) SENSING AMPLIFIER OUTPUT, ACROSS 160Ω

1V/cm
2000 μSEC/cm



k) DIFFERENCE SIGNAL ACROSS CAPACITORS C2-3 AND C3-3 AT THE INPUT

50mV/cm
2000 μSEC/cm

FIG. 19

BURST TEST FOR DETERMINING PRF SENSITIVITY OF SENSING AMPLIFIER. INPUT PULSES ARE SPACED 6μSEC APART

UNIPOLARITY CHAINS LAST FOR 8,600 μSEC. CHAINS CONSIST OF ABOUT 1430 PULSES. SENSING AMPLIFIER # 9, CHANNEL 3. CHIPPING LEVEL ≅ 30mV. RESISTIVE LOAD 160Ω

B-68645

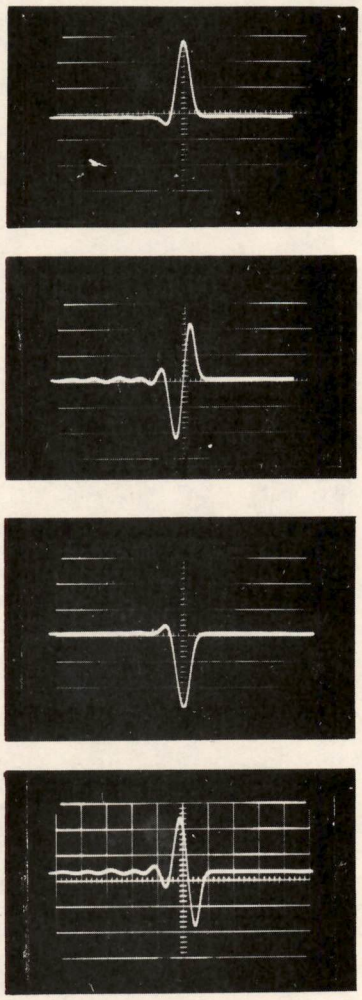



FIG. 20

EFFECT OF LARGE COMMON MODE SIGNAL

UPON THE SENSING AMPLIFIER OUTPUT

AMPLIFIER #9, CHANNEL 3. RESISTIVE LOAD = 160 Ω

A-68593

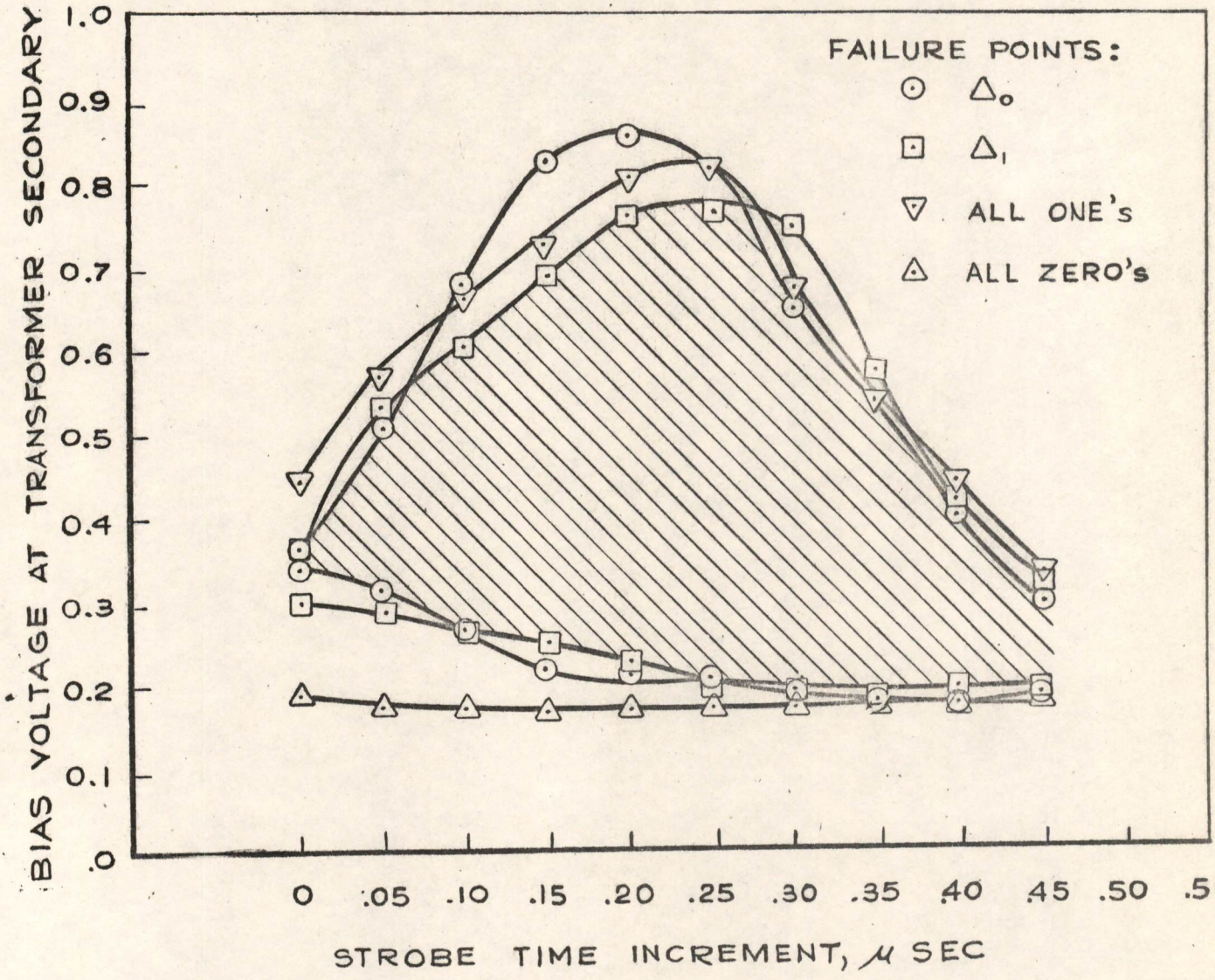



FIG. 21

MARGINS OF SENSING AMPLIFIER #3 WHEN TESTED WITH 256 x 256 MAGNETIC CORE MEMORY

A-68644

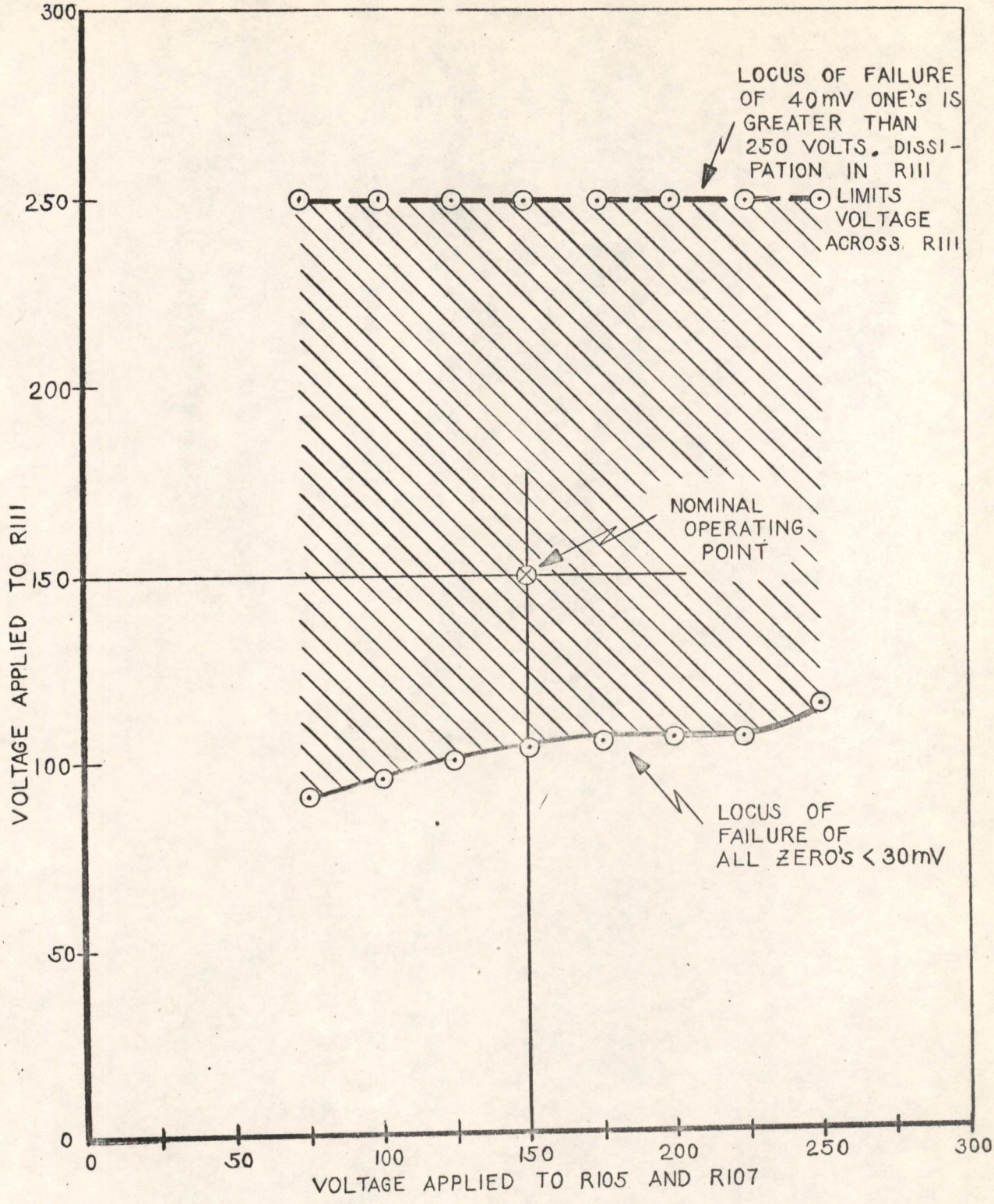



FIG. 22

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO RIII vs VOLTAGE APPLIED TO RIO5 AND RIO7.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30mV.

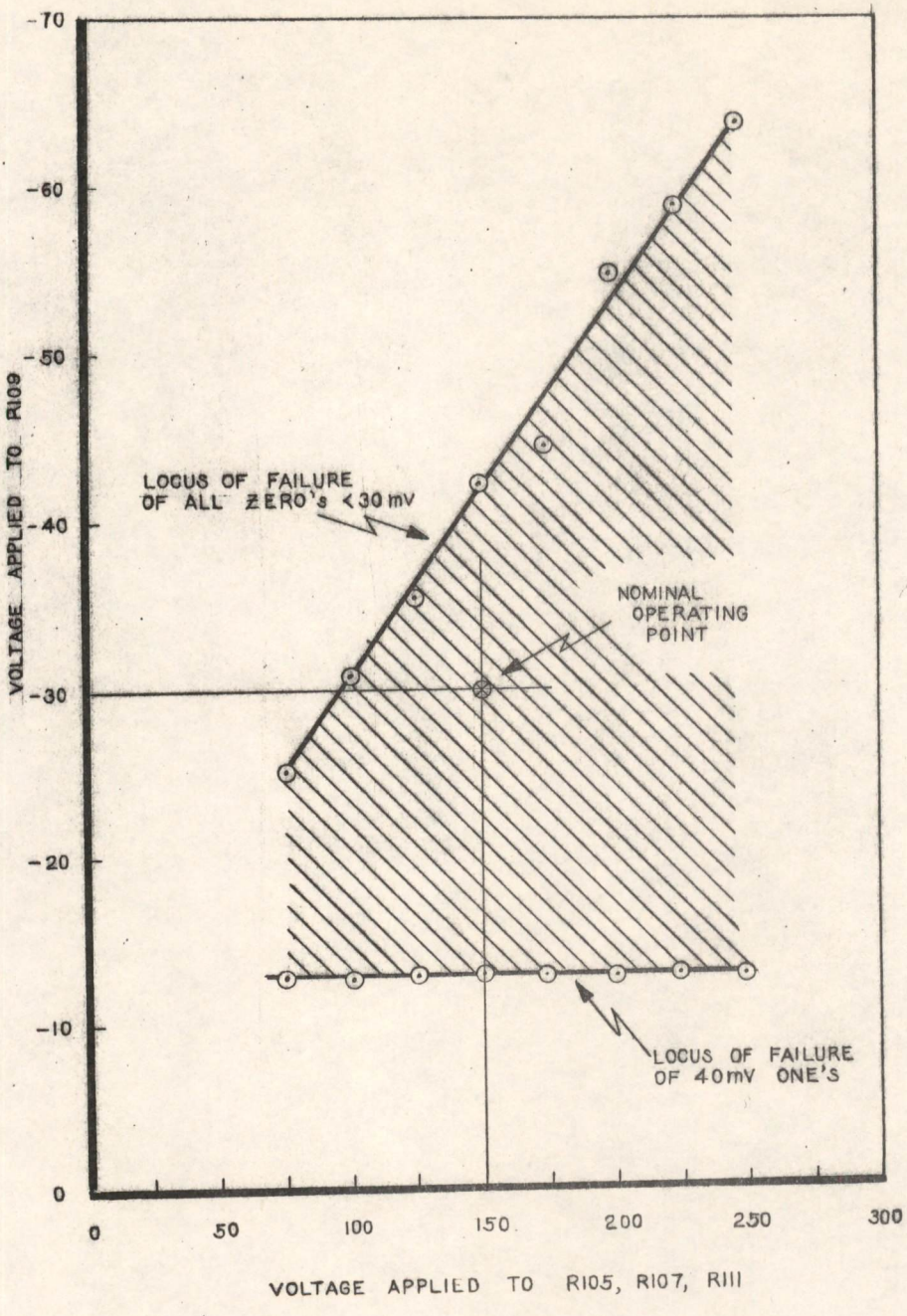



FIG. 23

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R109 vs VOLTAGE APPLIED TO R105, R107, RIII.

SENSE AMPLIFIER #9, CHANNEL 3.

CLIPPING LEVEL ≅ 30mV.

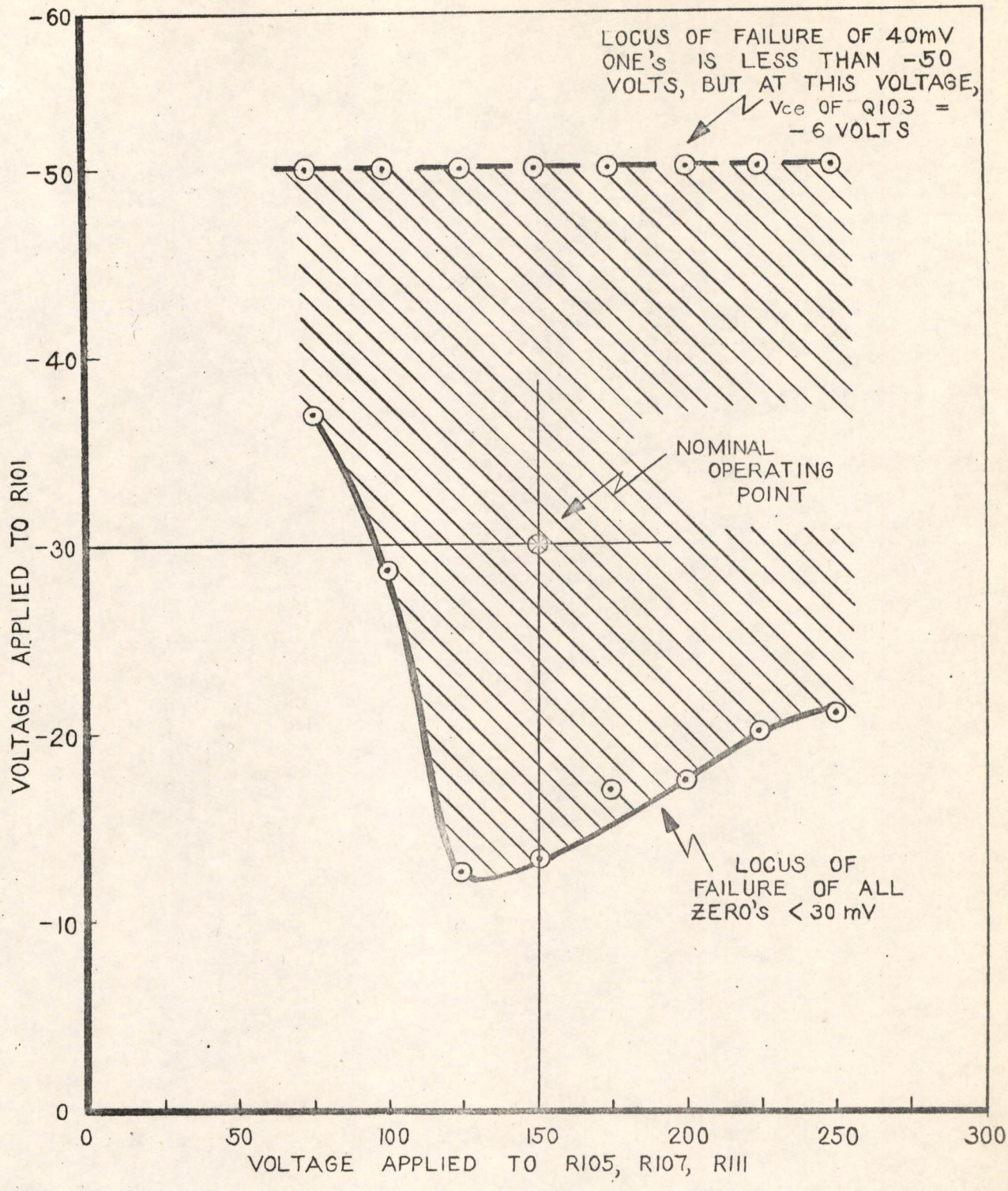



FIG. 24

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R101 vs VOLTAGE APPLIED TO R105, R107, R111.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30mV.

A-68718

R. L. Best
B-077



Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A Transistorized Sensing Amplifier for the 256 X 256 Core Memory

To: W. N. Papian

From: S. Bradspies

Date: November 16, 1956

Approved: R. L. Best
R. L. Best

Abstract: A transistorized sensing amplifier, suitable for use in conjunction with a 256 X 256 magnetic core memory plane has been designed. This plane will be equipped with four sensing windings, each of which feeds an independent amplifier input. The circuit rectifies the bi-polarity pulses, and mixes the four inputs so that there is only one output per plane. The output is a negative 10 ma pulse that feeds a 160 Ω cable.

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

## I Introduction:

Ever since the introduction of magnetic core memory devices to the digital computers at M.I.T. - Whirlwind I and MTC - the problem of supplying the information held by this memory to the computer has not been solved to everyone's satisfaction. [1, 2, 3, 4, 5]

It has been found impossible to ground either end of the sensing winding because of the presence of common mode signals.[3] This has led to the necessity for using a difference amplifier input.

The memory plane may display a variety of undesirable output pulses (Fig.1) in addition to the signal it is supposed to amplify. These signals may be listed:

a. ONE -- is the signal that is to be amplified and fed to the computer. It is nominally 50 millivolts high and 1 microsecond wide in the 256 X 256 memory.

b. ZERO -- is a signal that should not be present in the output. The absense of an output from the sense amplifier at the time of interrogation is taken to be ZERO. When a single core holding a ZERO is selected, its output is very small. However, in an n x n memory plane, there are 2 (n-1) partially selected cores and the noises produced by these cores may combine with the output of the selected core to produce a substantial output pulse. It is necessary that the sense amplifier be able to distinguish between the ONE and ZERO outputs, either in time or amplitude.

---


1. Laspina, C.A. "Basic Circuits - Sensing Amplifiers", M.I.T. Digital Computer Laboratory Memorandum, M - 1969, 10 April, 1953.

2. Laspina, C.A. "Basic Circuits - Sensing Amplifier, Preliminary Specifications, PB#20", M.I.T. Digital Computer Laboratory Memorandum, M-2274, 3 July, 1953.

3. Sarles, F.W.Jr. "A Transistorized Amplifier - Discriminator for Core Memory Output Sensing", S.M.Thesis Proposal, M.I.T. Lincoln Laboratory Memorandum 6M-3417, 7 March 1955.

4. Sarles, F.W.Jr. "A Transistorized Amplifier-Discriminator for Core Memory Output Sensing", S.M.Thesis, M.I.T. Department of Electrical Engineering, May 1955.

5. Zopatti, R.C. Private Communications

c. Inhibit Noise -- is caused when the digit plane winding is pulsed during the writing of a ZERO. When the inhibit current is applied, every core in the plane is partially selected. It has been found that in the worst case, for a 64 X 64 plane, that the signal is about 1 volt in amplitude. The amplifier must not be so disturbed by this large pulse that it is unable to respond correctly to a signal that is applied about 1.0 microsecond following the completion of the inhibit.

d. Common Mode Signals -- are probably caused by capacitive coupling between the drive lines and the sensing winding. It is expected that these signals (which raise both ends of the sense winding together) may be as large as 10 volts per 64 X 64 plane. These common signals must be totally rejected.

In connection with items c and d above, reference was made to disturbances caused by a single 64 X 64 plane ( or module). If the 256 X 256 plane was treated as a unit (with one sensing winding and one digit plane winding), then the noise pulses would be greatly increased. Fig. 2a demonstrates that during the read operation $2(n-1) = 2(256-1) = 510$ cores receive half select excitations. In a 64 X 64 plane, only $2(64-1) = 126$ cores are disturbed during read. It is seen, then, that if a single sense winding is used for the large plane, the noise is increased by a factor of 4.05. It is essential, therefore, that the sense winding be split so that a minimum of noise due to partial selects is found on any one sensing winding. If the winding is distributed as shown in Fig.2b (no sense winding passes through any two modules that are on the same vertical or horizontal line), this condition will be met, and a maximum of 128 partially selected cores will be sensed by any one sense winding. Furthermore, due to the fact that the sensing winding acts as a delay line, shortening the length of it, cuts the delay, and restricts the time interval during which an information pulse may arrive.

Experiments have demonstrated that it is not possible to use a single digit plane winding per plane. There are to be four of these windings per plane, and they will be connected as shown in Fig.2c. The memory will be operated in a manner that excites only the required digit winding when a ZERO is to be written. The other three digit drivers will be held off. The primary reason for this is to cut the ringing on the X and Y driving lines, and on the sensing windings due to capacitive coupling between these leads and the inhibit leads. This permits a large reduction in the memory cycle time (to less than 6 μsec). Of course, this operation aids the sensing amplifier because of the reduction in the sizes of the inhibit pulses to those seen by 64 X 64 planes.

It is found that a memory plane can put out a long chain of unipolarity pulses, followed immediately by pulses of the opposite

polarity. It is essential that the amplifier not be so prf sensitive that these kinds of pulse sequences cause a misreading of information.

## II Preliminary Considerations

One of the major requirements of the sensing amplifier is speed. It must be able to respond quickly and to recover quickly. These conditions lead to the necessity for using fast transistors, and Philco Surface Barriers (SBT's) -- which are used throughout the TX-0 computer-- are the best commercially available transistors in this respect.

If the amplifier is to perform satisfactorily, it is necessary that it be capable of recovery from the peculiar signals (mentioned above) that may be applied to it. Consequently, the sensing amplifier has about 1 microsecond in which to recover from a four volt inhibit pulse, and it must not be allowed to give false outputs when it is excited by a string of unipolarity pulses. Actually, a direct coupled amplifier would be ideal for this particular application. But this is not possible in the present application for reasons to be discussed below.

In order to permit the difference amplifier to operate most satisfactorily, it is necessary to have the circuit impedances adjusted in an attempt to block common signals and to aid difference signals. These ideals can be realized by use of either choke or transformer coupling, if the coil polarities are as shown in Fig. 3.

The circuit pictured in Fig. 3a works well in all respects save one. It fails to effectively eliminatethe common mode signal. On the other hand, the circuit pictured in Fig. 3b behaves as well as that which is choke coupled, and it also eliminates common mode signals to a large extent.

For the best results the choke, or transformer, should be wound as shown in Fig. 4. If the choke is used, windings c and d are eliminated. In order to achieve the proper coil polarities, leads 2 and 3 are connected to form the center tap of the primary. If the coupling element is a transformer, leads 6 and 7 are also joined to form the secondary center tap.

The two circuits of Fig. 3 may be analyzed, approximately, by drawing the simplified linearized equivalent circuits. These are shown in Fig. 5. In these equivalent circuits the following assumptions are made:

1.) Both halves of circuits are identically balanced;

2.) Grounded base current gain of each transistor is $\alpha$;

3.) Base resistance is $r_b$;

4.) Emitter resistance is $r_e$;

5.) Collector resistance is infinite;

6.) $Z_5$ is a non-linear impedance such as a diode -- low in one direction and high in the other direction;

7.) Mutual coupling between primary windings is $M_1$;

8.) Mutual coupling between secondary windings is $M_2$;

9.) Mutual coupling between any primary winding and any secondary winding is $M_{12}$;

10.) Sensing winding impedence is negligible.

Fig. 5a shows the equivalent circuit for the choke coupled case when a common mode signal $V_{cm}$, is applied. The output voltage is

$$V_{out\,cm} = -\frac{2\alpha V_{cm} Z_6 R_d (L_1 - M_1)s}{\left[R_d + Z_5 + 2Z_6\right]\left[R_p + (L_1 - M_1)s\right]\left[R_3 + r_e + r_b(1-\alpha)\right]}$$

$$\cong -\frac{2\alpha V_{cm} Z_6 R_d (L_1 - M_1)s}{R_3\left[R_d + Z_5 + 2Z_6\right]\left[R_p + (L_1 - M_1)s\right]} \qquad (1)$$

in which

$$R_p = \frac{R_d (Z_5 + 2Z_6)}{R_d + Z_5 + 2Z_6}.$$

It is observed that the only way in which the common mode signal can be eliminated is to have $M_1 = L_1$. In actual practice this is not possible, and so one must be content to allow some common mode to pass. Some help is achieved by allowing $R_3$ to be very large. However, there is a limit to this, for the supply voltage must be increased proportionally.

Fig. 5b shows the equivalent circuit that is presented to a difference signal. It is assumed that the capacitor across the resistors $R_3$ effectively shorts the emitters together.

It is found that

$$V_{out\,s} = -\frac{\alpha V_s R_d Z_6 \left[R_d + (L_1 - M_1)s\right]\left[L_1 + M_1\right]s}{2\left[r_e + r_b(1-\alpha)\right]\left[R_d + Z_5 + Z_6\right]\left[(R_L + L_1 s)(R_d + L_1 s) - (M_1 s)^2\right]} \qquad (2)$$

in which

$$R_L = \frac{R_d (Z_5 + Z_6)}{R_d + Z_5 + Z_6}.$$

The gain in this circuit is greater for the difference signal than it is for the common signal, but one cannot assume that the common signal is negligible.

Fig. 5c shows the equivalent circuit for a common mode signal in a transformer coupled circuit. The output is found to be

$$V_{out\,cm} = 0. \tag{3}$$

This is due to the fact that the net current in the primaries of the transformer is zero, and there can be no signal coupled through to the secondary. In actual practice, however, it is found that some signal may be transmitted by capacitive coupling between the leads of the primaries and secondaries. In order to minimize this capacity, the primaries and secondaries are isolated from each other to as great an extent as possible, as shown in Fig. 4. Another manner in which common mode may get through is if the circuit elements are not balanced. One percent resistors are used in attempt to minimize this. However, no attempt will be made to balance the transistors. It has been found that even with badly unbalanced transistors, common mode signals are not passed by the amplifier.

Fig. 5d shows the equivalent circuit when a difference signal is applied to the transformer coupled circuit. The output is

$$V_{out_s} = -\frac{\alpha V_s R_d Z_b M_{12} S}{\left[r_e + r_b(1-\alpha)\right]\left[(L_2 S + Z_b + Z_d)(R_d + L_3 S + M_{13} S) - 2(M_{12} S)^2\right]}. \tag{4}$$

These results show the vast superiority of the system that uses a transformer rather than a choke as a coupling element. The output signal is somewhat smaller in the latter case than it was before, but this drawback is of little consequence when the advantage gained by the loss of common mode signal is considered.

One problem that must be solved in connection with the transformer is whether to use a long time constant or a short time constant. In the following discussion, it will be assumed that inhibit pulses always come in pairs, one negative and one positive. In the case of a long time constant circuit, the effect of these inhibit pulses will not be bothersome (only insofar as the a.c. coupling is concerned). If a short time constant is used, the inhibits will cause trouble.

In order to understand how various time constants affect recovery, a simplified analysis shows how an inductor shunted by resistance reacts to a square current pulse. Fig. 6 shows the output voltage for three different time constants. It is to be noted that the shorter the time constant is made, the larger the negative overshoot is, but the more rapid is the recovery. However, it is apparent that when the long time constant is used, the circuit is immediately ready to respond almost fully to another positive current pulse. For shorter

time constants, some time must be allowed to elapse before a full output will be obtained.

It is now possible to discuss the various chains of memory outputs that might possibly occur, and to determine how the output is affected by various time constants. In fig. 1, it is observed that the length of time between two successive reads is six microseconds, and that the time between the end of the second inhibit and the beginning of the next read is from 0.5 to 1.0 microseconds.

From Fig. 7 (in which the non-linear operation of the input difference stage is shown), it is noted that due to the fact that pulses are considerably widened by a short time constant circuit, (Fig.7b), it may be difficult to distinguish between a ONE and a ZERO, if the information pulse closely follows an inhibit pulse because the information pulses ride on the overshoot of the inhibit pulse.

If a long time constant circuit is used, (Fig.7c), the overshoots are very small, but the circuit must wait a long time in order to completely recover. The pulses are not deformed, but after a long series of unipolarity pulses, the base line shifts in order that the net area may be zero. The inhibits do not cause any additional trouble, because the net area of a pair of bipolarity inhibit pulses is zero. The base line shift is caused solely by the unipolarity ONEs. The ONEs are present only for 1 microsecond out of a period of 6 microseconds, and so the base line will move not more than 16.6% the height of a ONE. The problem caused by this difficulty can be discussed fairly simply. Assume that a long burst of positive ONEs (the finish of which is shown in Fig.7), have been supplied by the memory. Assume the worst possible case occurs, and that each ONE occupies one microsecond out of the six microsecond cycle time. If all the ONEs were 50 millivolt pulses, the base line at the transformer will have decayed to -8.3 millivolts. The result is that any positive ONE will have a net effective input amplitude of 50-8.3 = 41.7 millivolts. Any negative ZERO, of 10 millivolts amplitude (for example), will display a net effective input amplitude of 10+8.3=18.3 millivolts. Thus, the ratio of signal to noise has decayed from

$$\frac{50}{10} = 5.0, \quad \text{to} \quad \frac{41.7}{18.3} = 2.3.$$

The remainder of the circuit can be designed so as to compensate for this annoyance.

Nothing can be done to rectify the damage caused by a short time constant.

In the actual circuit, a compromise solution was reached and an intermediate time constant was used.

## III The Circuit

The complete circuit diagram is shown in Fig. 8. Although the input stage was discussed in some detail in the previous section, there are several additional remarks that may be made concerning it.

In the input difference stage, large resistors and large power supplies are used in series with the transistors. The result is that slight differences in transistor characteristics do not noticeably alter the quiescent conditions in the circuit. If it is assumed that the two transistors used in the difference stage are identical, then the quiescent circuit may be represented as in Fig. 9.

The equations that describe this system are:

$$300 = I_e(.216+68) + V_{ec} + (I_1+I_e)(33+.216), \text{ and}$$

$$150 = .160\,I_1 + 1.3(I_1+I_b) + (I_1+I_e)(33+.216).$$

These equations may be rewritten as follows:

$$300 + V_{ce} = 101.4\,I_e + 33.2\,I_1 \qquad (5)$$

$$150 - 1.3I_b = 33.2\,I_e + 34.7\,I_1 . \qquad (6)$$

It is reasonable to assume that $V_{ce}$ and $1.3I_b$ are much smaller than 300 and 150 respectively, and they may be neglected. It is then found that $I_e$=2.26 ma and $I_1$=2.18 ma. The collector to base voltage in the quiescent state is $-1.3\,(I_1+I_b)$ volts. Therefore, this voltage is just about -3 volts, and to a very great extent is independent of the transistor that is used. The only contribution that a transistor makes to its own collector-to-base voltage is its base current through a 1.3k resistor with its emitter current at 2.26 ma. Even if $\alpha$ of the transistor is as low as 0.9, the base current is only about 0.2ma, and this is small compared to $I_1$.

Fig. 10, then, shows the quiescent operating point of either of the two input transistors. The collector-to-base voltage is about -3 volts and the emitter current is about 2.26 ma. A variation in transistor characteristics will only result in a change in the base current, and this results in only a slight variation of collector-to-base voltage. Fig. 10 shows that in the neighborhood of the operating point, the transistor characteristics do not vary when the collector voltage is altered.

If the input transistors are identical, and are operated linearly, it is found that the output current is

$$i_{out} = -\frac{V_s\,Z_m\,(\alpha r_c - Z_e)}{[r_b(r_c-\alpha r_e+Z_e+Z_L)+Z_e(r_c+Z_L)][Z_{sw}+Z_m]} \qquad (7)$$

where Vs is the input difference signal; $\frac{1}{Z_{11}} = \frac{1}{2}\left(\frac{1}{R_1} + \frac{1}{R_4} + \frac{1}{Z_{in}}\right)$

(refer to Figs. 3b and 5d) and

$$Z_{in} = r_b + \frac{Z_e(r_c + Z_L)}{r_c(1-\alpha) + Z_e + Z_L} \quad ;$$

Ze is the impedance in the emitter of one transistor; $Z_{SW}$ is the impedance of the sense winding; and $Z_L$ is the equivalent load that a transistor sees. In order to achieve a maximum output, it is noted from equation (7) that minimizing $Z_e$ will be of great benefit. Thus a large capacitor is used to shunt the two 68k resistors that feed the emitters. Because of the need for large capacity and extremely small physical size, it was necessary to use subminiature aluminum electrolytic capacitors. In order to insure uniform operation for positive and negative pulses, it was necessary to use two 5μf capacitors in series, back to back. When the signal is applied, the capacitor is essentially a short circuit, and $Z_e$ reduces to $r_e$. During the quiescent operation the two emitters are isolated from each other, and the current drawn by one does not affect the other.

The impedance that the capacitors face is about

$2\left[r_e + (1.3 + r_b)(1-\alpha)\right]$ kilohms.

It has been found for SBT's that at 2.26 ma of emitter current $r_e \cong 11.5\,\Omega$ and that $r_b \cong 350\,\Omega$. If transistors with $\alpha = 0.95$ are used, then the capacitors see an impedance of about 188 ohms. The time constant then is about 470 microseconds, and this is relatively long. Even if the transistors have α's as high as 0.99, the time constant is 140 μsec, and this is still quite long.

The output impedance of a common emitter transistor stage is about 10 kilohms. So far as a difference signal is concerned, there are 2 of these transistors in series, and they are shunted by the two damping resistors in series. Therefore, the output impedance is

$$\frac{(2\times 10) \times (2\times 6.8)}{(2\times 10) + (2\times 6.8)} = 8.1\ k\Omega$$

The impedance seen past the secondary is either infinite (when the emitter followers are off); or $(\beta_{EF}+1)$ $Z_{in}$ Q104 (where $\beta_{EF}=\beta$ for the on emitter follower) when one of the emitter followers is on, and the following stage, Q104 is still on; or $(\beta_{EF}+1)82k\Omega$, when one of the emitter followers conducts and Q104 is off. The first and last regions (those of very high impedance) last for a long time. The middle region, during which the transformer sees the relatively low impedance

$$(\beta_{EF}+1)\, Z_{in\,Q104} = (\beta_{EF}+1)\left(r_e + r_b(1-\alpha)\right)\Big|_{Q104}$$

lasts only for a very short period of time. Hence, for the major portion of the cycle, the impedance seen by the secondary is very much greater than the output impedance and may be neglected.

Fig. 11 shows a 60 cycle hysteresis loop for the transformer core. This core is manufactured by Arnold Engineering Co., and is a plastic encased, permalloy core, number 5340-S1. The loops shown are a minor loop on which the core operates, and the saturation loop. This data was taken with a single turn on the core.

It was found that no more than about 0.35 ma flowed through the primary of the transformer in the actual circuit when a difference signal was applied (whether the signal was 100 mv or 1.0 volts). Since there are 60 turns, the exciting force is 21 ma-turns. I have, therefore, assumed that the minor loop on which the core operates has a maximum excitation of about 21 ma-turns. The corresponding peak flux was 33.3 Maxwells. Because of the fact that the remanent flux is 30% of the maximum flux, the linearized inductance of the coil with a single turn is

$$L = \frac{1.3\,\phi_m}{I} \times 10^{-8} = \frac{1.3 \times 33.3 \times 10^{-8}}{21 \times 10^{-3}} = 20.6\,\mu h.$$

When 60 turns are used, as in the sense amplifier, the inductance is

$(60)^2 (20.6)\,\mu h = 74\,mh.$

The transformer time constant is $\frac{L}{R} = \frac{74}{8.1}\,\mu sec = 9.2\,\mu sec$. This time is considerably shorter than that of the capacitor circuit, and so the transformer time constant controls the circuit behavior. Apparently from the tests that have been run on this circuit thus far, the time constant is long enough to assure satisfactory performance.

A decrease in the number of turns on the transformer would result in several disadvantages. The signals coupled through to the remainder of the amplifier would be decreased, due to the lessening of the magnetizing inductance. Furthermore, the time constant would be decreased, and this is highly undesirable.

An increase in the number of turns apparently does not aid the circuit operation materially. This may be because of the corresponding increase in wiring capacity shunting the primary and the secondary.

The operation of the remainder of the circuit is fairly straight-forward. The eight emitter followers, (Q3 and Q4), whose bases are connected to the transformers (Fig.8) are biased slightly off. An applied difference signal on one of the four sensing windings results in the application of a pulse to one of the transformers. The base of one of its two transistors rises, and it is further cut-off. However, the other transistor has its base lowered, and if the signal is large enough, this transistor is turned on. The bias level can be adjusted by varying the 50k pot. All eight emitters fall with the one that has been switched. It is seen, therefore, that the memory output that controls the sense amplifier behavior is the largest output, and consequently a ONE will control the sense amplifier even if it is mixed with low level noise.

In this one section of the circuit, the operations of rectification, mixing and slicing have been accomplished. It is found that the sense amplifier output completely switches when the memory plane output varies by 1.1 millivolts. Below this level, there is no output; above it, a full 10 ma pulse.

The transistor Q104 is normally on. When one of the emitter followers is switched on, Q104 goes off. Its collector falls towards -30, turning Q103, which is normally held off, to the saturated state. Its collector rises, turning Q102 and Q100 off. Q102 then saturates Q101. With Q100 off, and Q101 saturated, the circuit output drops to -3 volts.

When the pulse at the input has ended, the cycle is reversed -- Q104 again goes on turning Q103 off. Q102 and Q100 are saturated; Q101 is shut off, and the output rises to ground potential.

Inhibit pulses turn out no larger than ONEs because of the fact that signals are limited by saturation and cutoff.

The resistors in this section of the circuit are chosen so that with minimum acceptable transistors and maximum allowable variation in the undesirable direction of resistance values, the circuit continues to operate satisfactorily.

The operation of the cable driver (consisting of transistors Q100 and Q101) deserves some comment. The cable driver consists of these two transistors connected in series, and the output is taken from the junction of the emitter of Q101 and the collector of Q100. Under standby conditions Q100 is saturated and Q101 is off. The output impedance is very low, and the output level is at ground potential. A pulse at the input to the sense amplifier turns Q100 off, but saturates Q101. (The circuit parameters are adjusted so that when an intermediate sized signal is applied, both Q100 and Q101 are off. If this were not done, it would be possible to saturate both transistors simultaneously, and this would result in the destruction of at least one of the transistors.) Consequently, the output drops to -3 volts, and the output impedance remains at a very low level.

The load that is to be driven is about 50 feet of 160-ohm cable. Because it is not feasible to terminate the cable at the far end, it is necessary to do so at the driving end. Therefore, a 130 ohm resistor is placed in series with the load and the output impedance is probably very close to 160 ohms. The figure of 130 ohms was determined by trying various values of terminations, and choosing that which gave the most satisfactory results.

## IV Results

There is, in this circuit, one result that is both theoretically and actually somewhat disturbing. This is the fact that if the different sensing amplifier input channels (of which there are four per memory plane) are not matched, then their gain characteristics will not be identical. There is only one variable element per sense amplifier - the clipping level potentiometer, R118 (Fig.8), and this cannot possibly be adjusted to satisfy all channels. Suppose the gain of channel A is greater than the gain of channel B, and R118 is set to just pass a 30 millivolt signal applied to channel A. It may then be found that perhaps a 35 mv signal in channel B will be blocked, because it is not amplified as strongly as a signal in A.

In the circuit, this is found to be the case, but it is possible to correct this mistake to a large extent.

In an effort to limit the differences between the various stages, 1% resistors are used exclusively in all channels. With this restriction in force, it is found that the gain of a channel depends upon the characteristics of the transistors and of the transformer used. If a detailed examination was made, it would probably be discovered that the results also depend on the individual resistors in the circuit.

In almost every case of excessive unbalance detected so far, it has been possible to satisfactorily equalize channels by juggling transformers - that is, place strong transformers in weak channels, and vice versa.

The variation of results as the transistors of an input stage are varied, is clearly shown in the following tables of data. In each case the negative voltage signal at the secondary of the transformers is measured for a 50 mv difference input signal. By connecting all four channels in parallel at their inputs, it is ascertained that the same voltage signal is applied to each. Three runs were taken. Sensing amplifier number 9 was used. The results are shown in Table 1.

TABLE 1.

| | Channel | Transistors | α | Negative Output (volts) at transformer Secondary for 50 mv. Input |
|---|---|---|---|---|
| Run 1 | 1 | A108 | 0.962 | 1.28 |
| | | A109 | .950 | |
| | 2 | A81 | .972 | 1.08 |
| | | A75 | .972 | |
| | 3 | A74 | .969 | 1.30 |
| | | A107 | .968 | |
| | 4 | A73 | .956 | 1.35 |
| | | A82 | .962 | |
| Run 2 | 1 | A108 | .962 | 1.35 |
| | | A109 | .950 | |
| | 2 | A81 | .972 | 1.10 |
| | | A75 | .972 | |
| | 3 | 3863 | .919 | 1.25 |
| | | 3866 | .918 | |
| | 4 | 9209 | .979 | 1.30 |
| | | 9215 | .978 | |
| Run 3 | 1 | A81 | .972 | 1.19 |
| | | A75 | .972 | |
| | 2 | A108 | .962 | 1.22 |
| | | A109 | .950 | |
| | 3 | 3863 | .919 | 1.25 |
| | | 3886 | .918 | |
| | 4 | 9209 | .979 | 1.28 |
| | | 9215 | .978 | |

These three runs should not be compared to each other numerically because of the fact that the data were not taken under the same conditions (e.g. the "50 mv" input in run 1 may not have been the same size as the "50 mv" input in run 3). But it is valid, and very interesting, to compare the magnitude obtained within the various runs.

Run 1 demonstrates the fact that the gain of a channel does not vary linearly with the transistor α's. For instance, channel 2

has the strongest transistors, and yet it is the weakest channel; but channel 4, the strongest, has a pair of intermediate gain transistors. It is also noted that channels 1, 3 and 4 are about equivalent.

Run 2 differs from the first run in that channel 3 now has very low $\alpha$ transistors and channel 4 has very high $\alpha$ transistors. It is noted that 3 is weakened just a bit relative to 4. But the really interesting fact is that 4 is weakened relative to 1. This tends to indicate that channel 4 has been significantly weakened when its transistors were replaced by supposedly better transistors. Channel 2 is still the weakest by a good margin.

Run 3 is the same as the second run, except that the transistors in channels 1 and 2 have been interchanged. The result is that the gain of channel 1 has fallen below that of channel 2. This virtually assures us that although transistors A75 and A81 have very high $\alpha$'s, they are poorer than A108 and A109. It also proves that the gain of a channel depends to a large extent upon all of the characteristics of the transistors used, and not merely $\alpha$, as shown in equation (4). That is,

$$V_{out} = -Z \frac{\alpha V_s}{r_e + r_b(1-\alpha)} \qquad (8)$$

It is apparent, therefore that not only $\alpha$, but $r_e$ and $r_b$ are very important parameters in determining the voltage gain of a common emitter transistor amplifier.

Fig. 12 shows the negative pulses at the transformer secondaries corresponding to the conditions of Run 1. This demonstrates that channels 1, 3 and 4 are about equal, while channel 2 is relatively weak.

In passing, it should be pointed out that the pulse size at these points is completely independent of the setting of the clipping level potentiometer. In Fig. 13, the effect of the different gains upon the output pulse is shown. It is observed that the pulse widths at the base of the outputsare as follows:

| | |
|---|---|
| Channel 1 | 0.95μsec |
| Channel 2 | 0.90μsec |
| Channel 3 | 0.99μsec |
| Channel 4 | 0.96μsec |

Run 1 yielded the most widely divergent results, and the complete data from this run is plotted in Fig. 14. From the slopes of these linear curves (they are linear because the signals are not large enough to drive the transistors into non-linear operation), it is observed that the difference in gains between the extreme cases is about 20%.

When the results shown in Fig. 12, 13, and 14 are observed, it is realized that great differences in channel gains do not yield very widely diverging results at the outputs.

It has been found for this circuit that the bias at the emitters of the emitter followers is several hundred millivolts positive. It is observed to a very close approximation, that when the d.c. level of the base voltage drops to ground potential, the corresponding transistor will begin to conduct. Consequently, by use of Fig. 14, it is possible to set the clipping level to any predetermined input level by adjusting R118 to give the proper voltage at the bases of the emitter followers. Because of the different gains achieved in different channels, it will be necessary to accept a compromise solution, however. For instance, assume that it is desired to set the clipping level at 30 mv. Fig.14 shows that, on the average a negative 750 mv pulse is obtained at the transformer secondary when a difference signal of 30 mv is applied at the input. Therefore, the bias point should be adjusted to +750mv. It will then be found that channel 2 will clip at 34 mv, and that channel 4 will clip at 28 mv.

An examination of the transfer characteristics of the complete sensing amplifier (from difference input signal to the output across a 160Ω terminating resistor) leads to the data tabulated below for a nominal clipping level of 30 mv.

This data is for channel 3 of sensing amplifier number 9. The input transistors are A74 and A107.

TABLE 2

| Difference Input Signal mv | Output Voltage Volts | Output Pulse Width μsec | Negative Signal at Transformer Secondary Volts |
|---|---|---|---|
| 100 | 1.55 | 0.95 | -- |
| 90 | 1.55 | 0.92 | -- |
| 80 | 1.55 | 0.86 | -- |
| 70 | 1.55 | 0.82 | -- |
| 60 | 1.55 | 0.77 | -- |
| 50 | 1.55 | 0.67 | -- |
| 40 | 1.55 | 0.50 | -- |
| 30+ | 1.55 | 0.18 | 0.89 |
| 30- | 0 | 0 | 0.86 |
| 20 | 0 | 0 | -- |
| 10 | 0 | 0 | -- |
| 0 | 0 | 0 | -- |

Channel 3 is about the same as channel 4 (Fig.12 and 13) and so the gain from input to transformer secondary is about 27. Thus, in the

active region (around 30 mv of input), the gain of the complete amplifier

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta V_{transformer\ secondary}}{\Delta V_{in}} \times \frac{\Delta V_{out}}{\Delta V_{trans\ sec}} = 27 \times \frac{1.55}{.03} = 1400.$$

That is, in the active region, the amplifier voltage gain is about 1400. Thus, in order to switch the amplifier from no output to full 1.55 volt output, a change of about 1.1 millivolts at the input is required.

These data are plotted in Fig.15. It is noted, that although the pulse height experiences a very sharp cutoff, the output pulse width depends upon the input signal to a very large extent. (The width of the input pulse remains fixed at about 1.0μsec). The reason for this is obvious: as the pulse height is reduced, clipping occurs at higher, and narrower points on the input waveform.

Figures 16 show the pulses obtained at various places in the sensing amplifier when a 50 mv ONE is applied to the input, and Figures 17 show the pulses at the same points when a 20 mv ZERO is applied. It should be noted that in each of these cases, the cycle time is about 4.5 μsec (the length of time between the beginning of the first ONE, and the beginning of the second ONE).

At the input (Fig.16A and B), the ONEs are about 50 mv high and the inhibit pulses are about 800 mv. However, due to the non-linear characteristic of the difference stage, the ONE is amplified more strongly than the inhibit pulse, and the difference signal at the transformer primary consists of 2-volt ONEs, and 6-volt inhibits (Fig.16C). The transformer is a 2 to 1 step down, and consequently the signals at either side of the transformer secondary are about 1 volt and 3 volts, respectively (Fig.16D). (It should be noted that the negative inhibit pulse cannot go far below ground because of the clamping action of the forward biased emitter follower transistor. This accounts for the peculiar shape of the large negative pulse.)

At the emitter follower output (Fig.16E), all pulses are negative. Some portion of the signal at the transformer is lost because the emitter followers are biased off. Hence the ratio of inhibit pulse to ONE signal has been increased. But, as is shown in Fig. 17E, this operation allows for the discrimination against ZEROs.

It is noted that all outputs of Q104 (Fig.16F) - ONEs and inhibits alike - are now the same size. This is caused by the fact that Q104 is turned off even by the small ONE pulse. The notches that are found in this waveform at a level of about $+0.22 - 0.3 \cong -0.1$ volts are caused by the saturation of Q103, the following stage. The output of Q104 is clamped at about -0.4 volts by the conducting base-to-emitter diode of Q103. It is possible for the base to go more negative than the emitter because it is connected directly to the -30 volt supply.

The output of Q103 (Fig.16G) is basically the same as the output of Q104, except that it is greatly amplified, and it is inverted. The pulses are clamped at about ground because when Q103 is saturated its collector-to-emitter voltage is very low, the input to Q102 (Fig.16H) is slightly peaked at its front edge, because the coupling capacitor, C107, is somewhat too large. At any rate, these pulses are large enough to shut Q102 off.

The input to Q100 (Fig.16I) has a slow rise, because its coupling capacitor, C101 is too small. Although this rise time can be greatly improved by adding 100μμf to C101, the affect on the output is unnoticeable. The reason is that Q100 is turned off long before the slow rise takes effect.

The output of Q102 (Fig.16J) (which is fed directly to Q101) is a negative-going square wave that turns Q101 full on. The pulse is able to sink lower than -3 volts because the emitter of Q101 falls to -3 volts, and the base is a little negative relative to the emitter.

The sensing amplifier output (Fig.16K)shows the typical well-defined negative-going 1.55 volt, 10ma pulses that are approximately the same shape for all input pulses that exceed the switching threshold.

Figures 17 show the results obtained when a signal that is below the cutoff level is applied. It is noted that the inhibits appear at the output just as they did in the previous case, but that the information signals are blocked.

Fig.18 demonstrates that the sensing amplifier delay is about 0.3 μsec as measured from the peak of the input pulse to the center point of the output pulse. This result is true, no matter where the clipping level is set, and it is independent of the input pulse amplitude of course.

Fig.19 traces chains of some 1430 unipolarity pulses through the amplifier. These pulses are spaced 6 μsec apart. The points of observation are the same as those used for Figs.16 and 17. It should be noted that the only spot at which there is any prf sensitivity is at the input to the amplifier. The pulse generator is prf sensitive; the sense amplifier obviously is not sensitive at any spot. Fig.19K demonstrates the almost negligible voltage buildup across the emitter-coupling capacitors of the difference stage.

The fact that no common mode signal should appear at the output was discussed earlier in this note. Fig.20 shows the results obtained when a large common signal is applied to the amplifier. With no load, the signal was ±65 volts; the sensing amplifier cut this signal to ±30 volts. There is no output from the amplifier due to either the positive or negative going common signal. The disturbances that are seen at this output (Fig.20B, 20D) are caused by pick-up due to radiation; it is not an output that feeds through the amplifier in the

normal manner. This is proven by the fact that the output obtained for positive and negative common signals are obviously merely the negatives of each other, and that the output amplitude varies directly with the input amplitude. It was found that even if the input transistors were very badly mis-matched, the results are the same. Thus, it would seem as though this amplifier is capable of eliminating common mode signals to a very large extent.

Some time ago D. H. Ellis took data concerning the successful operation of a 256 X 256 magnetic core memory plane as a function of strobe time and bias voltage of the sensing amplifier. This is plotted in Fig. 21. It is to be noted that area of safe and successful operation is the innermost enclosed area (shaded). A ONE fails when the bias is so large that the ONE signal is not passed by the amplifier. A ZERO fails when the bias is so low that the ZERO signal is passed by the amplifier.

A large amount of data has now been accumulated using 20 memory planes and 20 amplifiers. The results, so far as the amplifiers are concerned, have been very gratifying.

The graphs, Fig.22 through 25, show marginal checking data for the sensing amplifier when it drives a load of 50 feet of 160 ohm cable, terminated by 2.2 kilohms in parallel with 47 μμf. The shaded areas show the regions of safe operation. If the supply voltages stray beyond the boundaries shown, it may be expected that either: (1) ZEROs will be passed as ONEs because the amplifier is always in the "switched" condition; or (2) 40 mv ONEs will be blocked because they are not strong enough to switch the amplifier.

Fig.22 shows the plot of the voltage applied to resistor R111 as a function of the voltage applied to the resistors R105 and R107.

Fig.23 shows the variation of the voltage applied to R109 as a function of the voltage applied to R105, R107 and R111.

Fig.24 shows the variation of the voltage applied to R101 as a function of the voltage applied to R105, R107 and R111.

Fig.25 shows the variation of the voltage applied to R108 as a function of the voltage applied to R105, R107 and R111.

In each of these cases a variation of 30% in any voltage cannot possibly cause a failure.

In the actual circuit there are two +150 marginal check voltages. One is applied to R110 and the other to R104 (these resistors are merely decoupling resistors). The -30 volt marginal checking line is applied solely to R109. (See Fig.8) The resistor R104 is connected directly to resistors R105, R107 and R111. Hence, by varying the voltage to R104 and that to R109, a plot that is similar to Fig.23 is obtained.

The other marginal checking voltages (that applied to R110) can be used in two ways: (1) it can be lowered or raised in order to insure that all clipping level potentiometers (R118 and R138) are set to the same value; and (2) it can be used to vary the clipping levels of all amplifiers simultaneously in order to determine which amplifier or plane is weakest.

- - - - - - - - -

It is now intended that this circuit will be used as the sensing amplifier in the TDCM. Because this memory is only 64 X 64, it will only be necessary to employ one input channel. This will ease the restrictions on uniformity of components in the difference stage. There is no difficulty expected with this circuit. There are also several changes of components in the new circuit.

Sydney Bradspies

SB:rs

Sydney Bradspies

Drawings:

| | | | |
|---|---|---|---|
| Fig. 1 | A-68254 | Fig.14 | A-68508 |
| Fig. 2 | B-68255 | Fig.15 | A-68473 |
| Fig. 3 | B-68256 | Fig.16 | B-68402 |
| Fig. 4 | A-66352-1 | Fig.17 | B-68403 |
| Fig. 5 | C-68401 | Fig.18 | A-68262 |
| Fig. 6 | A-68531 | Fig.19 | B-68645 |
| Fig. 7 | B-68846 | Fig.20 | A-68593 |
| Fig. 8 | D-65501-1 | Fig.21 | A-68644 |
| Fig. 9 | A-68426 | Fig.22 | A-68717 |
| Fig.10 | A-68847 | Fig.23 | B-68719 |
| Fig.11 | A-68253 | Fig.24 | A-68718 |
| Fig.12 | B-68252 | Fig.25 | B-68720 |
| Fig.13 | A-68592 | | |

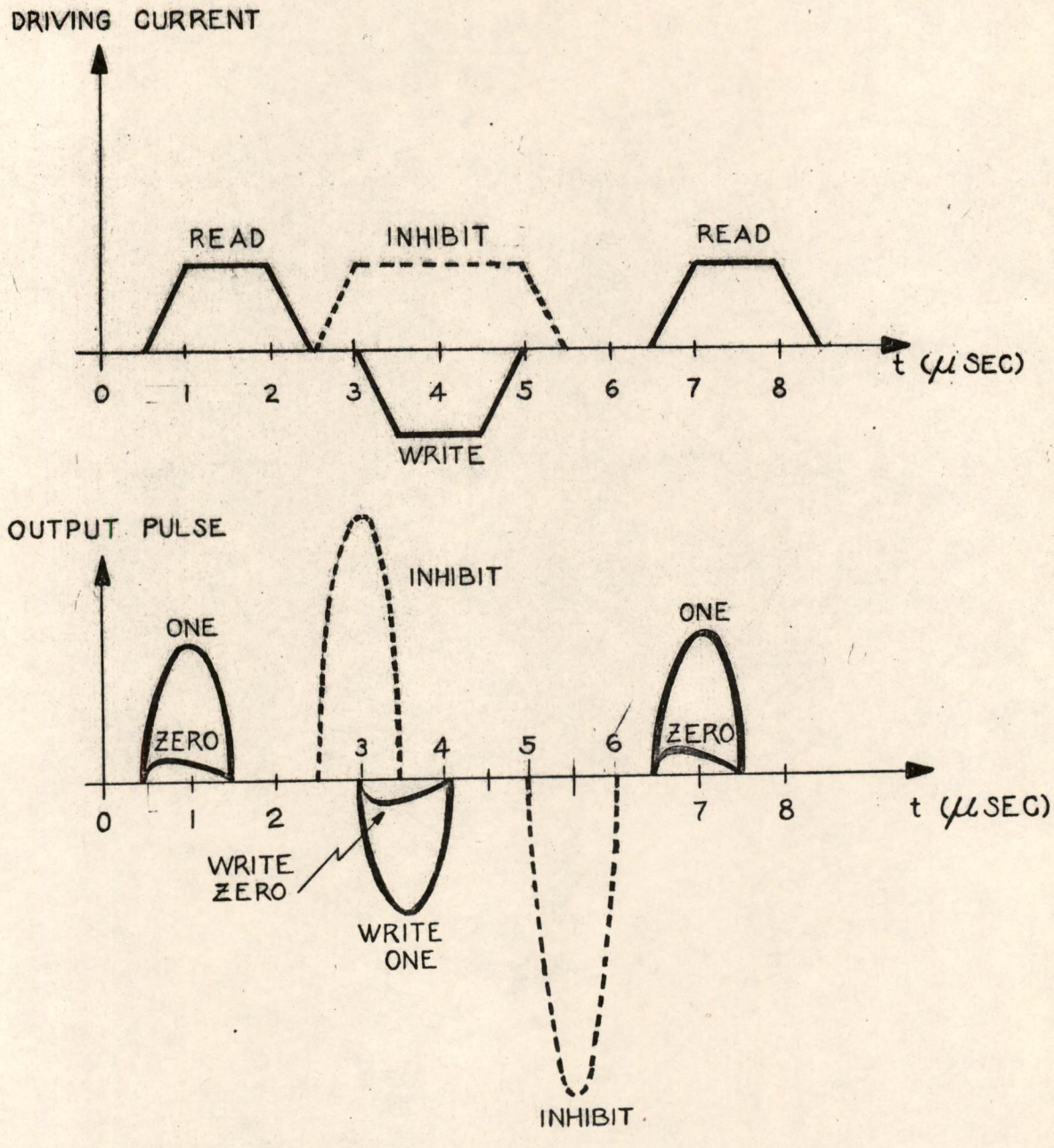
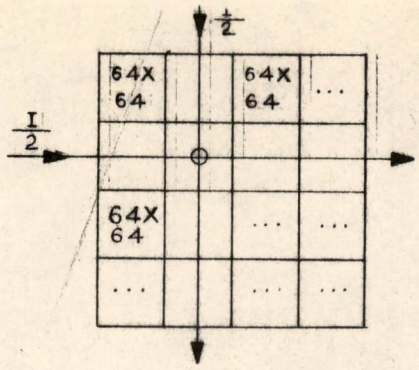


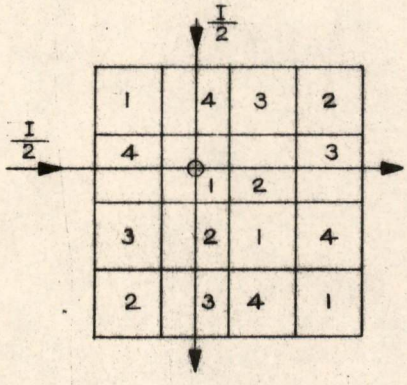

FIG. 1

DRIVING CURRENTS AND OUTPUT PULSES FOR MEMORY PLANES

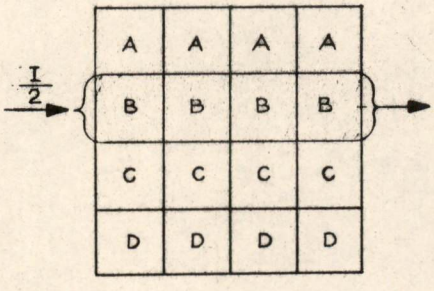
A-68254




a) PLANE CONNECTED WITH SINGLE SENSE WINDING AND SINGLE DIGIT WINDING



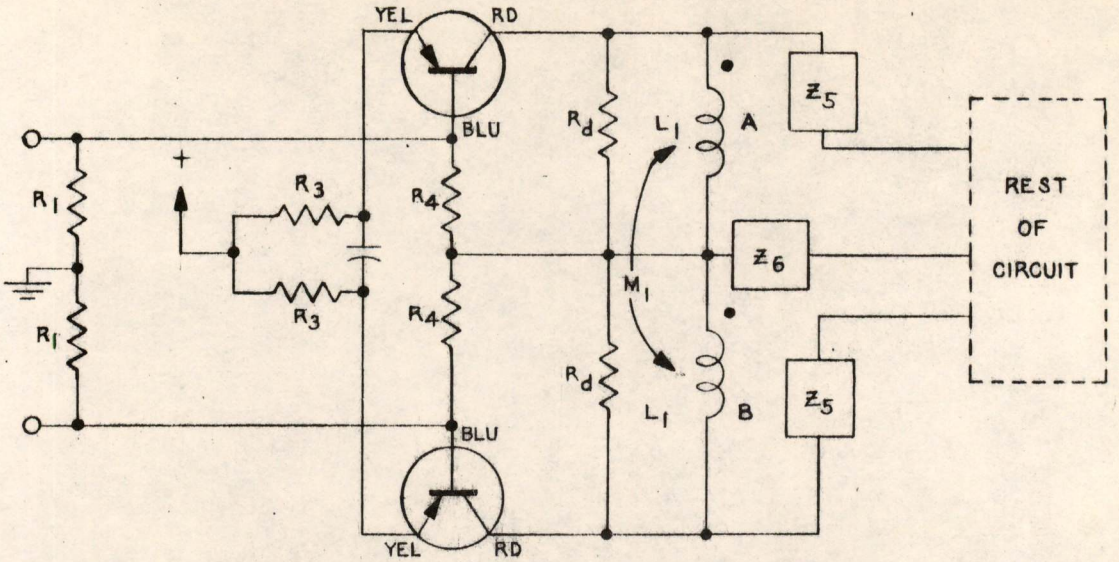

b) METHOD OF CONNECTING FROM SENSE WINDINGS – 1, 2, 3, AND 4 – SO AS TO MINIMIZE NOISE CONTRIBUTIONS OF PARTIALLY SELECTED CORES



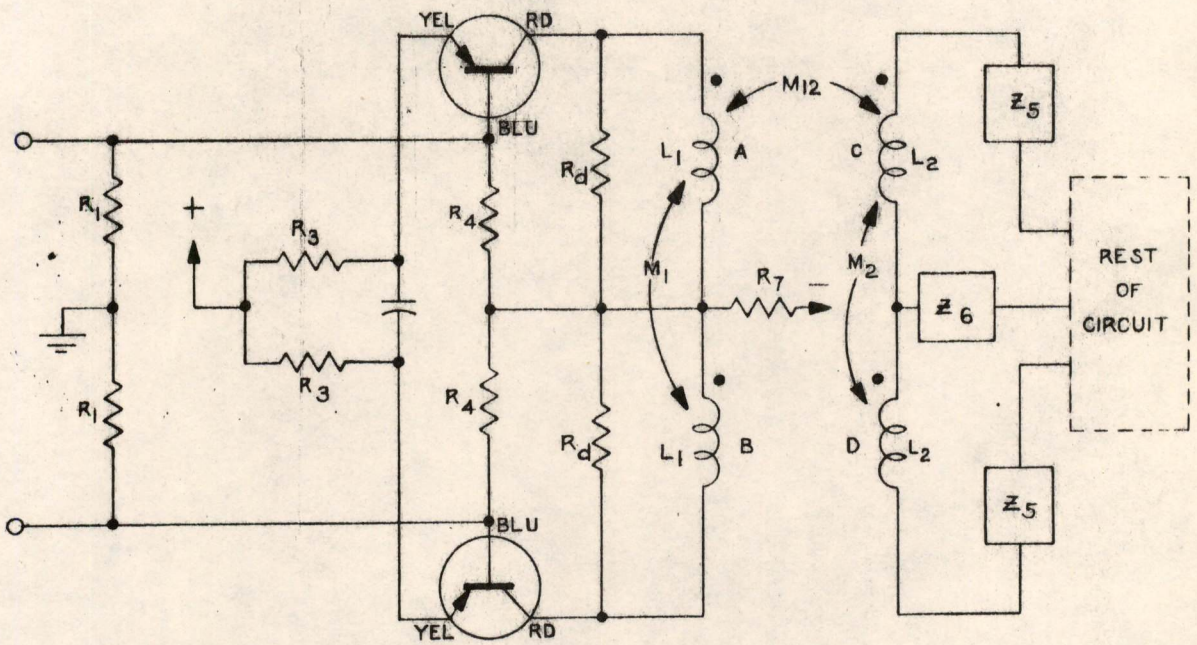

c) METHOD OF CONNECTING FOUR DIGIT WINDINGS – A, B, C AND D.

FIG. 2

256 × 256 PLANE BROKEN INTO 16 64 × 64 MODULES, WITH SENSING WINDING AND DIGIT PLANE WINDING CONNECTED IN VARIOUS WAYS.




a) CHOKE COUPLING



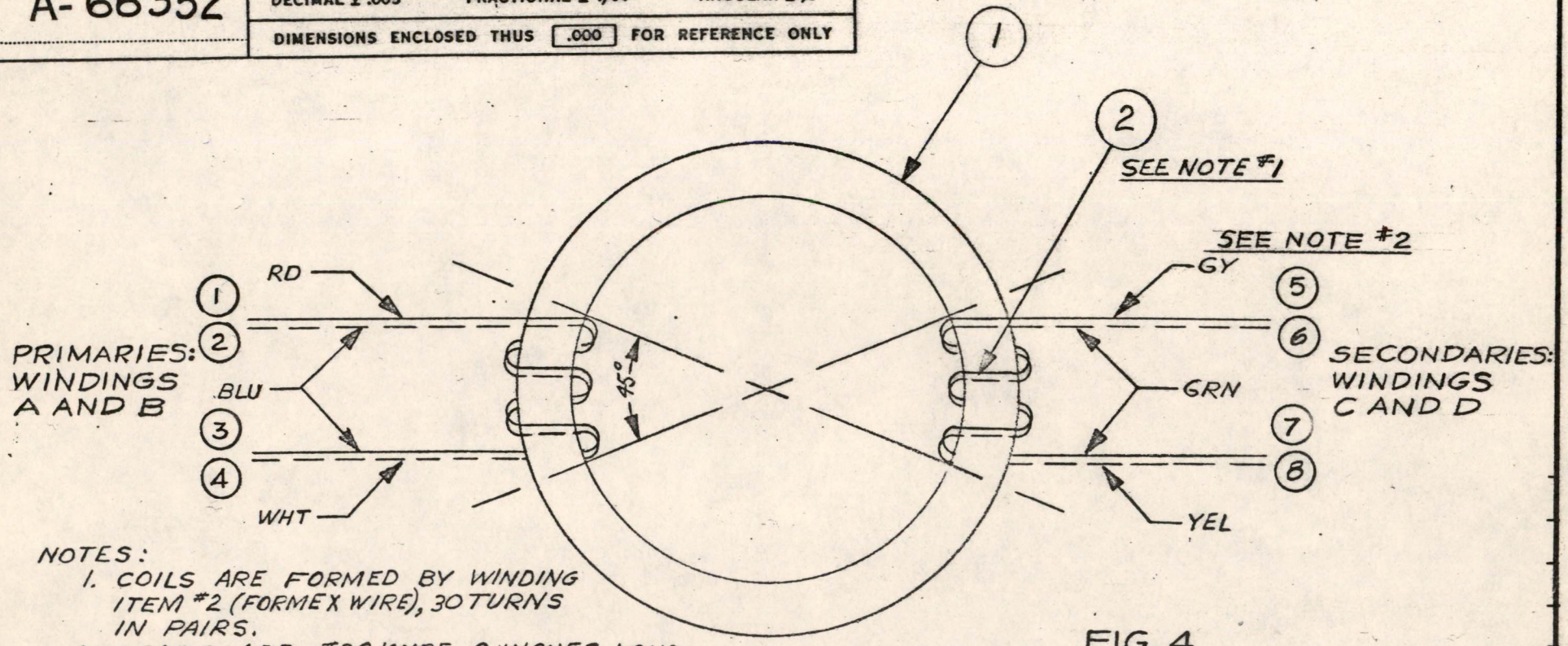

b) TRANSFORMER COUPLING

FIG. 3

TWO METHODS OF COUPLING FROM INPUT DIFFERENCE AMPLIFIER TO REMAINDER OF CIRCUIT

B-68256

| A-66352 | TOLERANCES NOT OTHERWISE SPECIFIED<br>DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°<br>DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY |
|---|---|




NOTES:
1. COILS ARE FORMED BY WINDING ITEM #2 (FORMEX WIRE), 30 TURNS IN PAIRS.
2. LEADS ARE #20 WIRE 2 INCHES LONG IN SPECIFIED COLORS.

FIG. 4
METHOD OF WINDING TRANSFORMER FOR CIRCUIT PICTURED IN FIG. 3b

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: Prei DATE: 19 6 56

| ITEM | MATERIAL - DESCRIPTION | PART NO. | QTY. |
|---|---|---|---|
| 2 | FORMEX MAGNET WIRE, #32 AWG G.E. | | AS REQD |
| 1 | PERMALLOY CORE PLASTIC ENCASED ARNOLD ENGINEERING CO. | 5340-SI | 1 |

| CHG. | CN# | DATE | APPD. |
|---|---|---|---|
| -1 | 8354 | 11-28-56 | 83 |

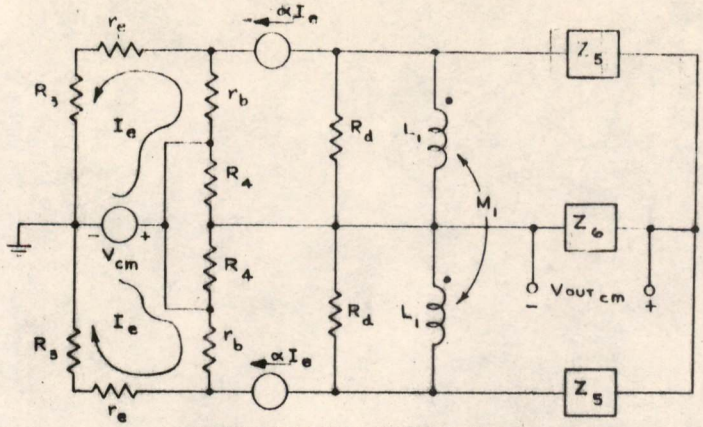
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

TRANSFORMER, SENSING AMPLIFIER

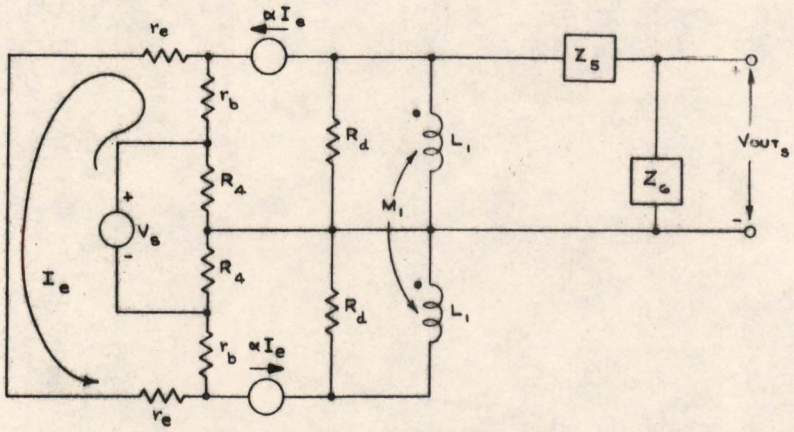
SCALE: NONE DR. A.D. Annetti 5-28-56
ENG. 6-5-56 CK. 6/5/56 APPD.

A-66352

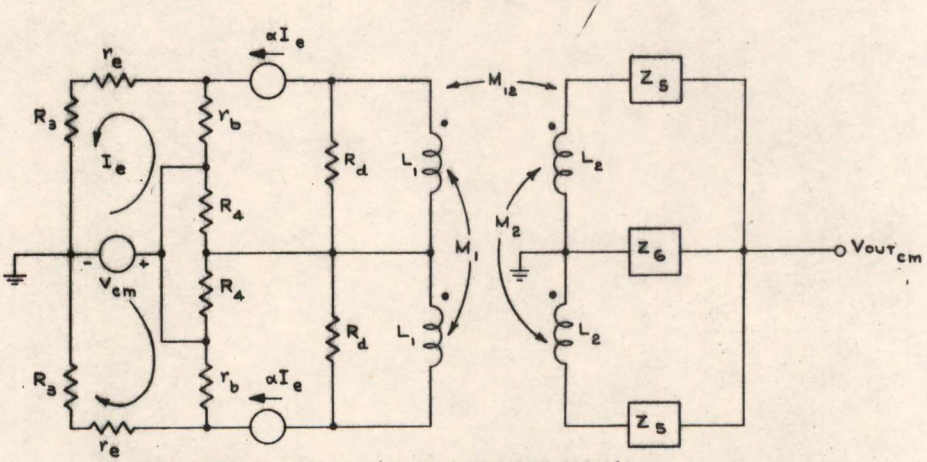
8M-7-54-Boston Blue Print



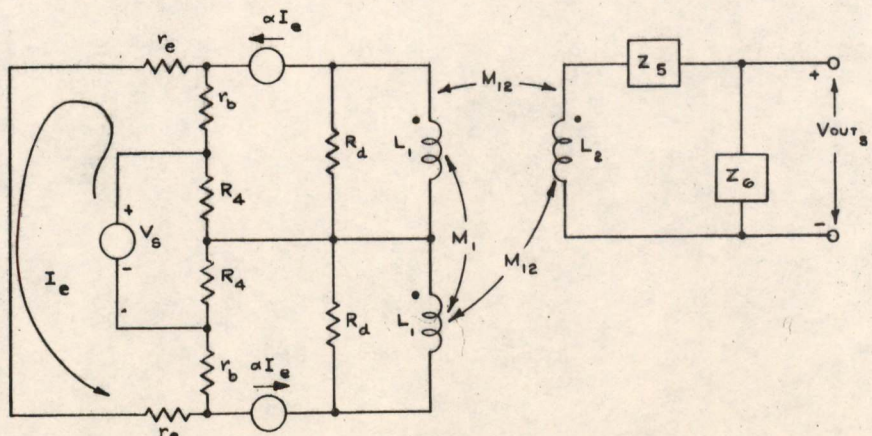

a. CHOKE COUPLING, COMMON MODE SIGNAL




b. CHOKE COUPLING, DIFFERENCE SIGNAL




c. TRANSFORMER COUPLING, COMMON MODE SIGNAL.




d. TRANSFORMER COUPLING, DIFFERENCE SIGNAL

FIG. 5

LINEARIZED AND BALANCED EQUIVALENT CIRCUITS FOR FIG. 3

C-68401

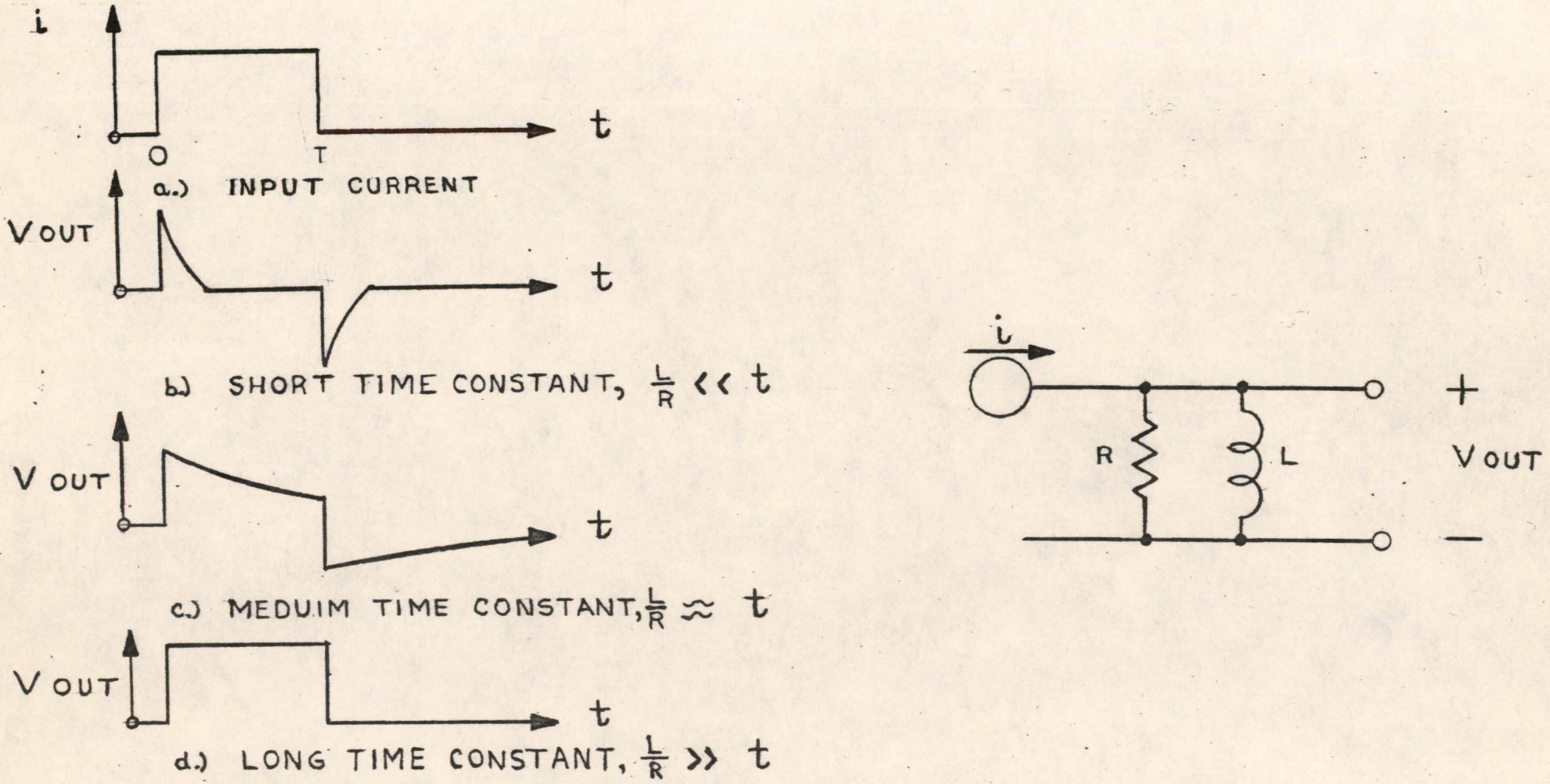
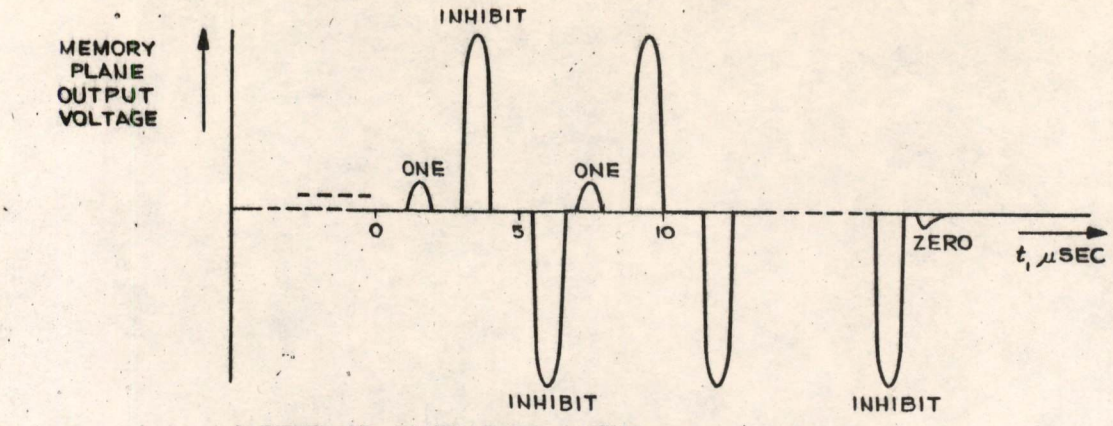
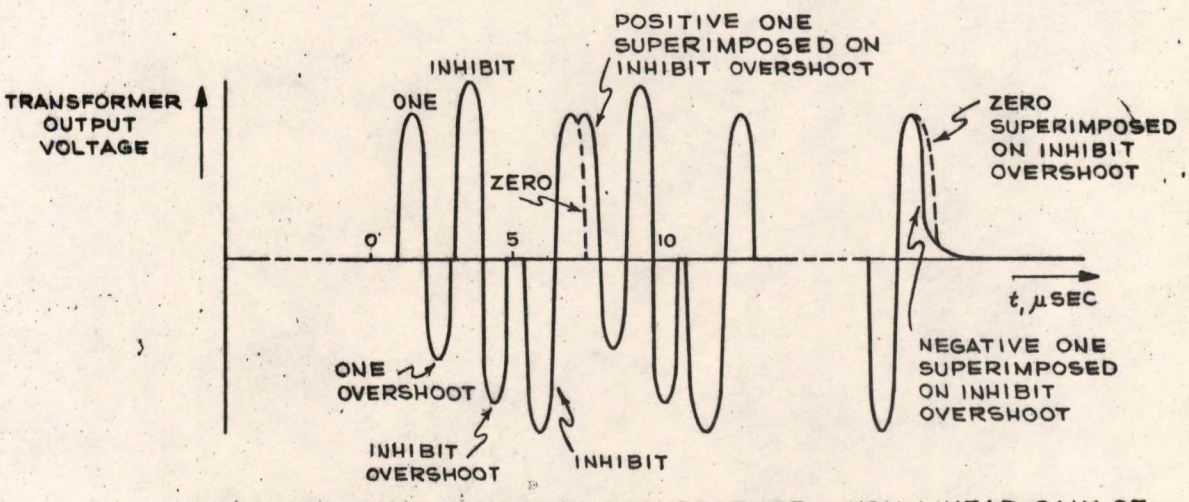



FIG 6

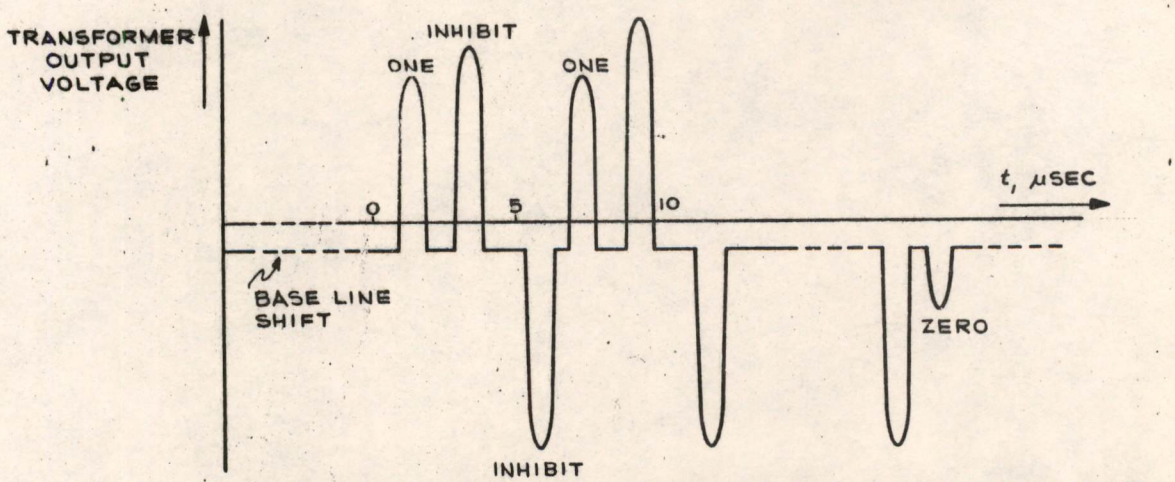
OUTPUTS OBTAINED FOR VARIOUS TIME CONSTANTS WHEN CURRENT SOURCE FEEDS PARALLEL RL CIRCUIT




a) SENSING AMPLIFIER INPUT




b) SHORT TIME CONSTANT TRANSFORMER – NON-LINEAR GAIN OF INPUT STAGE EXPLAINS GROWTH OF ONE's RELATIVE TO INHIBITS

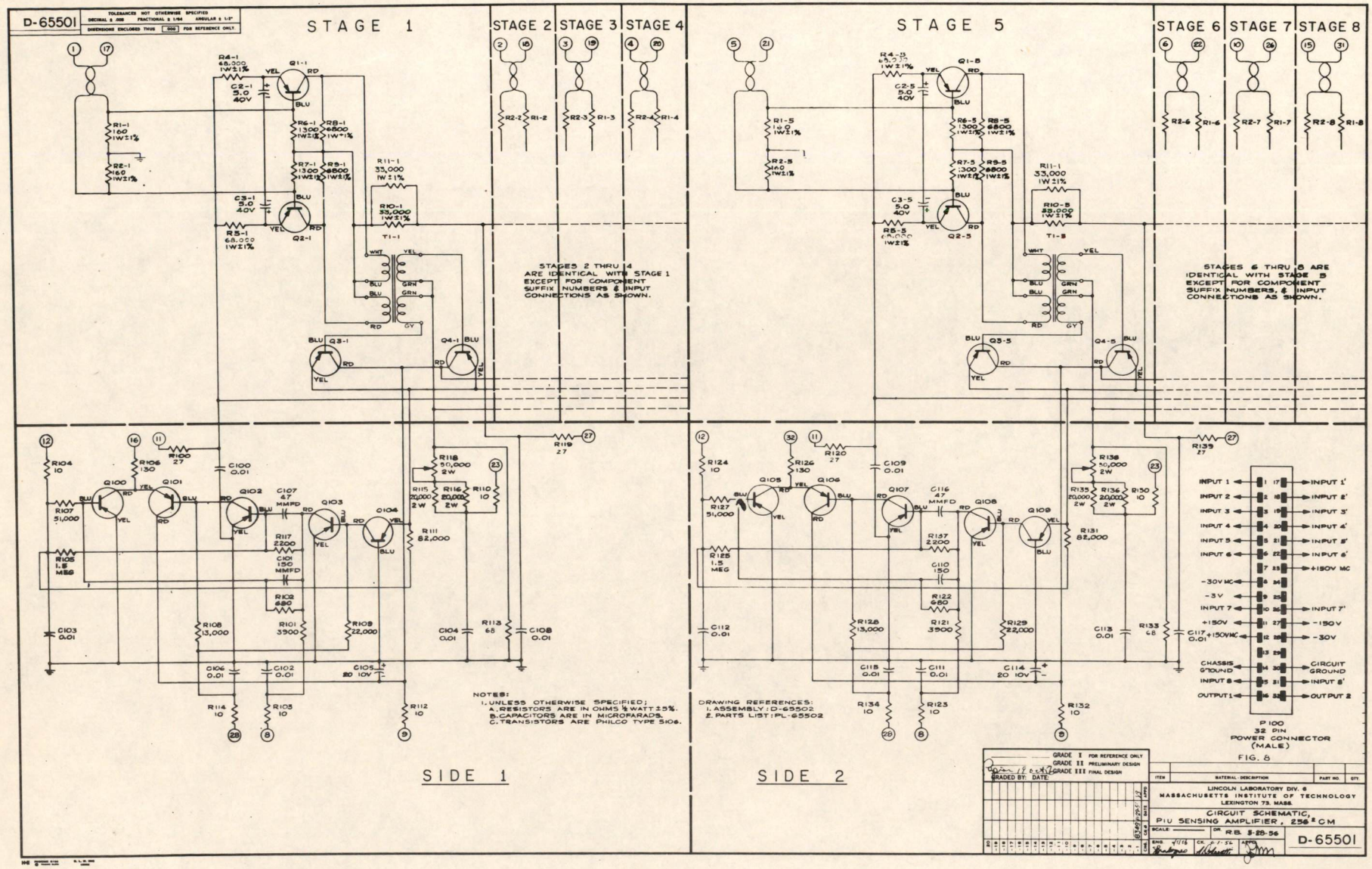



c) LONG TIME CONSTANT TRANSFORMER – NON-LINEAR GAIN OF INPUT STAGE EXPLAINS GROWTH OF ONE's RELATIVE TO INHIBITS

FIG. 7

EFFCTS CAUSED BY A CHAIN OF UNIPOLARITY (POSITIVE) ONE's, INTERSPERSED WITH INHIBIT PULSES. THESE SHOW DIFFICULTIES THAT ARE ENCOUNTERED BOTH WITH SHORT AND LONG TIME CONSTANT TRANSFORMERS.

B-6846


D-65501
STAGE 1
STAGE 2
STAGE 3
STAGE 4
STAGE 5
STAGE 6
STAGE 7
STAGE 8
STAGES 2 THRU 4 ARE IDENTICAL WITH STAGE 1 EXCEPT FOR COMPONENT SUFFIX NUMBERS & INPUT CONNECTIONS AS SHOWN.
STAGES 6 THRU 8 ARE IDENTICAL WITH STAGE 5 EXCEPT FOR COMPONENT SUFFIX NUMBERS, & INPUT CONNECTIONS AS SHOWN.
NOTES:
1. UNLESS OTHERWISE SPECIFIED;
A. RESISTORS ARE IN OHMS & WATT ±5%.
B. CAPACITORS ARE IN MICROFARADS.
C. TRANSISTORS ARE PHILCO TYPE 5106.
DRAWING REFERENCES:
1. ASSEMBLY: D-65502
2. PARTS LIST: PL-65502
INPUT 1
INPUT 2
INPUT 3
INPUT 4
INPUT 5
INPUT 6
+150V MC
-30V MC
-3V
INPUT 7
+150V
+150VMC
-150V
-30V
CHASSIS GROUND
CIRCUIT GROUND
INPUT 8
OUTPUT 1
OUTPUT 2
P 100
32 PIN
POWER CONNECTOR
(MALE)
SIDE 1
SIDE 2
FIG. 8
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.
CIRCUIT SCHEMATIC,
PIU SENSING AMPLIFIER, 256 ² CM
D-65501

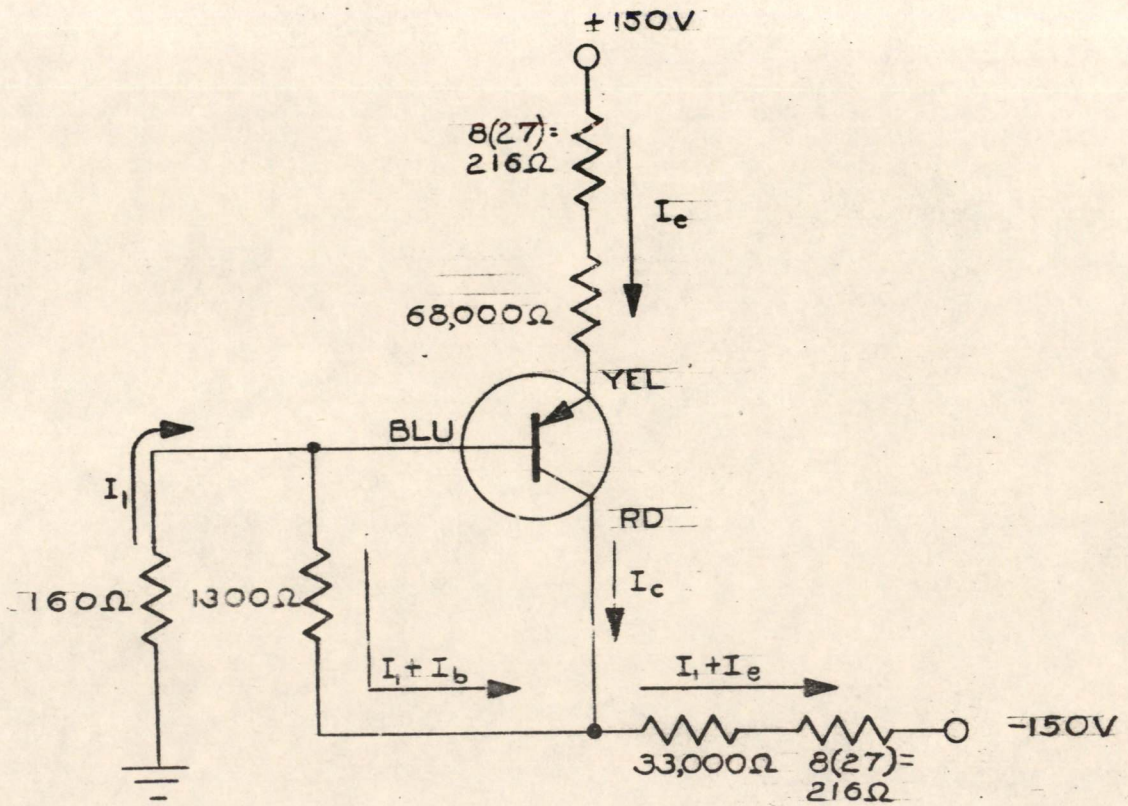



FIG. 9

D.C. OPERATION OF DIFFERENCE STAGE,
ASSUMING THAT INPUT TRANSISTORS ARE IDENTICAL

TRANSISTOR #48 BY M. PETERSON - DEC. 1954

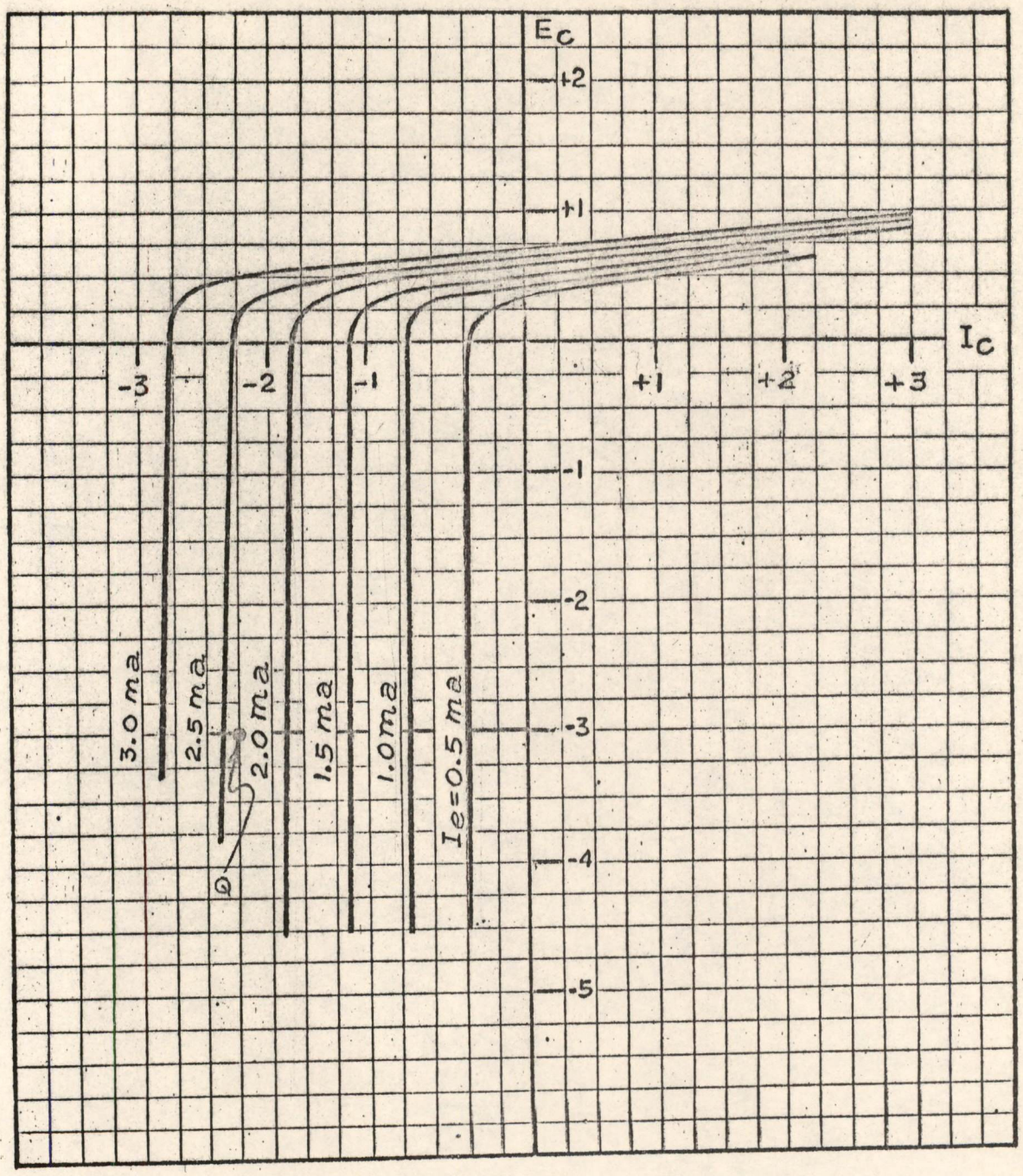
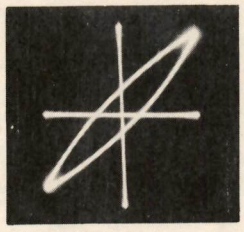



FIG. 10

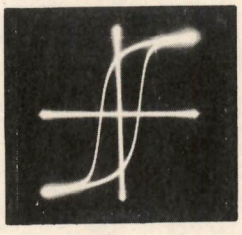
OPERATING POINT
OF DIFFERENCE STAGE TRANSISTORS AT Q

TYPICAL SBT CHARACTERISTICS GROUNDED BASE
$I_C$ vs $E_C$

A-68847



DRIVING CURRENT = 21 ma
MAXIMUM FLUX = 33.3 maxwells



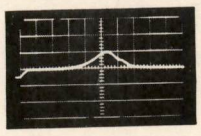
SATURATION LOOP
DRIVING CURRENT = 500 ma
SATURATION FLUX = 560 maxwells

FIG. 11

60 CYCLE HYSTERESIS LOOP OF TRANSFORMER CORE-PLASTIC ENCASED, PERMALLOY CORE, NUMBER 5340-SI MANUFACTURED BY ARNOLD ENGINEERING CO. ONE TURN (N=1) IS USED.

A-68253

INPUT DIFFERENCE SIGNAL

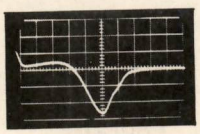


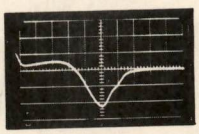
50 mV/cm

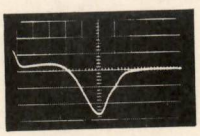
0.5 μSEC/cm

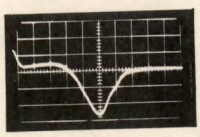
TRANSFORMER SECONDARIES

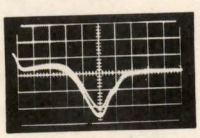
| | DIFFERENCE STAGE TRANSISTOR | α |
|---|---|---|
| CHANNEL 1 | A108 | 0.962 |
| | A109 | 0.950 |
| CHANNEL 2 | A81 | 0.972 |
| | A75 | 0.972 |
| CHANNEL 3 | A74 | 0.969 |
| | A107 | 0.968 |
| CHANNEL 4 | A73 | 0.956 |
| | A82 | 0.962 |











COMPOSITE OF FOUR CHANNELS

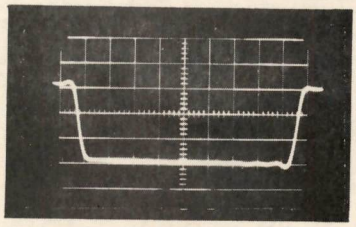
500 mV/cm

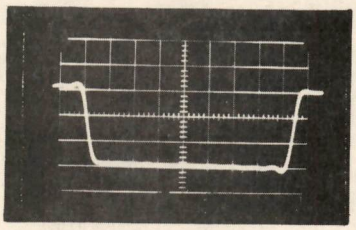
0.5 μSEC/cm

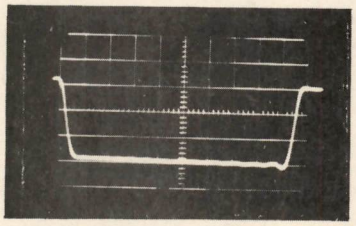
FIG 12

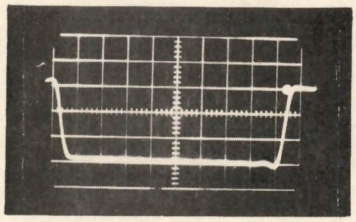
NEGATIVE PULSES AT TRANSFORMER SECONDARIES WHEN ALL INPUTS ARE CONNECTED IN PARALLEL. THIS SHOWS EFFECT OF DIFFERENT GAINS IN VARIOUS CHANNELS UPON THE SIZES OF PULSES APPLIED TO EMITTER FOLLOWERS. SENSING AMPLIFIER #9

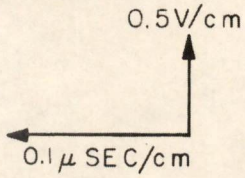
B-68252












| | DIFFERENCE STAGE TRANSISTORS | α |
|---|---|---|
| CHANNEL 1 | A108 | 0.962 |
| | A109 | 0.950 |
| CHANNEL 2 | A81 | 0.972 |
| | A75 | 0.972 |
| CHANNEL 3 | A74 | 0.969 |
| | A107 | 0.968 |
| CHANNEL 4 | A73 | 0.956 |
| | A82 | 0.962 |

FIG. 13

OUTPUT PULSES FROM DIFFERENT CHANNELS OF SENSING AMPLIFIER #9 FOR 50mV INPUT PULSES. THIS DEMONSTRATES THE EFFECT OF UNEQUAL GAINS IN DIFFERENT CHANNELS. RESISTIVE LOAD = 160Ω

A-68592

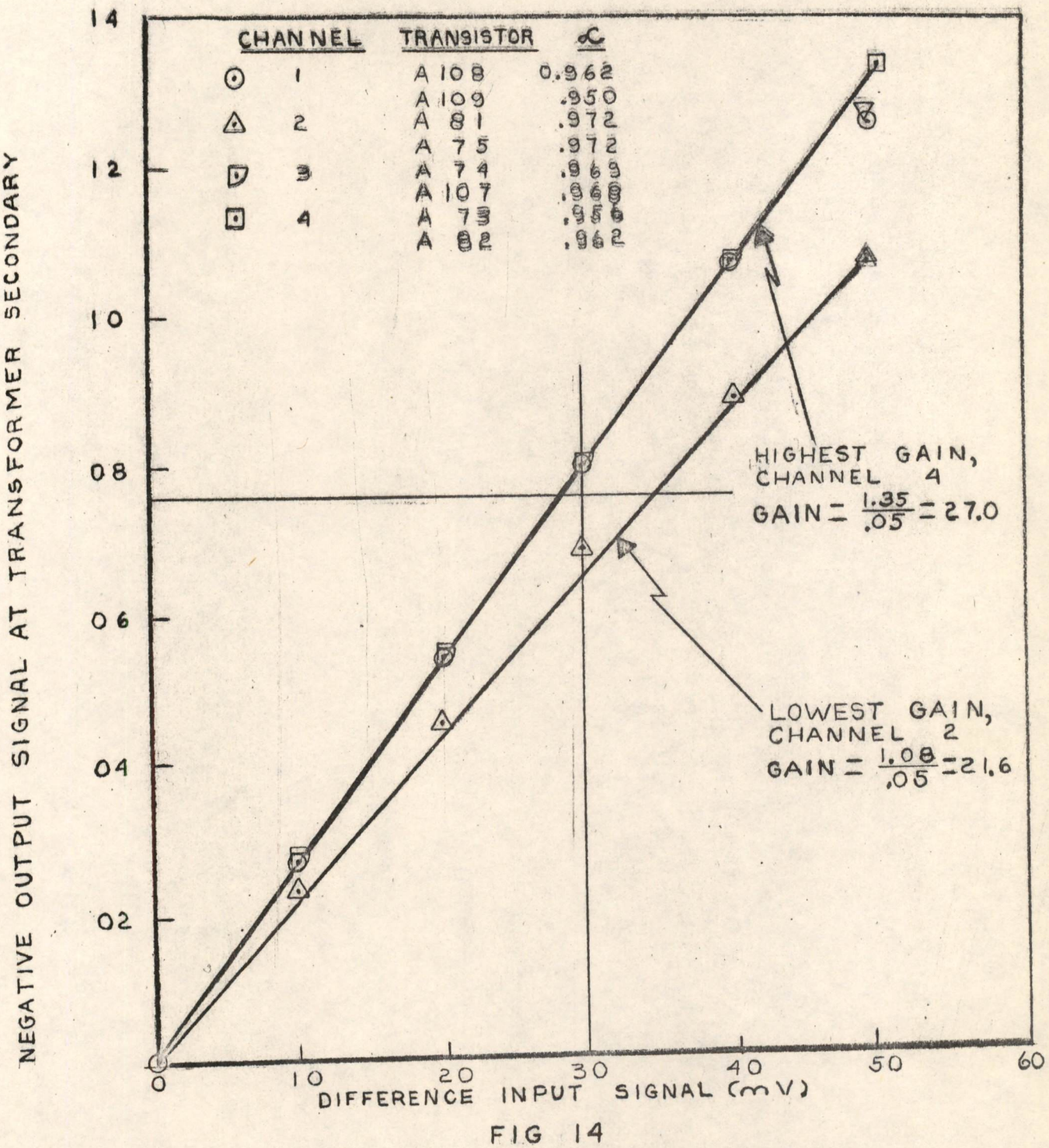



FIG 14

NEGATIVE SIGNAL AT TRANSFORMER SECONDARY AS A FUNCTION OF DIFFERENCE INPUT SIGNAL FOR THE DATA OF RUN 1

SENSING AMPLIFIER#9

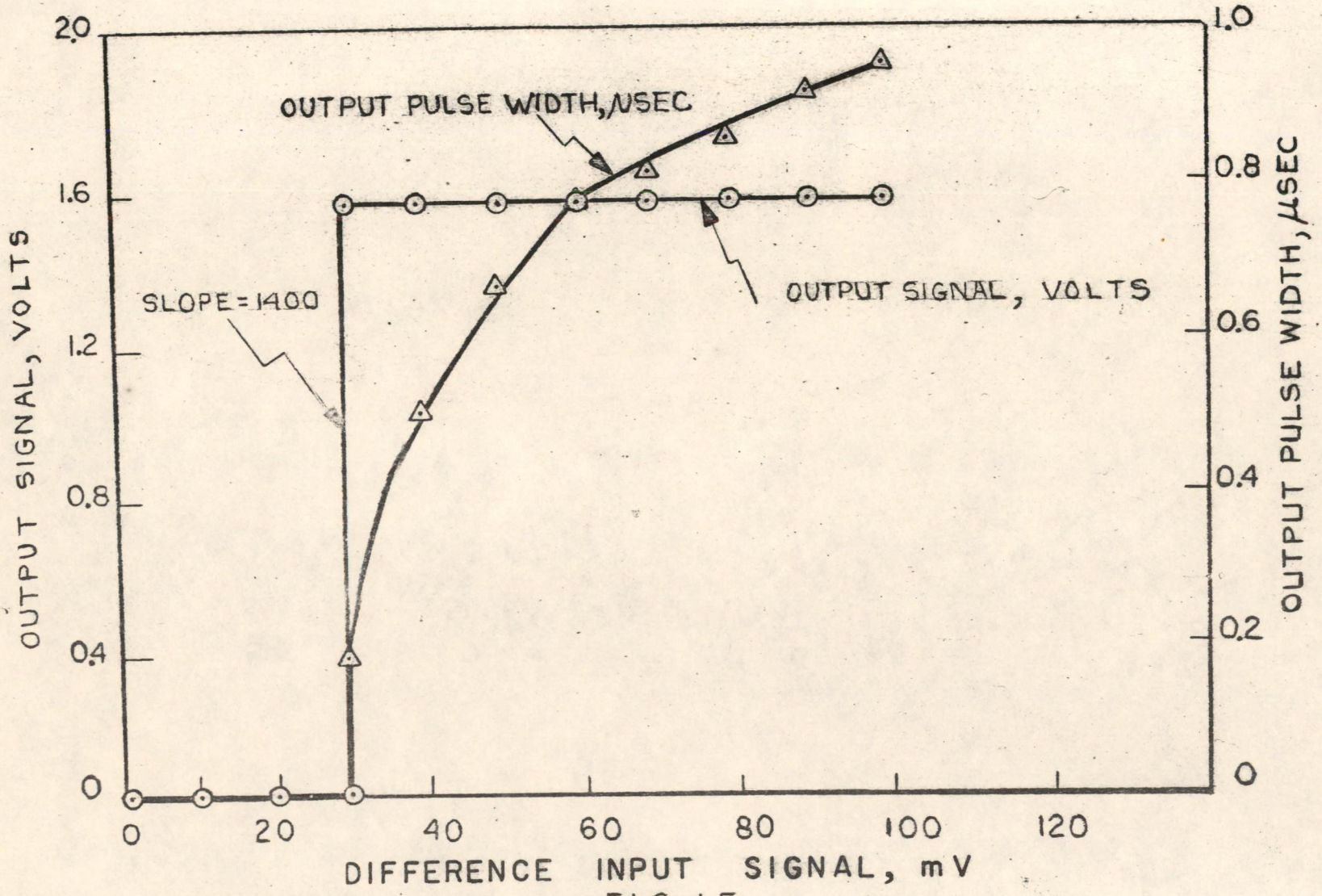
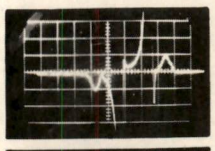



FIG. 15

TRANSFER CHARACTERISTIC OF TYPICAL SENSING AMPLIFIER

RESISTIVE LOAD = 160 Ω

SENSING AMPLIFIER # 9, CHANNEL 3



A. INPUT DIFFERENCE SIGNAL

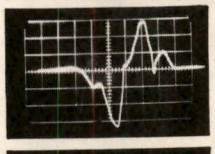
50 mV/cm

1.0 μSEC/cm

B. INPUT DIFFERENCE SIGNAL

500mV/cm

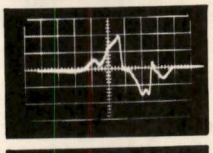
1.0 μSEC/cm



C. DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

2V/cm

1.0 μSEC/cm



D. SIGNAL AT ONE SIDE OF TRANSFORMER SECONDARY (D.C. LEVEL = +0.73 VOLTS)

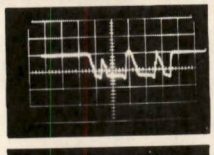
2V/cm

1.0 μSEC/cm

E. SIGNAL AT EMITTER FOLLOWER OUTPUT (D.C. LEVEL = +0.25 VOLTS)

1V/cm

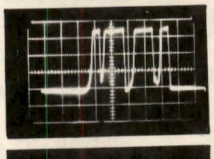
1.0 μSEC/cm



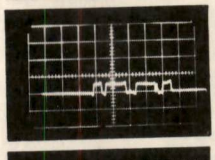
F. OUTPUT OF Q104 (D.C. LEVEL = +0.22 VOLTS)

500mV/cm

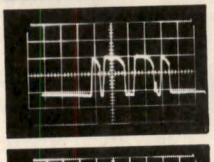
1.0 μSEC/cm



G. OUTPUT OF Q103 (D.C. LEVEL = -3.6 VOLTS)



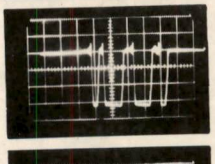
H. INPUT TO Q102 (D.C. LEVEL = -0.40 VOLTS)



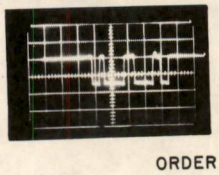
I. INPUT TO Q100 (D.C. LEVEL = -0.43 VOLTS)

1V/cm

1.0 μSEC/cm



J. OUTPUT OF Q102 (D.C. LEVEL = -0.04 VOLTS)



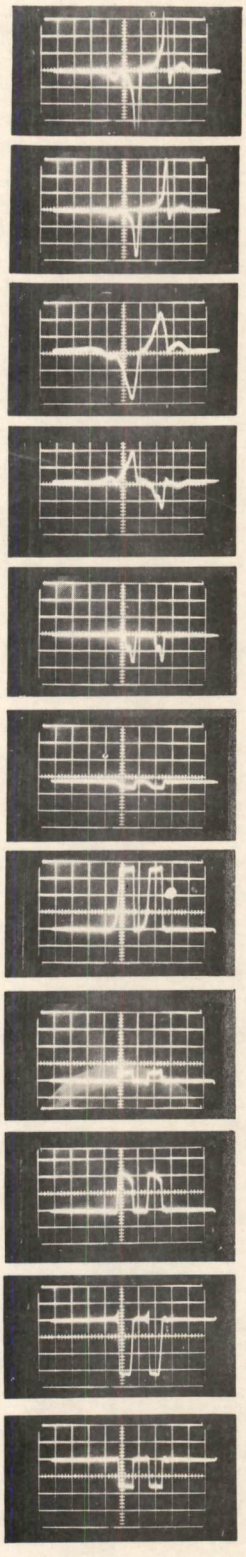
K. SENSE AMPLIFIER OUTPUT, ACROSS 160Ω (D.C. LEVEL = GROUND)

ORDER OF PULSES IS ONE, INHIBIT, INHIBIT, ONE

FIG. 16

TRACE SIGNAL THROUGH CIRCUIT.
INPUT ONE IS 50mV IN AMPLITUDE. CLIPPING LEVEL IS SET AT 30mV.
SENSE AMPLIFIER #9, CHANNEL 3. CYCLE TIME ≅ 4.5 μSEC. RESISTIVE LOAD = 160Ω.

B-68402



A. INPUT DIFFERENCE SIGNAL

50 mV/cm
1.0 μSEC/cm

B. INPUT DIFFERENCE SIGNAL

100 mV/cm
1.0 μSEC/cm

C. DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

2 V/cm
1.0 μSEC/cm

D. SIGNAL AT ONE SIDE OF TRANSFORMER SECONDARY (D.C. LEVEL = +0.73 VOLTS)

2 V/cm
1.0 μSEC/cm

E. SIGNAL AT EMITTER FOLLOWER OUTPUT (D.C. LEVEL = +0.25 VOLTS)

1 V/cm
1.0 μSEC/cm

F. OUTPUT OF Q104 (D.C. LEVEL = +0.22 VOLTS)

500 mV/cm
1.0 μSEC/cm

G. OUTPUT OF Q103 (D.C. LEVEL = -3.6 VOLTS)

H. INPUT TO Q102 (D.C. LEVEL = -0.40 VOLTS)

I. INPUT TO Q100 (D.C. LEVEL = -0.43 VOLTS)

J. OUTPUT OF Q102 (D.C. LEVEL = -0.04 VOLTS)

K. SENSE AMPLIFIER OUTPUT, ACROSS 160Ω (D.C. LEVEL = GROUND)

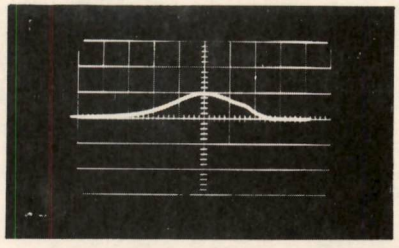
1 V/cm
1.0 μSEC/cm

ORDER OF PULSES IS ZERO, INHIBIT, INHIBIT, ZERO

FIG. 17

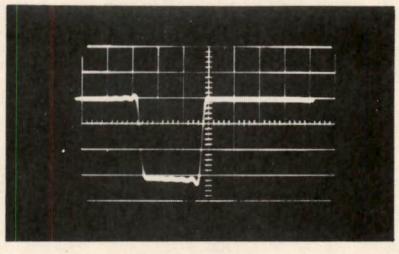
TRACE SIGNAL THROUGH CIRCUIT,
INPUT ZERO IS 20mV IN AMPLITUDE. CLIPPING LEVEL IS SET AT 30 mV.
SENSE AMPLIFIER #9, CHANNEL 3. CYCLE TIME ≅ 4.5 μSEC. RESISTIVE LOAD = 160Ω

B-68403



DIFFERENCE INPUT
50 mV/cm

0.2 μSEC/cm



OUTPUT ACROSS 160Ω
500 mV/cm

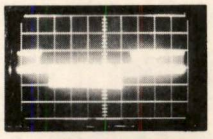
0.2 μ SEC/cm

FIG 18

THE DELAY OF A PULSE PASSING THROUGH THE SENSING AMPLIFIER

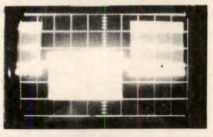
SENSING AMPLIFIER # 9, CHANNEL 3. CLIPPING LEVEL ≅ 30mV. DELAY ≅ 0.3 μ SEC. RESISTIVE LOAD = 160 Ω

A 68262



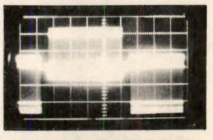
a) DIFFERENCE INPUT SIGNALS

50mV/cm
2000 μSEC/cm



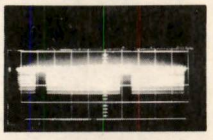
b) DIFFERENCE SIGNAL AT TRANSFORMER PRIMARY

1V/cm
2000 μSEC/cm



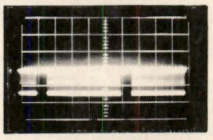
c) SIGNALS AT ONE SIDE OF TRANSFORMER SECONDARY

500mV/cm
2000 μSEC/cm



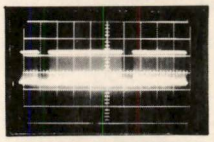
d) SIGNALS AT EMITTER FOLLOWER OUTPUT

500mV/cm
2000 μSEC/cm



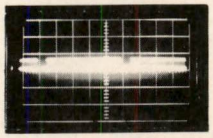
e) OUTPUT OF Q104

500mV/cm
2000 μSEC/cm



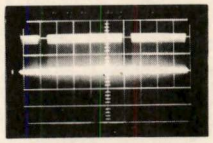
f) OUTPUT OF Q103

2V/cm
2000 μSEC/cm



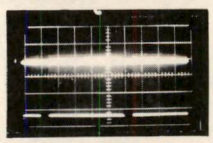
g) INPUT TO Q102

1V/cm
2000 μSEC/cm



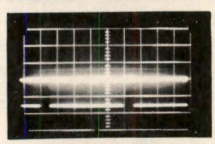
h) INPUT TO Q100

1V/cm
2000 μSEC/cm



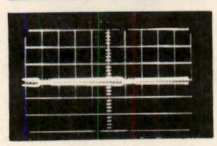
i) OUTPUT OF Q102

1V/cm
2000 μSEC/cm



j) SENSING AMPLIFIER OUTPUT, ACROSS 160Ω

1V/cm
2000 μSEC/cm



k) DIFFERENCE SIGNAL ACROSS CAPACITORS C2-3 AND C3-3 AT THE INPUT

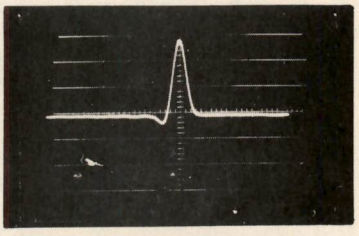
50mV/cm
2000 μSEC/cm

FIG. 19

BURST TEST FOR DETERMINING PRF SENSITIVITY OF SENSING AMPLIFIER. INPUT PULSES ARE SPACED 6μSEC APART

UNIPOLARITY CHAINS LAST FOR 8,600 μSEC. CHAINS CONSIST OF ABOUT 1430 PULSES. SENSING AMPLIFIER # 9, CHANNEL 3. CHIPPING LEVEL ≅ 30mV. RESISTIVE LOAD 160Ω

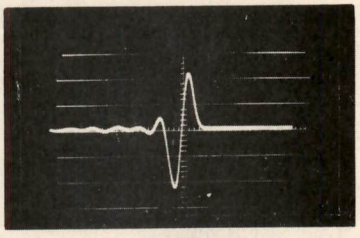
B-68645



a) POSITIVE COMMON MODE INPUT SIGNAL

10V/cm

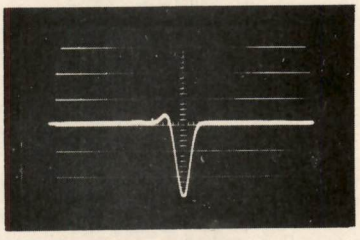
0.1μ SEC/cm



b) OUTPUT OF CHANNEL 3

2V/cm

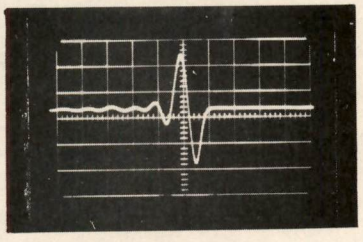
0.1μ SEC/cm



c) NEGATIVE COMMON MODE INPUT SIGNAL

10V/cm

0.1μ SEC/cm



d) OUTPUT OF CHANNEL 3

2V/cm

0.1μ SEC/cm

FIG. 20

EFFECT OF LARGE COMMON MODE SIGNAL

UPON THE SENSING AMPLIFIER OUTPUT

AMPLIFIER #9, CHANNEL 3. RESISTIVE LOAD = 160 Ω

A-68593

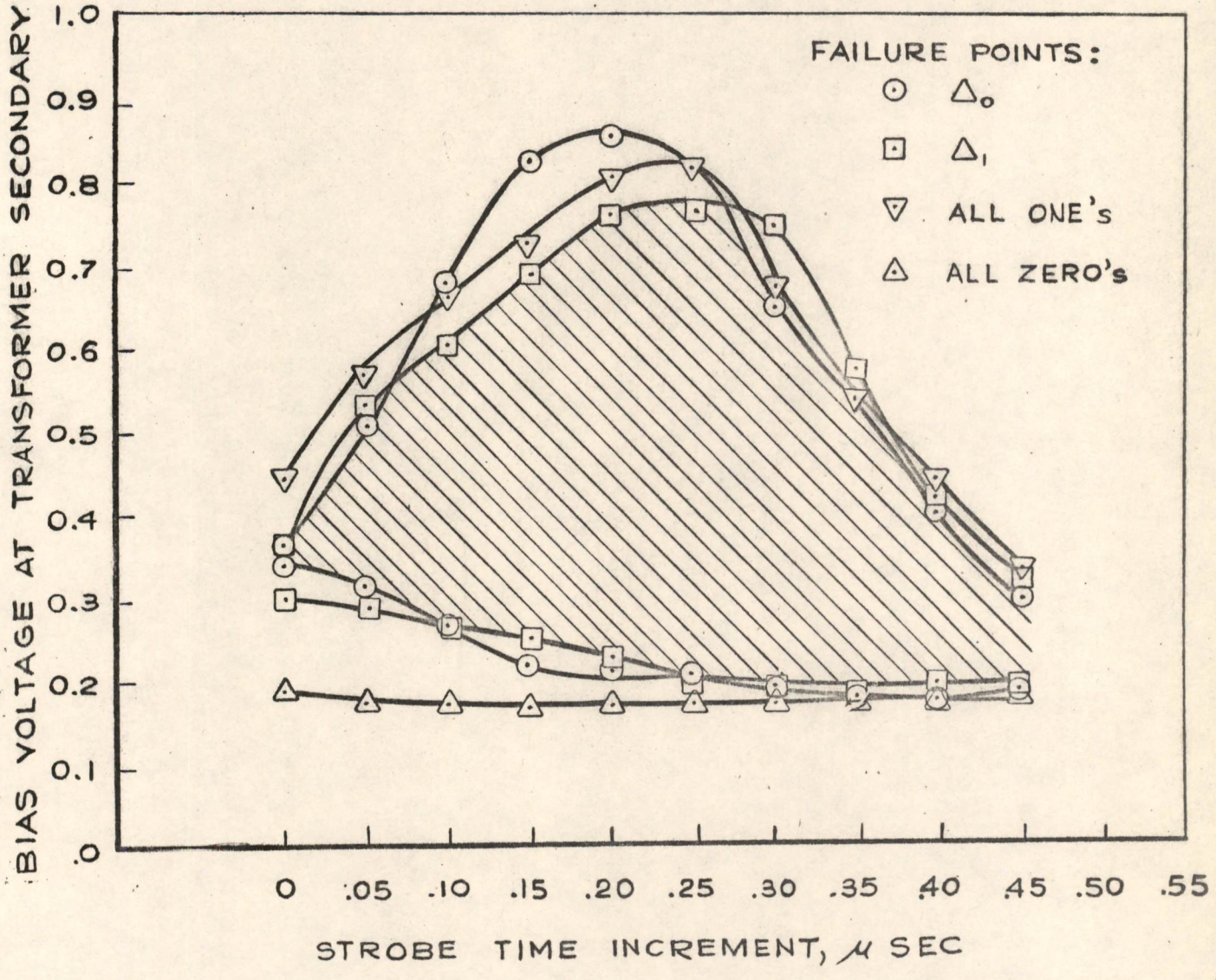



FIG. 21

MARGINS OF SENSING AMPLIFIER #3 WHEN TESTED WITH 256 x 256 MAGNETIC CORE MEMORY

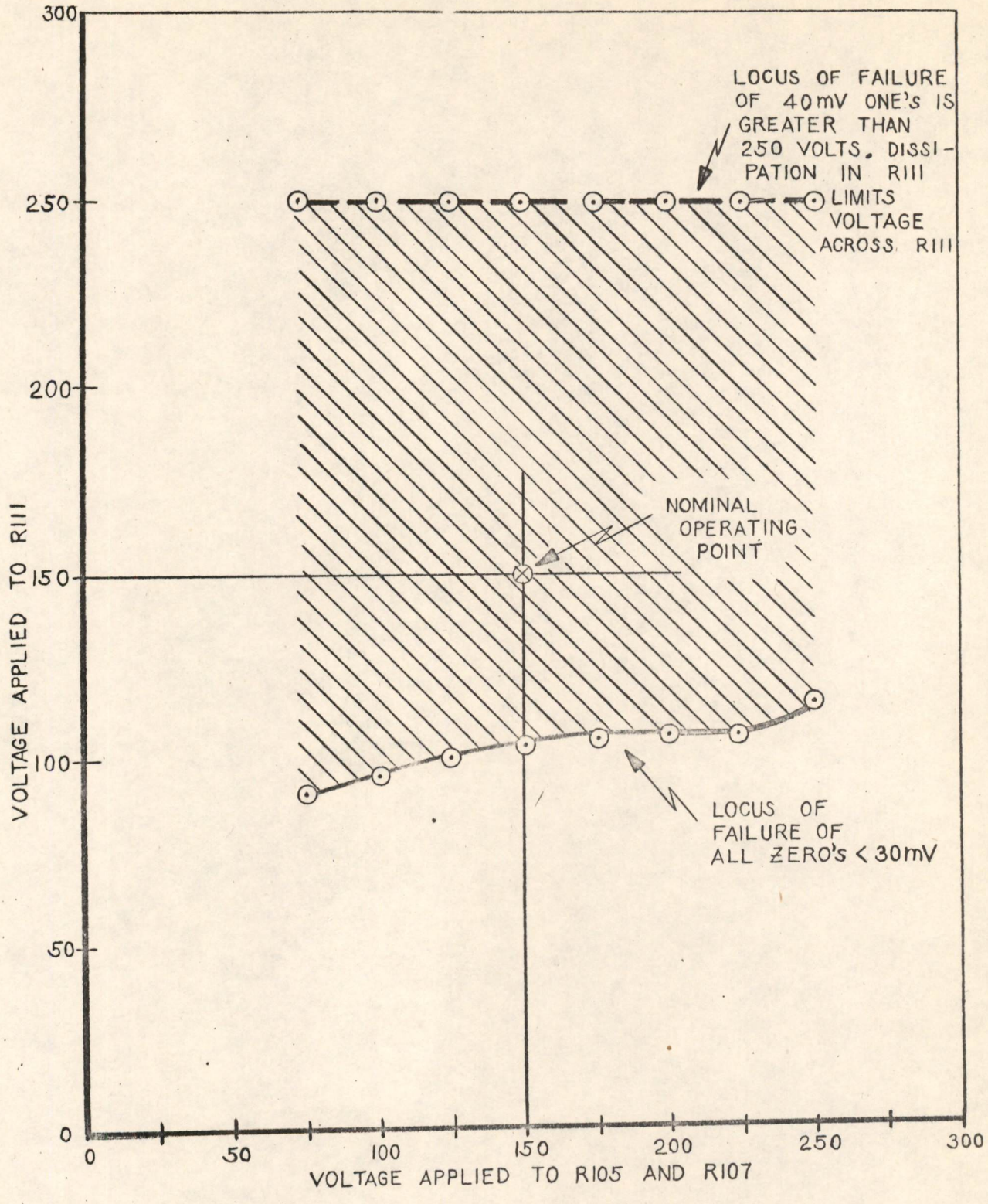



FIG. 22

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO RIII vs VOLTAGE APPLIED TO RIO5 AND RIO7.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30mV.

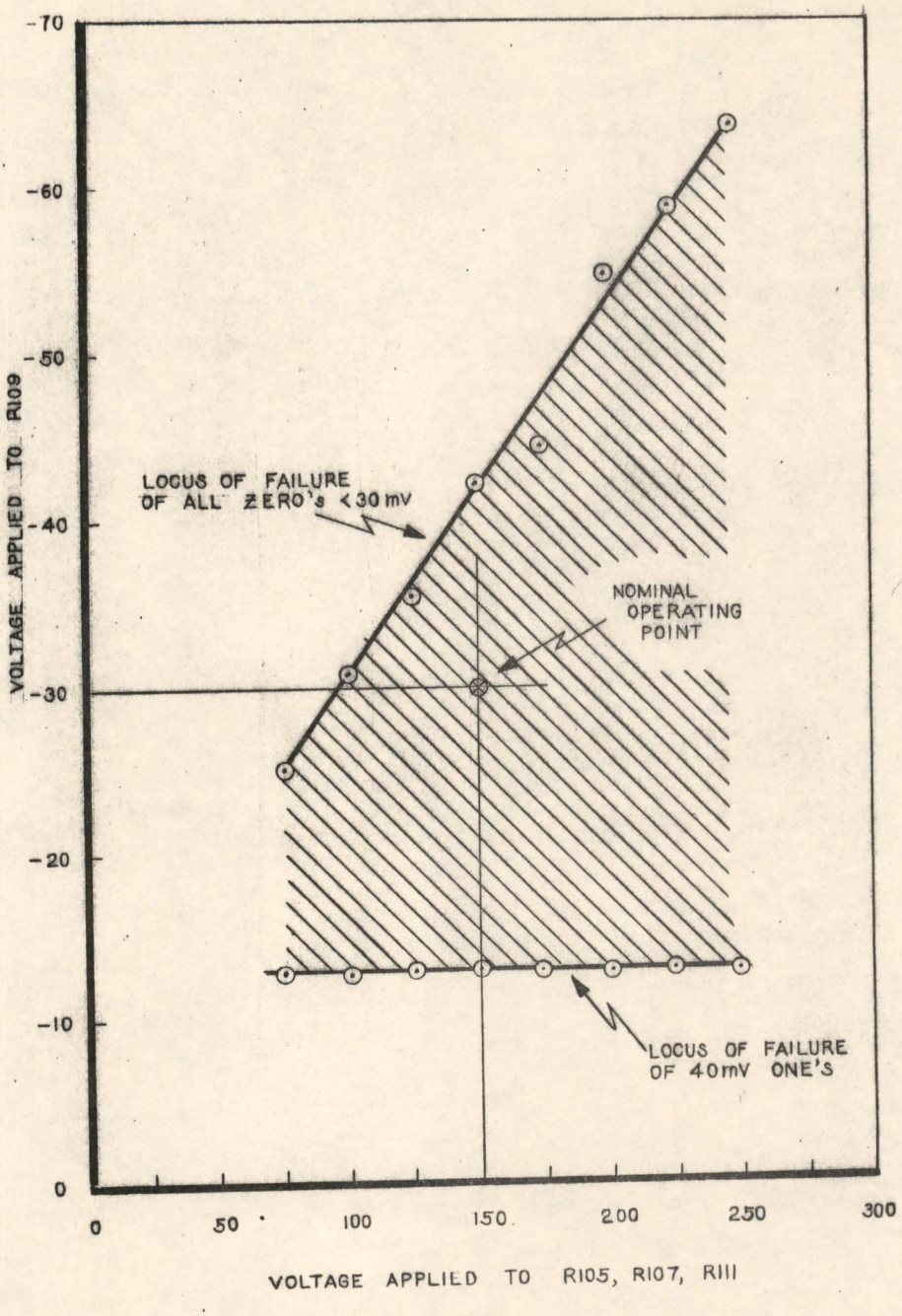



FIG. 23

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R109 vs VOLTAGE APPLIED TO R105, R107, R111.

SENSE AMPLIFIER #9, CHANNEL 3.

CLIPPING LEVEL ≅ 30mV.

B-68719

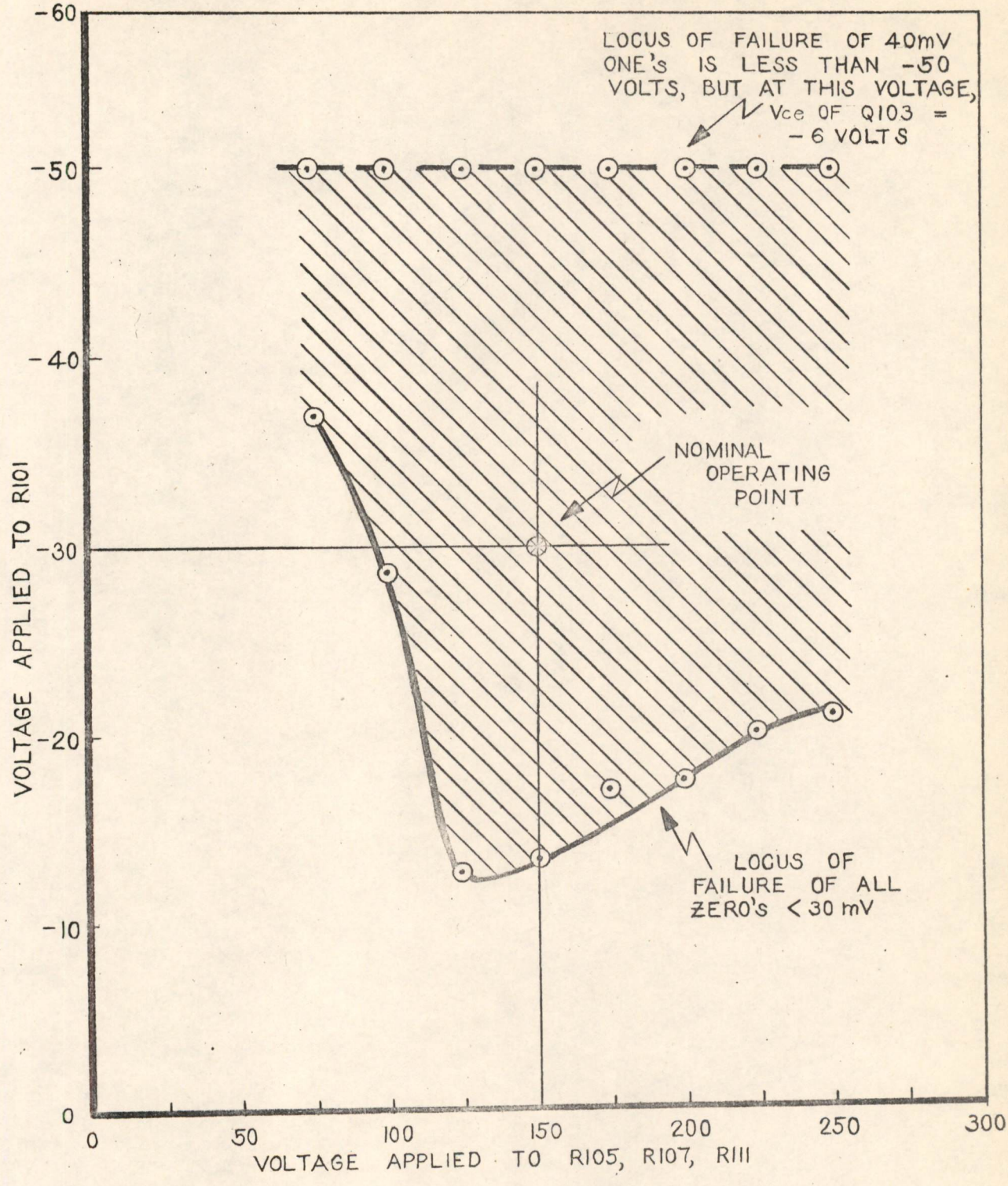



FIG. 24

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R101 vs VOLTAGE APPLIED TO R105, R107, R111.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30mV.

A-68718

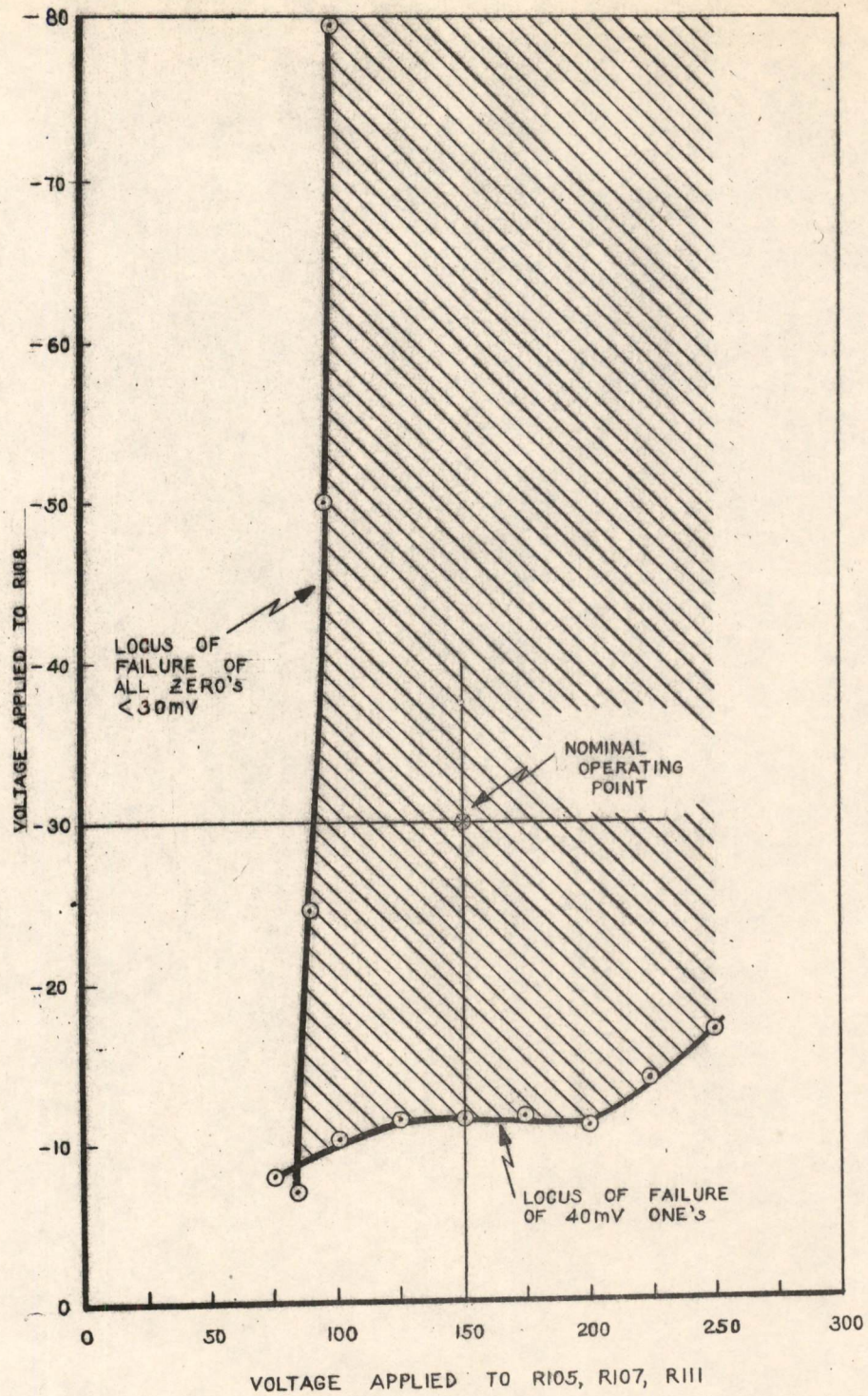



FIG. 25

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R108 vs VOLTAGE APPLIED TO R105, R107, R111.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30 mV.

Memorandum

6M-4789
Sheet 1 of 34 sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A FUNCTIONAL DESCRIPTION OF THE TX-0 COMPUTER

To: Distribution List

From: John T. Gilmore, Jr. and H. Philip Peterson

Date: November 20, 1956

Approved: Wesley A. Clark

Wesley A. Clark

Abstract: The TX-0 is an experimental digital computer which was constructed to check transistor circuitry and a 256 x 256 magnetic core memory. The logical design is rather simple since it has only four instructions. Three of these refer to memory in the normal way, but the fourth has the interesting feature of providing the facility to micro-program via time pulses. How useful this is will be determined by the experience gained in programming for TX-0. This memo has been written to give the reader a working knowledge of the computer's logic, usefullness, and capabilities.

Distribution List:

Group 63 Staff
Bagley, P. R.
Heart, F.
Mayer, R.
Dinneen, G. P.
Ziegler, H.
Vanderburgh, A.
Arden, Dean (Barta)
Attridge, W.
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Holmes, L.
Daggett, N.
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Zraket, C. A.
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Rich, E.
Bailey, D.
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Frachtman, H. E.
Vance, R. R.
Neeb, Donna (RAND)
Thomas, L. M.
Dustin, D. E.
Tritter, A. L.
Briscoe, H.



The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

# TABLE OF CONTENTS

## I INTRODUCTION

The TX-0 computer is a general purpose high-speed machine built primarily of transistors. The computer has one memory device which is a vacuum-tube-driven magnetic-core array capable of storing 1,179,648 bits of information. Each word contains 18 bits for a total of 65,536 or $2^{16}$ words.(1) The memory cycle time is approximately 6 μsec. The machine performs a complete operation every two memory cycles; the instruction is obtained in the first cycle and the data in the second.(2) Most of the logical and arithmetic operations are executed in the second cycle.

## II PRESENT TERMINAL EQUIPMENT

Input

1. A Ferranti photoelectric paper tape reader
   (a) Standard seven-hole flexowriter paper tape
   (b) 200 to 250 lines per second
2. Toggle switch registers
   (a) Toggle switch accmulator called TAC
   (b) Toggle switch buffer register called TBR
   (c) 16 toggle switch registers called toggle switch storage, TSS. These registers can replace the first 16 registers of magnetic core memory by means of a switch on the main console.
3. Flexoprinter input to live register bits 2, 5, 8, 11, 14, 17 setting $LR_0$ to a one when the key is struck.
4. Provision has been made for a photosensitive device, called the light pen, to control the computer from the display tube.

Output

1. One 12 1/2" cathode ray oscilloscope display tube
   (a) 511 points by 511 points in 7" by 7" array
   (b) a camera will be added in the future
2. Paper tape punch

---

1. The TX-2 which is in the process of being constructed will use this memory. The TX-0 will then have a transistor-driven core memory of $2^{13}$ registers.
2. Each memory cycle has eight time pulses and the notation we use in refering to them is cycle, time pulse, (i.e., cycle 0, time pulse 8 is written 0.8).

(a) Standard flexowriter tape

3. Standard flexowriter printer

III REGISTERS

1. Memory Buffer Register - (MBR, 18 bits + 1 parity check bit) - receives information from and sends information to the memory. The transfer of information from the memory is checked by means of the parity digit which makes the sum of all 19 digits odd.

2. Accumulator - (AC, 18 bits) - stores the results of numerical operations - is also used as buffer to in-out terminal equipment. The bits of AC are numbered from left to right, 0 to 17.

One interesting point with regard to the AC is that one may look upon it as strictly a ring adder. If we consider the left-most digit as a sign, then the largest representable number is $2^{18}-1$ and the smallest is $-2^{-18}+1$. If a one is added to the largest number the result is the smallest and likewise if a one is subtracted from the smallest the result is the largest. There is no overflow alarm. This feature has already been found to be useful in decision techniques.

3. Memory Address Register - (MAR, 16 bits) - selects the information in the memory and has another special feature of selecting operate class commands - (more about this later).

4. Program Counter - (PC, 16 bits) - is used by control and contains the address of the next instruction to be executed.

5. Instruction Register - (IR, 2 bits) - contains the operation part of the instruction which is to be executed.

6. Live Register - (LR, 18 bits) - may be considered as just another storage register which uses flip-flop rather than magnetic cores. It is referred to by means operate class commands which we shall see later.

7. Toggle Switch Buffer Register - (TBR, 18 toggle switches) - used for manual intervention in the normal and test modes.

8. Toggle Switch Accumulator - (TAC, 18 toggle switches) - used for manual intervention in the normal and test modes.

For a description of the flip-flops and logical control, see Figure 6.

## IV INSTRUCTIONS AND OPERATING MODES

The first two bits of the 18 bit TX-0 word designate one of four basic instructions. The machine recognizes which one to perform by means of two flip-flops $IR_0$ and $IR_1$ called the instruction register. The remaining 16 bits of three of the instructions are used to specify a memory location. The fourth instruction makes use of its remaining 16 bits to designate one or more special commands. These are called operate class commands and are the means by which TX-0 attains its versatility. (As we shall see in section VIII and IX).

TX-0 has three operating modes: Normal, Test, and Read-In. They are specified by two flip-flops, R and T called the mode register. The four instructions are carried out in one of the three modes and for each of the twelve combinations a different function is executed by the machine. The console has a push button to select the Test mode and also one for the Read-In mode. The Normal mode is initiated by instructions in the other two modes. In the Normal mode instruction words are taken from the stored program; in the Test mode, from the TBR; and in the Read-In mode, from the tape being read in.

The mode register (R and T) decodes the modes as follows:

| MODE | R | T |
|---|---|---|
| Normal | 0 | 0 |
| Test | 0 | 1 |
| Read-In | 1 | 1 |

## V THE NORMAL MODE

The four basic instructions in the Normal mode are interpreted as follows:

| $IR_0$ | $IR_1$ | ABBREVIATION | INSTRUCTION |
|---|---|---|---|
| 0 | 0 | sto x | Replace the contents of register x with the contents of the AC. Let the AC remain the same. |
| 0 | 1 | add x | Add the word in register x to the contents of the AC and leave the sum in the AC. |
| 1 | 0 | trn x | If the sign digit of the accumulator ($AC_0$) is negative (i.e. a one) take the next instruction from register x and continue from there. If the sign is positive (i.e. a zero) ignore this instruction and proceed to the next instruction. |
| 1 | 1 | opr x | Execute one of the operate class commands indicated by the number x. (See sections VIII and IX). |

## VI TEST MODE

The test mode is selected by a push button on the console. Primarily the Test mode was designed into the computer to aid engineers and operators to manually intervene with control and storage for test purposes.

Basically one may consider the test mode as being a one instruction program where the instruction is set in the TBR (Toggle Switch Buffer) and the data to be treated either already in the AC or set in the TAC (Toggle Switch AC). There are two switches on the console which allow a little more versatility to the one instruction. They are called the repeat and step switches. The repeat switch causes the instruction to be repeated over and over again (unless, of course, it is of the transfer

control type). The step switch allows the address section of the instruction to be indexed by one each time the instruction is executed.

When the test mode push button on the console is activated (i.e., pushed) the first two digits of the TBR are sent to the IR and the last 16 digits are sent to the MAR. (In the sto x case the AC is reset according to what is set in the TAC). The PC is set to MAR + 1 and the instruction is executed.

Then if:

| Repeat Switch | Step Switch | Operation After Execution of the Instruction |
|---|---|---|
| Off | Off | The computer will stop |
| Off | On | The computer will stop but the MAR will be changed to what is in the PC namely, the preceding MAR + 1 and then the PC will be indexed by 1. |
| On | Off | The computer will continue to perform the same instruction repeatedly at machine speed. |
| On | On | The MAR will be changed to what is in the PC, namely the preceding MAR + 1. Then the PC will again be indexed by 1 and the instruction will be executed repeatedly with the address section being stepped up by one each time. |

The four basic instructions for the test mode are classified as load, examine, test operate, and start.

| | | |
|---|---|---|
| "Load" | sto x<br>0 0 | The AC is set to what is in the TAC and then the contents of the AC are stored in register x. |

| | | |
|---|---|---|
| "Examine" | add x<br>0 1 | The contents of register x are added to the AC by means of the MBR. Hence x can be examined in the MBR. The AC could have been "anything" before the instruction so all we can say is that the AC will contain "anything" plus the contents of x. |
| "Test Operate" | opr x<br>1 1 | Any one of the operate class commands is executed. Stepping means nothing in this instruction. |
| "Start" | trn x<br>1 0 | Change to normal mode and transfer control to instruction in register x. Stepping and repeating mean nothing in this instruction. |

## VII READ-IN MODE

The Read-In mode is selected by a push button on the console and causes the photoelectric reader to be activated. As each line of tape passes under the read head, the information in tape positions 1, 2, 3, 4, 5, and 6 is transferred to digital positions 3, 6, 9, 12 and 15 of the AC. Once the first line of information is in the AC, the AC is cycled to the right one digital position. The second line is then read in, the AC cycled again one position, and the third line read in. At this point the first three lines are now assembled as a word in the AC. The tapes to be used by the Read-In mode have been made so that each word to be stored follows an instruction word on tape which will perform the storage. In order to transfer control to inner storage all that is required on tape is the transfer instruction itself and it will not be followed by the usual three lines of data as the store instruction is. Getting back to the mechanics of the read-in, the first three lines of information have been read in and assembled in the AC. Since this word will be an instruction in either the storage or the transfer case, the first two digits in the AC are transferred to the IR (Instruction Register) and the last 16 digits to the MAR. At this point the

instruction register is examined and if the instruction is of the storage type then the next three lines of tape are read in and assembled in the AC and then the instruction is executed. If when the IR was examined the instruction was of the transfer control type then no more information is read in and the transfer control instruction is executed. Summarizing, we can say that each data word requires six lines of tape; the first three indicating where to put it and the last three the word itself; each transfer control instruction requires only three lines of tape containing the instruction itself. The tape layout can be seen more clearly in Figure 5.

The four basic instructions of the Read-In mode are separated into two types - storage and transfer control.

| Type | First IR | Modified IR | Lines of tape | Symbol | Description |
|---|---|---|---|---|---|
| Storage | 0 0 | 0 0 | 6 | sto x | Store the word (which was read in behind this instruction) in register x. |
| Storage | 1 1 | 0 0 | 6 | opr x | When the two digits for opr x (11) are read into IR(in the Read-In mode) they are complemented and therefore opr x = sto x. |
| Transfer Control | 1 0 | 1 0 | 3 | trn x | When the two digits of trn (10) are read into IR (in the Read-In mode) the computer stops reading from tape; the computer is changed to the normal mode and control is immediately transferred to register x. |

| Type | First IR | Modified IR | Lines of tape | Symbol | Description |
|---|---|---|---|---|---|
| Transfer Control | 0 1 | 1 0 | 3 | add x | When the two digits of add (01) are read into IR (in the Read-In mode) they are complemented and the computer stops. Upon restarting (by pushing the restart button on the console) the computer performs the instruction trn x. Therefore, add x = stop + trn x. |

Note, that with a hand punch, instruction-words on the tape can be modified so that st (00) can become add (01) or transfer (10) and either add or transfer can become operate (11). The flexibility allows changes on the tape without preparing a new one.

In actual practice the Read-In mode is used to read a more efficient Read-In program into storage, since a binary tape with a store instruction following each word would be extremely large and cumbersome. A description of this program will be found in section X. It is called the Input Routine and further describes how data is put into storage and also gives the reader an example of TX-0 programming.

## VIII OPERATE CLASS COMMANDS

The following is a list of the operate class commands, the time pulse on which they are executed, the binary form they assume, what they do and the octal notation of the last 16 bits of the operate instruction, opr x.

IR | MAR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 2 | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 100,000 (octal) |

(0.8) CLL = Clear the left nine digital positions of the AC

| | | | 3 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 40,000 (octal) |

(0.8) CLR = Clear the right nine digital positions of the AC

| | | | | 4 | 5 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 20,000 (octal) |

(0.8) IOS In-Out Stop = Stop machine so that an In-Out command (specified by digits 6 7 8 of MAR) may be executed.

| | | | | 4 | 5 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 30,000 (octal) |

(1.8) Hlt = Halt the computer

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 7,000 (octal) |

(0.8) P7H = Punch holes 1-6 in flexo tape specified by AC digital positions 2, 5, 8, 11, 14, and 17. Also punch a 7th hole on tape.

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 6,000 (octal) |

(0.8) P6H = Same as P7H but no seventh hole

IR MAR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 4,000 (octal) |

(0.8) PNT = Print one flexowriter character specified by AC digits 2, 5, 8, 11, 14, and 17.

---

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 1,000 (octal) |

(0.8) R1C = Read one line of flexo tape so that tape positions 1, 2, 3, 4, 5, and 6 will be put in the AC digital positions 0, 3, 6, 9, 12 and 15.

---

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 3,000 (octal) |

(0.8) R3C = Read one line of flexo tape into AC digits 0, 3, 6, 9, 12, and 15. Then cycle the AC one digital position; read the next line on tape into AC digits 0, 3, 6, 9, 12 and 15, cycle the AC right one digital position and read the third and last line into AC digits 0, 3, 6, 9, 12 and 15. (This command is equal to a triple CYR-R1C.)

---

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 2,000 (octal) |

(0.8) DIS = Intensify a point on the scope with x and y coordinates where x is specified by AC digits 0-8 with digit 0 being used as the sign and y is specified by AC digits 9-17 with digit 9 being used as the sign for y. The complement system is in effect when the signs are negative.

---

| | | | | | | | | | 9 | 10 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 400 (octal) |

(1.4) SHR = Shift the AC right one place, i.e. multiply the AC by $2^{-1}$

---

| | | | | | | | | | 9 | 10 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 600 (octal) |

(1.4) CYR = Cycle the AC right one digital position ($AC_{17}$ will become $AC_0$)

---

| | | | | | | | | | 9 | 10 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 200 (octal) |

(1.3) MLR = Store the contents of the MBR (memory buffer register) in the live reg.

IR MAR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | 11 | | | | 15 | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 100 (octal) |

(1.1) PEN = Read the light pen flip-flops 1 and 2 into $AC_0$ and $AC_1$.

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | 11 | | | | 15 | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | = opr 4 (octal) |

(1.1) TAC = Insert a one in each digital position of the AC wherever there is a one in the corresponding digital position of the TAC.

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | 12 | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | = opr 40 (octal) |

(1.2) COM = Complement every digit in the accumulator

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | 13 | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | = opr 20 (octal) |

(1.4) PAD = Partial add AC to MBR, that is, for every digital position of the MBR that contains a one, complement the digit in the corresponding digital position of the AC. This is also called a half add.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Example: | AC = | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | MBR = | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| New | AC = | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

IR MAR

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

14

1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 = opr 10 (octal)

(1.7) CRY = Partial add the 18 digits of the AC to the corresponding 18 digits of the carry.

To determine what the 18 digits of the carry are, use the following rule:

"Grouping the AC and MBR digits into pairs and proceeding from right to left, assign the carry digit of the next pair to a one if in the present pair MBR = 1 and AC = 0 or if in the present pair AC = 1 and carry 1.

(Note: The $0^{th}$ digit-pair determines the $17^{th}$ pair's carry digit)

Example:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| MBR | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | |
| AC | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | |
| CARRY | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |
| CARRY | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |
| AC | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | |
| New AC | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 = opr 1

(1.2) AMB = Store the contents of the AC in the MBR.

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 = opr 3

(1.2) TBR = Store the contents of the TBR in the MBR.

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 = opr 2

(1.3) LMB = Store the contents of the LR in the MBR.

It should be noticed that the command CYL or cycle left was not listed. The reason for that is:

$$\underset{\text{CYL} = \text{AMB},\ \text{PAD},\ \text{CRY}}{\overset{(1.2)\ (1.4)\ (1.7)}{}}$$

Example

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| After AMB (1.2) | AC = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | MBR = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| After PAD (1.4) | MBR = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | AC = | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | CARRY = | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| After CRY (1.7) | AC = | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

This is an excellent example of how a programmer can accomplish many things with one operate instruction. Also notice that the AC was cleared by AMB + PAD. Any operate instruction-word is capable of having a large variety of commands within itself as long as the programmer is aware of the time pulse sequence. The preceding list of commands also lists the cycle and time pulse of each command. We have included a TX-0 logical flow chart in this memo with a few side remarks on the chart to assist you in reading it. Whenever there is some question as to what is happening on each time pulse this chart should give you the answer. If you find in experimenting with the operate class commands that a new operate class command would be useful to a programmer, we will be glad to consider your suggestions.

## IX COMBINATIONS OF OPERATE CLASS COMMANDS

The following list of combinations has already been found to be useful in programming. A conversion program which will be described in a later memo is capable of assembling most of these combinations using three letter mnemonic symbols (e.g. lac, alr, lad, etc.).

0.8 0.8
CLL + CLR = opr 140,000 = clear the AC (CLA)

1.2 1.4 1.7
AMB + PAD + CRY = opr 31 = cycle the AC left one digital position (CYL)

0.8 0.8 1.2
CLL + CLR + COM = opr 140,040 = clear and complement AC (CLC)

0.8 0.8
IOS + DIS = opr 22,000 = Display (this combination was included to remind you that with every in-out command the IOS must be included) (DIS)

0.8 0.8 0.8
IOS + CLL + CLR = opr 160,000 = In out stop with AC cleared.

0.8 0.8 1.4
IOS + P7H + CYR = opr 27,600 = Punch 7 holes and cycle AC right.

0.8 0.8 1.4
IOS + P6H + CYR = opr 26,600 = Punch 6 holes and cycle AC right.

0.8 0.8 0.8 0.8
IOS + CLL + CLR + P6H = opr 166,000 = Clear the AC and punch a blank space on tape.

0.8 0.8 0.8
IOS + PNT + CYR = opr 24,600 = Print and cycle AC right.

0.8 0.8 1.2 1.4
IOS + P7H + AMB + PAD = opr 27,021 = Punch 7 holes and leave AC cleared.

0.8 0.8 1.2 1.4
IOS + P6H + AMB + PAD = opr 26,021 = Punch 6 holes and leave AC cleared.

0.8 0.8 1.2 1.4
IOS + PNT + AMB + PAD = opr 24,021 = Print and leave AC cleared.

0.8 0.8 0.8
CLL + CLR + RIC = opr 141,000 = Clear AC and start petr running (notice no IOS - which means computer hasn't stopped to wait for information).

0.8 1.2 1.4 1.7
RIC + AMB + PAD + CRY = opr 1,031 = Start petr running and cycle AC left.

0.8 0.4
RIC + CYR = opr 1,600 = Start petr running and cycle right.

0.8 0.8 0.8 0.8
CLL + CLR + IOS + R3C = opr 163,000 = Clear AC, read 3 lines of tape.

0.8 0.8 0.8 0.8
CLL + CLR + IOS + RIC = opr 161,000 = Clear AC and read one line of tape.

0.8 0.8 0.8 0.8 1.4 1.7
CLR + CLR + IOS + RIC + PAD + CRY = opr 161,031 = Read 1 line of tape and cycle AC left.

0.8 0.8 0.8 0.8 1.4
CLL + CLR + IOS + RIC + CYR = opr 161,600 = Read one line of tape and cycle right.

0.8 0.8 1.1
CLL + CLR + TAC = opr 140,004 = Put contents of TAC in AC.

1.4 1.7
PAD + CRY = opr 30 = Full-add the MBR and AC and leave sum in AC.

0.8 0.8 1.3 1.4
CLL + CLR + LMB + PAD = opr 140,022 = Clear the AC - store LR contents in memory buffer register - add memory buffer to AC - i.e. store live reg. contents in AC. (LAC)

1.2 1.3
AMB + MLR = opr 201 = Store contents of AC in MBR, store contents of MBR in LR, i.e. store contents of AC in LR. (ALR)

1.3 1.4
LMB + PAD = opr 22 = Store contents of LR in MBR, partial add AC and MBR i.e. partial add LR to AC. (LPD)

1.3
MLR = opr 200 = Since MLR alone will have a clear MBR, this is really a clear LR. (LRO)

1.3 1.4 1.7
LMB + PAD + CRY = opr 32 = Full-add the LR to the AC. (LAD)

0.8 0.8 1.3 1.4
CLL + CLR + TBR + PAD = opr 140,023 = Store contents of TBR in AC.

## X PROGRAM EXAMPLE

This section was included to give the reader an example of a TX-0 program. The program which was chosen is used to read binary tapes into storage and is called the Input Routine. It was written to avoid the long and cumbersome tapes which would be required by the Read-In mode (a store instruction for each data word). When the conversion program has finished converting a program's flexowriter tape and is ready to punch a binary tape, it first punches the Input Routine on tape in the form that is required by the Read-In mode. Then the converted program is punched out in binary form according to the specifications required by the Input Routine.

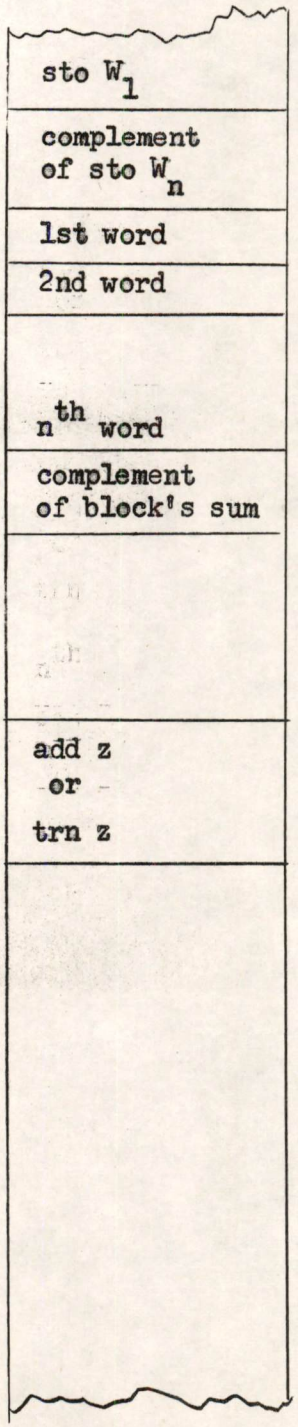
By having the Input Routine on the leader of each tape all that is required is the activation of the Read-In push button. The Input Routine is read in by the Read-In mode and then control is immediately transferred to the Input Routine which takes on the task of reading in the rest of the binary tape.

The specifications required by the Input Routine are very simple. The tape channel positions of a word are the same as they are in the Read-In mode. Words are transferred to storage in blocks of sequentially addressed words. The first word in the block is a store instruction word whose address section contains the address of the first word in the block. (Call it sto $W_1$.) The second word in the block is the complement of a store instruction word whose address contains the address of the last word in the block. (Call it sto $W_n$ where n = no. of words.) The data words follow these two pieces of information. Following the last data word of the block is a word which is the complement of the sum of all the preceding words in the block including the first two control words.

The address of the starting instruction follows the last block of data words. If it is in the form of an add instruction (add z) the computer will be stopped before the Input Routine transfers control to the program. If it is in the form of a transfer control instruction (trn z)

then the program will be started immediately after the last block of data words has been read into storage.

TAPE FORMAT REQUIRED BY INPUT ROUTINE




First block

Other blocks

Last three lines on tape

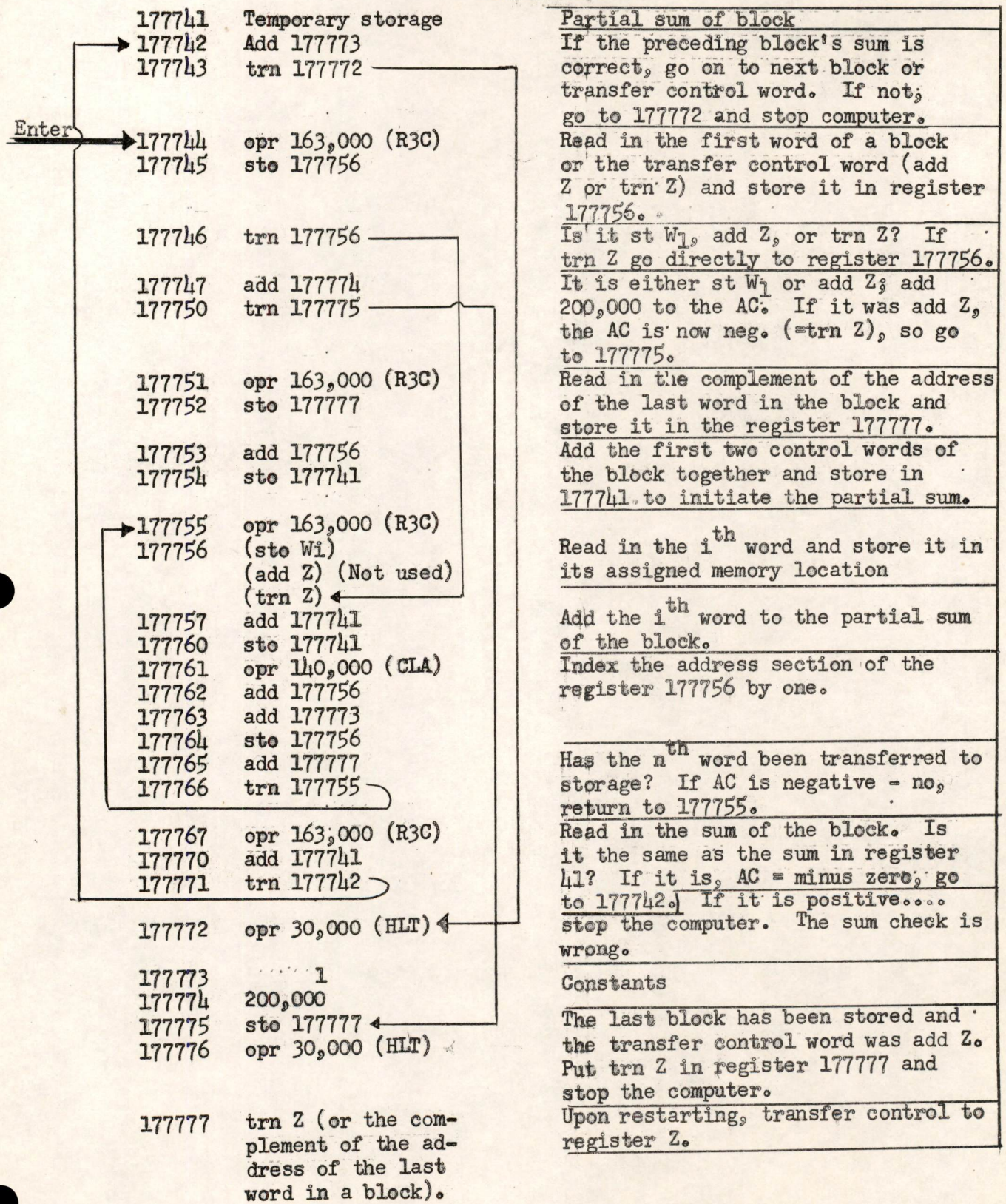
$W_1$ = Address of 1st word in block

$W_n$ = Address of $n^{th}$ word

trn z = Upon completion of last block transferred to storage take first instruction from register z.

Add z = Stop computer after last block has been transferred to storage. After restart, take first instruction from register z.

# INPUT ROUTINE



The operate class commands used in the Input routine were:

opr 160,000 = CLL + CLR + IOS + R3C

Clear AC and read three lines, cycling each time so that they are assembled as an 18 bit word in the AC.

opr 140,000 = CLL + CLR = CLA

Clear both halves of AC.

opr 30,000 = Halt the computer.

It should be noticed that a trn instruction (10) has a one in the sign digital position. In registers 177744, 45, and 46 when the transfer control word "trn Z" is read into the accumulator, the trn 177756 will transfer control to 177756. Since register 177756 will contain trn Z and the AC still contains trn Z, control will immediately be sent to register Z. This is a useful trick. (For example, transfering control to a subroutine with the exit word in the AC).

One other point of interest, if the word add Z is in the AC when instruction trn 177756 in register 177746 is performed, the AC is positive and the next instruction will be add 177774. This will cause the octal number 200,000 to be added to the AC and since the first two bits of the word add Z are 01, the result will be trn Z. This causes the instruction trn 177775 to be executed and 177775 will store the word trn Z in register 177777. The next instruction is the operate class command halt. Since the AC is not disturbed, it will still contain trn Z. If the restart push button is activated, the trn Z in register 177777 will transfer control to register Z.

## XI TOGGLE SWITCH STORAGE

The TX-0 has an auxiliary memory system consisting of sixteen toggle-switch registers which we shall refer to as toggle switch storage, TSS. The TSS can be used as a substitute for the first sixteen magnetic core registers 0 through 17. All sixteen registers of TSS can replace core registers 0 through 17 or they can be chosen individually to replace their respective core registers, i.e. $TSS_6$ can replace register 6 of core memory while the other fifteen can still be core.

The Live Register has been mentioned earlier as an eighteen bit flip-flop register with no address. Up to this point the only way reference could be made to it was by means of the operate class commands. The switches on the TSS panel allow the Live Register to be addressed like any other register. However, its contents can still only be changed by specific operate class commands or by data from the flexo typewriter (if the flexo input switch on the main console is in the on position).

The sixteen registers of TSS are located on the console. (See Figure 4) In addition to the eighteen toggle switches associated with each register there is a toggle switch located to the left of each register which we shall call "cm" and one to the right of each register which we shall call "lr". Also located on the console is a master switch called "core memory select" or CM select. When the CM select switch is on, the first sixteen registers will <u>always</u> be magnetic core. When the CM select switch is <u>off</u> then the first sixteen registers can be either magnetic core, toggle switch storage, or addresses of the live register.

The following is a breakdown of the possible combinations:

CM Select Switch = OFF

| Reg. | cm | $TSS_x$ | lr | |
|---|---|---|---|---|
| | | | | Case One |
| x | Off | W | Off | Register x is TSS and the word in x is W which is set by the toggle switches. |
| | | | | Case Two |
| x | Off | W | On | x is the address of the LR and the word in x will always be the word in the LR and not the toggle sw setting W. |
| | | | | Case Three |
| x | On | W | Off | Register x is magnetic core and the toggle switch setting W means nothing. |
| | | | | Case Four |
| x | On | W | On | The core switch cm takes precedence over the lr switch and this case becomes the same as case three. |

Note that the Live Register may have one, two, three or sixteen different addresses (0 - 17) or none at all if no lr switch is on.

JTG,HPP:bac

Attachments:
Appendix A
Appendix B
Appendix C
Fig. 1 A-68266
Fig. 2 A-68264
Fig. 3 A-68265
Fig. 4 A-68263
Fig. 5 A-68405
Fig. 6 E-69059
Fig. 7 D-47243

John T. Gilmore, Jr.

H. Philip Peterson

# APPENDIX A

## TX-0 Console

1. Push Buttons

   (a) Stop
   (b) Restart
   (c) Read-In
   (d) Test
   (e) Tape Feed

2. Flip-Flop Indicators

   (a) IR Two bit instruction register
   (b) C Cycle
   (c) RT Mode
   (d) MR Memory Read
   (e) MI Memory Inhibit
   (f) PAR Parity
   (g) SS Start Stop
   (h) PBS Push Button Synchronizer
   (i) IOS In Out Stop
   (j) CH Chime Alarm
   (k) LP Light Pen Flip-Flops 1 and 2.
   (l) PETR Photoelectric reader flip-flops 1, 2, 3 and 4
   (m) Alarm Indicator

3. Flip-Flop Registers

   (a) MAR
   (b) PC
   (c) MBR
   (d) AC
   (e) LR

4. Switches

(a) Suppress Alarm
(b) Suppress Chime
(c) Automatic Restart
(d) Automatic Read-In
(e) Automatic Test
(f) Stop on Cycle Zero
(g) Stop on Cycle One
(h) Step
(i) Repeat
(j) Printer Input

5. Toggle Switch Registers

(a) TAC - Toggle switch accumulator
(b) TBR - Toggle switch buffer register
(c) TSS - Sixteen toggle switch storage registers

# APPENDIX B

## Operate Class Command Summary

| | | | | |
|---|---|---|---|---|
| CLL | (0,8) | opr | 100,000 | Clear left AC |
| CLR | (0,8) | opr | 40,000 | Clear right AC |
| IOS | (0,8) | opr | 20,000 | In-out stop |
| HLT | (1,8) | opr | 30,000 | Halt |
| P7H | (0,8) | opr | 7,000 | Punch 7 holes |
| P6H | (0,8) | opr | 6,000 | Punch 6 holes |
| PNT | (0,8) | opr | 4,000 | Print |
| R1C | (0,8) | opr | 1,000 | Read 1 line |
| R3C | (0,8) | opr | 3,000 | Read 3 lines |
| DIS | (0,8) | opr | 2,000 | Display |
| SHR | (1,4) | opr | 400 | Shift right |
| CYR | (1,4) | opr | 600 | Cycle right |
| MLR | (1,3) | opr | 200 | MBR → LR |
| PEN | (1,1) | opr | 100 | Read light pen |
| TAC | (1,1) | opr | 4 | TAC ones → AC |
| COM | (1,2) | opr | 40 | Complement AC |
| PAD | (1,4) | opr | 20 | Partial ADD MBR and AC |
| CRY | (1,7) | opr | 10 | Partial ADD carry digits and AC |
| AMB | (1,2) | opr | 1 | AC → MBR |
| TBR | (1,2) | opr | 3 | TBR → MBR |
| LMB | (1,3) | opr | 2 | LR → MBR |

# APPENDIX C

## OPERATE CLASS COMMAND COMBINATION SUMMARY

| | | | | |
|---|---|---|---|---|
| opr | 140,000 | = | Clear AC - Clear AC | (CLA) |
| opr | 31 | = | Cycle left | (CYL) |
| opr | 140,040 | = | Clear and complement AC | (CLC) |
| opr | 22,000 | = | Display | |
| opr | 160,000 | = | In out stop and AC cleared | |
| opr | 27,600 | = | Punch 7 holes, cycle AC right | |
| opr | 26,600 | = | Punch 6 holes, cycle AC right | |
| opr | 166,000 | = | Clear AC - Punch blank tape | |
| opr | 24,600 | = | Print and cycle AC right | |
| opr | 27,021 | = | Punch 7 holes and clear AC | |
| opr | 26,021 | = | Punch 6 holes and clear AC | |
| opr | 24,021 | = | Print and leave AC cleared | |
| opr | 141,000 | = | Clear AC and start PETR running | |
| opr | 1,031 | = | Start PETR running and cycle left | |
| opr | 1,600 | = | Start PETR running, cycle right | |
| opr | 163,000 | = | Clear AC and read 3 lines of tape | |
| opr | 161,000 | = | Clear AC and read 1 line of tape | |
| opr | 161,031 | = | Read 1 line of tape and cycle left | |
| opr | 161,600 | = | Read 1 line of tape and cycle right | |
| opr | 140,004 | = | TAC → AC | |
| opr | 30 | = | Full add MBR and AC | |
| opr | 140,022 | = | LR → AC | (LAC) |
| opr | 201 | = | AC → LR | (ALR) |
| opr | 22 | = | Partial add LR and AC | (LPD) |
| opr | 200 | = | Clear LR | (LRO) |
| opr | 32 | = | Full add LR and AC | (LAD) |
| opr | 140,023 | = | TBR → AC | (TBR) |

A-68266

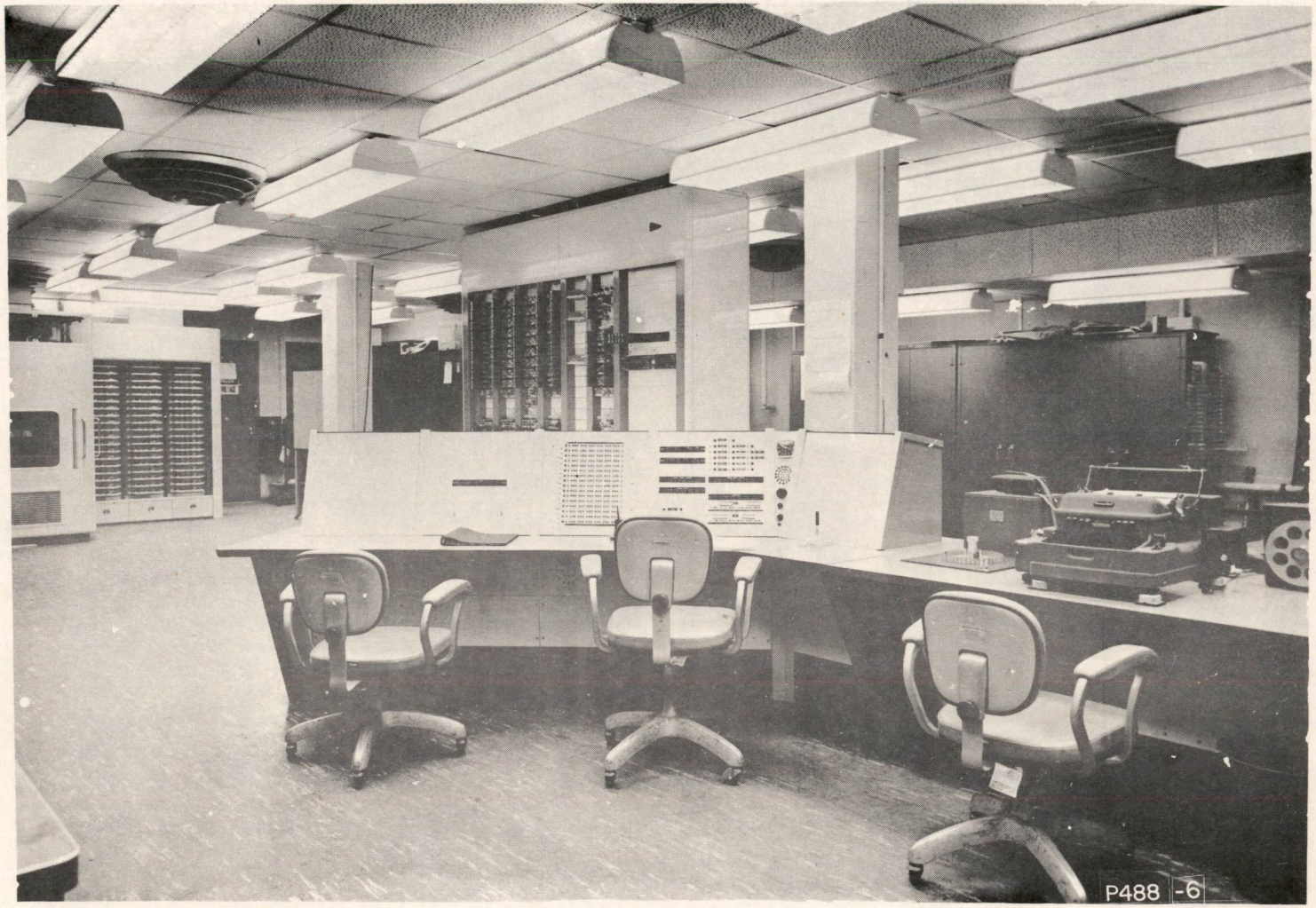



FIG. 1
TX-0 COMPUTER ROOM

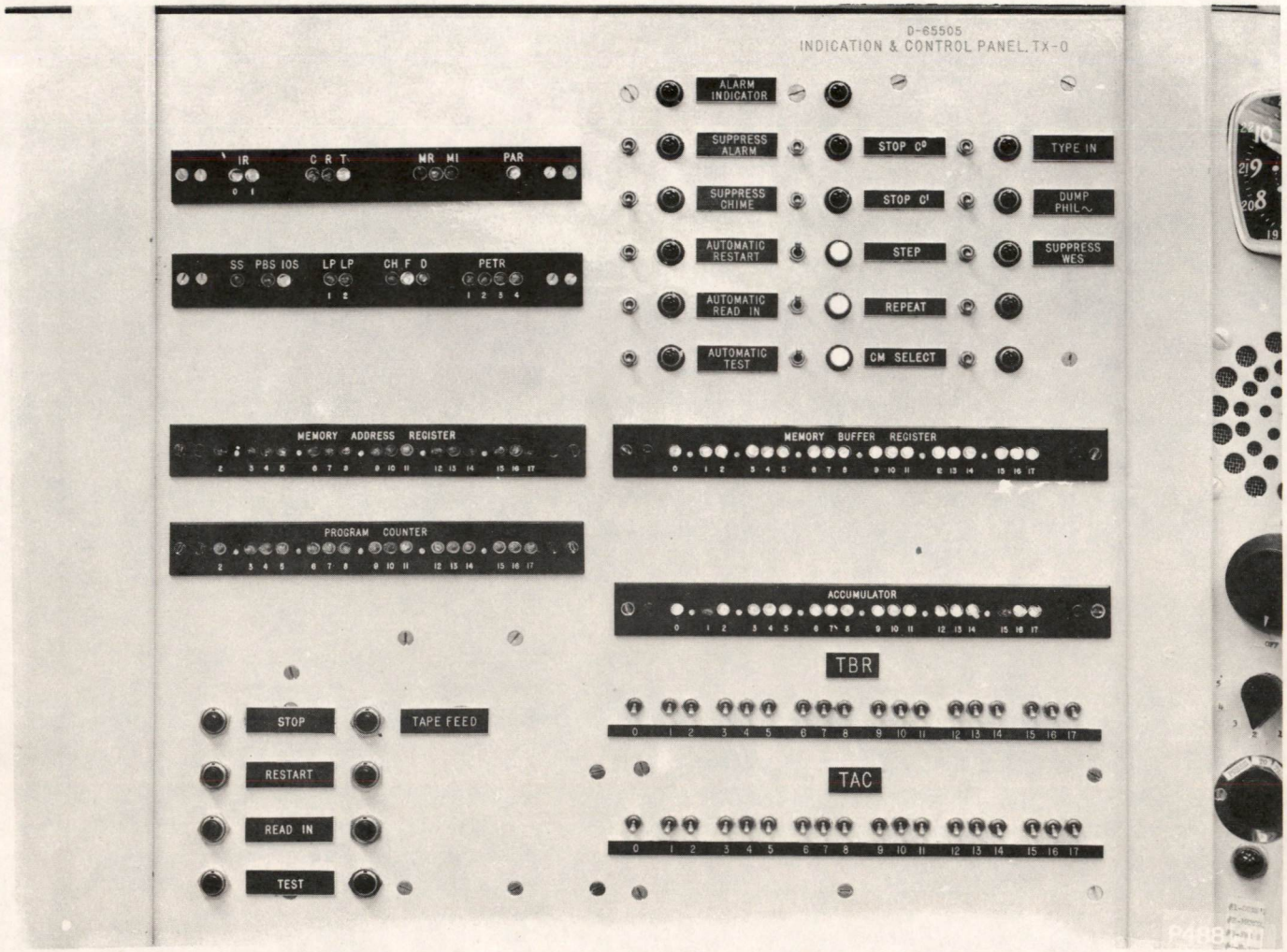



FIG. 3
TX-0 MAIN CONSOLE PANEL

A-68265

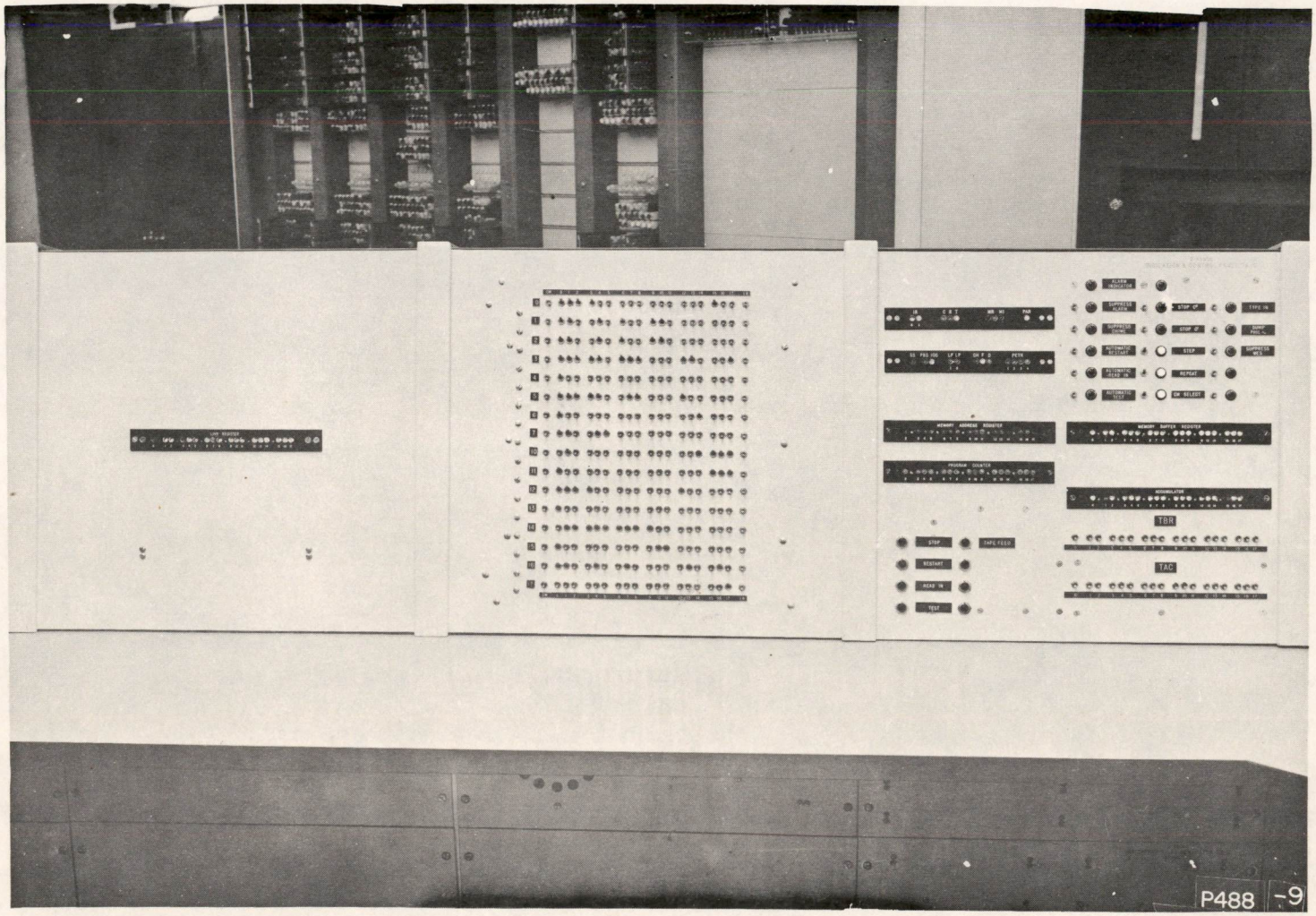



FIG. 2
TX-0 CONSOLE

A-68263

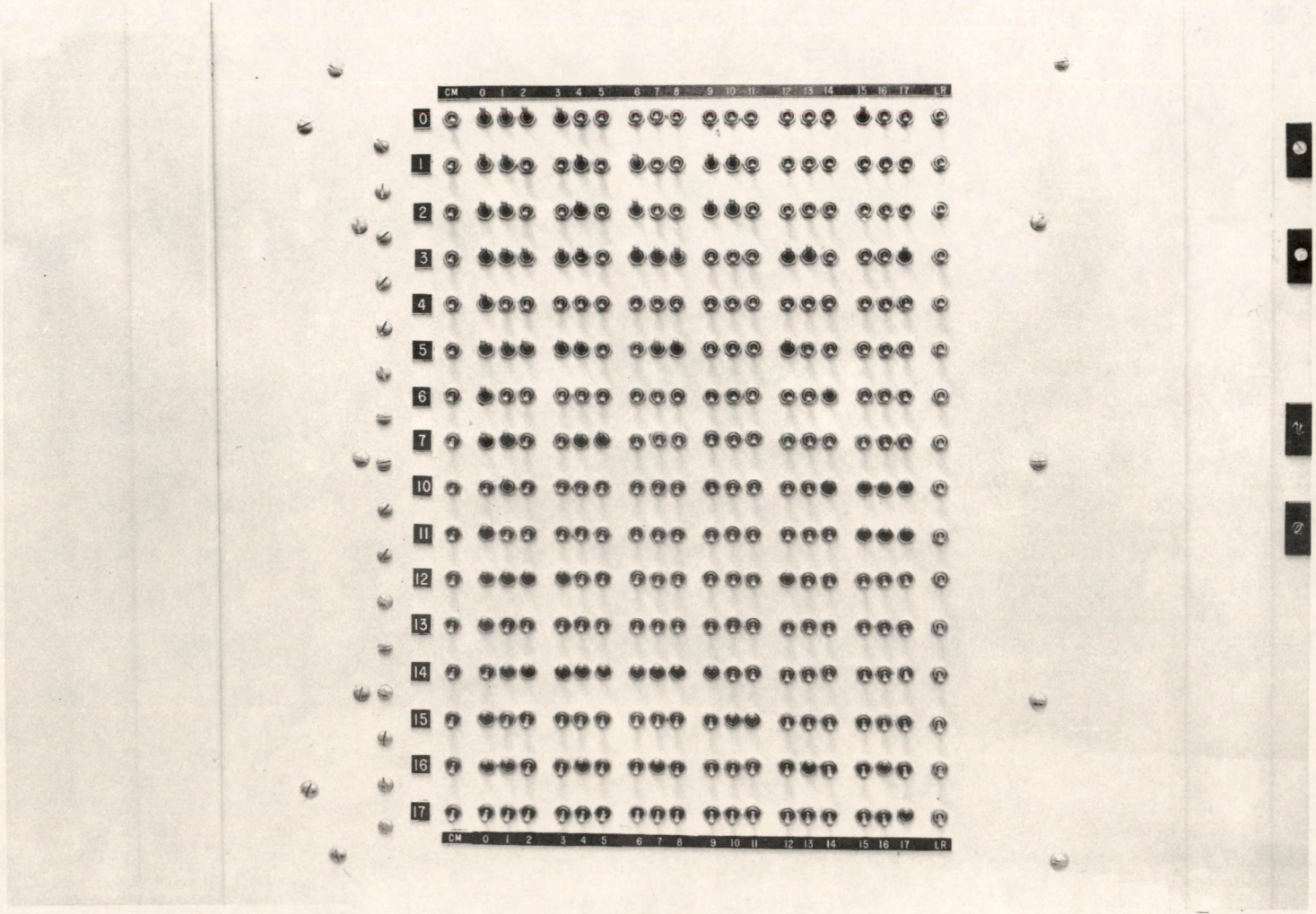
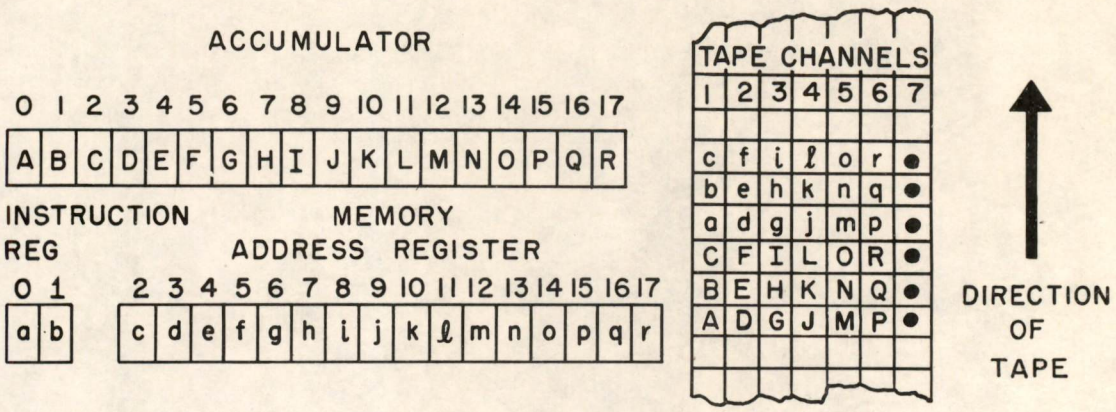
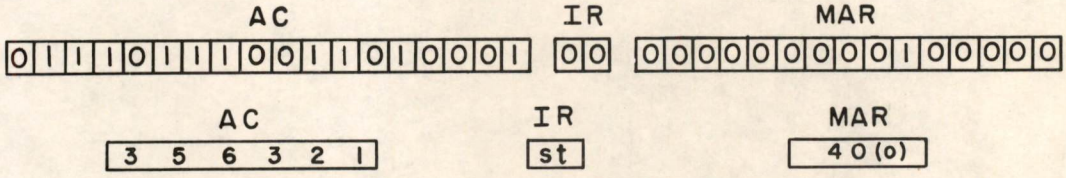
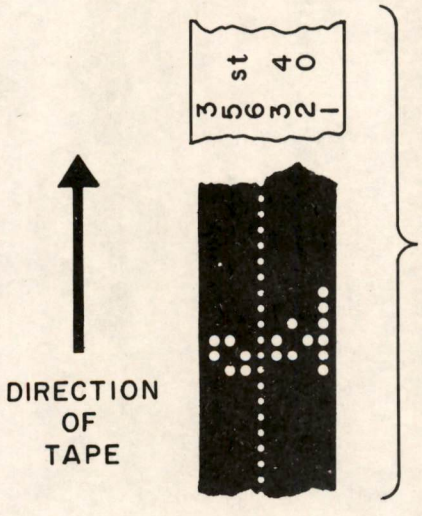



FIG. 4
TX-0 TOGGLE SWITCH STORAGE




EXAMPLE: STORE THE OCTAL WORD 356321 IN REGISTER 40 OCTAL




IF THE TAPE IS HELD SO THAT IT IS MOVING FROM LEFT TO RIGHT WITH THE SEVENTH HOLE NEXT TO THE BODY, THE DATA WORD AND STORE INSTRUCTION CAN BE READ OCTALLY IN HORZONTAL FASHION.

FIG. 5

TAPE LAYOUT FOR READ-IN MODE OF TX-0

A-68405

E-69059

TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8

THIS IS THE STANDBY CYCLE PATH

SS* | SS'

AFF* CLEAR ALARM FLIP FLOP

:MBR* :PAR* CLEAR MEMORY BUFFER REGISTER AND PARITY FLIP FLOP

C* C'

| MODE | R I |
|---|---|
| NORMAL | 0 0 |
| TEST | 0 1 |
| READ | 1 1 |

NORMAL T* | T' READ OR TEST

IN THE TEST MODE THE INSTRUCTION IS IN THE TBR

IN THE READ READ MODE THE INSTRUCTION WORD IS IN THE AC

NORMAL MODE T* | T' TEST R* R' READ

od, in, op | st

(TAC) → AC

IN THE TEST MODE st ∩ CASE, THE WORD TO BE STORED IS IN THE TAC

START READING FROM MEMORY

:MRFF'V

:MRFF'V,p,st

st | od | in | op

(TAC) → AC

READ LIGHT PEN

TEST R* R' READ

(TBR) → MBR

(AC) → MBR

:MRFF*V,p,24

PETR*5 PETR'5

PETR*3 PETR'3

(SEL TSS)* (SEL TSS)'

(SEL LR)* (SEL LR)'

TSS → MBR

LR → MBR

STROBE

CORRECT PARITY

(TBR) → MBR

(AC) → MBR

:AC'

COMPLEMENT THE ACCUMULATOR

(LR) → MBR

(MBR) → LR

:PETR'4

SHIFT

STORAGE WRITE OR REWRITE

:MIFF'

odd

:PC*

CLEAR PROGRAM COUNTER

:MRFF*4

(MBR) → IR

TRANSFER FIRST TWO DIGITS OF MBR TO INSTRUCTION REGISTER

(MAR) + 1 → PC

READ MODE

add = STOP + trn.
opr = sto
sto = sto
trn = trn

:PBS* :CH'

:IR*

(STOP ON C')* (STOP ON C)'

PARITY ODD | PARITY EVEN

(SUP ALARM)* (SUP ALARM)'

:PBS* :CH' :AFF'

(REPEAT)* (REPEAT)'

THIS CARRY COMPLETES THE PARTIAL ADD TO A FULL ADD

carry

AFF* AFF'

(PC) → MAR

(STEP)* (STEP)'

:MIFF*4

IOS* IOS'

PBS* PBS'

:SS*

:SS'

STROBE PETR*1 :PETR*1

PETR*2 PETR'2

PETR*1 PETR'1

IO RESTART (:IOS')

10 01 11

READ THREE LINES CASE

| PETR1 | PETR2 | |
|---|---|---|
| 0 | 1 | = READ FIRST LINE |
| 1 | 0 | = READ SECOND LINE |
| 1 | 1 | = READ THIRD LINE AND RESTART |

READ ONE LINE CASE

| PETR1 | PETR2 | |
|---|---|---|
| 1 | 1 | = READ FIRST LINE & RESTART |

st, od, in, op

:AC*L

:AC*R

IO STOP (:IOS*, :SS*)

READ 3 LINES

START DISPLAY

START PRINT

SPARE

START PUNCH

:C'

SET NORMAL (T*, R*)

RESET CYCLE FLIP FLOP TO ZERO

:C*

CLEAR LEFT 9 BITS OF AC

CLEAR RIGHT 9 BITS OF AC

FLIP FLOP LIST:

C = CYCLE FLIP-FLOP - DETERMINES WHICH CYCLE IS TO BE PERFORMED

R&T = MODE REGISTER - DETERMINES WHICH MODE IS TO BE PERFORMED

SS = START STOP FLIP-FLOP - DETERMINES WHETHER MACHINE WILL BE IN STANDBY CONDITION OR IN ONE OF THE OPERATING CYCLES

IOS = IN-OUT STOP FLIP-FLOP - SYNCHRONIZES COMPUTER WITH TERMINAL EQUIPMENT

PETR 1&2 = THESE TWO PETR FLIP FLOPS DETERMINE HOW MANY LINES WILL BE READ INTO THE COMPUTER

PETR 3&4 = THESE TWO PETR FLIP FLOPS SYNCHRONIZE THE COMPUTER WITH THE PHOTOELECTRIC READER WHEN INFORMATION IS AVAILABLE FROM THE TAPE.

PBS = PUSH BUTTON SYNCHRONIZER - USED TO PUT COMPUTER IN STANDBY CONDITION

MRFF = MEMORY READ FLIP-FLOP - USED TO SIGNAL READ OUT OF MEMORY TO MBR REGISTER

MIFF = MEMORY INHIBIT FLIP-FLOP - USED TO SIGNAL STORAGE WRITE FROM MBR TO MEMORY

CH = CHIME FLIP-FLOP - CAUSES CHIME TO SOUND WHEN COMPUTER STOPS (EXCEPT FOR IOS)

AFF = PARITY ALARM FLIP-FLOP - INDICATES THAT A PARITY ALARM HAS OCCURRED.

SEL TSS = SLELCT TOGGLE SWITCH STORAGE FLIP-FLOP - DETERMINES WHETHER STORAGE READ OUT WILL BE FROM CORE MEMORY OR EITHER TOGGLE SWITCH STORAGE OR LIVE REGISTER

SEL LR = SELECT LIVE REGISTER FLIP FLOP - DETERMINES WHETHER STORAGE READ OUT WILL BE FROM TOGGLE SWITCH STORAGE OR FROM LIVE REGISTER

NOTE - THE DOTTED LINES INDICATE THE BOUNDARIES OF THE TIME PULSES. EVERYTHING WITHIN THE LINES OCCURS SIMULTANEOUSLY ON THE INDICATED TIME PULSE.

PUSH BUTTON CONTROL

| | | |
|---|---|---|
| PB TEST | C*, R*, T', PBS' @ IOS' | |
| PB READIN | C' R', T', PBS', IOS', IR'4 @ IR* | |
| PB STOP | PBS*, PETR*3, PETR*4 @ FLEXO* | |
| PB RESTART | PBS' @ IOS' | |

FLOW DIAGRAM (TX-0 CONTROL WITH CHANGES)

E-69059

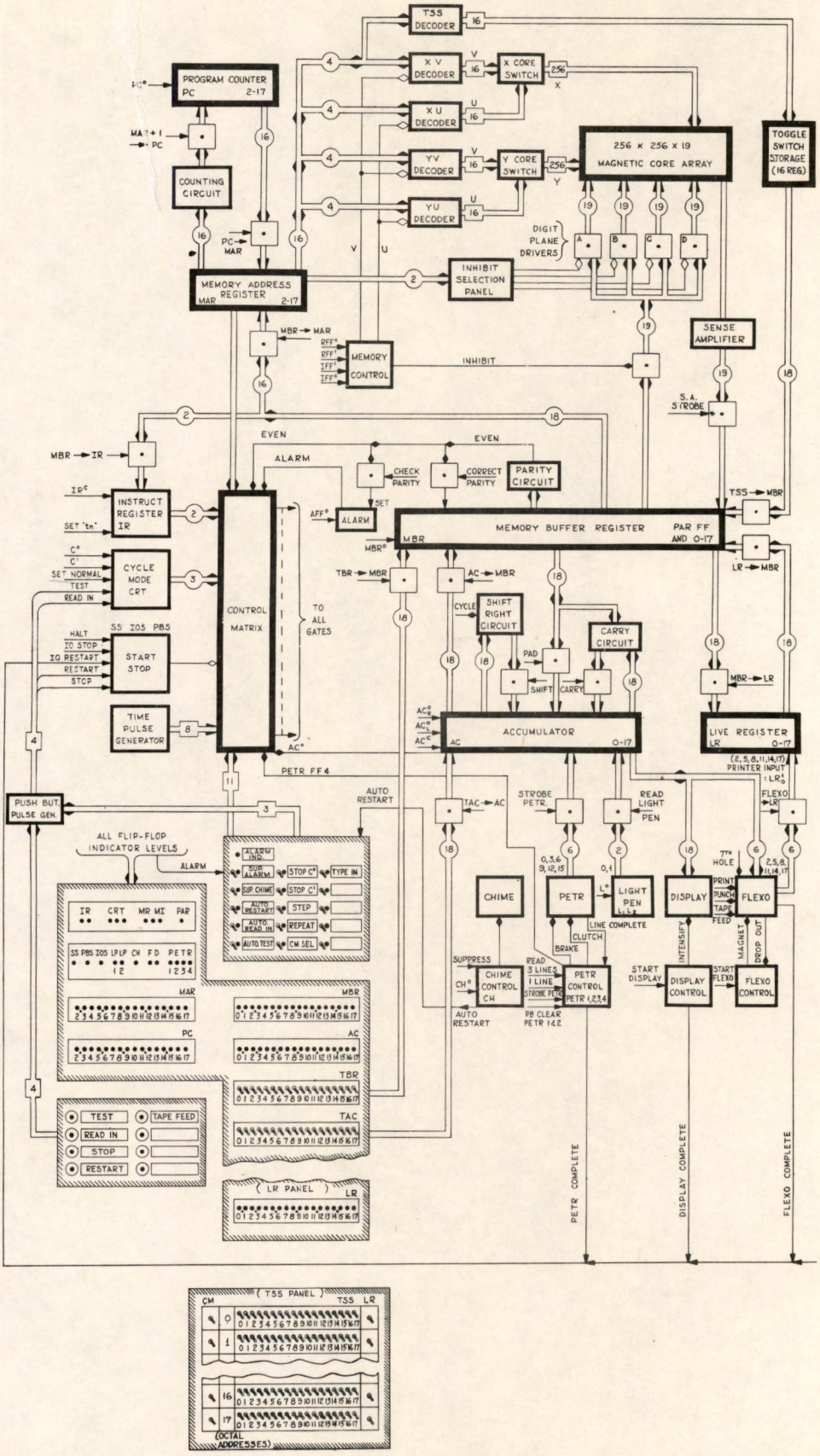



FIG. 7

BLOCK DIAGRAM, TX-0

D-47243

R. L. Best

6M-4789
Sheet 1 of 34 sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A FUNCTIONAL DESCRIPTION OF THE TX-0 COMPUTER

To: Distribution List

From: John T. Gilmore, Jr. and H. Philip Peterson

Date: November 20, 1956

Approved: Wesley A. Clark

Abstract: The TX-0 is an experimental digital computer which was constructed to check transistor circuitry and a 256 x 256 magnetic core memory. The logical design is rather simple since it has only four instructions. Three of these refer to memory in the normal way, but the fourth has the interesting feature of providing the facility to micro-program via time pulses. How useful this is will be determined by the experience gained in programming for TX-0. This memo has been written to give the reader a working knowledge of the computer's logic, usefullness, and capabilities.

Distribution List:

Group 63 Staff
Bagley, P. R.
Heart, F.
Mayer, R.
Dinneen, G. P.
Ziegler, H.
Vanderburgh, A.
Arden, Dean (Barta)
Attridge, W.
Hazel, F.P.
Hosier, W.
Grandy, C.
Buzzard, R.
Holmes, L.
Daggett, N.
Arnow, J.
Zraket, C. A.
Israel, D.
Rich, E.
Bailey, D.
Rising, H. K.
Frachtman, H. E.
Vance, R. R.
Neeb, Donna (RAND)
Thomas, L. M.
Dustin, D. E.
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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

# TABLE OF CONTENTS

## I INTRODUCTION

The TX-0 computer is a general purpose high-speed machine built primarily of transistors. The computer has one memory device which is a vacuum-tube-driven magnetic-core array capable of storing 1,179,648 bits of information. Each word contains 18 bits for a total of 65,536 or $2^{16}$ words.(1) The memory cycle time is approximately 6 μsec. The machine performs a complete operation every two memory cycles; the instruction is obtained in the first cycle and the data in the second.(2) Most of the logical and arithmetic operations are executed in the second cycle.

## II PRESENT TERMINAL EQUIPMENT

Input

1. A Ferranti photoelectric paper tape reader
   (a) Standard seven-hole flexowriter paper tape
   (b) 200 to 250 lines per second
2. Toggle switch registers
   (a) Toggle switch accmulator called TAC
   (b) Toggle switch buffer register called TBR
   (c) 16 toggle switch registers called toggle switch storage, TSS. These registers can replace the first 16 registers of magnetic core memory by means of a switch on the main console.
3. Flexoprinter input to live register bits 2, 5, 8, 11, 14, 17 setting $LR_0$ to a one when the key is struck.
4. Provision has been made for a photosensitive device, called the light pen, to control the computer from the display tube.

Output

1. One 12 1/2" cathode ray oscilloscope display tube
   (a) 511 points by 511 points in 7" by 7" array
   (b) a camera will be added in the future
2. Paper tape punch

---

1. The TX-2 which is in the process of being constructed will use this memory. The TX-0 will then have a transistor-driven core memory of $2^{13}$ registers.
2. Each memory cycle has eight time pulses and the notation we use in refering to them is cycle, time pulse, (i.e., cycle 0, time pulse 8 is written 0.8).

(a) Standard flexowriter tape

3. Standard flexowriter printer

III REGISTERS

1. Memory Buffer Register - (MBR, 18 bits + 1 parity check bit) - receives information from and sends information to the memory. The transfer of information from the memory is checked by means of the parity digit which makes the sum of all 19 digits odd.

2. Accumulator - (AC, 18 bits) - stores the results of numerical operations - is also used as buffer to in-out terminal equipment. The bits of AC are numbered from left to right, 0 to 17.

One interesting point with regard to the AC is that one may look upon it as strictly a ring adder. If we consider the left-most digit as a sign, then the largest representable number is $2^{18}-1$ and the smallest is $-2^{-18}+1$. If a one is added to the largest number the result is the smallest and likewise if a one is subtracted from the smallest the result is the largest. There is no overflow alarm. This feature has already been found to be useful in decision techniques.

3. Memory Address Register - (MAR, 16 bits) - selects the information in the memory and has another special feature of selecting operate class commands - (more about this later).

4. Program Counter - (PC, 16 bits) - is used by control and contains the address of the next instruction to be executed.

5. Instruction Register - (IR, 2 bits) - contains the operation part of the instruction which is to be executed.

6. Live Register - (LR, 18 bits) - may be considered as just another storage register which uses flip-flop rather than magnetic cores. It is referred to by means operate class commands which we shall see later.

7. Toggle Switch Buffer Register - (TBR, 18 toggle switches) - used for manual intervention in the normal and test modes.

8. Toggle Switch Accumulator - (TAC, 18 toggle switches) - used for manual intervention in the normal and test modes.

For a description of the flip-flops and logical control, see Figure 6.

## IV INSTRUCTIONS AND OPERATING MODES

The first two bits of the 18 bit TX-0 word designate one of four basic instructions. The machine recognizes which one to perform by means of two flip-flops $IR_0$ and $IR_1$ called the instruction register. The remaining 16 bits of three of the instructions are used to specify a memory location. The fourth instruction makes use of its remaining 16 bits to designate one or more special commands. These are called operate class commands and are the means by which TX-0 attains its versatility. (As we shall see in section VIII and IX).

TX-0 has three operating modes: Normal, Test, and Read-In. They are specified by two flip-flops, R and T called the mode register. The four instructions are carried out in one of the three modes and for each of the twelve combinations a different function is executed by the machine. The console has a push button to select the Test mode and also one for the Read-In mode. The Normal mode is initiated by instructions in the other two modes. In the Normal mode instruction words are taken from the stored program; in the Test mode, from the TBR; and in the Read-In mode, from the tape being read in.

The mode register (R and T) decodes the modes as follows:

| MODE | R | T |
|---|---|---|
| Normal | 0 | 0 |
| Test | 0 | 1 |
| Read-In | 1 | 1 |

## V THE NORMAL MODE

The four basic instructions in the Normal mode are interpreted as follows:

| $IR_0$ $IR_1$ | ABBREVIATION | INSTRUCTION |
|---|---|---|
| 0 0 | sto x | Replace the contents of register x with the contents of the AC. Let the AC remain the same. |
| 0 1 | add x | Add the word in register x to the contents of the AC and leave the sum in the AC. |
| 1 0 | trn x | If the sign digit of the accumulator ($AC_0$) is negative (i.e. a one) take the next instruction from register x and continue from there. If the sign is positive (i.e. a zero) ignore this instruction and proceed to the next instruction. |
| 1 1 | opr x | Execute one of the operate class commands indicated by the number x. (See sections VIII and IX). |

## VI TEST MODE

The test mode is selected by a push button on the console. Primarily the Test mode was designed into the computer to aid engineers and operators to manually intervene with control and storage for test purposes.

Basically one may consider the test mode as being a one instruction program where the instruction is set in the TBR (Toggle Switch Buffer) and the data to be treated either already in the AC or set in the TAC (Toggle Switch AC). There are two switches on the console which allow a little more versatility to the one instruction. They are called the repeat and step switches. The repeat switch causes the instruction to be repeated over and over again (unless, of course, it is of the transfer

control type). The step switch allows the address section of the instruction to be indexed by one each time the instruction is executed.

When the test mode push button on the console is activated (i.e., pushed) the first two digits of the TBR are sent to the IR and the last 16 digits are sent to the MAR. (In the sto x case the AC is reset according to what is set in the TAC). The PC is set to MAR + 1 and the instruction is executed.

Then if:

| Repeat Switch | Step Switch | Operation After Execution of the Instruction |
|---|---|---|
| Off | Off | The computer will stop |
| Off | On | The computer will stop but the MAR will be changed to what is in the PC namely, the preceding MAR + 1 and then the PC will be indexed by 1. |
| On | Off | The computer will continue to perform the same instruction repeatedly at machine speed. |
| On | On | The MAR will be changed to what is in the PC, namely the preceding MAR + 1. Then the PC will again be indexed by 1 and the instruction will be executed repeatedly with the address section being stepped up by one each time. |

The four basic instructions for the test mode are classified as load, examine, test operate, and start.

| | | |
|---|---|---|
| "Load" | sto x<br>0 0 | The AC is set to what is in the TAC and then the contents of the AC are stored in register x. |

| | | |
|---|---|---|
| "Examine" | add x<br>0 1 | The contents of register x are added to the AC by means of the MBR. Hence x can be examined in the MBR. The AC could have been "anything" before the instruction so all we can say is that the AC will contain "anything" plus the contents of x. |
| "Test Operate" | opr x<br>1 1 | Any one of the operate class commands is executed. Stepping means nothing in this instruction. |
| "Start" | trn x<br>1 0 | Change to normal mode and transfer control to instruction in register x. Stepping and repeating mean nothing in this instruction. |

## VII READ-IN MODE

The Read-In mode is selected by a push button on the console and causes the photoelectric reader to be activated. As each line of tape passes under the read head, the information in tape positions 1, 2, 3, 4, 5, and 6 is transferred to digital positions 3, 6, 9, 12 and 15 of the AC. Once the first line of information is in the AC, the AC is cycled to the right one digital position. The second line is then read in, the AC cycled again one position, and the third line read in. At this point the first three lines are now assembled as a word in the AC. The tapes to be used by the Read-In mode have been made so that each word to be stored follows an instruction word on tape which will perform the storage. In order to transfer control to inner storage all that is required on tape is the transfer instruction itself and it will not be followed by the usual three lines of data as the store instruction is. Getting back to the mechanics of the read-in, the first three lines of information have been read in and assembled in the AC. Since this word will be an instruction in either the storage or the transfer case, the first two digits in the AC are transferred to the IR (Instruction Register) and the last 16 digits to the MAR. At this point the

instruction register is examined and if the instruction is of the storage type then the next three lines of tape are read in and assembled in the AC and then the instruction is executed. If when the IR was examined the instruction was of the transfer control type then no more information is read in and the transfer control instruction is executed. Summarizing, we can say that each data word requires six lines of tape; the first three indicating where to put it and the last three the word itself; each transfer control instruction requires only three lines of tape containing the instruction itself. The tape layout can be seen more clearly in Figure 5.

The four basic instructions of the Read-In mode are separated into two types - storage and transfer control.

| Type | First IR | Modified IR | Lines of tape | Symbol | Description |
|---|---|---|---|---|---|
| Storage | 0 0 | 0 0 | 6 | sto x | Store the word (which was read in behind this instruction) in register x. |
| Storage | 1 1 | 0 0 | 6 | opr x | When the two digits for opr x (11) are read into IR(in the Read-In mode) they are complemented and therefore opr x = sto x. |
| Transfer Control | 1 0 | 1 0 | 3 | trn x | When the two digits of trn (10) are read into IR (in the Read-In mode) the computer stops reading from tape; the computer is changed to the normal mode and control is immediately transferred to register x. |

| Type | First IR | Modified IR | Lines of tape | Symbol | Description |
|---|---|---|---|---|---|
| Transfer Control | 0 1 | 1 0 | 3 | add x | When the two digits of add (01) are read into IR (in the Read-In mode) they are complemented and the computer stops. Upon restarting (by pushing the restart button on the console) the computer performs the instruction trn x. Therefore, add x = stop + trn x. |

Note, that with a hand punch, instruction-words on the tape can be modified so that st (00) can become add (01) or transfer (10) and either add or transfer can become operate (11). The flexibility allows changes on the tape without preparing a new one.

In actual practice the Read-In mode is used to read a more efficient Read-In program into storage, since a binary tape with a store instruction following each word would be extremely large and cumbersome. A description of this program will be found in section X. It is called the Input Routine and further describes how data is put into storage and also gives the reader an example of TX-0 programming.

## VIII OPERATE CLASS COMMANDS

The following is a list of the operate class commands, the time pulse on which they are executed, the binary form they assume, what they do and the octal notation of the last 16 bits of the operate instruction, opr x.

IR | MAR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 2 | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 100,000 (octal) |

(0.8) CLL = Clear the left nine digital positions of the AC

| | | | 3 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 40,000 (octal) |

(0.8) CLR = Clear the right nine digital positions of the AC

| | | | | 4 | 5 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 20,000 (octal) |

(0.8) IOS In-Out Stop = Stop machine so that an In-Out command (specified by digits 6 7 8 of MAR) may be executed.

| | | | | 4 | 5 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 30,000 (octal) |

(1.8) Hlt = Halt the computer

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 7,000 (octal) |

(0.8) P7H = Punch holes 1-6 in flexo tape specified by AC digital positions 2, 5, 8, 11, 14, and 17. Also punch a 7th hole on tape.

| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 6,000 (octal) |

(0.8) P6H = Same as P7H but no seventh hole

IR MAR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 4,000 (octal) |

(0.8) PNT = Print one flexowriter character specified by AC digits 2, 5, 8, 11, 14, and 17.

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 1,000 (octal) |

(0.8) R1C = Read one line of flexo tape so that tape positions 1, 2, 3, 4, 5, and 6 will be put in the AC digital positions 0, 3, 6, 9, 12 and 15.

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 3,000 (octal) |

(0.8) R3C = Read one line of flexo tape into AC digits 0, 3, 6, 9, 12, and 15. Then cycle the AC one digital position; read the next line on tape into AC digits 0, 3, 6, 9, 12 and 15, cycle the AC right one digital position and read the third and last line into AC digits 0, 3, 6, 9, 12 and 15. (This command is equal to a triple CYR-R1C.)

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 6 | 7 | 8 | | | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 2,000 (octal) |

(0.8) DIS = Intensify a point on the scope with x and y coordinates where x is specified by AC digits 0-8 with digit 0 being used as the sign and y is specified by AC digits 9-17 with digit 9 being used as the sign for y. The complement system is in effect when the signs are negative.

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 9 | 10 | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 400 (octal) |

(1.4) SHR = Shift the AC right one place, i.e. multiply the AC by $2^{-1}$

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 9 | 10 | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 600 (octal) |

(1.4) CYR = Cycle the AC right one digital position ($AC_{17}$ will become $AC_0$)

---

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | 9 | 10 | | | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 200 (octal) |

(1.3) MLR = Store the contents of the MBR (memory buffer register) in the live reg.

| IR | | MAR | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
| | | | | | | | | | | | 11 | | | | 15 | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | = opr 100 (octal) |

(1.1) PEN = Read the light pen flip-flops 1 and 2 into $AC_0$ and $AC_1$.

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | 11 | | | | 15 | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | = opr 4 (octal) |

(1.1) TAC = Insert a one in each digital position of the AC wherever there is a one in the corresponding digital position of the TAC.

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | 12 | | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | = opr 40 (octal) |

(1.2) COM = Complement every digit in the accumulator

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | 13 | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | = opr 20 (octal) |

(1.4) PAD = Partial add AC to MBR, that is, for every digital position of the MBR that contains a one, complement the digit in the corresponding digital position of the AC. This is also called a half add.

Example: AC = 1 0 1 0 1 0 1
MBR = 0 1 1 1 0 0 0

New AC = 1 1 0 1 1 0 1

IR MAR

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

14

1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 = opr 10 (octal)

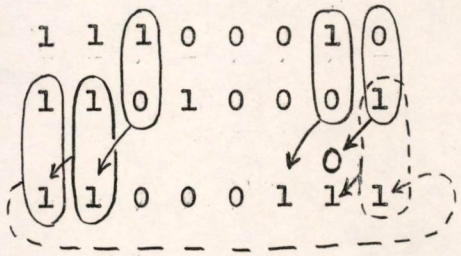
(1.7) CRY = Partial add the 18 digits of the AC to the corresponding 18 digits of the carry.

To determine what the 18 digits of the carry are, use the following rule:

"Grouping the AC and MBR digits into pairs and proceeding from right to left, assign the carry digit of the next pair to a one if in the present pair MBR = 1 and AC = 0 or if in the present pair AC = 1 and carry 1.

(Note: The $0^{th}$ digit-pair determines the $17^{th}$ pair's carry digit)

Example:




CARRY 1 1 0 0 0 1 1 1

AC 1 1 0 1 0 0 0 1

New AC 0 0 0 1 0 1 1 0

---

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 = opr 1

(1.2) AMB = Store the contents of the AC in the MBR.

---

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 = opr 3

(1.2) TBR = Store the contents of the TBR in the MBR.

---

16 17

1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 = opr 2

(1.3) LMB = Store the contents of the LR in the MBR.

It should be noticed that the command CYL or cycle left was not listed. The reason for that is:

$$\text{CYL} = \overset{(1.2)}{\text{AMB}},\ \overset{(1.4)}{\text{PAD}},\ \overset{(1.7)}{\text{CRY}}$$

Example

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| After AMB (1.2) | AC = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | MBR = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| After PAD (1.4) | MBR = | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | AC = | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | CARRY = | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| After CRY (1.7) | AC = | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

This is an excellent example of how a programmer can accomplish many things with one operate instruction. Also notice that the AC was cleared by AMB + PAD. Any operate instruction-word is capable of having a large variety of commands within itself as long as the programmer is aware of the time pulse sequence. The preceding list of commands also lists the cycle and time pulse of each command. We have included a TX-0 logical flow chart in this memo with a few side remarks on the chart to assist you in reading it. Whenever there is some question as to what is happening on each time pulse this chart should give you the answer. If you find in experimenting with the operate class commands that a new operate class command would be useful to a programmer, we will be glad to consider your suggestions.

## IX COMBINATIONS OF OPERATE CLASS COMMANDS

The following list of combinations has already been found to be useful in programming. A conversion program which will be described in a later memo is capable of assembling most of these combinations using three letter mnemonic symbols (e.g. lac, alr, lad, etc.).

0.8 0.8
CLL + CLR = opr 140,000 = clear the AC (CLA)

1.2 1.4 1.7
AMB + PAD + CRY = opr 31 = cycle the AC left one digital position (CYL)

0.8 0.8 1.2
CLL + CLR + COM = opr 140,040 = clear and complement AC (CLC)

0.8 0.8
IOS + DIS = opr 22,000 = Display (this combination was included to remind you that with every in-out command the IOS must be included) (DIS)

0.8 0.8 0.8
IOS + CLL + CLR = opr 160,000 = In out stop with AC cleared.

0.8 0.8 1.4
IOS + P7H + CYR = opr 27,600 = Punch 7 holes and cycle AC right.

0.8 0.8 1.4
IOS + P6H + CYR = opr 26,600 = Punch 6 holes and cycle AC right.

0.8 0.8 0.8 0.8
IOS + CLL + CLR + P6H = opr 166,000 = Clear the AC and punch a blank space on tape.

0.8 0.8 0.8
IOS + PNT + CYR = opr 24,600 = Print and cycle AC right.

0.8 0.8 1.2 1.4
IOS + P7H + AMB + PAD = opr 27,021 = Punch 7 holes and leave AC cleared.

0.8 0.8 1.2 1.4
IOS + P6H + AMB + PAD = opr 26,021 = Punch 6 holes and leave AC cleared.

0.8 0.8 1.2 1.4
IOS + PNT + AMB + PAD = opr 24,021 = Print and leave AC cleared.

0.8 0.8 0.8
CLL + CLR + RIC = opr 141,000 = Clear AC and start petr running (notice no IOS - which means computer hasn't stopped to wait for information).

0.8 1.2 1.4 1.7
RIC + AMB + PAD + CRY = opr 1,031 = Start petr running and cycle AC left.

0.8 0.4
RIC + CYR = opr 1,600 = Start petr running and cycle right.

0.8 0.8 0.8 0.8
CLL + CLR + IOS + R3C = opr 163,000 = Clear AC, read 3 lines of tape.

0.8 0.8 0.8 0.8
CLL + CLR + IOS + RIC = opr 161,000 = Clear AC and read one line of tape.

0.8 0.8 0.8 0.8 1.4 1.7
CLR + CLR + IOS + RIC + PAD + CRY = opr 161,031 = Read 1 line of tape and cycle AC left.

0.8 0.8 0.8 0.8 1.4
CLL + CLR + IOS + RIC + CYR = opr 161,600 = Read one line of tape and cycle right.

0.8 0.8 1.1
CLL + CLR + TAC = opr 140,004 = Put contents of TAC in AC.

1.4 1.7
PAD + CRY = opr 30 = Full-add the MBR and AC and leave sum in AC.

0.8 0.8 1.3 1.4
CLL + CLR + LMB + PAD = opr 140,022 = Clear the AC - store LR contents in memory buffer register - add memory buffer to AC - i.e. store live reg. contents in AC. (LAC)

1.2 1.3
AMB + MLR = opr 201 = Store contents of AC in MBR, store contents of MBR in LR, i.e. store contents of AC in LR. (ALR)

1.3 1.4
LMB + PAD = opr 22 = Store contents of LR in MBR, partial add AC and MBR i.e. partial add LR to AC. (LPD)

1.3
MLR = opr 200 = Since MLR alone will have a clear MBR, this is really a clear LR. (LRO)

1.3 1.4 1.7
LMB + PAD + CRY = opr 32 = Full-add the LR to the AC. (LAD)

0.8 0.8 1.3 1.4
CLL + CLR + TBR + PAD = opr 140,023 = Store contents of TBR in AC.

## X PROGRAM EXAMPLE

This section was included to give the reader an example of a TX-0 program. The program which was chosen is used to read binary tapes into storage and is called the Input Routine. It was written to avoid the long and cumbersome tapes which would be required by the Read-In mode (a store instruction for each data word). When the conversion program has finished converting a program's flexowriter tape and is ready to punch a binary tape, it first punches the Input Routine on tape in the form that is required by the Read-In mode. Then the converted program is punched out in binary form according to the specifications required by the Input Routine.

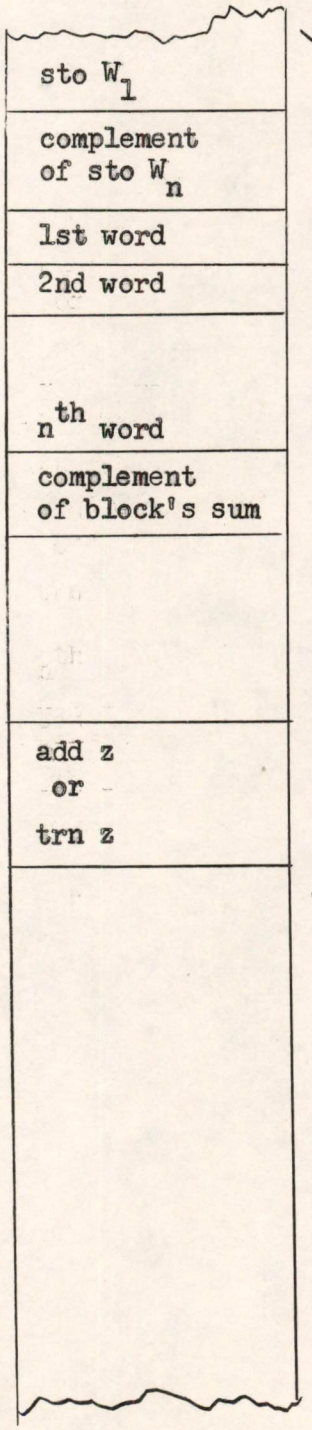
By having the Input Routine on the leader of each tape all that is required is the activation of the Read-In push button. The Input Routine is read in by the Read-In mode and then control is immediately transferred to the Input Routine which takes on the task of reading in the rest of the binary tape.

The specifications required by the Input Routine are very simple. The tape channel positions of a word are the same as they are in the Read-In mode. Words are transferred to storage in blocks of sequentially addressed words. The first word in the block is a store instruction word whose address section contains the address of the first word in the block. (Call it sto $W_1$.) The second word in the block is the complement of a store instruction word whose address contains the address of the last word in the block. (Call it sto $W_n$ where n = no. of words.) The data words follow these two pieces of information. Following the last data word of the block is a word which is the complement of the sum of all the preceding words in the block including the first two control words.

The address of the starting instruction follows the last block of data words. If it is in the form of an add instruction (add z) the computer will be stopped before the Input Routine transfers control to the program. If it is in the form of a transfer control instruction (trn z)

then the program will be started immediately after the last block of data words has been read into storage.

TAPE FORMAT REQUIRED BY INPUT ROUTINE




First block

Other blocks

Last three lines on tape

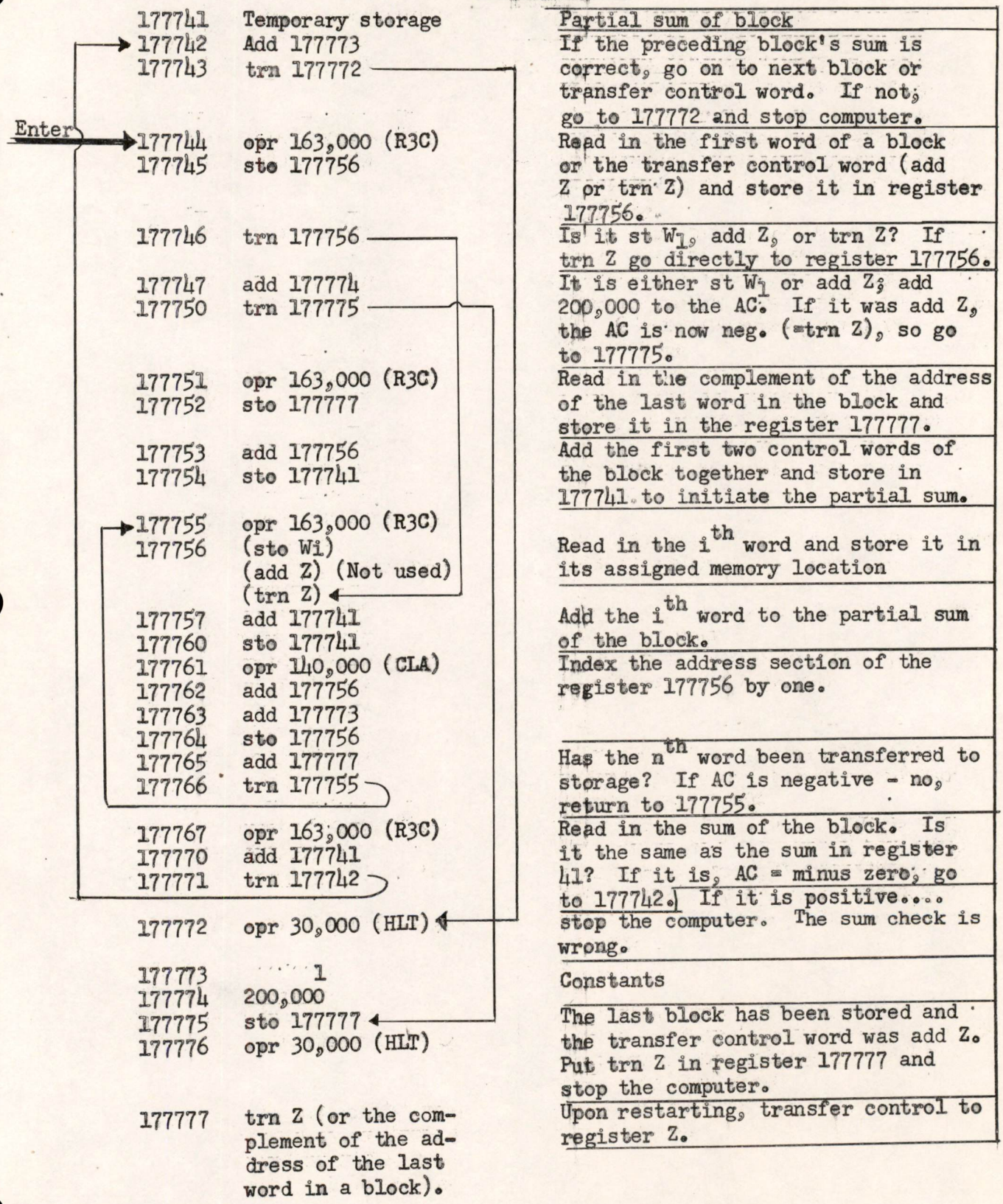
$W_1$ = Address of 1st word in block

$W_n$ = Address of $n^{th}$ word

trn z = Upon completion of last block transferred to storage take first instruction from register z.

Add z = Stop computer after last block has been transferred to storage. After restart, take first instruction from register z.

## INPUT ROUTINE



The operate class commands used in the Input routine were:

opr 160,000 = CLL + CLR + IOS + R3C
Clear AC and read three lines, cycling each time so that they are assembled as an 18 bit word in the AC.

opr 140,000 = CLL + CLR = CLA
Clear both halves of AC.

opr 30,000 = Halt the computer.

It should be noticed that a trn instruction (10) has a one in the sign digital position. In registers 177744, 45, and 46 when the transfer control word "trn Z" is read into the accumulator, the trn 177756 will transfer control to 177756. Since register 177756 will contain trn Z and the AC still contains trn Z, control will immediately be sent to register Z. This is a useful trick. (For example, transfering control to a subroutine with the exit word in the AC).

One other point of interest, if the word add Z is in the AC when instruction trn 177756 in register 177746 is performed, the AC is positive and the next instruction will be add 177774. This will cause the octal number 200,000 to be added to the AC and since the first two bits of the word add Z are 01, the result will be trn Z. This causes the instruction trn 177775 to be executed and 177775 will store the word trn Z in register 177777. The next instruction is the operate class command halt. Since the AC is not disturbed, it will still contain trn Z. If the restart push button is activated, the trn Z in register 177777 will transfer control to register Z.

## XI TOGGLE SWITCH STORAGE

The TX-0 has an auxiliary memory system consisting of sixteen toggle-switch registers which we shall refer to as toggle switch storage, TSS. The TSS can be used as a substitute for the first sixteen magnetic core registers 0 through 17. All sixteen registers of TSS can replace core registers 0 through 17 or they can be chosen individually to replace their respective core registers, i.e. $TSS_6$ can replace register 6 of core memory while the other fifteen can still be core.

The Live Register has been mentioned earlier as an eighteen bit flip-flop register with no address. Up to this point the only way reference could be made to it was by means of the operate class commands. The switches on the TSS panel allow the Live Register to be addressed like any other register. However, its contents can still only be changed by specific operate class commands or by data from the flexo typewriter (if the flexo input switch on the main console is in the on position).

The sixteen registers of TSS are located on the console. (See Figure 4) In addition to the eighteen toggle switches associated with each register there is a toggle switch located to the left of each register which we shall call "cm" and one to the right of each register which we shall call "lr". Also located on the console is a master switch called "core memory select" or CM select. When the CM select switch is on, the first sixteen registers will <u>always</u> be magnetic core. When the CM select switch is <u>off</u> then the first sixteen registers can be either magnetic core, toggle switch storage, or addresses of the live register.

The following is a breakdown of the possible combinations:

CM Select Switch = OFF

| Reg. | cm | $TSS_x$ | lr | |
|---|---|---|---|---|
| | | | | Case One |
| x | Off | W | Off | Register x is TSS and the word in x is W which is set by the toggle switches. |
| | | | | Case Two |
| x | Off | W | On | x is the address of the LR and the word in x will always be the word in the LR and not the toggle sw setting W. |
| | | | | Case Three |
| x | On | W | Off | Register x is magnetic core and the toggle switch setting W means nothing. |
| | | | | Case Four |
| x | On | W | On | The core switch cm takes precedence over the lr switch and this case becomes the same as case three. |

Note that the Live Register may have one, two, three or sixteen different addresses (0 - 17) or none at all if no lr switch is on.

JTG,HPP:bac

Attachments:
Appendix A
Appendix B
Appendix C
Fig. 1 A-68266
Fig. 2 A-68264
Fig. 3 A-68265
Fig. 4 A-68263
Fig. 5 A-68405
Fig. 6 E-69059
Fig. 7 D-47243

John T. Gilmore, Jr.

H. Philip Peterson

# APPENDIX A

## TX-0 Console

1. Push Buttons

   (a) Stop
   (b) Restart
   (c) Read-In
   (d) Test
   (e) Tape Feed

2. Flip-Flop Indicators

   (a) IR Two bit instruction register
   (b) C Cycle
   (c) RT Mode
   (d) MR Memory Read
   (e) MI Memory Inhibit
   (f) PAR Parity
   (g) SS Start Stop
   (h) PBS Push Button Synchronizer
   (i) IOS In Out Stop
   (j) CH Chime Alarm
   (k) LP Light Pen Flip-Flops 1 and 2.
   (l) PETR Photoelectric reader flip-flops 1, 2, 3 and 4
   (m) Alarm Indicator

3. Flip-Flop Registers

   (a) MAR
   (b) PC
   (c) MBR
   (d) AC
   (e) LR

4. Switches

(a) Suppress Alarm
(b) Suppress Chime
(c) Automatic Restart
(d) Automatic Read-In
(e) Automatic Test
(f) Stop on Cycle Zero
(g) Stop on Cycle One
(h) Step
(i) Repeat
(j) Printer Input

5. Toggle Switch Registers

(a) TAC - Toggle switch accumulator
(b) TBR - Toggle switch buffer register
(c) TSS - Sixteen toggle switch storage registers

4. Switches

(a) Suppress Alarm
(b) Suppress Chime
(c) Automatic Restart
(d) Automatic Read-In
(e) Automatic Test
(f) Stop on Cycle Zero
(g) Stop on Cycle One
(h) Step
(i) Repeat
(j) Printer Input

5. Toggle Switch Registers

(a) TAC - Toggle switch accumulator
(b) TBR - Toggle switch buffer register
(c) TSS - Sixteen toggle switch storage registers

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# APPENDIX B

## Operate Class Command Summary

| | | | | |
|---|---|---|---|---|
| CLL | (0,8) | opr | 100,000 | Clear left AC |
| CLR | (0,8) | opr | 40,000 | Clear right AC |
| IOS | (0,8) | opr | 20,000 | In-out stop |
| HLT | (0,8) | opr | 30,000 | Halt |
| P7H | (0,8) | opr | 7,000 | Punch 7 holes |
| P6H | (0,8) | opr | 6,000 | Punch 6 holes |
| PNT | (0,8) | opr | 4,000 | Print |
| R1C | (0,8) | opr | 1,000 | Read 1 line |
| R3C | (0,8) | opr | 3,000 | Read 3 lines |
| DIS | (0,8) | opr | 2,000 | Display |
| SHR | (1,4) | opr | 400 | Shift right |
| CYR | (1,4) | opr | 600 | Cycle right |
| MLR | (1,3) | opr | 200 | MBR → LR |
| PEN | (1,1) | opr | 100 | Read light pen |
| TAC | (1,1) | opr | 4 | TAC ones → AC |
| COM | (1,2) | opr | 40 | Complement AC |
| PAD | (1,4) | opr | 20 | Partial ADD MBR and AC |
| CRY | (1,7) | opr | 10 | Partial ADD carry digits and AC |
| AMB | (1,2) | opr | 1 | AC → MBR |
| TBR | (1,2) | opr | 3 | TBR → MBR |
| LMB | (1,3) | opr | 2 | LR → MBR |

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# APPENDIX C

## OPERATE CLASS COMMAND COMBINATION SUMMARY

| | | | | |
|---|---|---|---|---|
| opr | 140,000 | = | Clear AC Clear AC | (CLA) |
| opr | 31 | = | Cycle left | (CYL) |
| opr | 140,040 | = | Clear and complement AC | (CLC) |
| opr | 22,000 | = | Display | |
| opr | 160,000 | = | In out stop and AC cleared | |
| opr | 27,600 | = | Punch 7 holes, cycle AC right | |
| opr | 26,600 | = | Punch 6 holes, cycle AC right | |
| opr | 166,000 | = | Clear AC - Punch blank tape | |
| opr | 24,600 | = | Print and cycle AC right | |
| opr | 27,021 | = | Punch 7 holes and clear AC | |
| opr | 26,021 | = | Punch 6 holes and clear AC | |
| opr | 24,021 | = | Print and leave AC cleared | |
| opr | 141,000 | = | Clear AC and start PETR running | |
| opr | 1,031 | = | Start PETR running and cycle left | |
| opr | 1,600 | = | Start PETR running, cycle right | |
| opr | 163,000 | = | Clear AC and read 3 lines of tape | |
| opr | 161,000 | = | Clear AC and read 1 line of tape | |
| opr | 161,031 | = | Read 1 line of tape and cycle left | |
| opr | 161,600 | = | Read 1 line of tape and cycle right | |
| opr | 140,004 | = | TAC → AC | |
| opr | 30 | = | Full add MBR and AC | |
| opr | 140,022 | = | LR → AC | (LAC) |
| opr | 201 | = | AC → LR | (ALR) |
| opr | 22 | = | Partial add LR and AC | (LPD) |
| opr | 200 | = | Clear LR | (LRO) |
| opr | 32 | = | Full add LR and AC | (LAD) |
| opr | 140,023 | = | TBR → AC | (TBR) |

A-68266


FIG. 1
TX-0 COMPUTER ROOM

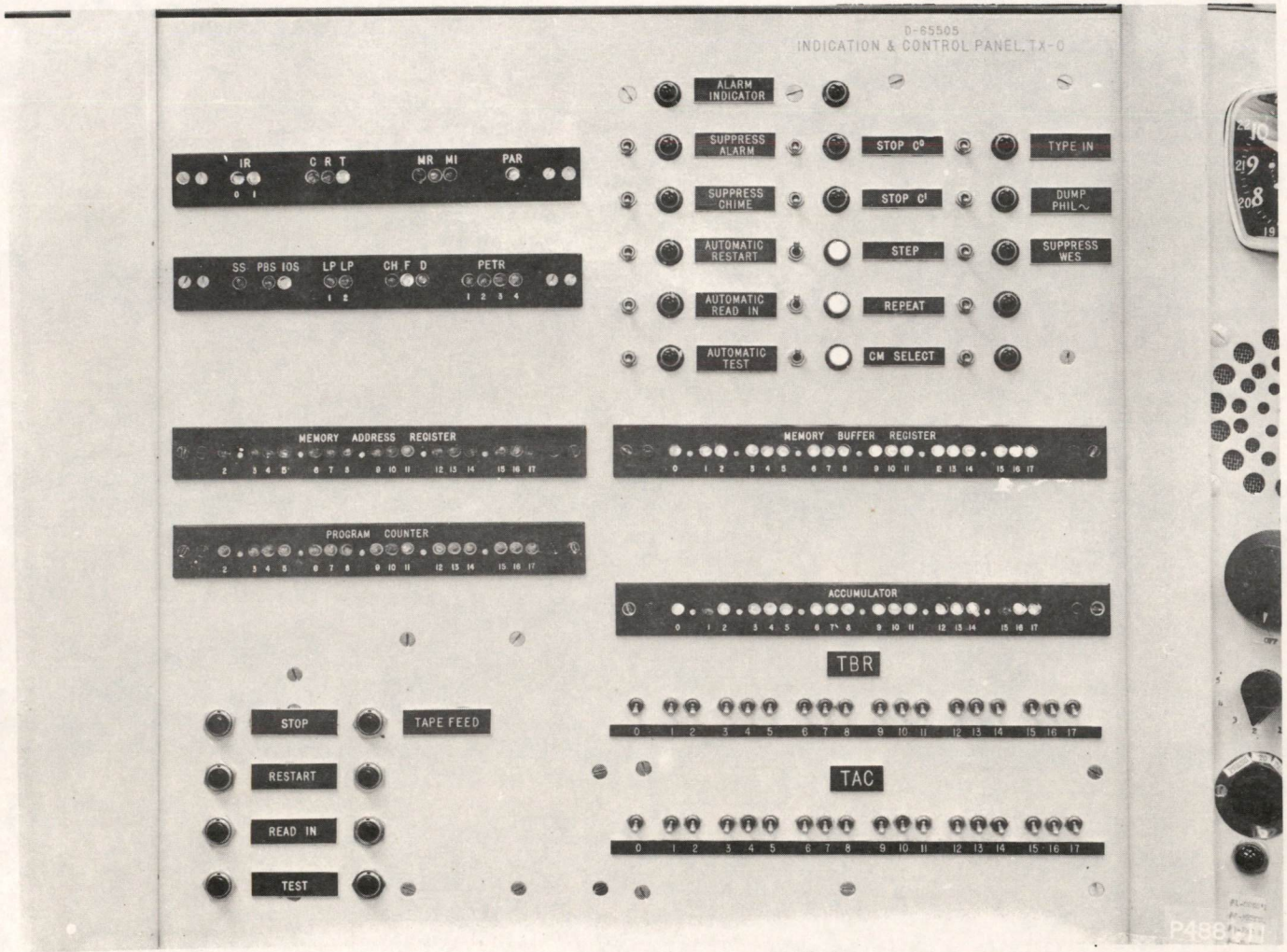



FIG. 3
TX-0 MAIN CONSOLE PANEL

A-68265

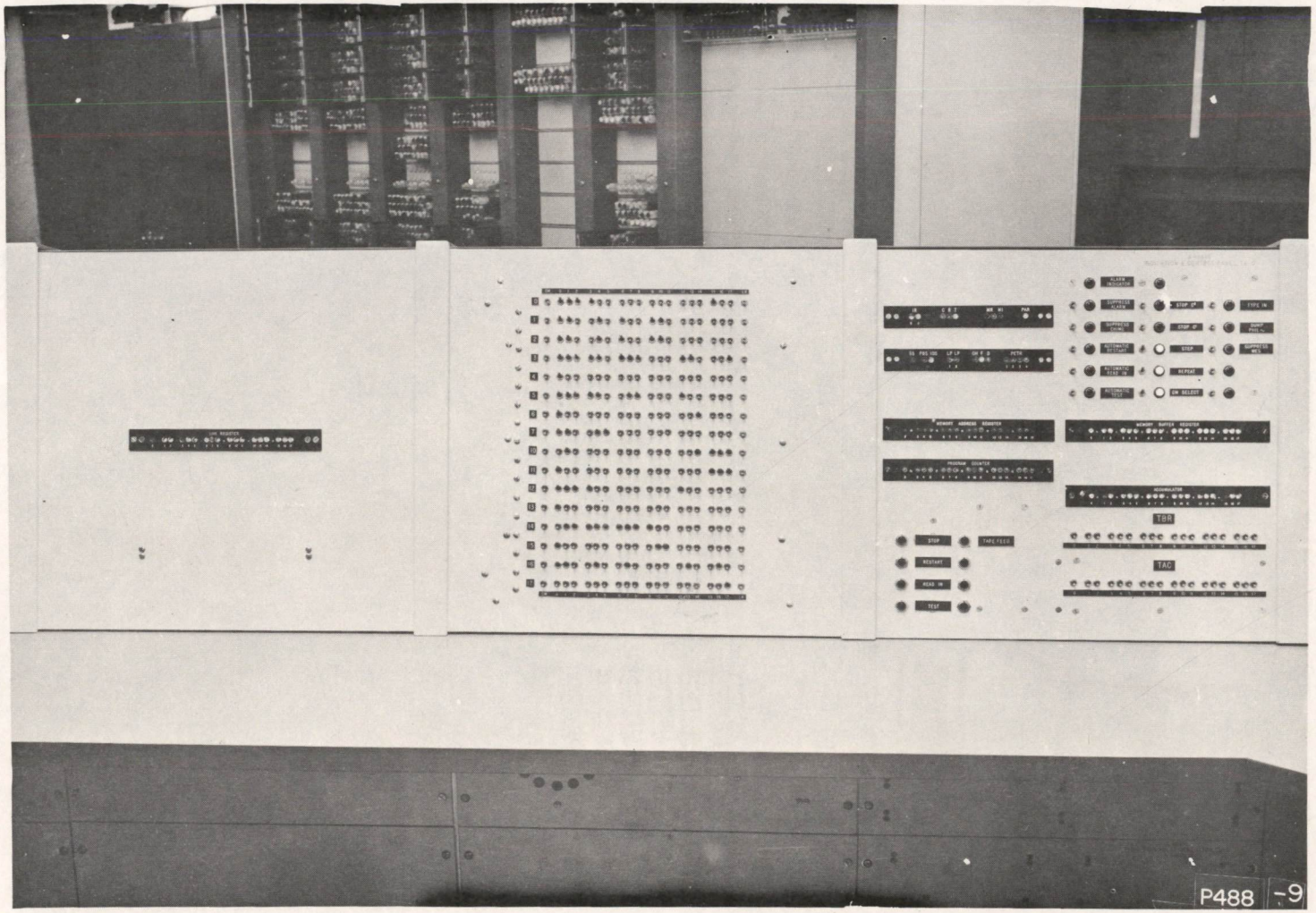



FIG. 2
TX-0 CONSOLE

A-68263

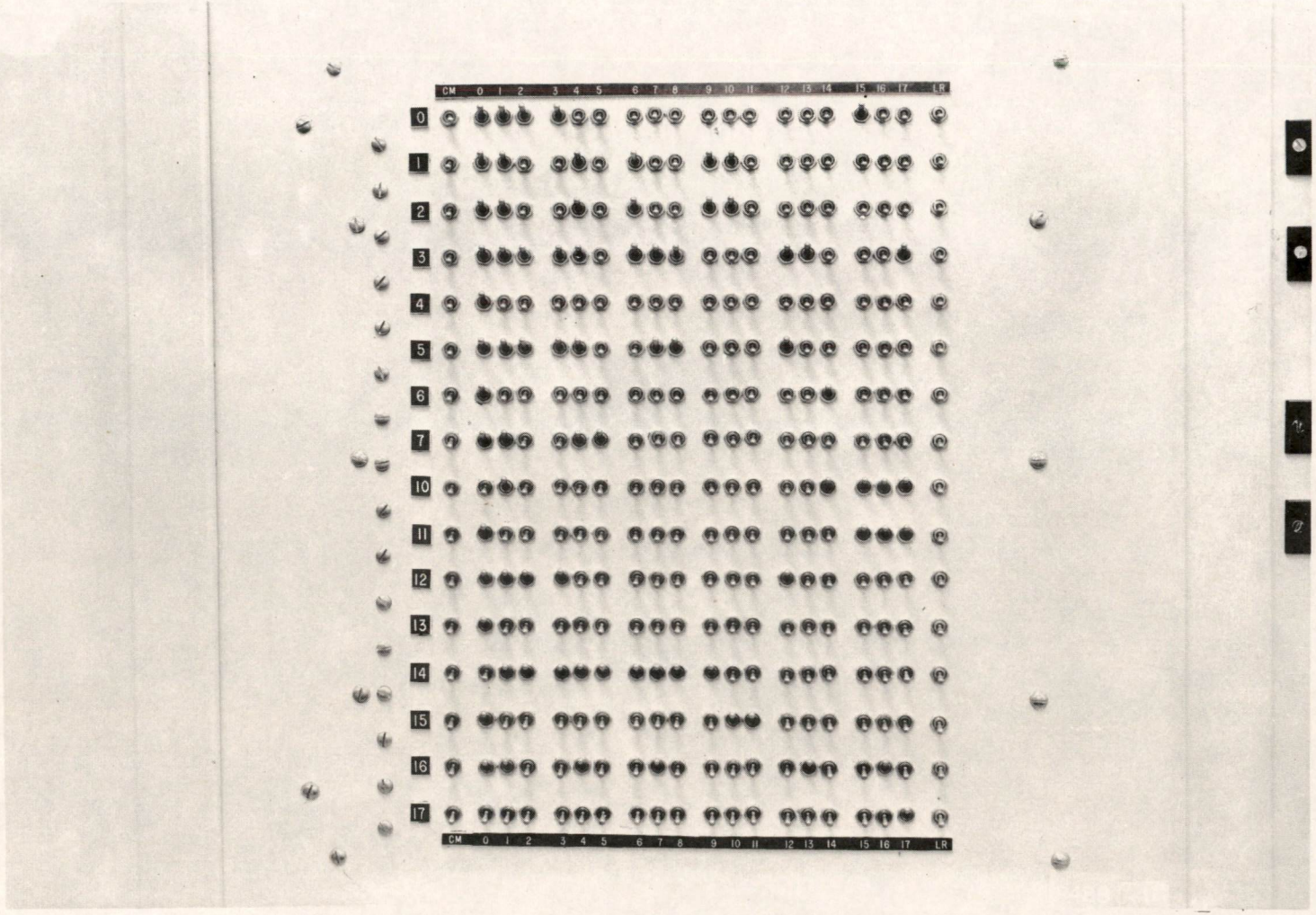
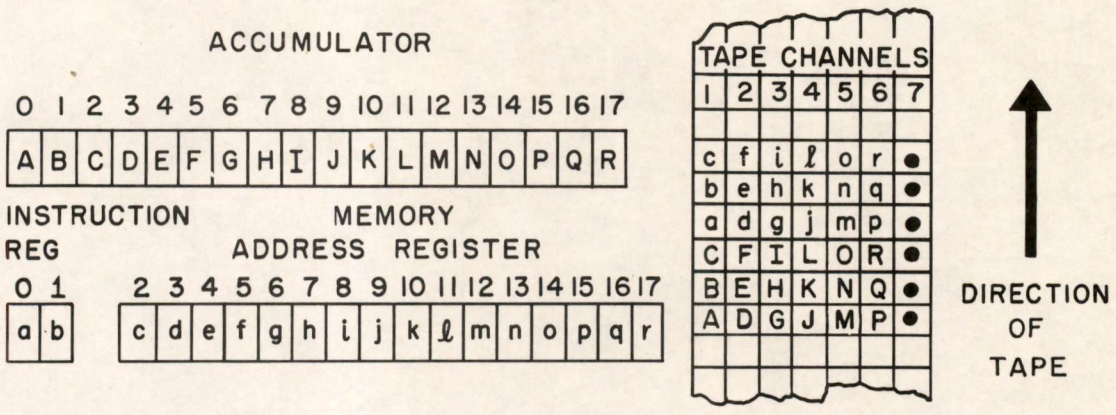
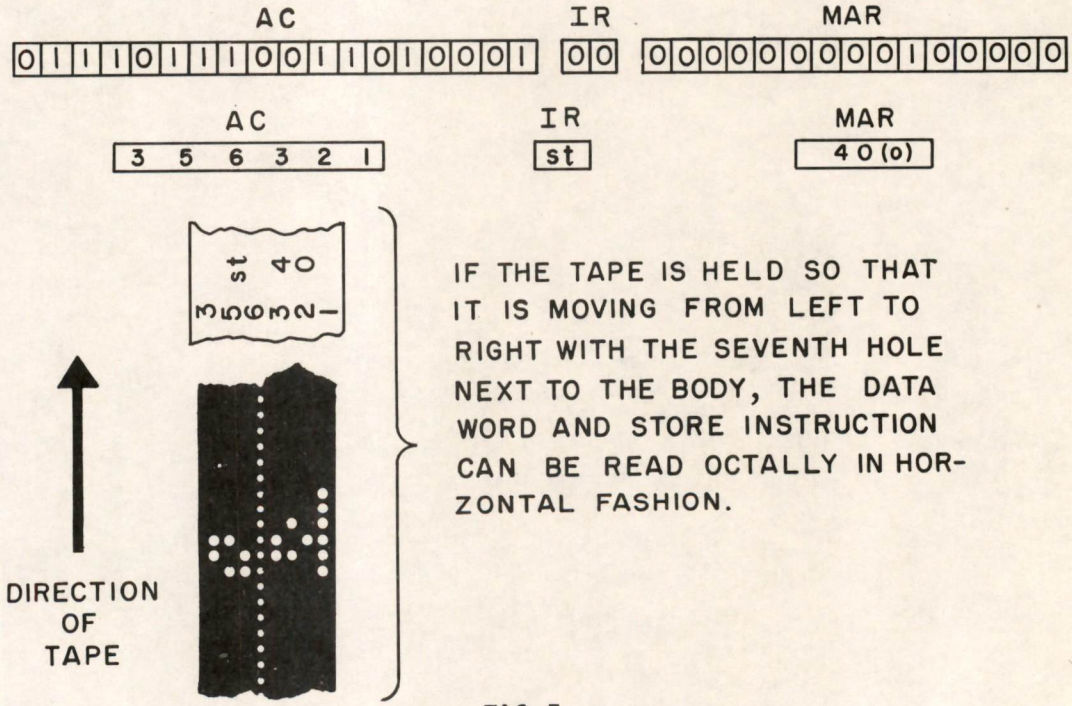



FIG. 4
TX-0 TOGGLE SWITCH STORAGE




EXAMPLE: STORE THE OCTAL WORD 356321 IN REGISTER 40 OCTAL

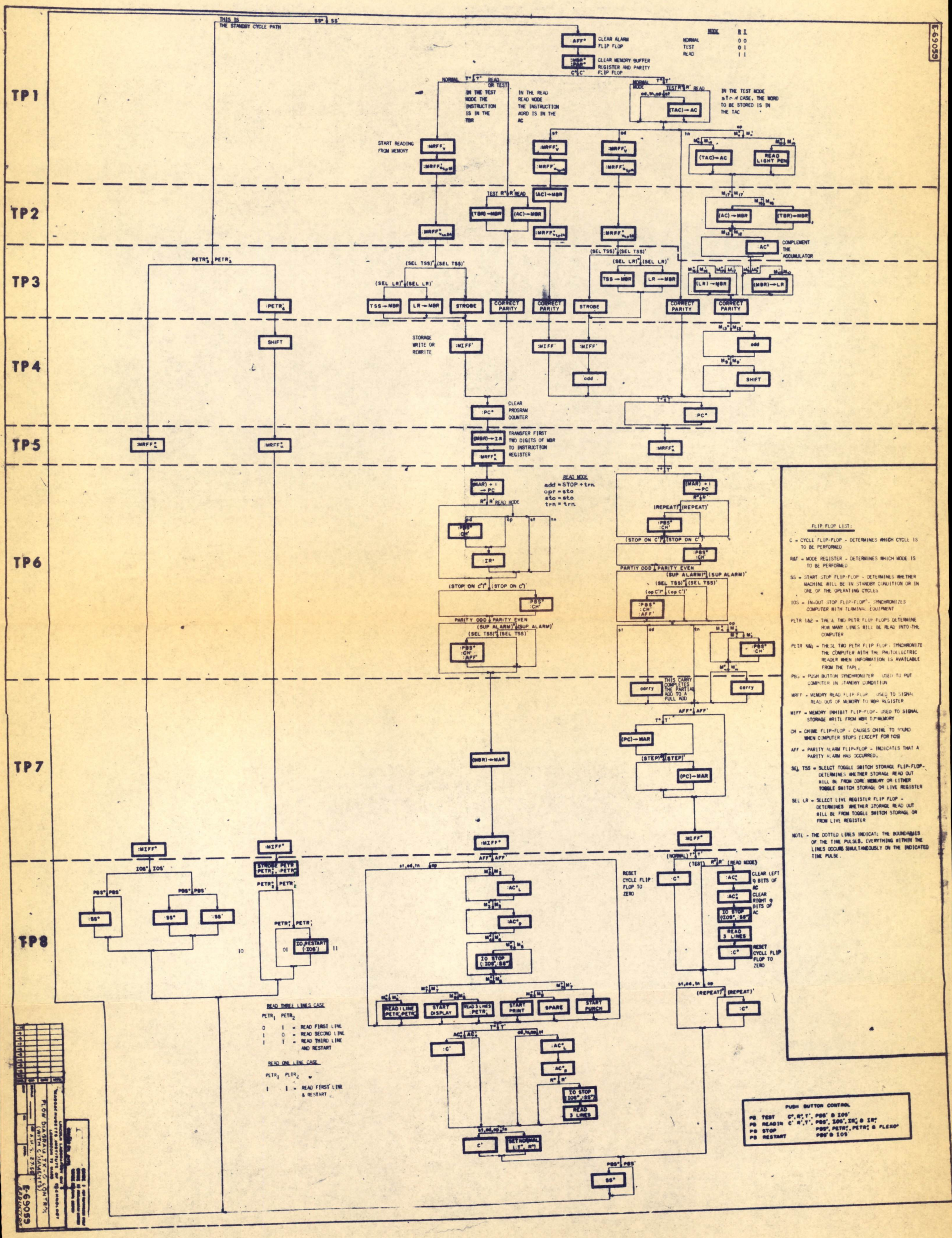



IF THE TAPE IS HELD SO THAT IT IS MOVING FROM LEFT TO RIGHT WITH THE SEVENTH HOLE NEXT TO THE BODY, THE DATA WORD AND STORE INSTRUCTION CAN BE READ OCTALLY IN HORZONTAL FASHION.

FIG. 5

TAPE LAYOUT FOR READ-IN MODE OF TX-0

A-68405


TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
THIS IS THE STANDBY CYCLE PATH
CLEAR ALARM FLIP FLOP
CLEAR MEMORY BUFFER REGISTER AND PARITY FLIP FLOP
MODE R I
NORMAL 0 0
TEST 0 1
READ 1 1
IN THE TEST MODE THE INSTRUCTION IS IN THE TBR
IN THE READ READ MODE THE INSTRUCTION WORD IS IN THE AC
IN THE TEST MODE st or tn CASE, THE WORD TO BE STORED IS IN THE TAC
START READING FROM MEMORY
(TAC) → AC
READ LIGHT PEN
(AC) → MBR
(TBR) → MBR
COMPLEMENT THE ACCUMULATOR
(SEL TSS)' (SEL TSS)
(SEL LR)' (SEL LR)
TSS → MBR
LR → MBR
STROBE
CORRECT PARITY
(LR) → MBR
(MBR) → LR
STORAGE WRITE OR REWRITE
odd
SHIFT
CLEAR PROGRAM COUNTER
(MBR) → IR
TRANSFER FIRST TWO DIGITS OF MBR TO INSTRUCTION REGISTER
(MAR) + 1 → PC
READ MODE
add = STOP + trn
opr = sto
sto = sto
trn = trn
(REPEAT)' (REPEAT)
(STOP ON C')' (STOP ON C')
PARITY ODD PARITY EVEN
(SUP ALARM)' (SUP ALARM)
(op C')' (op C')
THIS CARRY COMPLETES THE PARTIAL ADD TO A FULL ADD
carry
(PC) → MAR
(STEP)' (STEP)
(MBR) → MAR
IO STOP (IOS', SS')
READ 3 LINES
READ 1 LINE
START DISPLAY
START PRINT
SPARE
START PUNCH
RESET CYCLE FLIP FLOP TO ZERO
CLEAR LEFT 9 BITS OF AC
CLEAR RIGHT 9 BITS OF AC
IO, RESTART (IOS')
READ THREE LINES CASE
PETR1 PETR2
0 1 = READ FIRST LINE
1 0 = READ SECOND LINE
1 1 = READ THIRD LINE AND RESTART
READ ONE LINE CASE
PETR1 PETR2
1 1 = READ FIRST LINE & RESTART
FLIP FLOP LIST:
C = CYCLE FLIP-FLOP - DETERMINES WHICH CYCLE IS TO BE PERFORMED
R&T = MODE REGISTER - DETERMINES WHICH MODE IS TO BE PERFORMED
SS = START STOP FLIP-FLOP - DETERMINES WHETHER MACHINE WILL BE IN STANDBY CONDITION OR IN ONE OF THE OPERATING CYCLES
IOS = IN-OUT STOP FLIP-FLOP - SYNCHRONIZES COMPUTER WITH TERMINAL EQUIPMENT
PETR 1&2 = THESE TWO PETR FLIP FLOPS DETERMINE HOW MANY LINES WILL BE READ INTO THE COMPUTER
PETR 1&2 = THESE TWO PETR FLIP FLOPS SYNCHRONIZE THE COMPUTER WITH THE PHOTOELECTRIC READER WHEN INFORMATION IS AVAILABLE FROM THE TAPE.
PBS = PUSH BUTTON SYNCHRONIZER - USED TO PUT COMPUTER IN STANDBY CONDITION
MRFF = MEMORY READ FLIP FLOP - USED TO SIGNAL READ OUT OF MEMORY TO MBR REGISTER
MIFF = MEMORY INHIBIT FLIP-FLOP - USED TO SIGNAL STORAGE WRITE FROM MBR TO MEMORY
CH = CHIME FLIP-FLOP - CAUSES CHIME TO SOUND WHEN COMPUTER STOPS (EXCEPT FOR IOS)
AFF = PARITY ALARM FLIP-FLOP - INDICATES THAT A PARITY ALARM HAS OCCURRED.
SEL TSS = SELECT TOGGLE SWITCH STORAGE FLIP-FLOP - DETERMINES WHETHER STORAGE READ OUT WILL BE FROM CORE MEMORY OR EITHER TOGGLE SWITCH STORAGE OR LIVE REGISTER
SEL LR = SELECT LIVE REGISTER FLIP FLOP - DETERMINES WHETHER STORAGE READ OUT WILL BE FROM TOGGLE SWITCH STORAGE OR FROM LIVE REGISTER
NOTE - THE DOTTED LINES INDICATE THE BOUNDARIES OF THE TIME PULSES. EVERYTHING WITHIN THE LINES OCCURS SIMULTANEOUSLY ON THE INDICATED TIME PULSE.
PUSH BUTTON CONTROL
PB TEST C*, R', T', PBS' @ IOS'
PB READ IN C' R', T', PBS', IOS', IR; @ IR;
PB STOP PBS*, PETR1, PETR2 @ FLERO*
PB RESTART PBS' @ IOS
E-69059
FLOW DIAGRAM TX-0 CONTROL (WITH CYMBOLIC LOGIC)
LINCOLN LABORATORY OF MASSACHUSETTS INSTITUTE OF TECHNOLOGY

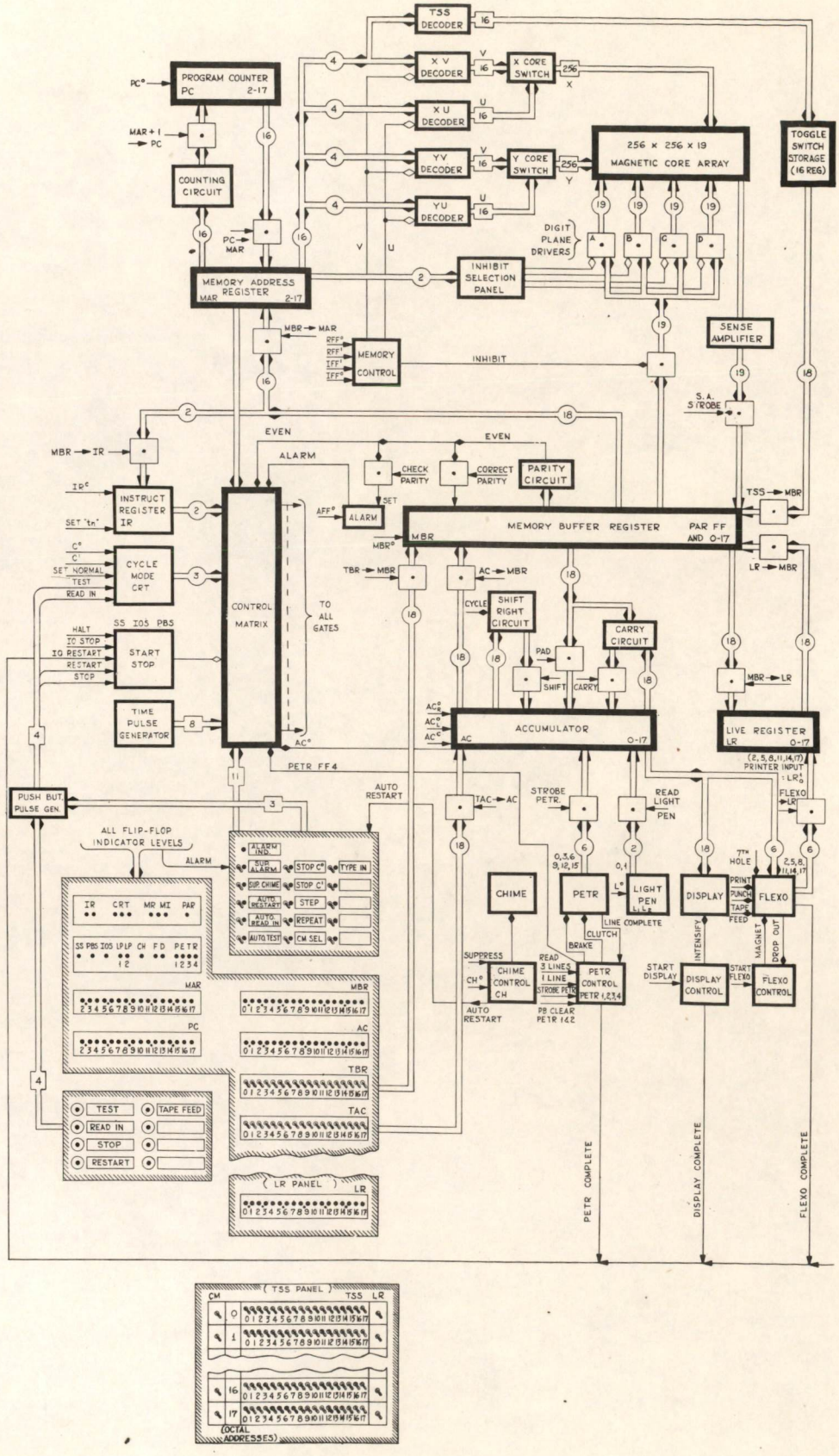



FIG. 7

BLOCK DIAGRAM, TX-0

D-47243

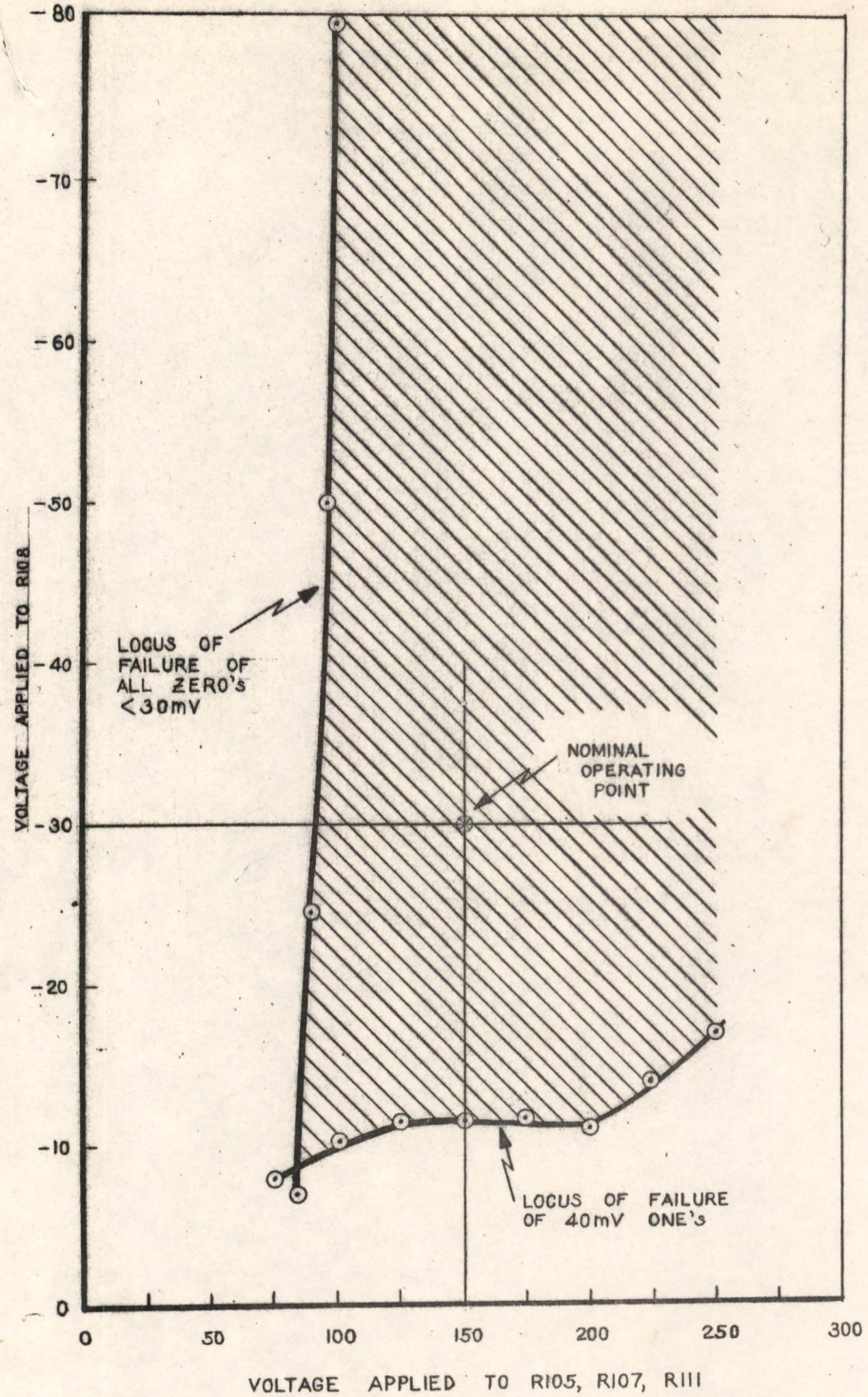



FIG. 25

MARGINAL CHECKING PLOT OF VOLTAGE APPLIED TO R108 vs VOLTAGE APPLIED TO R105, R107, R111.

SENSE AMPLIFIER #9, CHANNEL 3.
CLIPPING LEVEL ≅ 30 mV.