R. L. Best
D063

Memorandum 6M-4521

Sheet 1 of 5 Sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A LAPLACE TRANSFORM ANALYSIS OF PULSE BETA

To: Donald J. Eckl

From: Ralph C. Johnston Ralph C. Johnston

Date: August 21, 1957

Approved: D J Eckl

Abstract: The current gain of a common-emitter pulse amplifier is obtained for a half sine wave input. An analytic expression for the output current is obtained as a function of d-c gain, cutoff frequency, and pulse width. For pulse gains appreciably less than the d-c gains, the former is shown to be almost independent of the latter but directly proportional to the cutoff frequency.

RCJ/md

Distribution:

Barck, P.
Best, R.L.
Bradspies, S.
Cantella, M.J.
Corderman, C.L.
Davidson, G.A.
Eckl, D. J.
Fadiman, J.
Goodenough, J.B.
Gurley, B.M.
Johnston, R.C.
Kirk, C.T.
Kleinrock, L.
Konkle, K.
Langford, J.
Mitchell, J. L.
Neumann, L.
Olsen, K.H.
Papian, W.N.
Pugsley, J.
Raffel, J.
Savell, R.
Hughes, R.A.

Abstracts to the remainder of Group 63 Staff.

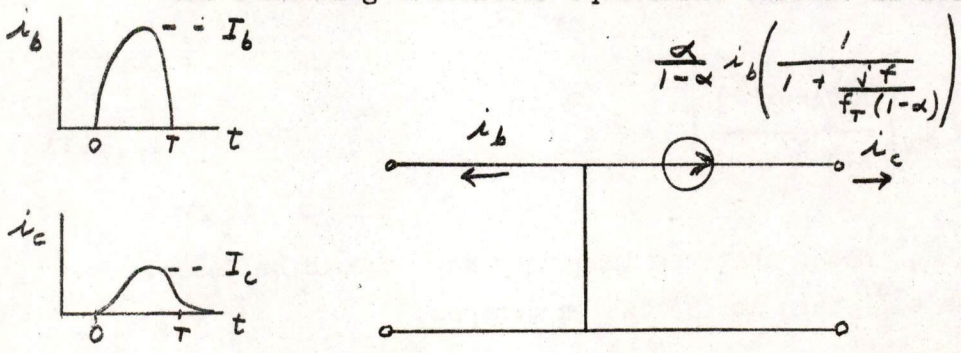
2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

A LAPLACE TRANSFORM ANALYSIS OF PULSE BETA

1. Introduction

Pulse beta or the common-emitter current gain with a half sine-wave input current pulse is of importance in pulse amplifier and gating circuits. It is not usually given in transistor specifications and so its relation to the common parameters of d-c gain and cutoff frequency is desirable.

The following transistor equivalent circuit is assumed.



Pulse beta is defined as follows:

$$\beta_{pulse} = \frac{I_c}{I_b} \qquad (1)$$

where I_b and I_c are peak values as shown above. The collector current generator is the product of the d-c beta, the base current, and a frequency response term which gives the magnitude and phase to a sinusoidal input. f_T is the cutoff frequency measured on the fh_{fe} test and equals[1] $\frac{2}{2.43} f_\alpha$. The common-emitter cutoff frequency is then $f_T (1-\alpha)$.

2. Laplace Transform Analysis

The procedure for solution is to convert the transfer function from frequency to the s domain by replacing jw by s (this establishes

---

1. Johnston, R.C., "Transient Response of Junction Transistors -II" Lincoln Laboratory 6M-4913,S-1, June 19, 1957, eq (109)(110)(106).

zero initial conditions), transform the input current, and take the inverse transform of the product by expansion into partial fractions.

$$I_c(s) = \frac{\alpha}{1-\alpha} I_b(s) \frac{1}{1 + \frac{s}{2\pi f_T(1-\alpha)}} \tag{2}$$

$$I_b(s) = \mathcal{L} I_b(\text{Sin } \tfrac{\pi t}{T}) \left[u(t)-u(t-T)\right]$$

$$= \mathcal{L} \, \mathcal{I}_m I_b \, e^{j\pi t/T} \left[u(t)-u(t-T)\right]$$

$$= \mathcal{I}_m \left[\frac{I_b(1+e^{-sT})}{s-j\,\pi/T}\right] \tag{3}$$

The symbol, $\mathcal{I}_m$, means that the imaginary part should be taken. For $0 < t < T$, the e^{-sT} term in (3) can be dropped.

Next we substitute (3) in (2) and expand in partial fractions.

$$I_c(s) = \mathcal{I}_m \left(\frac{\alpha}{1-\alpha}\right) I_b \left(\frac{1}{1 + \frac{s}{2\pi f_T(1-\alpha)}}\right)\left(\frac{1}{s-j\pi/T}\right) = \mathcal{I}_m \left(\frac{K_1}{1 + \frac{s}{2\pi f_T(1-\alpha)}} + \frac{K_2}{s-j\pi/T}\right) \tag{4}$$

$$K_1 = \frac{(-1)\left(\frac{\alpha}{1-\alpha}\right) I_b}{2\pi f_T(1-\alpha) + j\pi/T}$$

$$K_2 = \frac{\left(\frac{\alpha}{1-\alpha}\right) I_b}{1 + \frac{j}{2Tf_T(1-\alpha)}}$$

The inverse transform of (4) is

$$i_c(t) = \mathcal{I}_m \left[2\pi f_T(1-\alpha)K_1 \, e^{-2\pi f_T(1-\alpha)t} + K_2 \, e^{j\frac{\pi t}{T}}\right]$$

$$= \left(\frac{\alpha}{1-\alpha} I_b\right)\left[\frac{\frac{1}{2Tf_T(1-\alpha)}}{1+\frac{1}{\left[2Tf_T(1-\alpha)\right]^2}} e^{-2Tf_T(1-\alpha)\frac{\pi t}{T}}\right.$$

$$\left. + \frac{1}{\sqrt{1+\frac{1}{\left[2Tf_T(1-\alpha)\right]^2}}} \operatorname{Sin}\left(\frac{\pi t}{T} - \psi\right)\right]\left[u(t) - u(t-T)\right] \quad (5)$$

where

$$\psi = \operatorname{Tan}^{-1} \frac{1}{2Tf_T(1-\alpha)}$$

For $T < t < \infty$ the e^{-st} term is retained

$$I_c(s) = \mathcal{L}\left(\frac{\alpha}{1-\alpha} I_b\right)\left(\frac{1}{1+\frac{s}{2\pi f_T(1-\alpha)}}\right)\left(\frac{1+e^{-st}}{s-j\,\pi/T}\right) = \mathcal{L}\left[\frac{K_1}{1+\frac{s}{2\pi f_T(1-\alpha)}} + \frac{K_2}{s-j\frac{\pi}{T}}\right]$$

$$K_1 = \frac{\alpha}{1-\alpha} I_b \left(\frac{(-1)(1+e^{2\pi Tf_T(1-\alpha)})}{2\pi f_T(1-\alpha) + j\,\pi/T}\right) \qquad K_2 = 0$$

$$i_c(t) = \left(\frac{\alpha}{1-\alpha} I_b\right)\left[\frac{\frac{1}{2Tf_T(1-\alpha)}}{1+\frac{1}{\left[2Tf_T(1-\alpha)\right]^2}} \left(1+e^{2\pi Tf_T(1-\alpha)}\right) e^{-2\pi Tf_T(1-\alpha)\frac{t}{T}}\right] \quad (6)$$

$$\left[u(t-T)\right]$$

The result may be expressed in more compact form by letting

$$2Tf_T(1-\alpha) = \frac{1}{x}$$

and

$$\frac{t}{T} = \tau$$

$$i_c(T) = \begin{cases} \frac{\alpha}{1-\alpha} I_b \left[\frac{x}{1+x^2} e^{\frac{-\pi\tau}{x}} + \frac{1}{\sqrt{1+x^2}} \sin(\pi\tau - \psi) \right] & 0 < \tau < 1 \qquad (7) \\ \frac{\alpha}{1-\alpha} I_b \left[\frac{x}{1+x^2} (1+e^{-\pi/x}) e^{\frac{-\pi}{x}(\tau-1)} \right] & \tau > 1 \end{cases}$$

where $\psi = \mathrm{Tan}^{-1} x$

This function is plotted in Fig. 1 for x = 0, 1, and 3. The sinusoidal and exponential components are shown dotted.

3. Pulse Beta Approximation

It is desirable to have a simple expression for pulse beta. By adding the peak value of the sine term to the value of the exponential term at $\tau = 1$ an approximate formula is obtained which is 3 percent low at x = 1 and has less error for other values of x.

$$\beta_{pulse} = \frac{\alpha}{1-\alpha} \left(\frac{x}{1+x^2} e^{-\pi/x} + \frac{1}{\sqrt{1+x^2}} \right) \qquad (8)$$

A useful form may be obtained for large x.

$$\beta_{pulse} = \frac{\alpha}{1-\alpha} \frac{2}{x} = \frac{\alpha}{1-\alpha} 4Tf_T(1-\alpha)$$

$$\cong 4Tf_T \qquad (9)$$

For x between 3 and 12 the formula

$$\beta_{pulse} \cong 3Tf_T \qquad (10)$$

is about 10 percent accurate. Thus it is seen that when the pulse beta is less than say 1/3 the d-c beta, it is almost independent of d-c gain and directly proportional to the common-base cutoff frequency.

Attachment

Drawing No. B-82690

R. S. Best

B063

Memorandum 6M-4521, S-1

Sheet 1 of 3 Sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A LAPLACE TRANSFORM ANALYSIS OF PULSE BETA

To: Donald J. Eckl

From: Ralph C. Johnston Ralph C. Johnston

Date: September 12, 1957

Approved: DJE

Abstract: Figure 1 is included, which was omitted by mistake from the main body of the note. The results of an experimental verification by K. Konkle are given and discussed.

RJC/md

Distribution:

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Olsen, K.H.
Papian, W.N.
Pugsley, J.
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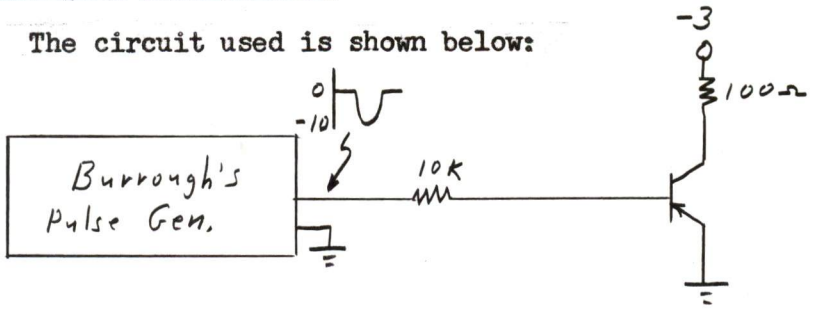
2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

A LAPLACE TRANSFORM ANALYSIS OF PULSE BETA

4. Experimental Verification

The circuit used is shown below:



The peak base current is 1 ma. giving a maximum measurable value for pulse beta of 30.

The main difficulty in checking the theory is that the "constants" f_T and α are not. Actually f_T varies about as the fourth root of collector voltage and drops off for emitter currents below a few tenths of a ma. The value of α tends to decrease with collector current, especially on the surface barrier transistor.

Type	No.	f_T, mc	β_o	x	β pulse	
					Calc.	exp.
MAT	ST276	42	40	5.83	11.3	11.6
MAT	ST1111	55	207	11.2	17.7	17.3
SBT	214	34	11	1.72	6.65	6.0

Figure 2. Summary of Experimental Verification

Figure 2 gives the results of measurements on three transistors by K. Konkle. It is felt that the agreement between calculated and experimental values is quite good considering the measurement problems discussed previously.

Attachment
Drawing No. B-82690

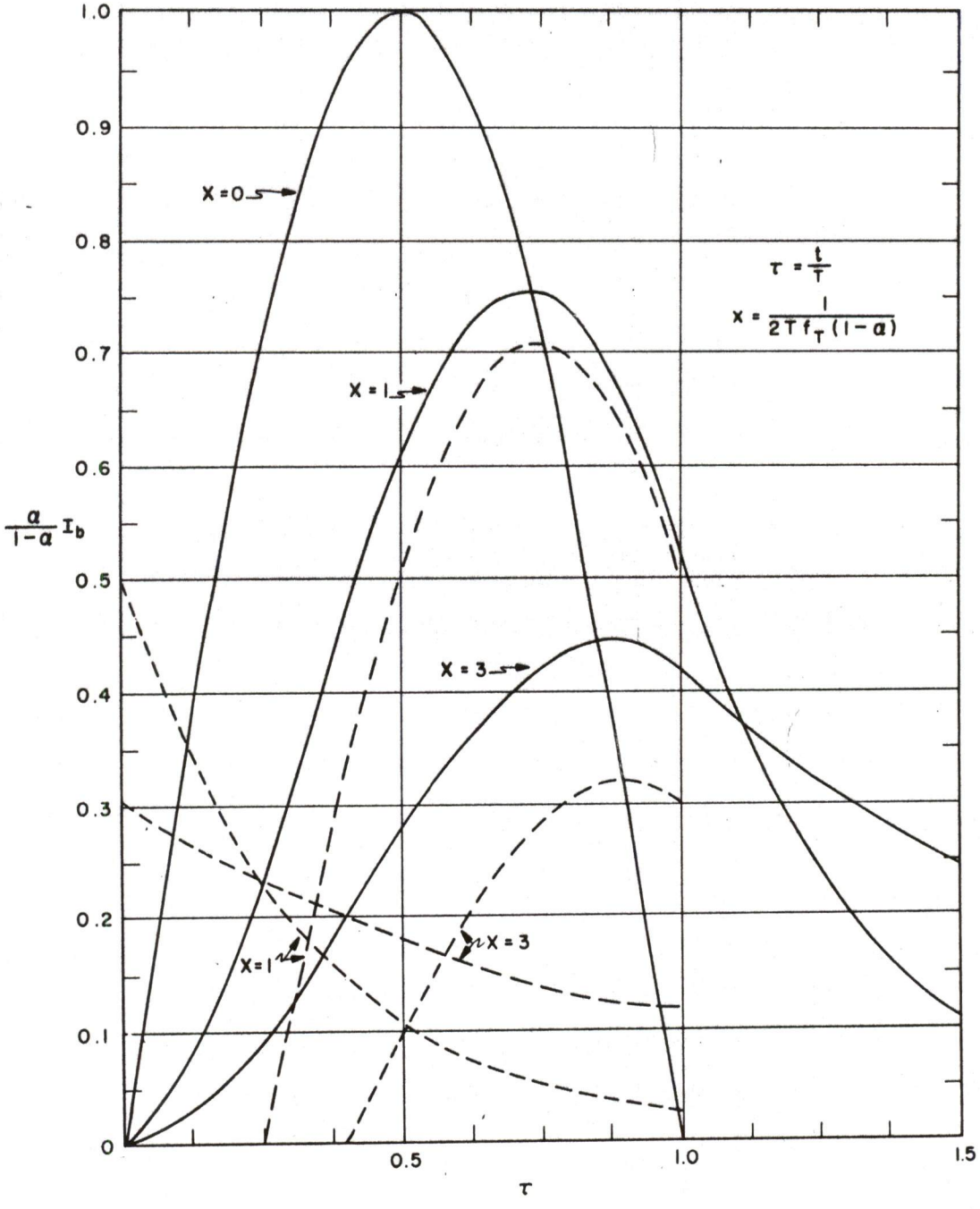


FIG. 1

COMMON – EMITTER RESPONSE TO HALF SINE WAVE PULSE

B-82690

K H Olsen

Memorandum 6M-4544

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: Electronically Variable Power Supply

To: Donald J. Eckl

From: Edmund U. Cohler

Date: 30 November 1956

Approved: D. J. Eckl
Donald J. Eckl

Abstract: The design considerations for a supply capable of supplying from 50 millivolts to 40 volts to a 12 ohm load are presented. The supply is unique in being capable of excellent regulation, electronic control of output by means of a variable reference, and fast response to changes of electronic input. The supply is reversible with respect to ground (it may not be operated floating). The input requirement from the electronic standard is about 5 microamperes. The supply employs transistor regulators and semiconductor rectifiers for maximum efficiency at these low voltages and high currents. A supplement to this note will discuss the measured characteristics of this supply.

Distribution List

Bradspies, S.
Brown, D. R.
Coffin, S. T.
Davidson, G. A.
Eckl, D. J.
Fadiman, J. R.
Fergus, P. A.
Gurley, B. M.
Hudson, R. W.
Hughes, R. A.
Jahn, R. C.
Kirk, C. T.
Olsen, K. H.
Norman, C. A.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

I. INTRODUCTION

Requirements

A supply was desired which would provide a means for automatic marginal checking of a computer. This application required the following features.

a. Output voltage to be electronically variable from close to zero to +40 volts.

b. The response should be much less than 1 millisecond.

c. A minimum load resistance of close to 10 ohms.

d. Ambient conditions from 20°C to 55°C should not cause deterioration or failure.

e. Regulation should be on the order of 0.2 volts.

f. About 5 microamperes should be drawn from the electronic standard.

g. Either end of the supply should be capable of being grounded.

Basic Design

As a starting point a supply designed for TX-0 by Robert Hughes was used. The circuit of this supply is shown in Fig. 1. Excellent as this supply was, it needed extensive modification to meet the above requirements. The dissipation in the series regulator transistors has been kept to a minimum in the TX-0 supply by reducing the input voltage with tapped transformers and a range switch, (S2). This method could not be used in the new supply since electronic variation was desired. The maximum load current to be supplied is four times as great since the load resistance is the same but the maximum voltage is four times as great. Thus the power capabilities are multiplied 16 times. Voltages in the regulator are also higher which in some cases would overrun the transistor capabilities if the design were unchanged. Finally, the input circuit must be modified to permit a grounded reference with either end of the supply grounded.

II. DESIGN

Series Regulators

The series regulators were tackled first. They would be required to handle considerably more power than they had in the previous supply. The straightforward approach to solution of this problem was to provide enough series regulators of sufficient rating to pass the desired current at the required voltage. It can easily be shown that the dissipation required in such a regulator is:

$$V_s^2/4R_{ls} = P_{max} \qquad (1)$$

where V_s is the maximum voltage of the unregulated supply, and R_{ls} is the sum of the internal resistance of the unregulated supply and the load resistance. In the case of a negligible supply resistance and a total load of 10 ohms on a 56 volt supply, the dissipation, P_{max}, is 78.4W. As can be seen from Figure 3 the maximum voltage of unregulated supply for an input of 122.5 volts is 56 volts. It was felt that the AC input tolerance could be set at 115 volts + 7.5 - 10.0 volts because of the closer control on overvoltage inherent in the distribution system.

The transistors to be used in the series regulator position were to be Minneapolis-Honeywell's H-7's[1]. These transistors may be operated at a junction temperature of 95°C. Thus, at an ambient of 55°C we may allow a drop of 40°C in the thermal resistance from junction to ambient.

Assuming a total thermal resistance of 2.55°C/watt, 2.2°C/w for the H-7 and 0.35°C/w for the dissipator[2], we then require 5 transistors in the series regulator.

CURRENT EQUALIZATION

In order to maintain equal currents in all five series regulator transistors, small resistors were inserted in series with each emitter. The collector current in the active region is given by

$$I_c = I_B\beta = \frac{V_B\beta}{R_{input} + \frac{R_{EX}}{1-\alpha}} \qquad (2)$$

where R_{EX} is the extermal emitter resistance and R_{input} is the grounded emitter input resistance of the transistor.

---

1. Minneapolis Honeywell 2N57 power transistor specifications sheet Form number TR17

$$I_c \approx \frac{V_B}{\frac{R_{inp}}{\beta} + R_{EX}} \tag{3}$$

$$\frac{I_{c\ min}}{I_{c\ max}} \approx \frac{R_{EX} + \frac{R_{inp\ min}}{\beta\ max}}{R_{EX} + \frac{R_{inp\ max}}{\beta\ min}} \tag{4}$$

Actually Eq. 4 gives an extremely conservative estimate since the input resistance is very closely associated with beta. A more realistic estimate of the variation might be obtained from

$$\frac{I_{c\ min}}{I_{c\ max}} \approx \frac{R_{EX} + \frac{R_{inp\ min}}{\beta_{min}}}{R_{EX} + \frac{R_{inp\ max}}{\beta\ max}} \tag{5}$$

Let us then compute the ratio of the minimum to maximum current per transistor, in terms of Eq. 5.

$r = \frac{I_{min}}{I_{max}}$; n = number of transistors in the series regulator.

A = Average current/transistor

I = Maximum current in any one transistor.

The worst case will occur where all of the transistors except one are carrying the minimum current and the other is carrying the maximum current. Then:

$$\text{Total current} = nA = (n-1)r\ I + I \tag{6}$$

$$I/A = \frac{1}{r + \frac{1-r}{n}}$$

---

2. See 6M-4390, Heat Dissipator Characteristics, E. Cohler, 9 July 1956

If we now substitute in Eqs. 5 and 7 the value of R_{EX} shown in Fig. 2. and the known variation of R_{inp} for the H-7[1]. at 560 ma, we find: r = .84 and I/A = 1.15. The final rated load, may then be calculated to allow a 15 percent increase in transistor dissipation over the average dissipation.

SERIES FEED TO SERIES REGULATORS

Series feed, rather than shunt feed, was used for the transistor supplying the series regulators. This allowed a decrease of beta in the power requirements from the series regulator stage to the feeding stage. Thus, beta being 80 minimum in the H-7, the requirement for this stage is 78.4/80 = 0.98 watts. Series feed meant using an n-p-n transistor in the feeding stage, and the best available in the desired dissipation range was the Sylvania 2N142[3]. In fact, this transistor attached to the chassis (for a heat sink) is rated at 4.0 watts at 25°C derated 0.1 watt/°C or 1.0 watt at 55°C. Moreover, the transistor will be forced-air cooled which will further increase its capacity.

ZERO OUTPUT LEVEL

In order to get the output voltage down to low levels, it is necessary that the off current in the H-7's is a minimum. To accomplish this one must also reduce the off current in the 2N142 to a very low level. The positive and negative biasing arrangements involving external supplies and R1 and R2 achieve this result. By biasing the bases in the reverse direction for the off condition, one achieves leakage currents which are no more than a few times the grounded base I_{co} for the transistor. Measurements of the low value of output current run about 2.5 ma for a typical set of 2N57's (H-7's should be better since their 60 V. maximum I_{co} is one-half that for the 2N57). This will then give a 50 millivolt minimum output for a 20 ohm load.

AMPLIFIER

The rest of the amplifier is designed with the object in mind of requiring about 5 microamperes from the standard to completely cut off the output transistors. The two input transistors are in series to provide

3. Sylvania Engineering Data Service. Advance Data on the 2N142 Feb. 8, 1956

double the voltage capability. The pair of 33 ohm bleeder resistors serve both to provide a bias for the voltage division in the input transistors and to keep the unregulated supply voltage down. Of course, with a negative standard (when the positive side of the supply is grounded) the two 4.7K resistors provide the voltage division for the input transistors (2N182's).

PROTECTION

For economic reasons it is wise to protect this supply, in case of fan failure or excessive ambient temperature. If either of these conditions occurs the thermal switch will open and prevent operation of the H-7's above their rated junction temperature. In case of a current overload the fuse in the transformer primary will open. In either instance of failure, a neon light on the panel will flash, warning of the burn-out.

To provide the thermal protection, the thermal switch has been put at the warmest point of the chassis (under fan failure conditions) and set to switch off at 55°C.

REVERSIBILITY

In order to reverse the polarity of the supply, relays are provided to change the location of the ground. This process runs into two problems: 1. The mercury relays, which are used for reliability, are of the make-before-break type, and sufficient interlocking must be provided to assure that the supply is not shorted while reversing. This is done by the circuit shown, provided the difference between the pull up or break time of two different contacts on the same relay is less than the pull up time of any contact on the relay. 2. The input for the standard must be such as to allow for either a positive or negative standard to be grounded. There was no simple way found for accomplishing this type of input, so two separate inputs were provided for the two standards. These inputs must then be switched when the supply is reversed.

SYSTEMS

The control of the supply from the system point of view will be discussed more fully in the notes on the decoder and total system. How-

ever, it might be well to mention the speed of response here as a supply characteristic. The design set forth above has not yet been tested under various load conditions: however, the prototype supply was modified by reduction of capacities which brought the response to changes in the standard voltage to well below 1 millisecond. The only other important response time of the supply is the time required to switch polarities. In switching from plus to minus (and in returning to plus), at least two relay times will be used up. For the mercury relays used this will require 20 to 30 milliseconds. Fortunately, this switching is done much less often than the voltage switching.

LIMITATIONS

As mentioned before, the supply load must be kept to 15 percent less than the load presented by 10 ohms. Thus, the rated load is 12 ohms. Moreover, a maximum load of 100 ohms is specified to allow the supply to go to 1/4 volt. Any higher resistance loads must be padded. In addition, no negative current can be supplied, that is, no current can be supplied in a direction opposite to the voltage. This is a basic characteristic of supplies using unilateral series regulators. The ambient temperature of the supply must be kept below 55°C. The resistance of the standard should be high enough to limit the surge currents resulting from sudden change of voltage. A resistance of 5K is sufficient for this purpose and will cause no appreciable error in the standard voltage under load.

SUGGESTIONS FOR FURTHER WORK

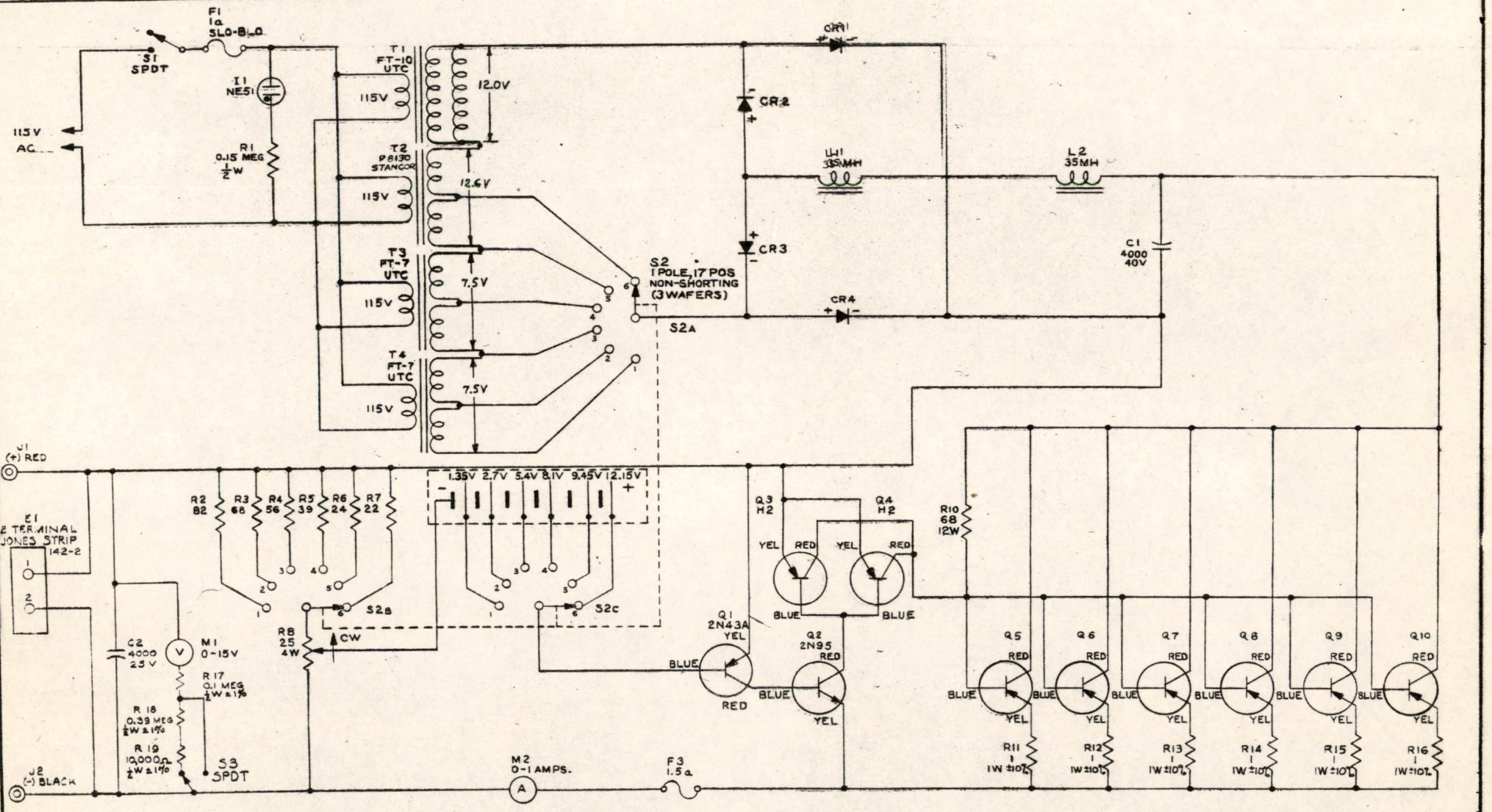
Consideration might be given to the following as improvements or tests to be made on the above design: 1. Thorough tests of regulation under load, operation of the thermal switch, response under various conditions of load, and accuracy of output for given standard characteristics. 2. Replacement of the single 2N142 by a series pair of 2N142's to provide sufficient voltage rating. 3. Physical layout of the supply, including location of various associated devices such as the variable standard and the switching circuitry.

E. U. Cohler / RW Hudson
Edmund U. Cohler

EUC:bac
Attachments: Fig. 1 - 15 volt 1 amp power supply Mod I TE Drawing #C63605
Fig. 2 - Electronically variable power supply Dwg. #C67152
Fig. 3 - Output vs. Input, electronically variable power supply. (Unregulated Supply) Dwg. #A67151

C-63605

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, 2W, ±5%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. CONNECTORS ARE DCL #046-11.
2. CR1 THRU CR4 ARE SILICON DIODES, IN347.
3. Q5 THRU Q10 ARE 2N57.

DRAWING REFERENCES:
ASSEMBLY: E-64915
PARTS LIST: PL-64915

FIG. 1

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DRB 1-25-56 DATE:

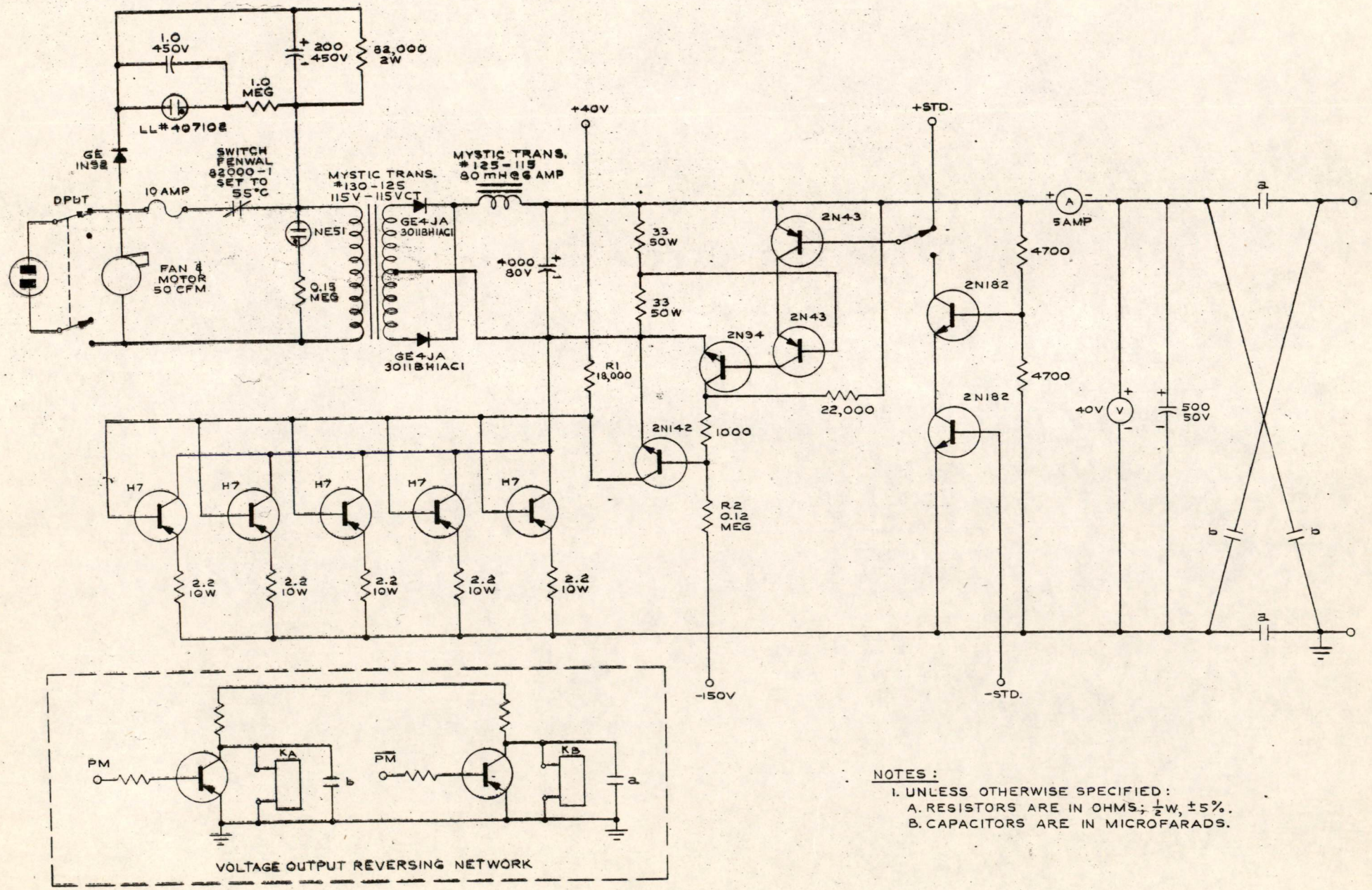
ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC, 15 VOLT 1 AMP
POWER SUPPLY MOD I, TE

SCALE: —— DR. B. LOFGREN 11-12-55
ENG. 11-29-55 CK. 11-23-55 APPD.
C-63605

CHG.	CN#	DATE	APPD.
-1	78135	2-10-56	
-2	78193	3-2-56	



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; $\frac{1}{2}$W, ±5%.
   B. CAPACITORS ARE IN MICROFARADS.

FIG. 2

ELECTRONICALLY VARIABLE POWER SUPPLY

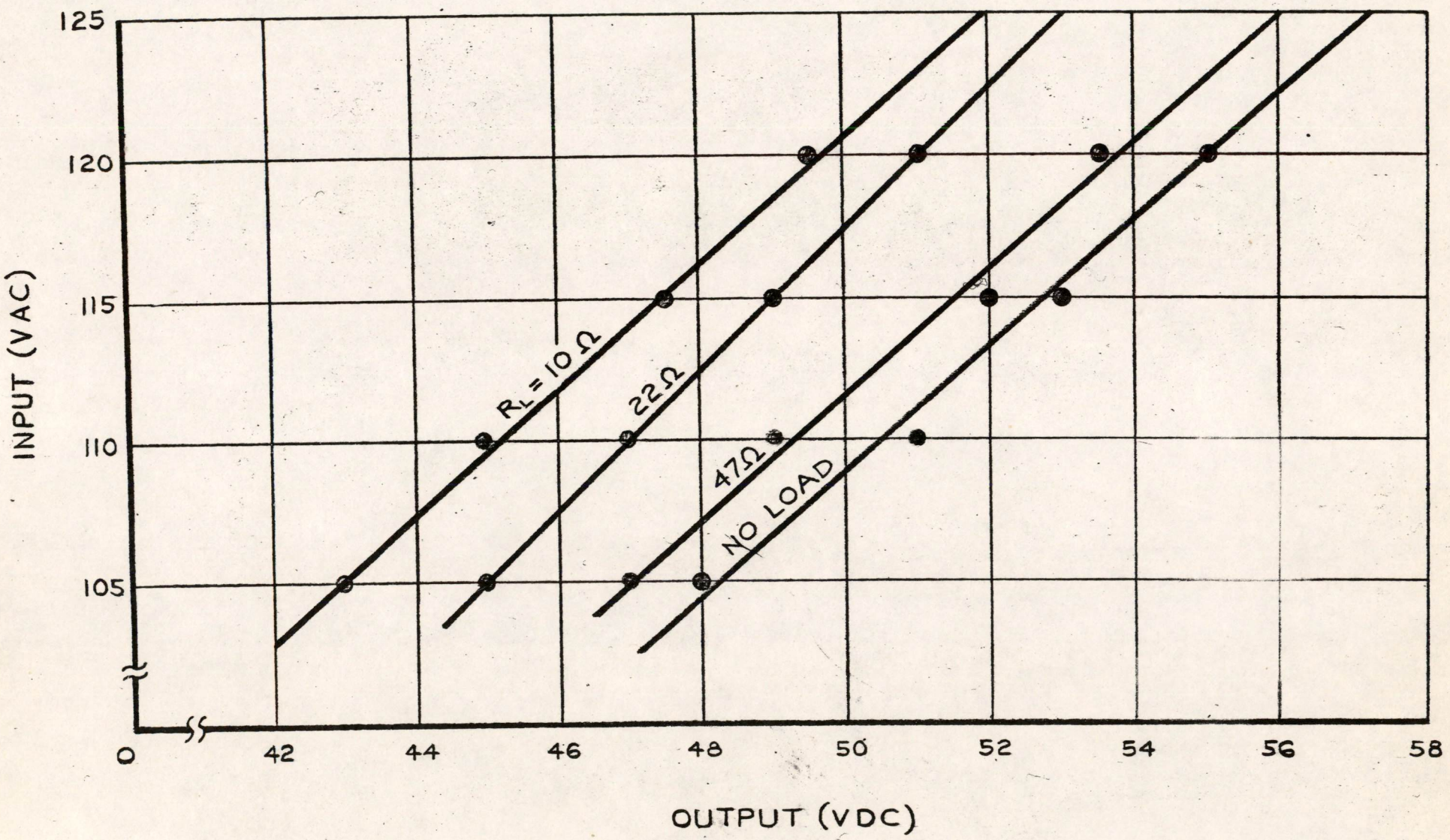


FIG. 3

OUTPUT vs INPUT ELECTRONICALLY VARIABLE POWER SUPPLY (UNREGULATED SUPPLY)

K. H. Olsen

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: A PRINTED WIRE MEMORY PLANE

To: W. N. Papian

From: E. A. Guditz

Date: September 10, 1956

Approved: J. L. Mitchell
J. L. Mitchell

Abstract: A 4 x 4 memory plane, made entirely with printed wiring, has been constructed and successfully operated. It demonstrates the techniques for making larger units which are the electrical equivalent of hand-sewn memory planes. The practical limit in size for planes made by this method is not yet known.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Introduction:

Memory planes constructed to date comprise cores and wires sewn in various configurations and strung in a suitable frame. Such planes are highly satisfactory from an operational point of view, but present some undesirable problems in fabrication. Not the least of these is the need for highly-skilled workers to sew the conductors through the cores. The object of the work reported here was to produce a plane which contained no hand-sewn wires. This was successfully accomplished in the form of a small 4 x 4 plane with 16 cores, four windings linking each core, and 128 dip-soldered connections. Two such planes have been made to date, and two more are being constructed. The nature of this experimental plane can best be understood by referring to the accompanying drawings and photographs while reading the text.

The Assembly:

Figure 1 is an exploded view of a segment of a printed plane of this type. Sheets 20 and 40 formed of phenolic have printed wiring on their outer surfaces. Sheet 30 serves as a spacer layer for positioning the cores. Base 10 with posts 11 serves as a jig to properly orient the sheets during the assembly operations.

The steps in construction are as follows:

Sheet 20 with the printed wiring facing down is placed upon base 10. Then sheet 30 is placed over sheet 20. Next, cores 50 are positioned in the holes of sheet 30. This may be done by automatically vibrating the cores into position. A surplus of cores may be applied with the excess being brushed off after all of the holes have been automatically filled. Next, sheet 40 is applied with the printed wiring facing up. At this point, the cores are sandwiched between the two sheets containing printed wiring, and the pegs 60 forming the circuit connections between the two layers of printed planes are now inserted. If desired the pegs may be attached to a strip in comb-like fashion as shown in Figure 4 so that the pegs for an entire line of cores may be inserted at once. The completed assembly may now be removed from base 10 and dip soldered on both sides to make permanent connections. The solder forms fillets at the junctions between conducting lines on the pegs and printed wire lines. These are shown in the photograph, F-3248.

The detailed paths of the x, y digit and sense windings are shown in the accompanying drawings SB-60322, SB-60321, SB-60324, and SB-60323 respectively. Actual conducting paths for all windings are shown in SC-60365 and in photographs F-3203 and F-3204.

These conducting circuit paths may best be understood by continued reference to Figure 1. The wiring circuit for a row or "x" line will be considered first. Line 1 on sheet 20 connects with line 1B on peg 60. This conducting line goes through core 50 and connects with line 1C on sheet 40. Line 1C connects with line 1D on peg 60B. Line 1D goes through core 50B and connects with line 1E on

sheet 20. This conducting path continues on in a similar fashion for the rest of the row.

To illustrate a "Y" line, or a column circuit, line 2 on sheet 20 connects with line 2B on peg 60. Line 2B goes through core 50 and connects with line 2C on sheet 40. Line 2C connects with line 2D on peg 60C. Line 2D goes through core 50C and connects with line 2E on sheet 20. Line 2 continues on in a similar fashion for the rest of the column. It will be noted that while the initial appearance of the printed wire sandwich is different from that of the conventionally wired memory, the effective electrical paths for the rows and columns are identical with those obtained by threading wires through the rows and columns of a conventional memory. The remaining printed circuits may be traced out in a manner analogous to that used for the row and column circuits. These are the sense winding starting at line 3 and the inhibit winding starting at line 4, and are the overall electrical equivalent of those windings in a conventionally constructed memory.

However, since it is difficult if not impossible to achieve a diagonally wired sense winding with this type of printed wire layout, the sense winding is rectangular in format. The cancellation of pulses from half-selected cores and air flux pickup normally accomplished by the diagonal format of the sense winding in conventionally wired memory planes is achieved by appropriate interconnection of rectangular subsections of the printed wire plane. Thus if two appropriately chosen quadrants are connected in one polarity and the other two quadrants in the opposite polarity, any row or column will have one-half of its cores sensed in one polarity and one-half sensed in the opposite polarity, and also cancellation of air flux pickup will be effected. The interconnection of these quadrants is shown in Figure 5. For convenience in wiring layout, the digit winding is also printed in quadrants as is shown in Figure 6. Figure 3 shows how sheet 30 is made thinner than the memory cores to permit cooling the plane by passing air through it sideways.

The core density for this type of construction is the same as for planes in the MTC and TX-0 memories. This design does, however, reduce the thickness of the memory plane. The major obstacle to be overcome in making larger planes of this type is control of the dip-soldering operation. Even in the 4 x 4 size the operator technique is very important. If larger numbers of junctions can be simultaneously soldered, then this could be a practical way to make a printed plane.

The first plane of this type to be completed has been operated in Memory Test Setup VI. It has output waveforms and operating margins comparable to conventional hand-wired memory planes.

E. A. Guditz

EAG:jd
Attachments:

B-67164	A-66029	A-67156	SB-60322	SB-60321	SB-60324
SB-60323	SC-60365	A-67077	A-67157	A-67074	A-67075

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ALL PERSONS LISTED ABOVE ARE TO RECEIVE COMPLETE MEMO.

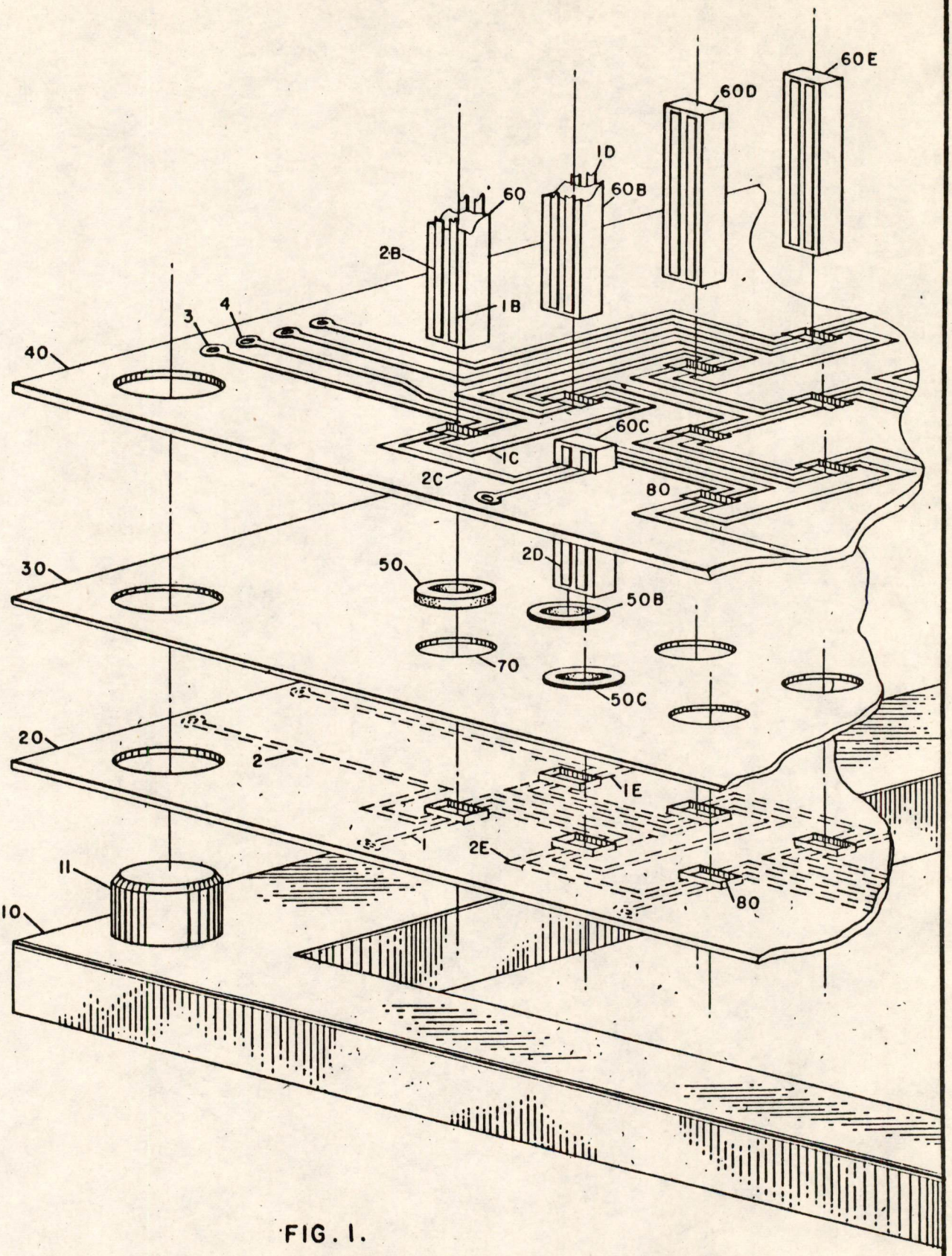


FIG. 1.

EXPLODED VIEW, 4X4 PEG-TYPE PRINTED PLANE

B-67164

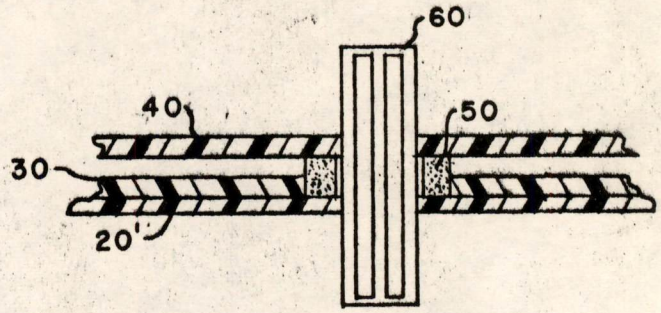


FIG. 3.

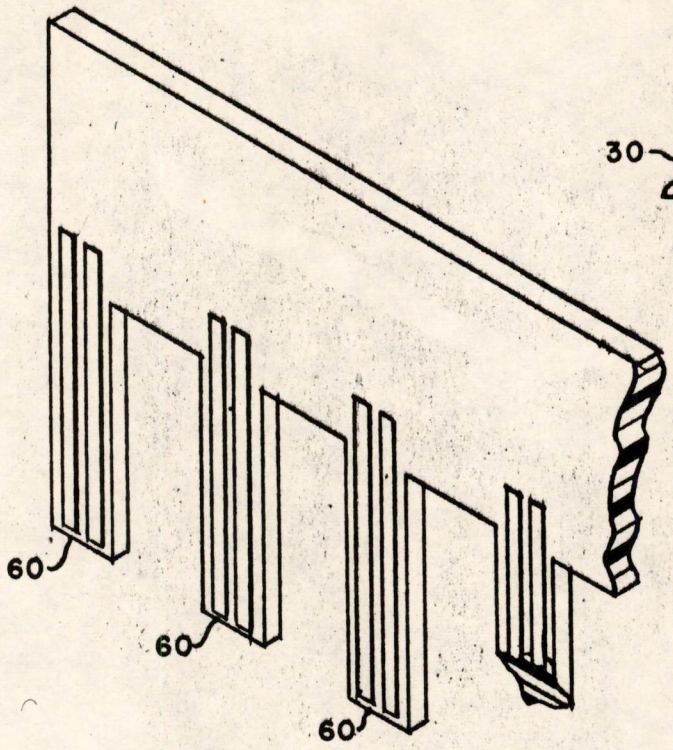
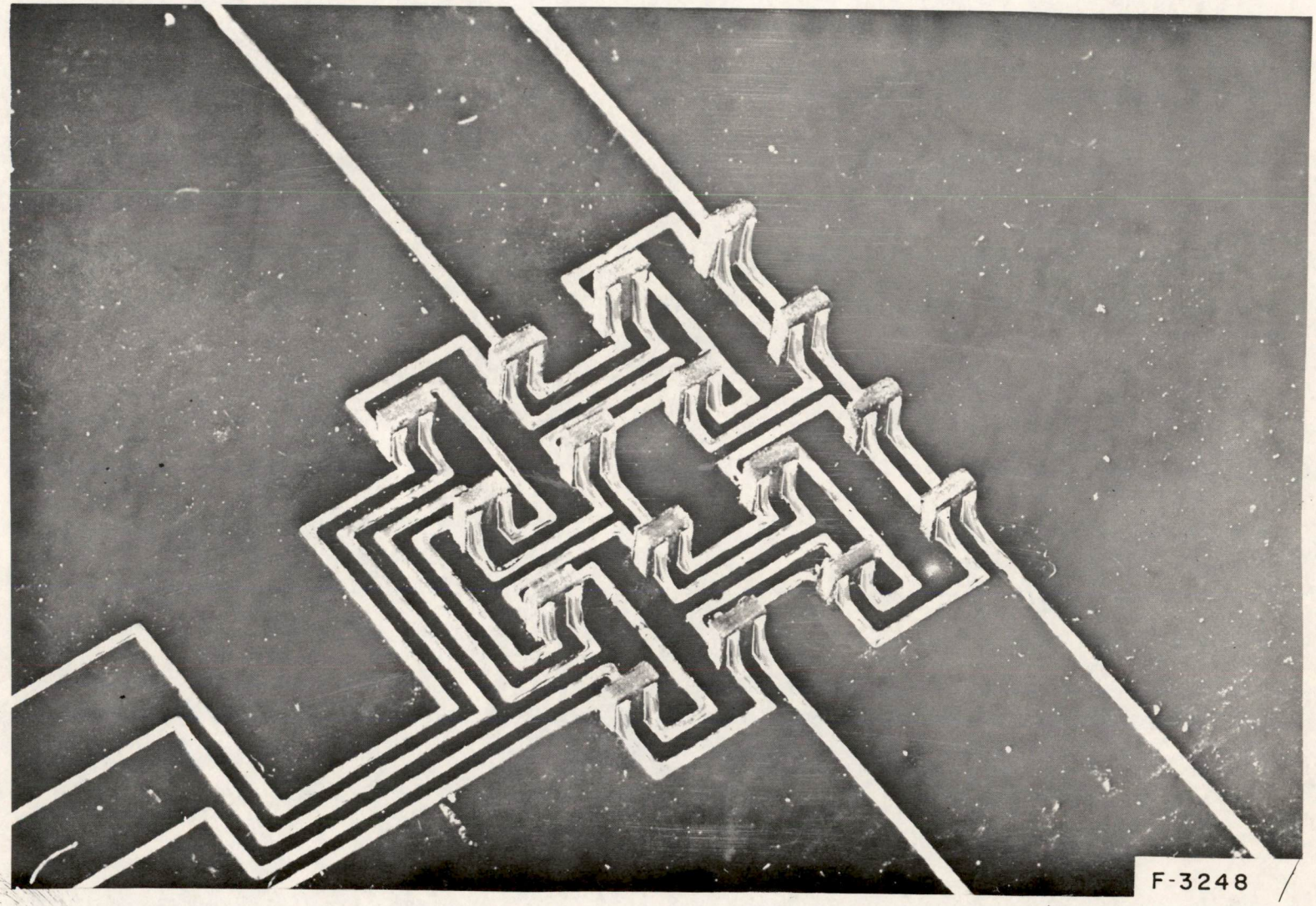


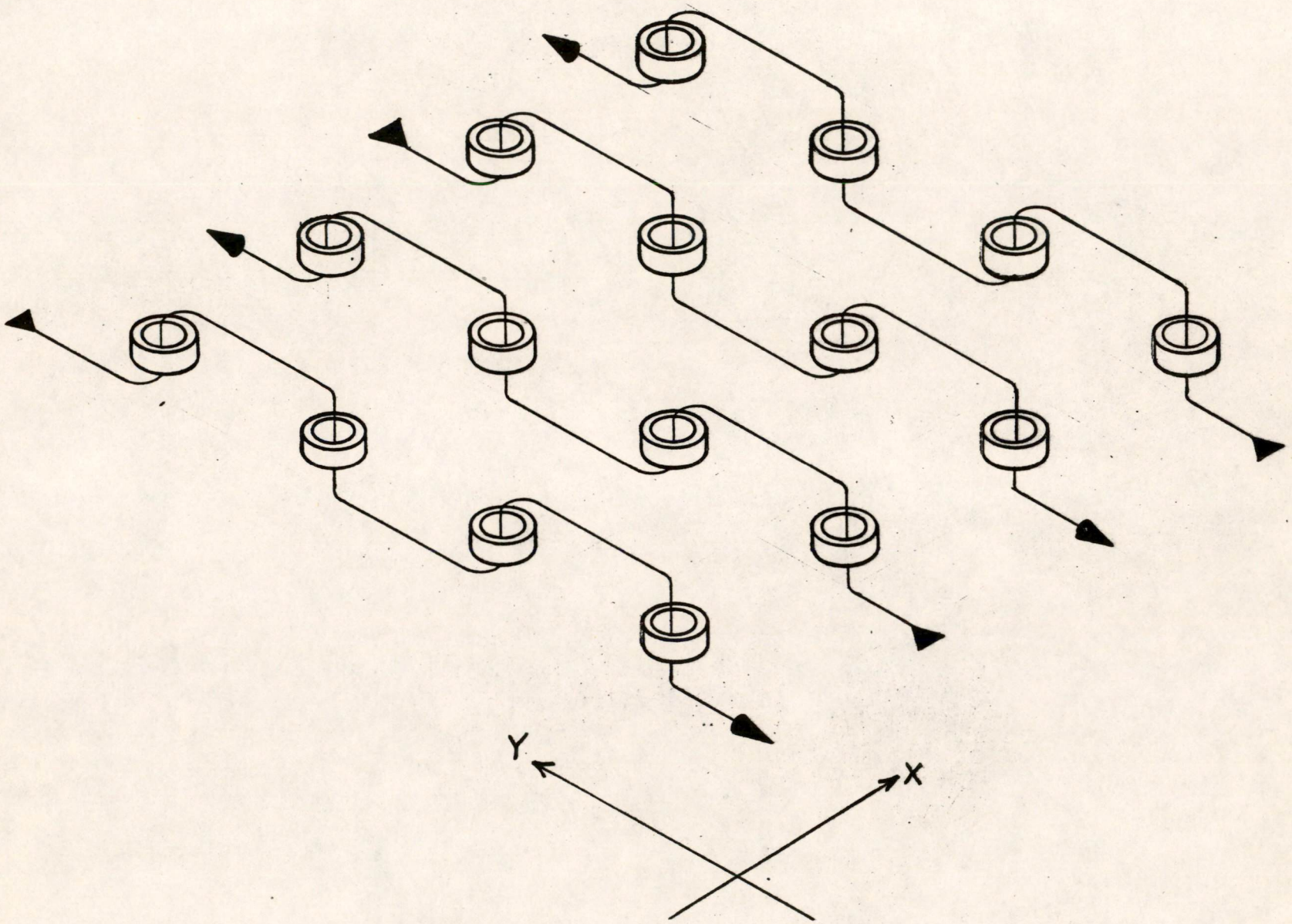
FIG. 4

PRINTED PLANE COMB CONNECTOR

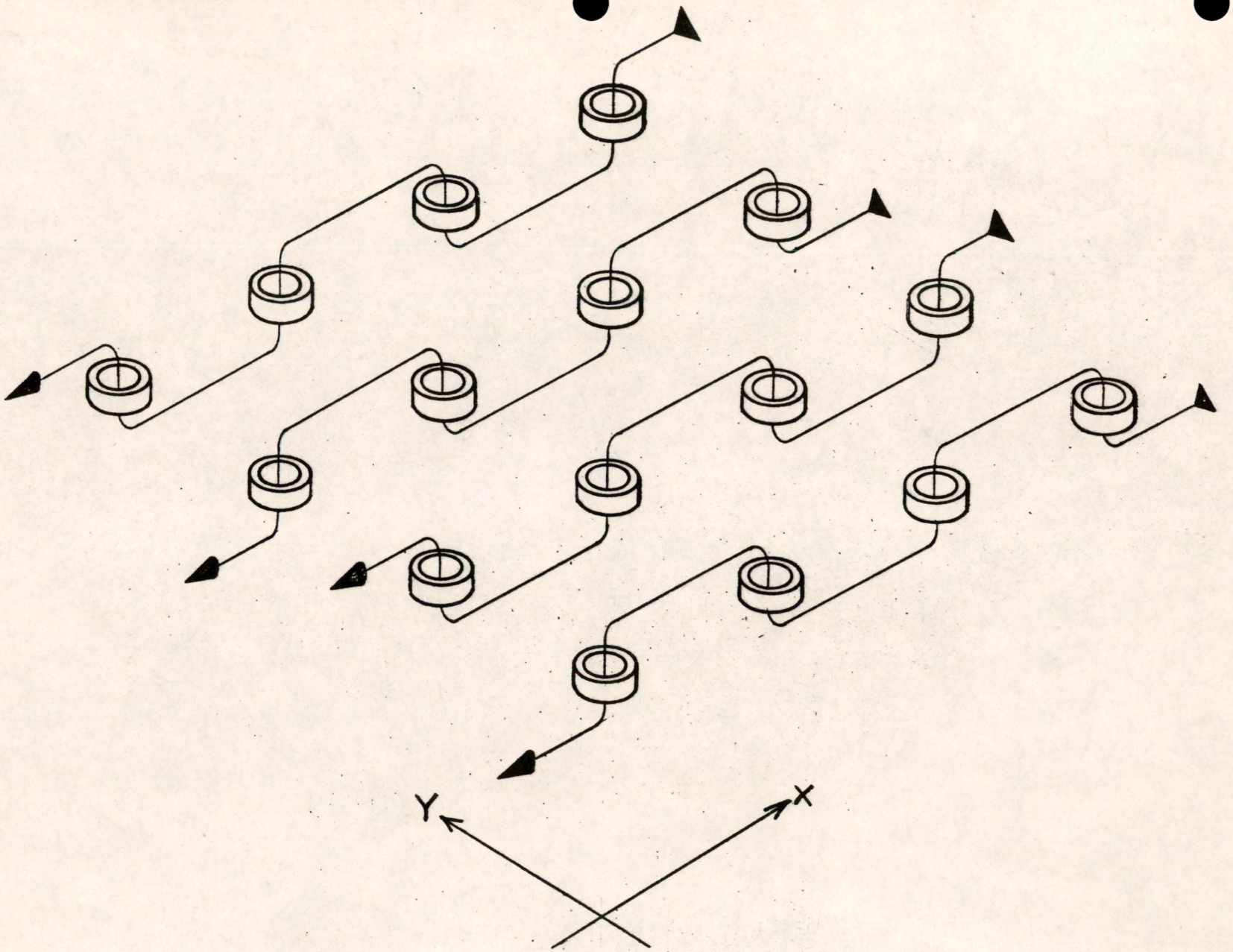
A-66029



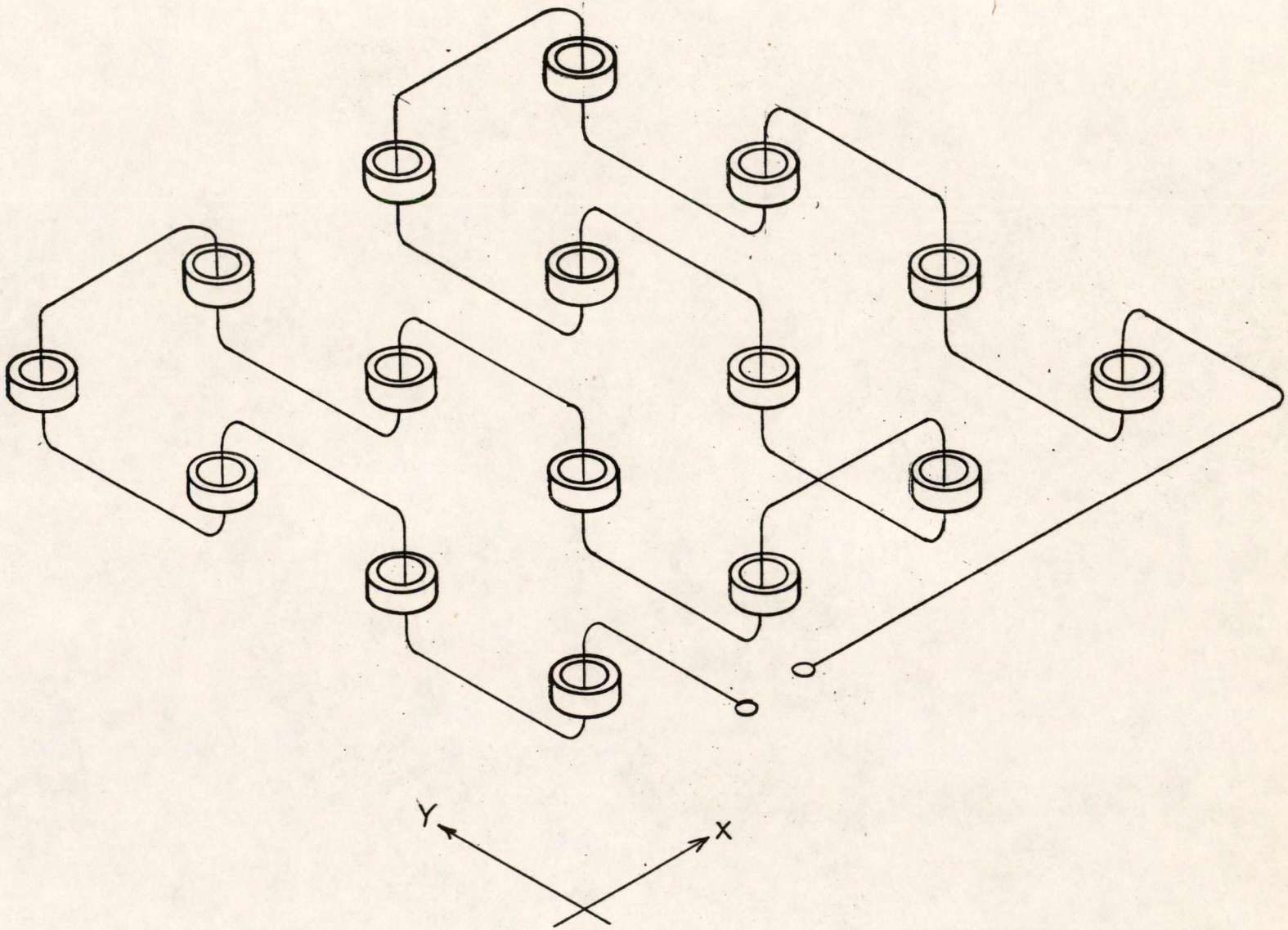
4 X 4 PRINTED MEMORY PLANE SHOWING SOLDER FILLETS



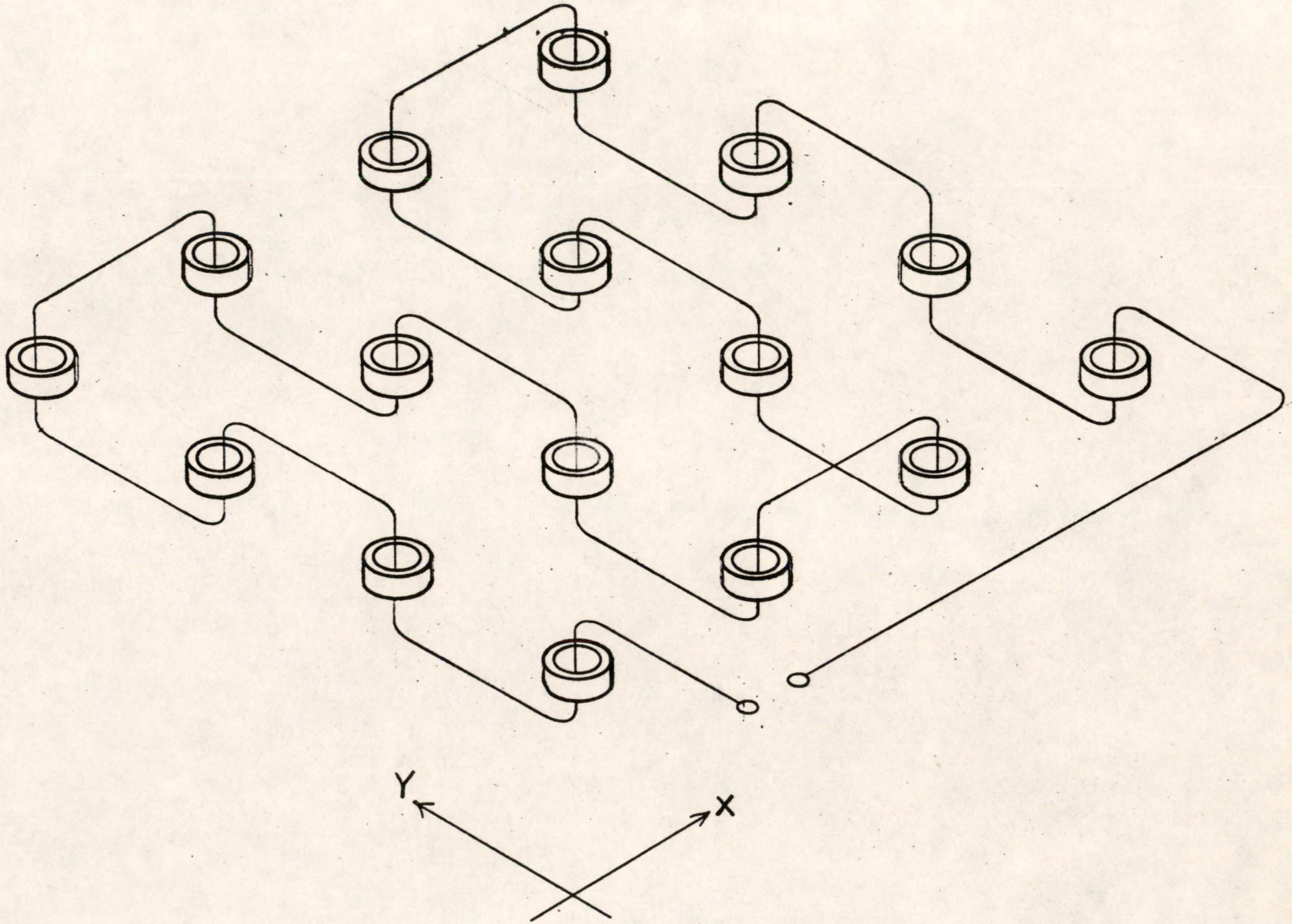
X COORDINATE DRIVING WIRES



Y COORDINATE DRIVING WIRES



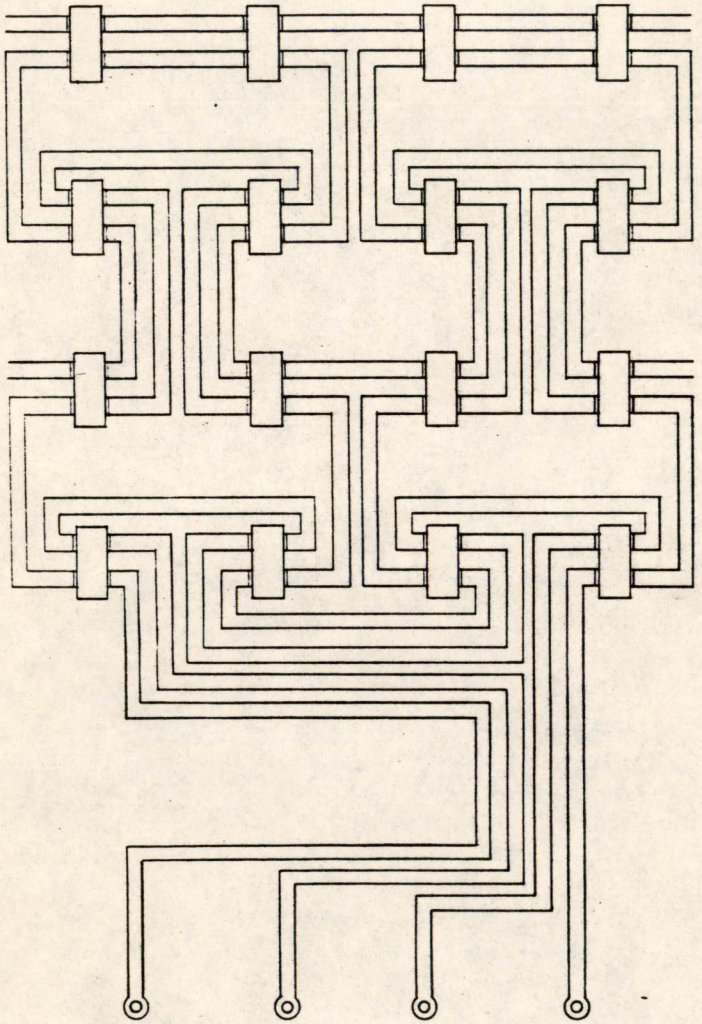
DIGIT PLANE WINDING



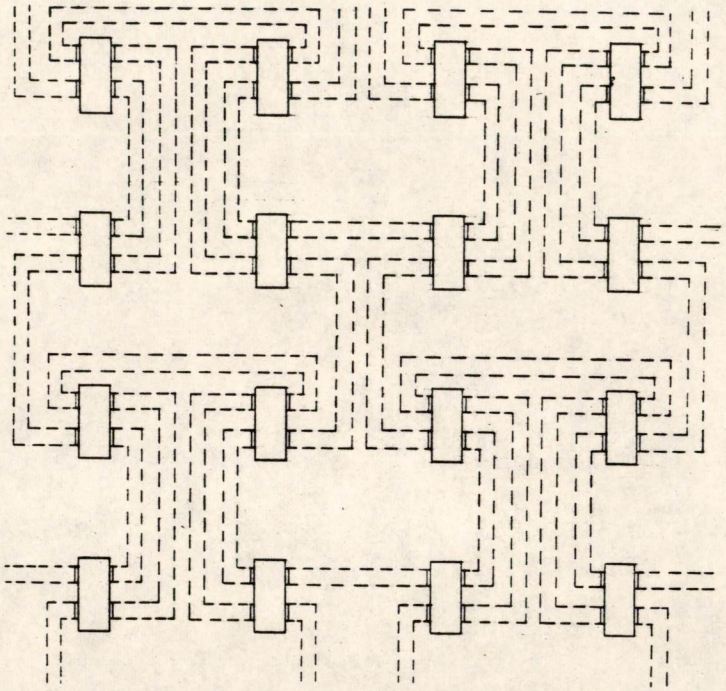
SENSE WINDING

C-60365

DECIMALS NOT OTHERWISE SPECIFIED
FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY



TOP CIRCUIT



BOTTOM CIRCUIT AS SEEN FROM TOP

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
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GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

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1	10/8	CNP	

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO.

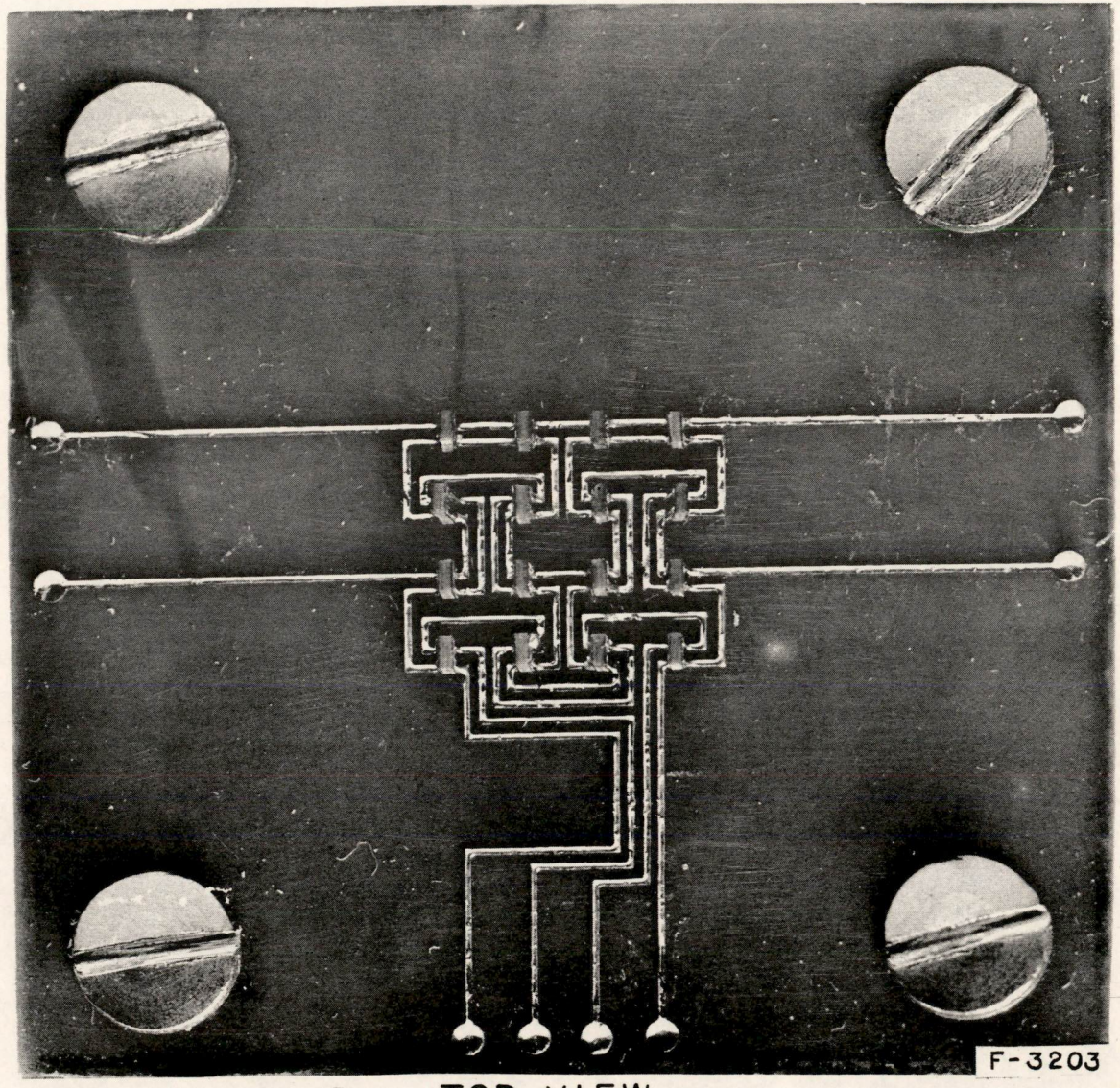
PRINTED CIRCUIT PATHS RECTANGULAR PEGS

SCALE: 20:1 DR. B. Ewalt 9-30-54 SC-60365

ENG. C.G. Guild CK. APPD.

ALBANENE 1955

A-67077

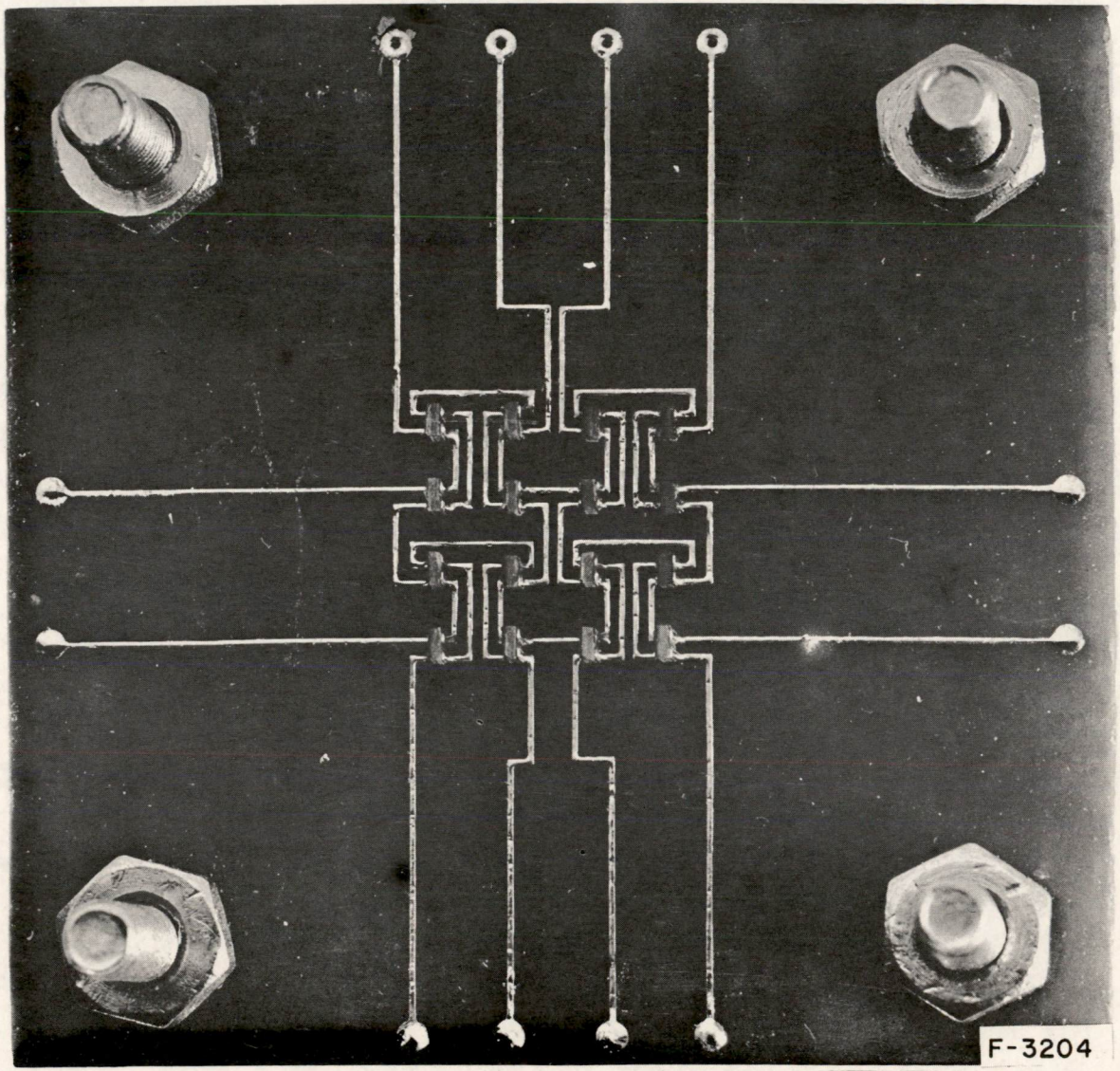


TOP VIEW,

4 X 4 PEG-TYPE PRINTED MEMORY PLANE

(FIRST WORKING MODEL)

A-67157



BOTTOM VIEW,
4 X 4 PEG-TYPE PRINTED MEMORY PLANE
(FIRST WORKING MODEL)

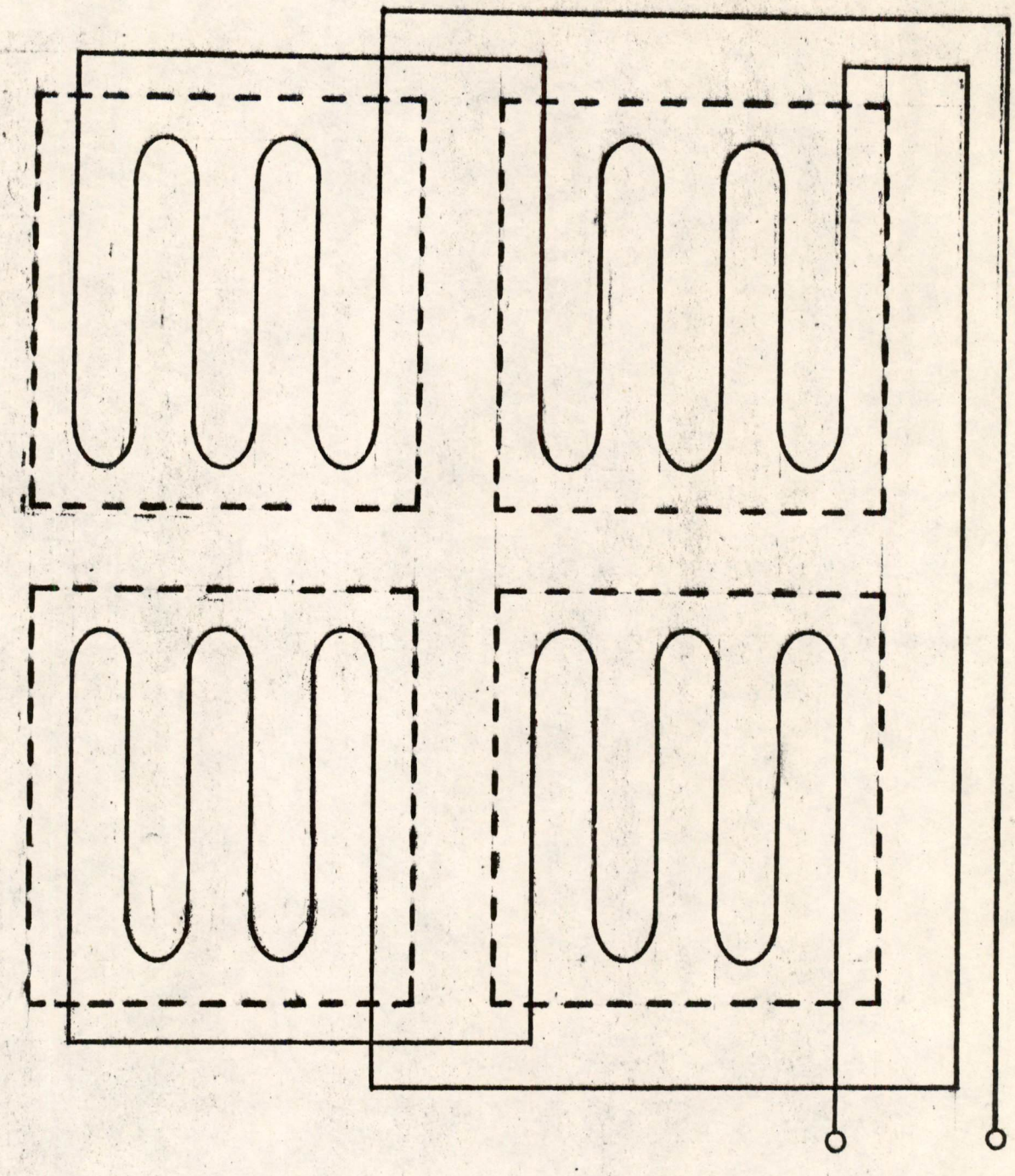


FIG. 5

QUADRANT SENSE WINDING
FOR PRINTED MEMORY PLANE

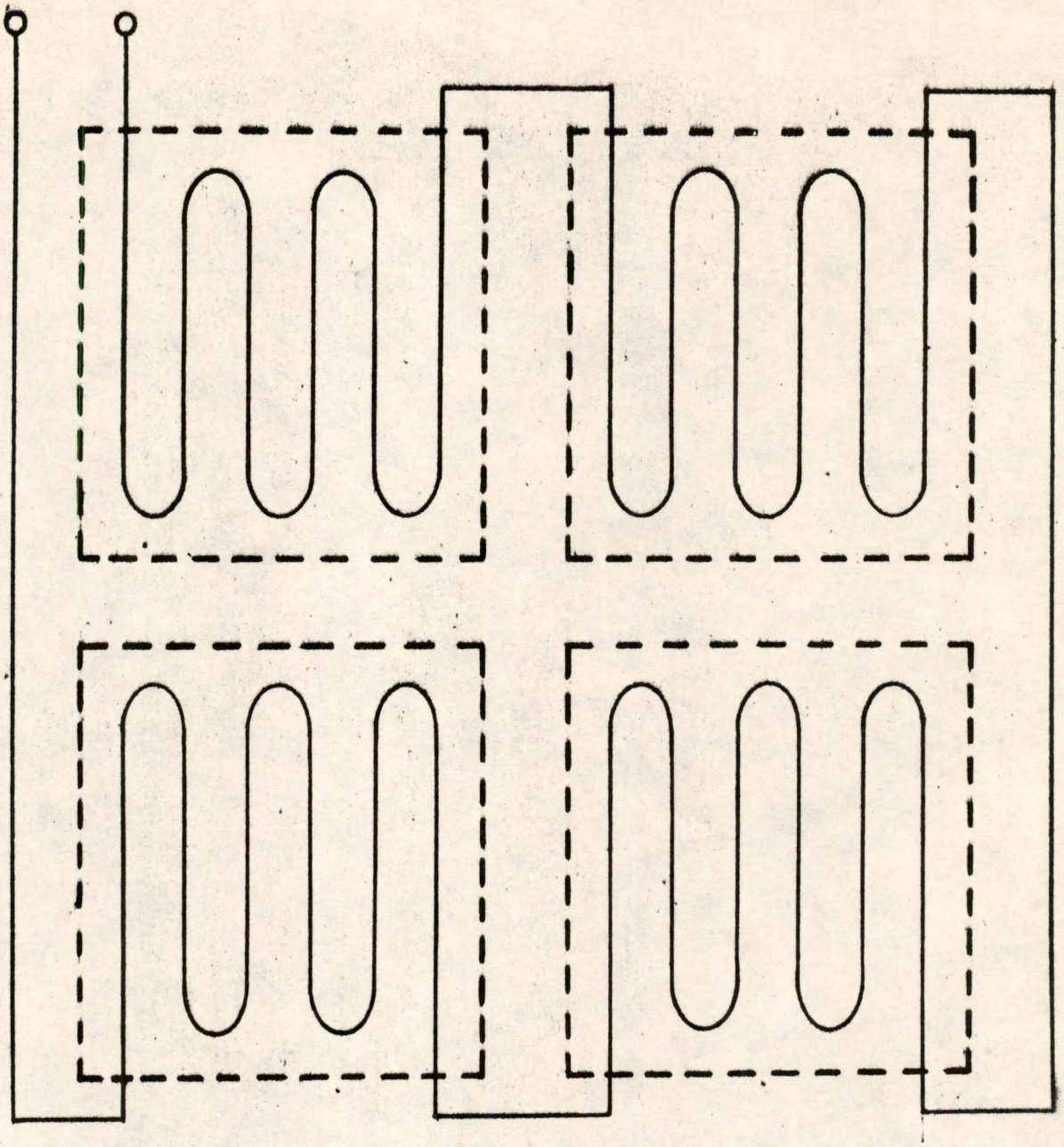


FIG. 6

QUADRANT DIGIT WINDING
FOR PRINTED MEMORY PLANE

R. Best Grp 63

B063

Memorandum 6M-4581-S-1

Sheet 1 of 13 Sheets

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: SOME NOTES ON THE THEORY AND DESIGN OF ALLOY JUNCTION TRANSISTORS FOR SWITCHING PURPOSES - PART III†

To: Donald J. Eckl

From: Charles T. Kirk, Jr. Charles T. Kirk Jr.

Date: August 21, 1957

Approved: D.J.E.

Abstract: In Parts I and II of this paper, some equations relating to the design of switching transistors were obtained, based on Ebers' and Moll's approximate analysis of the transient behavior of a junction transistor, for the assumption that the effective minority carrier lifetime in the base region is independent of the mode of operation. In Part III, experimental evidence to the contrary is discussed and a more detailed analysis of the Ebers and Moll switching theory is made showing that indeed the effective base lifetime is a function of the mode of operation of the transistor. As a result of this, corrections are made in the set of transform equations originally obtained in Part I as equation set (29). The effects of these corrections on the design equations are discussed in Part IV of this paper.

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† Parts I and II of this paper have been published as Division 6 Lincoln Laboratory Memorandum 6M-4581.

2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

PART III

A REVIEW OF FIRST-ORDER SWITCHING THEORY FOR P-N JUNCTION TRANSISTORS

Introduction

In Part II of this paper, we found that the principal switching parameters of a transistor, β_n, β_i, ω_n, ω_i, and τ_s, could be related by an equation of the form

$$(\beta_n + 1) = \omega_n \tau_s \tag{50}$$

$$(\beta_i + 1) = \omega_i \tau_s \tag{51}$$

Konkle[1] has shown that (51) agrees quite well with experimental data obtained from a group of L-5122 surface-barrier transistors with the exception that values of τ_s calculated from (51) were 10 to 20 percent higher than the measured value. No such agreement, however, could be found for (50).

Now (50) and (51) are derived from the valid relationships

$$(\beta_{n,i} + 1) = \omega_{n,i} \tau_{n,i} \tag{52}$$

and

$$\tau_s \approx \tau_b \text{ (to a first-order approximation)} \tag{53}$$

where τ_n, τ_i, and τ_b are various effective minority carrier lifetimes in the base region, such that, by identifying τ_n, τ_i with τ_b, we arrive at (50) and (51) and the resultant dilemma between theory and experiment.

In assuming that τ_n and τ_i are identical to τ_b, we have neglected to consider that these lifetimes are each defined under different transistor operating conditions. Consider the lifetimes τ_n and τ_i. τ_n is the effective base lifetime defined for the normal mode of active region operation of the transistor. Under this operating condition, the minority carrier density in the base varies from a maximum at the emitter junction boundary to zero at the collector junction boundary. Similarly, τ_i is the effective base lifetime defined for the inverted mode of active region transistor operation in which case the minority carrier density varies

---

1. K. Konkle, "Hole Storage in a Saturated Grounded-Emitter Transistor Circuit", M.I.T., Department of Electrical Engineering, Master's Thesis, Submitted in January, 1957.

from zero at the emitter junction boundary to a maximum at the collector junction boundary. τ_b, on the other hand is the effective base lifetime defined for the saturation condition of the transistor in which the minority carrier density is more or less distributed uniformly through the base region.

In Part I of this paper, the effective base lifetime, τ_b, was assumed to be approximately of the form

$$\frac{1}{\tau_b} = \frac{1}{\tau_p} + \frac{2s}{w} \tag{54}$$

where τ_p is the bulk lifetime
s is the surface recombination velocity
w is the width of the material.

This relation is derived for a uniform hole density distribution, and, consequently, neglects any effects on the effective base lifetime due to a non-uniform spacial distribution of the minority carrier density. Thus, the effective base lifetime as defined by this relation is seen to be symmetrical with respect to the mode of operation and independent of the region of operation. As a result of this interpretation of (54), we are led to assume that τ_n and τ_i must be identical with τ_b and hence with τ_s. If, however, a non-uniform spacial distribution of the minority carrier density does affect the value of the effective base lifetime (as is indeed indicated by the experimental evidence) then we must regard (54) as a zero-order approximation to the actual effective base lifetime for any given spacial distribution of the minority carriers. To a first-order approximation, therefore, we require that in general

$$\tau_n \neq \tau_i \neq \tau_b \approx \tau_s \tag{55}$$

In this part of the paper, we shall show that (55), which is required to hold in view of the experimental evidence, is consistent with the first order switching theory of Ebers and Moll.† As we shall show in Part IV of this paper, the distinction we have made among the various minority carrier lifetimes in the base region of a transistor leads to a

† Ebers, J.J. and Moll, J.L., Op. Cif.

set of design equations relating the electrical switching characteristics to the physical and geometrical design parameters of the transistor which are in agreement with the experimental evidence. In particular, we shall be able to show theoretically why (51) agrees so well with experimental data while (50) does not.

2.0 Some Remarks Concerning the Solution to the Transient Response of an Alloy Junction Transistor

In order to see more clearly the material presented in the remaining parts of the paper, it is worthwhile to consider in some detail the general approach to the analytical solution for the transient response of an alloy junction transistor. Given an alloy junction transistor of arbitrary geometry, a typical case of which is shown in Figure 7, we desire the analytical solution to the transient response of the output current, usually the collector current, i_c, for a specified input driving current, which can either be the emitter current i_e or the base current i_b, depending on the configuration in which the transistor is operated.

The direct approach to this problem is to solve the time-dependent diffusion equation of the form

$$D_p \nabla^2 p - \frac{p}{\tau_p} = \frac{\partial p}{\partial t} \tag{56}$$

where $p = p(x,y,z,t)$, is the excess minority carrier density distribution in the base region

τ_p is the bulk lifetime of the minority carriers in the base region

D_p is the diffusion constant for the minority carriers,

for p as a function of position in the base region and time subject to the boundary conditions:

$$-D_p \vec{\nabla p} \cdot d\vec{S} = s\, p\, ds \text{ (at the free base surfaces)} \tag{57}$$

$$i_p = -q \int_S D_p \vec{\nabla p} \cdot d\vec{S} \text{ at the junction boundaries of the base region} \tag{58}$$

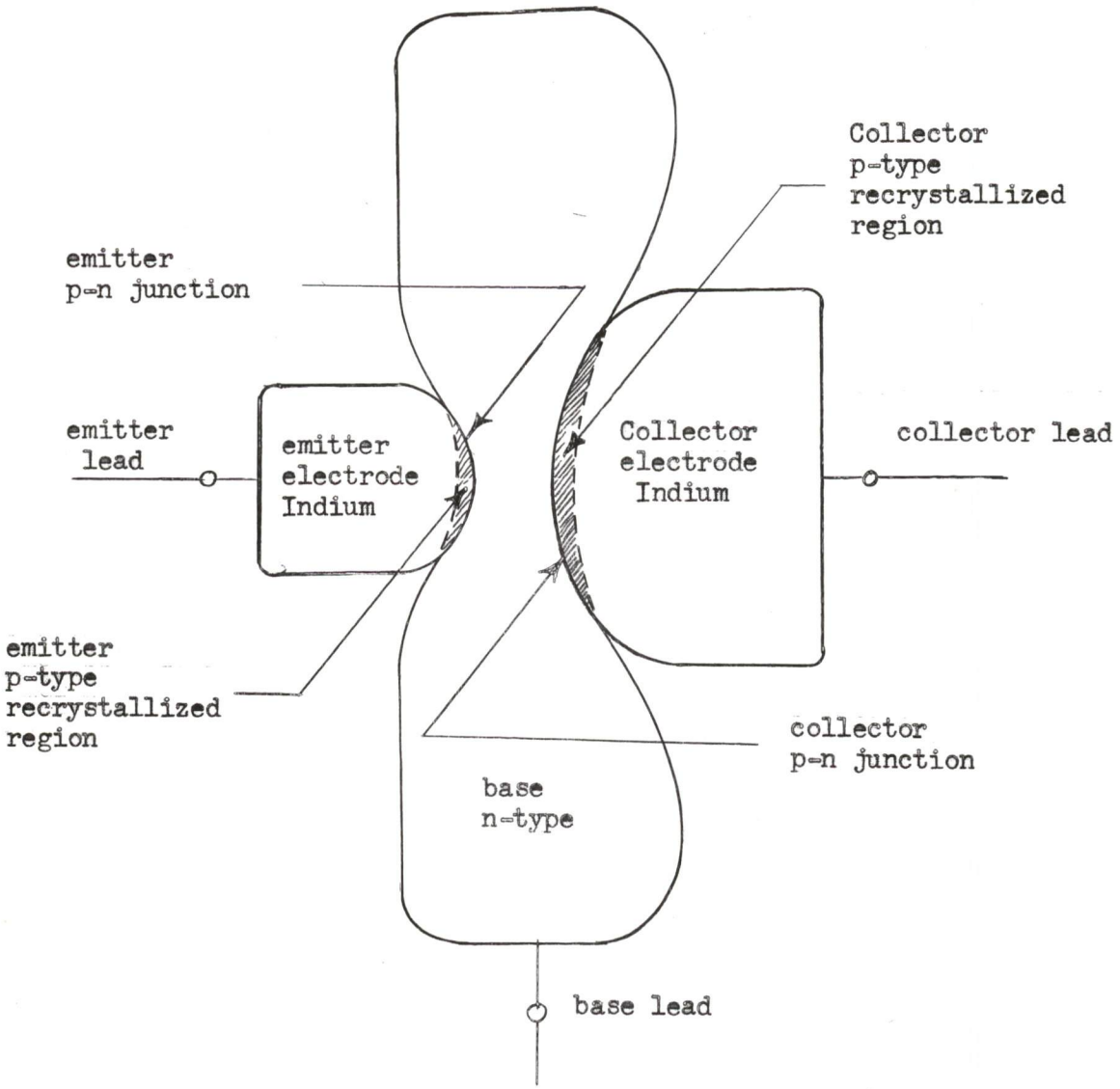

Collector
p-type
recrystallized
region
emitter
p-n junction
emitter
lead
emitter
electrode
Indium
Collector
electrode
Indium
collector lead
emitter
p-type
recrystallized
region
collector
p-n junction
base
n-type
base lead

Figure 7

$$p = p_{no}\left(e^{\frac{q}{kT}\phi} - 1\right) \quad \text{at the junction boundaries of the base region} \qquad (59)$$

where s — is the surface recombination velocity of the minority carriers at the free base surfaces

S — refers to the base surface

i_p — is the total minority carrier current at a junction boundary

q — is the electronic charge

p_{no} — is the equilibrium minority carrier density in the base region

d — is the voltage across a p-n junction and is positive if the drop occurs in going from the p-region to the n-region of the junction.

Once the solution for the excess minority carrier density in the base region is found, it is a simple matter to obtain the transient response of the collector current $i_c(t)$ from the relation

$$i_c(t) \approx i_p(t) = -qD_p \int_{S_c} \vec{\nabla} p \Big|_{\text{collector}} \cdot \vec{dS_c} \qquad (60)$$

where S_c is the surface of the base region at the collector junction boundary.

Except for special cases, however, involving simple geometric transistor structures, exact analytic solutions to the transient response of an alloy junction transistor are impossible or at least very difficult to obtain.

3.0 Ebers' and Moll's Approximate Solution for the Transient Response of an Alloy Junction Transistor

A good approximation to the solution for the transient response of an alloy junction transistor with an arbitrary geometry can be obtained by a method based on a linear separation of solutions developed by Ebers and Moll.

We notice that the diffusion equation (56) and the boundary conditions (57) and (58) are linear. Therefore, we can write the solution for $p = p(x,y,z,t)$ as the sum of two independent excess minority carrier distributions, $p_1 = p_1(x,y,z,t)$ and $p_2 = p_2(x,y,z,t)$ provided that a linear combination of these two independent solutions also satisfies the boundary condition given by (59). In general (59) is nonlinear and any linear combination of two arbitrary independent solutions will not satisfy this boundary condition. However, if we choose the solutions to be of the form

$$p_1 = p_{no}\left[e^{\frac{q}{kT}\phi_e(t)} - 1\right] f(x,y,z,t) \tag{61}$$

where $f(x,y,z,t) = \begin{cases} 1 & \text{at the emitter junction boundary} \\ 0 & \text{at the collector junction boundary} \end{cases}$

and $$p_2 = p_{no}\left[e^{\frac{q}{kT}\phi_c(t)} - 1\right] g(x,y,z,t) \tag{62}$$

where $g(x,y,z,t) = \begin{cases} 0 & \text{at the emitter junction boundary} \\ 1 & \text{at the collector junction boundary} \end{cases}$

and note that (59) is linear if and only if all the independent solutions except one are zero at a junction boundary, then the linear combination of p_1 and p_2 as given by (61) and (62), respectively, of the form

$$p = p_1 + p_2 \tag{63}$$

is also a solution.

If we now define, p, in (63) to be the complete solution for the excess minority carrier density distribution, then we can represent the separation of p into the two independent solutions, p_1 and p_2, as defined by (61), (62), and (63), schematically as shown in Figure 8. This schematic representation of an alloy junction transistor with an arbitrary geometry consists of two identical transistors of the same geometrical structure as the original transistor with their emitter, base, and collector leads each paired together to form single emitter, base,

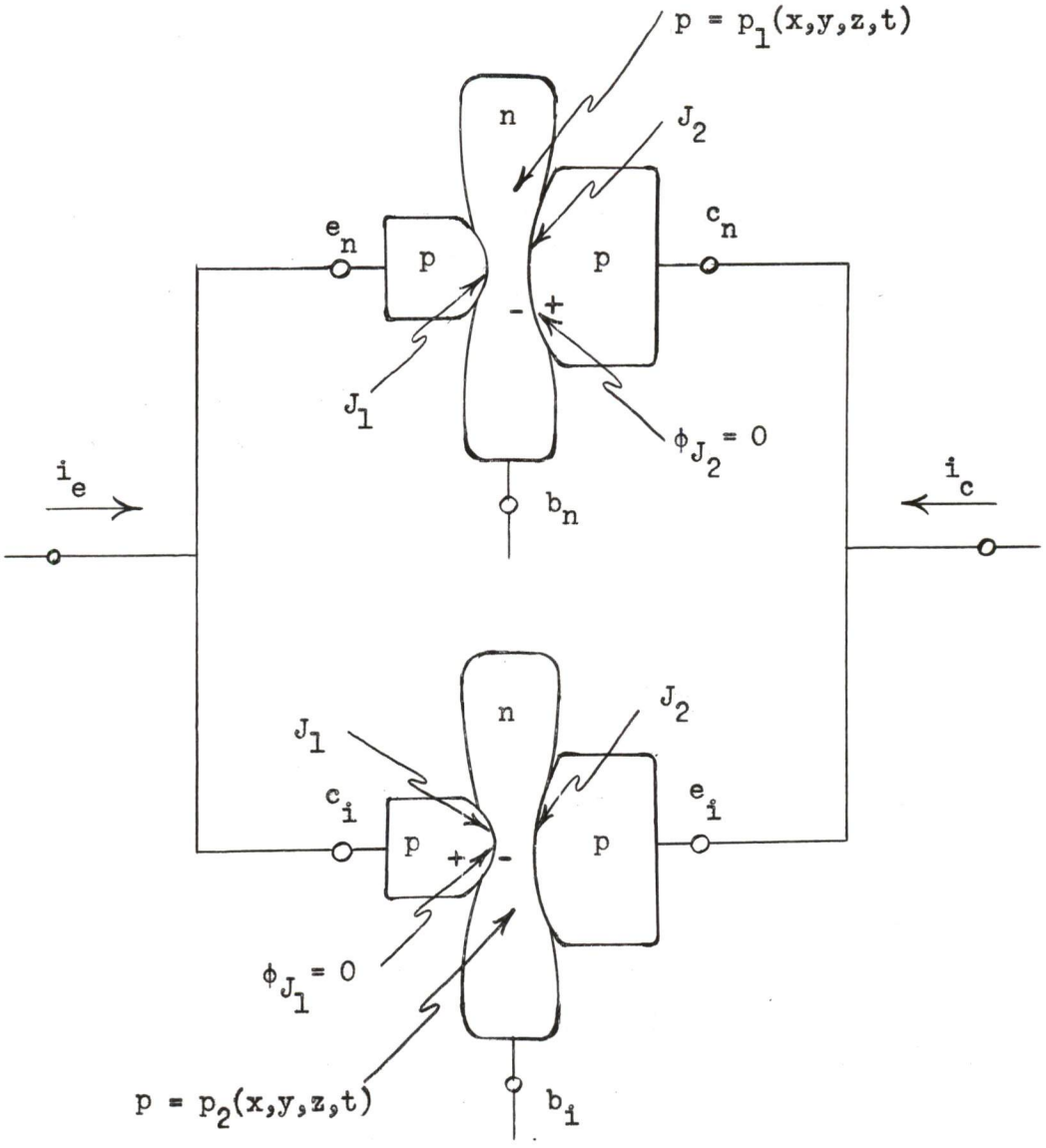

p = p1(x,y,z,t)
n
J2
en
p
p
cn
-
+
J1
φJ2 = 0
ie
ic
bn
J1
J2
n
ci
ei
p
+
-
p
φJ1 = 0
p = p2(x,y,z,t)
bi

Figure 8

and collector leads which are identical to the corresponding leads of the original transistor shown in Figure 7. Arbitrarily, the top transistor is designated to have an excess minority carrier distribution solution of the form, p_1, and the bottom transistor a solution of the form, p_2. Later on, we shall show that an alloy junction transistor having an excess minority carrier distribution of the form, p_1 or p_2, can be transformed into an ideal one-dimensional junction transistor structure for which the transient response is known in analytical form. First, however, we shall indicate how the schematic representation of the alloy junction is derived by considering the physical significance of breaking down the complete solution for the excess minority carrier density into two independent solutions in the manner described above by (61),(62) and (63).

The derivation of the schematic representation of an alloy junction transistor shown in Figure 8 is analogous to the derivation of a similar schematic representation for the one dimensional form of a p-n junction transistor. Therefore, for simplicity and convenience, we shall consider this derivation in terms of the one-dimensional case.

Figure 9(a) shows a one-dimensional step junction transistor in which $p = p(x,t)$. The excess minority carrier density distribution in the base region for some time, t, (solid line) is separated into two independent solutions, p_1 and p_2, (broken lines) as defined by (61) and (62). Now the gradient of p_1 is such that it represents a minority carrier diffusion current in the direction of the collector. Since p_1 is by definition zero at the collector junction boundary of the base region at all times, the gradient of p_1 at the collector junction boundary represents a minority carrier current, i_{cn}, into the collector that is independent of the collector voltage. In the collector region of the transistor this minority carrier current splits into two components. One component is the true collector current, i_c. The second component, i_{ei}, which is equal to the difference between i_{cn} and i_c is reinjected into the base region through the collector junction giving rise to the excess minority carrier density distribution, p_2. The gradient of p_2 shows that the reinjected current is a diffusion current in the direction of the emitter. The resultant gradient of p_2 at the emitter junction boundary of the base region represents a minority carrier current, i_{ci}, into

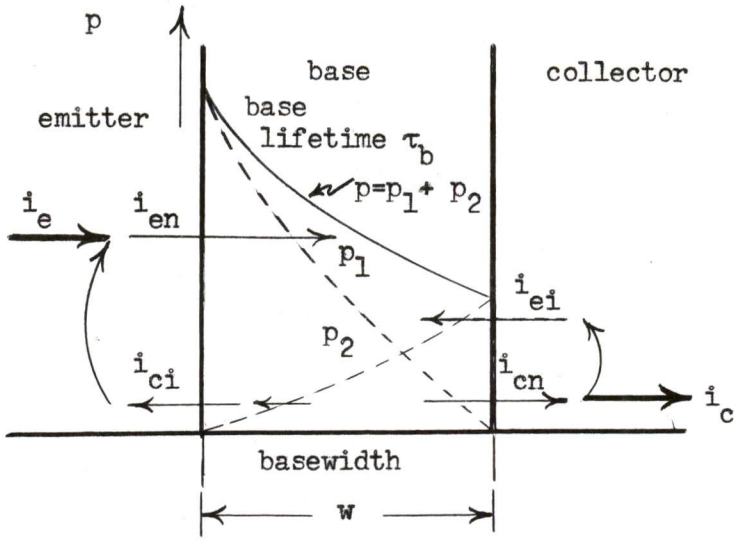


Fig. 9 (a)

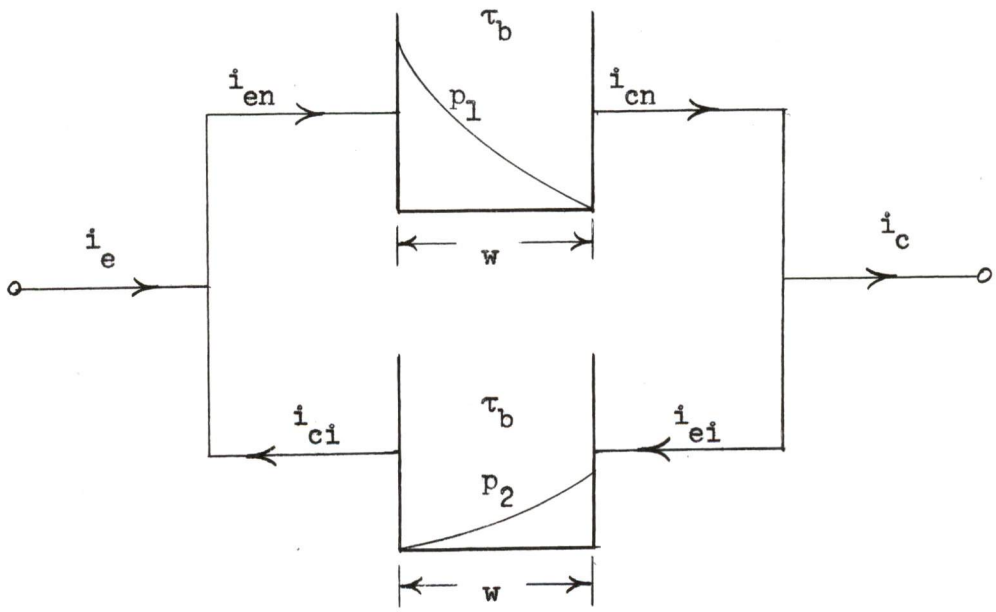


Figure 9(b)

the emitter. By definition, p_2 is zero at the emitter junction boundary and therefore i_{ci} is independent of the emitter voltage. In the emitter region i_{ci} combines with the true emitter current i_e to yield a current i_{en} which is injected into the base region through the emitter junction. The injection of i_{en} gives rise to the excess minority carrier distribution, p_1, which we assumed to exist at the beginning of this discussion.

Now, since the two excess minority carrier density distributions, p_1 and p_2, are independent of each other, the only interaction that occurs as a result of separating, p, the complete solution for the excess hole density distribution, into p_1 and p_2 is a Kirchoff's summation of the various currents in the emitter and collector regions. Thus the problem can be treated in the completely equivalent form shown in Figure 9(b). This equivalent form of the problem is obtained by replacing the one-dimensional transistor having an excess minority carrier density distribution of the form $p = p(x,t)$ in Figure 9(a) by two, one-dimensional transistors both of which are identical to the original one-dimensional transistor. The pairs of emitters, bases and collectors are each connected together as shown in Figure 9(b). The leads common to the emitters, bases and collectors of the two transistors correspond to the actual emitter base and collector electrodes of the original transistor shown in Figure 9(a). In a similar manner, the schematic representation of an alloy junction transistor by two transistors with the same geometry as the original and excess minority carrier distributions of the form of (61) and (62) can be obtained.

A transistor having a minority carrier distribution of the form of (61) or (62) in which $P_c = 0$ at all times in the case of (61) (or $P_e = 0$ at all times in the case of (62)) is by definition operating in its active region. In order to distinguish as to whether p_e (or p_c) is zero in a particular case, we have designated the case in which $P_c = 0$ as the "normal mode" of operation in the active region and the case in which $p_e = 0$ as the "inverted mode" of operation in the active region. Thus, we see that by making a linear separation of the excess minority carrier density distribution into distributions of the forms (61) and (62) we now need only to obtain the transient solution for the transistor operating in the active region in order to determine the transient behavior of the transistor

under any arbitrary operating conditions.

Having discussed the derivation and physical significance of the schematic representation of an alloy junction transistor shown in Figure 8, we shall next consider the problem of showing that an alloy junction transistor with an excess minority carrier density distribution of the form of (61) or (62), e.i., operating in the active region, can be transformed into an ideal, one-dimensional, junction transistor structure. Once this is done, we can transform the schematic representation of an alloy junction transistor into a one-dimensional form for which an analytical solution to the transient response can be obtained.

4.0 Small-Signal Response of an Idealized† One-Dimensional P-N Junction Transistor

In order to obtain the equations for transforming an alloy junction transistor into an electrically equivalent, one-dimensional transistor, it is necessary to consider certain aspects of the active small-signal behavior of an ideal one-dimensional transistor. The solution for the small-signal response of the one-dimensional idealized transistor was developed in Part I of this paper. In normalized form, we see from (12) (16) (18) and (19) that this response is given by the expression

$$\frac{i_c}{i_e} \triangleq \alpha(\omega) \approx \frac{\alpha_o}{1 + j\frac{\omega}{\omega_{c\alpha}}} \tag{64}$$

$$\text{where } \alpha_o = \frac{1}{1 + \frac{w^2}{2D_p}\frac{1}{\tau_p}} \tag{65}$$

$$\omega_{c\alpha} = \frac{2D_p}{w^2} + \frac{1}{\tau_p} \tag{66}$$

The parameters α_o and $\omega_{c\alpha}$ appearing in (64) are defined as the common base d-c current-gain and cutoff-frequency, respectively, and are related to the base width, w, and the base bulk-lifetime, τ_p, of the idealized one-dimensional transistor by (65) and (66).

† "Idealized" means here that the conductivity of the emitter and collector regions is extremely large compared to the base conductivity so that the emitter efficiency can be regarded as unity.

From linear circuit theory, we know that if the sinusoidal amplitude and phase characteristics of a device are known for all frequencies then the output response of the device can be determined for any arbitrary input function. This is the case for the idealized one-dimensional transistor, since from (64) we can write

$$|\alpha| = \left|\frac{i_c}{i_e}\right| = \frac{\alpha_o}{\left[1 + \left(\frac{\omega}{\omega_{c\alpha}}\right)^2\right]^{1/2}} \tag{67}$$

$$\angle i_c/i_e = \arctan\left(\frac{\omega}{\omega_{c\alpha}}\right) \tag{68}$$

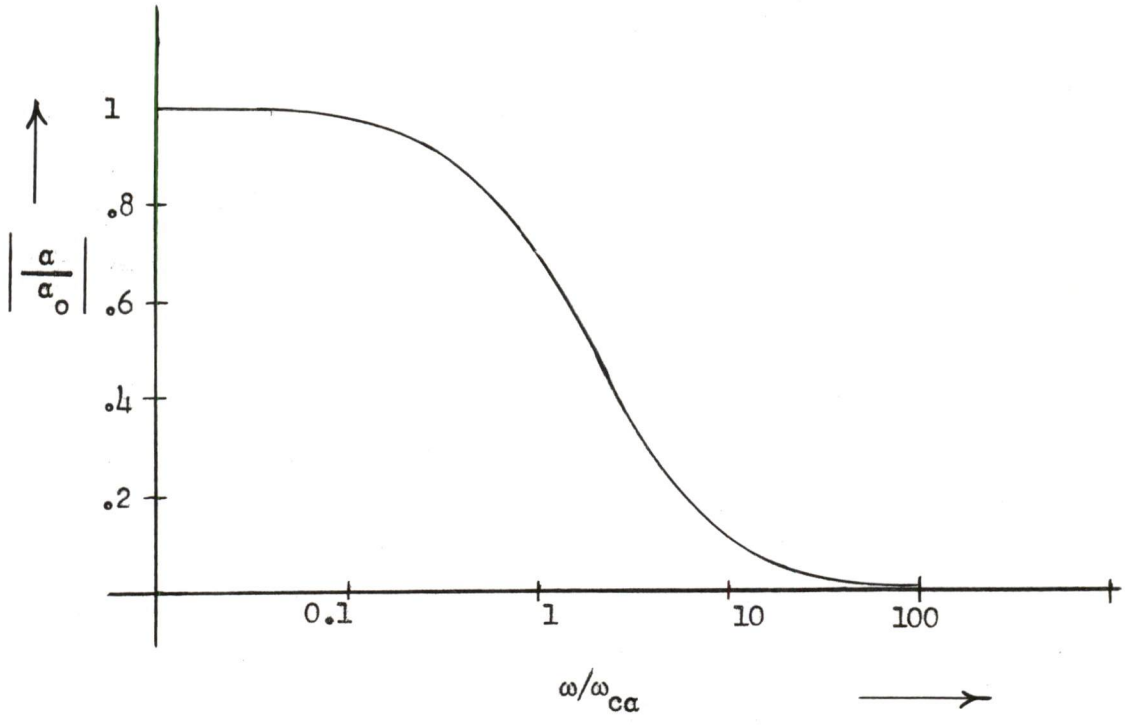
where (67) and (68) describe the amplitude response and phase characteristics, respectively of the idealized, one-dimensional transistor as a function of the drive frequency ω and the parameters α_o and $\omega_{c\alpha}$. Figure 10 shows a normalized plot of these amplitude and phase characteristics as a function of $\omega/\omega_{c\alpha}$.

From this brief discussion of the small-signal behavior of the idealized, one-dimensional transistor we see that when operating in the active region the output response of this device to any arbitrary input signal is completely characterized by the electrical parameters $\omega_{c\alpha}$ and α_o and, ultimately, through (65) and (66) by the base width w and the minority carrier lifetime, τ_p.

5.0 Small-Signal Behavior of Alloy Junction Transistors

Figure 11 shows a typical normalized plot of the sinusoidal amplitude and phase characteristics of an alloy junction transistor (solid lines) in comparison with the normalized characteristics of the idealized one-dimensional transistor (dotted lines). We see from this Figure that the small-signal frequency characteristics of amplitude and phase approximates quite closely those of the idealized one-dimensional transistor from d-c out to three to five times $\omega_{c\alpha}$. It can be shown from linear circuit theory that the transient behavior of an alloy junction transistor with such small-signal characteristics is almost identical to the transient behavior of the idealized transistor except during the time

$$0 < t < \frac{1}{3\omega_{c\alpha}}$$


1
.8
.6
.4
.2
$\left|\frac{\alpha}{\alpha_o}\right|$
0.1
1
10
100
$\omega/\omega_{c\alpha}$

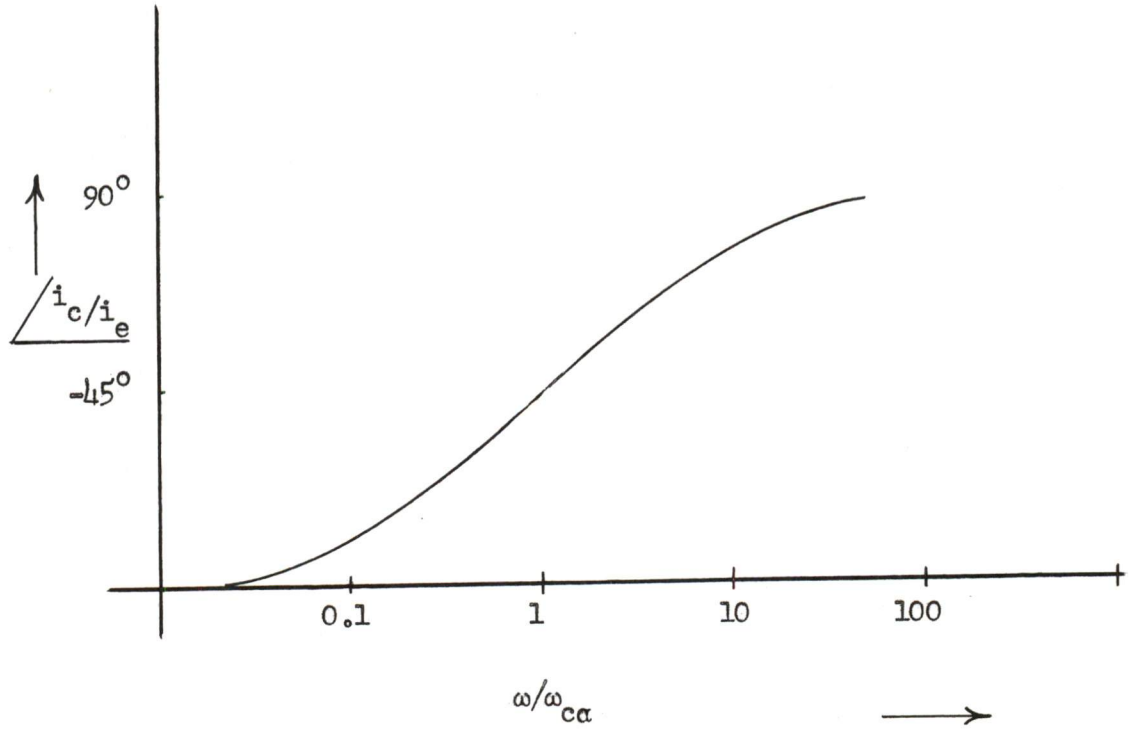

90°
i_c/i_e
-45°
0.1
1
10
100
$\omega/\omega_{c\alpha}$

Figure 10

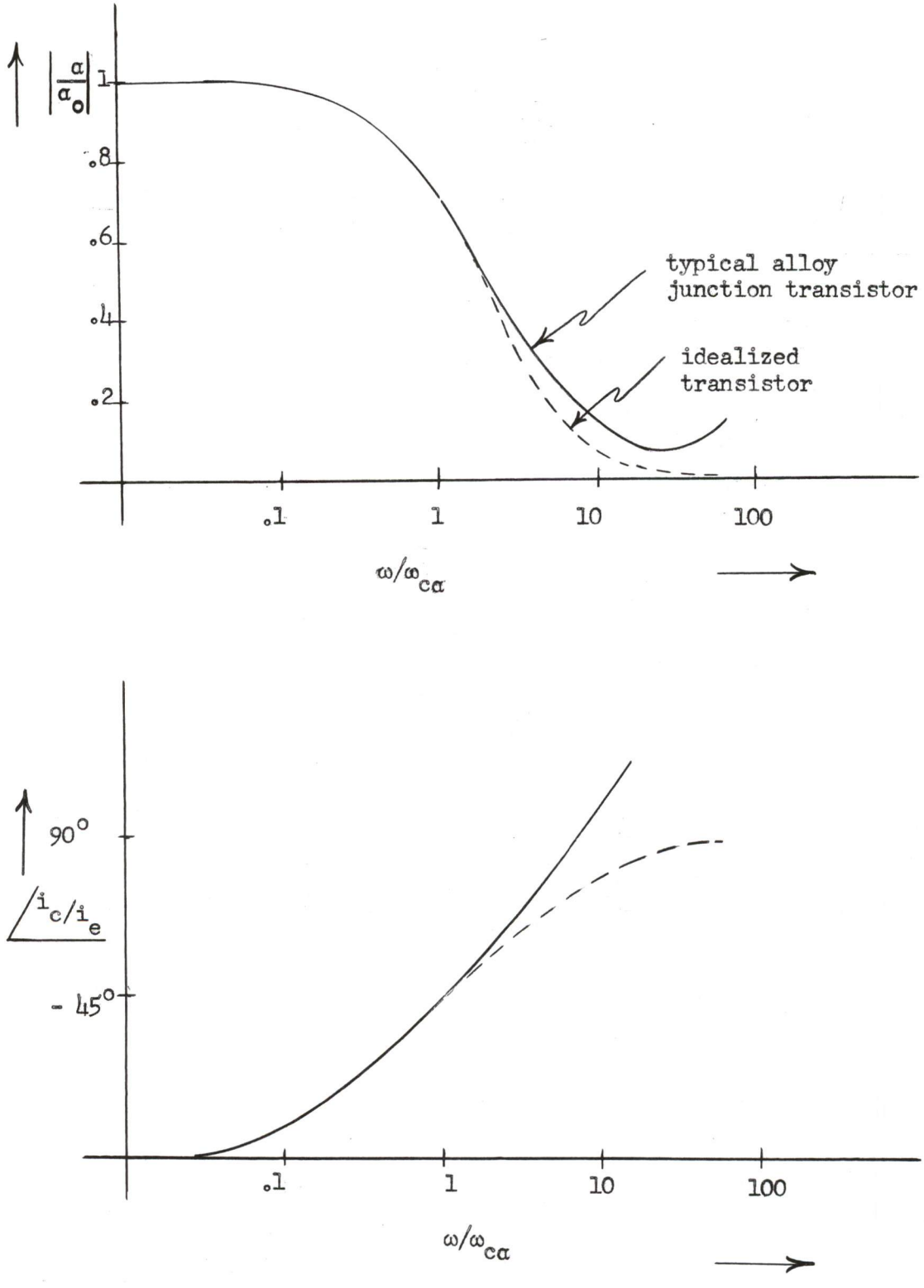

$\left|\frac{\alpha}{\alpha_o}\right|$
1
.8
.6
.4
.2
typical alloy
junction transistor
idealized
transistor
.1
1
10
100
$\omega/\omega_{c\alpha}$
90°
i_c/i_e
- 45°
.1
1
10
100
$\omega/\omega_{c\alpha}$

Figure 11

As an example of the veracity of this last statement we compare, in Figure 12, the collector current response of a typical, alloy junction transistor, and an equivalent†, idealized, one-dimensional transistor for a step input of emitter current. We see from this Figure that for time $t > 1/3\omega_{c\alpha}$ the transient response for the alloy transistor is fairly well approximated by the response of the idealized transistor. While for $t < 1/3\omega_{c\alpha}$, the transient response of the two devices differ considerably from one another owing to the differences in their high frequency ($> 3\text{-}5\ \omega_{c\alpha}$) amplitude and phase characteristics.

Fortunately, in switching circuit applications, we are seldom if ever concerned with times much less than $1/3\omega_{c\alpha}$. Consequently, it is possible, in the analysis of transistor switching circuits, to replace the alloy junction by an equivalent, idealized, one-dimensional transistor. The results obtained by this approximation are accurate to within $1/3\omega_{c\alpha}$ which turns out to be quite satisfactory in the analysis of a transistor's switching characteristic.

6.0 Continuation of Ebers' and Moll's Approximate Solution for the Transient Response of an Alloy Junction Transistor

Having shown that, to a good approximation, equivalence exists between the active region transient behavior of the alloy junction transistor and that of the idealized, one-dimensional transistor, we can now go on and complete our discussion of Ebers' and Moll's solution for the transient response of an alloy junction transistor.

Previously, we had found that the alloy junction transistor shown in Figure 7 could be replaced by the equivalent circuit shown in Figure 8 in which the alloy junction unit is replaced by two alloy junction transistors both identical to the original transistor but with each restricted to operating in the active-off regions only and interconnected as shown in Figure 8. As before, we shall arbitrarily consider the top transistor in this Figure to be operating in the normal-mode and the bottom transistor to be operating in the inverted-mode.

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† By "equivalent", we mean that the dc current gain, α_o, and the cutoff frequency $\omega_{c\alpha}$ of the two devices are identical.

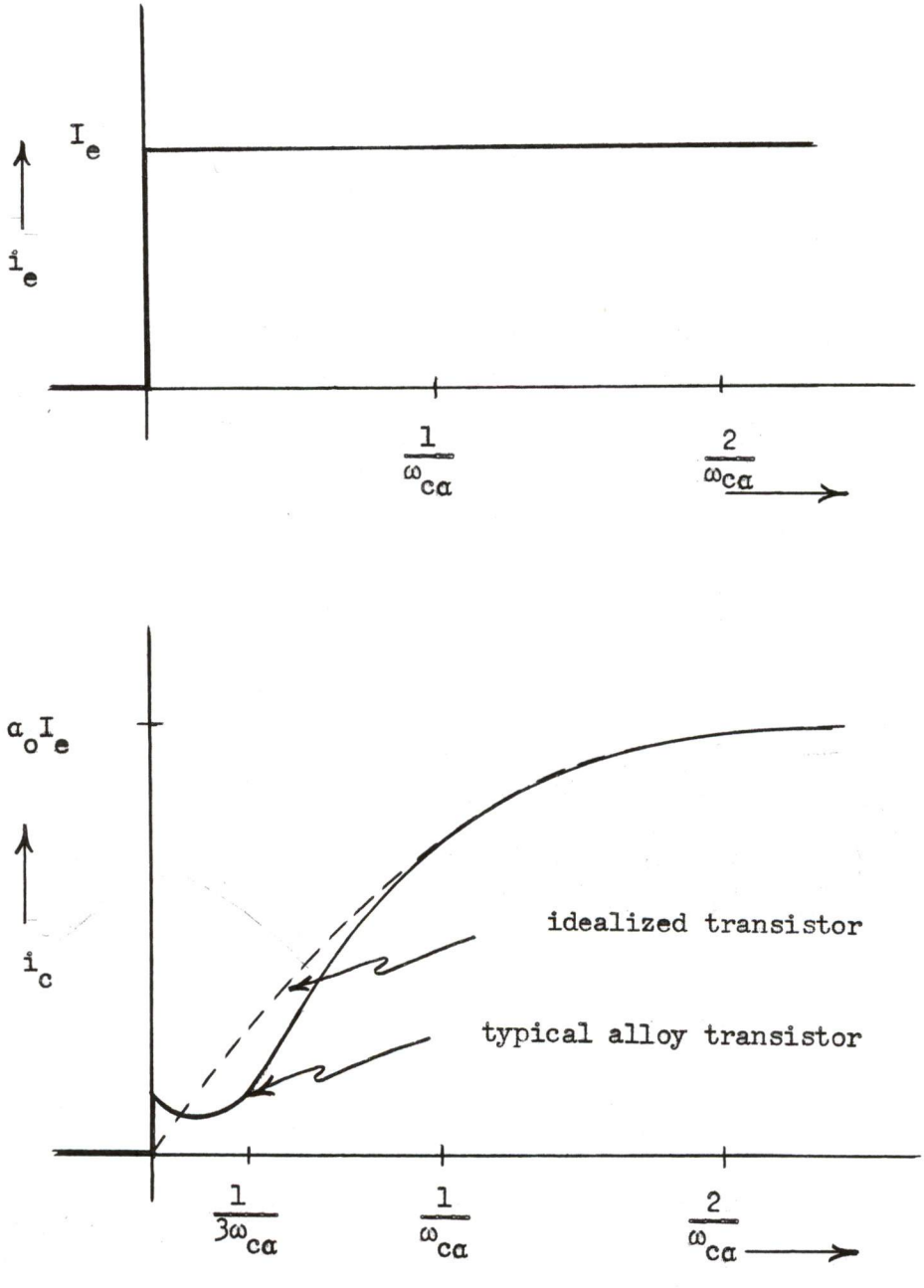
I_e
i_e
$\frac{1}{\omega_{c\alpha}}$
$\frac{2}{\omega_{c\alpha}}$
$\alpha_o I_e$
i_c
idealized transistor
typical alloy transistor
$\frac{1}{3\omega_{c\alpha}}$
$\frac{1}{\omega_{c\alpha}}$
$\frac{2}{\omega_{c\alpha}}$

Figure 12

Now as we have just seen the transient behavior of each of these two transistors can be completely characterized by their dc current-gains and cutoff frequencies. These parameters can be obtained by direct measurement on the actual alloy junction transistor under consideration. The normal, common-base, dc, current-gain, α_n, and cutoff frequency, ω_n, are obtained by making the appropriate measurements on the transistor while operating it in the active region under normal-mode conditions. The inverted, common-base, dc, current-gain, α_i, and cutoff frequency, ω_i, are also obtained in a similar manner while operating the transistor in the active region under inverted-mode conditions. In general,

$$\alpha_n \neq \alpha_i$$

and $$\omega_n \neq \omega_i$$

principly because of the differences in geometry and electrical characteristics of the two p-n junctions.

Having characterized the top transistor in Figure 8 by α_n and ω_n, and the bottom transistor by α_i and ω_i, we can replace each of these transistors by equivalent, idealized one-dimensional transistors, respectively. Thus, the equivalent circuit for an alloy junction transistor is now as shown in Figure 13. It is to be noted that the equivalent circuit of Figure 13 is only approximate and that the switching times to be derived from it shortly are accurate only to within $1/3\omega_{c\alpha}$ seconds.

A detailed analysis of the small-signal characteristics of the idealized one-dimensional transistor would show that the frequency response characteristics as given by (64) represent only a first order approximation to the actual expression[†]. Consequently, in order to obtain consistent results, the behavior of the minority carrier density distribution in the base region must be considered only to a first order approximation, e.i., the minority carrier density distribution is at all times a linear function of distance through the base region as shown in Figure 13 for times t and $t + \Delta t$.

Under these conditions, then, the current at the collector, i_c, and anywhere in the base region, $i(x)$, of an idealized transistor is from (6) of the form

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[†] This is the principal reason why the transient response of an equivalent, idealized, one-dimensional transistor differs from the true response of an alloy junction transistor for $t < 1/3\omega_{c\alpha}$.

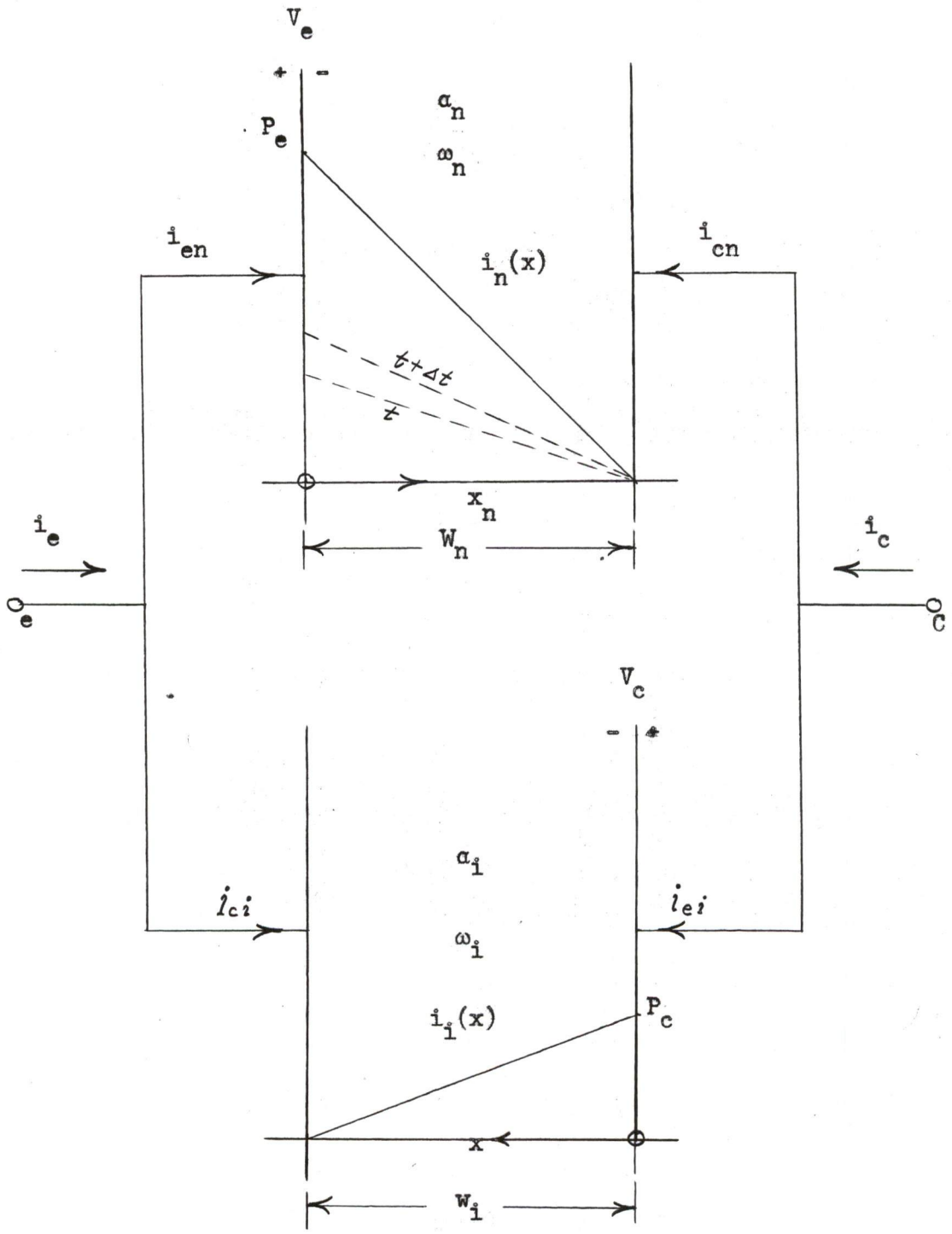
V_e
+ -
α_n
P_e
ω_n
i_{en}
$i_n(x)$
i_{cn}
$t+\Delta t$
t
x_n
i_e
W_n
i_c
e
c
V_c
- +
α_i
i_{ci}
i_{ei}
ω_i
$i_i(x)$
P_c
x
W_i

Fig. 13

$$i(x) = - i_c = - qD_p \frac{p}{w} \tag{69}$$

such that for the normal-mode case this equation becomes

$$i_n(x) = - i_{c_n} = - qD_p \frac{p_e}{w_n} \tag{70}$$

and for the inverted-mode case

$$i_i(x) = - i_{c_i} = - qD_p \frac{p_c}{w_i} \tag{71}$$

where the currents, minority carrier densities, and base widths are defined in Figure 13. Since, $i_{(x)} = - i_c$ everywhere in the base region, we can write that

$$\alpha_n \triangleq \frac{-i_{cn}}{i_{en}} = \frac{i_{n(x)}}{i_{en}} = \frac{i_n(w_n)}{i_{en}} \tag{72}$$

and

$$\alpha_i \triangleq \frac{-i_{ci}}{i_{ei}} = \frac{i_i(x)}{i_{ei}} = \frac{i_i(w_i)}{i_{ei}} \tag{73}$$

and, thus, α_n and α_i are seen to behave as injection efficiencies in this analysis. Consequently, we can set the transport factor equal to unity and let

$$\tau_p \longrightarrow \infty \tag{74}$$

In the time domain, the behavior of the equivalent, idealized, one-dimensional transistors in Figure 13 is governed by the differential equations

$$qw_n \frac{dp_e}{dt} = \alpha_n i_{en} + i_{cn} \tag{75}$$

$$q w_i \frac{dp_c}{dt} = \alpha_i i_{ei} + i_{ci} \tag{76}$$

where (75) refers to the one-dimensional equivalent of the alloy junction transistor operating in the normal mode and (76) refers to the one-dimensional equivalent of the alloy junction transistor operating in the inverted mode. Eliminating p_e from (70) and (75) and p_c from (71) and

(76) and noting that (66) and (74) allow us to write the cutoff frequencies ω_n and ω_i in the form

$$\omega_n = \frac{2D_p}{w_n^2} \tag{77}$$

and

$$\omega_i = \frac{2D_p}{w_i^2} \tag{78}$$

we can rewrite (75) and (76), the differential equations governing the behavior of the one-dimensional equivalent transistors, in the respective forms

$$-\frac{1}{\omega_n}\frac{di_{cn}}{dt} = \alpha_n i_{en} + i_{cn} \tag{79}$$

$$-\frac{1}{\omega_i}\frac{di_{ei}}{dt} = \alpha_i i_{ei} + i_{ci} \tag{80}$$

These two equations together with the node equations

$$i_{en} + i_{ci} = i_e \tag{81}$$

$$i_{ei} + i_{en} = i_c \tag{82}$$

and the appropriate boundary and initial conditions on i_e and i_c lead to the approximate expressions originally obtained by Ebers and Moll† for the switching times characterizing the transient response of a p-n junction transistor.

The most common and most useful configuration in which a transistor is utilized in a switching circuit is the common emitter configuration. In this case, the switching time expressions obtained in the manner just described are of the form

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† Ebers, J.J., and Moll, J.L., Op Cit.

$$t_r = \frac{1}{(1-\alpha_n)\,\omega_n} \ln \left[\frac{I_{b_1}}{I_{b_1} - 0.9\,\frac{(1-\alpha_n)}{\alpha_n} I_{c1}} \right] \tag{83}$$

$$t_s = \frac{\omega_n + \omega_i}{\omega_n \omega_i (1-\alpha_n \alpha_i)} \ln \left[\frac{I_{b_2} - I_{b_1}}{I_{b_2} - \frac{1-\alpha_n}{\alpha_n} I_{c1}} \right] \tag{84}$$

$$t_{t_f} = \frac{1}{(1-\alpha_n)\,\omega_n} \ln \left[\frac{I_{c1} - \left(\frac{\alpha_n}{1-\alpha_n}\right) I_{b_2}}{\frac{1}{10} I_{c_1} - \left(\frac{\alpha_n}{1-\alpha_n}\right) I_{b_2}} \right] \tag{85}$$

where the currents and switching times are as defined in Figure 14. In addition to the switching times, two steady-state parameters are of considerable interest in the design of a switching transistor namely: -- the normal mode common-emitter current gain, β_n, the saturation region collector to emitter voltage, $V_{ce\ sat}$. The first of these parameters is related to α_n by an equation of the form

$$\beta_n = \frac{\alpha_n}{1-\alpha_n} \tag{86}$$

The second parameter is obtained by solving the equivalent circuit of Figure 13 subject to the boundary condition

$$p_e = p_{no} \left(e^{\frac{q}{kt} V_e} - 1\right) \tag{87}$$

$$p_c = p_{no} \left(e^{\frac{q}{kt} V_c} - 1\right) \tag{88}$$

for

$$V_{ce} \triangleq V_c - V_e \tag{89}$$

In the saturation region, this solution, originally obtained by Ebers and Moll† has the form

† Ebers, J.J., and Moll, J.L., Op. Cit.

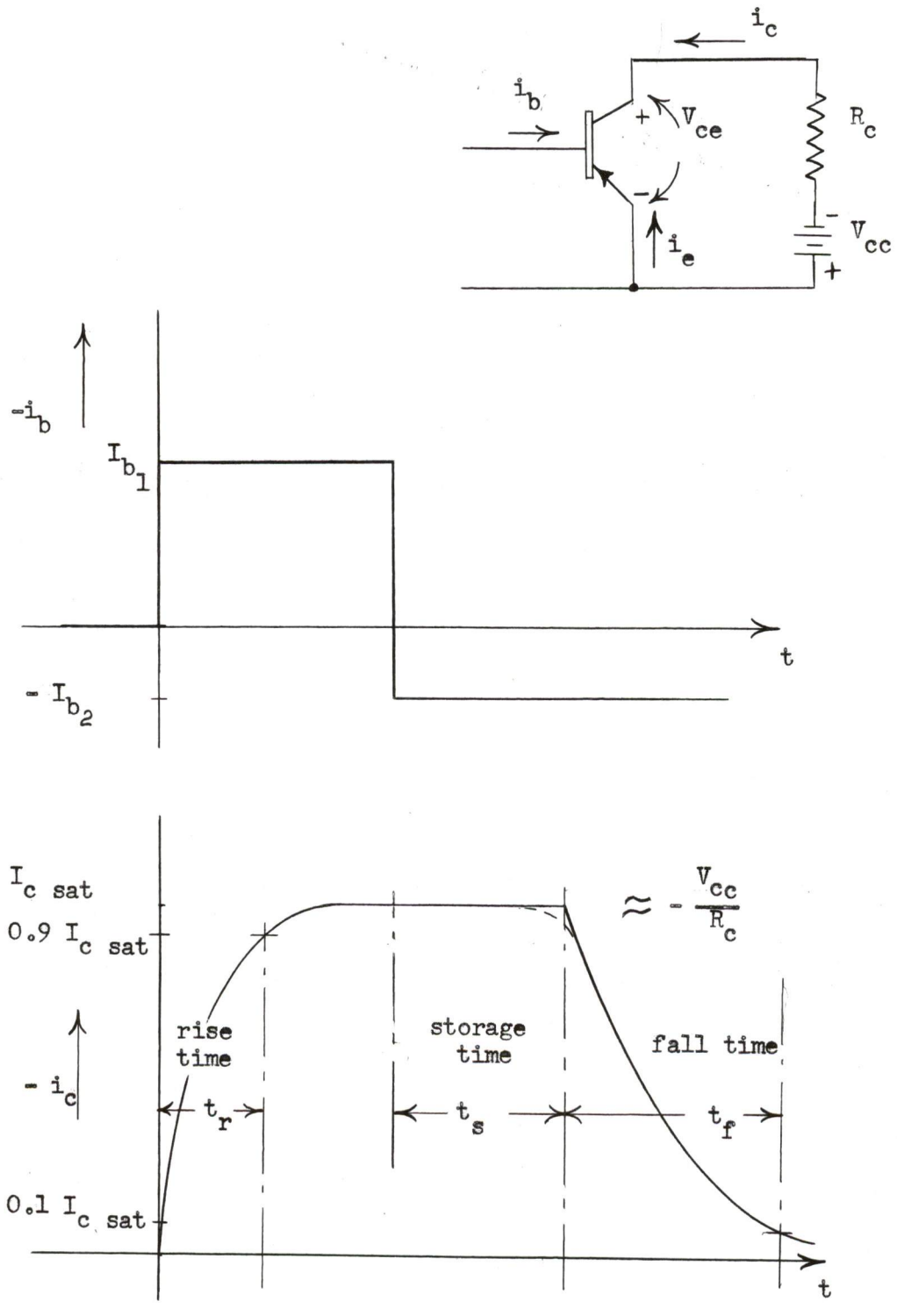

i_c
i_b
+
V_{ce}
R_c
-
V_{cc}
+
i_e
$-i_b$
I_{b_1}
t
$-I_{b_2}$
$I_{c\ sat}$
$0.9\ I_{c\ sat}$
$\approx -\frac{V_{cc}}{R_c}$
rise time
storage time
fall time
$-i_c$
t_r
t_s
t_f
$0.1\ I_{c\ sat}$
t

Figure 14

$$V_{ce\ sat} = \frac{kT}{q} \ln \left[\frac{1 - \frac{I_{c1}}{I_{b_1}} \left(\frac{1 - \alpha_n}{\alpha_n} \right)}{1 + \left(1 + \frac{I_{c1}}{I_{b_1}} \right) \left(\frac{1 - \alpha_i}{\alpha_i} \right)} \right] \qquad (90)$$

From the point of view of switching circuit design, equations (83) to (86) and (90) present the transistor switching characteristics in a highly satisfactory form. Knowing the normal and inverted, common-base, current gains, α_n, and α_i, and their respective cutoff frequencies, ω_n, and ω_i, of a transistor, one can relate the switching behavior of the transistor to its circuit environment in terms of the base current drives, I_{b_1}, and I_{b_2}, and the collector current, I_{c_1}. Thus, from a knowledge of the small-signal transistor parameters, α_n, α_i, ω_n, and ω_i, one can obtain a good idea of the over-all switching characteristics of a given switching circuit design for any particular type of transistor.

From the point of view of device design, on the other hand, the above-mentioned equations are not very useful. While these equations indicate the numerical values of α_n, α_i, ω_n and ω_i necessary to obtain a set of desired switching characteristics or, for a given transistor design, how and to what extent each of the electrical parameters should be varied to optimize its switching characteristics, the equations do not show how the electrical parameters are related to the physical design parameters of the transistor nor do they show how the electrical parameters are related, through the physical design parameters, among themselves. As we shall show, the electrical parameters are related in such a manner that in many cases the variation in a particular physical design parameter which results in a desired improvement in one electrical parameter produces undesirable changes (from the point of view of optimizing the switching characteristics of a transistor) in others. Consequently, in order to utilize equations (83) to (86) and (90) for the design of switching transistors, it is necessary first to establish the equations relating the electrical parameters α_n, α_i, ω_n and ω_i to the physical design parameters.

7.0 The Transformation Equations

In the foregoing pages of Part III of this paper, we have seen that the transient behavior of a transistor of arbitrary geometry with normal and inverted small-signal characteristics α_n, ω_n and α_i, ω_i, respectively, can be approximated with reasonable accuracy by two, idealized, one-dimensional transistors, one of which has the small-signal characteristics α_n, ω_n and the other α_i, ω_i, connected as shown in Figure 13. The analysis of the idealized, one-dimensional transistor which was discussed briefly above shows that the common-base, current gain, α_o, and its cutoff frequency, $\omega_{c\alpha}$, can be expressed in terms of the physical and geometrical parameters τ_p, the minority carrier life-time in the base region, and w, the width of the base region. The forms of these equations are given by (65) and (66). By identifying α_n with α_o, and ω_n with $\omega_{c\alpha}$, we have from (65) and (66) that

$$\alpha_n = \frac{1}{1 + \frac{W_n^2}{2D_p}\frac{1}{\tau_n}} \tag{91}$$

and

$$\omega_n = \frac{2D_p}{W_n^2} + \frac{1}{\tau_n} \tag{92}$$

where W_n is defined to be the base width of the equivalent, idealized, one-dimensional transistor for the normal-mode operation of the actual transistor.

τ_n is defined to be the minority carrier life-time in the base region of the equivalent, idealized, one-dimensional transistor for normal-mode operation of the actual transistor.

Similarly, by identifying α_i with α_o, and ω_i with $\omega_{c\alpha}$, we also have from (65) and (66) that

$$\alpha_i = \frac{1}{1 + \frac{w_i^2}{2D_p}\frac{1}{\tau_i}} \tag{93}$$

and

$$\omega_i = \frac{2D_p}{W_i^2} + \frac{1}{\tau_i} \tag{94}$$

where W_i is defined to be the base width of the equivalent, idealized, one-dimensional transistor for the inverted-mode operation of the actual transistor.

τ_i is defined to be the minority carrier lifetime in the base region of the equivalent, idealized, one-dimensional transistor for the inverted-mode operation of the actual transistor.

From (91), (92), (93), and (94), we see that the four small-signal parameters α_n, α_i, ω_n, and ω_i can be expressed completely in terms of w_n, w_i, τ_n and τ_i, the physical and geometric properties of the equivalent, idealized, one-dimensional transistors. As such, these relationships can be regarded as a set of transform equations since they essentially transform a realizable transistor into a pair of transistors of idealized one-dimensional form.

Comparing (91) (92) (93) and (94) with the set of equations given by (29) in Part I of this paper, we note that they are almost identical except for the fact that τ_b in the normal-mode transform equation of (29) is replaced by τ_n in (91) and (92) and, in the inverted-mode transform equations of (29), τ_b is replaced by τ_i in (93) and (94). The intended implication here, by making this symbolic distinction between the effective minority carrier lifetimes of the normal and inverted modes of operation, is that, in general,

$$\tau_n \neq \tau_i$$

The experimental evidence which substantiates this fact was pointed out and discussed in some detail in the introduction to this part (Part III) of the paper. Furthermore, in developing the first order switching theory which led to the transform equation (91) through (94), it was not necessary to impose nor did the switching theory imply any direct relationship between τ_n and τ_i. Consequently, in the rest of this paper we shall consider that, in general, no direct relationship exists between τ_n and τ_i.

As we shall see in Part IV of this paper, the rather subtle distinction that we have made between the minority carrier lifetimes in the base region of the normal- and inverted-mode, equivalent, one-dimensional transistor will enable us to express α_n, α_i, ω_n and ω_i more or less explicitly in terms of the actual physical and geometrical parameters of the realizable transistor and, ultimately, we shall be able to obtain expressions relating the switching characteristics, β_n, τ_s, $V_{ce\ sat}$ etc., to these same physical and geometrical parameters.

R. Best

Memorandum 6M-4561

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TX-0 Circuitry

To: K. H. Olsen

From: J. R. Fadiman

Date: October 22, 1956

Approved: K. Olsen
K. H. Olsen

Abstract: The high speed logical circuitry used in the TX-0 transistor computer uses Philco 5122 Surface Barrier transistors. AND and OR gates are formed from inverter or emitter follower combinations. The cascode configuration is used as a power amplifier for fast rise and fall times. Timing pulses are generated by vacuum tubes, and gated on and off by a register driver circuit. Marginal checking is accomplished by varying a positive base bias voltage. The TX-0 flip-flop is a high-speed flip-flop package using 10 SBTs and capable of 5 mcps operation.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

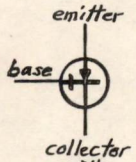
I. Introduction

A. The high speed circuitry for the TX-0 computer uses the Philco 5122 Surface Barrier transistor. The two logical levels are ground and -3 volts. Pulses are negative, with an amplitude of -3 volts and a width of from 80 to 100 mu sec. The supply voltages used for the SBT circuitry are -3, -10 and +10 volts.

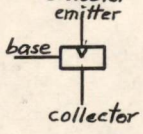
B. Symbols (Note)

The following symbols are used.

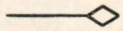
Transistor (in circuit schematics)



Transistor (in block schematics)



-3 volt level

Ground level 

Negative pulse (ground to -3 volts)

Positive pulse (-3 volts to ground)

-3 volt supply ●

ground ○

-10 volt supply ■

+10 volt supply □

Note 1: For detailed considerations of transistor logic and symbology, refer to: 6M-4571, by R. C. Jeffrey.

The logical circuitry for the central machine is constructed out of small plug-in units, each containing one, two, or three transistors and associated components. The types of units and their functions are listed below. The schematic circuit diagrams are in figure 1 and detailed descriptions are in the appendix.

Unit	Transistor	Use
P	1 SBT	Pulse input gate to flip-flop
L	1 SBT	Level input gate and inverter
M	1 SBT	Level input gate with high positive bias
R	1 SBT	Register driver inverter
S	1 SBT	Steering gate
T	1 SBT	Single transistor for single emitter-follower
E	2 SBT	Two emitter followers with separate outputs
A	3 SBT	Three emitter followers with a common output
C	2 SBT	Cascode Circuit
F	1 GE4JD1A17	Ferranti Circuit
F (Mod II)	1 GE4JD1A17	Ferranti Circuit
B	None	Emitter bias for register driver
G	1 GE4JD1A17	Indicator light circuit

II Logic

A. "AND" and "OR" Gates

The "AND" and "OR" gates for TX-0 are either emitter followers in parallel or inverters in series or parallel. The AND gate for ground level in, ground level out is emitter followers in parallel as shown in Fig. 2. Because of the restrictions of speed for 5 mcps circuits, a maximum of 10 emitter followers may be placed in parallel in this fashion, providing up to a 10-way AND gate. An inverting AND gate for ground level in, -3 level out is shown in Fig. 3. Because of limitations of speed, only two inverters may be placed in parallel. The capacitance to ground goes up as βC_c where C_c is the collector capacitance of an off transistor and β is the current gain of the transistor, grounded emitter. The inverting OR gate for ground level in, -3 level out is shown in Fig. 4. Because there is a finite voltage drop across a saturated transistor, (about 0.1 volt), only two inverters may be placed in series in this manner.

B. Inverter Circuit

For the inverter circuit (Fig. 5) the values of the input resistance and positive bias resistance are so calculated that there is safety margin when the transistor is saturated and when it is cut-off. This insures maximum noise rejection and tolerance to signal variation. It is assumed on the basis of several tests that no transistor will have a β of less than 5 at 5.5 ma. collector current. (Our minimum acceptance β at low current is 15, and 11 at end of life). A larger amount of positive bias is used on inverter input gates to flip-flops when the input is from a distant frame, such as from core memory, toggle switch storage, or the photo-electric tape reader. In these cases the induced noise voltages are apt to be larger than usual, and the input impedance to the flip-flop is sufficiently high to allow the use of the larger positive bias current, and consequently smaller input base current.

This bias is also used in cases where the ground level for the emitter is supplied from an emitter follower gate. Such a level goes

0.3 volt positive and thus it is necessary for the base to be held at about +0.5 volts to provide adequate margins during cut-off.

All of the inverters in TX-0 use a supply voltage of -10 volts. However, the actual voltage at the collector never exceeds -4 volts, since it is clamped, either by an emitter follower following it, or by a voltage divider to ground. A single inverter provides current sufficient for driving three emitter followers or two inverters. It can drive a capacitance of 75 uuf, with a fall time of 0.1 μ sec.

C. Emitter Follower Circuit

The logical circuitry utilizes a combination of inverters and emitter followers which in general are alternated. This ensures that when an emitter follower is turned on, it is always kept in saturation since its base is returned effectively to -10 volts through the load resistor of the previous inverter. The difference in driving capabilities of the saturated and non-saturated emitter follower is shown in the graph of Fig. 6. The load resistance of the emitter follower is returned to +10 volts instead of to ground to shorten the rise time of the emitter follower. This emitter follower will provide 8 ma. of output current at -3 volts and will drive a capacitive load of 120 uuf, with a rise time of 0.1 μ sec.

D. Cascode Circuit

In order to achieve faster rise and fall times and greater driving ability than is possible with either the emitter follower or the inverter, the "cascode" circuit is used. The logical and circuit schematics are shown in Fig. 7. The inputs to Q_2 and Q_3 are always opposite in phase so that in the steady state case only one transistor is conducting. Q_3 acts as an emitter follower which provides the driving current and pulls the input quickly down to -3 volts. Q_2 acts as an inverter whose function is to pull the output quickly up to ground during the transition. Thus, the circuit utilizes the fast rise time of the inverter and the fast fall time of the emitter follower.

This configuration is capable of driving a capacitive load of 420 uuf. with a transition time of 0.1 μ sec. No power is wasted in load resistances, and this circuit is designed to provide 12 ma. output current at -3 volts. It will drive 12 emitter followers or 8 inverter bases, and one emitter of an inverter. TX-0 uses the cascode as the output stage of all flip-flops, as a power amplifier for driving many transistor bases, and as a cable driver.

Cascode cable drivers are used when sending levels to the memory over 160 ohm coaxial cable. The cable is terminated at the input end by a resistance in series with the cable. This series termination is possible because, unlike the emitter follower or inverter, the cascode circuit looks like a very low impedance (less than 10 ohms) when driving in either direction. Thus, the driven end of the cable is properly terminated at all times.

III Pulse Circuitry

A. Timing Pulses

The timing pulses for the computer are generated by vacuum tubes. Thirty volt positive pulses are sent to the computer through 93 ohm coaxial cables. 7:1 pulse transformers with a one turn secondary are used at the computer to provide approximately 3.4 volt negative pulses. A 1N283 diode is used across the primary in order to damp the overshoot.

B. Register Driver

Gated register drivers (Figures 8 and 9) supply the 3 volt negative pulses to the input gates of the flip-flops. The pulse input is at the collector of Q_3 and the output is from the emitter. A pulse is passed when Q_3 is saturated from the negative output of inverters Q_1 and Q_2. Thus, a ground input to either Q_1 or Q_2 is necessary to pass a pulse through the register driver. The two inverters in series thus give a two-way OR circuit for the pulses. Up to a 10 way OR circuit can be constructed by paralleling register drivers with a common pulse input and output but different gating. In order to form an AND circuit for pulses, emitter follower gates are

placed in parallel to feed the inputs of the inverters. All the inputs must be at ground to pass a pulse. The pulse output of the register driver closely follows the pulse input. The maximum pulse current is 30 ma., sufficient for driving 10 pulses bases, and the pulse voltage drop through the register driver is less than 0.5 volt.

C. Pulse Inputs to Flip-Flops

In order to set or clear the TX-0 flip-flop the "one" or "zero" input must be brought up to ground by the output of a pulse inverter. Up to 15 such inputs may be tied in parallel to one side of the flip-flop. The negative pulse is inverted and gated by a circuit such as this: Fig. 10. Or, alternately, only one transistor may be used as a gate in this manner: Fig. 11. Here a ground level must be supplied to the emitter in order to pass the pulse. This arrangement requires a level current equal to $\frac{I_c}{\alpha}$ while the two transistor gate requires a level current equal only to $\frac{I_c}{\beta} = \frac{I_c}{\alpha}(1-\alpha)$. In order to complement the flip-flop, the pulse must be steered to the proper side of the flip-flop. The circuit which does this is shown symbolically in Fig. 12.

IV Marginal Checking

Marginal checking of all TX-0 circuitry is accomplished by varying the +10 voltage on the base of the inverter transistors. Increasing this positive bias supply effectively reduces the negative base current into the transistor and tends to bring it out of saturation. Making the positive bias supply negative tends to allow the transistor to conduct when it should be held cut off. Emitter followers are not directly marginal checked, but their condition can be investigated by marginal checking the inverters which proceed and follow it. For these inverters normal margins are slightly greater than $\pm$ 10 volts either side of the normal +10 volt supply.

V Flip-Flop

The TX-0 flip-flop is shown in Fig. 13. The circuitry is similar to that already described, with RC coupling between inverters, positive bias, and emitter follower clamping. Q_1 and Q_2 are pulse amplifiers

which are normally conducting and are cut off by the positive input pulse at the "zero" or "one" input. Q_3 and Q_4 are the flip-flop transistors themselves which are arranged in a conventional RC-coupled Eccles-Jordan trigger circuit. When an input pulse cuts off Q_1 or Q_2 this opens the emitter circuit of Q_3 or Q_4, and changes the state of the flip-flop. Q_5 and Q_6 are inverters which are used to saturate the emitter followers of the output cascode. Q_7 and Q_8, and Q_9 and Q_{10} form the cascode circuits on the "one" and "zero" sides respectively. Their operation is the same as that previously described for the cascode circuit, with the opposite phases being obtained from the inverters on opposite sides of the flip-flop.

The output wave form at 10 mcps is shown in Fig. 14, and various marginal checking curves and output characteristics of the flip-flop are shown in Figs. 15 through 22.

J. R. Fadiman

J. R. Fadiman

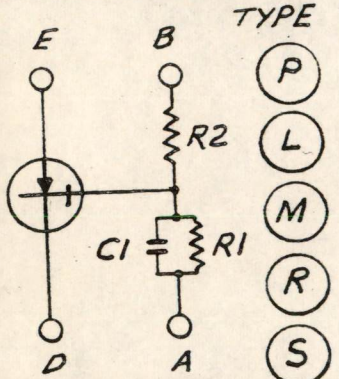
Attachments:

Fig. 1: SA-65640-3
Figs. 2 through 12
Fig. 13: D-63369
Fig. 14: A-65366
Fig. 15: A-67294
Fig. 16: B-65729
Fig. 17: B-65721
Fig. 18: B-65720
Fig. 19: B-65719
Fig. 20: B-65727
Fig. 21: B-65717
Fig. 22: B-65718
Appendix (15 pages)

JRF:mmw

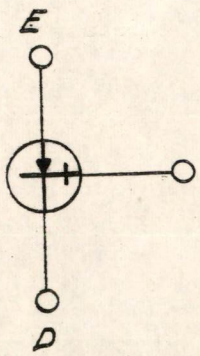
SA 65640-3

TYPE	R1	C1	R2	USE
P	2.7K	22pf	56K	PULSE INPUT GATE
L	2.2K	47pf	82K	LEVEL INPUT GT. & INV.
M	2.2K	47pf	39K	MBR LEVEL RD-IN FROM MEMORY
R	1.5K	68pf	15K	REGISTER DRIVER INV.
S	3.9K	47pf	180K	STEERING GATE



PHILCO 5122

TYPE T

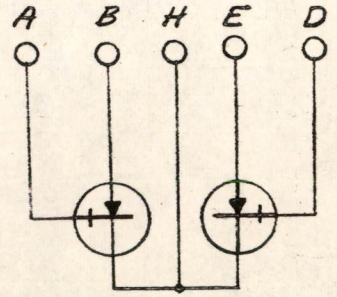


SINGLE TRANSISTOR

PHILCO 5122

TYPE E

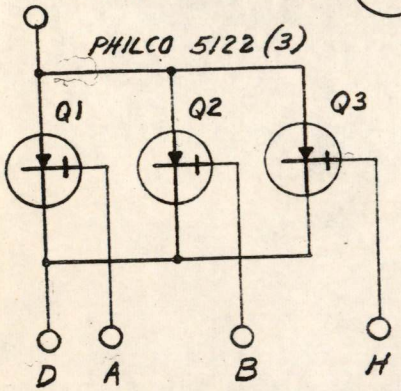
TWO E.F'S.

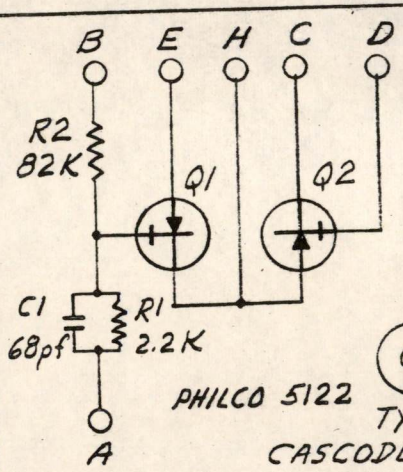


PHILCO 5122

E THREE E.F.s TYPE A

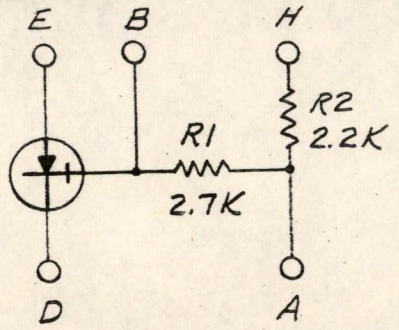
PHILCO 5122 (3)





PHILCO 5122

TYPE C CASCODE

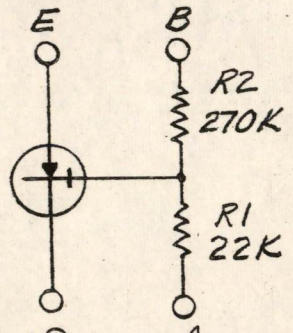


GE 4JD1A17

TYPE F

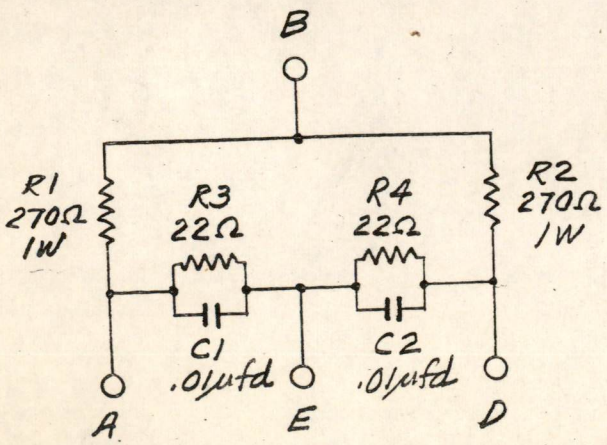
FERRANTI

TYPE G



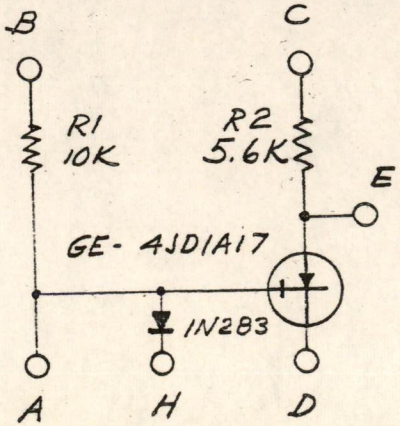
GE 4JD1A17

INDICATOR LIGHT CIRCUIT



TYPE B

BIAS



FERRANTI (MOD II) F II

"BOTTLED" PLUG-IN UNITS PIN CONNECTIONS.

3-19-56

SA 65640-3

AND

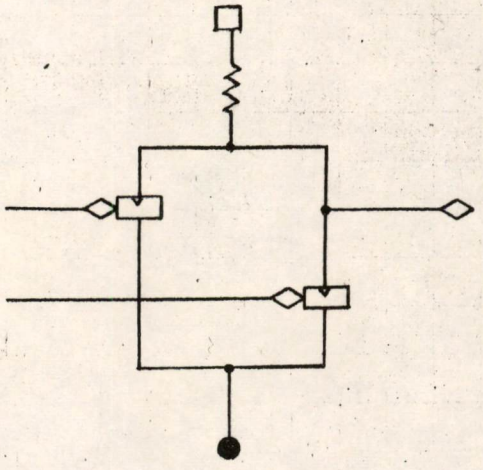


FIG. 2

AND

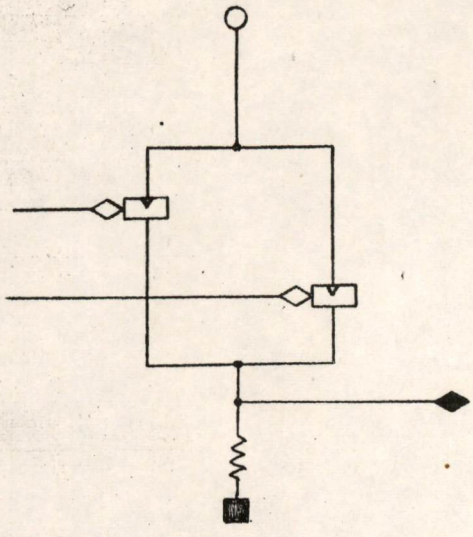


FIG. 3

OR

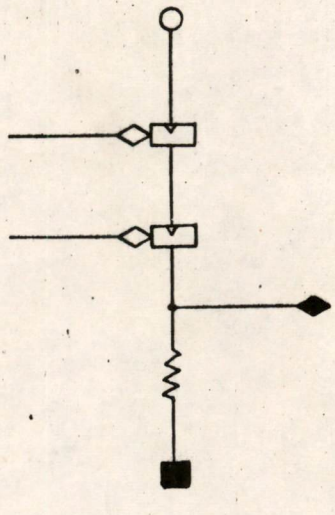


FIG. 4

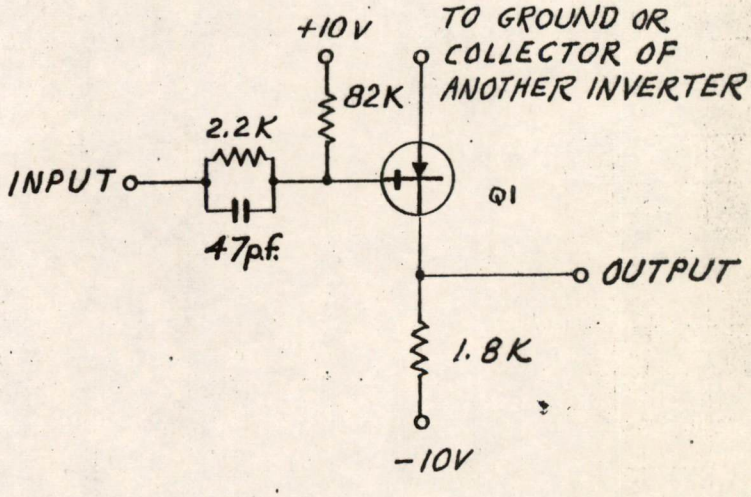


FIG. 5

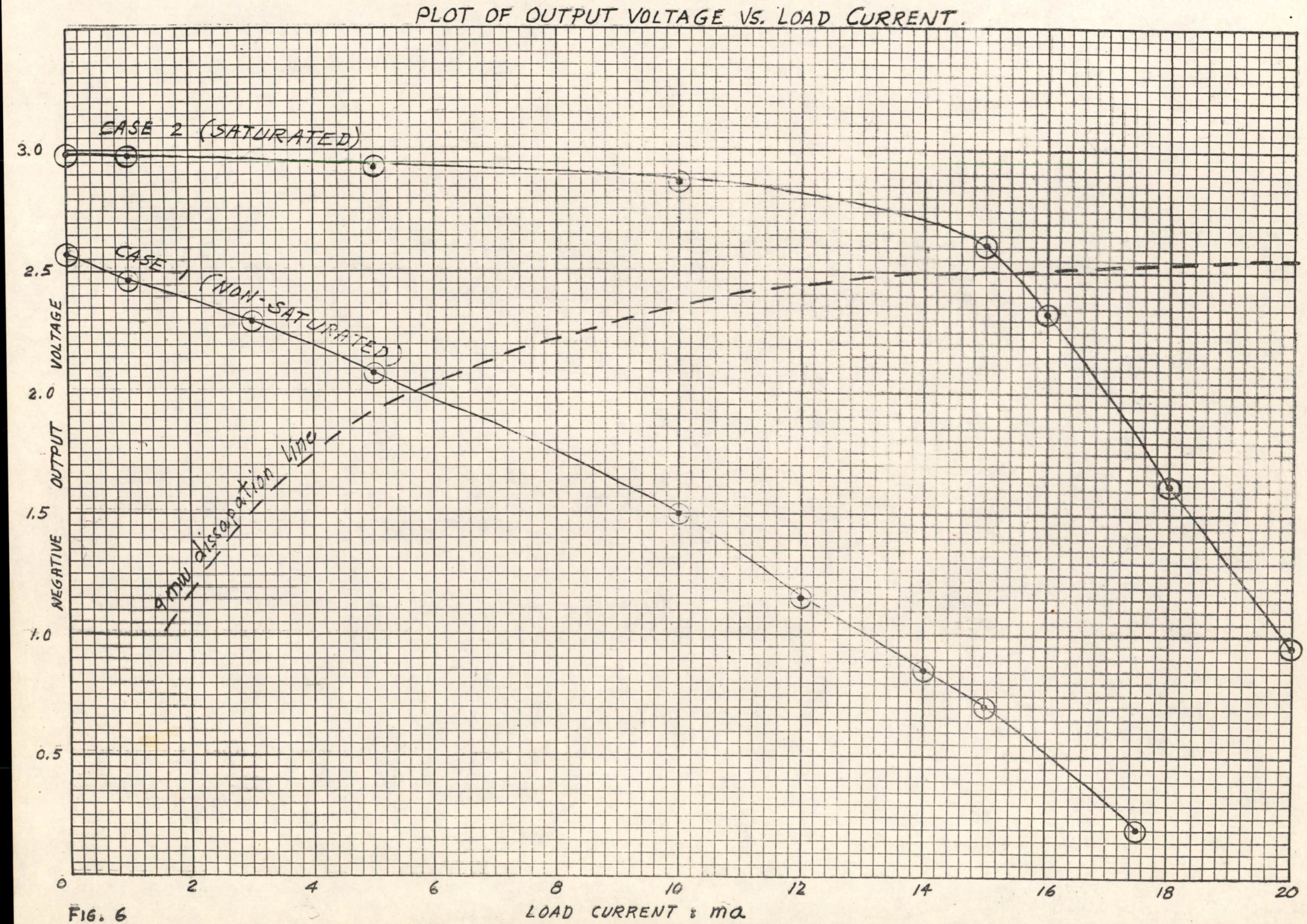
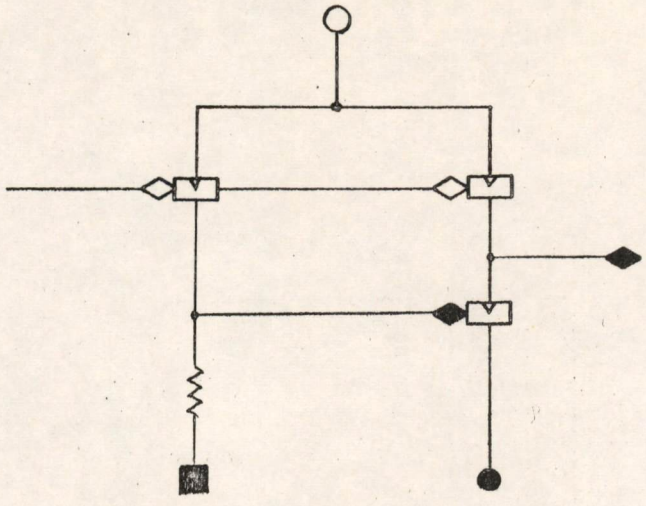
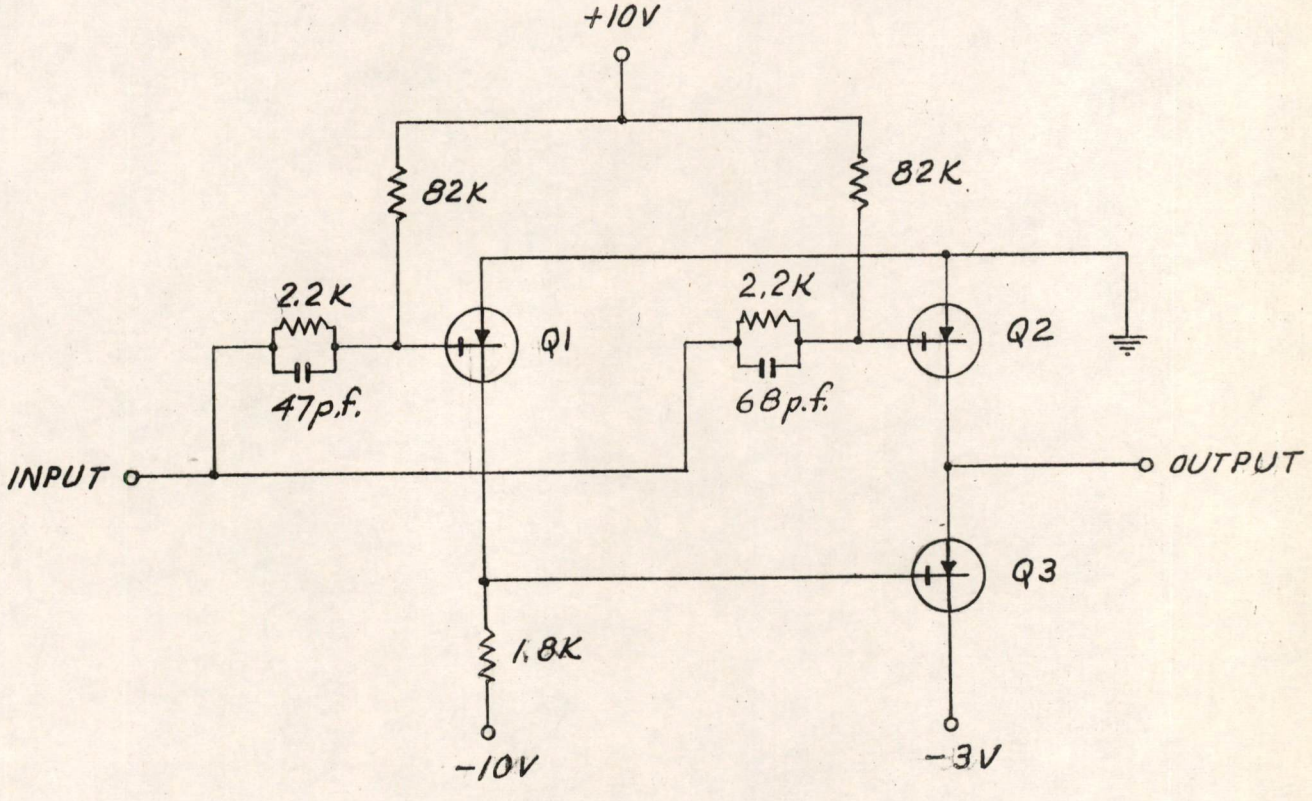


FIG. 6





FIGS. 7

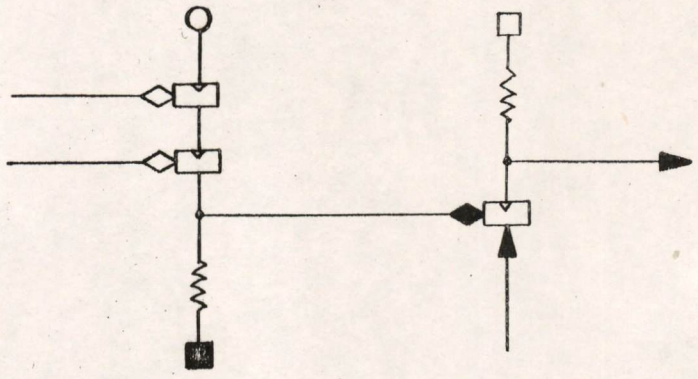


FIG. 8

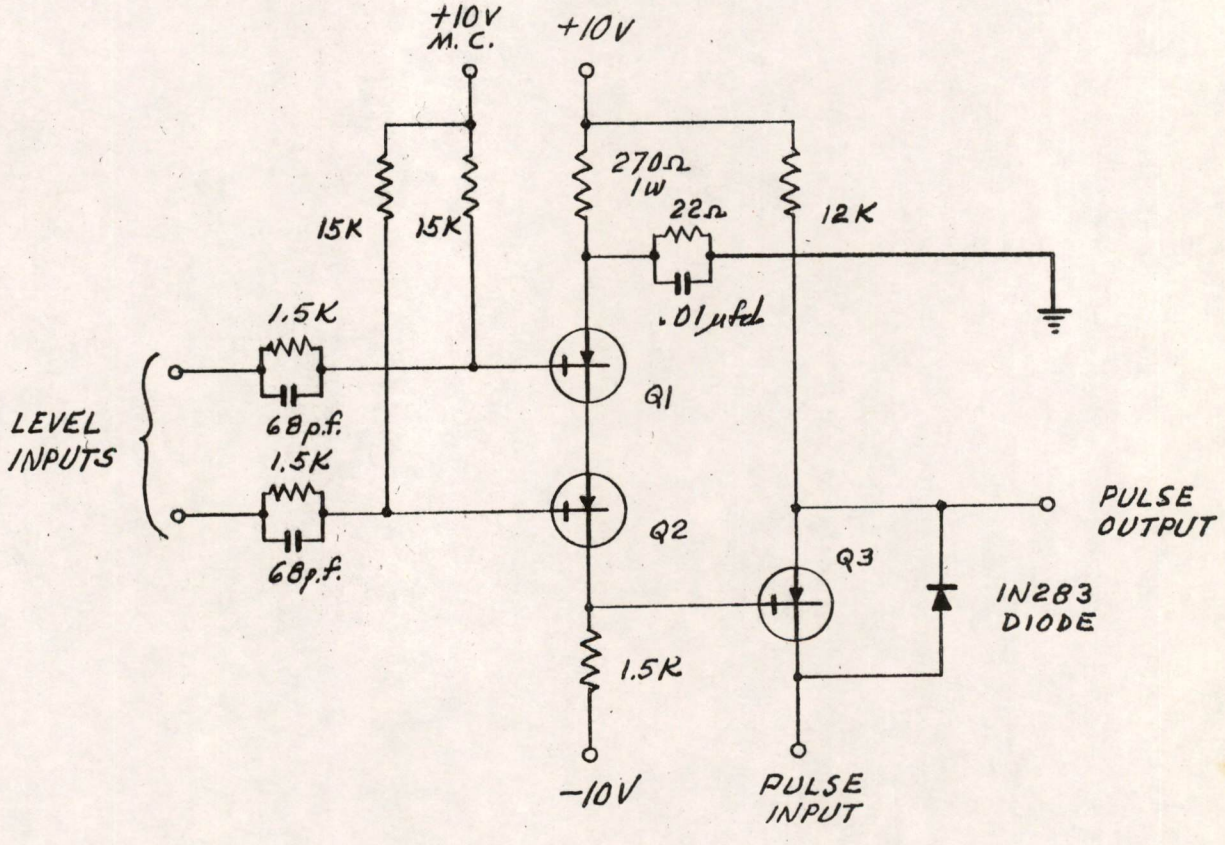

+10V
M.C.
+10V
270Ω
1W
22Ω
12K
15K
15K
.01 μfd.
1.5K
Q1
LEVEL
INPUTS
68p.f.
1.5K
Q2
68p.f.
PULSE
OUTPUT
Q3
IN283
DIODE
1.5K
-10V
PULSE
INPUT

FIG. 9

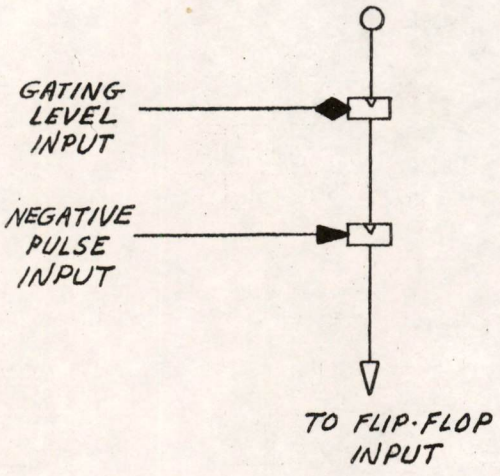


FIG. 10

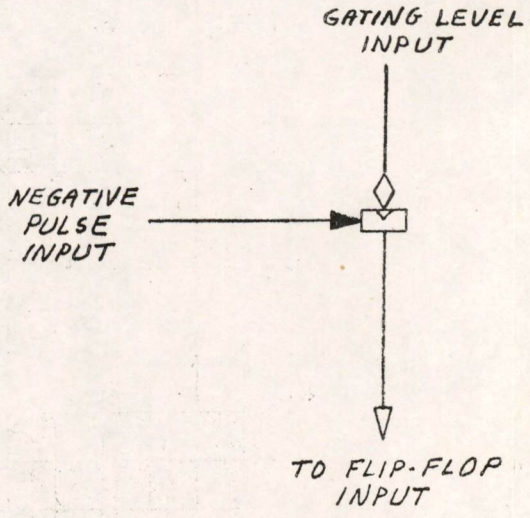


FIG. 11

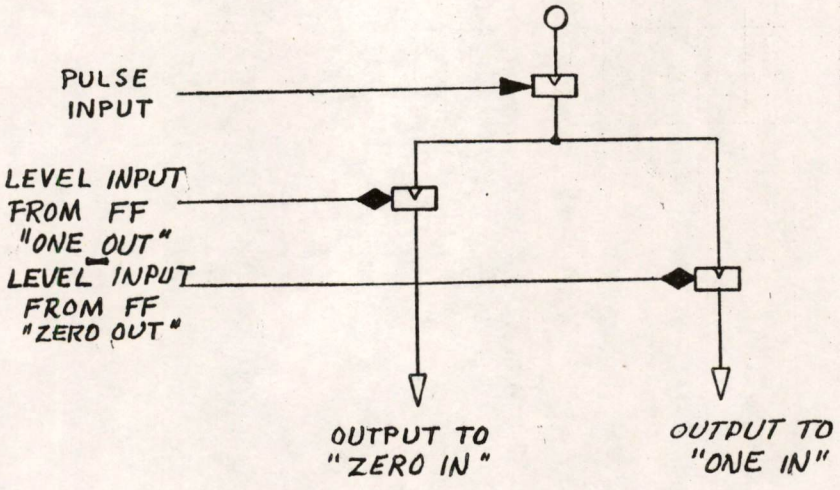


FIG. 12

D-63369
VG-71
F-3140
SN-1328
F-3181

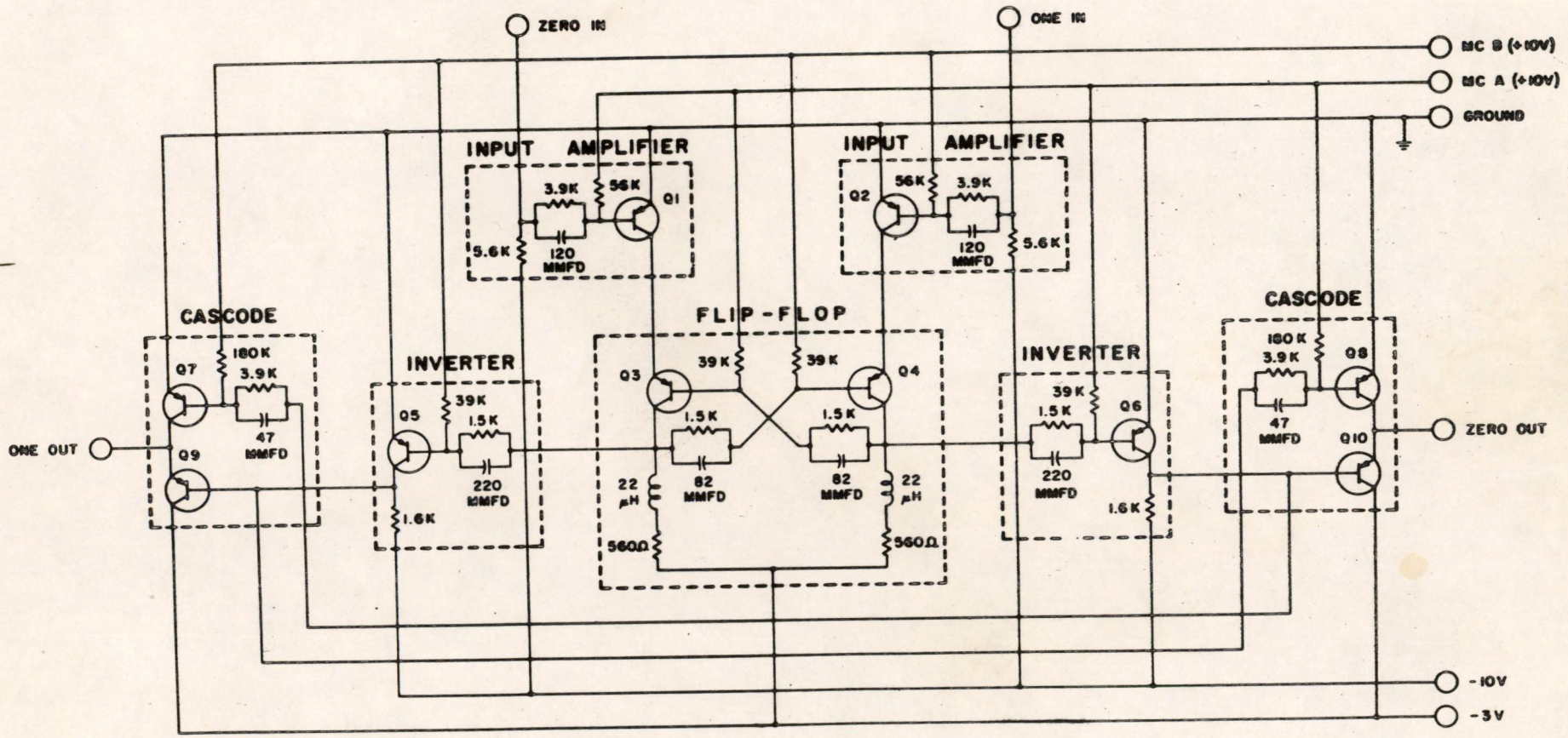
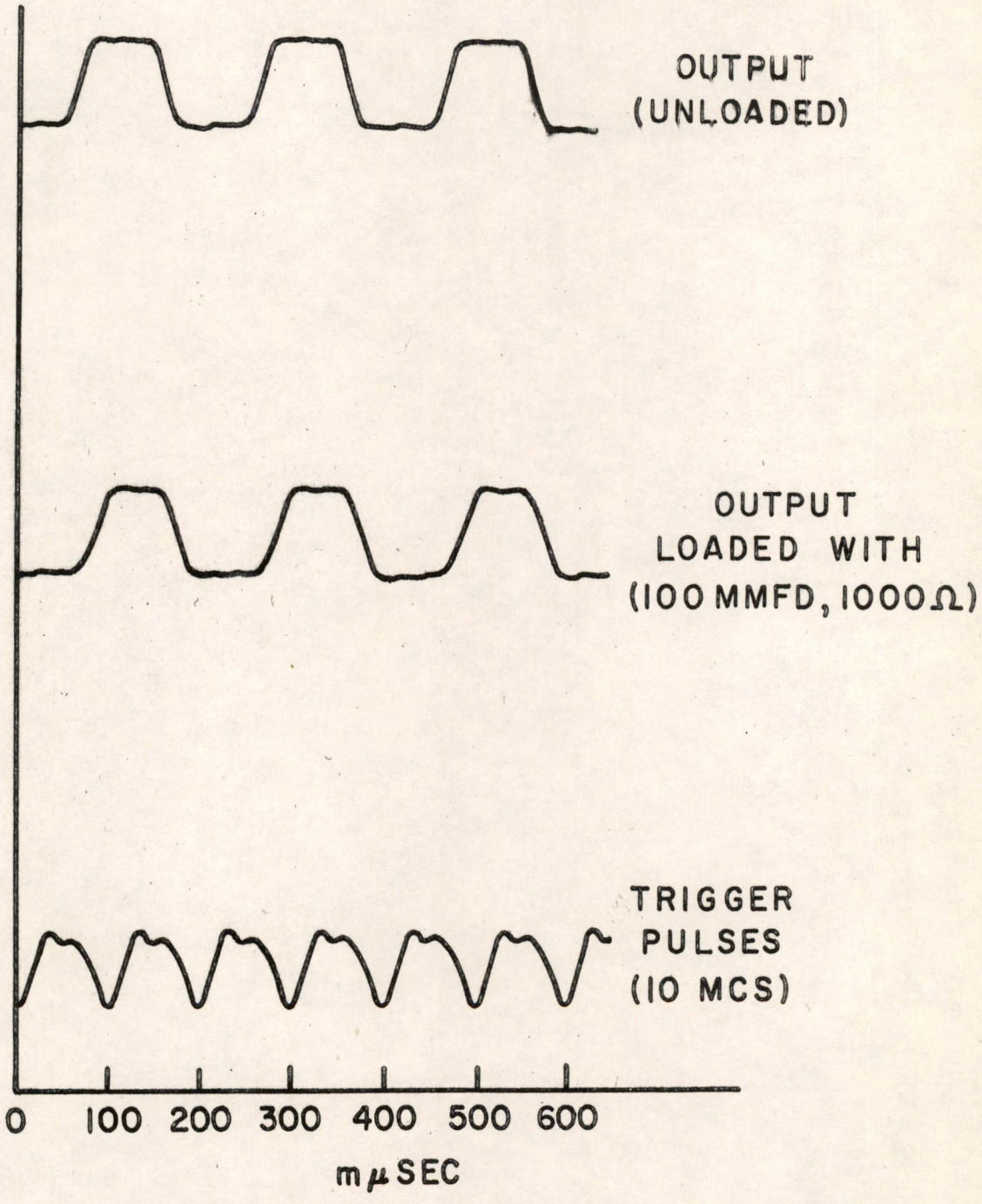


FIG. 13

TX-0 FLIP-FLOP



TX-0 FLIP-FLOP

A-65366
VG-82
SN-1327
F-3180

063-11

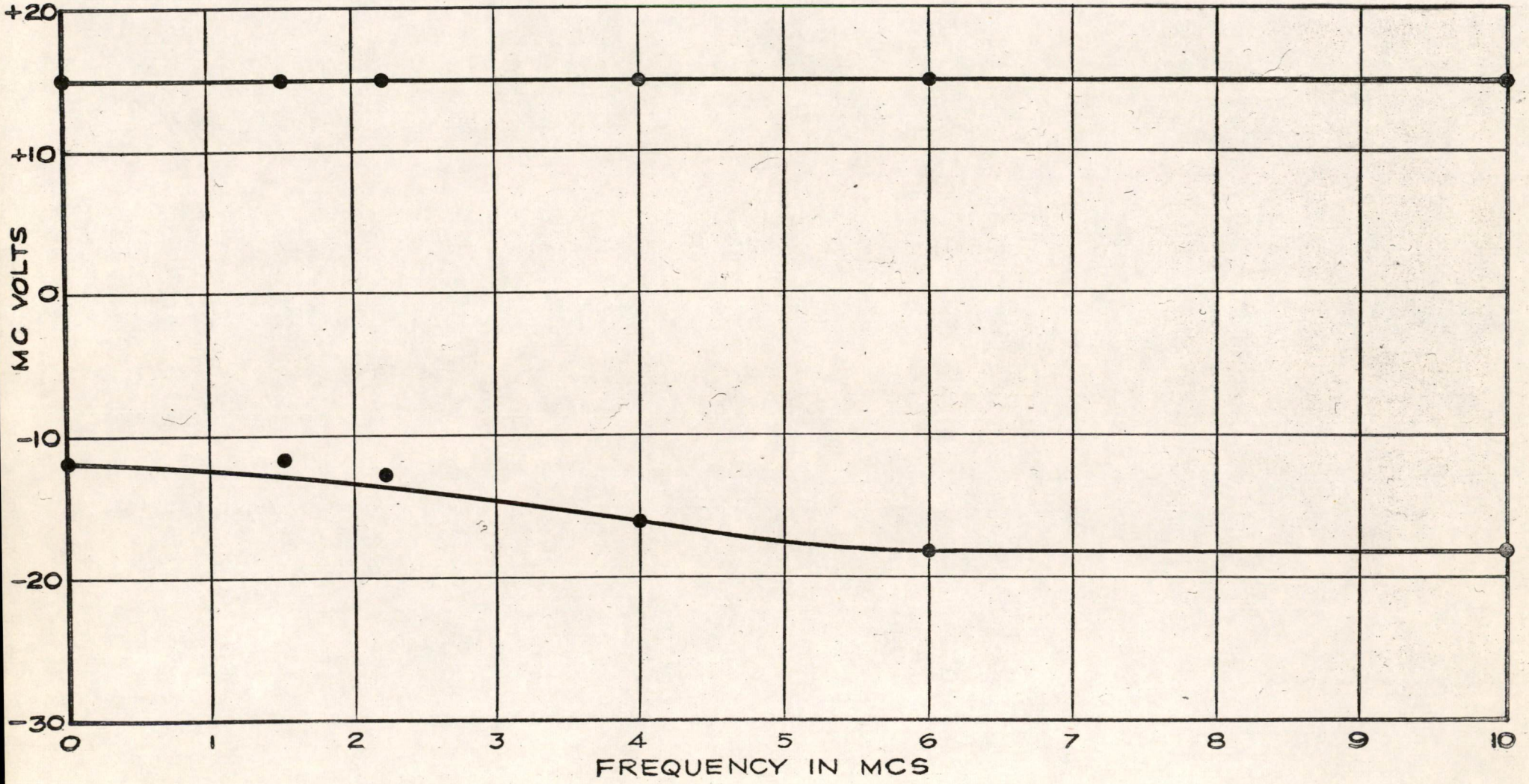
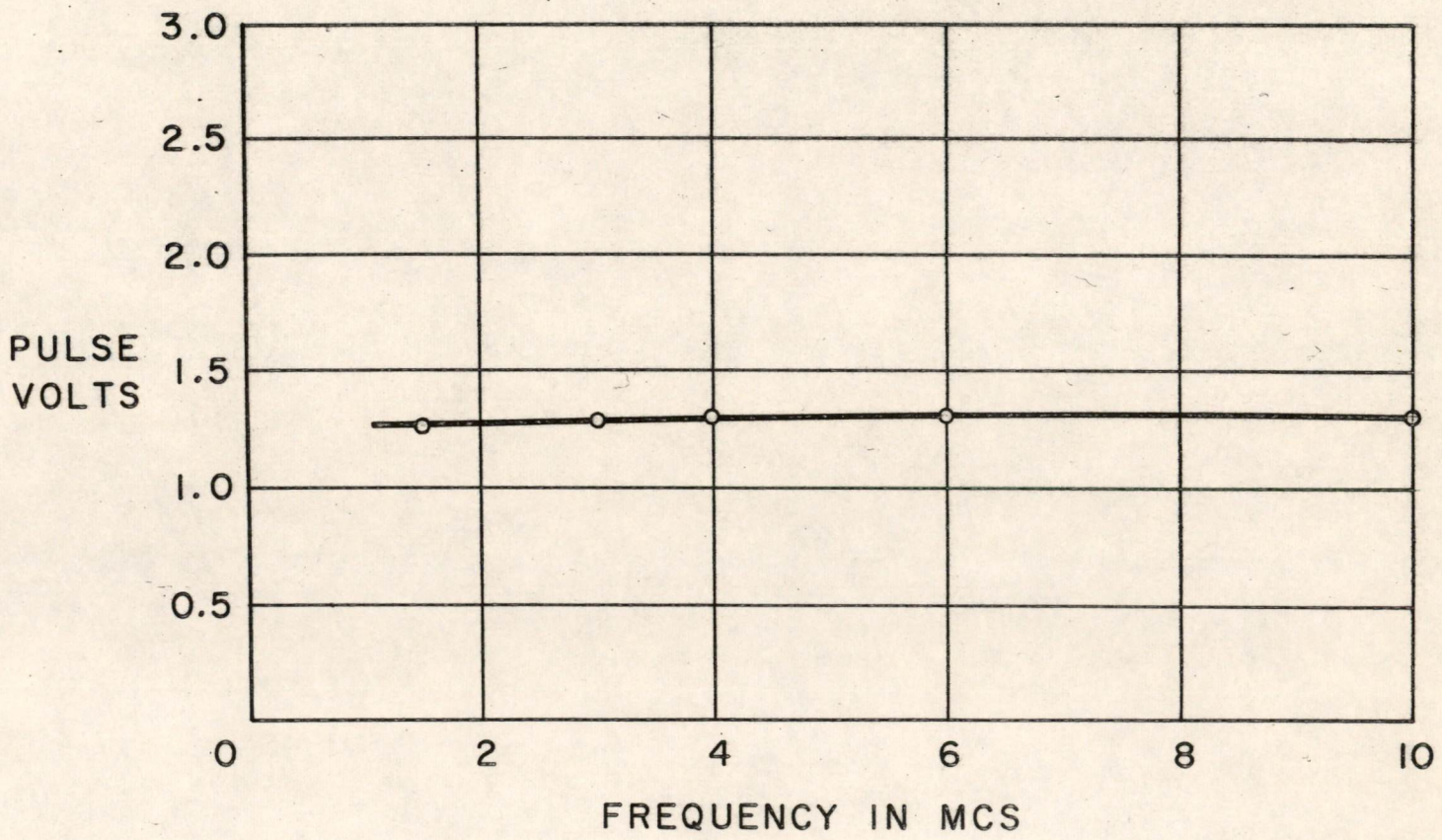


FIG. 15

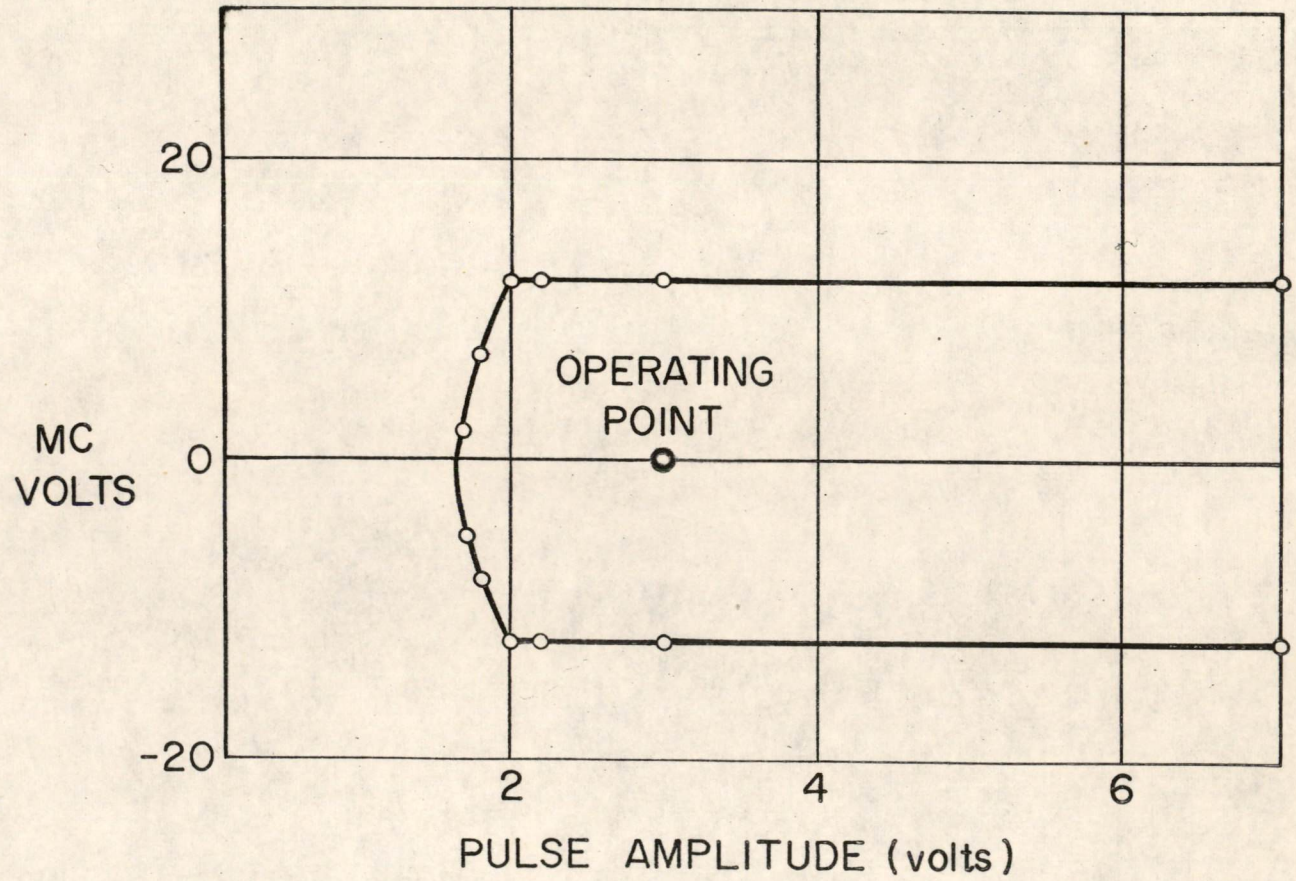
FREQUENCY MARGINS

B-65729
SN-1329
F-3184



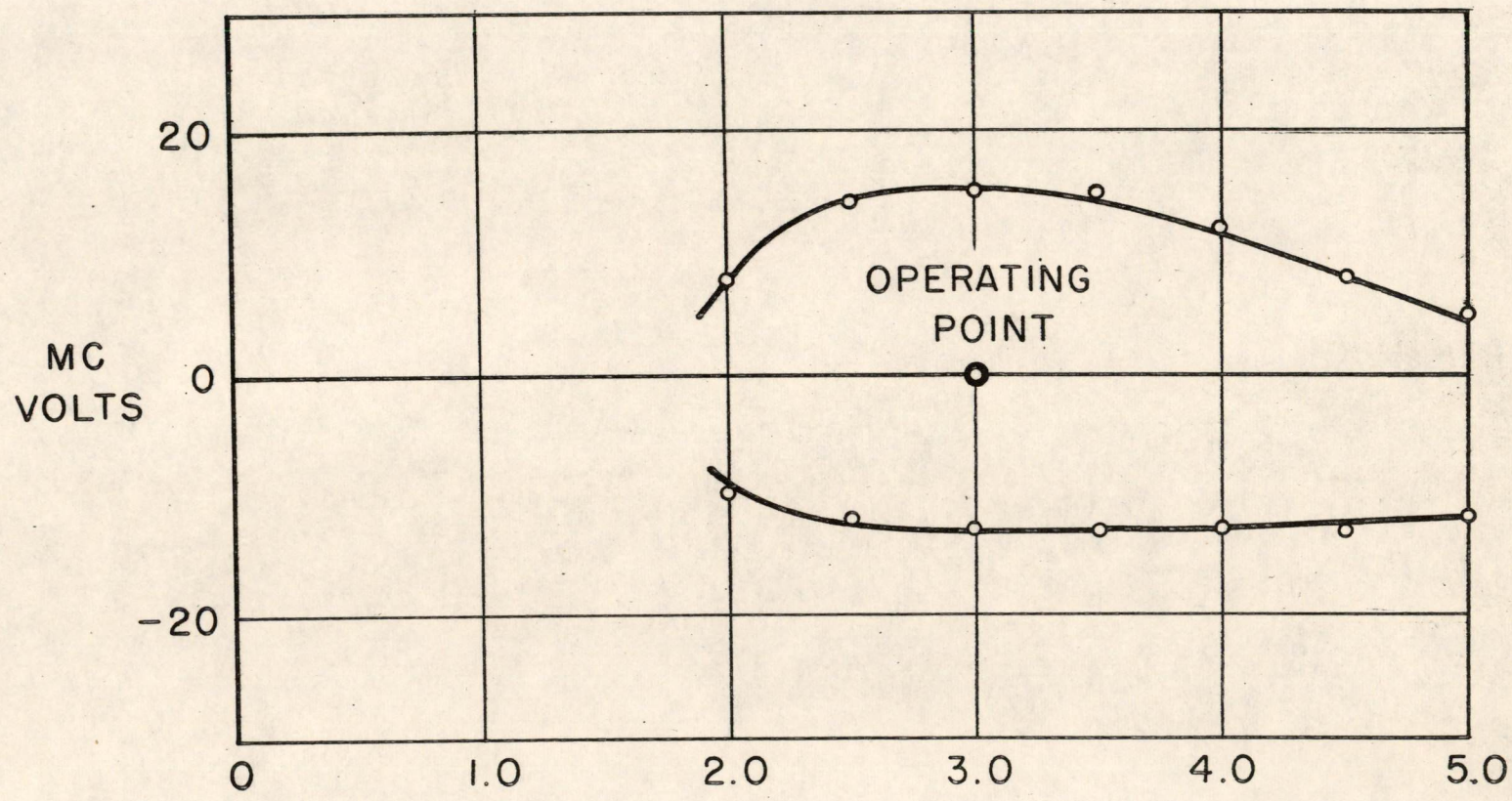
TRIGGER SENSITIVITY

B-65721
SN-1325
F-3178



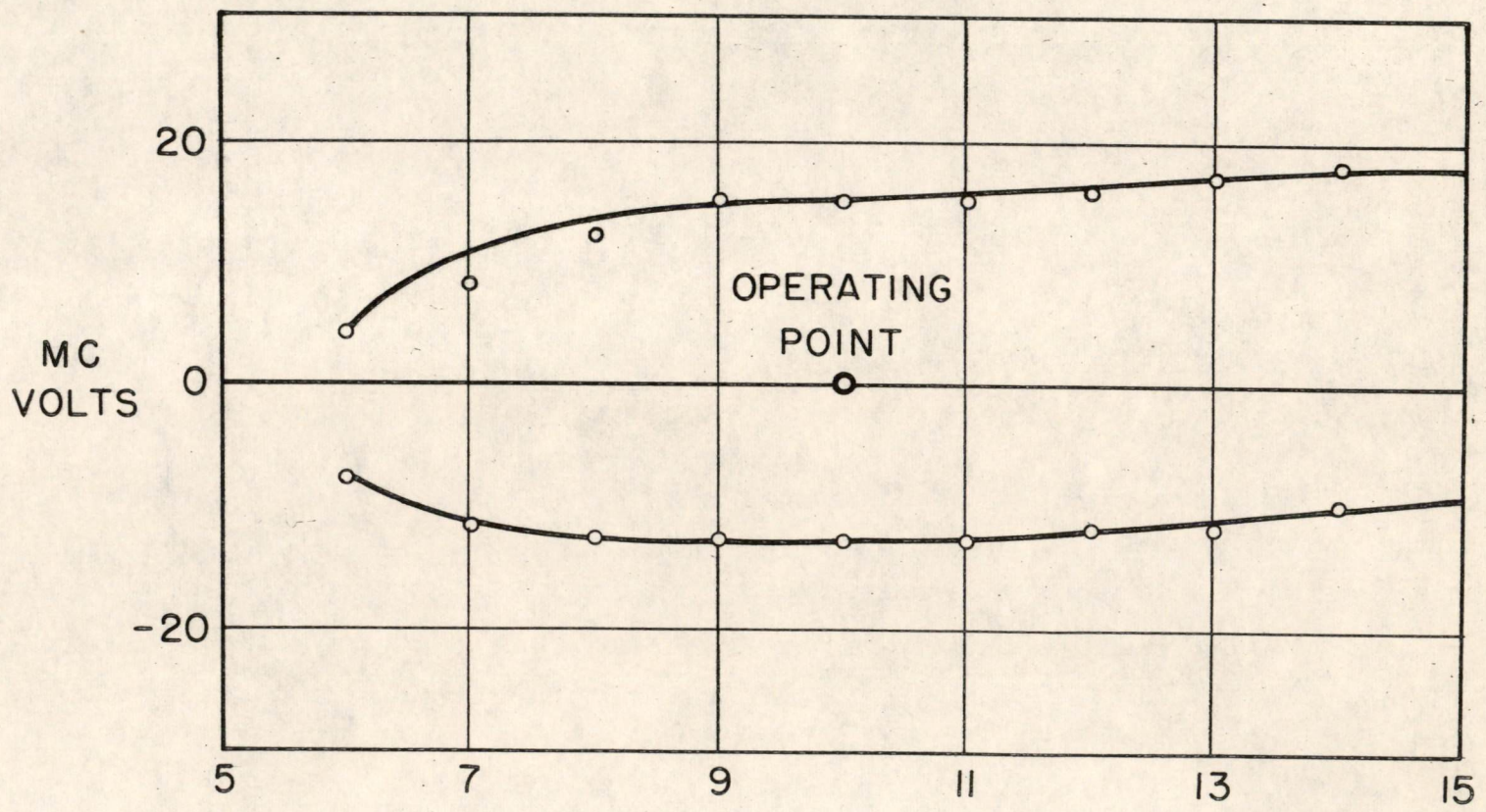
PULSE MARGINS

B-65720
SN-1324
F-3177



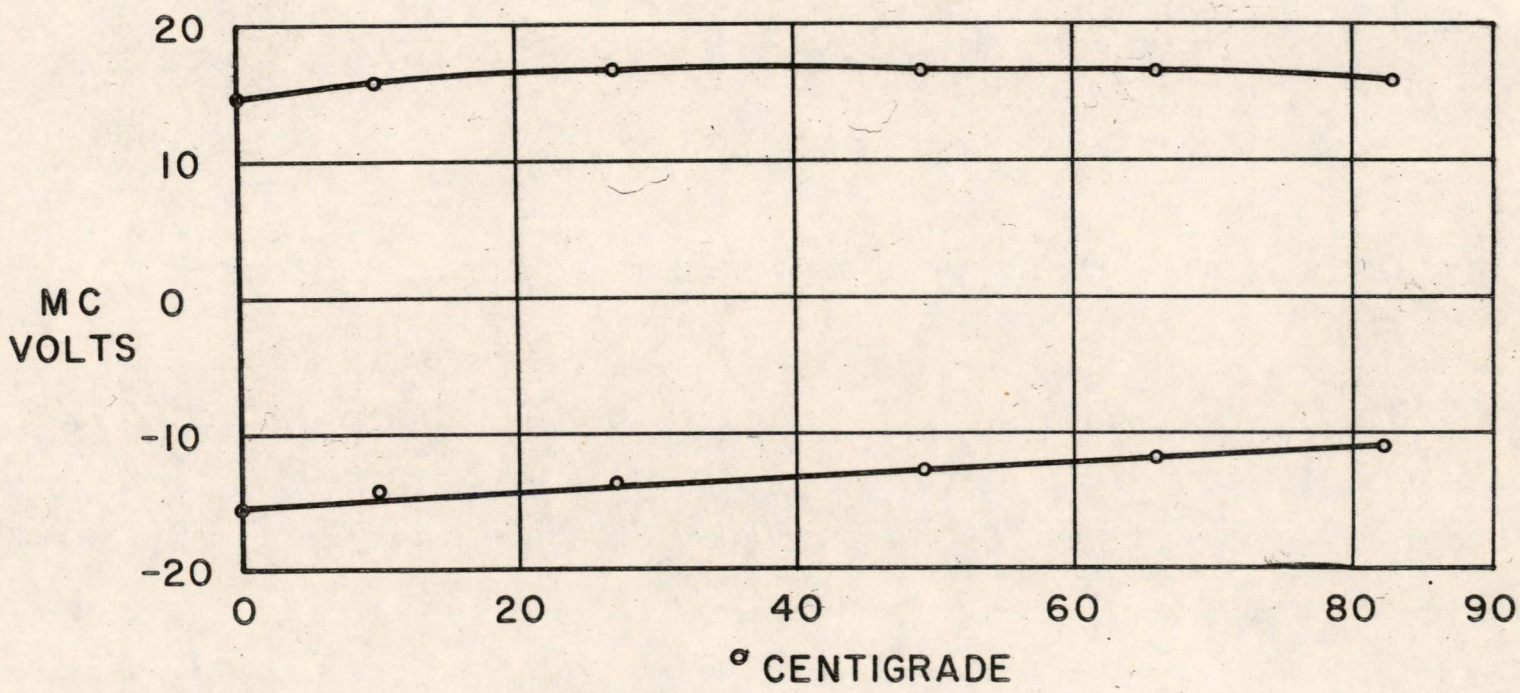
-3 VOLT SUPPLY MARGINS

B - 65719
SN - 1323
F - 3176



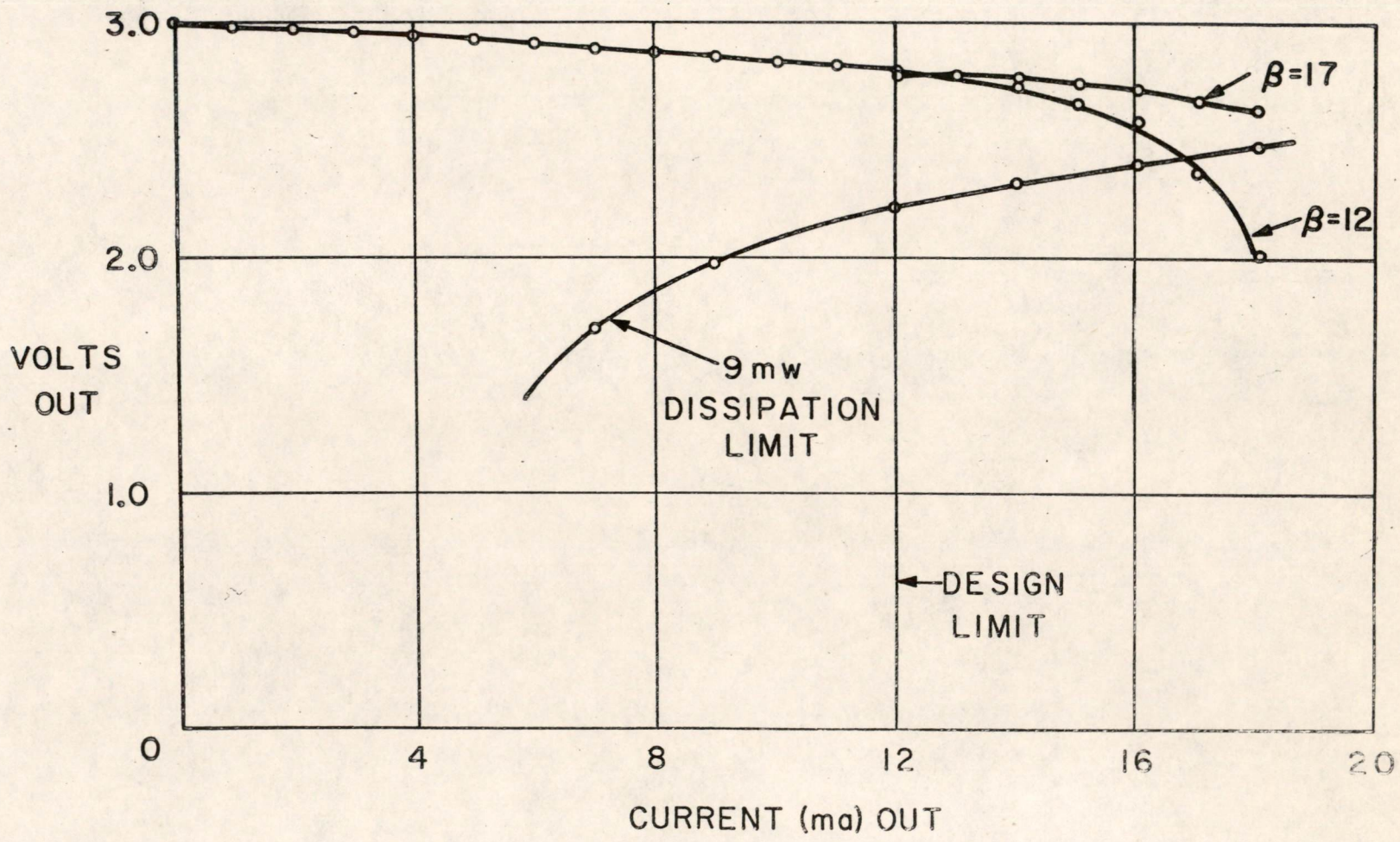
-10 VOLT SUPPLY MARGINS

B-65727
SN-1330
F-3185

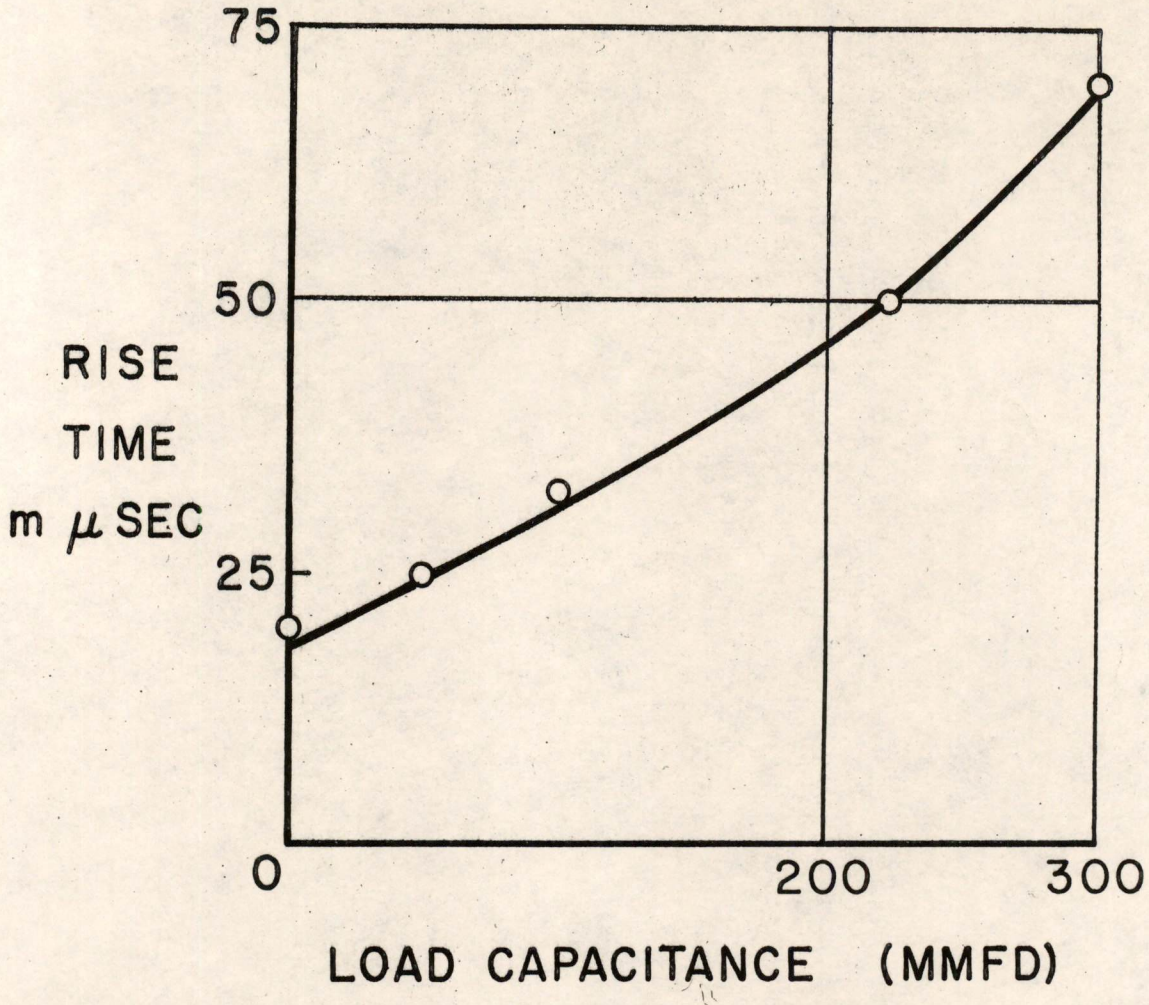


TEMPERATURE MARGINS

B-65717
SN-1321
F-3174



OUTPUT VOLTAGE



RISE TIME

A-65718-1
SN-1414
E-3275

APPENDIX

Data On Individual TX-0 Circuits

Inverter

1) Uses: Logical inverter and voltage amplifier. When placed in series, gives OR circuit for ground in, -3 out. When placed in parallel, gives AND circuit for ground in, -3 out.

2) Input: Voltage level at ground or -3 volts. Input current required: 1.1ma.

3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current at -3 volts: 3.5 ma. can drive maximum of 3 emitter followers or two inverters. Load capacitance for 0.1 μsec fall time: 75 uuf. Delay: 30mμsec.

4) Restrictions: When turned off, collector voltage must not exceed -4 volts. Maximum of two inverters in series. Maximum of 2 inverters in parallel for 5 mcps operation.

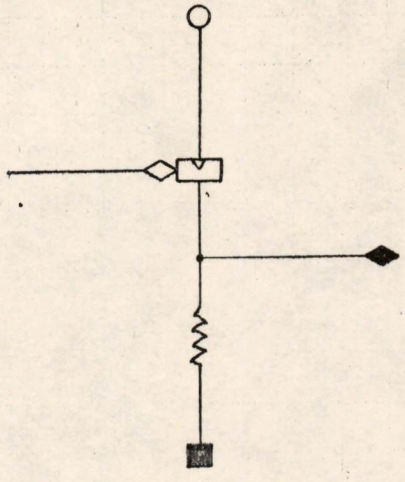
5) Power required: 5.5ma at -10v.

0.12 ma. at +10v.

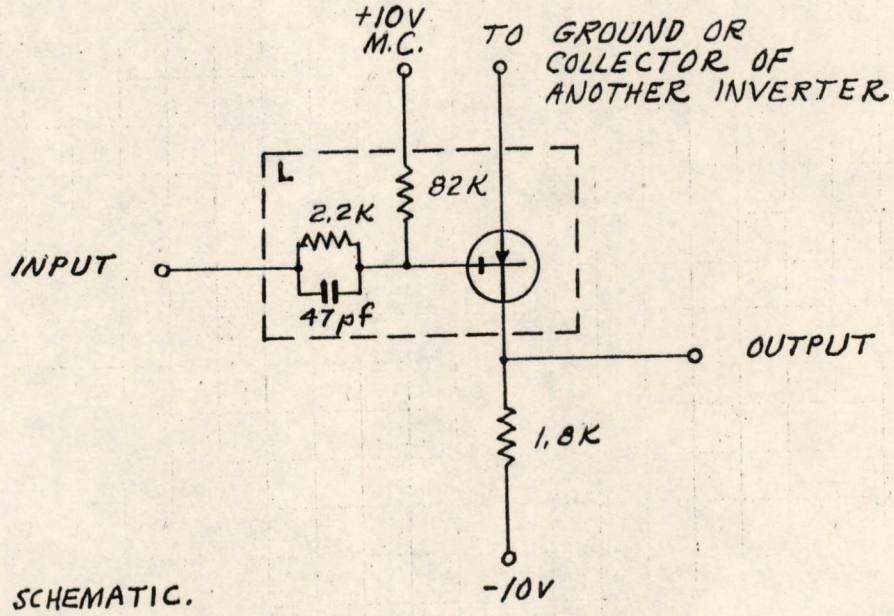
6) Marginal checking: Vary +10 volt positive bias on base.

7) Plug-in units used: L or M.

INVERTER.



8) BLOCK SCHEMATIC.



9) CIRCUIT SCHEMATIC.

EMITTER FOLLOWER

1) Uses: Current amplifier. When placed in parallel with common load resistance gives AND circuit for ground in, ground out.

2) Input: Voltage level at ground or -3 v. Input current required: $\frac{\text{Load current +3 ma.}}{6}$ Input current will be from 0.5 to 1.8 ma.

3) Output: Same polarity as input. Voltage level at +0.3 v. or -2.9v. Maximum output current at -3 v.: 8 ma. Can drive maximum of 8 emitter followers or 2 inverters, providing output current does not exceed 8 ma. Two emitter followers in parallel (R=2K to +10 v.) can drive one emitter of pulse transistor with no delay or one emitter of level transistor with 90 mμsec. rise time. Maximum output current at ground in this latter type of operation: 5 ma. Load capacitance for 0.1 μsec rise time: 120 uuf.

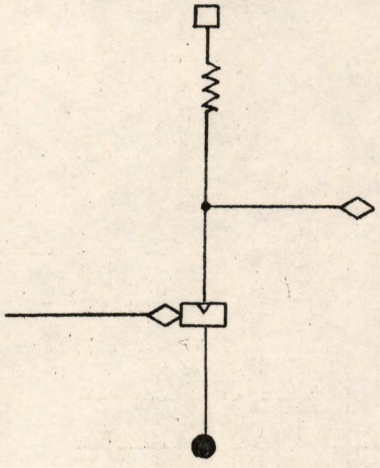
4) Restrictions: Not more than 10 emitter followers may be placed in parallel for 5 mcps operation. Emitter followers cannot be placed in series. Only 2 emitter followers may be cascaded provided that the first emitter follower is saturated from -10 volts. Otherwise, emitter followers may not be cascaded.

5) Power required: 8 ma. at -3 v. (maximum)
3.3 ma. at +10 v.

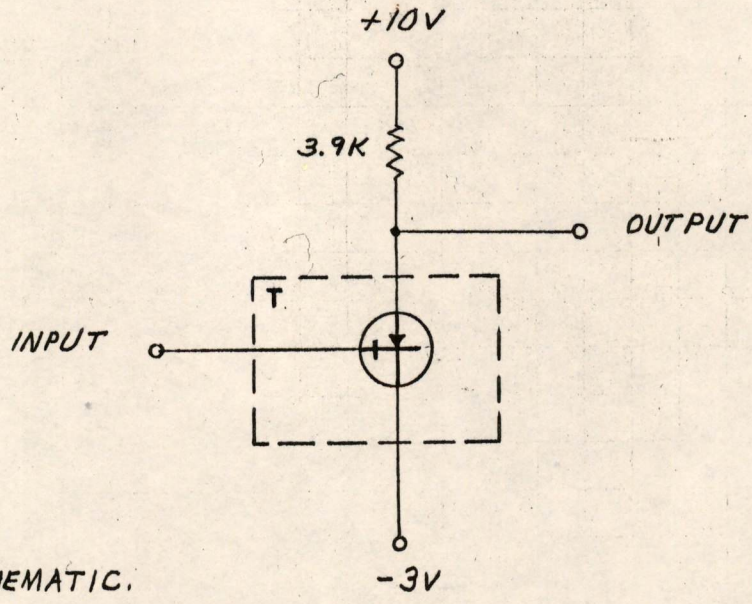
6) Marginal checking: None.

7) Plug-in units used: T or E or A.

EMITTER-FOLLOWER



8). BLOCK SCHEMATIC



9). CIRCUIT SCHEMATIC.

Register Driver

1) Use: Gating circuit for pulses for pulse inputs to flip-flops.

2) Level input: Ground level for passing pulse. -3 volt level for no pulse output. Level input current required: 2.2 ma.

3) Pulse input: -3.4 volt 80 to 100 musec pulse. Input pulse current equal to output pulse current.

4) Output: -3 volt 80 to 100 musec. pulse. Pulse amplitude equals input amplitude minus transistor drop. Drop less that 0.5 volt. Maximum pulse current: 30 ma. Can drive maximum of 10 pulse bases. Set-up delay: about 20 musec.

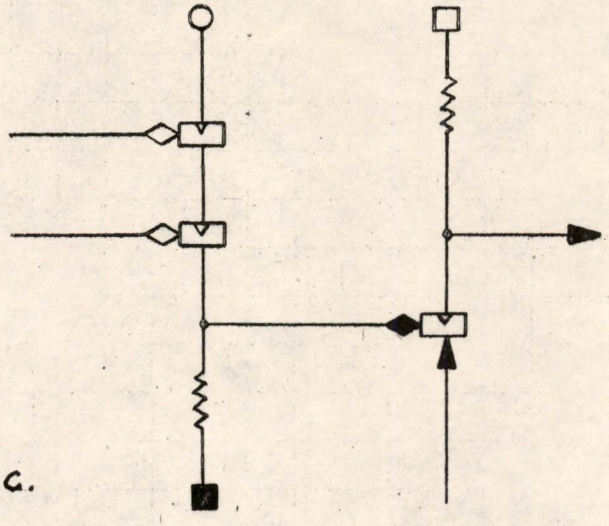
5) Restrictions: Two register drivers driven from the same input gate will drive maximum of 20 bases. Up to 10 register drivers may be placed in parallel with different gating to form a 10-way OR circuit for pulses. Placing up to 10 emitter follower gates in parallel before the register driver gives a 10-way AND circuit for pulses.

6) Power required: 6.6 ma. at -10 v.
35 ma. at +10 v.

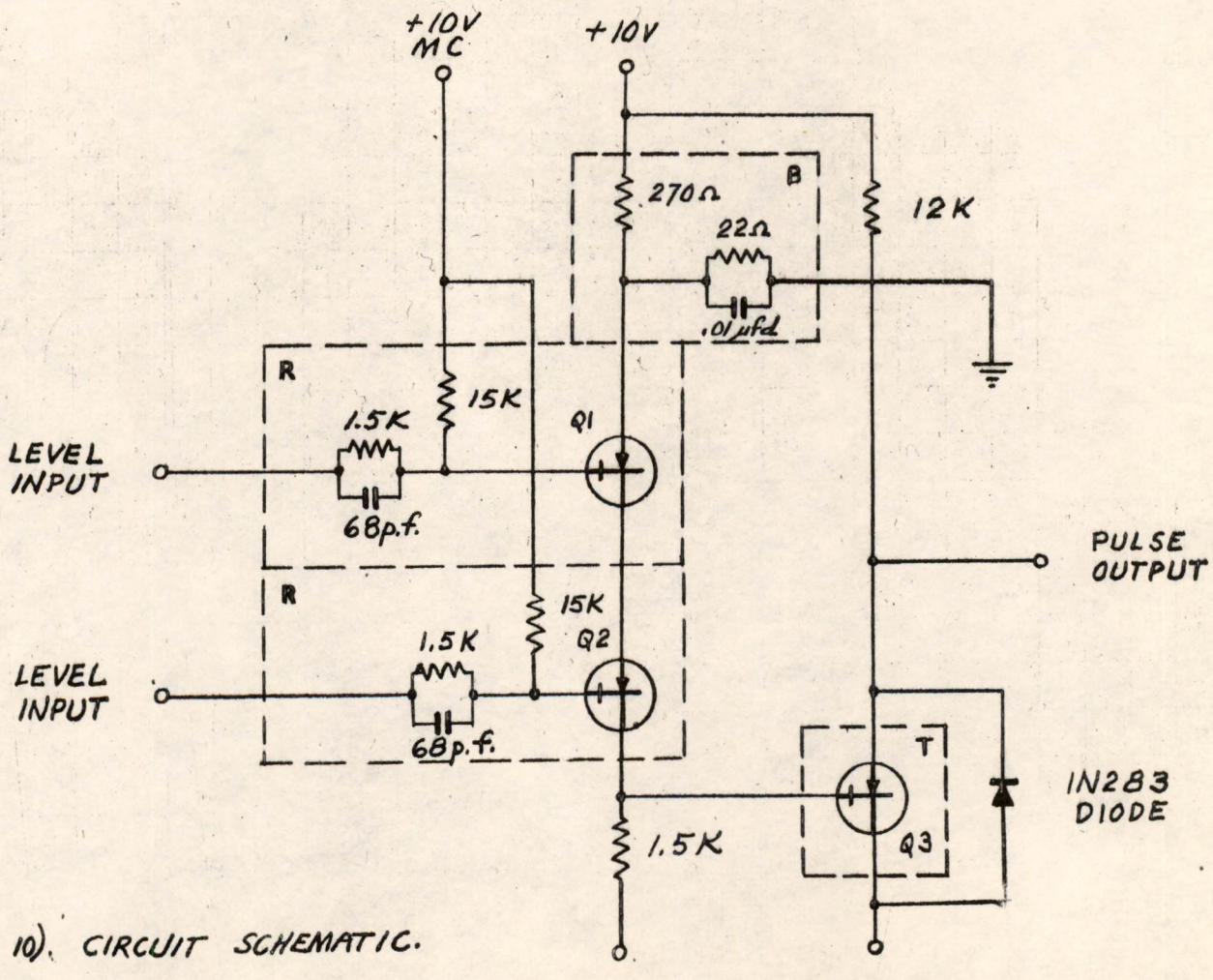
7) Marginal Checking: Vary +10 volt positive bias on inverter bases.

8) Plug-in units used: 1 or 2 R, B, T or E or A.

REGISTER DRIVER.



9). BLOCK SCHEMATIC.



10). CIRCUIT SCHEMATIC.

Pulse and Steering Gates

1) Use: Provide pulses to complement flip-flop.

2) Pulse input: -3 volt 80 to 100 μsec. pulse. Pulse current required: Maximum of 3 ma.

3) Level inputs: Voltage level at ground on one input, -3 volts on the other, coming from the outputs of the flip-flop to be complemented. Input current required to each base at -3 v.: 0.67 ma.

4) Output: Positive pulse up to ground. Will complement one flip-flop.

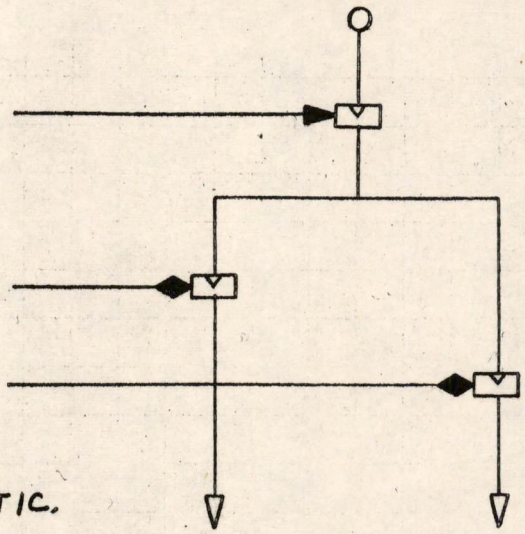
5) Restrictions: There must be no more than 3 transistors in series, including gating level input, pulse input, and steering gate. Up to 15 gates may be placed in parallel on one side of flip-flop input.

6) Power required: 0.24 ma. at +10 v.

7) Marginal checking: Vary +10 volt positive bias on bases.

8) Plug-in units used: 1P, 2S.

PULSE & STEERING GATES.



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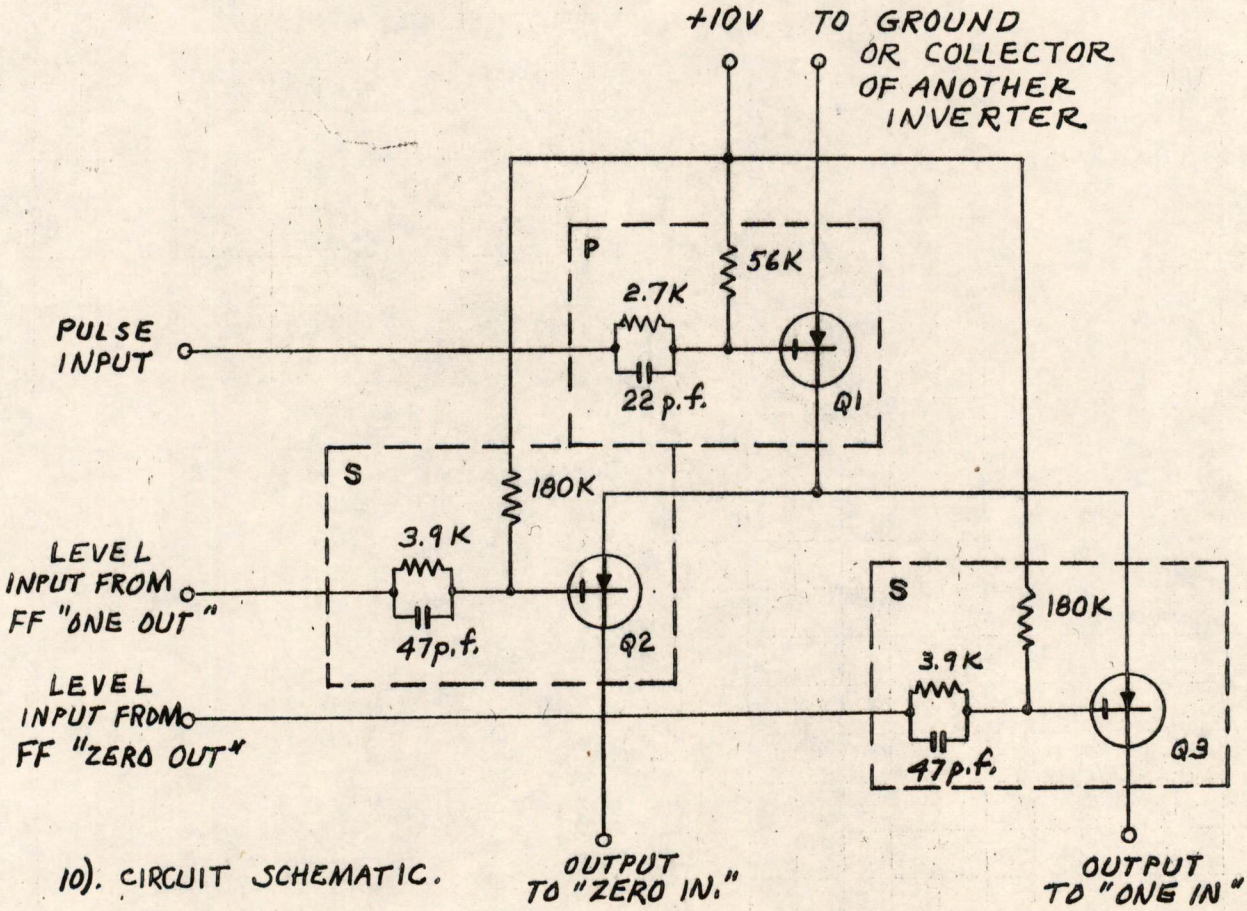


10). CIRCUIT SCHEMATIC.

Inverting Cascode

1) Uses: Power amplifier and level driver.

2) Input: Voltage level at ground or -3 volts. Input current required: 2.2ma.

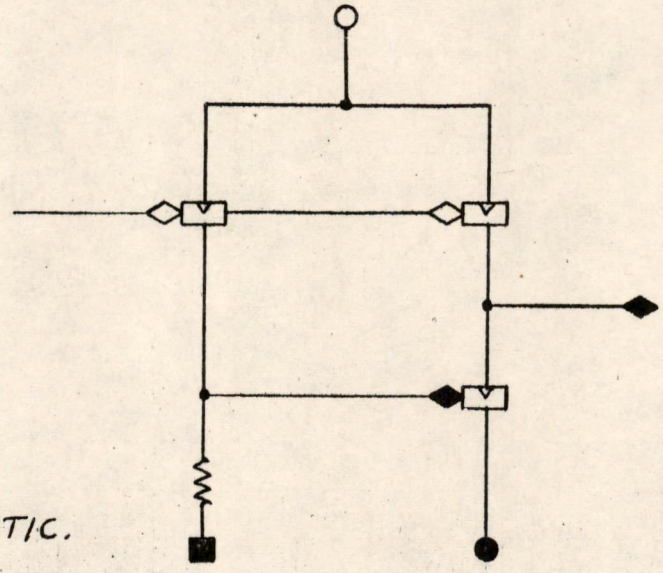
3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current: 12 ma. at -3 v.: 4 ma. at ground level. Can drive maximum of 12 emitter followers or 8 inverters, and one emitter of pulse or level transistor on the same time pulse. Load capacitance for 0.1 μ sec. rise time: 420 uuf. Delay = 30 mμsec.

4) Power required: 12 ma. at -3 v.
5.5 ma. at -10v.
0.24 ma. at +10 v.

5) Marginal Checking: Vary +10 volt positive bias on bases.

6) Plug-in units used: L,C

INVERTING CASCODE.



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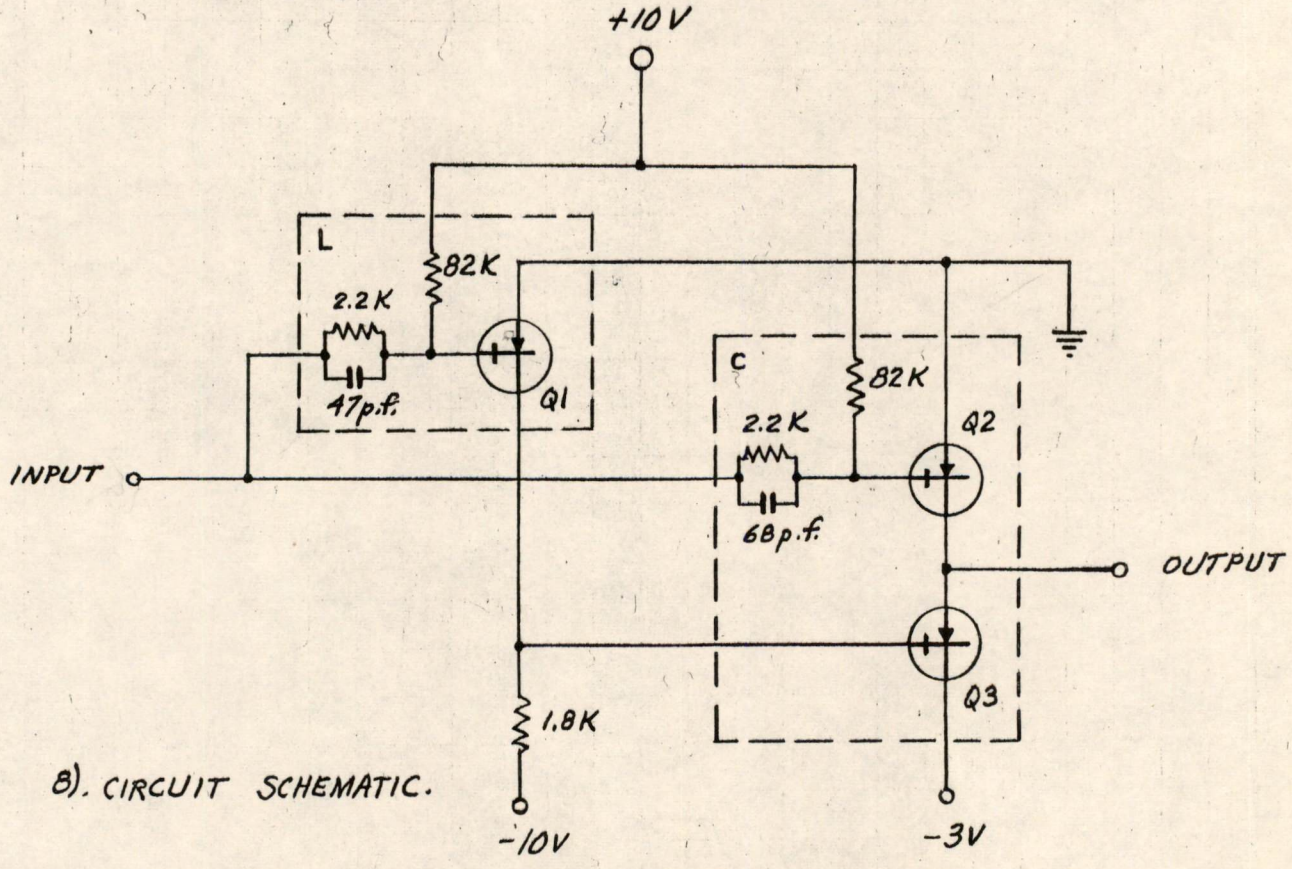


8). CIRCUIT SCHEMATIC.

Cable Driver (Inverting Cascode)

1) Use: To provide level input into 160 ohm cable, which drives transistor base.

2) Input: Voltage level at ground or -3 volts, from emitter follower gate or inverter gate. Input current required: 2.2 ma.

3) Output: Opposite polarity from input. Voltage level at ground or negative level less than -3 volts determined by voltage drop through 130 ohm resistor in series with cable. Maximum output current: 12 ma. Will drive maximum of 100 feet of K109 coaxial cable (Z_o = 160 ohms; D.C. resistance = 0.7 ohms/ft.)

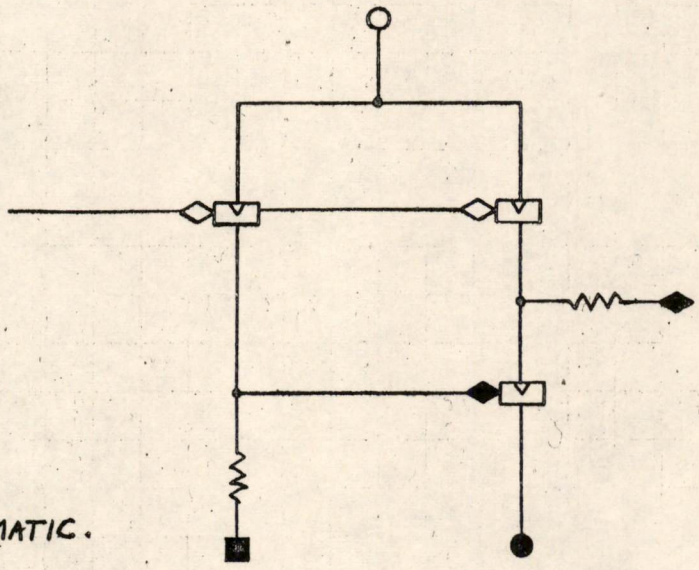
4) Restrictions: No termination should be added at end of cable, as cable is terminated in a resistance of 130 ohms in series with the input end at the cable driver.

5) Power required: 12 ma at -3 volts.
5.5 ma. at -10 volts.
0.24 ma. at +10 v.

6) Marginal checking: Vary +10 volt positive bias on bases.

7) Plug-in units used: L, C.

CABLE DRIVER.



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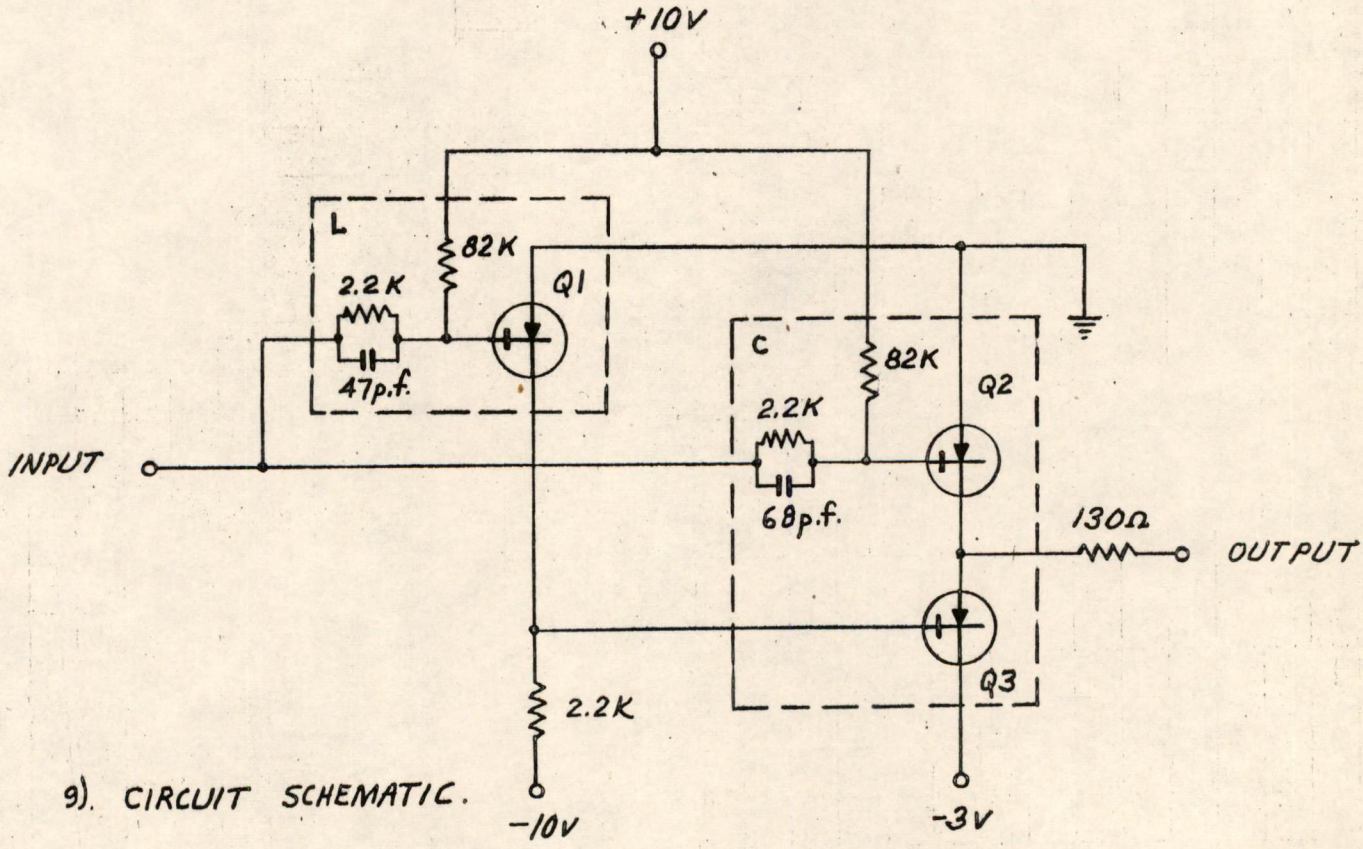


9). CIRCUIT SCHEMATIC.

Flip-Flop

1) Use: To provide logical levels at ground or -3 volts.

2) Input: Positive pulse up to ground from output of pulse gate.

3) Output: One side at ground: other side at -3 volts. Output circuit is inverting cascode. (See Inverting Cascode for specifications) Logical delay before start of rise or fall: 90 to 100 mμsec.

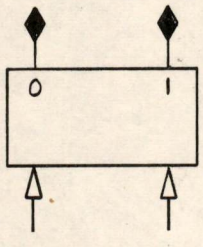
4) Restrictions: Maximum complement rate: 5 mcps.

5) Power required: 18 ma. at -3 volts (maximum)
12 ma. at -10 volts
1.8 ma. at +10 volts.

6) Marginal checking: Vary +10 volt positive bias on inverter bases by varying +10 volt input to "MCA" or "MCB".

7) Plug-in unit used: Flip-flop plug-in unit.

8) Logical symbol



9) Circuit drawing. See Figure 13.

Note on Resistance Values

Inverters

All load resistance to -10 volts are 1.8K, with the following exceptions:

2.2K for inverter in Cable driver cascode, for inverter when followed by two other inverters, and for Accumulator carry chain.

1.5 K for inverters in register drivers.

Normal positive bias resistance for RC input of 2.2 K and 47 uuf is: 82 K. 39 K is used for level input to MBR from memory frame, toggle switch storage, and PETR, and when the level transistor (L unit) in the Program Counter is driven from emitter followers.

Emitter Followers

All load resistance to +10 volts are 3.9 K with the following exception:

2 K is used when two emitter followers are used in parallel to drive another emitter of a pulse or level transistor. In this case 47 ohm resistors are used in the emitters of the emitter followers as current sharing resistances.

Distribution List

Group 63 Staff

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Phil Bagley

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TX-0 Circuitry

To: K. H. Olsen

From: J. R. Fadiman

Date: October 22, 1956

Approved: K. H. Olsen
K. H. Olsen

Abstract: The high speed logical circuitry used in the TX-0 transistor computer uses Philco 5122 Surface Barrier transistors. AND and OR gates are formed from inverter or emitter follower combinations. The cascode configuration is used as a power amplifier for fast rise and fall times. Timing pulses are generated by vacuum tubes, and gated on and off by a register driver circuit. Marginal checking is accomplished by varying a positive base bias voltage. The TX-0 flip-flop is a high-speed flip-flop package using 10 SBTs and capable of 5 mcps operation.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

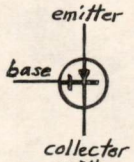
I. Introduction

A. The high speed circuitry for the TX-0 computer uses the Philco 5122 Surface Barrier transistor. The two logical levels are ground and -3 volts. Pulses are negative, with an amplitude of -3 volts and a width of from 80 to 100 mu sec. The supply voltages used for the SBT circuitry are -3, -10 and +10 volts.

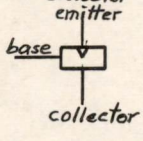
B. Symbols (Note)

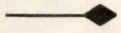
The following symbols are used.

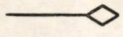
Transistor (in circuit schematics)

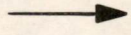


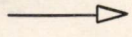
Transistor (in block schematics)



-3 volt level 

Ground level 

Negative pulse (ground to -3 volts) 

Positive pulse (-3 volts to ground) 

-3 volt supply ●

ground ○

-10 volt supply ■

+10 volt supply □

Note 1: For detailed considerations of transistor logic and symbology, refer to: 6M-4571, by R. C. Jeffrey.

The logical circuitry for the central machine is constructed out of small plug-in units, each containing one, two, or three transistors and associated components. The types of units and their functions are listed below. The schematic circuit diagrams are in figure 1 and detailed descriptions are in the appendix.

Unit	Transistor	Use
P	1 SBT	Pulse input gate to flip-flop
L	1 SBT	Level input gate and inverter
M	1 SBT	Level input gate with high positive bias
R	1 SBT	Register driver inverter
S	1 SBT	Steering gate
T	1 SBT	Single transistor for single emitter-follower
E	2 SBT	Two emitter followers with separate outputs
A	3 SBT	Three emitter followers with a common output
C	2 SBT	Cascode Circuit
F	1 GE4JD1A17	Ferranti Circuit
F (Mod II)	1 GE4JD1A17	Ferranti Circuit
B	None	Emitter bias for register driver
G	1 GE4JD1A17	Indicator light circuit

II Logic

A. "AND" and "OR" Gates

The "AND" and "OR" gates for TX-0 are either emitter followers in parallel or inverters in series or parallel. The AND gate for ground level in, ground level out is emitter followers in parallel as shown in Fig. 2. Because of the restrictions of speed for 5 mcps circuits, a maximum of 10 emitter followers may be placed in parallel in this fashion, providing up to a 10-way AND gate. An inverting AND gate for ground level in, -3 level out is shown in Fig. 3. Because of limitations of speed, only two inverters may be placed in parallel. The capacitance to ground goes up as βC_c where C_c is the collector capacitance of an off transistor and β is the current gain of the transistor, grounded emitter. The inverting OR gate for ground level in, -3 level out is shown in Fig. 4. Because there is a finite voltage drop across a saturated transistor, (about 0.1 volt), only two inverters may be placed in series in this manner.

B. Inverter Circuit

For the inverter circuit (Fig. 5) the values of the input resistance and positive bias resistance are so calculated that there is safety margin when the transistor is saturated and when it is cut-off. This insures maximum noise rejection and tolerance to signal variation. It is assumed on the basis of several tests that no transistor will have a β of less than 5 at 5.5 ma. collector current. (Our minimum acceptance β at low current is 15, and 11 at end of life). A larger amount of positive bias is used on inverter input gates to flip-flops when the input is from a distant frame, such as from core memory, toggle switch storage, or the photo-electric tape reader. In these cases the induced noise voltages are apt to be larger than usual, and the input impedance to the flip-flop is sufficiently high to allow the use of the larger positive bias current, and consequently smaller input base current.

This bias is also used in cases where the ground level for the emitter is supplied from an emitter follower gate. Such a level goes

0.3 volt positive and thus it is necessary for the base to be held at about +0.5 volts to provide adequate margins during cut-off.

All of the inverters in TX-0 use a supply voltage of -10 volts. However, the actual voltage at the collector never exceeds -4 volts, since it is clamped, either by an emitter follower following it, or by a voltage divider to ground. A single inverter provides current sufficient for driving three emitter followers or two inverters. It can drive a capacitance of 75 uuf, with a fall time of 0.1 μ sec.

C. Emitter Follower Circuit

The logical circuitry utilizes a combination of inverters and emitter followers which in general are alternated. This ensures that when an emitter follower is turned on, it is always kept in saturation since its base is returned effectively to -10 volts through the load resistor of the previous inverter. The difference in driving capabilities of the saturated and non-saturated emitter follower is shown in the graph of Fig. 6. The load resistance of the emitter follower is returned to +10 volts instead of to ground to shorten the rise time of the emitter follower. This emitter follower will provide 8 ma. of output current at -3 volts and will drive a capacitive load of 120 uuf, with a rise time of 0.1 μ sec.

D. Cascode Circuit

In order to achieve faster rise and fall times and greater driving ability than is possible with either the emitter follower or the inverter, the "cascode" circuit is used. The logical and circuit schematics are shown in Fig. 7. The inputs to Q_2 and Q_3 are always opposite in phase so that in the steady state case only one transistor is conducting. Q_3 acts as an emitter follower which provides the driving current and pulls the input quickly down to -3 volts. Q_2 acts as an inverter whose function is to pull the output quickly up to ground during the transition. Thus, the circuit utilizes the fast rise time of the inverter and the fast fall time of the emitter follower.

This configuration is capable of driving a capacitive load of 420 uuf. with a transition time of 0.1 μ sec. No power is wasted in load resistances, and this circuit is designed to provide 12 ma. output current at -3 volts. It will drive 12 emitter followers or 8 inverter bases, and one emitter of an inverter. TX-0 uses the cascode as the output stage of all flip-flops, as a power amplifier for driving many transistor bases, and as a cable driver.

Cascode cable drivers are used when sending levels to the memory over 160 ohm coaxial cable. The cable is terminated at the input end by a resistance in series with the cable. This series termination is possible because, unlike the emitter follower or inverter, the cascode circuit looks like a very low impedance (less than 10 ohms) when driving in either direction. Thus, the driven end of the cable is properly terminated at all times.

III Pulse Circuitry

A. Timing Pulses

The timing pulses for the computer are generated by vacuum tubes. Thirty volt positive pulses are sent to the computer through 93 ohm coaxial cables. 7:1 pulse transformers with a one turn secondary are used at the computer to provide approximately 3.4 volt negative pulses. A 1N283 diode is used across the primary in order to damp the overshoot.

B. Register Driver

Gated register drivers (Figures 8 and 9) supply the 3 volt negative pulses to the input gates of the flip-flops. The pulse input is at the collector of Q_3 and the output is from the emitter. A pulse is passed when Q_3 is saturated from the negative output of inverters Q_1 and Q_2. Thus, a ground input to either Q_1 or Q_2 is necessary to pass a pulse through the register driver. The two inverters in series thus give a two-way OR circuit for the pulses. Up to a 10 way OR circuit can be constructed by paralleling register drivers with a common pulse input and output but different gating. In order to form an AND circuit for pulses, emitter follower gates are

placed in parallel to feed the inputs of the inverters. All the inputs must be at ground to pass a pulse. The pulse output of the register driver closely follows the pulse input. The maximum pulse current is 30 ma., sufficient for driving 10 pulses bases, and the pulse voltage drop through the register driver is less than 0.5 volt.

C. Pulse Inputs to Flip-Flops

In order to set or clear the TX-0 flip-flop the "one" or "zero" input must be brought up to ground by the output of a pulse inverter. Up to 15 such inputs may be tied in parallel to one side of the flip-flop. The negative pulse is inverted and gated by a circuit such as this: Fig. 10. Or, alternately, only one transistor may be used as a gate in this manner: Fig. 11. Here a ground level must be supplied to the emitter in order to pass the pulse. This arrangement requires a level current equal to $\frac{I_c}{\alpha}$ while the two transistor gate requires a level current equal only to $\frac{I_c}{\beta} = \frac{I_c}{\alpha}(1-\alpha)$. In order to complement the flip-flop, the pulse must be steered to the proper side of the flip-flop. The circuit which does this is shown symbolically in Fig. 12.

IV Marginal Checking

Marginal checking of all TX-0 circuitry is accomplished by varying the +10 voltage on the base of the inverter transistors. Increasing this positive bias supply effectively reduces the negative base current into the transistor and tends to bring it out of saturation. Making the positive bias supply negative tends to allow the transistor to conduct when it should be held cut off. Emitter followers are not directly marginal checked, but their condition can be investigated by marginal checking the inverters which proceed and follow it. For these inverters normal margins are slightly greater than $\pm$ 10 volts either side of the normal +10 volt supply.

V Flip-Flop

The TX-0 flip-flop is shown in Fig. 13. The circuitry is similar to that already described, with RC coupling between inverters, positive bias, and emitter follower clamping. Q_1 and Q_2 are pulse amplifiers

which are normally conducting and are cut off by the positive input pulse at the "zero" or "one" input. Q_3 and Q_4 are the flip-flop transistors themselves which are arranged in a conventional RC-coupled Eccles-Jordan trigger circuit. When an input pulse cuts off Q_1 or Q_2 this opens the emitter circuit of Q_3 or Q_4, and changes the state of the flip-flop. Q_5 and Q_6 are inverters which are used to saturate the emitter followers of the output cascode. Q_7 and Q_8, and Q_9 and Q_{10} form the cascode circuits on the "one" and "zero" sides respectively. Their operation is the same as that previously described for the cascode circuit, with the opposite phases being obtained from the inverters on opposite sides of the flip-flop.

The output wave form at 10 mcps is shown in Fig. 14, and various marginal checking curves and output characteristics of the flip-flop are shown in Figs. 15 through 22.

J. R. Fadiman

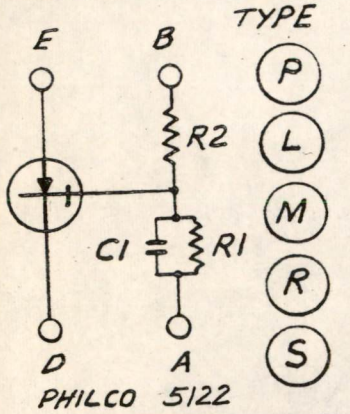
J. R. Fadiman

Attachments:

Fig. 1: SA-65640-3
Figs. 2 through 12
Fig. 13: D-63369
Fig. 14: A-65366
Fig. 15: A-67294
Fig. 16: B-65729
Fig. 17: B-65721
Fig. 18: B-65720
Fig. 19: B-65719
Fig. 20: B-65727
Fig. 21: B-65717
Fig. 22: B-65718
Appendix (15 pages)

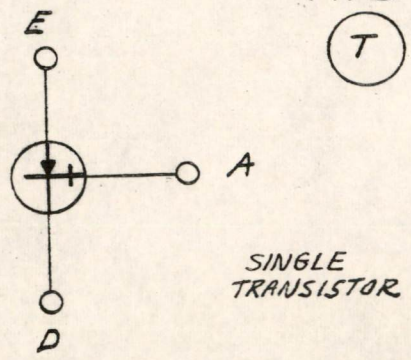
JRF:mmw

SA 65640-3



TYPE	R1	C1	R2	USE
P	2.7K	22pf	56K	PULSE INPUT GATE
L	2.2K	47pf	82K	LEVEL INPUT GT. & INV.
M	2.2K	47pf	39K	MBR LEVEL RD-IN FROM MEMORY
R	1.5K	68pf	15K	REGISTER DRIVER INV.
S	3.9K	47pf	180K	STEERING GATE

PHILCO 5122



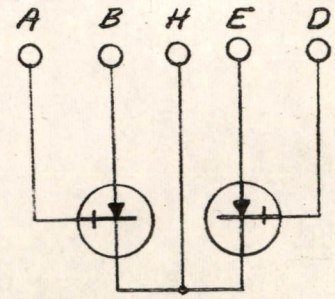
TYPE T

SINGLE TRANSISTOR

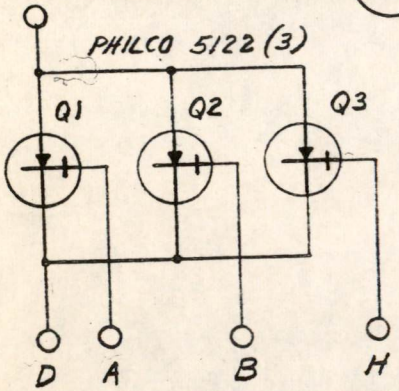
PHILCO 5122

TYPE E

TWO E.F.'S.

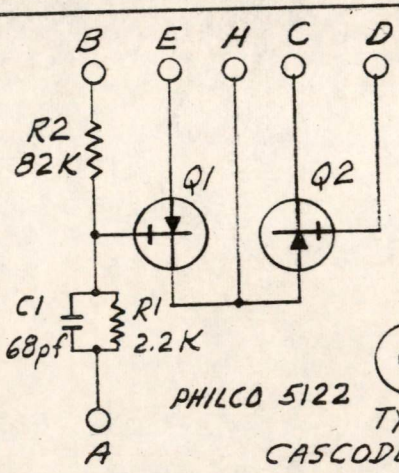


PHILCO 5122



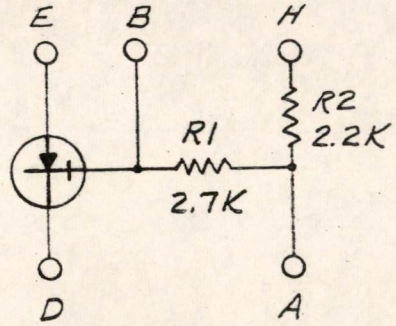
E THREE E.F.s TYPE (A)

PHILCO 5122 (3)



PHILCO 5122 (C)

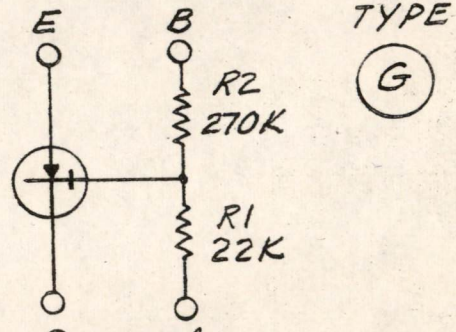
TYPE CASCODE



GE 4JD1A17

FERRANTI

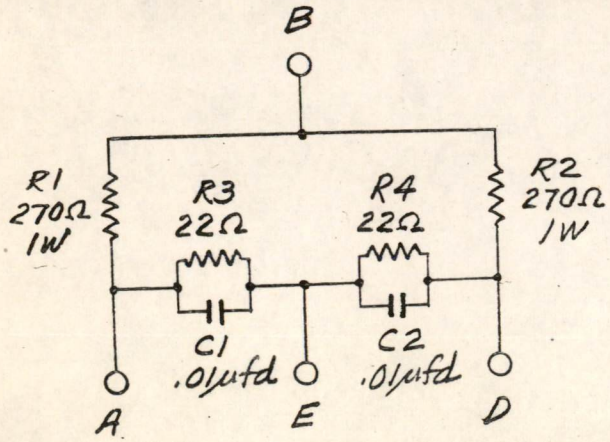
TYPE (F)



TYPE (G)

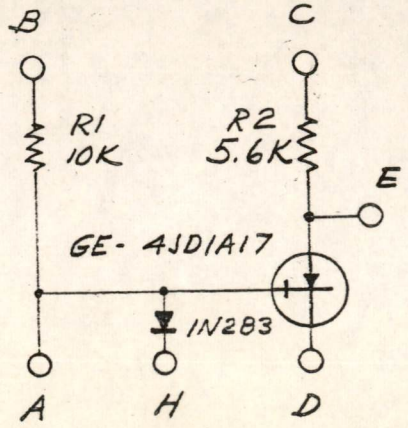
GE 4JD1A17

INDICATOR LIGHT CIRCUIT



TYPE (B)

BIAS



FERRANTI (MOD II) (F II)

"BOTTLED" PLUG-IN UNITS PIN CONNECTIONS.

3-19-56

SA 65640-3

AND

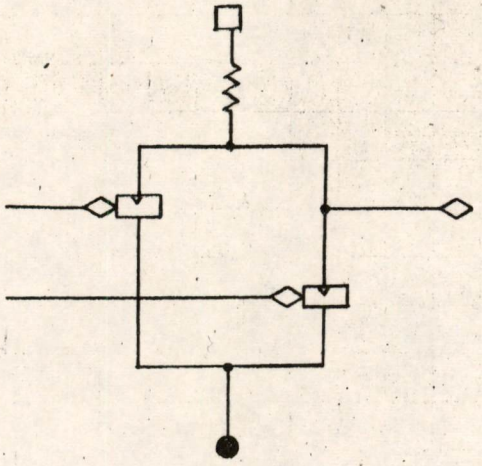


FIG. 2

AND

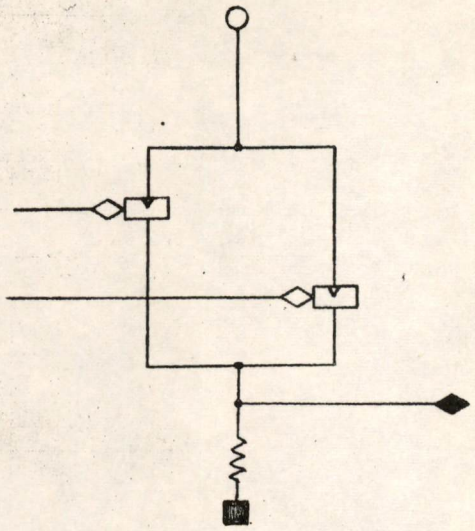


FIG. 3

OR

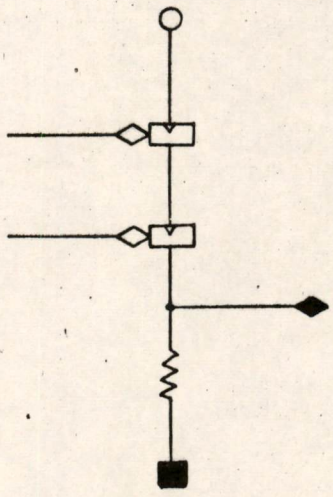


FIG. 4

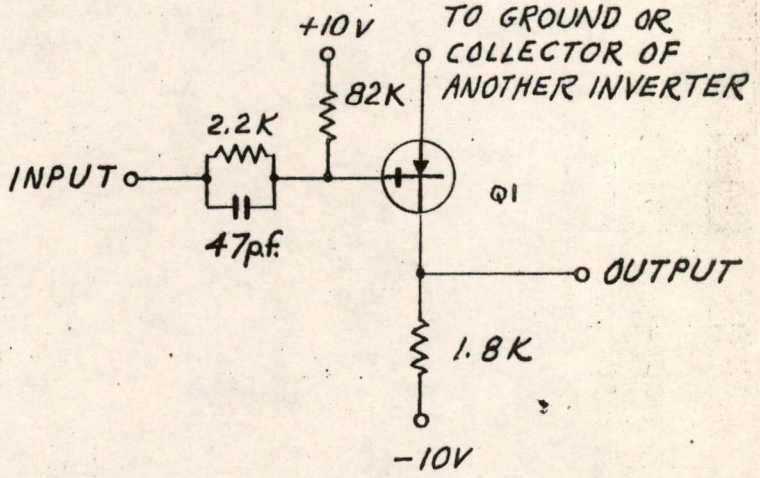


FIG. 5

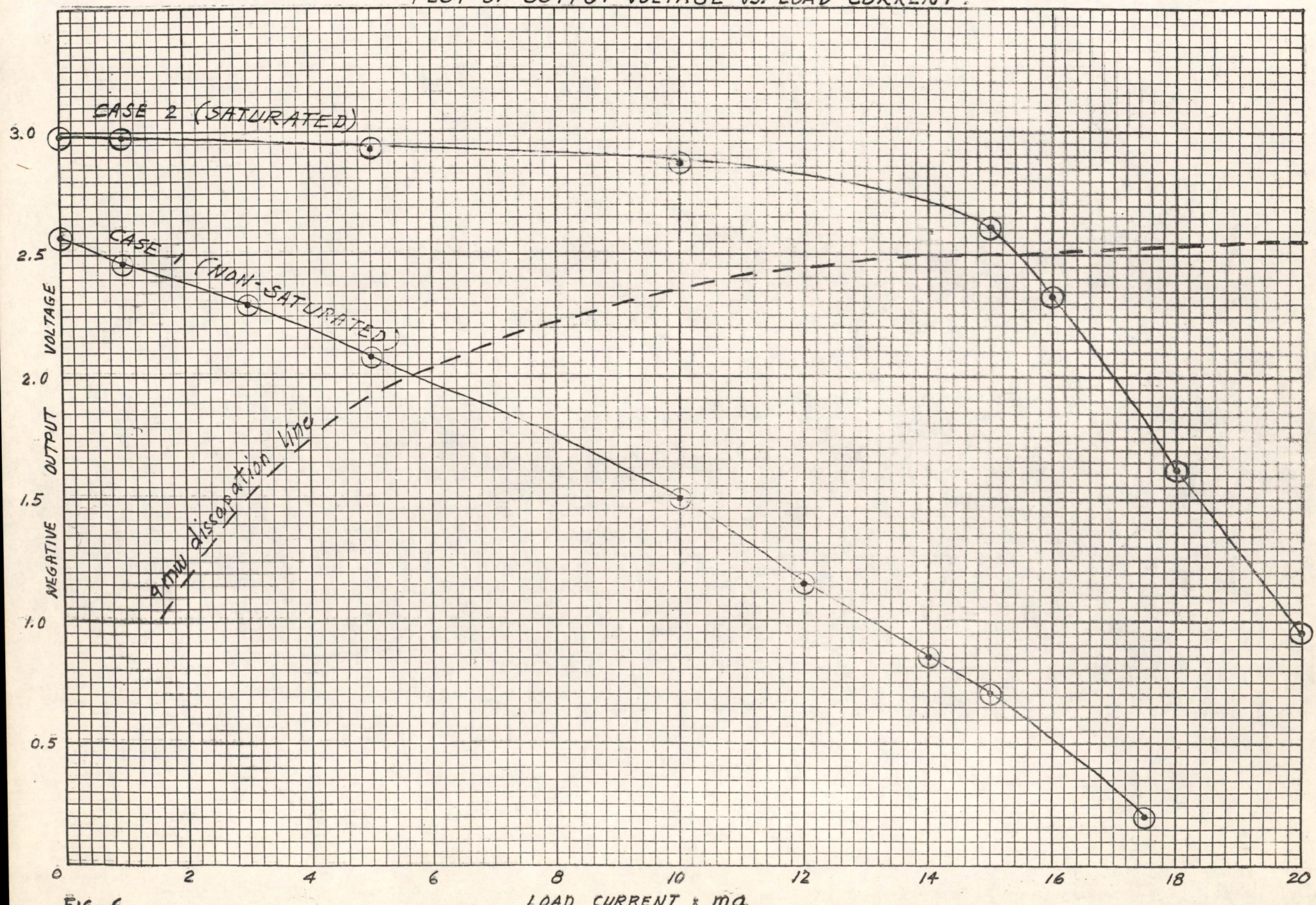
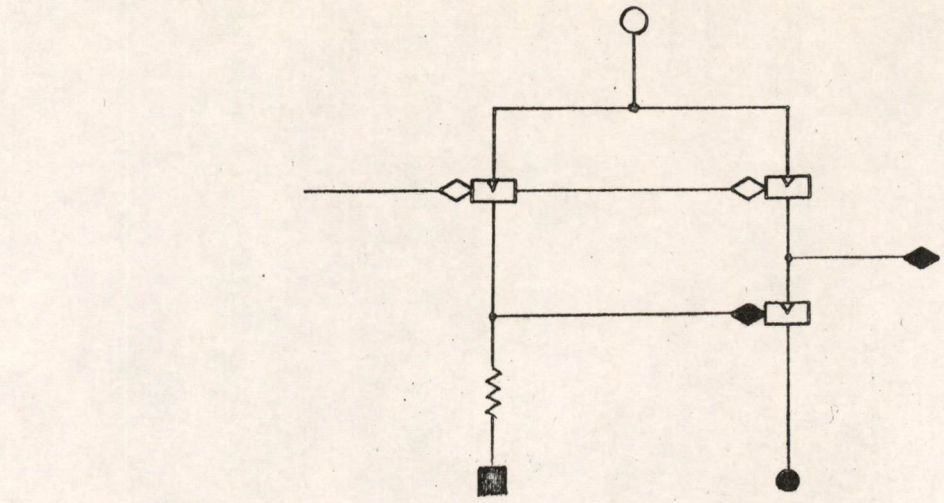
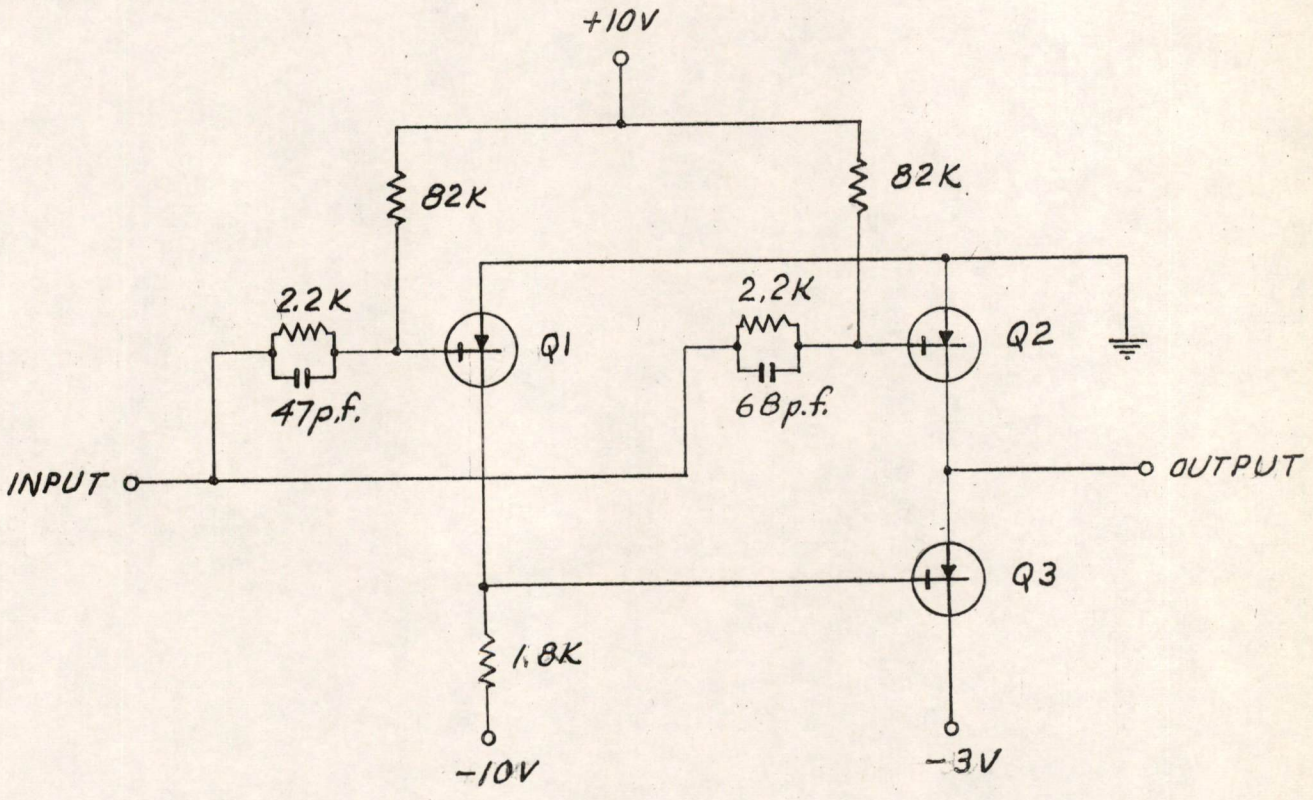


FIG. 6





Title?

FIGS. 7

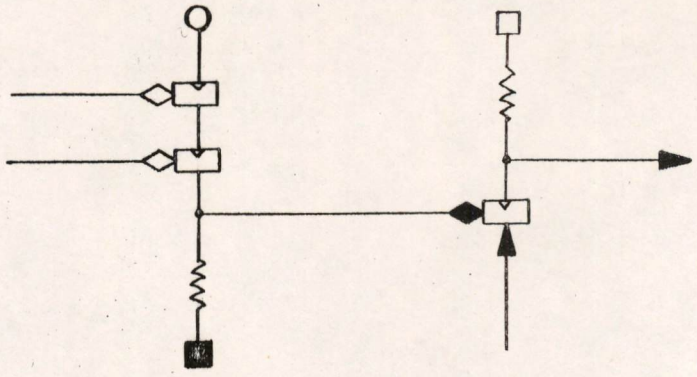


FIG. 8

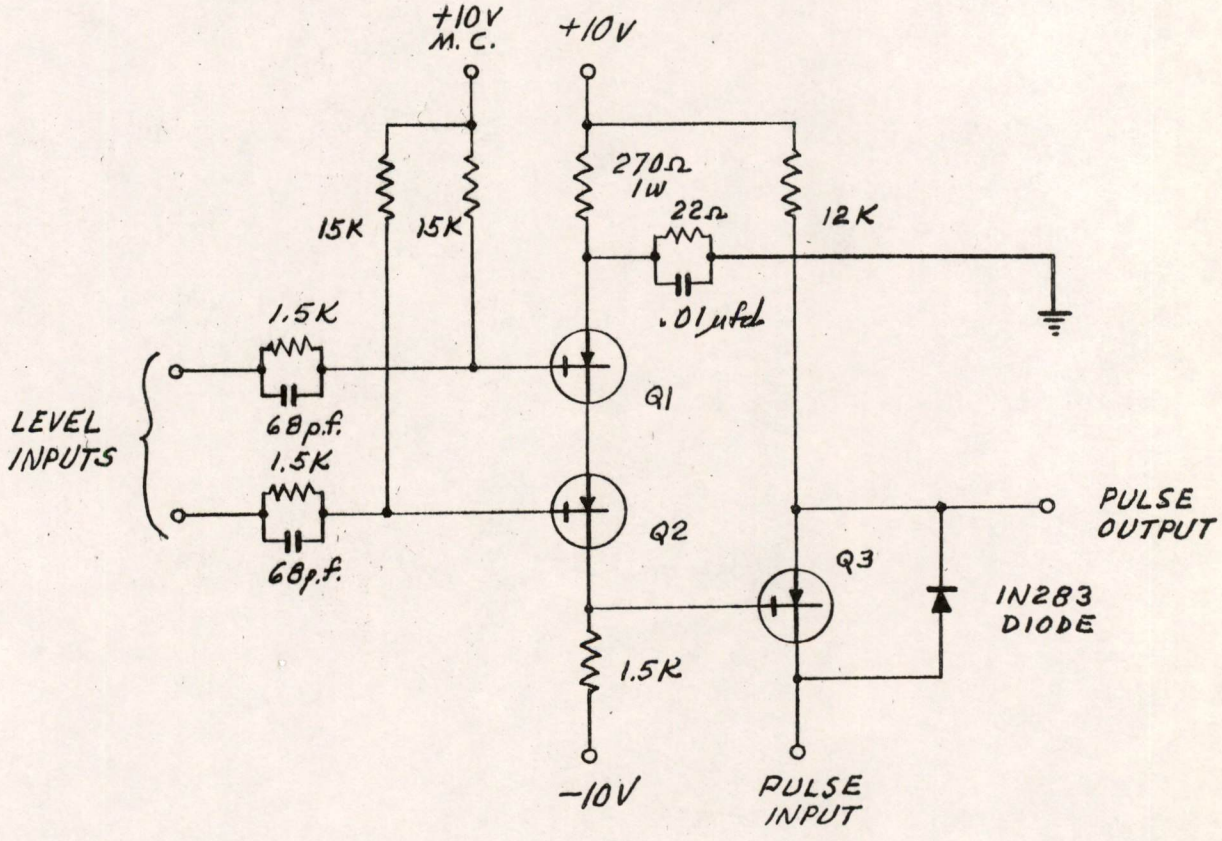

+10V
M.C.
+10V
270Ω
1W
22Ω
12K
15K
15K
.01 μfd.
1.5K
Q1
LEVEL
INPUTS
68p.f.
1.5K
Q2
68p.f.
Q3
PULSE
OUTPUT
IN283
DIODE
1.5K
-10V
PULSE
INPUT

FIG. 9

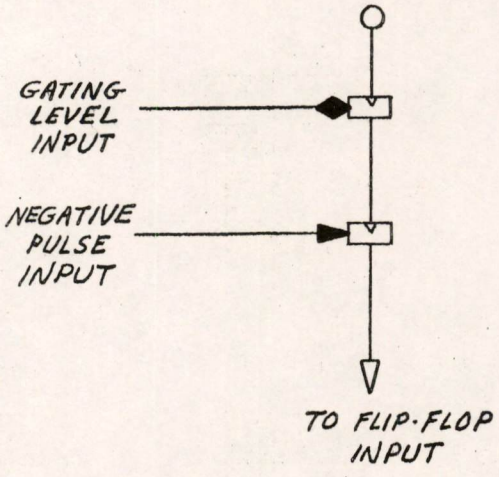


FIG. 10

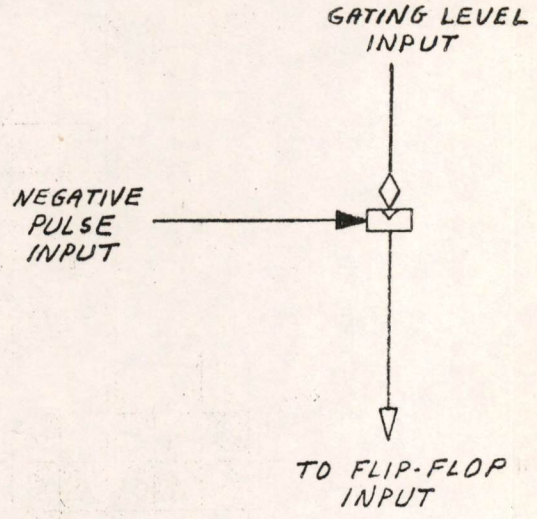


FIG. 11

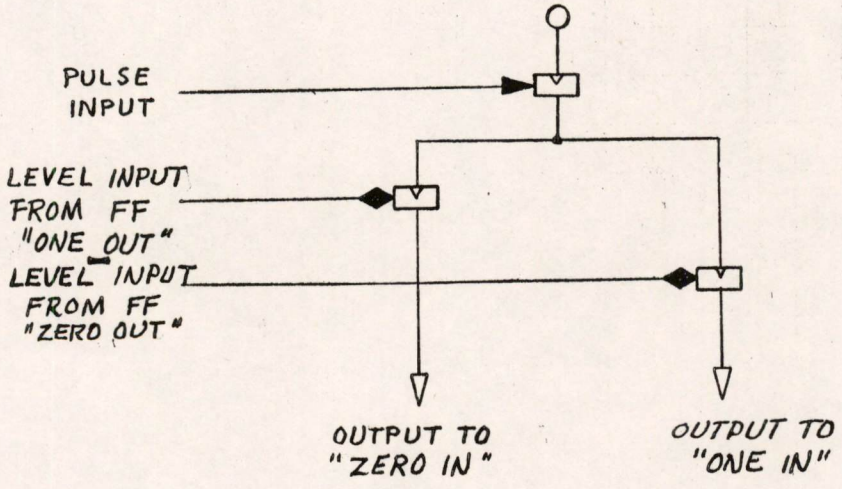


FIG. 12

D-63369
VG-71
F-3140
SN-1328
F-3181

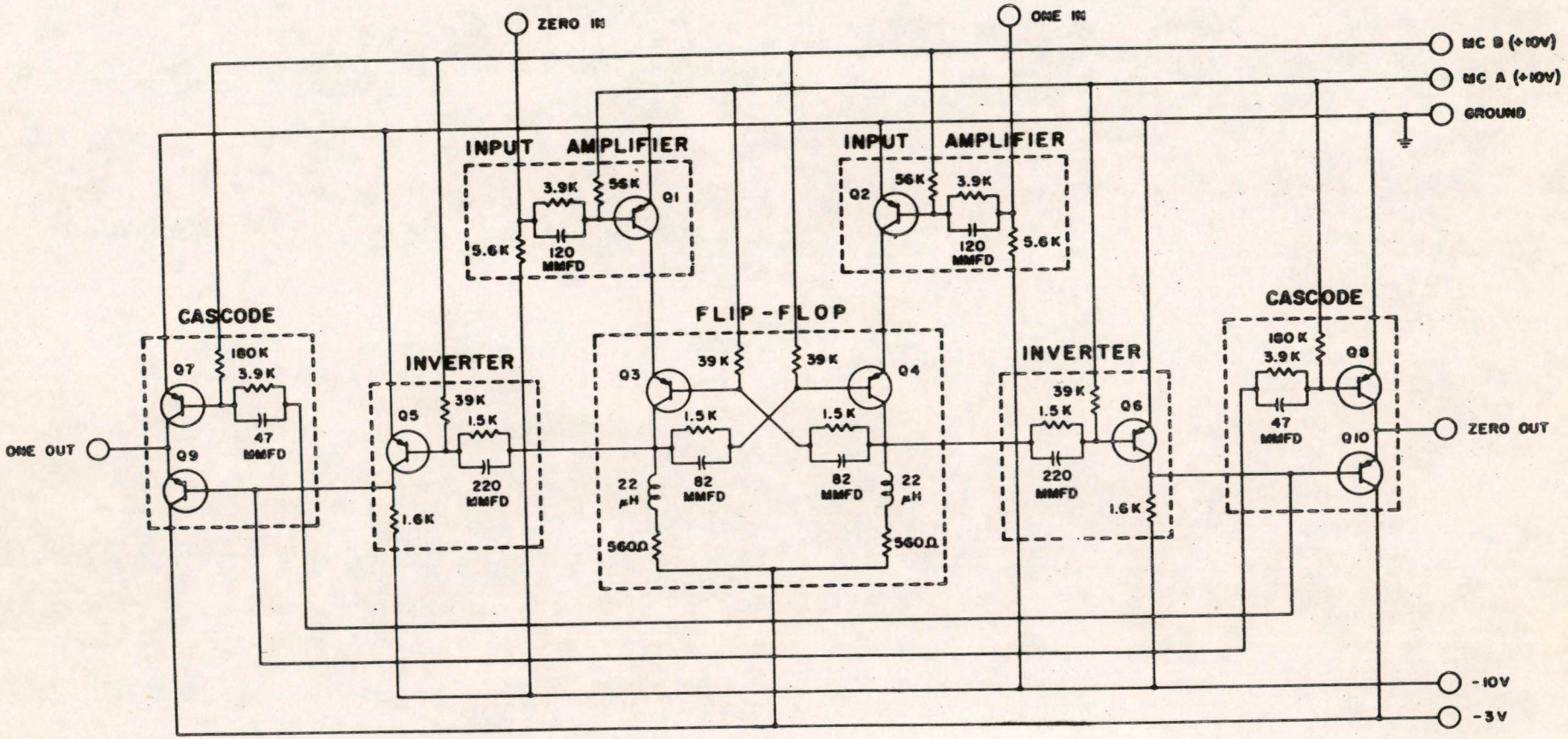
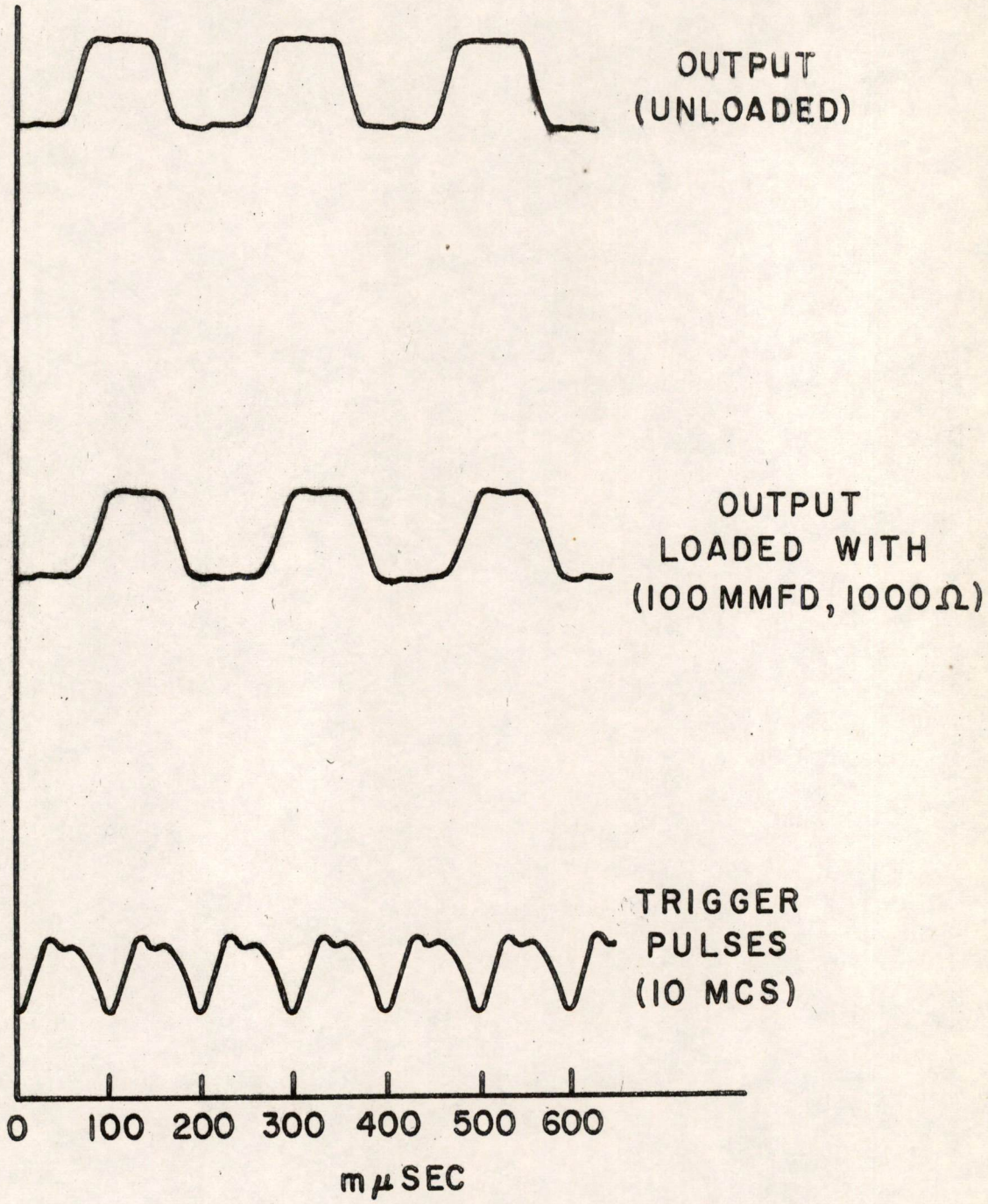


FIG. 13

TX-0 FLIP-FLOP



TX-0 FLIP-FLOP

A-65366
VG-82
SN-1327
F-3180

063-11

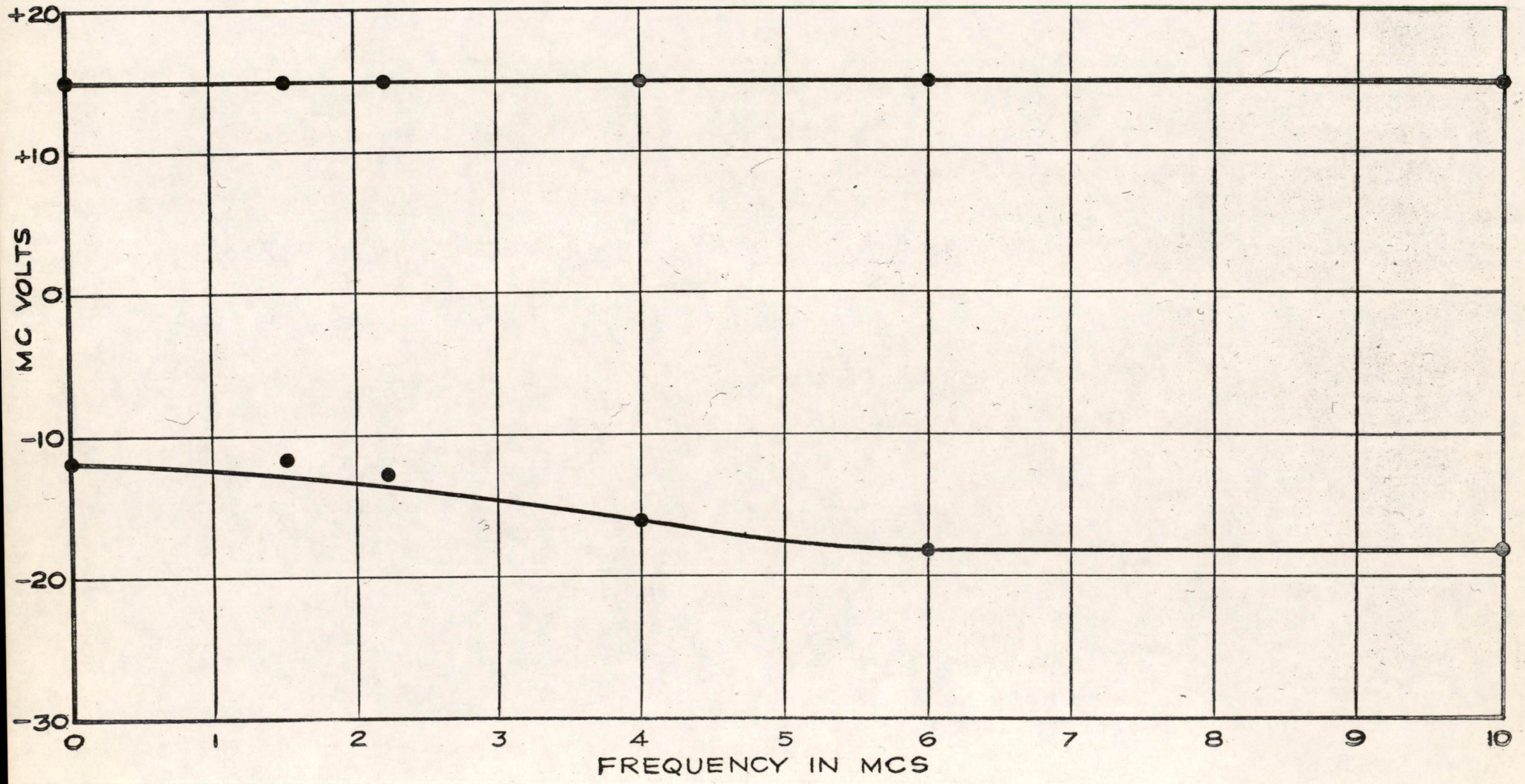
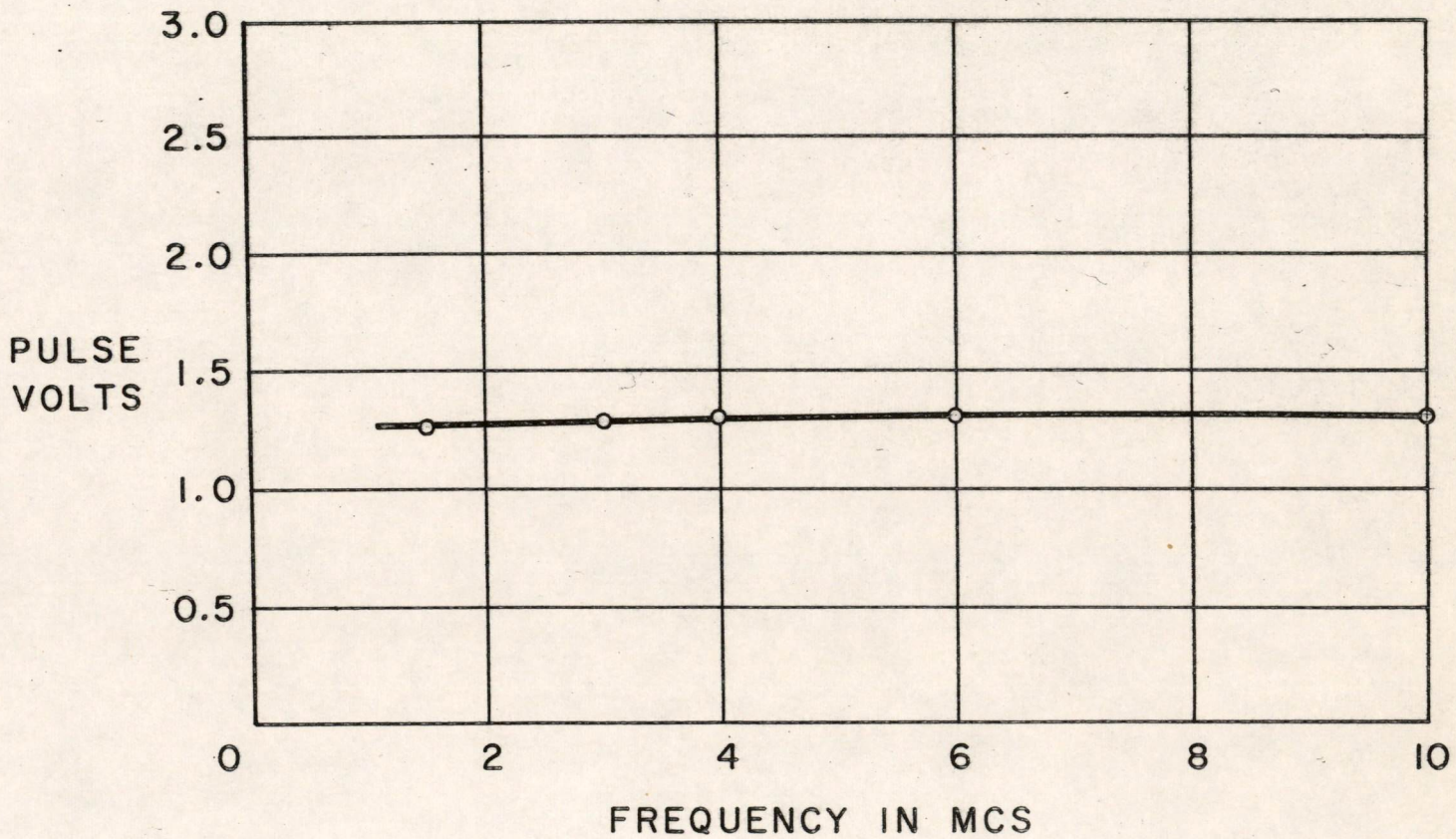


FIG. 15

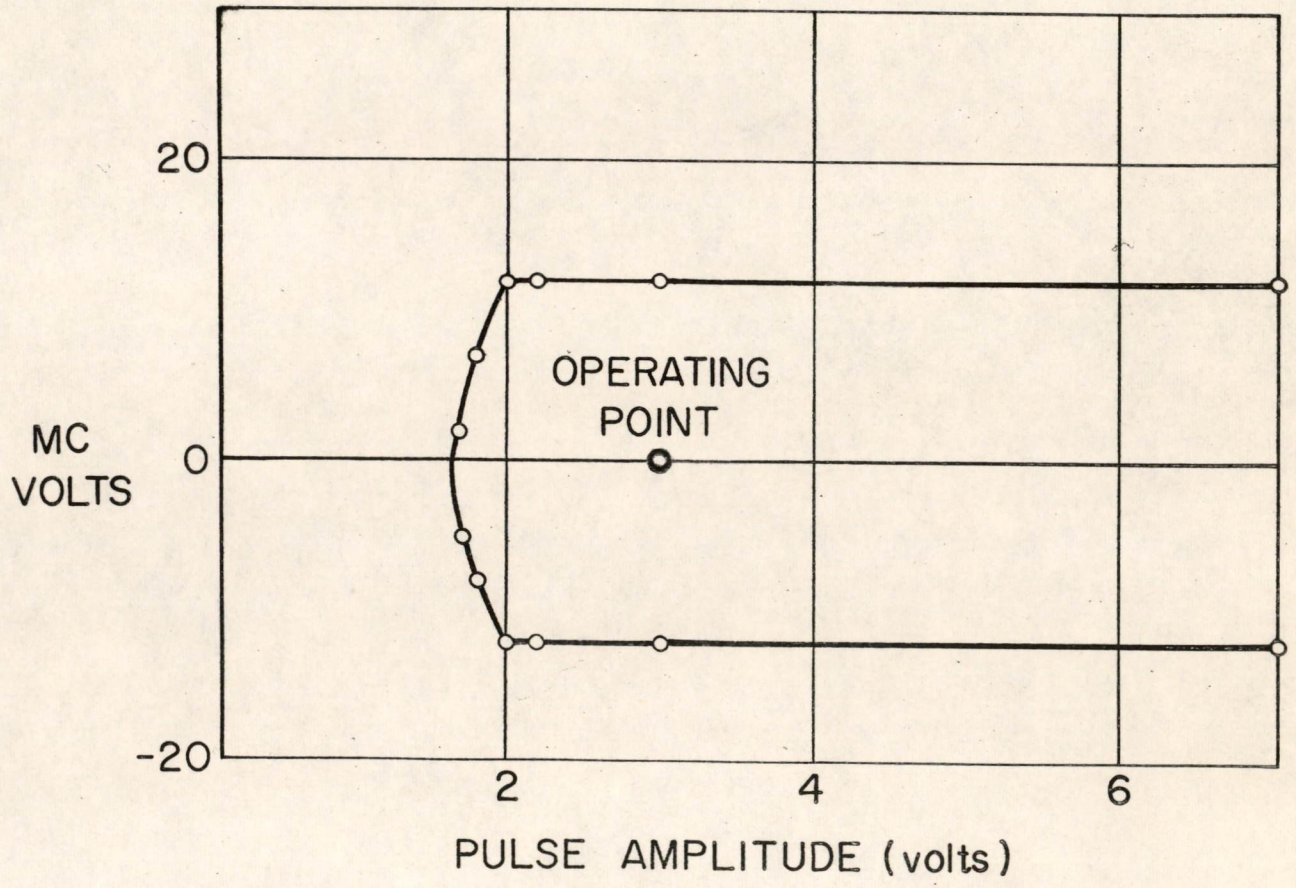
FREQUENCY MARGINS

B-65729
SN-1329
F-3184



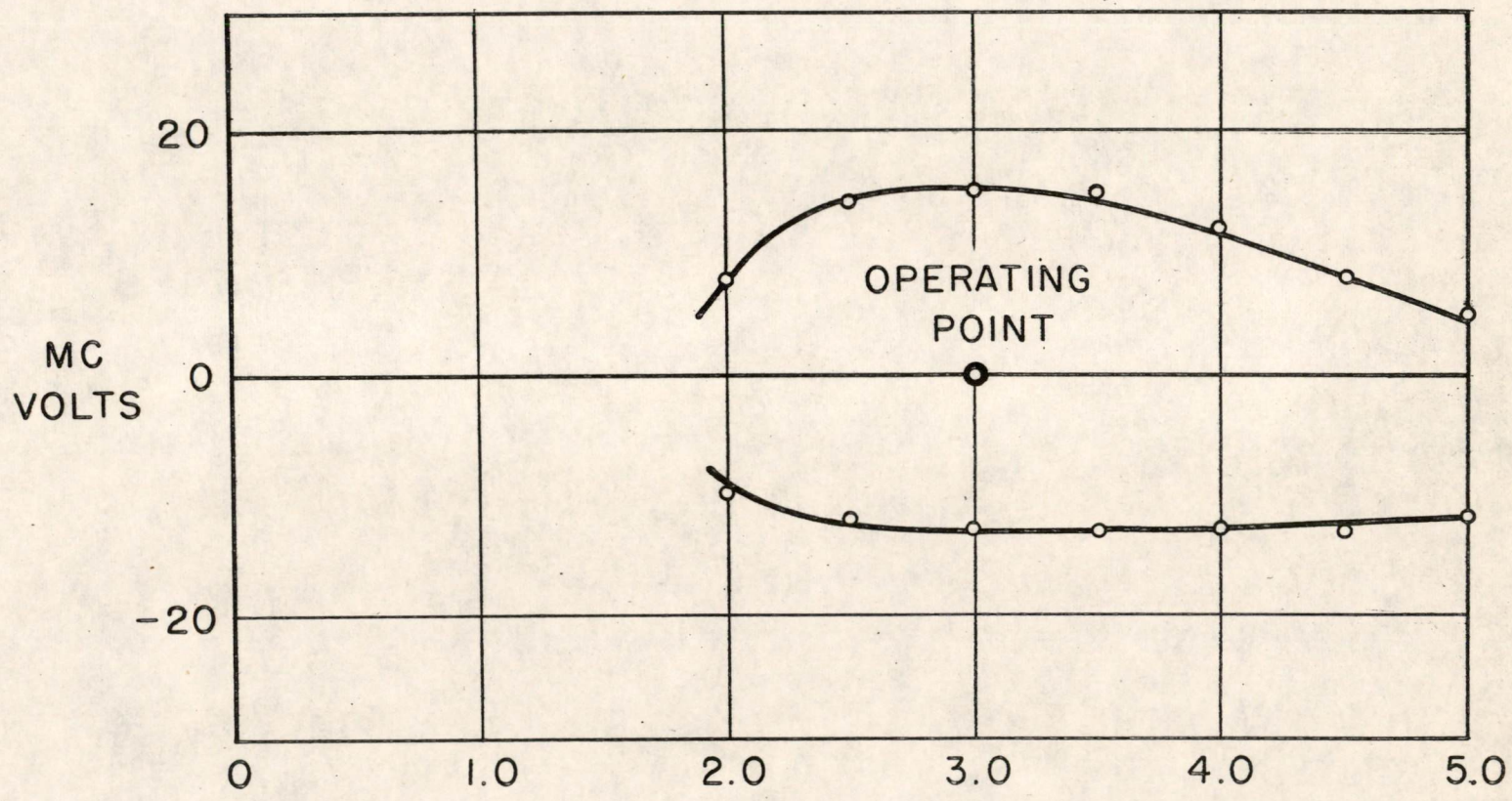
TRIGGER SENSITIVITY

B-65721
SN-1325
F-3178



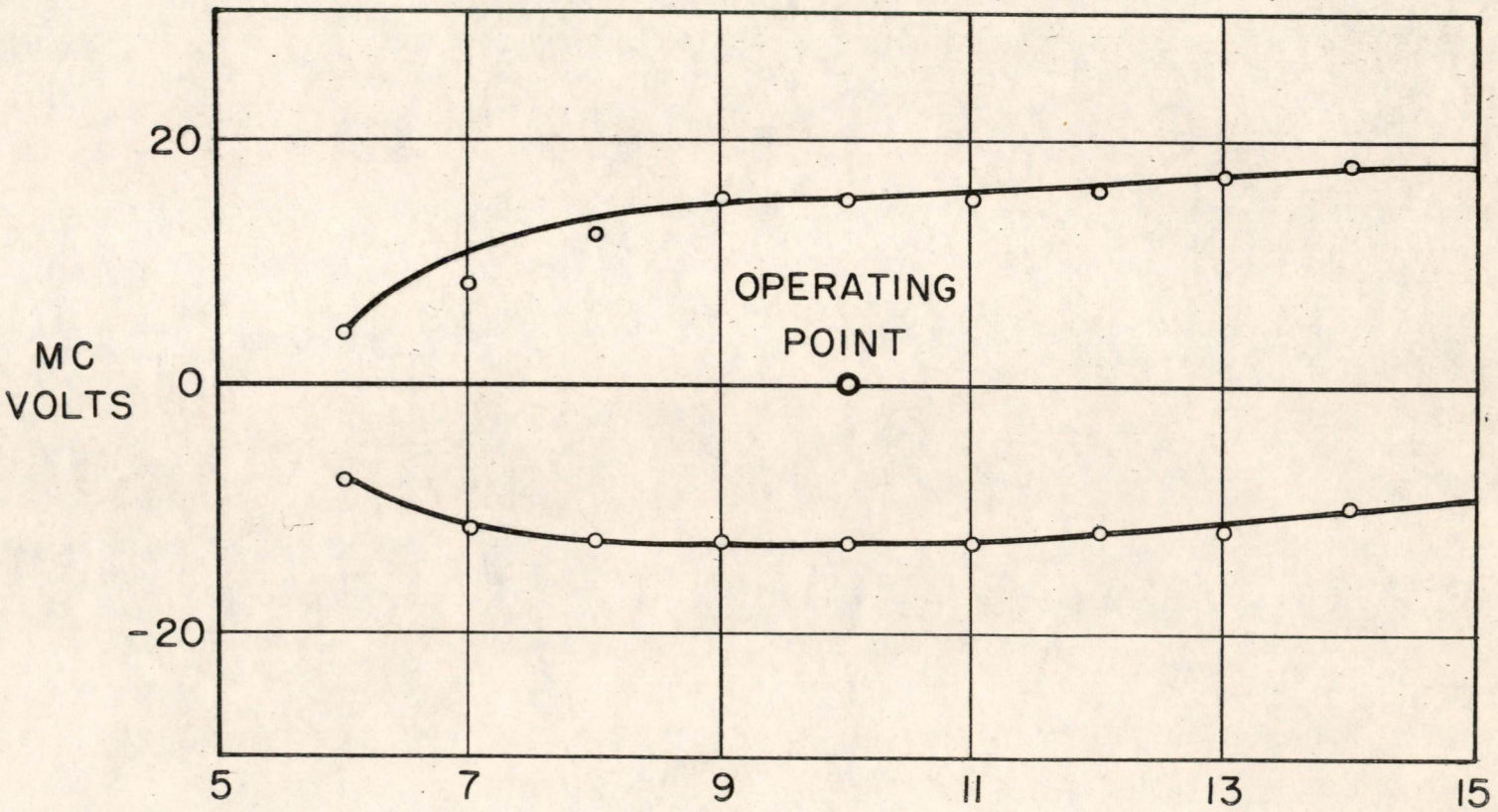
PULSE MARGINS

B-65720
SN-1324
F-3177



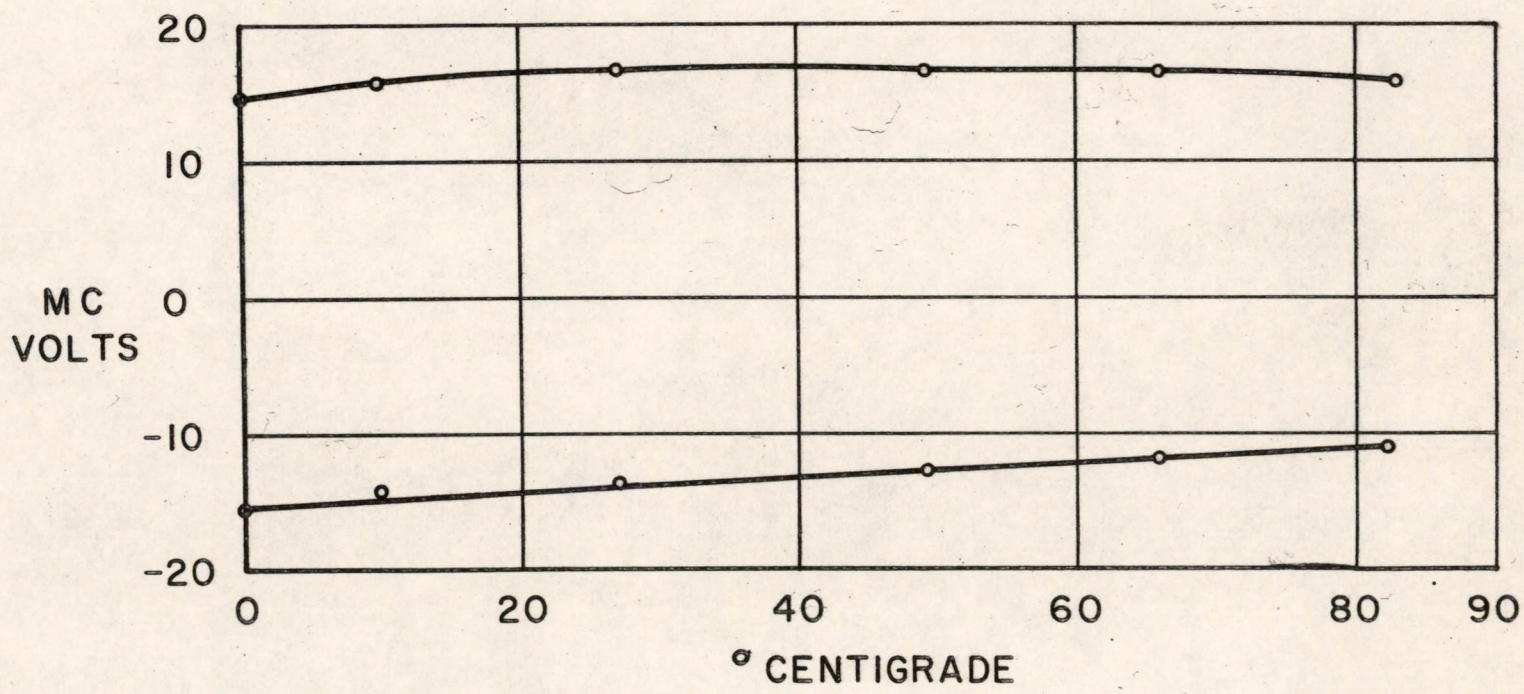
-3 VOLT SUPPLY MARGINS

B-65719
SN-1323
F-3176



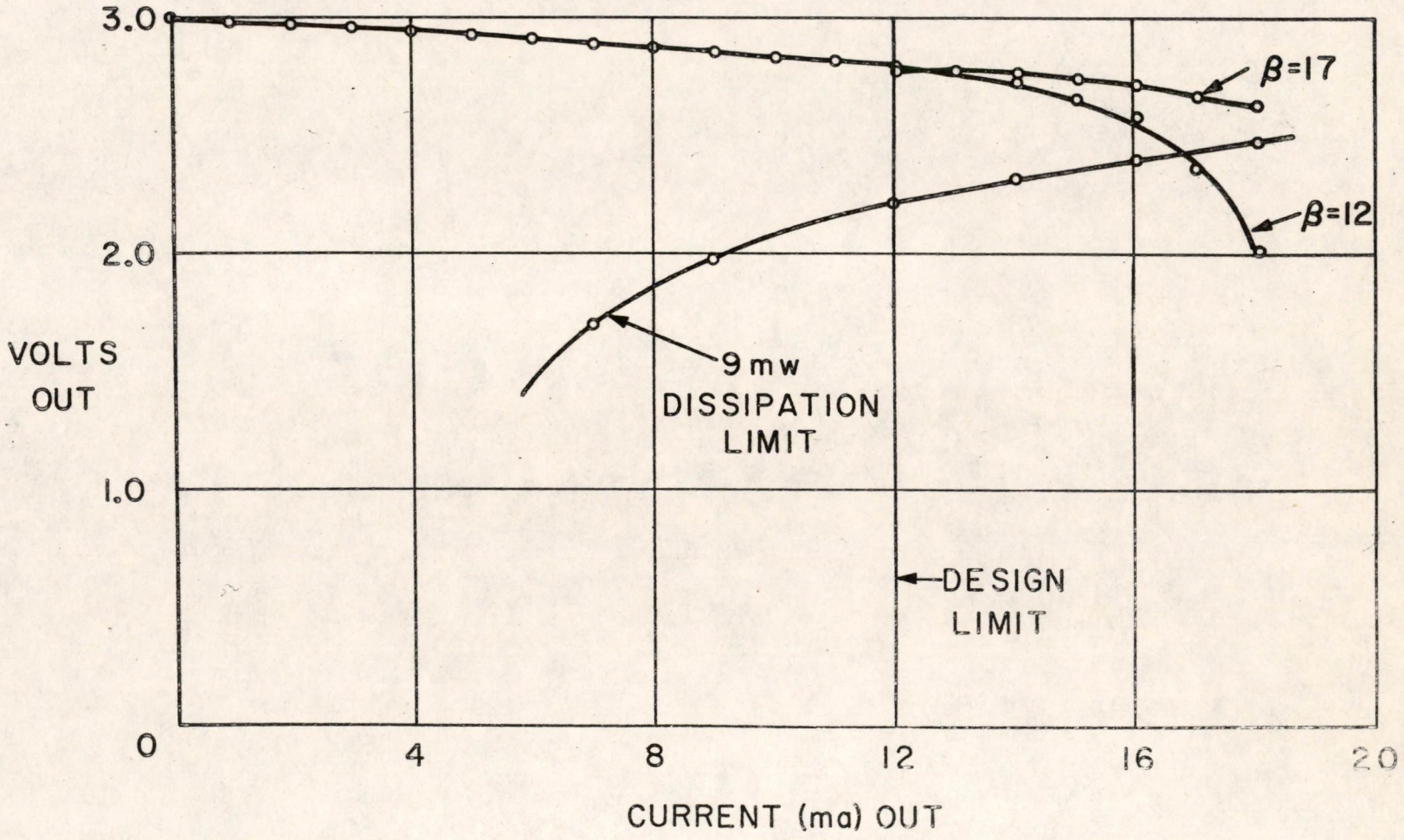
-10 VOLT SUPPLY MARGINS

B-65727
SN-1330
F-3185

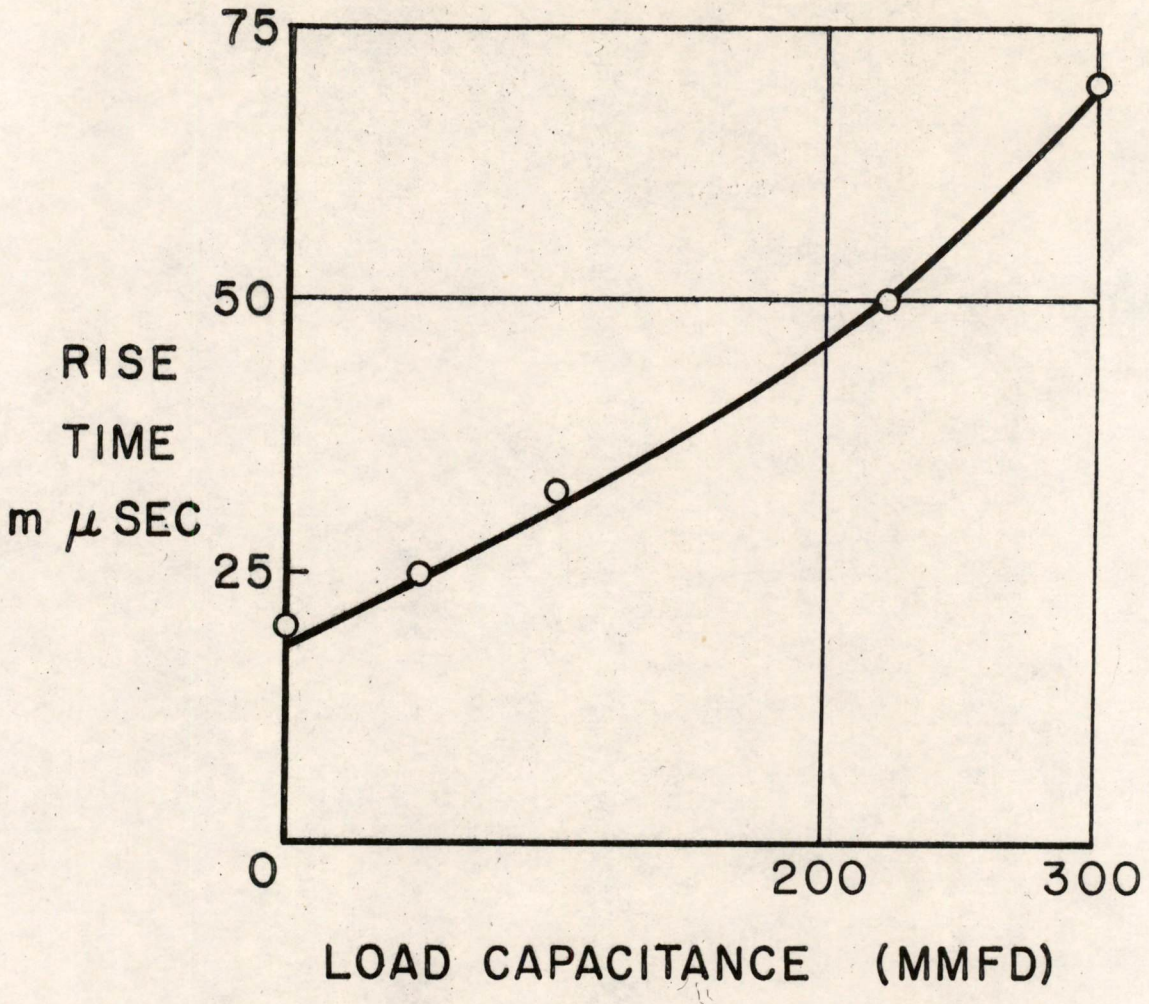


TEMPERATURE MARGINS

B-65717
SN-1321
F-3174



OUTPUT VOLTAGE



RISE TIME

A-65718-1
SN-1414
E-3275

APPENDIX

Data On Individual TX-0 Circuits

Inverter

1) Uses: Logical inverter and voltage amplifier. When placed in series, gives OR circuit for ground in, -3 out. When placed in parallel, gives AND circuit for ground in, -3 out.

2) Input: Voltage level at ground or -3 volts. Input current required: 1.1ma.

3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current at -3 volts: 3.5 ma. can drive maximum of 3 emitter followers or two inverters. Load capacitance for 0.1 μsec fall time: 75 uuf. Delay: 30mμsec.

4) Restrictions: When turned off, collector voltage must not exceed -4 volts. Maximum of two inverters in series. Maximum of 2 inverters in parallel for 5 mcps operation.

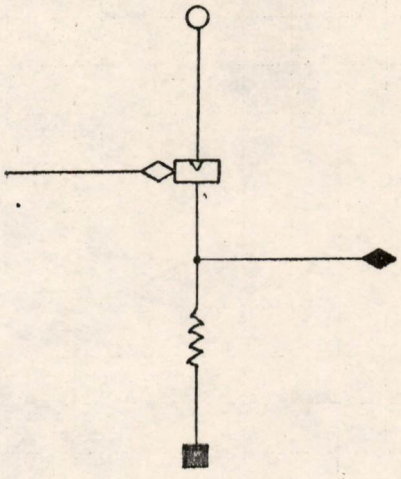
5) Power required: 5.5ma at -10v.

0.12 ma. at +10v.

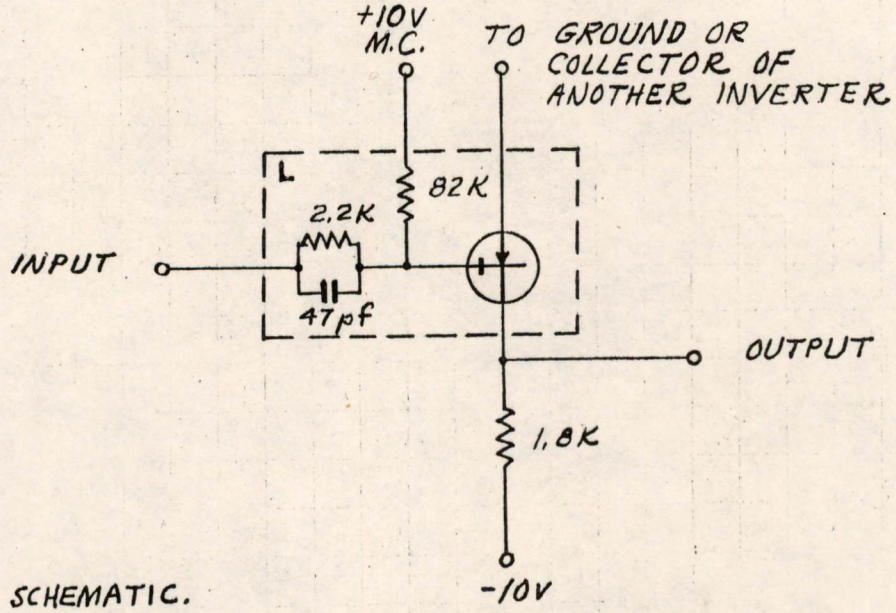
6) Marginal checking: Vary +10 volt positive bias on base.

7) Plug-in units used: L or M.

INVERTER.



8) BLOCK SCHEMATIC.



9) CIRCUIT SCHEMATIC.

EMITTER FOLLOWER

1) Uses: Current amplifier. When placed in parallel with common load resistance gives AND circuit for ground in, ground out.

2) Input: Voltage level at ground or -3 v. Input current required: Load current / 6 +3 ma. Input current will be from 0.5 to 1.8 ma.

3) Output: Same polarity as input. Voltage level at +0.3 v. or -2.9v. Maximum output current at -3 v.: 8 ma. Can drive maximum of 8 emitter followers or 2 inverters, providing output current does not exceed 8 ma. Two emitter followers in parallel (R=2K to +10 v.) can drive one emitter of pulse transistor with no delay or one emitter of level transistor with 90 mμsec. rise time. Maximum output current at ground in this latter type of operation: 5 ma. Load capacitance for 0.1 μsec rise time: 120 uuf.

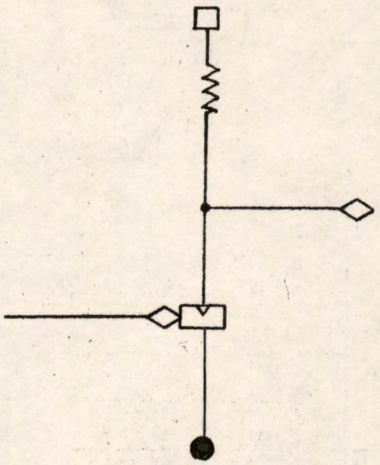
4) Restrictions: Not more than 10 emitter followers may be placed in parallel for 5 mcps operation. Emitter followers cannot be placed in series. Only 2 emitter followers may be cascaded provided that the first emitter follower is saturated from -10 volts. Otherwise, emitter followers may not be cascaded.

5) Power required: 8 ma. at -3 v. (maximum)
3.3 ma. at +10 v.

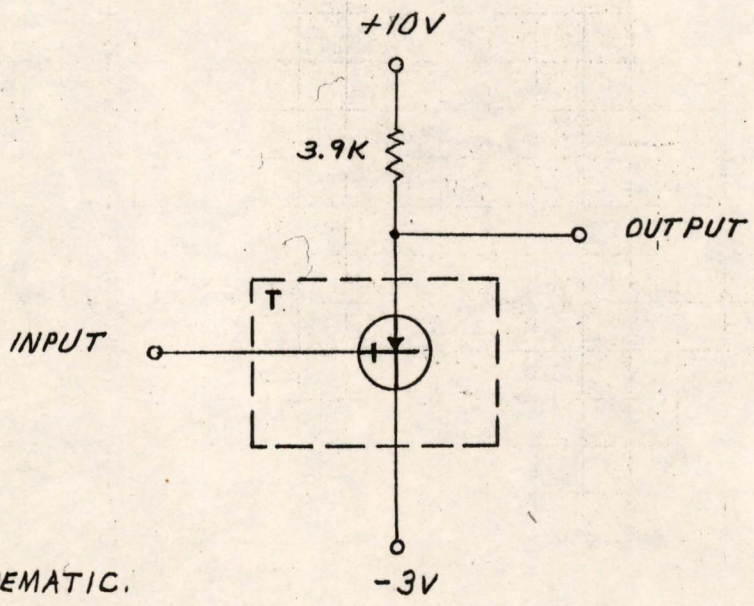
6) Marginal checking: None.

7) Plug-in units used: T or E or A.

EMITTER-FOLLOWER



8). BLOCK SCHEMATIC



9). CIRCUIT SCHEMATIC.

Register Driver

1) Use: Gating circuit for pulses for pulse inputs to flip-flops.

2) Level input: Ground level for passing pulse. -3 volt level for no pulse output. Level input current required: 2.2 ma.

3) Pulse input: -3.4 volt 80 to 100 musec pulse. Input pulse current equal to output pulse current.

4) Output: -3 volt 80 to 100 musec. pulse. Pulse amplitude equals input amplitude minus transistor drop. Drop less that 0.5 volt. Maximum pulse current: 30 ma. Can drive maximum of 10 pulse bases. Set-up delay: about 20 musec.

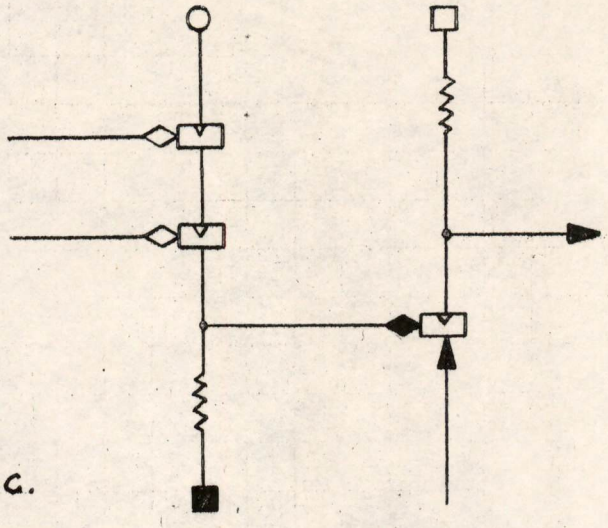
5) Restrictions: Two register drivers driven from the same input gate will drive maximum of 20 bases. Up to 10 register drivers may be placed in parallel with different gating to form a 10-way OR circuit for pulses. Placing up to 10 emitter follower gates in parallel before the register driver gives a 10-way AND circuit for pulses.

6) Power required: 6.6 ma. at -10 v.
35 ma. at +10 v.

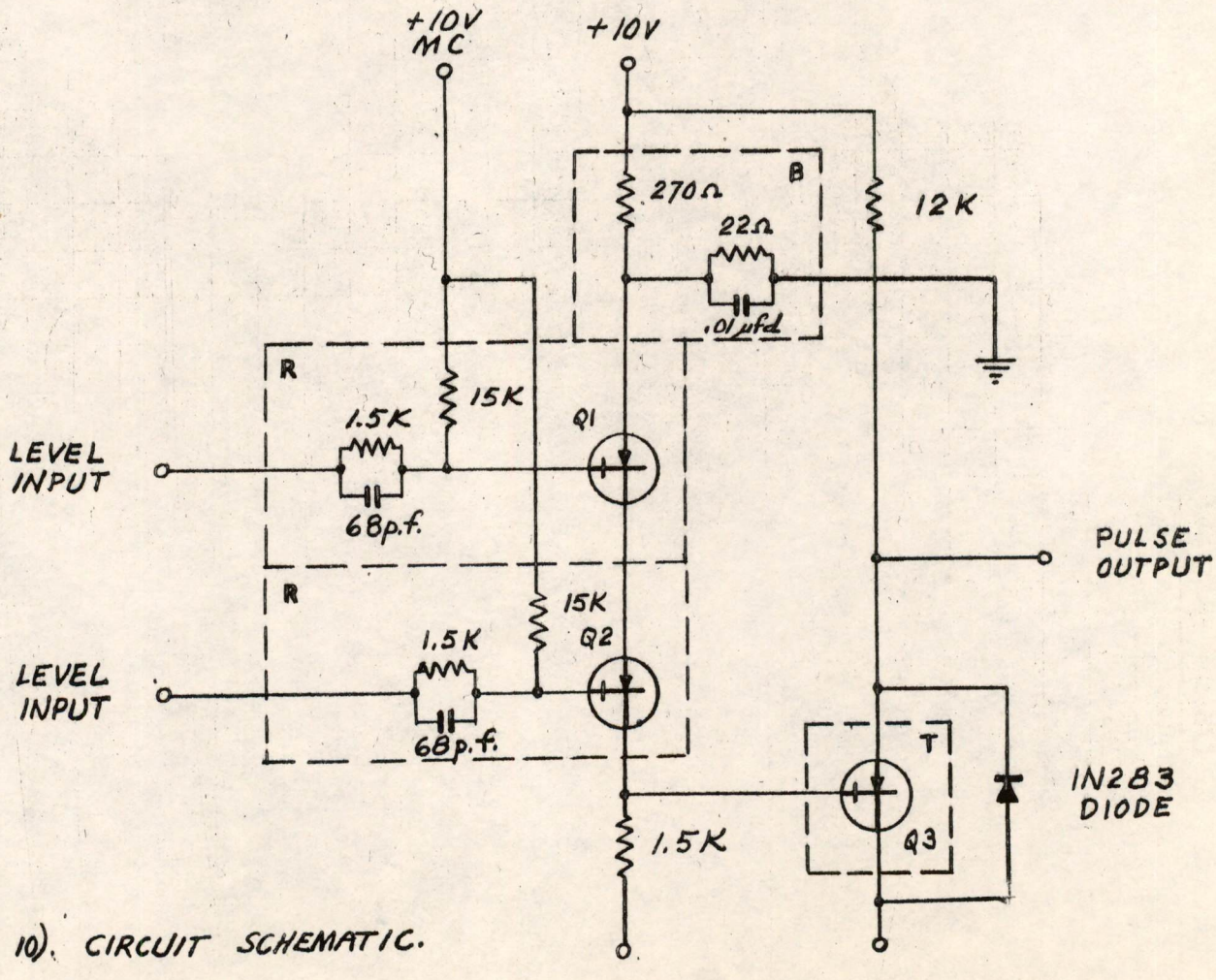
7) Marginal Checking: Vary +10 volt positive bias on inverter bases.

8) Plug-in units used: 1 or 2 R, B, T or E or A.

REGISTER DRIVER.



9). BLOCK SCHEMATIC.



10). CIRCUIT SCHEMATIC.

Pulse and Steering Gates

1) Use: Provide pulses to complement flip-flop.

2) Pulse input: -3 volt 80 to 100 μsec. pulse. Pulse current required: Maximum of 3 ma.

3) Level inputs: Voltage level at ground on one input, -3 volts on the other, coming from the outputs of the flip-flop to be complemented. Input current required to each base at -3 v.: 0.67 ma.

4) Output: Positive pulse up to ground. Will complement one flip-flop.

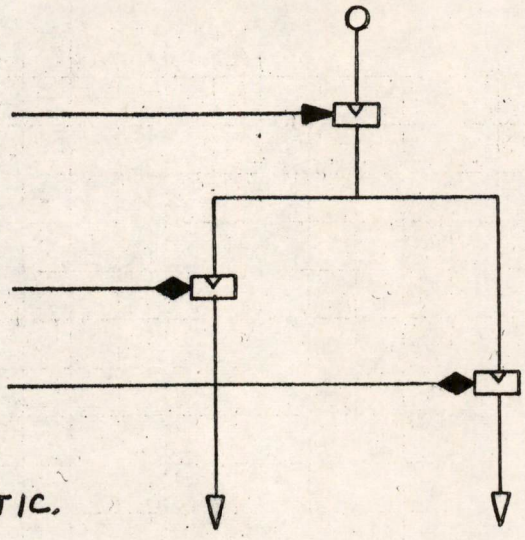
5) Restrictions: There must be no more than 3 transistors in series, including gating level input, pulse input, and steering gate. Up to 15 gates may be placed in parallel on one side of flip-flop input.

6) Power required: 0.24 ma. at +10 v.

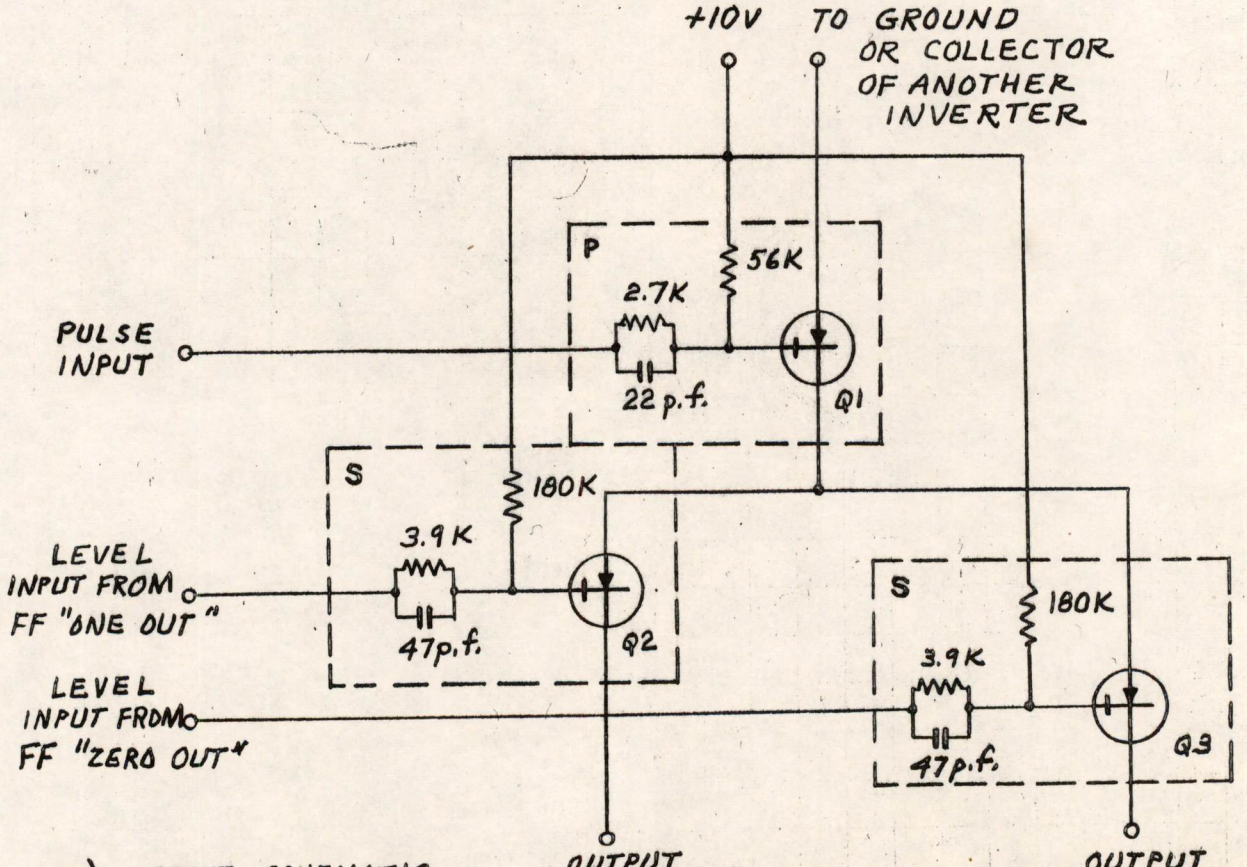
7) Marginal checking: Vary +10 volt positive bias on bases.

8) Plug-in units used: 1P, 2S.

PULSE & STEERING GATES.



9). BLOCK SCHEMATIC.



10). CIRCUIT SCHEMATIC.

Inverting Cascode

1) Uses: Power amplifier and level driver.

2) Input: Voltage level at ground or -3 volts. Input current required: 2.2ma.

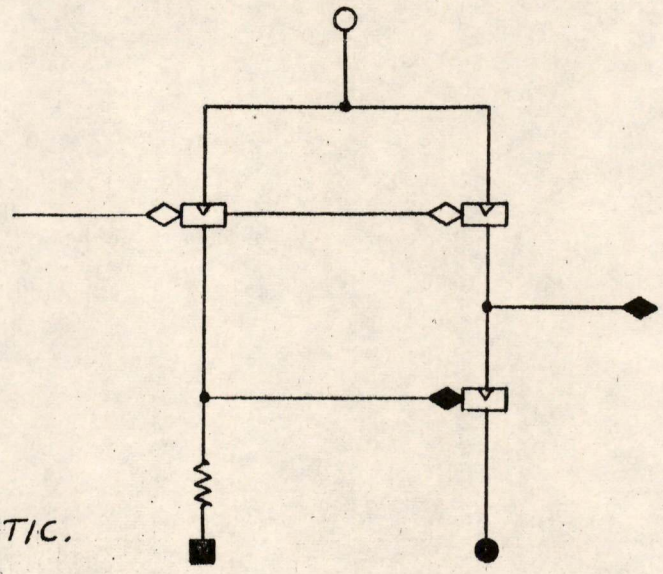
3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current: 12 ma. at -3 v.: 4 ma. at ground level. Can drive maximum of 12 emitter followers or 8 inverters, and one emitter of pulse or level transistor on the same time pulse. Load capacitance for 0.1 μ sec. rise time: 420 uuf. Delay = 30 mμsec.

4) Power required: 12 ma. at -3 v.
5.5 ma. at -10v.
0.24 ma. at +10 v.

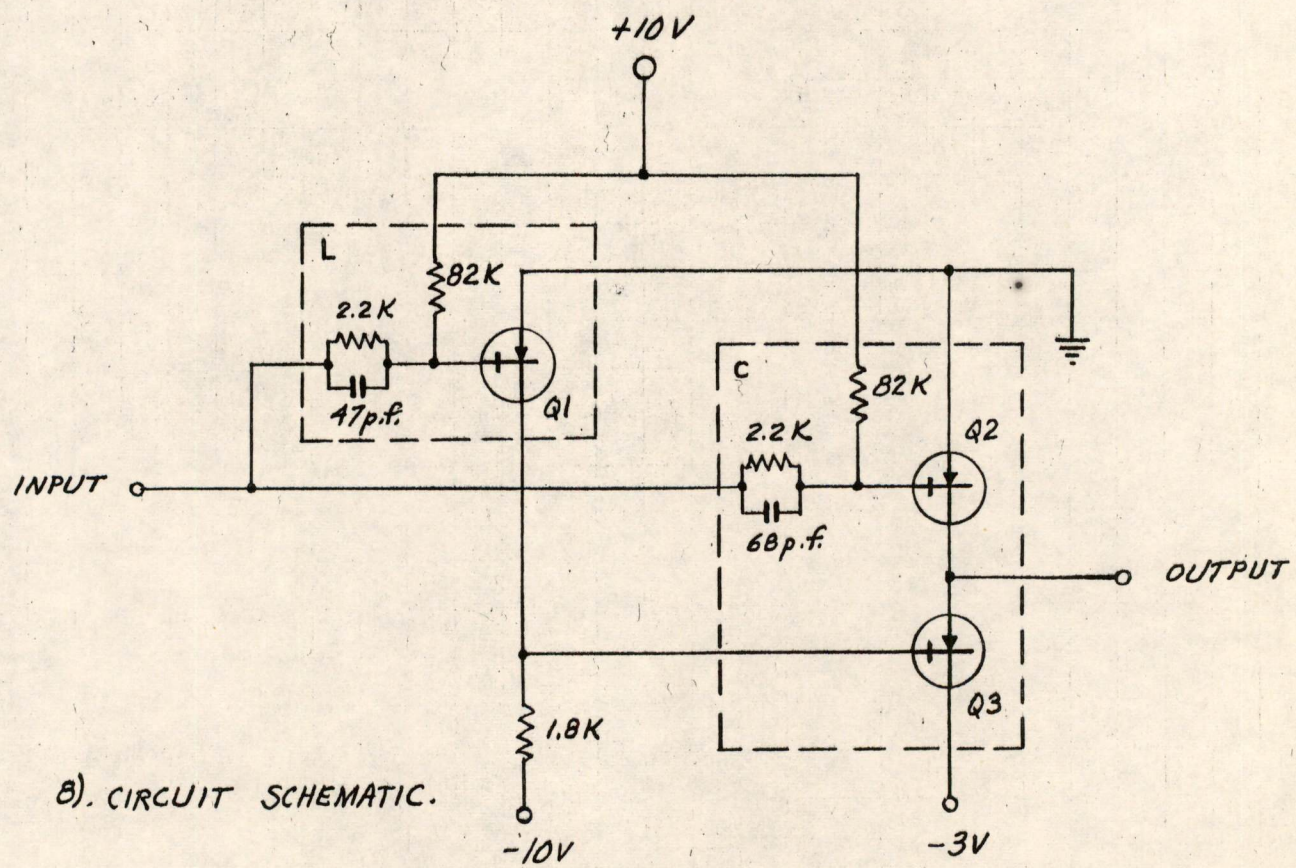
5) Marginal Checking: Vary +10 volt positive bias on bases.

6) Plug-in units used: L,C

INVERTING CASCODE.



7). BLOCK SCHEMATIC.



8). CIRCUIT SCHEMATIC.

Cable Driver (Inverting Cascode)

1) Use: To provide level input into 160 ohm cable, which drives transistor base.

2) Input: Voltage level at ground or -3 volts, from emitter follower gate or inverter gate. Input current required: 2.2 ma.

3) Output: Opposite polarity from input. Voltage level at ground or negative level less than -3 volts determined by voltage drop through 130 ohm resistor in series with cable. Maximum output current: 12 ma. Will drive maximum of 100 feet of K109 coaxial cable (Z_o = 160 ohms; D.C. resistance = 0.7 ohms/ft.)

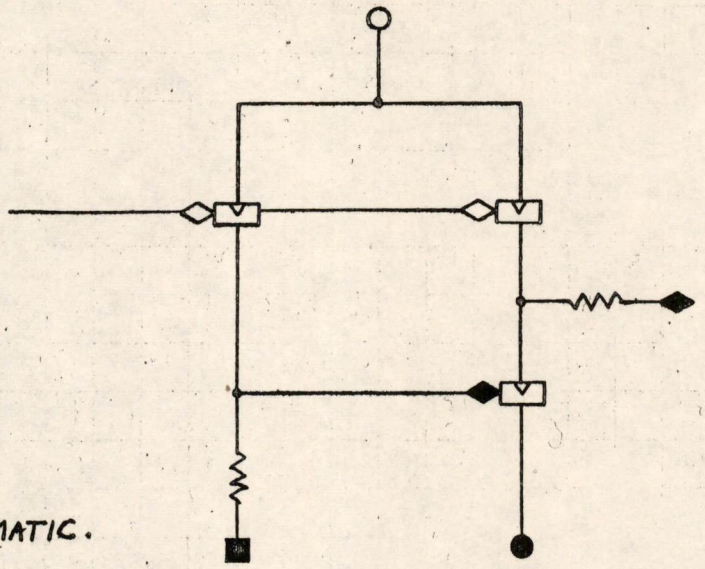
4) Restrictions: No termination should be added at end of cable, as cable is terminated in a resistance of 130 ohms in series with the input end at the cable driver.

5) Power required: 12 ma at -3 volts.
5.5 ma. at -10 volts.
0.24 ma. at +10 v.

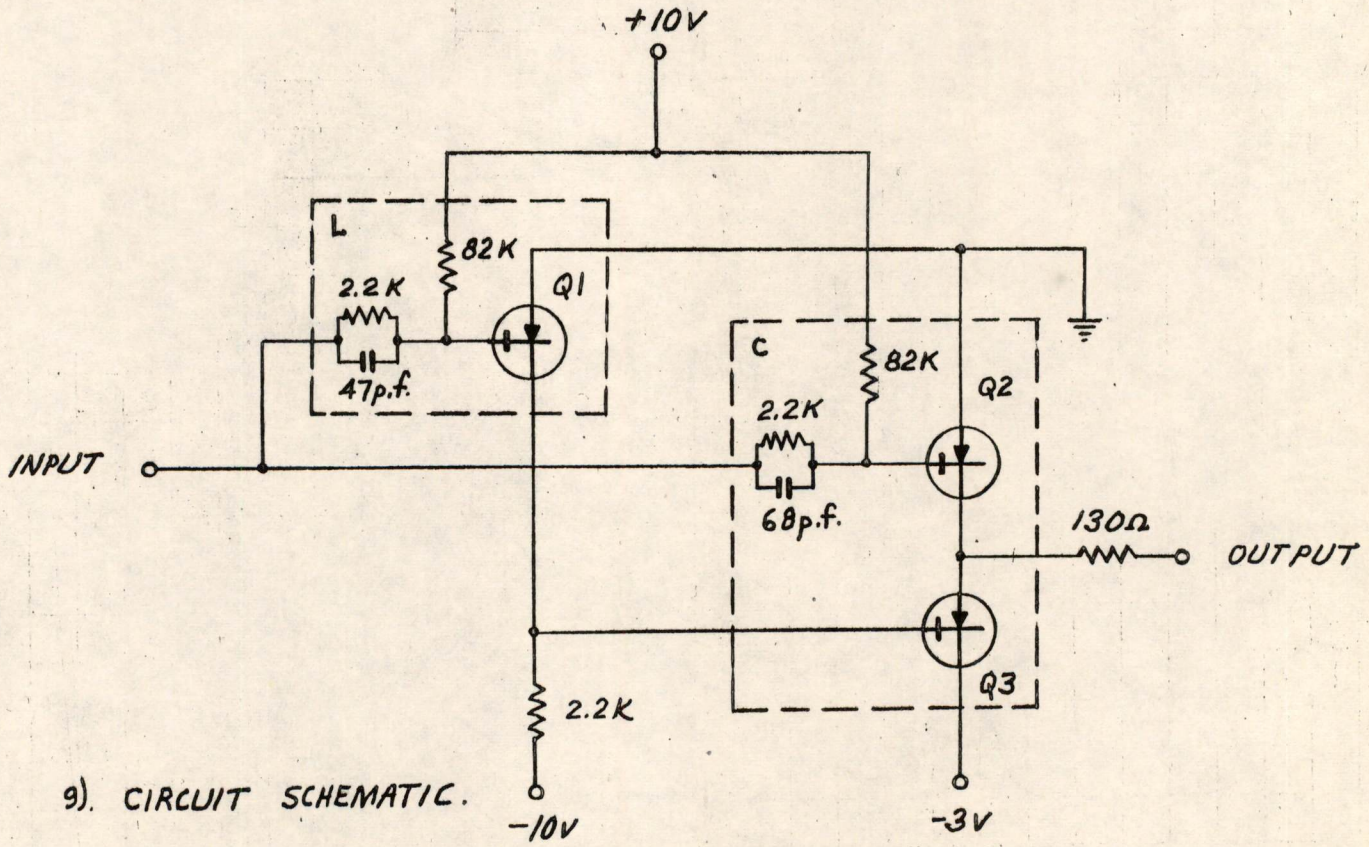
6) Marginal checking: Vary +10 volt positive bias on bases.

7) Plug-in units used: L,C.

CABLE DRIVER.



8). BLOCK SCHEMATIC.



9). CIRCUIT SCHEMATIC.

Flip-Flop

1) Use: To provide logical levels at ground or -3 volts.

2) Input: Positive pulse up to ground from output of pulse gate.

3) Output: One side at ground: other side at -3 volts. Output circuit is inverting cascode. (See Inverting Cascode for specifications) Logical delay before start of rise or fall: 90 to 100 mμsec.

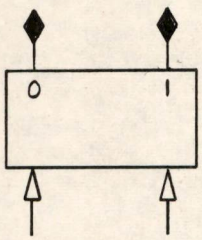
4) Restrictions: Maximum complement rate: 5 mcps.

5) Power required: 18 ma. at -3 volts (maximum)
12 ma. at -10 volts
1.8 ma. at +10 volts.

6) Marginal checking: Vary +10 volt positive bias on inverter bases by varying +10 volt input to "MCA" or "MCB".

7) Plug-in unit used: Flip-flop plug-in unit.

8) Logical symbol



9) Circuit drawing. See Figure 13.

Note on Resistance Values

Inverters

All load resistance to -10 volts are 1.8K, with the following exceptions:

2.2K for inverter in Cable driver cascode, for inverter when followed by two other inverters, and for Accumulator carry chain.

1.5 K for inverters in register drivers.

Normal positive bias resistance for RC input of 2.2 K and 47 uuf is:

82 K. 39 K is used for level input to MBR from memory frame, toggle switch storage, and PETR, and when the level transistor (L unit) in the Program Counter is driven from emitter followers.

Emitter Followers

All load resistance to +10 volts are 3.9 K with the following exception:

2 K is used when two emitter followers are used in parallel to drive another emitter of a pulse or level transistor. In this case 47 ohm resistors are used in the emitters of the emitter followers as current sharing resistances.

Distribution List

Group 63 Staff

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E. Dobbyn
R. A. Eastman
G. W. Geralds
A. J. Grennel
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Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
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SUBJECT: TX-0 Circuitry

To: K. H. Olsen

From: J. R. Fadiman

Date: October 22, 1956

Approved: K. Olsen
K. H. Olsen

Abstract: The high speed logical circuitry used in the TX-0 transistor computer uses Philco 5122 Surface Barrier transistors. AND and OR gates are formed from inverter or emitter follower combinations. The cascode configuration is used as a power amplifier for fast rise and fall times. Timing pulses are generated by vacuum tubes, and gated on and off by a register driver circuit. Marginal checking is accomplished by varying a positive base bias voltage. The TX-0 flip-flop is a high-speed flip-flop package using 10 SBTs and capable of 5 mcps operation.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

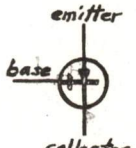
I. Introduction

A. The high speed circuitry for the TX-0 computer uses the Philco 5122 Surface Barrier transistor. The two logical levels are ground and -3 volts. Pulses are negative, with an amplitude of -3 volts and a width of from 80 to 100 mu sec. The supply voltages used for the SBT circuitry are -3, -10 and +10 volts.

B. Symbols (Note)

The following symbols are used.

Transistor (in circuit schematics)



Transistor (in block schematics)

-3 volt level

Ground level

Negative pulse (ground to -3 volts)

Positive pulse (-3 volts to ground)

-3 volt supply

ground

-10 volt supply

+10 volt supply

Note 1: For detailed considerations of transistor logic and symbology, refer to: 6M-4571, by R. C. Jeffrey.

The logical circuitry for the central machine is constructed out of small plug-in units, each containing one, two, or three transistors and associated components. The types of units and their functions are listed below. The schematic circuit diagrams are in figure 1 and detailed descriptions are in the appendix.

Unit	Transistor	Use
P	1 SBT	Pulse input gate to flip-flop
L	1 SBT	Level input gate and inverter
M	1 SBT	Level input gate with high positive bias
R	1 SBT	Register driver inverter
S	1 SBT	Steering gate
T	1 SBT	Single transistor for single emitter-follower
E	2 SBT	Two emitter followers with separate outputs
A	3 SBT	Three emitter followers with a common output
C	2 SBT	Cascode Circuit
F	1 GE4JD1A17	Ferranti Circuit
F (Mod II)	1 GE4JD1A17	Ferranti Circuit
B	None	Emitter bias for register driver
G	1 GE4JD1A17	Indicator light circuit

II Logic

A. "AND" and "OR" Gates

The "AND" and "OR" gates for TX-0 are either emitter followers in parallel or inverters in series or parallel. The AND gate for ground level in, ground level out is emitter followers in parallel as shown in Fig. 2. Because of the restrictions of speed for 5 mcps circuits, a maximum of 10 emitter followers may be placed in parallel in this fashion, providing up to a 10-way AND gate. An inverting AND gate for ground level in, -3 level out is shown in Fig. 3. Because of limitations of speed, only two inverters may be placed in parallel. The capacitance to ground goes up as βC_c where C_c is the collector capacitance of an off transistor and β is the current gain of the transistor, grounded emitter. The inverting OR gate for ground level in, -3 level out is shown in Fig. 4. Because there is a finite voltage drop across a saturated transistor, (about 0.1 volt), only two inverters may be placed in series in this manner.

B. Inverter Circuit

For the inverter circuit (Fig. 5) the values of the input resistance and positive bias resistance are so calculated that there is safety margin when the transistor is saturated and when it is cut-off. This insures maximum noise rejection and tolerance to signal variation. It is assumed on the basis of several tests that no transistor will have a β of less than 5 at 5.5 ma. collector current. (Our minimum acceptance β at low current is 15, and 11 at end of life). A larger amount of positive bias is used on inverter input gates to flip-flops when the input is from a distant frame, such as from core memory, toggle switch storage, or the photo-electric tape reader. In these cases the induced noise voltages are apt to be larger than usual, and the input impedance to the flip-flop is sufficiently high to allow the use of the larger positive bias current, and consequently smaller input base current.

This bias is also used in cases where the ground level for the emitter is supplied from an emitter follower gate. Such a level goes

0.3 volt positive and thus it is necessary for the base to be held at about +0.5 volts to provide adequate margins during cut-off.

All of the inverters in TX-0 use a supply voltage of -10 volts. However, the actual voltage at the collector never exceeds -4 volts, since it is clamped, either by an emitter follower following it, or by a voltage divider to ground. A single inverter provides current sufficient for driving three emitter followers or two inverters. It can drive a capacitance of 75 uuf, with a fall time of 0.1 μ sec.

C. Emitter Follower Circuit

The logical circuitry utilizes a combination of inverters and emitter followers which in general are alternated. This ensures that when an emitter follower is turned on, it is always kept in saturation since its base is returned effectively to -10 volts through the load resistor of the previous inverter. The difference in driving capabilities of the saturated and non-saturated emitter follower is shown in the graph of Fig. 6. The load resistance of the emitter follower is returned to +10 volts instead of to ground to shorten the rise time of the emitter follower. This emitter follower will provide 8 ma. of output current at -3 volts and will drive a capacitive load of 120 uuf, with a rise time of 0.1 μ sec.

D. Cascode Circuit

In order to achieve faster rise and fall times and greater driving ability than is possible with either the emitter follower or the inverter, the "cascode" circuit is used. The logical and circuit schematics are shown in Fig. 7. The inputs to Q_2 and Q_3 are always opposite in phase so that in the steady state case only one transistor is conducting. Q_3 acts as an emitter follower which provides the driving current and pulls the input quickly down to -3 volts. Q_2 acts as an inverter whose function is to pull the output quickly up to ground during the transition. Thus, the circuit utilizes the fast rise time of the inverter and the fast fall time of the emitter follower.

This configuration is capable of driving a capacitive load of 420 uuf. with a transition time of 0.1 μ sec. No power is wasted in load resistances, and this circuit is designed to provide 12 ma. output current at -3 volts. It will drive 12 emitter followers or 8 inverter bases, and one emitter of an inverter. TX-0 uses the cascode as the output stage of all flip-flops, as a power amplifier for driving many transistor bases, and as a cable driver.

Cascode cable drivers are used when sending levels to the memory over 160 ohm coaxial cable. The cable is terminated at the input end by a resistance in series with the cable. This series termination is possible because, unlike the emitter follower or inverter, the cascode circuit looks like a very low impedance (less than 10 ohms) when driving in either direction. Thus, the driven end of the cable is properly terminated at all times.

III Pulse Circuitry

A. Timing Pulses

The timing pulses for the computer are generated by vacuum tubes. Thirty volt positive pulses are sent to the computer through 93 ohm coaxial cables. 7:1 pulse transformers with a one turn secondary are used at the computer to provide approximately 3.4 volt negative pulses. A 1N283 diode is used across the primary in order to damp the overshoot.

B. Register Driver

Gated register drivers (Figures 8 and 9) supply the 3 volt negative pulses to the input gates of the flip-flops. The pulse input is at the collector of Q_3 and the output is from the emitter. A pulse is passed when Q_3 is saturated from the negative output of inverters Q_1 and Q_2. Thus, a ground input to either Q_1 or Q_2 is necessary to pass a pulse through the register driver. The two inverters in series thus give a two-way OR circuit for the pulses. Up to a 10 way OR circuit can be constructed by paralleling register drivers with a common pulse input and output but different gating. In order to form an AND circuit for pulses, emitter follower gates are

placed in parallel to feed the inputs of the inverters. All the inputs must be at ground to pass a pulse. The pulse output of the register driver closely follows the pulse input. The maximum pulse current is 30 ma., sufficient for driving 10 pulses bases, and the pulse voltage drop through the register driver is less than 0.5 volt.

C. Pulse Inputs to Flip-Flops

In order to set or clear the TX-0 flip-flop the "one" or "zero" input must be brought up to ground by the output of a pulse inverter. Up to 15 such inputs may be tied in parallel to one side of the flip-flop. The negative pulse is inverted and gated by a circuit such as this: Fig. 10. Or, alternately, only one transistor may be used as a gate in this manner: Fig. 11. Here a ground level must be supplied to the emitter in order to pass the pulse. This arrangement requires a level current equal to $\frac{I_c}{\alpha}$ while the two transistor gate requires a level current equal only to $\frac{I_c}{\beta} = \frac{I_c}{\alpha}(1-\alpha)$. In order to complement the flip-flop, the pulse must be steered to the proper side of the flip-flop. The circuit which does this is shown symbolically in Fig. 12.

IV Marginal Checking

Marginal checking of all TX-0 circuitry is accomplished by varying the +10 voltage on the base of the inverter transistors. Increasing this positive bias supply effectively reduces the negative base current into the transistor and tends to bring it out of saturation. Making the positive bias supply negative tends to allow the transistor to conduct when it should be held cut off. Emitter followers are not directly marginal checked, but their condition can be investigated by marginal checking the inverters which proceed and follow it. For these inverters normal margins are slightly greater than $\pm$ 10 volts either side of the normal +10 volt supply.

V Flip-Flop

The TX-0 flip-flop is shown in Fig. 13. The circuitry is similar to that already described, with RC coupling between inverters, positive bias, and emitter follower clamping. Q_1 and Q_2 are pulse amplifiers

which are normally conducting and are cut off by the positive input pulse at the "zero" or "one" input. Q_3 and Q_4 are the flip-flop transistors themselves which are arranged in a conventional RC-coupled Eccles-Jordan trigger circuit. When an input pulse cuts off Q_1 or Q_2 this opens the emitter circuit of Q_3 or Q_4, and changes the state of the flip-flop. Q_5 and Q_6 are inverters which are used to saturate the emitter followers of the output cascode. Q_7 and Q_8, and Q_9 and Q_{10} form the cascode circuits on the "one" and "zero" sides respectively. Their operation is the same as that previously described for the cascode circuit, with the opposite phases being obtained from the inverters on opposite sides of the flip-flop.

The output wave form at 10 mcps is shown in Fig. 14, and various marginal checking curves and output characteristics of the flip-flop are shown in Figs. 15 through 22.

J. R. Fadiman

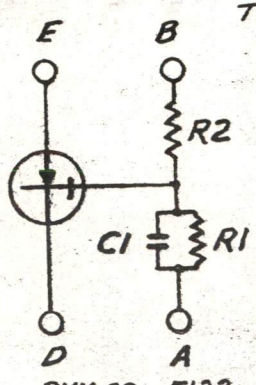
J. R. Fadiman

Attachments:

Fig. 1: SA-65640-3
Figs. 2 through 12
Fig. 13: D-63369
Fig. 14: A-65366
Fig. 15: A-67294
Fig. 16: B-65729
Fig. 17: B-65721
Fig. 18: B-65720
Fig. 19: B-65719
Fig. 20: B-65727
Fig. 21: B-65717
Fig. 22: B-65718
Appendix (15 pages)

JRF:mmw

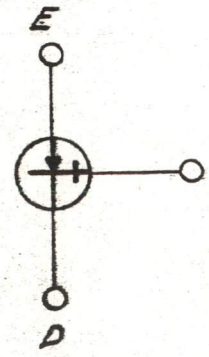
SA 65640-3



TYPE	R1	C1	R2	USE
P	2.7K	22pf	56K	PULSE INPUT GATE
L	2.2K	47pf	82K	LEVEL INPUT GT. & INV.
M	2.2K	47pf	39K	MBR LEVEL RD-IN FROM MEMORY
R	1.5K	68pf	15K	REGISTER DRIVER INV.
S	3.9K	47pf	180K	STEERING GATE

PHILCO 5122

TYPE T

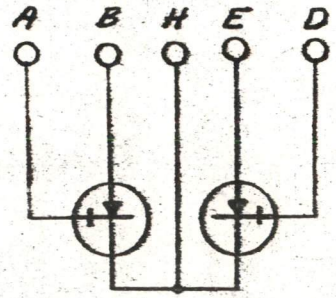


SINGLE TRANSISTOR

PHILCO 5122

TYPE E

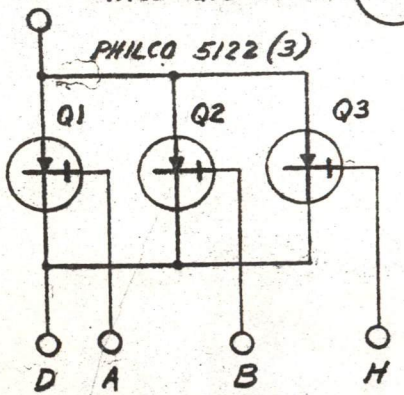
TWO E.F.'S.

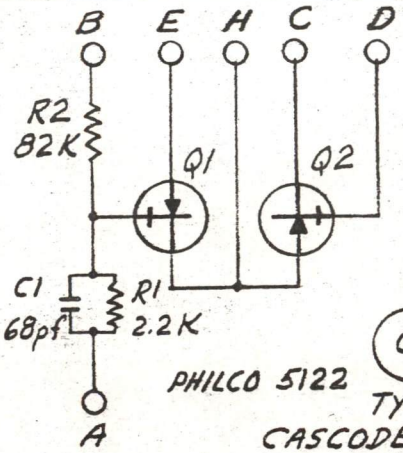


PHILCO 5122

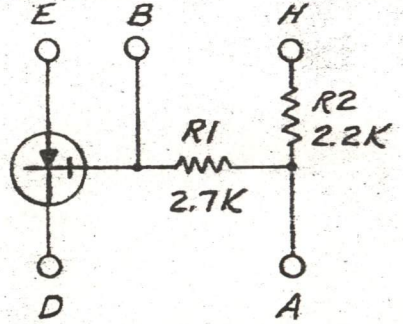
E THREE E.F.s TYPE A

PHILCO 5122 (3)



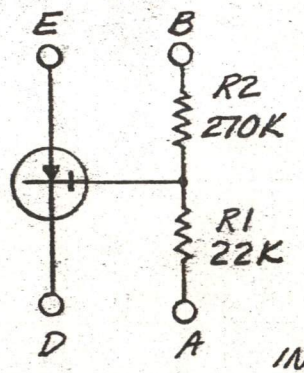


PHILCO 5122 TYPE C CASCODE

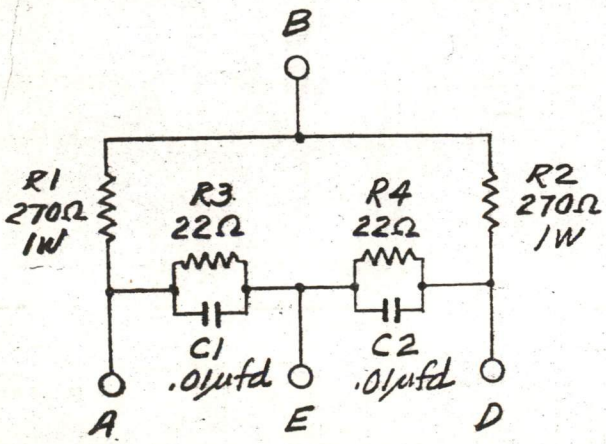


GE 4JD1A17 TYPE F FERRANTI

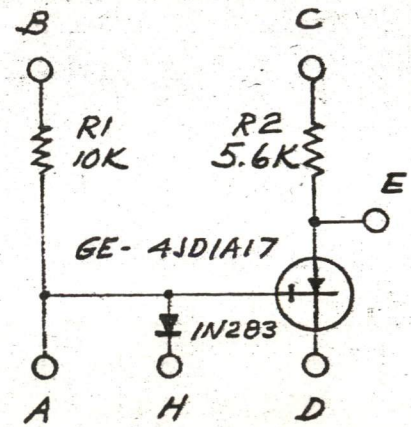
TYPE G



GE 4JD1A17 INDICATOR LIGHT CIRCUIT



TYPE B BIAS



FERRANTI (MOD II) F II

"BOTTLED" PLUG-IN UNITS PIN CONNECTIONS.

3-19-56 ~~DP~~

SA 65640-3

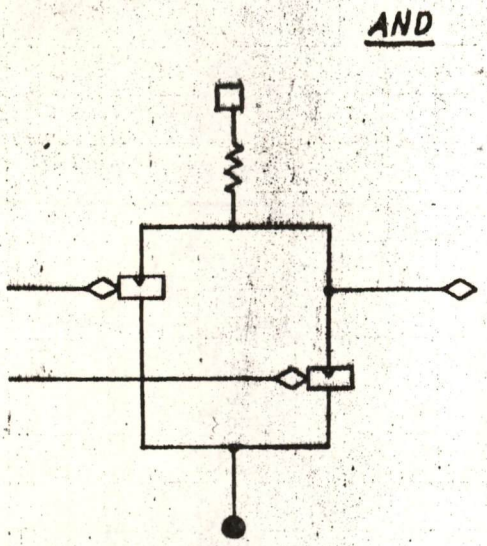


FIG. 2

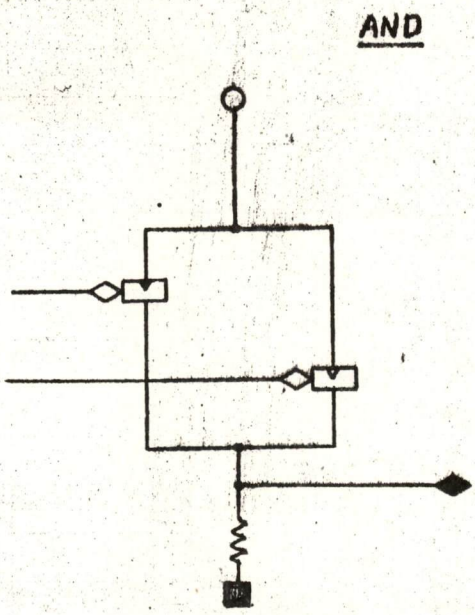


FIG. 3

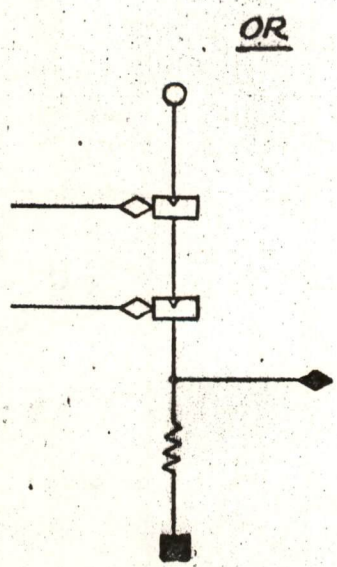


FIG. 4

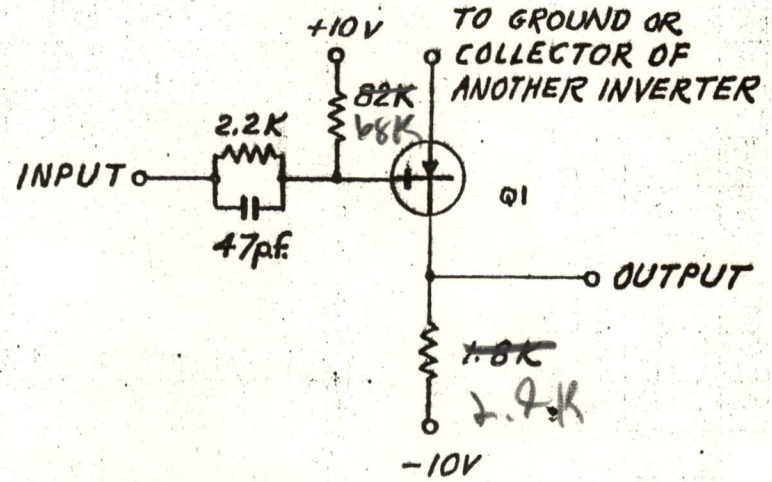
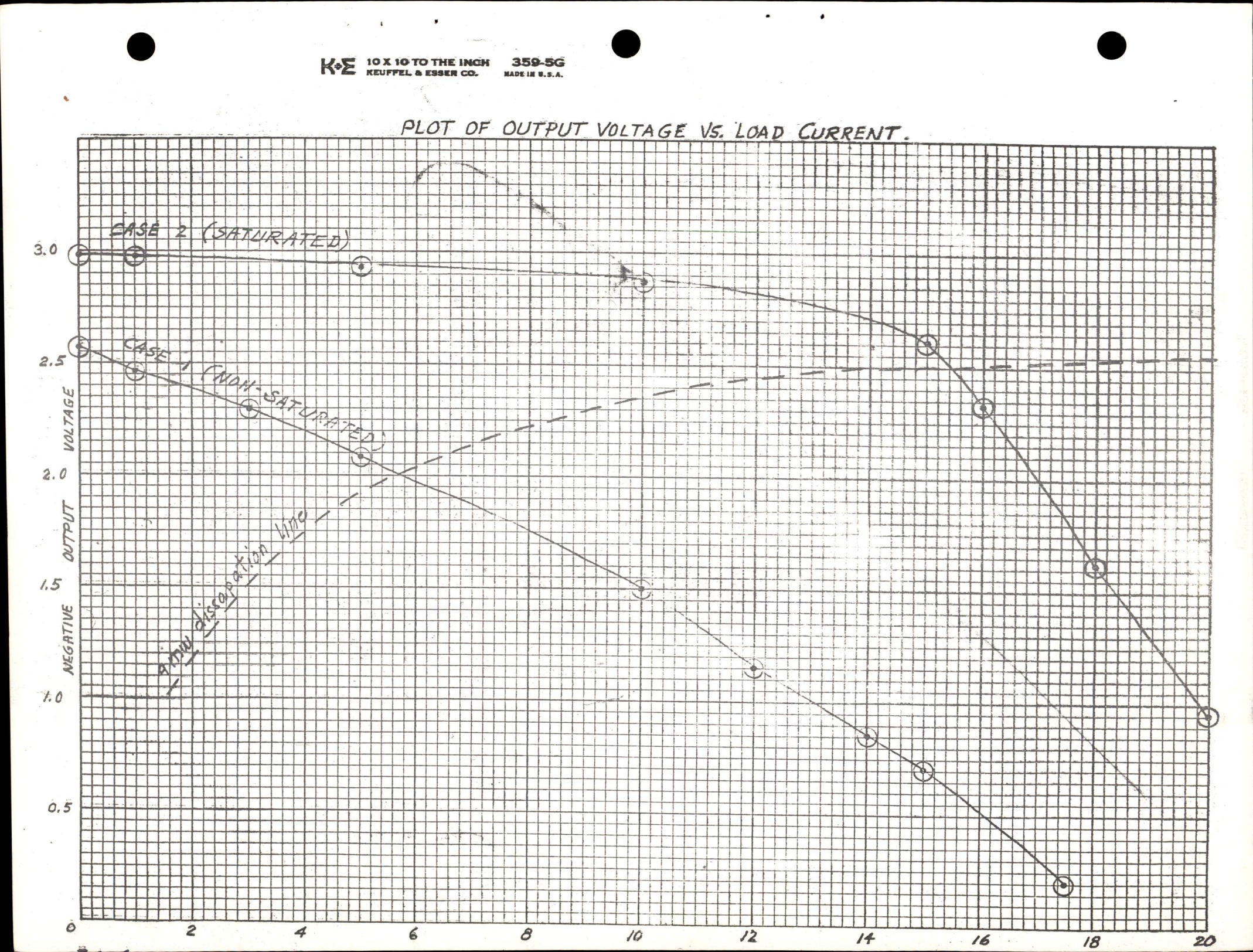
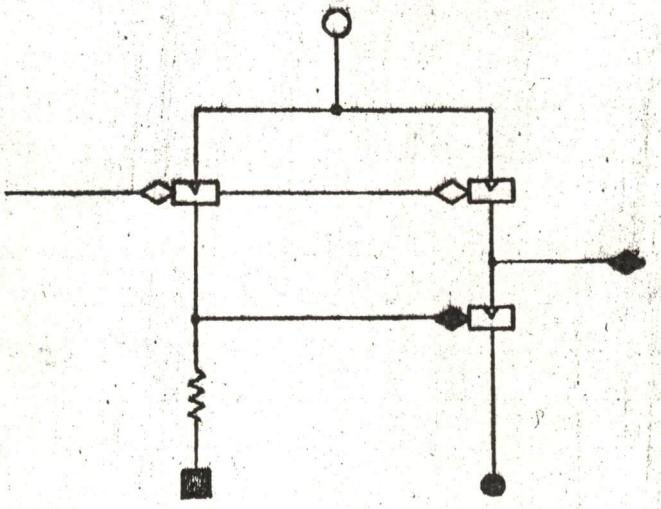
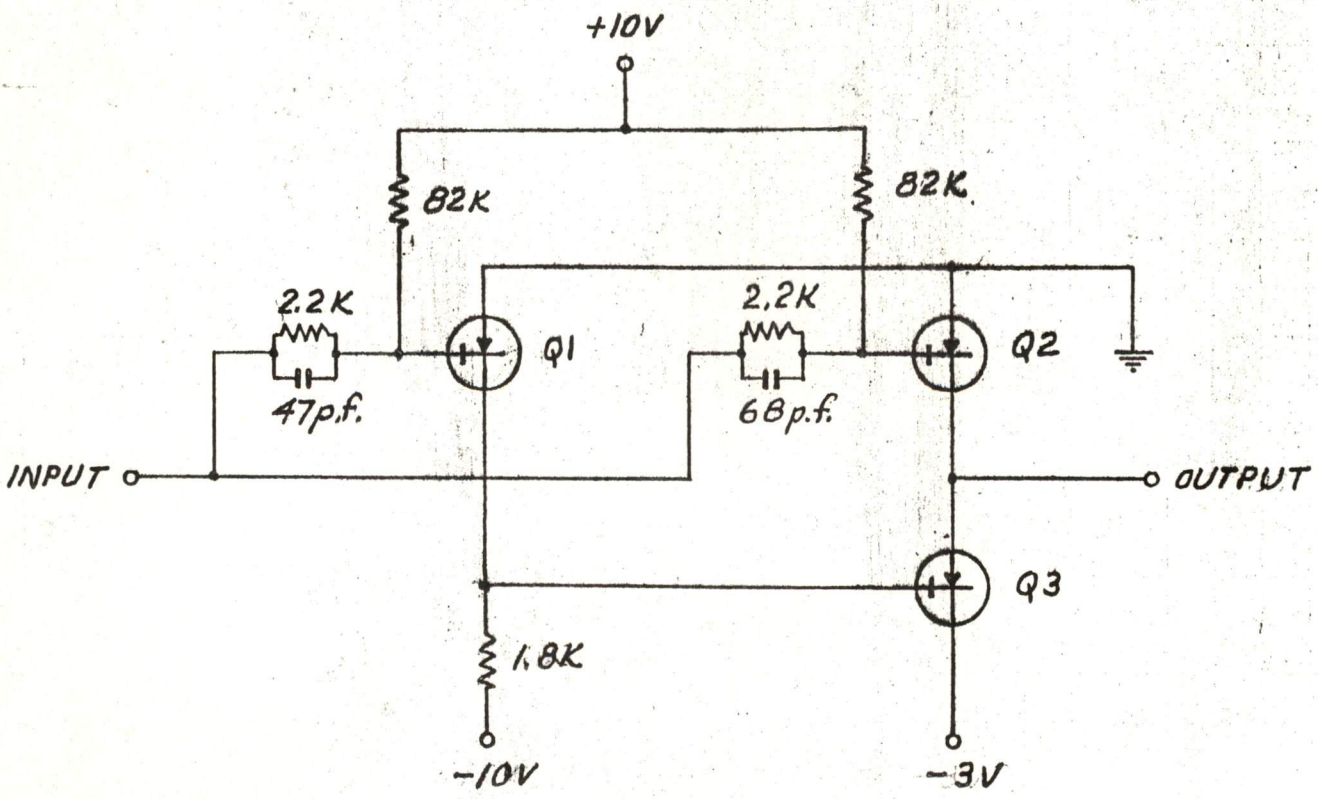


FIG. 5







FIGS. 7

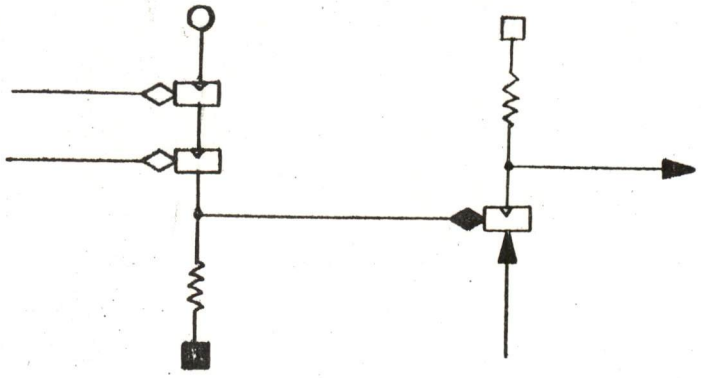


FIG. 8

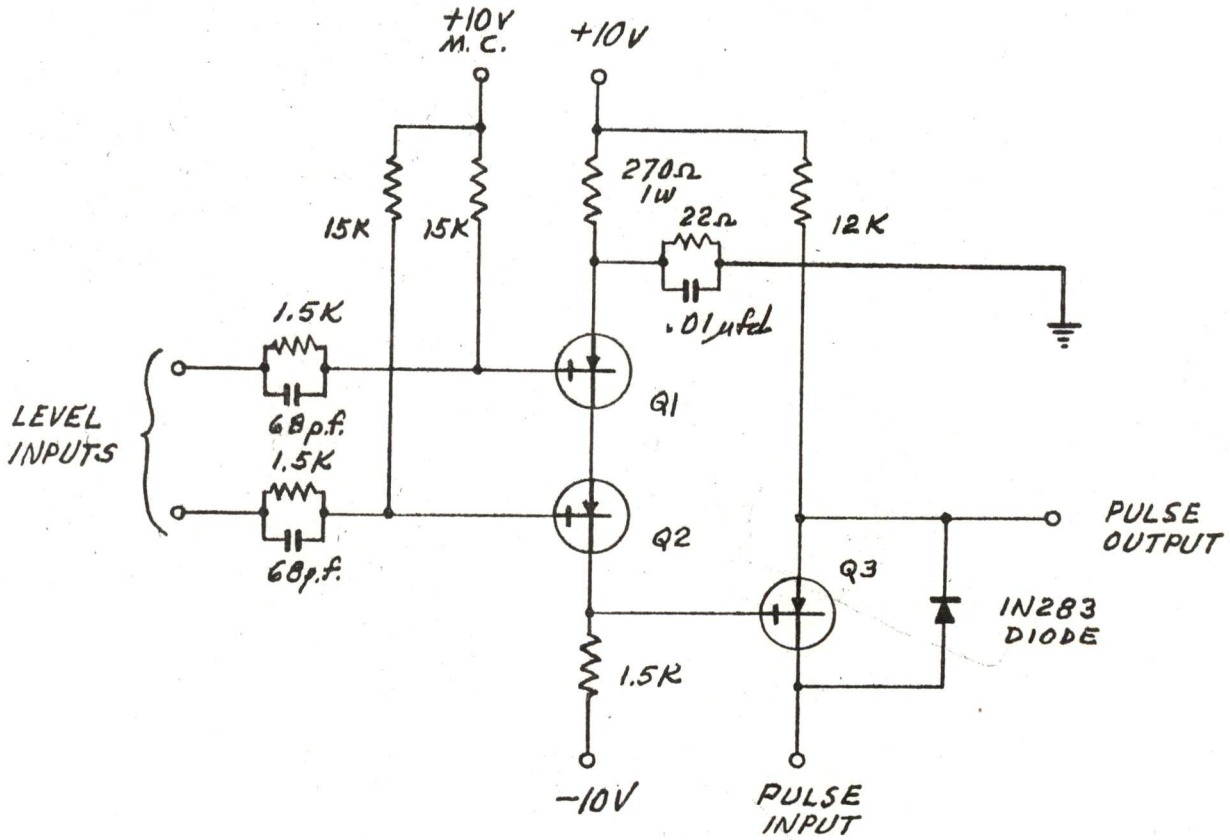

+10V
M.C.
+10V
270Ω
1W
22Ω
12K
15K
15K
.01 μfd.
1.5K
LEVEL
INPUTS
68 p.f.
1.5K
68 p.f.
Q1
Q2
Q3
PULSE
OUTPUT
IN283
DIODE
1.5K
-10V
PULSE
INPUT

FIG. 9

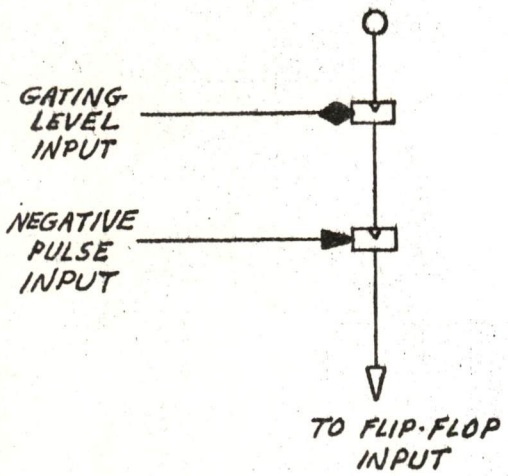


FIG. 10

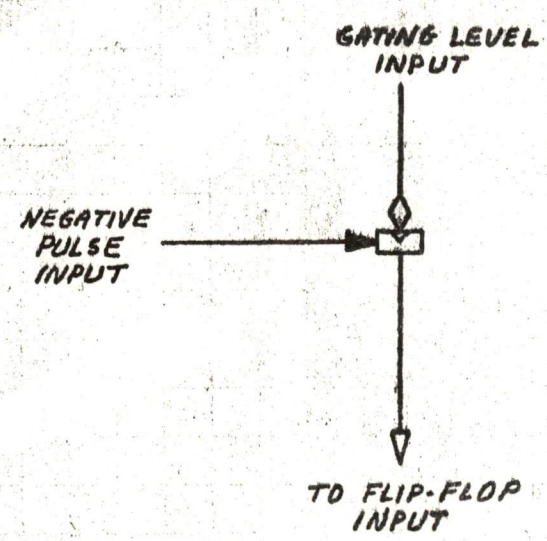


FIG. 11

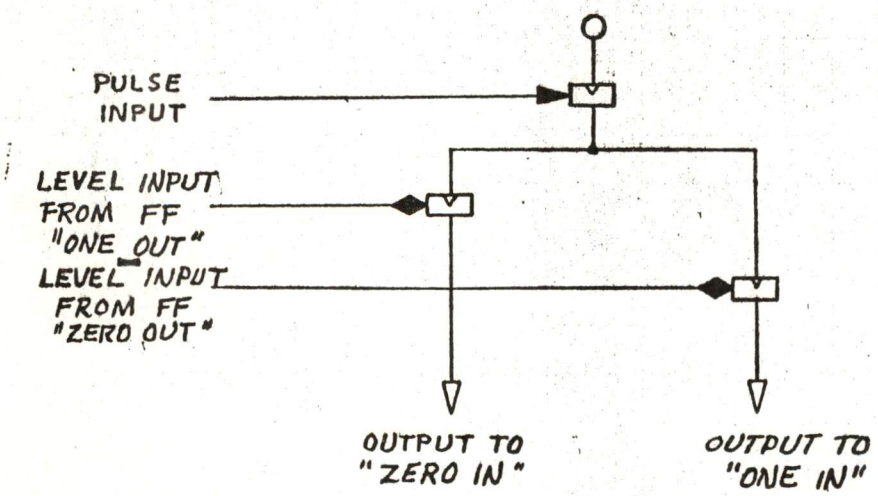


FIG. 12

D-63369
VG-71
F-3140
SN-1328
F-3181

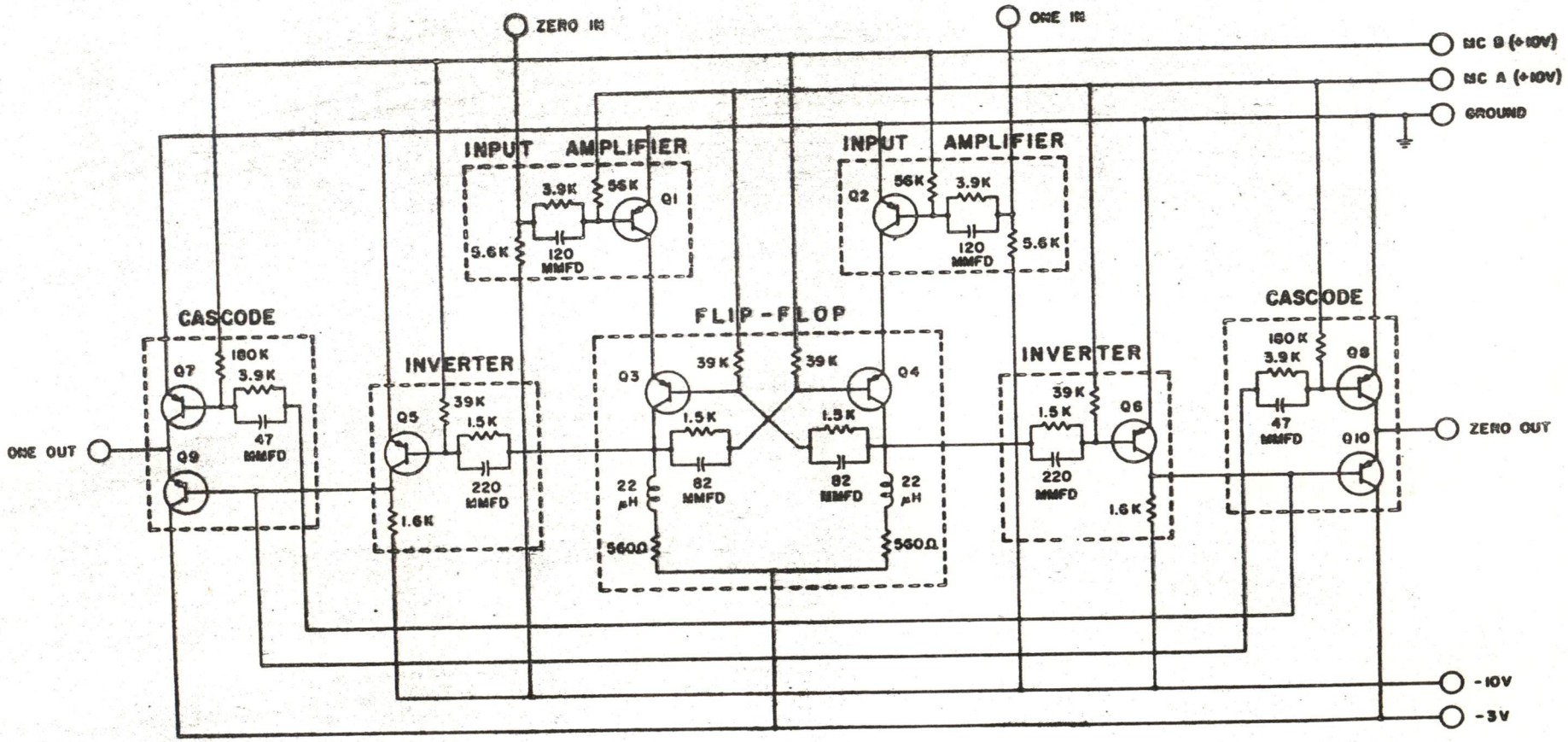
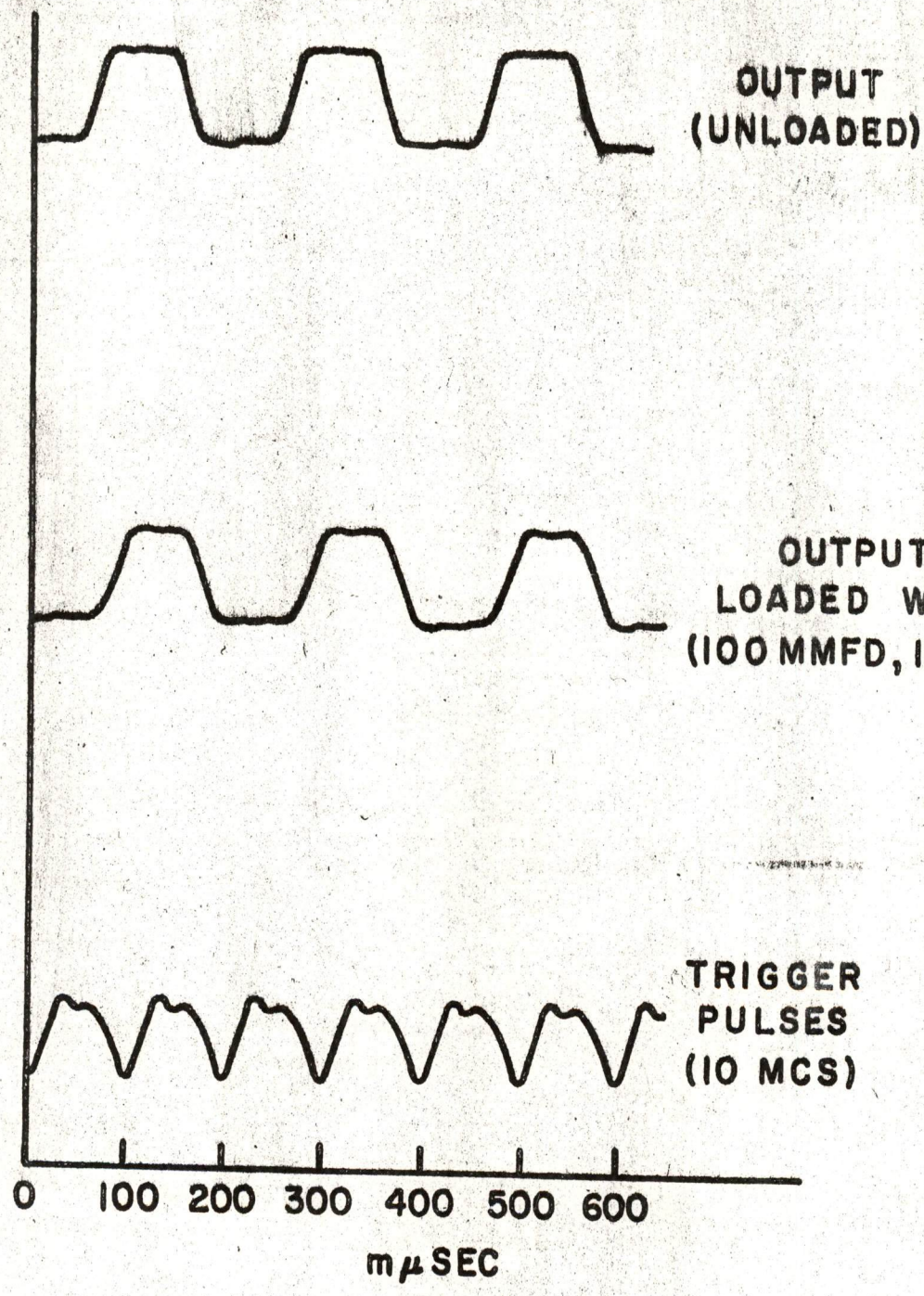


FIG. 13

TX-0 FLIP-FLOP



TX-0 FLIP-FLOP

A-65366
VG-82
SN-1327
F-3180

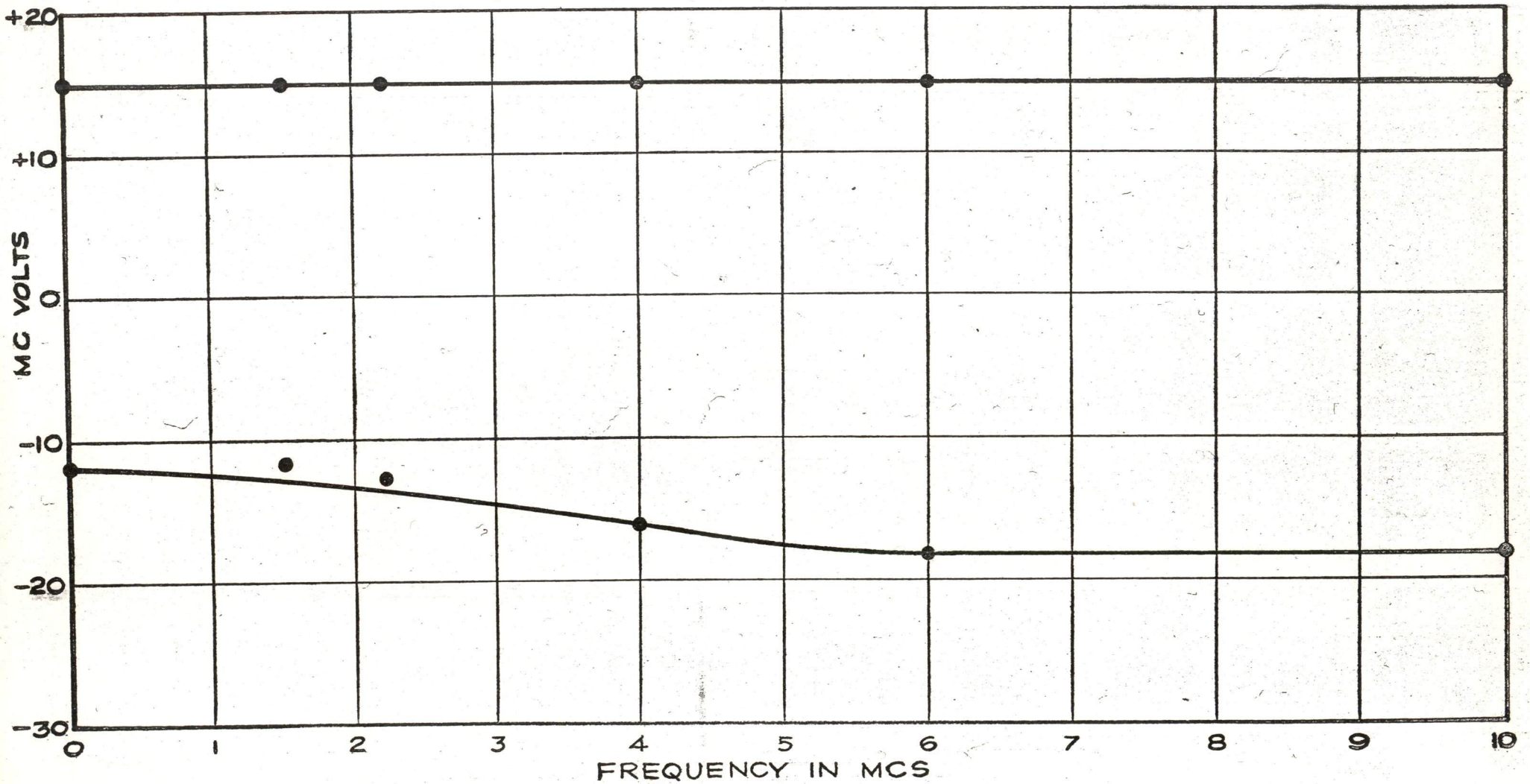
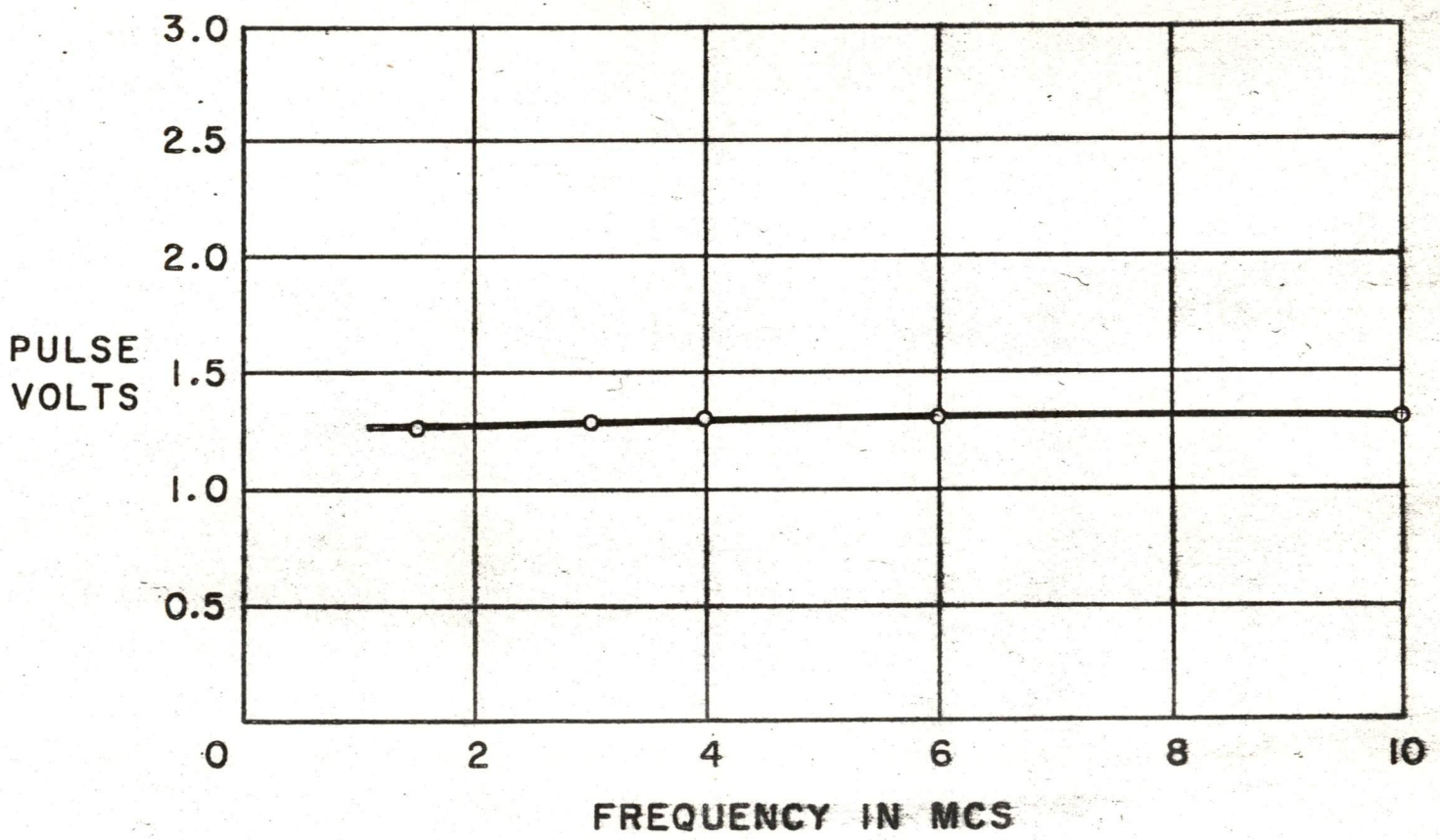


FIG. 15

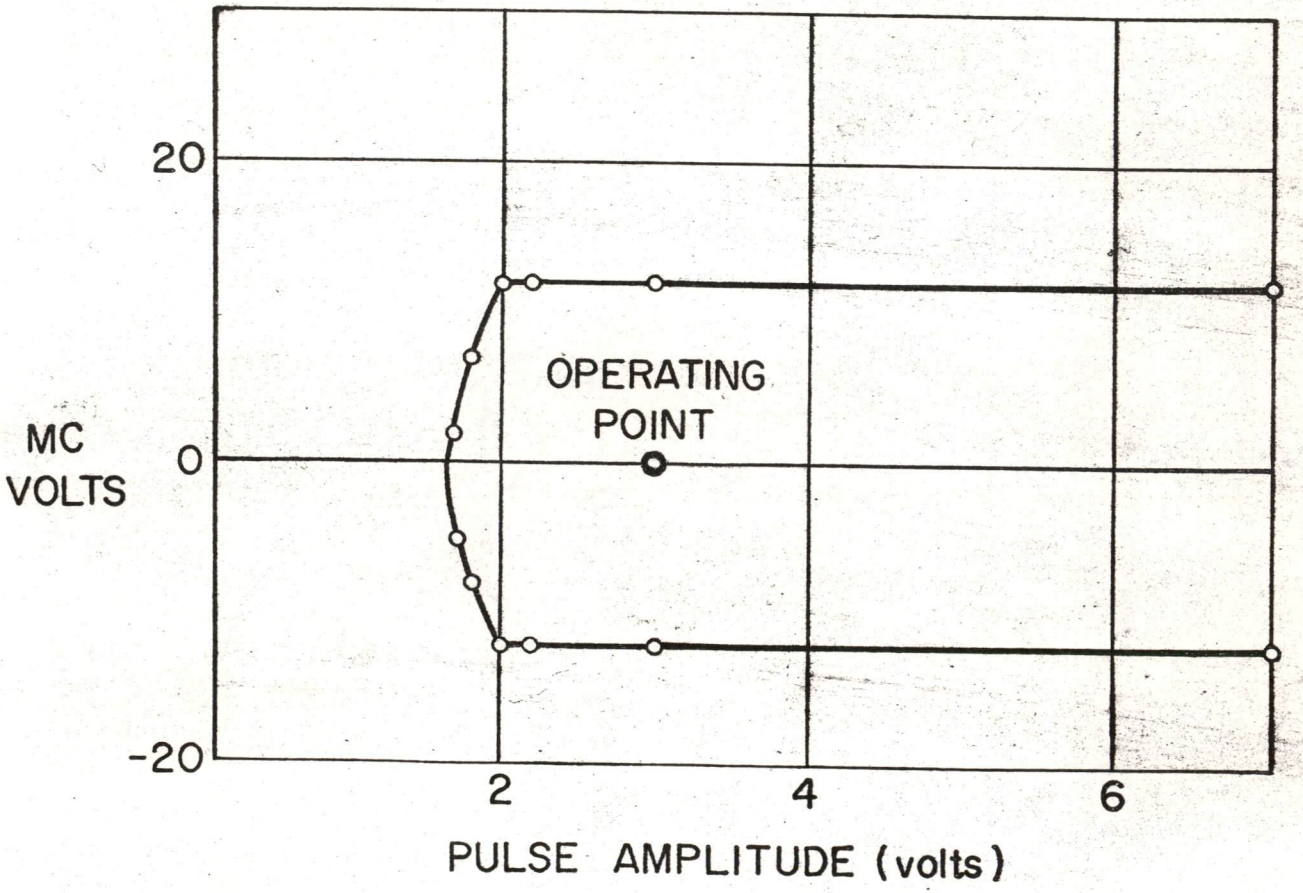
FREQUENCY MARGINS

B-65729
SN-1329
F-3184



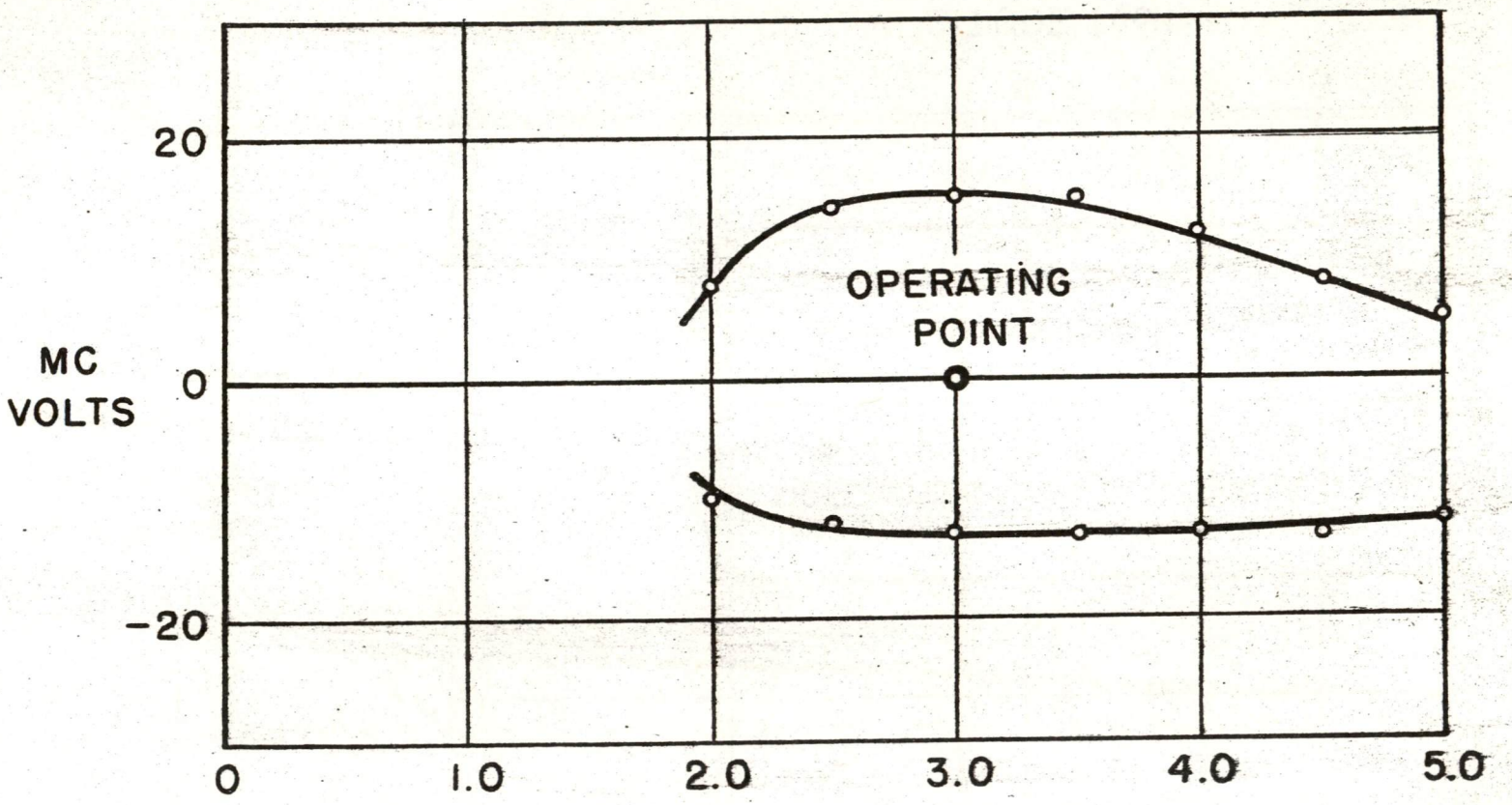
TRIGGER SENSITIVITY

B-65721
SN-1325
F-3178



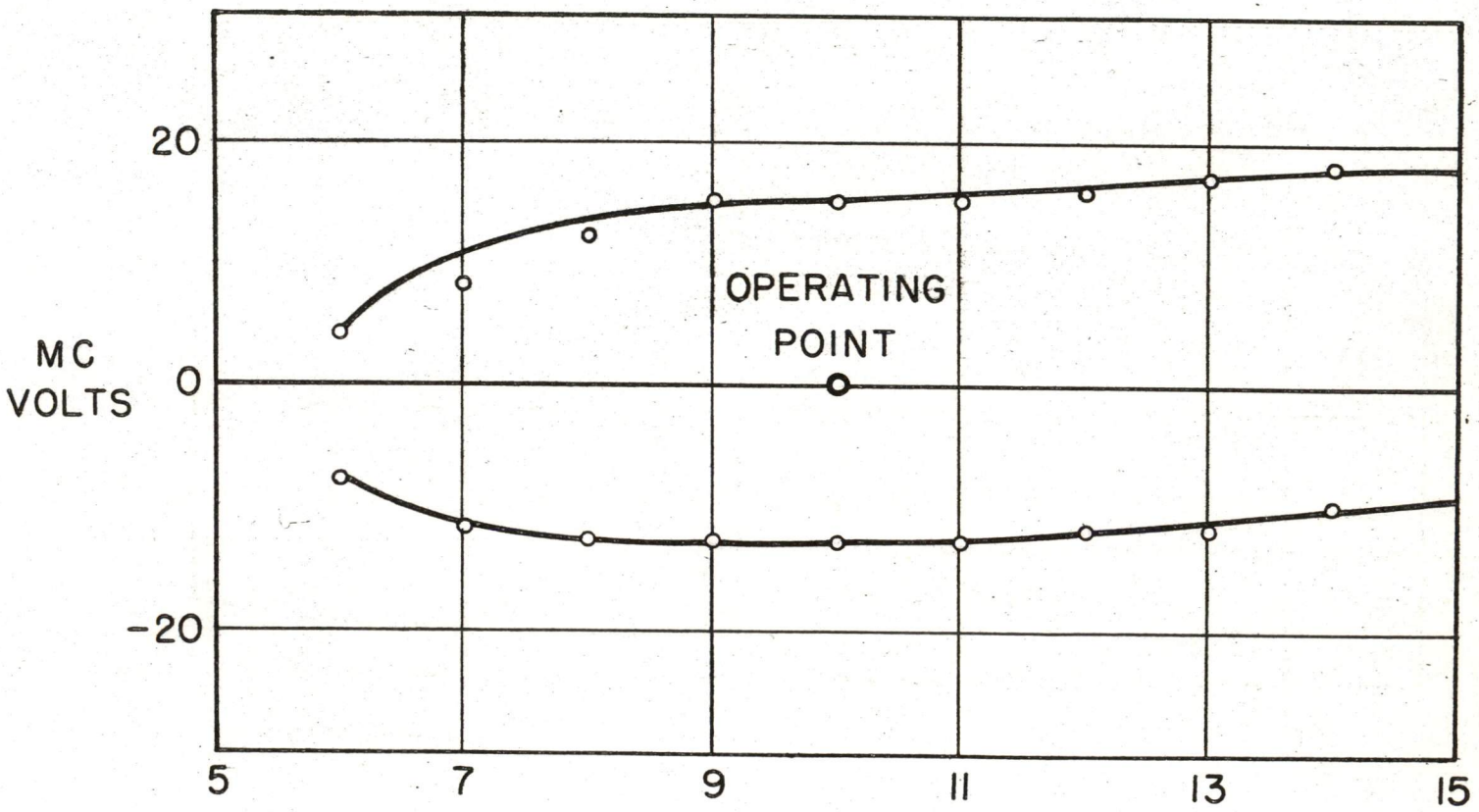
PULSE MARGINS

8-65720
SN-1324
F-3177



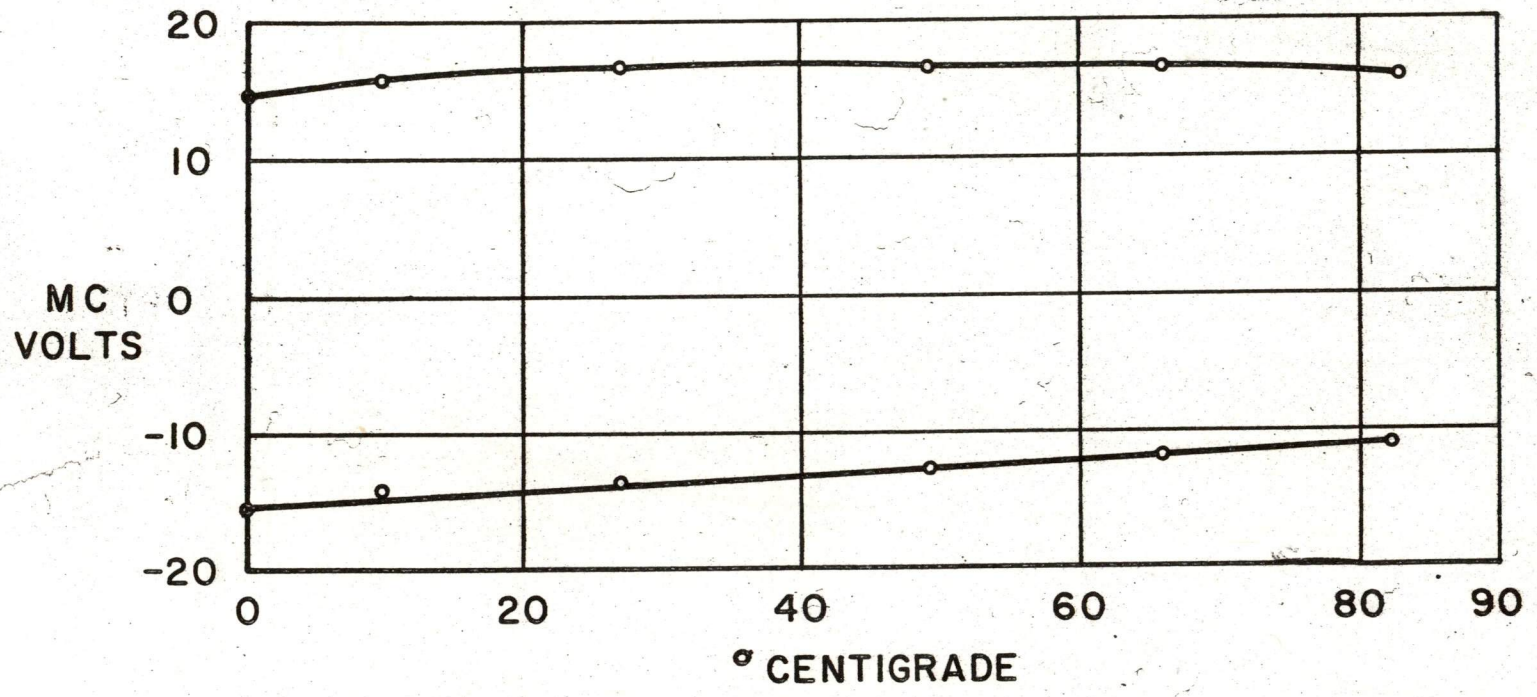
-3 VOLT SUPPLY MARGINS

B-65719
SN-1323
F-3176



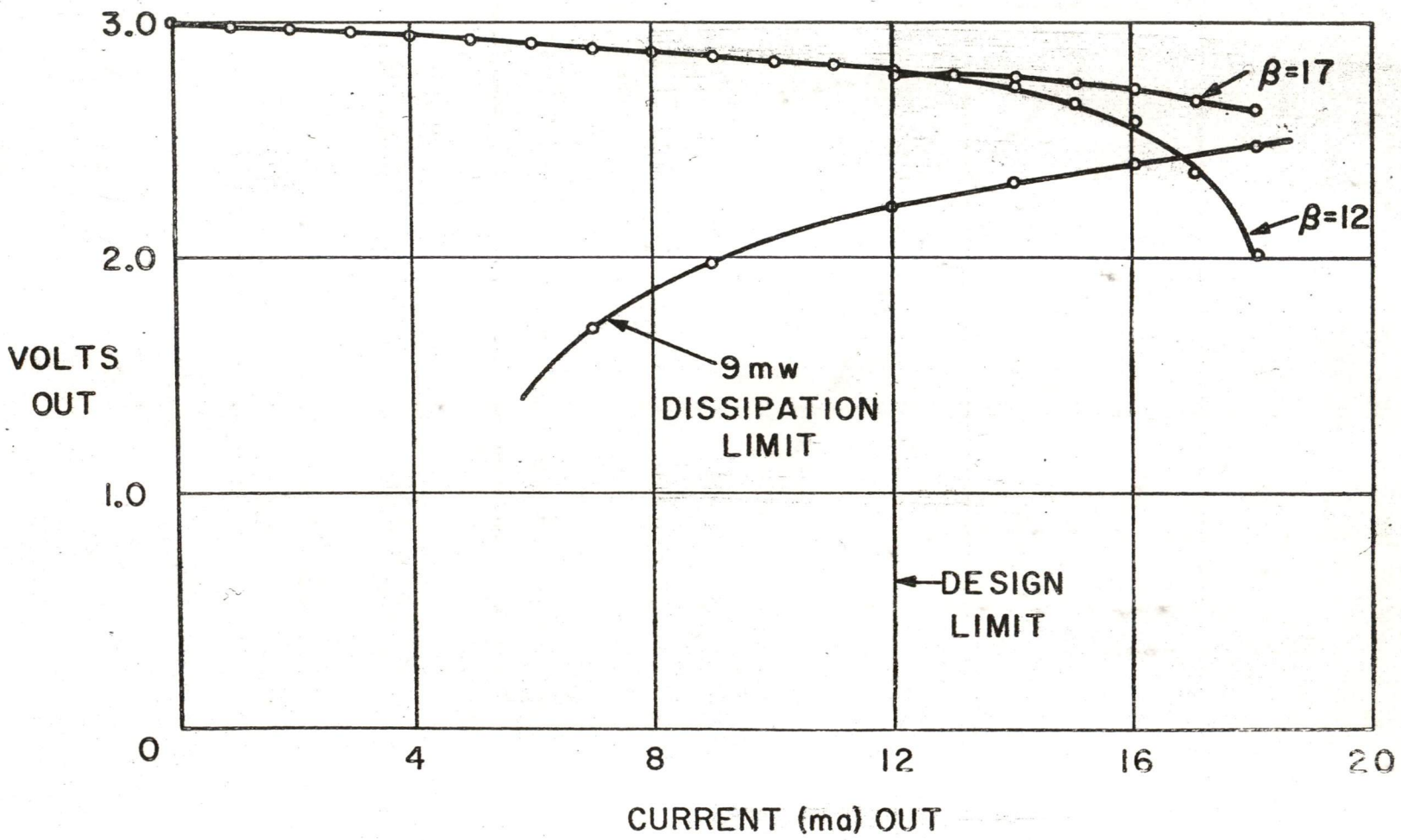
-10 VOLT SUPPLY MARGINS

B-65727
SN-1330
F-3185

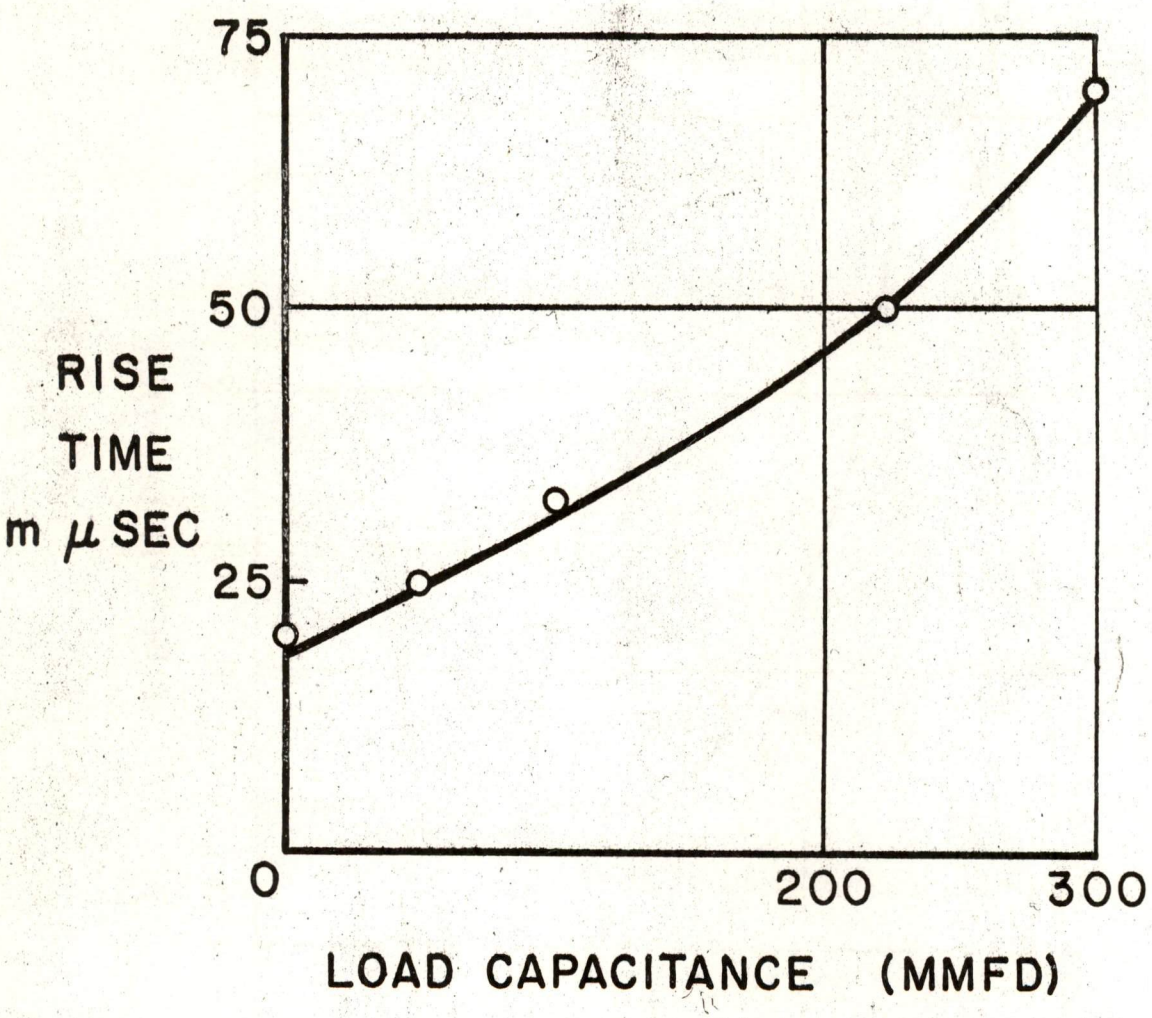


TEMPERATURE MARGINS

B-65717
SN-1321
F-3174



OUTPUT VOLTAGE



RISE TIME

A-65718-1
SN-1414
E-3275

APPENDIX

Data On Individual TX-0 Circuits

Inverter

1) Uses: Logical inverter and voltage amplifier. When placed in series, gives OR circuit for ground in, -3 out. When placed in parallel, gives AND circuit for ground in, -3 out.

2) Input: Voltage level at ground or -3 volts. Input current required: 1.1ma.

3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current at -3 volts: 3.5 ma. can drive maximum of 3 emitter followers or two inverters. Load capacitance for 0.1 μsec fall time: 75 uuf. Delay: 30mμsec.

4) Restrictions: When turned off, collector voltage must not exceed -4 volts. Maximum of two inverters in series. Maximum of 2 inverters in parallel for 5 mcps operation.

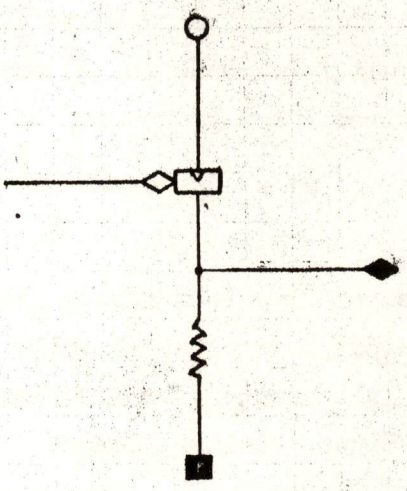
5) Power required: 5.5ma at -10v.

0.12 ma. at +10v.

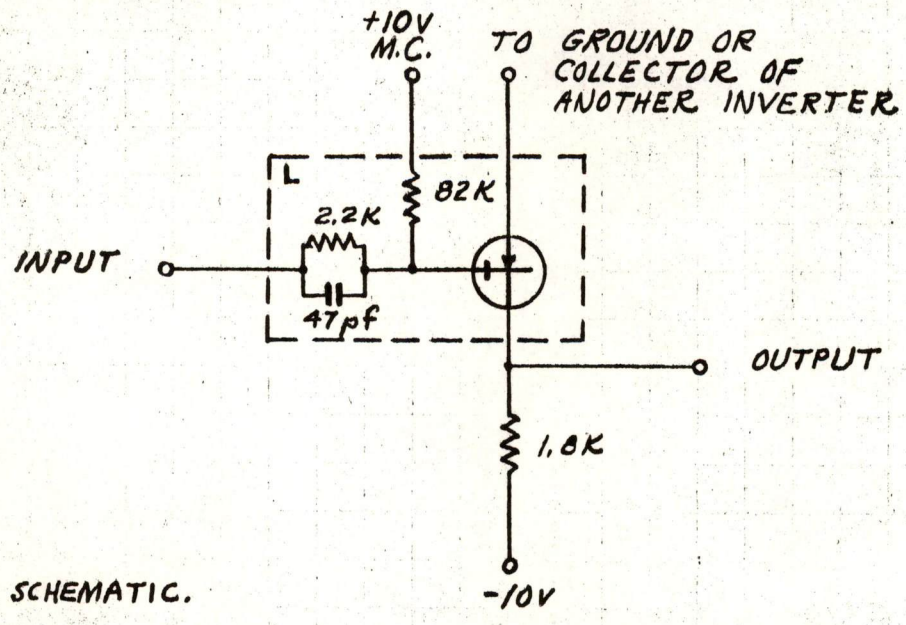
6) Marginal checking: Vary +10 volt positive bias on base.

7) Plug-in units used: L or M.

INVERTER.



8) BLOCK SCHEMATIC.



9) CIRCUIT SCHEMATIC.

EMITTER FOLLOWER

1) Uses: Current amplifier. When placed in parallel with common load resistance gives AND circuit for ground in, ground out.

2) Input: Voltage level at ground or -3 v. Input current required: Load current +3 ma. Input current will be from 0.5 to 1.8 ma.
6

3) Output: Same polarity as input. Voltage level at +0.3 v. or -2.9v. Maximum output current at -3 v.: 8 ma. Can drive maximum of 8 emitter followers or 2 inverters, providing output current does not exceed 8 ma. Two emitter followers in parallel (R=2K to +10 v.) can drive one emitter of pulse transistor with no delay or one emitter of level transistor with 90 mμsec. rise time. Maximum output current at ground in this latter type of operation: 5 ma. Load capacitance for 0.1 μsec rise time: 120 uuf.

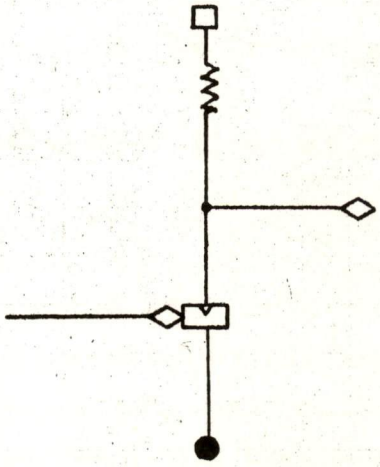
4) Restrictions: Not more than 10 emitter followers may be placed in parallel for 5 mcps operation. Emitter followers cannot be placed in series. Only 2 emitter followers may be cascaded provided that the first emitter follower is saturated from -10 volts. Otherwise, emitter followers may not be cascaded.

5) Power required: 8 ma. at -3 v. (maximum)
3.3 ma. at +10 v.

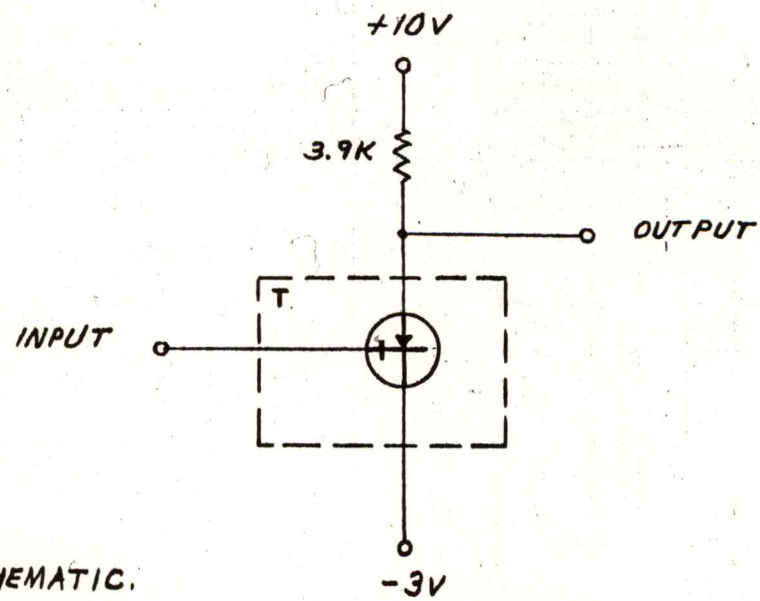
6) Marginal checking: None.

7) Plug-in units used: T or E or A.

EMITTER-FOLLOWER



8). BLOCK SCHEMATIC



9). CIRCUIT SCHEMATIC.

Register Driver

1) Use: Gating circuit for pulses for pulse inputs to flip-flops.

2) Level input: Ground level for passing pulse. -3 volt level for no pulse output. Level input current required: 2.2 ma.

3) Pulse input: -3.4 volt 80 to 100 musec pulse. Input pulse current equal to output pulse current.

4) Output: -3 volt 80 to 100 musec. pulse. Pulse amplitude equals input amplitude minus transistor drop. Drop less that 0.5 volt. Maximum pulse current: 30 ma. Can drive maximum of 10 pulse bases. Set-up delay: about 20 musec.

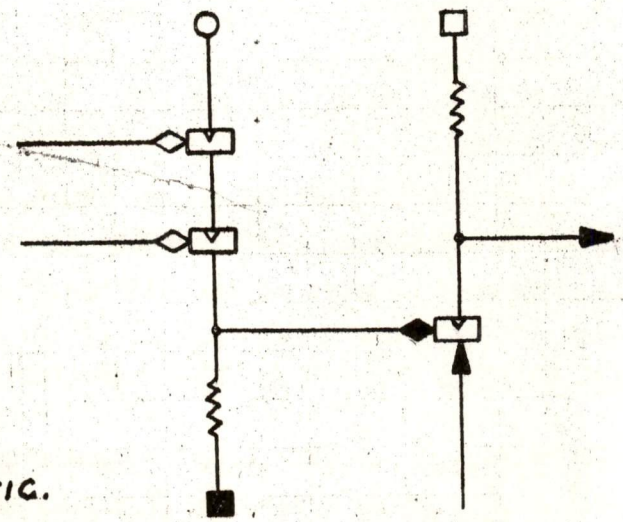
5) Restrictions: Two register drivers driven from the same input gate will drive maximum of 20 bases. Up to 10 register drivers may be placed in parallel with different gating to form a 10-way OR circuit for pulses. Placing up to 10 emitter follower gates in parallel before the register driver gives a 10-way AND circuit for pulses.

6) Power required: 6.6 ma. at -10 v.
35 ma. at +10 v.

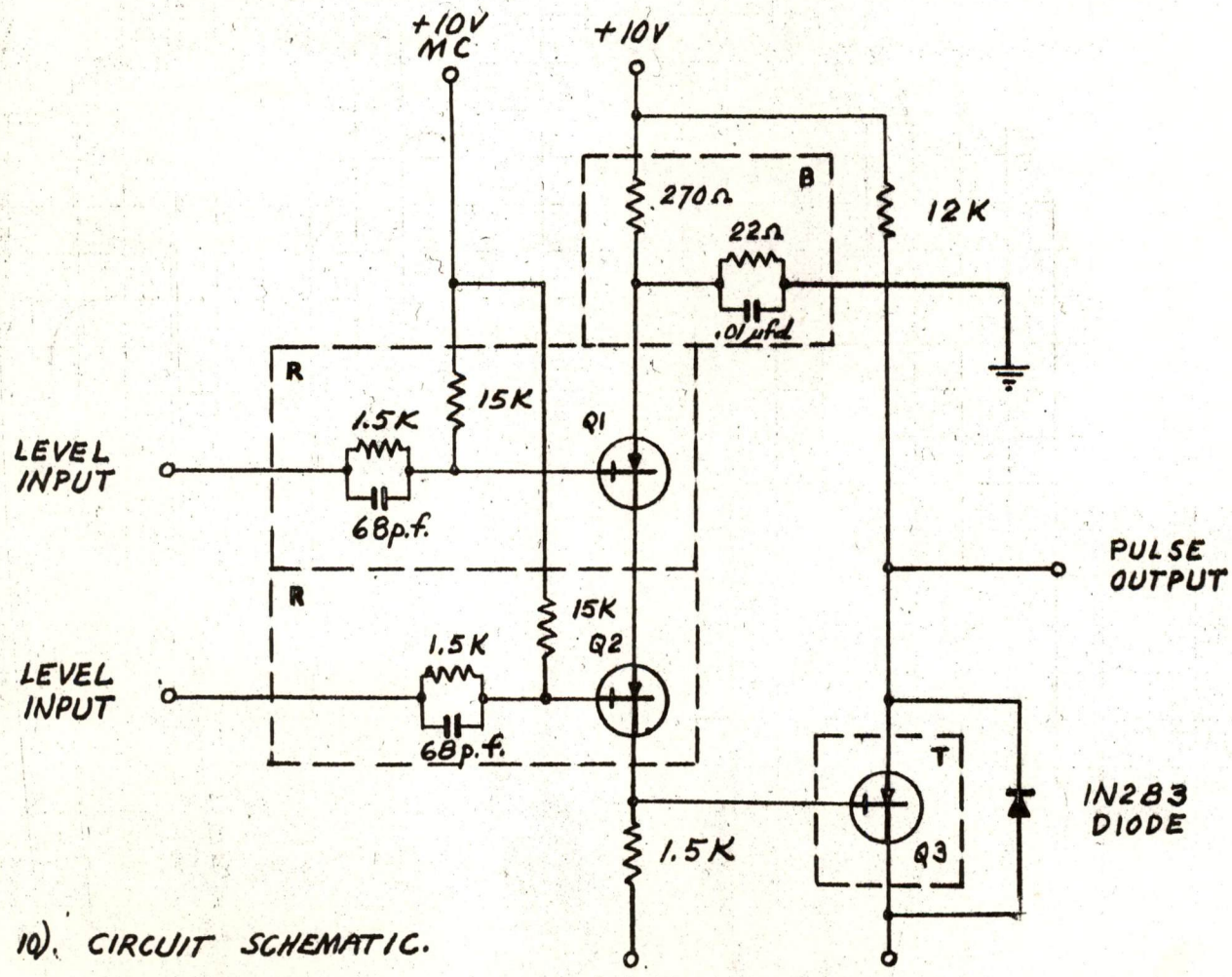
7) Marginal Checking: Vary +10 volt positive bias on inverter bases.

8) Plug-in units used: 1 or 2 R, B, T or E or A.

REGISTER DRIVER.



9). BLOCK SCHEMATIC.



10). CIRCUIT SCHEMATIC.

Pulse and Steering Gates

1) Use: Provide pulses to complement flip-flop.

2) Pulse input: -3 volt 80 to 100 μsec. pulse. Pulse current required: Maximum of 3 ma.

3) Level inputs: Voltage level at ground on one input, -3 volts on the other, coming from the outputs of the flip-flop to be complemented. Input current required to each base at -3 v.: 0.67 ma.

4) Output: Positive pulse up to ground. Will complement one flip-flop.

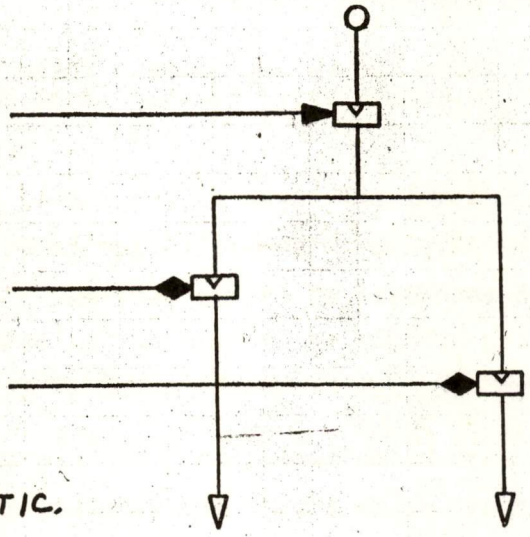
5) Restrictions: There must be no more than 3 transistors in series, including gating level input, pulse input, and steering gate. Up to 15 gates may be placed in parallel on one side of flip-flop input.

6) Power required: 0.24 ma. at +10 v.

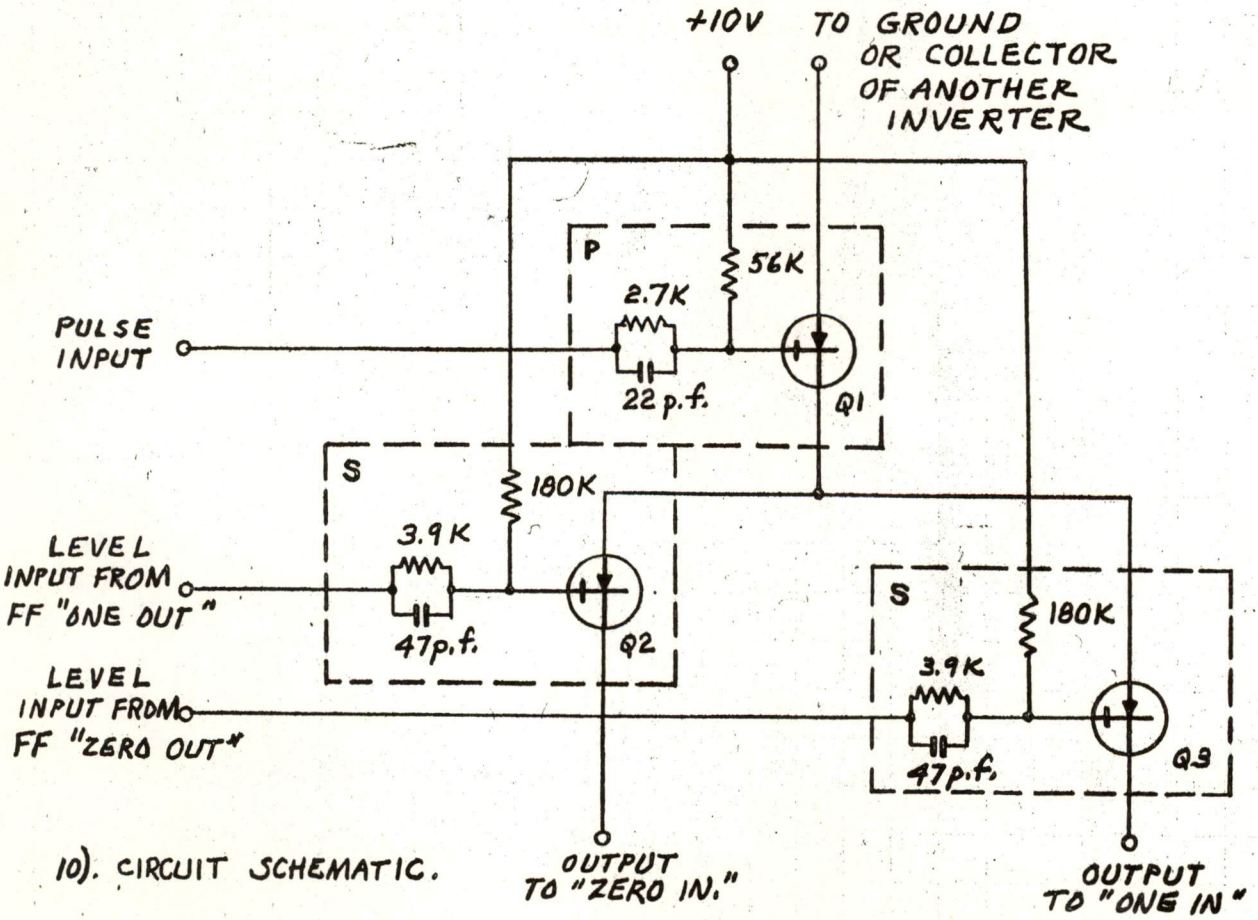
7) Marginal checking: Vary +10 volt positive bias on bases.

8) Plug-in units used: 1P, 2S.

PULSE & STEERING GATES.



9). BLOCK SCHEMATIC.



10). CIRCUIT SCHEMATIC.

Inverting Cascode

1) Uses: Power amplifier and level driver.

2) Input: Voltage level at ground or -3 volts. Input current required: 2.2ma.

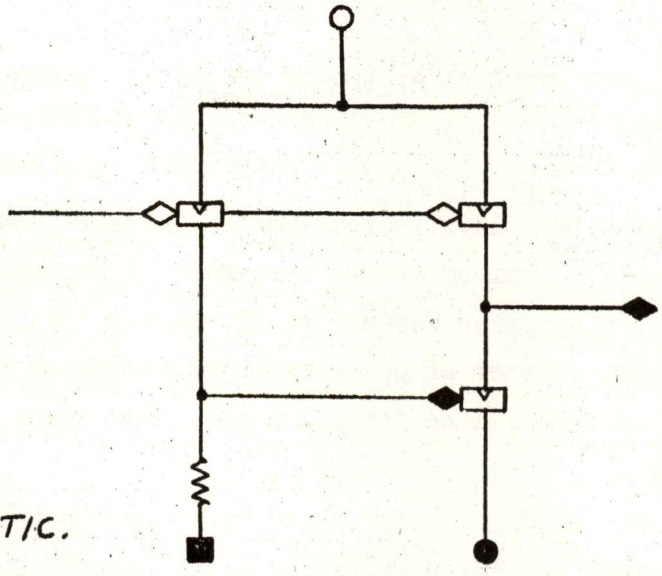
3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current: 12 ma. at -3 v.: 4 ma. at ground level. Can drive maximum of 12 emitter followers or 8 inverters, and one emitter of pulse or level transistor on the same time pulse. Load capacitance for 0.1 μ sec. rise time: 420 uuf. Delay = 30 mμsec.

4) Power required: 12 ma. at -3 v.
5.5 ma. at -10v.
0.24 ma. at +10 v.

5) Marginal Checking: Vary +10 volt positive bias on bases.

6) Plug-in units used: L,C

INVERTING CASCODE.



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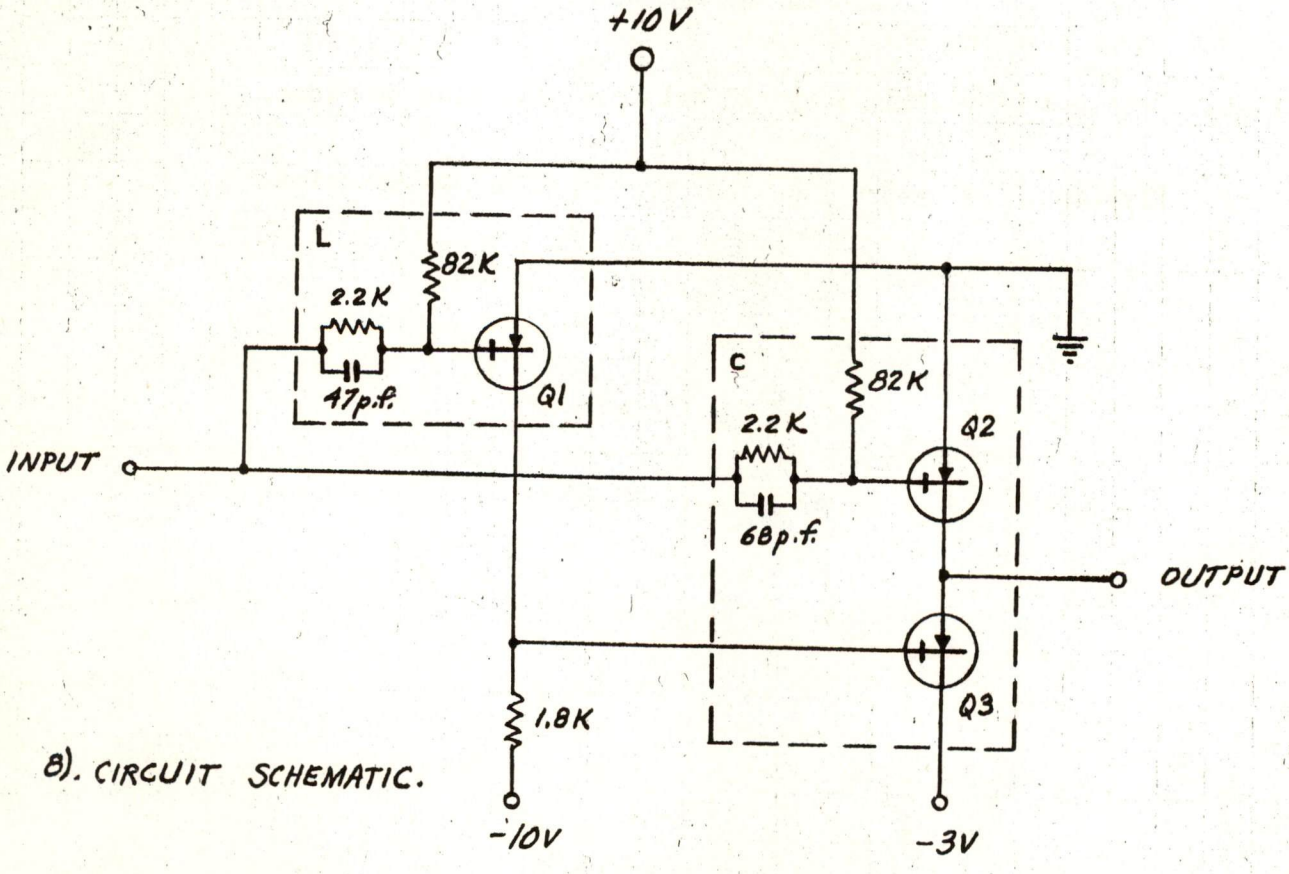


8). CIRCUIT SCHEMATIC.

Cable Driver (Inverting Cascode)

1) Use: To provide level input into 160 ohm cable, which drives transistor base.

2) Input: Voltage level at ground or -3 volts, from emitter follower gate or inverter gate. Input current required: 2.2 ma.

3) Output: Opposite polarity from input. Voltage level at ground or negative level less than -3 volts determined by voltage drop through 130 ohm resistor in series with cable. Maximum output current: 12 ma. Will drive maximum of 100 feet of K109 coaxial cable (Z_o = 160 ohms; D.C. resistance = 0.7 ohms/ft.)

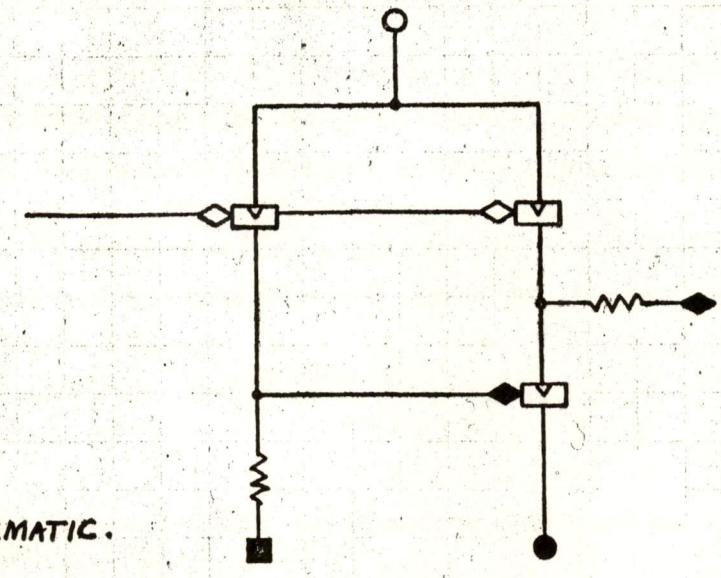
4) Restrictions: No termination should be added at end of cable, as cable is terminated in a resistance of 130 ohms in series with the input end at the cable driver.

5) Power required: 12 ma at -3 volts.
5.5 ma. at -10 volts.
0.24 ma. at +10 v.

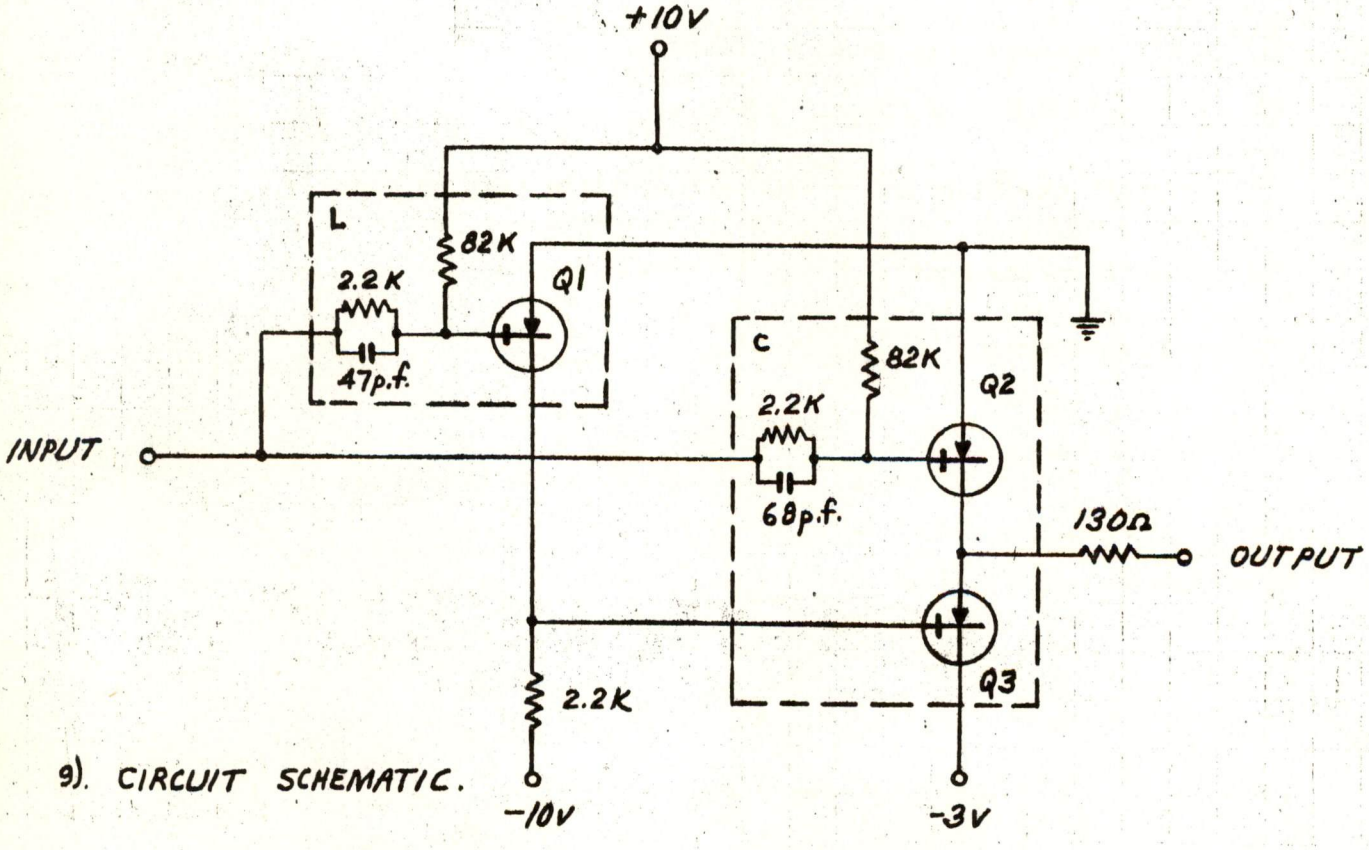
6) Marginal checking: Vary +10 volt positive bias on bases.

7) Plug-in units used: L,C.

CABLE DRIVER.



8). BLOCK SCHEMATIC.



9). CIRCUIT SCHEMATIC.

Flip-Flop

1) Use: To provide logical levels at ground or -3 volts.

2) Input: Positive pulse up to ground from output of pulse gate.

3) Output: One side at ground: other side at -3 volts. Output circuit is inverting cascode. (See Inverting Cascode for specifications) Logical delay before start of rise or fall: 90 to 100 mμsec.

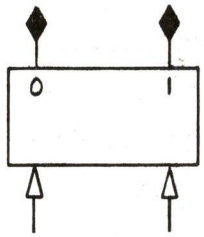
4) Restrictions: Maximum complement rate: 5 mcps.

5) Power required: 18 ma. at -3 volts (maximum)
12 ma. at -10 volts
1.8 ma. at +10 volts.

6) Marginal checking: Vary +10 volt positive bias on inverter bases by varying +10 volt input to "MCA" or "MCB".

7) Plug-in unit used: Flip-flop plug-in unit.

8) Logical symbol



9) Circuit drawing. See Figure 13.

Note on Resistance Values

Inverters

All load resistance to -10 volts are 1.8K, with the following exceptions:

2.2K for inverter in Cable driver cascode, for inverter when followed by two other inverters, and for Accumulator carry chain.

1.5 K for inverters in register drivers.

Normal positive bias resistance for RC input of 2.2 K and 47 uuf is: 82 K. 39 K is used for level input to MBR from memory frame, toggle switch storage, and PETR, and when the level transistor (L unit) in the Program Counter is driven from emitter followers.

Emitter Followers

All load resistance to +10 volts are 3.9 K with the following exception:

2 K is used when two emitter followers are used in parallel to drive another emitter of a pulse or level transistor. In this case 47 ohm resistors are used in the emitters of the emitter followers as current sharing resistances.

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SUBJECT: TRANSISTOR LOGIC IN TX-0

To: Distribution List

From: Richard C. Jeffrey

Date: September 5, 1956

Approved: W A Clark
W. A. Clark

Abstract: This note is a supplement to 6M-4561, "TX-0 Circuitry". A simple analogy between transistors and switches is used to explain the operation of the transistor networks in TX-0. (material in this note will apply with minor changes to TX-2 as well.) Conventions for the use of arrowheads (—►, —▷, —◆, —◇) in TX-0 and TX-2 logical schematic diagrams are explained. An inventory of TX-0 basic circuits is appended for use in logical design

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1. INTRODUCTION

From the point of view of someone trying to design new basic circuits, transistors are rather complicated devices; but for purposes of understanding what an existing basic circuit or network of basic circuits does, transistors may be thought of simply as switches (sec. 2). This simplified model of the transistor gives an entirely reliable interpretation of the "logical schematic" diagrams of TX-0 (and of those which are being prepared for TX-2). The simplified model is also a useful guide for the logical designer: under certain restrictions, any network built from the basic circuits listed in the appendix will behave in the manner predicted by the switch-analogy. The restrictions are indicated in the appendix to this note and, in greater electronic detail, in 6M-4561, "TX-0 Circuitry". It should be noted that no attempt is made here to give a complete or even an entirely accurate description of how transistors work. What is provided is rather a rule of thumb, as simple as possible, which gives correct results. The rule is sometimes right for the wrong reasons, but it is never wrong.

In addition to the general exposition of transistor logic, the various special notational devices used in TX-0 and TX-2 block schematics are explained.

2. TRANSISTORS AS SWITCHES

Figure 1 (fold-out, last page) is an example of a "logical schematic" diagram. Working from the logical schematic one can reconstruct and wire up the actual circuit, which contains some additional resistors, condensers, and voltage sources. (For details, see 6M-4561, "TX-0 Circuitry.") In the diagram,

' ■ ' stands for a -10 volt source,

' ● ' stands for a -3 volt source,

' □ ' stands for +10 volt source, and

' ○ ' stands for 0 volt source (ground).

For our purposes it is sufficient to remember that <u>filled-in squares or circles</u> are negative voltage sources, and hollow squares or circles are non-negative.

In Figure 1, '  ' stands for a transistor: the short side of the rectangle represents the base, and the long sides represent the emitter and collector. But for our purposes we can imagine that <u>each transistor is a switch which closes when the base is negative, and is open otherwise</u>.* Let us use a solid diamond (—◆) to indicate negative points, and hollow diamonds (—◇) to indicate points which have 0 or positive voltage.

*Throughout this note, "transistor" means specifiaclly <u>p-n-p transistor</u> (the only kind currently used in TX-0). n-p-n transistors have opposite characteristics from p-n-p; specifically, thought of as switches, they close when the base is ◇ and open when the base is ◆.

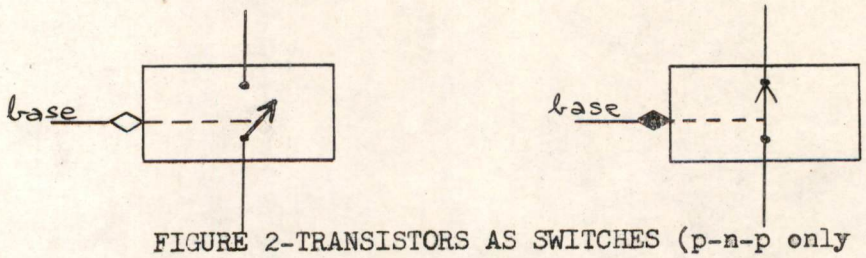


FIGURE 2-TRANSISTORS AS SWITCHES (p-n-p only *)

The function of the resistors (-∿∿-) in Figure 1 is simply this: a point like u which is connected to a negative source through a resistor will be ◆ unless it is forced to become ◇ by a direct connection to a ◇ source. Thus if point a in Figure 1 is ◆, the transistor "switch" between u and ○ closes and thus forces u to become ◇. Similarly, a point like x, which is connected through a resistor to a ◇ source will be ◇ unless it is forced to become ◆ by direct connection to a ◆ source. In this case the direct connection might be via any one of the three transistors between x and ●; for example, if u is ◆, x will become ◆.

3. THE ARROWHEAD NOTATION

To get an overall view of the action of a transistor net it is convenient to break it up into basic circuits as indicated by the broken lines in Figure 1. The behavior of each basic circuit can be analyzed separately and then combined with the rest to get the total picture. Thus in the basic circuit at the left, u is ◆ if and only if a is ◇, and, saying the same thing in a different way, u is ◇ if and only if a is ◆. These statements can be written briefly as "equations":

$$u\blacklozenge = a\diamond \qquad (1)$$

$$u\diamond = a\blacklozenge \qquad (1')$$

where '=' is shorthand for "if and only if".

The basic circuit at the right in Figure 1 is somewhat more complicated: v is ◆ if and only if c is ◇ or both d and e are ◇. Here the word "or" is to be understood in the inclusive sense: and/or. Using the sign '+' for or in this sense, and using '.' for and, the statement can be abbreviated as:

$$v\blacklozenge = c\diamond + (d\diamond \cdot e\diamond) \qquad (2).$$

The companion statement, to the effect that v is ◇ if and only if c is ◆ and in addition either d or e (or both) are ◆, is:

$$v\diamond = c\blacklozenge \cdot (d\blacklozenge + e\blacklozenge) \qquad (2').$$

*See footnote page 2

In summary, the shorthand is:

'=' means <u>if and only if</u>,

'+' means <u>or</u> in the inclusive sense ("and/or").

'.' means <u>and</u>,

'a◆', 'v◇', etc. mean <u>a is negative, v is non-negative</u>, etc.

The basic circuit in the middle of Figure 1 can be described:

$$x◆ = u◆ + b◆ + v◆ \qquad (3)$$

$$x◇ = u◇ . b◇ . v◇ \qquad (3'),$$

i.e., x is◆ if and only if u or b or (at least one) are◆, and x is◇ if and only if u and b and v are all◇.

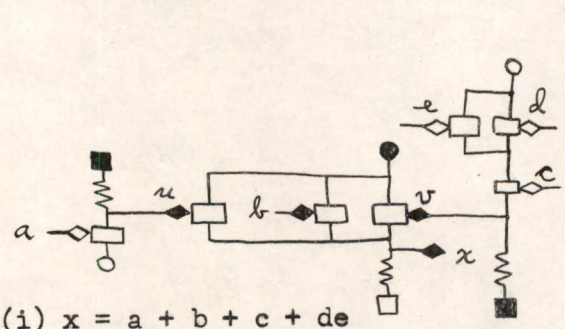
Using (1) and (2) we can eliminate 'u◆' and 'v◆' from (3) to get a single equation which expreses the output directly in terms of the inputs:

$$x◆ = a◇ + b◆ + c◇ + (d◇ . e◇) \qquad (4).$$

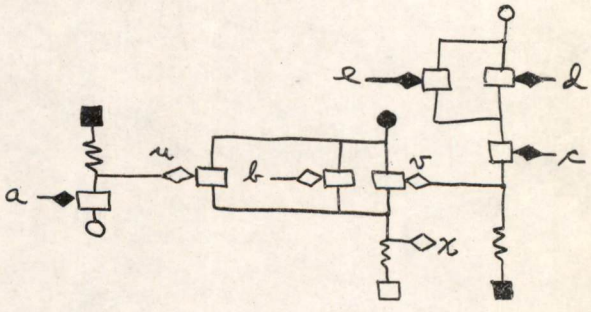
Similarly using (1') and (2') to eliminate 'u◇' and 'v◇' from (3') we get an equivalent description in terms of x◇:

$$x◇ = a◆ . b◇ . c◆ . (d◆ + e◆) \qquad (4').$$

Now to make these equations less cumbersome, we move the diamonds out into the diagram; Figure 3 shows two ways of doing this, corresponding to equations (4) and (4').



(i) x = a + b + c + de
(see equation (4))



(ii) x = abc(d + e)
(see equation (4'))

FIGURE 3 - TWO DISTRIBUTIONS OF ARROWHEADS FOR THE NET OF FIGURE 1

The simplified equation (i) above might be read: "x is as shown in the accompanying diagram (namely, ◆◇) if and only if a, or b, or c, or both d and e, are as shown there (i.e., if and only if a is◇ or b is◆ or ...)." The equation by itself is ambiguous; the diamonds which fix its meaning

must be gotten from the diagram. Similarly equation (ii) must be read in conjunction with its diagram.

In case it is desired to write equations which will be unambiguous without the aid of diagrams, one can indicate the kind of diamond associated with each letter by some such shorthand as:

'x' means x◆

'$\bar{x}$' means x◇.

Then equation (4) becomes

$$x = \bar{a} + b + \bar{c} + \bar{d}\,\bar{e} \qquad (5)$$

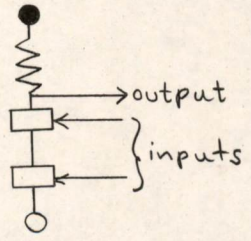
And equation (4') becomes

$$\bar{x} = a\bar{b}c(d + e) \qquad (5').$$

Equations such as (5) and (5') can be manipulated according to the ordinary rules of Boolean algebra, interpreting '$\bar{x}$' as the complement of x. (See R. K. Richards, Arithmetical Operations in Digital Computers, Chapters I and II, or engineering note E-458-1, "The Use of Boolean Algebra in Logical Design".) In cases where our symbols for and ('.') and or ('+') may be confused with the arithmetical product and sum, the following notation is suggested: '&' for and, 'v' for or, and '≡' or '⇔' for if and only if. For example, equation (5) becomes '$x \Leftrightarrow \bar{a} v b v \bar{c} v (\bar{d}\&\bar{e})$' in this notation. The expressions '$\sim x$', '$-x$' and 'x'' are often used instead of our '$\bar{x}$'.

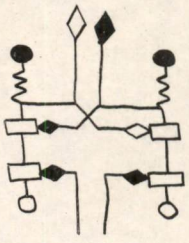
4. FLIP-FLOPS AND AUXILIARY DEVICES

The basic flip-flop is a feedback net consisting of two "series inverter" circuits of this sort:

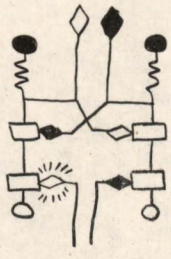


The inverter's output is◆unless both inputs are◆. The delay between a change in the input voltages and the resulting change in the output is about 35 musec.

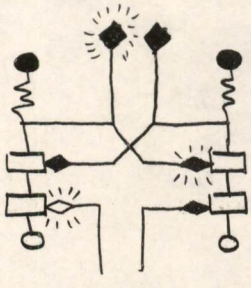
As shown in Figure 4, the output of each series inverter is connected to one of the intputs of the other. Normally, both inputs are ◆, and in this condition (see Figure 4 (i) and (v)) the flip-flop "remembers", i.e., one of the outputs holds the other in the◇condition, and the second holds the first in the◆condition. To "set" the flip-flop to the opposite configuration (i.e., to complement it), the appropriate input is grounded for a period of 80-90 μsec. (Ground the input on the side where the output is◇.)



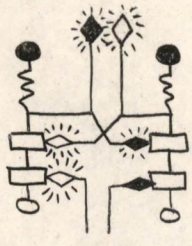
(i) Initial situation. The flip-flop remains in this condition until...



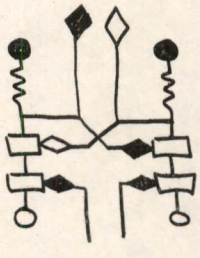
(ii) one input is grounded; but the effect is not felt at the output until...



(iii) about 35 μsec have elapsed; at this time the left output goes to ◆. The right output does not respond until.....



(iv) another 35 μsec. have elapsed; now the right output takes over the job of holding the the left at ◆. Now...

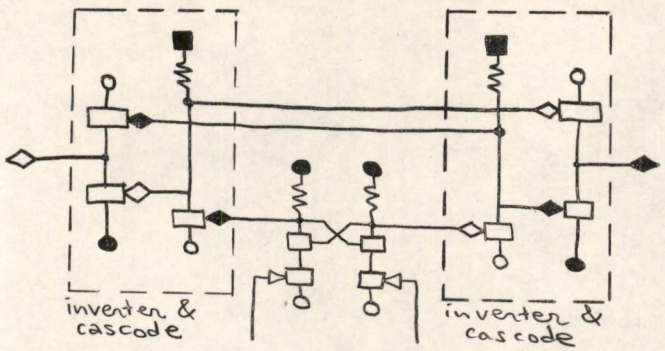


(v) the left input can be returned to ◆.

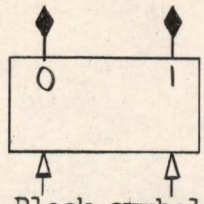
FIGURE 4 - RESETTING A FLIP-FLOP FROM THE ◇◆ CONDITION TO ◆◇.

It is important that the input remain at ◇ until situation (iv) is reached, i.e., for at least 70 μsec.; otherwise the circuit will oscillate.

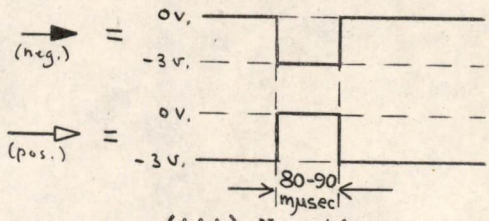
The TX-0 flip-flop consists of the circuit shown in Figure 4, together with a power amplifier at each output:



(i) Logical Schematic



(ii) Block symbol



(iii) Negative vs. positive pulses.

FIG. 5 - TX-0 Flip-Flop

The "invert-cascode" circuits invert and amplify the outputs; in the situation shown in Figure 5(i), the outputs of the basic flip-flop circuit are ◆ and ◇ , while the corresponding outputs from the amplifiers are ◇ and ◆ .

The flip-flop inputs are "positive" pulses, i.e., they are normally at the ◆ level, but are brought to ◇ for a period of 80-90 musec, to set the flip-flop. Pulses (—►or—▷) are distinguished from levels (—◆or—◇) by the shape of arrowheads; the two sorts of pulses are distinguished by solid or hollow arrowheads as in Fig. 5(iii).

We speak of flip-flops as "holding a 0" ("being in the '0' state") or "holding a 1" ("being in the '1' state"). What does this mean, physically? The physical flip-flop is a symmetric circuit with two output terminals. One of the terminals has a "0" stamped beside it, and the other has "1". Logically it is irrelevant, which is stamped "0" and which "1". It is also an arbitrary decision, whether the flip-flop is said to "hold a 0" when the output configuration is ◆ ◇ or when the configuration is ◇ ◆ . All that matters is that whichever of these configuration is identified with the "0" state the other must be identified with the "1" state.

A wiring diagram pictures the physical situation by showing, for example, which points are connected to the flip-flop output terminal stamped "1". But a logical schematic diagram shows the "logical" situation by showing, for example, which points are ◆ and which are ◇ when the flip-flop holds a 1. In such diagrams, lines going to the side marked "1" (for example) need not correspond to wires connected to the output terminal of the physical flip-flop which is stamped '1'. Instead, the convention illustrated in Fig. 6 is followed.

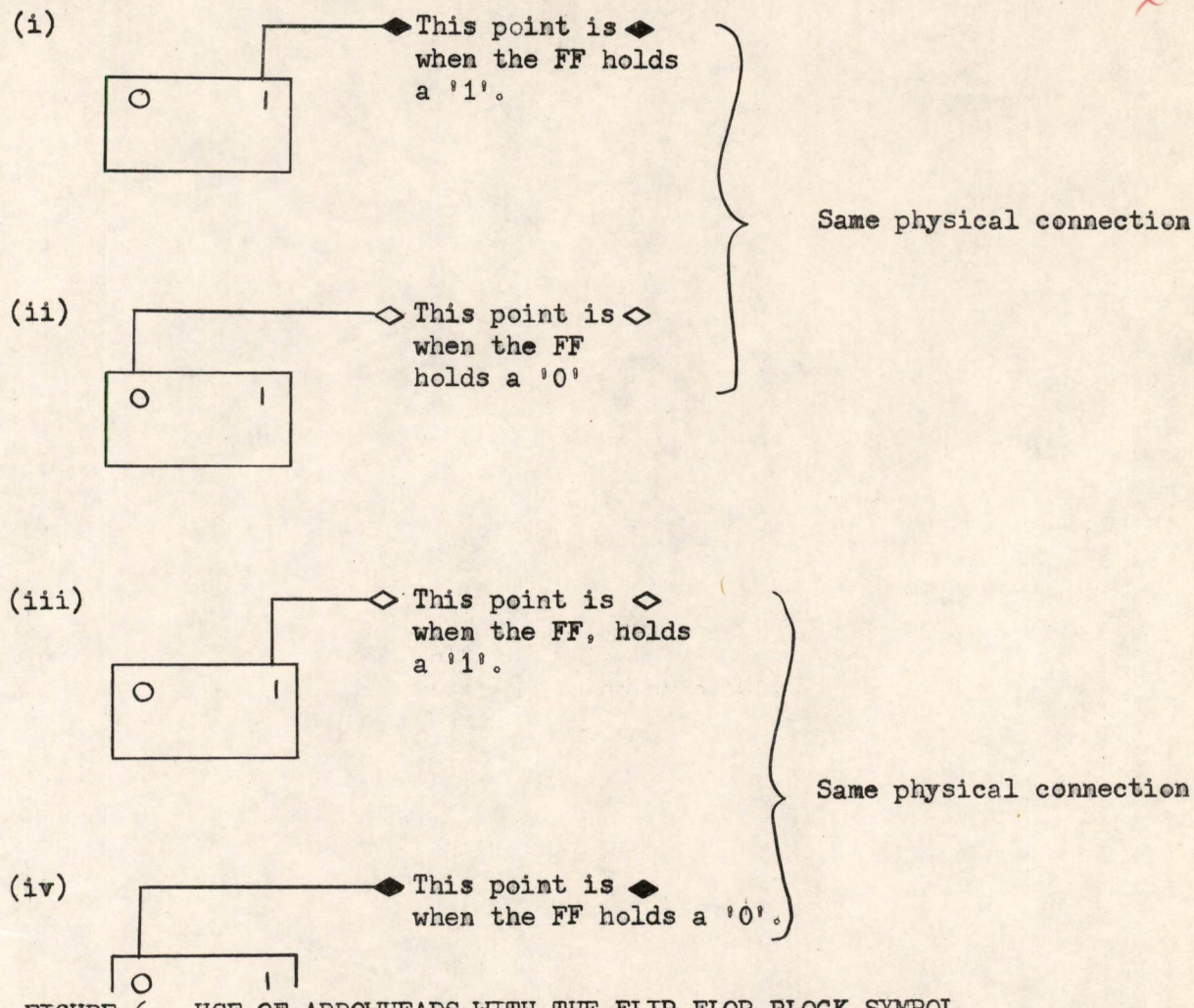
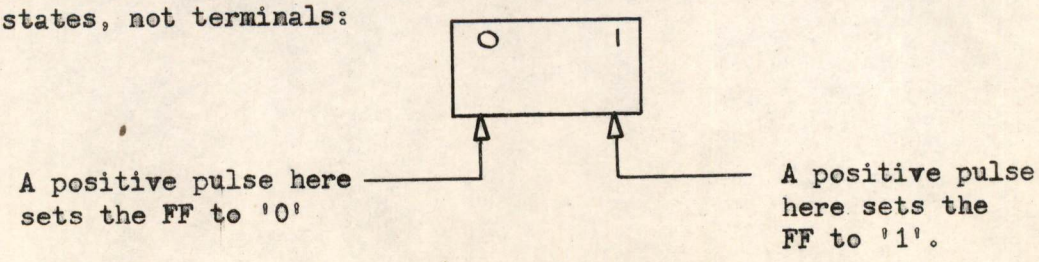


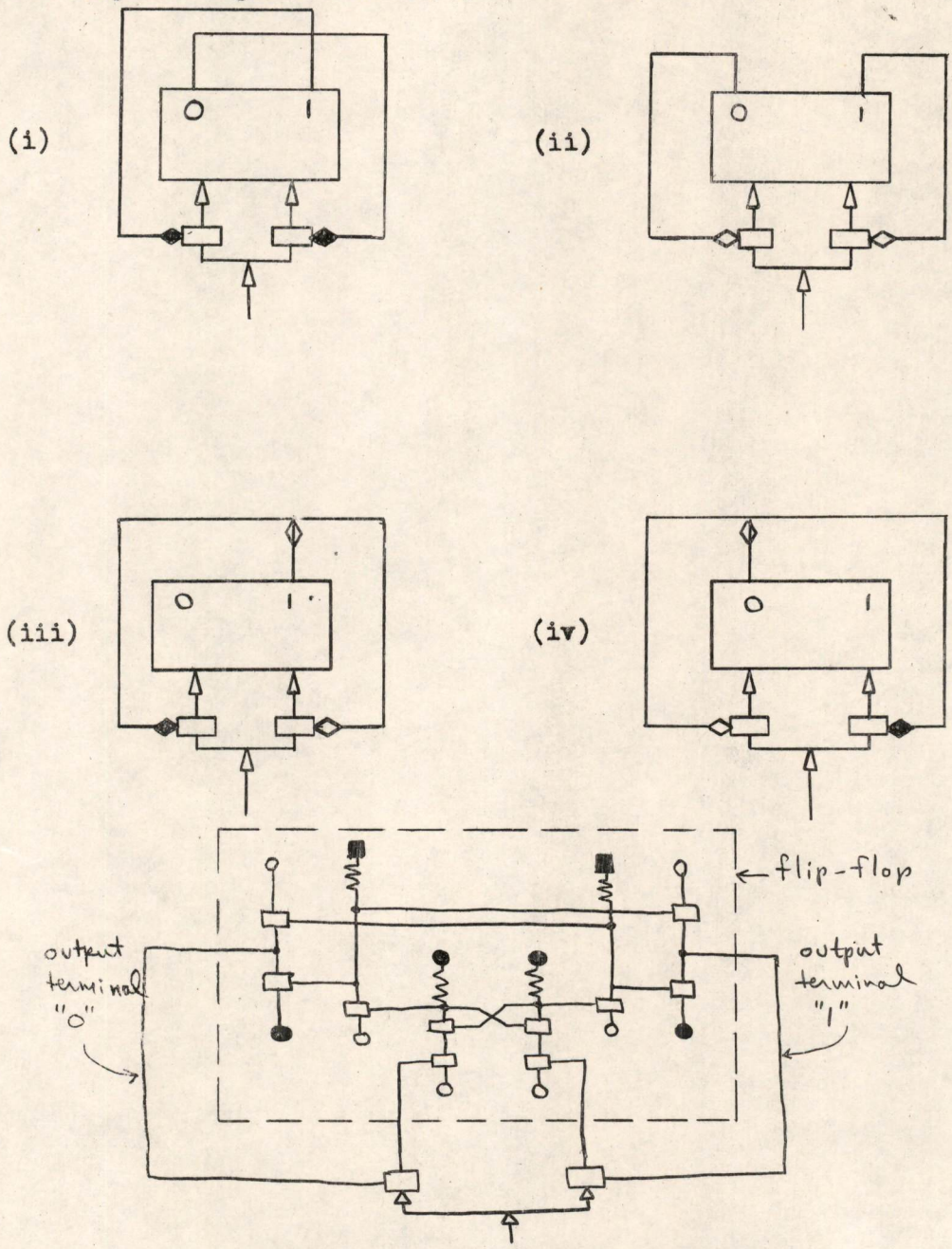
FIGURE 6 - USE OF ARROWHEADS WITH THE FLIP-FLOP BLOCK SYMBOL

Note that physically, the output wires indicated in Figure 6 (i) and (ii) go to the same terminal of the flip-flop, i.e., the terminal which is ◆ when the flip-flop holds a '1' and which is therefore ◇ when the flip-flop holds a '0'. In the physical flip-flop this terminal might be stamped "1" or might be stamped "0" - the logical schematic would be the same in either case. Similarly, the output wires in (iii) and (iv) would both be wired to the terminal <u>opposite</u> the one used for (i) and (ii).

Like the outputs, the input lines to a flip-flop block symbol refer to states, not terminals:



To illustrate the use of this symbolism, Figure 7 (i) through (iv) shows four different ways of drawing the circuit for which (v) is the complete logical schematic.



(v) COMPLETE LOGICAL SCHEMATIC

FIGURE 7 - ALL 5 WOULD BE WIRED UP IN THE SAME WAY

Note the difference between the complete logical schematic (v) and the schematics which use the block symbol for the flip-flop. In (v) the output terminals are shown, whereas in (i) through (iv), states are shown instead. In (v), it is not necessary to tag the flip-flop outputs (terminals) as ◆ or ◇; but (i) through (iv) would lose their meaning if the diamond arrowheads were erased, since it would then be impossible to tell which state of the flip-flop makes a point ◆ or ◇. (However, the split diamonds in (iii) and (iv) could be dropped; they are included only as an aid to the eye in identifying the input line at a junction of lines.)

The reason of devoting so much space to our convention for the use of arrowheads at flip-flop outputs is that it differs from the usual convention. It would be more in keeping with general usage to regard this: 

as simply an abbreviation for the circuit enclosed in broken lines in Figure 7 (v). Then the two lines at the top of the box marked "FF" would represent output terminals, and the two styles of diamonds would be superfluous. However, the TX-0 logical schematics (and presumably those for TX-2 as well) follow the notation of Figure 6.

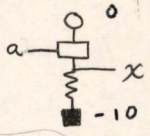
APPENDIX: INVENTORY OF BASIC CIRCUITS IN TX-0

Note on Symbolism

Most of the following diagrams are accompanied by two "equations", which describe the operation of the circuit in two different but equivalent ways. For fuller explanation of the "equations", see page 4.

I. INVERTERS (VOLTAGE AMPLIFIERS).

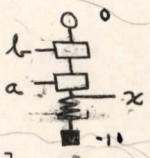
A. Simple



$x = \bar{a}$

$\bar{x} = a$

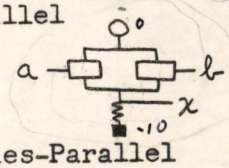
B. Series



$x = \bar{a} + \bar{b}$

$\bar{x} = ab$

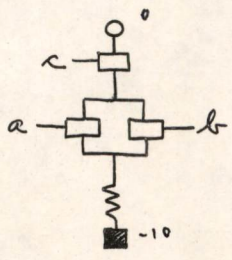
C. Parallel



$x = \bar{a}\,\bar{b}$

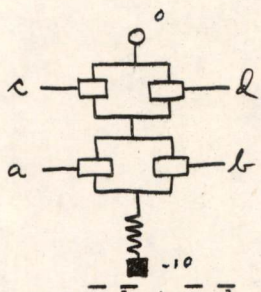
$\bar{x} = a + b$

D. Series-Parallel



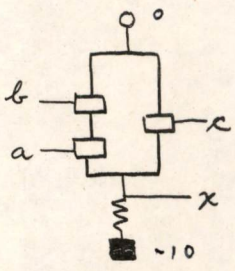
$x = \bar{a}\,\bar{b} + \bar{c}$

$\bar{x} = (a + b)c$



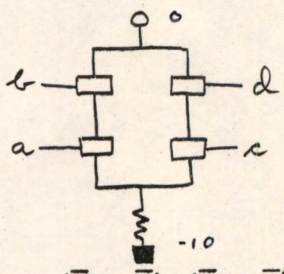
$x = \bar{a}\,\bar{b} + \bar{c}\,\bar{d}$

$\bar{x} = (a + b)\,(c + d)$



$x = (\bar{a} + \bar{b})\bar{c}$

$\bar{x} = ab + c$



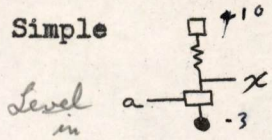
$x = (\bar{a} + \bar{b})\,(\bar{c} + \bar{d})$

$\bar{x} = ab + cd$

Restrictions: Delay ≈ 35 musec. Output (x) may not be connected to the bases of more than 3 emitter-follower transistors or more than 2 inverter transistors.

II. EMITTER - FOLLOWERS (CURRENT AMPLIFIERS)

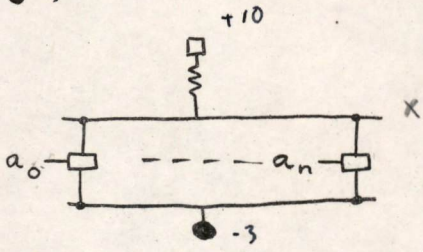
A. Simple



$x = a$

$\bar{x} = \bar{a}$

B. Parallel



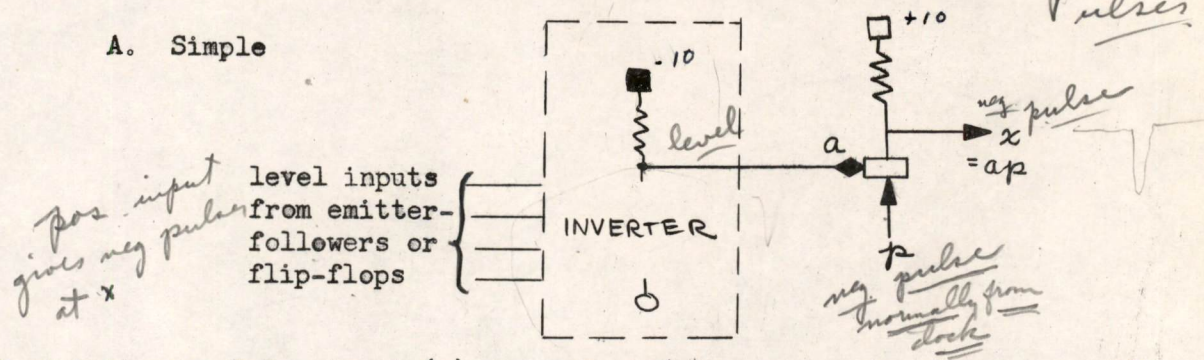
$x = a_o + \ldots + a_n$

$\bar{x} = \bar{a}_o \bullet \ldots \bullet \bar{a}_n$ $\Big\}$ $n \leq 9$

Restrictions. Delay $\approx$ 10 μsec for A. For B, delay $\approx$ 10 + 2n μsec. Output in each case can go to a maximum of 8 emitter - follower bases or 2 inverter bases. In B, x may go the emitter of a single pulse transistor (neglegible delay) or the emitter of a single level transistor with 90 μsec delay in the transition from ◆ to ◇. In A and B, x may go the base of another emitter-follower, but the output of that second emitter-follower may not in turn go to the base of a third emitter-follower.

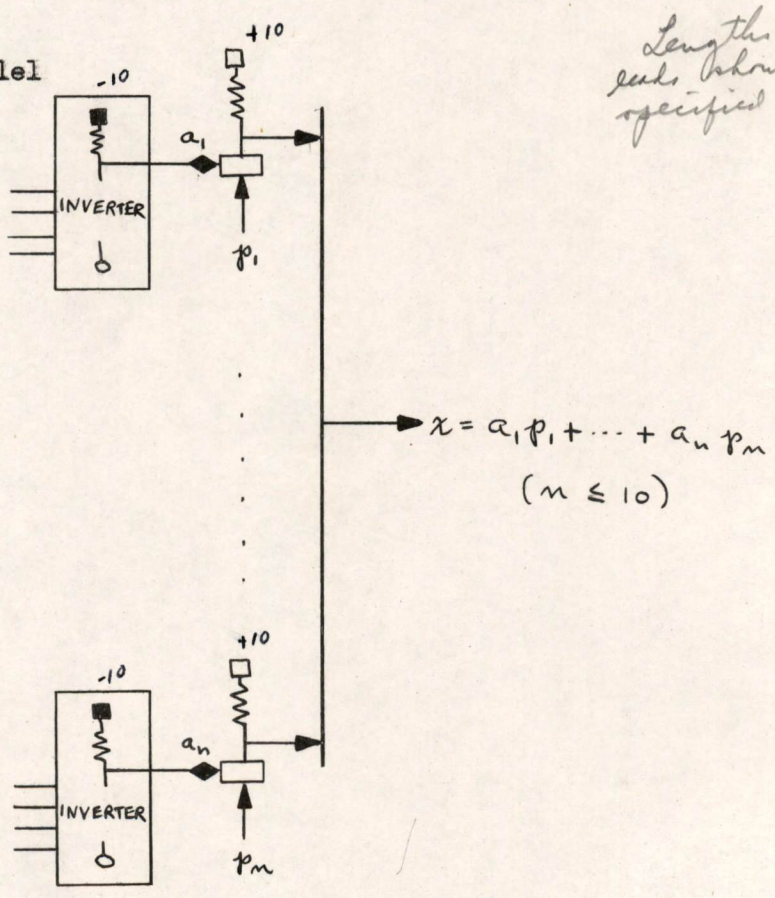
III. "REGISTER DRIVER" (GATE FOR HEAVY PULSES)

A. Simple

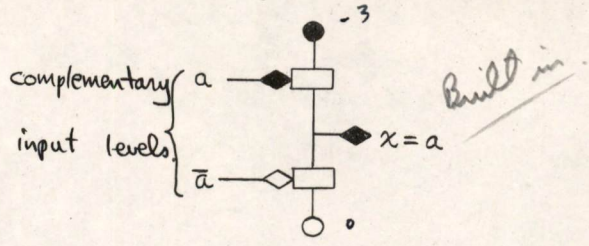


Restrictions: Pulse input (p) and output (x) are negative (i.e., normally ◇). a must be the output of an inverter (any of IA through ID). The same emitter-follower or flip-flop output may be used as a level input to at most 2 register drivers. Output (x) drives a maximum of 10 bases.

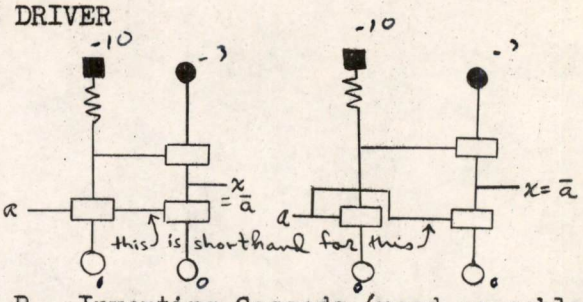
B. Parallel



IV. CASCODE (POWER AMPLIFIER) & CABLE DRIVER



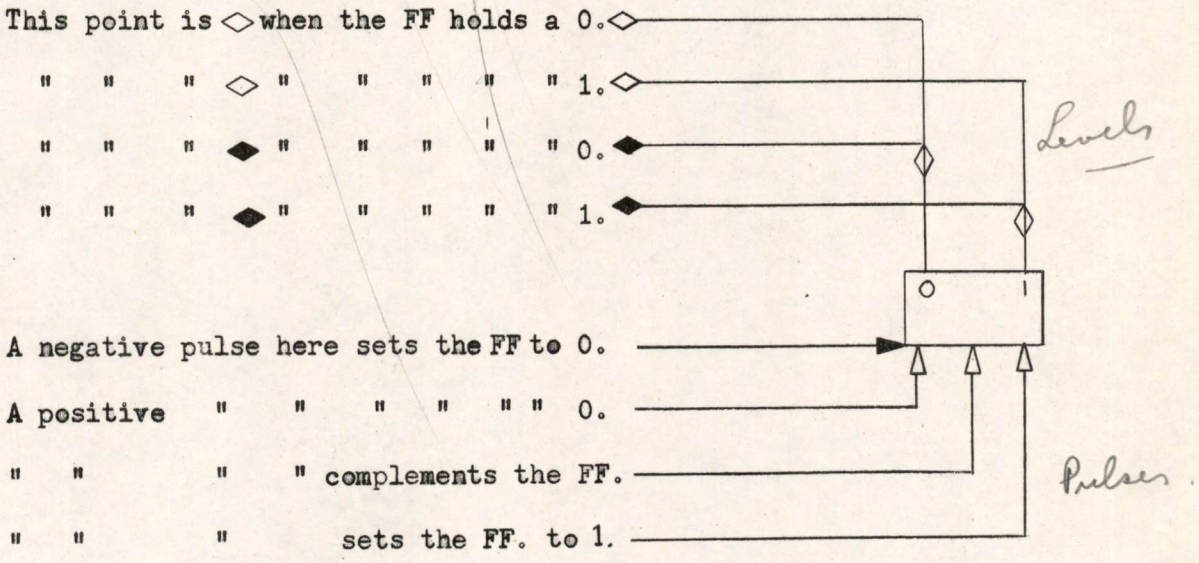
A. Simple Cascode.



B. Inverting Cascode (used as cable driver, with minor circuit modifications).

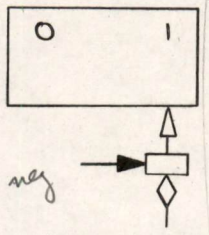
Restrictions: Inputs to cascode must be complementary (when one is ◆, the other is ◇). As power amplifier, can drive maximum of 12 emitter-follower bases or 8 inverter bases, and 1 emitter.

V. FLIP-FLOPS

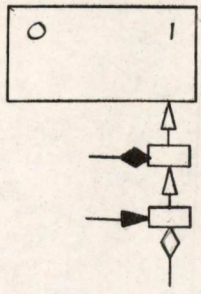


Restrictions: Delay between start of input pulse and time when output is stablilized in its new state is about .1 μsec. Only one of the input lines may be pulsed at any time. The TX-0 flip-flop lacks the negative pulse input (→) and the complement input; TX-2 flip-flops will have all 4 inputs. Output lines are driven by inverting cascodes internal to the flip-flops; therefore output restrictions are the same as in IV above.

VI. PULSE AND STEERING GATES (AT FLIP-FLOP INPUTS).

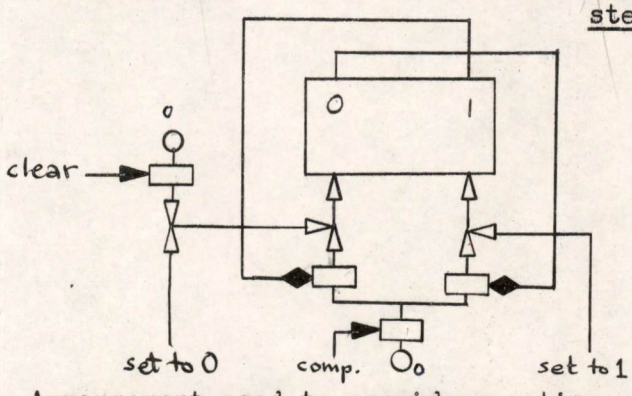


A. Pulse gate.



What is the difference between a pulse gate & steering gate? polarity?

B. Pulse gate followed by a steering gate.



C. Arrangement used to provide negative-pulse clear and complement inputs to TX-0 flip-flops.

Note: The positive-pulse set and clear input terminals to the basic flip-flop are held at ◆ unless they are forced to ◇ by being grounded through a transistor "switch".

Restrictions: No path to a ◇ source from either of the positive-pulse input terminals of the basic flip-flop may pass through more than three transistor "switches". For example, the ◇ input in B may come directly from a flip-flop output terminal, or from the output of an emitter-follower (IIA or B) or of a simple inverter (IA). This means that paths to ground from the positive-pulse complement input of a flip-flop may pass through no more than two transistor "switches". The negative clear pulse input must come directly from a register driver.

Signed: Richard C. Jeffrey
Richard C. Jeffrey

RCJ:elc
Attachment: Figure 1

GM-4571

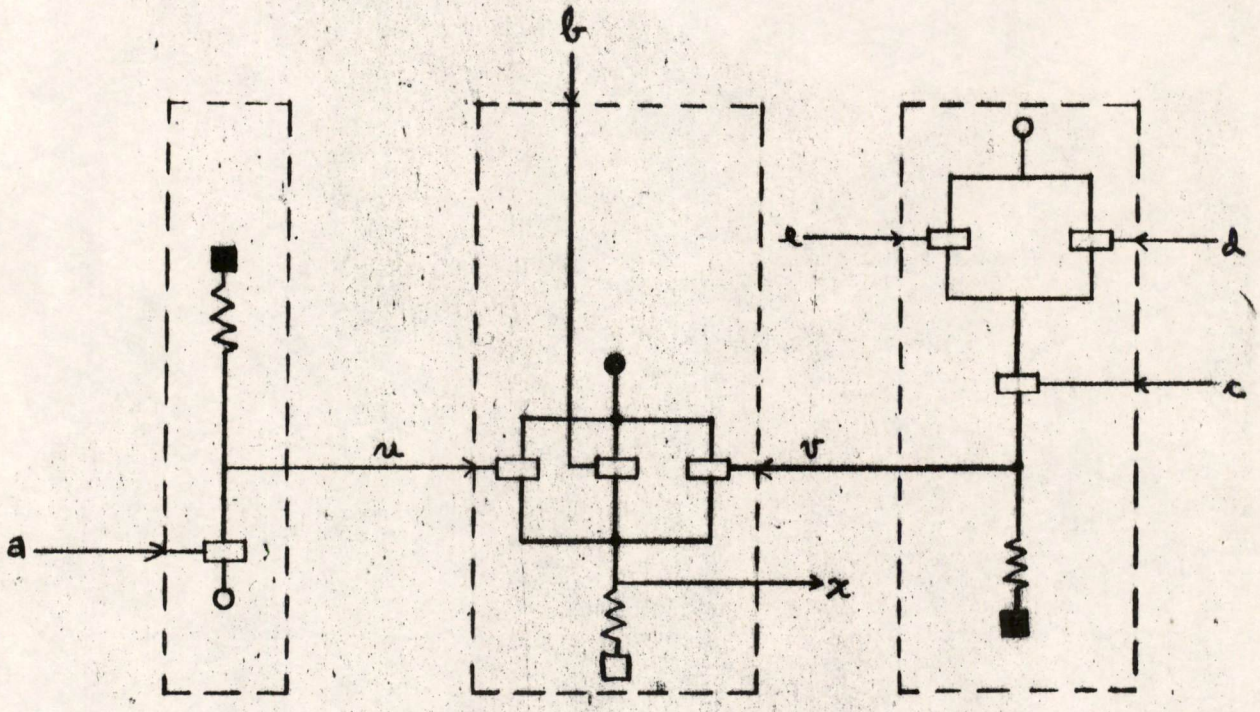


FIG 1 - LOGICAL SCHEMATIC DIAGRAM OF A TRANSISTOR NET

(fold out)

J. R. Jeffrey
B 662

Memorandum 6M-4571

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRANSISTOR LOGIC IN TX-0

To: Distribution List

From: Richard C. Jeffrey

Date: September 5, 1956

Approved: W A Clark
W. A. Clark

Abstract: This note is a supplement to 6M-4561, "TX-0 Circuitry". A simple analogy between transistors and switches is used to explain the operation of the transistor networks in TX-0. (material in this note will apply with minor changes to TX-2 as well.) Conventions for the use of arrowheads (→, ▷, ◆, ◇) in TX-0 and TX-2 logical schematic diagrams are explained. An inventory of TX-0 basic circuits is appended for use in logical design

Distribution List

*Group 63

*Jeffrey, L. R.
*Mayer, R. P.

*Indicates recipient of complete memorandum

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1. INTRODUCTION

From the point of view of someone trying to design new basic circuits, transistors are rather complicated devices; but for purposes of understanding what an existing basic circuit or network of basic circuits does, transistors may be thought of simply as switches (sec. 2). This simplified model of the transistor gives an entirely reliable interpretation of the "logical schematic" diagrams of TX-0 (and of those which are being prepared for TX-2). The simplified model is also a useful guide for the logical designer: under certain restrictions, any network built from the basic circuits listed in the appendix will behave in the manner predicted by the switch-analogy. The restrictions are indicated in the appendix to this note and, in greater electronic detail, in 6M-4561, "TX-0 Circuitry". It should be noted that no attempt is made here to give a complete or even an entirely accurate description of how transistors work. What is provided is rather a rule of thumb, as simple as possible, which gives correct results. The rule is sometimes right for the wrong reasons, but it is never wrong.

In addition to the general exposition of transistor logic, the various special notational devices used in TX-0 and TX-2 block schematics are explained.

2. TRANSISTORS AS SWITCHES

Figure 1 (fold-out, last page) is an example of a "logical schematic" diagram. Working from the logical schematic one can reconstruct and wire up the actual circuit, which contains some additional resistors, condensers, and voltage sources. (For details, see 6M-4561, "TX-0 Circuitry.") In the diagram,

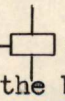
' ■ ' stands for a -10 volt source,

' ● ' stands for a -3 volt source,

' □ ' stands for +10 volt source, and

' ○ ' stands for 0 volt source (ground).

For our purposes it is sufficient to remember that <u>filled-in squares or circles</u> are negative voltage sources, and hollow squares or circles are non-negative.

In Figure 1, '  ' stands for a transistor: the short side of the rectangle represents the base, and the long sides represent the emitter and collector. But for our purposes we can imagine that <u>each transistor is a switch which closes when the base is negative, and is open otherwise</u>.* Let us use a solid diamond (—◆) to indicate negative points, and hollow diamonds (—◇) to indicate points which have 0 or positive voltage.

*Throughout this note, "transistor" means specifiaclly <u>p-n-p transistor</u> (the only kind currently used in TX-0). n-p-n transistors have opposite characteristics from p-n-p; specifically, thought of as switches, they close when the base is ◇ and open when the base is ◆.

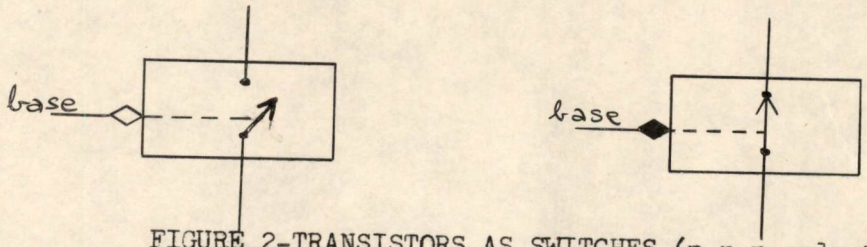


FIGURE 2-TRANSISTORS AS SWITCHES (p-n-p only *)

The function of the resistors (-ww-) in Figure 1 is simply this: a point like u which is connected to a negative source through a resistor will be ◆ unless it is forced to become ◇ by a direct connection to a ◇ source. Thus if point a in Figure 1 is ◆, the transistor "switch" between u and ○ closes and thus forces u to become ◇. Similarly, a point like x, which is connected through a resistor to a ◇ source will be ◇ unless it is forced to become ◆ by direct connection to a ◆ source. In this case the direct connection might be via any one of the three transistors between x and ●; for example, if u is ◆, x will become ◆.

3. THE ARROWHEAD NOTATION

To get an overall view of the action of a transistor net it is convenient to break it up into basic circuits as indicated by the broken lines in Figure 1. The behavior of each basic circuit can be analyzed separately and then combined with the rest to get the total picture. Thus in the basic circuit at the left, u is ◆ if and only if a is ◇; and, saying the same thing in a different way, u is ◇ if and only if a is ◆. These statements can be written briefly as "equations":

$$u\blacklozenge = a\diamond \qquad (1)$$

$$u\diamond = a\blacklozenge \qquad (1')$$

where '=' is shorthand for "if and only if".

The basic circuit at the right in Figure 1 is somewhat more complicated: v is ◆ if and only if c is ◇ or both d and e are ◇. Here the word "or" is to be understood in the inclusive sense: <u>and/or</u>. Using the sign '+' for <u>or</u> in this sense, and using '.' for <u>and</u>, the statement can be abbreviated as:

$$v\blacklozenge = c\diamond + (d\diamond \cdot e\diamond) \qquad (2).$$

The companion statement, to the effect that v is ◇ if and only if c is ◆ and in addition either d or e (or both) are ◆, is:

$$v\diamond = c\blacklozenge \cdot (d\blacklozenge + e\blacklozenge) \qquad (2').$$

---

*See footnote page 2

In summary, the shorthand is:

'=' means <u>if and only if</u>,

'+' means <u>or</u> in the inclusive sense ("and/or").

'.' means <u>and</u>,

'a◆', 'v◇', etc. mean <u>a is negative, v is non-negative</u>, etc.

The basic circuit in the middle of Figure 1 can be described:

$$x◆ = u◆ + b◆ + v◆ \qquad (3)$$

$$x◇ = u◇ \cdot b◇ \cdot v◇ \qquad (3'),$$

i.e., x is◆ if and only if u or b or (at least one) are◆, and x is◇ if and only if u and b and v are all◇.

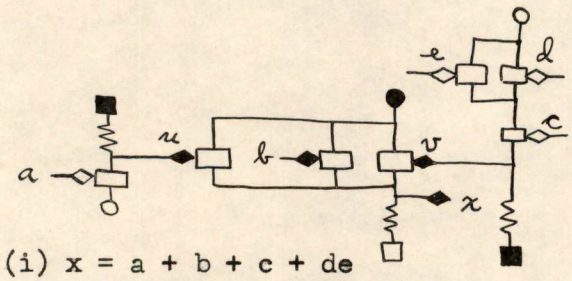
Using (1) and (2) we can eliminate 'u◆' and 'v◆' from (3) to get a single equation which expreses the output directly in terms of the inputs:

$$x◆ = a◇ + b◆ + c◇ + (d◇ \cdot e◇) \qquad (4).$$

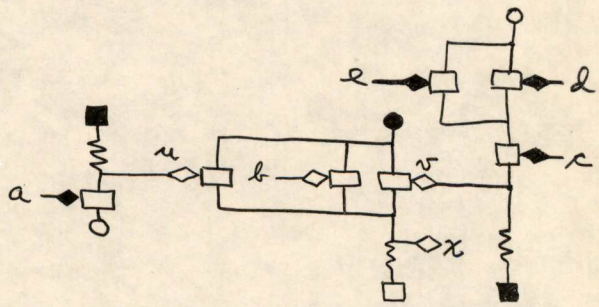
Similarly using (1') and (2') to eliminate 'u◇' and 'v◇' from (3') we get an equivalent description in terms of x◇:

$$x◇ = a◆ \cdot b◇ \cdot c◆ \cdot (d◆ + e◆) \qquad (4').$$

Now to make these equations less cumbersome, we move the diamonds out into the diagram; Figure 3 shows two ways of doing this, corresponding to equations (4) and (4').



(i) x = a + b + c + de
(see equation (4))



(ii) x = abc(d + e)
(see equation (4'))

FIGURE 3 - TWO DISTRIBUTIONS OF ARROWHEADS FOR THE NET OF FIGURE 1

The simplified equation (i) above might be read: "x is as shown in the accompanying diagram (namely, ◇) if and only if a, or b, or c, or both d and e, are as shown there (i.e., if and only if a is◇ or b is◆ or ...)." The equation by itself is ambiguous; the diamonds which fix its meaning

must be gotten from the diagram. Similarly equation (ii) must be read in conjunction with its diagram.

In case it is desired to write equations which will be unambiguous without the aid of diagrams, one can indicate the kind of diamond associated with each letter by some such shorthand as:

'x' means x◆

'$\bar{x}$' means x◇.

Then equation (4) becomes

$$x = \bar{a} + b + \bar{c} + \bar{d}\,\bar{e} \qquad (5)$$

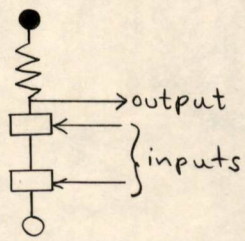
And equation (4') becomes

$$\bar{x} = a\bar{b}c(d + e) \qquad (5').$$

Equations such as (5) and (5') can be manipulated according to the ordinary rules of Boolean algebra, interpreting '$\bar{x}$' as the complement of x. (See R. K. Richards, Arithmetical Operations in Digital Computers, Chapters I and II, or engineering note E-458-1, "The Use of Boolean Algebra in Logical Design".) In cases where our symbols for and ('.') and or ('+') may be confused with the arithmetical product and sum, the following notation is suggested: '&' for and, 'v' for or, and '≡' or '⇔' for if and only if. For example, equation (5) becomes '$x \Leftrightarrow \bar{a} v b v \bar{c} v (\bar{d} \& \bar{e})$' in this notation. The expressions '∼x', '-x' and 'x′' are often used instead of our '$\bar{x}$'.

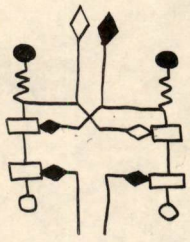
4. FLIP-FLOPS AND AUXILIARY DEVICES

The basic flip-flop is a feedback net consisting of two "series inverter" circuits of this sort:

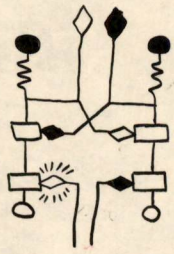


The inverter's output is◆unless both inputs are◆. The delay between a change in the input voltages and the resulting change in the output is about 35 musec.

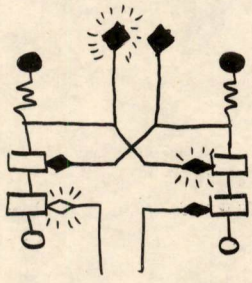
As shown in Figure 4, the output of each series inverter is connected to one of the intputs of the other. Normally, both inputs are ◆, and in this condition (see Figure 4 (i) and (v)) the flip-flop "remembers", i.e., one of the outputs holds the other in the◇condition, and the second holds the first in the◆condition. To "set" the flip-flop to the opposite configuration (i.e., to complement it), the appropriate input is grounded for a period of 80-90 μsec. (Ground the input on the side where the output is◇.)



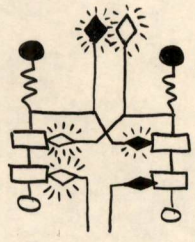
(i) Initial situation. The flip-flop remains in this condition until...



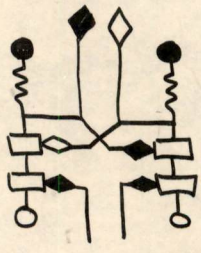
(ii) one input is grounded; but the effect is not felt at the output until...



(iii) about 35 μsec have elapsed; at this time the left output goes to ◆. The right output does not respond until.....



(iv) another 35 μsec. have elapsed; now the right output takes over the job of holding the the left at ◆. Now...

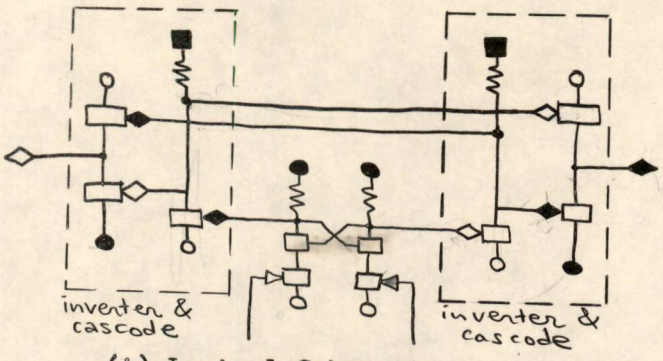


(v) the left input can be returned to ◆.

FIGURE 4 - RESETTING A FLIP-FLOP FROM THE ◇◆ CONDITION TO ◆◇.

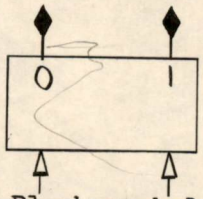
It is important that the input remain at ◇ until situation (iv) is reached, i.e., for at least 70 μsec.; otherwise the circuit will oscillate.

The TX-0 flip-flop consists of the circuit shown in Figure 4, together with a power amplifier at each output:

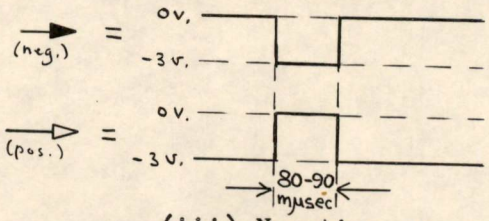


(i) Logical Schematic

FIG. 5 - TX-0 Flip-Flop



(ii) Block symbol



(iii) Negative vs. positive pulses.

The "invert-cascode" circuits invert and amplify the outputs; in the situation shown in Figure 5(i), the outputs of the basic flip-flop circuit are ◆ and ◇ , while the corresponding outputs from the amplifiers are ◇ and ◆ .

The flip-flop inputs are "positive" pulses, i.e., they are normally at the ◆ level, but are brought to ◇ for a period of 80-90 musec, to set the flip-flop. Pulses (—►or—▷) are distinguished from levels (—◆or—◇) by the shape of arrowheads; the two sorts of pulses are distinguished by solid or hollow arrowheads as in Fig. 5(iii).

We speak of flip-flops as "holding a 0" ("being in the '0' state") or "holding a 1" ("being in the '1' state"). What does this mean, physically? The physical flip-flop is a symmetric circuit with two output terminals. One of the terminals has a "0" stamped beside it, and the other has "1". Logically it is irrelevant, which is stamped "0" and which "1". It is also an arbitrary decision, whether the flip-flop is said to "hold a 0" when the output configuration is ◆ ◇ or when the configuration is ◇ ◆ . All that matters is that whichever of these configuration is identified with the "0" state the other must be identified with the "1" state.

A wiring diagram pictures the physical situation by showing, for example, which points are connected to the flip-flop output terminal stamped "1". But a logical schematic diagram shows the "logical" situation by showing, for example, which points are ◆ and which are ◇ when the flip-flop holds a 1. In such diagrams, lines going to the side marked "1" (for example) need not correspond to wires connected to the output terminal of the physical flip-flop which is stamped '1'. Instead, the convention illustrated in Fig. 6 is followed.

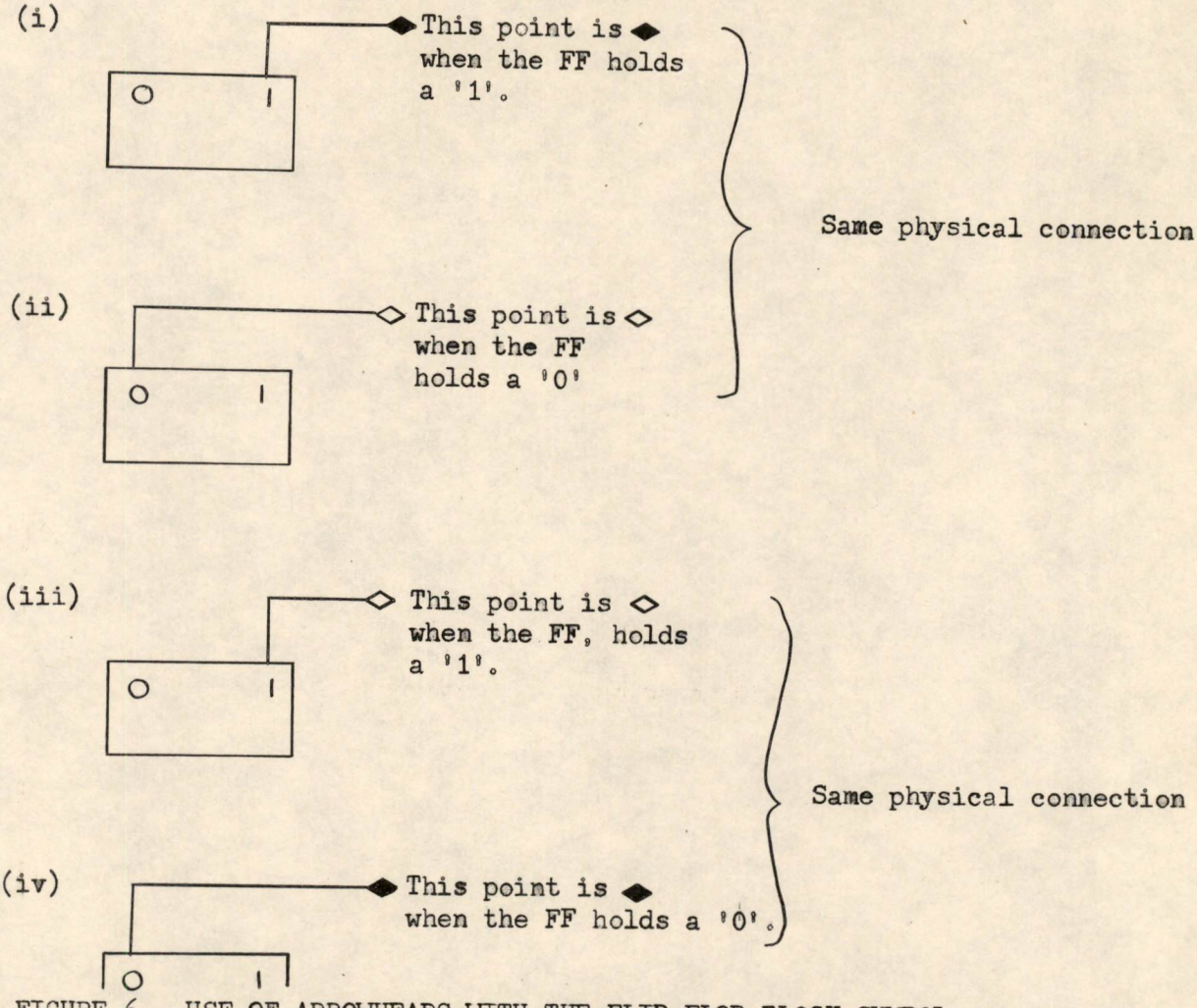
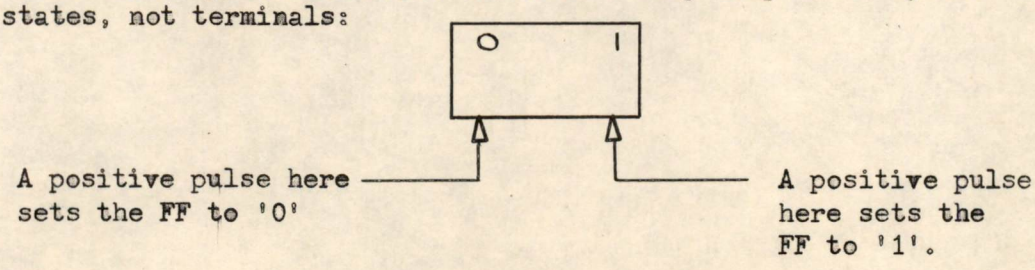


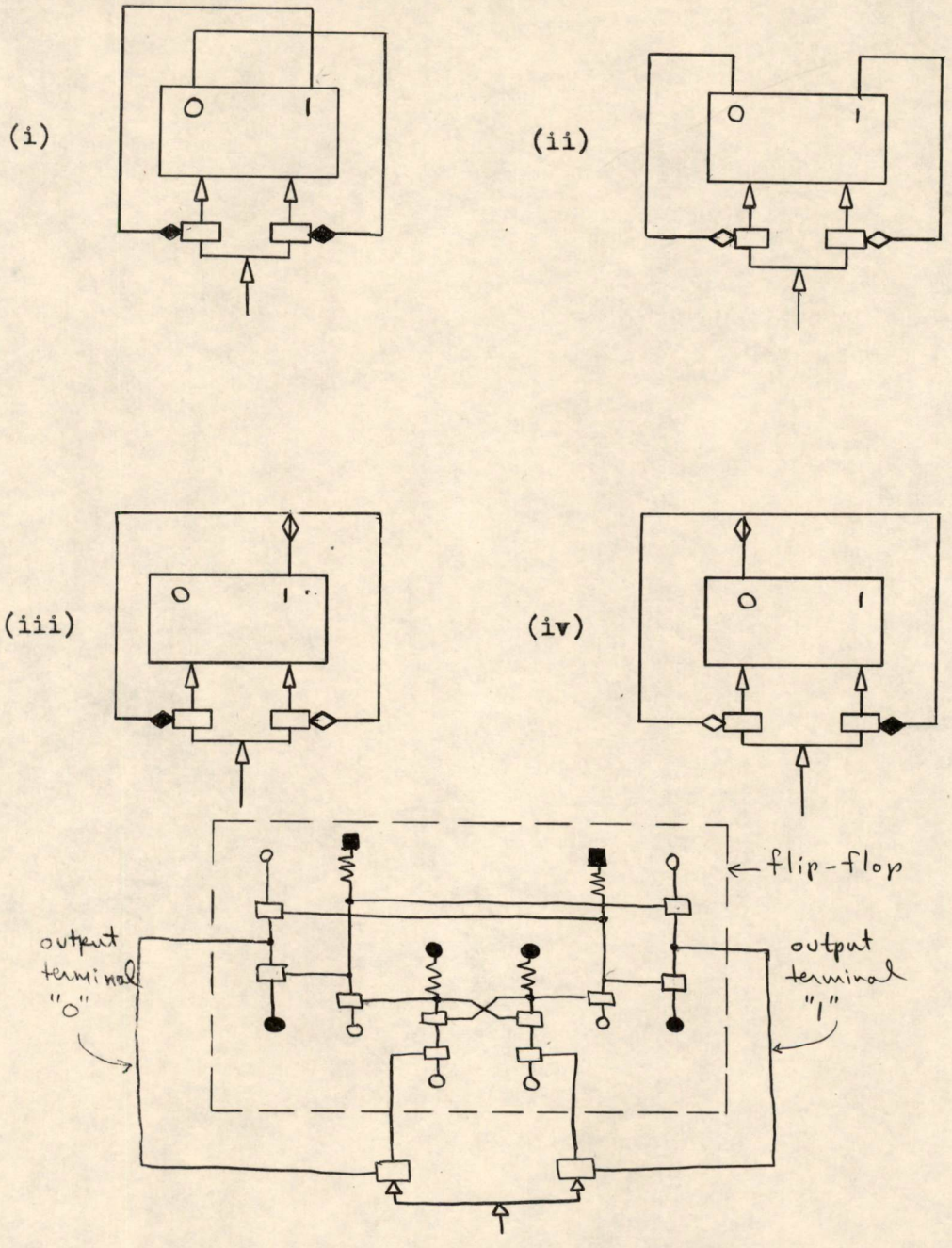
FIGURE 6 - USE OF ARROWHEADS WITH THE FLIP-FLOP BLOCK SYMBOL

Note that physically, the output wires indicated in Figure 6 (i) and (ii) go to the same terminal of the flip-flop, i.e., the terminal which is ◆ when the flip-flop holds a '1' and which is therefore ◇ when the flip-flop holds a '0'. In the physical flip-flop this terminal might be stamped "1" or might be stamped "0" - the logical schematic would be the same in either case. Similarly, the output wires in (iii) and (iv) would both be wired to the terminal <u>opposite</u> the one used for (i) and (ii).

Like the outputs, the input lines to a flip-flop block symbol refer to states, not terminals:



To illustrate the use of this symbolism, Figure 7 (i) through (iv) shows four different ways of drawing the circuit for which (v) is the complete logical schematic.



(v) COMPLETE LOGICAL SCHEMATIC

FIGURE 7 - ALL 5 WOULD BE WIRED UP IN THE SAME WAY

Note the difference between the complete logical schematic (v) and the schematics which use the block symbol for the flip-flop. In (v) the output terminals are shown, whereas in (i) through (iv), states are shown instead. In (v), it is not necessary to tag the flip-flop outputs (terminals) as ◆ or ◇; but (i) through (iv) would lose their meaning if the diamond arrowheads were erased, since it would then be impossible to tell which state of the flip-flop makes a point ◆ or ◇. (However, the split diamonds in (iii) and (iv) could be dropped; they are included only as an aid to the eye in identifying the input line at a junction of lines.)

The reason of devoting so much space to our convention for the use of arrowheads at flip-flop outputs is that it differs from the usual convention. It would be more in keeping with general usage to regard this: 

as simply an abbreviation for the circuit enclosed in broken lines in Figure 7 (v). Then the two lines at the top of the box marked "FF" would represent output terminals, and the two styles of diamonds would be superfluous. However, the TX-0 logical schematics (and presumably those for TX-2 as well) follow the notation of Figure 6.

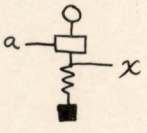
APPENDIX: INVENTORY OF BASIC CIRCUITS IN TX-0

Note on Symbolism

Most of the following diagrams are accompanied by two "equations", which describe the operation of the circuit in two different but equivalent ways. For fuller explanation of the "equations", see page 4.

I. INVERTERS (VOLTAGE AMPLIFIERS).

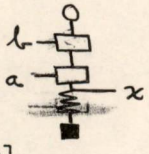
A. Simple



$x = \bar{a}$

$\bar{x} = a$

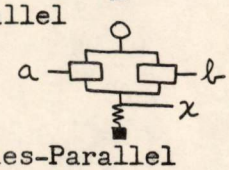
B. Series



$x = \bar{a} + \bar{b}$

$\bar{x} = ab$

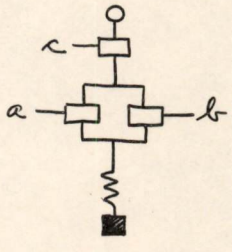
C. Parallel



$x = \bar{a}\,\bar{b}$

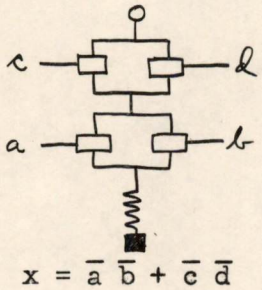
$\bar{x} = a + b$

D. Series-Parallel



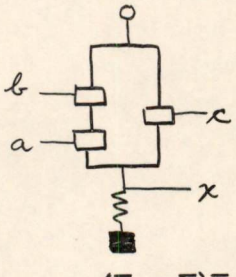
$x = \bar{a}\,\bar{b} + \bar{c}$

$\bar{x} = (a + b)c$



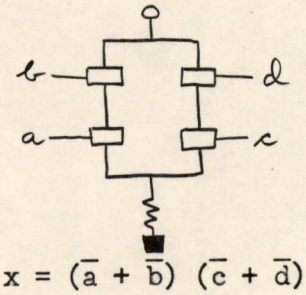
$x = \bar{a}\,\bar{b} + \bar{c}\,\bar{d}$

$\bar{x} = (a + b)\,(c + d)$



$x = (\bar{a} + \bar{b})\bar{c}$

$\bar{x} = ab + c$



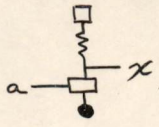
$x = (\bar{a} + \bar{b})\,(\bar{c} + \bar{d})$

$\bar{x} = ab + cd$

Restrictions: Delay $\approx$35 musec. Output (x) may not be connected to the bases of more than 3 emitter-follower transistors or more than 2 inverter transistors.

II. EMITTER - FOLLOWERS (CURRENT AMPLIFIERS)

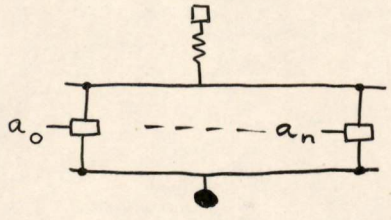
A. Simple



$x = a$

$\bar{x} = \bar{a}$

B. Parallel

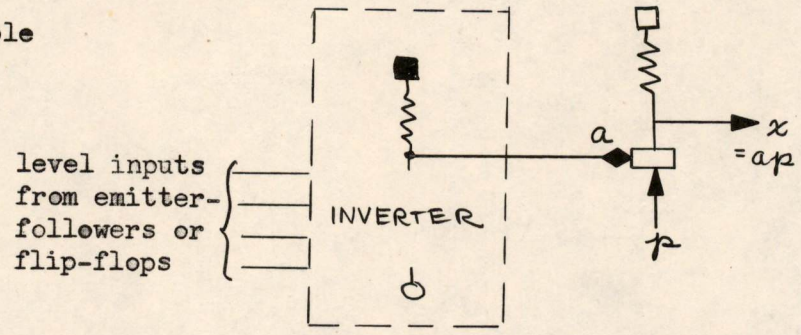


$$\left.\begin{aligned} x &= a_o + \ldots + a_n \\ \bar{x} &= \bar{a}_o \bullet \ldots \bullet \bar{a}_n \end{aligned}\right\} \quad n \leq 9$$

Restrictions. Delay $\approx$10 mμsec for A. For B, delay $\approx 10 + 2n$ mμsec. Output in each case can go to a maximum of 8 emitter - follower bases or 2 inverter bases. In B, x may go the emitter of a single pulse transistor (neglegible delay) or the emitter of a single level transistor with 90 mμsec delay in the transition from ◆ to ◇. In A and B, x may go the base of another emitter-follower, but the output of that second emitter-follower may not in turn go to the base of a third emitter-follower.

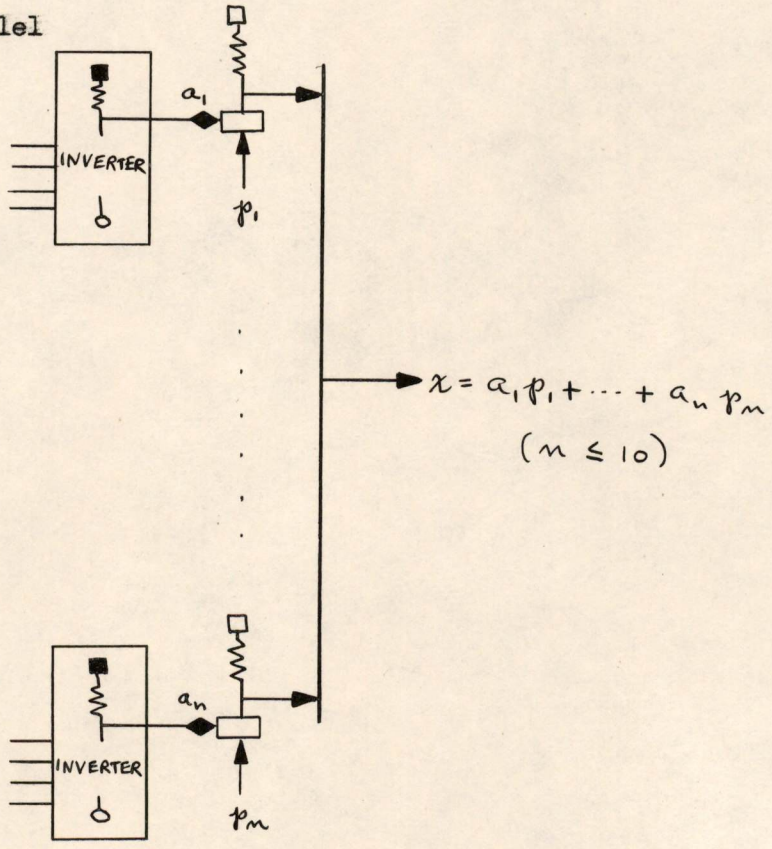
III. "REGISTER DRIVER" (GATE FOR HEAVY PULSES)

A. Simple

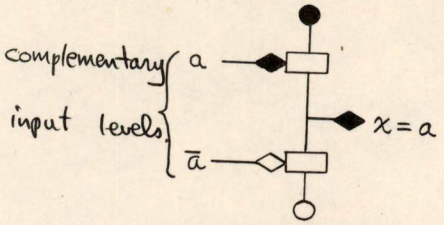


Restrictions: Pulse input (p) and output (x) are negative (i.e., normally ◇). a must be the output of an inverter (any of IA through ID). The same emitter-follower or flip-flop output may be used as a level input to at most 2 register drivers. Output (x) drives a maximum of 10 bases.

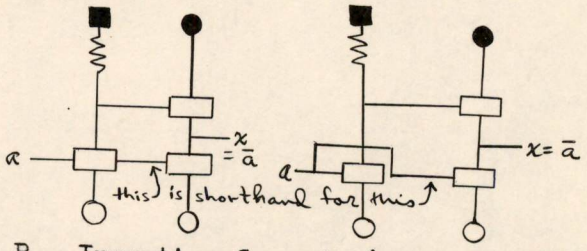
B. Parallel



IV. CASCODE (POWER AMPLIFIER) & CABLE DRIVER



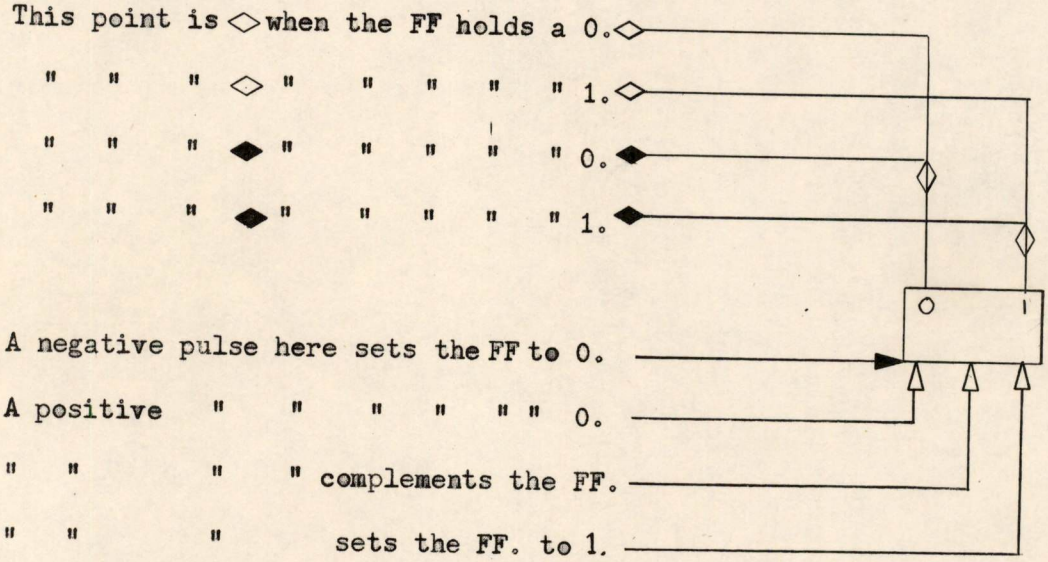
A. Simple Cascode.



B. Inverting Cascode (used as cable driver, with minor circuit modifications).

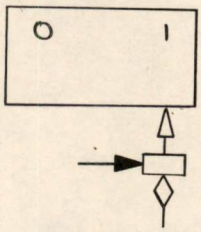
Restrictions: Inputs to cascode must be complementary (when one is ◆, the other is ◇). As power amplifier, can drive maximum of 12 emitter-follower bases or 8 inverter bases, and 1 emitter.

V. FLIP-FLOPS

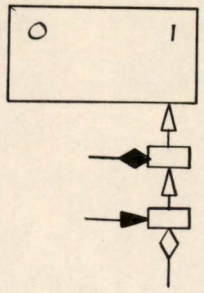


Restrictions: Delay between start of input pulse and time when output is stablilized in its new state is about .1 μsec. Only one of the input lines may be pulsed at any time. The TX-0 flip-flop lacks the negative pulse input (—►) and the complement input; TX-2 flip-flops will have all 4 inputs. Output lines are driven by inverting cascodes internal to the flip-flops; therefore output restrictions are the same as in IV above.

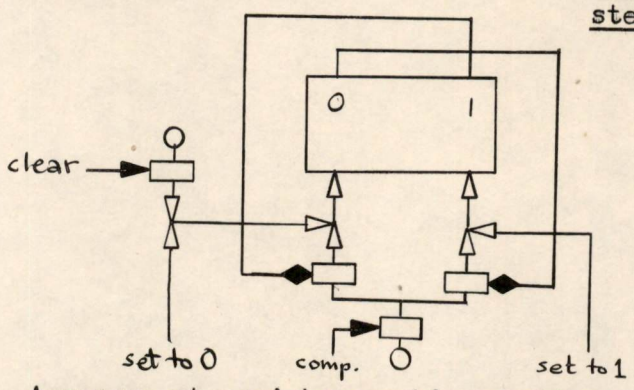
VI. PULSE AND STEERING GATES (AT FLIP-FLOP INPUTS).



A. Pulse gate.



B. Pulse gate followed by a steering gate.



C. Arrangement used to provide negative-pulse clear and complement inputs to TX-0 flip-flops.

Note: The positive-pulse set and clear input terminals to the basic flip-flop are held at ◆ unless they are forced to ◇ by being grounded through a transistor "switch".

Restrictions: No path to a ◇ source from either of the positive-pulse input terminals of the basic flip-flop may pass through more than three transistor "switches". For example, the ◇ input in B may come directly from a flip-flop output terminal, or from the output of an emitter-follower (IIA or B) or of a simple inverter (IA). This means that paths to ground from the positive-pulse complement input of a flip-flop may pass through no more than two transistor "switches". The negative clear pulse input must come directly from a register driver.

Signed: Richard C. Jeffrey
Richard C. Jeffrey

RCJ:elc
Attachment: Figure 1

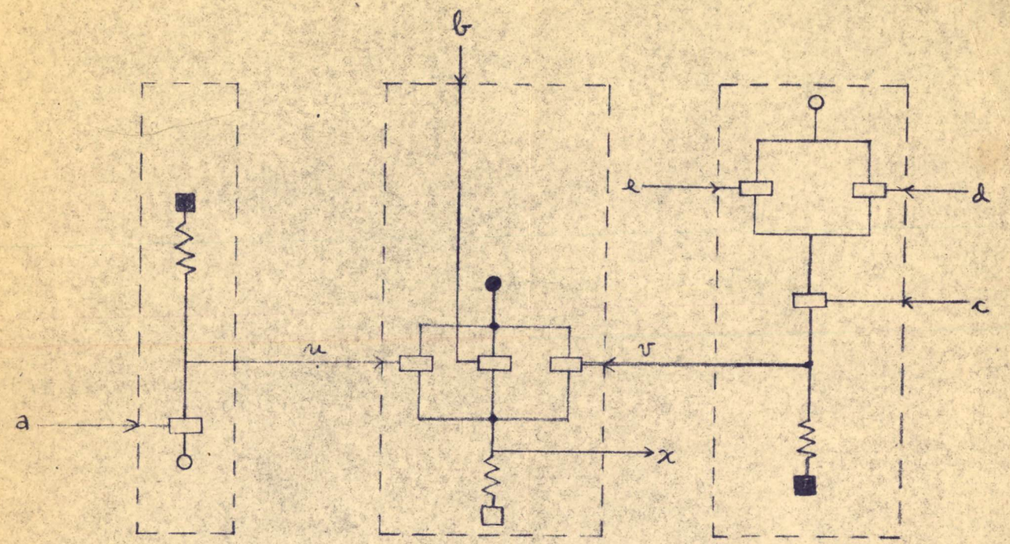


FIG 1 - LOGICAL SCHEMATIC DIAGRAM
OF A TRANSISTOR NET
(fold out)

R. L. Best
B-077

Memorandum 6M-4571

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRANSISTOR LOGIC IN TX-0

To: Distribution List

From: Richard C. Jeffrey

Date: September 5, 1956

Approved: W A Clark
W. A. Clark

Abstract: This note is a supplement to 6M-4561, "TX-0 Circuitry". A simple analogy between transistors and switches is used to explain the operation of the transistor networks in TX-0. (material in this note will apply with minor changes to TX-2 as well.) Conventions for the use of arrowheads (→, ▷, ◆, ◇) in TX-0 and TX-2 logical schematic diagrams are explained. An inventory of TX-0 basic circuits is appended for use in logical design

Distribution List

*Group 63

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1. INTRODUCTION

From the point of view of someone trying to design new basic circuits, transistors are rather complicated devices; but for purposes of understanding what an existing basic circuit or network of basic circuits does, transistors may be thought of simply as switches (sec. 2). This simplified model of the transistor gives an entirely reliable interpretation of the "logical schematic" diagrams of TX-0 (and of those which are being prepared for TX-2). The simplified model is also a useful guide for the logical designer: under certain restrictions, any network built from the basic circuits listed in the appendix will behave in the manner predicted by the switch-analogy. The restrictions are indicated in the appendix to this note and, in greater electronic detail, in 6M-4561, "TX-0 Circuitry". It should be noted that no attempt is made here to give a complete or even an entirely accurate description of how transistors work. What is provided is rather a rule of thumb, as simple as possible, which gives correct results. The rule is sometimes right for the wrong reasons, but it is never wrong.

In addition to the general exposition of transistor logic, the various special notational devices used in TX-0 and TX-2 block schematics are explained.

2. TRANSISTORS AS SWITCHES

Figure 1 (fold-out, last page) is an example of a "logical schematic" diagram. Working from the logical schematic one can reconstruct and wire up the actual circuit, which contains some additional resistors, condensers, and voltage sources. (For details, see 6M-4561, "TX-0 Circuitry.") In the diagram,

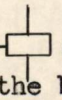
' ■ ' stands for a -10 volt source,

' ● ' stands for a -3 volt source,

' □ ' stands for +10 volt source, and

' ○ ' stands for 0 volt source (ground).

For our purposes it is sufficient to remember that <u>filled-in squares or circles</u> are negative voltage sources, and hollow squares or circles are non-negative.

In Figure 1, '  ' stands for a transistor: the short side of the rectangle represents the base, and the long sides represent the emitter and collector. But for our purposes we can imagine that <u>each transistor is a switch which closes when the base is negative, and is open otherwise</u>.* Let us use a solid diamond (—◆) to indicate negative points, and hollow diamonds (—◇) to indicate points which have 0 or positive voltage.

*Throughout this note, "transistor" means specifiaclly <u>p-n-p transistor</u> (the only kind currently used in TX-0). n-p-n transistors have opposite characteristics from p-n-p; specifically, thought of as switches, they close when the base is ◇ and open when the base is ◆.

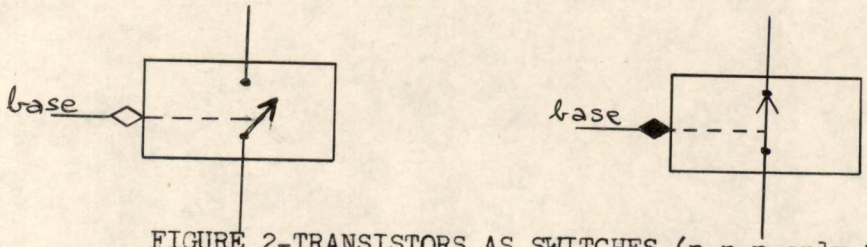


FIGURE 2-TRANSISTORS AS SWITCHES (p-n-p only *)

The function of the resistors (-ww-) in Figure 1 is simply this: a point like u which is connected to a negative source through a resistor will be ◆ unless it is forced to become ◇ by a direct connection to a ◇ source. Thus if point a in Figure 1 is ◆, the transistor "switch" between u and ○ closes and thus forces u to become ◇. Similarly, a point like x, which is connected through a resistor to a ◇ source will be ◇ unless it is forced to become ◆ by direct connection to a ◆ source. In this case the direct connection might be via any one of the three transistors between x and ●; for example, if u is ◆, x will become ◆.

3. THE ARROWHEAD NOTATION

To get an overall view of the action of a transistor net it is convenient to break it up into basic circuits as indicated by the broken lines in Figure 1. The behavior of each basic circuit can be analyzed separately and then combined with the rest to get the total picture. Thus in the basic circuit at the left, u is ◆ if and only if a is ◇, and, saying the same thing in a different way, u is ◇ if and only if a is ◆. These statements can be written briefly as "equations":

$$u\blacklozenge = a\diamond \qquad (1)$$

$$u\diamond = a\blacklozenge \qquad (1')$$

where '=' is shorthand for "if and only if".

The basic circuit at the right in Figure 1 is somewhat more complicated: v is ◆ if and only if c is ◇ or both d and e are ◇. Here the word "or" is to be understood in the inclusive sense: and/or. Using the sign '+' for or in this sense, and using '.' for and, the statement can be abbreviated as:

$$v\blacklozenge = c\diamond + (d\diamond \cdot e\diamond) \qquad (2).$$

The companion statement, to the effect that v is ◇ if and only if c is ◆ and in addition either d or e (or both) are ◆, is:

$$v\diamond = c\blacklozenge \cdot (d\blacklozenge + e\blacklozenge) \qquad (2').$$

---

*See footnote page 2

In summary, the shorthand is:

'=' means <u>if and only if</u>,

'+' means <u>or</u> in the inclusive sense ("and/or").

'.' means <u>and</u>,

'a◆', 'v◇', etc. mean <u>a is negative, v is non-negative</u>, etc.

The basic circuit in the middle of Figure 1 can be described:

$$x◆ = u◆ + b◆ + v◆ \qquad (3)$$

$$x◇ = u◇ . b◇ . v◇ \qquad (3'),$$

i.e., x is◆ if and only if u or b or (at least one) are◆, and x is◇ if and only if u and b and v are all◇.

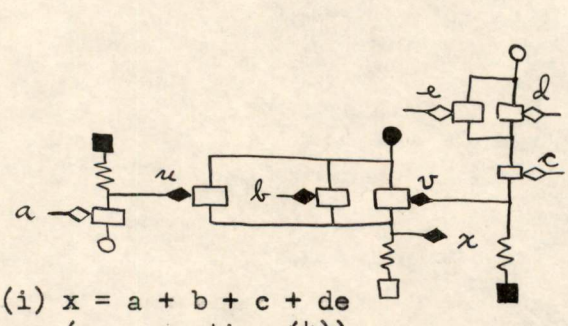
Using (1) and (2) we can eliminate 'u◆' and 'v◆' from (3) to get a single equation which expreses the output directly in terms of the inputs:

$$x◆ = a◇ + b◆ + c◇ + (d◇ . e◇) \qquad (4).$$

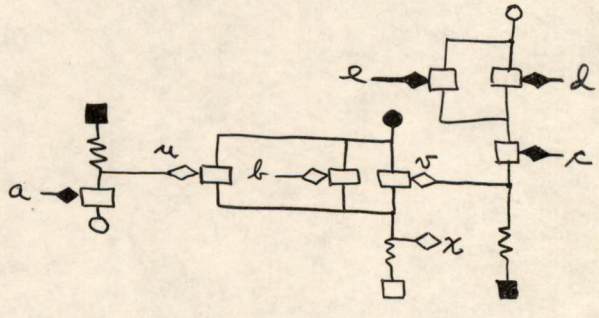
Similarly using (1') and (2') to eliminate 'u◇' and 'v◇' from (3') we get an equivalent description in terms of x◇:

$$x◇ = a◆ . b◇ . c◆ . (d◆ + e◆) \qquad (4').$$

Now to make these equations less cumbersome, we move the diamonds out into the diagram; Figure 3 shows two ways of doing this, corresponding to equations (4) and (4').



(i) x = a + b + c + de
(see equation (4))



(ii) x = abc(d + e)
(see equation (4'))

FIGURE 3 - TWO DISTRIBUTIONS OF ARROWHEADS FOR THE NET OF FIGURE 1

The simplified equation (i) above might be read: "x is as shown in the accompanying diagram (namely, ◆) if and only if a, or b, or c, or both d and e, are as shown there (i.e., if and only if a is◇ or b is◆ or ...)." The equation by itself is ambiguous; the diamonds which fix its meaning

must be gotten from the diagram. Similarly equation (ii) must be read in conjunction with its diagram.

In case it is desired to write equations which will be unambiguous without the aid of diagrams, one can indicate the kind of diamond associated with each letter by some such shorthand as:

'x' means x◆

'$\bar{x}$' means x◇.

Then equation (4) becomes

$$x = \bar{a} + b + \bar{c} + \bar{d}\,\bar{e} \qquad (5)$$

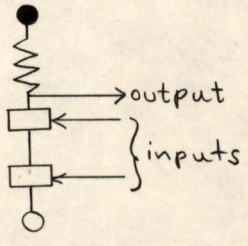
And equation (4') becomes

$$\bar{x} = a\bar{b}c(d + e) \qquad (5').$$

Equations such as (5) and (5') can be manipulated according to the ordinary rules of Boolean algebra, interpreting '$\bar{x}$' as the complement of x. (See R. K. Richards, Arithmetical Operations in Digital Computers, Chapters I and II, or engineering note E-458-1, "The Use of Boolean Algebra in Logical Design".) In cases where our symbols for and ('.') and or ('+') may be confused with the arithmetical product and sum, the following notation is suggested: '&' for and, 'v' for or, and '≡' or '⇔' for if and only if. For example, equation (5) becomes '$x \Leftrightarrow \bar{a} v b v \bar{c} v (\bar{d} \& \bar{e})$' in this notation. The expressions '∼x', '-x' and 'x′' are often used instead of our '$\bar{x}$'.

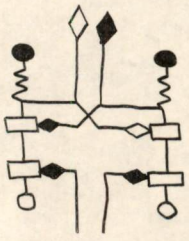
4. FLIP-FLOPS AND AUXILIARY DEVICES

The basic flip-flop is a feedback net consisting of two "series inverter" circuits of this sort:

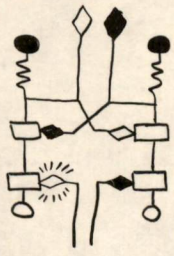


The inverter's output is◆ unless both inputs are◆. The delay between a change in the input voltages and the resulting change in the output is about 35 musec.

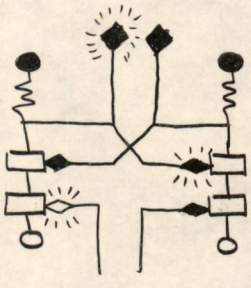
As shown in Figure 4, the output of each series inverter is connected to one of the intputs of the other. Normally, both inputs are ◆, and in this condition (see Figure 4 (i) and (v)) the flip-flop "remembers", i.e., one of the outputs holds the other in the◇ condition, and the second holds the first in the◆ condition. To "set" the flip-flop to the opposite configuration (i.e., to complement it), the appropriate input is grounded for a period of 80-90 μsec. (Ground the input on the side where the output is◇.)



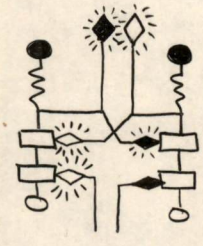
(i) Initial situation. The flip-flop remains in this condition until...



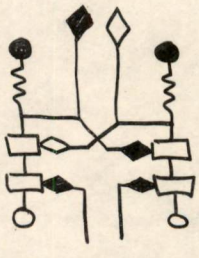
(ii) one input is grounded; but the effect is not felt at the output until...



(iii) about 35 μsec have elapsed; at this time the left output goes to ◆. The right output does not respond until.....



(iv) another 35 μsec. have elapsed; now the right output takes over the job of holding the the left at ◆. Now...

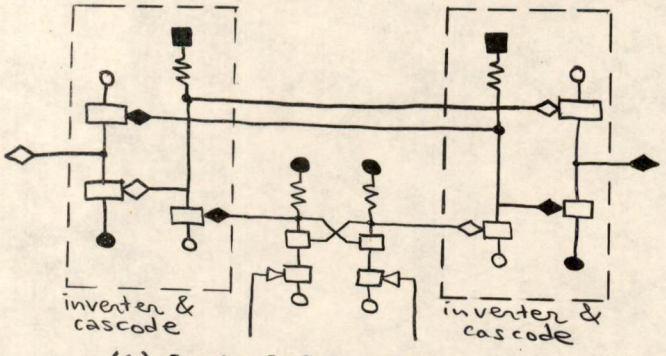


(v) the left input can be returned to ◆.

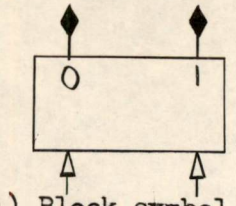
FIGURE 4 - RESETTING A FLIP-FLOP FROM THE ◇◆ CONDITION TO ◆◇.

It is important that the input remain at ◇ until situation (iv) is reached, i.e., for at least 70 μsec.; otherwise the circuit will oscillate.

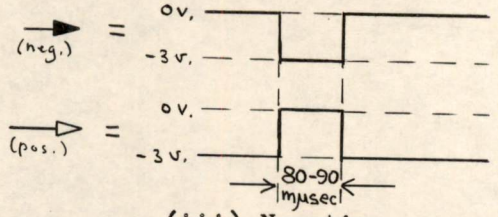
The TX-0 flip-flop consists of the circuit shown in Figure 4, together with a power amplifier at each output:



(i) Logical Schematic
FIG. 5 - TX-0 Flip-Flop



(ii) Block symbol



(iii) Negative vs. positive pulses.

The "invert-cascode" circuits invert and amplify the outputs; in the situation shown in Figure 5(i), the outputs of the basic flip-flop circuit are ◆ and ◇ , while the corresponding outputs from the amplifiers are ◇ and ◆ .

The flip-flop inputs are "positive" pulses, i.e., they are normally at the ◆ level, but are brought to ◇ for a period of 80-90 musec, to set the flip-flop. Pulses (—►or—▷) are distinguished from levels (—◆or—◇) by the shape of arrowheads; the two sorts of pulses are distinguished by solid or hollow arrowheads as in Fig. 5(iii).

We speak of flip-flops as "holding a 0" ("being in the '0' state") or "holding a 1" ("being in the '1' state"). What does this mean, physically? The physical flip-flop is a symmetric circuit with two output terminals. One of the terminals has a "0" stamped beside it, and the other has "1". Logically it is irrelevant, which is stamped "0" and which "1". It is also an arbitrary decision, whether the flip-flop is said to "hold a 0" when the output configuration is ◆ ◇ or when the configuration is ◇ ◆ . All that matters is that whichever of these configuration is identified with the "0" state the other must be identified with the "1" state.

A wiring diagram pictures the physical situation by showing, for example, which points are connected to the flip-flop output terminal stamped "1". But a logical schematic diagram shows the "logical" situation by showing, for example, which points are ◆ and which are ◇ when the flip-flop holds a 1. In such diagrams, lines going to the side marked "1" (for example) need not correspond to wires connected to the output terminal of the physical flip-flop which is stamped '1'. Instead, the convention illustrated in Fig. 6 is followed.

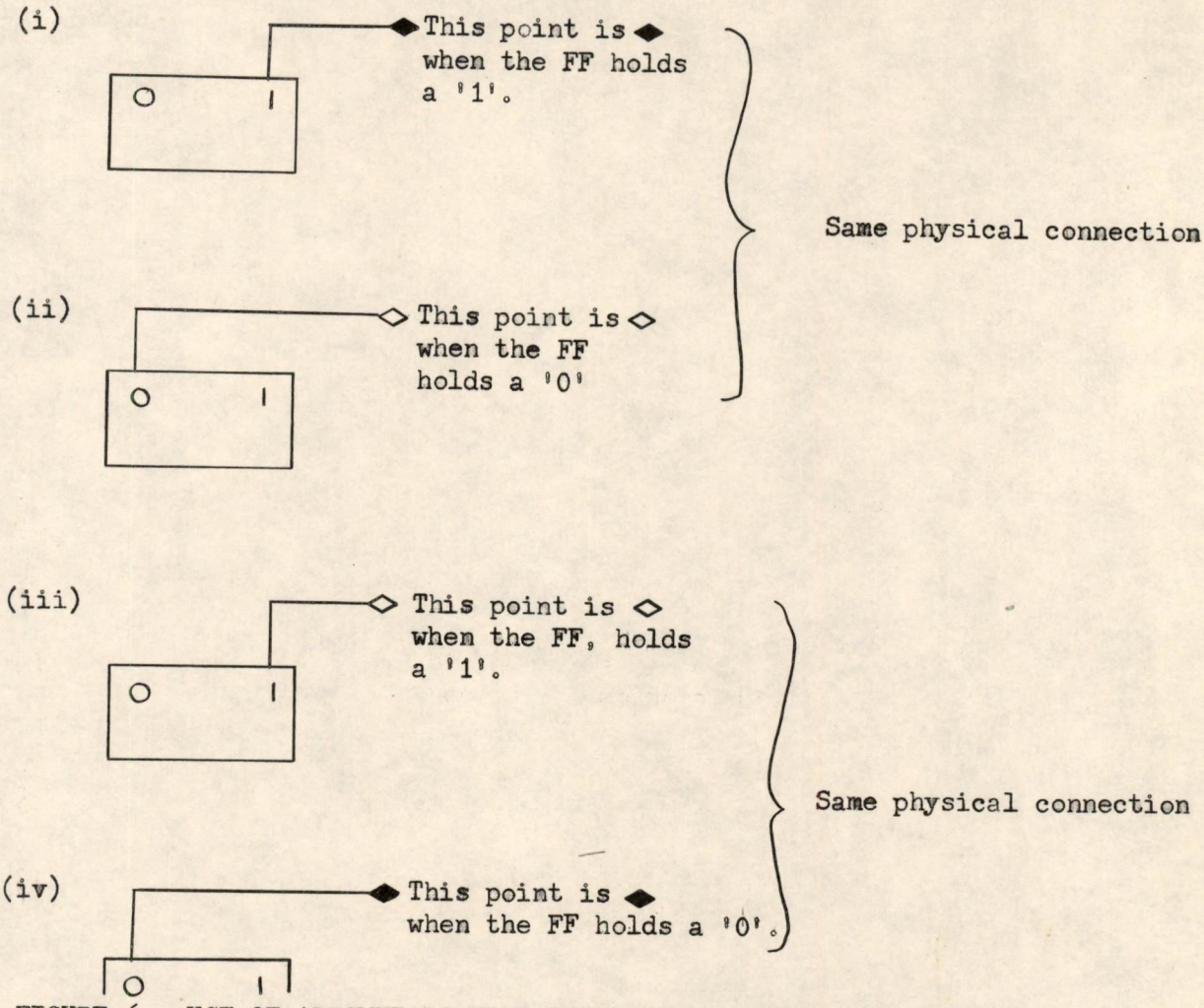
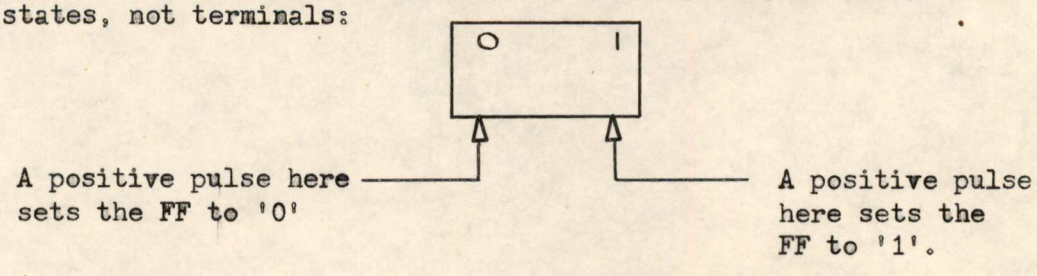


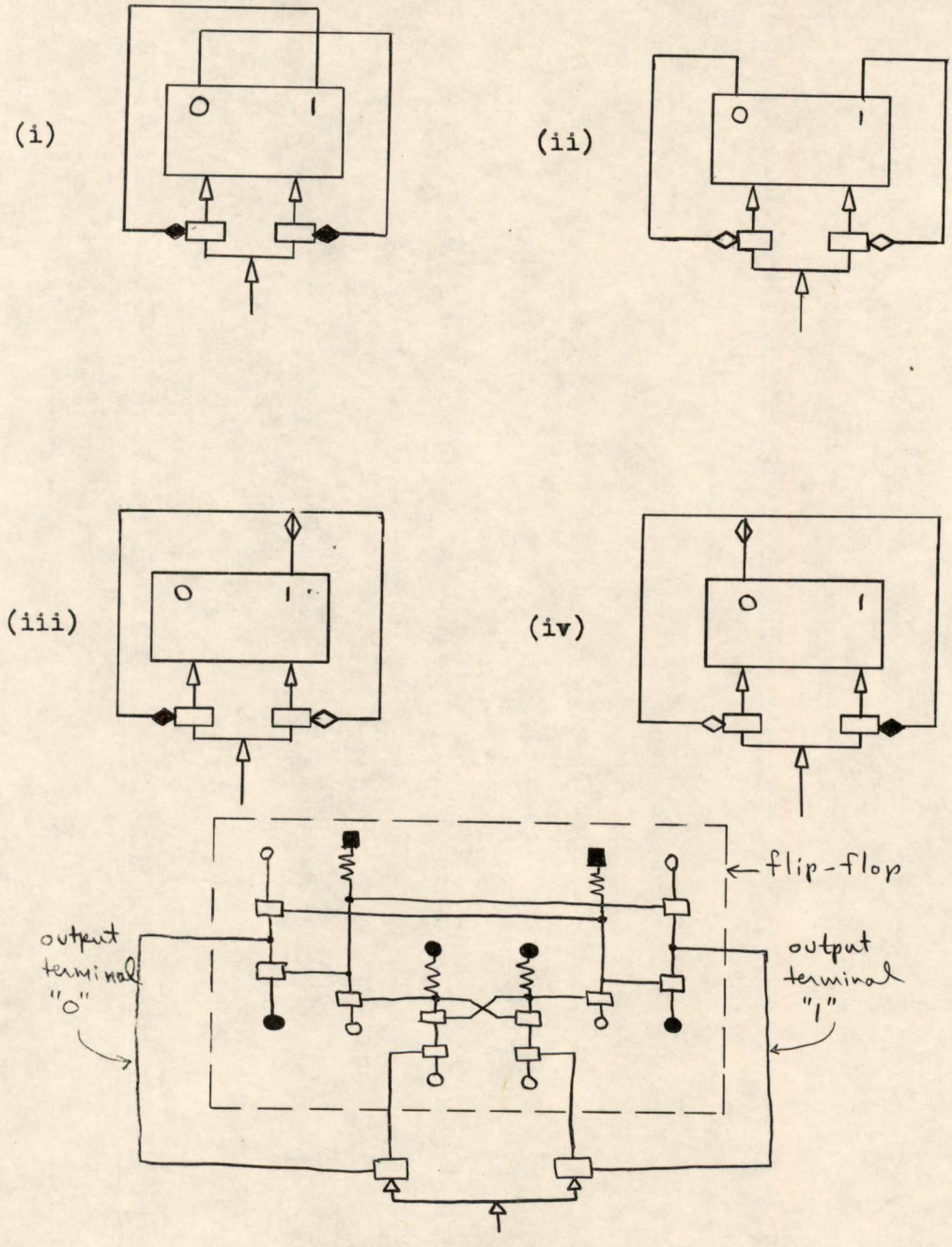
FIGURE 6 - USE OF ARROWHEADS WITH THE FLIP-FLOP BLOCK SYMBOL

Note that physically, the output wires indicated in Figure 6 (i) and (ii) go to the same terminal of the flip-flop, i.e., the terminal which is ◆ when the flip-flop holds a '1' and which is therefore ◇ when the flip-flop holds a '0'. In the physical flip-flop this terminal might be stamped "1" or might be stamped "0" - the logical schematic would be the same in either case. Similarly, the output wires in (iii) and (iv) would both be wired to the terminal <u>opposite</u> the one used for (i) and (ii).

Like the outputs, the input lines to a flip-flop block symbol refer to states, not terminals:



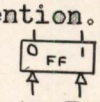
To illustrate the use of this symbolism, Figure 7 (i) through (iv) shows four different ways of drawing the circuit for which (v) is the complete logical schematic.



(v) COMPLETE LOGICAL SCHEMATIC

FIGURE 7 - ALL 5 WOULD BE WIRED UP IN THE SAME WAY

Note the difference between the complete logical schematic (v) and the schematics which use the block symbol for the flip-flop. In (v) the output terminals are shown, whereas in (i) through (iv), states are shown instead. In (v), it is not necessary to tag the flip-flop outputs (terminals) as ◆ or ◇; but (i) through (iv) would lose their meaning if the diamond arrowheads were erased, since it would then be impossible to tell which state of the flip-flop makes a point ◆ or ◇. (However, the split diamonds in (iii) and (iv) could be dropped; they are included only as an aid to the eye in identifying the input line at a junction of lines.)

The reason of devoting so much space to our convention for the use of arrowheads at flip-flop outputs is that it differs from the usual convention. It would be more in keeping with general usage to regard this: 

as simply an abbreviation for the circuit enclosed in broken lines in Figure 7 (v). Then the two lines at the top of the box marked "FF" would represent output terminals, and the two styles of diamonds would be superfluous. However, the TX-0 logical schematics (and presumably those for TX-2 as well) follow the notation of Figure 6.

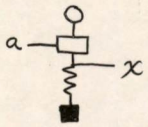
APPENDIX: INVENTORY OF BASIC CIRCUITS IN TX-0

Note on Symbolism

Most of the following diagrams are accompanied by two "equations", which describe the operation of the circuit in two different but equivalent ways. For fuller explanation of the "equations", see page 4.

I. INVERTERS (VOLTAGE AMPLIFIERS).

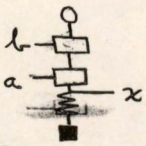
A. Simple



$x = \overline{a}$

$\overline{x} = a$

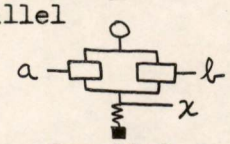
B. Series



$x = \overline{a} + \overline{b}$

$\overline{x} = ab$

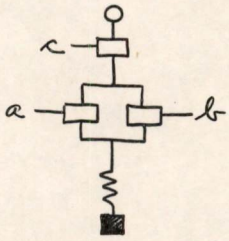
C. Parallel



$x = \overline{a}\,\overline{b}$

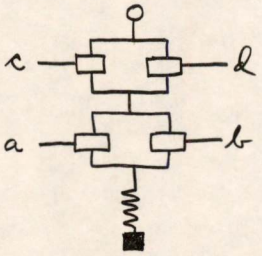
$\overline{x} = a + b$

D. Series-Parallel



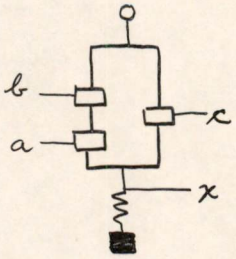
$x = \overline{a}\,\overline{b} + \overline{c}$

$\overline{x} = (a + b)c$



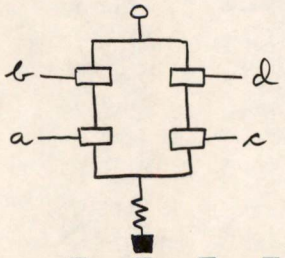
$x = \overline{a}\,\overline{b} + \overline{c}\,\overline{d}$

$\overline{x} = (a + b)\,(c + d)$



$x = (\overline{a} + \overline{b})\overline{c}$

$\overline{x} = ab + c$



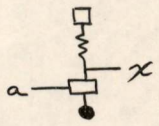
$x = (\overline{a} + \overline{b})\,(\overline{c} + \overline{d})$

$\overline{x} = ab + cd$

Restrictions: Delay $\approx$35 musec. Output (x) may not be connected to the bases of more than 3 emitter-follower transistors or more than 2 inverter transistors.

II. EMITTER - FOLLOWERS (CURRENT AMPLIFIERS)

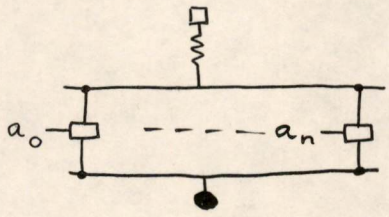
A. Simple



$x = a$

$\bar{x} = \bar{a}$

B. Parallel

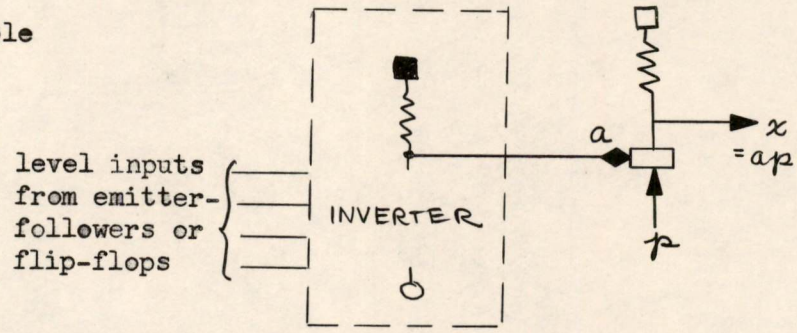


$$\left.\begin{aligned} x &= a_o + \ldots + a_n \\ \bar{x} &= \bar{a}_o \bullet \ldots \bullet \bar{a}_n \end{aligned}\right\} \quad n \leq 9$$

Restrictions. Delay $\approx$10 μsec for A. For B, delay $\approx$ 10 + 2n μsec. Output in each case can go to a maximum of 8 emitter - follower bases or 2 inverter bases. In B, x may go the emitter of a single pulse transistor (neglegible delay) or the emitter of a single level transistor with 90 μsec delay in the transition from ◆ to ◇. In A and B, x may go the base of another emitter-follower, but the output of that second emitter-follower may not in turn go to the base of a third emitter-follower.

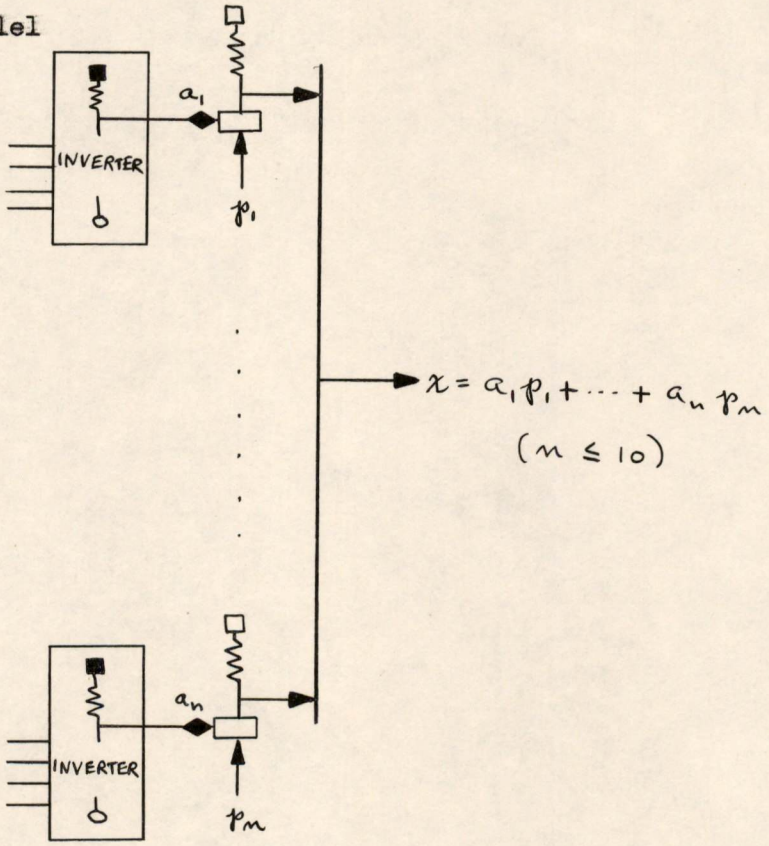
III. "REGISTER DRIVER" (GATE FOR HEAVY PULSES)

A. Simple

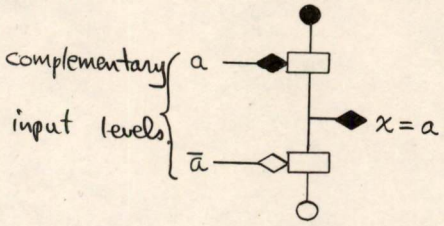


Restrictions: Pulse input (p) and output (x) are negative (i.e., normally ◇). a must be the output of an inverter (any of IA through ID). The same emitter-follower or flip-flop output may be used as a level input to at most 2 register drivers. Output (x) drives a maximum of 10 bases.

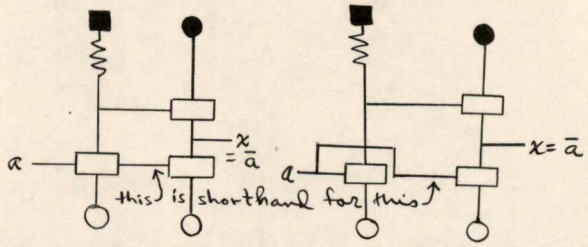
B. Parallel



IV. CASCODE (POWER AMPLIFIER) & CABLE DRIVER



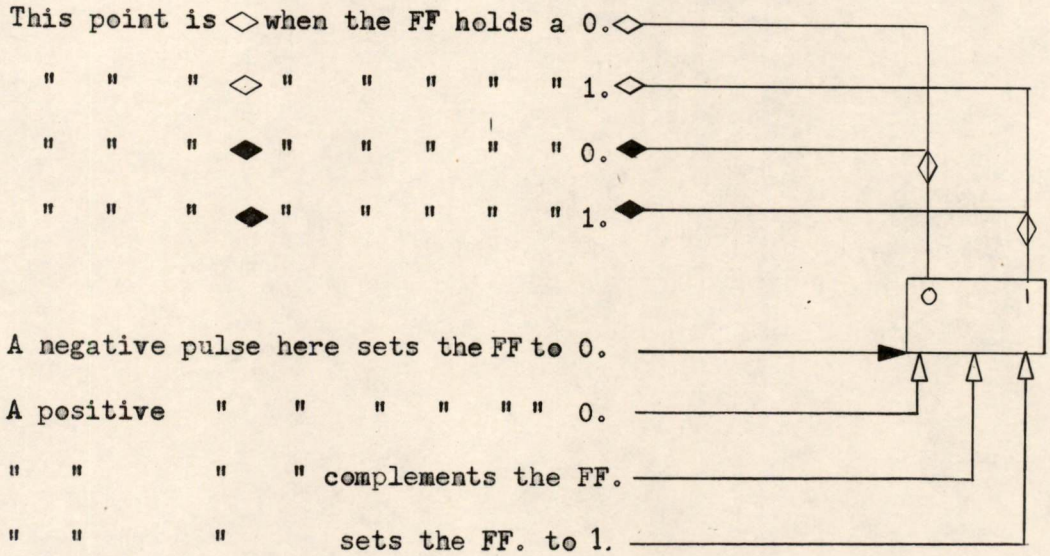
A. Simple Cascode.



B. Inverting Cascode (used as cable driver, with minor circuit modifications).

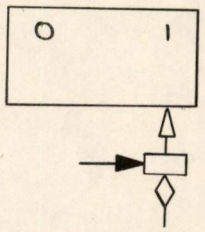
Restrictions: Inputs to cascode must be complementary (when one is ◆, the other is ◇). As power amplifier, can drive maximum of 12 emitter-follower bases or 8 inverter bases, and 1 emitter.

V. FLIP-FLOPS

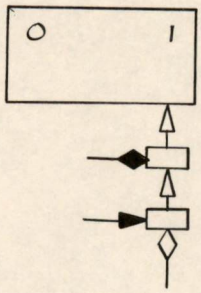


Restrictions: Delay between start of input pulse and time when output is stablilized in its new state is about .1 μsec. Only one of the input lines may be pulsed at any time. The TX-0 flip-flop lacks the negative pulse input (→◆) and the complement input; TX-2 flip-flops will have all 4 inputs. Output lines are driven by inverting cascodes internal to the flip-flops; therefore output restrictions are the same as in IV above.

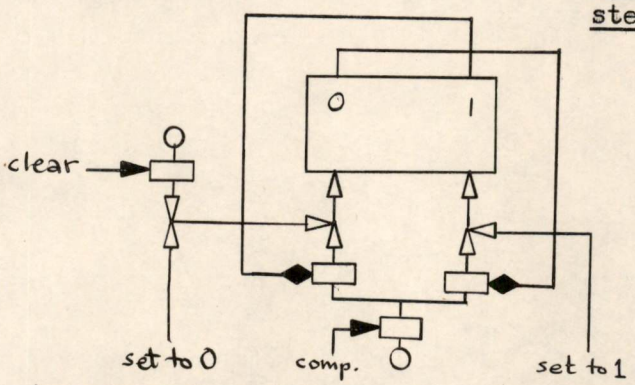
VI. PULSE AND STEERING GATES (AT FLIP-FLOP INPUTS).



A. Pulse gate.



B. Pulse gate followed by a steering gate.



C. Arrangement used to provide negative-pulse clear and complement inputs to TX-0 flip-flops.

Note: The positive-pulse set and clear input terminals to the basic flip-flop are held at ◆ unless they are forced to ◇ by being grounded through a transistor "switch".

Restrictions: No path to a ◇ source from either of the positive-pulse input terminals of the basic flip-flop may pass through more than three transistor "switches". For example, the ◇ input in B may come directly from a flip-flop output terminal, or from the output of an emitter-follower (IIA or B) or of a simple inverter (IA). This means that paths to ground from the positive-pulse complement input of a flip-flop may pass through no more than two transistor "switches". The negative clear pulse input must come directly from a register driver.

Signed: Richard C. Jeffrey
Richard C. Jeffrey

RCJ:elc
Attachment: Figure 1

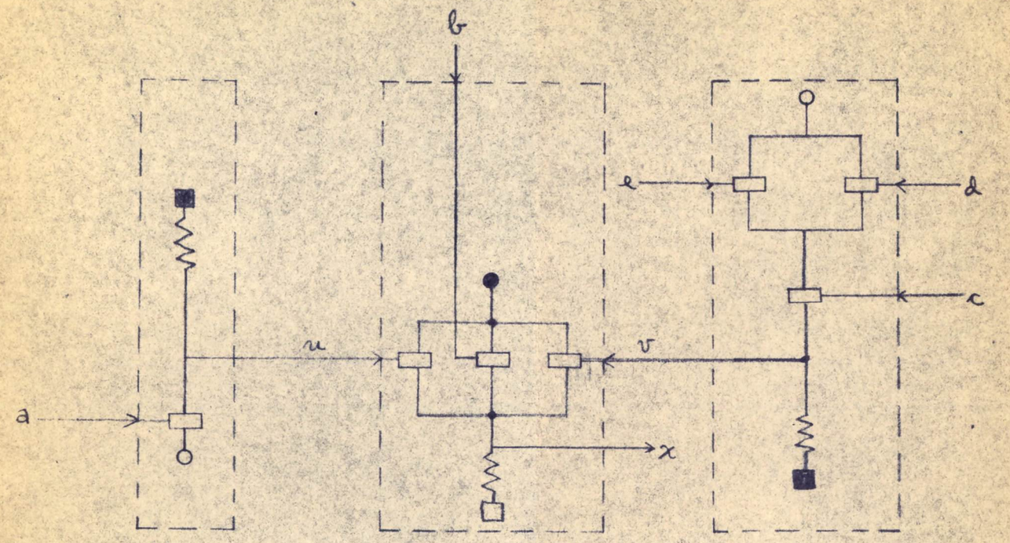


FIG 1 - LÓGICAL SCHEMATIC DIAGRAM
OF A TRANSISTOR NET
(fold out)

P. Bust

Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: SOME NOTES ON THE THEORY AND DESIGN OF ALLOY JUNCTION TRANSISTORS FOR SWITCHING PURPOSES

To: Donald J. Eckl

From: Charles T. Kirk, Jr.

Date: September 28, 1956

Approved: Donald J. Eckl
Donald J. Eckl

Abstract: Ebers and Moll have shown that it is theoretically possible to completely describe the switching characteristics of an alloy junction transistor by four parameters, α_n and α_i, the normal and inverted, common-base, d-c, short-circuit, current-gains, respectively, and, ω_n and ω_i, their respective cutoff frequencies. In Part I of this paper, it is shown that these parameters can be expressed in terms of the transistor physical parameters, $\bar{w}_n$, the average path length of the minority carriers in the base when diffusing from the emitter to the collector (normal operation), $\bar{w}_i$, the average path length of the minority carriers in the base when diffusing from the collector to the emitter (inverted operation), and, τ_b, the effective lifetime of the minority carriers in the base region. In Part II, the equations relating Ebers' and Moll's parameters to the physical parameters of the transistor are used to show that the switching parameters, β_n and β_i, the normal and inverted, common-emitter, d-c, short-circuit, current-gains, respectively, and τ_s, a storage time coefficient, can be interrelated according to an equation of the form

$$(\beta_{n,i} + 1) = \omega_{n,i}\tau_s$$

As a consequence of this equation, it is shown that the switching characteristics of the transistor can be completely described by only three basic switching parameters, β_n, β_i and τ_s. Finally, some aspects of the

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

design of alloy junction transistors for switching purposes are considered in the light of the relationships developed in this paper.

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PART I

ON THE PHYSICAL INTERPRETATION OF THE TRANSISTOR PARAMETERS α_n, α_i, ω_n, and ω_i

INTRODUCTION

A little over a year and a half ago Ebers and Moll[1,2] introduced four transistor parameters which, theoretically, completely characterize the transient behavior of a homogeneous-base, junction transistor. These four parameters are:

- α_n, the normal†, d-c, common-base, short-circuit, current-gain
- α_i, the inverted††, d-c, common-base, short-circuit, current-gain
- ω_n, the cutoff frequency in radians per second of the normal, common-base, short-circuit, current-gain
- ω_i, the cutoff frequency in radians per second of the inverted, common-base, short-circuit, current-gain.

According to the theory, the rise, fall, and delay (storage) times which characterize the transient behavior of a transistor can be expressed in terms of these parameters and the external circuit conditions.

---

1. Ebers, J. J., and Moll, J.L., "Large-Signal Behavior of Junction Transistors," Proc. I.R.E., Vol. 42, No. 12, pp. 1761-1772, December, 1954.

2. Moll, J. L., "Large-Signal Transient Response of Junction Transistors," Proc. I.R.E., Vol. 42, No. 12, pp. 1773-1784, December, 1954.

† The transistor is said to be operating in its normal mode when the transistor is connected so that the designated emitter junction is operated as an emitter and the designated collector junction is operated as a collector.

†† The transistor is said to be operating in its inverted mode when the transistor is connected so that the designated emitter junction is operated as a collector and the designated collector junction is operated as an emitter.

An elementary, current-controlled, saturating, transistor switching circuit is shown in Figure 1 together with pertinent emitter and collector current waveforms of the turn-on and turn-off transient responses of the transistor. The rise, storage, and fall times for this circuit are designated by t_r, t_s and t_f, respectively, and are defined as follows:

t_r, the rise time, is the time required for the collector current to reach 90 per cent of its limiting or saturation value, $I_{c\ sat}$, after a turn-on step of emitter current I_{e1} has been applied.

t_s, the storage time, is the time during which the collector current remains (approximately) at its saturation value after a turn-off step of emitter current, I_{e2}, has been applied, or, more accurately, the time interval between the application of the turn-off step of emitter current and the entrance of the operating point of the transistor into the active region.

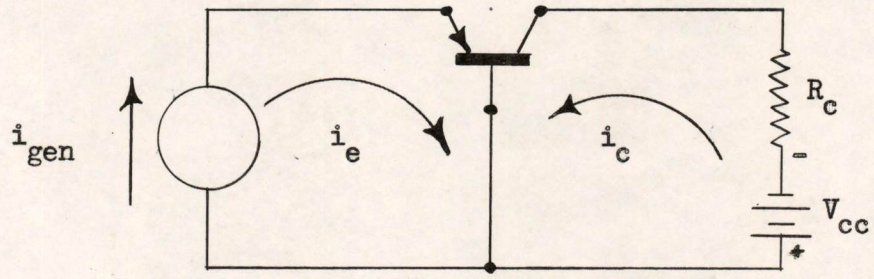
t_f, the fall time, is the time required after the operating point has entered the active region for the collector current to decay to 10 per cent of its saturation value.

In their papers Ebers and Moll show that these rise, storage, and fall times as defined above can be expressed for the common-base circuit configuration shown in Figure 1 by the following relations:

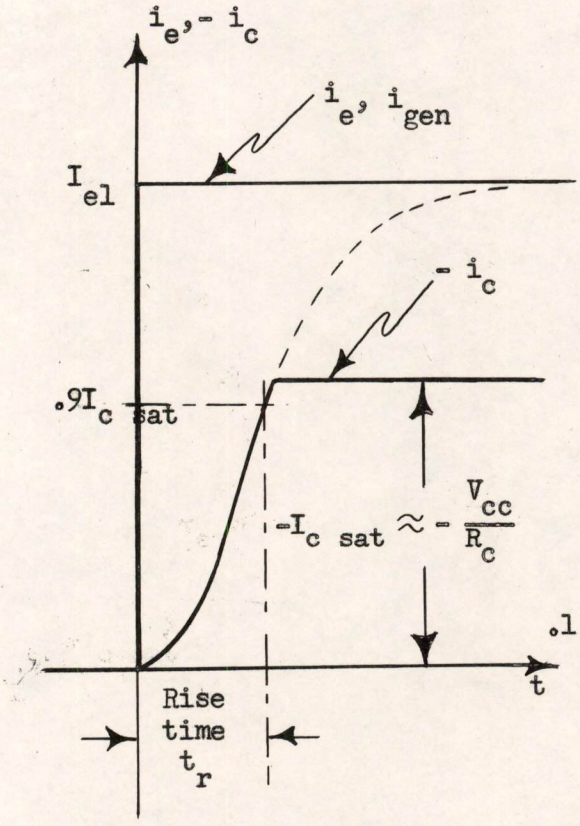
$$t_r = \frac{1}{\omega_n} \ln \frac{I_e}{I_e + .9 \frac{I_{c\ sat}}{\alpha_n}} \tag{1}$$

$$t_s = \frac{\omega_n + \omega_i}{\omega_n \omega_i (1 - \alpha_n \alpha_i)} \ln \frac{I_{e2} - I_{e1}}{I_{e2} + \frac{I_{c\ sat}}{\alpha_n}} \tag{2}$$

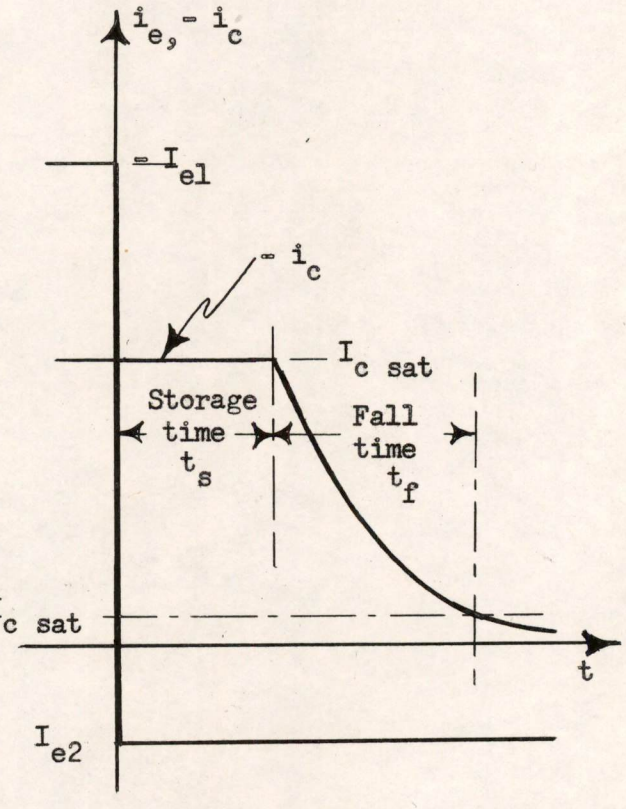
$$t_f = \frac{1}{\omega_n} \ln \frac{I_{e2} + \frac{I_{c\ sat}}{\alpha_n}}{I_{e2} + .1 \frac{I_{c\ sat}}{\alpha_n}} \tag{3}$$



(a) A simple, saturating, transistor switching circuit



(b) Collector Current Transient Response to a "Turn-On" Step of Emitter Current, I_{el}



(c) Collector Current Response to a "Turn-Off" Step of Emitter Current, I_{e2}

Figure 1

While the four switching parameters α_n, α_i, ω_n, and ω_i can be measured electrically for a particular transistor, their functional relationship to the physical design parameters of a transistor has not been shown directly. The purpose of Part I of this paper is to interpret these electrical switching parameters in terms of the physical design parameters of the transistor and to develop a set of equations which describe this relationship.

In order to obtain the desired relationships between α_n, α_i, ω_n, and ω_i, and the physical parameters of the transistor, we first review the development of the common-base, short-circuit current gain, α_o, and its cutoff frequency, $\omega_{c\alpha}$, in terms of the transistor physics from the general solution of the time dependent diffusion equation for a one-dimensional transistor model. Because of the symmetry of the one-dimensional transistor, the relations obtained seemingly lead to an impasse. They state that α_n and α_i are identically equal to α_o and that ω_n and ω_i are identically equal to $\omega_{c\alpha}$ neither of which is the case in a practical transistor. This dilemma does not resolve itself until one realizes that while the identities which exist between α_n, α_i and α_o and ω_n, ω_i and $\omega_{c\alpha}$ must necessarily hold in the one-dimensional transistor model, they do not have to hold in the case of a tri-dimensional model which more nearly approximates a practical transistor. With the postulation of a tri-dimensional model, the degeneracy of the formal relations obtained between the α's and the physical design parameters of the transistor, and the ω's and the physical design parameters is removed. As a result four distinct equations each relating one of the switching parameters, α_n, α_i, ω_n, and ω_i, to the physical design parameters of the transistor can be obtained.

The One-Dimensional Transistor

A model of a one-dimensional, homogeneous-base, junction transistor is shown in Figure 2. For the purposes of this paper, it is unimportant as to whether the model represents a p-n-p or an n-p-n type transistor structure. The abscissa or x-dimension of the model represents distance through the base region in a direction perpendicular to the planes of the emitter and collector junctions with the positive direction of x being defined as going from left to right. The ordinate or p-direction

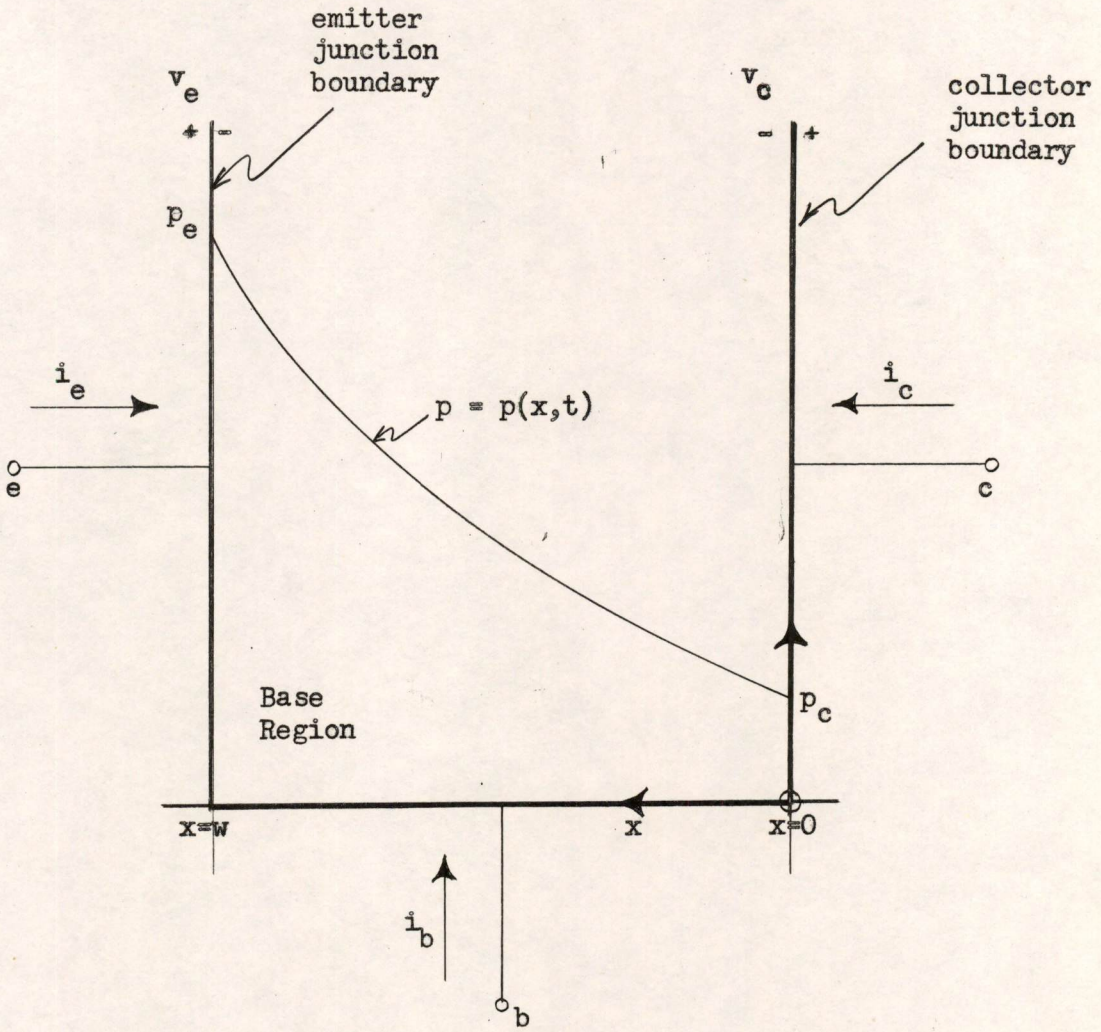


Figure 2

Model of A One-Dimensional Transistor

represents the excess minority carrier density at any point in the base region.

In general, the excess minority carrier density, p, is a function of time, t, and distance through the base, x. This function is determined by the one-dimensional diffusion equation of the form

$$D_p \frac{\partial^2 p}{\partial x^2} - \frac{p}{\tau_p} = \frac{\partial p}{\partial t} \tag{4}$$

where $p = p(x,t)$ is the excess minority carrier density at any point in the base

D_p is the diffusion constant of the minority carriers in the base region

τ_p is the bulk lifetime of the minority carriers in the base region,

together with the boundary conditions imposed on the excess minority carrier density at the emitter and collector junctions. In general, either the carrier density, p, or its gradient, $\partial p/\partial x$, can be specified at a junction as a boundary condition. The choices as to which function is to be specified is determined from the circuit conditions by the relationships,

$$p_{e,c} = \begin{cases} p_o \left(e^{q/kT\, v_{e,c}} - 1\right) & \text{for } v_{e,c} \geq 0 \\ 0 & \text{for } v_{e,c} \leq 0 \end{cases} \tag{5}$$

and

$$i_{e,c} = \pm q D_p \left.\frac{\partial p}{\partial x}\right|_{e,c} \tag{6}$$

where p_e, p_c are the excess minority carrier densities in the base at the emitter and collector junctions, respectively

i_e, i_c are the current densities at the emitter and collector junctions, respectively

p_o is the equilibrium minority carrier density in the base region and is a constant for a homogeneous base transistor

T is the junction temperature in degrees Kelvin

k is Boltzmann's constant

q is the electronic charge.

The symbol, $(\pm)$, in (6) means that the plus (+) sign is to be used when currents at the emitter junction are being considered and that the minus sign (-) is to be used when the collector junction current is being considered.

The form of the diffusion equation given by (4) and relations of (5) and (6) have been derived by Shockley[3] under the following assumptions:

(1) The base region is field free.

(2) The emitter and collector junction are ideal step junctions.

(3) The density of minority carriers everywhere in the base region is at all times negligible compared to the majority carriers in the base region.

(4) The density of the majority carriers in the base region is negligible in comparison to the majority carriers in the emitter and collector regions. This is tantamount to saying that the injection efficiencies of the emitter and collector junction are unity.

(5) The majority carrier density in any region is small compared to the density of available states in the semiconductor material.

(6) The ambient temperature of the semiconductor material is sufficiently large that the carrier energy distribution can be approximated by the Boltzmann statistics. For germanium and silicon this holds quite well at room temperature.

These assumptions will also apply throughout this paper since the relations developed in Part I and Part II depend to some extent on the solution of (4) for certain boundary conditions obtained from (5) and (6).

---

3. Shockley, W., "The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors," BSTJ, Vol. 28, pp. 435-489, July, 1949.

The currents i_e, i_b, and i_c pertaining to the transistor model shown in Figure 2 are the emitter, base, and collector currents, respectively, and, because of the one-dimensionality of the model, they have the dimensions of current density. The voltages, v_e and v_c, are the voltage drops across the emitter and collector junctions, respectively, and are considered to be positive when the voltage drop occurs in going from the emitter or collector to the base.

In theory, it is possible to solve (4) for the excess minority carrier density distribution in the base as a function of x and t, and the physical design parameters of the transistor for any appropriate set of boundary conditions. Once the solution for the excess minority carrier density is obtained, the analytic expressions for the collector and emitter currents can be found by forming the gradient of p, $\partial p/\partial x$, at the particular boundary in question and substituting the resulting expression into the appropriate form of (6).

The Common-Base, Short-Circuit, Transient Response of a One-Dimensional, Homogeneous-Base, Junction Transistor

α, the common-base, short-circuit, current-gain of a junction transistor is, by definition

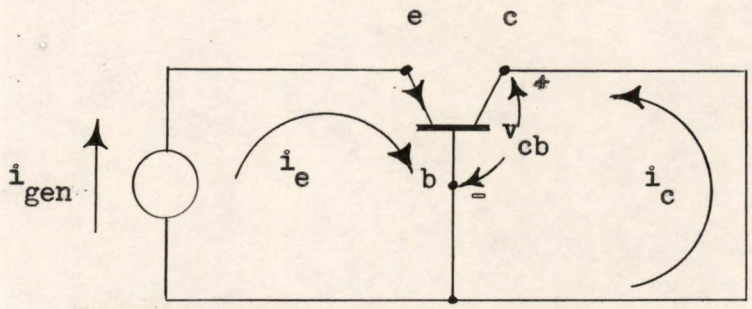
$$\alpha \equiv \left. \frac{\partial i_c}{\partial i_e} \right|_{v_c} \tag{11}$$

For the transistor connected as shown schematically in Figure 3(a), we can, by neglecting the base resistance and the collector bulk resistance, rewrite (11) in the form

$$\alpha = \frac{i_c}{i_e} \tag{12}$$

Shockley[4] and others[5] have derived a small-signal, steady-state expression for α from the one-dimensional transistor model described in the previous section connected as shown in Figure 3(b) of the form

4. Shockley, W., et al, "The P-N Junction Transistors," Physical Review, Vol. 83, No. 1, pp. 151-162, July, 1951.
5. See, for example, Steele, E.L., "Theory of Alpha for P-N-P Diffused Junction Transistors," Proc. I.R.E., Vol. 40, No. 11, pp. 1424-1428, November, 1952.



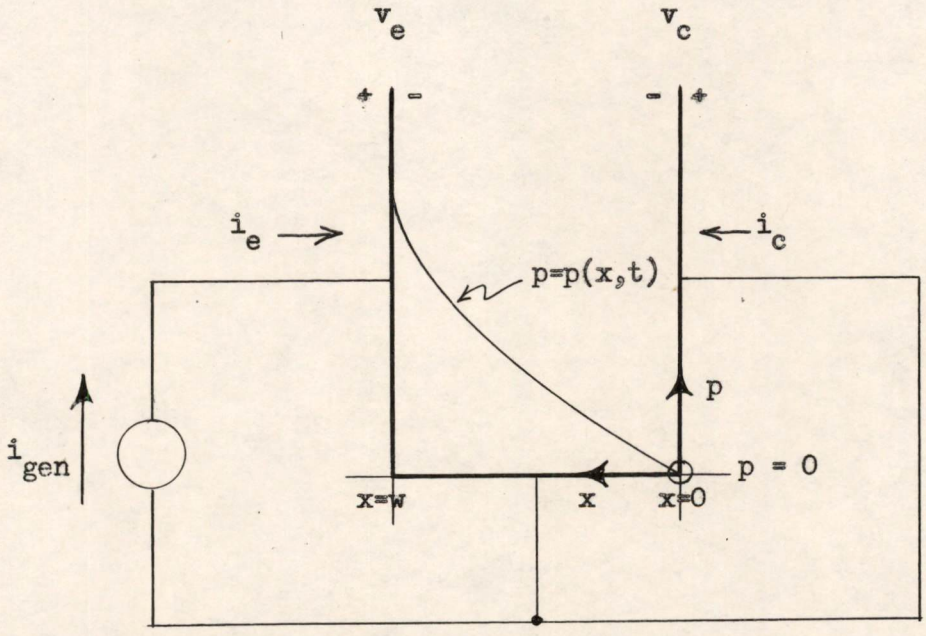
Circuit conditions:

(1) $v_{cb} = v_c = 0$

(2) $i_e = i_{gen} = I_{el}\, e^{j\omega t}$

Figure 3(a)

Circuit Configuration for the Determination of α



Equivalent circuit conditions:

(1) $p_c = 0$

(2) $\left.\frac{\partial p}{\partial x}\right|_e = \frac{I_{el}}{qD_p}\, e^{j\omega t}$

Figure 3(b)

Equivalent Circuit of Figure 3(a)

$$\alpha = \frac{1}{\text{Cosh}\ \frac{w}{L_p}\ (1+j\omega\tau_p)^{1/2}} \tag{13}$$

where $L_p = \sqrt{D_p \tau_p}$

For any "good" transistor

$$\frac{w}{L_p} \ll 1 \tag{14}$$

In which case, the expression for α given by (13) can be rewritten for the "good" transistor in the form

$$\alpha = \frac{1}{1 + \frac{1}{2}\ (1+j\omega\tau_p)\ \frac{w^2}{L_p^2}} \tag{15}$$

The d-c value of α, α_o, is obtained by setting ω equal to zero in (14). Thus

$$\alpha_o = \frac{1}{1 + \frac{1}{2}\ \frac{w^2}{L_p^2}} \tag{16}$$

The cutoff frequency for the common-base, short-circuit, current-gain, $\omega_{c\alpha}$, is defined as the frequency at which

$$\left| \frac{\alpha\ (\omega)}{\alpha_o} \right|^2_{\omega = \omega_{c\alpha}} = \frac{1}{2} \tag{17}$$

From (13), (16) and (17) this frequency ($\omega_{c\alpha}$) is found to be given by the equation

$$\omega_{c\alpha} = \frac{2D_p}{w^2}\ (1 + \frac{1}{2}\ \frac{w^2}{L_p^2}\ ) \tag{18}$$

An alternate expression for α which is more useful than (13) can be obtained in terms of α_o, $\omega_{c\alpha}$, and ω by properly combining (16) and (18) with (13).

$$\alpha = \frac{\alpha_o}{1 + j\,\omega/\omega_{c\alpha}} \tag{19}$$

In the form given by (19), α is seen to have the frequency spectrum of a system with single relaxation time constant of $1/\omega_{c\alpha}$. The response of such a system to a step input is known to be a simple exponential function of time which in the case of our one-dimensional transistor has the form

$$-i_c = \alpha_o I_e \left(1 - e^{-\omega_{c\alpha} t}\right)\left[u_{-1}(t)\right]$$

where $$i_e = I_e\left[u_{-1}(t)\right] \tag{20}$$

By solving (20) for the rise time, t_r, as defined earlier in this paper, we obtain that

$$t_r = \frac{1}{\omega_{c\alpha}} \ln \frac{I_e}{I_e + .9\frac{I_c}{\alpha_o}} \tag{21}$$

which is identical to the Ebers and Moll equation for the normal, common-base, rise-time of a transistor given by (1) provided that we set

$$\omega_n = \omega_{c\alpha} \tag{22}$$

$$\alpha_n = \alpha_o$$

According to Ebers and Moll, the inverted common-base, rise-time of a transistor is given by the equation

$$t_r = \frac{1}{\omega_i} \ln \frac{I_e}{I_e + .9\frac{I_c}{\alpha_i}} \tag{23}$$

The inverted rise time of the one-dimensional transistor model is found to be exactly the same as the normal rise time as given by (21). This must be true because of the symmetry which exists in the one-dimensional model. In view of this fact and equations (21), (22), and (23), we must conclude from our one-dimensional analysis that

$$\omega_n = \omega_i = \omega_{c\alpha} = \frac{2D_p}{w^2}\left(1 + \frac{1}{2}\frac{w^2}{L_p^2}\right)$$

$$\alpha_n = \alpha_i = \alpha_o = \frac{1}{1 + \frac{1}{2}\left(\frac{w^2}{L_p^2}\right)} \tag{24}$$

As we will show, (24) represents a degenerate set of equations relating the electrical parameters α_n, α_i, ω_n, and ω_i to the physical parameters and they hold only for the "so-called" symmetrical transistor.

Transistor Geometry and its Effects on Current Gain and Cutoff Frequency

Measurements† have shown in the case of the non-symmetrical junction transistor that invariably

$$\alpha_n > \alpha_i$$
$$\omega_n > \omega_i \qquad (25)$$

In view of this, it is evident that the one-dimensional transistor model is inadequate as far as interpreting the physical significance of α_n, α_i, ω_n, and ω_i in a non-symmetrical transistor.

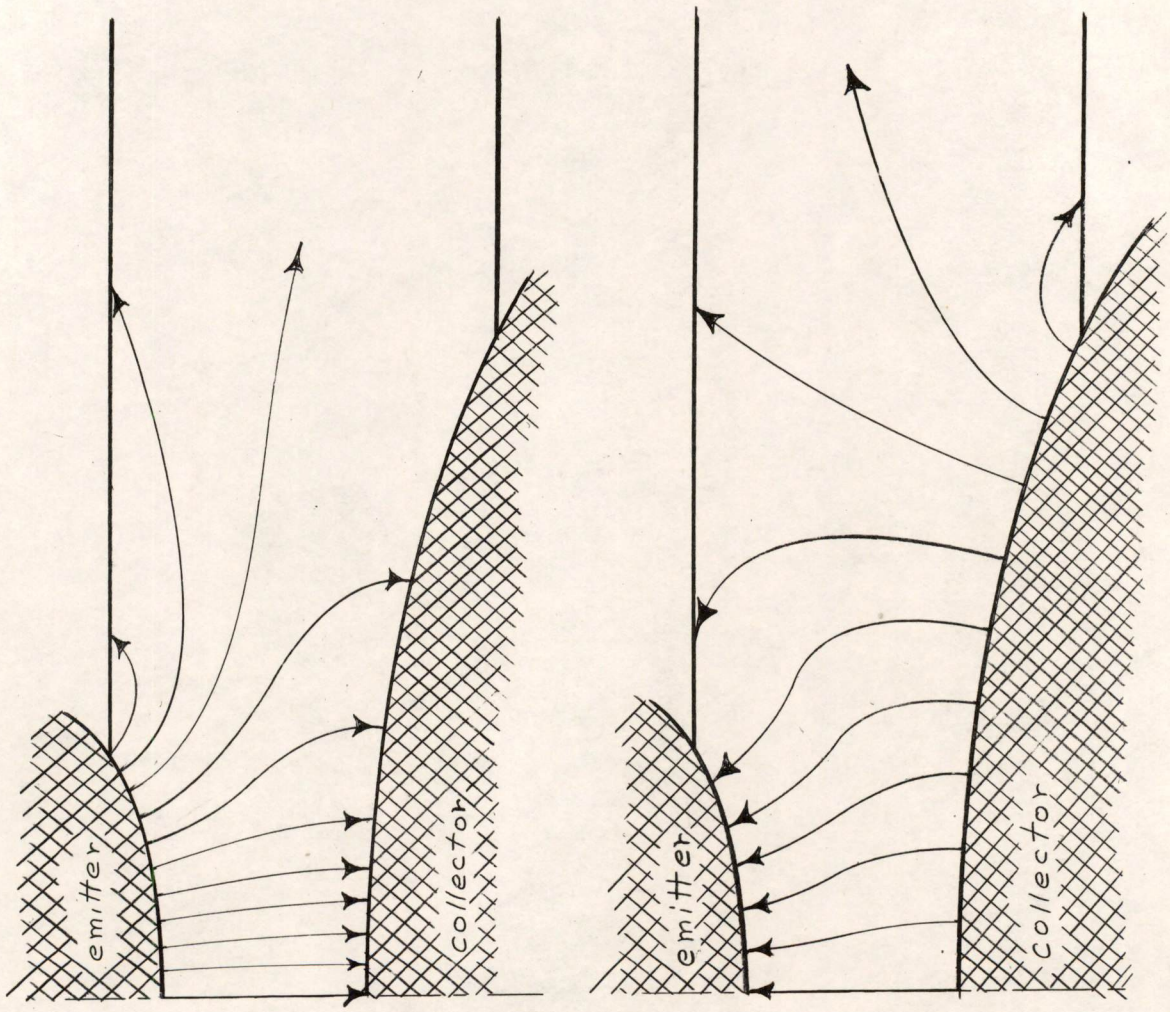
A more accurate model of any alloy junction transistor would be a three-dimensional one which is cylindrically symmetric about an axis passing perpendicularly through the center of the emitter and collector junctions. Such a model is shown in Figure 4 together with a sketch of the hole flow paths when the transistor is connected in the normal manner and in the inverted manner. The hole flow paths sketched in the models of Figure 4 are intended only to point out that the flow paths are different for the normal and inverted operation of the transistor and they are not to be taken as the exact paths that would exist in such a model. The conclusion to be drawn from this discussion is that the average path length of the holes that would be found for normal operation, $\bar{w}_n$, differs from that which would be found for inverted operation, $\bar{w}_i$. Furthermore, in view of (24) and (25) we must also assume that

$$\bar{w}_i > \bar{w}_n \qquad (26)$$

The effective diffusion length, L_b, is determined by the effective base lifetime of the minority carriers, τ_b, according to the equation

$$L_b = \sqrt{D_p \tau_b} \qquad (27)$$

† Ebers, J. J. and Moll, J. L., Op. Cit.



Normal Operational Mode

Inverted Operational Mode

Figure 4

Sketches of an Alloy Junction Transistor
Showing Hole Flow Paths for Normal
and Inverted Mode of Operation

For a thin slab of germanium such as would be used in a high frequency alloy junction transistor where the width of the slab would be much smaller than any other dimension, the effective minority carrier lifetime is given approximately by the relation

$$\frac{1}{\tau_b} = \frac{1}{\tau_p} + \frac{2s}{w} \tag{28}$$

where τ_p is the bulk lifetime of the material
s the surface recombination velocity, and
w is the width of the material.

In this case, w, has to do with the physical width of the base material and is not directly related to the base widths used to describe the average path-lengths over which the holes diffuse through the base. The base width with which we are concerned in the case of the diffusion length depends only on the geometry of the base material used to fabricate the transistor and, consequently, does not change with the type of operation, e.i., normal or inverted operation. The base width with which we are concerned in determining $\omega_{c\alpha}$ or α_o, however, is not only a function of the base geometry but also is a function of the emitter junction geometry and the collector junction geometry which do change with the type of operation. Consequently, while $\bar{w}$ differs with the type of operation, L_b does not.

From the above discussion of transistor geometry and its effects on the current gain and the cutoff frequency for the normal and inverted type of common-base operation of the transistor, it is apparent that the electrical parameters α_n, α_i, ω_n and ω_i can be related to the physical parameters of the transistor by a set of equations which are degenerate only for the case of the symmetrical transistor. Thus, it can be shown that

$$\alpha_n = \frac{1}{1 + \frac{1}{2}\frac{\bar{w}_n^2}{L_b^2}} = \frac{1}{1 + \frac{1}{2D_p}\tau_b}$$

$$\alpha_i = \frac{1}{1 + \frac{1}{2}\frac{\bar{w}_i^2}{L_b^2}} = \frac{1}{1 + \frac{1}{2D_p/\bar{w}_i^2\,\tau_b}} \qquad (29)$$

$$\omega_n = \frac{2D_p}{\bar{w}_n^2}\left[1 + \frac{1}{2}\left(\frac{w_n^2}{L_b^2}\right)\right] = \frac{2D_p}{\bar{w}_n^2} + \frac{1}{\tau_b}$$

$$\omega_i = \frac{2D_p}{\bar{w}_i^2}\left[1 + \frac{1}{2}\left(\frac{w_i^2}{L_b^2}\right)\right] = \frac{2D_p}{\bar{w}_i^2} + \frac{1}{\tau_b}$$

where

$$\frac{\bar{w}_n}{L_b} \ll 1$$

$$\frac{\bar{w}_i}{L_b} \ll 1$$

As we have already discussed, $\bar{w}_n$ and $\bar{w}_i$ are functions of the transistor geometry. Unfortunately, we cannot show explicitly how $\bar{w}_n$ and $\bar{w}_i$ are related to the geometry of the transistor since a solution for the transistor model given in Figure 4 has not been obtained as yet.

Summary

By using the conventional small-signal theory developed by Shockley, it has been shown that the transistor switching parameters, α_n, α_i, ω_n, and ω_i as defined by Ebers and Moll can be related, as in (29), to the following physical parameters of the transistor:

$\bar{w}_n$ - the average path length of holes when diffusing from the emitter to the collector (normal mode of operation)

$\bar{w}_i$ - the average path length of holes when diffusing from the collector to the emitter (inverted mode of operation)

τ_b - the effective lifetime of a hole in the base region.

PART II

SOME THEORETICAL EQUATIONS PERTAINING TO THE THEORY AND DESIGN OF ALLOY JUNCTION SWITCHING TRANSISTORS

INTRODUCTION

In Part I of this paper we developed some equations relating the switching parameters, α_n, α_i, ω_n, and ω_i, to the physical design parameters of the transistor. Part II of this paper is devoted to the development of some theoretical relations pertaining to the theory and design of alloy junction switching transistors.

Specifically, we shall show that it is possible using the equations given in (29) to interrelate the various transistor switching parameters, the most important of which are $\beta_{n,i}$, $\omega_{n,i}$, and τ_s. As a consequence of developing the equations describing the interrelationships among the switching parameters, it is shown that only three basic parameters are necessary to describe the switching characteristics of a transistor, namely; β_n, β_i, and τ_s. In the final section of this paper, we describe how these basic switching parameters, when expressed in terms of the physical design parameters for the one-dimensional transistor model discussed in Part I, can be used to determine the approximate effects of a parameter change on the performance of a switching transistor.

It should be realized that in using the results obtained in Part I of this paper, e.i, (29), to derive the relations just described, we incur the simplifying assumptions made in Part I as restrictions on the application of these relations to practical switching transistors.

Basic Transistor Time Constants and Their Relation to the Physical Design Parameters of the Transistor

The switching times given by (1), (2), and (3) completely define the common-base transient behavior of a transistor operated in the normal mode under constant-current circuit conditions. In addition to these, Ebers and Moll have developed similar expressions for the switching times of a transistor operated in the common-emitter and common-collector configuration, as well, all of which have the same general form,

$$t = \tau \ln \left[F(\alpha, I_e, I_b, I_c) \right] \tag{30}$$

where t is the switching time

τ is a time constant of the transistor and is a function of the configuration, mode, and region of operation

$F(\alpha, I_e, I_b, I_c)$ is a function of the circuit conditions, the common-base, short-circuit current-gain, and the configuration, mode, and region of operation.

The basic transistor time-constants for the various configurations, modes and regions of operation have been determined in terms of the electrical parameters, α_n, α_i, ω_n, and ω_i. Table 1 shows the different time constants that are obtained for the various conditions under which the transistor can be operated. These time-constants can be expressed directly in terms of the physical design parameters of the transistor by simple substitution of the equations given in (29) into the expression for the various time constants. Thus, we have directly from (29) that the normal and inverted, common-base, time-constants, $\frac{1}{\omega_n}$ and $\frac{1}{\omega_i}$, respectively, are related to the transistor design parameters by equations of the form

$$\frac{1}{\omega_n} = \frac{\tau_b}{\frac{2D_p}{w_n^2}\tau_b + 1} = \frac{1}{\frac{2D_p}{w_n^2} + \frac{1}{\tau_b}} \tag{31}$$

$$\frac{1}{\omega_i} = \frac{\tau_b}{\frac{2D_p}{w_i^2}\tau_b + 1} = \frac{1}{\frac{2D_p}{w_i^2} + \frac{1}{\tau_b}} \tag{32}$$

The remaining time-constants listed in Table 1 can be expressed in terms of the physical design parameters of the transistor by the single equation

$$\frac{\omega_n + \omega_i}{\omega_n\omega_i(1 - \alpha_n\alpha_i)} \approx \frac{1}{\omega_n(1 - \alpha_n)} = \frac{1}{\omega_i(1 - \alpha_i)} = \tau_b \tag{33}$$

Table 1

BASIC TRANSISTOR TIME-CONSTANTS

Transistor Operating Conditions	Switching Time-Constant
Common Base Configuration Normal Mode Active Region	$\frac{1}{\omega_n}$
Common Base Configuration Inverted Mode Active Region	$\frac{1}{\omega_i}$
Common Emitter or Collector Configuration Normal Mode Active Region	$\frac{1}{\omega_n(1-\alpha_n)}$
Common Emitter or Collector Configuration Inverted Mode Active Region	$\frac{1}{\omega_i(1-\alpha_i)}$
Common Base, Emitter, or Collector Configuration Normal or Inverted Mode Saturated Region	$\frac{\omega_n + \omega_i}{\omega_n\omega_i(1-\alpha_n\alpha_i)}$

From (31), (32), and (33) it can be seen that the switching time-constants of a transistor can be completely described in terms of the physical parameters, $\bar{w}_{n,i}$ the average hole path lengths in the base and τ_b the effective lifetime of the minority carriers in the base region.

The time-constant of the saturation operating region, $\omega_n + \omega_i/\omega_n\omega_i(1-\alpha_n\alpha_i)$, is usually reffered to as the storage coefficient and designated by the symbol, τ_s. In view of (33) we can write that

$$\tau_s = \tau_b \tag{34}$$

From (33) and (34) it should be clear that the storage coefficient, τ_s, is one of the most important electrical switching parameters of the transistor even if the transistor is to be used in non-saturating switching circuitry. The reason for this is that, in addition to being the basic factor in governing the storage time of a transistor, it is numerically equal to the normal and inverted time-constants which occur for active operation of the transistor in the common-emitter and common-collector configurations. Consequently, the storage coefficient is also the basic factor governing the rise and fall times of a transistor operated in these configurations.

The Common-Emitter, Short-Circuit Current Gain and Its Relation to the Physical Design Parameters of the Transistor

The common-emitter, short-circuit, current-gain, β, is defined as

$$\beta \equiv \left.\frac{\partial i_c}{\partial i_b}\right|_{v_c} \tag{35}$$

which reduces to the form

$$\beta = \frac{i_c}{i_b} \tag{36}$$

for the idealized transistor model described in Part I of this paper. It can be shown from (36) and (12) that the d-c, common-emitter, short-circuit, current-gain, β_o, is related to the d-c, common-base, short-circuits current-gain, α_o, by an equation of the form

$$\beta_o = \frac{\alpha_o}{1 - \alpha_o} \tag{37}$$

Equation (37) can be generalized to include the more important case of the non-symmetrical, alloy-junction, switching transistor by defining a normal and inverted d-c β in the same manner as we defined α_n and α_i. Then, by setting α_o in (37) equal to α_n and β_o equal to β_n in the first instance and similarly setting α_o equal to α_i and β_o equal to β_i in the second instance we obtain a generalized form of (37) which can be written as

$$\beta_{n,i} = \frac{\alpha_{n,i}}{1 - \alpha_{n,i}} \tag{38}$$

where β_n is the normal, d-c, common-emitter, short-circuit, current-gain

β_i is the inverted, d-c, common-emitter, short-circuit current-gain

The normal and inverted dc β's, β_n and β_i, can be expressed in terms of the physical design parameters of the transistor by substituting the appropriate equations in (29) into the right-hand member of (38). The resulting expressions for β_n and β_i can be simplified to yield an equation of the form

$$\beta_{n,i} = \frac{2D_p}{\bar{w}_{n,i}^2}\,\tau_b \tag{39}$$

Basic Switching Parameters

It has been shown[†] that, in theory, the four parameters, α_n, α_i, ω_n, and ω_i, are required to completely describe the transient switching characteristics of a transistor. However, according to (29) in Part I of this paper, these four parameters can be expressed in terms of three independent physical parameters of the transistor, $\bar{w}_n$, $\bar{w}_i$ and τ_b. From

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† Ebers and Moll, Op. Cit.

this it can be concluded that only three of the four parameters given above are mutually independent and thus, in theory, only three electrical parameters are necessary to completely describe the transient switching behavior of a transistor.

One such a minimal set of parameters is the set, β_n, β_i, and τ_s.† The necessary and sufficient conditions for this set to be a desired minimal set of parameters are:

(1) that it is a set of mutually independent parameters

(2) that it is a set of parameters which completely describes the switching characteristics of a transistor.

In order to see that this set satisfies the necessary and sufficient conditions just stated, we write the equations expressing the parameters in this set in terms of the physical design parameters of the transistor. From (34) and (39) we have that

$$\beta_n = \frac{2D_p}{\bar{w}_n^2}\tau_b$$

$$\beta_i = \frac{2D_p}{\bar{w}_i^2}\tau_b \qquad (40)$$

$$\tau_s = \tau_b$$

Assuming that the parameters, $\bar{w}_n$, $\bar{w}_i$, and τ_b, are mutually independent on the basis of the discussion these physical parameters in Part I, we can conclude from (40) that the switching parameters β_n, β_i, and τ_s are also mutually independent since none of these switching parameters can be described as a function of the other two alone. In order to show that these three switching parameters completely describe the switching characteristics of a transistor, we combine the set of equations given in (40) with the equations for ω_n and ω_i given in (29) in such a manner as to eliminate the physical parameters $\bar{w}_n$, $\bar{w}_i$ and τ_b. By doing this, we obtain two equations of the form††

† A set of parameters similar to these was first suggested to describe the transient switching characteristics of a transistor in a paper by G. Messenger, Switching Circuits, Office Correspondence, Philco Corp. June 12, 1956.

†† A relation, similar in form to (41) has been obtained empirically by G. Messenger, Op. Cit.

$$(\beta_n + 1) = \omega_n \tau_s \tag{41}$$

$$(\beta_i + 1) = \omega_i \tau_s$$

Rearranging (41) and (38) we can write that

$$\alpha_n = \frac{\beta_n}{\beta_n + 1}$$

$$\alpha_i = \frac{\beta_i}{\beta_i + 1} \tag{42}$$

$$\omega_n = \frac{\beta_n + 1}{\tau_s}$$

$$\omega_i = \frac{\beta_i + 1}{\tau_s}$$

Having stated previously that α_n, α_i, ω_n, and ω_i completely characterize the switching behavior of a transistor and having shown in (42) that these four parameters can be expressed as functions of β_n, β_i and τ_s alone, we can see that these latter three parameters form a desired minimal set of switching parameters for a transistor.

A concise plot of the interrelationships between the various transistor switching parameters described by (38), (41), and (42) is given in Figure 5. A plot such as this is quite useful for comparing the switching performance of different transistors or for determining the effects of parameter variations on the switching characteristics of a particular type of alloy junction transistor.

The Design Theory of a Symmetrical, One-Dimensional, Switching Transistor

The symmetrical, one-dimensional, transistor that will be discussed here refers to any switching transistor that can be reasonably approximated by the one-dimensional transistor model described in Part I of this paper. In the case of this particular type of transistor, the physical design parameters $\bar{w}_n$, $\bar{w}_i$ and τ_b can be expressed in terms of w,

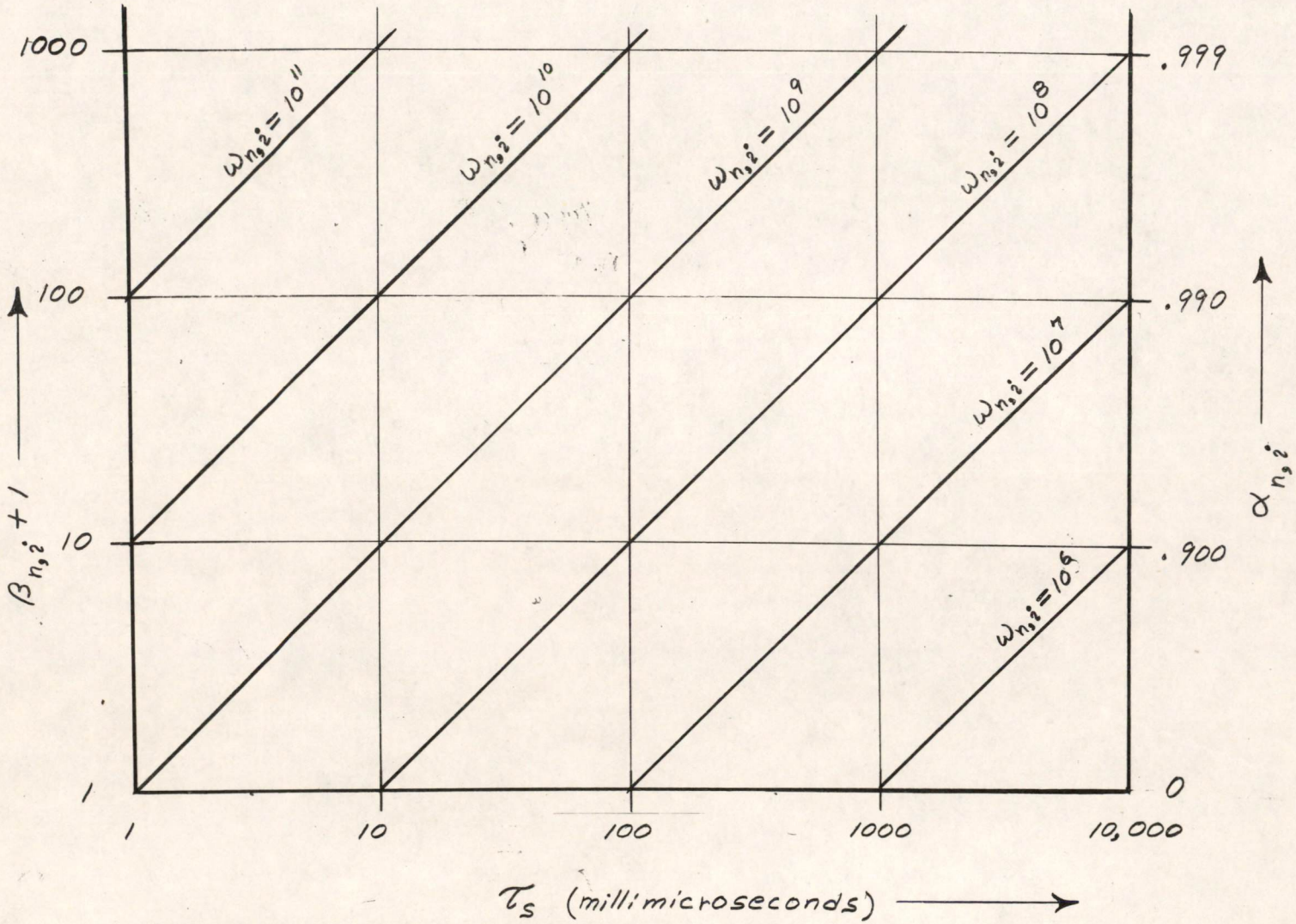

Figure 5. A Plot Showing the Interrelation of the Switching Parameters $\alpha_{n,i}, \beta_{n,i}, \omega_{n,i}$ and τ_s

the actual base width of the transistor, and s, the surface recombination velocity of the free base surfaces.

From the geometry of the one-dimension model, it is clear that

$$\bar{w}_n = \bar{w}_i = w \tag{43}$$

and from (28) we can write that

$$\tau_b \approx \frac{w}{2s} \tag{44}$$

In approximating (28) by (44), we have assumed that the minority carrier bulk lifetime of the base material is much larger than the apparent lifetime due to surface recombination and, therefore, can be neglected.

By substituting the equivalent expressions for $\bar{w}_n$, $\bar{w}_i$, and τ_b given in (43) and (44) into (40), we can relate the basic switching parameters, β_n, β_i, and τ_s, to the design parameters of the one-dimensional transistor, w and s. As a result of this, we obtain that

$$\beta_o = \beta_n = \beta_i = \frac{D_p}{ws} \tag{45}$$

and

$$\tau_s = \frac{w}{2s} \tag{46}$$

where β_o is the d-c common-emitter, short-circuit, current-gain for the one-dimensional transistor.

From equations (45) and (46), we can see that β_o and τ_s are mutually independent. While from a modified form of (41)

$$(\beta_o + 1) = \omega_{c\alpha}\, \tau_s \tag{47}$$

where $\omega_{c\alpha} = \omega_n = \omega_i$,

we are able to express the common-base, α-cutoff frequency, $\omega_{c\alpha}$, as a function of β_o and τ_s alone. As a result of this, we can conclude that the parameters, β_o and τ_s, completely describe the transient switching

characteristics of the one-dimensional, symmetrical-switching-transistor.

By eliminating the parameters, w and s, one at a time from (45) and (46), we obtain two equations, one in which β_o and τ_s are related in terms of w only and one in which β_o and τ_s are related in terms of s only. These equations have the form

$$\beta_o = \frac{D_p}{2s^2} \frac{1}{\tau_s} \tag{48}$$

and

$$\beta_o = \frac{2D_p}{w^2} \tau_s \tag{49}$$

A log plot of (48) and (49) (solid lines) together with (47) (dotted lines) is given in Figure 6. This plot shows graphically the interrelationships between the switching parameters, α_o, β_o, $\omega_{c\alpha}$, and τ_s, and the design parameters, w and s as described by equations (37) and (44) through (49). This graph can be used to determine how various changes in w and s either singly or together affect the switching parameters of the one-dimensional, symmetrical transistor. In the same manner, this graph also shows qualitatively what effect changes in w and s will have on the switching parameters of a non-symmetrical, alloy, switching-transistor described in the previous section of this paper, where, in this latter case, w represents a measure of the actual base width instead of the average path lengths of the holes.

For example, if w is decreased such that the term, $\frac{2D_p}{w^2}$, increases by two orders of magnitude while the surface recombination velocity is maintained constant, then the current gain, β_o, will increase by an order of magnitude and the storage time τ_s will decrease by an order of magnitude. Alternately, if s is increased such that the term, $2S^2/D_p$, increases by two orders of magnitude while the base width is maintained constant, the storage time will decrease by an order of magnitude, as in the previous example, but the current gain will decrease rather than increase by an order of magnitude.

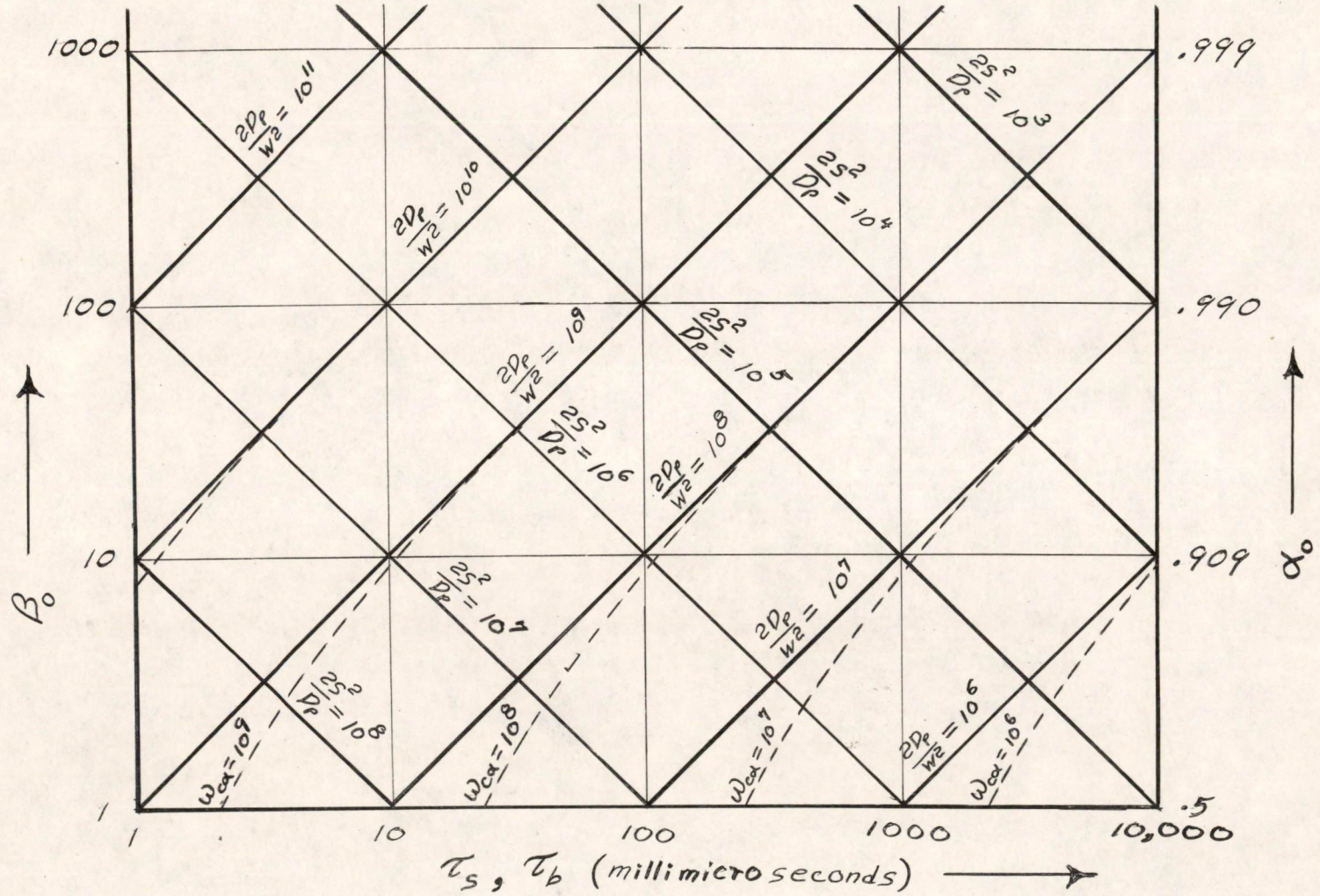

Figure 6.

A Plot Showing the Interrelation of the Switching and Design Parameters of the One-Dimensional Transistor

Supposing, now, we desire to reduce the storage time by an order of magnitude (thereby decreasing the switching time) while at the same time maintaining the current-gain constant. From Figure 6, we can see that this can be done if w is decreased and s is increased in such a manner as to cause each of the terms, $2D_p/w^2$ and $2S^2/D_p$, to increase by an order of magnitude. On the other hand, if we desire to maintain the storage time constant while increasing the current gain by an order of magnitude, then we find from Figure 6 that we must decrease w and s simultaneously in such a manner that the term, $2D_p/w^2$, is increased by an order of magnitude and the term, $2S^2/D_p$, is decreased by an order of magnitude.

In addition to showing how changes in the design parameter, w and s, affect the switching parameters of a transistor as demonstrated by the examples described above, the graph of Figure 6 can also be used to show roughly how the design parameters of different alloy transistors differ in terms of w and s. In the case of a non-symmetrical, alloy, transistor, the values of w and s that would be obtained from the graph of Figure 6 for, say, the normal current-gain, β_n, and the storage time, τ_s, should be interpreted as the design parameters of an equivalent, one-dimensional, transistor, e.i., a one-dimension transistor having the same switching characteristics as the non-symmetrical transistor has when operated in the normal mode. As such, the values of w and s obtained from Figure 6 for ordinary non-symmetrical, alloy, junction transistors should be used for comparison purposes only.

The dotted lines on the graph shown in Figure 6 represent curves of constant $\omega_{c\alpha}$, the α-cutoff frequency in radians per second. Since $\omega_{c\alpha}$ is a function of τ_b and hence the surface recombination velocity, S, (see equations (24) (27) and (44)) as well as the base width, w, the curves of constant $\omega_{c\alpha}$ will not coincide with curves of constant w. As S approaches zero ($\tau_b \rightarrow \infty$), however, the constant $\omega_{c\alpha}$ curves asymptotically approach the curves of constant w.

Summary - Part II

By using some of the relations developed in Part I of this paper, it has been shown that the switching parameters, $\beta_{n,i}$, $\omega_{n,i}$, and τ_s can be interrelated by two equations of the the form

$$(\beta_n + 1) = \omega_n \tau_s$$

$$(\beta_i + 1) = \omega_i \tau_s$$

Furthermore, it has been shown that only three of these parameters are necessary to completely describe the transient switching characteristics of a transistor. From the point of view of simplicity of measurement, the parameter set, β_n, β_i, and τ_s, is discussed in this paper.

In the case of the one-dimensional transistor, it has been shown that only two switching parameters, β_o and τ_s, are needed to describe its switching characteristics and that these two parameters can be related to the transistor's design parameters, w and s, by the equations

$$\beta_o = \frac{D_p}{ws}$$

$$\tau_s = \frac{w}{2s}$$

Using these two relations, we have described how variations in w and s affect the switching properties of the one-dimensional transistor with the idea in mind that the results can be applied, qualitatively at least, toward improving the switching properties of a practical alloy junction transistor.

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