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Record Control # 03-00006
Series 1955-58
Description MIT and Lincoln Lab Memos
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- Memorandum 6M-3971
  Division 6 - Lincoln Laboratory, MIT
  "Component Circuits for Digital-to-Analog Decoders"
  author H.E. Zieman 7/11/55

- Memorandum 6M-3984
  EE Dept. Master's Thesis Proposal 11/9/55
  author L. Jedynak
  "Circuit Application of the Avalanche Phenomenon in Junction Transistors"

- Memorandum 6M-4035
  "Transistor Circuits Course. Number 5. Thermal Stability of Transistors" author D. Eckl 12/2/55

- Memo 6M-4062
  "Design and Static Analysis of Emitter-Follower Inverter Combination" ~~Author~~ author T.H. Meisling
  12/19/55

- Memo 6M-4089
  "Geometry of Magnetic Memory Elements"
  author J. Childress 1/18/56

- Memo 6M-4109 "High Speed Flip Flop" (MTC Model IV)
  author N. Ockene 3/2/56

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- Memo 6M-4110 "Surface Barrier Transistor Life Tests" author D. Eckl + R. Burke 12/14/55

- Memo 6M-437 "Memory Core Heating by Switching at High Frequencies" Author J. Childress 1/31/56

- Memo 6M-4155 Master's Thesis Proposal, K. Konkle 2/10/56 "Hole Storage in a Saturated Grand-Emitter Transistor Circuit"

- Memo 6M-4218 "A Sequential Access Three Microsecond Core Memory" author R. Best and T. Meising 3/8/56

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  S. Coffin 4-3-57

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  R. Johnston ~~1/21/57~~ 2/21/57

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- Memo 6M-4956 "Selective Masking" G. Heidler 4/9/57

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- Memo 6M-4789 "A Functional Description of the TX-0 Computer" J. Gilmore, H. Peterson 11/20/56

- Memo 6M-4968 "The Lincoln TX-2 Computer" 4/1/57 W. Clark, J. Frankovich, H. Peterson, J. Forgie, R. Best, K. Olsen

- Memo 6M-5097 "TX-0 Direct Input Utility System" J. Gilmore 4/10/57

- Memo 6M-5780 "Some Examples of TX-2 Programming" H. Peterson 7/23/58

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- Memo 6M-5649 "Remote Display I" H. Zieman 6/2/58

- Memo 6M-5780 "Some Examples of TX-2 Programming" H. Peterson 7/23/58

FOLDER 13

Engineering Drawings
- Assy, Composite, Schematic PIV, Decoder Power Unit, TX-2
- " " " " 8 Transistor Emitter Follower, TX-2
- Remote Display Flip Flop Plug In
- Remote Display Blocking Oscillator

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- Remote Display Inverter Pkg
- " " Gate Pkg
- " " Selector Driver
- Circuit schematic, power room, power control panel TX-0
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- Cascode and Cable Driver, TX-2
- Series (8R) Inverter, TX-2
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Engineering Drawings

- Parallel (7) Inverter TX-2
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- Memory Selector TX-2
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- Block Schematic MTC Alarm System, K
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- TX-2 D Register Digits 0, 1, 2
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- Lincoln Transistorized Multiple Sequence Computer (LITMUS)
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- IBM Card Machines, Write Operation
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- IBM Console Selector Unit
- "Proposal for Block Symbols + Diagrams"
- IBM Left Arithmetic Element
- " " " " One Digit Column
- Circuit Schematic Register Driver
- KO drawing "Single Digit Adder"
- KO drawing "4 Position Magnetic Matrix Switch" 2/26/52
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- " " "Blocking Oscillator Stepping Register"
- " " "Flux Current Plotter" 4/19/52
- " " "Core Driving Flip Flop" 6/23/50
- " " "Sensing Amp, Ceramic Array II" 5/19/52
- " " "Ceramic Memory Array II" 4/4/52
- " " "Magnetic Matrix Switch II (Alternate) 4/4/52

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SUBJECT: Component Circuits For Digital-To-Analog Decoders.

To: N. H. Taylor and Group 62

From: Henry E. Zieman

Date: July 11, 1955

Approved: C. L. Corderman
C. L. Corderman

Abstract:

A digital-to-analog decoder is a circuit which converts digital information to a quantized voltage. The decoders discussed consist of four basic circuits: a voltage reference source, a constant current source, a current gate tube, and a decoder ladder. Each of these circuits is described in detail with typical operating values for the evaluation and maintenance of each circuit. Detailed analysis of a variably terminated push-pull decoder ladder is included showing the advantages of this ladder over the standard terminated single-sided ladder discussed by Walquist in R220. A second report (6M-3915) discusses three complete decoders in which these component circuits are used.

1.0 General

A Digital-To-Analog decoder is a circuit which transforms digital information in the form of flip-flop levels to a quantized analogue voltage which, through suitable amplification, can be used to deflect an electron beam in a cathode ray tube. Figure 1a (SA47174) shows a block diagram of a typical balanced decoder stage, or bit. Voltage reference source (R) acting on a current source ("CUs") produces a regulated source of current. This current can then be switched through either one of two current gate tubes ("CGT") into a ladder section ("LS") by an appropriate flip-flop level on the CGT input.

The inputs to the two current gate tubes are connected to opposite sides of a single flip-flop. Thus one input will be at +10 volts while the other will be at -30 volts. The current gate tube whose input is at +10 volts will conduct current from the current source to the ladder section connected to it. The companion gate tube will be completely cut off.

The

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

The ladder sections are resistive networks connected to a common supply voltage. As current passes through a ladder section, an output voltage is produced in this section in a negative direction from the supply voltage. Simultaneously the current in the companion ladder section is cut-off, and its output voltage approaches the supply voltage. If the output is taken across the output terminals of both ladder sections the output will be a push-pull signal whose amplitude is twice the swing of a single ladder section.

In a multi-stage decoder the various ladder sections are connected in series as shown in fig. 1b (SA47174). It will be shown that a property of this connection is to weigh the output of each individual section in a binary fashion. That is, for a given current flowing successively in sections 1, 2, and 3, section one will produce the greatest effect on the output, section two only one half the effect of section one, and section three only one quarter the effect of the first section.

2.0 Specific Component Circuits

2.1 Voltage Reference Source (R)

Figure 2 (SA63288) shows the block symbol and circuit diagram of the voltage reference source. Drawings 3006898, 3006899, 3007706, and 3007707 show the required card assemblies and details to make up the circuit.

The circuit on card assembly 3006898 functions as the primary voltage regulator and has a control pot (R3) which will permit setting the output of the circuit to 160 volts across R1, despite normal variations in the output voltage of the reference tubes V_1 and V_2 on this card. Because of manufacturing tolerances and aging the operating voltages at (H) will be $86^v \pm 5^v$ referred to the -300v supply line, while point (G) will be $172^v \pm 10^v$. Thus for the extreme conditions on (G) the control pot can vary e_{R1} between 139^v to 162^v and 156^v to 182^v. The 160^v across R1 can therefore be realized at all times.

Card 3007706 functions as a secondary regulator to reduce variations in the supply voltages to card 3006898. In both circuits the 1M 1/2W resistors are used to insure proper firing of the VR tubes. Table 2.1 gives pertinent data for the evaluation and maintenance of this circuit.

Table 2.1a

Voltage Measurements (referred to ground)

Point	Voltage	Point	Voltage
A	$+250^{V} \pm 5^{V}$	F	$-299^{V} \pm 6^{V}$
B	$+45^{V} \pm 18^{V}$	G	$-127^{V} \pm 11^{V}$
C	$-41^{V} \pm 15^{V}$	H	$-213^{V} \pm 9^{V}$
D	$-127^{V} \pm 12^{V}$	J	-139 ± 6^{V}
E	$-213^{V} \pm 9^{V}$		

Table 2.1b

Component Loading

Component card 3006898	Voltage (in volts)	Current (in ma.)	Max. Power (in watts)
R_1 150K 1w 1%	160	1.07 ± .01	0.173
R_2 56K 2w 1%	172 ± 17	3.08 ± .34	0.646
R_3 25K pot	11 ± 5	1.07 ± .01	0.42 rating required
R_6 1M 1/2w 5%	86 ± 3	.086 ± .007	0.0081
V_1 5783 WA	86 ± 2	2.01 ± .35	0.208
V_2 5783 WA	86 ± 3	1.93 ± .36	0.204
card 3007706			
R_1 75K 2W 1%	205 ± 23	2.73 ± .33	0.698
R_2 68K 2W 1%	205 ± 23	3.02 ± .37	0.773
R_3 1M 1/2W 5%	172 ± 6	.172 ± .014	0.0331
R_4 1M 1/2W 5%	86 ± 3	.086 ± .007	0.0081
V_1 5783 WA	86 ± 3	2.67 ± 1.04	0.330
V_2 5783 WA	86 ± 3	2.67 ± 1.04	0.330
V_3 5783 WA	86 ± 3	2.59 ± 1.05	0.324
V_4 5783 WA	86 ± 3	2.51 ± 1.06	0.325

Table 2.1c

Power Supply Requirments

Voltage	Current	Power
+250	5.75 ± .70ma	1.44w
-300	5.75 ± .70ma	1.73W

Figure 3 (SA 48619-G) shows the behaviour of this circuit as the -300^V marginal check line is varied. It will be noticed that the output across R_1 remains within 0.1 $^o/_o$ while the marginal check line is varied from $-300^V \pm 31^V$. In this region the output varies at a rate of .01$^o/_o$ for every 1$^o/_o$ change of the marginal check voltage. This gives a transfer function $\Delta eo/\Delta emc = 0.00355 = K1$. This value of K1 also holds for low frequency noise in either the -300^V line or the $+250^V$ line. As the -300^V in the further reduced, the current through V3 and V4 on the card 3007706 is eventually reduced to a point where the tubes can no longer sustain conduction. This has occurred in the circuit under test at -197^V. Beyond this point the output varies at a rate of .05$^o/_o$ for each 1$^o/_o$ change in the -300^V line, giving a transfer function $\Delta eo/\Delta_{emc} = 0.0265$. Once V_3 has been extinguished, the marginal check line must be returned beyond the point at which V_3 extinguished before sufficient voltage is available to re-ignite V_3. In the circuit under test this occurred at -230^V. It is to be understood that the variations on this MC line are not intended to marginal check this circuit. The variation will be used to marginal check the current source tubes. Hence, this study is intended to check whether the reference is sufficiently constant for the marginal check to be a valid indication of failure of the current source tubes. The only indication of failure of this circuit is the inability to adjust e_{R1} to 160^V. This voltage will have to be checked periodically and when the range of adjustment on R1 becomes critically small the circuit should be removed from service and repaired.

2.2 Current Source Circuit (CU_s)

Figure 4 (SA 63702) shows the block symbol and circuit diagram of the current source circuit. Drawings 3006893, 3006894, 3006896, 3006897, 3006908, 3006913, 3006914 shows the necessary card details and assemblies to make up the circuit with its necessary variations.

The constant current source is essentially a cathode follower with a fixed voltage applied to its grid. By definition a constant current source will supply a fixed current despite variations in load voltage. Therefore, a figure of merit for a constant current source is its dynamic output impedance (or equivalent resistance) $\Delta eo/\Delta io$ (in conjuction with the voltage reference source). It can be shown for this circuit (see Appendix A) that

$$Req = \frac{\Delta eb}{\Delta ib} = \frac{rp + (\mu+1) Rk}{\quad + \mu K1} \qquad eq\ 2.21$$

From this equation it can be seen that for a given change in output voltage, Req should be as high as possible to minimize the change in current.

$$\Delta ib = \frac{\Delta eb}{Req} = \frac{\Delta\ eb\ (1 + \mu K1)}{rp + (\mu+1)\ R_k}$$

A quantity which is related to the circuit equivalent resistance is the circuit equivalent voltage. For this circuit:

$$E\ eq = ib\ Req \qquad eq.\ 2.22$$

Considering equations 2.21 and 2.22 it is found that the circuit is optimized by making R_k as large as possible. However, rise time considerations in the later circuits will limit the size of R_k if the available minus supply voltage is fixed. These considerations have dictated that the cathode resistance should be about 30K. Therefore, a current source with a 27K cathode resistor in series with a 5K variable resistor is considered a unity current source. In certain special decoders two additional values of current are required: one to give 1 1/8 unity current and a second to give 3/4 unity current. These are obtained by changing the fixed 27K cathode resistor to 24K and 36K respectively.

In each decoder one current source has a fixed 2.4K resistor in series with the 27K resistor (RK). This current source is then considered a reference current source and all other current sources can be adjusted with the 5K pot to give the same current as the reference current source, or the required proportionate amount. This adjustment is most easily carried out by connecting one side of a sensitive voltmeter to point E on the reference current source and the second side to point E on the variable current source under adjustment; then adjusting the pot until the voltage reads zero. This guarantees that the voltage across each R_k is equal, and since these are 1% resistors the current through the variable current source is within 2% of that in the reference current source. To adjust these currents more accurately a special procedure will be needed to emphasize any inaccurracies in adjustment, and final trimming will have to be made by comparing the decoder output to a very accurate calibration signal. This procedure will be written up in more detail in an IBM Technical Report by J. Seeland.

From section 2.1 we have $K_1 = 0.0035$ for variations in the -300^V line, and $K_1 = 0$ for variations in the +10 volt level of the plate. Using these and the above values for R_k and the following values for tube parameters μ=46, rp=10k, we get two sets of values for R eq and E eq. These values plus other pertinent data for the evaluation and maintenance of this circuit are presented in table 2.2.

Table 2.2a

Voltage Measurements (Fig 4)

Points	Voltage in volts	Point	Voltage in volts
A	-298±6	D	-138 ± 7^V
B	-139±6	E	-150 ± 7^V
C	+10 ±4		

Table 2.2b

Component Loading

Component Unit current source	Voltage in volts	Current in ma.	Max Power in watts
RK = 27K2W1%	148 ± 1	5.485 ± .095	0.83
R_2 = 2.4K 1W 1%	13.2 ± .3	5.485 ± .095	0.074
R_2 = 5K Pot	13.2 ± 2.3	5.485 ± .095	0.16 (required)
V_1 = Z2177	148 ± 9	5.485 ± .095	0.88
e_g = (bogey bias)	1.8^V minimum gm = 28% of bogey		
3/4 current source			
R_k = 36K2W 1%	148 ± 1	4.115 ± .065	0.63
R_2 = 5K Pot	13.2 ± 2.3	4.115 ± .065	0.09 (required)
V_1 = Z2177	148 ± 9	4.115 ± .065	0.66
e_g (bogey bias)	2.1^V minimum gm = 21% of bogey		
1 1/8 current source			
R_k = 24k 2w 1%	148 ± 1	6.17 ± .11	0.94
R_2 = 5k Pot	13.2 ± 2.3	6.17 ± .11	0.2 (required)
V_1 = Z2177	148 ± 9	6.17 ± .11	0.99
e_g (bogey bias)	1.7^V minimum gm = 31% og bogey		

Table 2.2c

Power Supply Requirements

+250^V (indirectly) α 4.12 ±.06 ma, 5.48 ±.1 ma, 6.17 ±.11 ma

-300^V α 4.12 ± .06 ma, 5.48 ± .1 ma, 6.17 ± .11 ma

6.3^V AC α .45 amp/2 current sources biased at -150^V

Table 2.2d

Transfer Functions

Current Source	-300^V line variations		+10^V plate variations	
	Req in megohms	Eeq in kilovolts	Req in megohms	Eeq in kilovolts
3/4 = 4.115 ma	1.44	5.93	1.80	7.50
1 = 5.485 ma	1.11	6.00	1.39	7.56
1 1/8 = 6.170 ma	1.00	6.02	1.25	7.58

To insure proper operation of this current source it is important to insure that no grid current flows. Since the regulated current is actually the cathode current, any grid current which flows subtracts from the plate current. However, since the required regulated current is not the cathode current but the plate current, the grid current must be kept to a negligible quantity. In a Z2177 the grid current at zero bias is about 10 μa. which is about 0.2 % of the regulated plate current, but increases rapidly beyond this point. The zero bias point can therefore be used as a limit of operation. The other limit is determined by the maximum allowable plate voltage, which is 200 volts. Thus, the limits of operation on the plate with the marginal check at -300^{V} are $+60^{V}$ to -95 volts for a bogey tube. The limits on the marginal check line, with the plate at $+10^{V}$, are -205^{V} to -360^{V}.

Figures 5, 6, 7, 8, 9, 10 (SA48613-G, SA48617-G, SA48614-G, SA48615-G, SA 48618-G, and SA 48616-G respectively) show the behavior of these various constant current sources as the -300^{V} marginal check line is varied. Figures 5, 7, and 9 show the variation in the "constant" current of each source as the mc line is varied and the plate voltage is held constant at +10 volts. Figure 5 emphasizes the effect of a "down" tube by substituting for the Z2177 a 6072 which has approximately 25% of the perveance of a Z2177. (25% of the plate current under same conditions of plate voltage and grid current.) Figures 6, 8 and 10 show the change in plate voltage necessary to maintain a constant current within given limits as the MC line is varied. It will be noticed in all of these cases that the current remains constant within 0.1% for normal variations of the -300^{V} line ($+6^{V}$). Since variations of less than 1% will not produce appreciably noticable effects in the display, the marginal check line will probably have to be raised 30 or 40 volts to pick out weak tubes. Assuming that the MC line is raised 30 volts the minimum perveance to cause failure would be 27%, and 36%, and 40% respectively for the 3/4, 1, and 1 1/8 current sources. Thus, the 30 volt excursion would pick out tubes which are within 29% of failure under normal operating conditions.

Figures 5, 7, and 9 also show the effect of grid current. The increased slope in the plate current curve in the vicinity of -230 to -240 volts is caused by grid current replacing the plate current in the "constant" cathode current.

2.3 Current Gate Tube (CGT)

Figure 11 (SA 63717) shows the block symbol and circuit diagram of the current gate tube. Since the circuit contains only a tube and no other components, no special cards are needed for this circuit. However, the following card drawings show the necessary leads to make connections to this circuit: 3006893, 3006894, 3006908, 3006911.

Two current gate tubes are always operated in parallel with their cathodes tied together to a constant current source. The constant surrent source requires that current must flow constantly from one CGT or the other, or both. If the grids were at exactly the same potential and if the tube characteristics were always identical then the current would split equally between these tubes. However, if these conditions cannot be guaranteed then the amount of current through each tube is indeterminate unless it can be guaranteed that no current flows through one tube. This is the case that is used by connecting the CGT's to opposite sides of a single flip-flop. In this case if we assume that point A (Fig. 11) is at +10 volts, then point D will be at -30^V. Under this condition Va will conduct and point B will be at $+10^V$ plus the necessary bias required by the voltage at point C and the current being conducted. In all cases point D will be at least 35 volts negative to B so that Vb will be completely cut off. The exact bias on Va cannot be specified because it depends on the voltage at C which, in turn, depends on the position of the CGT in a given ladder and on the number of bits which are simultaneously conducting. Curves are presented in section 2.4 which specify this voltage for several special cases. In general this variation will fall within the range of $+150^V \pm 50^V$.

The figure of merit for this circuit is similar to that of the constant current source: that is, a measure of the variation of "constant" current for various voltage inputs is required. Since the current source acts as buffer for variations in the -300^V line, and the current gate tube acts as a cathode-follower to the current source for flip-flop inputs, the equivalent resistance for this circuit to -300^V and $+10^V$ variations is the same as for the current source, namely

$$R \text{ eq} = \frac{(\mu+1)\ Rk + rp}{1 + \mu K_1} \qquad \text{(eq 2.21)}$$

where $K_1 = 0.0035$ for $+250^V$ and -300 variations and $K_1 = 0$ for $+10^V$ variations; μ, rp, and R_k refer to the values of the current source feeding this current gate tube.

For variations in the plate voltage of the current gate tube we can use the above equation with R_k equal to the equivalent resistance of the current source to variations in the $+10^V$ level.

$$R \text{ eq} = (\mu_1 \mu_2 + \mu_1 + \mu_2 + 1) R_k + (\mu_2 + 1) rp_1 + rp_2 \qquad \text{(eq 2.31)}$$

where μ_1, R_k refer to the values of the current source, and μ_2, rp_2 refer to the values of the current gate tube. For $\mu_1 = \mu_2$, $rp_1 = rp_2$

$$R \text{ eq} = (\mu + 1)^2 R_k + (\mu + 2)\ rp \qquad \text{(eq 2.32)}$$

In Section 2.4 it is shown that noise on the +250° line appears directly on the plates of the CGT. For these noise signals equation 2.32 must be modified to include the effect of this noise on the voltage reference source.

$$R\ eq = \frac{(\mu+1)^2\ Rk + (\mu+2)\ rp}{1 + \mu K1} \quad (eq\ 2.32a)$$

Table 2.3d shows the calculated values of Req for variations in -300^V, $+10^V$, and $+250^V$ lines using $\mu_2 = 40$, $rp_2 = 10K$. These can then be compared to the measured values shown in figures 12, 13, and 14 (SA 48610-G, SA 48609-G, SA 48611-G respectively).

The importance of grid current is emphasized if figure 12, 13, and 14 in the vicinity of $+80^V$. The Req becomes considerably lower in this region so that the regulation deteriorates very rapidly. This reduction is the result of grid current which reduces the plate current by an equivalent amount. Figure 13 further emphasizes the effect by substituting a 6072 for a Z2177 to show the effect of a lower perveance, and consequently introducing grid current at a higher plate voltage.

This effect of grid current can conveniently be used to marginal check this circuit. If the +250 volt line is lowered, the signal voltage on each tube plate will be lowered by an equivalent amount because of the constant current being drawn. If this voltage is lowered to a point where the operating voltage on all tubes is still slightly above the point of grid current, only a negligible effect on the plate current will be noticed. However, if a tube is below specs it will begin to draw grid current and the plate current will change by an equivalent amount. This effect is then reflected in a change in the output voltage of the decoder.

An effect similar to grid current is produced by plate current in the cut-off companion gate tube. It had been tacitly stated earlier that the cut-off bias on the circuit would be a minimum of 35 volts. However, if the input deteriorates from its $+10^V$ and -30^V levels it could happen that the cut-off tube might not have enough bias to completely cut off. With a weak-on tube the cathode of both tubes will be at the same potential as the input to the on-tube. Under this condition the cut-off bias on the companion tube is exactly equal to the difference in input levels. The exact minimum value of this difference can not be determined because the cut-off characteristics of the tube are not controlled to the degree required. However, a test of a representative group of tubes indicates that 13 volts bias will cut off 97°/o of the tubes tested to within 10 μa. This indicates that with the inputs deteriorated to a difference of 13 volts, the "on" tube should still conduct 99.8°/o of its nominal current. By limiting the minimum difference between inputs to 20 volts we should not expect any difficulty from this source.

The input impedance of this circuit is entirely capacitive but varies in magnitude depending on the state of the tube. Neglecting wiring capacity, there are three states during which the capacity differs. The first state occurs in the region between +10^{V} input and the start of current transition between companion tubes. During this time the cathode essentially follows the grid but the plate remains constant because of the constant current source. At this time the only capacity of importance is the grid to plate capacity of the tube. The second state occurs during transition. At this time the cathode remains essentially fixed but the plate voltage varies depending on the gain of the tube. At this time the capacity is highest being equal to the grid to cathode capacity plus Miller capacity. The third state occurs between -30^{V} and the start of current transition from a negative approach. At this time the plates are again constant but the cathode follows the grid of the companion tube. The capacity at this time is essentially the grid to plate capacity plus twice the grid to cathode capacity. The calculated values of capacity for states 1, 2, and 3 are respectively 3, 36, 11 μμf. Measured values of capacity necessarily include the wiring capacity in the plug-in-unit and the integrated effect of all three states. The measured value was 12 μμf ± 20%.

Table 2.3 presents pertinent information for the evaluation and maintenance of this circuit.

Table 2.3a

Voltage Measurements (Fig. 11)

Point	Voltage in volts	Point	Voltage in volts
A	+10 ± 2^{V} (or -30 ± 2^{V})	D	-30 ± 2 (or +10 ± 2)
B	+11.5 ± 3.5	E	+150 ± 50
C	+150^{V} ± 50		

Table 2.3b

Component	Voltage in volts	Current in ma	Max. Power in watts
Z2177 "on" section			
Plate to cathode	143 ± 43	4.115 ± .065	0.78
	140 ± 40	5.485 ± .095	1.0
	139 ± 39	6.17 ± .11	1.1

Component	Voltage in volts	Current in ma	Max. Power in watts
"ON" SECTION			
grid to cathode	-1.5 ± 1.5	0	0
"OFF" section			
Plate to cathode	+150 ± 50	0	0
grid to cathode	-40 ± 5V	0	0

Table to 2.3c

Power Requirements

6.3V ac at .45 amp/2 CGT biased at ground

Table 2.3d

Transfer Functions

Voltage Source having noise	Req (in megohms) 3/4 current source	Unit current source	1 1/8 current source
+250	71.0	54.4	49.0
+10 (input signal)	1.80	1.39	1.25
-300	1.44	1.11	1.00

2.4 Decoder Ladder

Figure 15a (SA 63878) shows the block symbol and circuit diagram of a single ladder section. Figure 15b shows how a number of these sections are tied together to make up a push-pull decoder ladder. Drawings 3006-895, 3006898, 3006899, 3006902, 3007694, show the necessary card details and assemblies to make up a decoder ladder and its gain control.

To study the steady state response of a general push-pull ladder it is convenient to analyze it by use of symmetrical components. It will be slightly easier to visualize the behavior of this circuit by redrawing it in the form shown in figure 16a (SA-63879). In this circuit current gate tube #0 (CGT-0) will switch a current I_0 between a_0 and b_0, CGT-1 will switch I_1 between a_1 and b_1, and CGT-j will switch I_j between a_j and b_j. To consider this circuit symmetrically, we will have to break I_j into two components, the common mode $I_{jcm} = I_j/2$ going into both a_j and b_j continuously, and the differential mode $I_{jdm} = I_j/2$ going into a_j and out of b_j, or the reverse.

Considering only the common mode response of this circuit (figure 16a), it is easily seen that $E_1 = E_2$ and $E0 = 0$. For this condition no

current exists in KR and the circuit can be simplified to that shown in figure 16b. In this case the voltage at any terminal aj due to a current I_{cmj} alone is simply this current multiplied by the impedance presented by the ladder to this point. In appendix B it is shown that this impedance for terminal aj is

$$R_{jcm} = \frac{2RL}{3}\left(\frac{2^{2j-1}+1}{2^{2j-1}}\right) + 2R_d \qquad \text{eq 2.41}$$

Thus the voltage at any terminal aj due to the current I_{jcm} is

$$E_{jj} = 2\, I_{jcm}\, Rd + \frac{RL}{3}\,\frac{(2^{2j-1}+1)}{2^{2j-1}}$$

Since $I_{jcm} = I_j/2$

$$E_{jj} = I_j\left[Rd + \frac{RL}{3}\left(\frac{2^{2j-1}+1}{2^{2j-1}}\right)\right] \qquad \text{eq. 2.42}$$

To consider the total common mode voltage at terminal aj we must also consider the effect on a_j by currents in all other terminals ($\sum IgRg + \sum ImRm$). Considering first the effect of currents I_g at terminal a_g where $g < j$, the voltage of a_g is

$$E_{gg} = I_g\left[Rd + \frac{RL}{3}\left(\frac{2^{2g-1}+1}{2^{2g-1}}\right)\right] \qquad \text{eq 2.42a}$$

Since only a fraction of this voltage will appear at a_j, it is shown in appendix C that the voltage at a_j due to a current at a_g is

$$E_{jg} = I_g\left[Rd + \frac{RL}{3}\left(\frac{2^{2g-1}+1}{2^{j+g-1}}\right)\right] \qquad \text{eq 2.43}$$

Similarily the voltage at a_j due to a current in a_m where $m > j$ is shown to be

$$E_{jm} = Im\left[Rd + \frac{RL}{3}\left(\frac{2^{2j-1}+1}{2^{j+m-1}}\right)\right] \qquad \text{eq 2.44}$$

The common mode voltage at a_j due to currents in all terminals is, by superposition

$$E_{jcm} = E_{jj} + \sum_{g=0}^{g=j-1} E_{jg} + \sum_{m=j+1}^{m=n} E_{jm}$$

Substituting equation 2.42, 2.43, and 2.44 and simplifying gives

$$E_{jcm} = \sum_{g=0}^{g=n} I_g \left[Rd + \frac{RL}{3} \left(\frac{1}{2^{j+g-1}} + \frac{1}{2^{|j-g|}} \right) \right] \qquad \text{eq 2.45}$$

Considering the differential mode, a similar line of reasoning can be followed.

The impedance presented by the ladder to any terminal a_j is (See Appendix B)

$$R_{jdm} = \frac{2RL}{K+2} \left[\frac{(2^{2j-1}+1)(K+2)-3}{3 \times 2^{2j-1}} \right] \qquad \text{eq 2.46}$$

The voltage at terminal a_j due to the current in this terminal is

$$E_{jj} = \frac{IjRL}{K+2} \left[\frac{(2^{2j-1}+1)(K+2)-3}{3 \times 2^{2j-1}} \right] \qquad \text{eq 2.47}$$

The voltage at terminal a_j due to a current IN terminal a_g where $g < j$ is (See Appendix C)

$$Ejg = \frac{IgRL}{K+2} \left[\frac{(2^{2g-1}+1)(K+2)-3}{3 \times 2^{j+g-1}} \right] \qquad \text{eq 2.48}$$

The voltage at a_j due to a current in a_m where $M > j$ is (See Appendix C)

$$E_{jm} = \frac{ImRL}{K+2} \left[\frac{(2^{2j-1}+1)(K+2)-3}{3 \times 2^{j+m-1}} \right] \qquad \text{eq 2.49}$$

The voltage at a_j due to currents in all terminals is

$$E_{dmj} = E_{dmjj} + \sum_{g=0}^{g=g-1} E_{dmjg} + \sum_{m=j+1}^{m=n} E_{dmjm}$$

Substituting equations 2.47, 2.48, and 2.49 in the above and simplfying gives

$$E_{jdm} = \sum_{g=0}^{g=n} \frac{IgRL}{3} \left[\left(\frac{K-1}{K+2} \right) \frac{1}{2^{j+g-1}} + \frac{1}{2^{|j-g|}} \right] \qquad \text{eq 2.410}$$

The total voltage at any terminal is the sum of the common mode and difference mode signals subtracted from the positive supply voltage. Since the difference mode may be either positive or negative depending on the setting of the input signal, the differential mode current is either positive or negative. However, to simplify the resulting expression we can consider the current always positive and associate the reversal of sign with the impedance term.

$$Ej = Ebb - Ejem \pm Ejdm$$

Substituting equations 2.45 and 2.410 we get

$$Ej = Ebb - \sum_{g=0}^{g=n} Ig\left\{Rd + \frac{RL}{3}\left[\frac{(K+2) \pm (K-1)}{(K+2)\,2^{j+g-1}} + \frac{1 \pm 1}{2^{|j-g|}}\right]\right\} \quad \text{eq. 2.411}$$

The minimum voltage at any terminal a_j will occur when all currents are flowing through one side of the decoder ladder. In this case we can use the plus signs in eq 2.411 to get,

$$Ejmin = Ebb - \sum_{g=0}^{g=n} Ig\left\{Rd + \frac{RL}{3}\left[\frac{2K+1}{(K+2)\,2^{j+g-1}} + \frac{2}{2^{|j-g|}}\right]\right\} \quad \text{eq. 2.412}$$

Similarly the maximum voltage will be of interest and can be derived by using the minus signs of eq. 2.411

$$Ejmax = Ebb - \sum_{g=0}^{g=n} Ig\left\{Rd + \frac{R_L}{(K+2)\,2^{j+g-1}}\right\} \quad \text{eq. 2.413}$$

The binary weighting properties of this ladder can now be proven by determining the maximum push-pull differential output of the ladder. Setting $j = 0$ in equations 2.412 and 2.413 we have

$$Eod = 2\,(Eomin - Eomax)$$

$$Eod = \frac{4\,R_L K}{K+2} \sum_{0}^{n} \frac{I_g}{2^g} \quad \text{eq. 2.414}$$

The term $\frac{I_g}{2^g}$ emphasizes the binary weighting property of this ladder despite the variation of the terminating resistor.

For most decoder purposes the current to all bits is the same ($I_g = I$) with the exception of an additional common mode current (I_L) drawn by the load attached to the decoder. Under this condition several of the preceding equations can be simplified. (See Appendix D)

$$E_{jmin} = E_{bb} - \left[I_L+(n+1)I\right] R_d - 2IR_L - \frac{I_L R_L}{2^j} - \frac{2IR_L}{K+2}\left\{Kx2^{-j} - \frac{1}{3x2^n}\left[(K+2)2^j+(2K+1)2^{-j}\right]\right\}$$

EQ. 2.412a

$$E_{omin} = E_{bb} - \left[I_L+(n+1)I\right] R_d - (2I+I_L)R_L - \frac{2IR_L}{K+2}\left(K - \frac{K+1}{2^n}\right) \quad \text{EQ. 2.412b}$$

$$E_{jmax} = E_{bb} - \left[I_L+(N+1)I\right] R_d - \frac{R_L}{2^j}\left[I_L + \frac{2I}{K+2}(2-2^{-n})\right] \quad \text{EQ. 2.413a}$$

$$E_{omax} = E_{bb} - \left[I_L+(n+1)I\right] R_d - R_L\left[I_L + \frac{2I}{K+2}(2-2^{-n})\right] \quad \text{EQ. 2.413b}$$

$$E_{od} = \frac{4IR_LK\ (2-2^{-n})}{K+2} \quad \text{EQ. 2.414a}$$

In general use it is necessary to amplify the output of a decoder. (See 6M-3284 for a typical amplifier) To reduce the complexity of this amplifier it is desirable to produce as large an output from the decoder as possible. One of the governing factors in the allowable output swing is the bounded limit on the voltage across the current gate tube. The maximum voltage across the tube is dictated by the manufacturer, while the minimum voltage is restricted by the bias condition of the tube. The requirement that the grid current shall not be more than a given percentage of the plate current automatically limits the minimum plate voltage for any given current.

It has been shown in Walquist's Report (R220) that for an infinite decoder ladder terminated in its characteristic impedance and having all its current sources equal, the maximum voltage at the various bits varies, reading a maximum at the center of the ladder, where it is 50% greater than at the output. Since this point then has the minimum voltage across the current gate tube, the output voltage is only 67% of the maximum attainable if the full tube swing could be used at the output. By increasing the output termination it is possible to arrange the maximum voltage distribution along the ladder so that the maximum voltage will occur at the most significant bit. Since the output is taken from this bit, this will insure that the maximum possible output can be obtained. The necessary amount of increase in the termination can be calculated for the case of a decoder having equal currents going to all its bits by using equation 2.412a. (See Appendix D)

$$K \geq -2^{-n} \quad \text{eq. 2.415}$$

Since this term is always negative, any terminating resistor used in figure 15b will insure that the minimum plate voltage will appear at the output tube. This in turn insures that the maximum possible output can be obtained from the decoder when this output is limited by the voltage swing on any plate.

These results apply to push-pull decoders directly. Equation 2.415 can be extended to include single sided decoders by assuming a variable termination of MR (where R is nominal resistance of that decoder). Considering the similarity between a variably terminated single-sided decoder and the push-pull decoder shown in Figure 16A with all current sources conducting on only one side, the two resultant terminations can be equated.

$$MR = 2KR + 2R = 2(K+1)R$$

$$M = 2(K+1)$$

$$M \geq 2(1-2^{-n})$$

eq. 2.415a

Several typical decoders are discussed in 6M-3915 (Push-pull Display Decoders in XD-1). Figures 17 and 18 (SA 48620-G and SA 48623-G) show the typical behavior of one of these. This is a three stage decoder using nominal currents of 5.45 ma. a nominal ladder resistance of 5600 ohms, a dropping resistor Rd of 1640 ohms, and a B supply of 244 volts. The output of the decoder is also loaded with an amplifier whose equivalent input circuit consists of a 235K resistor from each input terminal to a -150 volt supply.

Applying these values to equations 2.412a, 2.413a, and 2.414a gives:

$$E_{J\,min} = 152 + 5.08 \times 2^{J} - \left[14.06 + 5.08\left(\frac{10K-1}{K+2}\right)\right] 2^{-J}$$

$$E_{J\,max} = 213 - \frac{5.6}{2^{J}}\left(2.51 + \frac{19.1}{K+2}\right)$$

$$E_{od} = 214\,\frac{K}{K+2}$$

Figure 17 shows how these voltages vary as a function of the terminating resistor and the position of the current gate tube in a ladder. For E_j min: j = 0 for V9a. j = 1 for V7a, and j = 2 for V6a. For E_j max: j = 0 for V9b. j = 1 for V7b. and j = 2 for V6b. Figure 18 shows how the output voltage varies as a function of the terminating resistor.

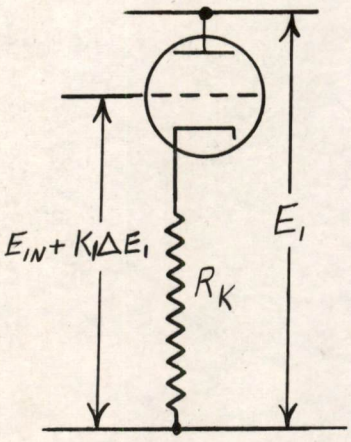
Equation 2.412 shows the feasibility of using the B+ supply as a means of marginal checking the current gate tube. Any variation on this line appears directly on the plates of all the current tubes so that the plate voltage can be reduced below its normal operating level whatever that may be, by lowering the B+ supply by an equivalent amount.

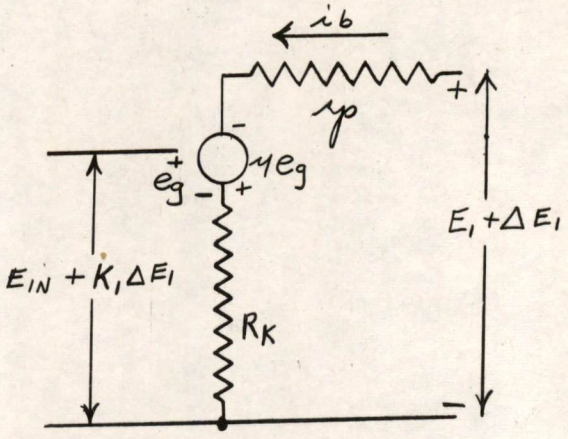
There is no direct method of marginal checking the ladder sections. It has been shown in Walquist's Report that variations in the ladder resistors affect the output linearly and can be compensated for by re-adjusting the current sources. This adjustment is therefore an indication of the state of the ladder resistors as well as the current source cathode resistors. If the range of adjustment on the current source tubes becomes critically small, the ladder resistors and current source cathode resistors must be checked.

Experiments have shown that a delay line effect exists in the decoder ladder, apparently caused by the output capacity of the current gate tubes. This effect can be emphasized by operating the decoder in the following manner. First all bits are set in a fixed position except the least significant bit. This bit is then switched at a 100 KC rate by the output of a flip-flop and the rise time characteristic noted. Figure 19a (SA 48709) shows the result of this experiment on the above mentioned decoder showing especially the rise time and the exponential nature of this rise time. Secondly all bits are connected to the same flip-flop, with the most significant bit connected in the "1" position and all others connected in the "0" position. With no delays present, the output rise time characteristics and magnitude should appear exactly the same as in the first part of the experiment. Figure 19b (SA 48709) shows the result of this experiment. The large overshoot is caused by the signal of the most significant bit appearing at the output before the signal from any of the other bits. This effect has been compensated for experimentally by adding "speed-up" capacitors to the ladder sections as shown in Figure 20 (SA 64005). Figure 19c shows the result of the second part of the above experiment when the capacitors have been added to the ladder.

APPENDIX A:

Equivalent resistance and equivalent voltage of a constant current source:





$$\Delta E_1 = \Delta i_b (r_p + R_K) - \mu \Delta e_g$$

$$\Delta e_g = K_1 \Delta E_1 - R_K \Delta i_b$$

$$\Delta E_1 (1+\mu K_1) = \Delta i_b \left[(\mu+1) R_K + r_p\right]$$

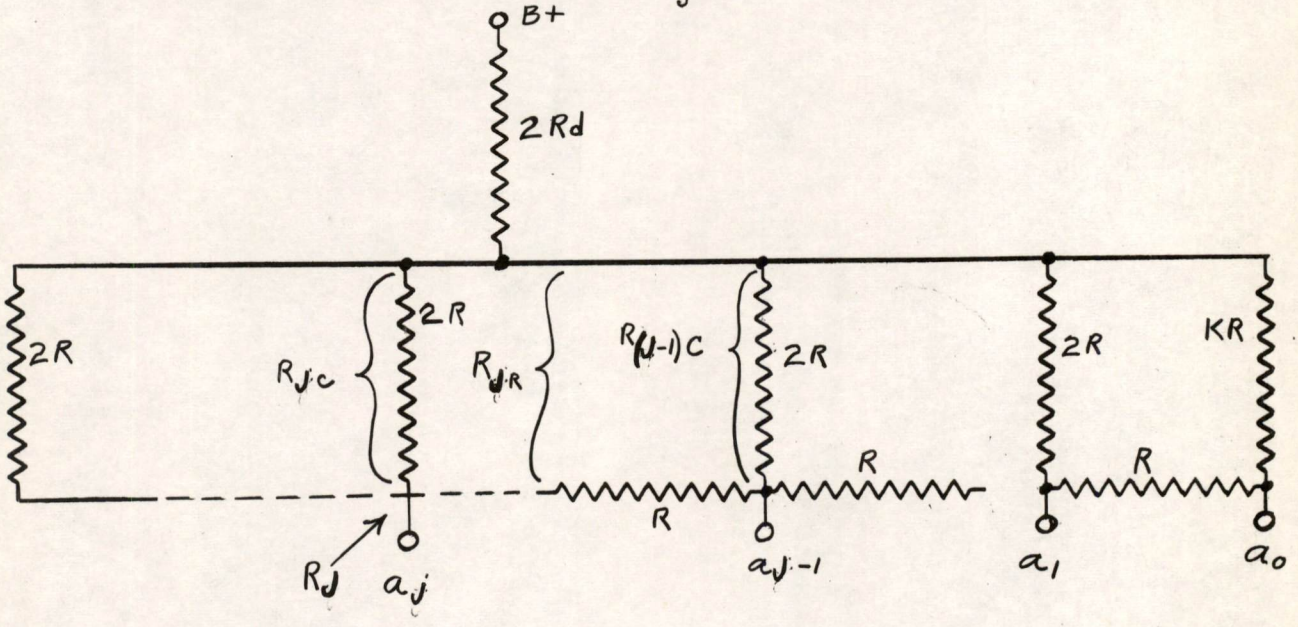
$$R_{eQ} = \frac{\Delta E_1}{\Delta i_b} = \frac{(\mu+1) R_K + r_p}{1+\mu K_1} \qquad \text{EQ } 2.21$$

$$E_{eQ} = i_b R_{eQ} \qquad \text{EQ } 2.22$$

Appendix B

Impedance R_j presented by a decoder ladder with variable termination to any terminal a_j.

Consider the impedance R_j to be composed of three parallel components, the left section of the ladder, the 2R resistor going directly to a_j, and the right section of the ladder. It is easily shown that the equivalent resistance of the left section of ladder is 2R since that end is terminated in the characteristic impedance of the ladder. The figure below shows the resultant simplification of the impedance R_j.



Thus

$$R_j = 2R \| R_{jc} + 2Rd$$

$$R_{jc} = 2R \| R_{jR}$$

$$R_{jR} = R + R_{(j-1)c}$$

The first few terms for R_j can be calculated as in the table below.

J	R_{JR}	R_{Jc}	R_J	N
0	—	KR_L	$2R_d + \frac{2R_L}{K+2}(K)$	1/2
1	$R_L(K+1)$	$2R_L\left(\frac{K+1}{K+3}\right)$	$2R_d + \frac{2R_L}{K+2}\left(\frac{K+1}{2}\right)$	1
2	$R_L\left(\frac{3K+5}{K+3}\right)$	$2R_L\left(\frac{3K+5}{5K+11}\right)$	$2R_d + \frac{2R_L}{K+2}\left(\frac{3K+5}{8}\right)$	3
3	$R_L\left(\frac{11K+21}{5K+11}\right)$	$2R_L\left(\frac{11K+21}{21K+43}\right)$	$2R_d + \frac{2R_L}{K+2}\left(\frac{11K+21}{32}\right)$	11
4	$R_L\left(\frac{43K+85}{21K+43}\right)$	$2R_L\left(\frac{43K+85}{85K+171}\right)$	$2R_d + \frac{2R_L}{K+2}\left(\frac{43K+85}{128}\right)$	43

From this table it will be noticed that the values of R_j are in the form.

$$R_J = 2R_d + \frac{2R_L}{K+2}\left(\frac{NK + 2N-1}{3N-1}\right) \quad \text{for } J \geq 0$$

The resultant values of N are calculated and are found to form a series having the ratio 4N-1. This series can be expressed more generally as

$$N = \frac{2^{2J-1}+1}{3}$$

Substituting this general expression of N into the above expression for R_j

$$R_J = 2R_d + \frac{2R_L}{K+2}\left[\frac{(2^{2J-1}+1)(K+2)-3}{3 \times 2^{2J-1}}\right] \quad \text{for } 0 \leq J \leq n$$

where n+1 is the total number of bits in the ladder.

For common mode analysis K = ∞ so that

$$R_J = 2R_d + \frac{2R_L}{3}\left(\frac{2^{2J-1}+1}{2^{2J-1}}\right) \quad \text{for} \quad 0 \leq J \leq n \qquad \text{Eq. 2.41}$$

For differential mode analysis Rd = 0 so that

$$R_J = \frac{2R_L}{K+2}\left[\frac{(2^{2J-1}+1)(K+2)-3}{3 \times 2^{2J-1}}\right] \quad \text{for} \quad 0 \leq J \leq n \qquad \text{Eq 2.46}$$

Similarly

$$R_{JC} = 2R_L\left[\frac{NK+2N-1}{(2N-1)K+4N-1}\right]$$

again

$$N = \frac{2^{2J-1}+1}{3}$$

So that

$$R_{JC} = 2R_L\left[\frac{(2^{2J-1}+1)K+2^{2J}-1}{(2^{2J}-1)K+2^{2J+1}+1}\right] \quad \text{for} \quad 0 \leq J \leq n$$

For differential mode analysis Rd = 0. However, since it does not appear here, this expression is correct for differential mode analysis.

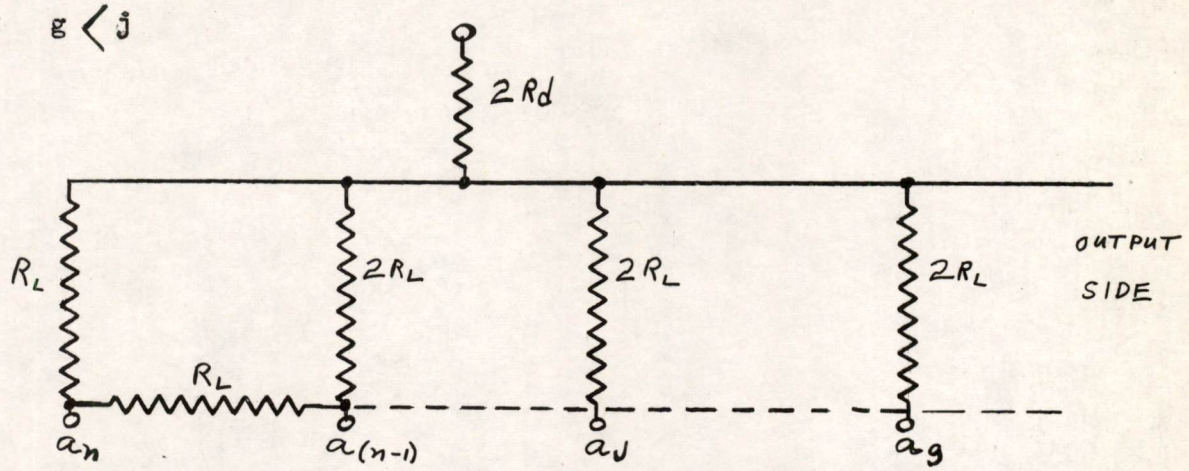
For common mode analysis K = ∞ so that

$$R_{JC(cm)} = 2R_L\left(\frac{2^{2J-1}+1}{2^{2J}-1}\right)$$

Appendix C

Voltage at terminal a_j of a decoder ladder caused by a current I_g is some other terminal a_g.

Case I: $g < j$



The total ladder impedance to the left of a_j together with the 2R resistor at a_j forms a termination at a_j equal to R. Thus, of the entire voltage developed at a_g ($I_g R_g$), the entire portion developed across $2R_d$ will appear at a_j, but only a $\frac{1}{2^{J-g}}$ portion of the remainder (See R-220 "Analysis and Design of a Digital-to-Analog Decoder" by Robert Louis Walquist Sect. 4.3 pp 31-64)

$$E_{Jg} = 2I_g R_d + \frac{I_g R_g - 2I_g R_d}{2^{J-g}}$$

$$E_{Jg} = I_g \left(2R_d + \frac{R_g - 2R_d}{2^{J-g}}\right)$$

For common mode analysis we have R_g from Appendix B:

$$R_g = 2R_d + \frac{2R_L}{3}\left(\frac{2^{2g-1}+1}{2^{2g-1}}\right)$$

Thus

$$E_{Jg\,cm} = I_{g\,cm}\left[2R_d + \frac{2R_L}{3}\left(\frac{2^{2g-1}+1}{2^{J+g-1}}\right)\right]$$

But $I_{g\,cm} = I_g/2$

$$E_{Jg\,cm} = I_g\left[R_d + \frac{R_L}{3}\left(\frac{2^{2g-1}+1}{2^{J+g-1}}\right)\right] \qquad \text{Eq. 2.43}$$

For differential mode analysis

$$R_g = \frac{2R_L}{K+2}\left[\frac{(2^{2g-1}+1)(K+2)-3}{3\times 2^{2g-1}}\right]$$

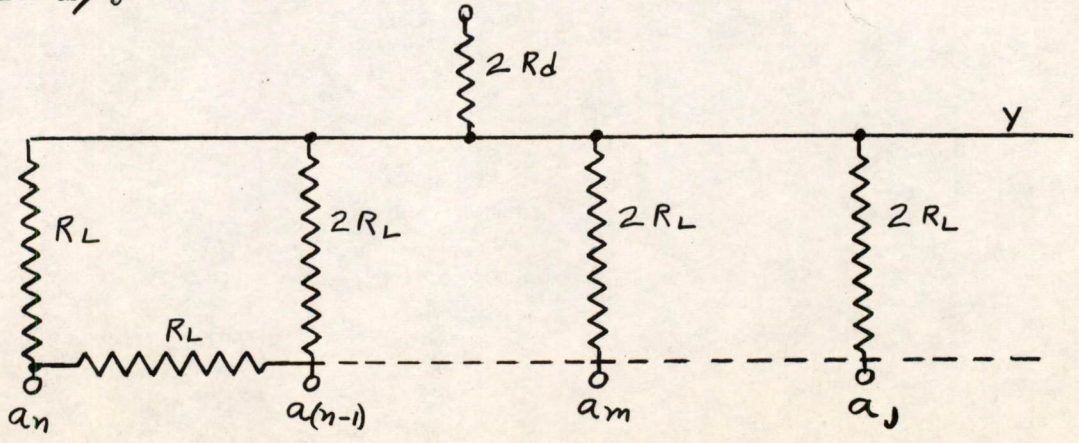
and $R_d = 0$

$$E_{Jg\,dm} = I_{g\,dm}\,\frac{2R_L}{K+2}\left[\frac{(2^{2g-1}+1)(K+2)-3}{3\times 2^{J+g-1}}\right]$$

But $I_{g\,dm} = I_{g/2}$ - therefore:

$$E_{Jg\,dm} = \frac{I_g R_L}{K+2}\left[\frac{(2^{2g-1}+1)(K+2)-3}{3\times 2^{J+g-1}}\right] \qquad \text{Eq. 2.48}$$

Case II: m > j



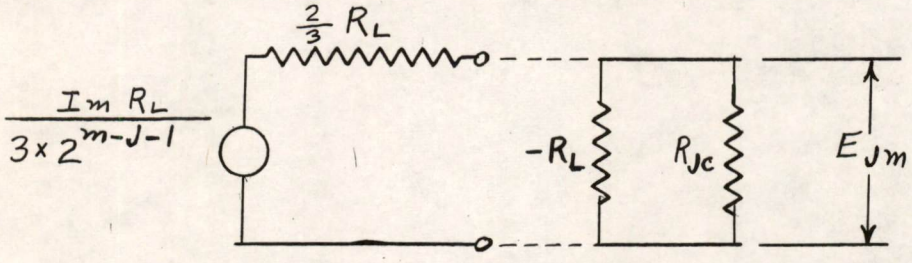
Consider terminal a_j terminated with the characteristic impedance of the ladder (R_L). Under this condition the voltage at a_m due to I_m is

$$E_{mm} = \frac{2}{3} I_m R_L + 2 I_m R_d$$

Using the results of Walquist Report R220, the voltage at a_j due to the current at a_m is

$$E_{Jm} = I_m \left(2R_d + \frac{R_L}{3 \times 2^{m-J-1}} \right)$$

The output impedance between terminal a_j and line Y at this time is 2/3R. This portion of the decoder can thus be replaced with its Thevenin equivalent circuit. If this Thevenin circuit is then shunted with an impedance equal to -R in parallel with R_{jc} of Appendix B, the output voltage will be equal to the voltage at a_j due to I_m at a_m when the ladder is terminated in other than the characteristic impedance.



For common mode analysis Appendix B shows the value of R_{jc}

$$R_{JC\,cm} = 2R_L \left(\frac{2^{2J-1} + 1}{2^{2J} - 1} \right)$$

E_{jm} can be calculated from the Thevenin circuit and the above expression for R_{jc}.

$$E_{Jm\,cm} = I_{m\,cm} \left[2R_d + R_L \left(\frac{2^{2J-1} + 1}{3 \times 2^{m+J}} \right) \right]$$

However $I_{m\,cm} = I_m/2$. Therefore

$$E_{Jm\,cm} = I_m \left[R_d + \frac{R_L}{3} \left(\frac{2^{2J-1} + 1}{2^{J+m-1}} \right) \right] \qquad \text{Eq. 2.44}$$

Similarily for differential mode analysis

$$R_{JC} = 2R_L \left[\frac{(2^{2J-1}+1)K + 2^{2J} - 1}{(2^{2J}-1)K + 2^{2J+1} + 1} \right]$$

E_{jm} can again be calculated from the Thevenin circuit and the above expression for R_{jc}.

$$E_{Jm\,dm} = \frac{I_{m\,dm}\, R_L}{K+2} \left[\frac{(2^{2J-1}+1)(K+2) - 3}{3 \times 2^{m+J-2}} \right]$$

But $I_{m\,dm} = I_m/2$. Therefore

$$E_{Jm\,dm} = \frac{I_m R_L}{K+2} \left[\frac{(2^{2J-1}+1)(K+2) - 3}{3 \times 2^{J+m-1}} \right] \qquad \text{Eq. 2.49}$$

Appendix D

E_j min., E_o min., E_j max., E_o max., and K for

E_o min $\leq E_j$ min when all $I_g = I$ and load is a constant current I_L from both output terminals.

$$E_{J\,cm} = \sum_{g=0}^{g=n} I_g \left[R_d + \frac{R_L}{3} \left(\frac{1}{2^{J+g-1}} + \frac{1}{2^{|J-g|}} \right) \right] \qquad \text{EQ 2.45}$$

$$E_{J\,cm} = \left[I_L + (n+1) I \right] R_d + \frac{I_L R_L}{2^J} + \frac{I R_L}{3} \left[\frac{2}{2^J} \sum_{g=0}^{g=n} \frac{1}{2^g} + \sum_{g=0}^{g=J} \frac{1}{2^{J-g}} + \sum_{g=J+1}^{g=n} \frac{1}{2^{g-J}} \right]$$

$$\sum_{g=0}^{g=n} \frac{1}{2^g} = 2 - 2^{-n}$$

$$\sum_{g=0}^{g=J} \frac{1}{2^{J-g}} = \sum_{g=0}^{g=J} \frac{1}{2^g} = 2 - 2^{-J}$$

$$\sum_{g=J+1}^{g=n} \frac{1}{2^{g-J}} = \sum_{g=1}^{g=n-J} \frac{1}{2^g} = 1 - 2^{J-n}$$

$$E_{J\,cm} = \left[I_L + (n+1) I \right] R_d + \frac{I_L R_L}{2^J} + \frac{I R_L}{3} \left[2^{1-J} (2 - 2^{-n}) + 2 - 2^{-J} + 1 - 2^{J-n} \right]$$

$$\boxed{E_{J\,cm} = \left[I_L + (n+1) I \right] R_d + \frac{I_L R_L}{2^J} + I R_L \left[1 + 2^{-J} - \frac{1}{3 \times 2^n} \left(2^J + 2^{1-J} \right) \right]}$$

$$E_{J\,dm} = \sum_{g=0}^{g=n} \frac{I_g R_L}{3} \left[\left(\frac{K-1}{K+2}\right) \frac{1}{2^{J+g-1}} + \frac{1}{2^{|J-g|}} \right] \quad \text{EQ 2.410}$$

$$E_{J\,dm} = \frac{I R_L}{3} \left[\left(\frac{K-1}{K+2}\right) 2^{1-J}\left(2-2^{-n}\right) + 2 - 2^{-J} + 1 - 2^{J-n} \right]$$

$$\boxed{E_{J\,dm} = I R_L \left\{ 1 + \frac{K-2}{K+2} 2^{-J} - \frac{1}{3\times 2^n} \left[2^J + \left(\frac{K-1}{K+2}\right) 2^{1-J} \right] \right\}}$$

$$E_{J\,MIN} = E_{bb} - E_{J\,cm} - E_{J\,dm}$$

$$E_{J\,MIN} = E_{bb} - \left[I_L + (n+1)I\right] R_d - \frac{I_L R_L}{2^J} - 2 I R_L \left\{ 1 + \frac{K 2^{-J}}{K+2} - \frac{1}{3\times 2^n} \left[2^J + \left(\frac{2K+1}{K+2}\right) 2^{-J} \right] \right\}$$

$$E_{J\,MIN} = E_{bb} - \left[I_L + (n+1)I\right] R_d - \frac{I_L R_L}{2^J} - 2 I R_L - \frac{2 I R_L}{K+2} \left\{ K 2^{-J} - \frac{1}{3\times 2^n} \left[(K+2) 2^J + (2K+1) 2^{-J} \right] \right\}$$

EQ. 2.412a

$$E_{o\,MIN} = E_{bb} - \left[I_L + (n+1)I\right] R_d - \left(I_L + 2I\right) R_L - \frac{2 I R_L}{K+2} \left(K - \frac{K+1}{2^n} \right) \quad \text{Eq 2.412b}$$

$$E_{J\,MAX} = E_{bb} - E_{J\,cm} + E_{J\,dm}$$

$$E_{J\,MAX} = E_{bb} - \left[I_L + (n+1)I\right] R_d - \frac{I_L R_L}{2^J} - I R_L \left\{ 1 + 2^{-J} - 1 - \frac{K-2}{K+2} 2^{-J} - \frac{1}{3\times 2^n} \left[2^J - 2^J + 2^{1-J} - \left(\frac{K-1}{K+2}\right) 2^{1-J} \right] \right\}$$

$$E_{J\,MAX} = E_{bb} - \left[I_L + (n+1)I\right] R_d - \frac{R_L}{2^J} \left[I_L + \frac{2I}{K+2} \left(2 - 2^{-n}\right) \right] \quad \text{EQ. 2.413a}$$

$$E_{o\,MAX} = E_{bb} - \left[I_L + (n+1)I\right] R_d - R_L \left[I_L + \frac{2I}{K+2} \left(2 - 2^{-n}\right) \right] \quad \text{Eq. 2.413b}$$

FOR $E_{OMIN} \leqslant E_{JMIN}$ $\quad 0 \leqslant J \leqslant n$

UNDER WORST CONDITION $I_L = 0$

$$K - \frac{K+1}{2^n} \geqslant K2^{-J} - \frac{1}{3\times 2^n}\left[(K+2)2^J + (2K+1)2^{-J}\right]$$

$$3\times 2^n\left(K - K2^{-n} - K2^{-J} - 2^{-n}\right) \geqslant -\left[K2^J + 2^{J+1} + K2^{1-J} + 2^{-J}\right]$$

$$K\left(3\times 2^n - 3 - 3\times 2^{n-J} + 2^J + 2^{1-J}\right) \geqslant 3 - 2^{J+1} - 2^{-J}$$

$$K \geqslant \frac{3 - 2^{J+1} - 2^{-J}}{3\times 2^n(1-2^{-J}) + 2^J - 3 + 2^{1-J}}$$

$$K \geqslant \frac{1 - 2^{J+1}}{3\times 2^n + 2^J - 2}$$

$$K \geqslant \frac{-2/3}{\frac{2^n - 1/2}{2^J - 1/2} + \frac{1}{3}}$$

FOR $0 < J \leqslant n$ K WILL HAVE ITS LEAST NEGATIVE VALUE AS $J \to 0$. THEREFORE LET $J = 1$

$$K \geqslant -2^{-n}$$

Appendix E: Glossary of Symbols

CGT	Current Gate Tube (See section 2.3)
CU_s	Constant current source (See section 2.2)
E_{eq}	Equivalent voltage source of a circuit - the voltage which would have to be applied to the equivalent resistance of a circuit to produce the same current which the actual circuit carries.
$E_{gg\ cm}$	The common mode voltage at terminal g of a decoder ladder measured with respect to the B + supply and caused by the common mode current through terminal g.
$E_{gg\ dm}$	Same as $E_{gg\ cm}$ except for differential mode voltage and differential mode current.
E_j	Total voltage at terminal j measured with respect to ground and caused by any currents through any terminals
$E_{j\ cm}$	Total common mode voltage at terminal j measured with respect to B + and caused by any common mode currents through any terminals.
$E_{j\ dm}$	Same as $E_{j\ cm}$ except differential mode voltage and differential mode currents.
$E_{j\ max}$	Maximum voltage at terminal j measured with respect to ground when all currents in the decoder are switched to the opposite side of the decoder ladder.
$E_{j\ min}$	Minimum voltage at the terminal j measured with respect to ground when all currents in the decoder are switched to the same side of the decoder ladder.
$E_{jg\ cm}$	The common mode voltage at terminal j measured with respect to B + caused by a common mode current in the terminal g when $g < j$.
$E_{jg\ dm}$	Same as $E_{jg\ cm}$ except differential mode voltage and differential mode current.
$E_{jj\ cm}$	Same as $E_{gg\ cm}$ except for terminal j.
$E_{jj\ dm}$	Same as $E_{gg\ dm}$ except for terminal j.
$E_{jm\ cm}$	Same as $E_{jg\ cm}$ except for terminal m instead of terminal g and $m > j$.

$E_{jm\ dm}$	Same as $E_{jg\ dm}$ except for terminal m instead of terminal g and m>j.
E_{od}	Differential output voltage
$E_{o\ max}$	Same as $E_{j\ max}$ except for output terminal.
$E_{o\ min}$	Same as $E_{j\ min}$ except for output terminal.
I_g	Total current out of both g(a and b) terminals.
I_j	Same as I_g except for j terminals.
$I_{j\ cm}$	Common mode current out of terminal j.
$I_{j\ dm}$	Differential mode current out of terminal j.
I_m	Same as I_g except for terminal m.
K	Proportionality factor relating value of terminating resistor of a push-pull decoder ladder to $2R_L$ where R_L is the nominal resistance of the ladder.
K_1	Transfer function for the output voltage variation of the voltage reference circuit vs supply voltage variations. For the circuit under consideration this value is 0.00355.
LS	Ladder section (See section 2.4)
M	Proportionality factor relating the value of a terminating resistor of a single-sided decoder ladder to the characteristic impedance of the ladder.
n	One less than the total number of bits in a decoder ladder.
N	Total number of bits in a decoder ladder. N = n + 1.
R	Voltage Reference Source (See section 2.1)
R_L	Characteristic resistance of a decoder ladder.
R_d	Dropping resistor which lowers the B + supply voltage to a level at which the decoder ladder is to operate.
R_{eq}	Equivalent resistance of a circuit. It is the ratio of a change in the supply voltage of the circuit to the change in current caused by the change in voltage.
R_{jc}	The resistance which a ladder presents to a current at terminal j when all resistors from less significant bits are removed. (See appendix B)

$R_{j\ cm}$ The resistance which a ladder presents to a common mode current at terminal j.

$R_{j\ dm}$ The resistance which a ladder presents to a differential mode current at terminal j.

$R_{j\ r}$ The resistance which a ladder presents to a current at terminal j when the 2R resistor at terminal j and all other resistors at less significant bits are removed.

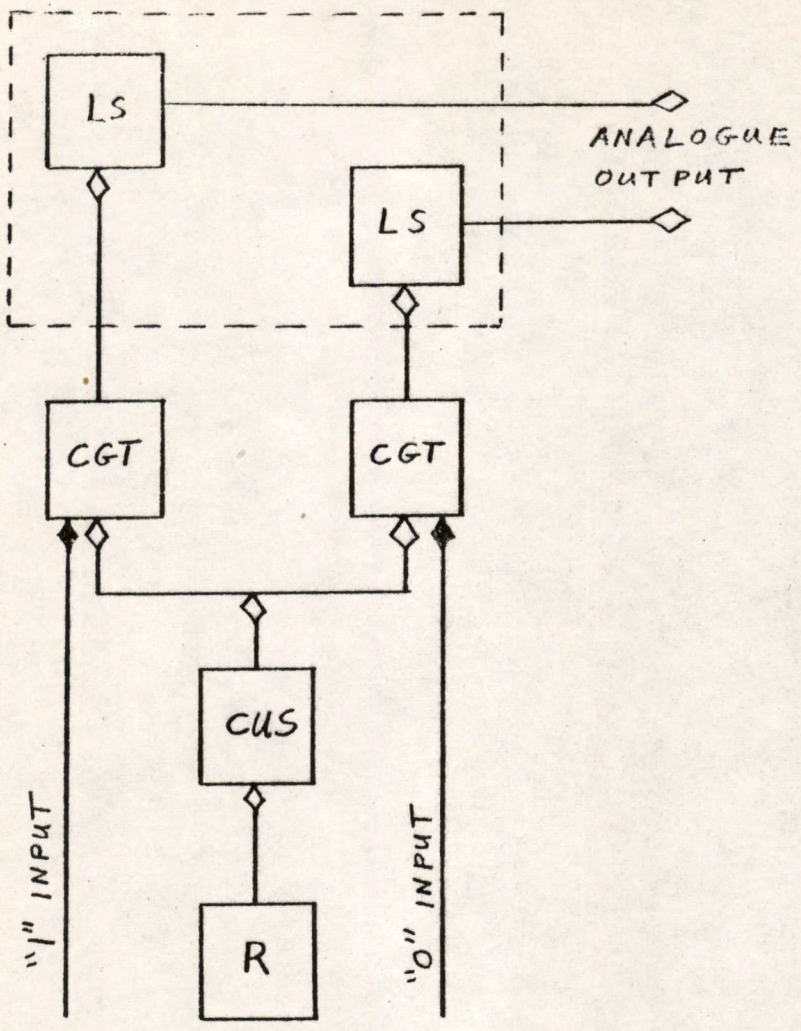
$R_{j\ r} = R_{j\ c}$ in parallel with -2R.

Signed H. E. Zieman
H. E. Zieman

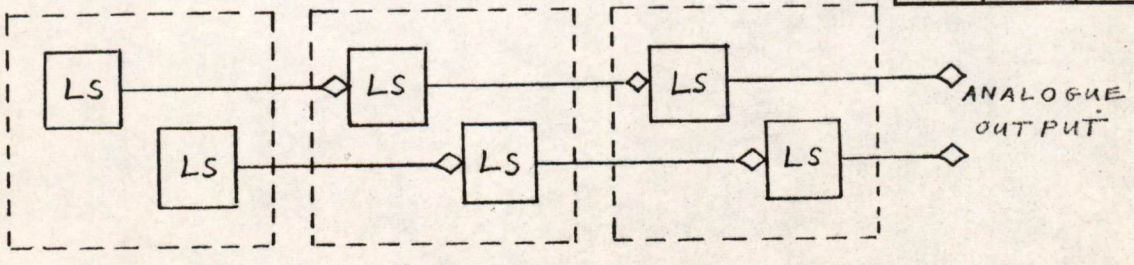
Attached drawings:

Figure 1 - SA 47174
Figure 2 - SA 63288
Figure 3 - SA 48619-G
Figure 4 - SA 63702
Figure 5 - SA 48613-G
Figure 6 - SA 48617-G
Figure 7 - SA 48614-G
Figure 8 - SA 48615-G
Figure 9 - SA 48618-G
Figure 10- SA 48616-G
Figure 11 - SA 63717
Figure 12 - SA 48610-G
Figure 13 - SA 48609-G
Figure 14 - SA 48611-G
Figure 15 - SA 63878
Figure 16 - SA 63879
Figure 17 - SA 48620-G
Figure 18 - SA 48623-G
Figure 19 - SA 48709
Figure 20 - SA 64005

CC:
Group 62 Staff
I.B.M. Poughkeepsie
Cecil Branson
John Swatton



DECODER STAGE (OR BIT)
FIGURE 1a



CASCADED DECODER LADDER SECTIONS
FIGURE 1b

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO.

DECODER STAGE AND DECODER LADDER

SCALE:
DR. K.E. Brennan
CK.
ENG. K.E. Brennan
APPD.

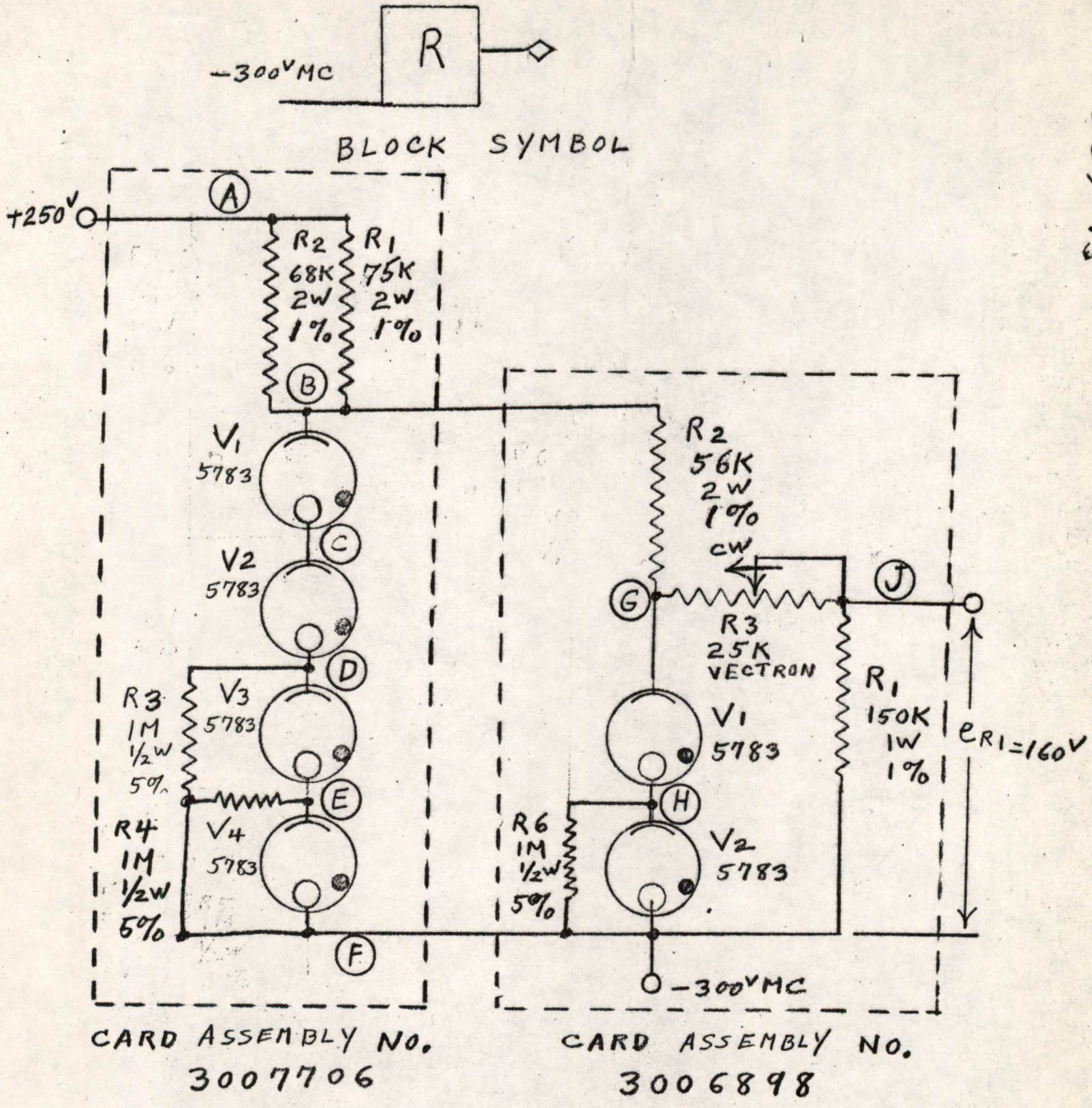
SA- 47174-1

CHG.	CN#	DATE	APPD.
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			

SA- 47174-1

K&E ALBANENE 1951 TRACING PAPER

FIGURE 2



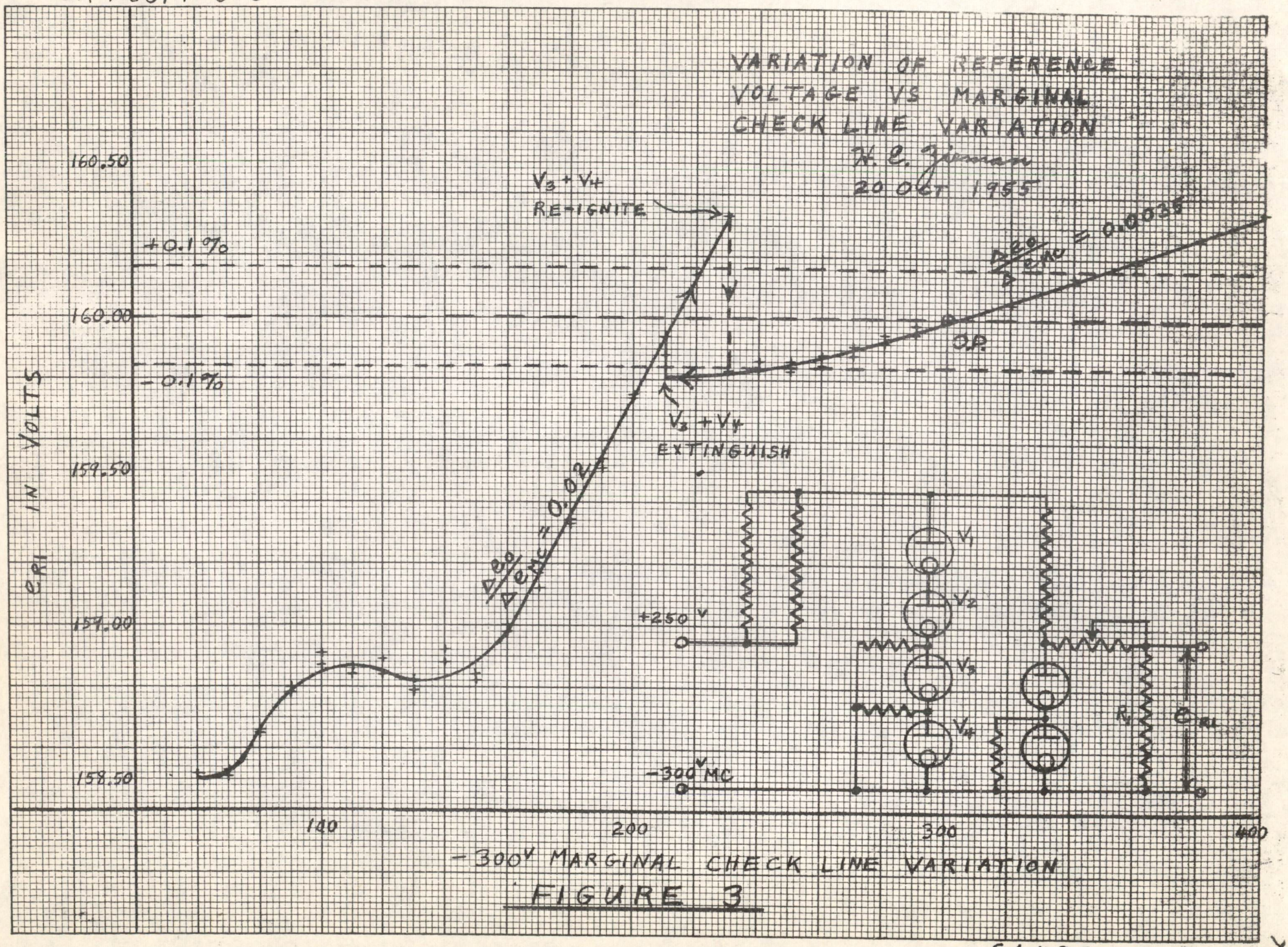
SA 63288-3

SA 63288-3

VOLTAGE REFERENCE SOURCE FOR DECODERS

H E Grieman 11 JULY '55

SA 48619-G-3

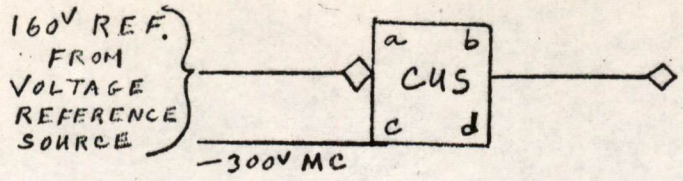


-300V MARGINAL CHECK LINE VARIATION

FIGURE 3

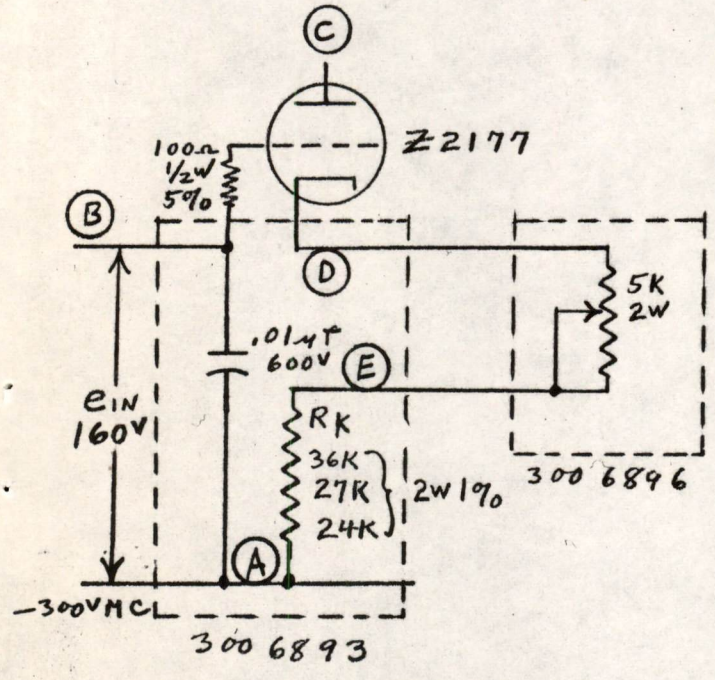
SA 48619-G-3

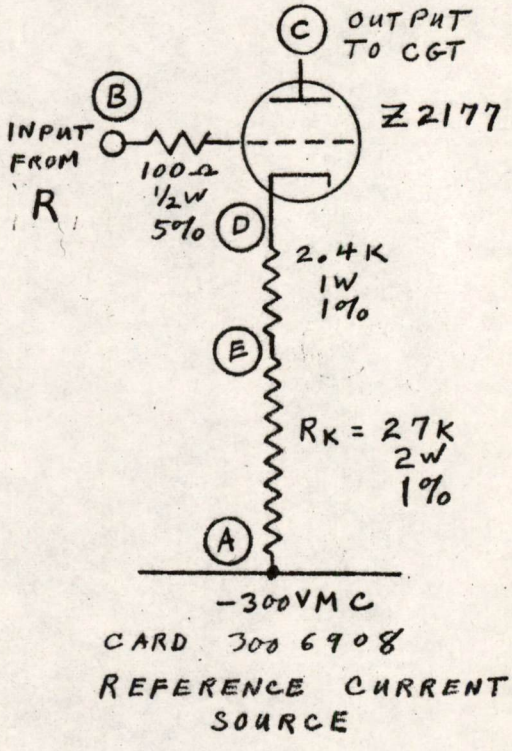
SA-63102



a = SLOT LOCATION OF CONTROL POT.
b = LOCATION OF CONTROL POT ON CARD.
c = NOMINAL CURRENT OF CUS IN Ma.
d = LOCATION AND SECTION OF TUBE IN PLUGGABLE UNIT

BLOCK SYMBOL





CIRCUIT DIAGRAM

FIGURE 4

CURRENT SOURCE FOR DECODERS

H. E. Zieman 1 aug '55

SA-63702

SA 48613-G-1

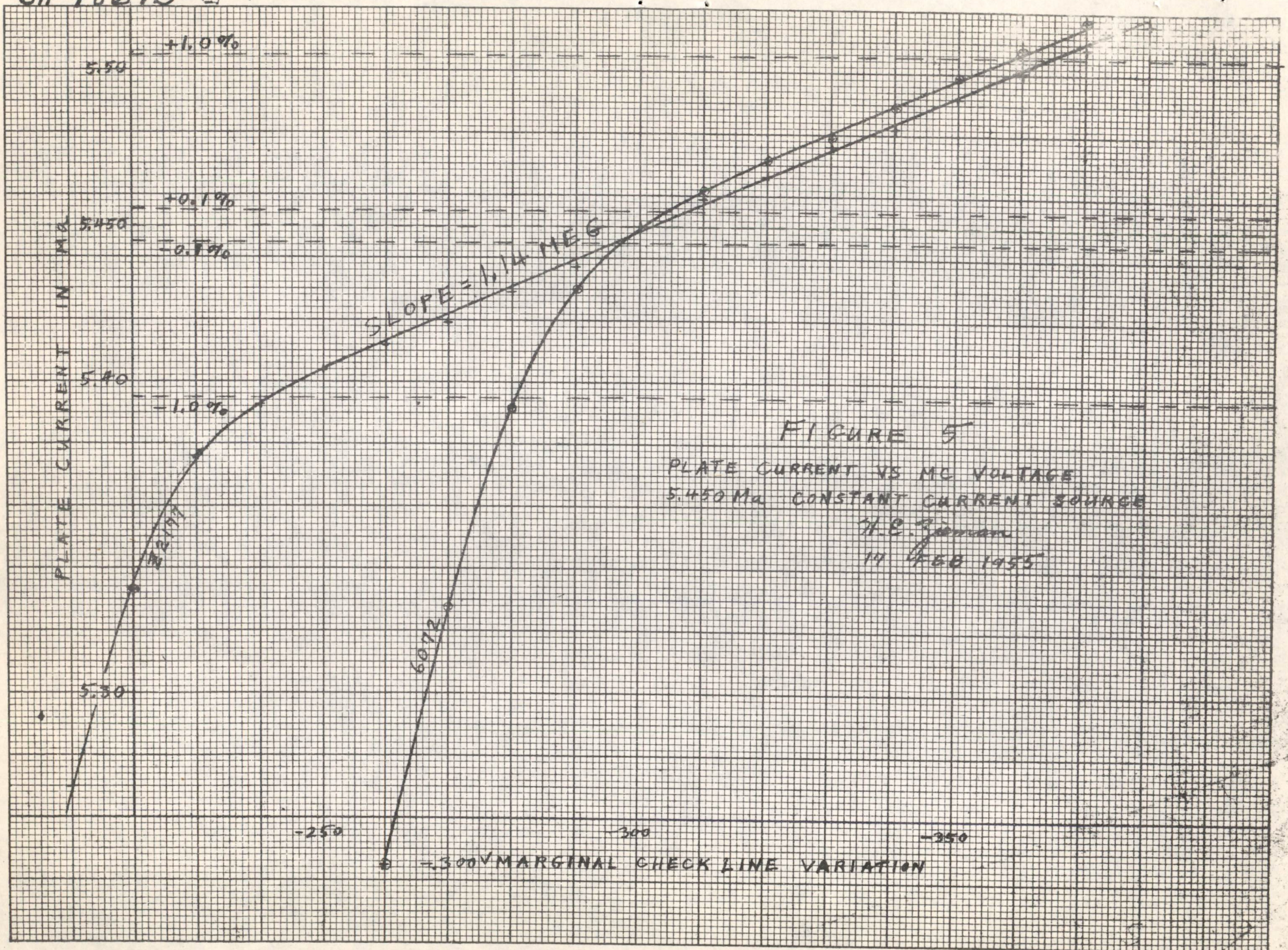


FIGURE 5

PLATE CURRENT VS MC VOLTAGE
5.450 Ma CONSTANT CURRENT SOURCE
W. C. Jensen
14 FEB 1955

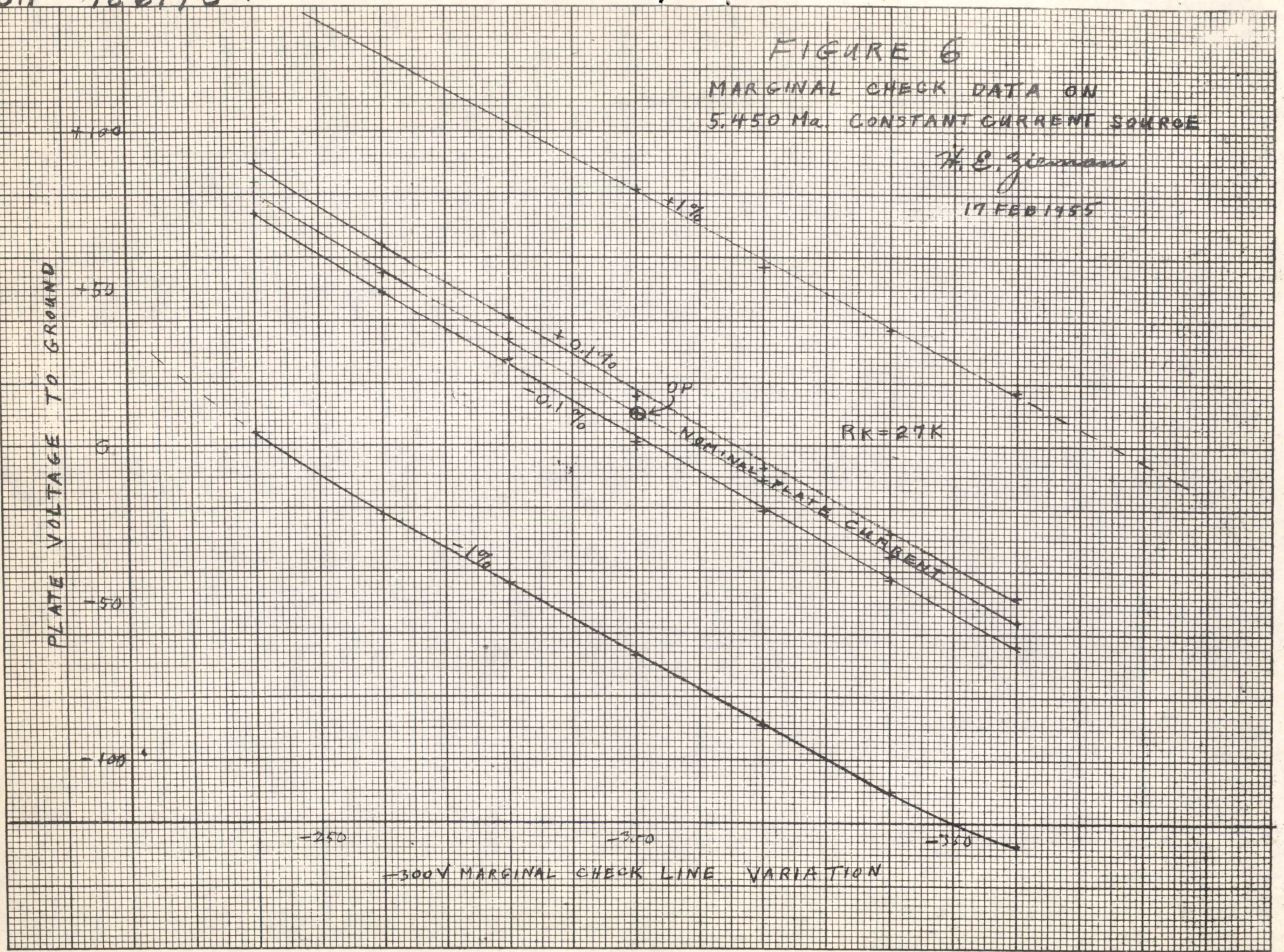
SA-48613-6

SA-48617-G-1

FIGURE 6

MARGINAL CHECK DATA ON
5.450 Ma. CONSTANT CURRENT SOURCE

W. E. Zimmerman
17 FEB 1955



SA-48617-G-1

SA-48614-G-1

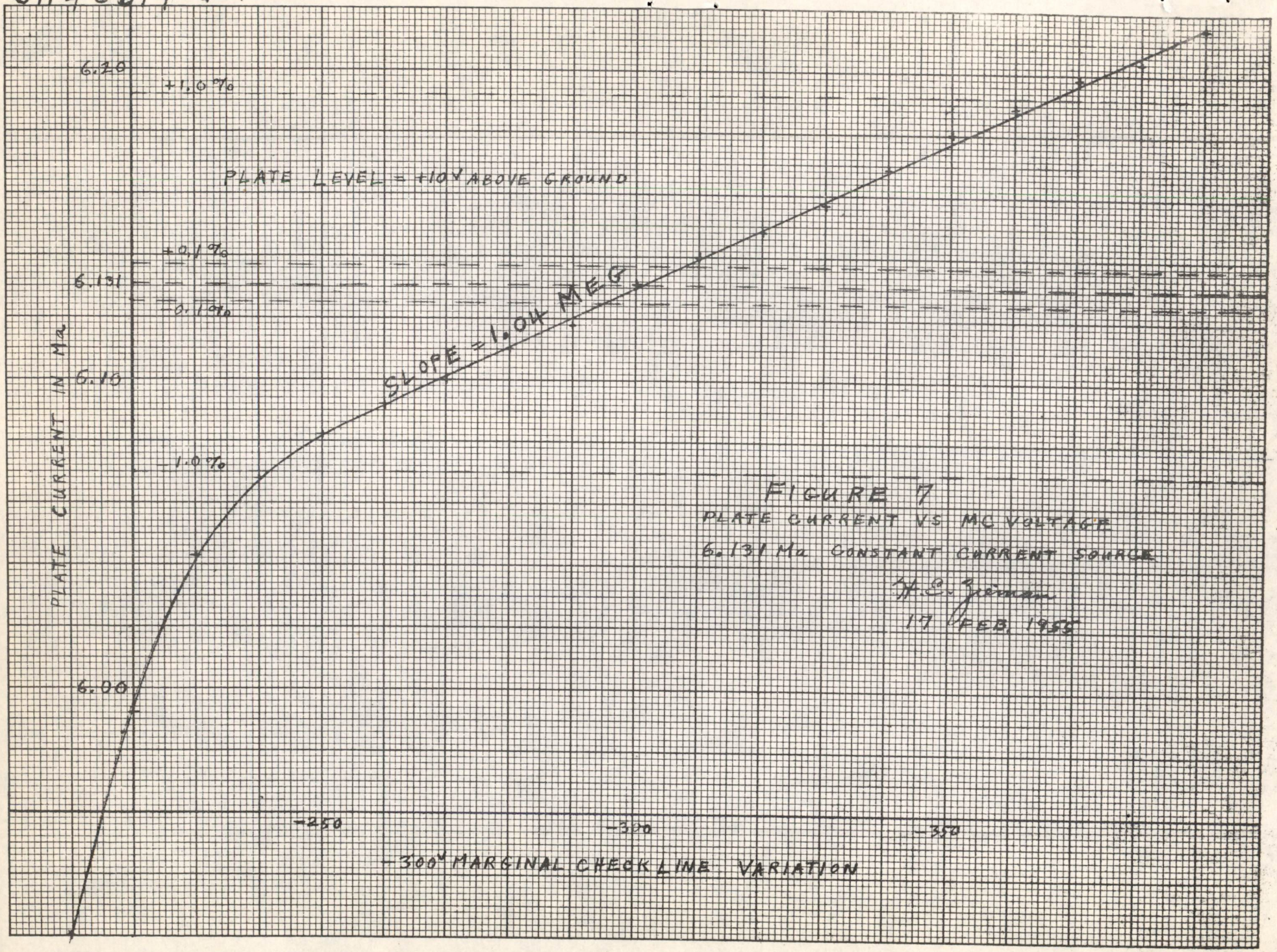
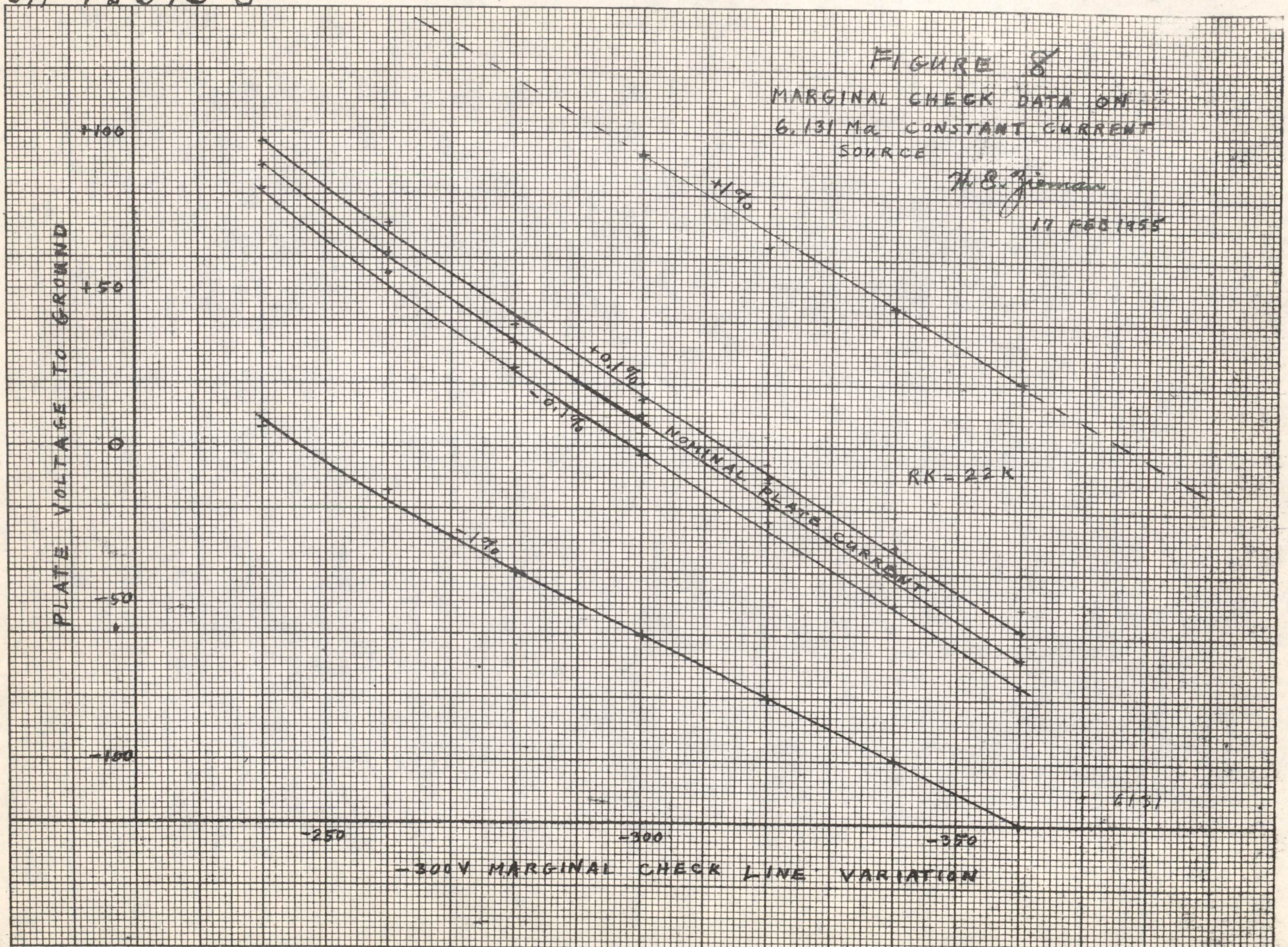


FIGURE 7
PLATE CURRENT VS MG VOLTAGE
6.131 Ma CONSTANT CURRENT SOURCE
W. S. Freeman
17 FEB. 1955

SA-48614-G1

SA-48615-G-1



SA-48615-G

SA-48618-G-1

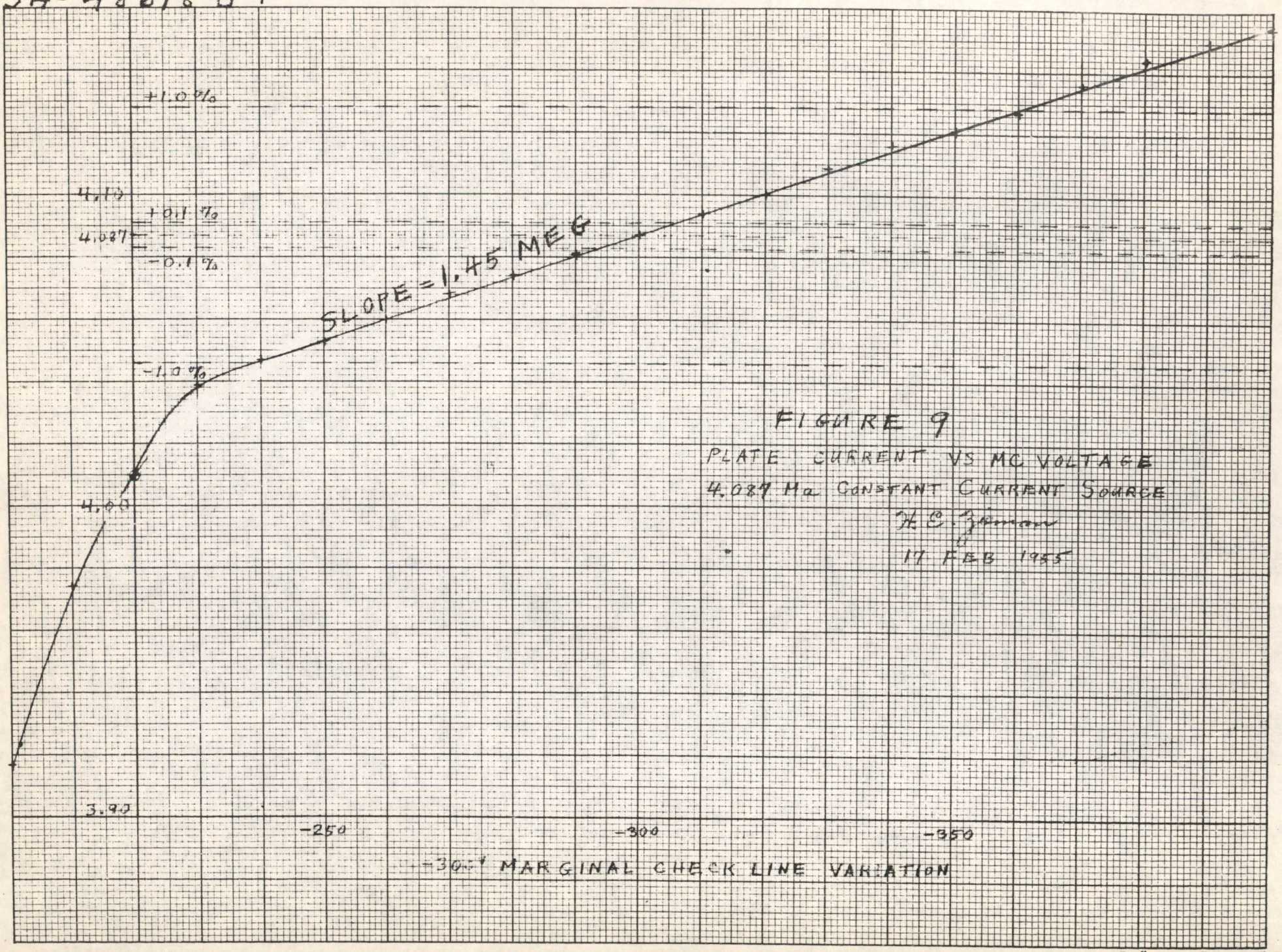
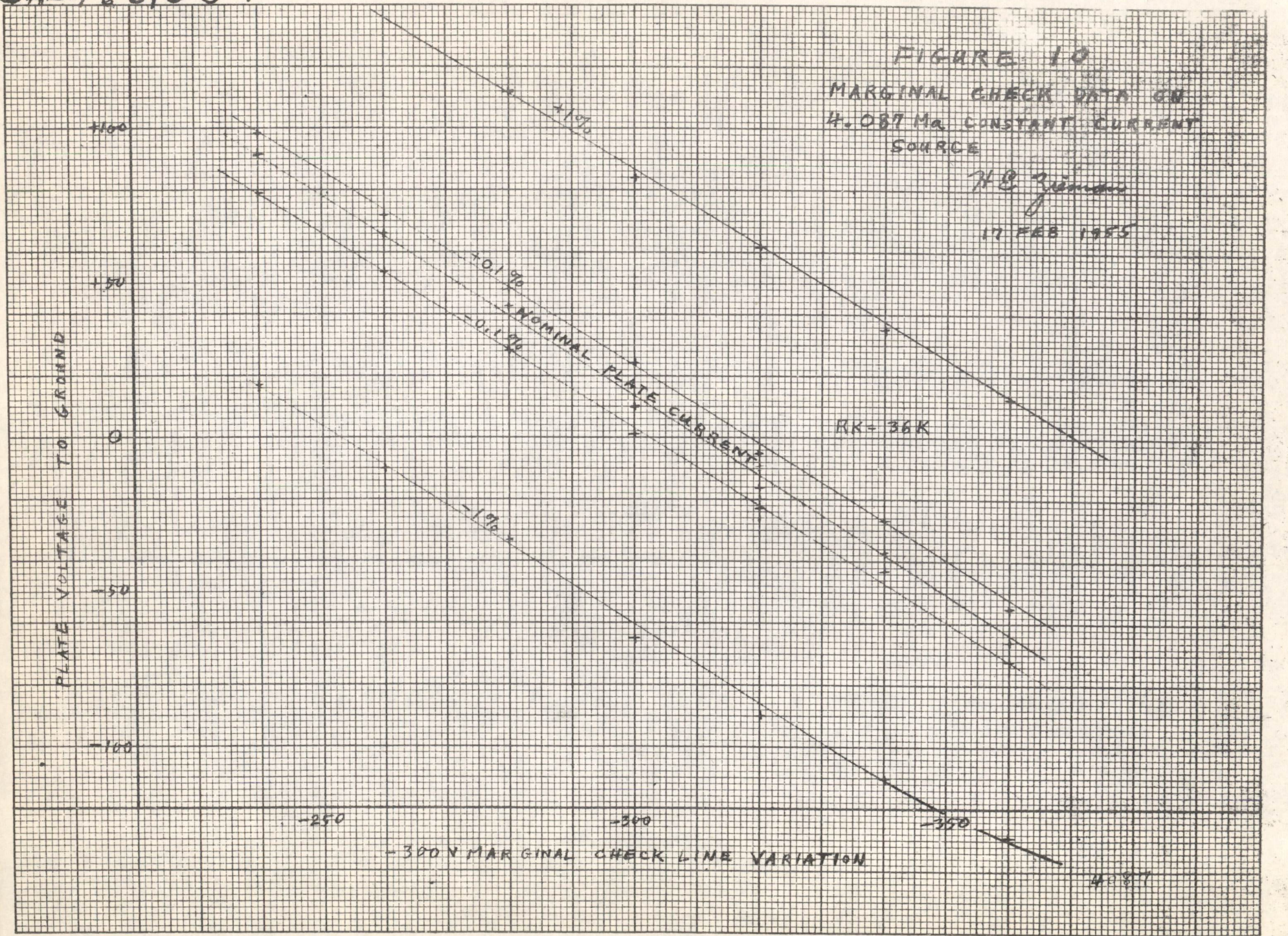


FIGURE 9

PLATE CURRENT VS MC VOLTAGE
4.087 Ma CONSTANT CURRENT SOURCE
H. E. Jensen
17 FEB 1955

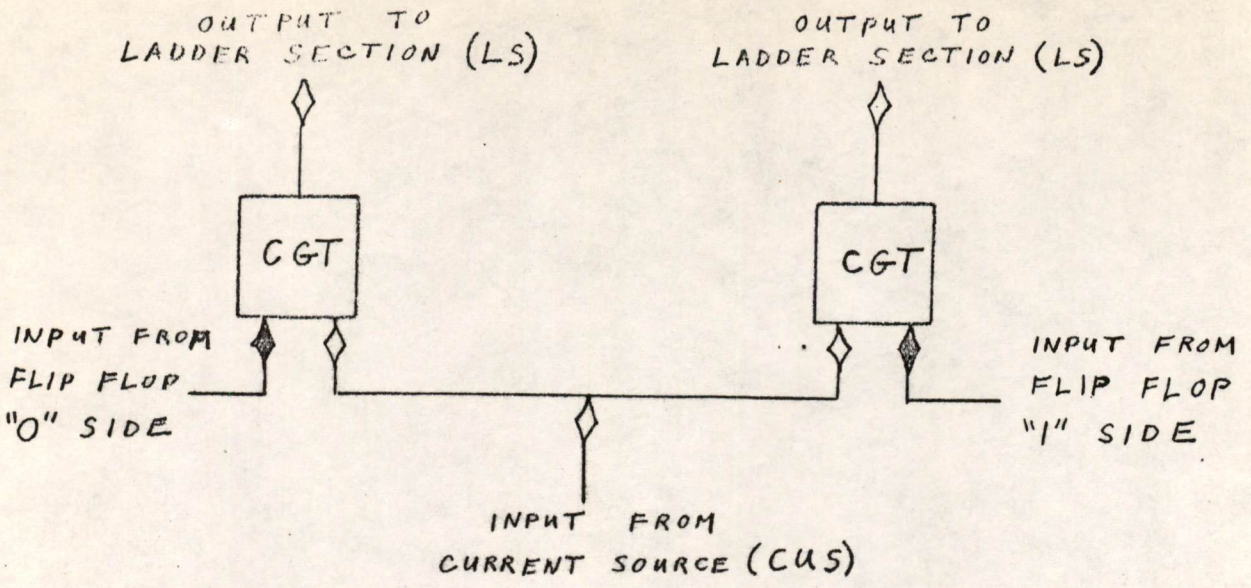
SA-48616-G-1

FIGURE 10
MARGINAL CHECK DATA ON
4.087 Mc CONSTANT CURRENT
SOURCE
H E [redacted]
17 FEB 1955

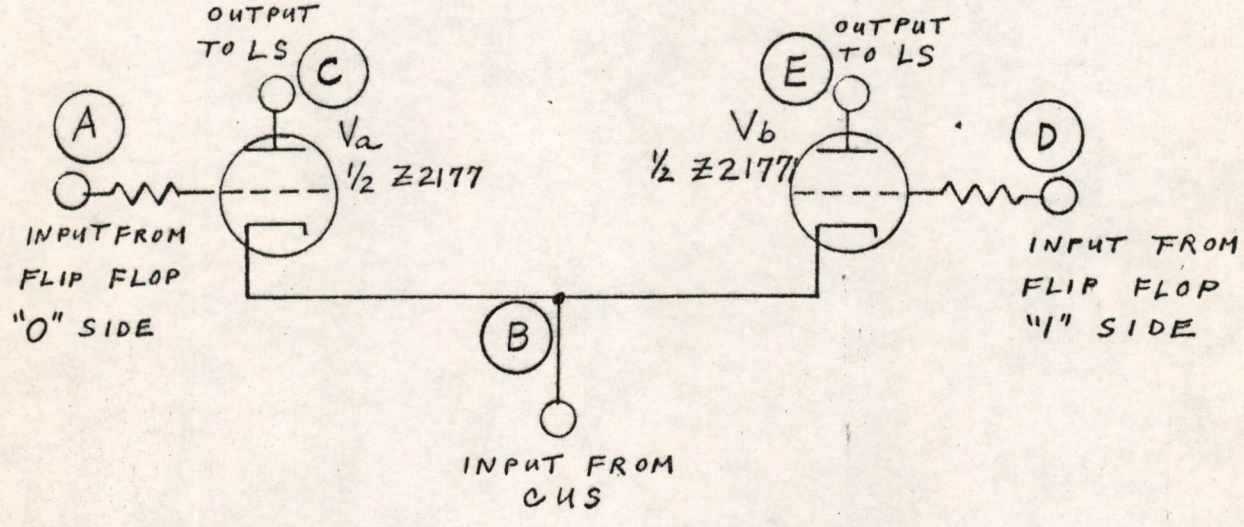


SA-48616-G-1

SA-63717



BLOCK SYMBOL



CIRCUIT DIAGRAM

FIGURE 11

CURRENT GATE TUBE
FOR DECODERS

H. E. Ziemer

SA-. 48.6 10-G-1

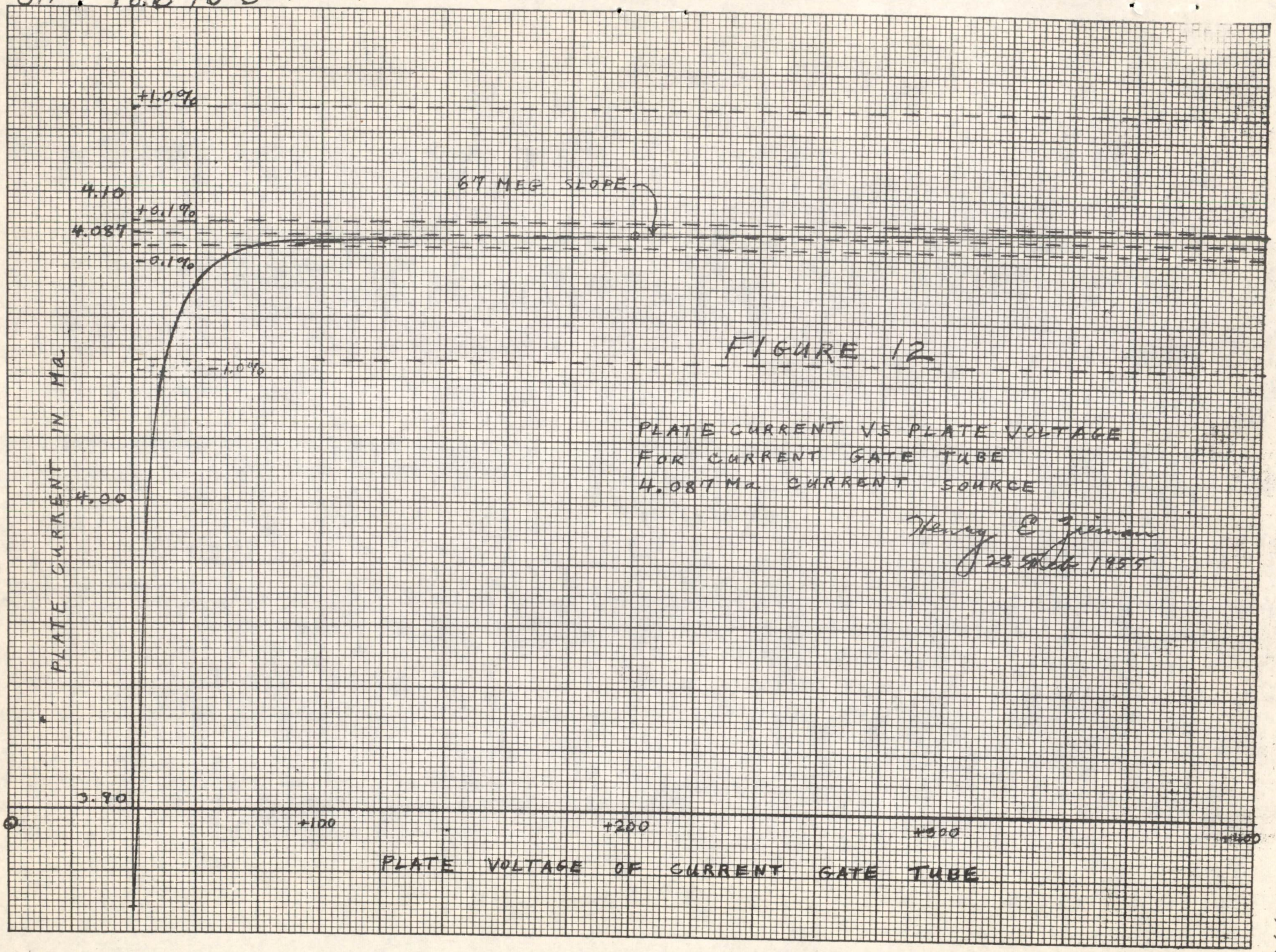


FIGURE 12

PLATE CURRENT VS PLATE VOLTAGE
FOR CURRENT GATE TUBE
4.087 Ma. CURRENT SOURCE

Henry E Freiman
23 Feb 1955

SA-48609-G-1

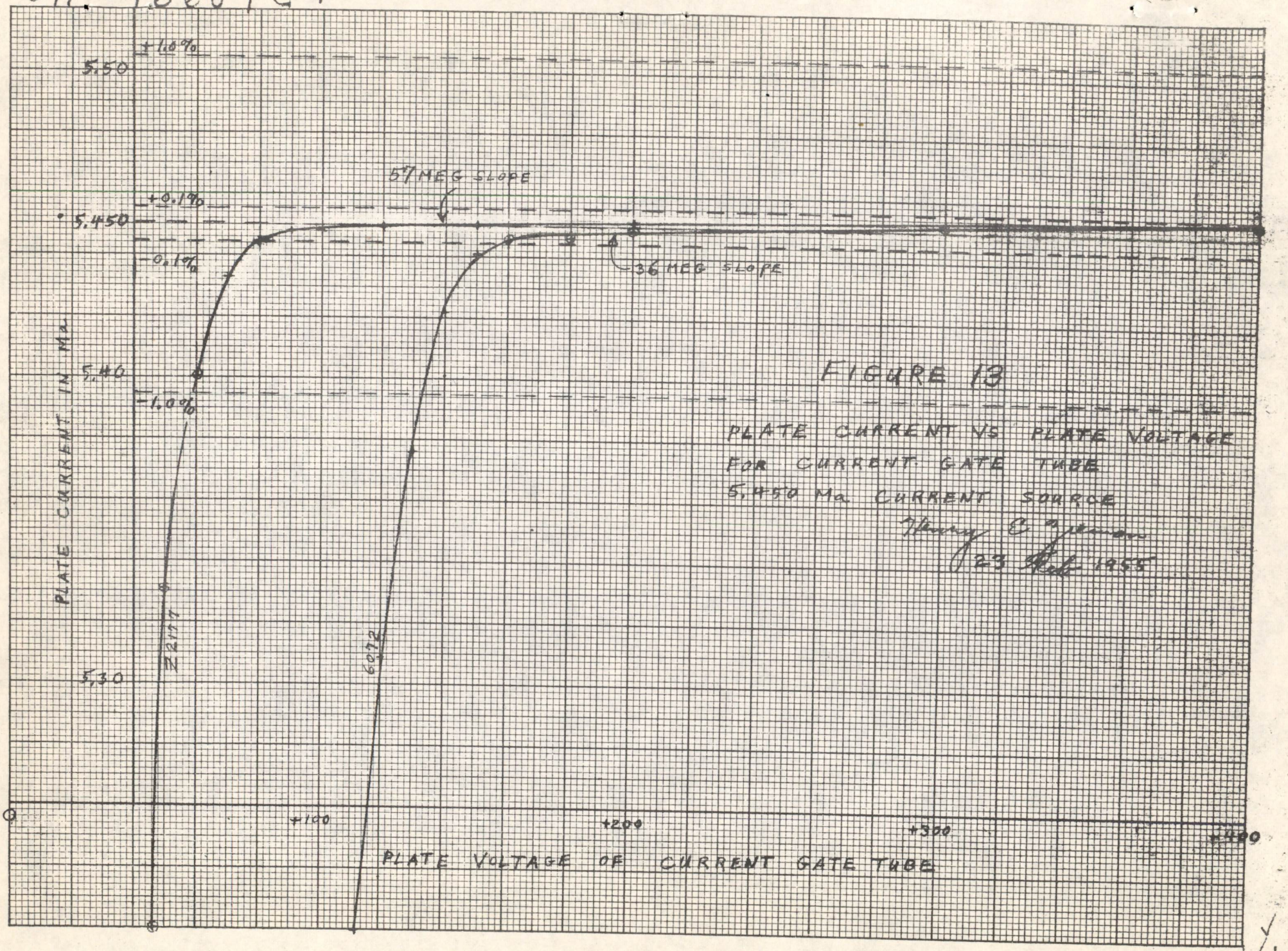


FIGURE 13

PLATE CURRENT VS PLATE VOLTAGE
FOR CURRENT GATE TUBE
5.450 Ma CURRENT SOURCE

Henry C. Jensen
23 Feb 1955

SA-4861-G-1

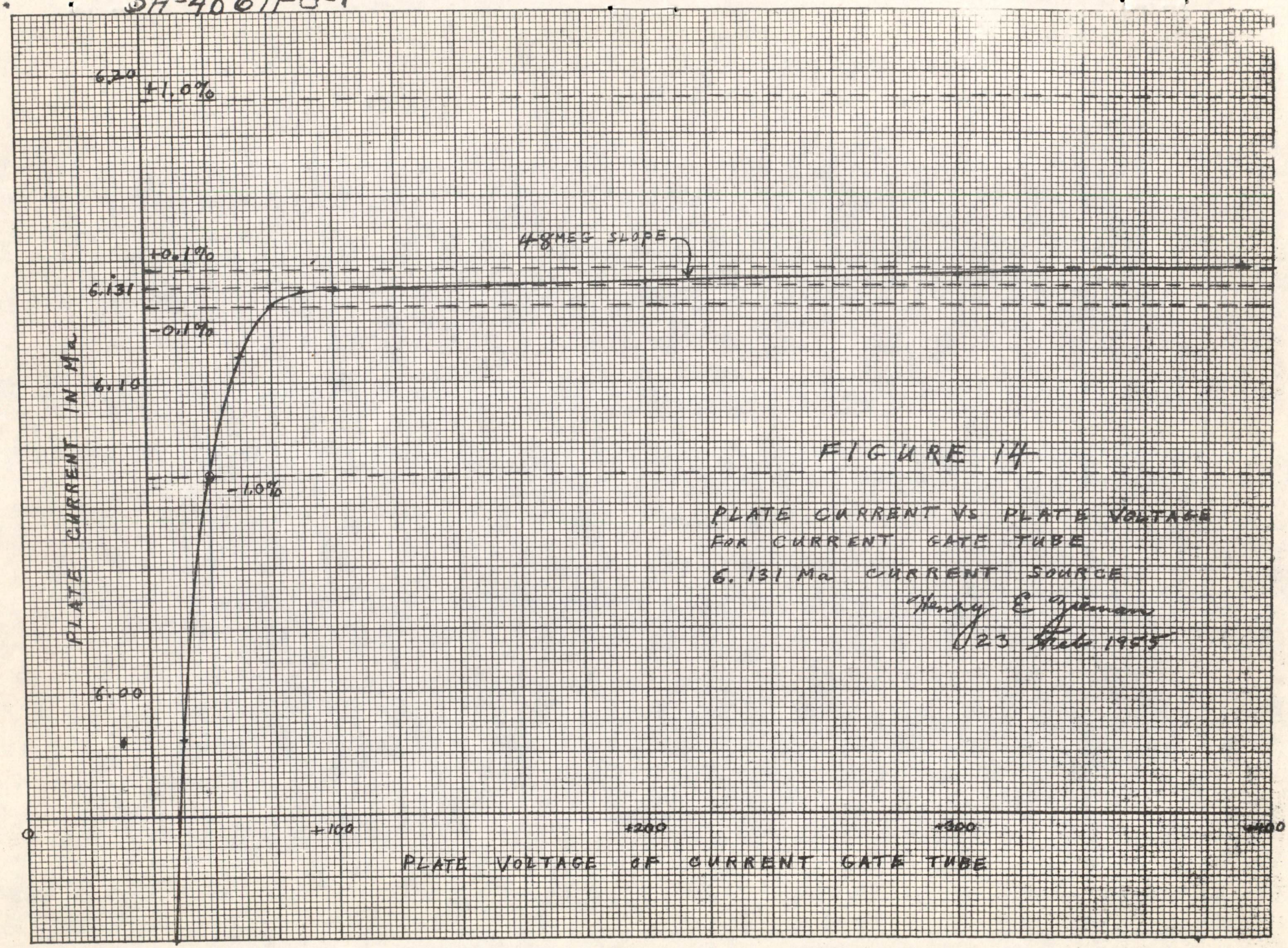
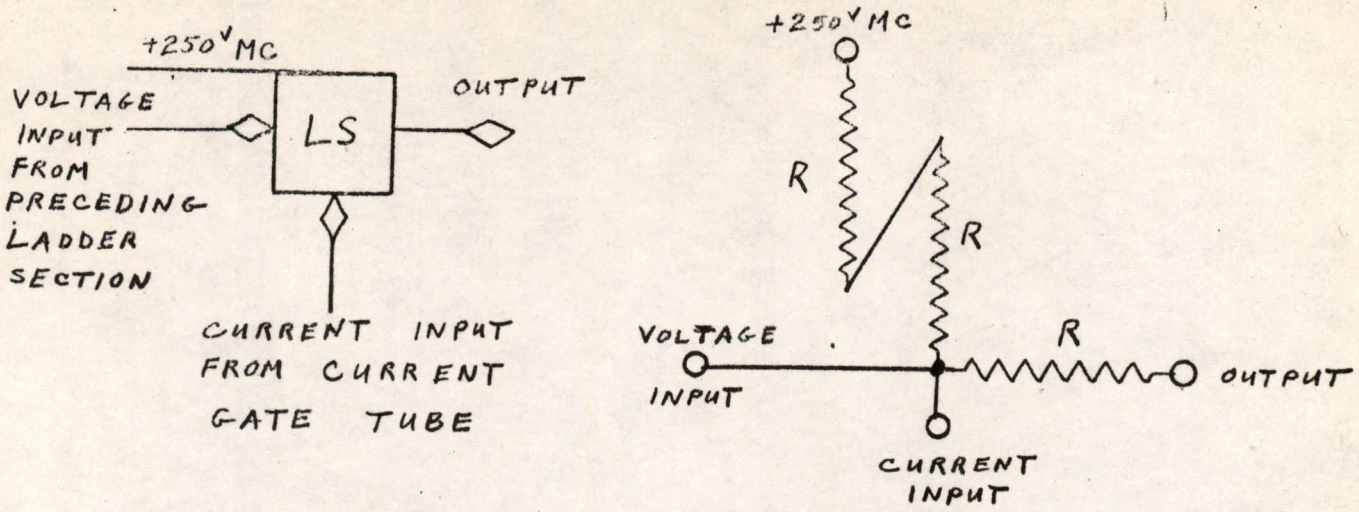


FIGURE 14

PLATE CURRENT VS PLATE VOLTAGE
FOR CURRENT GATE TUBE
6.131 Ma CURRENT SOURCE
Henry E Yeaman
23 Feb 1955

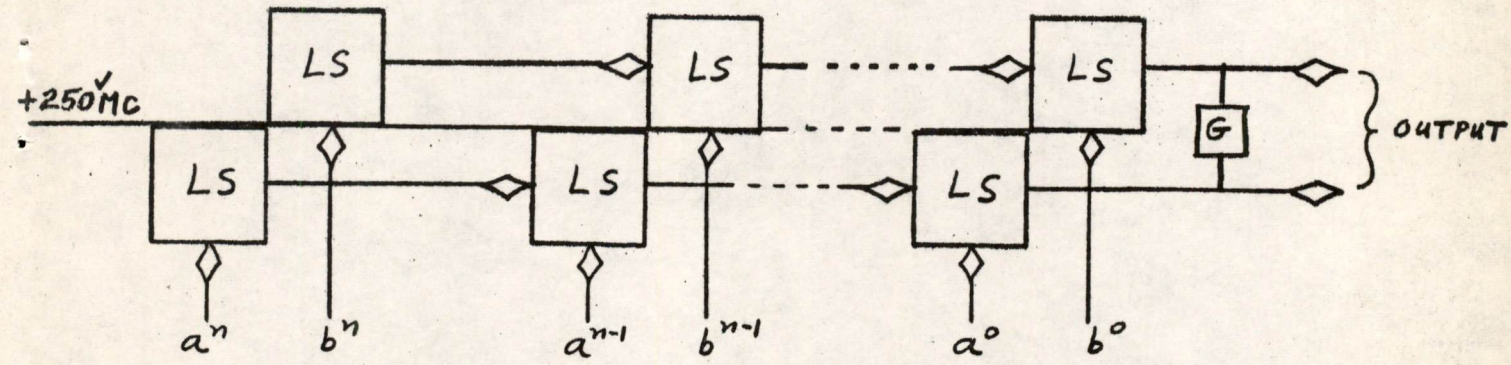


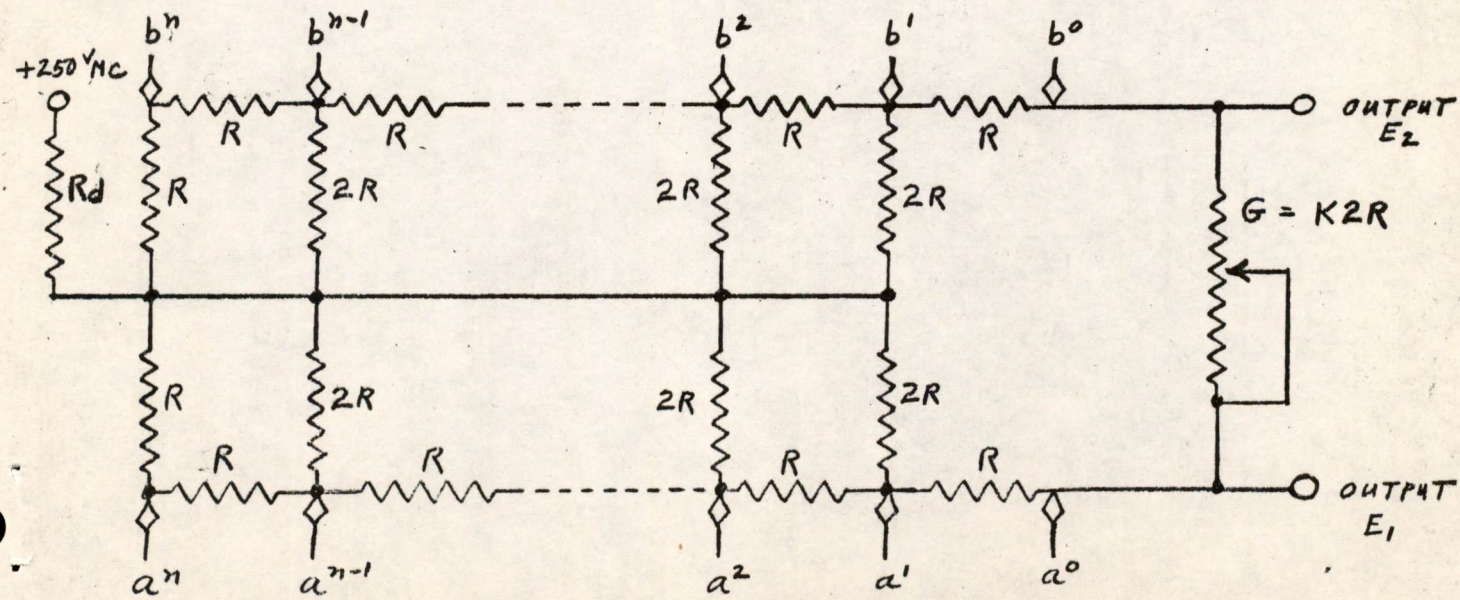
BLOCK SYMBOL

CIRCUIT DIAGRAM

SINGLE LADDER SECTION

FIGURE 15a





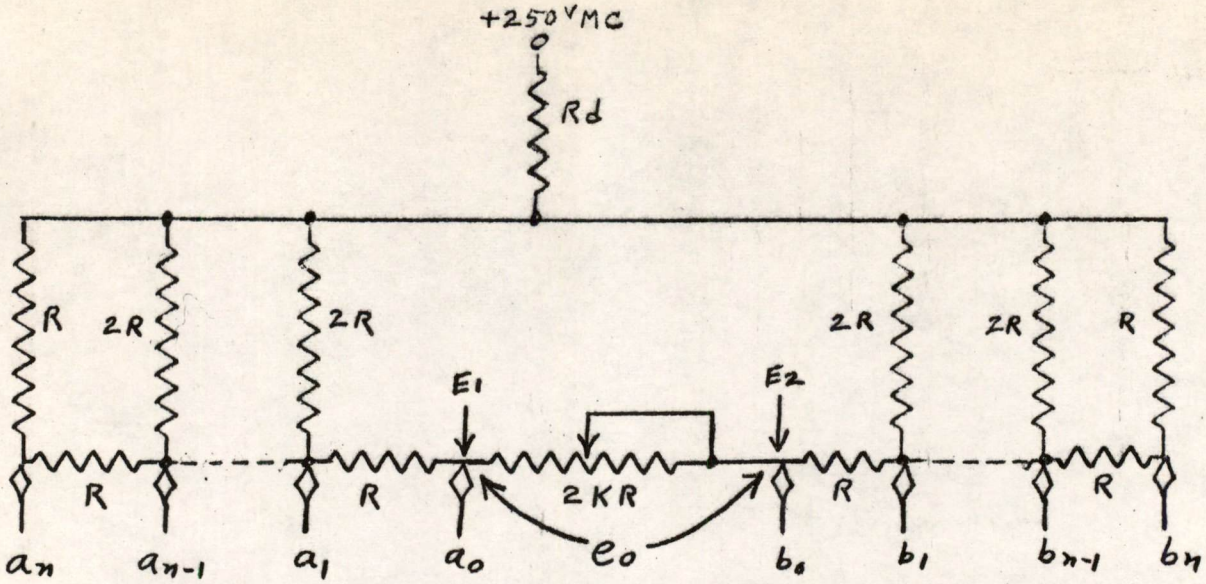
COMPLETE DECODER LADDER

FIGURE 15B

DECODER LADDER I.

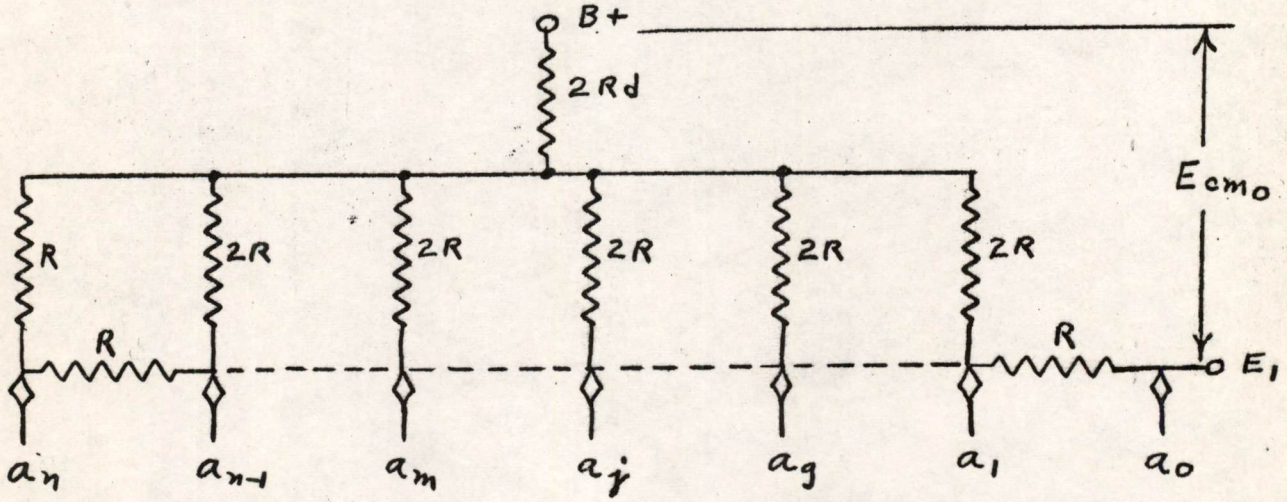
H. E. Zieman

SA-63878



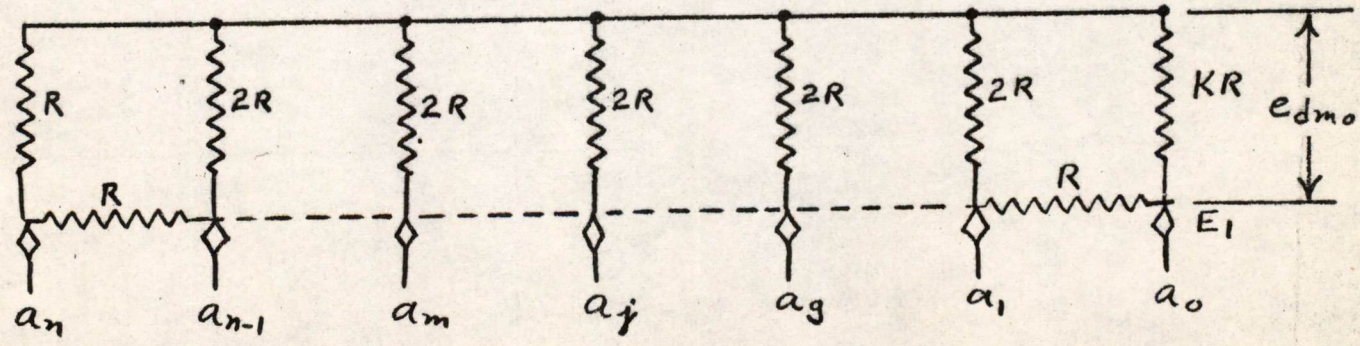
COMPLETE PUSH-PULL DECODER LADDER
WITH VARIABLE TERMINATION

FIGURE 16 a



COMMON MODE EQUIVALENT
OF
DECODER LADDER

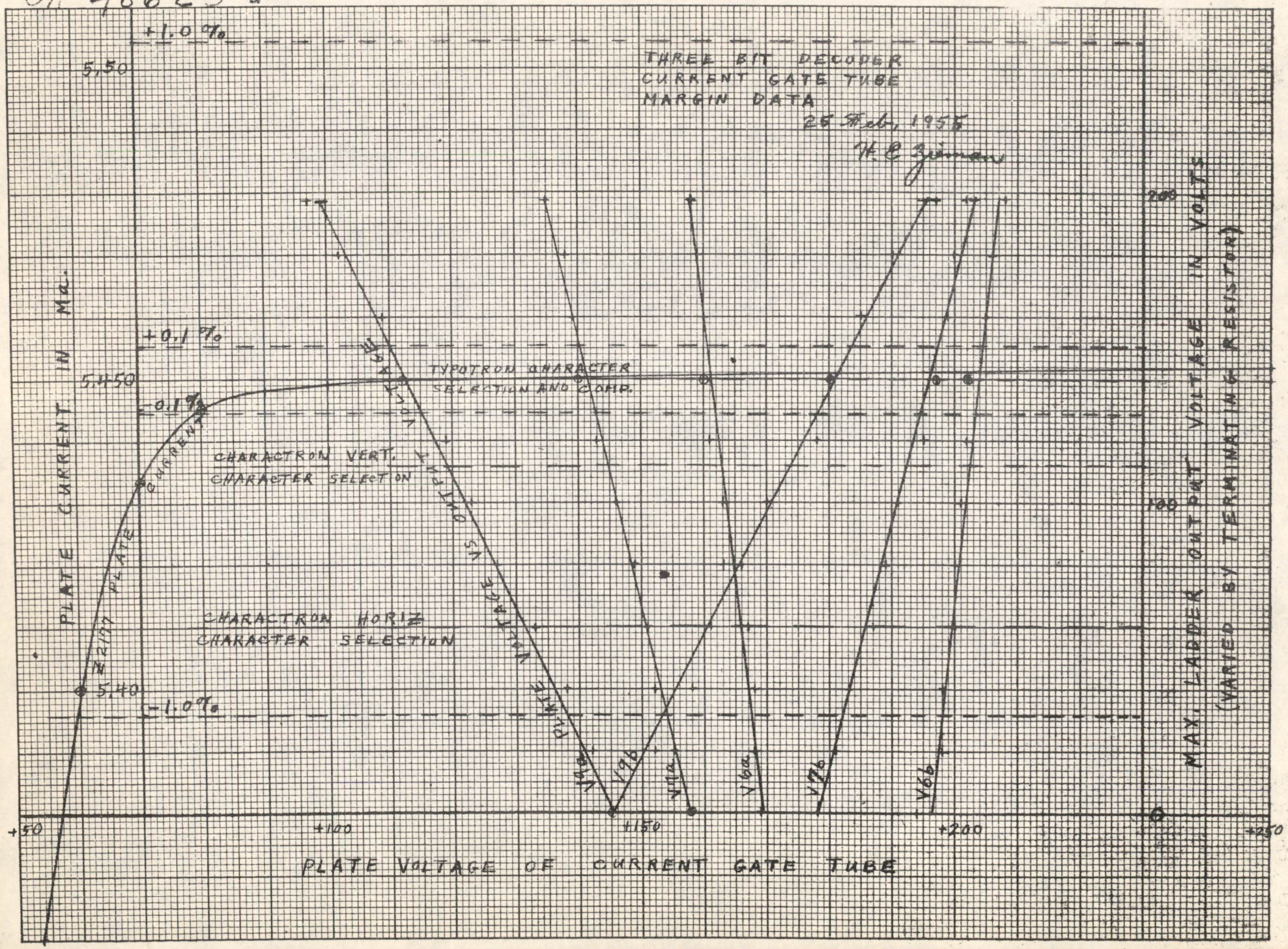
FIGURE 16b



DIFFERENTIAL MODE EQUIVALENT
OF
DECODER LADDER

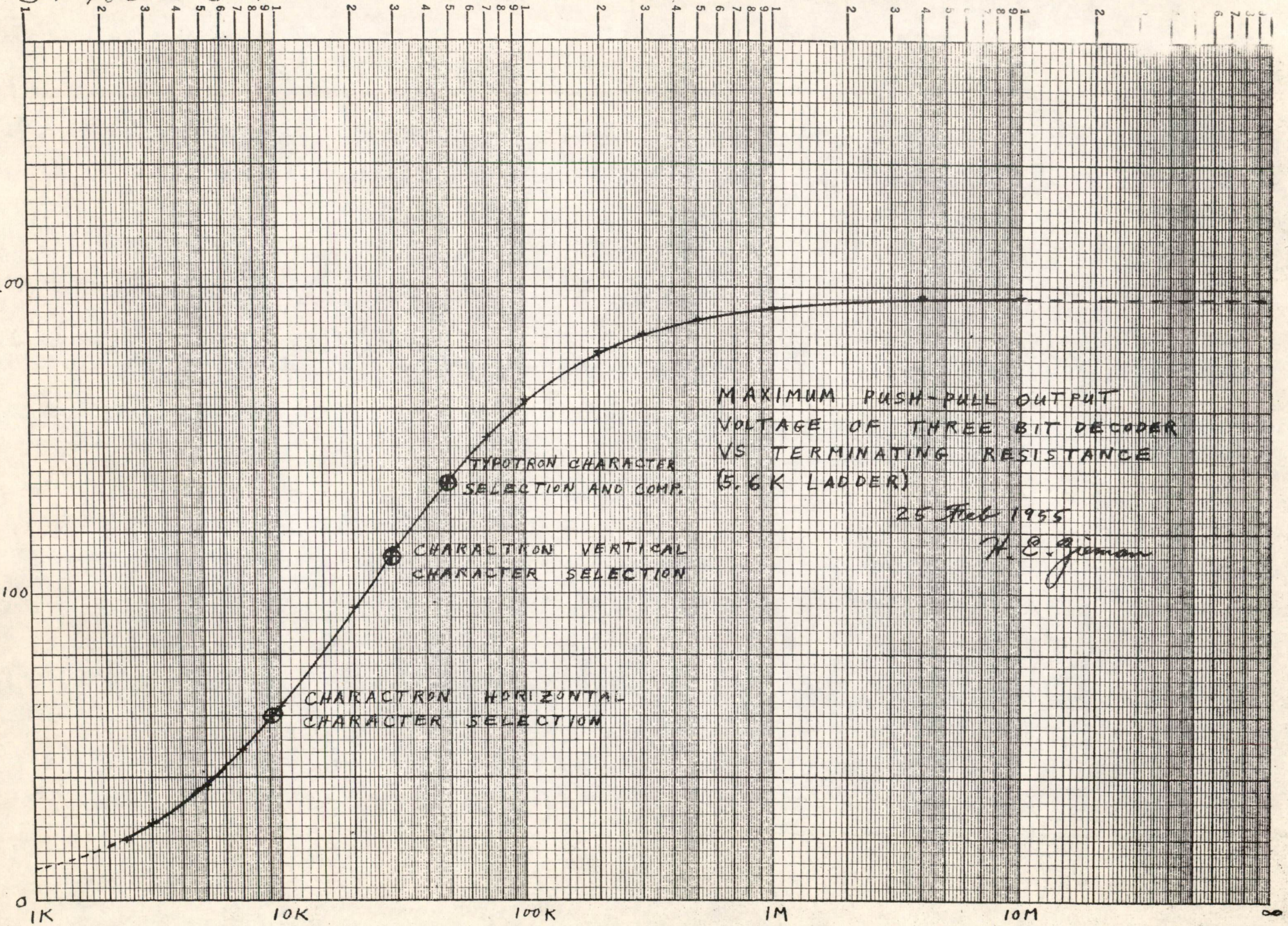
FIGURE 16C

SR-4862D-G-1



K+E SEMI-LOGARITHMIC 359-91G
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS

SA-48623-G-1



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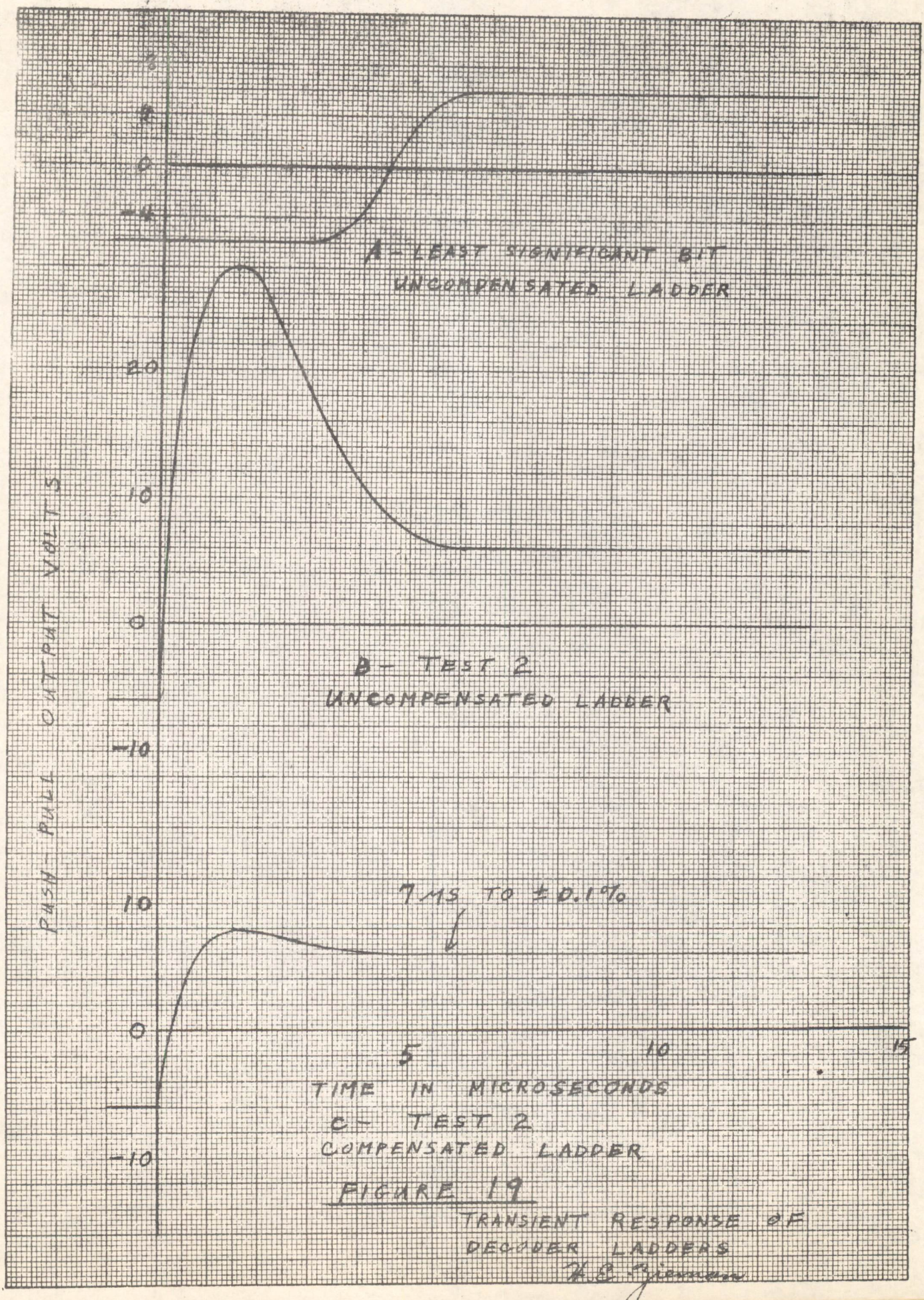


FIGURE 19

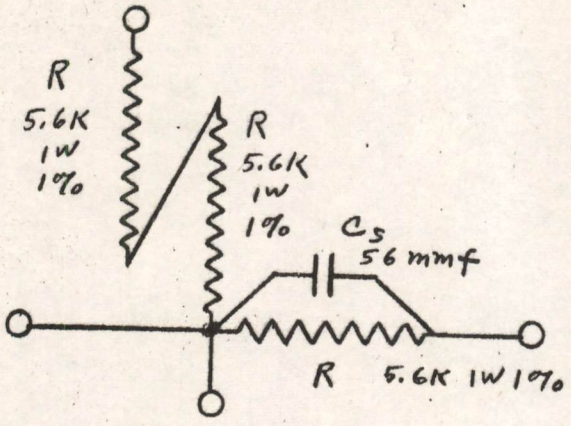
TRANSIENT RESPONSE OF DECODER LADDERS

R. E. Gjessing

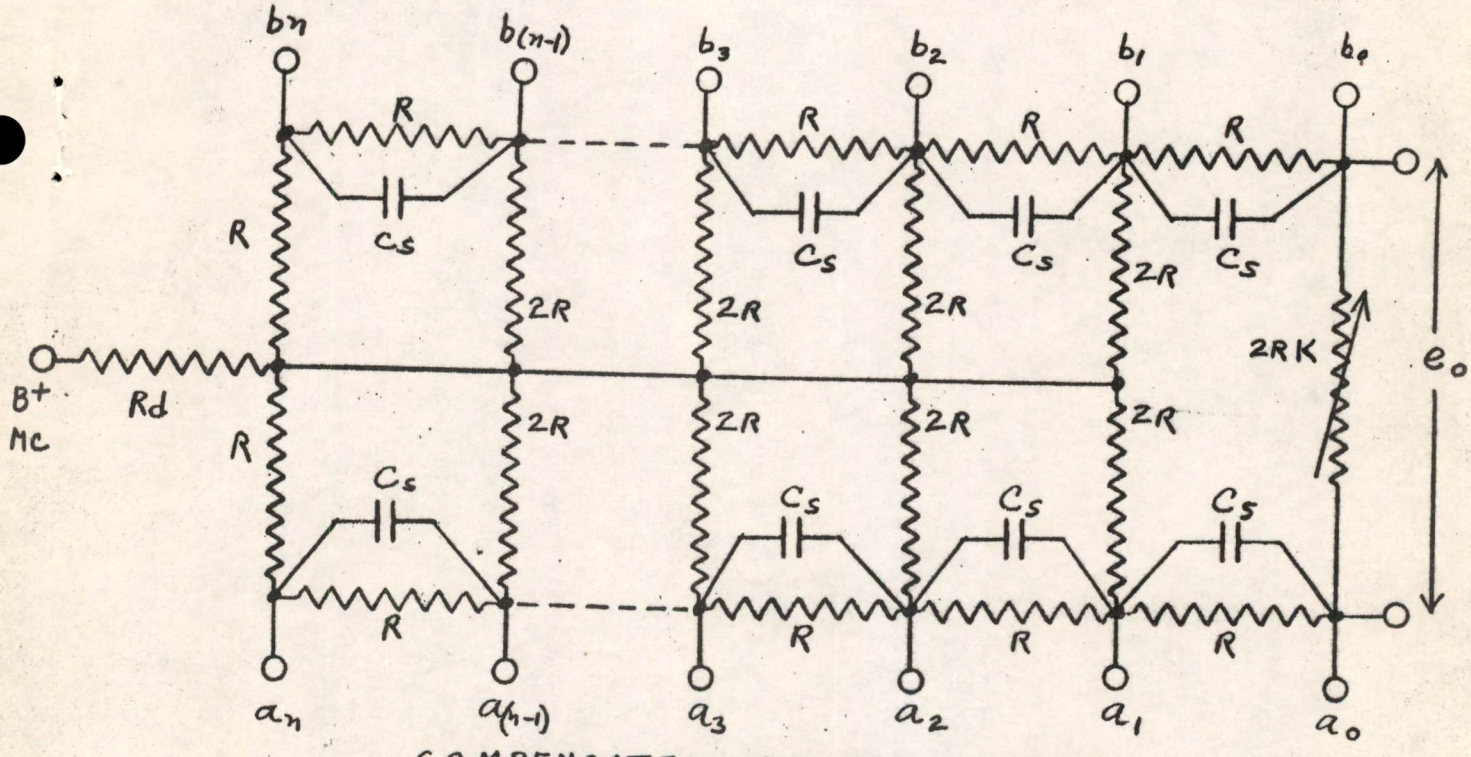
SA-48709

SA-48709

KEUFFEL & ESSER CO.
359-14
Millimeters, 5 mm. lines accented, cm. lines heavy.
MADE IN U.S.A.



COMPENSATED DECODER LADDER SECTION



COMPENSATED DECODER LADDER

FIGURE 20

COMPENSATED DECODER LADDER
H. E. Zieman

K. H. Olsen

B-191

Leo Jedynak
November 9, 1955

ELECTRICAL ENGINEERING DEPARTMENT

MASTER'S THESIS PROPOSAL

I. TITLE: CIRCUIT APPLICATION OF THE AVALANCHE PHENOMENON IN JUNCTION TRANSISTORS

II. STATEMENT OF THE PROBLEM:

Recent research has indicated that the avalanche region of operation of junction transistors has outstanding possibilities in circuit application. Attention is to be given to the problem of application of this effect to practical circuitry. There are four distinct parts to this problem:

1. A survey of the variation in the static characteristics of regular low frequency junction transistors in the avalanche region of operation. At present there are no transistors whose avalanche region characteristics have been controlled in manufacture.

2. Design, construction, and test of basic circuits employing the avalanche region of operation.

3. Formulation of design principles for the design of circuits using the avalanche region of operation of junction transistors.

4. Specification of the most desirable set, or sets, of transistor static characteristics in the avalanche region.

III. HISTORY OF THE PROBLEM:

A new mode of operation of junction transistors has recently been developed. This new mode of operation employs the avalanche phenomenon which occurs in semiconductors under high electric field conditions.[1,2] In the region of the collector characteristics where avalanche breakdown occurs the emitter to collector current gain is equal to or greater than unity. In many ways avalanche breakdown in

transistors is similar to gaseous breakdown in cold-cathode gas tubes, with one notable exception; the control element of the transistor, the base, does not lose control after the breakdown is initiated, as is the case in gas tubes.

The sequence of events which occurs in a junction transistor as it approaches and reaches avalanche breakdown is well understood by the researchers in the semiconductor field.[3] The phenomenon is adequately described mathematically and thus the factors affecting the characteristics are known and can be controlled in the manufacturing process. However, there has been very little work done in actual application of the avalanche phenomenon to circuitry. Kidd, Hasenberg, and Webster of RCA have recorded the results of the application to several basic circuits and suggest that considerable attention is merited by these and other circuit applications.[4] They found that typical low frequency junction transistors could be made to operate at the speeds displayed by point-contact transistors. Switching times measured in millimicroseconds were found easily attainable. It was also found that for a given power dissipation the junction transistor could be operated at a higher voltage than could the point-contact transistor. In brief, the junction transistor was found to be more versatile since it has all the characteristics of both types of transistors, but not all the disadvantages.

If the base electrode of a p-n-p junction transistor is positive with respect to the emitter electrode no emitter current flows and the transistor is said to be in "cutoff". If the collector voltage is now caused to become increasingly negative the depletion layer -- a region of existence of an electric field -- at the collector junction extends increasingly further into the base region and the electric field increases in strength. If surface breakdown due to contamination of the semiconductor surface, or punch-through due to the extension of the depletion layer to the emitter junction does not occur first, avalanche breakdown will eventually occur at some relatively large negative voltage -- from 50 volts to 100 volts for most types of junction transistors.

Avalanche breakdown occurs when a sufficient number of the holes in the depletion layer, which have been thermally generated in the base, attain sufficient energy from the electric field to produce one or more hole-electron pairs by impact ionization. The newly generated holes move rapidly to the collector and the corresponding electrons are swept back into the base region, and out the base electrode, where they forward bias the emitter into conduction. The holes injected at the emitter may now cause impact ionization and these resultant electrons bias the emitter even further into conduction. In fact, a high base-collector current gain is in operation and thus it is easily seen that the process can become highly regenerative with only a small percentage of the holes causing ionization.

The effect of the flow of electrons out of the base lead while the transistor is in the avalanche region of operation can be controlled by a resistance or a voltage. This results in a direct control of the collector current. If the base is caused to go sufficiently positive the emitter will again become back biased and the transistor will return to the cutoff state.

Operation in the avalanche region is characterized by emitter-collector current gain greater than unity, by a reversal of base current from that encountered in normal operation, and by three possible output resistances. Typical collector V-I curves show a negative resistance for the highest voltages, a zero resistance for slightly lower voltages, and a positive resistance for even lower voltages.[4] Both p-n-p and n-p-n junction transistors display these characteristics, but investigations have indicated that the p-n-p is by far the most useable of the two.[3]

IV. PROPOSED PROCEDURE:

Since no transistors are being made expressly for operation in the avalanche region it will be necessary to use regular low frequency junction transistors. The characteristics in the avalanche region will vary considerably from one unit to the next since there has been no

effort made to control them. A survey of the collector characteristics, in the avalanche region, of perhaps seventy-five junction transistors will be made. Both p-n-p and n-p-n transistors will be considered. From these transistors will be selected groups which display fundamental differences in characteristics. Special attention will be given to the useable range of collector voltage in the avalanche region, as well as to the magnitudes and voltage ranges of the negative and positive output resistances and the voltage range of the zero output resistance region. The linearity or nonlinearity of the characteristics will also be considered.

The selected transistors will be used in a variety of simple, basic circuits to determine the effects of their characteristics upon circuit operation and design. Using this experimental data and standard circuit theory a set of design principles will be developed to facilitate the design of circuits employing the avalanche phenomenon in junction transistors. The most desirable set, or sets, of transistor characteristics will also be indicated as the result of the experimental work.

The circuits to be built using the junction transistor in the avalanche region of operation will include, among others, a single-shot multivibrator, a flip-flop, and a free-running multivibrator. These three circuits employ a negative resistance region for operation and should give considerable information on the negative resistance portion of the collector characteristics. Another circuit which can employ the negative resistance characteristic is the regenerative amplifier. A chain of these amplifiers, with the output of the last amplifier used as the input to the first amplifier, will oscillate if the feedback is positive. This circuit will be built to facilitate measurement of response times without the need for complex triggering equipment.

The zero impedance region of operation can be studied with a voltage-regulator circuit. Here the transistor would be used to maintain a constant voltage across a varying load. If the load were made to

change abruptly, transient response could be observed over the active range of the zero impedance region of the collector characteristics. The zero or low output resistance region can also be studied with an impedance switch circuit. The principle of operation of one form of impedance switch puts the output impedance of the transistor in parallel with the load resistance of another transistor.[4] If the shunt transistor is placed in the low or zero output resistance region of operation it will attenuate the output signal of the other transistor. If the shunt transistor is in the normal state of operation it will produce negligible attenuation of the output.

There are probably additional circuits which merit consideration, a pulse amplifier for instance, and they will be investigated if time permits. The objective here is, however, to determine the principles of circuit design and the effects of transistor characteristics on these principles rather than to produce a group of optimized circuits. All of the information obtained, experimentally or otherwise, will be used to specify a desirable set, or sets, of collector characteristics in the avalanche region of transistor operation.

V. EQUIPMENT NEEDED:

The test equipment and materials will be supplied by Lincoln Laboratory.

VI. ESTIMATED TIME:

	Hours
Preparation of Proposal	70
Further search of literature	30
Experimental work and analysis	175
Correlation of results and formulation of conclusions	60
Preparation of thesis	70
Total	405

SIGNED: Leo Jedynak
L. Jedynak

LJ/md

Date: November 9, 1955

VII. SUPERVISION AGREEMENT:

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

APPROVED: Torben Meisling
Torben Meisling

Distribution:

Baker, Richard H.
Best, Richard L.
Linvill, William K.
Rediker, Robert H.
Stevenson, Donald T.

Group 63, Staff

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1. McKay and McAfee, "Electron Multiplication in Silicon and Germanium," Phys. Rev., 91, p. 1079, 1953.

2. K. G. McKay, "Avalanche Breakdown in Silicon," Phys. Rev., 94, p. 877, 1954.

3. S. L. Miller and J. J. Ebers, "Alloyed Junction Avalanche Transistors," Bell System Technical Journal, Vol. XXXIV, No. 5, p. 883, September, 1955.

4. Kidd, Hasenberg, and Webster, "Delayed Collector Conduction, a New Effect in Junction Transistors," RCA Review, Vol. XVI, No. 1, p. 16, March, 1955.

H. Olsen
B-191A

Memorandum 6M-4035

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: TRANSISTOR CIRCUITS COURSE. NUMBER 5.
THERMAL STABILITY OF TRANSISTORS.

To: Distribution List

From: Donald J. Eckl

Date: December 2, 1955

Approved: DJE
for David R. Brown

Abstract: The properties of transistors depend considerably on temperature. It has been pointed out previously that above a certain temperature impurity semiconductors behave like intrinsic material, putting an end to transistor action. However, even well below this point temperature plays an important part in circuit stability. The cutoff or leakage current in germanium transistors increases about 10 per cent per degree centigrade. Other parameters are also affected but to a lesser extent. Thermal runaway may be an important consideration in power transistors and may lead to their destruction if sufficient precautions are not undertaken.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

1.0 The I_{co} (leakage current) Problem

The normal grounded-base transistor output characteristics appear as shown in the solid lines of Figure 1. The cutoff or leakage current is shown as I_{co}.

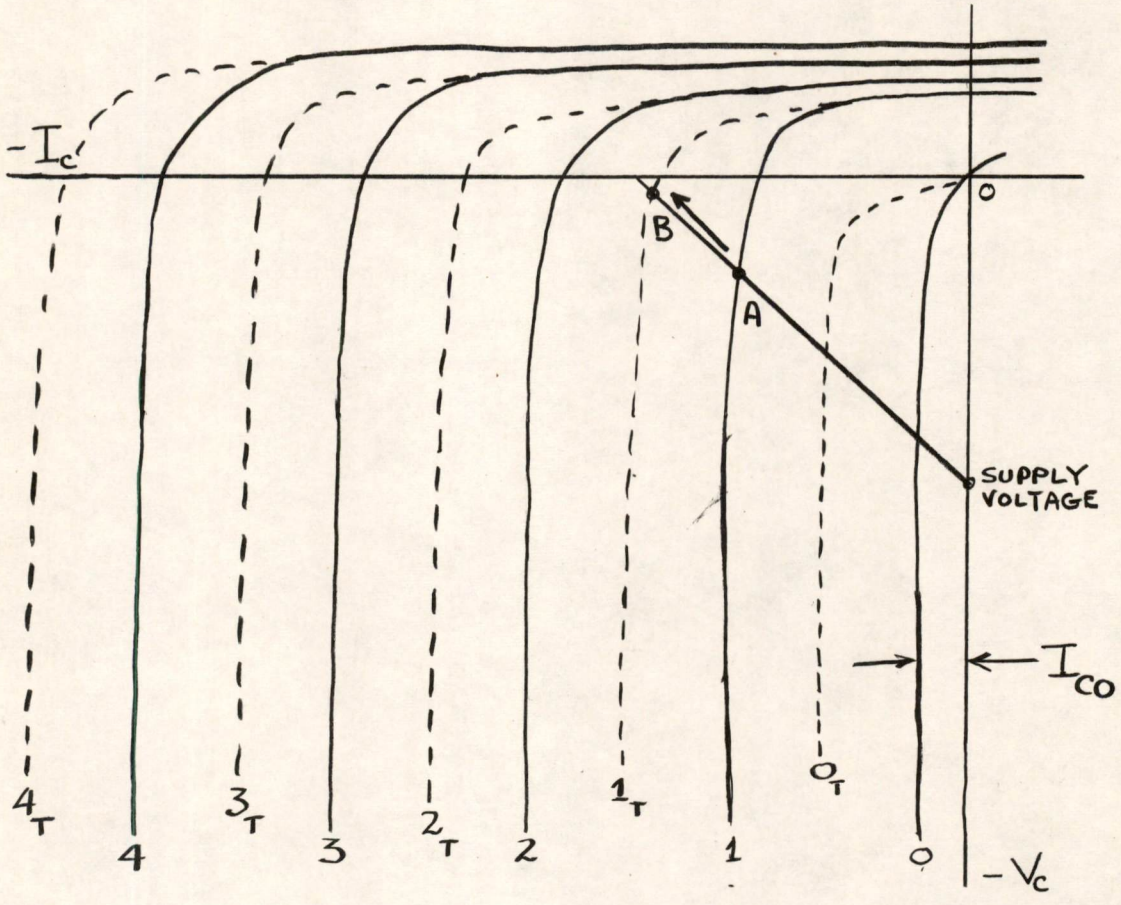

Fig. 1 Effect of I_{co} on Bias Point

A typical load line is shown with a bias point at A having an emitter current fixed at 1 ma. At some higher temperature T^{o} the characteristics become the dotted lines, and the operating point shifts to B which is no longer suitable for linear operation with reasonable signal amplitudes. This shift is almost entirely due to the increase of leakage current I_{co} with temperature.

Consider, moreover, the case of the grounded-emitter amplifier shown in Figure 2. The biases are such that the transistor is cut off. However, the leakage I_{co} represents a current flow outward from the base. To get current gain from a grounded-emitter stage normally

requires a current flow outward through the base lead. However, the transistor only knows that "forward current" is being taken from the base; its ultimate destination is of no concern. It has already been

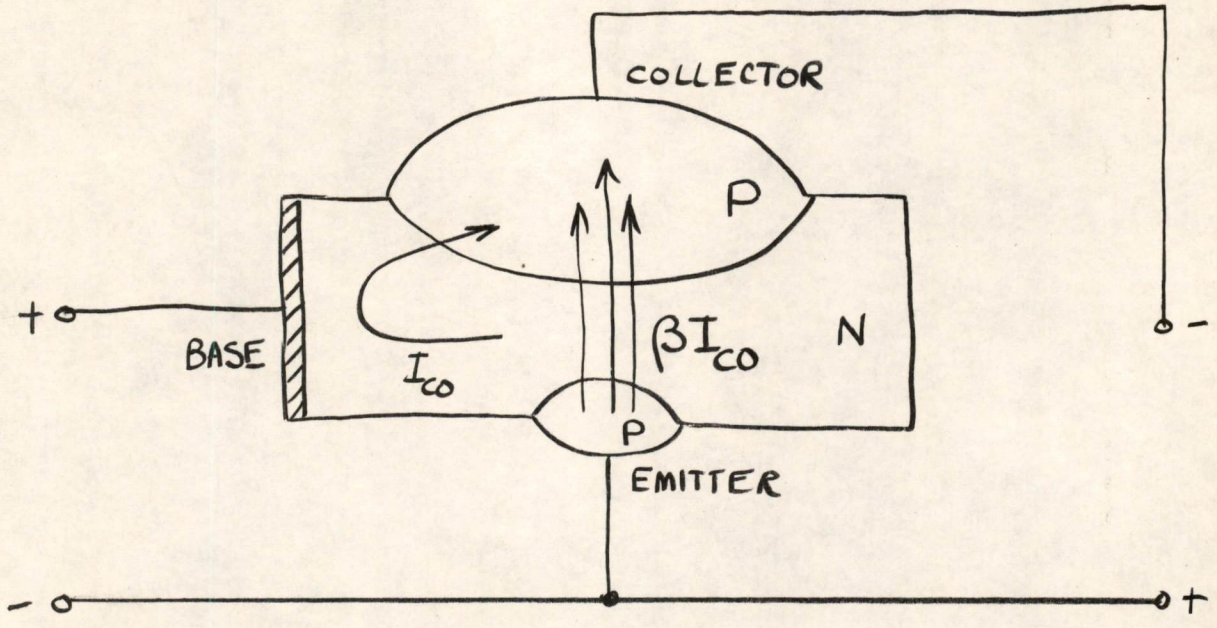

Fig. 2 Leakage in a Grounded-Emitter Stage

pointed out in a previous note that the only way the transistor can supply such a base current is by means of an emitter-collector current $\beta = \alpha / 1-\alpha$ times as large. The removal of holes from the base causes the base to go negative with respect to the emitter until such a current flow can occur. Therefore, I_{co} temperature-dependence is more serious in a grounded-emitter circuit since the resultant leakage current may be 10-50 times as large.

To get a quantitative picture of the I_{co} temperature-dependence we will look at the case of the p-n-p junction transistor.

2.0 Leakage Current at the Collector of a P-N-P Transistor

We are interested in conditions at a reverse-biased collector junction of a p-n-p transistor. This is shown in Figure 3 along with a potential profile for the junction. Note that the entire voltage drop takes place across the junction. Holes, which act as charge carriers, are thermally generated in the valance band of the N-region. These holes in the absence of an electric field will diffuse to the junction

boundary where they are accelerated into the P-region immediately by the field existing there.

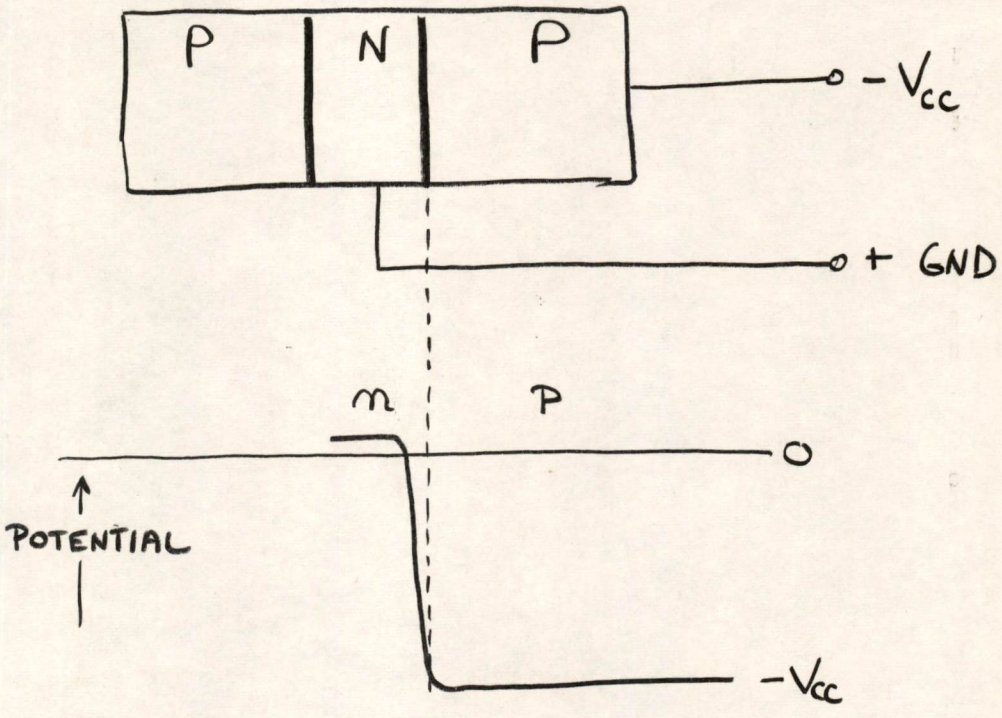

Fig. 3 Back-Biased Collector Junction

Suppose, following a treatment given by Shockley, we consider for a moment a slab of N-type material which has an average hole concentration of p_n per unit volume. Assume that these holes decay by recombination with electrons and that they have an average lifetime τ. The rate in numbers per second at which these holes combine with electrons per unit volume must be p_n/τ. Under equilibrium conditions this must also be the rate of thermal generation of holes per unit volume.

Now in the case of the base region of the transistor, we would expect all thermally generated holes within a diffusion length of the junction to drift rapidly to the junction and be accelerated into the P-region. The diffusion length, L_p, is an average distance which a hole can drift before recombining with an electron and is a few millimeters in transistor base material. Since the transistor base width W is small compared to the diffusion length, all thermally generated holes in the base will diffuse to the boundary. The rate of flow will be

$\left(\frac{p_n}{\tau}\right)$ W. holes per square centimeter per second.

Multiplying by q will give the leakage current density flowing across the junction.

$$\therefore I_{co} = q \frac{p_n}{\tau} W. \text{ per square centimeter junction area.} \quad (1)$$

If we make use of the relationship,

$$L_p = \sqrt{D_p \tau_p} \qquad \text{or} \qquad \tau = L^2/D.$$

where D_p = the diffusion coefficient in cm^2/sec, we get the customary expression for I_{co}.

$$I_{co} = qD_p \left(\frac{P_n}{L_p{}^2}\right) W. \quad (2)$$

It is well to note that for a grown p-n diode with end pieces wider than the diffusion length, L_p must be substituted for W and the familiar expression for diode leakage is obtained.

There will also be a leakage term of the same form for thermal electrons generated in the collector region and accelerated into the base. However, the width of the recrystallized p-type collector region is much smaller than W and n_p (the number of thermal electrons) is smaller than p_n because the collector region resistivity is much less. As a result, the electron contribution to I_{co} for an alloy pnp is slight.

3.0 Temperature Dependence of I_{co}

The following derivation is based on the energy-band theory of semiconductors and Fermi-Dirac statistics and follows Shockley's method. (Those unfamiliar with this theory may skip the next few equations and consider the result of the derivation which gives the relation between I_{co} and temperature.)

As shown above, $I_{co} = p_n \left(\frac{qw}{\tau}\right)$ per square centimeter.

Now it can be shown[1] that,

$$n_n p_n = 2.33 \times 10^{31} T^3 \exp\left(-\frac{E_G}{kT}\right). \quad (3)$$

---

1. Shockley, W., "Electrons and Holes in Semiconductors," p.245, D. Van Nostrand Company, Inc., New York, 1950.

$$\therefore I_{co} = 2.33 \times 10^{31} \left(\frac{qw}{n_n} \cdot \frac{1}{\tau}\right) T^3 \exp\left(-\frac{E_G}{kT}\right).$$

But $n_n \approx N_D - N_A$, the difference in the number of donors and acceptors. Also we can make the assumption (not necessarily a very good one) that

$$\tau = \frac{m}{q}\mu \approx \frac{m}{q}\mu_o T^{-3/2}$$

$$\therefore I_{co} = 2.33 \times 10^{31} \left\{\frac{q^2 w}{(N_D - N_A) m \mu_o}\right\} T^{3/2} \exp\left(-\frac{E_G}{kT}\right)$$

The temperature-dependent part of the expression is

$$T^{3/2} \exp\left(-\frac{E_G}{kT}\right)$$

Suppose we evaluate this at some temperature

$$T_o + \Delta T$$

where T_o is a fixed temperature and ΔT a small increment.

$$\therefore (T_o + \Delta T)^{3/2} \exp\left\{\frac{-E_G}{k(T_o + \Delta T)}\right\} =$$

$$T_o^{3/2}\left(1 + \frac{\Delta T}{T_o}\right)^{3/2} \exp\left\{\frac{-E_G}{kT_o\left(1 + \frac{\Delta T}{T_o}\right)}\right\}$$

Expanding each part separately:

$$\left(1 + \frac{\Delta T}{T_o}\right)^{3/2} \approx 1 + \frac{3}{2}\frac{\Delta T}{T_o} + \sim\sim\sim \approx \exp\left(\frac{3}{2}\frac{\Delta T}{T_o}\right).$$

$$\exp\left\{\frac{-E_G}{kT_o\left(1 + \frac{\Delta T}{T_o}\right)}\right\} \approx \exp\left\{\frac{-E_G}{kT_o}\left(1 - \frac{\Delta T}{T_o}\right)\right\} \approx \exp\left(\frac{-E_G}{kT_o}\right)\exp\left(\frac{E_G \Delta T}{kT_o^2}\right).$$

Therefore we can express the temperature dependence of I_{co} (subject to the above assumptions and approximations) as follows:

$$I_{co} = \text{const.}\ T_o^{3/2} \exp\left(-\frac{E_G}{kT_o}\right)\exp\left\{\left(\frac{3}{2T_o} + \frac{E_G}{kT_o^2}\right)\Delta T\right\} \qquad (4)$$

or $$I_{co} = \left(I_{co}\right)_o \exp (\text{const}\ \Delta T).$$

The constant evaluated at 278°K is

$$\frac{3}{2T_o} + \frac{E_G}{kT_o^2} = \frac{3}{2 \times 278} + \frac{8300}{(278)^2} = 0.11 \text{ per deg C.}$$

Therefore the I_{co} temperature dependence is given by

$$I_{co} = (I_{co})_{25°C} \exp \left[0.11\ (T-25)\right] \text{ per unit area.} \qquad (5)$$

That is, the leakage current increases about 11 per cent per degree centigrade at room temperature, or it doubles every 6 or 7°C.

4.0 Thermal Stability of Transistors

Consider the equivalent circuit of a transistor which has an I_{co} leakage as shown below.

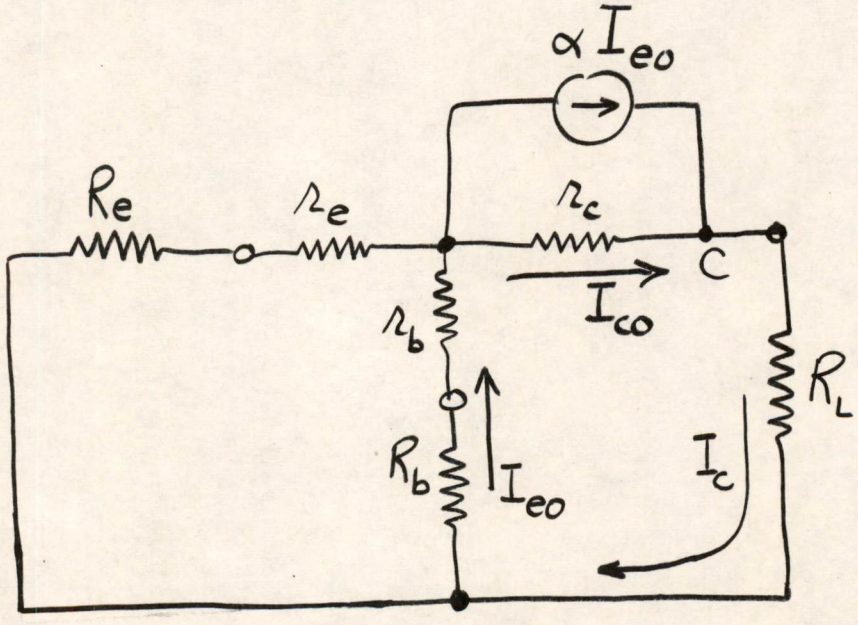

Fig. 4 Transistor with Leakage

The leakage current I_{co} splits between the base and emitter branches. The emitter current I_{eo} causes the current generator to become active, increasing the collector current. In the steady state,

$$I_c = I_{co} + \alpha I_{eo} \qquad \text{at point C.}$$

But $$I_{eo} = \left(\frac{\bar{R}_b}{\bar{R}_e + \bar{R}_b} \right) I_c.$$

where $\bar{R}_b = R_b + r_b$ and $\bar{R}_e = R_e + r_e$.

$$\therefore I_c - \left(\frac{\alpha \bar{R}_b}{\bar{R}_e + \bar{R}_b} \right) I_c = I_{co}$$

or $$I_c = \frac{I_{co}}{1 - \left(\frac{\alpha \bar{R}_b}{\bar{R}_e + \bar{R}_b} \right)} = SI_{co} \qquad (6)$$

The quantity S is called the circuit stability and may be written,

$$S = \frac{1}{1 - \frac{\alpha}{1 + \bar{R}_e/\bar{R}_b}} \qquad (7)$$

If we add d-c biases the equation for I_c becomes,

$$I_c = SI_{co} + f_1(V_E) + f_2(V_c)$$

The circuit stability is therefore given by

$$S = \frac{\delta I_c}{\delta I_{co}} \qquad (8)$$

Now consider the question of thermal stability. The maximum internal power dissipation in a transistor occurs at the collector junction under normal bias conditions. This dissipation causes a temperature rise which increases I_{co} and causes more dissipation.

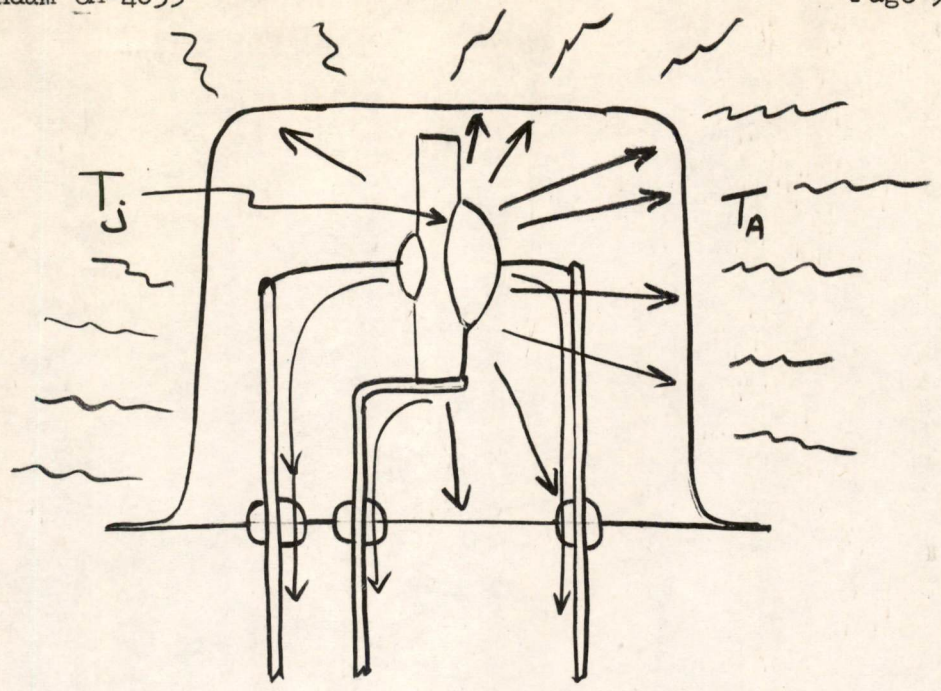

Fig. 5 Heat Flow in a Junction Transistor

The heat generated at the junction (temperature T_j) flows outward to the atmosphere (temperature T_a) through the potting compound and along the leads.

The condition for thermal stability is that the increase in heat dissipation due to the temperature rise at the junction must be less than the corresponding increase in heat flow from the junction. That is,

$$\frac{dP}{dT_j} < \frac{1}{H} \quad \text{for thermal stability.} \tag{9}$$

where P = total power dissipation in the transistor

T_j = collector junction temperature

H = total thermal resistance, i.e., the rise per watt dissipation of the junction temperature above ambient.

Now suppose we consider the case of Figure 4 and use the expression relating I_{co} to temperature.

Then $$I_c = SI_{co} = SI_{co25} \exp\left(\frac{\Delta T}{\Theta}\right)$$

where I_{co25} is the leakage current at 25°C

ΔT is the junction temperature rise above 25°C

Θ is the "thermal constant" of germanium

With a back collector-bias applied, the power dissipation is

$$P = V_c I_c = V_c S I_{co25} \exp\left(\frac{\Delta T}{\Theta}\right)$$

$$\therefore \frac{dP}{dT_j} = \frac{V_c S I_{co25}}{\Theta} \exp\left(\frac{\Delta T}{\Theta}\right)$$

Now suppose we evaluate this with the junction at room temperature where $\Delta T = 0$.

$$\therefore \frac{dP}{dT_j} = \frac{V_c S I_{co25}}{\Theta} < \frac{1}{H} \text{ for stability.}$$

or, to maintain a stable condition when the transistor is connected to a circuit with only a collector bias applied at room temperature, the supply voltage must be below a maximum given by :

$$V_o = \frac{\Theta}{H S I_{co25}} . \qquad (10)$$

Now consider what happens when the transistor is biased so that an additional bias collector current I_{c_1} is flowing. In this case,

$$I_c = S I_{co25} \exp\left(\frac{\Delta T}{\Theta}\right) + I_{c_1} .$$

and $$P_c = V_c S I_{co25} \exp\left(\frac{\Delta T}{\Theta}\right) + V_c I_{c_1} .$$

but $\Delta T = H P_c$ so for stability:

$$\frac{dP_c}{dT_j} = \frac{dP_c}{d(HP_c)} = \frac{V_c S I_{co25}}{\Theta} \exp\left(\frac{HP_c}{\Theta}\right) < \frac{1}{H} .$$

or $$\exp\left(\frac{HP_c}{\Theta}\right) < \frac{\Theta}{H S I_{co25} V_c} = \frac{V_o}{V_c} .$$

$$P_c < \frac{\Theta}{H} \ln\left(\frac{V_o}{V_c}\right) .$$

or, to prevent thermal runaway the collector current must meet the

the condition below:

$$I_c < \frac{\Theta}{HV_c} \ln\left(\frac{V_o}{V_c}\right). \qquad (11)$$

There is one important consideration that has been neglected for the sake of simplicity in the above calculations -- i.e.-- the variation of collector voltage with I_c due to the drop across the collector load. The expressions above are for zero R_L (Vc assumed constant). The larger the load resistance, the more the safety factor above the predicted values.

The purpose of the above discussion was to show qualitatively how thermal runaway can take place, rather than to calculate a quantitative runaway point.

There are, in general, three factors which limit the operating range of power transistors: the maximum dissipation rating, thermal runaway, and ambient temperature. These limits are shown below in Figure 5.

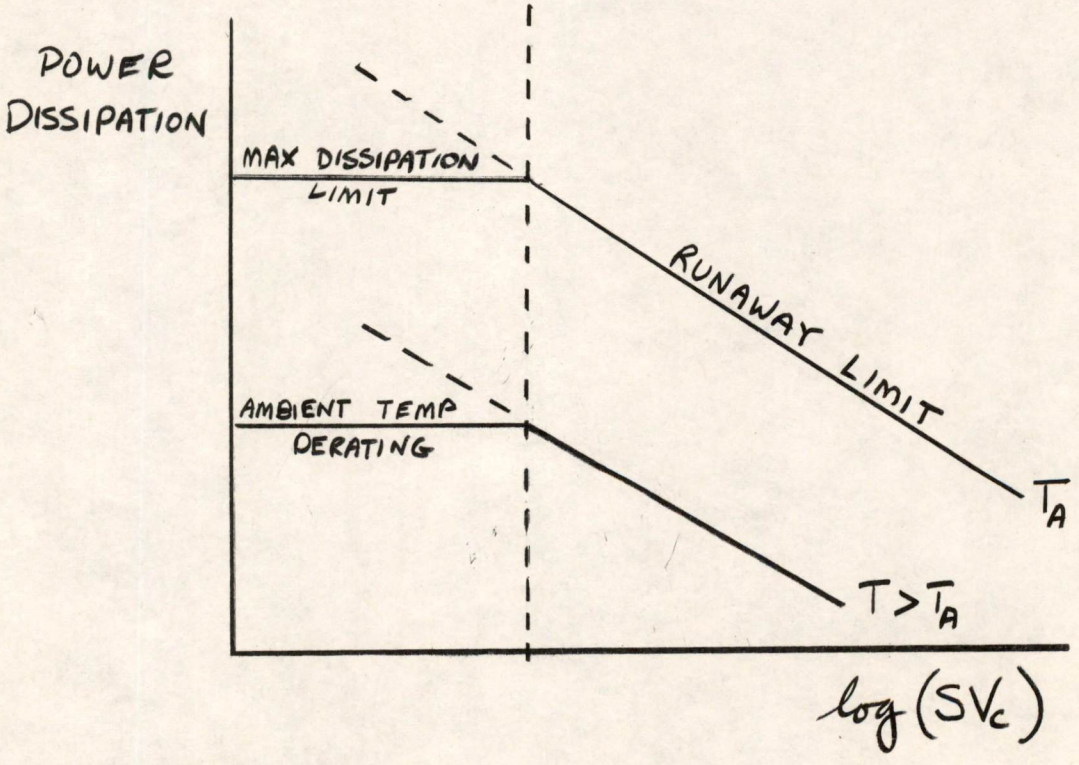

Fig. 5 Power Dissipation Limits

The transistor has a maximum dissipation based on the maximum allowable junction temperature. It must be derated for ambient temperatures above 25°C and for runaway conditions as shown in Figure 5. This derating may be expressed by the following equation:

$$P_{allowable} = P_{max} - C_1 \ln(SV_c) - C_2(T-T_A). \qquad (12)$$

In general there may be two other limiting factors. One, the maximum current rating, usually applies only to maintaining certain gain specifications. The second, the maximum voltage rating, puts a right-hand limit to the operating region in Figure 5.

The problems discussed in this note affect all types of transistors. They become particularly acute, however, in the case of power transistors where currents and dissipations are unusually high. Thermal runaway can destroy a transistor if proper precautions are not taken.

Donald J. Eckl

Donald J. Eckl

DJE:dg

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Webster, W.M., Private discussion on thermal runaway.

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SUBJECT: DESIGN AND STATIC ANALYSIS OF EMITTER-FOLLOWER INVERTER COMBINATION

To: D. R. Brown

From: T. H. Meisling

Date: December 19, 1955

Approved: DRB
D. R. Brown

Abstract: Design equations for an emitter-follower inverter combination (EFI) are developed. The only constraint placed on the circuit is that the point of unit (dc) voltage amplification is situated half-way between the two extremes of input (or output) voltage. The number, n, of EFI stages which may be driven from one EFI stage is expressed as a function of collector supply voltage, the degree of saturation required in the inverter, an internal resistance ratio, and the alphas. The effect on the degree of saturation when the alphas vary is calculated. It is shown quantitatively how requirements of a large n and large tolerances conflict.

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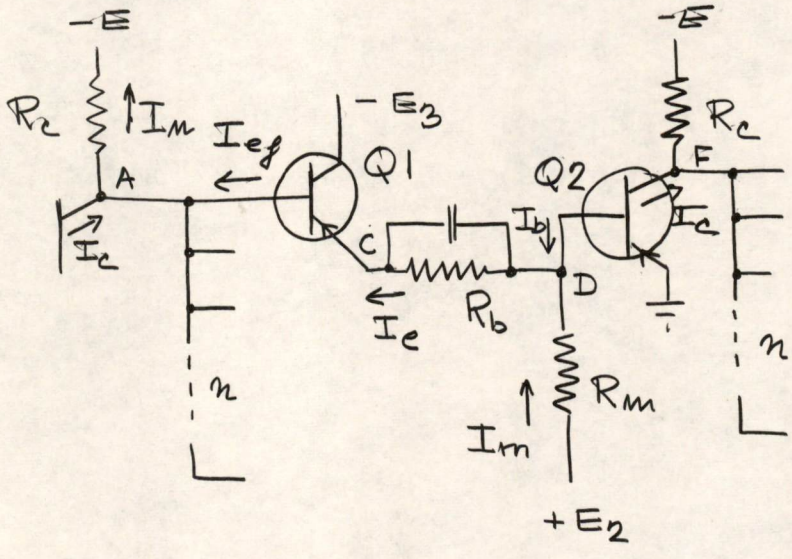
The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Introduction

The circuit to be analyzed was intended as a building block with the same functional properties as a surface-barrier transistor, but with improved electrical characteristics. Such a unit has the advantage that it can be used in simple "direct-coupled" logic and in flip-flops; all circuit complications are concentrated in the emitter-follower inverter combination (EFI) which may be packaged and handled the same way a transistor is now handled.

Design

The circuit to be analyzed is shown below.



I" = larger of two current values

I' = smaller of two current values

I = halfway value (see below)

In the analysis all emitter-base voltages and the emitter-collector voltage during saturation of Q_2 will be assumed 0. λ shall mean $\frac{\beta \text{ active}}{\beta \text{ sat.}}$ for the chosen degree of saturation of Q_2. $\lambda > 1$. Q_1 operates as an emitter-follower. E_3 is chosen so that it remains in the active region. Q_2 draws no base current in the off-condition.

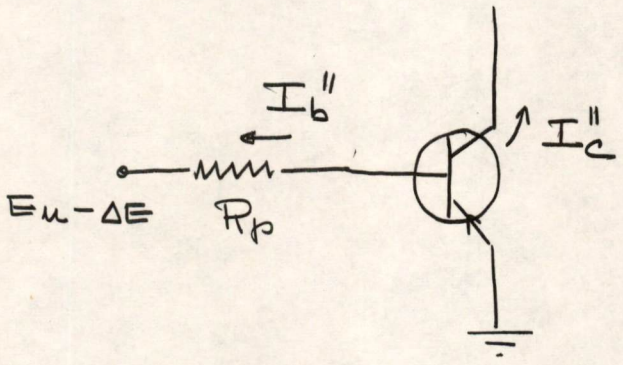
The circuit will be constrained to have a point of unit amplification situated half-way between the two extremes (in terms of input and output voltages). The constraint insures a transfer characteristic with a maximum of margin against noise.

ΔE = voltage swing at point D

δE = voltage swing at point C and A

E_u = the more positive voltage at D.

Introduce $R_p = \frac{R_m R_b}{R_m + R_b}$ and consider base circuit of Q_2 saturation:



$$I_b'' = \frac{\Delta E - E_u}{R_p} \tag{1}$$

Halfway:

$$I_b = \frac{\frac{\Delta E}{2} - E_u}{R_p} \tag{2}$$

At the halfway point the transistor is in the active region, then

$$I_b = \frac{1}{\beta} I_c'' \cdot \frac{1}{2} \tag{3}$$

according to the constraint mentioned earlier.

In saturation we have

$$I_b'' = \lambda \frac{1}{\beta} I_c'' \tag{4}$$

Now according to equations (1),(2),(3), and (4)

$$\frac{I_b''}{Ib} = 2\lambda = \frac{\Delta E - E_u}{\frac{\Delta E}{2} - E_u} = \frac{\frac{\Delta E}{E_u} - 1}{\frac{1}{2}\frac{\Delta E}{E_u} - 1} \tag{5}$$

Solving for $\frac{\Delta E}{Eu}$ one obtains

$$\frac{\Delta E}{E_u} = \frac{2\lambda - 1}{\lambda - 1} \tag{6}$$

Inserting (6) in (1) we obtain

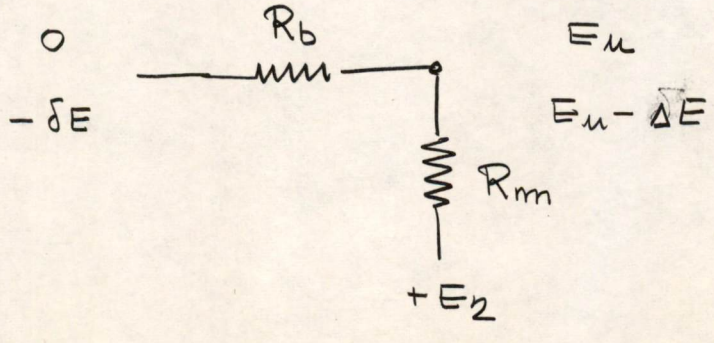
$$I_b'' = \frac{E_u}{R_p}\left[\frac{2\lambda - 1}{\lambda - 1} - 1\right] = \frac{E_u}{R_p}\ \frac{\lambda}{\lambda - 1} \tag{7}$$

This equation represents one constraint on E_u and R_p after I_b'' and λ have been chosen. Eq. (6) gives the constraint on ΔE. If we assume ΔE given a more convenient form of the equations is

$$E_u = \Delta E\ \frac{\lambda - 1}{2 - 1} \tag{8}$$

$$R_p = \frac{\Delta E}{I_b''}\ \frac{\lambda}{2\lambda - 1} \tag{9}$$

We must now introduce R_b,R_m,E_2 and δE as variables instead of R_p,E_u, and ΔE. Consider the resistance divider in the base connections of Q_2



$$\text{let } \rho = \frac{R_b}{R_m + R_b} \tag{10}$$

$$\text{then } \Delta E = (1-\rho)\ \delta E \tag{11}$$

$$\text{and } R_p = \rho R_m \tag{12}$$

$$E_u = E_2 \rho \tag{13}$$

Equations (11),(12), and (13) together with equations give us

$$R_m \frac{\rho}{1-\rho} = \frac{\delta E}{I_b''} \quad \frac{\lambda}{2\lambda - 1} \tag{14}$$

$$E_2 \frac{\rho}{1-\rho} = \delta E \quad \frac{\lambda - 1}{2\lambda - 1} \tag{15}$$

In equations (14) and (15) λ is chosen to give the degree of saturation required by consideration of switching speed, parameter variations, and emitter-collector voltage drop for Q_2.

E and ρ are free to vary within reasonable limits. R_m and E_2 are dependent variables giving circuit values corresponding to the choice of λ , δE, I_b'', and ρ in conformity with the half-way requirement mentioned earlier. Note that

$$R_b = \rho\ (R_m + R_b) = \frac{\rho}{1-\rho} R_m = \frac{\delta E}{I_b''} \quad \frac{\lambda}{2\lambda - 1} \tag{16}$$

In the off-condition Q_2 draws no base current

$$I_b' = 0 \tag{17}$$

we obtain

$$I_e' = \frac{E_2}{R_b + R_m} = (1-\rho) \frac{E_2}{R_m} \tag{18}$$

Using equations (14 and(15)

$$I_e' = (1-\rho)\frac{\lambda-1}{\lambda} I_b'' \tag{19}$$

and

$$I_e'' = I_b'' + \frac{E_2}{R_m} \tag{20}$$

Again using equations (14) and (15)

$$I_e'' = I_b'' \frac{2\lambda-1}{\lambda} \tag{21}$$

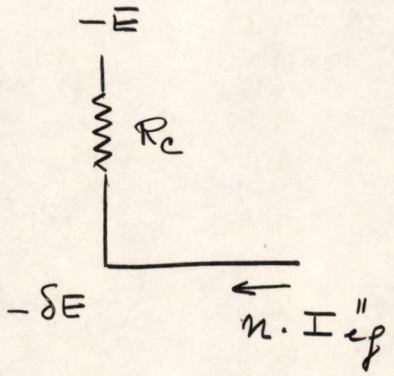
Furthermore

$$I_{ef}' = \frac{\alpha}{\beta} I_e' \tag{22}$$

and

$$I_{ef}'' = \frac{\alpha}{\beta} I_e'' \tag{23}$$

Next consider the inverter collector circuit. It will be assumed that the collector is always fully loaded with emitter followers or an equivalent dummy load. The on-condition corresponds to the following diagram

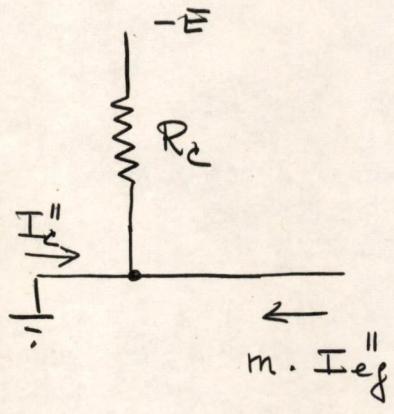


giving

$$- E + n \cdot I_{ef}'' R_c = - \delta E \tag{24}$$

$$R_c = \frac{E - \delta E}{n \cdot I_{ef}''} \tag{24.5}$$

The off-condition corresponds to



giving

$$(nI_{ef}' + I_c'')R_c = E \tag{25}$$

Eliminating R_c between (24) and (25) we obtain

$$I_c'' = n \frac{E}{E - \delta E} I_{ef}'' - I_{ef}' \tag{26}$$

and solving for n

$$n = \frac{I_c''}{\frac{E}{E - \delta E} I_{ef}'' - I_{ef}'} \tag{27}$$

Using equations (23),(22),(21), (20), and (4) we obtain

$$n = \frac{\frac{1}{\alpha}\beta^2}{\frac{E}{E-\delta E}(2\lambda - 1) - (1-\rho)(\lambda - 1)} \tag{28}$$

Now for $E >> \delta E$

$$n = \frac{\frac{1}{\alpha}\beta^2}{\lambda + \rho(\lambda - 1)} \tag{29}$$

and for $\rho = 0$

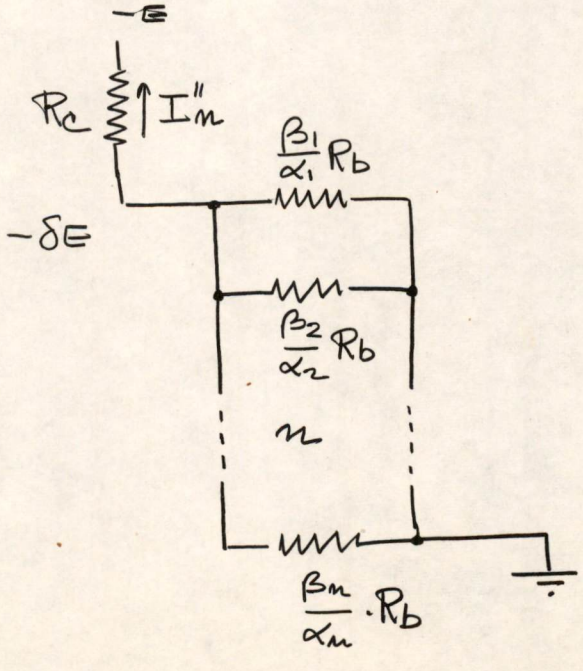
$$n = \frac{1}{\alpha} \cdot \frac{\beta^2}{\lambda} \tag{30}$$

This, of course, is the maximum obtainable.

Tolerance to variations in β:

Next we will determine what happens to the degree of saturation, λ, of Q_2 when the β's are different from the average values assumed in the design. Secondly, what can be done in the design to reduce the effect of variations in β?

Consider the input circuit in the on-condition. (Remember assumptions mentioned at beginning.)



The combined emitter-follower input impedance is z. For simplicity let

$$\gamma = \frac{\alpha}{\beta} \tag{31}$$

$$\frac{1}{z} = \frac{1}{R_b} \sum_{1}^{n} \gamma_i \tag{32}$$

$$I_n'' = \frac{E}{R_c + Z} \tag{33}$$

$$E = I_n'' z = \frac{E \dfrac{R_b}{\sum_{1}^{n} \gamma_i}}{R_c + \dfrac{R_b}{\sum_{1}^{n} \gamma_i}} \tag{34}$$

and

$$I_{ef_1} = \frac{\delta E}{\dfrac{R_b}{\gamma_1}} = \frac{\dfrac{\gamma_1}{\sum_{1}^{n} \gamma_i}}{R_c + \dfrac{R_b}{\sum_{1}^{n} \gamma_i}} \tag{35}$$

How does I_{ef_1} vary when γ_i varies?

$$\frac{\partial I_{ef_1}}{\partial \gamma_i} = \frac{R_c \dfrac{R}{\sum_{1}^{n} \gamma_i} E \dfrac{\gamma 1}{\sum_{1}^{n} \gamma_i} 2 + E \dfrac{\gamma 1}{\sum_{1}^{n} \gamma_i} \dfrac{R_b}{\left(\sum_{1}^{n} \gamma_i\right)^2}}{\left[R_c + \dfrac{R_b}{\sum_{1}^{n} \gamma_i}\right] 2} \tag{36}$$

Assume next that at the point of differentiation

$$\gamma_1 = \gamma_2 = \ldots = \gamma_i = \ldots = \gamma_n \quad \gamma \tag{37}$$

and simplify (36)

$$\frac{\partial I_{ef_1}}{\partial \gamma_i} = \frac{-E R_c \dfrac{1}{n^2 \gamma}}{\left[R_c + \dfrac{R_b}{n\gamma}\right]^2} \tag{38}$$

In the above we assumed that $i \neq 1$. Then from (35) assuming (37)

$$\frac{\partial I_{ef_1}}{\partial \gamma_1} = \frac{\partial I_{ef_1}}{\partial \gamma_i} + \frac{E \frac{1}{n\gamma}}{R_c + \frac{R_b}{n\gamma}} \tag{39}$$

The parameters in equations (38) and (39) obey the relationships derived in the first part of this paper. We can therefore express $\frac{\partial I_{ef_1}}{\partial \gamma_i}$ and $\frac{\partial I_{ef_1}}{\partial \gamma_1}$ in terms of other circuit parameters using these relationships.

For simplicity let us write

$$A = \frac{E R_c \frac{1}{n^2\gamma}}{\left(R_c + \frac{R_b}{n\gamma}\right)^2} \tag{40}$$

$$B = \frac{E \frac{1}{n\gamma}}{R_c + \frac{R_b}{n\gamma}} \tag{41}$$

then

$$\frac{\partial I_{ef_1}}{\partial \gamma_i} = - A \tag{42}$$

and

$$\frac{\partial I_{ef_1}}{\partial \gamma_1} = - A + B \tag{43}$$

A simple consideration shows that

$$\frac{E}{R_c + \frac{R_b}{n\gamma}} = n I''_{ef} \tag{44}$$

Then

$$B = \frac{1}{\gamma} I''_{ef} \tag{45}$$

Similarly

$$\frac{E}{R_c + \frac{R_b}{n\gamma}} \cdot \frac{R_c}{R_c + \frac{R_b}{n\gamma}} = nI''_{ef} \cdot \frac{E - \delta E}{E} \tag{46}$$

Then

$$A = \frac{1}{n\gamma} I''_{ef} \frac{E - \delta E}{E} \tag{47}$$

For simplicity we will consider a systematic simultaneous drift (or deterioration) of all β's (or γ's). Then

$$dI_{ef_1} = d\gamma((n-1)(-A) - A+B) = d\gamma\,(-nA+B) \tag{48}$$

$$dI_{ef_1} = \frac{d\gamma}{\gamma} I''_{ef} \frac{\delta E}{E} \tag{49}$$

However

$$I''_{e_1} = \frac{1}{\gamma} I''_{ef_1} \tag{50}$$

and

$$dI''_{e_1} = \frac{1}{\gamma} dI_{ef_1} - \frac{1}{\gamma^2} I''_{ef}\, d\gamma \tag{51}$$

Then

$$dI''_{e_1} = -\frac{d\gamma}{\gamma^2} I''_{ef} \frac{E - \delta E}{E} \tag{52}$$

Now since the base of Q2 is fixed at 0 volts

$$dI''_b = dI''_{e_1} \tag{53}$$

Furthermore using (23) and (21)

$$dI_b'' = -\frac{d\gamma}{\gamma} \cdot I_b'' \cdot \frac{2\alpha-1}{\alpha} \frac{E-\delta E}{E} \tag{54}$$

However according to (4) for fixed I_c''

$$d\lambda = d\beta \frac{I_b''}{I_c''} + \beta \frac{dI_b''}{I_c''} \tag{55}$$

To distinguish the two β's (α's and γ's) let index 1 refer to Q1 and 2 to Q2 for the moment.

$$d\lambda = \lambda \frac{d\beta_2}{\beta_2} - \frac{d\gamma_1}{\gamma_1} (2\lambda - 1) \frac{E-\delta E}{E} \tag{56}$$

Equation (56) gives the change in the degree of saturation $\lambda = \frac{\beta \text{ act}}{\beta \text{ sat}}$ when β_1 and β_2 vary.

As an approximation we may write

$$\gamma \approx \frac{1}{\beta}$$

$$\frac{d\lambda}{\lambda} \approx \frac{d\beta_2}{\beta_2} + \frac{d\beta_1}{\beta_1} \frac{(2\lambda-1)}{\lambda} \frac{E-\delta E}{E} \tag{57}$$

Conclusion

From (28) it follows that E must be large compared with δE to give a large n. From (57) it follows that $E-\delta E$ must be small compared with δE in order to give good tolerance to variations in the beta of Q1. These requirements conflict. Since n is of the order of magnitude of $\frac{\beta^2}{\lambda} > 100$ a decrease in n can easily be tolerated. The relative variation $\frac{d\lambda}{\lambda}$ in the degree of saturation, is at best $\frac{d\beta_2}{\beta_2}$ which is approximately what would be obtained in a simple inverter (without emitter-follower).

When properly designed the circuit will lead to approximately the same sensitivity to variations in beta in Q2. The large n presumably means that fewer Q2's will be required in a computer, however.

Design Example

Let us assume that Q2 be operated (in saturation) at $I_c'' = 2$ mA $I_b'' = 0.3$ mA. Assume further an average $\beta = 20$, $\alpha = 0.95$, then $\lambda = \frac{20}{\frac{2}{0.3}} = 3$.

In order to reduce the effect of variations in the β of Q1 (see equation 57) $\frac{E - \delta E}{E}$ must be small; choose $E = 3$ v and $\delta E = 2.5$ v. Then from equation 57

$$\frac{d\lambda}{\lambda} = \frac{d\beta_2}{\beta_2} + 0.28 \frac{d\beta_1}{\beta_1}$$

Random variations in Q1 will tend to cancel.

For the design we may use the following four equations setting $\rho = 0$ for simplicity

$$\frac{E_2}{R_m} = I_m = I_b'' \frac{\lambda - 1}{\lambda} \tag{58}$$

derived from (14 and (15).

$$n = \frac{\frac{\beta^2}{\alpha}}{\frac{E}{E - E}(2\lambda - 1) - (\lambda - 1)} \tag{28}$$

$$R_b = \frac{\delta E}{I_b''} \frac{\lambda}{2\lambda - 1} \tag{16}$$

and from (24.5), (23), and (21)

$$R_c = \frac{E - \delta E}{n \frac{\alpha}{\beta} I_b'' \frac{2\lambda - 1}{\lambda}} \tag{59}$$

we obtain

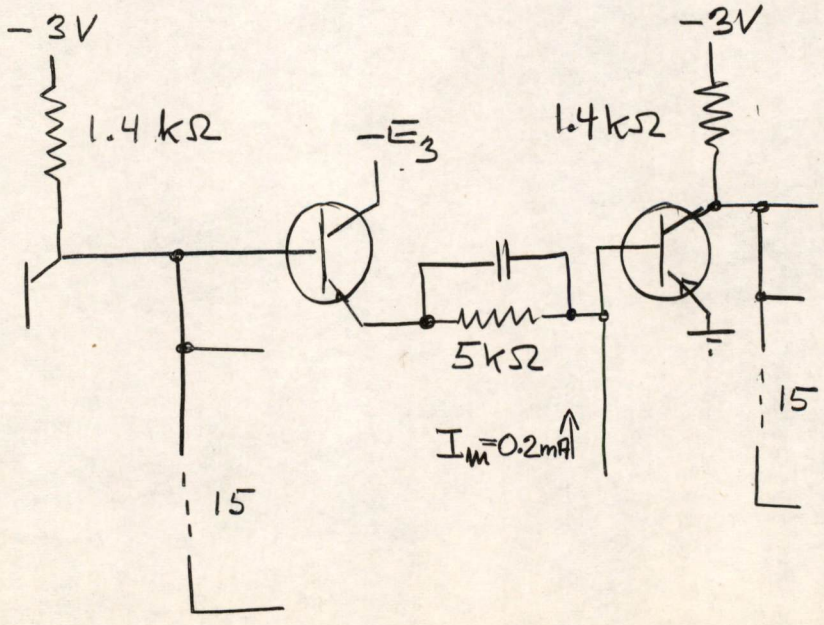
$$I_m = 0.3\,\frac{3-1}{3} = 0.2 \text{ mA}$$

$$n = \frac{\frac{20^2}{0.95}}{\frac{3}{3-2.5}(2.3-1)-(3-1)} = 15$$

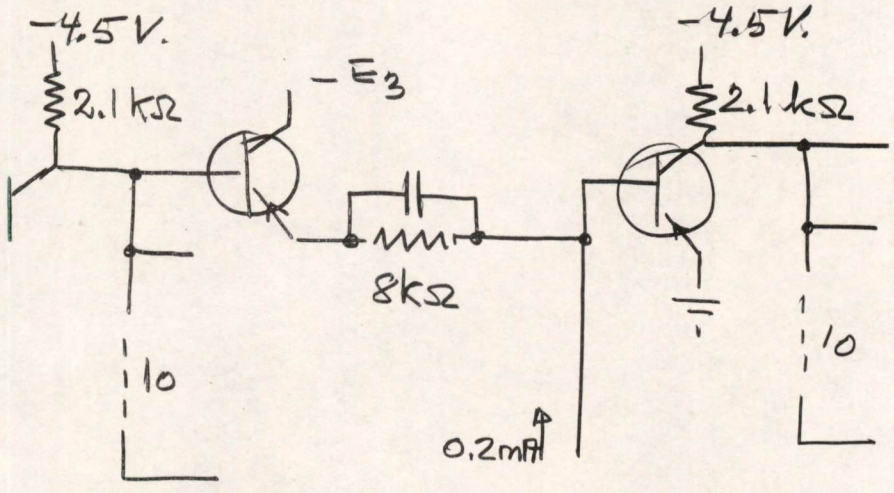
$$R_b = \frac{2.5}{0.3}\,\frac{3}{2.3-1} = 5 \text{ k}\Omega$$

$$R_c = \frac{3-2.5}{15\,\frac{0.95}{20}\,0.3\,\frac{2.3-1}{3}} = 1.4 \text{ k}\Omega$$

The resulting design, shown below, would have to be corrected to take into account the small transistor voltage drops which have been neglected in the above analysis.



A flip-flop capable of driving 14 EFI stages will consist of two of the above stages simply cross connected. Choosing $\rho = 0$, $\lambda = 3$, $I_b'' = 0.3$ mA, $I_c'' = 2$ mA; $\beta = 20$ and $E = 4$v and $E = 4.5$ v the following circuit is obtained



For this circuit

$$\frac{d\lambda}{\lambda} = \frac{d\beta_2}{\beta_2} + \frac{d\beta_1}{\beta_1} \circ 0.18$$

In the final design this circuit would also have to be corrected to take transistor voltage drops into account.

Torben Meisling

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THM/md

K. H. Olsen

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SUBJECT: GEOMETRY OF MAGNETIC MEMORY ELEMENTS

To: Group 63, Staff

From: James D. Childress

Date: January 18, 1956

Approved: John B. Goodenough
John B. Goodenough

Abstract: Two possible memory element geometries -- the thin film and the toroid -- are considered. The calculations show that under certain conditions the thin film geometry may be preferable for use in a very high-speed memory.

J. D. Childress
James D. Childress

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The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Introduction:

The peak current and average power which the memory-plane drivers must deliver can be reduced by decreasing the dimensions of the magnetic memory elements. The following analysis indicates the limits of size reduction and the results which such reductions may yield.

I. Theoretical Ruminations

A. Possible Geometries

The two geometries to be considered and their dimensions are shown in Fig. 1A - Thin Film and Fig. 1B - Toroid.

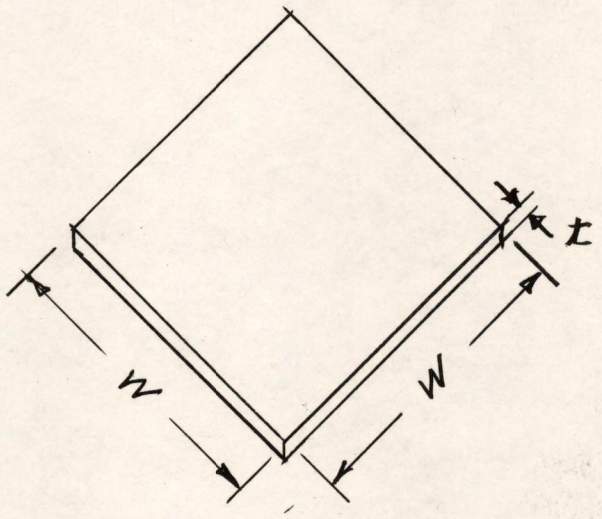

Fig. 1A - Thin Film

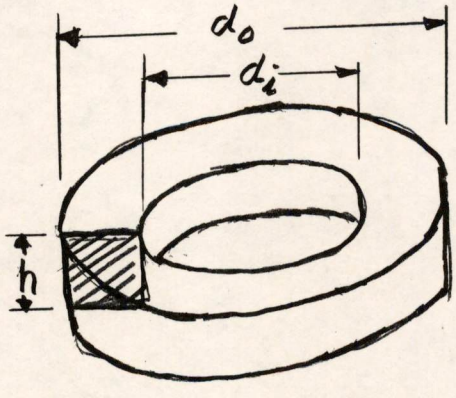

Fig. 1B - Toroid

B. Primary Limits on Geometry

The primary limits on geometry are (1) the peak voltage signal V_p must be great enough to be sensed reliably and (2) the switch time τ_s must be suitable to the desired memory cycle time (certainly less than half the cycle time).

The instantaneous output voltage for a one turn sense winding is

$$v(t) = 10^{-8} A \frac{dB}{dt} .$$

Therefore

$$\int_{-B_r}^{+B_m} dB = \frac{10^{+8}}{A} \int_{o}^{\infty} v(t)dt \approx \frac{1}{2} \times \frac{10^{+8}}{A} \times V_p \tau_s \approx 2B_m,$$

where V_p is in volts, τ_s in seconds, A in square centimeters, and B_m (the maximum induction in the square hysteresis loop) in gauss. We can express the requirement on A in terms of the material parameter B_m and the memory limits V_p and τ_s as

$$A \gtrapprox \frac{1}{4} \times 10^{+8} \frac{V_p \tau_s}{B_m} \qquad (1)$$

C. Cross-Sectional Areas

1. Thin Film

Let $w = C_1 t$, where C_1 is a constant determined by the magnitude of the demagnetizing field tolerable for a square loop; C_1 is in the order of 10^3. The cross-sectional area is thus

$$A = \frac{w^2}{C_1} \qquad (2)$$

2. Toroid

Because about four mutually perpendicular wires of assumed diameter d_w must pass through the toroidal memory element, the inner diameter d_i has a lower limit, $d_i > 2d_w$; also geometry dictates that

the following assumptions be made:

(a) $d_o = C_2 d_i$; $C_2 > 1$

(b) $h = C_3 d_i$; $C_3 > 1$

The area is given as

$$A = C_3 \frac{C_2 - 1}{2} d_i^2 \qquad (3)$$

D. H-I Relationships:

1. Thin Film

In the calculation of the field between two sheets of current, the following approximations are made:

(a) The field inside a rectangular coil of length w centimeters and of N turns is the same as for a similar solenoid.

(b) The current sheets above and below the thin film can be created by overlapping the rectangular coil as shown in Fig. 2.

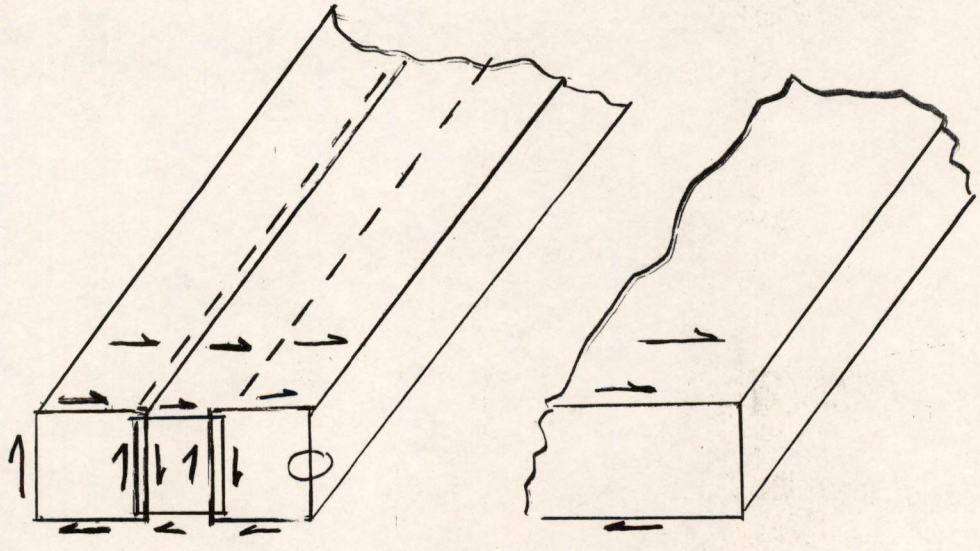

Fig. 2 - Approximation of Current Sheets

From this crude analysis we get

$$H \approx \frac{4\pi N_i}{10w} = \frac{4\pi I}{10w} \tag{4}$$

where I is the total current in amperes flowing in both sheets (split equally between the two) and H is in oersteds.

2. Toroid

The field in a toroid is

$$H \approx \frac{8I}{10(d_o+d_i)} \tag{5}$$

E. Geometry Factor

We define a geometry factor F_g as

$$F_g = \frac{H}{I} . \tag{6}$$

Substituting the cross-sectional area limit of Eq. (1) into Eqs. (2) and (3) and these into Eqs. (4) and (5), respectively, gives

$$F_g(\text{thin film}) \approx \frac{8\pi}{\sqrt{C_1}} \times 10^{-5} \sqrt{\frac{B_m}{V_p \tau_s}} \tag{7}$$

and

$$F_g(\text{toroid}) \quad 8\sqrt{2} \times 10^{-5} \frac{\sqrt{C_3(C_2-1)}}{C_2+1} \sqrt{\frac{B_m}{V_p \tau_s}} \tag{8}$$

F. Order-of-Magnitude Calculations

For purposes of comparison, the geometry factor of the F397 toroid (d_i = 54 mills, d_o = 80 mills, h = 22 mills) is 2.4. We make the following general assumptions for both geometries:

(1) $V_p \approx 10^{-2}$ volt (in present memory $V_p \approx 10^{-1}$ volt)

(2) $\tau_s \approx 10^{-7}$ second (present τ_s is 10^{-6} second).

With these assumptions, we get for thin films

$$F_g(\text{thin film}) \approx 16 \frac{\text{oersted}}{\text{ampere}}$$

where $C_1 = 2 \times 10^3$; $B_m = 8 \times 10^3$ gauss, typical for square loop metals. For a toroid where $C_2 = 1$; $C_3 = 2$; $B_m = 1.5 \times 10^3$ gauss, typical for ferrites,

$$F_g(\text{toroid}) \approx 50 \frac{\text{oersted}}{\text{ampere}}$$

The next section indicates the relative difficulty of obtaining the above geometry factors.

II. Discussions and Conclusions:

The ease of fabrication is one factor governing the practicality of a given memory-element geometry. In the F_g factors above, the thin film would have the dimensions $w = 7 \times 10^{-2}$ cm by $t = 3.5 \times 10^{-5}$ cm; the toroid, $d_i \approx 3 \times 10^{-3}$ cm, $d_o = 6 \times 10^{-3}$ cm, $h = 3 \times 10^{-3}$ cm. The thin film could be made by evaporation techniques with relative ease; but the ultra-small toroid would be almost impossible to make. A toroid a scale magnitude larger would be possible; this gives $F_g \approx 5$. Also it must be remembered that a minimum of three conductors each capable of carrying milliampere currents must pass through the toroid.

Thus fabrication difficulties seem to make the thin film geometry more feasible. Other geometries may offer more than the thin film so that a further study of geometry is worthwhile.

Changing geometry alone is not the answer to the very-fast-memory problem. In the preceding calculations it has been assumed that magnetic materials and memory scheme exist such that a memory cycle time of about 2×10^{-7} second is possible and the $V_p \approx 10^{-2}$ volts can be sensed reliably.

In conclusion, a memory element can be reduced in size (1) yielding an improvement in the peak current-average power requirement of the memory (2) at the expense of the peak signal voltage if and only if

(3) a material and memory scheme exist such that $\tau_s \approx 10^{-7}$ second is possible.

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SUBJECT: HIGH SPEED FLIP-FLOP (MTC MOD. IV)

To: Norman H. Taylor

From: Norman J. Ockene

Date: 12 March 1956

Approved: R. L. Best
R. L. Best

Abstract: This report describes a redesigned high-speed flip-flop which was developed for MTC for the Z2177 (0528) vacuum tube. Some of its advantages over previously existing flip-flops are:

1) faster mode of operation (4mc)
2) decreased upper and lower level delays
3) greater reliability
4) ability to drive larger loads (this characteristic may make it possible to eliminate cathode followers following the high-speed flip-flop in some applications.)

The performance characteristics may be summarized as follows:

1) for set and clear operation (unbalanced load), the flip-flop will drive 300 μμf at a 2 mc rate and will drive light loads (20 μμf) at a 4 mc rate.
2) for set and clear operation (balanced load), the flip-flop will drive 200 μμf at a 1.5 mc rate and will drive all loads less than 100 μμf at a rate of 2 mc or more.
3) for complement operation (unbalanced load), the flip-flop will drive 200 μμf at a 1 mc rate and will drive all loads less than 47 μμf at a rate of 2 mc or more.
4) for complement operation (balanced load), the flip-flop will drive 100 μμf at a 1 mc rate and will drive all loads less than 47 μμf at a rate of 2 mc or more.
5) the upper and lower level delays for set and clear operation (regardless of the amount of loading) is 0.04 and 0.01 μsec respectively.
6) the lower level delay for complement operation (regardless of the amount of loading is 0.04 μsec).
7) the upper level delay for complement operation varies from 0.11 to 0.15 μsec depending on trigger amplitude (but is also independent of the amount of loading).

Also included is a history of the high-speed flip-flop leading up to the design changes. A circuit diagram, layout, and complete set of performance characteristics are also embodied in the report.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

1.0 Background History

This high-speed flip-flop is the result of a study made on existing high-speed vacuum tube flip-flops. It was originally precipitated by a decision made several years ago to eventually replace all 5965 vacuum tubes in computer equipment by a more reliable version called the Z2177. The major change in the Z2177 over the 5965 (besides its superior mechanical construction) is the use of a gold-plated grid structure whereas a silver plating had previously been used. Since gold is more active than silver in the electrochemical series, it produces (in a bogie tube) a contact potential which averages about $\frac{1}{2}$ volt more positive at the grid terminal. The additional bias (small that it may sound) has an extreme deteriorating effect on flip-flop operation. The reason for this is that the conducting tube in a flip-flop is operating approximately at zero bias (actually it is several tenths of a volt positive). As shown in Fig. 1. the operating path of the MTC Mod. IV flip-flop is plotted on the "Average Plate Characteristics" of the Z2177 tube. An "on" tube will be sitting at pt "A" on the operating Path. The average Z2177 tube will then draw somewhat over 8 ma. when conducting according to these characteristics. Fig. 2. shows the same path of operation plotted on the "Average Plate Characteristics" of the 5965 tube. According to these characteristics an "on" tube will also draw somewhat over 8 ma. However, the respective grid biases are 0.25 volt and -0.30 volt. Therefore, the insertion of a Z2177 tube into a given high-speed flip-flop means that there is a bias shift of 0.55 volt. This is essentially the same as inserting a 35 percent "down" 5965 into the flip-flop. A seemingly simple solution is to increase the available plate current either by more positive grid bias or by increasing the plate voltage while keeping the grid bias constant. The circuit is already operating at several tenths of a volt positive. More positive grid bias is highly undesirable because of the complement trigger diode which diverts the grid current around the grid-cathode path effectively shorting the grid to the cathode. This will induce flip-flop failure and is the main reason for not trying to increase the available plate current by making the bias more positive. It is also prudent to avoid excessive grid current which adversely affects tube reliability. The other method suggested of increasing performance is to increase the plate voltage while keeping the grid bias constant. This means using higher supply voltages and consequently higher circuit dissipation. However, this is not a disadvantage per se. The disadvantage lies in the use of the higher value of resistances which increase time constants and in general slows circuit performance such as introducing excessive delays, etc. This is highly undesirable in a high-speed flip-flop. An obvious solution would be to use a "hotter" tube. This was ruled out because the Z2177 has been eminently successful in all its other circuit applications to date and it was thought to be more feasible to adapt the flip-flop to the Z2177 rather than to adopt another tube for use in the flip-flop. In addition, other "bugs" which appeared while using the Z2177 tube in the flip-flop were an increased trigger sensitivity. Most flip-flops actually free-run with only slightly "down" Z2177's in use while bogie Z2177's have a minimum trigger sensitivity of only several volts when used in the flip-flop. This increased circuit sensitivity with the Z2177 is at least partially caused by the decreased

amount of bias available at the grid of the tube which is cut-off.

The use of passive networks in either the grid or cathode circuits of a flip-flop can be used to overcome extreme trigger sensitivity. These circuits generally make use of additional bias (either self or fixed) to increase the negative voltage on the cut-off tube thereby necessitating larger triggers to initiate flip-flop action and also to allow the grid to go positive without the grid shunting effects. Some of these biasing circuits have been used successfuly in previous models of low speed flip-flops. One such arrangement is shown in Fig. A.

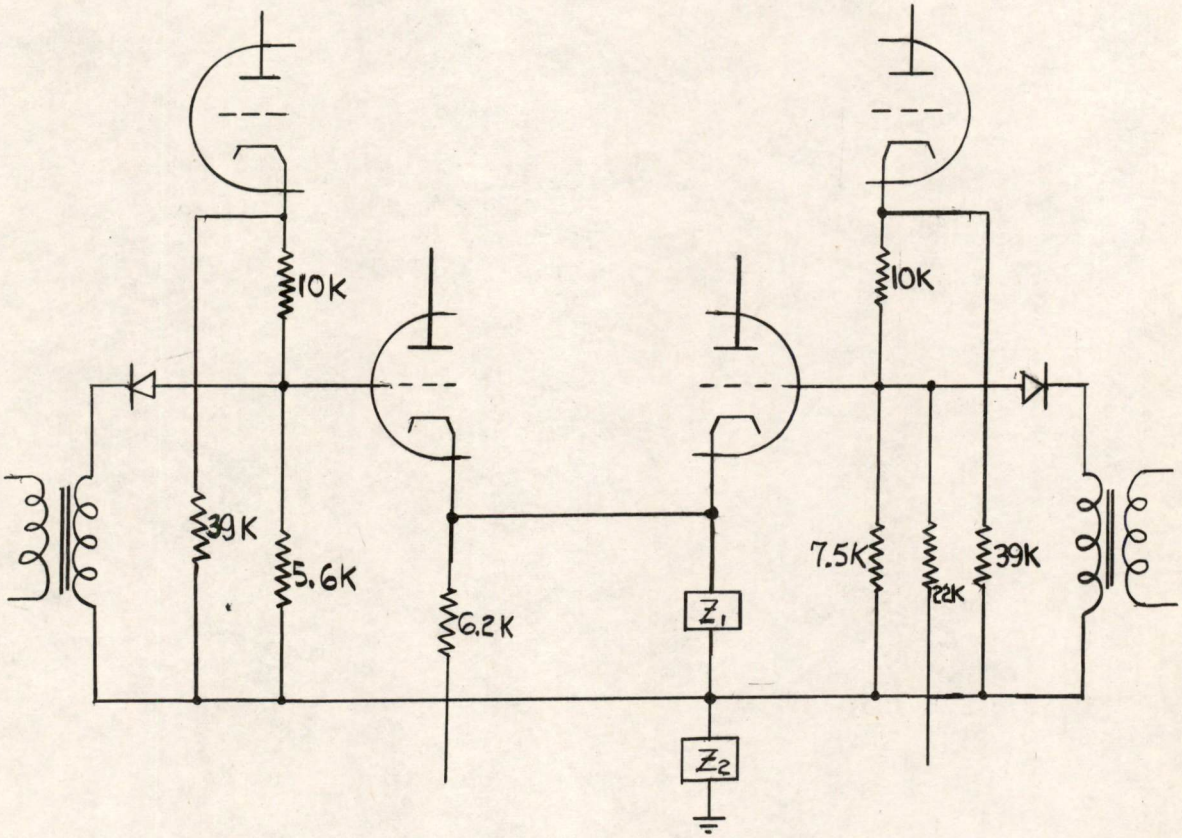

FIG. A

The inherent disadvantage in these circuits is that in order to achieve sufficient biasing action reasonable large values of resistance and/or reactance are necessary (in the order of several thousand ohms). At low repetition rates this magnitude of resistance can be tolerated without adverse effects on performance. However, at high repetition rates, the time constants in the grid or trigger circuits are appreciably affected by the use of these bias networks. This results in PRF sensitivity problems. In addition, the output loading characteristics of a flip-flop are also adversely affected by these networks. The reason for this is that a tube under a given set of operating parameters will supply just so much current. If some of this current is dissipated to develop

bias there is that much less current available for driving the output load. In a given flip-flop this means decreased operating margins.

Another method of overcoming high trigger sensitivity is to attenuate the trigger pulse. However, when trigger sensitivities are so high that the flip-flop free-runs with practically no input pulse, this method is impractical.

The use of silicon diodes as a bias device to decrease trigger sensitivity was also attempted. These units have a forward conduction characteristic which allows approximately $\frac{1}{2}$ volt to be impressed across them before forward conduction occurs. They also have an obvious advantage of not adding any significant additional resistance into the circuit in which they are placed (although their capacitance must be taken into account when used in high frequency applications.) The results obtained by the use of these diodes were very encouraging; however, in order to get sufficient biasing action, five or six diodes had to be added in series.

The seeming dilemma was partially solved by using negative grid clamping as well as previously existent positive grid clamping. As explained later in the report the grid was clamped to a cathode tap which supplies approximately a -9 Volt clamp. In addition, the voltage dividers were redesigned so that the tube will operate with slightly less positive bias. This should mean longer tube life in the circuit. The -30 V diode still provides approximately 2.5 ma of current. This ensures that the -30 V clamp will hold even with a "40% down" Z2177. In addition the elimination of the pulse transformers (for set and clear action) reduces delays to a minimum. The elimination of cathode capacity also aids in keeping delays at a minimum.

Another inovation was the use of positive pulses in triggering the flip-flop. Positive pulses are less sensitive in triggering a flip-flop than are negative pulses. The reason for this is that regenerative action does not occur until the triggered grid has passed cutoff and thus a portion of the input pulse has been used just to raise the level of the grid to cutoff. The remainder of the pulse is amplified in the normal manner and aids in the transition of the flip-flop. This phenomena has been extremely useful in this case because the Z2177 tube as used in flip-flops has been very sensitive to triggers.

Another useful aspect of the redesigned flip-flop is the higher impedance the circuit offers to an incoming pulse (due to the fact that triggering is accomplished on the "off" side). This reduced loading on the input pulse line is especially helpful in computer applications where many flip-flops may be triggered at the same time. The redesigned flip-flop is shown in Fig. 37.

2.0 Waveform Specifications

Fig. 3. shows the output waveform specifications which are met by the new design. Since two distinct methods of triggering the flip-flop are employed, (for complementing and setting and clearing) there are two sets of output specifications given. These characteristics are tied down by means of formulii in which the output loading C is specified by the user. This same data is also shown in Fig. 4 and 5 in which the various parts of the component waveshape are broken down and plotted versus the output loading capacities.

One of the reasons why this flip-flop may be operated as high as four megacycles is that the inherent delays have been materially reduced. For set and clear operation the input pulses are capacitively-coupled eliminating the pulse transformer delay (approximately 0.02 μsec; positive triggering is employed by which method inherently lower values of delay are encounted; the cathode stiffness has been reduced by eliminating all circuit capacitance at the cathode which allows the cathode to follow the grid waveform more readily; and by using negative grid-clamping (as well as the previously - existent positive clamping), allows the memory capacitor to complete its charging in a shorter time. These changes have reduced the upper level delay to approximately 0.04 μsec and the lower level delay to 0.01 μsec for set and clear operation. Other advantages gained are that both upper and lower level delays are independent of capacitive loading and the upper level delay is independent of trigger amplitude changes.

For complement operation, due to triggering difficulties, transformer-coupled negative-pulse triggering was retained. However, the upper level delay was kept independent of changes in capacitive loading by the previously-mentioned method of grid clamping. In addition, the upper level delay was made independent of capacitive loading by the elimination of cathode capacity. These changes produced an upper level delay of approximately 0.13 μsec and a lower level delay of 0.04 μsec. Actually there is an advantage to an increased delay for complement operation. In counting applications of the flip-flop, the outputs are sensed during the triggering operation; therefore, it is desirable that the outputs remain at their original levels until after the trigger has passed (0.1 μsec). The negative grid clamp has been instrumental in reducing the changes in upper level delay with trigger amplitude from 0.1 μsec at 10 V trigger to 0.15 μs at 40 V trigger (Fig. 6).

3.0 PRF Response Characteristics (vs Pulse Width)

Fig. 7. shows the effect of various pulse widths on the ability of the flip-flop to complement at a given pulse repetition frequency. The curves are shown only for complement operation since set and clear operation produces the same effects. The ability of a pulse to successfully trigger a flip-flop is dependent upon the energy content of the pulse or the area defined by the pulse. For example, a square pulse of unity amplitude has approximately 37% more energy content than a half sine wave pulse of same maximum amplitude. This means that the square

pulse would be 37% more effective in triggering a flip-flop. For this reason, in all tests performed in this report the sine wave shape was adhered to as closely as possible.

4.0 PRF Response Characteristics (vs Load)

Fig. 8 and 9 show the effects of placing capacitive load on the output. As seen in the characteristics the effect of a given capacitance on performance depends upon the mode of operation desired, either complement or set and clear, with load either unbalanced or balanced. These characteristics are necessary in order to set up a criteria of operation limitations for the flip-flop. In all cases the pulse width is 0.1 μs. A rather unusual aspect of the set and clear unbalanced load characteristics is that for PRF's up to 2 mc the flip-flop sensitivity is independent of loading. However, if this mode of operation is to be selected, attention must also be given to rise and fall times and margins (as is true in all cases).

5.0 Capacitive Load Characteristics

One of the basic criteria in determining the maximum capacitive load which can be driven is the transition time of the flip-flop. The transition time will determine whether or not the proper levels will be reached for a given PRF. The levels, in turn will be determined by whether gate-tubes or both gate-tubes and diode-logic are to be driven. This dictates a lower level of either -15 V or -30 V respectively. It is interesting to note that the transition time (to -30 V) is always $\geqslant$ the transition time (to +10 V). However, this is not true for the (fall) transition time (to -15 V) which can be either greater than or less than the transition time (to +10 V). Therefore, when driving gate-tubes either the (fall) transition time (to -15 V) or the transition time (to +10 V) may be the limiting value. When driving both gate-tubes and diode-logic the transition time (to -30 V) is always the limiting value.

In order to simplify the selection of maximum load capacity for a given mode of operation, a group of curves was complied called "Limits Of Capacitive Loading For Various Modes Of Operation". These curves are shown in Fig. 10. In compiling these curves, the only criteria considered was that of pulse sensitivity and margins. In a given application, after one has consulted these curves, the next step is to check the "Capacitance Load Characteristics" (Fig. 8 and 9) to see if the desired load is compatible with the transition time to obtain the desired levels.

6.0 Resistive Load Characteristics

The amount of "and" current (the resistive current drawn from the flip-flop when the output is down) which can be taken, is determined by the maximum transition time, the lower voltage level, and the margins on the same side as the "and" gate. The circuit will supply adequate

levels at sufficient margins up to approximately 10 ma of resistive load current (with no capacitive load). Using the curves already included for capacitive loading, the new transition time may be computed if the external resistive load is known.

It should be noted that whenever a resistive load is drawn from the flip-flop the output impedance of the cathode follower must be changed. This must be done in order to insure that when the output is up, the cathode follower will draw the same amount of current it had been drawing without load. This can be done either internally (by changing the 30K resistor) or externally (by adding a resistance to the output returned either to the -150 V or +150 V sources).

7.0 Grid Clamp Return Characteristics

The most significant improvement in this flip-flop was the direct result of the negative clamping circuit at each flip-flop grid. Previously, the grid, upon switching from conduction to non-conduction went through a level change of 40 volts times the DC attenuation ratio. This was equivalent to 14.3 volts. From the Z2177 characteristic curves it is seen that the tube requires only about -3 volts to cut it off as compared to the theoretical cutoff value $\frac{e_b}{\mu_o}$ or for this case $\frac{110}{20} = -5.5$ volts. The lowest cutoff μ (μ_o) for a Z2177 tube is 20, at 0.15 ma plate current. The μ that is important in this circuit is at a plate current of 2.5 ma. With these specifications in mind a series of tests were run by complementing the flip-flop at various pulse repetition frequencies while different tap points on the cathode resistor were selected. These curves are shown in Fig. 11 as PRF curves for various values of "a" (where "a" is the ratio of the resistance from cathode-to-tap to the entire cathode resistance). The curves show that the only difference in the selection of tap points (as far as the PRF characteristics are concerned) is the trigger sensitivity. This would tend to indicate a value of "a" between 0.15 and 0.20. The selection was further narrowed down by the availability of RMA values of resistance to an "a" of 0.173. As seen in the circuit schematic this ratio is produced by using 1100 and 5100 ohm resistances. This ratio produces a negative clamp voltage of approximately 9.1 volts. This value of clamp voltage appears to limit the negative grid overshoot to a minimum and at the same time has a margin of safety over tubes with the most remote cutoff (-5.5V). These results were further substantiated by the running of margins.

The use of this clamp circuit does not materially affect the stability factor of the flip-flop as the stability factor is determined mainly by the DC divider network.

8.0 DC Divider Network And Tube Margins

As a result of many performance tests made on the high-speed flip-flop using Z2177 tubes in all states (from 40% down to 20% high) it was felt that improved reliability and performance would be obtained by

reducing the ratio of the divider network somewhat. These circuit changes are shown in Fig. 37. The effects produced by these circuit changes are plotted in Fig. 12 and 12 as tube margins for both old and new divider networks.

All tests in this report were run with the old divider network (Fig. A) because several resistors in the old divider network of the MTC Mod. II flip-flop were not very accessible. However, it is suggested that all future models of the high-speed flip-flop should be constructed with the new divider network. (Fig. 39).

9.0 Marginal Checking

The circuit margins are shown for the four modes of operation (set and clear, unbalanced and balanced, complement, unbalanced and balanced) in Fig. 14 through 17. As memtioned previously in the report all curves were obtained with the old divider network. The new divider network will produce margins which are approximately 40% greater than the old divider network. This is caused by the greater attenuation ratio of the marginal checking voltage prior to the grid. However, in spite of this difference both circuits will perform in similar fashion. The curves of complement margins (unbalanced load) are shown both at 2KC and 2MC trigger PRF. However, since for this case the high frequency margins closely follow the low frequency margins only the no-load high frequency curve is shown. The curves for set and clear margins both unbalanced and balanced loads should be taken only at low PRF's since for the high frequency case the margins are extremely large. This is seen in Fig. 15.

10.0 Tolerances

Since flip-flops are by nature symmetrical circuits, they require close matching components in places where the components can effect the performance adversely. Such a place, for instance, is in the grid divider circuit where "off-center" tolerances effect the grid bias and consequently the loop gain. The plate circuit is also sensitive to deterioration of performance due to tolerances. Fig. 18 shows the effect of changes in plate tolerance voltage upon flip-flop margins. In Fig. B is shown the circuit which was used to obtain the curves.

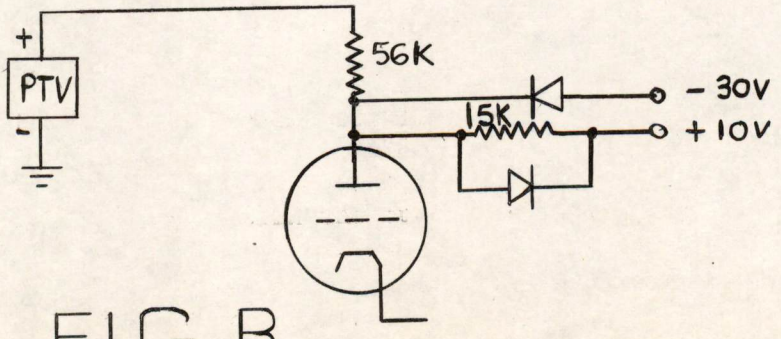

FIG. B

The PTV (Plate Tolerance Voltage) is a useful concept in analyzing the effects upon performance of all tolerances involved in the plate circuit. These tolerances were then used to compute the maximum tolerance excursions permissible for both the 56K and the 15K plate resistors. The diode back resistances were neglected in the computations which follow: The open circuit voltage at the flip-flop plate with a PTV of 250 V is

$$\frac{15}{71} \quad (250 \; - \; 10) \; + 10 = 60.8 \text{ V.}$$

The Thevenin impedance which the flip-flop plate sees is 15K in parallel with 56K or 11.8K. The amount of (56K) resistance tolerance (T) which will produce the above plate voltage and the same Thevenin impedance is:

$$\left[\begin{array}{l} \dfrac{56\,(1+T) \quad (11.8)}{56\,(1+T) \quad -11.8} \\ \\ \dfrac{56\,(1+T) \quad (11.8)}{56\,(1+T) \quad +56\,(1+T) \quad -11.8} \end{array} \right] \quad (250 - 10) \; + \; 10 = 60.8$$

Where: $T = +0.715$ or $+71.5\%$

However, since the Thevenin impedance was 11.8K the 15K resistor must be 13.4K when the 56K resistor was 96.0K (+71.5%)

In a similar fashion the minimum tolerance of the 15K resistor was found to be -13.4%. The tolerance of the 56K plate resistor at the same time is 127%.

Fig. 19 shows the effects on margins of lowered back resistance on the grid trigger diode. (CR5 or CR6.)

11.0 Performance Photographs

Fig. 20 through 36 show typical performance characteristics in photographs. Fig. 20 through 24 show the internal effects due to pulse trains. This particular method of testing flip-flops is extremely useful since the high and low frequency performance characteristics as well as any DC level changes are immediately evident. As can be seen by the above mentioned sequence of photographs no part of the flip-flop is adversely PRF sensitive nor is there any significant level changes at any circuit point which would indicate future trouble. Fig. 29 and 30 show the effects of the clamping circuit in preventing set pulses from affecting the clear side of the flip-flop and clear pulses from affecting the set side of the flip-flop. Fig. 29 was taken at a set and clear PRF of 2 mc while Fig. 30 was taken at 1 mc. The small feed-through to the opposite side at 1 mc operation will not in any way affect the performance of the flip-flop. Fig. 31. and 32. show the critical pulse which is necessary to clear the flip-flop after a relatively long pulse train. For the case shown (2 MC PRF) the critical pulse amplitude is 12 V as seen in Fig. 31. The remaining photographs (Fig. 33 through 36) are self-explanatory as they show the flip-flop under various modes of operation for both input conditions and output loading.

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Attachments:

Fig. 1 - A65390
Fig. 2 - A65391
Fig. 3 - A65337
Fig. 4 - A65347
Fig. 5 - A65339
Fig. 6 - A65338
Fig. 7 - B65342
Fig. 8 - B65340
Fig. 9 - B65341
Fig. 10 - A65349
Fig. 11 - A65351
Fig. 12 - A65350
Fig. 13 - A65352
Fig. 14 - A65346
Fig. 15 - A65345
Fig. 16 - A65344
Fig. 17 - A65348
Fig. 18 - A65343
Fig. 19 - A65135
Fig. 20 through Fig. 24 - A65333
Fig. 25 through Fig. 28 - A65334
Fig. 29 through Fig. 32 - A65336
Fig. 33 through Fig. 36 - A65335
Fig. 37 - C63287
Fig. 38 - C65137

Distribution List:

*Best, R. L.
*Ziegler, H. L.
*Gates, E. K.
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*Hofler, J. (" ")
*Mansfield, H. (" ")
*Jahn, R. C.
*Callahan, R. J.
*Barrett, B. W.
*Flanagan, M. J.
*Hingston, A.
*McCusker, J. H.
*Paddock, R.
*Boyd, H. W.

All Division 6 Group Leaders
Group 62 and 64 Staff Members not listed above.

*Indicates recipient of complete Memorandum.

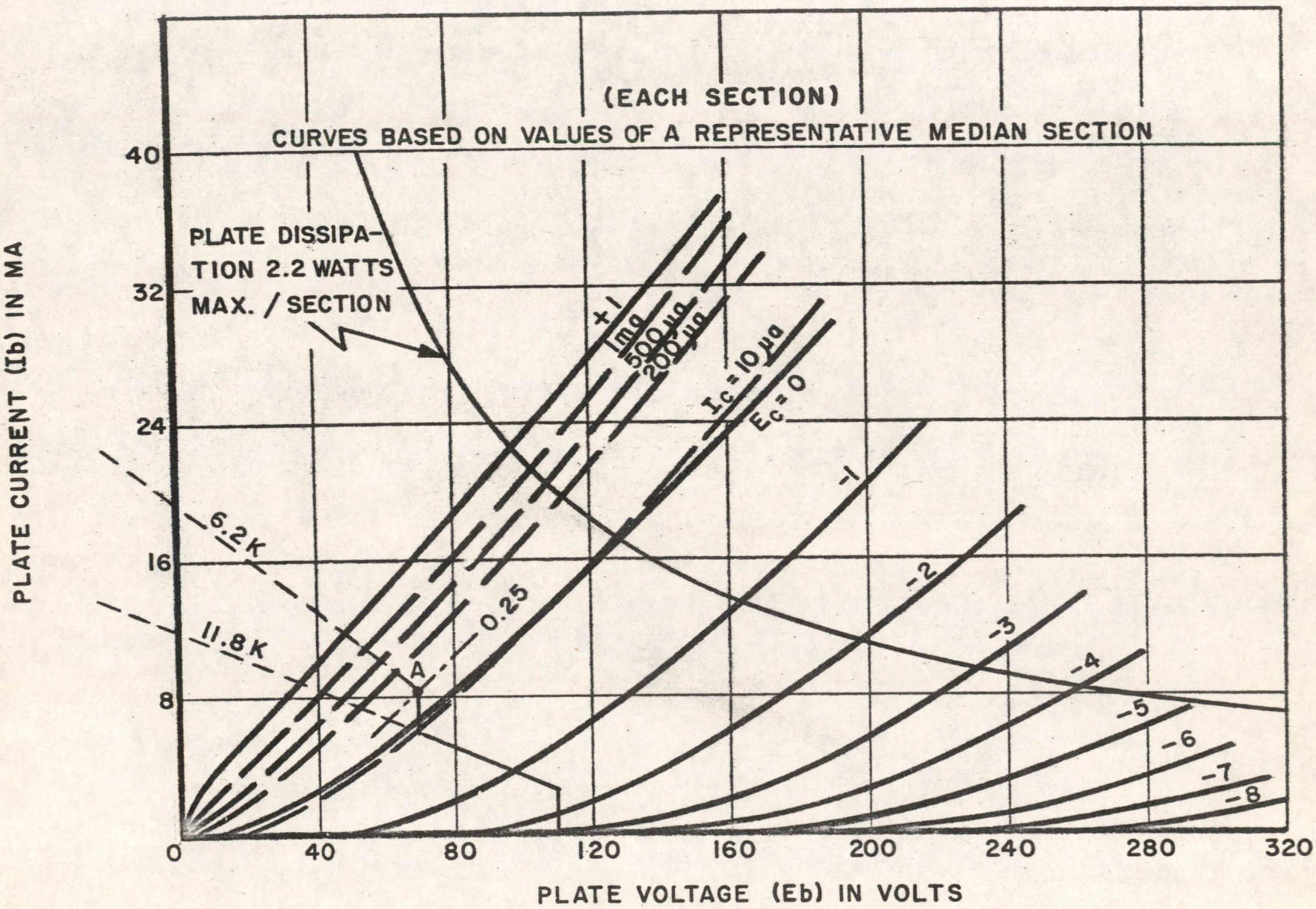


FIG. 1

FLIP-FLOP PATH OF OPERATION PLOTTED ON AVERAGE PLATE CHARACTERISTICS, Z-2177

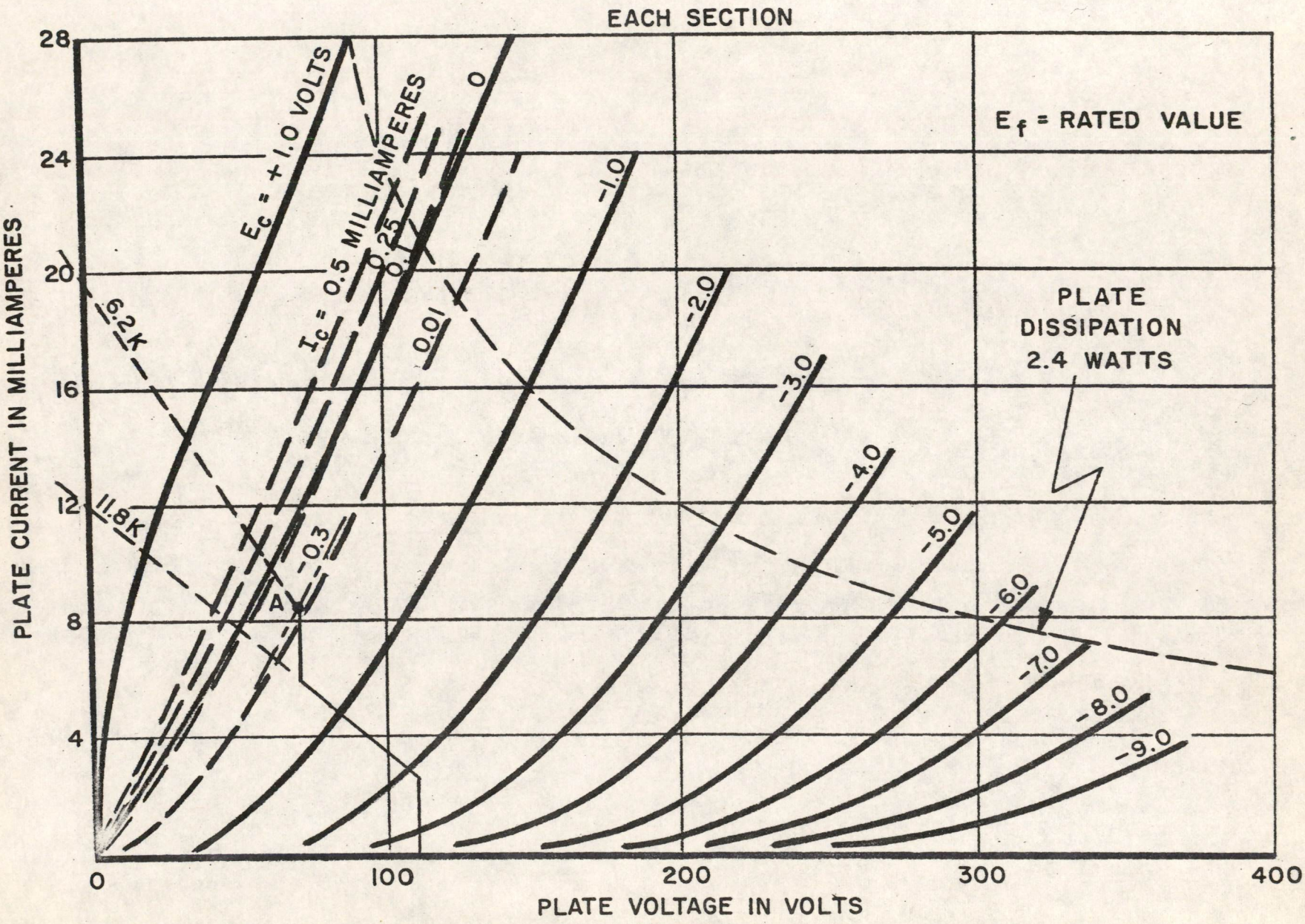
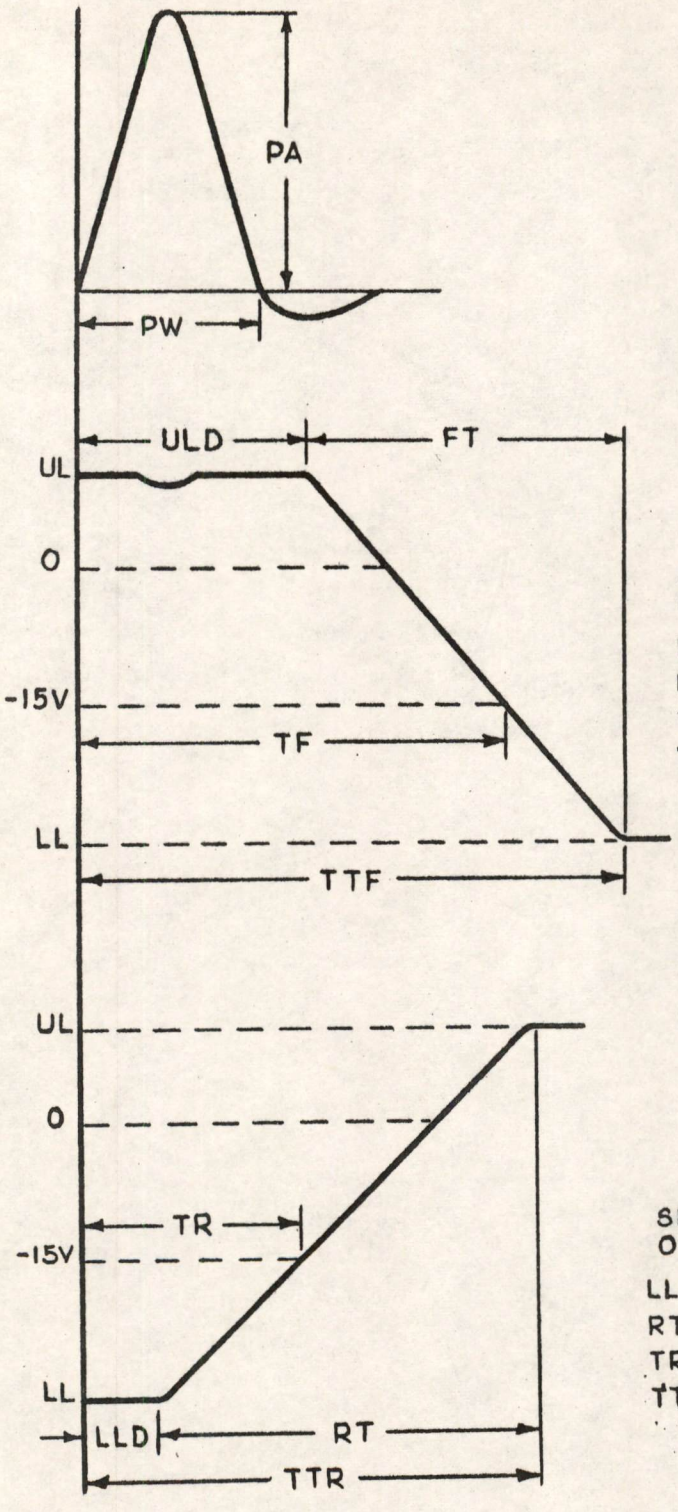


FIG. 2

FLIP-FLOP PATH OF OPERATION PLOTTED ON AVERAGE PLATE CHARACTERISTICS, 5965



PA = PULSE AMPLITUDE
PW = PULSE WIDTH

$20V \leq PA \leq 40V$
$0.08\,\mu SEC. \leq PW \leq 0.12\,\mu SEC.$

UL = UPPER LEVEL
ULD = UPPER LEVEL DELAY
FT = FALL TIME
TF = TRANSITION TIME (FALL) TO -15V
TTF = TRANSITION TIME TO LOWER LEVEL

SET AND CLEAR OPERATION:	COMPLEMENT OPERATION:
ULD ≈ 0.04 μSEC.	ULD ≈ 0.13 μSEC.
FT = 0.20 + 0.00365C	FT = 0.23 + 0.00365C
TF = 0.12 + 0.00215C	TF = 0.24 + 0.00215C
TTF = 0.24 + 0.00365C	TTF = 0.36 + 0.00365C

WHERE: C IS IN MMFD
TIMES ARE IN μSEC.

LL = LOWER LEVEL
LLD = LOWER LEVEL DELAY
RT = RISE TIME
TR = TRANSITION TIME (RISE) TO -15V
TTR = TRANSITION TIME TO UPPER LEVEL

SET AND CLEAR OPERATION:	COMPLEMENT OPERATION:
LLD ≈ 0.01 μSEC.	LLD ≈ 0.04 μSEC.
RT = 0.23 + 0.0009C	RT = 0.21 + 0.0008C
TR = 0.09 + 0.0002C	TR = 0.24 + 0.0021C
TTR = 0.24 + 0.0009C	TTR = 0.25 + 0.0008C

WHERE: C IS IN MMFD
TIMES ARE IN μSEC.

FIG. 3

WAVEFORM SPECIFICATIONS

A-65337

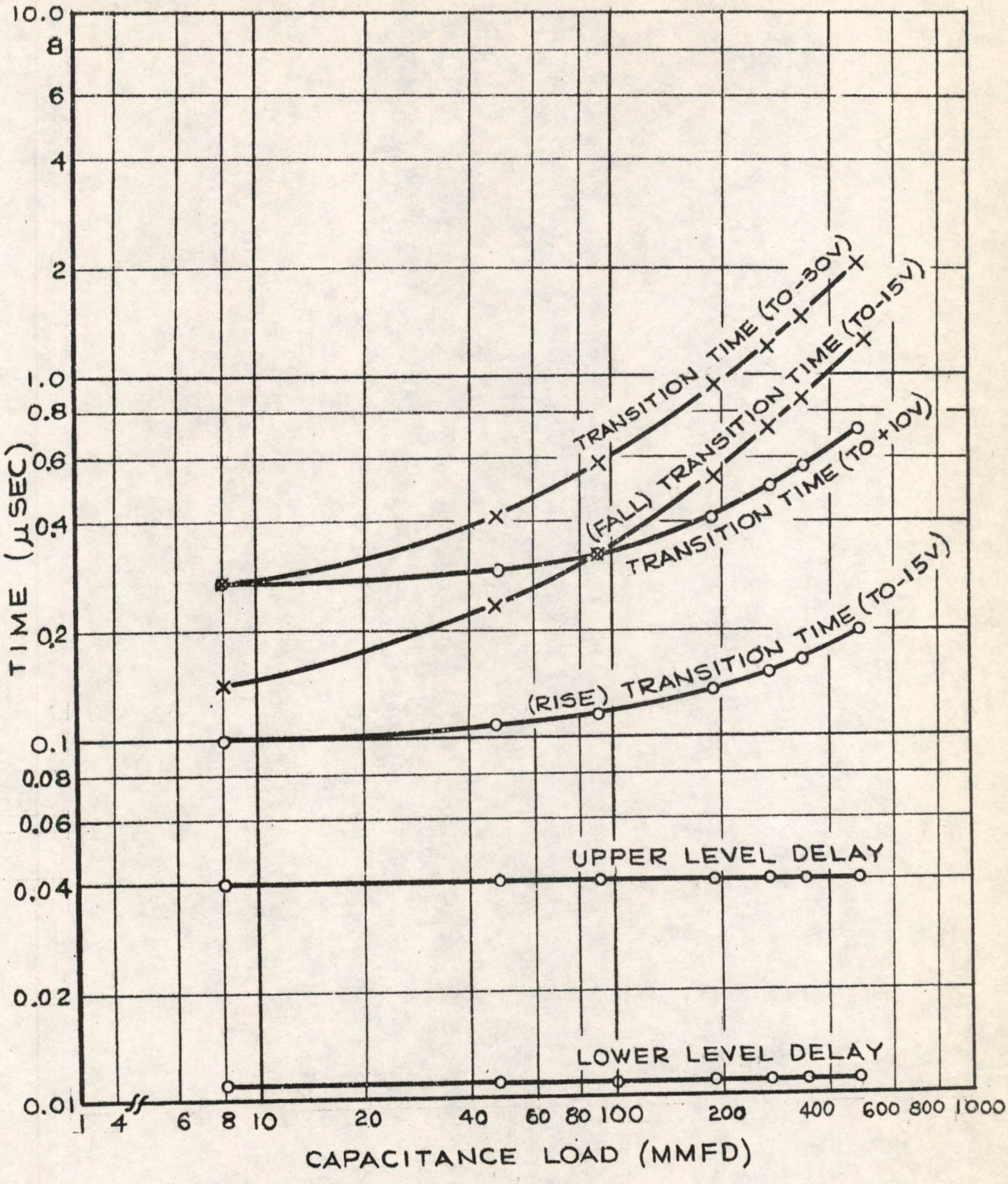


FIG. 4

CAPACITIVE LOAD CHARACTERISTICS
FOR SET AND CLEAR OPERATION

A-65347

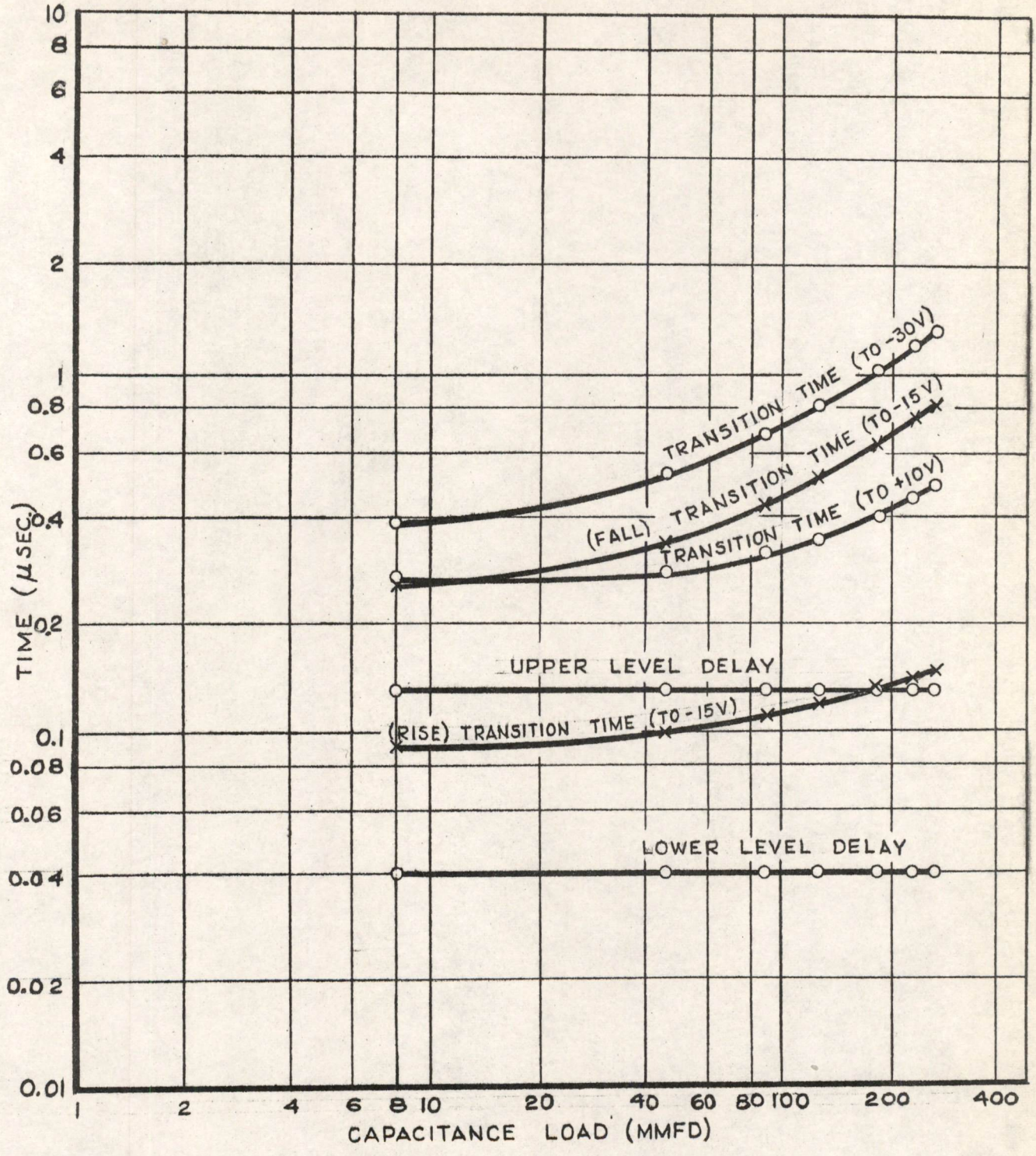


FIG. 5

CAPACITANCE LOAD CHARACTERISTICS FOR COMPLEMENT OPERATION

A-65339

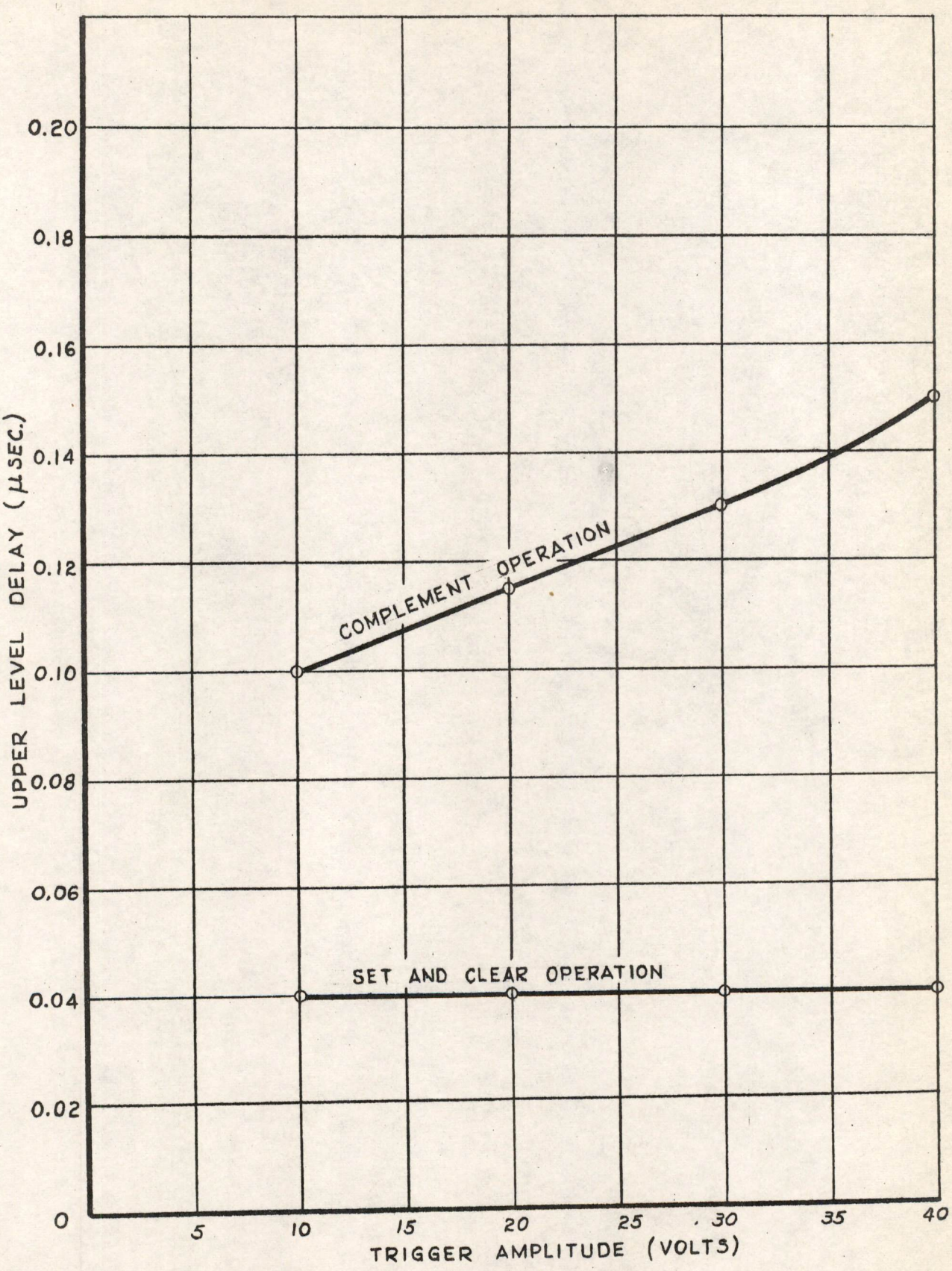


FIG. 6

EFFECTS OF TRIGGER AMPLITUDE ON UPPER LEVEL DELAY

A-65338

B-65342

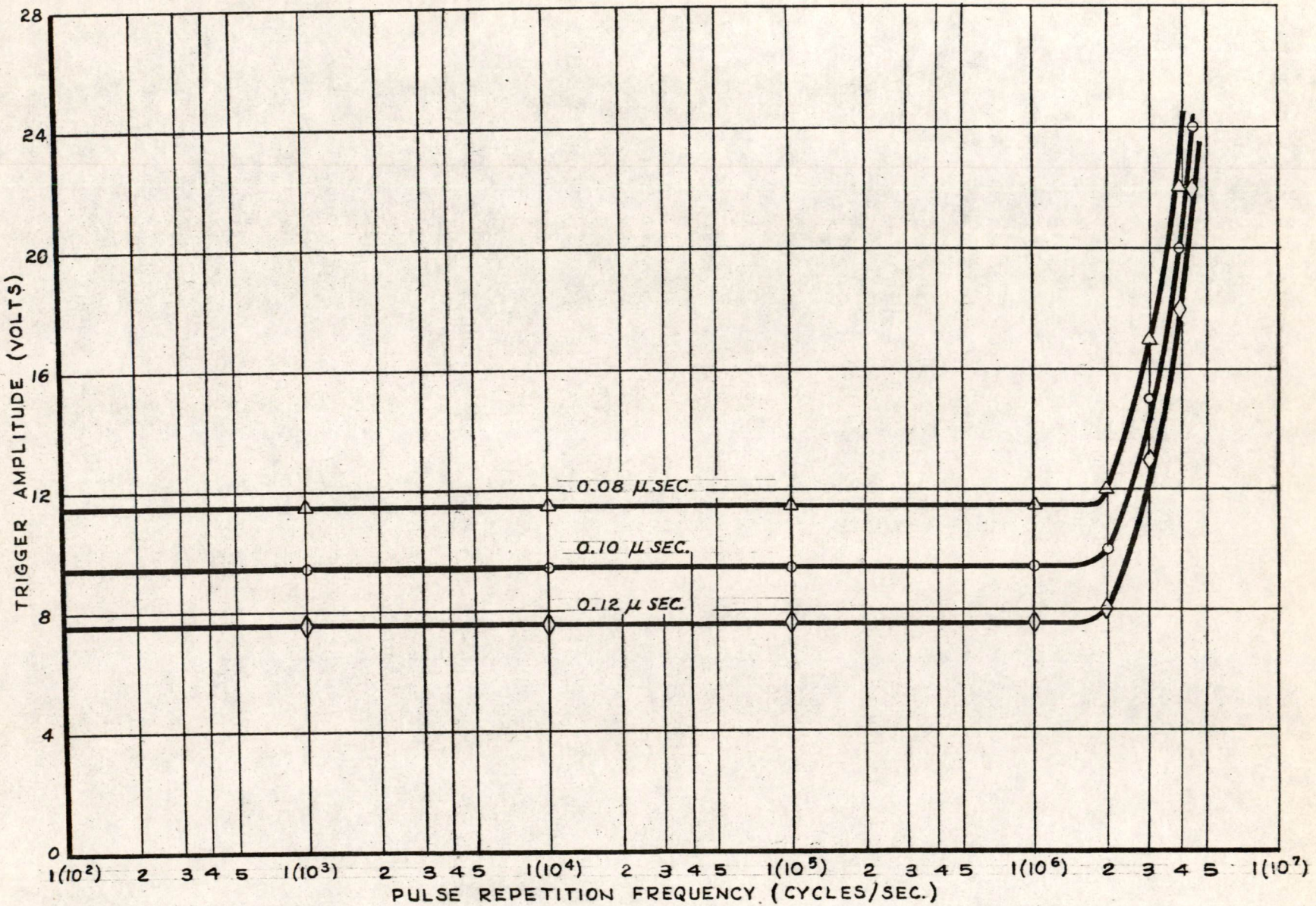


FIG. 7

COMPLEMENT PULSE REPETITION FREQUENCY PULSE WIDTH CHARACTERISTICS

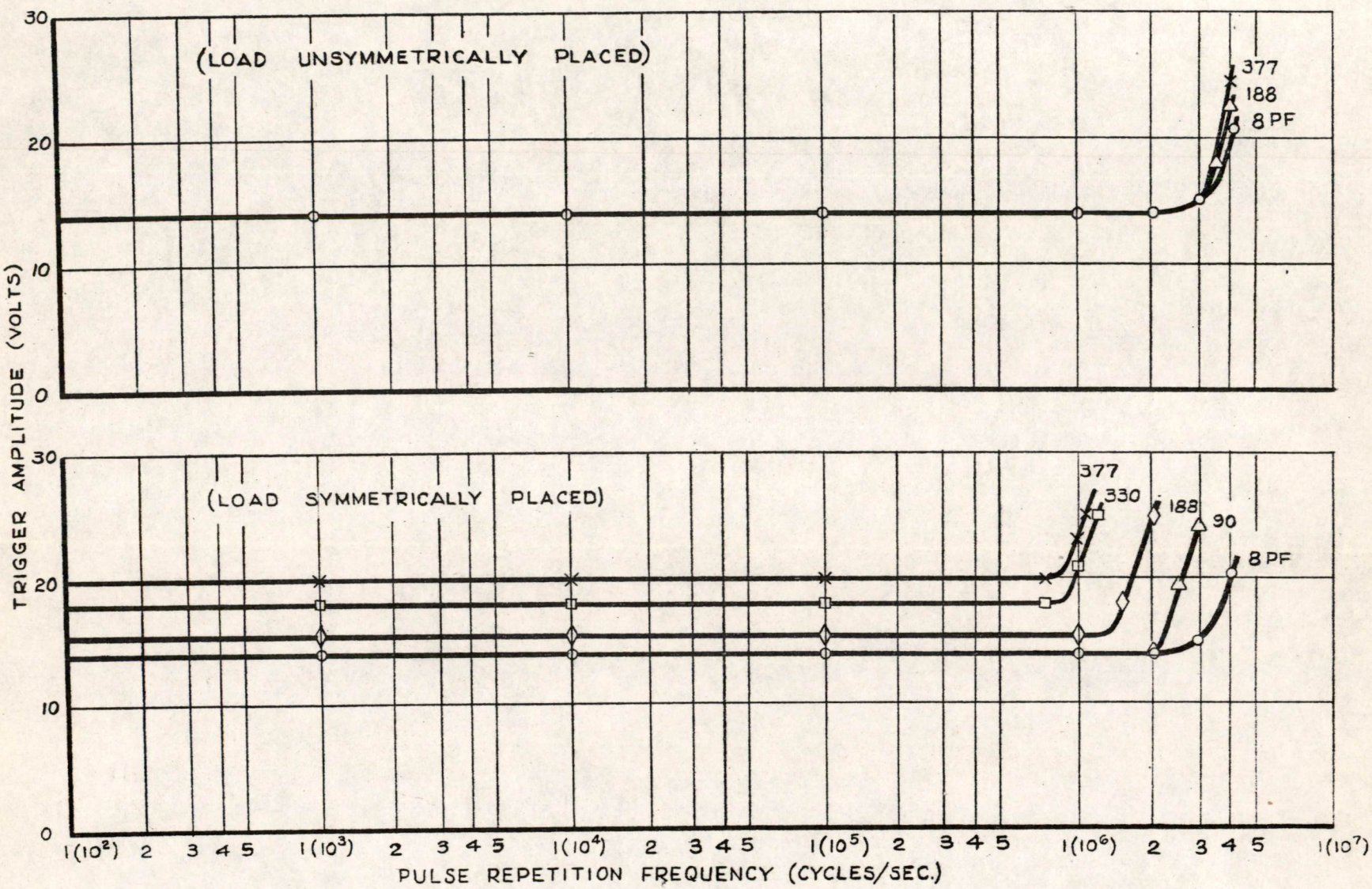


FIG. 8

SET AND CLEAR PULSE REPETITION FREQUENCY CHARACTERISTICS

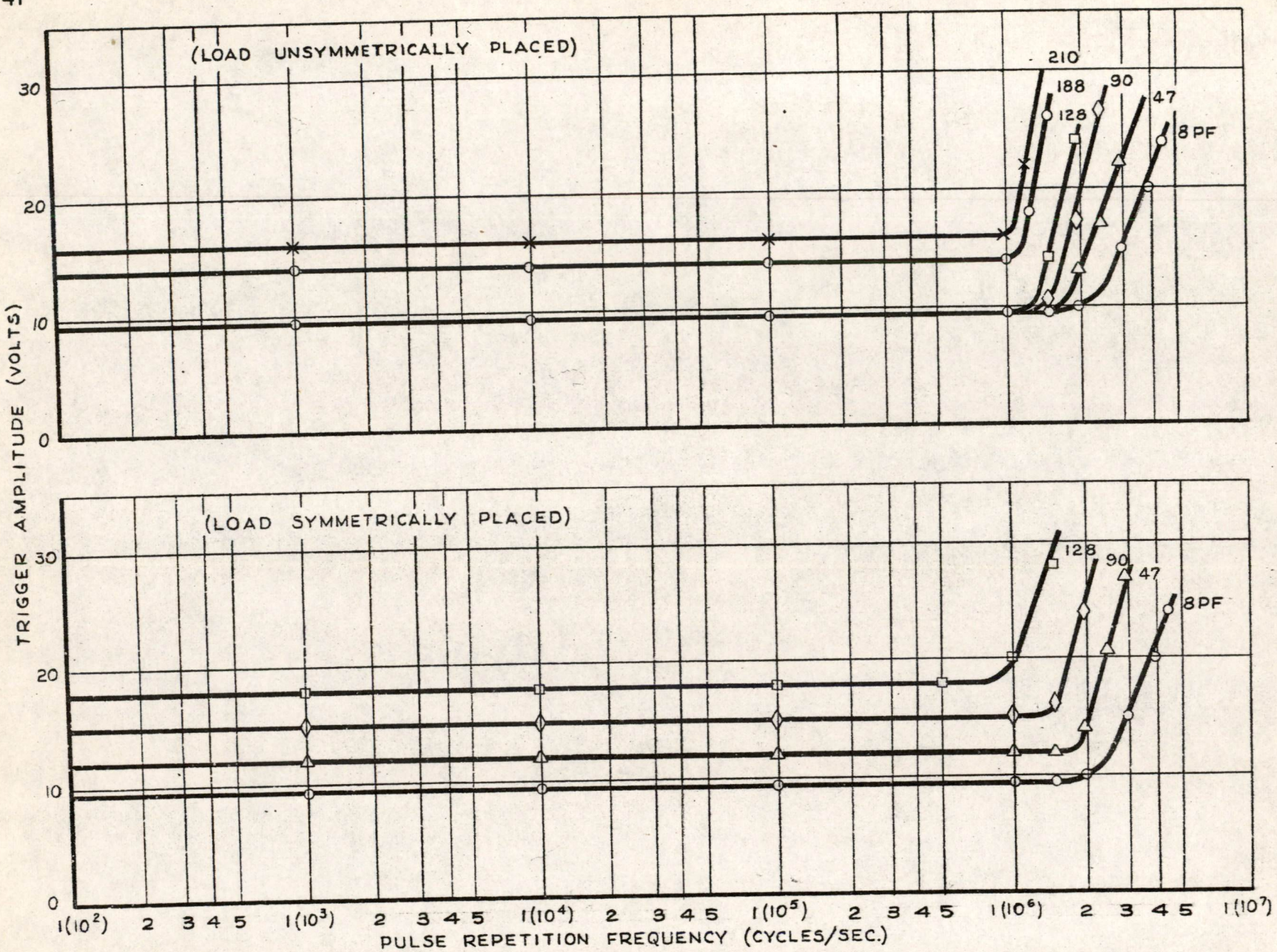


FIG. 9

COMPLEMENT PULSE REPETITION FREQUENCY CHARACTERISTICS

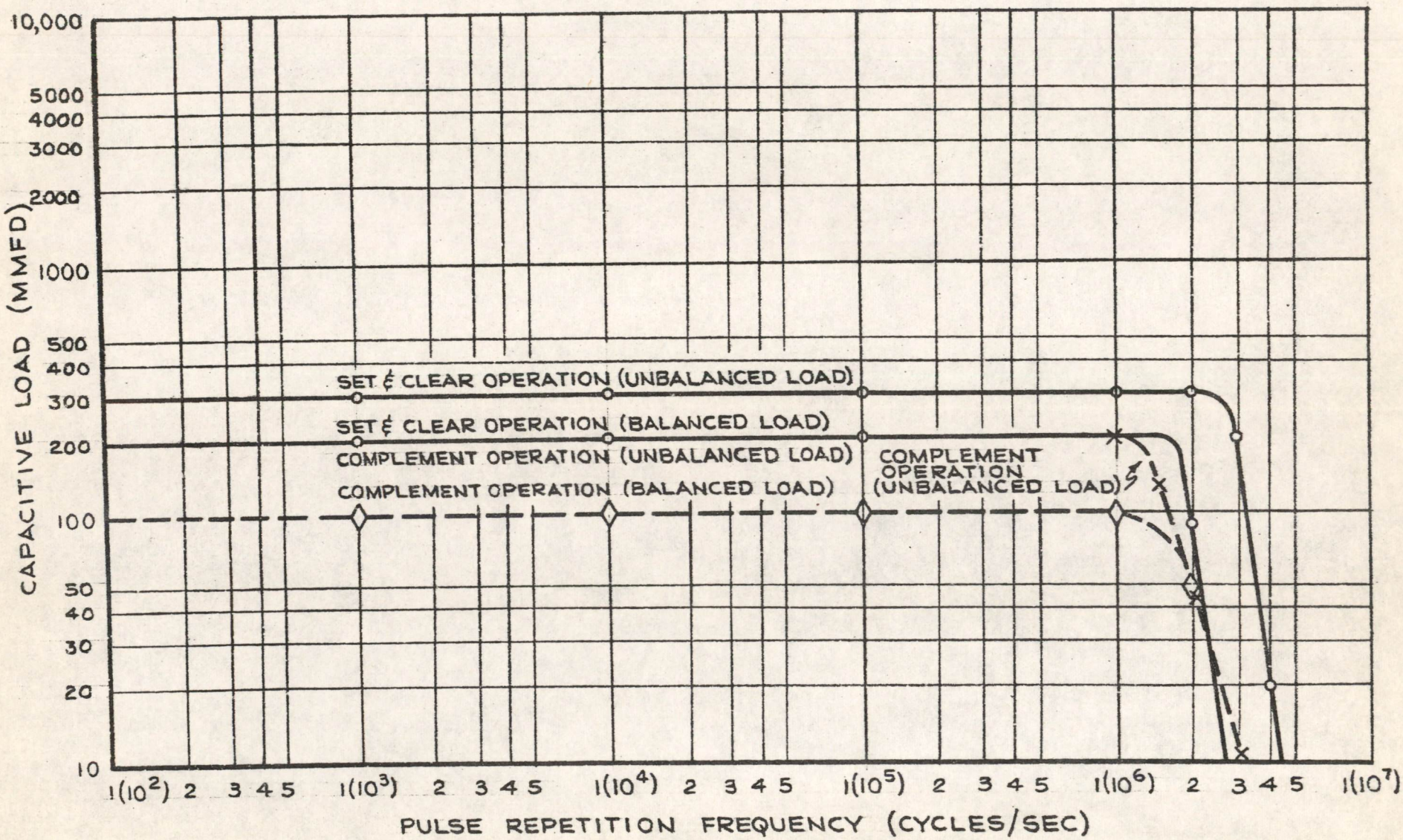


FIG. 10

LIMITS OF CAPACITIVE LOADING FOR VARIOUS MODES OF OPERATION

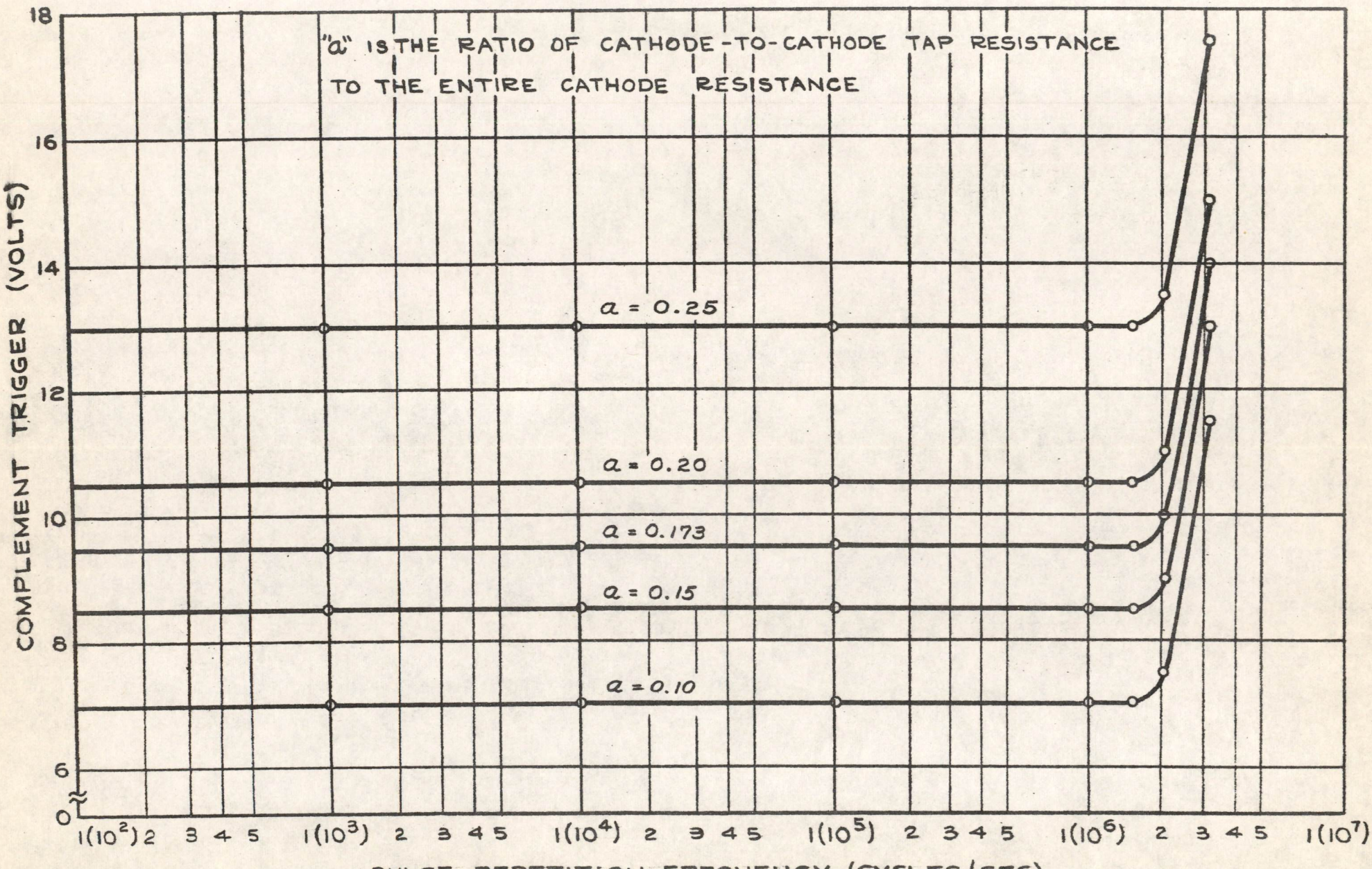


FIG. 11

PULSE REPETITION FREQUENCY CHARACTERISTIC vs. "a"

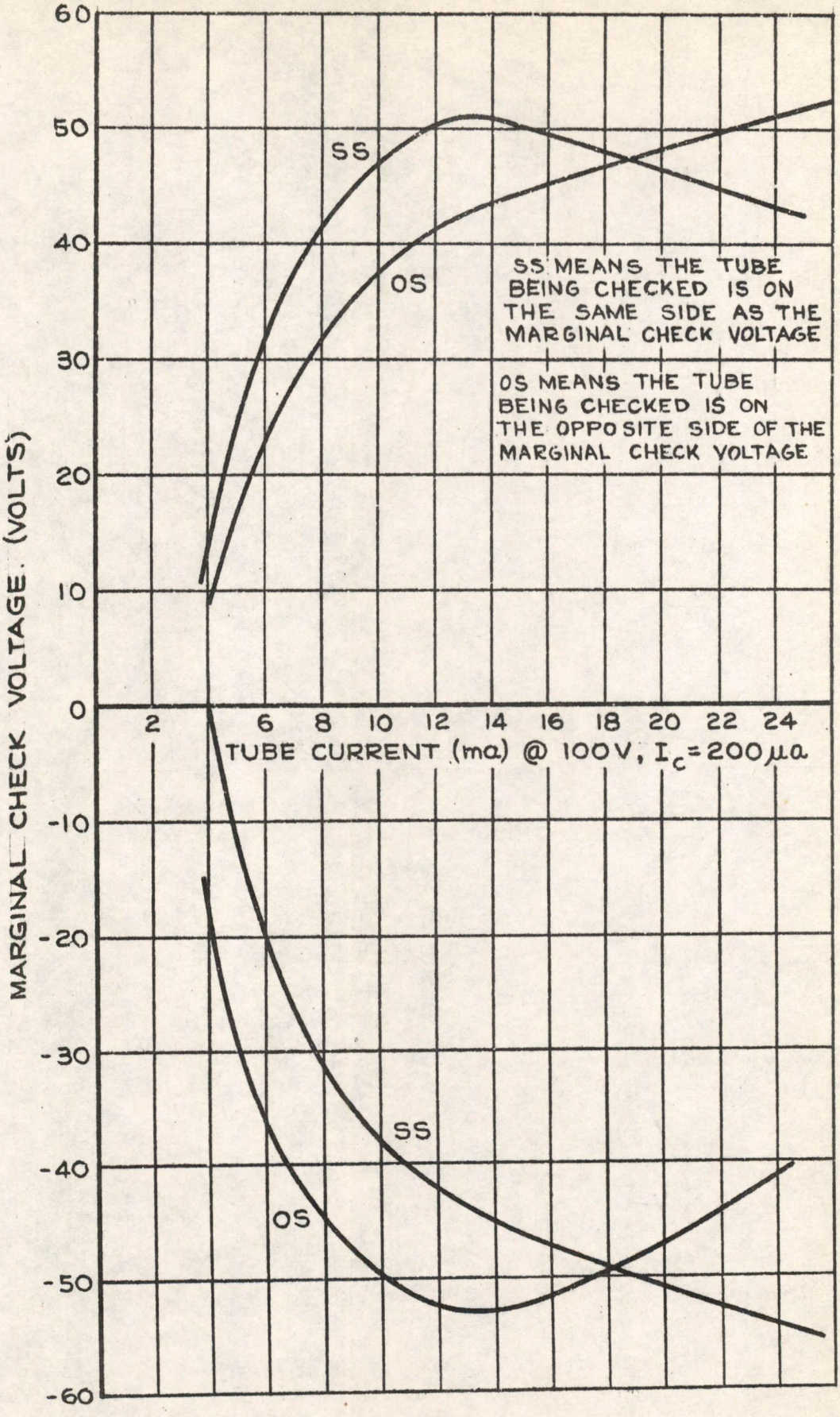


FIG. 12

TUBE MARGINS (USING OLD DIVIDER NETWORK)

A-65350

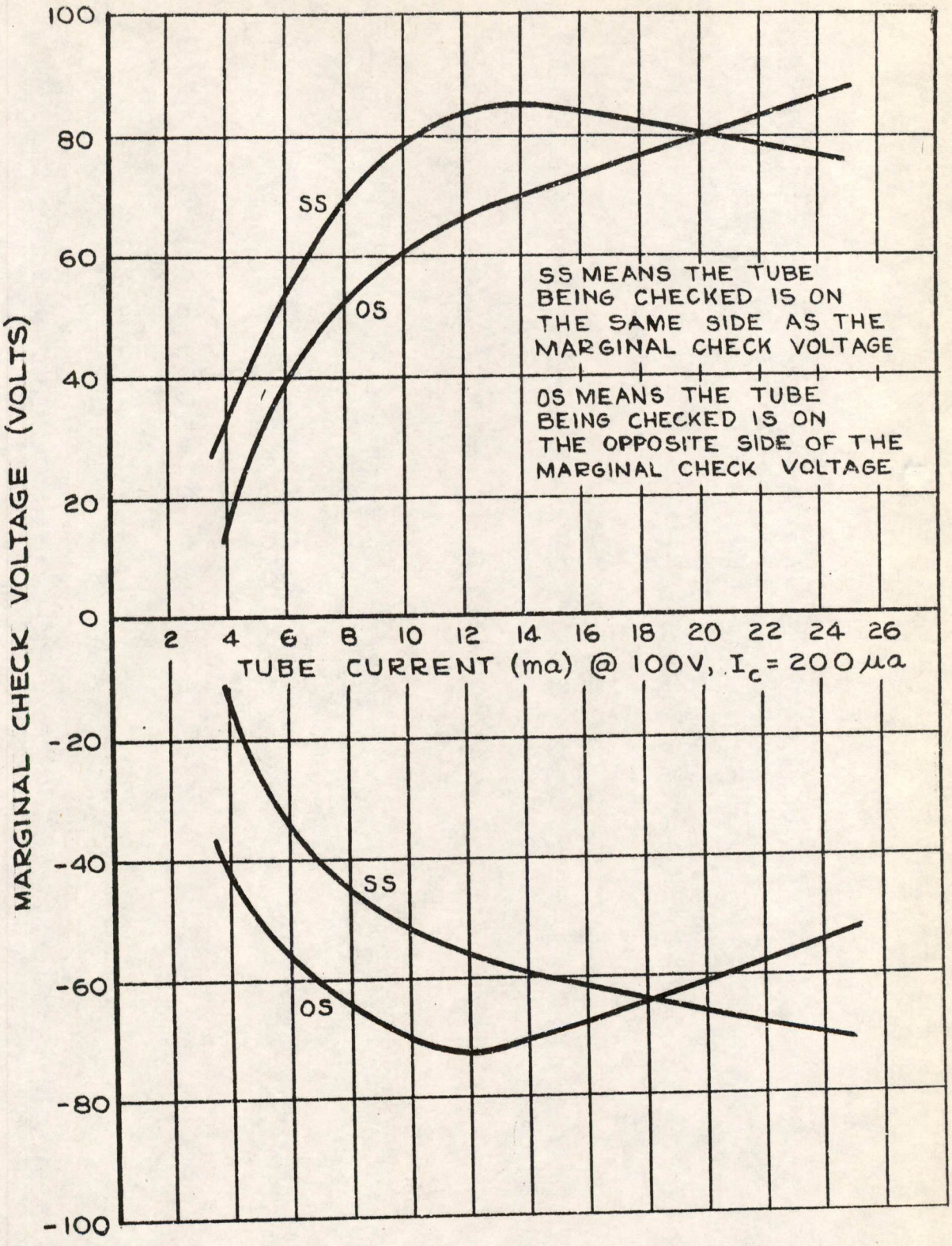


FIG. 13

TUBE MARGINS (USING NEW DIVIDER NETWORK)

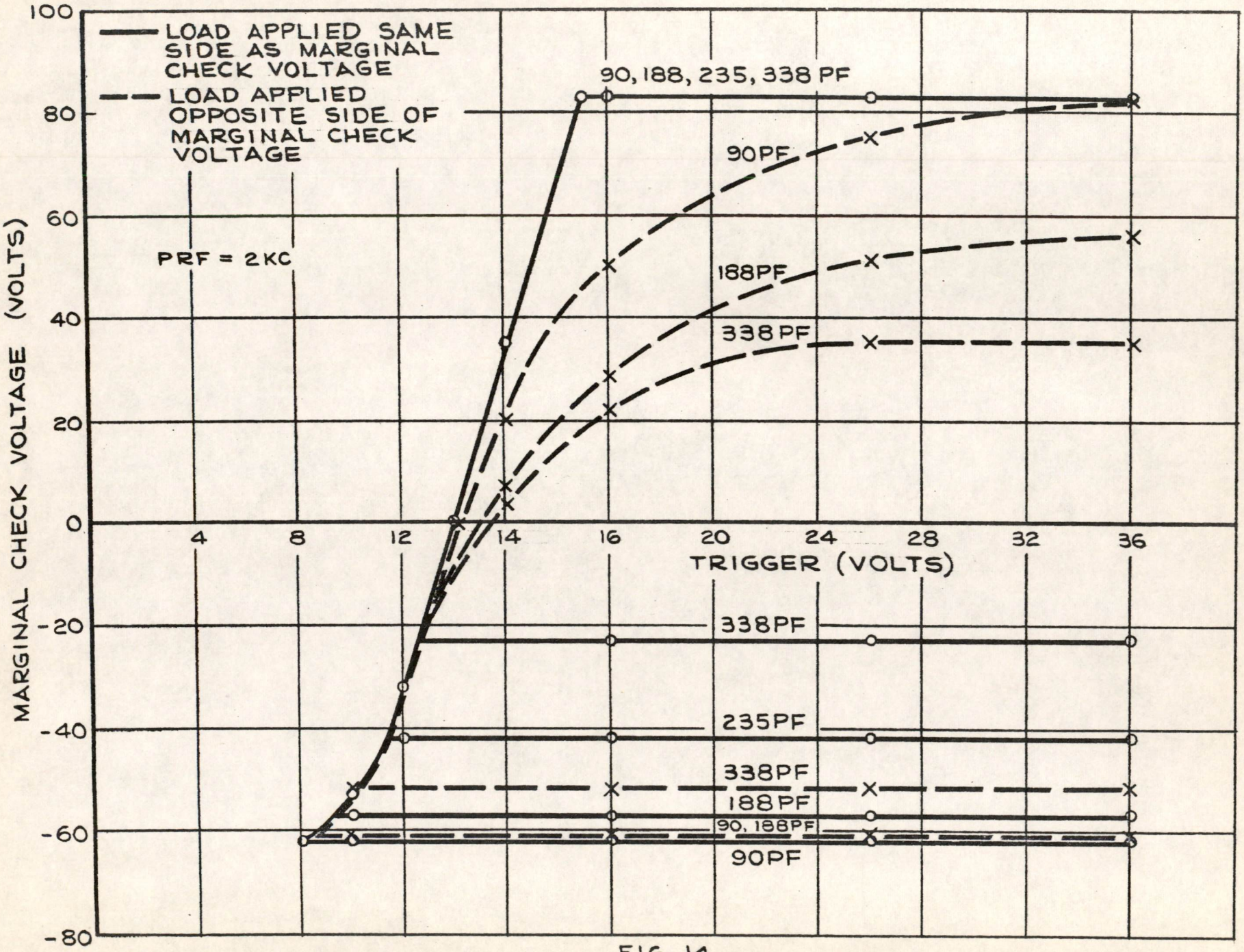


FIG. 14

SET AND CLEAR MARGINS (UNBALANCED LOAD)

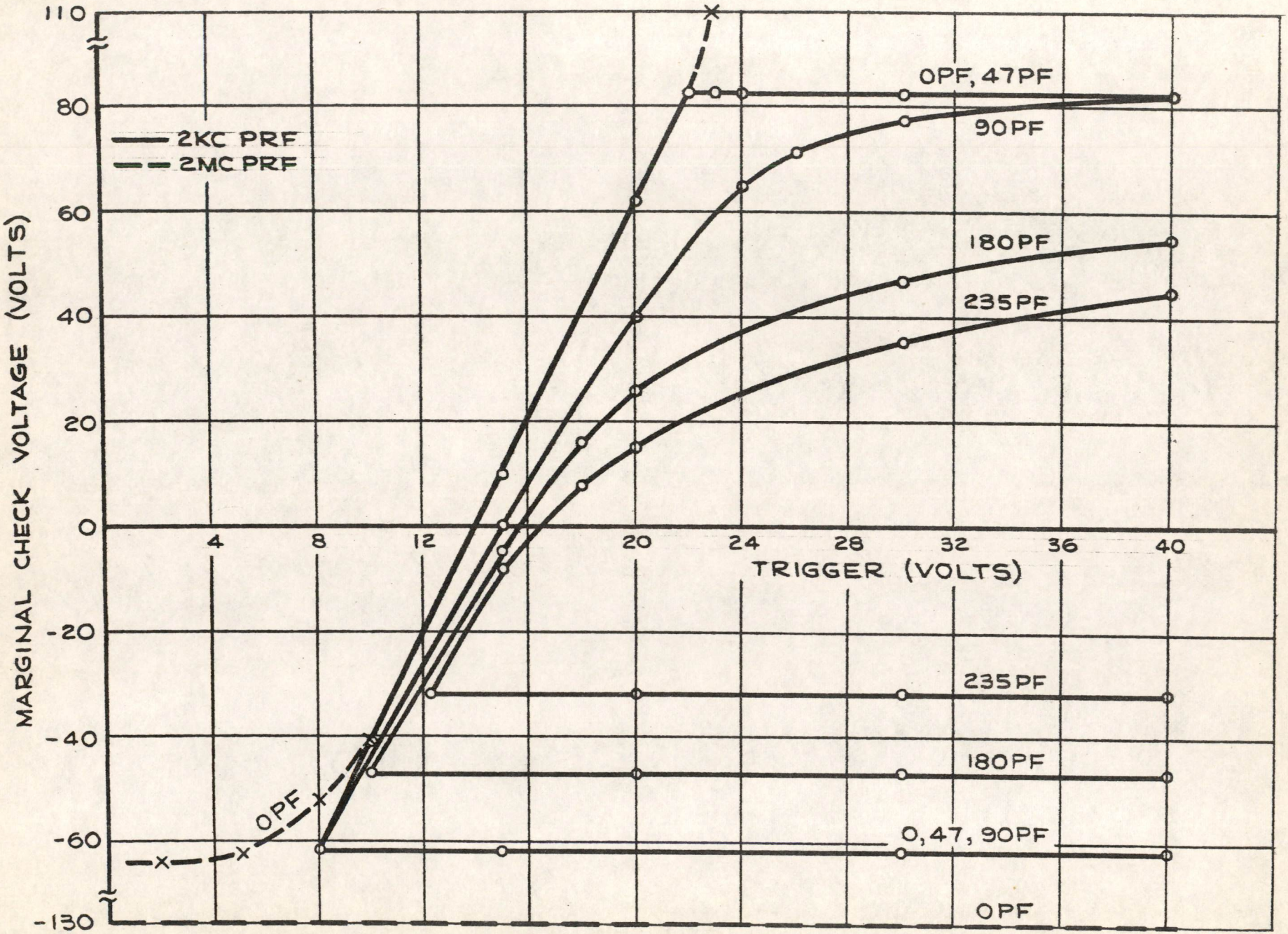


FIG. 15

SET AND CLEAR MARGINS (BALANCED LOAD)

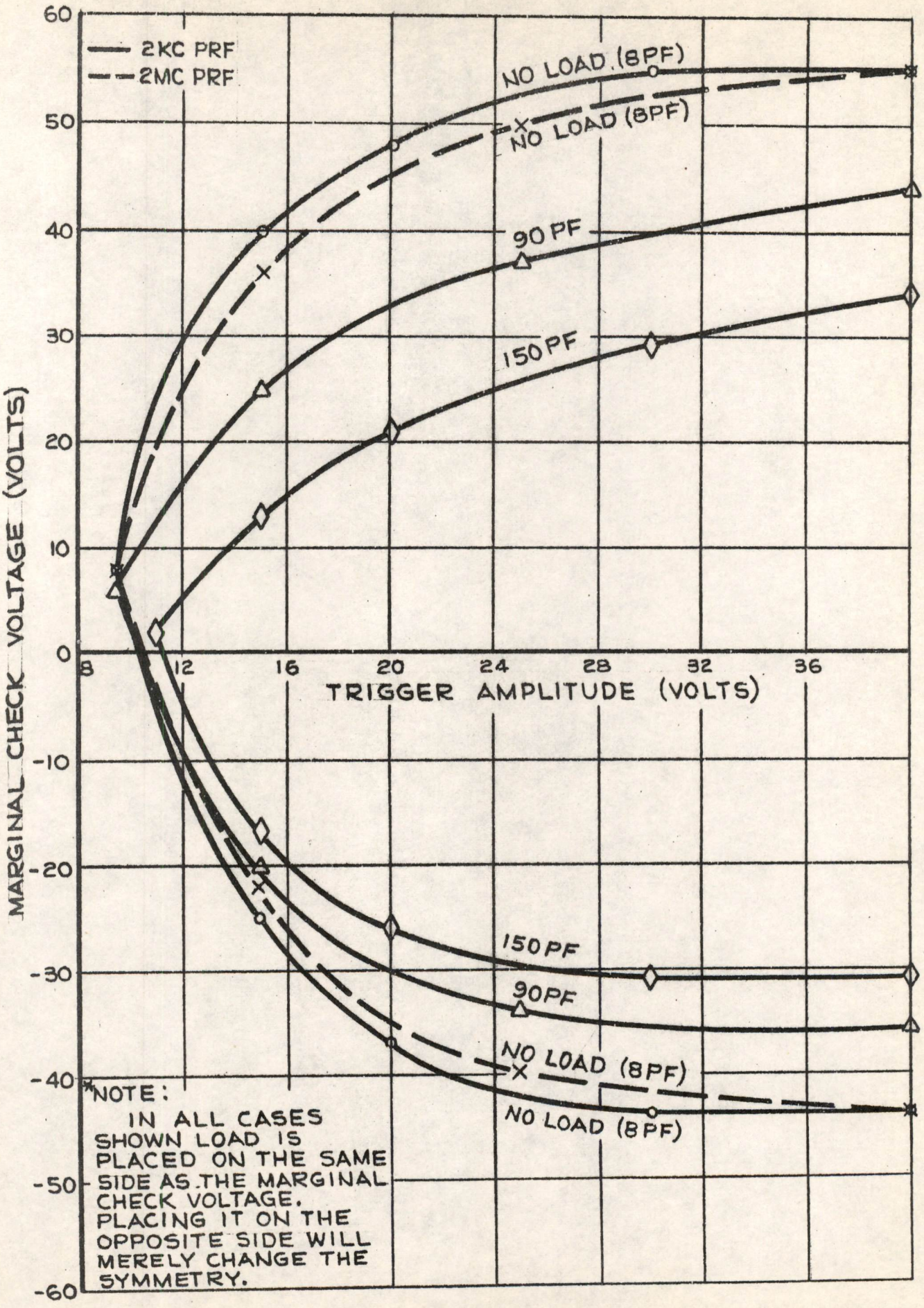


FIG. 16

COMPLEMENT MARGINS (UNBALANCED LOAD)*

A-65344

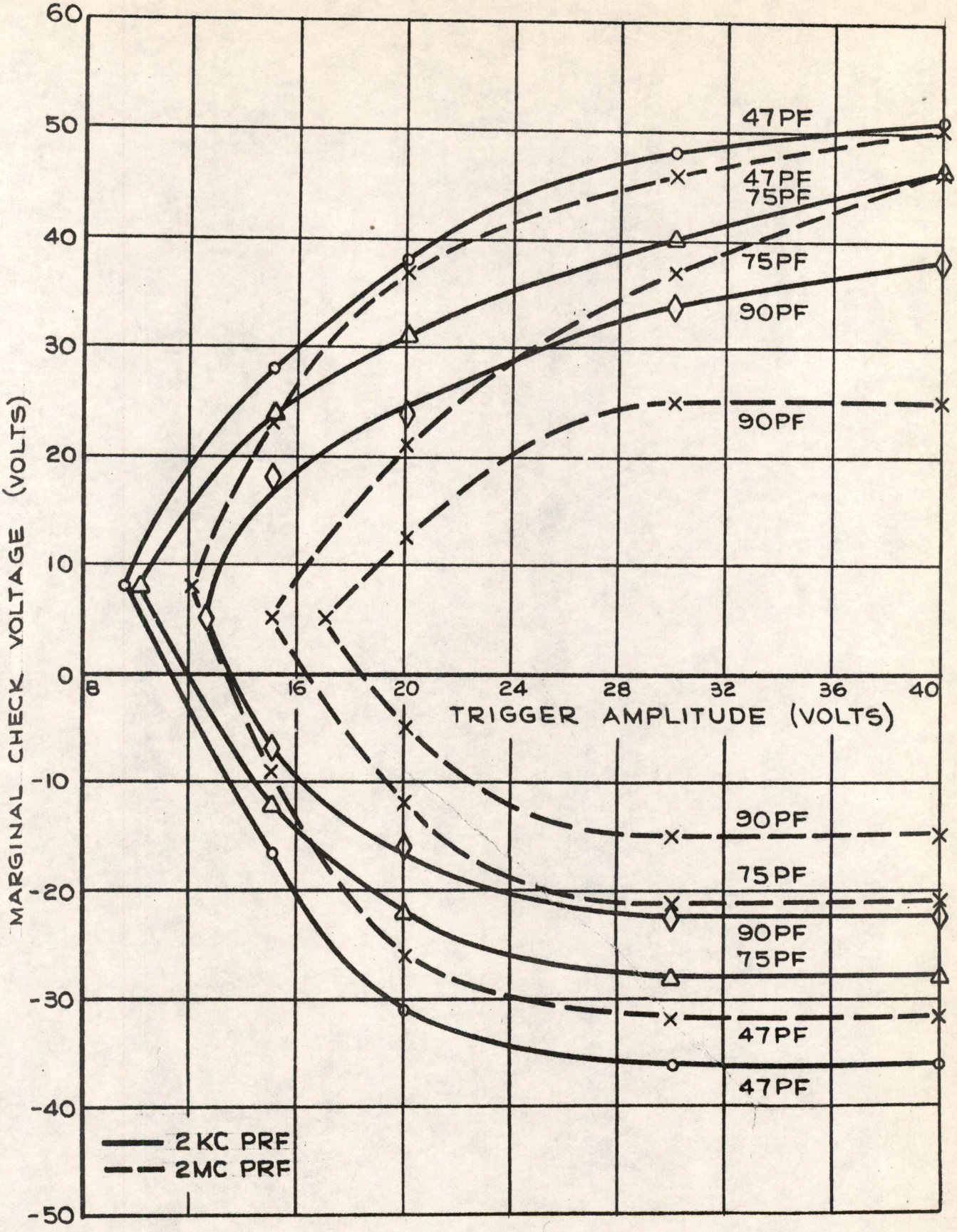
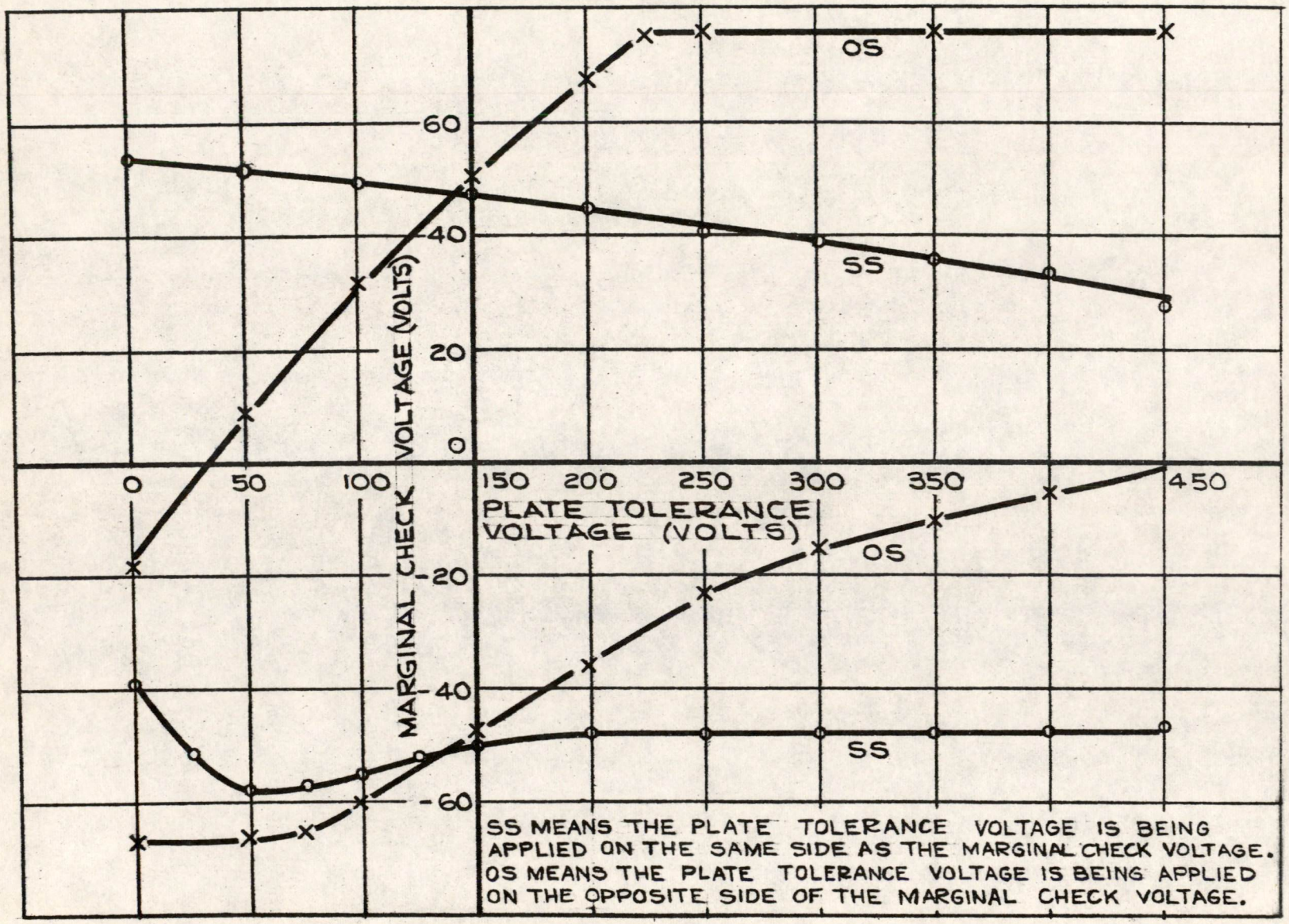


FIG. 17

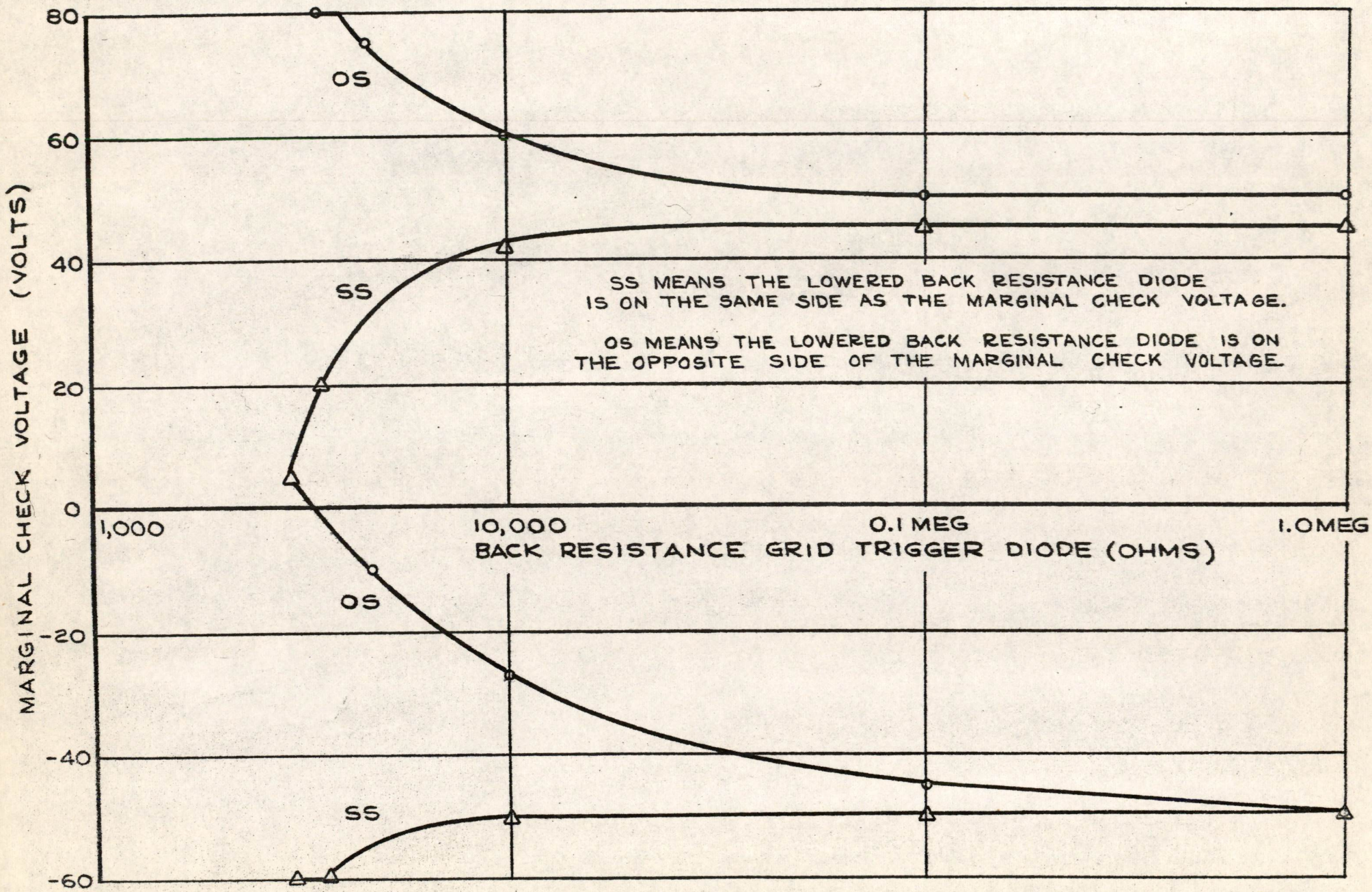
COMPLEMENT MARGINS (BALANCED LOAD)

A-65348



MARGINS vs. INJECTED PLATE TOLERANCE VOLTAGE

A-65135



GRID TRIGGER DIODE BACK RESISTANCE MARGINAL CHECK

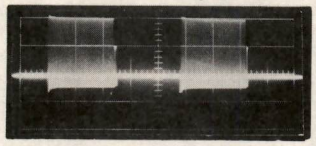


FIG. 20

INPUT PULSE TRAIN ON SET SIDE.

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μ SEC./CM

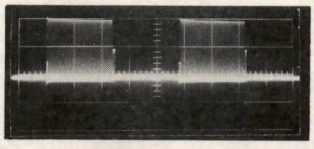


FIG. 21

PULSE TRAIN AT 39 μH CHOKE.

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μ SEC./CM

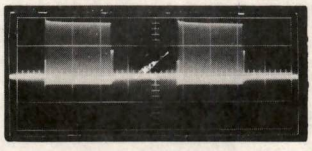


FIG. 22

PULSE TRAIN AT DAMPING DIODE.

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μSEC./CM

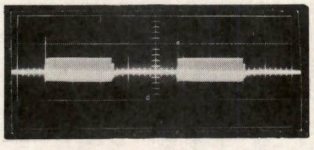


FIG. 23

PULSE TRAIN AT CATHODE TAP.

VERT. SCALE: 10V/CM
HOR. SCALE: 10 μSEC./CM

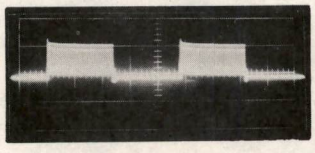


FIG. 24

PULSE TRAIN AT CATHODE.

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μSEC./CM

RECOVERY OF FLIP-FLOP TO PULSE TRAINS AT VARIOUS TEST POINTS

A-65333

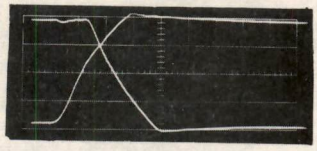


FIG. 25

NO LOAD (8PF)
VERT. SCALE: 10V/CM
HOR. SCALE: 0.1 μSEC./CM

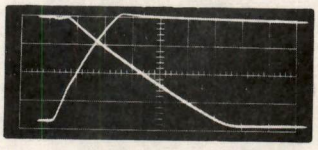


FIG. 26

270 PF LOAD
VERT. SCALE: 10V/CM
HOR. SCALE: 0.2 μSEC./CM

COMPLEMENT OPERATION

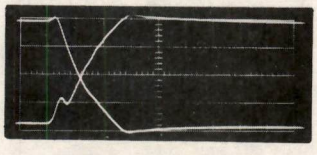


FIG. 27

NO LOAD (8PF)
VERT. SCALE: 10V/CM
HOR. SCALE: 0.1 μSEC./CM

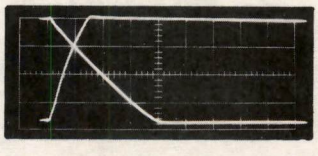


FIG. 28

478 PF LOAD
VERT. SCALE: 10V/CM
HOR. SCALE: 0.5 μSEC./CM

SET AND CLEAR OPERATION

EFFECTS OF CAPACITIVE LOADING ON OUTPUT WAVEFORM

A-65334

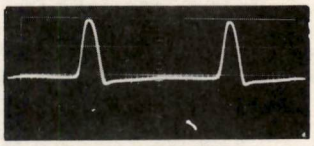


FIG. 29

WAVESHAPE PRIOR TO GRID DIODE.

VERT. SCALE: 10V/CM
HOR. SCALE: 0.1 μSEC./CM
SET & CLEAR: 2MC/SEC.

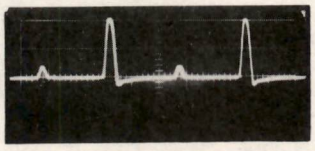


FIG. 30

WAVESHAPE PRIOR TO GRID DIODE.

VERT. SCALE: 10V/CM
HOR. SCALE: 0.2 μSEC./CM
SET & CLEAR: 1MC/SEC.

EFFECT OF CLAMPING CIRCUIT AT DIFFERENT PULSE REPETITION FREQUENCIES

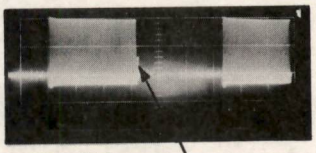


FIG. 31 — CRITICAL PULSE

INPUT PULSE TRAIN WITH CRITICAL PULSE NECESSARY TO CLEAR FLIP-FLOP AFTER EACH BURST.

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μSEC./CM

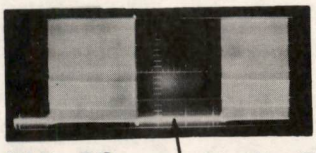


FIG. 32 — FLIP-FLOP CLEARED BETWEEN PULSE TRAINS

OUTPUT OF FLIP-FLOP FOR INPUT CONDITIONS OF FIG. 31

VERT. SCALE: 20V/CM
HOR. SCALE: 10 μSEC./CM

RECOVERY OF FLIP-FLOP FROM LONG PULSE TRAINS

A-65336

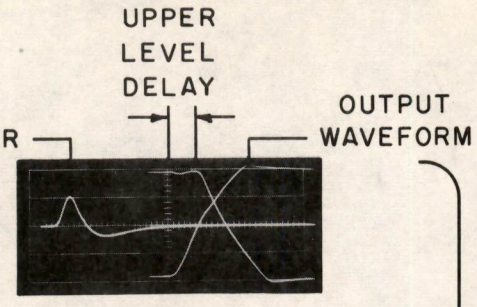


FIG. 33

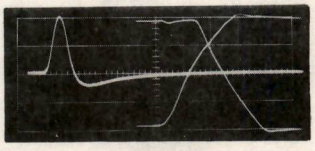


FIG. 34

COMPLEMENT
OPERATION

VERT. SCALE: 10V/CM
HOR. SCALE: 0.1 μSEC/CM

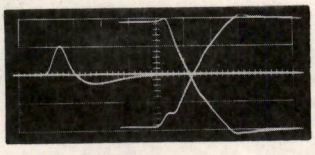


FIG. 35

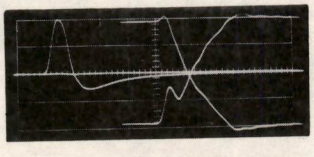


FIG. 36

SET AND CLEAR
OPERATION

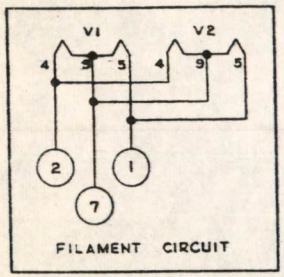
VERT. SCALE: 10V/CM
HOR. SCALE: 0.1 μSEC/CM

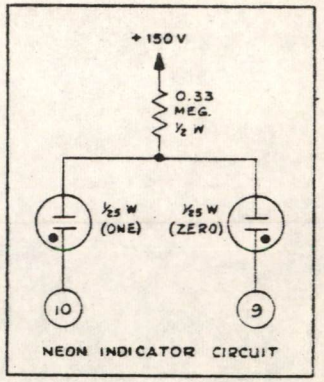
EFFECTS OF PULSE AMPLITUDE ON UPPER LEVEL DELAY

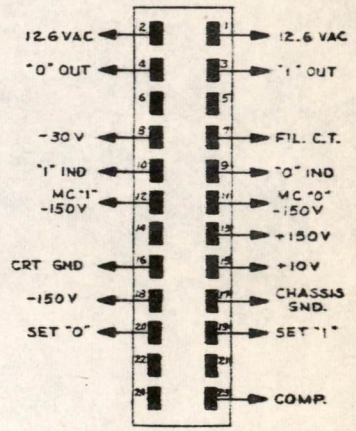
A-65335

C-63287

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± 1/2°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY







NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, 1W ±10%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34.
   D. TRIGGER DIODES MUST BE USED EXTERNALLY AT SET "0" AND SET "1".

DRAWING REFERENCES:
1. ASSEMBLY: C-65638
2. PARTS LIST: PL-65638
3. PHYSICAL LAYOUT: C-65137

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADED BY: DATE: 3/21/56 GRADE III FINAL DESIGN

FIG. 37

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC,
PIU MOD IV FLIP-FLOP, MTC

SCALE: DR. JK 1-26-56
ENG. 3/16/56 CK. 3-16-56 APPD. 3/21/56
C-63287

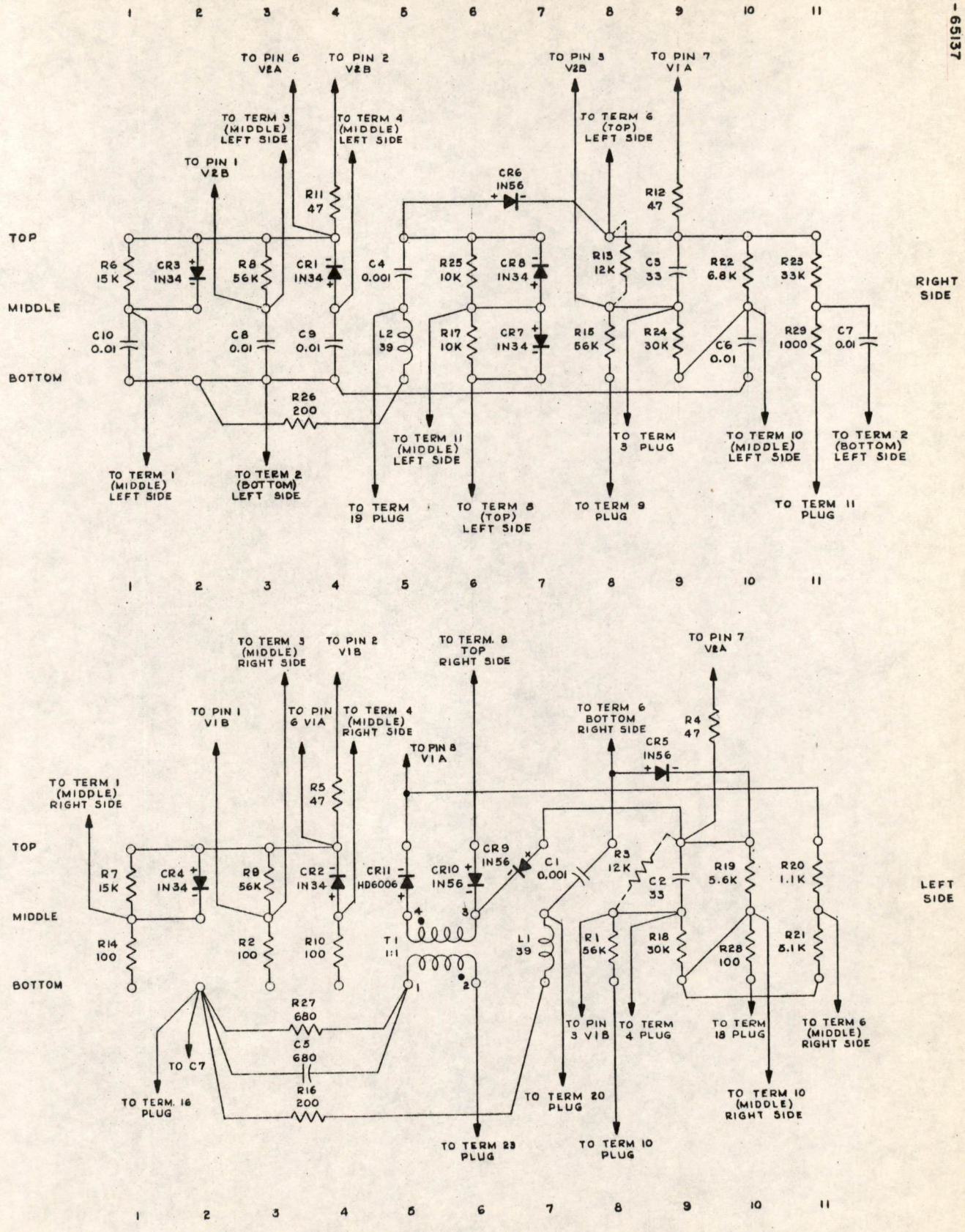


FIG. 38

PHYSICAL LAYOUT OF THE MTC HIGH SPEED FLIP-FLOP (MOD. IV)

K. H. Olsen

B 191

Memorandum 6M-4110

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: Surface-Barrier Transistor Life Tests

To: D. R. Brown

From: D. J. Eckl and R. L. Burke

Date: December 14, 1955

Approved: DRB
D. R. Brown

Abstract: The question of transistor reliability can be answered with assurance only by testing reasonable numbers of units under conditions similar to those which will occur in use. Toward this end 444 surface-barrier transistors (type SB-100) have been placed on life test and have accumulated a total of 1,653,500 transistor-hours with 2 failures. In addition an 8-digit multiplier (TM-1) has operated for 2,800 hours with 480 transistors with 1 transistor failure. 1,500,000 hrs

TM-1, which uses modified direct-coupled circuits, has operated for periods of a week without error on building AC power. A double-rank 8-digit shift register using direct-coupled circuits and completely shielded, has maintained a fixed pattern while shifting at a 1 mc/s rate for 4,526 hours and at this writing is continuing to do so.

All transistors considered, the failure rate is about 0.1% per thousand hours.

3000
500
1,500,000

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

1.0 INTRODUCTION

When new components are used in applications where reliability and longevity may be measured in terms of very large amounts of money and perhaps even human life, it is essential to know in advance the reliability and life expectancy of the new device. This information can best be obtained by working with the component in a system of reasonable size, but setting up such a system takes time. As an alternative special circuits can be built rapidly and in quantity to test the device under conditions similar to those anticipated in service. This latter approach has been used for the most part in life-testing transistors in Group 63.

Life testing[1] of transistors started in 1952-53 when 91 point-contact transistors of various types were placed in some rather severe tests for a 5000 hour period. There were 14 failures. Some more useful life tests were made on junction transistors during 1952-54 by R. H. Baker of Group 24. A brief summary of the results he obtained is listed below:

TYPE OF TRANSISTOR	No. OF UNITS	DURATION OF TESTS	FAILURES
PNP Alloy (audio)	128	16,016 hours	9 (4 Mechanical)
PNP Alloy (audio)	350	6,000	1
PNP Alloy (audio)	32	10,264	0
PNP Alloy (audio) (Plastic encapsulation)	32	10,264	3
PNP Alloy (computer type)	36	8,264	0
Si NPN Alloy	50	7,000	0
SYSTEM	1,200	1,900	1

These tests showed that conventional transistors could be used with success in carefully designed circuits. A failure was defined to have occurred when the circuit quit operating normally. The transistor parameters in some cases varied considerably during the course of the tests.

The overall tests, including a few not listed here, total about 8 million transistor-hours and the failure rate is somewhat over 0.1% per thousand hours.

---

1. Results of Transistor Life Tests; June 1952 to April 1953, Div. 6 Memorandum 6M-2325.

When it was decided to use large numbers of surface-barrier transistors in high-speed computer circuits, it was considered necessary to initiate life tests immediately. This memorandum describes the present status of these tests.

2.0 DIRECT-COUPLED FLIP-FLOP TESTS

When surface-barrier transistors became available to the laboratory in Nov. '54, a life test consisting of two flip-flops of the type shown in Fig. 1 was started. About a month later four more such circuits were placed on test. Initially to save time the trigger pulses were supplied by a system of Burroughs Pulse Control vacuum tube equipment. This system was replaced on Dec. 1, 1955 by the transistorized control shown in Fig. 2. There have been two transistor failures, both sudden and complete and both apparently caused by external means. The first at 125 hours occured when the ground clip of a scope probe brushed the collector of a flip-flop transistor. The second failure occurred at 7,075 hours during the removal of a driver transistor for testing.

The transistors are soldered into circuits so there can be no regular parameter checks. However, all transistors were tested initially and were removed for retesting at 7,075 hours. The results of this test are:

Average change in forward α = none
Average change in reverse α = none
Average change in I_{co} = +0.7 μa
Average change in I_{eo} = +0.7 μa

A summary of the flip-flop tests is presented below:

Circuit	Running Time	No. Transistors
FF no. 1 and 2	9,166 hours	8
FF no. 3 thru 6	8,371 hours	16
Control	336 hours	9
		33 Total

Total Transistor Hours = 210,288
Number of Failures = 2

3.0 SHELF LIFE TEST

As a control test 16 transistors were placed in sockets in the same area as the other tests but not connected to any supply voltages. These transistors have been measured periodically with no change in parameter values.

A summary of the test follows:

Number of transistors = 16
Number of hours = 5,014
Total transistor hours = 80,224
Number of failures = 0

4.0 FREE-RUNNING DIRECT-COUPLED SHIFT REGISTER

Three free-running shift-registers, each containing 16 transistors, have been placed on life test. These are 2-digit double-rank registers with transfer gates directly coupled in such a manner that the pattern shifts continually at a rate determined by the circuit parameters. The transistors are mounted in sockets so they can be removed for testing.

The first of these is the direct-coupled register shown in Figure 3. This unit runs at 1.75 mc/sec. and has an output voltage swing of 0.45 volts. During its 5,536 hours of operation the transistor parameters have been checked periodically. The results are:

Forward and reverse α = no change
I_{co} = +0.27 μa average change in 4,200 hours
I_{eo} = +0.26 μa average change in 4,200 hours

The present status of this test is listed below:

Number of transistors = 16
Number of hours = 5,536
Total transistor hours = 88,576
Number of failures = 0

5.0 FREE-RUNNING DIODE-COUPLED SHIFT REGISTER

This circuit, shown in Fig. 4 is the same as the previous one except that diodes are used for collector-to-base coupling of all transistors. This arrangement gives an output swing of 1 volt at a frequency of 1.61 mc/sec. The parameter data shows the following:

Forward and reverse α = no change
I_{co} = +0.06 μa average change in 4,000 hours
I_{eo} = +0.08 μa average change in 4,000 hours

The results to date of the tests are:

Number of transistors = 16
Number of hours = 4,576
Total transistor hours = 73,216
Number of failures = 0

6.0 FREE-RUNNING RC-COUPLED SHIFT REGISTER

The third register of the same type uses RC-coupling between each collector and base as shown in Fig. 5. The circuit operates at 3.03 mc/sec with an output of 1.0 volts. Parameter tests are listed below:

Forward and reverse α = no change
I_{co} = +1.17 μa average increase in 4,100 hours
I_{eo} = +1.31 μa average increase in 4,100 hours

The change in I_{co} and I_{eo} for the three registers is different. However, at this time there is no evidence to suggest that this is the result of anything other than variation in groups of transistors. The results of the RC-coupled register tests are as follows:

Number of transistors = 16
Number of hours = 5,484
Total transistor hours = 87,744
Number of failures = 0

7.0 8-DIGIT DIRECT-COUPLED SHIFT REGISTERS

Two 8-digit direct-coupled shift registers with control circuits have been placed on life test. These are double rank units which shift at a rate of 1 mc/sec. There are 80 transistors in each register and 19 in each control. One unit is completely shielded and the other is unshielded in an attempt to determine the effect of outside noise. 3-volt batteries are used for supply voltages. The power requirements are 420 mw each. The circuit of the register is shown in Fig. 6; the control in Fig. 7.

7.1 SHIELDED 8-DIGIT SHIFT REGISTER

The pattern circulating in the register is 11001000 and the register is checked morning and night to see that it is unchanged. The present run was started June 8, 1955 and as of December 14, an elapsed time of 4,526 hours, it has still remained unchanged. Batteries are changed once a week without stopping the register's operation. During the course of a week the supply voltage varies from -3 volts to about -2 volts. A summary of the results of the test follows:

Number of transistors = 99
Total number of operating hours = 5,828
Longest error-free run = 4,526 hours, continuing.
Total transistor hours = 576,972
Number of failures = 0

7.2 UNSHIELDED 8-DIGIT SHIFT REGISTER

This register is also circulating a 11001000 pattern at 1mc/sec. It is operated under conditions in all respects similar to the first except that there is no shielding. The longest error-free run made by this unit was 1,801 hours. A comparison of the error-free intervals of the two registers is given on the following page. An error here means a loss of pattern.

UNSHIELDED REGISTER

Error No.	Hours since Last Error
Testing, etc.	164
1	2
2	1
3	67
4	27
5	314
6	332
7	6
8	362
9	665
10	24
11	24
12	153
13	15
14	1801
15	312
16	217 (continuing)
	4486 Hours Total

SHIELDED REGISTER

Error No.	Hours since Last Error
Testing, etc.	77
1	60
2	71
3	469
4	55
5	90
6	336
7	144
8	4526 (continuing)
	5828 Hours Total

The record of the shielded register has been the better, but part of the early poor record of each unit was due to cold solder joints, unsoldered connections, poor grounds, etc. There is no satisfactory way of comparing these factors in each case and no details are available. A summary of the information on the unshielded register follows:

Number of transistors = 99
Total number of operating hours = 4486
Longest error-free run = 1,801 hours
Total transistor-hours = 444,114
Number of failures = 0

8.0 SINGLE-RANK 8-DIGIT SHIFT REGISTER

A single-rank 8-digit shift register, using the TM-1 flip-flop shown in Fig. 8, has recently been put into operation. The driving circuits are shown in Fig. 9 and 10. This unit has not been in operation long enough to give any significant results. A summary of the data avilable follows:

Number of transistors = 149
Total number of operating hours = 620
Total Transistor-hours = 92,380
Number of failures = 0

The unit is still undergoing initial checks and error-free runs last only a day or two at present. Margins can be measured and will be checked daily in the future.

9.0 THE 8-DIGIT MULTIPLIER

An 8-digit multiplier, TM-1, has been in operation 2,800 hours. The unit has 480 transistors and there has been one failure, a mechanical break at the base tab inside the case, which showed up as an intermittant. The pulse rate is 4 mc/sec. The unit operates from 110V AC building power and consequently one 8-day period has been the longest error-free run. A typical TM-1 flip-flop is shown in Fig. 8. A summary of the present information follows:

Number of transistors = 480
Operating time = 2,800 hours
Total transistor hours = 1,344,000
Number of failures = 1

10.0 SUMMARY

There are 444 transistors in straight life-test circuits which have accumulated 1,653,500 transistor-hours. There are 480 transistors in TM-1 which have amassed 1,344,000 transistor-hours. There have been 3 failures. This is summarized in the accompanying table. The failure rate works out to about 0.1% per thousand hours.

Signed: D. J. Eckl
D. J. Eckl

DJE:lj

Signed: R. L. Burke
R. L. Burke

TEST	NO. OF TRANSISTORS	OPERATING TIME HOURS	TRANSISTOR-HOURS	FAILURES
FF#1 and 2	8	9166		
FF#3 and 6	16	8371	210,288	2
Control for above	9	336		
Shelf Life	16	5014	80,224	0
Direct-coupled Shift-reg.	16	5536	88,576	0
Diode-coupled Shift-reg.	16	4576	73,216	0
R-C Coupled Shift-reg.	16	5484	87,744	0
Shielded Shift-reg.	99	5828	576,972	0
Unshielded Shift-reg.	99	4486	444,114	0
Single-rank Shift-reg.	149	620	92,380	0
TM-1 (Multiplier)	480	2800	1,344,000	1
	924		2,997,514	3

TABLE 1 - SUMMARY OF SBT LIFE TESTS

Attachments:

Fig. 1.	A-65100
Fig. 2.	A-65101
Fig. 3.	B-63083
Fig. 4.	B-63067
Fig. 5.	B-63066
Fig. 6.	C-62994
Fig. 7.	C-63051
Fig. 8.	B-65102
Fig. 9.	B-65103
Fig. 10.	B-65104

Distribution List:

*D. Best
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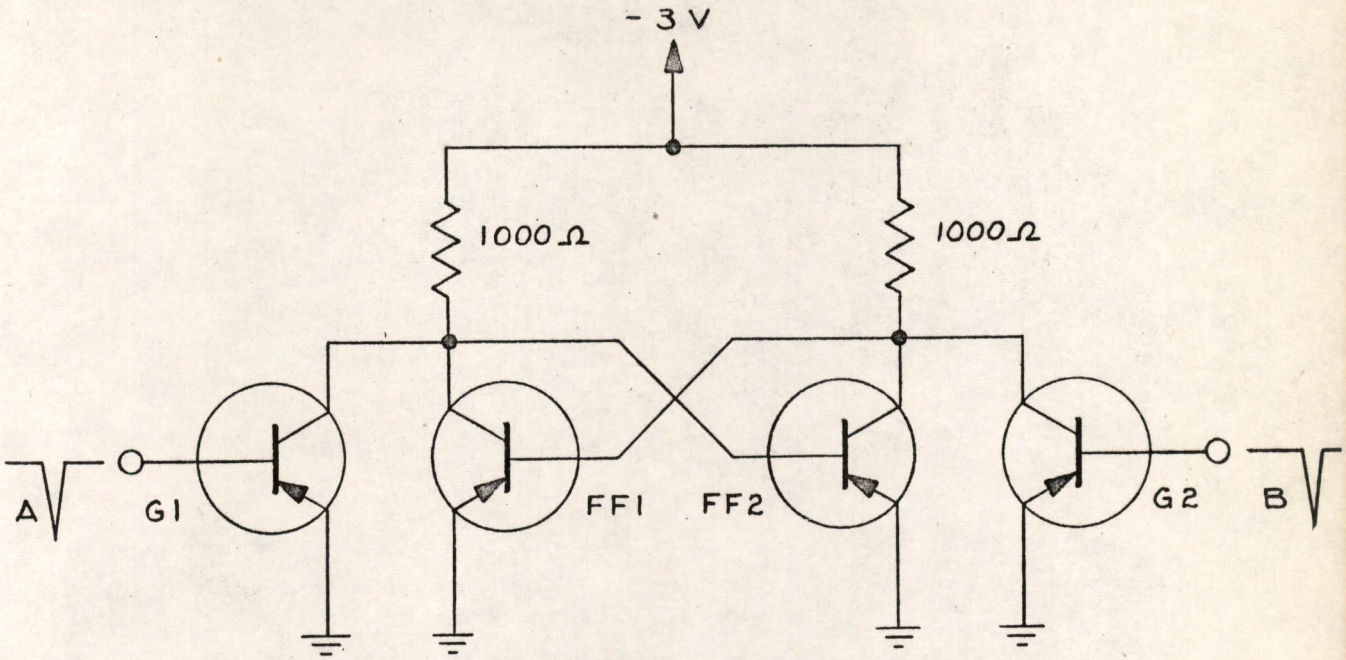
*Recipient of complete Memorandum.



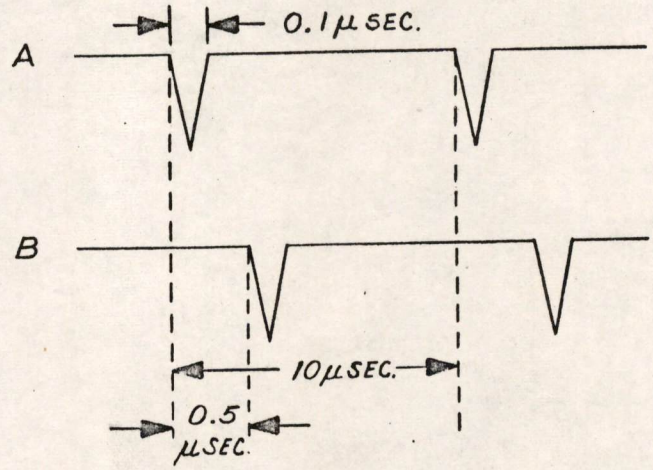


FIG. 1

DIRECT-COUPLED SBT FLIP-FLOP TEST

A-65100

C-65101

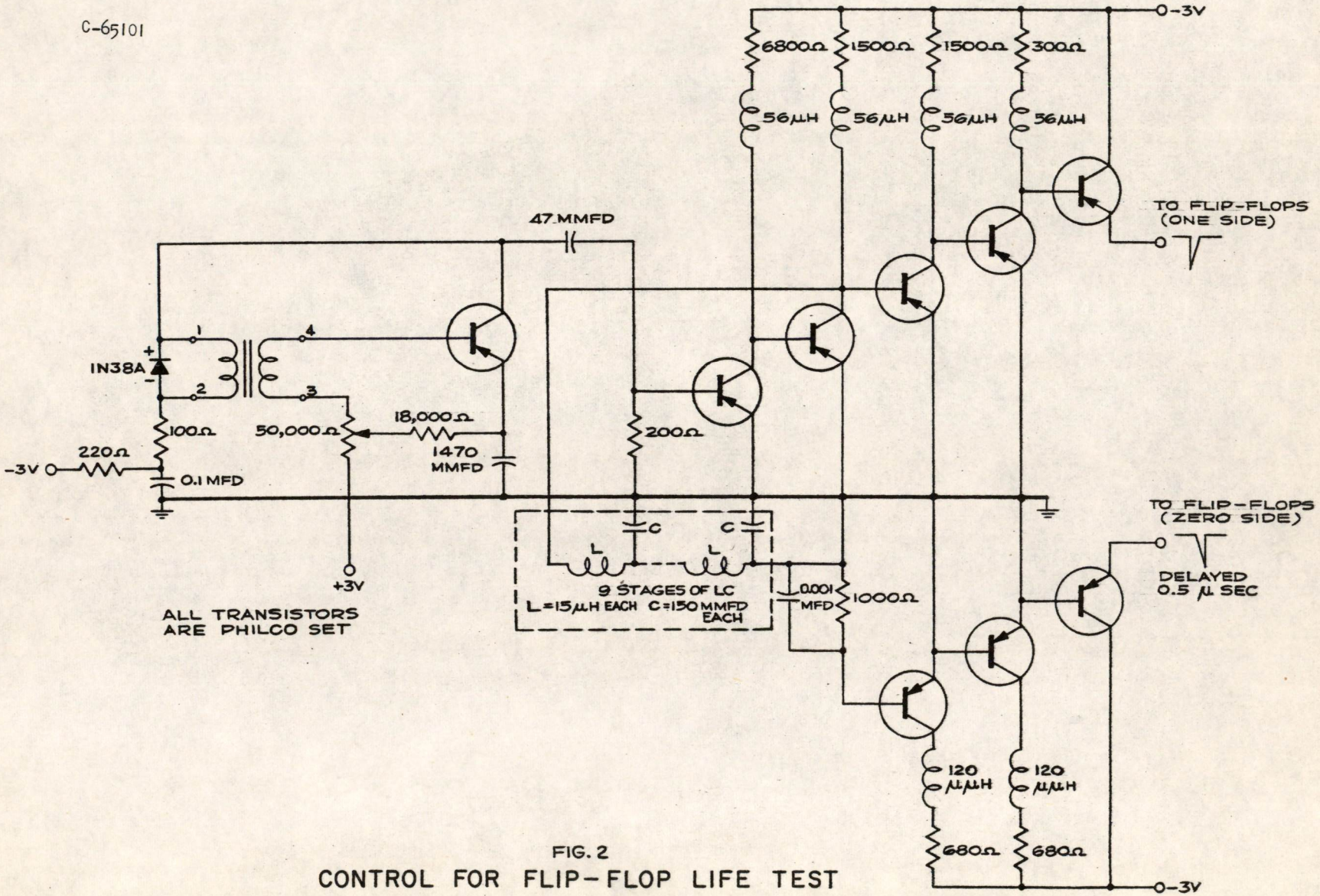


FIG. 2

CONTROL FOR FLIP-FLOP LIFE TEST

B-63083

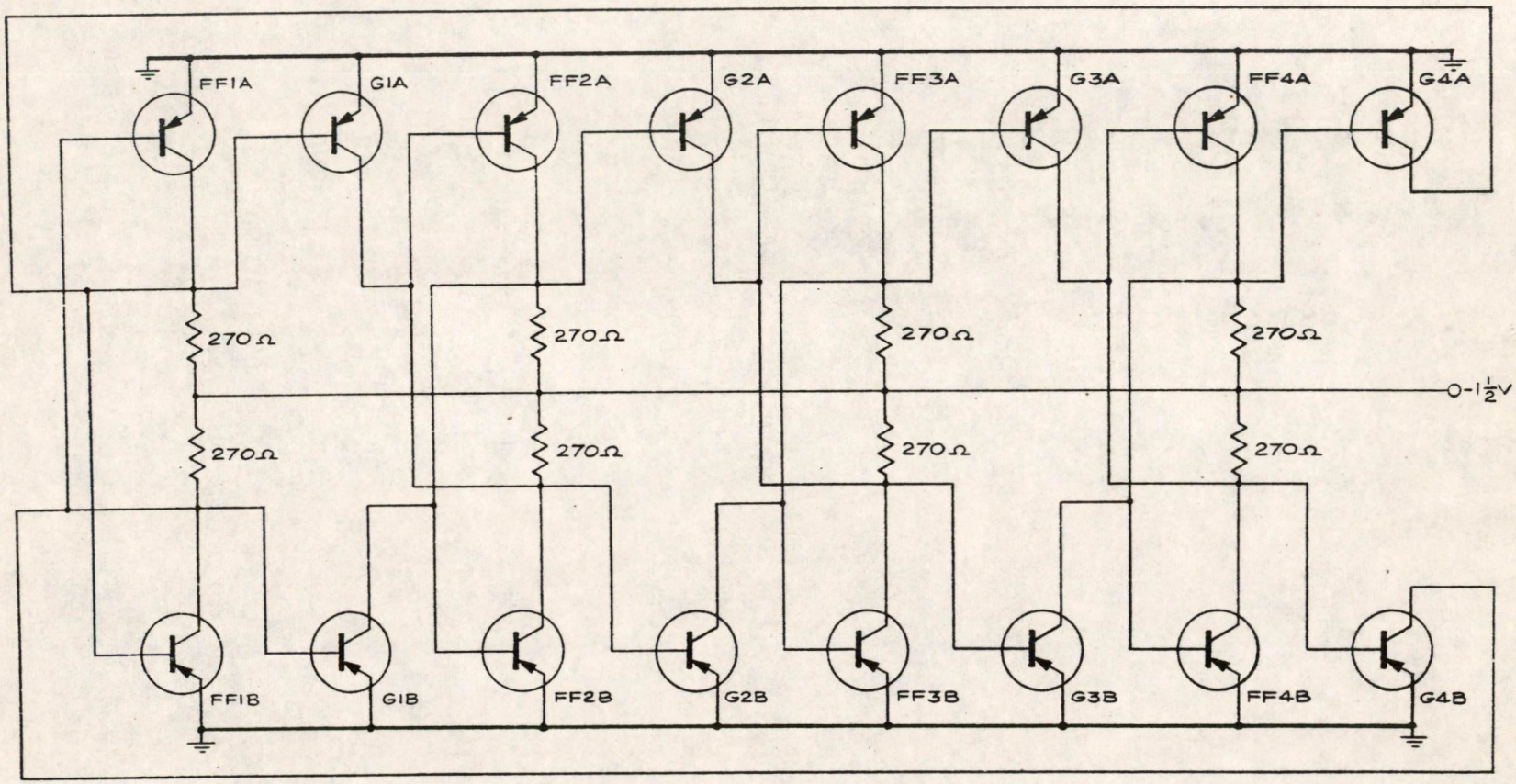
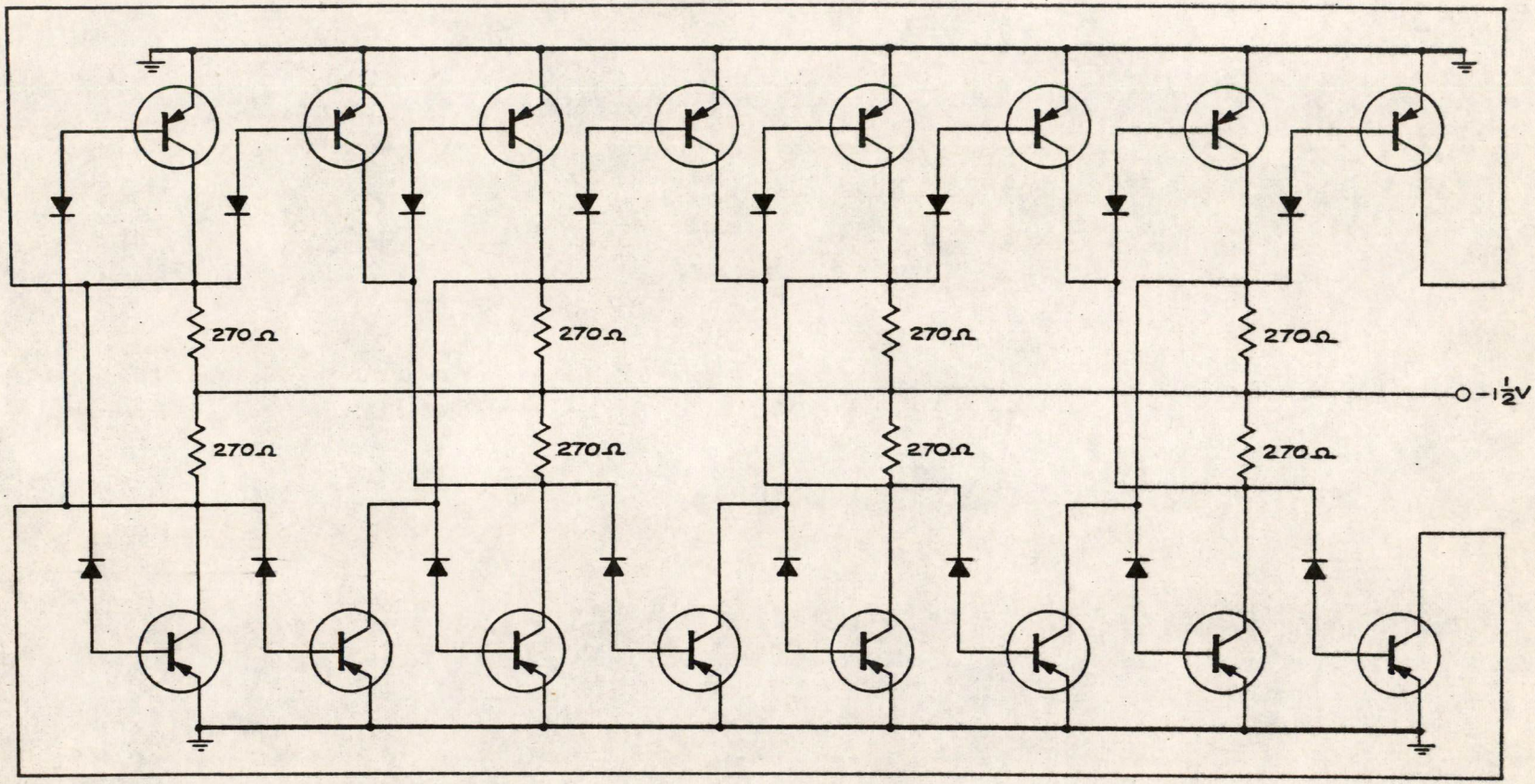


FIG. 3
FREE-RUNNING SHIFT REGISTER (DIRECT-COUPLED)



NOTE: ALL DIODES ARE SYLVANIA 1N138A

FIG. 4

FREE-RUNNING SHIFT REGISTER (DIODE-COUPLED)

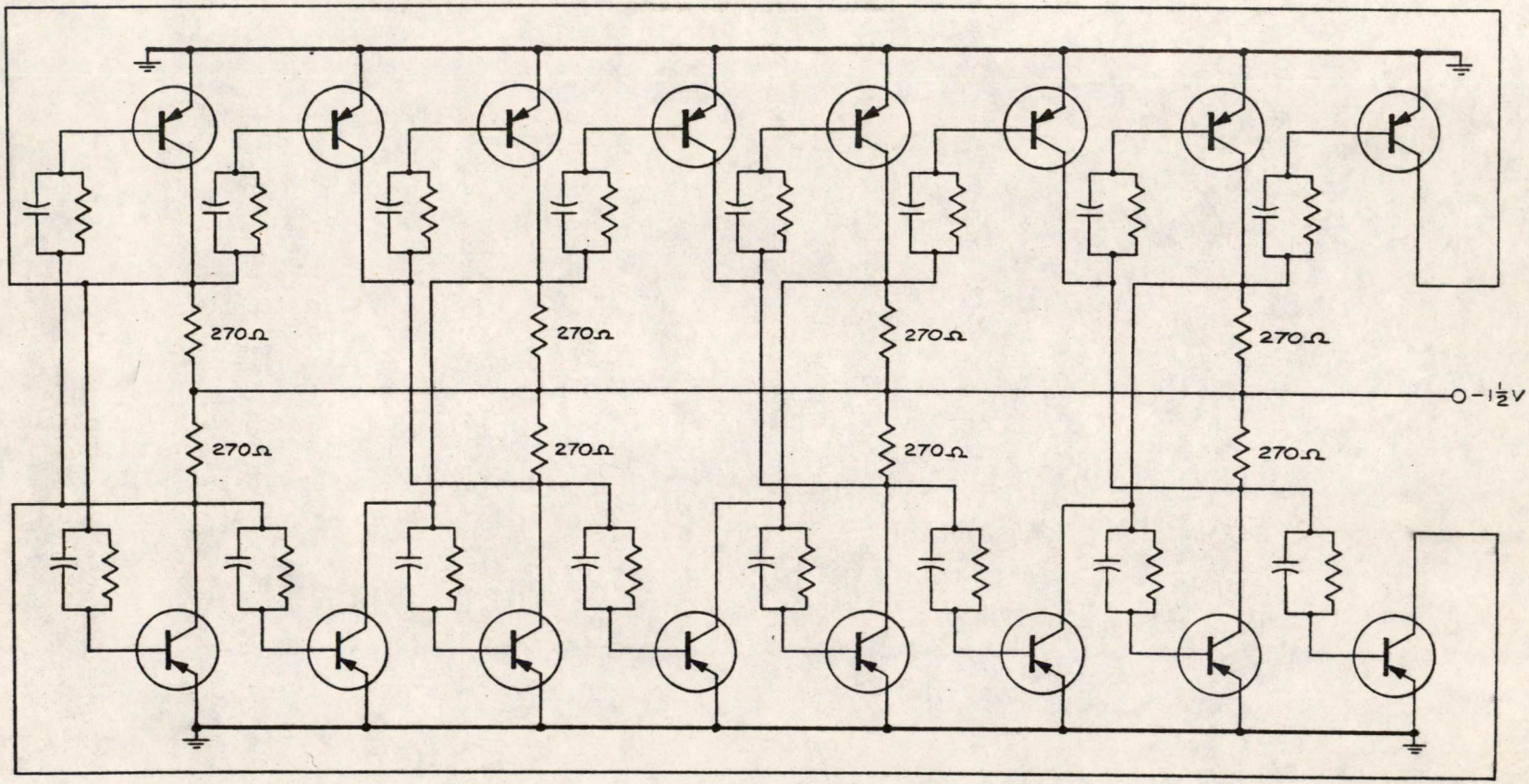


FIG. 5
FREE-RUNNING SHIFT REGISTER (R-C COUPLED)

C-62994
MN

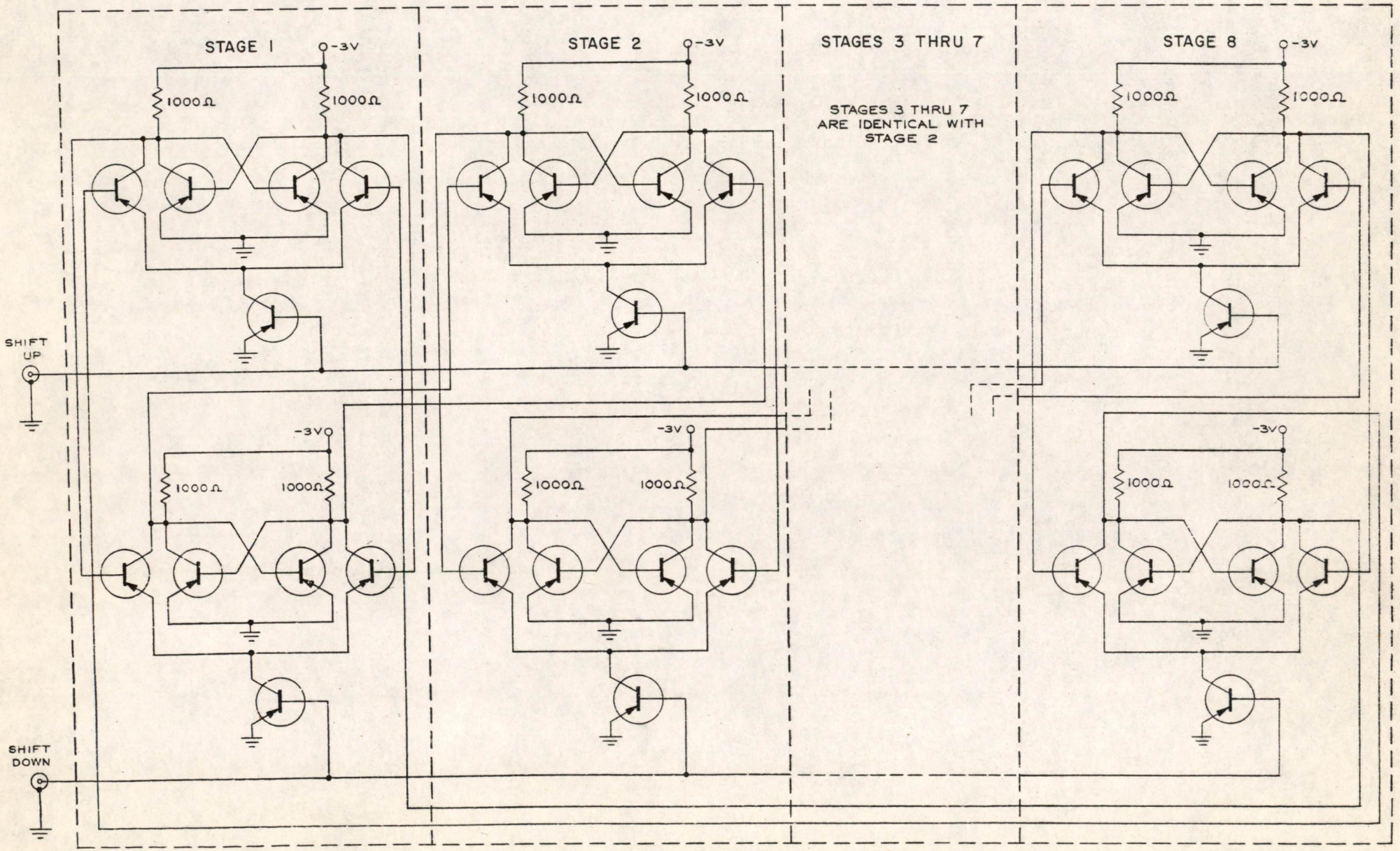


FIG. 6
CIRCUIT SCHEMATIC,
8-DIGIT SBT SHIFT REGISTER

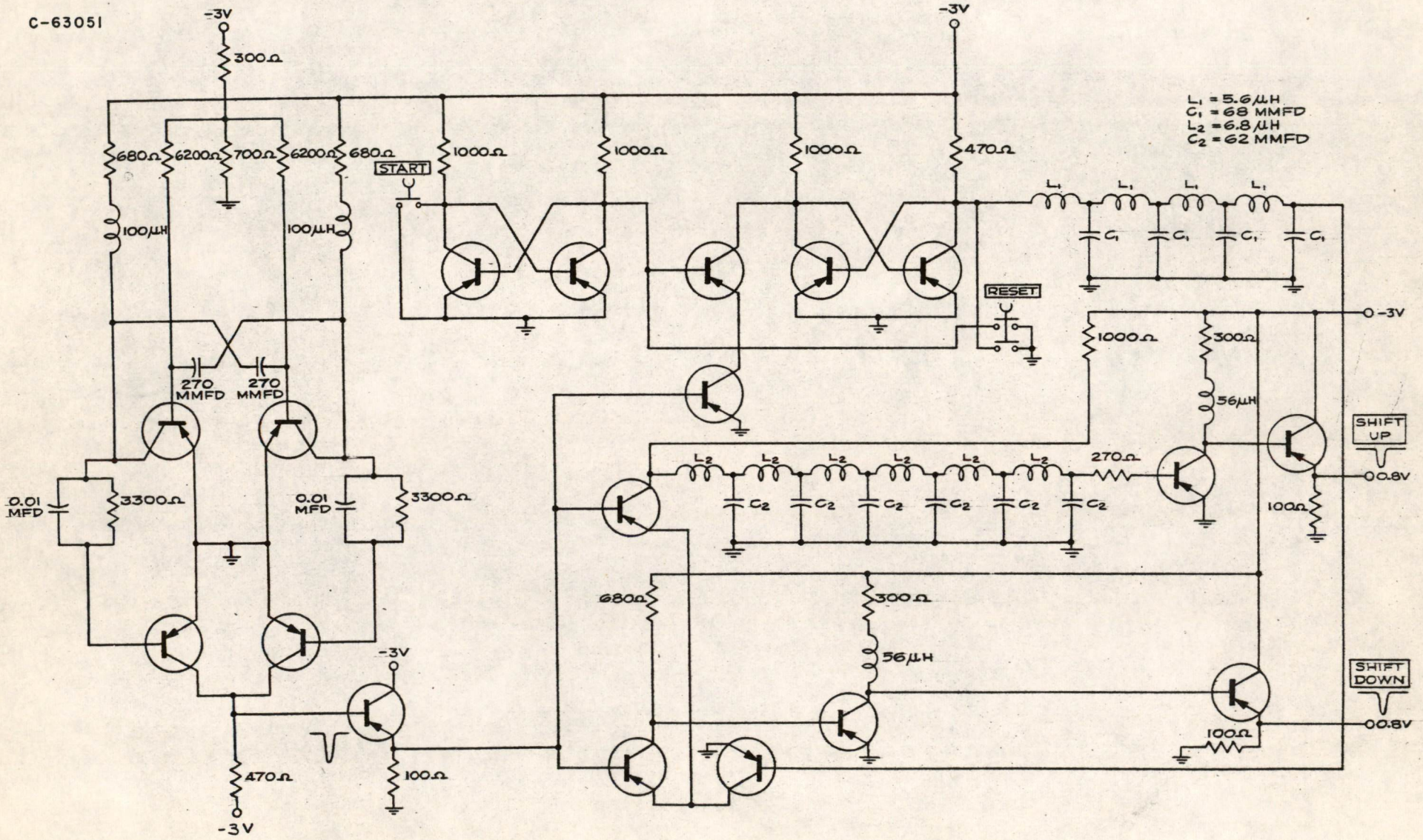


FIG. 7

CONTROL FOR SBT SHIFT REGISTER

B-65102

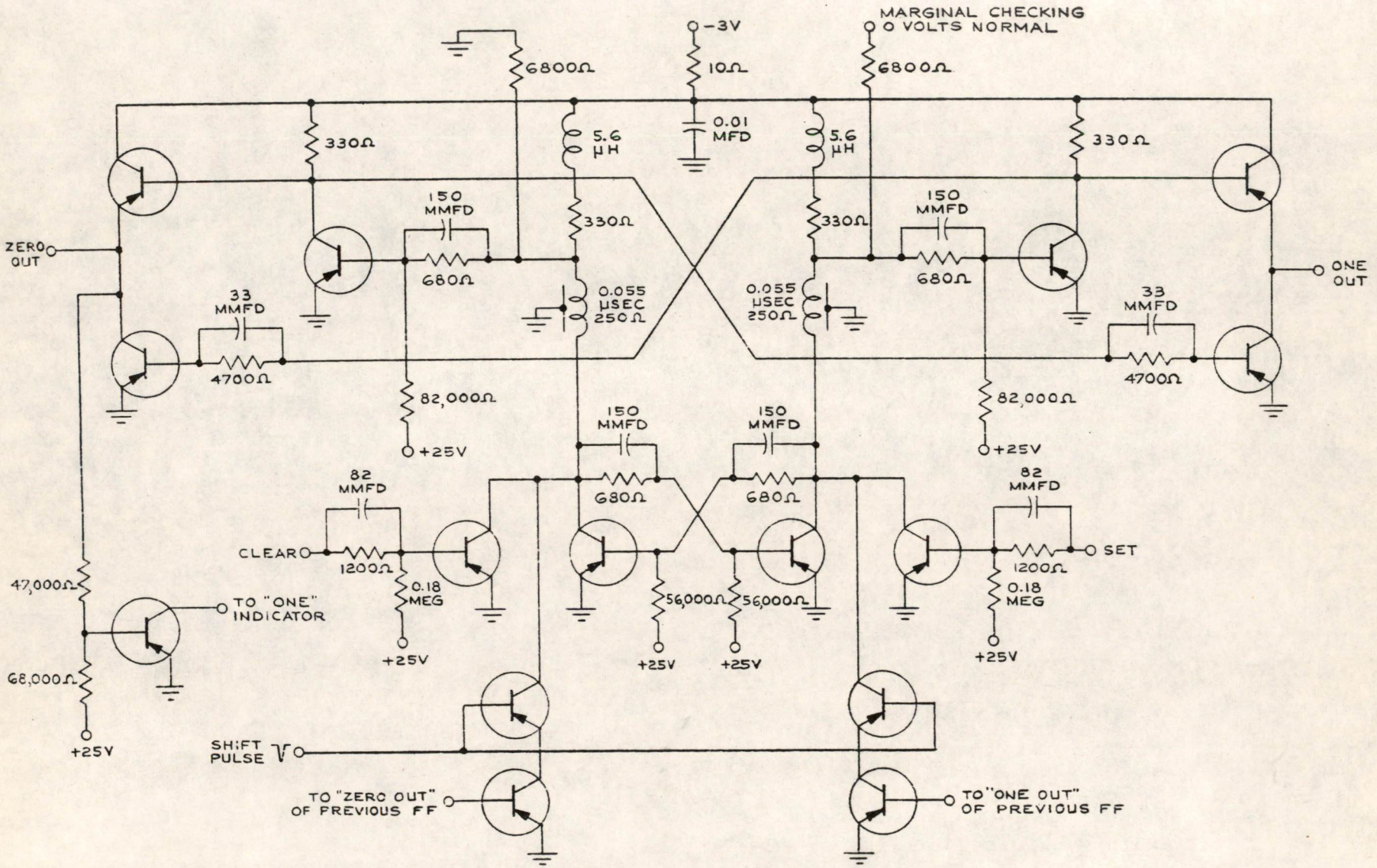


FIG. 8

TM-I PLUG-IN FLIP-FLOP

B-65103

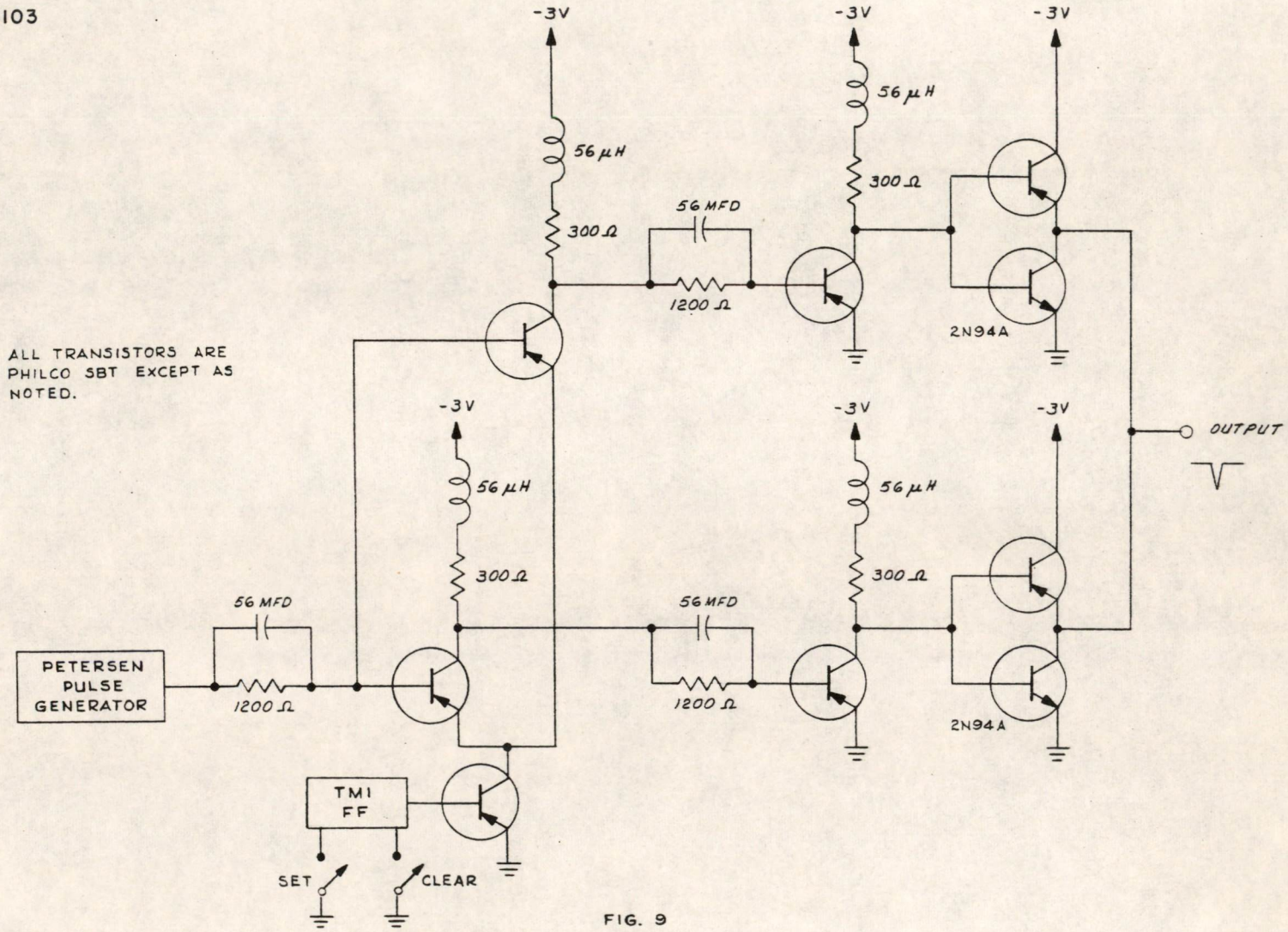


FIG. 9

DRIVER CIRCUIT FOR TM-1 TYPE SHIFT REGISTER

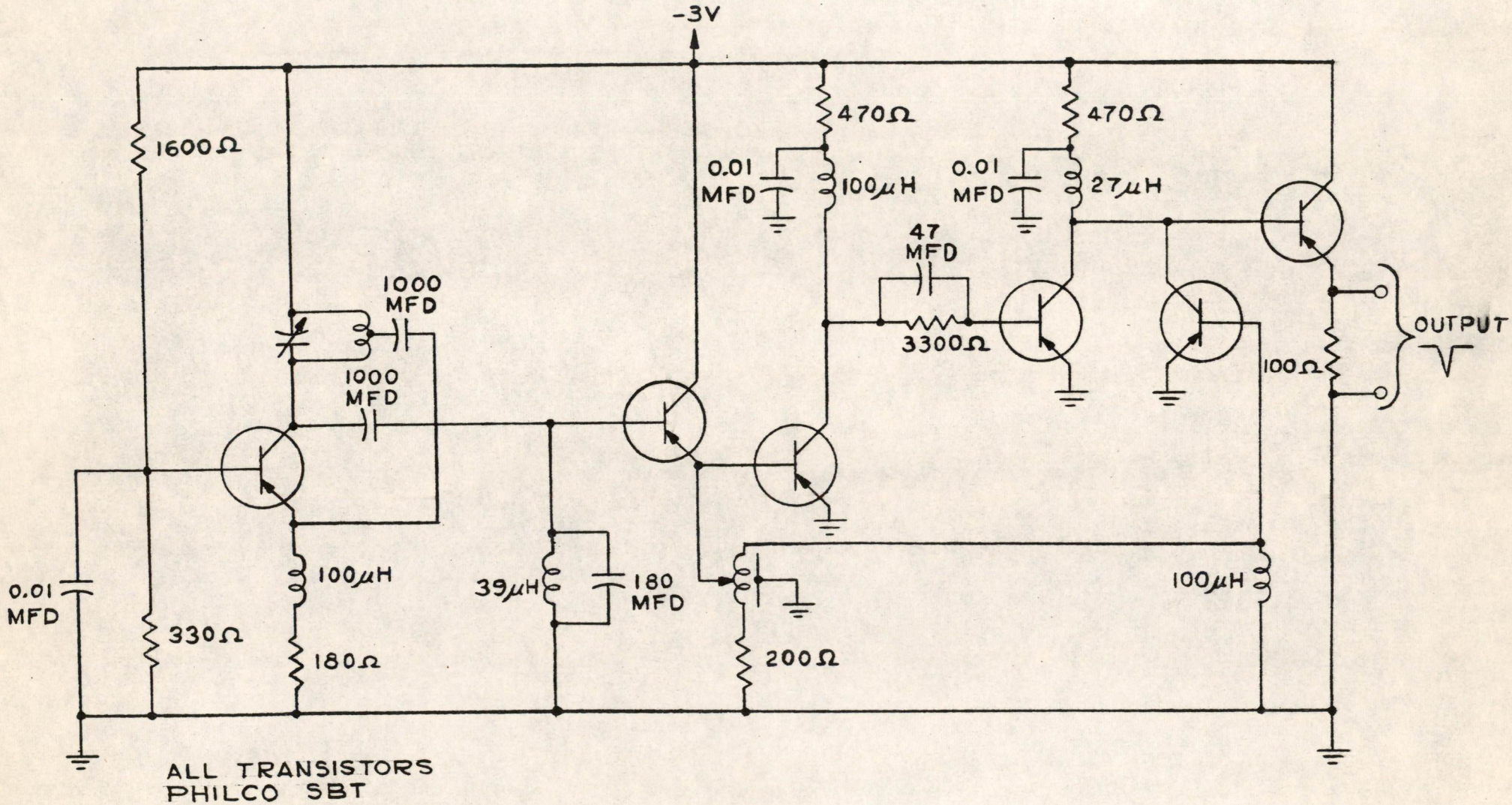


FIG. 10

PETERSEN PULSE GENERATOR

K Olsen
13-1

Memorandum 6M-4137

Division 6 – Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: MEMORY CORE HEATING BY SWITCHING AT HIGH FREQUENCIES

To: D. R. Brown

From: J. D. Childress

Date: January 31, 1956

Approved: John B. Goodenough
John B. Goodenough

Abstract: The heating of a memory core caused by high frequency switching has been studied experimentally. For a switching frequency of 400 kilocycles(the maximum frequency possible in a coincident-current two-to-one selection memory of 5 microsecond cycle time)the temperature of the memory core (DCL material) may rise more than 57°C above ambient in still air or 34°C in an oil bath. At 200 kilocycles (the maximum reasonable switching frequency in the memory) the temperature rises are 33°C and 22°C, respectively. At 30°C above ambient (25°C), the memory core fails to hold information dependably. Thus, with forced air cooling the present memory should have no problem with heating; however, memories of shorter cycle time face serious heating problems.

Distribution: The following are to receive the complete memorandum:

Best, R., B-131
Bradspies, S.
Brown, D.R.
Childress, J.D.
Davidson, G.
Ellis, D.H.
Freeman, J.R.
Goodenough, J.B.
Guditz, E. A.
Gurley, B.
Mitchell, J. L.
Menyuk, N.
Olsen, K.H.
Pacl, R.A.
Sarles, F.W.
Smith, D.O.
Zopatti, R.
Papian, W.N.

Other staff in Group 63 are to receive abstracts only.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

Introduction:

The power P in ergs per second dissipated in a memory core switching at a frequency f in cycles per second is

$$P = fx10^7 V \int_{-B_r}^{B_m} H_m dB \approx 5 \times 10^6 x\, f_u V_1 I_m \tau_s \qquad (1)$$

where V is the volume of the core in cubic centimeters, where H_m is the maximum field in oersteds, B is in gauss, ${}_uV_1$ is the output voltage signal in volts, I_m is the maximum current in amperes, and τ_s is the switch time in seconds. Thus, for a memory core switching at f = 500 kc,

$$P \approx 3 \times 10^5 \frac{\text{ergs}}{\text{seconds}} \approx 3 \times 10^{-2} \text{ watt}, \qquad (2)$$

an appreciable amount of power to be dissipated by an element the size of a memory core.

The heat energy dissipated by a memory core is a function of (1) the difference between the temperature of the core and the ambient temperature and (2) the nature of the medium into which the heat must go. Thus, as the frequency of switching is increased, the core temperature rises to effect the necessary additional dissipation.

Unfortunately, the properties of the core are dependent on the temperature. As the temperature increases, the switch time τ_s decreases and the critical field H_d (the minimum amplitude of disturb pulses which cause disturb sensitivity) decrease. When H_d becomes equal to $\frac{H_m}{2}$, the memory core fails to hold information; thus T_{no}, the maximum operating temperature for the core, is defined as the temperature at which $H_d = \frac{H_m}{2}$.

The maximum temperature T_{no} depends on the type memory scheme in which the core must operate. For a perfect memory scheme (by "perfect" is meant that the only material requirement is that it be magnetic) $T_{no} \simeq T_c$, the Curie temperature; for less ingenious schemes, the requirement on T_{no} is that it be higher than the maximum temperature a core can reach in normal memory operation.

Experimental Procedure:

The heating by high frequency switching of a core of the DCL memory core composition was measured indirectly. First the undisturbed output voltage $_uV_1$ for $I_m = 0.9$ amperes was measured as a function of temperature. Then $_uV_1$ was measured as a function of the frequency of switching. By means of the first set of data, the increase in $_uV_1$ caused by high frequency switching was translated into the equivalent change in temperature. The results are presented in Fig. 1.

Fig. 2 is a plot of field amplitude margins as a function of temperature. The upper limit on H_m is given by

$$R_{sp} = \frac{H_d}{H_m} = 0.5, \qquad (3)$$

the condition for operation in a coincident-current memory, two-to-one selection. An additional margin, $R_{sp} = 0.55$ is also shown. The lower limit is determined by the minimum field for which the switching time τ_s is

$$\tau_s = 1.25 \text{ microsecond}, \qquad (4)$$

the upper limit of τ_s in the MTC type memory. An additional limit, $\tau_s = 1.0$ microseconds, is also included.

Discussion and Conclusions:

The memory operates at the point $H_m = 1.9$ oersted and $T_o = 25^oC$ on the Operation Limits plot, Fig. 2. Thus for these conditions $T_{no} = 53^oC$; so a rise of temperature $\Delta T \approx 28^oC$ is permissible.

If the memory were operated at $H_m = 2.3$ oersteds and $T_o = -30^oC$, the maximum temperature would be $T_{no} = 25^oC$ and $\Delta T \approx 55^oC$. Thus at the expense of higher driving power to the memory and refrigeration, wider temperature limits could be obtained.

The present MTC memory is cooled by forced air circulation. The cooling of the core by forced air circulation is better than that for still air and somewhat less than for immersion in an oil bath. The cooling would depend on the air velocity. An experiment with a fan

blowing air over a core gave values almost midway between those for still air and those for oil immersion.

The maximum possible frequency at which a core in a memory of 5 microsecond cycle time could be switched is 500 kilocycles. This means that a single register is being continuously selected and at least one bit is having a ONE read out and rewritten continuously. This is a somewhat improbable occurrence -- and a useless one in terms of information handling. The reasonable occurrence is that a particular register be selected every other cycle resulting in a maximum switching frequency of 200 kilocycles.

From Fig. 1, ΔT for a core switching at 400 kilocycles is greater than 57°C in still air or 34°C in an oil bath (Dow Corning 550 Silicone Oil); for 200 kilocycles, ΔT is 33°C and 22°C, respectively. Since the maximum allowable temperature rise is about 28°C, it is evident that the memory may operate near the temperature limit but should not exceed the limit so long as the cooling system functions.

For very high-speed memories, heating is a serious problem. Two approaches suggest themselves:

(1) Increase the surface area to volume ratio of the element;

(2) Move the memory operating point to a lower temperature.

James D. Childress

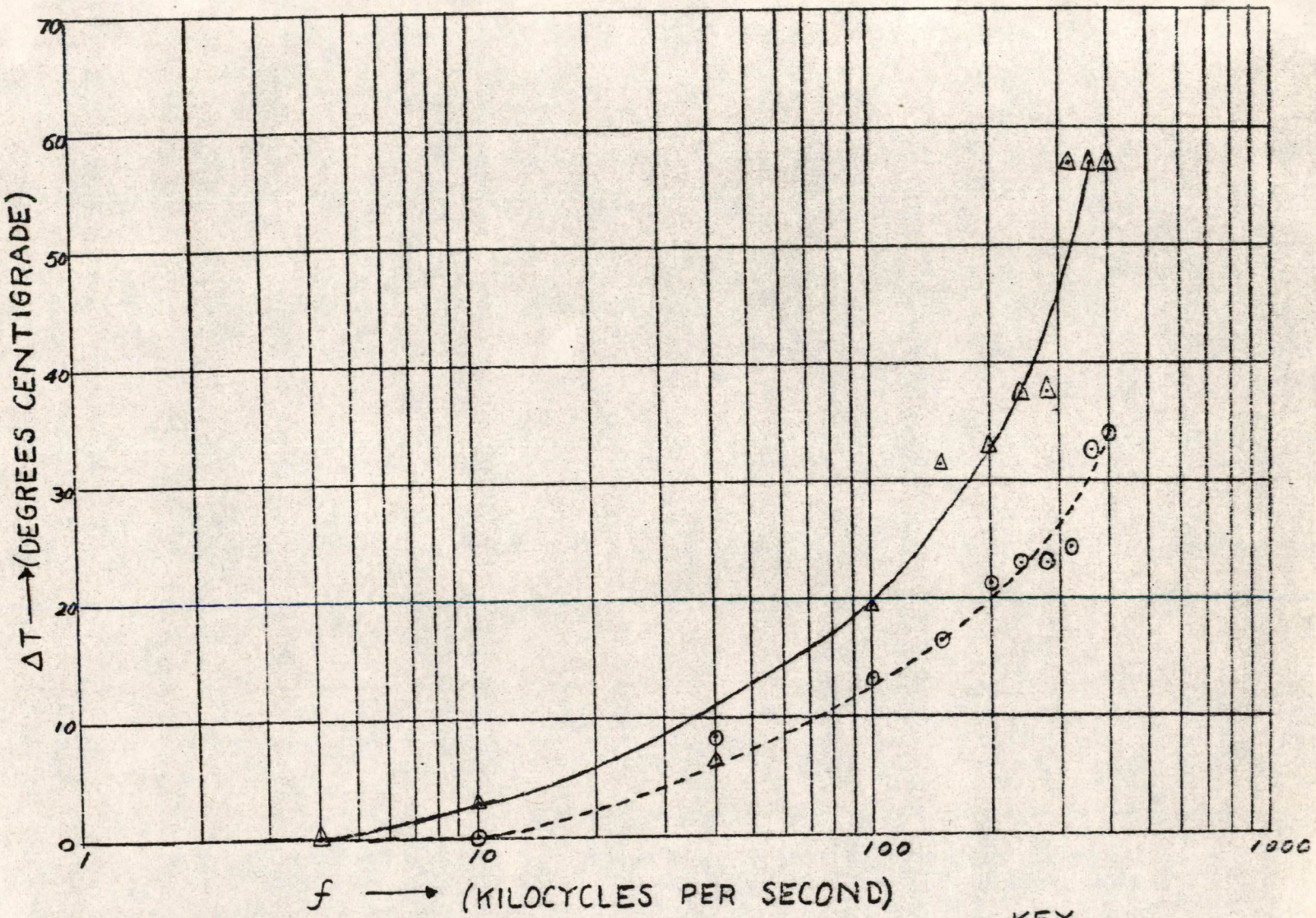
James D. Childress

JDC/md

Dwg. Numbers

SB-65079 - Figure 1
B-64423 - Figure 2

SB-65079



MEMORY CORE HEATING BY SWITCHING

CHANGE IN TEMPERATURE

VS

FREQUENCY OF SWITCHING

KEY

△ — STILL AIR

⊙ --- OIL BATH

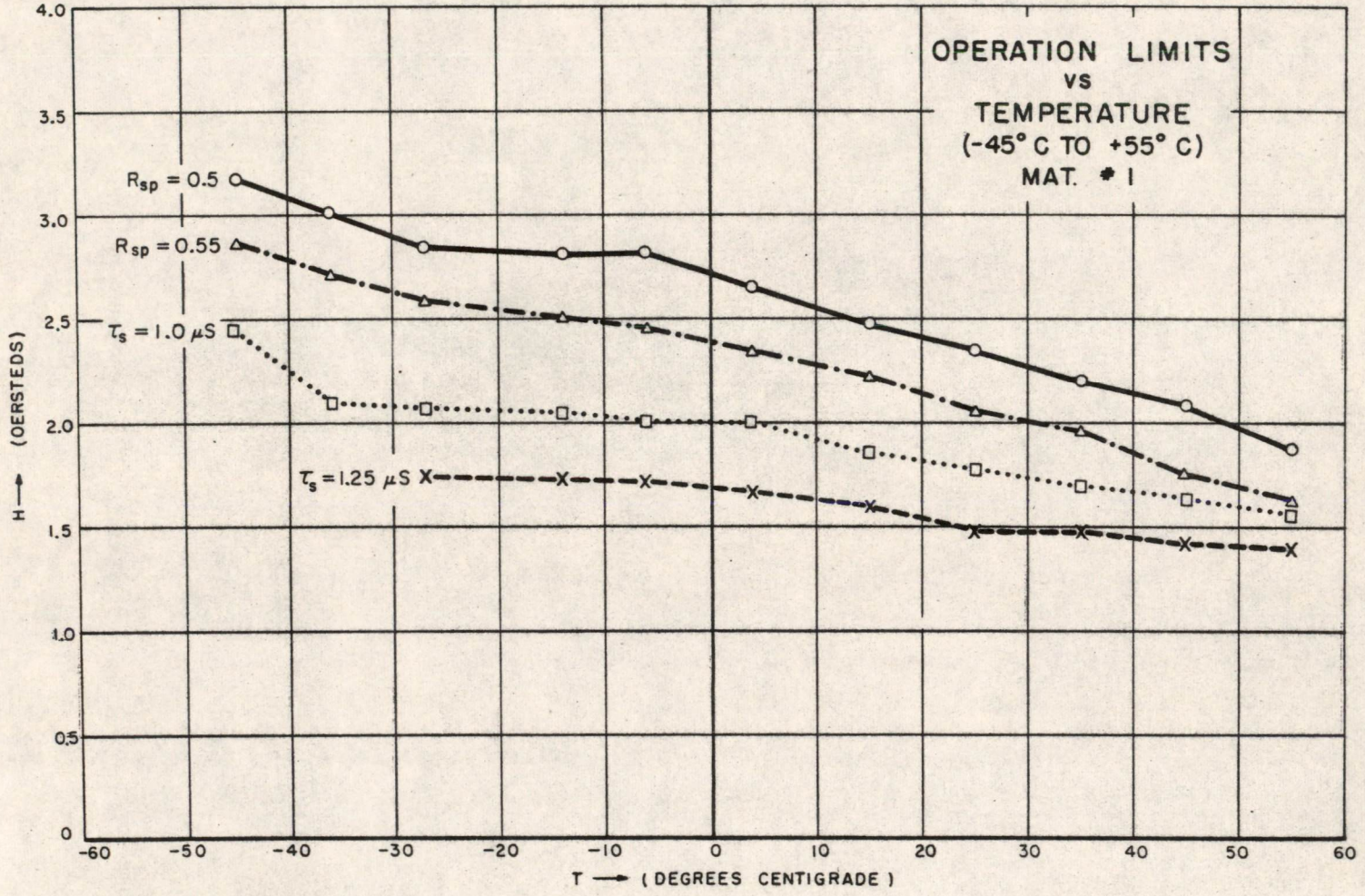
DCL MATERIAL

1-19-56 m.s.t.

BK JWC

SB-65079 ✓

B-64423


OPERATION LIMITS
vs
TEMPERATURE
(-45° C TO +55° C)
MAT. # 1
R_{sp} = 0.5
R_{sp} = 0.55
τ_s = 1.0 μS
τ_s = 1.25 μS
H ⟶ (OERSTEDS)
T ⟶ (DEGREES CENTIGRADE)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
-60
-50
-40
-30
-20
-10
0
10
20
30
40
50
60

K. H. Olsen

Kenneth H. Konkle
February 10, 1956

MASTER'S THESIS PROPOSAL

Massachusetts Institute of Technology

Department of Electrical Engineering

TITLE: HOLE STORAGE IN A SATURATED GROUND-EMITTER TRANSISTOR CIRCUIT

STATEMENT OF THE PROBLEM:

A solution for the variation with time of the distribution of minority carriers in a transistor will be determined for a saturated, RC-coupled, grounded-emitter circuit during turnoff. This solution will be broken into several phases, and the effect of circuit and transistor parameters upon the shape and duration of each phase will be determined.

HISTORY OF THE PROBLEM:

Digital computers use large numbers of vacuum tubes, in the range of 1000 to 10,000, and hence require large amounts of plate and filament power, space, and cooling. For these reasons transistors are attractive as replacements for the vacuum tubes in newer computers. As the various type transistors have been developed, each has been tried out in digital computer circuits, flip-flops, gates, and pulse amplifiers. The first transistors, the point-contact type, were experimented with but due to the difficulty of producing large numbers of similar units and to their instability, no large systems were built using them.[1] Junction transistors, which were developed next, are much more uniform and can be manufactured with good control, however, digital computer circuits using

---

1. Superscripts refer to the bibliography at the end of the proposal.

them cannot compete with vacuum tubes in many applications where speed is important.

Computer circuitry is essentially large signal circuitry wherein circuit levels take on one of two values to represent the binary numbers 0 and 1. The collector characteristics of junction transistors are divided into three regions, collector current cutoff, active, and collector current saturation regions. In the collector current cutoff region the transistor is an open circuit and in the current saturation region it acts as if it were a short circuit.[2] These two regions therefore provide built-in level clamping for computer circuitry. Due to a phenomenon called hole storage, a considerable time is required for the transistor to recover after removing the drive which has put it into the saturated region.[3] Therefore, to maintain fairly good switching times with junction transistors elaborate circuits have been developed to prevent the transistor from saturating.[4]

By allowing the transistor to enter saturation many simplifications in circuitry and computer logic may be made, since the transistor may now be treated as a relay.[5] In addition, the circuits become less critical with respect to transistor parameter and component values. With the development of the surface-barrier transistor, which has very high speed due to its small dimensions and excellent control in manufacturing due to the fabrication technique, saturating type circuits have become practical for high speed systems.[6] Other considerations rule out the use of nonsaturating circuits with surface-barrier transistors, the low voltage swings encountered in the circuits do not allow effective clamping with diodes having faster recovery than the transistors.

The original saturating switching circuits using surface-barrier transistors are direct coupled in that the collector of one circuit is connected directly to the base of the next circuit as shown in Fig. 1a.[5] This circuit requires that the emitter-collector voltage of a transistor in saturation be less than the voltage required to cause any base current to flow in the second stage which is off. This type circuit leads to a small component count and fairly good speeds. It has been found in investigations carried out at Lincoln Laboratory that by the addition of a parallel RC coupling circuit with positive bias, an improvement could be made in the tolerance of these circuits to transistor parameters and in the speed with which a saturated transistor could be turned off. The basic circuit for RC coupled switching circuits is shown in Fig. 1b.

Typical computer circuits using RC coupled saturating grounded-emitter transistors are shown in Fig. 2., where (a) is an "or" gate, (b) is an "and" gate, and (c) is a flip-flop with its associated "set" and "clear" inputs. It can easily be seen that all of these circuits are combinations of the basic circuit of Fig. 1b. A simplified unloaded equivalent to this basic circuit is shown in Fig. 3a with the mercury relay corresponding to the preceeding transistor. It is this circuit which will be evaluated with respect to hole storage in this thesis.

The phenomenon under study is similar to that which causes reverse recovery problems in point-contact and junction diodes.[7,8] The hole storage phenomenon has been investigated for junction transistors, but under different conditions, i.e., the base being an open circuit during turnoff, or the base being shorted to the emitter during turnoff.[3,9] The desired result therefore will be obtained by solving the transistor

equations for the particular boundary conditions imposed by the RC coupling circuit.

For a p-n-p transistor in current saturation, a plot of hole density, p, vs. distance through the base, x, combined with a simple equivalent circuit is shown in Fig. 3b, and that for an active transistor, in Fib. 3c. Using many simplifying assumptions, the transistor equations which relate the variables in these figures[10] can be approximated as follows.

$$I_E = \frac{1}{\gamma} I_\epsilon(p) \quad , \quad I_C = I_c(p)$$

where γ is the emitter efficiency, I_E, the emitter current density, I_C, the collector current density, I_ϵ (p), the emitter hole current density, and I_c(p), the collector hole current density. If no electric fields exist in the base, the hole current densities are:

$$I_\epsilon(p) = -q D_p \left.\frac{dp}{dx}\right|_{x=x_\epsilon} \quad , \quad I_c(p) = -q D_p \left.\frac{dp}{dx}\right|_{x=x_c}$$

where q is the charge on a hole and D_p, the diffusion constant for holes. The equation governing the hole distribution in the base reduces to

$$d^2p/dx^2 = 0$$

in the steady state if volume and surface recombination are neglected. This yields a solution for p as follows

$$p = p_\epsilon - \left[\frac{I_c}{q D_p}\right](x - x_\epsilon)$$

and gives $I_\epsilon(p) = I_c(p)$, where p_ϵ is the hole density at the emitter junction. If infinite planar junctions are assumed, on a per unit area basis

$$I_B = I_E - I_C = \left(\frac{1}{\gamma} - 1\right) I_C$$

where γ is a function of p_ϵ due to such effects as surface recombination and resistivity modulation in the base. The hole density at the junctions are also related to the junction voltages by

$$p_\epsilon = p_B\left(e^{q\Phi_\epsilon/kT} - 1\right) \quad , \quad p_c = p_B\left(e^{q\Phi_c/kT} - 1\right)$$

where p_ϵ and p_c are the hole densities at the emitter and collector junctions; Φ_ϵ and Φ_c are the emitter and collector junction voltages, and p_B is the normal hole density in the base. In the active region, Φ_c is negative and hence p_c is approximately zero. From I_c we can find p_ϵ, from which we obtain γ, then I_B. However in the saturated region, I_B and I_c are determined by external circuit conditions. From them we can find a value for γ, and hence p_ϵ and from it p_c. In this case, p_c is not zero as shown in Fig. 3a. As a result of this, Φ_c is positive which accounts for the low voltage across the transistor in saturation.

In the turnoff period it is obvious that the collector junction voltage cannot go negative into the active region until p_c has been reduced to zero. Therefore the switching time is largely dependent on the speed with which the hole density at the collector junction can be reduced to zero. During turnoff, as always, $I_E = I_c + I_B$, hence if we can cause reverse base current to flow, the value of $I_\epsilon(p)$ will be reduced. In fact, if I_B can be made more negative than I_c, holes will

be removed through the emitter junction in addition to those leaving through the collector. At present, only qualitative hole density distributions can be given for the circuit of Fig. 3a, however, typical base and collector waveshapes are shown in Fig. 4 for the listed circuit parameters. A break in the active region rise will be noted for those waveshapes obtained with small C_B. The cause of this break is not known at present but it will be investigated in the course of this thesis.

PROPOSED PROCEDURE:

All of the equations previously quoted are obtained through the use of a large number of questionable assumptions. Such affects as surface and volume recombination, variation in emitter efficiency, electric fields in the base region, or others, may be responsible for the hole storage recovery as observed in Fig. 4. Observations will be made using simpler turnoff conditions such as open base or constant reverse base current, and from these observations a mathematical model incorporating the pertinent effects will be developed. A solution for the hole density and collector waveshape will be determined which is valid for the various phases of the waveshape and for various combinations of transistor and circuit parameters which are met in typical surface-barrier saturating RC-coupled switching circuits.

EQUIPMENT NEEDED:

All test equipment and material will be supplied by Lincoln Laboratory.

ESTIMATED DIVISION OF TIME:

Preparation of the proposal	50
Further study of the literature	50
Experimental work and analysis	150
Correlation of results and formulation of deductions and conclusions	100
Preparation of the thesis report	100
TOTAL	450

Signed: Kenneth H. Konkle
Kenneth H. Konkle

Date: February 10, 1956

SUPERVISION AGREEMENT:

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

Approved: R. B. Adler
Richard B. Adler
Associate Professor of
Electrical Engineering

KK/js

Attached Drawings: Figure 1 - A-65355
Figure 2 - A-65356
Figure 3 - A-65357
Figure 4 - A-65358

Distribution List: Group 63 Staff
Building 10 Staff
Adler, Richard B., 20A-118
Linvill, William K., 10-318

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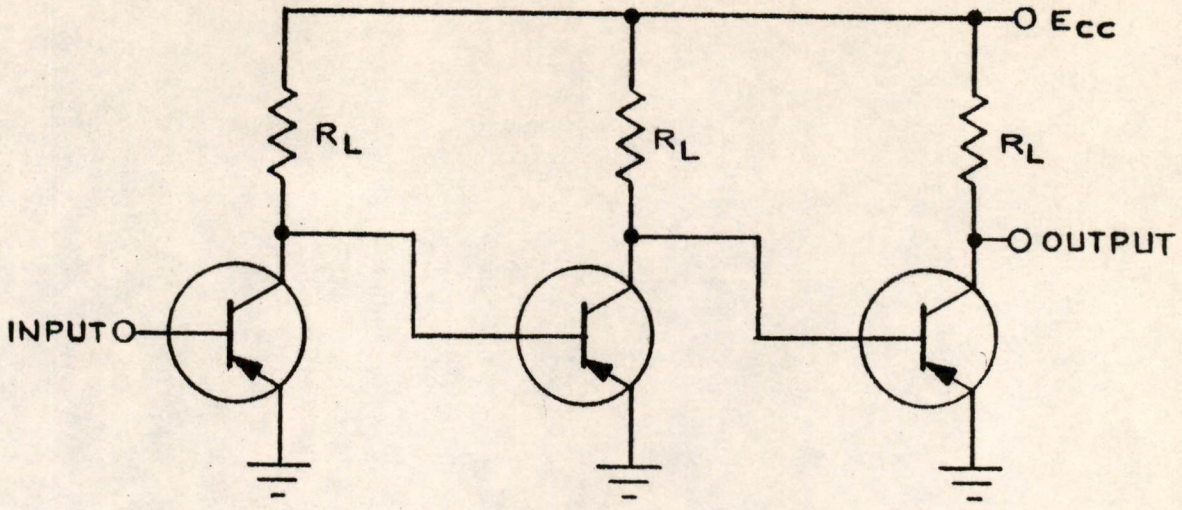


FIG. 1(a)
BASIC DIRECT COUPLED SWITCHING CIRCUIT

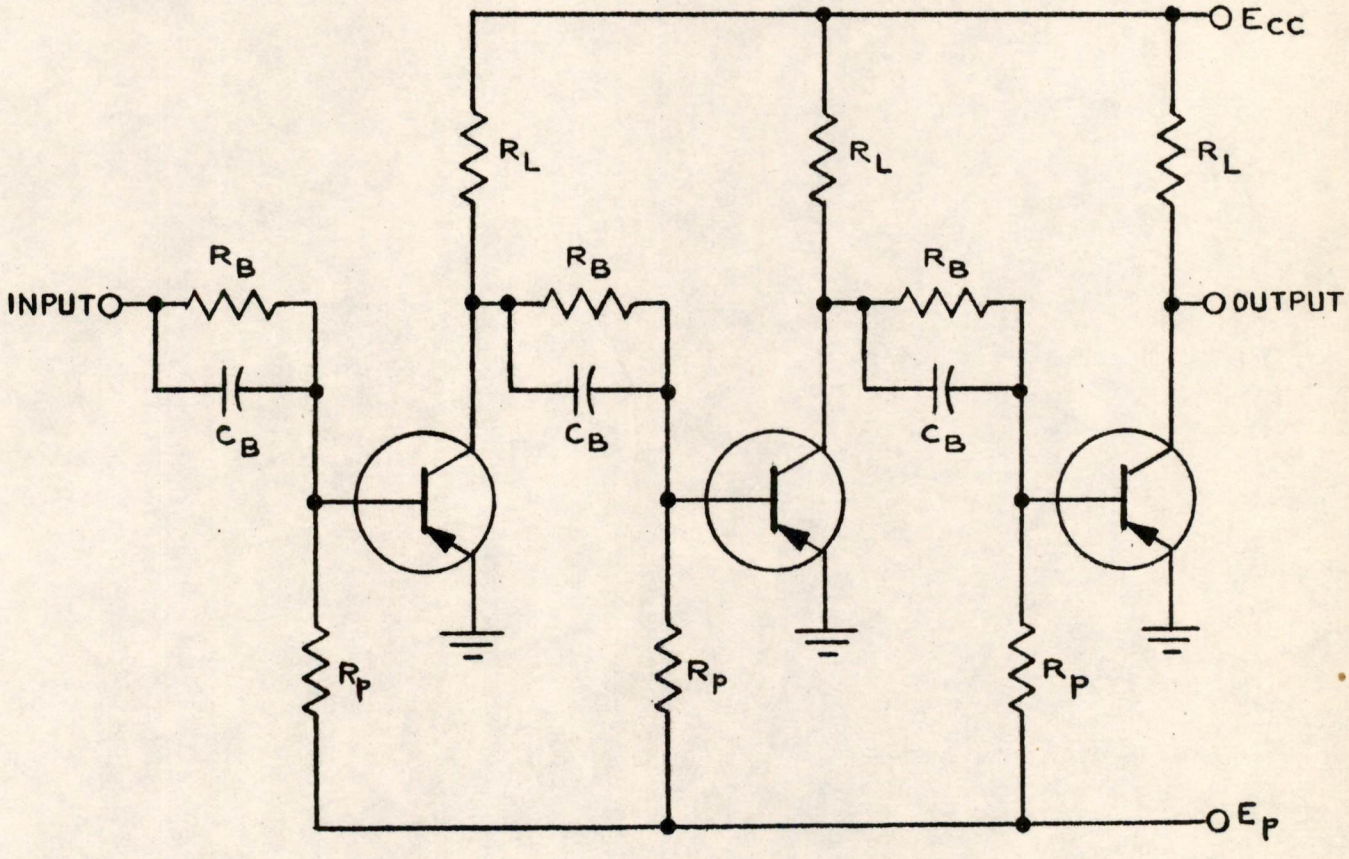


FIG 1(b)
BASIC RC – COUPLED SWITCHING CIRCUITS

A-65355

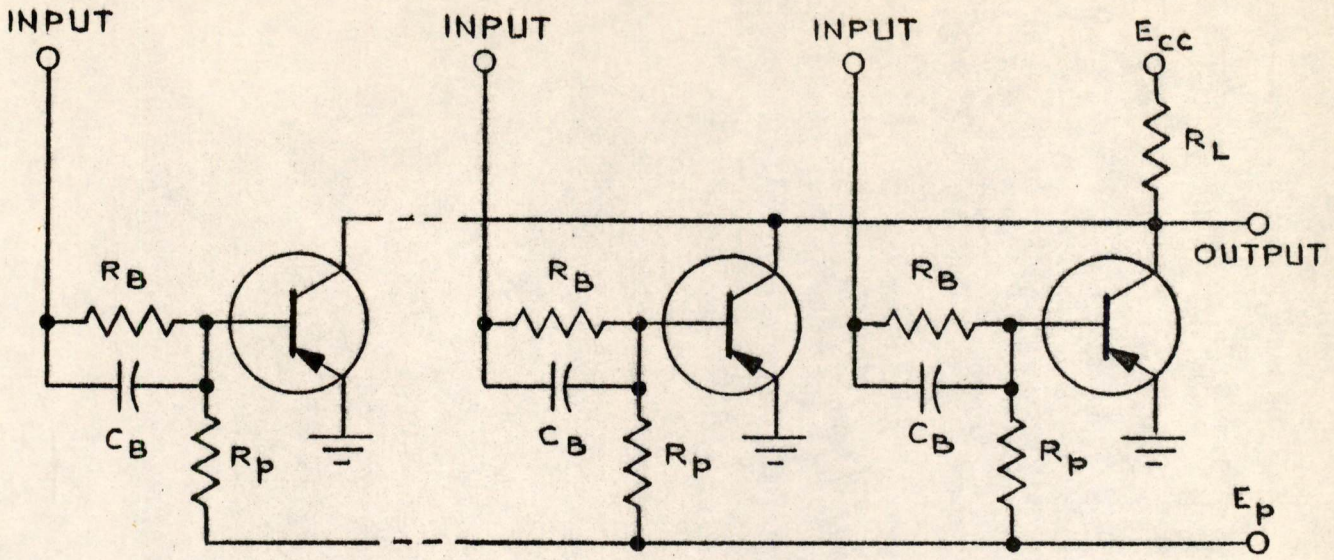


FIG. 2(a)
"OR" CIRCUIT

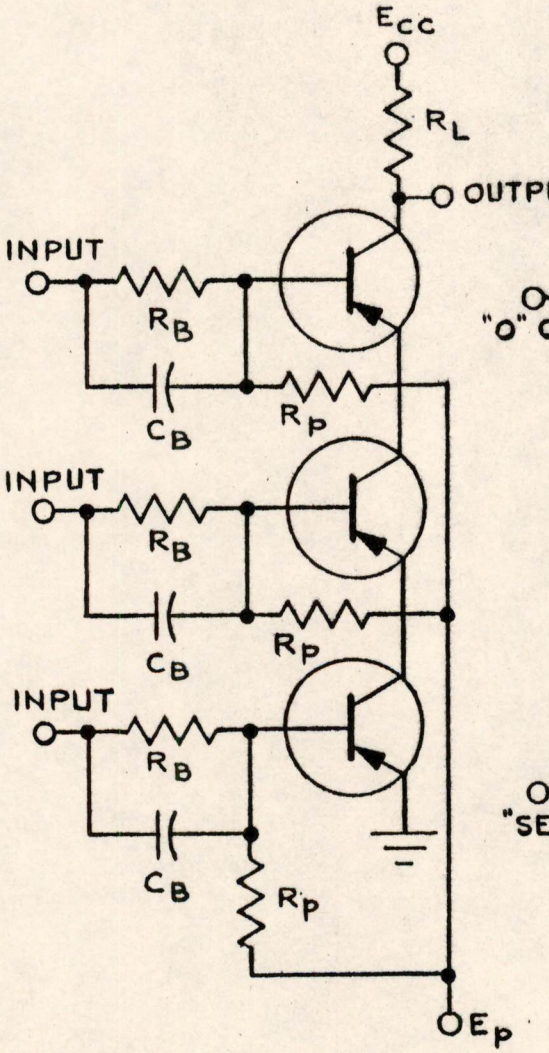


FIG. 2(b)
"AND" CIRCUIT

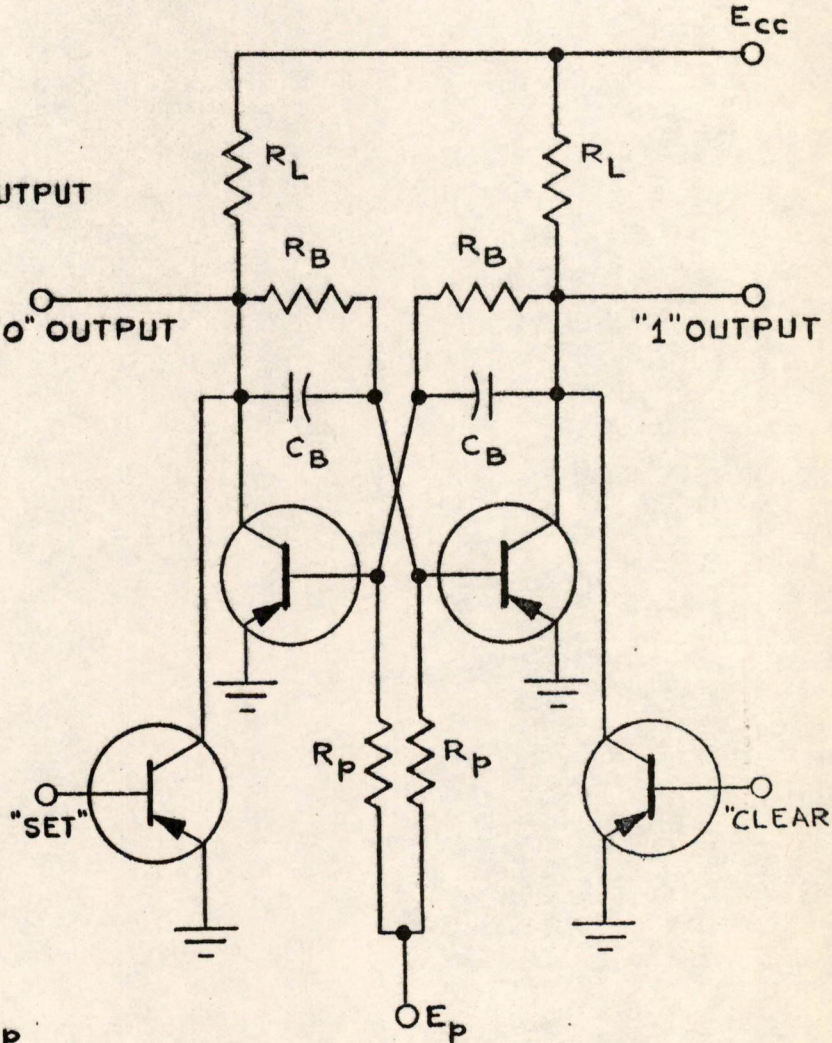


FIG. 2(c)
FLIP-FLOP WITH
SET AND CLEAR INPUTS

A-65356

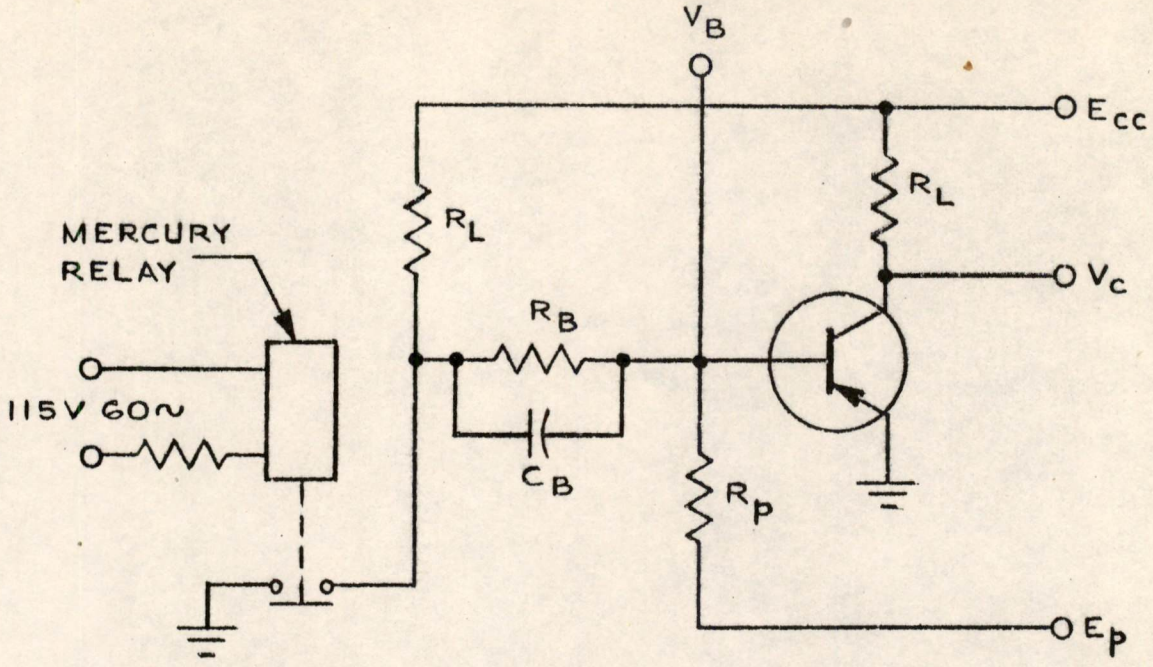


FIG. 3(a)
CIRCUIT UNDER TEST

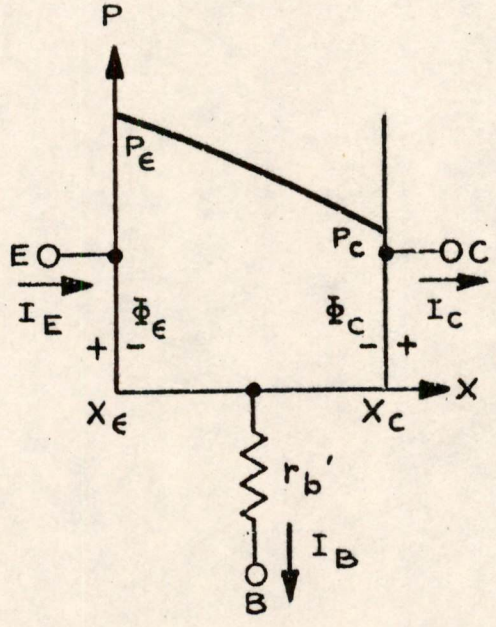


FIG. 3(b)
HOLE DENSITY FOR
A SATURATED TRANSISTOR

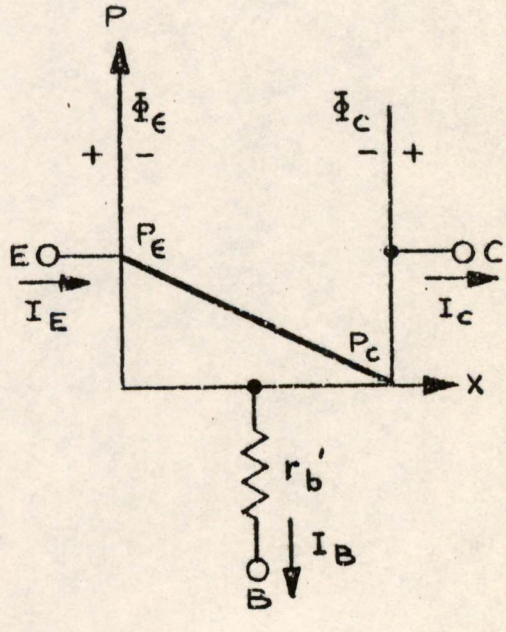
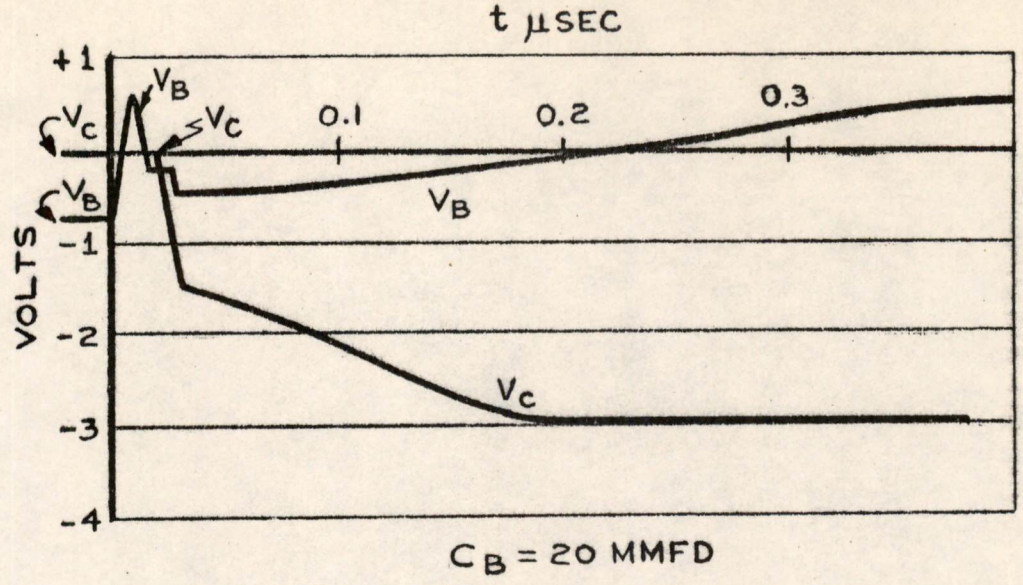
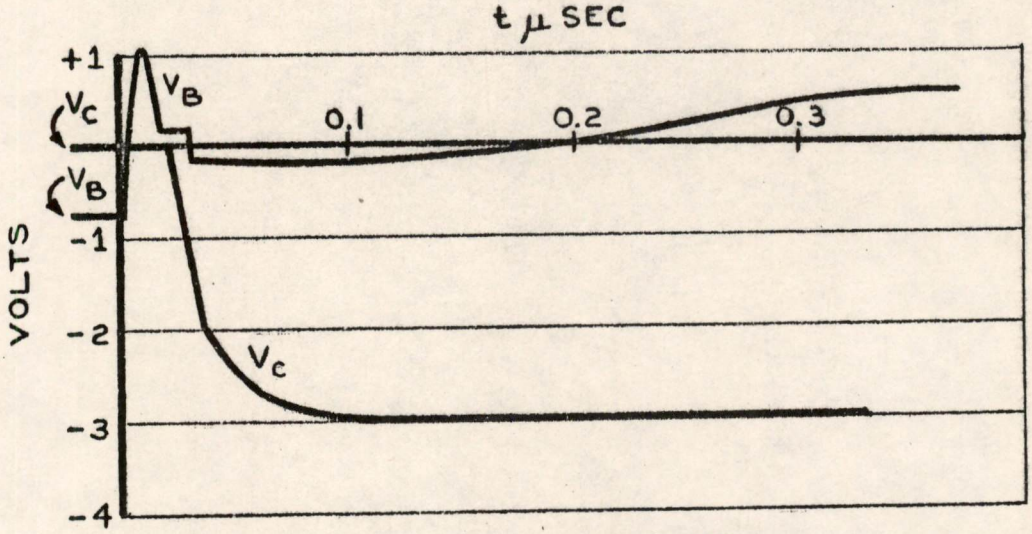


FIG. 3(c)
HOLE DENSITY FOR
AN ACTIVE TRANSISTOR

A-65357



C_B = 20 MMFD



C_B = 30 MMFD

E_{CC} = -3.0 VOLTS

E_p = +10 VOLTS

R_B = 2.2 K

R_p = 180 K

PHILCO SB-100 SURFACE BARRIER TRANSISTOR

FIG. 4
BASE AND COLLECTOR WAVEFORMS

A-65358