SHIMA

R.T. KIKOSHIMA

#16

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Standard Figuring Book

No. 1602½

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Made in U. S. A.

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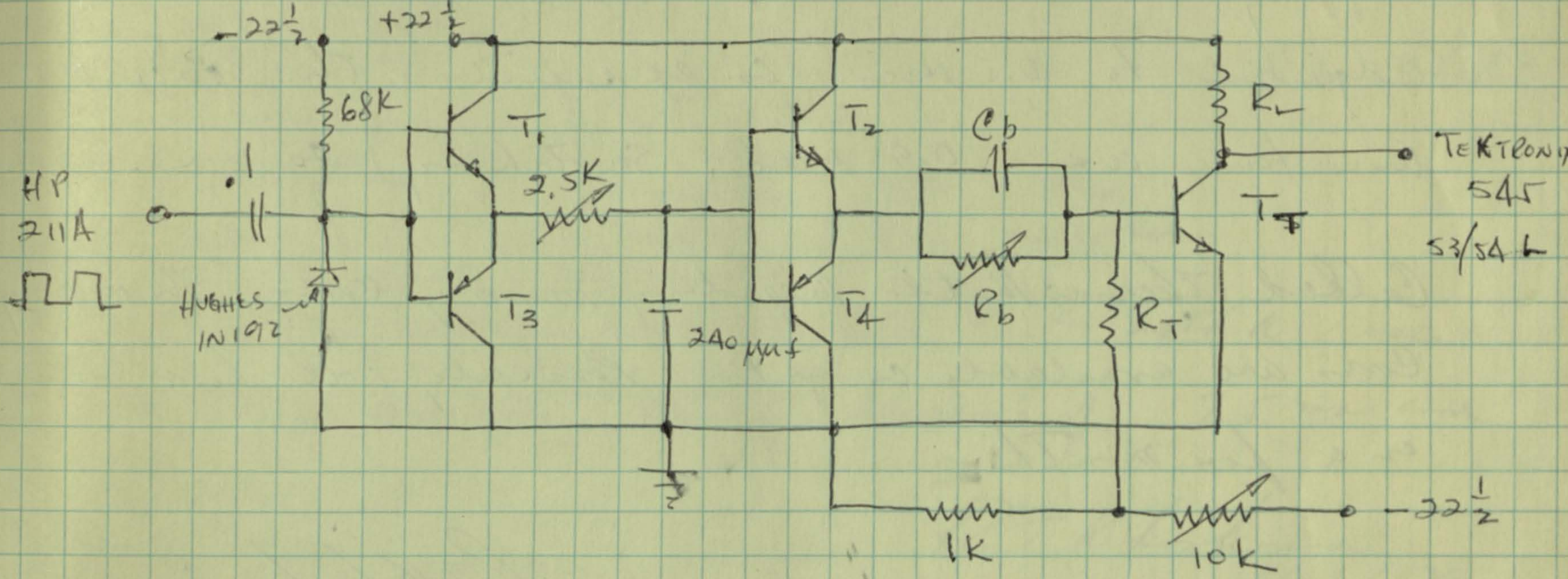
5/21/58

Connected circuit as shown in accordance with IBM Spec. No 557-0009 (4/11/58)



T1, T2 — 85-1, 85-2

T3, T4 — GT 1N317

T7 — 85-3

Rb — 1K POT

RL — 1K

Cb - variable -

"Critical coupling" could not be obtained with the values of Rb, Cb used.

R T Kikoshima

5/21/58

5/22/58

Increased C_B (Fig on P. 1) to .004 μf. and "critical coupling" was obtained. With the rise time adjusted to 0.5 μsec as specified, the output rise time was 0.9 μsec, switching 20 ma.

Called Thermo Mat'ls regarding memory cores. No memory cores are available as yet. Possibly will have some in a few month

R T Klinkenberg [illegible] 5/22/58

5/23/58

Continued work on IBM Test. Obtained the following data for two transistors

Transistor	β	R_L	t_r	R_B	C_B	τ_B
85-3 (1ma)	26	20k.	2.3 μsec	761.5 Ω	.01204 μf	9.16 μsec
85-3 (30 ma)	36	1K	0.9	318.5	.004165 μf	1.33 μsec
85-7 (1ma)	26	20K	1.4	977.9	.01204 μf	11.8 μsec
85-7 (30 ma)	36	1K	0.65	425.2	.004165 μf	1.77 μsec

V_{CC} = 22½ volts t_r in = 0.5 μsec

V_0 = 20 V

5/23/58
(Cont.)

Received some sample Int'l Telemeter cores from Jeff McKnight (Rep.) 50 T2 and 80 T5.

Quote on 10 x 10 matrix of 80 T5 is $70, (x, y, inhibit and sense.)

50 mil cores } $0.30 tested
80 mil cores } 0.20 untested.

VG suggested repeating IBM test with a rise time of 0.1 μsec and current of 7.5 ma and 150 ma.

RT Kirkorian
5/23/58

5/26/58

Calculated f_α' and C_c' from the data on page 2 using the equations in the spec:

$$f_\alpha' = \frac{\alpha_{cbo_1}\left(\frac{R_{L1}}{R_{L2}} - 1\right)}{2\pi\left[\frac{R_{L1}}{R_{L2}}\left(\frac{\alpha_{cbo_1}}{\alpha_{cbo_2}}\right)\tau_{b_2} - \tau_{b_1}\right]}$$

(Using this data) ◁—

$$C_c' = \frac{\tau_{b_1} - \frac{\alpha_{cbo_1}}{\alpha_{cbo_2}}\tau_{b_2}}{\alpha_{cbo_1}\frac{V_{cc}}{V_0}\left(R_{L1} - R_{L2}\right)}$$

Transistor	f_α'	C_c'
85-3	7.8 mc	14.7 μμf
85-7	5.3 mc	17.1 μμf

5/26/58 (Cont.)

Checked out the Mercury Relay Core Driver. It is ready to test cores.

R.T. Kikoshima 5/26/58

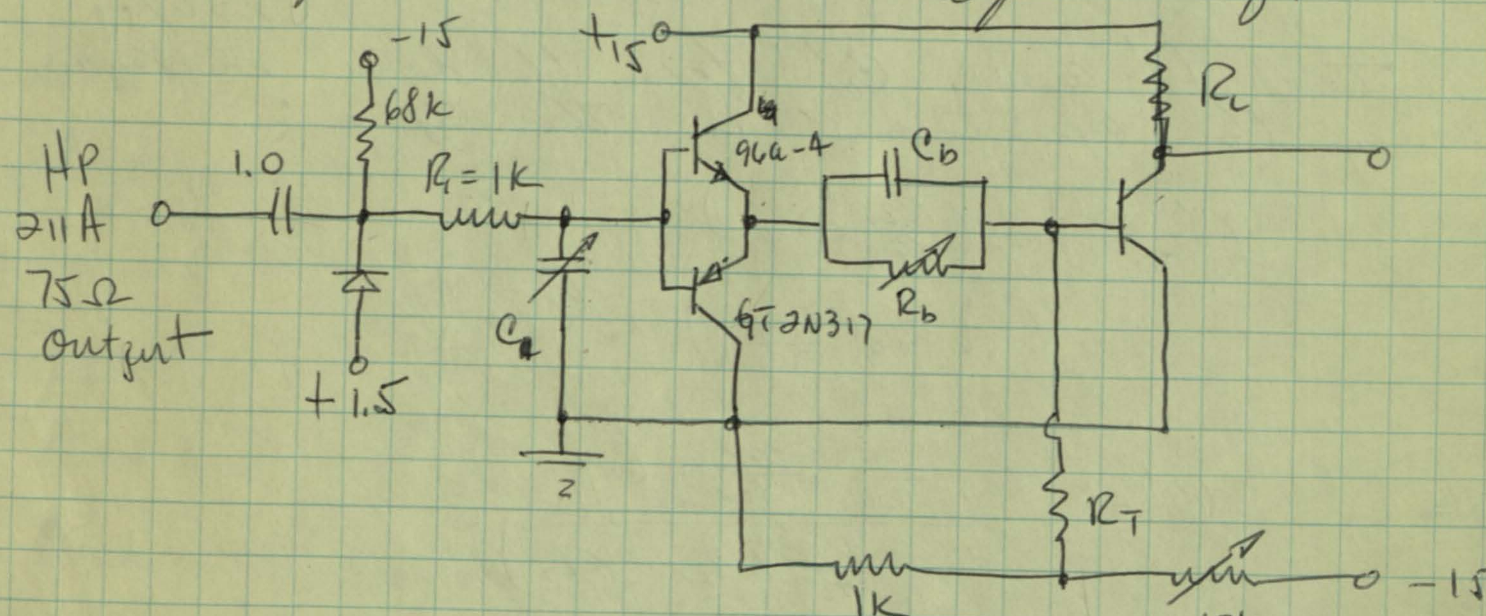
5/27/58

Worked on the IBM test circuit.

R.T. Kikoshima 5/27/58

5/28/58

Changed test circuit to the following:



R_T = 10K

Took the following data →

5/28/58 Cont

TRANSISTOR	R_L	β	t_r	R_b	C_b	$\tau = R_b C_b$
85-3	2k	38	0.6	460	4165 μμf	1.92 μsec
	100	26	0.11	250	986	0.246
85-2	2k	36	0.2	240	4165	1.0
	100	26	0.11	230	986	0.226
85-7	2k	36	0.2	510	4165	2.12
	100	26	0.1	260	986	0.256
from Gordon: 104-54	2k	48	0.5	450	4165	1.87
	100	36	0.12	250	986	0.246
104-41	2k	32	0.4	270	4165	1.12
	100	26	0.12	150	986	0.148
104-40	2k	44	0.3	400	4165	1.66
	100	42	0.12	190	986	0.187

$V_{cc} = 22\frac{1}{2}$ $\qquad I_1 = 7.5$ ma

$V_0 = 15$ V $\qquad I_2 = 150$ ma.

t_r in = 0.1 μsec

R.T. Ukoshena 5/28/58

5/29/58

Calculated f_α' & C_c' from above data

TRANSISTOR	f_α'	C_c'
85-3	27 mc	14.4 μμf
85-2	20.7	6.7
85-7	21.8	17.3
104-54	33.	11.2
104-41	41.	10.3
104-40	65.6	11.6

5/29/58 (Cont.)

Will rerun the test with an $R_c = 40\ \Omega$ for 150 ma and $V_{cc} = 8-12$ volts and a rise time as short as possible.

R.T. Kikoshima 5/29/58

6/2/58

~~Re~~built new test chassis as shown in Page 4.

R.T. Kikoshima 6/2/58

6/3/58

Reran IBM test on new box (chassis)

TRANSISTOR	R_L	β(ac)	t_r	R_b	C_b	$\tau = R_b C_b$
85-6	780	45	150	460	4165	1.92
	39	30	30	260	986	0.256
85-2	780	34	140	400	4165	1.67
	39	24	30	220	986	0.217
85-7	780	38	150	420	4165	1.75
	39	26	30	215	986	0.212
104-54	780	45	450	310	4165	1.29
	39	32	90	300	986	0.296
104-41	780	32	350	170	4165	0.71
	39	24	50	230	986	0.227
104-40	780	37	250	270	4165	1.13
	39	36	40	160	986	0.157

$V_0 = 6V$ $\quad t_r(in) = 30$ mμsec

$V_{ce} = 8V$

R.T. Kikoshima 6/3/58

6/~~3~~ 4/58

Calculated f_α' and C_c' from the data on P. 6.

Transistor	f_α'	C_c'
85-6	23.6 mc	34.8 μμf
85-2	23.	40.7
85-7	25.9	38.3
104-54	19.3	19.5
104-41	18.2	13.
104-40	53.5	26.5

Ran the test for 85-6 with V_{cc} = 8, 9, 10, 11, 12 volts

Transistor	V_{cc}	R_b (150ma)	C_b (150ma)	R_b (7.5ma)	C_b (7.5ma)	τ_{b2}	τ_{b1}	f_α'	C_c'
85-6	8 V	275	986	510	4165	0.271	2.12	23.8 mc	38.5 μμf
	9	260	"	460	"	0.256	1.91	23.5	30.6
	10	250	"	440	"	0.246	1.83	24.5	26.2
	11	250	"	430	"	0.246	1.75	24.1	22.5
	12	250	"	405	"	0.246	1.67	23.8	19.5

$V_0 = 6V$

$t_r(in) = 30$ mμsec.

$$f_\alpha' = \frac{136}{30\tau_{b2} - \tau_{b1}}, \quad C_c' = \frac{\tau_{b1} - 1.5\tau_{b2}}{5560\, V_{cc}} \qquad \text{85-6}$$

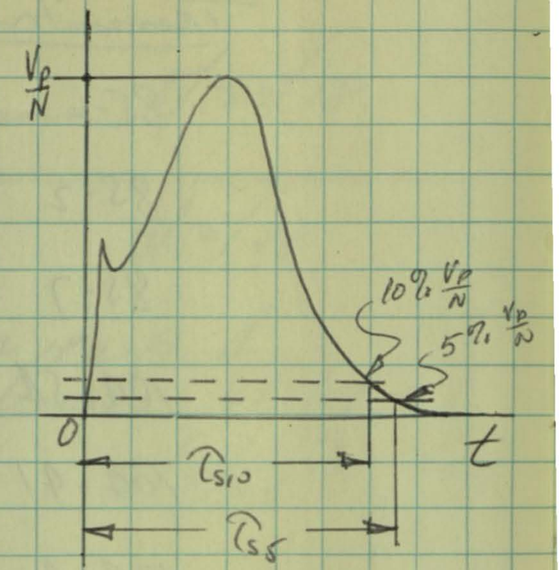
R.T. Kikushima 6/4/58

6/5/58

Took characteristics on 4 - #80T5 cores.

Reset $NI \simeq 3AT$

Core	$\frac{V_p}{N}$	$\tau_{s,10}$	τ_{s5}	τ_p	NI
1	—	—	—	—	275 MAT
2	—	—	—	—	
3	—	—	—	—	
4	—	—	—	—	
1	—	—	—	—	300 MAT
2	3 mv	40 μsec	40 μsec	14 μsec	
3	—	—	—	—	
4	1 mv	50	50	18	
1	—	—	—	—	320
2	3.5	40	40	9	
3	3	40	40	14	
4	2	40	40	13	
1	3	35	35	11	340
2	5.5	40	40	6.2	
3	6.	35	35	8.7	
4	4.	40	40	8.5	
1	5.5	30	40	6.0	360
2	7.5	30	35	4.7	
3	9.	25	30	5.3	
4	6.	30	30	5.8	
1	9.	25	30	3.8	380
2	10.5	18	20	3.6	
3	11.	20	24	4.0	
4	9.	20	23	4.3	
1	11.5	17	20	3.0	400
2	13.5	16	18	3.0	
3	14.5	16	18	3.2	
4	11.5	17.5	20	3.3	
1	15.5	13.4	16.	2.3	420
2	17.0	12	14.	2.5	
3	17.5	12	13.7	2.7	
4	15.0	13.4	15.8	2.9	
1	20	10.8	13.7	1.9	440
2	20	9.9	11.0	2.1	
3	22	9.9	10.6	2.3	
4	19	11.3	12.8	2.5	



6/5/58 (cont)

Core	V_p/N	$\tau_{s,10}$	τ_{s5}	τ_p	NI
1	25.5 mv/T	8.9 μsec	10.3 μsec	1.55 μsec	460 mAT
2	24.0	8.1	8.7	1.9	
3	27.0	7.6	8.5	2.0	
4	23.0	8.9	9.9	2.1	
1	30.0	7.1	8.5	1.4	480
2	29.0	6.8	7.8	1.65	
3	32.0	6.5	7.1	1.7	
4	27.0	7.3	8.1	1.85	
1	36.0	5.7	6.8	1.2	500
2	34.0	5.7	6.6	1.5	
3	38.0	5.5	6.3	1.5	
4	33.0	6.0	6.9	1.65	
1	42.0	4.6	5.6	1.2	520
2	39.0	5.0	5.7	1.4	
3	42.0	4.7	5.3	1.4	
4	37.0	5.5	6.0	1.5	
1	50	3.5	4.6	1.0	540
2	44	4.3	5.0	1.2	
3	48	4.2	4.5	1.3	
4	43	4.5	5.1	1.3	
1	66	2.9	3.3	0.83	580
2	56	3.3	3.7	1.05	
3	62	3.15	3.6	1.05	
4	55	3.4	3.9	1.1	
1	58	3.3	3.9	0.87	~~600~~ 560
– 2	50	3.8	4.25	1.15	
3	56	3.5	4.0	1.15	
4	48	4.0	4.5	1.25	
1	75	2.4	2.85	0.78	600
2	64	3.0	3.45	0.93	
3	70	2.8	3.1	0.92	
4	62	3.0	3.5	1.0	
1	143	1.25	1.45	0.45	800
2	115	1.56	1.76	0.56	
3	125	1.50	1.70	0.56	
4	115	1.58	1.8	0.58	

 6/5/58 cont.

Core 3 is average for the 4 cores tested. Will plot $\frac{1}{\tau_s}$, $\frac{1}{\tau_p}$, $\frac{V_p}{N}$, for core #3 from the preceding data.

NI	$\tau_{s_{10}}$	τ_{s_5} ~~T_{s_5}~~	τ_p	$\frac{V_p}{N}$	$\frac{1}{\tau_{s10}}$	$\frac{1}{\tau_{s5}}$	$\frac{1}{\tau_p}$
275 mAT	~	—	—	—			
300	~~40 μsec~~	~~40 μsec~~	~~14 μsec~~	~~2 mv/T~~			
320	40 μsec	40 μsec	14 μsec	3 mv/T	.0250 μsec^{-1}	.0250 μsec^{-1}	0.0714 μsec^{-1}
340	35	35	8.2	6	.0286	.0286	.122
360	25	30	5.3	9	~~.0333~~ .0400	.0333	.189
380	20	24	4.0	11.	~~.0417~~ .0500	.0417	.250
400	16	18	3.2	14.5	~~.0556~~ .0625	.0556	.312
420	12	13.7	2.7	17.5	~~.0730~~ .0833	.0730	.370
440	9.9	10.6	2.3	22.	~~.0943~~ .101	.0943	.435
460	7.6	8.5	2.0	27.0	0.132	.118	.500
480	6.5	7.1	1.7	32.0	0.154	.141	.588
500	5.5	6.3	1.5	38.0	0.182	.159	.667
520	4.7	5.3	~~5.3~~ 1.4	42.	0.213	.189	.714
540	4.2	4.5	1.3	48.	0.238	.222	.770
560	3.5	4.0	1.15	56	0.286	.250	.870
580	3.15	3.6	1.05	62	0.317	.278	.951
600	2.8	3.1	0.92	70	0.357	.322	1.09
800	1.5	1.7	0.56	~~125~~ 140 ok	0.666	.589	1.79

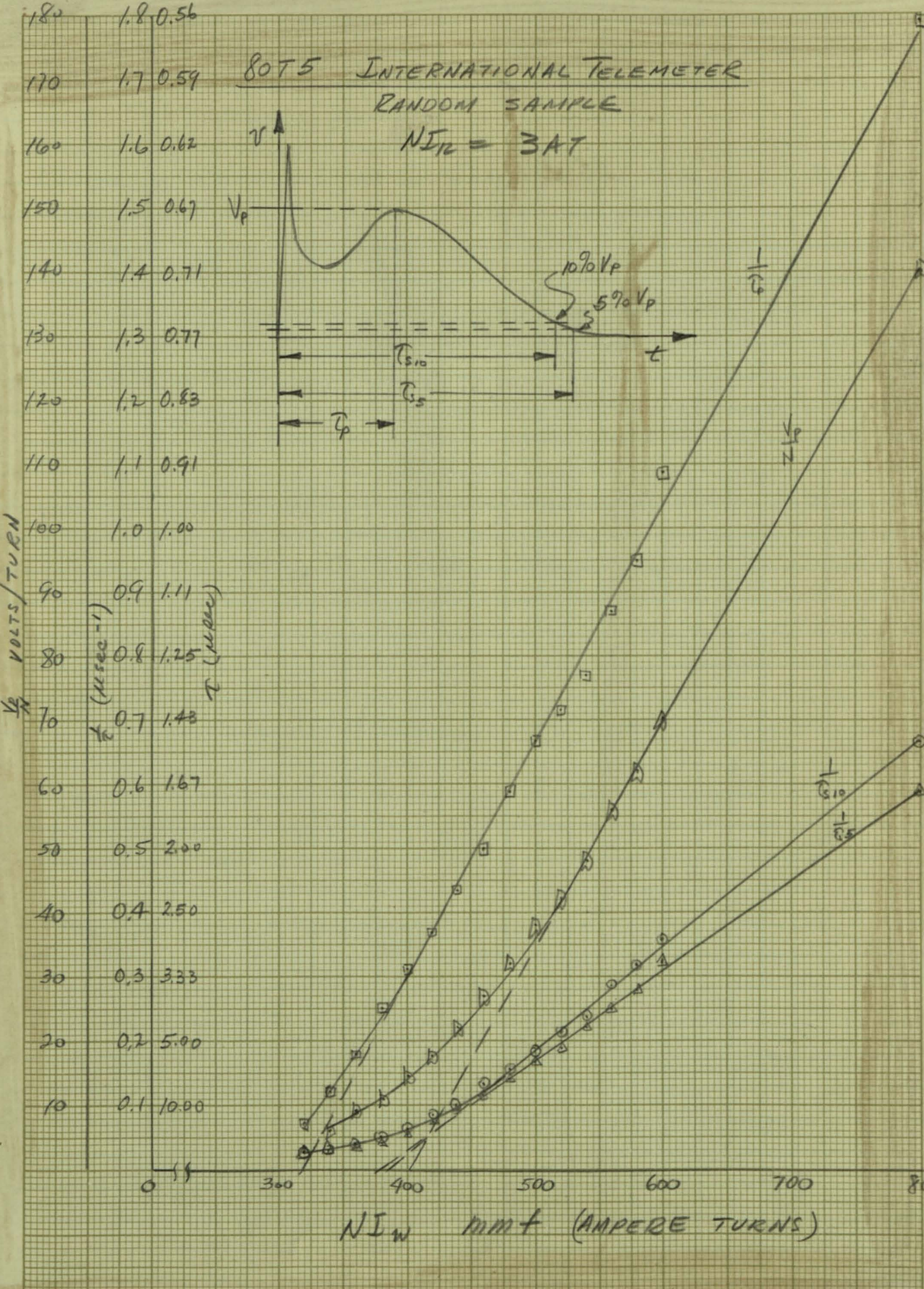
R T Kikoshima 6/5/58

6/6/58

Plotted the above data →

The curves indicate too high a value of full select current for our transistors. Called Jeff McKnight about 50T5 cores — They have no samples available.

Ray T Kikoshima
6/6/58



R T Kikoshima
6/6/58

6/9/58

Measured the linear (saturated) inductance of the core (80 T5).

Measured: $\frac{di}{dt} = \frac{200 \text{ ma}}{6 \text{ m}\mu\text{sec}}$

$L\frac{di}{dt} = 250 \text{ mV}$

$$L = \frac{(250 \text{ mv})(6 \text{ m}\mu\text{sec})}{200 \text{ ma}} = 7.5 \times 10^{-9} \frac{\text{Webers}}{\text{amp}}$$

$$= 7.5 \text{ m}\mu\text{henrys}$$

Since measured rise times were scope limited, measurements should be taken again. Also, air coupling should be minimized.

Geo Allen measured the DC β for the transistors tested on pages 6, 7.

transistor	β (dc) 7.5ma @ 10V	β (dc) 150ma @ 10V
85-6	45	37.5
85-2	30	30.0
85-7	33	32.0
104-54	41.5	41.0
104-41	35.0	33.5
104-40	30.0	38.0

Use the DC β in the calculations for f_α' and C_c'

Phoned Wm J Purdy Co., reps for Ferroxcube ~~regd~~ for info on their M3 core. They will mail information

6/9/58 Cont.

Picked up 4 - General Ceramics F 394 - 53
4 - " " F 426 - 53

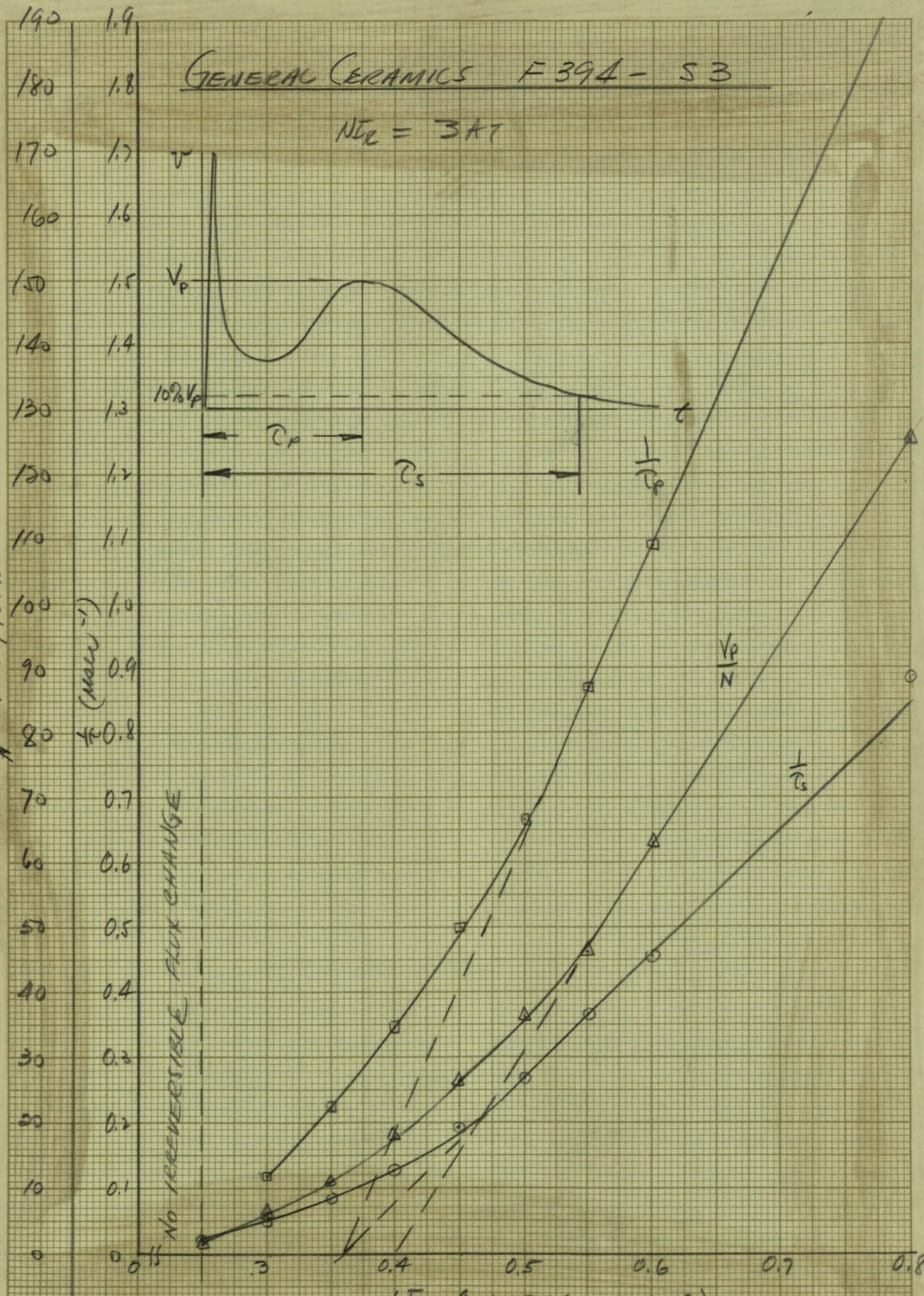
from Geo Owens, IBM San Jose.

R.T. Kikoshima 6/9/58

Tested 2 - F394 - 53 Cores.

General Ceramics F 394 - 53 Reset NI ≈ 3 AT.

NI	Core	V_p	τ_p	$\tau_{s_{10}}$	$\frac{1}{\tau_p}$	$\frac{1}{\tau_{s_{10}}}$
230 maT	1	—	~	~	~	~
	2	—	—	—	-	~
250 maT	1	1.5 mv	?	40 μsec	—	0.025 μsec⁻¹
	2	1.5		50	—	0.02
300 maT.	1	6.5 mv	8.5 μsec	22	0.118 μsec⁻¹	0.045
	2	6 mv	8.5	20 μsec	0.118	0.050
350 maT	1	10 mv	4.5	13	0.222	0.077
	2	11 mv	4.5	12	0.222	0.083
400	1	16.5	2.8	8.5	0.357	0.118
	2	18 mv	2.9	8	0.345	0.125
450	1	24	1.9	5.5	0.526	0.182
	2	26	2.0	5.2	0.500	0.192
500	1	34	1.45	3.9	0.690	0.256
	2	36	1.5	3.7	0.667	0.270
550	1	44	1.1	3.0	0.910	0.333
	2	46	1.15	2.75	0.870	0.364
600	1	58	0.90	2.3	1.11	0.435
	2	63	0.92	~~1.15~~ 2.2	1.09	0.455
800	1	120	0.48	1.16	2.08	0.862
	2	125	0.50	1.13	2.00	0.885



R T Kikorian
6/10/58

6/10/58 (Cont)

Measured L(Sat) for the General Ceramics F396-S3

$$\frac{di}{dt} = \frac{200\,ma}{6\,m\mu sec}$$

$$L_s \frac{di}{dt} \simeq 200\,mv$$

$$L_{sat} = \frac{200\,mv\ 6\,m\mu sec}{200\,ma} = 6\ m\mu henry/turn^2$$

Phoned Bob Allen of Cochrane + Barron, San Mateo, Rep. for General Ceramics.

Quoted: 10 x 10 $ 2.50
F394-S3 0.25 ea min 100

He will send samples and literature.

R. T. Kilcoshenin 6/10/58

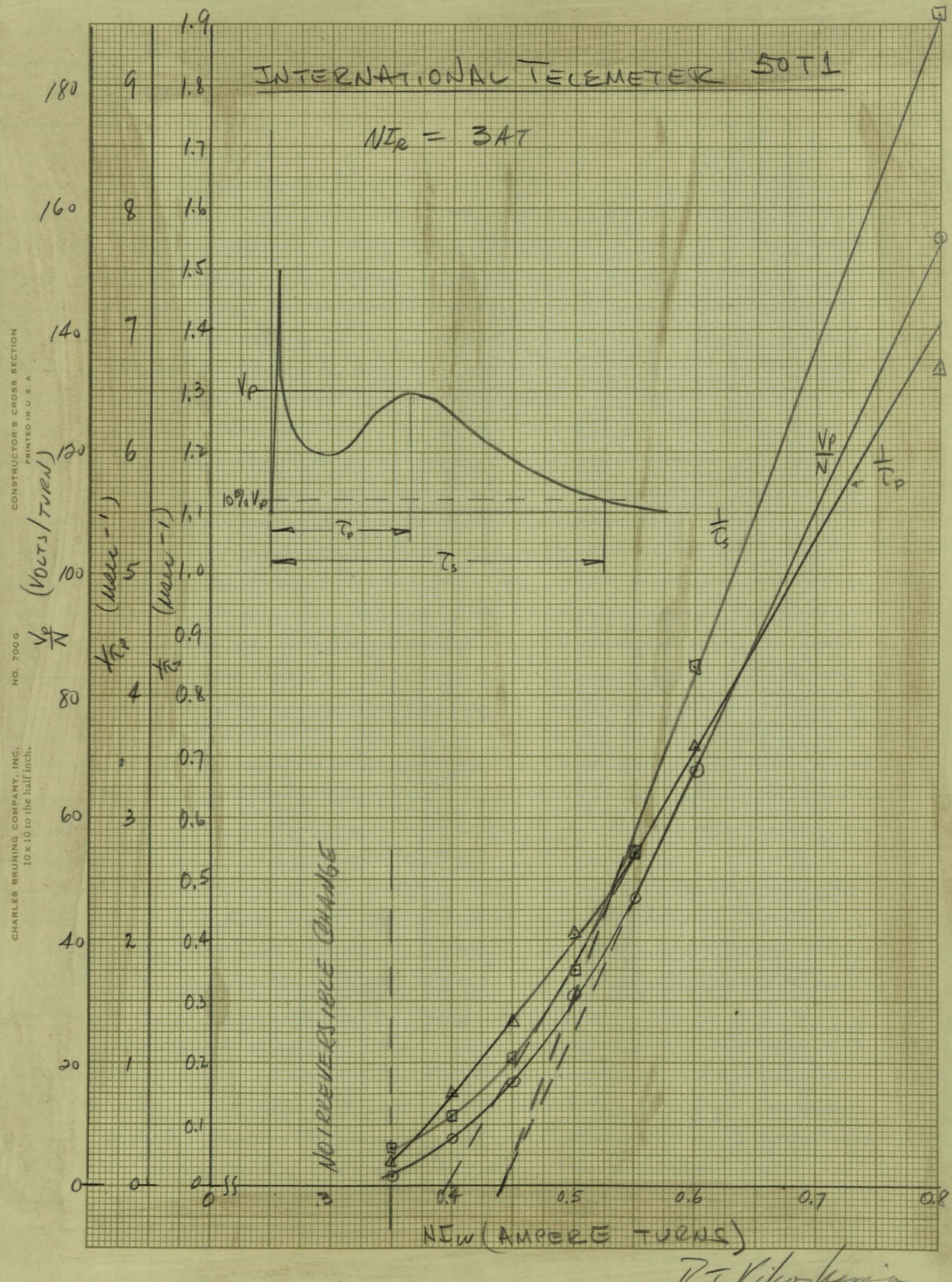
6/11/58

Tested 50 T1 International Tecemeter Sample.

NI	V_p/N	τ_p	τ_s	$1/\tau_p$	$1/\tau_s$
0.335	—	—	—	—	—
0.350	1.5 mv	5.4 μsec	16 μsec.	0.185 μsec⁻¹	0.062
0.400	7.8 mv	1.35	9 μsec	0.740	0.111
0.450	17.0 mv	0.75	4.9 μsec	1.33	0.204
0.500	31.0 mv	0.49	2.85	2.04	0.351
0.550	47. mv	0.37	1.85	2.70	0.540
0.600	68. mv	0.28	1.18	3.57	0.848
0.800	155.	0.15	0.52	6.67	1.920

Reset NI = 3.0 A.T.

Rise time < 20 mμsec.



R.T. Kikoskenia

6/11/58

6/12/58

INTERNATIONAL TELEMETER 50 T 1

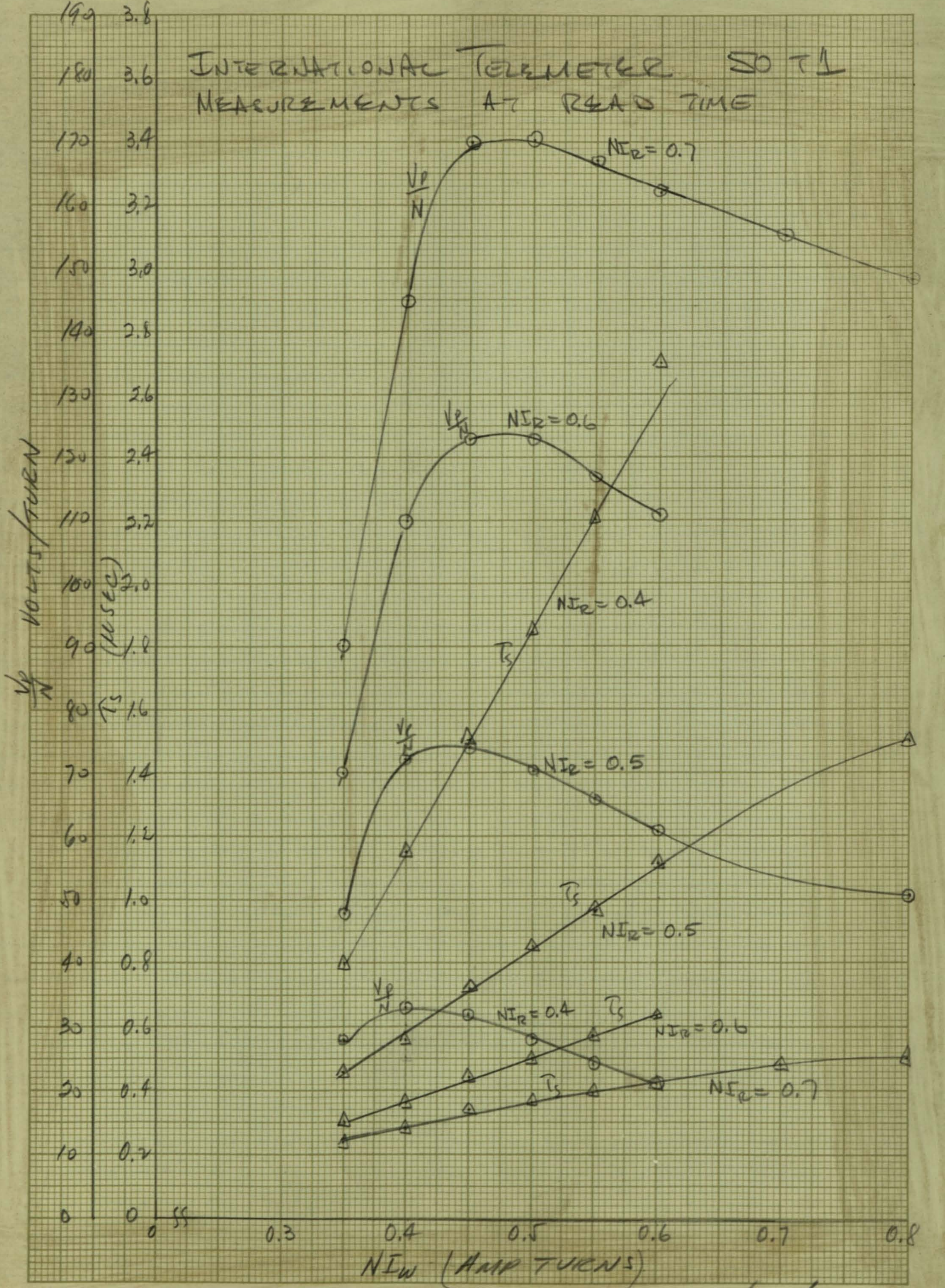
NI	Reset NI = 0.4 V_p/N	τ_s		Reset NI = .50 V_p/N	τ_s		Reset NI = 0.60 V_p/N	τ_s	
0.35	28 mv	0.8	22.4	48 mv	0.45 μsec	21.6	70 mv	0.3 μsec	21.
0.40	33	~~1.08~~ 1.15	38.	72 mv	0.56	40.3	110	0.36	39.6
0.45	32	1.5	48	74	0.72	53.3	123	0.44	54.1
0.50	28	1.82	51	70	0.85	59.5	123	0.50	61.5
0.55	24	2.2	52.8	66	0.96	63.3	117	0.57	66.7
0.60	21	2.7	56.7	61	1.12	67.3	111	0.63	69.9
0.65									

NI	Reset NI = .70 V_p/N	τ_s	
0.35	90 mv	0.24 μsec	21.6
0.40	145 mv	0.28	40.6
0.45	170	0.34	57.8
0.50	170	0.36	61.1
0.55	167	0.39	65.1
0.60	162	0.42	68.
0.70	155	0.48	74.4
0.80	148	0.50	74.

With a constant reset, read current varied the write current and measured the corresponding peak volts per turn and the switching time at read time.

The plotted results show the effect of read current on the core response — the cores ~~under~~ actual operating conditions i.e., $NI_R \simeq NI_W$, will perform much better than the curve on page 16 indicates.

R.T. [illegible] 6/12/58



R.T. Kikoshyma
6/12/58

6/13/58

Since the 50 T1's are too "stiff" for our application, have ordered 100 - General Ceramics F 769-55 cores 050 x 030 x 015.

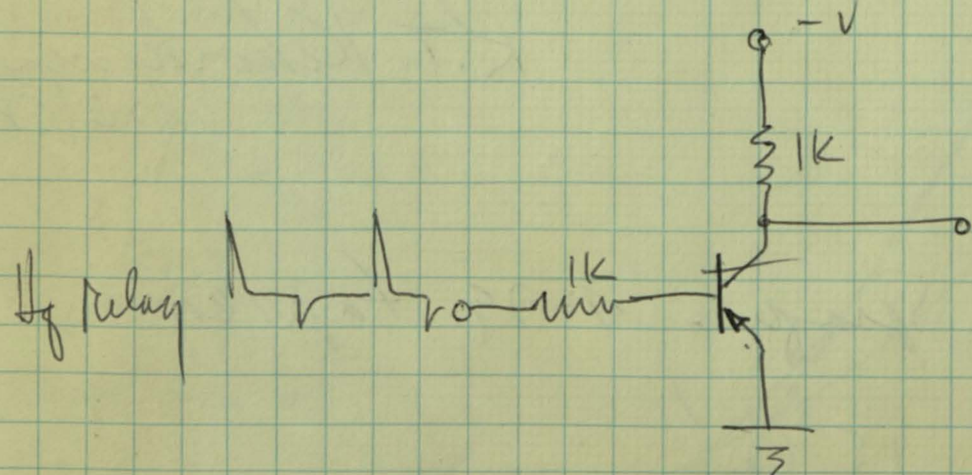
Started to look at some PNPN's.

[signature] 6/13/58

6/16/58

Phoned Jack Steiner, Applications Engr for RCA in regard to the availability of ferrite plate memories. Was referred to Bob Harlan. Bob Harlan will be back on the west coast next week.

Switched the pnpn's "on" and "off" with the Hg relay driver. The rise time, switching 100 ma, was 60 musec. The fall time (turn off) was about 3.5 μsec.



[signature]
6/16/58

6/20/58

Sprague 4-79 tape cores.

Reset $NI \simeq$ 4.5 AT

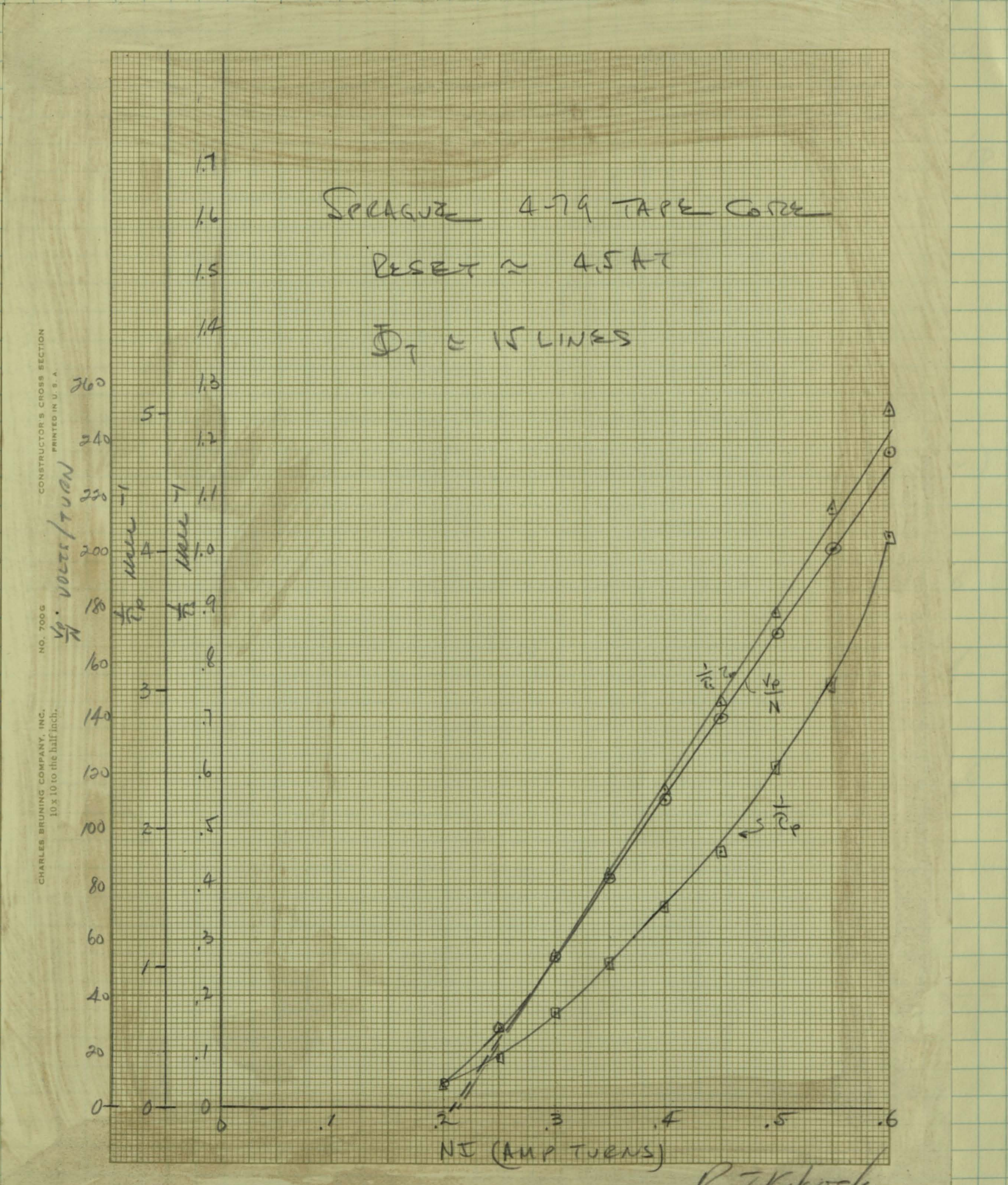
NI	τ_s	τ_p	$\frac{V_p}{N}$	$\frac{1}{\tau_s}$	$\frac{1}{\tau_p}$	
.120	—	—	—	—	—	no switching
.150	~	~	~	~	~	Some switching
.200	24 μsec	7	9 mV	.0417 μsec⁻¹	.143	
.250	7.3	2.8	28	.137	.357	
.300	3.7	1.5	54	.270	.667	
.350	2.4	.98	82	.417	1.02	
.400	~~2.10~~ 1.76	.7	110	.568	1.43	
.450	1.38	.52	140	.725	1.92	
.500	1.14	.41	170	.887	2.44	
.550	0.93	.33	200	1.075	3.03	
.600	0.80	.22	235	1.25	4.55	

R.T. Kikoshima
6/20/58

6/23/58

Measured Φ_T for Sprague 4-79 tape cores

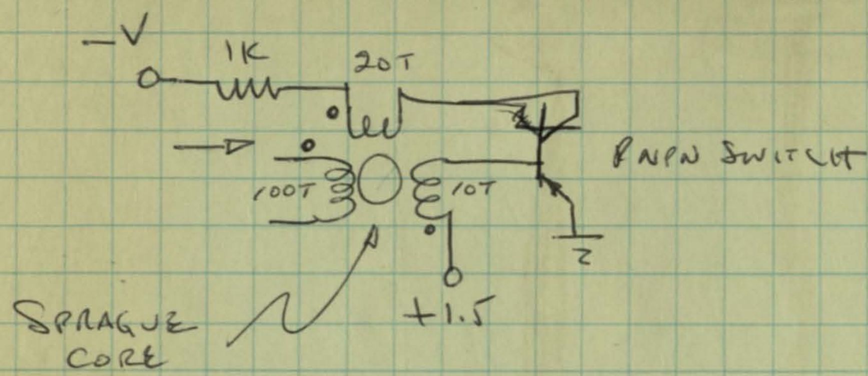
$\Phi_T \simeq$ 15 lines



R T Kikoshima
6/20/58

6/23/58 (Cont.)

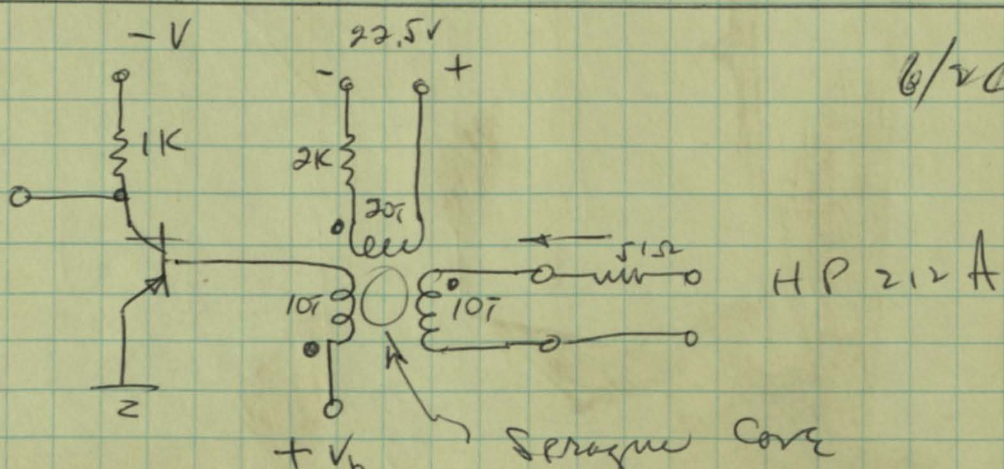
Connected up the following circuit



The circuit is degenerative, i.e., once the input pulse is removed, the current flowing in the collector circuit will reverse the flux in the core. The resultant current flowing in the base circuit is in a direction to turn the PNPN switch "off." Circuit is not working properly.

R. T. Kikushima 6/23/58

6/26/58



With the above circuit, 150 ma pulses approx 0.5 usec wide at the base were generated. The PNPN used had poor BV_{CBO} characteristics.

6/24/58 (cont)

First circuit shown on preceding page (22) did not work. ~~because~~

R T Khoshkenia 6/24/58

6/25/58

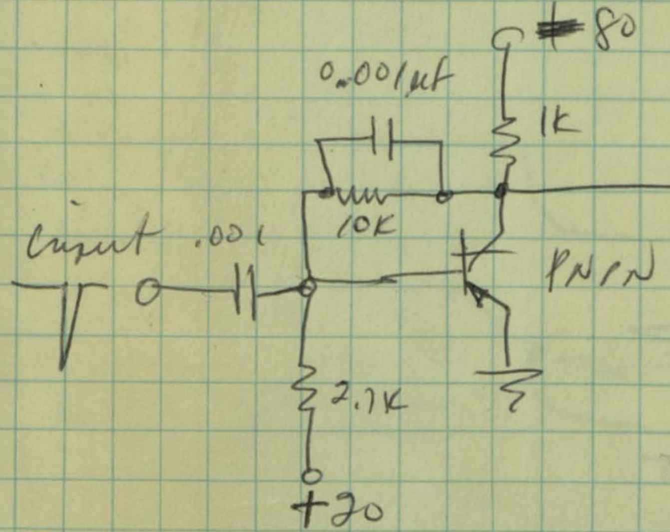
Tried a different PNPN in the circuit shown on page 22 bottom. Switched 100 ma with V_b = 3 volts. Operation was better than with the first PNPN tried.

Took rough measurements of the power gain

$P_i \simeq$ 1.5 watts (not including I^2R of 51Ω resistor)

$P_o \simeq$ 6.5 watts

Tried another pulse circuit suggested by Vic Grinich



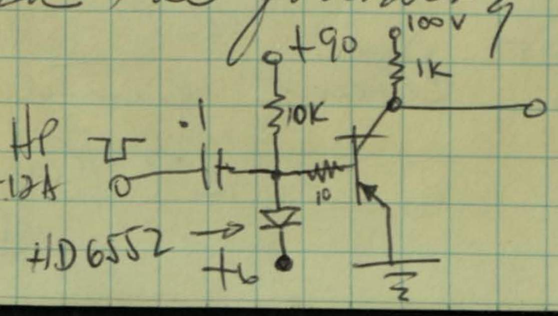
Circuit would not turn off.

The feedback capacitor may not be large enough.

R T Khoshkenia 6/25/58

6/27/58

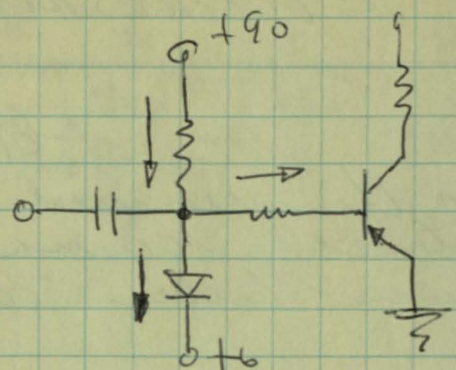
Connected the following circuit.



Circuit tended to stay "on" when input pulses were of an amplitude to just overcome the 6 V bias.

6/27/58 (cont.)

when the pulses were much greater (turning it "on" harder), the switch would turn "off" with the fall of the input pulse.

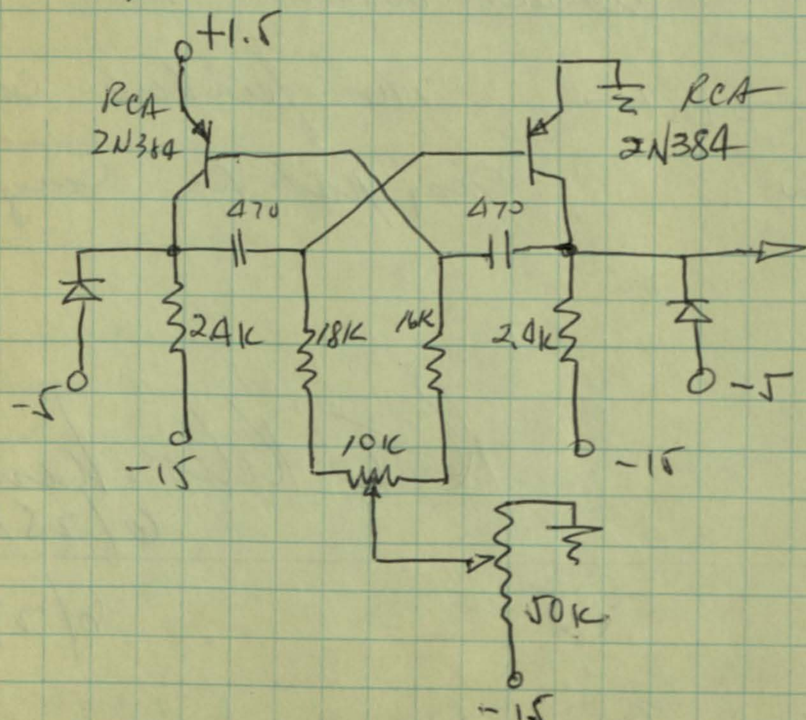


The reason for this action is not yet fully understood

R.T. Kikoshima

7/1/58.

To get an idea of the speed of the 608 circuits, had the following MV built.

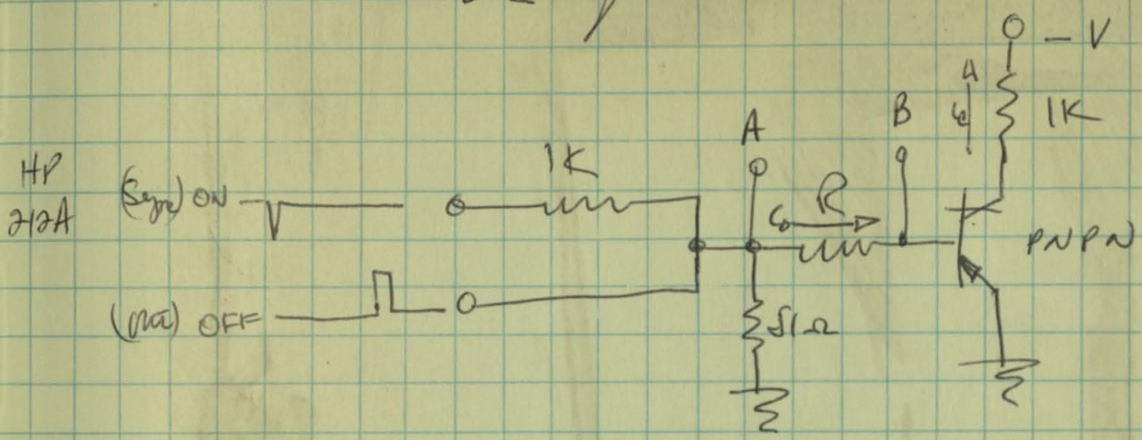


No measurements were made. Circuit operated properly

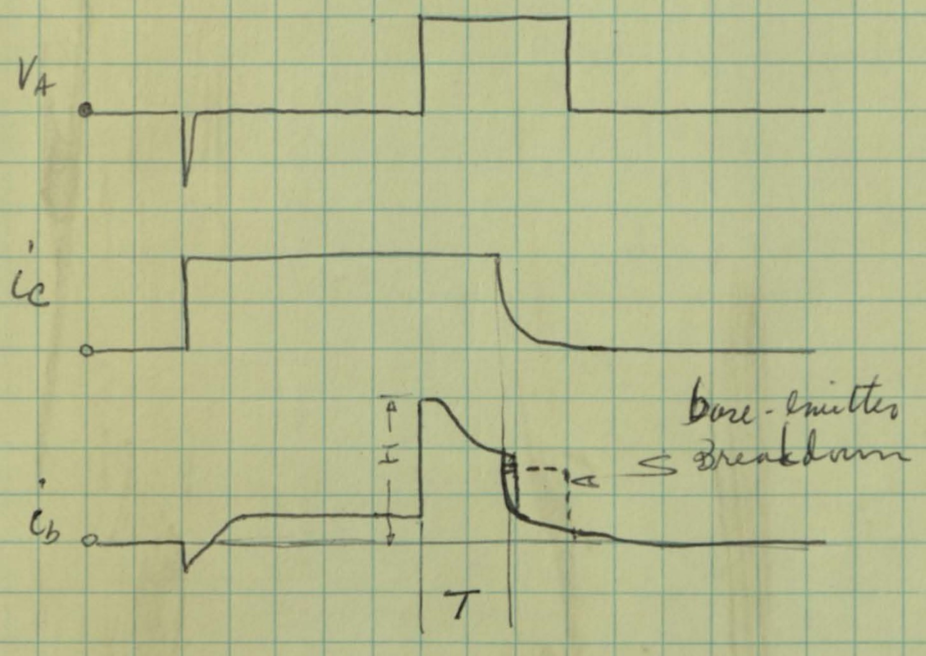
R.T. Kikoshima
7/1/58

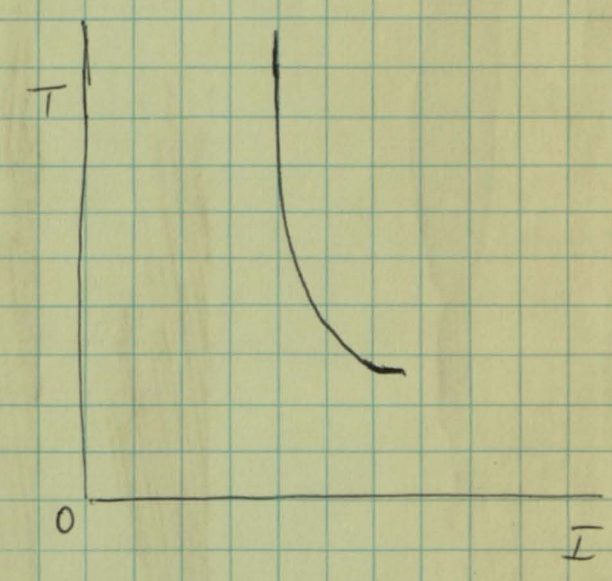
7/2/58

Set up the following circuit to observe the turn-off characteristic of the PNPN switch.



Turned the switch "on" with neg sync pulse from the HP 212A and turned it "off" with the ~~positive~~ output pulse. Observed the base current ~~[illegible]~~ across R.

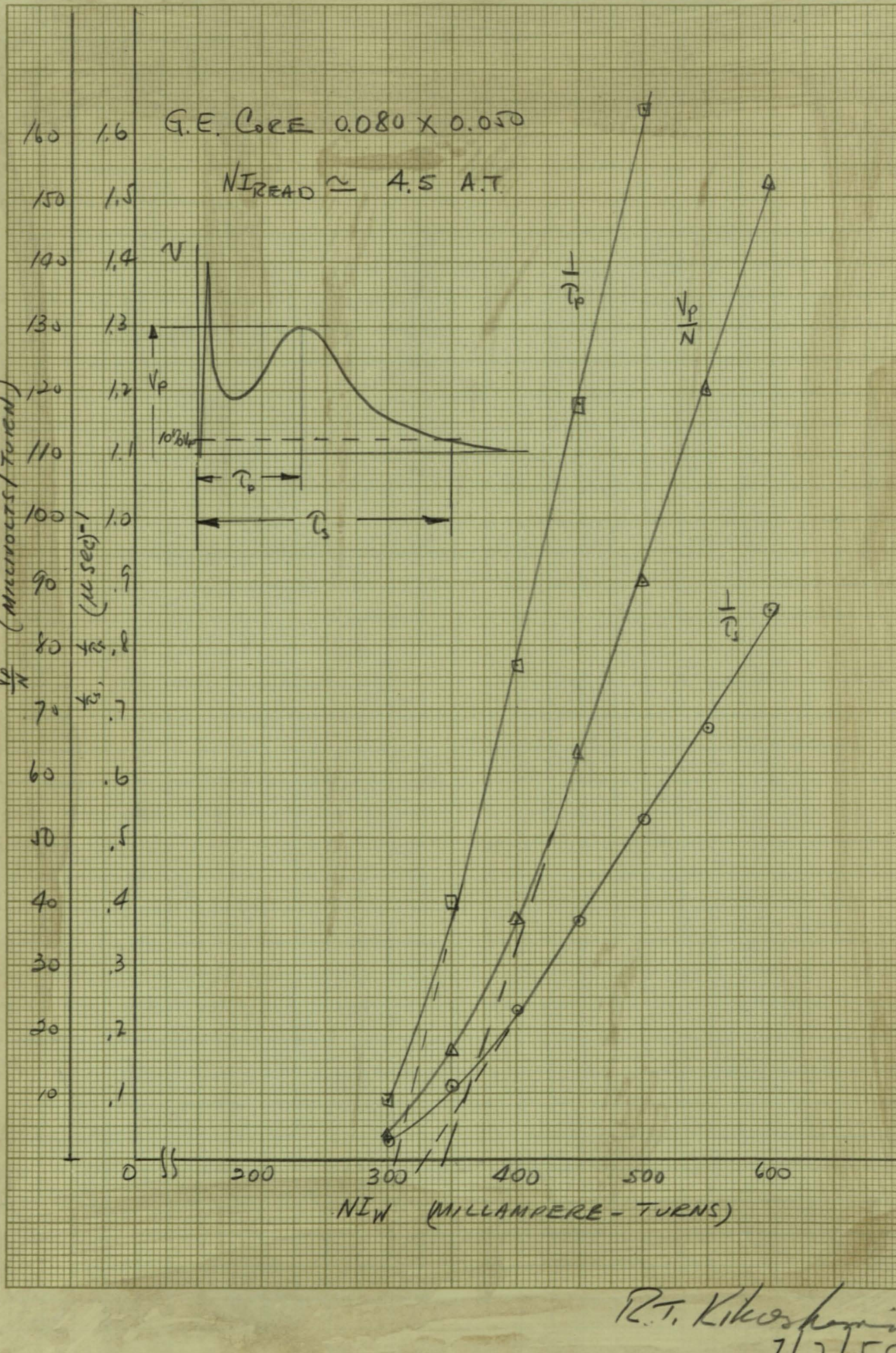




The relationship between the turn off delay, T, and the current I is shown above. R = 100 Ω.

~~[illegible]~~ 608 single shot built.

R. T. [signature]
7/2/58



R.T. Kikoshima
7/7/58

7/7/58

Observed the DC "on" currents in the pnpn. Took no data.

Tested some GE cores from Dr Gruich. NI (reset) = 4.5 ampereturns

NI_{set}	τ_s	τ_p	$\frac{V_p}{N}$	$\frac{1}{\tau_s}$	$\frac{1}{\tau_p}$
280 maT	—	—	—	—	—
300	~35 μsec	11 μsec	3.5 mv	0.0286 μsec⁻¹	0.091 μsec⁻¹
350	9.1	2.5	16.5	0.11	0.40
400	4.4	1.3	37.	0.227	0.77
450	2.7	0.85	63.	0.37	1.18
500	1.9	0.61	90.	0.526	1.64
550	1.45	0.48	120.	0.67	2.08
600	1.17	0.40	152	0.855	2.5

	τ_s	τ_p	$\frac{V_p}{N}$
NI_{reset}, NI_{set} = 400 maTurns	1.64 μsec	0.7 μsec.	63 mv

This core apparently lies somewhere between the General Ceramics S_1 and S_3 (new designation S4 & S5)

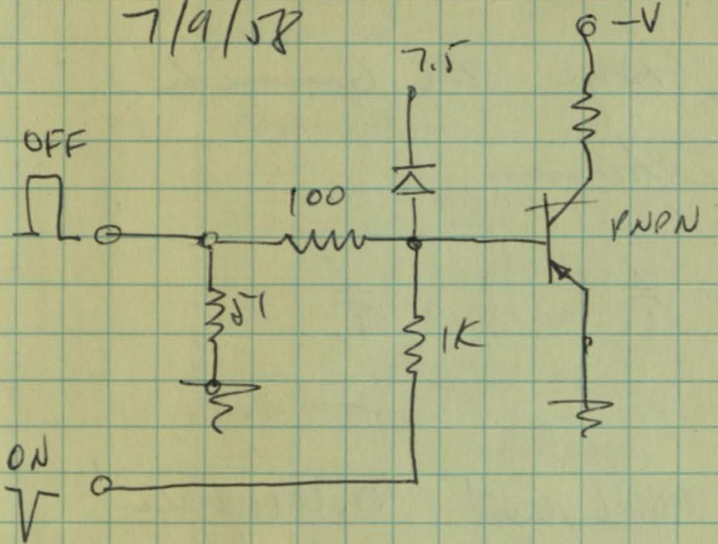
R A Kiloskeris 7/7/58

7/8/58

Continued work on the PNPN Switch.

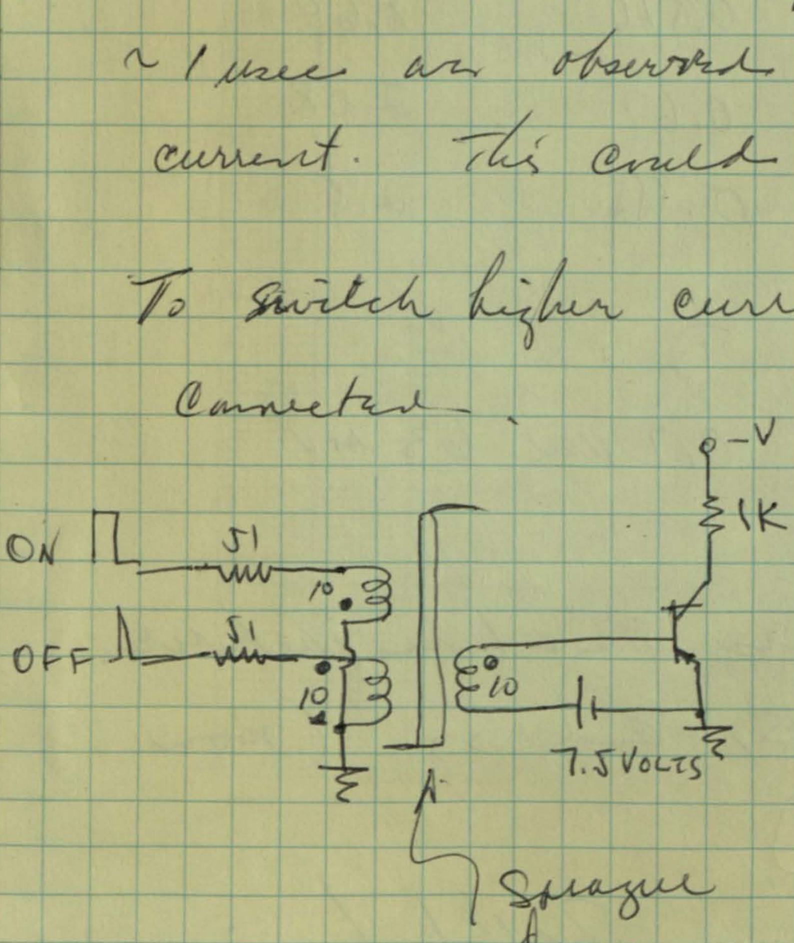
R. T. Kikoshima 7/8/58

7/9/58

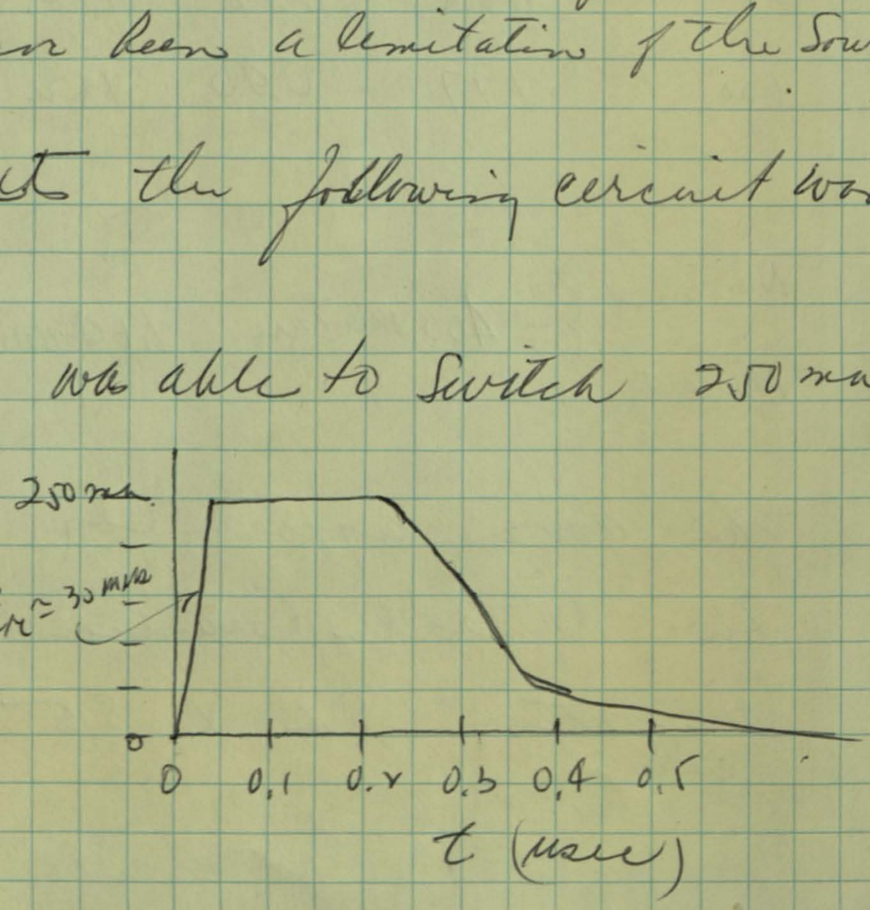


With the circuit as shown, observed the turn off currents and voltage. The diode was added to prevent base-emitter breakdown. Since the base-emitter turn-off source voltage is limited by the breakdown, a low impedance base circuit is necessary for high current. The turn-off current - delay characteristic was too complex to record. A definite minimum turn off delay of ~1 usec was observed apparently independent of the turn off current. This could have been a limitation of the Source.

To switch higher currents the following circuit was connected.



was able to Switch 250 ma



Destroyed one PNPN (120-59).

R.T. [signature] 7/9/58

7/10/58

With the circuit as shown on page 28, bottom, destroyed ~~to~~ 120-52 ~~when~~ in an attempt to switch 300 ma. 120-52 now has a very low avalanche breakdown.

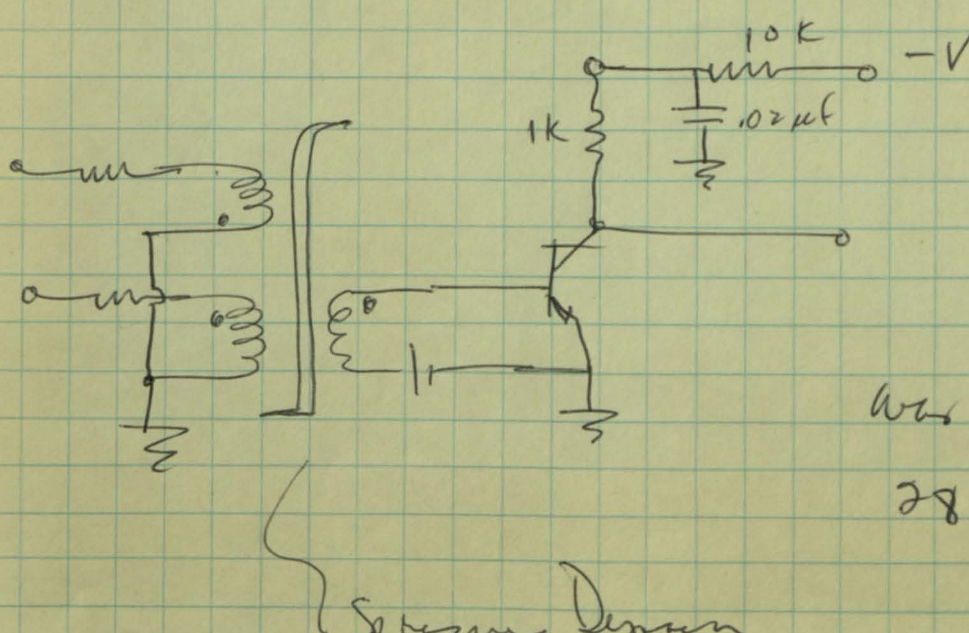
Measured some of the parameters of the PNPN's available for future use. Will complete the data tomorrow.

R.T. [signature] 7/10/58

7/11/58

Completed the measurements on the PNPN's.

Added an RC protective circuit as shown



The maximum current switched was approximately 280 ma.

R.T. [signature] 7/11/58

Batch No. ________

PNPN

FT-4000 PREPRODUCTION EVALUATION SHEET

Device No.													
	I_c	ma	ma	ma	XXXXX	1μa	150ma	~~150ma~~ 100	150ma	XXXXX			XXXXX
	I_b	XXXXX	XXXXX	XXXXX	.2 ma	XXXXX	XXXXX	15ma	15ma	XXXXX			XXXXX
	V_c	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	10v	XXXXX	XXXXX	10v			XXXXX
		XXXXX	R= Ω	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	XXXXX	I_E = 10ma			XXXXX
	Date	BV_{CEO}	BV_{CER}	BV_{CBO}	BV_{BEO}	V_{CBO}	I_b	$V_{CE(Sat)}$	$V_{BE(Sat)}$	C_{OB}			Class
120-20		200+		Sloppy	Sloppy			1.0					
-25		90V			Sloppy			1.0					
-													
-													
-42		90V			7.9			0.95					
-43		200+			8.2			1.0					
-46		200+			7.6			1.0					
-47		28V			8.3			1.0					
-48		200+			8.5			0.97					
-49		6V			8.2			0.96					
-50		62			8.0			0.98					
-51		98			7.3			0.95					
-53		100+	emitter open					—					
-55		5.5V			8.5			1.0					
-58		200+			8.6			1.08					
-60		200+			8.4			1.0					
-61		200+			8.6			1.0					
-62		5V			8.4	Sharp		0.96					
-63		200+			5.8	round		0.97					
-64		200+			8.6			0.96					

Batch No. ______

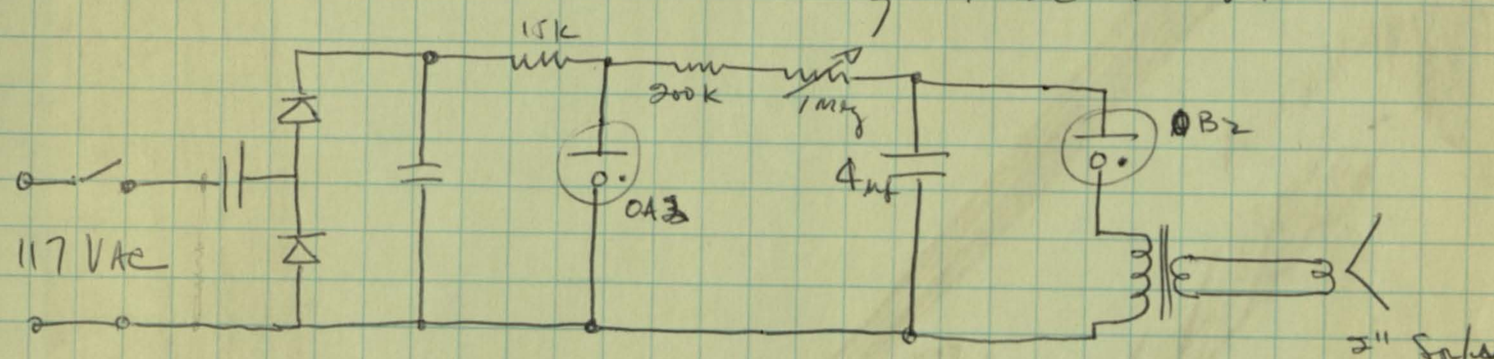
PNPN FT-4000 PREPRODUCTION EVALUATION SHEET

Device No.													
	I_c	ma	ma	ma		1μa	150ma	100 ~~150ma~~	150ma				
	I_b				.2 ma			15ma	15ma				
	V_c						10v			10v			
			R= Ω							I_E = 10ma			
	Date	BV_{CEO}	BV_{CER}	BV_{CBO}	BV_{BEO}	V_{CBO}	I_b	$V_{CE(Sat)}$	$V_{BE(Sat)}$	C_{OB}			Class
120-65		200+			8.4			.95					
-66		200+			5.5 rounded			.92					
-67		200+			emitter open			~~[illegible]~~					
-68		70✓			8.2			.95					
-69		200+			8.3			.95					
-70		200+			8.5			.95					
-71		200+			8.4			.98					
-72		200+			12 sloppy			2.6	(2)				
-73		27✓			8.7			.98					
-74		24			8.4			.97					
-75		200+			8.7			1.05					
-76		200+			7.8			.96					
-77		112			7.9			1.03					
-78	good	200+			8.5			.98					
-79		200+			4.8 sloppy			.97					
-80		200+			7.8			.96					
-81		140+			7.3			1.0					
~~-90~~													

7/14/58

V. Grinich suggested that I look at the turn-off of the PNPN for some current - time relationship. Started to set-up the circuit.

Started building a metronome for Gordon Moore. Circuit will be something like this.



R.T. [illegible] 7/14/58

7/15/58

Completed the metronome.

R.T. [illegible] 7/15/58

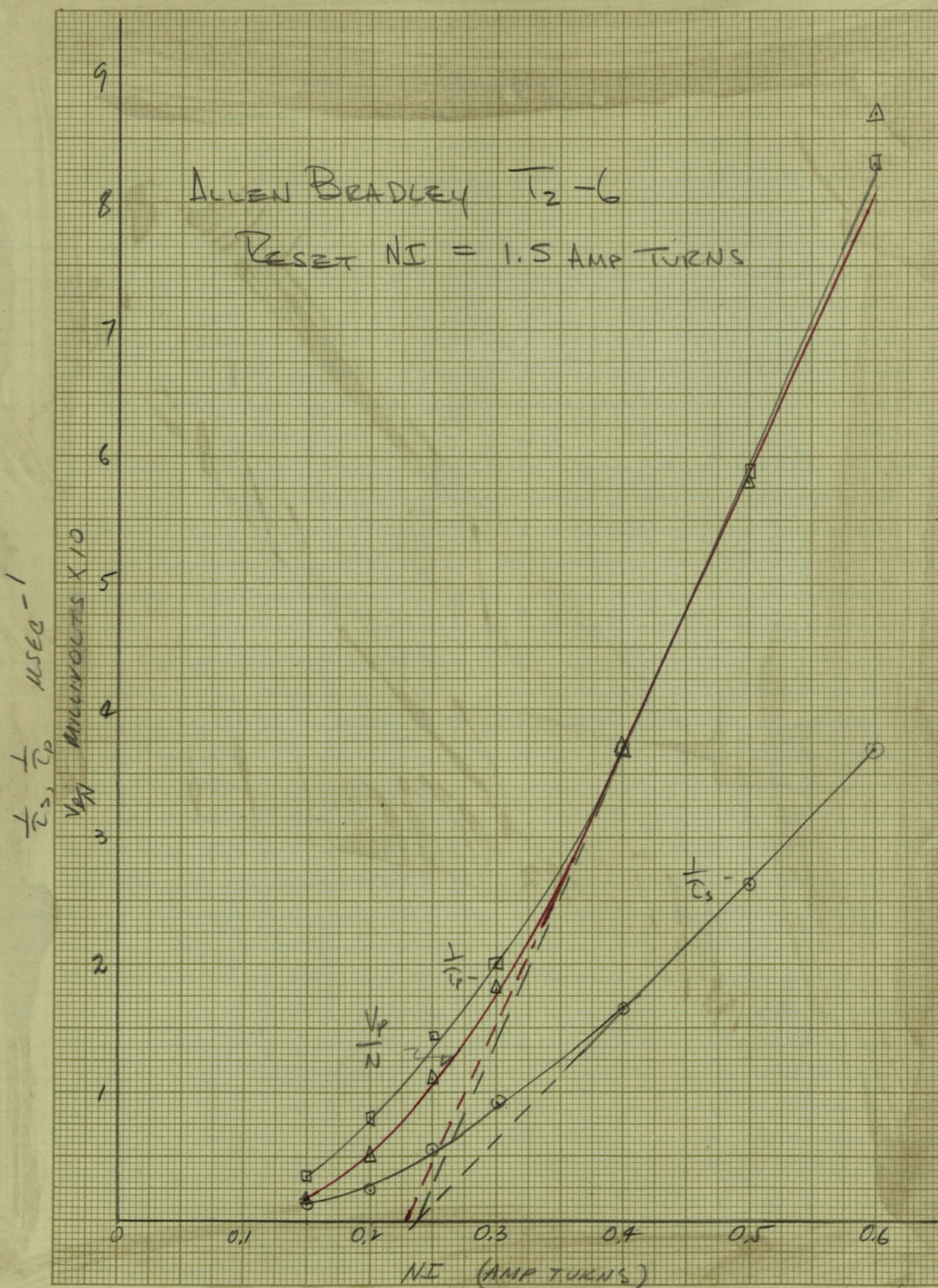
7/18/58

Took switching data for the Allen-Bradley T_2-6 Core (0.030" OD). Brake the other sample, T_3-8, before any measurements were taken -

NI	τ_s	τ_p	V_p/N	$1/\tau_s$	$1/\tau_p$
.1	—	—	—	—	—
.15	8 (?) μsec	3 (?) μsec	1.5 mV	0.125 μsec^{-1}	0.333 μsec^{-1}
.2	4.5	1.25	5.	0.222	0.8
.25	1.8	0.7	11.	0.555	1.43
.3	1.1	0.5	18.	0.91	2.0
.4	0.6	0.27	37.	1.67	3.7
.5	0.38	0.17	58.	2.63	5.9
.6	0.27	0.12	87	3.70	8.3

NI_{reset} = 1.5 AT. Curve on next page.

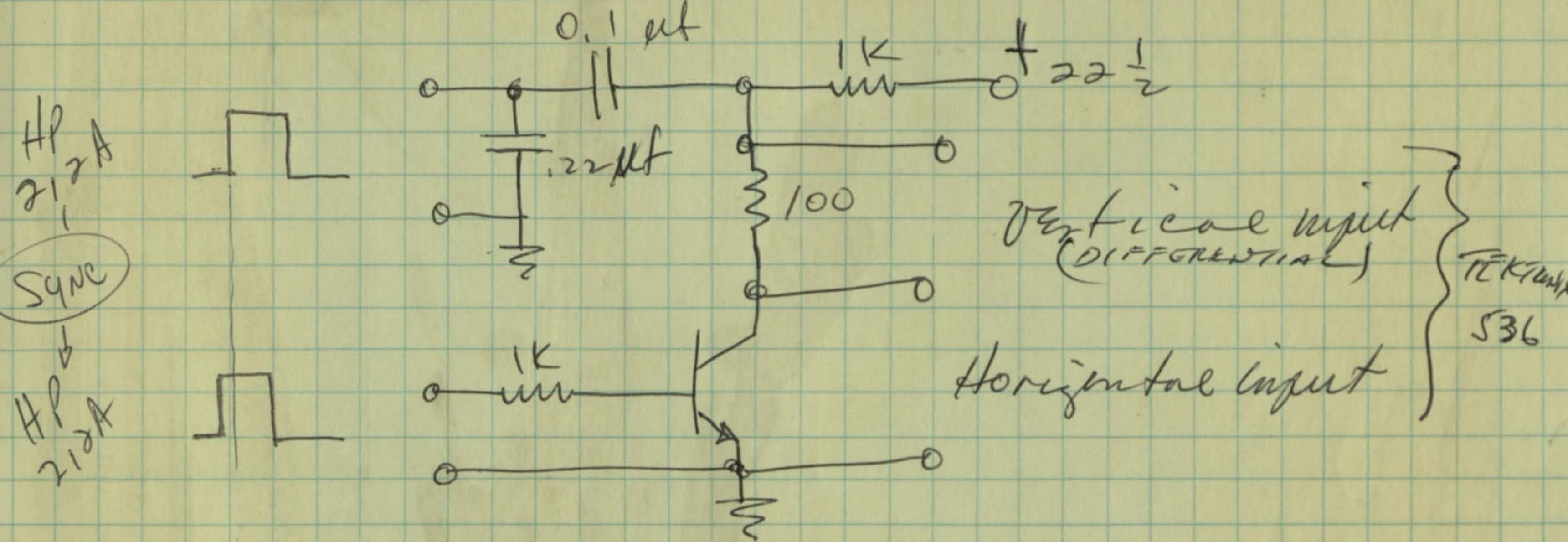
R.T. [illegible]


ALLEN BRADLEY T2-6
RESET NI = 1.5 AMP TURNS
1/τs, 1/τp μsec⁻¹
Vp/N MILLIVOLTS X 10
Vp/N
1/τp
1/τs
0
0.1
0.2
0.3
0.4
0.5
0.6
1
2
3
4
5
6
7
8
9
NI (AMP TURNS)

7/18/58

7/25/58

Set up circuit for ~~ckt~~ pulsed collector family.

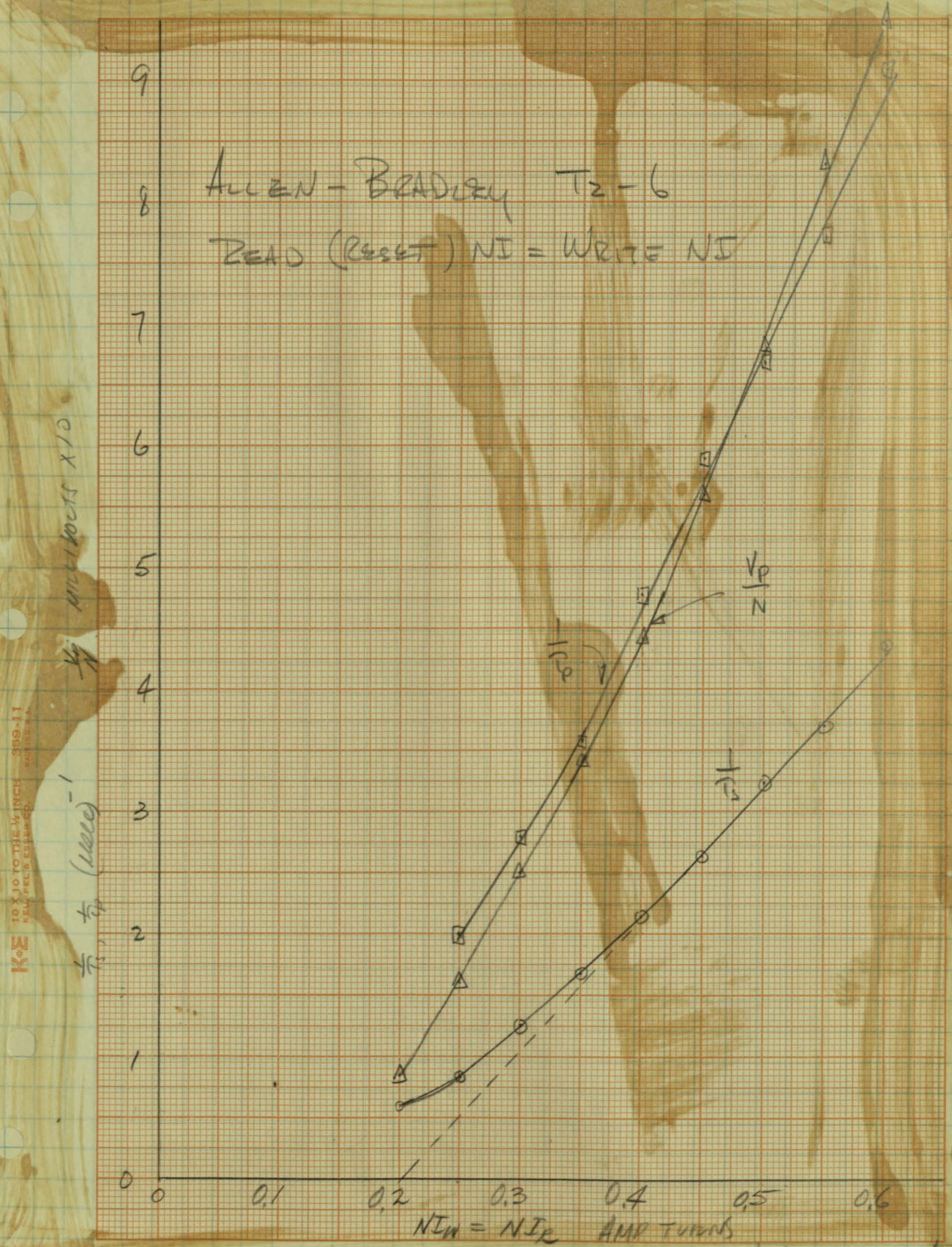


R. T. Kikushima 7/24/58

8/1/58

Took the switching characteristics of the Allen Bradley T2-6 core with the reset ~~current~~ mmf equal to the set mmf. This test will give more realistic results for a core operating in a coincident current memory

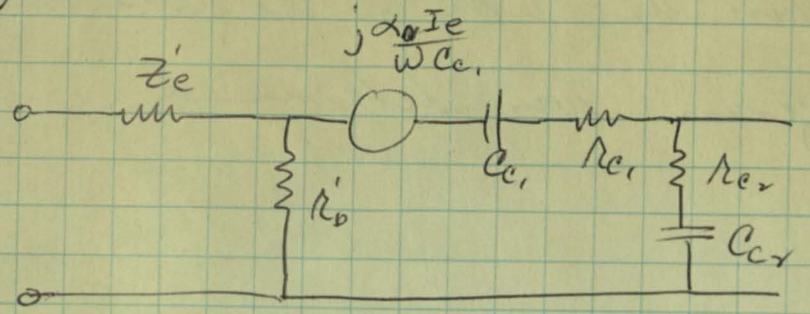
$\frac{NI_R}{NI_S}$	τ_s	τ_p	$\frac{V_p}{N}$	$\frac{1}{\tau_s}$	$\frac{1}{\tau_p}$
0.25 AT	1.2 µs	0.5 µs	'16 mv	0.825 µs⁻¹	2.0 µs⁻¹
0.30	0.8	0.36	25 mv	1.25	2.78
0.35	0.6	0.v8	34 mv	1.67	3.57
0.40	0.47	0.21	44 mv	2.13	4.76
0.45	0.38	0.17	56 mv	2.63	5.89
0.50	0.31	0.15	68 mv	3.2v	6.67
0.55	0.27	0.13	83 mv	3.70	7.70
0.60	0.23	0.11	95 mv	4.35	9.10


ALLEN-BRADLEY T2-6
READ (RESET) NI = WRITE NI
$\frac{V_P}{N}$ MILLIVOLTS x10
$\frac{1}{T_P}$, $\frac{1}{T_S}$ (μsec)$^{-1}$
0
1
2
3
4
5
6
7
8
9
0
0.1
0.2
0.3
0.4
0.5
0.6
$NI_W = NI_R$ AMP TURNS
$\frac{V_P}{N}$
$\frac{1}{T_P}$
$\frac{1}{T_S}$
K+E 10 X 10 TO THE ½ INCH 359-11
KEUFFEL & ESSER CO.

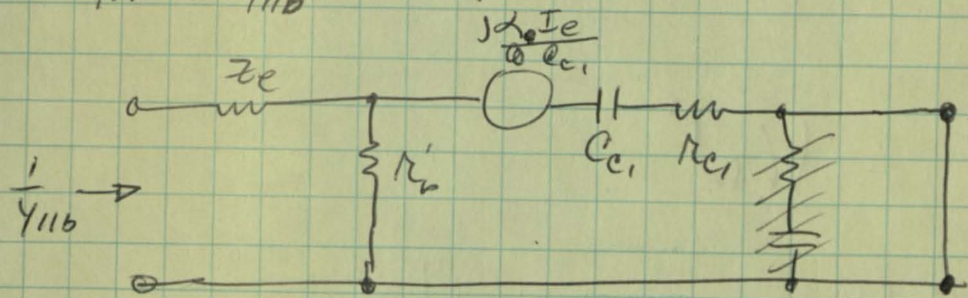
8/1/58 R.T. [illegible]

8/5/58

Equivalent Ckts (H.F.) 30 mc



For $\frac{1}{y_{11b}}$



Equivalent generator impedance, z_g

$$z_g = \frac{-(r_b' + r_{c_1}) + j\frac{1}{\omega C_{c_1}}}{1 + j\frac{\omega r_b' C_c}{\alpha}}$$

$$\frac{1}{y_{11b}} = z_e' + \frac{r_b'\left[1 - \alpha + j\omega r_{c_1} C_{c_1}\right]}{1 + j\omega C_{c_1}(r_b' + r_{c_1})} \simeq z_e' + \frac{r_b'[1-\alpha]}{1 + j\omega r_b' C_{c_1}}$$

Let $\frac{1}{y_{11b}} - z_e' = A + jB$ and $\alpha = a - jb$

Then $$r_b' = \frac{(1-a)A + bB}{(1-a)^2 + b^2}$$

$$C_{c_1} = \frac{\left[(1-a)^2 + b^2\right]\left[bA - (1-a)B\right]}{\omega\left[(1-a)A + bB\right]^2}$$

$$\frac{(1-a)}{b} = \frac{A}{B} \quad \text{critical case}$$

8/5/58

Since $\alpha = a - jb$ was not known at 30 mc, the restriction on α when $|h_{fe}|$ @ 30 mc is given was determined.

$$\left|\frac{\alpha}{1-\alpha}\right| = |h_{fe}|$$

$$\alpha = a - jb$$

$$\frac{\alpha}{1-\alpha} = \frac{a - jb}{1 - a + jb}$$

$$\left|\frac{\alpha}{1-\alpha}\right| = \left[\frac{a^2 + b^2}{(1-a)^2 + b^2}\right]^{\frac{1}{2}} = |h_{fe}|^2$$

$$a^2 + b^2 = |h_{fe}|^2 \left[1 - 2a + a^2 + b^2\right]$$

$$(|h_{fe}|^2 - 1) b^2 = -(|h_{fe}|^2 - 1) a^2 + 2|h_{fe}|^2 - |h_{fe}|^2$$

$$b = \left[-a^2 + \frac{2|h_{fe}|^2 a}{[|h_{fe}|^2 - 1]} - \frac{|h_{fe}|^2}{|h_{fe}|^2 - 1}\right]^{\frac{1}{2}}$$

R.T. Kilcoshimin
8/5/58

8/13/58

Rec'd 100 General Ceramics cores # 764 - S5

.030" x .050" cores.

R.T. Kilcoshimin
8/13/58

8/14/58

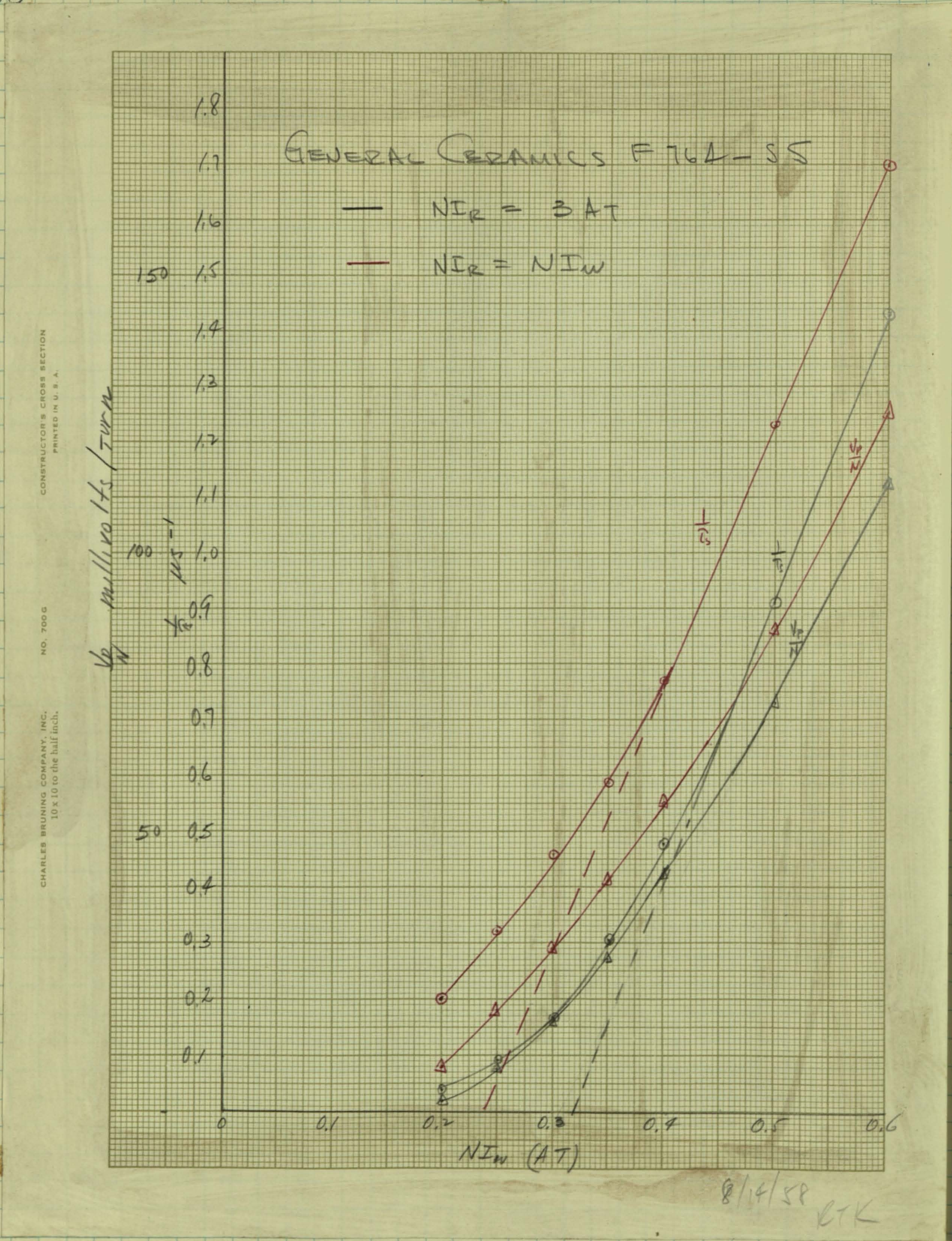
General Ceramics F 764 - 55

NI_R = 3 Amp Turns

	NI_W	τ_s	τ_p	V_p/N	$1/\tau_s$	$1/\tau_p$
	150 mAT	—	—	—		
5	200	25 μsec	8 μsec	2 mv	.04 μsec^{-1}	.125 μsec^{-1}
4	250	11 μsec	2.6	7.5	.091 [struck]	.416
3.3	300	6.1	1.3	16	.164	.83
2.86	350	3.3	0.85	27	.303	1.18
2.5	400	2.1	0.63	42	.476	1.59
	500	1.1	0.38	73	.910	2.63
	600	0.7	0.26	112	1.43	3.85

$NI_R = NI_W$

NI_W	τ_s	τ_p	V_o/N	$1/\tau_s$	$1/\tau_p$
100 mA-T	—	—	—	—	—
~~150~~ 200	5	2.2	8 mv	0.2 μsec^{-1}	0.455
250	3.1	1.5	18 mv	0.322	0.667
300	2.2	1.0	29 mv	0.455	1.0
350	1.7	0.78	41	0.588	1.28
400	1.3	0.6	55	0.770	1.67
500	0.81	0.38	86	1.23	2.63
600	0.59	0.26	125	1.70	3.84


GENERAL CERAMICS F764-55
NI_R = 3 AT
NI_R = NI_W
1/τ_s
1/τ_s
V_p/N
V_p/N
V_p/N millivolts/turn
1/τ_s μs^-1
150
100
50
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
NI_W (AT)

8/14/58
RTK

8/14/58
Cont

Comparison of test results:

$NI_W = NI_R = 0.200$ AT

	Allen Bradley	ours
Peak Voltage per turn	0.01 V/turn	0.0085 V/turn
Switching time	1.2 μs	1.7 μs.
Load Resistance / turns²	49 Ω/turn²	51 Ω/turn²

8/18/58

A more practical test for memory cores is to set $NI_{read} = 2NI_{write}$. Then increasing NI_{write} from zero to the threshold of switching will determine the maximum half-select current.

Allen Bradley T-6

MAX HALF SELECT = 110 mA-turns

HALF SELECT = 100 mA-Turns
Full " = 200 mA-Turns

$\frac{V_P}{N}$ = 6 mv/turn

τ_s = 1.7 μsec

τ_p = 0.7 μsec.

8/18/58 cont

General Ceramics F764-55

MAX HALF SELECT = 200 mA-Turns

Full Select = 400 ma-Turns	Full select = 300 mA-Turns
$\frac{V_o}{N}$ = 48 mv/Turn.	$\frac{V_r}{N}$ = 23 mv/Turn
τ_s = 1.1 μsec.	τ_s = 2 μsec.
τ_p = 0.56 μsec.	τ_p = 1 μsec.

General Electric Cores

A 7151990	A 7152019
Max half select 235 mA-Turns	Max half select 250 mA-Turns
Full select = 400 ma-turns	Full select 400 mA Turns
$\frac{V_o}{N}$ = 58 mV/Turn	$\frac{V_o}{N}$ = 40 mV/Turn
τ_s = 1.55 μsec	τ_s = 1.9 μsec
τ_p = 0.7 μsec	τ_p = 0.96 μsec.

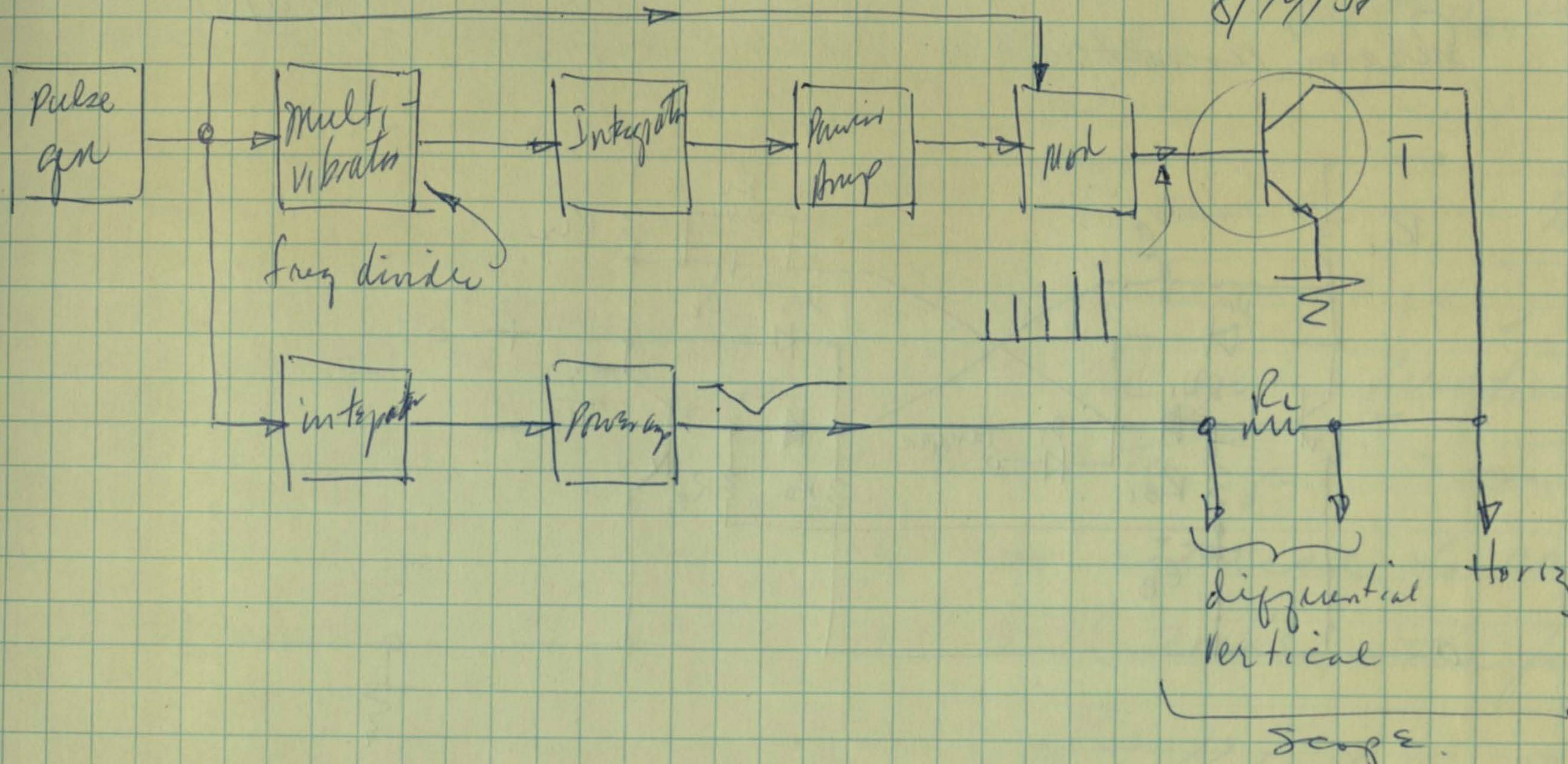
So far the General Ceramics F764-55 has the best characteristics of the commercially available cores -

R.T. Kikoshima.
8/18/58

8/19/58

Discussed the Gulsad VI platter with R H Beeson

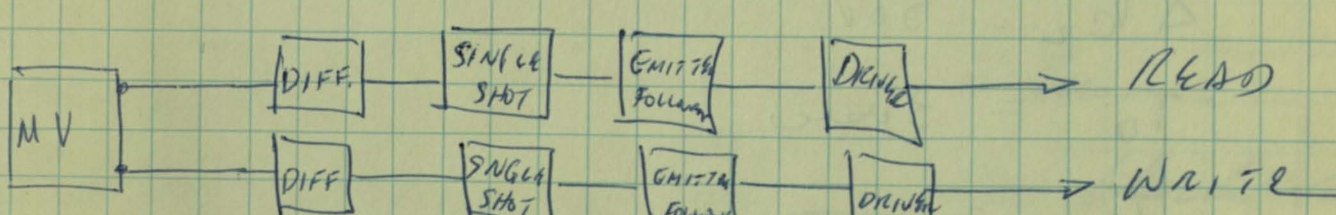
8/19/58



R.T. Kikoskimia 8/19/58

8/20/58

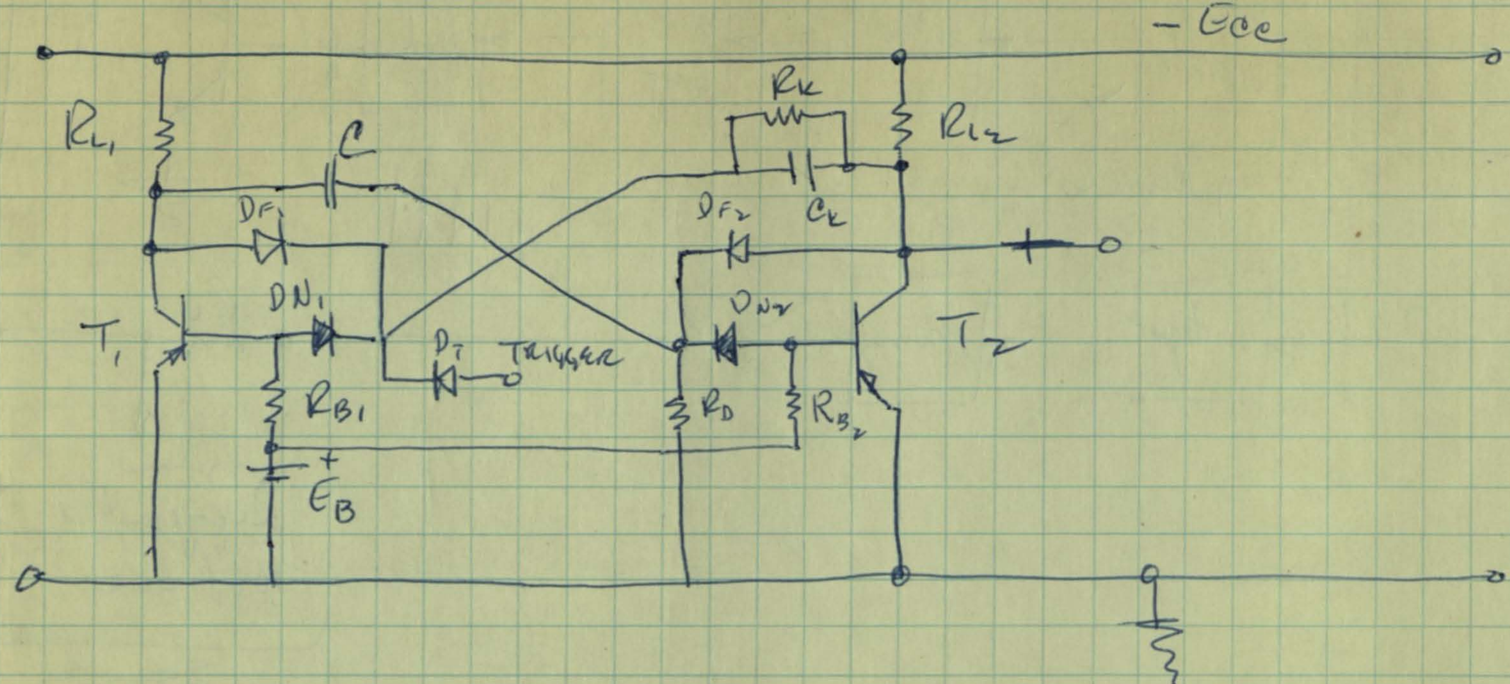
Read the paper by J.J. Suran, "Transistor Monostable Multivibrators for Pulse Generation", Proc IRE June 58. Would like to try this circuit for the single shots for the read and write core driver pulses.



R T Kikoskimia 8/20/58

8/21/58

Surans' circuit:



T_1, T_2 - RCA 2N384 (Drift)

D_{N_1}, D_{N_2} - HD 6552 (Silicon)

D_{F_1}, D_{F_2}, D_T — Syl 1N119 Germanium

GIVEN: $E_{cc} = 22\frac{1}{2}$ V

$E_B = 1.5$ V

$\Delta I_{C_2} \doteq 10$ mA

$\Delta V_{C_2} = 20$ V

$T_D = 3$ μsec

$T_{P min} =$ ——.

Calculated: $R_{L_2} = R_{L_1} = 2$k $C = .01$ μf

$R_K = 18$K $R_D = 4.7$K

$R_{B_1} = 2900$ Ω

$C_K = 156$ pf

$R_{B_2} = 4.7$K

8/21/58 Cont

Connected the circuit with the calculated values. Circuit did not operate because both T_1 and T_2 were "off".
Shunted R_K with 33K (resistance now ≈ 14.5K)
The circuit then operated, but the pulse duration, T_D was ≈ 50 μsec. In order to get 3 usec with the other circuit values; C was reduced to 0.005 μf
The rise time was excellent (? mus) the fall time was poor.

R.T. Kikoskinen 8/21/58

8/22/58

The circuit shown on page 42 was saturating because the drop across D_{N1} & D_{N2} was not enough. Will try Zener diode in this circuit.

R.T. Kikoskinen 8/22/58

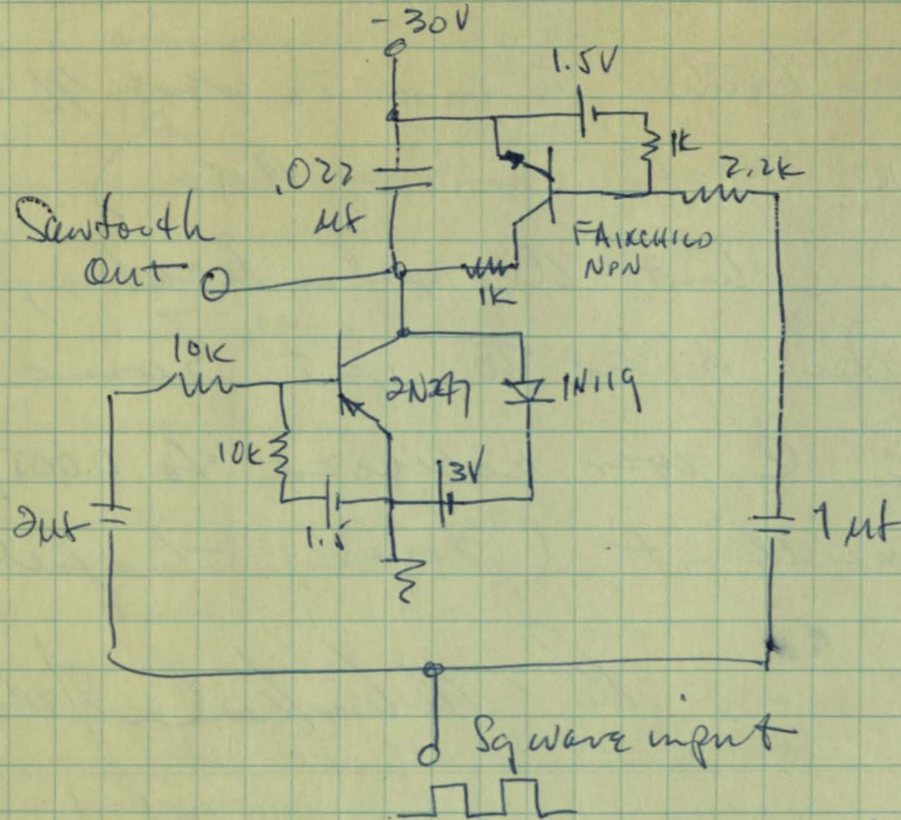
8/25/58

Discussed the VI problem with RH Brown.
Will start the circuit design of the blocks as shown on page 41.

R.T. Kikoskinen 8/25/58

8/26/58

Built a linear saw-tooth shaper as follows:

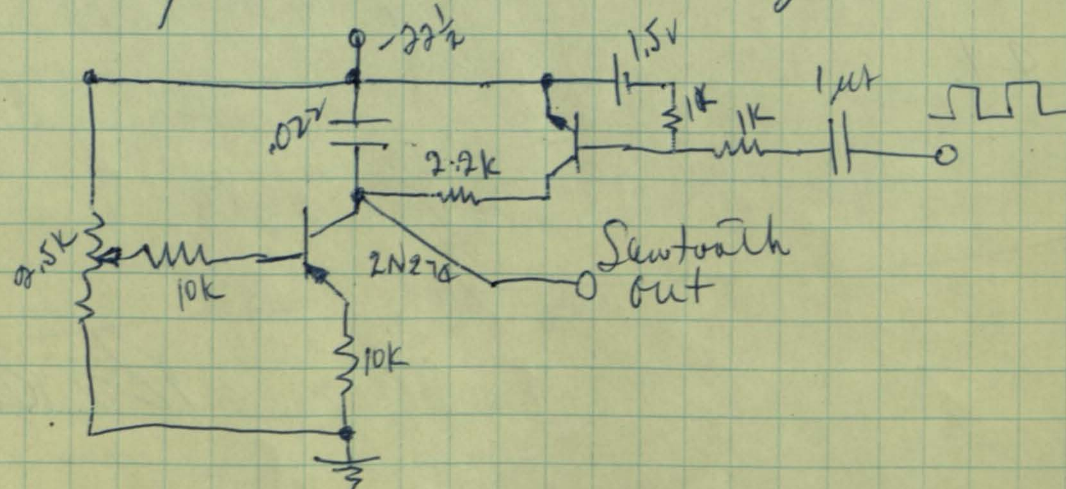


The .022 μf condenser charges thru the 2N247 transistor (constant current source), when the base is negative. The Fairchild npn is cut-off during the charge cycle. ~~The~~ When the input reverses polarity, the Fairchild transistor conducts, discharging the condenser. The 2N247 is cut-off during this time - The linearity was very good. ~~ab~~ within ± 5%.

R.T. Kikoshima 8/26/58

8/29/58

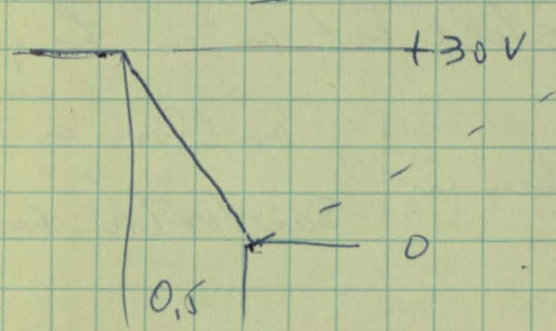
In considering other types of linear sawtooth shapers, the following circuit was designed:



8/29/58

This circuit is simpler than that shown on page 44 (top) and is more stable. We will use this circuit in the V-I plotter.

Have been thinking about the collector voltage sweep source. ~~The~~

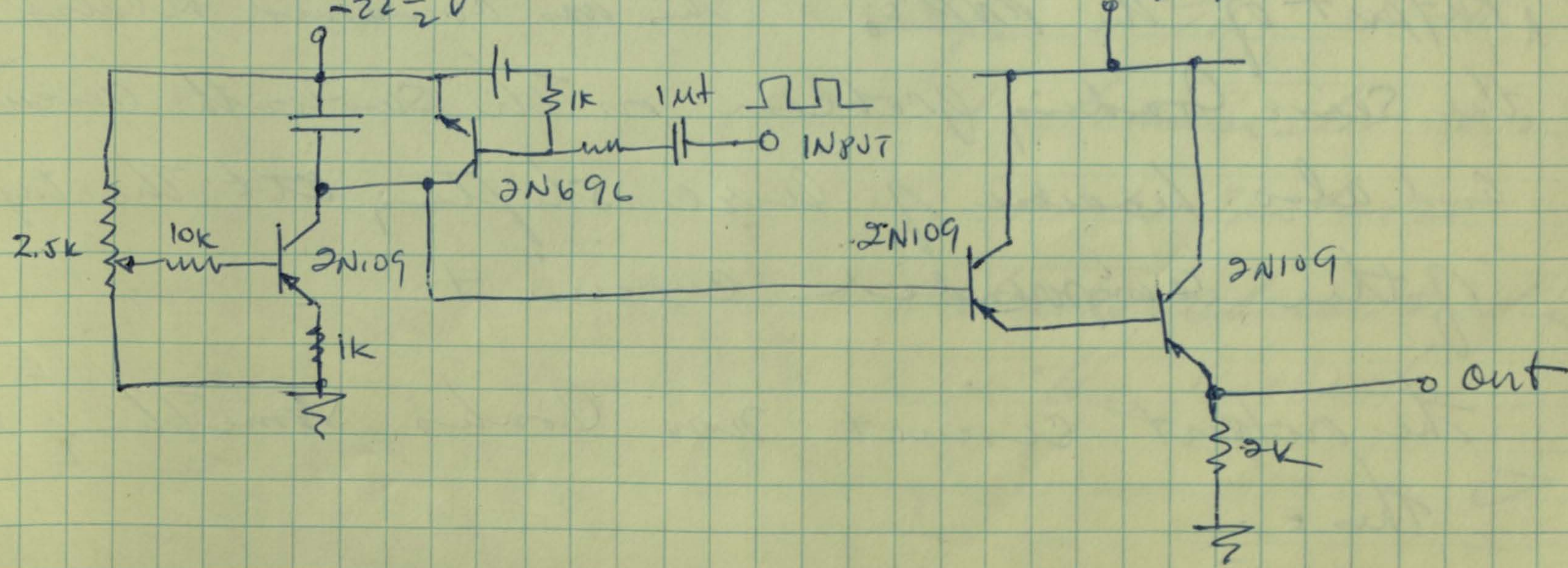


This circuit ~~will~~ must provide a voltage from +30 to 0 in 0.5 μsec. It must be capable of delivering at least 1 Amp to the load.

[signature] 8/29/58

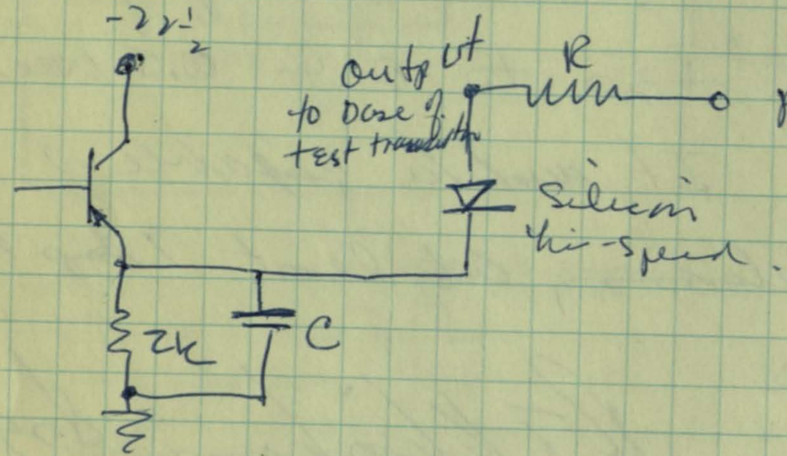
9/8/58

Continuing work on the V-I Plotter. The sawtooth circuit shown on page 44 Bottom ~~top~~ was modified to produce a "stiffer" output for clipping the pulse.



9/8/58

R.A. Beeson suggested bypassing the Emitter resistor of the output stage with a capacitor to act as a low impedance to the pulses. This will help to prevent the pulses from "pulling up" the sawtooth. It will still act as a high impedance as far as the sawtooth is concerned



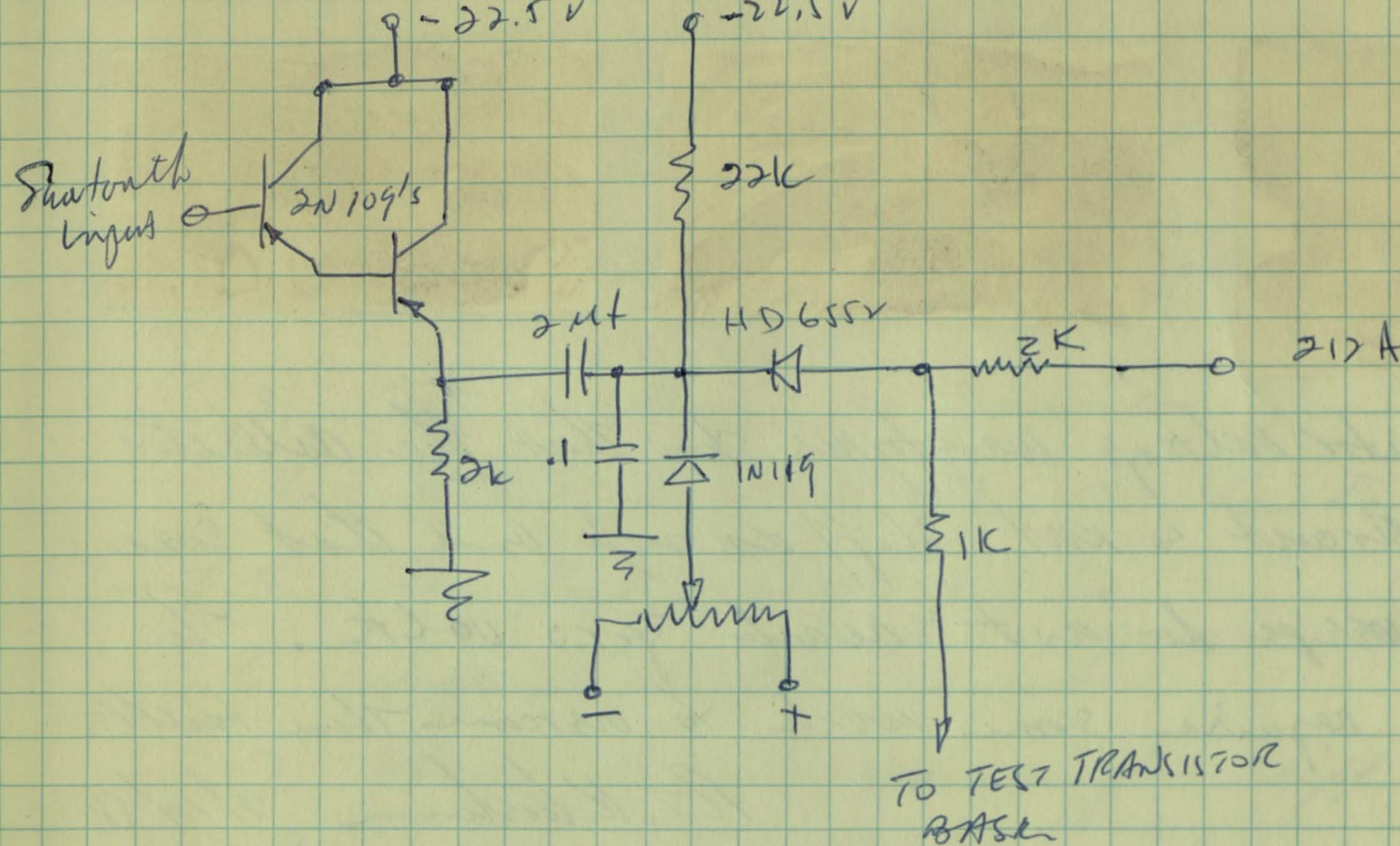
R T Kirkorian 9/8/58

9/9/58

An attempt was made to change the compounded output circuit to NPN's ~~and~~ with ac coupling from the sawtooth shaper instead of dc coupling ~~at~~ at the relatively high power output of the PNP's. This was abandoned because of the severe loading problem on the sawtooth circuit and also because of level shifting at the input of the compounded circuit.

The output circuit now looks something like this.

9/9/58

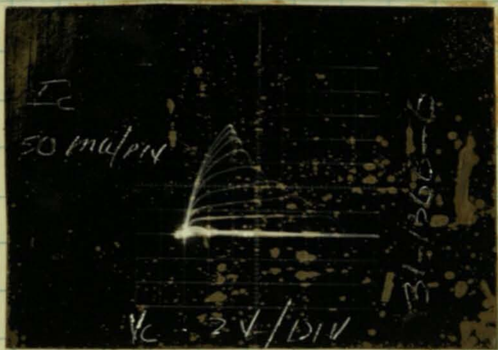


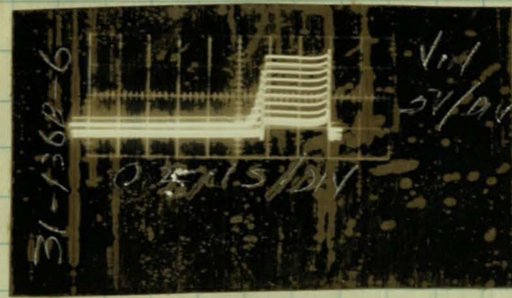
The breadboarded circuit as shown above worked satisfactorily. The maximum base current ~~was~~ is approximately 13 ma. This is adequate for the first pulsed VI genetor.

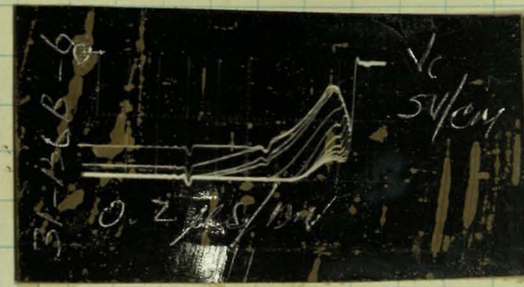
R.T. Kikoshian

9/10/58

The complete breadboarded system was put together and worked satisfactorilly. The $I_c - V_c$ characteristics of a test transistor was displayed on the 536 and pictures were taken of the ~~pulsed~~ collector characteristics, the input voltage steps and the collector voltage. (next page.) ⟶







The collector voltage waveforms show that the collector sweep circuit is not stiff enough and that some of the sweeps do not reach zero volts. This circuit requires some work to overcome these faults.

R.T. [illegible] 9/10/58

9/12/58

The chassis model of the V-I plotter was operated. ~~Circuit~~ The waveforms, in general, were cleaner than the bread board. Some de-bugging is still necessary.

R.T. [illegible]

9/16/58

Took pictures of the V_c-I_c characteristics of a transistor. Also V_c vs time, V_b vs time, ~~and~~ V_{in} vs time, and I_B vs I_c.

Discussed plotter with V Grinich and the following improvements were brought out (suggested)

9/16/58

1. More accurate base current (Larger voltage and resistor)

2. Precision (1%) resistors in all current measuring circuits

3. Try a high β transistor

4. Switch from $V_C - I_C$ to $I_B - I_C$

✓ 5. Try direct probes for I_B

6. Improve blanking circuits

7. Check collector source for stiffness

8. Modify for wider (up to 10 μs) pulses (Start with plug in capacitors in the collector sweep circuits.)

9. Built-in power supply.

Doug Ferris set up the non saturating (diode feedback) circuit. Circuit appeared to be operating correctly. Will make a closer study of the circuit.

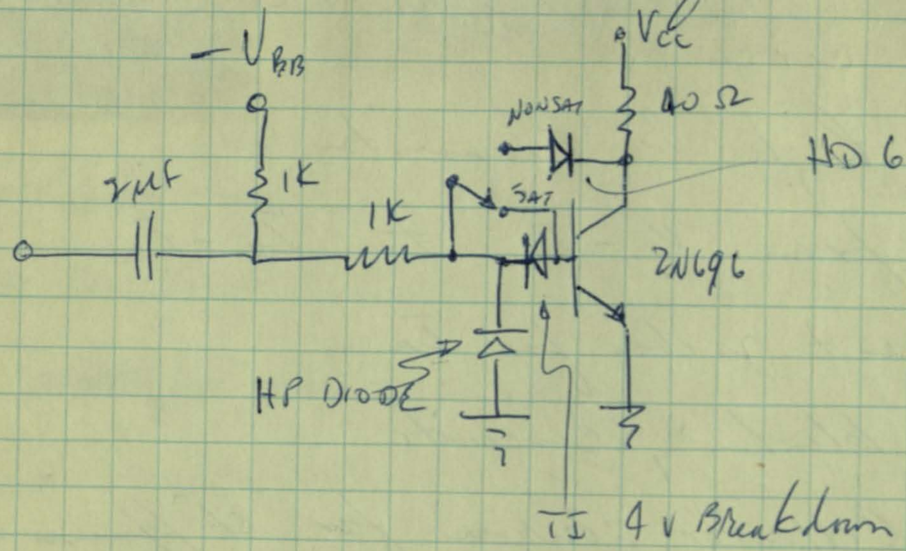
R.T. Kikeshimi

9/18/58

Tried direct probes for I_B (#5 above), but the waveform was too distorted because of the capacity to ground. Also tried the high gain differential, but the bandwidth wasn't wide enough for these pulses.

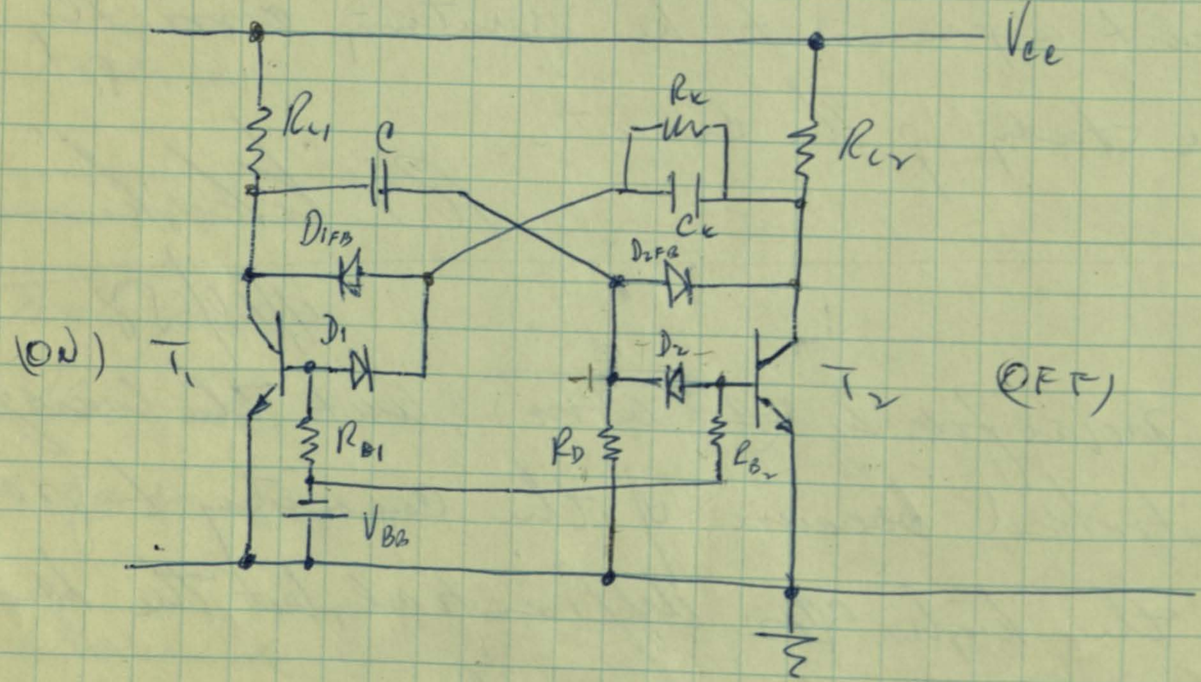
9/22/58

Set up the saturating and non saturating (Diode feedback) circuits on a breadboard for the NEC Display.



The diode feedback circuit work satisfactorily. ~~with~~ Circuit is in good shape for the NEC show.

9/24/58 Resumed work on the non saturating monostable multivibrator.



$V_{CC} = 22.5$ VOLTS $\qquad \beta = 20$

$V_{BB} = 6$ VOLTS

$D_{1FB} = D_{2FB} =$ 1N119

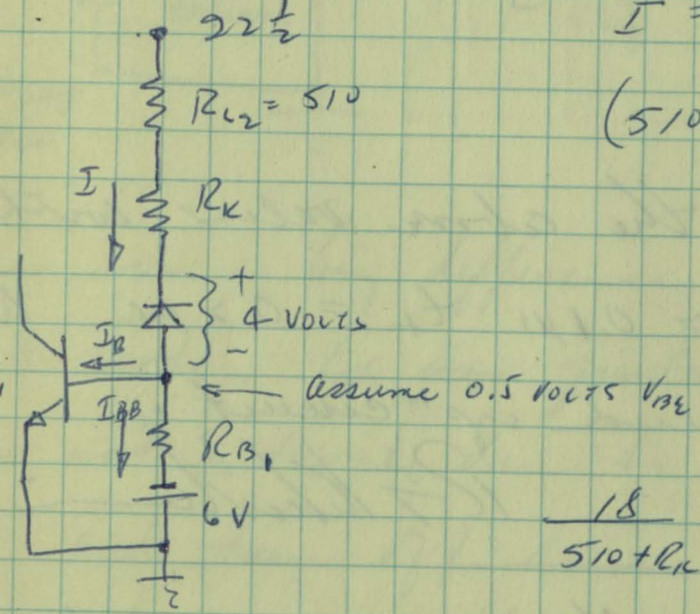
D_1 & D_2 TI 4 VOLT BREAKDOWN DIODE

$T_0 = 3\,\mu s$

R_{L_1} & $R_{L_2} = 510\,\Omega$

T_1, T_2 FAIRCHILD 2N 696

FOR T_1 "ON"



$I = I_B + I_{BB}$

$(510 + R_K)I = 22\tfrac{1}{2} - 4 - 0.5 = 18$

$I_{BB} = \frac{6.5}{R_{B_1}}$

$I_B = \frac{1}{\beta}\,\frac{22.5}{510} = \frac{1}{20}\,\frac{22.5}{510} = .00022$

$= 2.2$ mA

$\frac{18}{510 + R_K} = \frac{0.0022 R_{B_1} + 6.5}{R_{B_1}}$

$18 R_{B_1} = (510 + R_K)(.0022\,R_{B_1} + 6.5)$

Let $R_{B_1} = 3k$

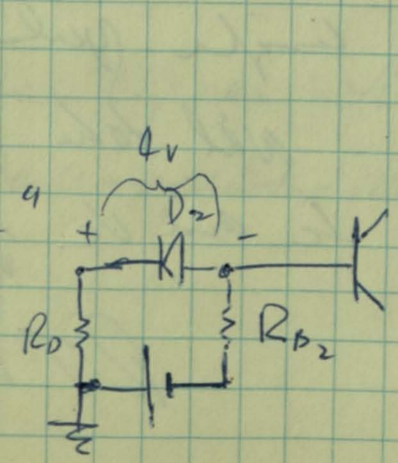
$18(3000) = (510 + R_K)(6.6 + 6.5)$ [13.1]

$54000 = 6670 + 13.1 R_K$

$13.1\,R_K = 47330$

$R_K = 3600\ \Omega$

T_2 "OFF"



Let $R_O = R_{B_2} = 1k$

9/20/58

$$C_K < \frac{(R_K + R_{C2} + R_{B1})\,T_0}{5R_K(R_{C2}+R_{B1})}$$

$$< \frac{(3600 + 510 + 3000)\,3\times10^{-6}}{5\,(1200)(510+3000)}$$

$$< \frac{7110 \times 10^{-6}}{5(1200)(3510)}$$

$$\underline{\underline{< 338\ pf}}$$

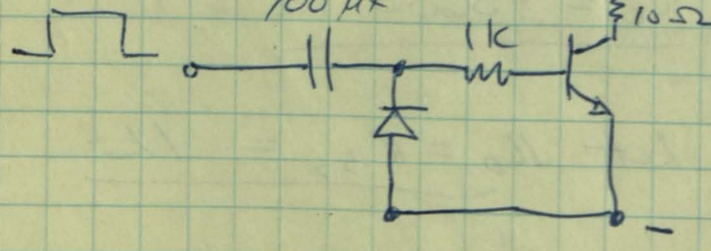
$$C \simeq \frac{3\times10^{-6}}{510 \ln\left[\frac{20(510)(21.5)}{(510)(21.5)\times 30\ 510\ 6)}\right]}$$

$$\underline{\simeq 0.005\ \mu f}$$

Circuit operated with the above values with a T_0 of ~ 3 μsec, $t_r \simeq 0.1 \mu s$ $t_f = 0.2 \mu s$. Will do some work to speed up circuit.

R.T. Kibreslin 9/20/58

9/26/58 Tried to modify the V-I plotter for long pulses (3 ms) but the long time constants make this impossible without a complete redesign. Observed the V_c, I_c for a single pulse.

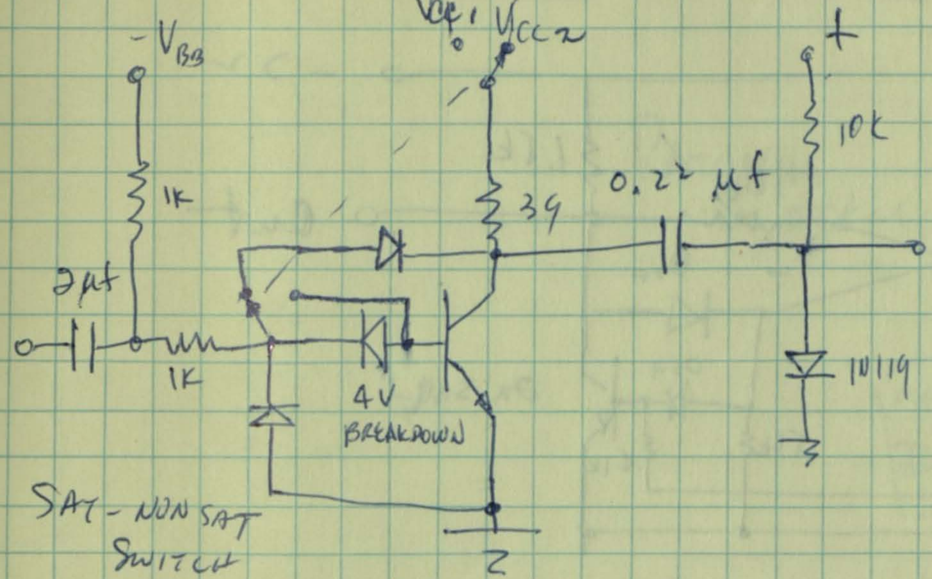


Will take picture of the I_c and V_c of this circuit

R.T. Kibreslin 9/26/58

9/29/58

Continued work on the saturating and non-saturating display for the NEC. The circuit now is as follows



The driver gate needs some work to make it "stiffer". Will try lower resistance gates.

There was a big difference in t_r and t_f in the non-sat mode. t_f was quite a bit shorter than t_r. This was not entirely due to the difference in the turn on and turn off drives caused by the breakdown diode. Will breadboard the circuit again to study this effect

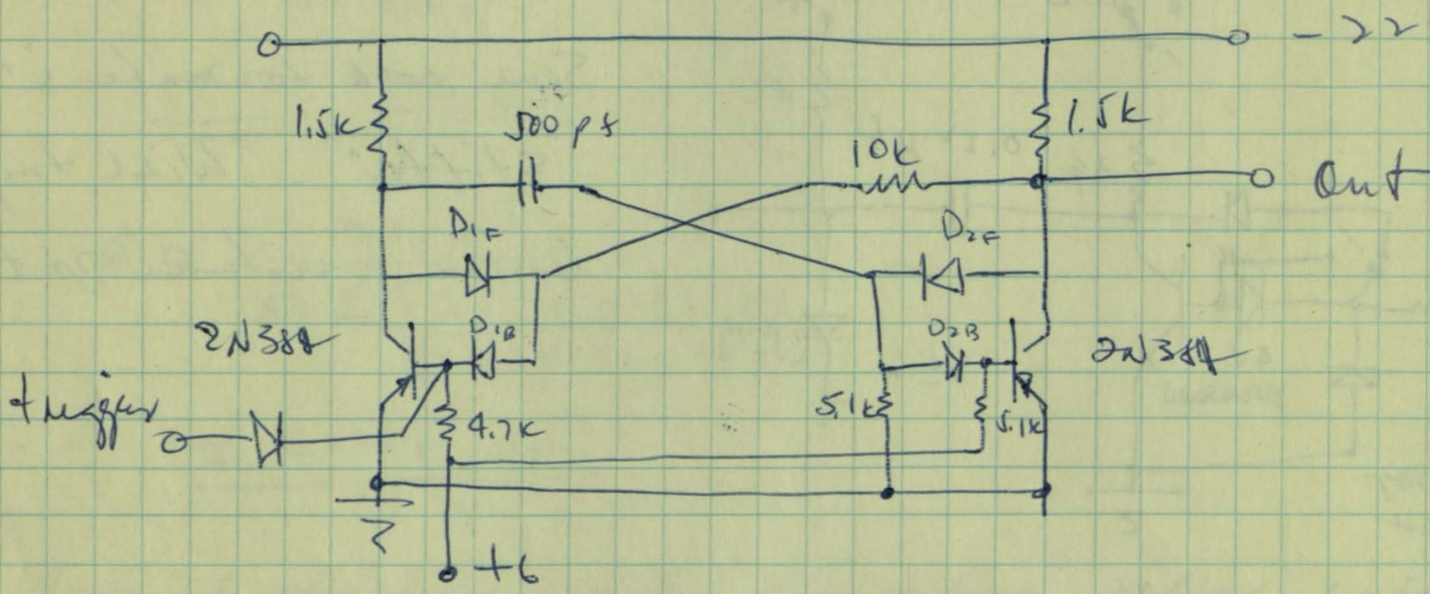
R.T. Kobashima 9/29/58

9-30-58 thru 10/3/58

Worked mainly on the NEC display. The testing circuit was completed and shipped to Chicago on 10/3/58

R.T. Kobashima 10/3/58

10/8/58 In order to get the desired rise time in the non saturating single shot, the following circuit was designed using RCA 2N384 drift transistors.



D1F, D2F Qutronics Q50-750C

D1B, D2B TJ 650C Breakdown diode 4 volts.

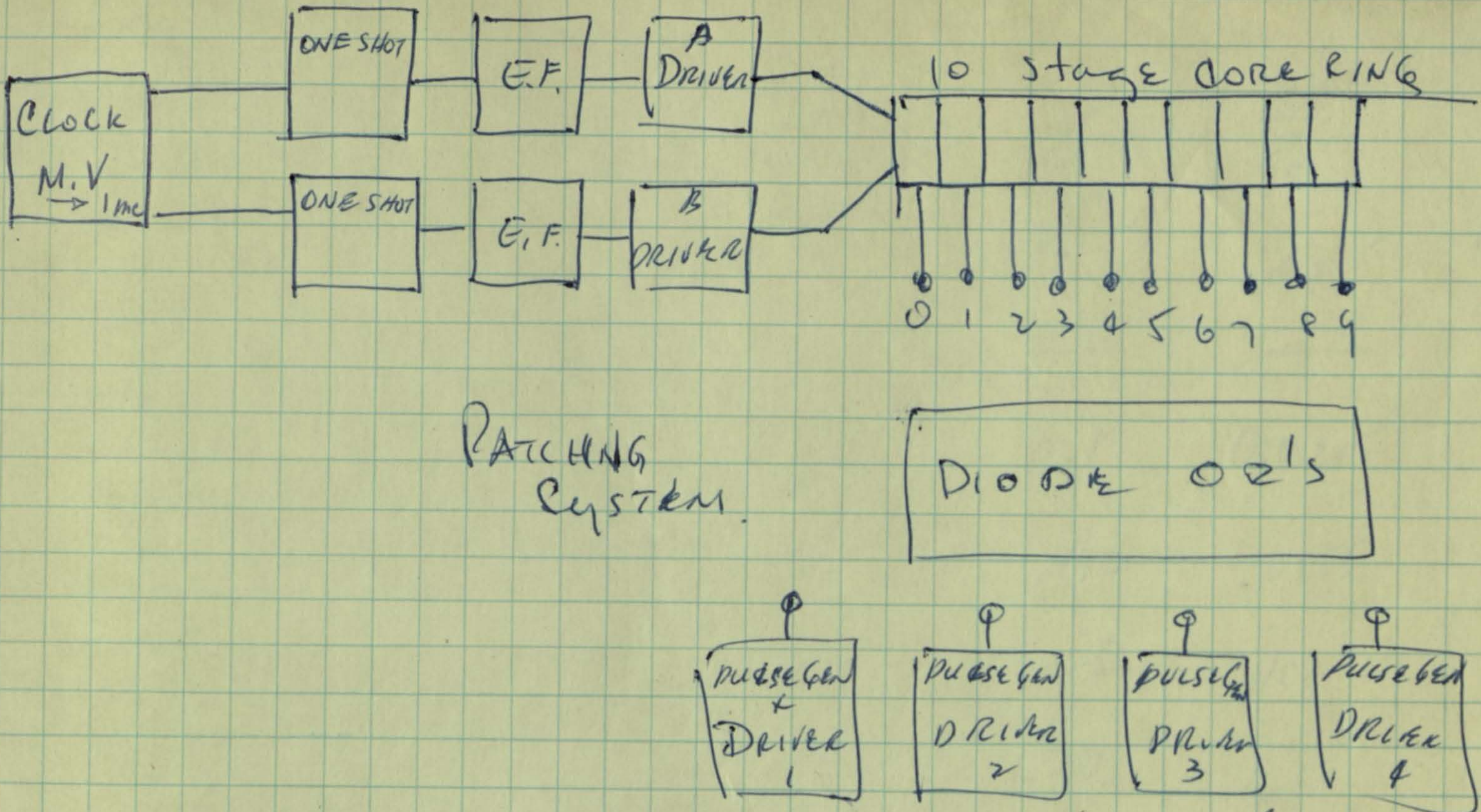
t_{rise} ~ 25 mμs

t_{fall} ~ 360 mμs

t_{width} ~ 1.4 μsec

The fall could not be improved. The output was connected to an emitter follower using a Fairchild 2N696. This circuit is suitable for the pulse programming system in the following way -

10/8/58

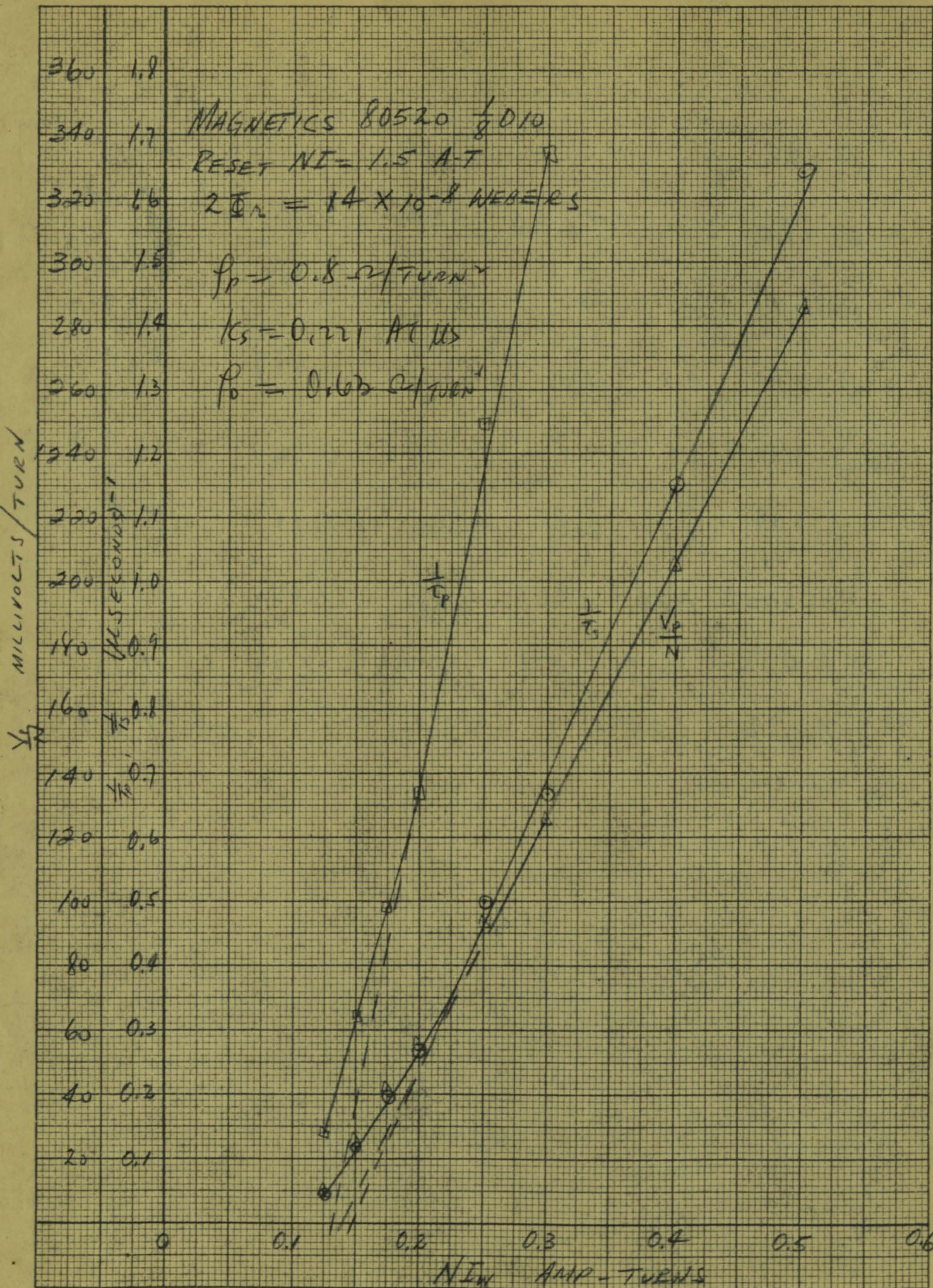


R T Kikoshima 10/8/58

10/9/58

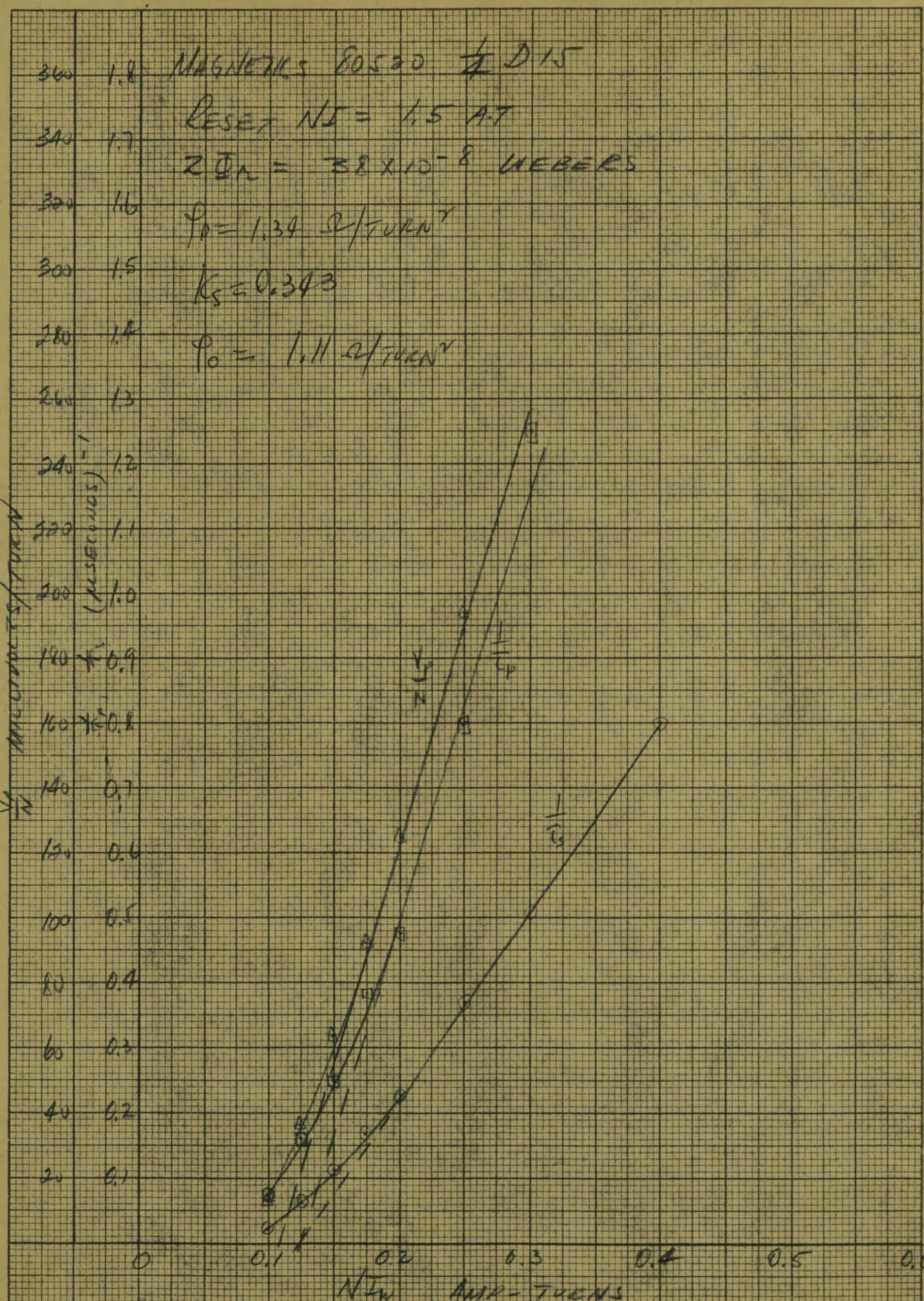
Tested the Magnetics 979 Mo Perm cores as they will be used in the 10 stage ring shown above. The curves and data are on the following page. A ~~suitable~~ suitable core is the 80S-20S D00.

R T Kikoshima 10/9/58


MAGNETICS 80520 1/8 D10
RESET NI = 1.5 A-T
2Φr = 14 X 10^-8 WEBERS
ρp = 0.8 Ω/TURN²
Ks = 0.221 AT us
ρ0 = 0.63 Ω/TURN²
MILLIVOLTS/TURN
(μSECONDS)^-1
1/τp
1/τs
Vp/N
360 340 320 300 280 260 240 220 200 180 160 140 120 100 80 60 40 20
1.8 1.7 1.6 1.5 1.4 1.3 1.2 1.1 1.0 0.9 0.8 0.7 0.6 0.5 0.4 0.3 0.2 0.1
0 0.1 0.2 0.3 0.4 0.5 0.6
NIw AMP-TURNS

KTK
10/9/58

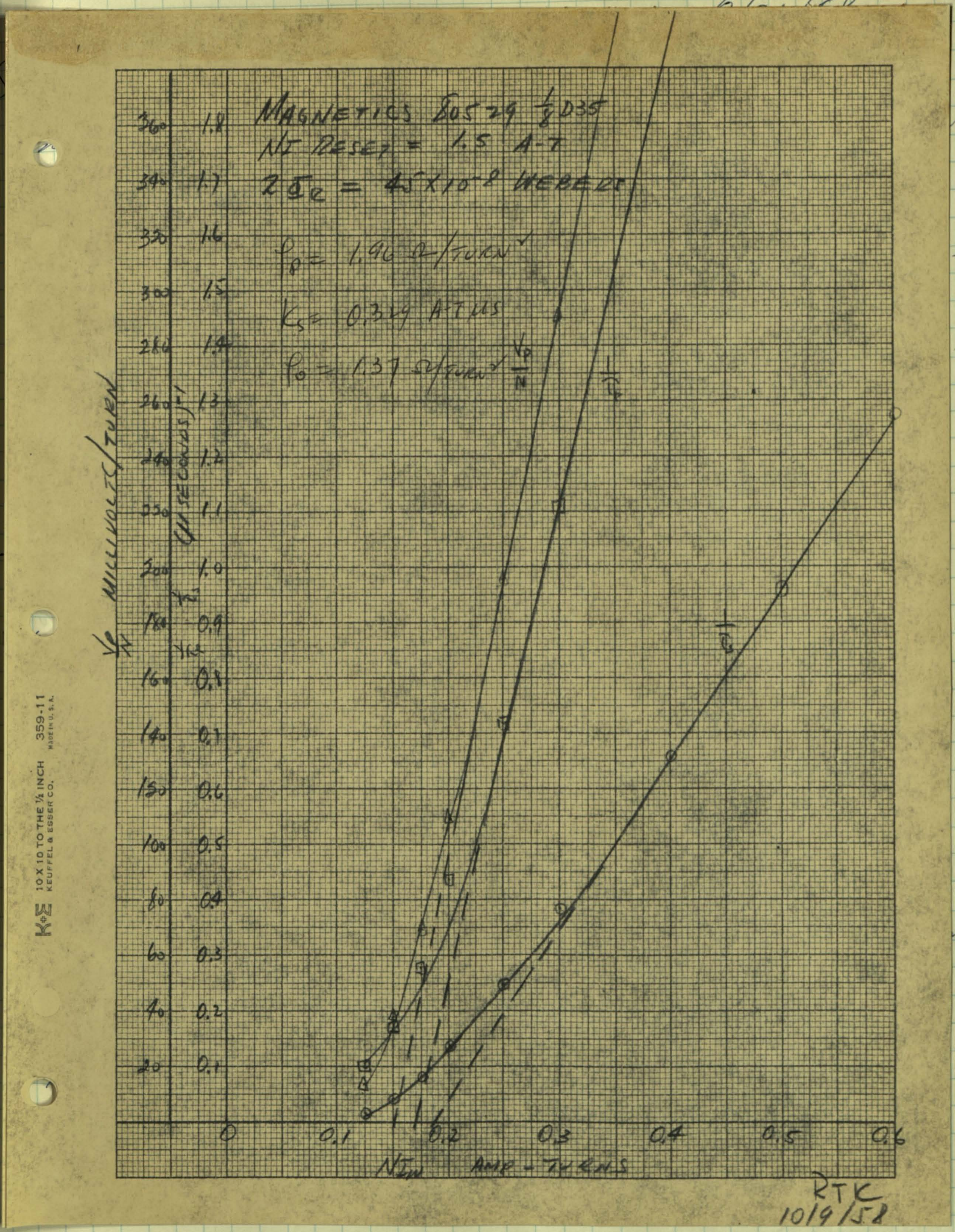
NI	V_p/N	T_p	T_s	$1/T_p$	$1/T_s$
A-T	mV/T	μs	μs	μs^{-1}	μs^{-1}
0.1	—	—	—		
0.125	16.4	6.5	33	0.154	0.03
0.150	35	3.7	13.9	.270	.072
0.175	62	2.3	6.8	.435	.147
0.200	90	1.65	4.7	.606	.213
0.250	165	0.9	2.5	1.11	.40
0.300	230	0.64	1.64	1.56	.61
0.400	365	0.34	0.96	2.94	1.04
0.500	520	0.2	0.68	5.0	1.47



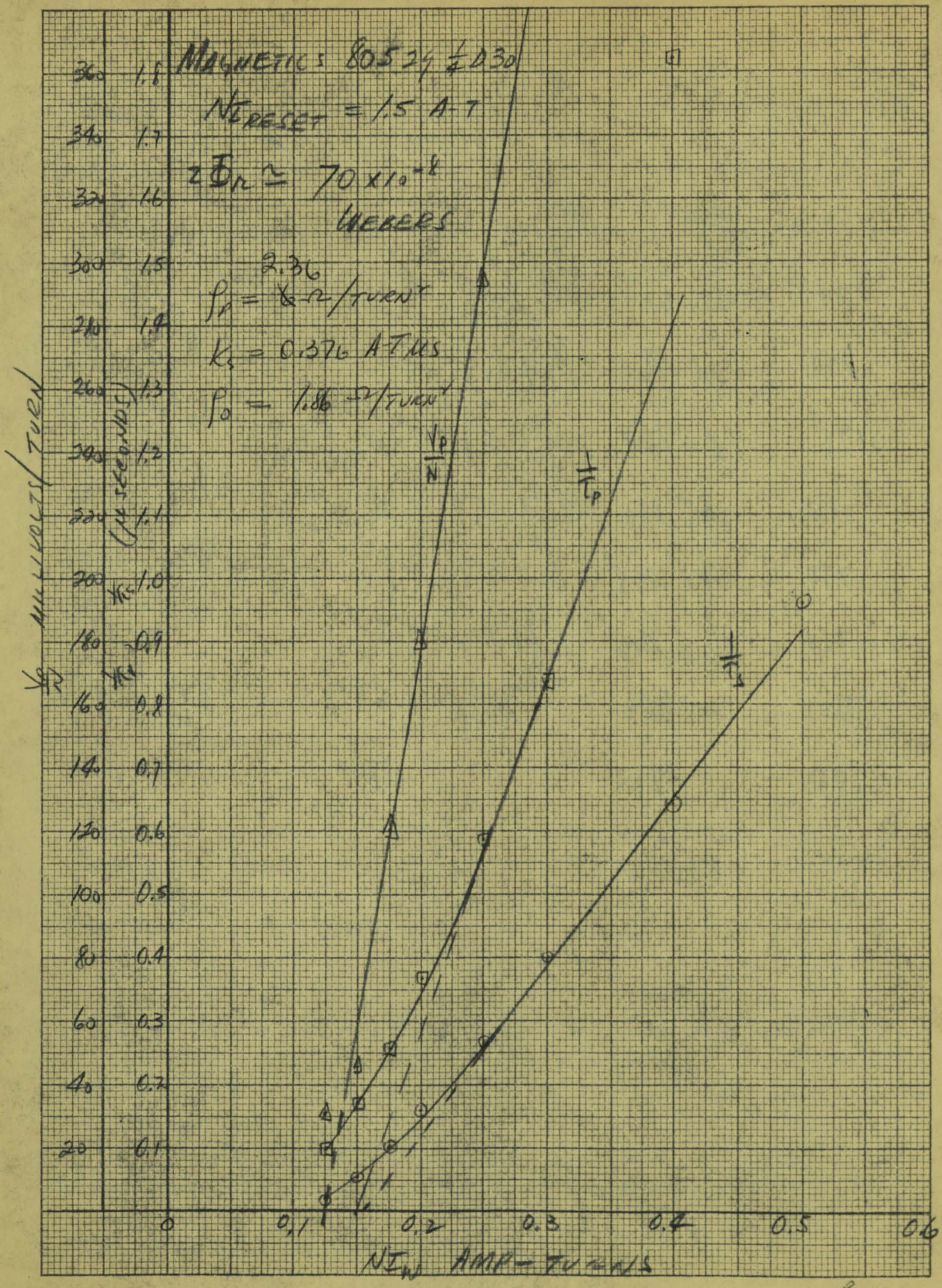
MAGNETICS 80520 ½ D 15
RESET NI = 1.5 A-T
$2\Phi_r$ = 38 × 10⁻⁸ WEBERS
ρ_p = 1.34 Ω/TURN²
k_s = 0.343
ρ_0 = 1.11 Ω/TURN²
V_p/N MILLIVOLTS/TURN
$\frac{1}{\tau}$ (μSECONDS)⁻¹
$\frac{1}{t_p}$
$\frac{1}{t_s}$
NI_w AMP-TURNS

RTK
10/9/58

NI	$\frac{V_D}{N}$	T_D	T_S	$\frac{1}{T_D}$	$\frac{1}{T_S}$
A-T	mV/TURN	μs	μs	μs^{-1}	μs^{-1}
0.100	14 mV	13	43	.077	.023
0.125	36	6.2	16.2	.161	.062
0.150	63	4.	8.9	.250	.112
0.175	92	2.6	5.9	.384	.170
0.200	125	2.1	4.4	.476	.227
0.250	187	1.25	2.7	.8	.370
0.300	250	0.8	1.99	1.25	.503
0.400	400		1.25		.8


MAGNETICS 80529 1/8 D35
NI RESET = 1.5 A-T
2Φr = 45 X 10^-8 WEBERS
ρp = 1.96 Ω/TURN
Ks = 0.319 A-T μS
ρo = 1.37 Ω/TURN
Vp/N
1/τs
1/τ
Vp/N MILLIVOLTS/TURN
1/τ (μSECONDS)^-1
NI_IN AMP - TURNS
RTK
10/9/58
10 X 10 TO THE 1/2 INCH
KEUFFEL & ESSER CO.
359-11
MADE IN U.S.A.

NI (A-T)	V_0/N (mV/T)	T_p (μs)	T_s (μs)	$1/T_p$ ($μs^{-1}$)	$1/T_s$ ($μs^{-1}$)
0.1	—	—	—	—	—
0.125	13.5	10	69	0.1	0.014
.150	38	6	24	.167	.042
.175	69	3.6	12.2	.278	.082
.200	110	2.3	7.2	.435	.139
.250	195	1.4	4.0	.714	.250
.300	590	0.9	2.6	1.11	.385
.400	960	0.5	1.53	2.0	.654
.500	640	0.33	1.04	3.03	.962
.600	850	—	0.79		1.27

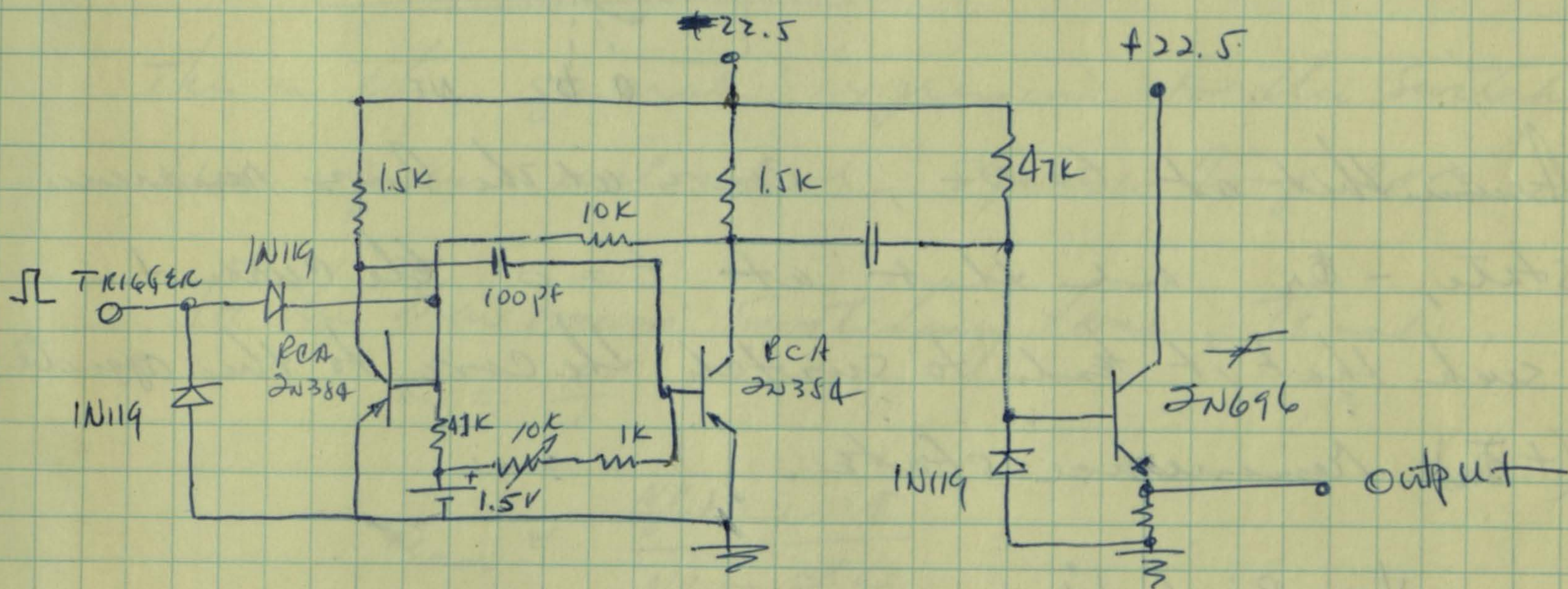

MAGNETICS 80524 1/4 D30
NI_{RESET} = 1.5 A-T
$2\Phi_r \simeq 70 \times 10^{-8}$ WEBERS
ρ_r = 2.36 Ω/TURN²
k_s = 0.376 AT μs
ρ_0 = 1.86 Ω/TURN²
V_p/N
$1/\tau_p$
$1/\tau_s$
V_p/N MILLIVOLTS / TURN
(μ SECONDS)
NI_W AMP-TURNS
0 0.1 0.2 0.3 0.4 0.5 0.6
20 40 60 80 100 120 140 160 180 200 220 240 260 280 300 320 340 360
0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8

RTK
10/9/58

NI	$\frac{V_p}{N}$	T_p	T_s	$\frac{1}{T_p}$	$\frac{1}{T_s}$
AT	mV/T	μs	μs	μs⁻¹	μs⁻¹
0.100	~~37~~	~~10~~	—	—	—
.125	31	10	46.5	0.1	0.0215
.150	96	5.8	18	.172	.0555
.175	120	3.9	9.9	.256	.101
.200	180	2.7	6.2	.37	.161
.250	295	1.7	3.8	.588	.264
.300	400	1.2	2.5	.833	.40
.400	660	0.55	1.55	1.82	.645
.500	950		1.04		.961

10/21/58

Single shot for core drive circuitry:
Since there appeared to be no advantage to the non-saturating (diode feedback) circuit for this (core driver pulse source) application, the following standard single shot MV was designed:

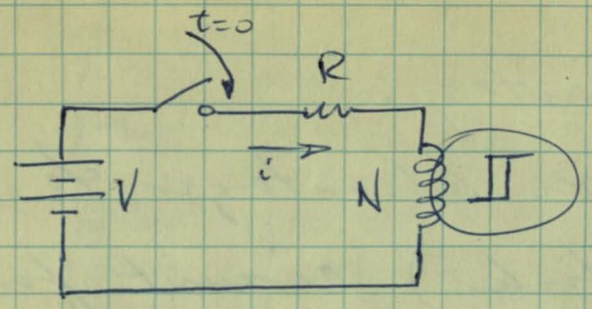


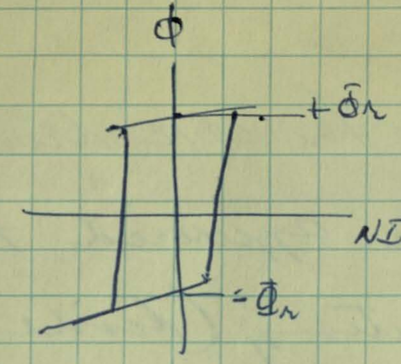
This circuit had the best fall characteristic of the circuits tried.

Pluggable unit are being built for the system shown on page 55.

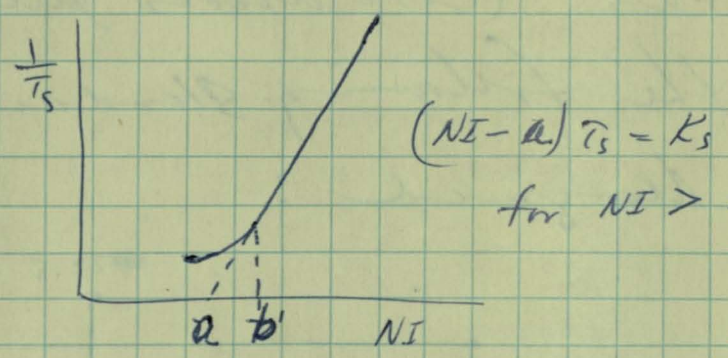
Reviewed some of the terminal properties of square loop cores (next page)

 10/31/58 continued





Core characteristics as shown



Assume that at $t = 0-$, core is at the lower remanence state, $-\Phi_r$ and that at $t = 0$ the current i such that it tends to switch the core to the opposite ($+\Phi_r$) remanence state.

$$V = Ri + N\dot{\phi}$$

Let $\Phi = 2\Phi_r$

$$\int_0^{T_s} v\,dt = R\int_0^{T_s} i\,dt + N\int_0^{T_s} \dot{\phi}\,dt$$

Choose $T_s \ni N\int_0^{T_s} \dot{\phi}\,dt = \Phi$

$$VT_s = R\int_0^{T_s} i\,dt + N\Phi \qquad \text{for } \frac{NV}{R} > b$$

Now $\int_0^{T_s} (Ni - a)\,dt \simeq K_s$

10/31/58 Continued

$$VT_s = \frac{R}{N}\int_0^{T_s}(Ni - a)\,dt + \frac{R}{N}\int_0^{T_s} a\,dt + N\Phi$$

$$VT_s \simeq \frac{R}{N}K_s + \frac{R}{N}aT_s + N\Phi$$

$$\left(V - \frac{Ra}{N}\right)T_s \simeq \frac{R}{N}K_s + N\Phi$$

$$T_s \simeq \frac{RK_s + N^2\Phi}{NV - Ra} \quad \text{for } \frac{NV}{R} > b$$

This is the general expression for the switching time of an unloaded square loop core.

For the maximum switching time, $T_{s\,max}$,

$$R = \frac{NV}{b}$$

$$T_{s\,max} \simeq \frac{\frac{NV}{b}k_s + N^2\Phi}{NV - \frac{NV}{b}a}$$

$$T_{s\,max} \simeq \frac{K_s + \frac{N\Phi}{V}}{b - a}$$

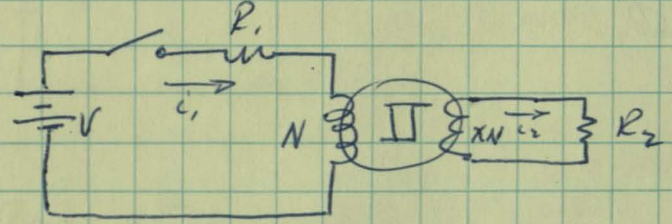
And for $V \gg N\Phi$

$$T_{s\,max} \simeq \frac{k_s}{b - a}$$

R. T. Kekoshian
10/31/58

10/22/58

Considered the case of a square loop core loaded with a purely resistive load using the same analysis as p 58, 59



$$V = R_1 i_1 + N\dot{\phi} \qquad (1)$$

$$xN\dot{\phi} = R_2 i_2 \qquad (2)$$

$$N i_1 = xN i_2 + (Ni)_{net} \qquad (3)$$

$$\int_0^{T_s} \left[(Ni)_{net} - a \right] dt = K_s \qquad (4)$$

Substituting (3) in (1)

$$V = \frac{R_1}{N}\left[xN i_2 + (Ni)_{net} \right] + N\dot{\phi} \qquad (5)$$

and (2) into (5)

$$V = \frac{R_1}{N}\left[\frac{x^2 N^2 \dot{\phi}}{R_2} + (Ni)_{net} \right] + N\dot{\phi}$$

$$V = \left[\frac{R_1 x^2}{R_2} + 1 \right] N\dot{\phi} + \frac{R_1}{N}\left[(Ni)_{net} - a \right] + \frac{R_1 a}{N} \qquad (6)$$

Integrating (6) from $0 \rightarrow T_s$

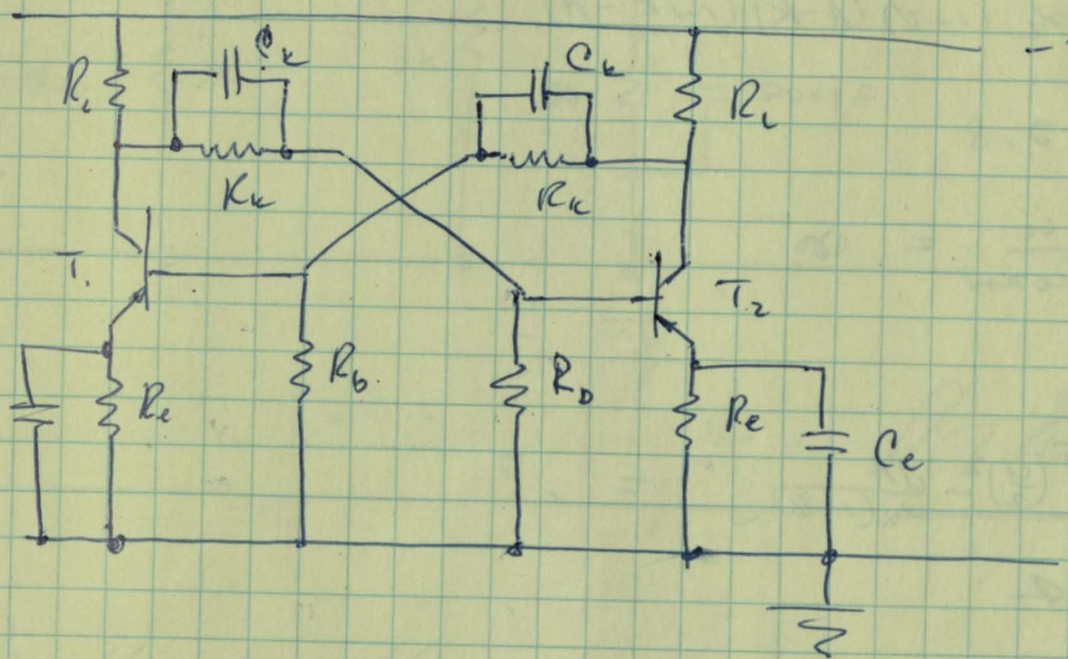
$$\left[\int_0^{T_s} \right] \quad V T_s \cong \left[\frac{R_1 x^2}{R_2} + 1 \right] N\Phi + \frac{R_1 K_s}{N} + \frac{R_1 a}{N} T_s$$

$$\boxed{T_s \cong \frac{\left[\frac{R_1 x^2}{R_2} + 1 \right] N^2 \Phi + R_1 K_s}{NV - R_1 a}} \qquad (8a) \quad (7)$$

This is the general expression for the switching time of a core loaded with a resistive load

10/22/58 Cont

Designing 1 mc multivibrator (free running) for the core driver clock using the procedure outlined in "Transistor Circuit Engineering", Shea pp 250 — 255



Given: $V = 22.5\ v$
$\Delta v_c = 15\ V$
$\Delta i_c = 10\ ma$
$f = 10^6\ cps$
T_1, T_2 RCA 2N384 drift

$A = \frac{\Delta v_c}{V} = \frac{15}{22.5} = 0.67$

$A > K >> \left|\frac{v_{BE}}{V}\right|$

$.67 > K >> .009$

choose $K = 0.2$

$\psi = \frac{1}{K}\left[\frac{v_{BE}}{V}\right] = 0.045$

10/22/58 (Cont)

$$u > \frac{(1-K)^2}{1-K-\frac{A}{\alpha_{bo}(1-\nu)}} = 6.4$$

$$\alpha_{eo} \gg u > \frac{A}{\alpha_{bo}(1-\nu)(A-K)(1+K-A)}$$

$$60 \gg u > 2.8$$

$$u \ll \frac{\Delta i_c}{I_{co\,max}} = 100$$

Let $u = 7$

$$(KX) = \frac{u}{2} - \left[\left(\frac{u}{2}\right)^2 - \frac{uA}{\alpha_{bo}(1-\nu)}\right]^{\frac{1}{2}} = .8$$

$$X = \frac{.8}{2} = 4$$

$$R_e = \frac{KV}{\alpha_{oo}\Delta i_c}(1-\nu) = 443\ \Omega$$

$$R_c = X R_e = 1772\ \Omega$$

$$R_b = u R_e = 3001\ \Omega$$

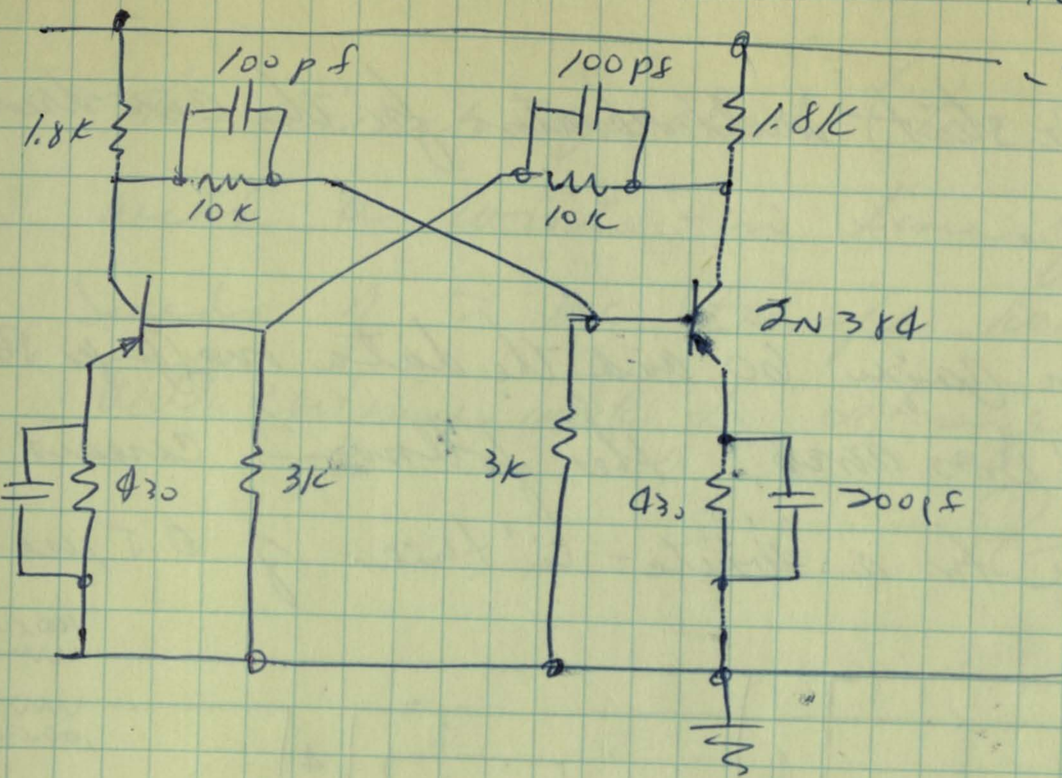
$$R_k = ~~(\frac{u}{K}+u+X) R_d~~ \left(\frac{u}{K} - u - X\right) R_e = 10,600\ \Omega$$

$$C_k = \frac{-1}{2 f R_k K\left(1+\frac{X}{u}\right) \ln\left[\left(\frac{1-A}{A}\right)\left(\frac{K+\frac{KX}{u}}{1-K-\frac{KX}{u}}\right)\right]}$$

$$= 100\ pf$$

$$\frac{1}{2\pi f_1 R_e} > C_e \gg \frac{1}{R_e \omega_{ab}}$$

$$330\ pf > C_e \gg 3.3\ pf$$

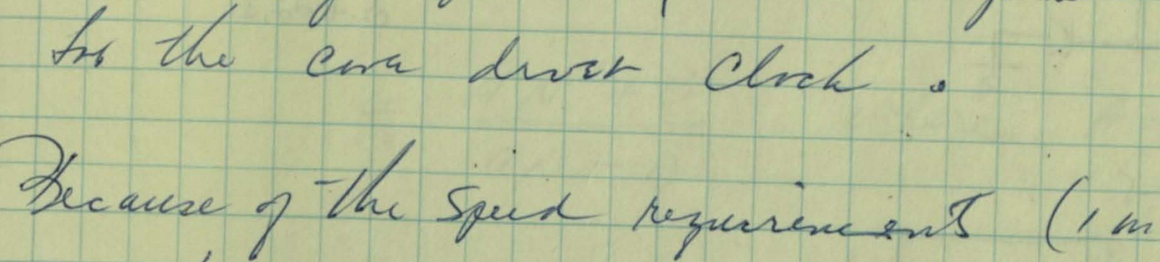


[signature] 10/22/58

10/23/58

Breadboarded the circuit as shown above. The frequency was approximately 500kc. Will add a frequency and symmetry control for the core drive clock.

Because of the speed requirements (1 mc) the following core-transistor ring circuit is being considered:

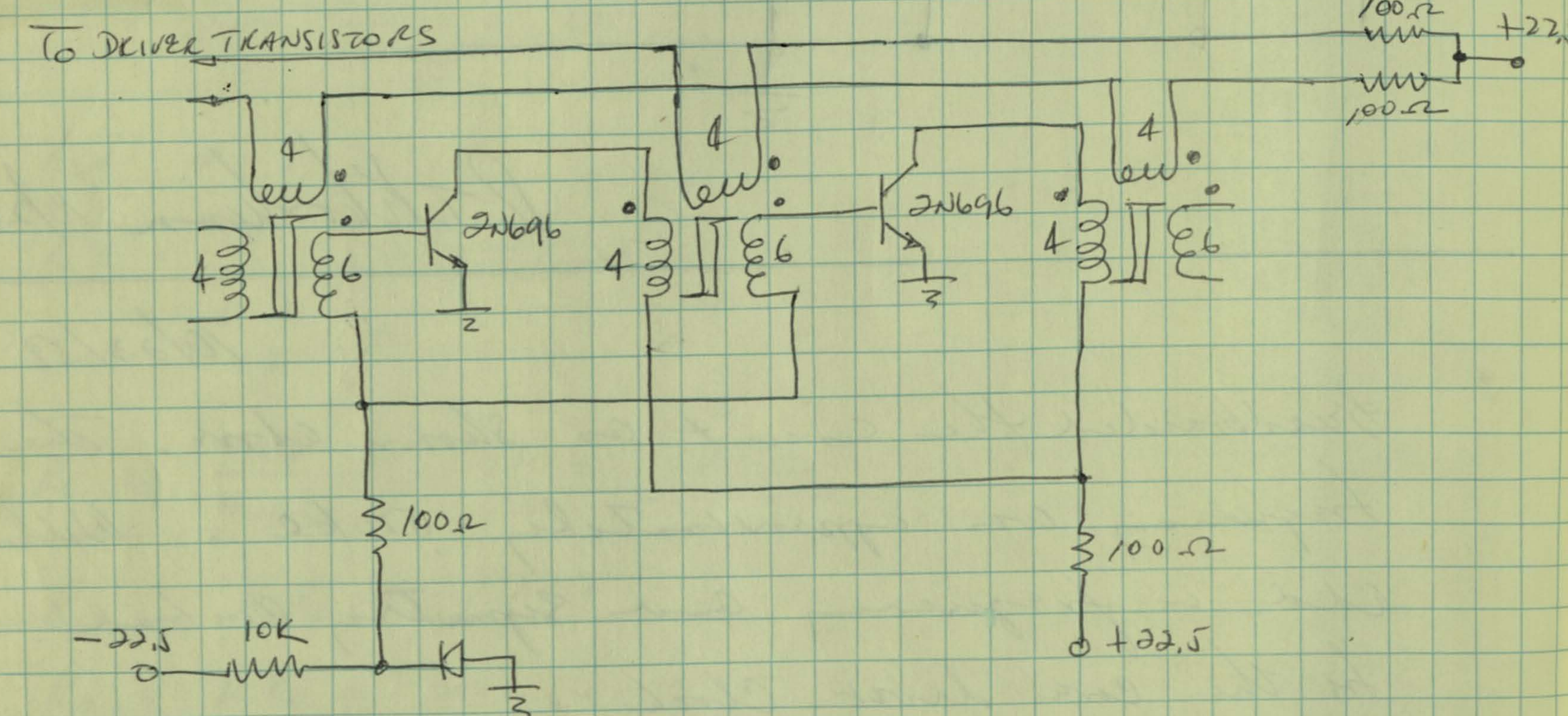


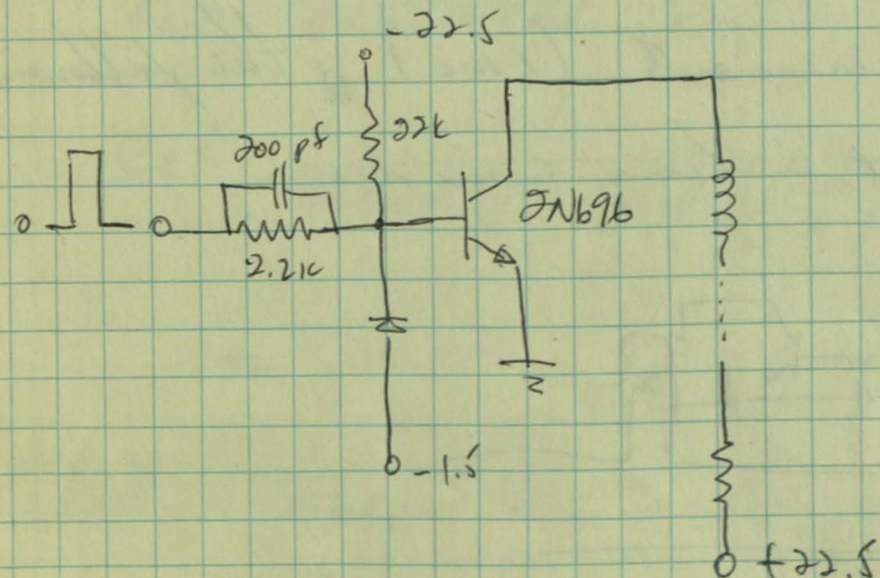
[signature] 10/23/58

10/27/58

The MV and one shot multivibrators for the core driver were completed.

Using eqn (7) on page 60 and the data on page 56 for the 80520 & D20 cores, the following circuit was designed for a "write-in" time of 0.5 μsec





DRIVER CIRCUIT

10/27/58 Cont

The circuit operated (two stages) as shown with a write-in time of 0.7 μsec. Speeds of > mc (transfer rate) are indicated. Will continue work to optimize circuit.

R. T. Kirkpatrick 10/27/58

10/28/58

Examined the equation for switching time, T_s, on page 60 to determine the condition(s) for minimum T_s.

$$T_s = \frac{\left[\frac{R_1}{R_2}x^2 + 1\right] N^2 \Phi + R_1 K_s}{NV - R_1 a}$$

$$= \frac{AN^2 + B}{CN - D} \quad \text{where } A = \left[\frac{R_1}{R_2}x^2 + 1\right]\Phi$$

$$B = R_1 K_s$$

$$C = V$$

$$D = R_1 a$$

Considering N as a continuous (rather than discrete) variable:

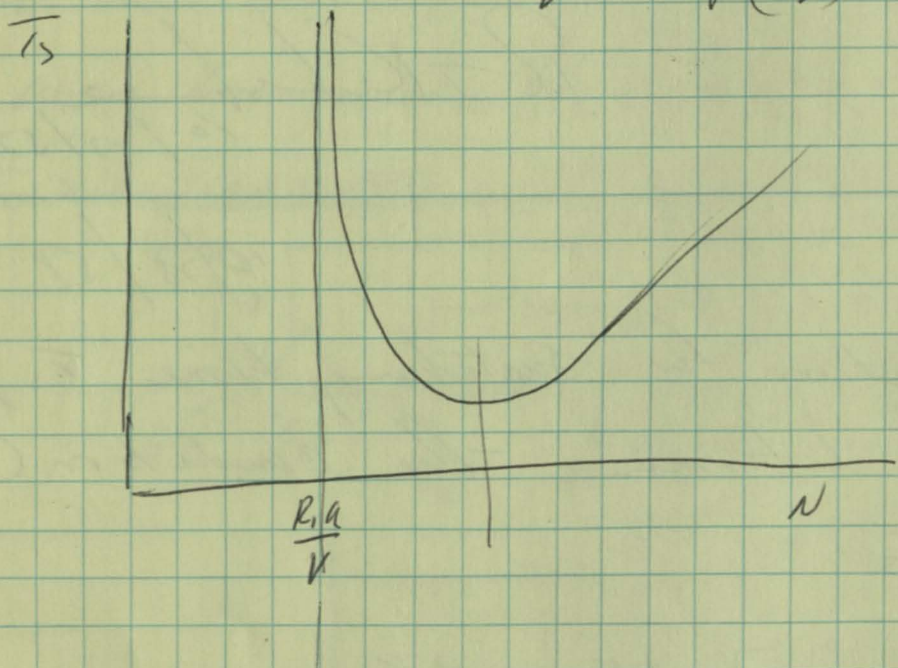
$$\frac{dT_s}{dN} = \frac{(CN-D)\,2AN - (AN^2+B)C}{(CN-D)^2} = 0$$

10/28/58, cont.

The N for minimum T_s is

$$N = \frac{D}{C} \pm \sqrt{\left(\frac{D}{C}\right)^2 + \frac{B}{A}}$$

$$= \frac{R_1 a}{V} \pm \sqrt{\left(\frac{R_1 a}{V}\right)^2 + \frac{R_1 k_s}{\left[\frac{R_1}{R_2} x^2 + 1\right]\Phi}} \qquad [1]$$



For a given core with constants Φ, k_s and a
T_s is kept small or minimized by choosing

- Large V
- Large R_2
- Small R_1
- $N = \frac{R_1 a}{V} + \sqrt{\left(\frac{R_1 a}{V}\right)^2 + \frac{R_1 k_s}{\left(\frac{R_1}{R_2} x^2 + 1\right)\Phi}}$

For $R_1 = R_2 = 100\ \Omega$, $V = 32.5V$, $x = 1.5$,

$N(\min T_s) \cong 6$ turns.

Will check this result experimentally

R. H. Kenkima[?]
10/28/58

10/29/58

Core 80570 $\frac{1}{8}$D20:
$\Phi = 0.3 \times 10^{-6}$ webers
$K_s = 0.231 \times 10^{-6}$ A-T sec
$a = 0.16$ A-T

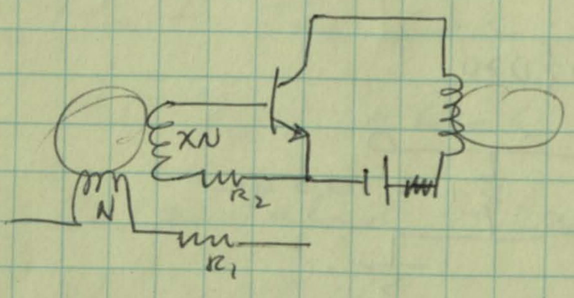
CHOOSE
$V = 22.5$ VOLTS
$R_1 = 100\,\Omega$
$R_2 = 100\,\Omega$
$x = 1$

WITH the above values, calculated N for minimum T_s using [1] on page 66.

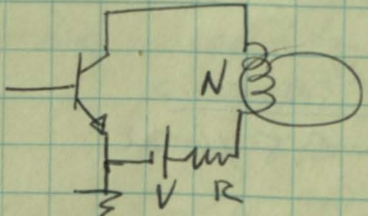
$N(T_{s\,min}) = \underline{6}$

$T_{s\,min} = \underline{0.375\ \mu s}$ USING [7] on p 60

This is for the drive - transfer case



For the write-in case, let the T_s equal to the switching time of the drive-transfer case



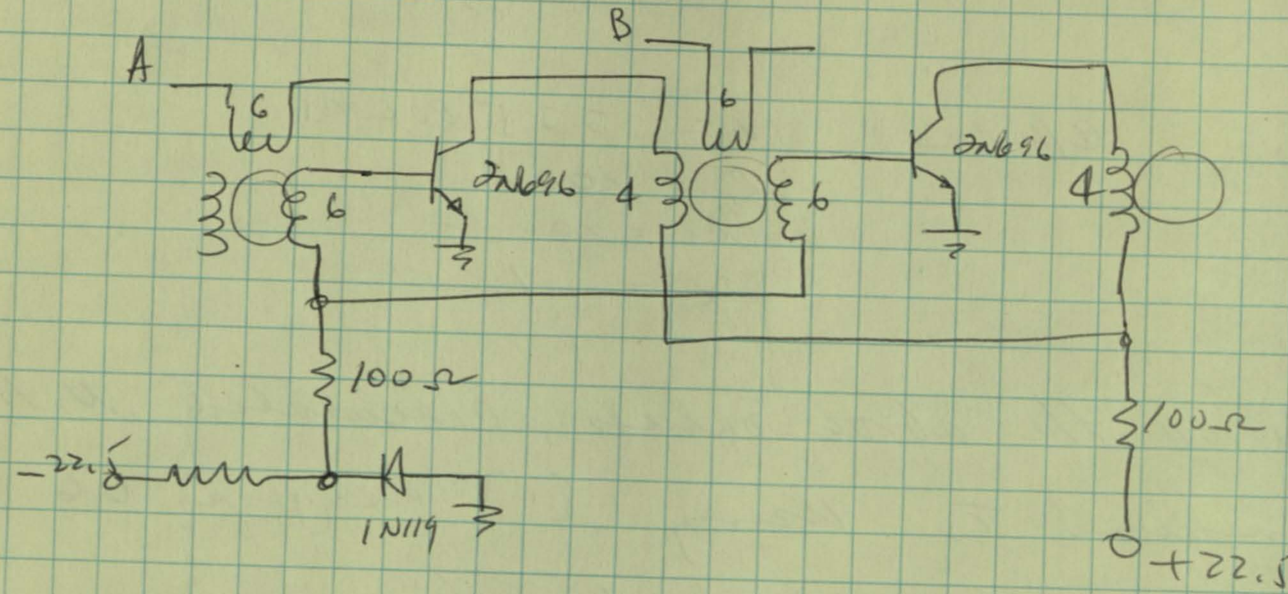
$$T_s = \frac{N^2\Phi + R_1 K_s}{NV - R_1 a}$$

$$.375 = \frac{N^2(.3) + (100)(.23)}{22.5V - (100)(.16)}$$

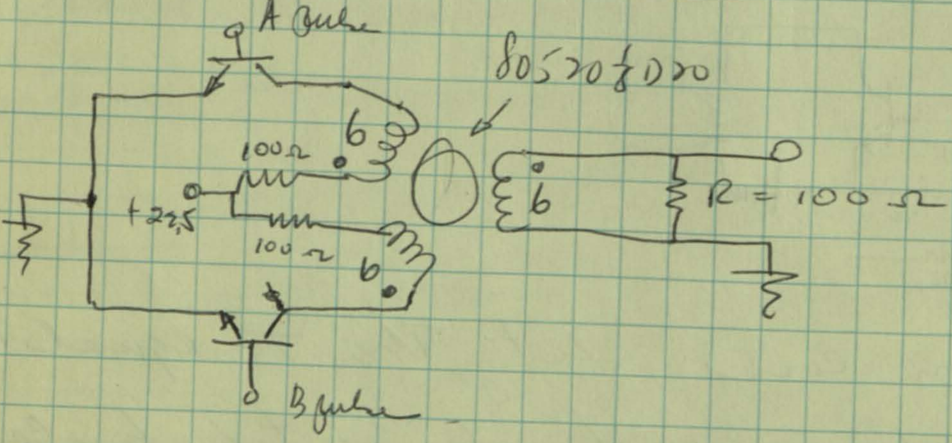
$\underline{N = 4}$

10/29/57 cont.

The ring circuit thus is, as follows, optimized for minimum transfer time:



As a one point check on the accuracy of eqn [7] on page 60, the following circuit was set up



Measured the switching time with R = 100 and R = ∞

	MEASURED	CALCULATED
T_s (R = 100)	0.5 μsec	0.375 μsec
T_s (R = ∞)	0.37 μsec	0.284 μsec

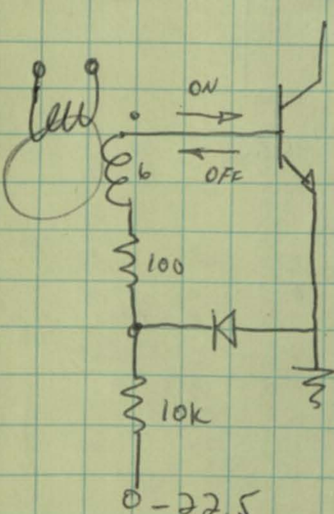
10/29/58 cont

Part of the difference could be due to the non step fn drive of the transistors.
Will do some more work to determine the accuracy of [7] on page 60 —

R T Hubschman 10/29/58

10/30/58

The "writing in" time of the core transistor ring was found to be much larger than the calculated switching time of the core (measured from base to ground). Observing the output of another winding indicated that the core was switching in 950 mμs which is much closer to the calculated value. The reason for the large difference in the turn off time is that the "off" base current (after Nφ goes to zero) was sufficient to back bias the diode resulting in a very high impedance base circuit. This accounts for the long time required to clear out the base circuit. The diode was replaced by a 1.5 volt battery and the "writing in" time was reduced to 0.6 μsec.



10/30/58 Continued

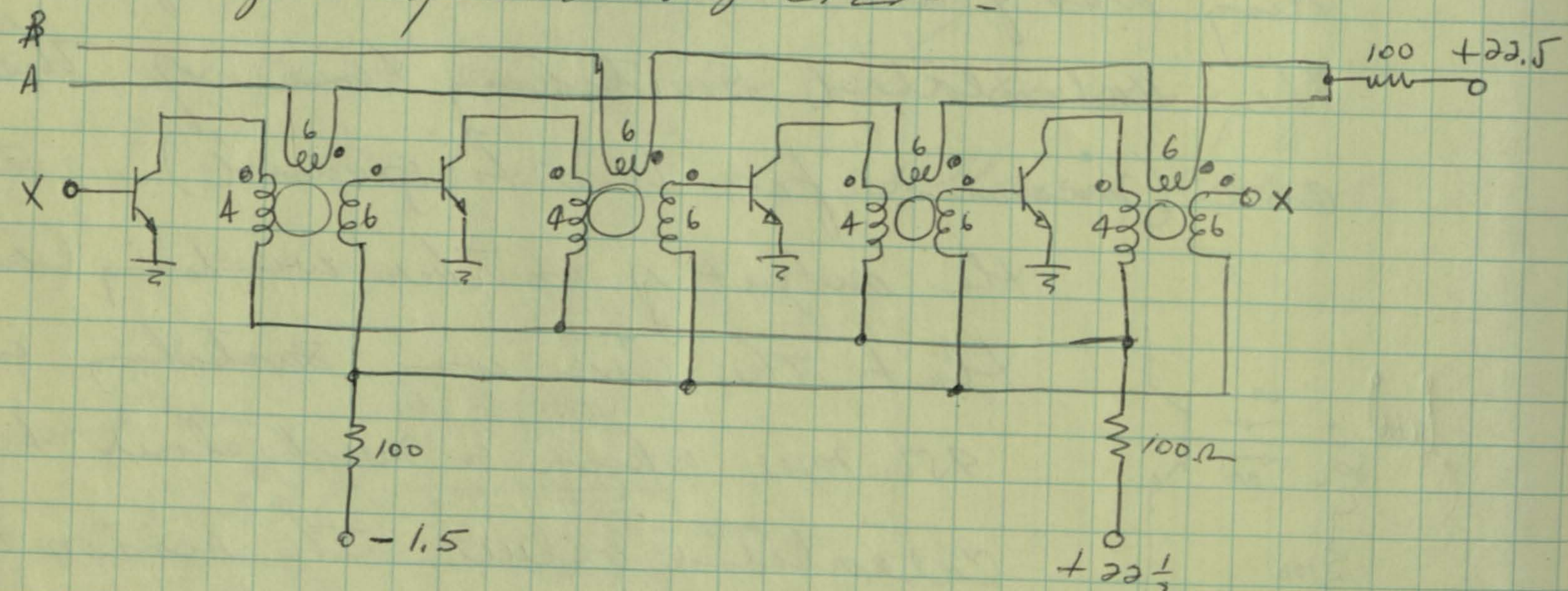
This now approached the core switching time of 0.5 μsec.

Started work on a four stage ring.

R. T. Rikoskinen[?]
10/30/58

10/31/58

The four stage ring was completed.



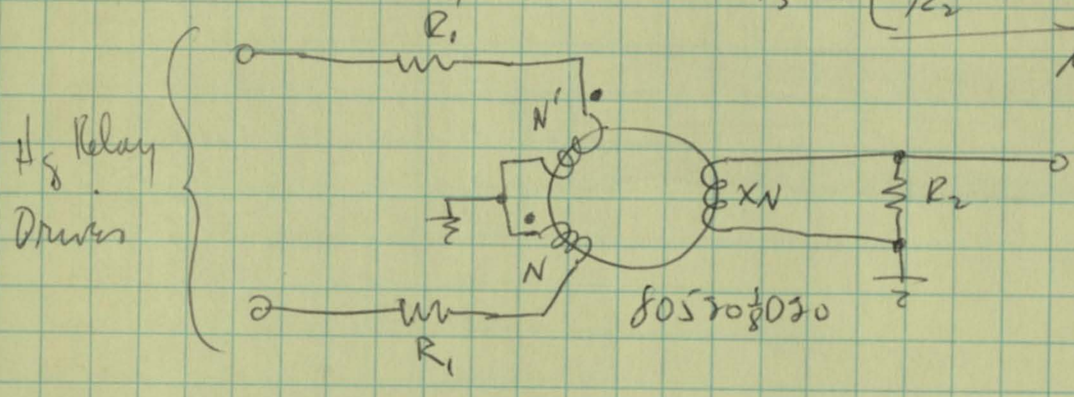
CORES: 80520 ⅛D 20 Magnetics Inc
TRANSISTORS 2N696/7

Transfer time was approximately 0.6 μseconds. The operation was solid and there was no tendency for the ring to pick up extra bits. Extra bits are discouraged by the common 100 Ω collector and base returns.

10/31/58

To check the accuracy of the equation for switching time, (7) p. 60, the following experiment was performed —

$$T_s = \frac{\left[\frac{R_1 x^2}{R_2} + 1\right] N^2 \Phi + R_1 K_s}{NV - R_1 a}$$



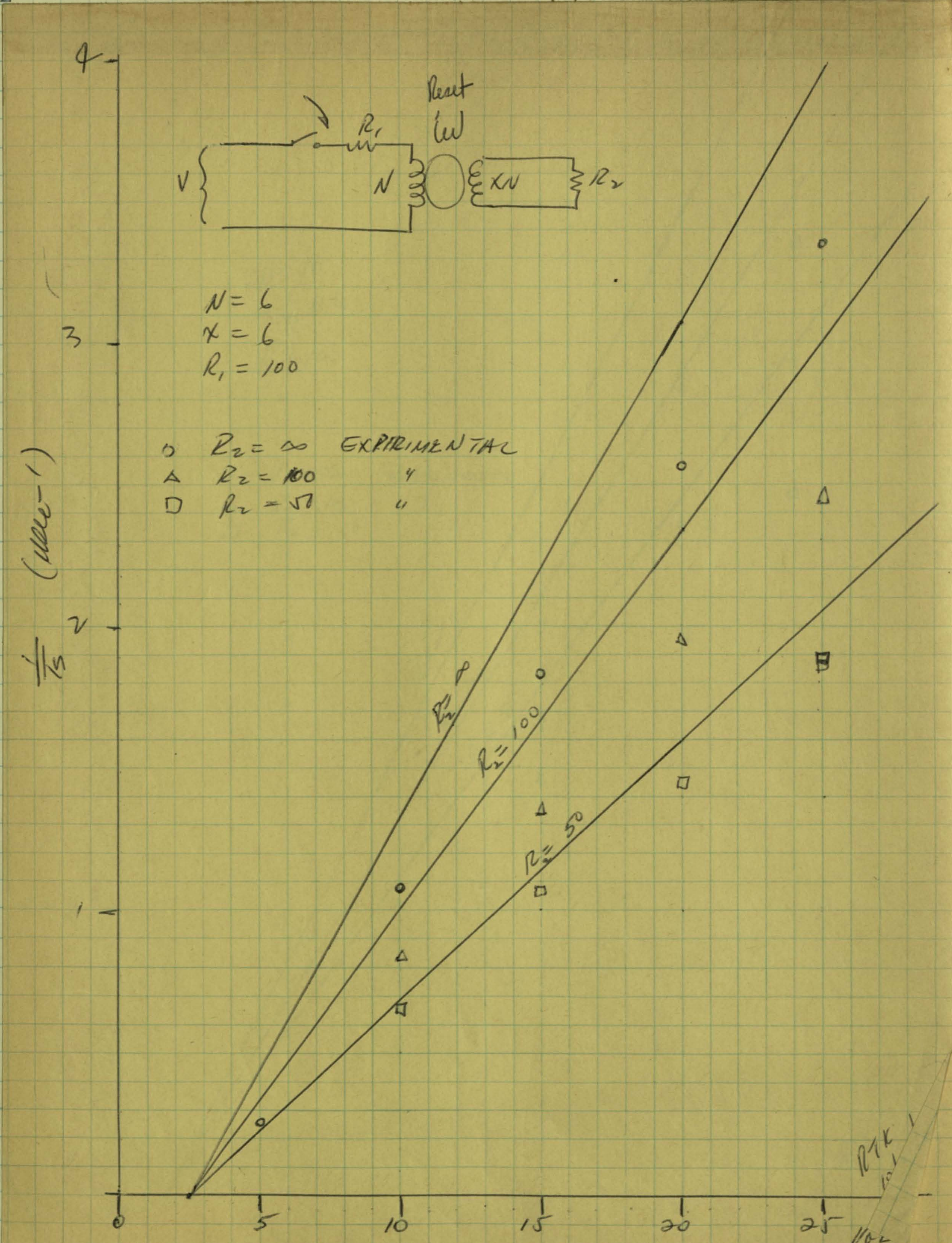
The switching time was measured as a fn of V for different values of N, XN, R2.

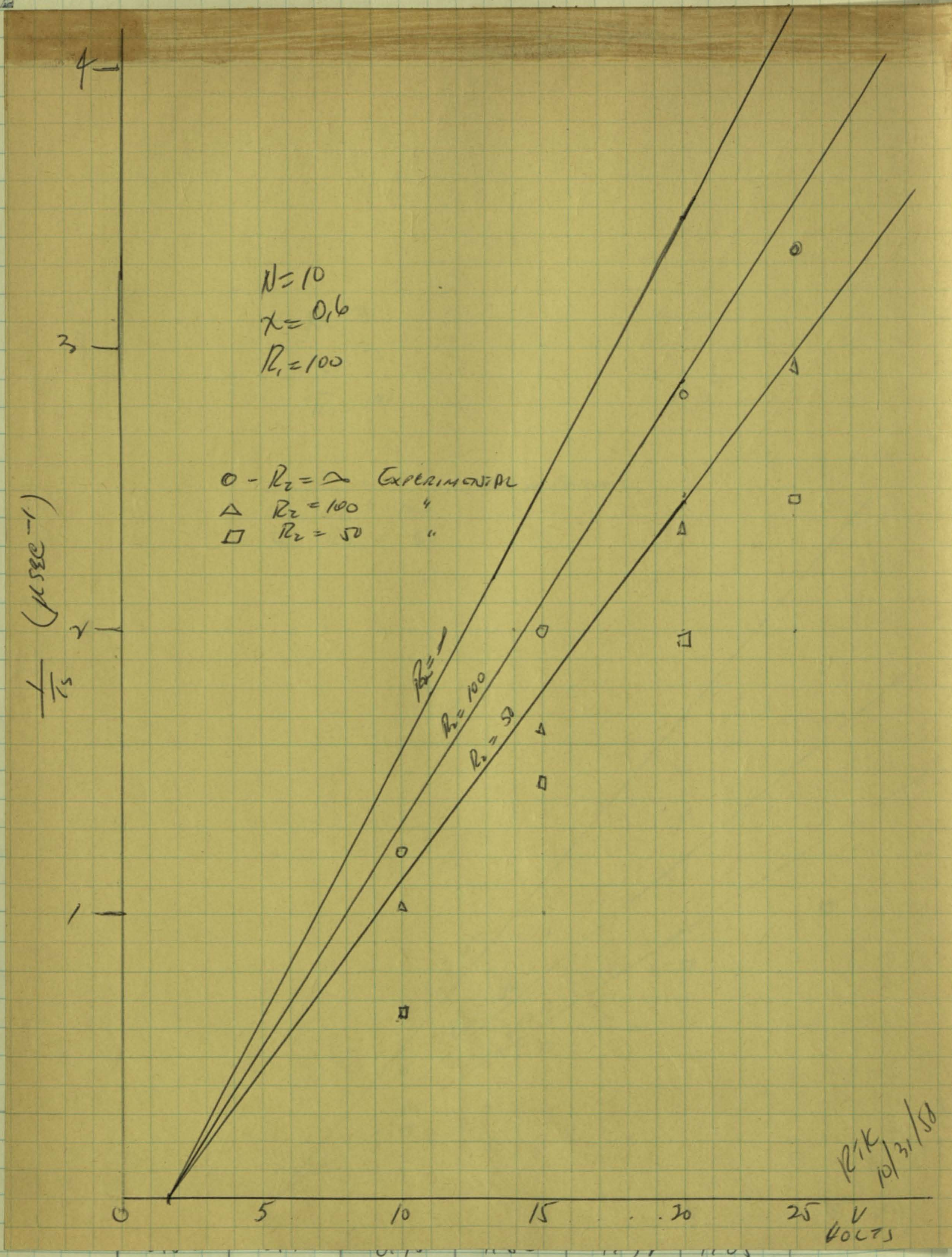
N = 6.
XN = 6

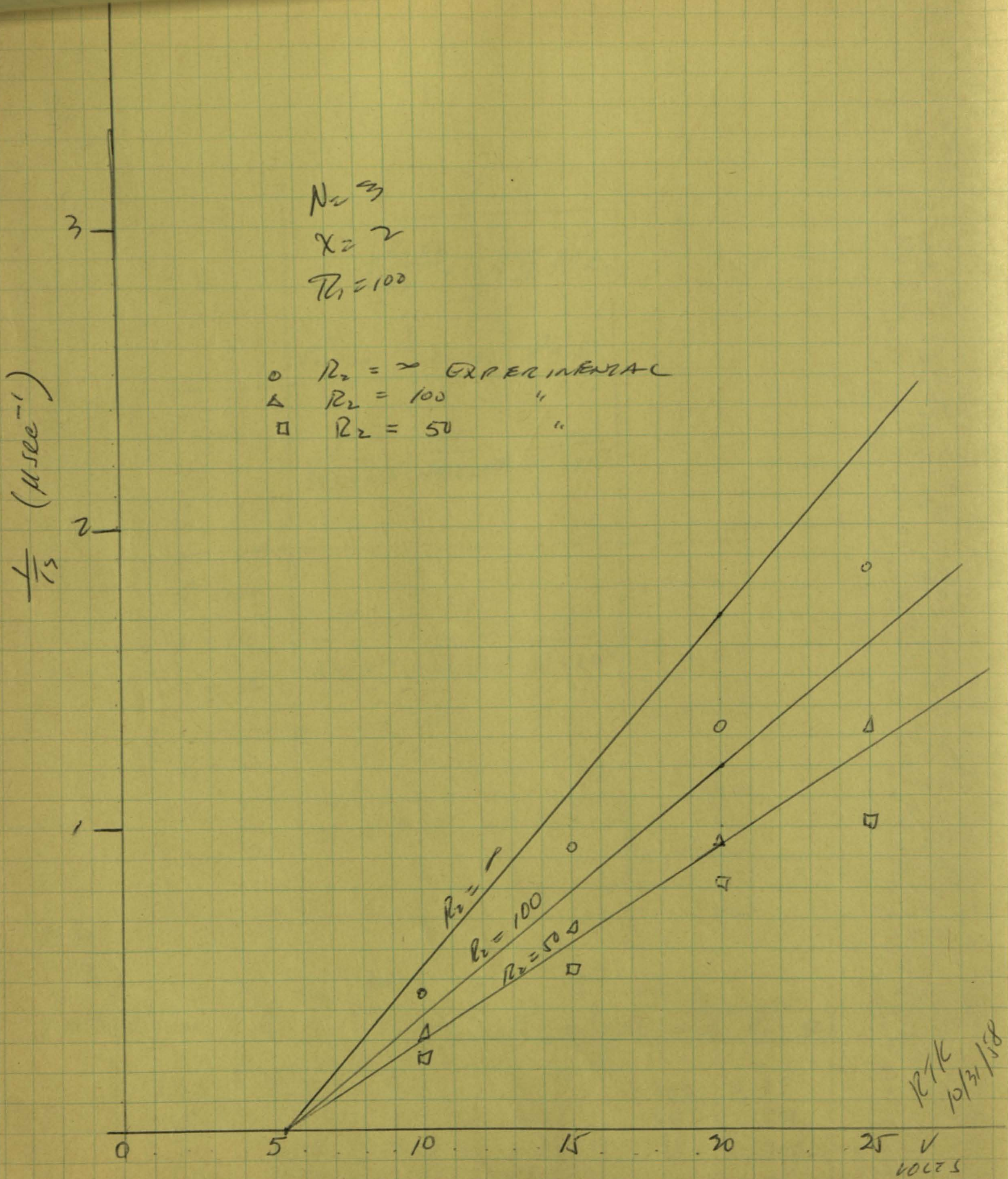
V	T_s (μsec)			$\frac{1}{T_s}$ (μsec)$^{-1}$		
volts	$R_2 = \infty$	$R_2 = 100\Omega$	$R_2 = 50\Omega$	$R_2 = \infty$	$R_2 = 100\Omega$	$R_2 = 50$
5	3.9			0.256		
10	0.93	1.22	1.5	1.07	0.82	0.67
15	0.55	0.74	0.93	1.82	1.35	1.08
20	0.39	0.51	0.69	2.56	1.96	1.45
25	0.3	0.41	0.53	3.33	2.44	1.89

N = 10
XN = 6

V	T_s μsec			$\frac{1}{T_s}$ μsec^{-1}		
volts	$R_2 = \infty$	$R_2 = 100\Omega$	$R_2 = 50\Omega$	$R_2 = \infty$	$R_2 = 100\Omega$	$R_2 = 50\Omega$
10	0.82	0.95	1.6	1.22	1.05	0.625
15	.5	.6	.68	2.0	1.67	1.47
20	.35	.42	.51	2.86	2.38	1.96
25	.29	.34	.41	3.35	2.94	2.44


Reset
R_1
V
N
XN
R_2
N = 6
x = 6
R_1 = 100
○ $R_2 = \infty$ EXPIRIMENTAL
△ R_2 = 100 "
□ R_2 = 50 "
$R_2 = \infty$
R_2 = 100
R_2 = 50
1
2
3
4
0
5
10
15
20
25
Vol


N = 10
x = 0,6
R1 = 100
○ - R2 = ∞ EXPERIMENTAL
△ R2 = 100 "
□ R2 = 50 "
R2 = ∞
R2 = 100
R2 = 50
1/τs (μsec⁻¹)
V VOLTS
RIK 10/31/58


N = 3
X = 2
R1 = 100
o R2 = ∞ EXPERIMENTAL
Δ R2 = 100 "
□ R2 = 50 "
1/τs (μsec⁻¹)
3
2
1
0
5
10
15
20
25
V
VOLTS
R2 = ∞
R2 = 100
R2 = 50
RTK 10/31/58

$$\frac{1}{\left[\frac{R_1 X 2}{R_2}+1\right] N^2 \Phi + R_1 k_s}$$

	$R=\infty$	$R=100$	$R=50$
$R_1=100$, $N=6$, $X=1$	$\frac{1}{33.8\times10^{-6}}$	$\frac{1}{44.6\times10^{-6}}$	$\frac{1}{65.4\times10^{-6}}$
$R_1=100$, $N=10$, $X=.6$	$\frac{1}{53\times10^{-6}}$	$\frac{1}{63.8\times10^{-6}}$	$\frac{1}{74.6\times10^{-6}}$
$R_1=100$, $N=3$, $X=2$	$\frac{1}{25.7\times10^{-6}}$	$\frac{1}{36.5\times10^{-6}}$	$\frac{1}{47.3\times10^{-6}}$

$N=6$

$XN=3$

	T_s μsec			$\frac{1}{T_s}$ μsec^{-1}		
V volts	$R_2=\infty$	$R_2=100$	$R_2=50$	$R_2=\infty$	$R_2=100$	$R_2=50$
10	2.2	3.3	4.0	0.455	0.303	0.25
15	1.08	1.5	1.9	.925	.667	.526
20	0.76	1.05	1.26	1.32	.95	.794
25	0.54	0.76	0.95	1.85	1.32	1.05

10/31/58

The results are encouraging. This indicates that by knowing the three core constants, Φ, K_s and a, one can predict the reversal time of a loaded core with a reasonable amount of accuracy. The equation is simple enough to be used in design work. In all cases, the experimental curves have a smaller slope than the theoretical curves.

Rearranging the equation for switching time:

$$\frac{1}{T_s} = \left[\frac{1}{\left[\frac{R_1 X^2}{R_2} + 1\right] N^2\Phi + R_1 K_s} \right] \left[NV - R_1 a \right] \qquad (1)$$

$$= \left[\frac{1}{\left[\frac{R_1 X^2}{R_2} + 1\right] \frac{N^2\Phi}{R_1} + K_s} \right] \left[\frac{NV}{R_1} - a \right] \qquad (2)$$

This reduces to the familiar $(NI - a)T_s = K_s$ when

$R_1 >> N^2\Phi$

Errors in the initial measurements of K_s and Φ could account for the difference in the experimental and theoretical results. Better results can be obtained by assuming (2) to be true and then determining Φ and K_s since (2) is more general than $(NI - a)T_s = K_s$

R. T. Kikoshima
10/31/58

11/3/58

Changed 2 of the cores in the four stage ring to 80520 1/8 D10 (half the flux capacity of the 80520 1/8 D20). Operated them as a 2 stage ring. The operation was shaky - the maximum bias before failure was -0.8 volts. Transfer time was approximately 0.35 - 0.40 usec. Will use the 80520 1/8 D20 in the ring as originally planned.

R T Nikoskinen 11/3/58

11/5/58

The ten stage ring was completed and operated as well as the 9 stage breadboard. Transfer time is approximately 0.6 μsec.

The change to lower Φ cores on 11/3/58 was not a fair test inasmuch as the turns were not changed in accordance with [1] page 66 and [7] in 60

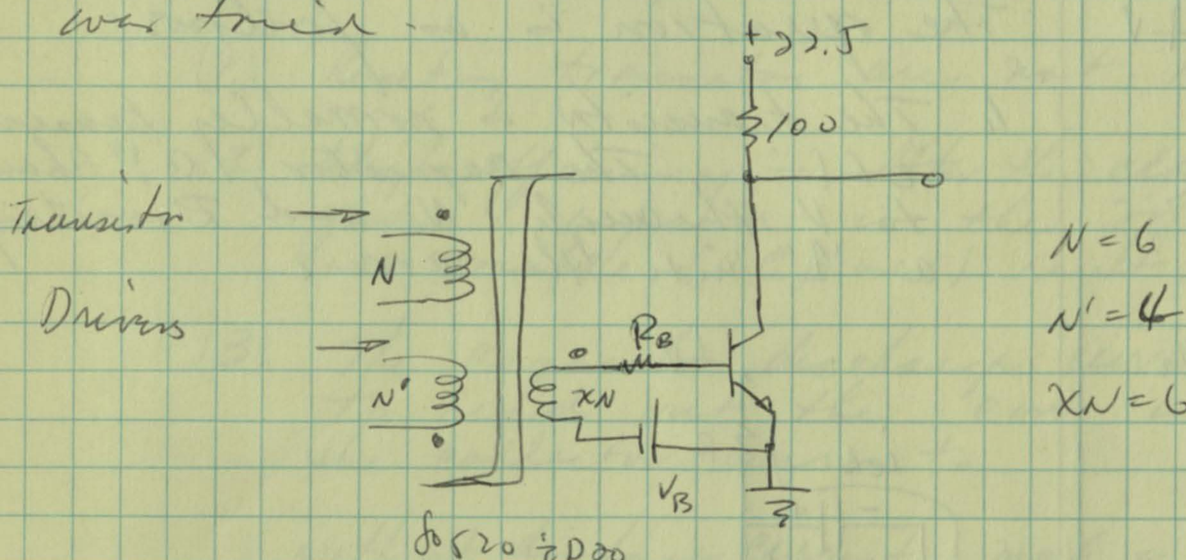
R T Nikoskinen

11/5/58

11/6/58

The ten stage ring was rather "noisy". This was improved by changing the ground system. The ring operation is good and solid.

Since the breadboard for the four stage ring was available, the following "stiff turnoff" circuit was tried.



Switched approximately 300 ma with a rise and fall less than 100 m μs. With R_B small storage time was a minimum.

Experimented with feedback, but no data was taken.

R. T. Kikuchi
11/6/58

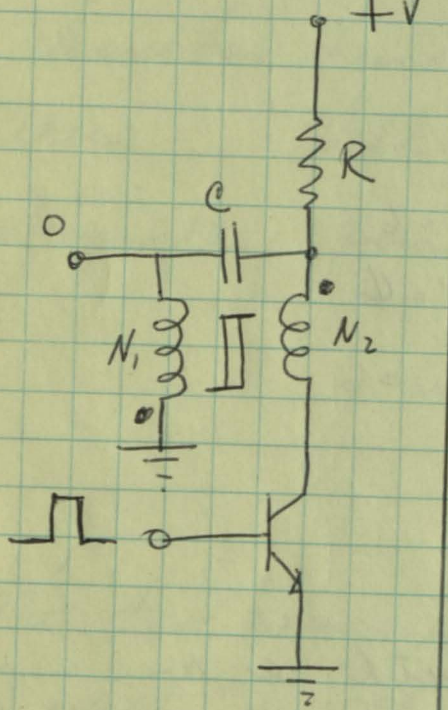
11/7/58

Got the V-I plotter in operation for the R_{sat} measurements.

R. T. Kikuchi
11/7/58

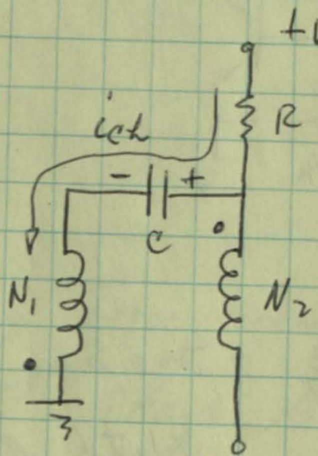
11/11/58

While looking into Single Swing Blocking oscillators as a power pulser (then using square loop cores) the problem of resetting the core was considered. Thought of a self resetting core-transistor amplifier circuit.

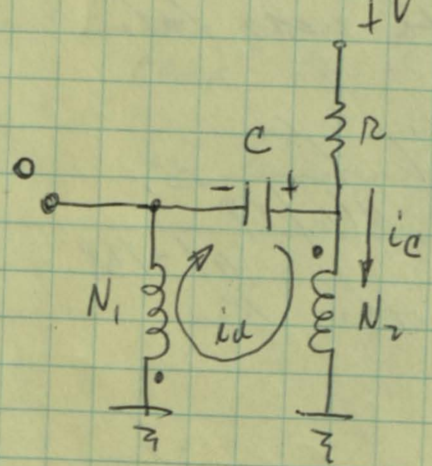


The operation is as follows:

1. The transistor is normally biased "off". The capacitor, C, is charged to V through N_1 and R writing a "1" into the core.



2. The transistor is then turned "on" by an input pulse. The capacitor c is discharged. The 1 is read out of the core by an mmf equal to $N_1 i_d + N_2(i_d + i_c)$. An output pulse will appear at point o until the core saturates.



R T Mikoshiba 11/11/58

Witnessed & Understood 11/25/58
V H Grinich

11/11/58 Cont.

3. when the input pulse is over, the transistor returns to the "off" state and the capacitor charges as in (2.). The circuit is then ready for another input pulse.

The advantage of this circuit over other resetting circuits ~~are as follows~~

(1.) Resetting transistors are not required

(2) High efficiency — After the charge cycle, no power is required in the "off" state as in trickle (D.C. Biased) reset circuits.

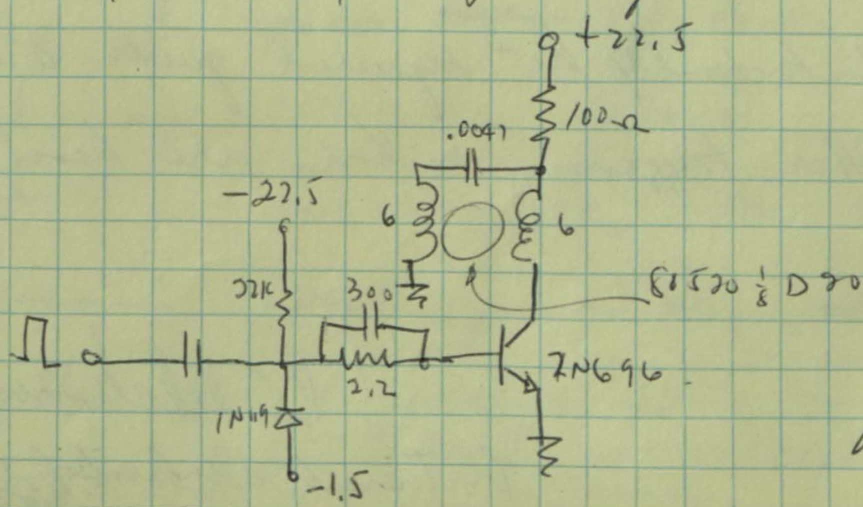
(3). The capacitor discharge current ~~can be~~ is used to read out the core in addition to the collector current.

without discharge current $mmf = N_2 i_c$

with " " $mmf = N_1 i_d + N_2(i_d + i_c)$

Net increase in $mmf = (N_1 + N_2) i_d$

The following circuit was tried in the breadboard. The values of R, N_1, N_2 and V were used only because the core was already wound (for the ring circuit), and parts of the circuit was already built up.



With the circuit as shown the pulse width was 0.2 μsec and the circuit recovered in 0.7 μsec

R.T. Kekahuna 11/11/58

Witnessed & Understood 11/25/58
V.A. Jenick

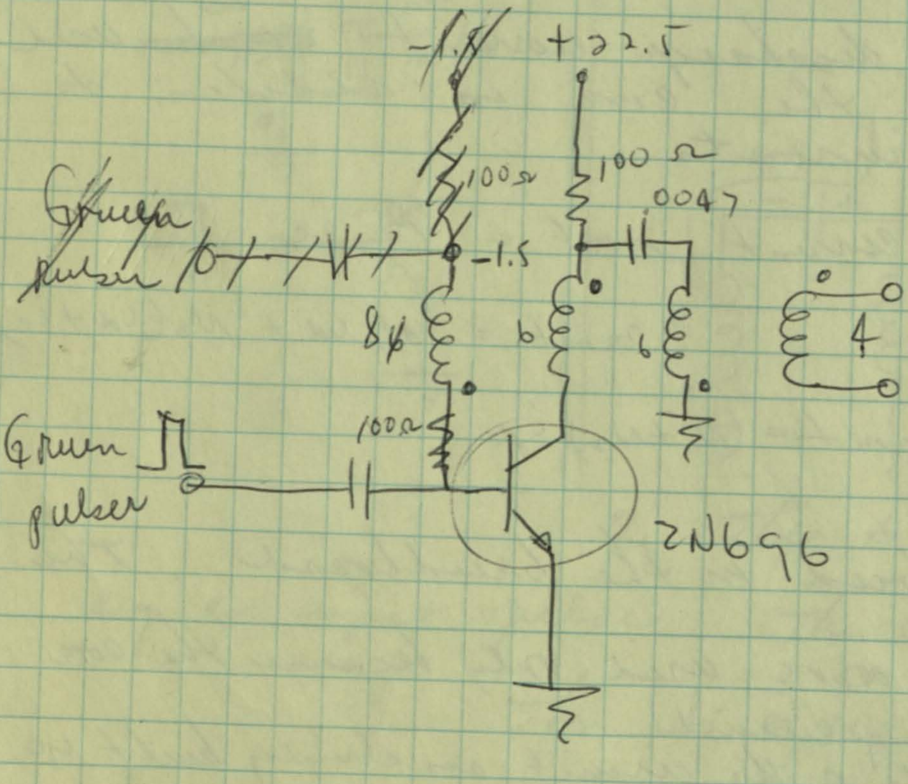
11/11/58

Will ~~consider the desen~~ attempt to analyze the circuit and possibly come up with design equations before attempting a blocking oscillator circuit.

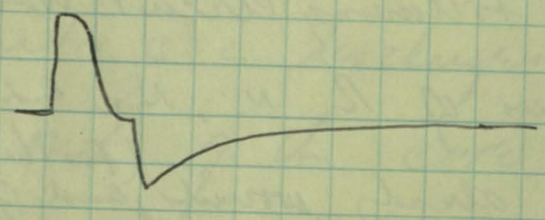
R T Kekoshian
11/11/58

11/12/58

Built up a feedback circuit (B.O) with the capacitor resetting circuit.



pulse width ~ 0.2 μs
Ampl ~ 6 V
Recovery ~ 1 μsec

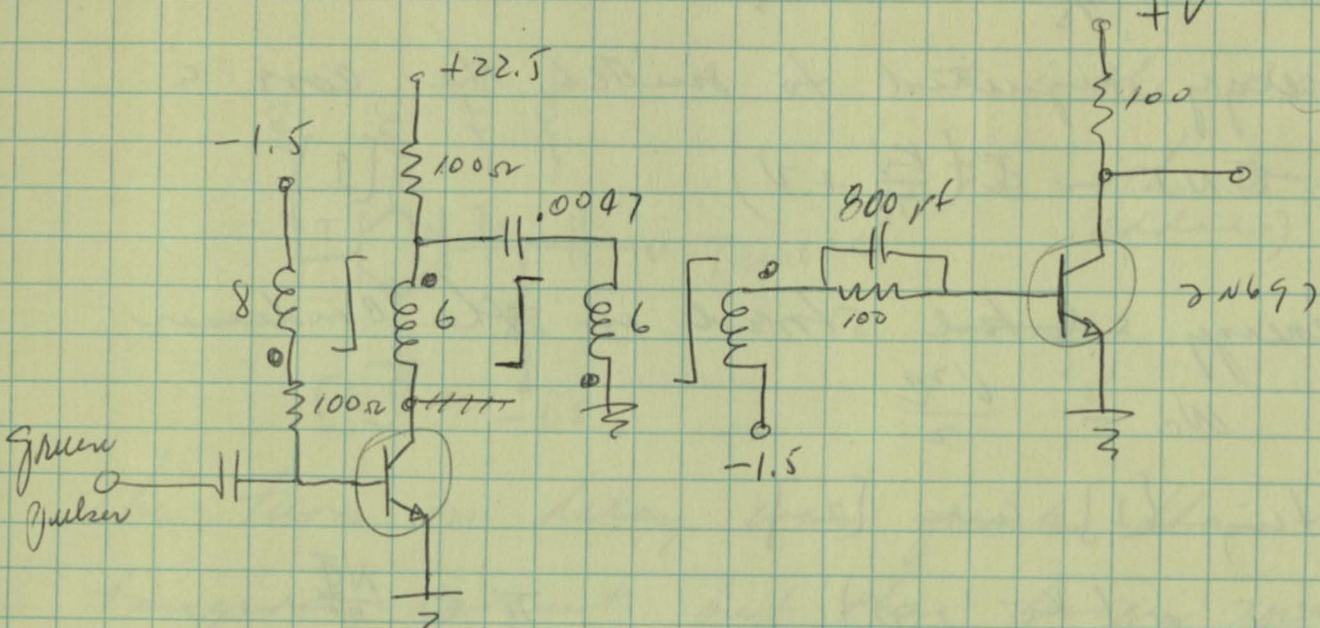


Circuit operated satisfactorily but required quite a lot of trigger power. Other triggering methods are being considered.

R T Kekoshian 11/12/58
Witnessed & Understood 11/25/58
V H Shimat

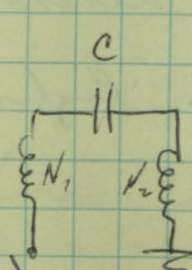
11/13/58

The output of the B.O. circuit was fed into a grounded emitter stage. ~~to~~



Currents up to 800 ma were switched with t_r and t_f < 40 musec. The rise and fall time could be decreased by increasing the turn-on and turn off drive currents.

Blocking Osc circuit:



If the circuit is approximated as shown from ~~turn~~ "off" to "on", the minimum size of C can be determined by matching energies, ie, the stored energy in the capacitor must equal the ~~stored~~ energy required by the core to switch at a given rate.

R T Kirkpatrick 11/13/58

Witnessed & Understood 11/25/58 V A Grimek

11/13/58 cont

For a step of current

$$(NI - v)T_s = k_s$$

or $$NI = \frac{k_s}{T_s} + v$$

The energy required to switch the core is

$$W = \Phi NI = \Phi\left(\frac{k_s}{T_s} + v\right) \quad [1]$$

The energy ~~started~~ stored in the condenser

$$W_c = \frac{V^2C}{2} \quad [2]$$

Equating [1] and [2]

$$\frac{V^2C}{2} \geq \Phi\left(\frac{k_s}{T_s} + v\right) \qquad T_s \approx \frac{N\Phi}{V}$$

$$C \geq \frac{2\Phi}{V^2}\left(\frac{k_s}{T_s} + v\right) \quad [3]$$

Using the constants of the 80520 1/8 D20 core and $T_s = 0.2$ μsec, $V = 20$ volts

$C \geq$ ~~0.0015~~ 0.002 μf.

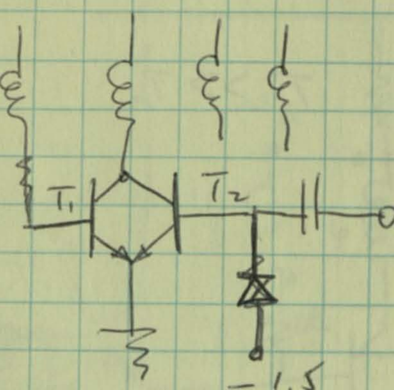
Will look into the reset cycle to determine which cycle (set or reset) has the highest minimum allowable capacitor

Witnessed & Understood 11/21/58
[signature]

[signature]
11/13/58

11/14/58

Tried a separate transistor for triggering the circuit on page 79.



T_1 is the B.O. Transistor
T_2 is the triggering transistor (added)

The turn on delay was greater than for the direct triggering circuit but the trigger power was greatly reduced. Will look into other triggering methods.

R T Kekorkian 11/14/58
Witnessed & Understood 11/25/58 V Hyrinick

11/17/58

Started work on a circuit to measure the ~~switching~~ storage constant, K_s, of transistors

$$T_s = K_s \ln \frac{I_{B1} - I_{B2}}{I_{BS} - I_{B2}} \qquad [1]$$

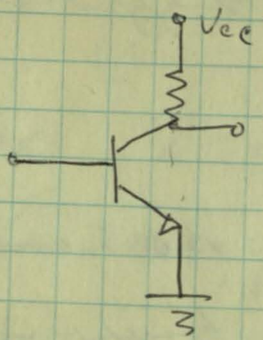
where I_{B1} is the turn on base current
I_{B2} " " " off " "
$I_{BS} = \frac{I_C}{\beta_0}$ where β_0 is the grounded emitter current gain at the edge of saturation.

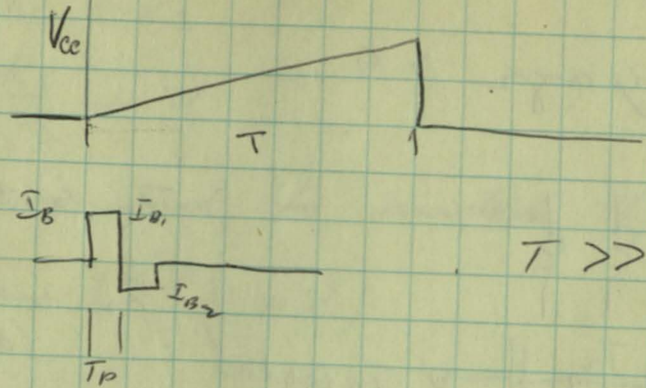
Ref: Semiconductor Products May/June 1958
Ebers and Moll Proc IRE Dec 54

Witnessed & Understood V Hyrinick 11/25/58

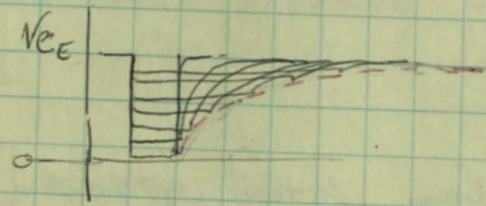
11/17/58 cont.

Rewriting [1] $I_C = \beta_0 \{ I_{B2} + \beta_0 (I_{B1} - I_{B2}) e^{-\frac{1}{K_s} T_s}$



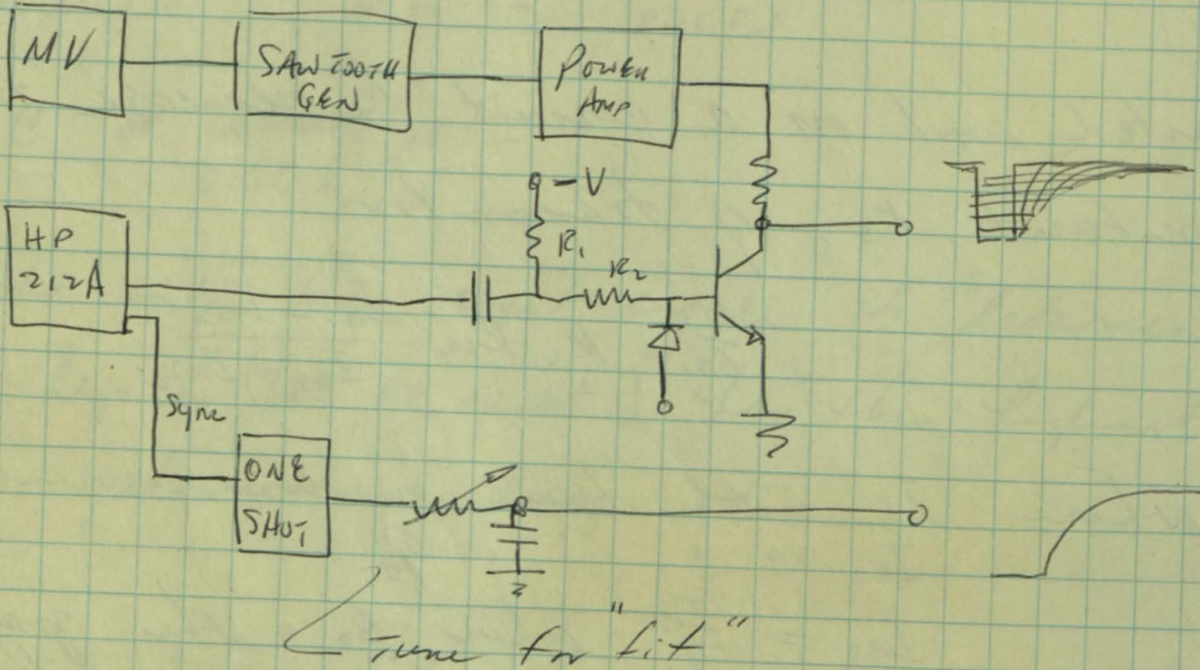


$T >> T_p$



The curve of the envelope (in red) can be matched with an RC circuit and K_s can be determined.

To start with the following circuit will be tried:

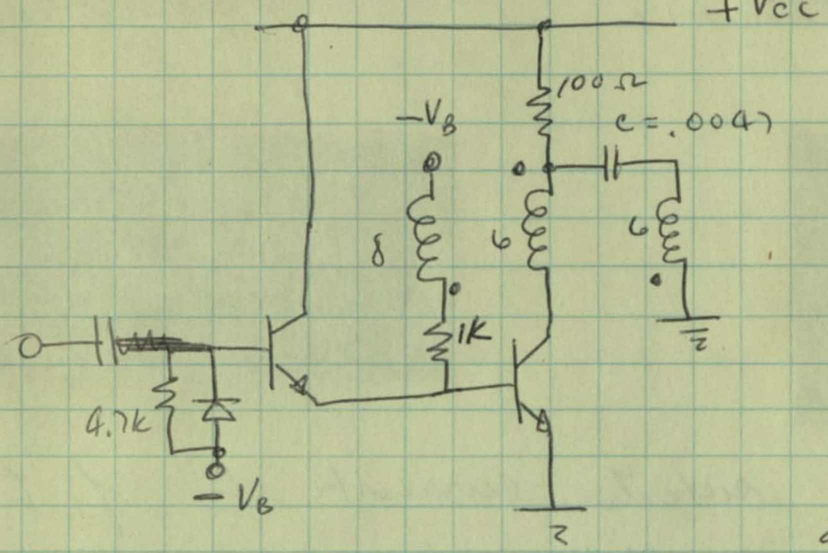


By allowing the MV to free run with respect to the HP 212A, a well "filled in" output will be obtained

R.T. Kikoshian 11/17/58

11/18/58

Tried another triggering circuit for the self resetting Blocking oscillator circuit



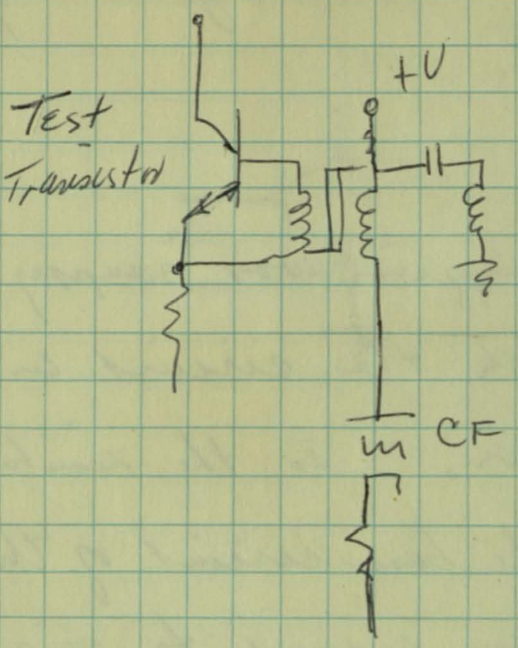
Triggering was "snappy" with the circuit as shown. If the resistance in the base circuit of the B.O was reduced to give a faster turn-off, triggering was sluggish and resetting was slower because of the loading effect of the E.F. The bias on the E.F. was not sufficient to hold the transistor "off" at reset time. ~~Current drawn through the 8 turn base win~~ This circuit ~~still le~~ leaves something to be desired since the turn off of the B.O. transistor ~~was~~ is slow.

R.T. Kikushima 11/18/58
Witnessed & Understood 11/25/58 [illegible]

11/19/58

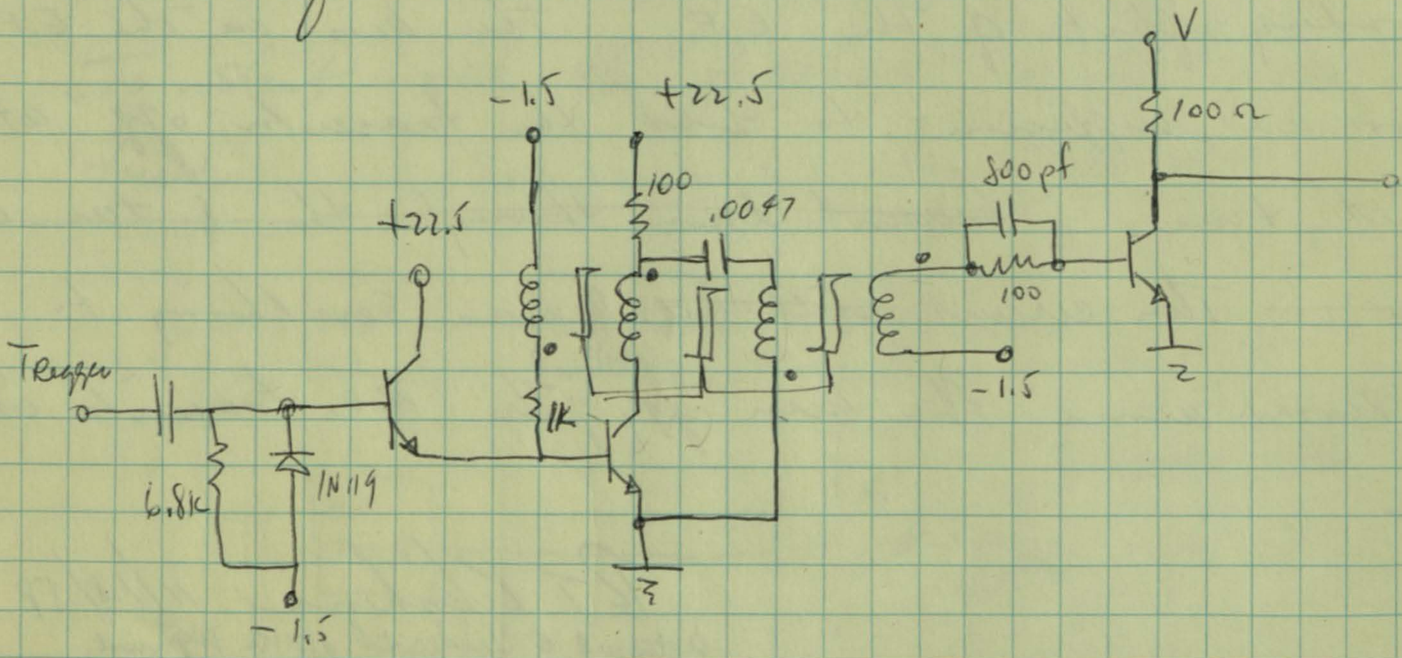
Looked into possible methods of modifying the Asymptotic tester from an open base ~~test~~ to a shorted base-to emitter test. Have decided to use a Square loop core in the base circuit to turn the base on.

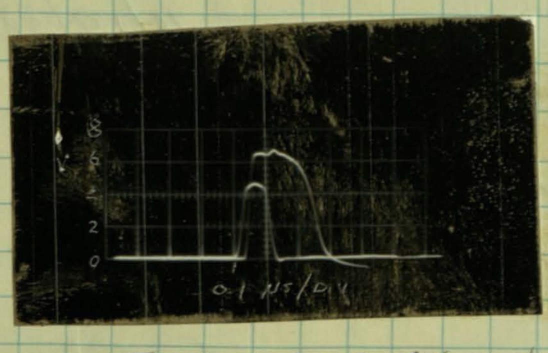
11/19/58



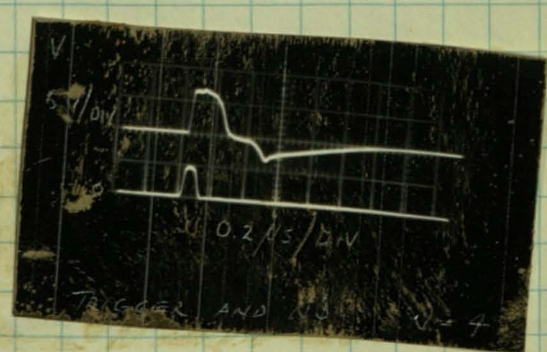
The proposed changes will be indicated in detail on the schematic

Took pictures of the outputs, currents etc of the Self resetting Blocking Oscillator triggered with an emitter follower.



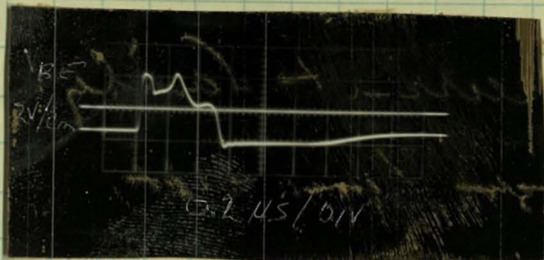


TRIGGER PULSE AND NØ

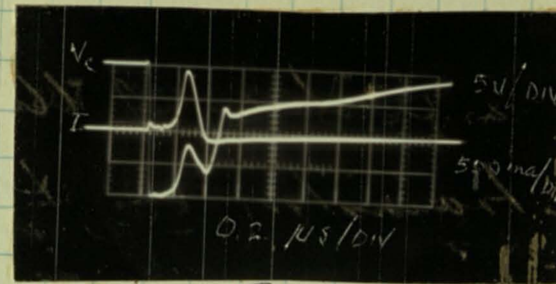


TRIGGER PULSE & NØ

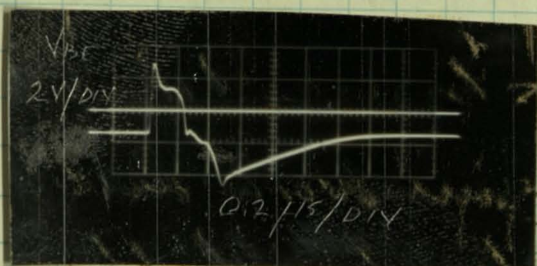
Witnessed & Understood 11/25/58 VHgrinch



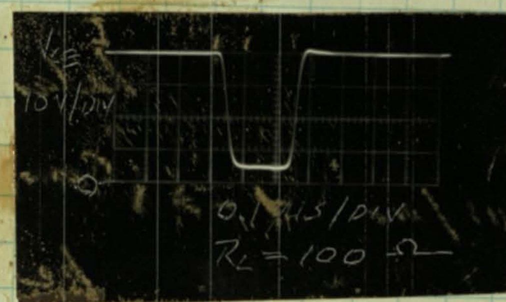
VBE (B.O)



VCE + IDISCHARGE (B.O)



VBE GND EMITTER



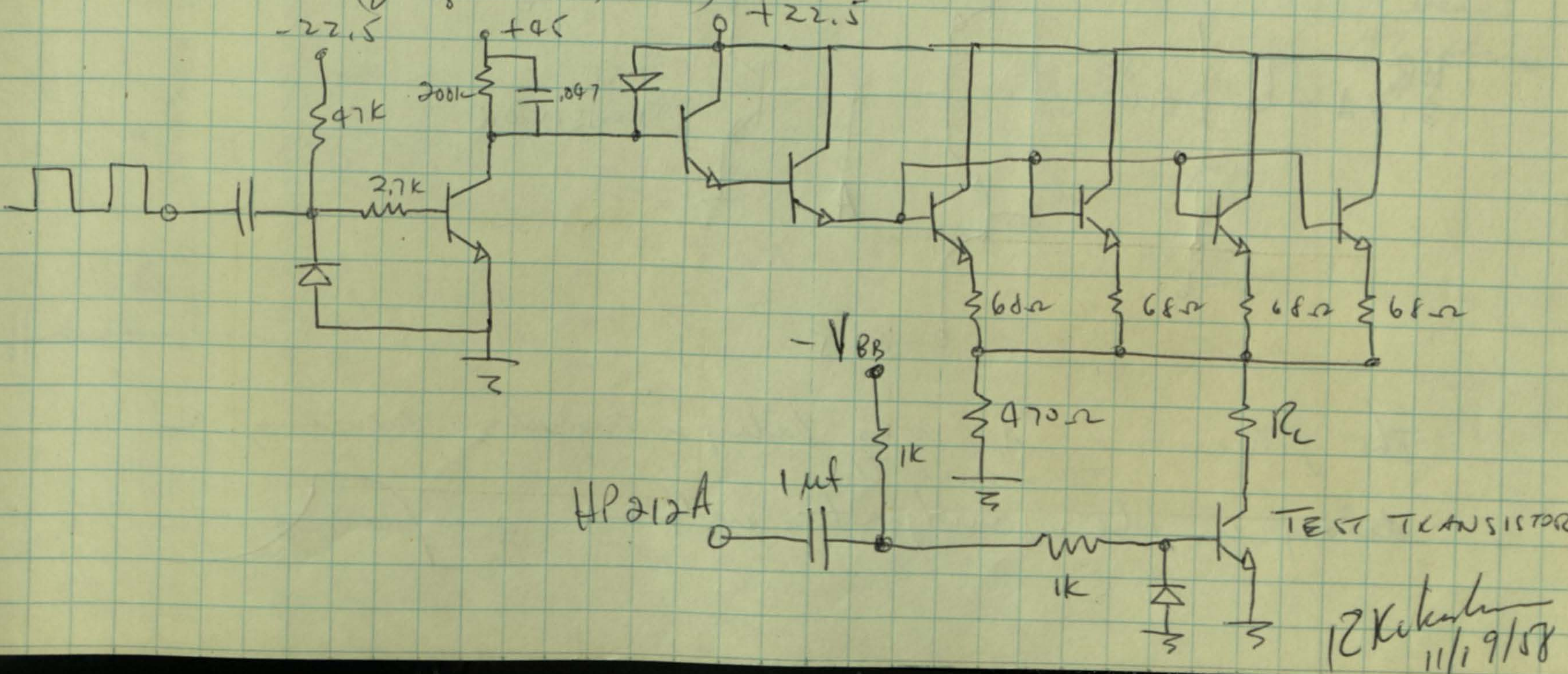
VCE GND EMITTER

While the triggering action is good, the recovery time of the circuit is longer than for other methods of triggering.

R T Kukoshima 11/19/58

Witnessed & Understood 11/21/58 V H Grinich

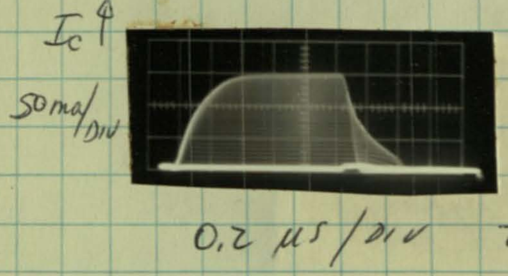
Had D. Ferris set up the following sawtooth Vce circuit from I. Haas, for the storage time constant measuring circuit (page 81, 82)



R Kukoshima 11/19/58

11/20/58

Took a picture of the plate current family for a transistor in the storage time test circuit.

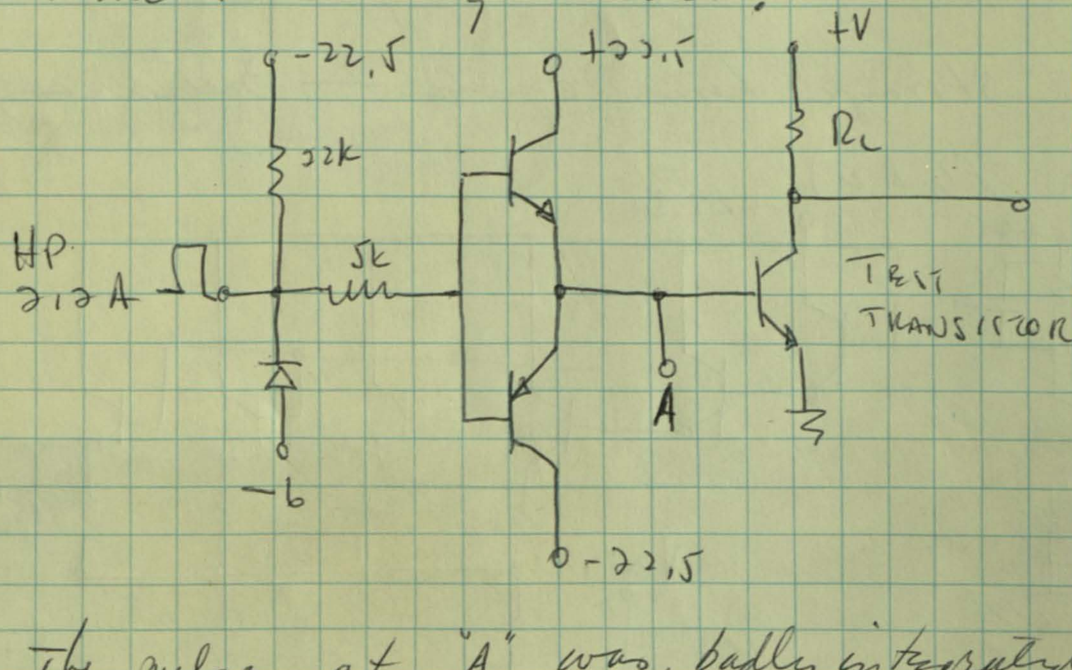


The envelope of the trailing edge determines the storage time constant K_s. Work will be continued to finish the other circuit.

R T [illegible]
11/20/58

11/21/58

Set up the following circuit as a possible switching time measuring circuit.



The pulse at "A" was badly integrated causing a delay in the turn on of the output pulse

11/21/58

V. H. Grinich suggested a load resistor from A to ground to provide a current path for the "off" current.

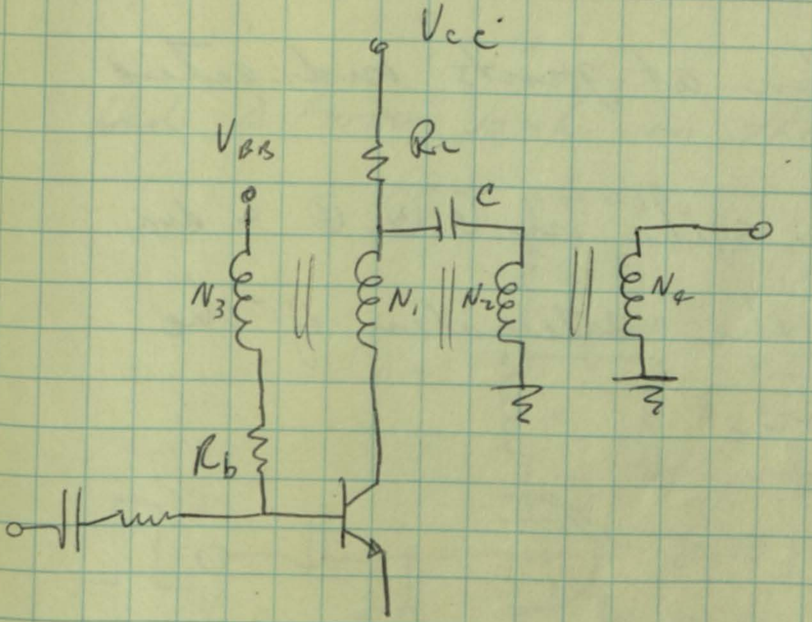
Started work on a fixed pulse generator for the switching time measuring set-ups.

Specs:

Pulse Amplitude 30 VOLTS
Output impedance 50 Ω
$t_r = t_f < .020$ μs
Width – 1 μs
Rep rate – 1 KC

Will start with a blocking oscillator circuit driving a grounded emitter with an emitter follower output stage.

Blocking oscillator.



Will use an 80529 1/4 030 core

$\Phi = 0.70$ volt μsec
$K_s = 0.376$ AT μsec
$\nu = 0.155$ AT

LET $V_{CC} = 30$ VOLTS

WANT $\tau_s = 1$ μsec

$(N_1 + N_2) \simeq \frac{V\tau_s}{\Phi} = \frac{30}{.7}$

$\simeq 45$ turns

Let $N_1 = N_2 \simeq 20$ turns

$N_3 = 20$ T
$N_4 = 10$ T

11/21/58 cont.

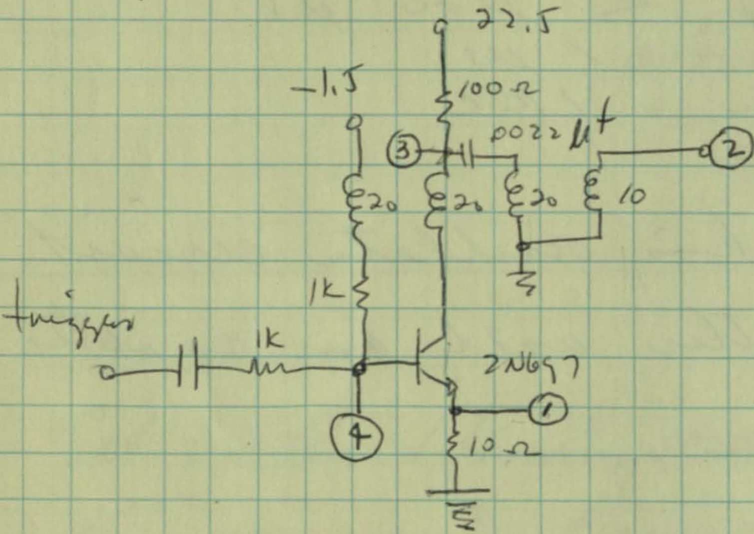
From eqn [3] page 80,

$$C > \frac{2\Phi}{V^2}\left(\frac{k_s}{\tau_s} + 2\right)$$

$$> \frac{2(.7)}{30^2}\left(\frac{.376}{1} + .155\right) \times 10^{-6}$$

$$> 825 \text{ pf.}$$

In the circuit, .00220 μf was required for circuit operation:



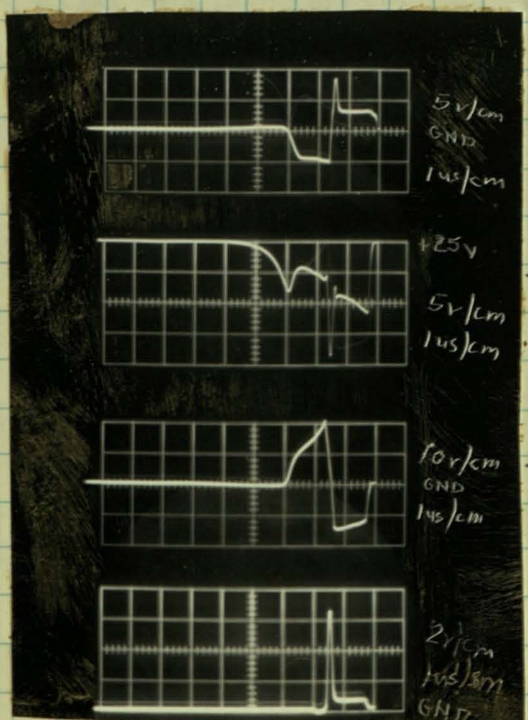
Circuit operates well as shown.

Will have D. Ferris take pictures of the outputs, etc.

[signature] 11/21/58

11/24/58

Pictures taken at points indicated above



← ④

← ③

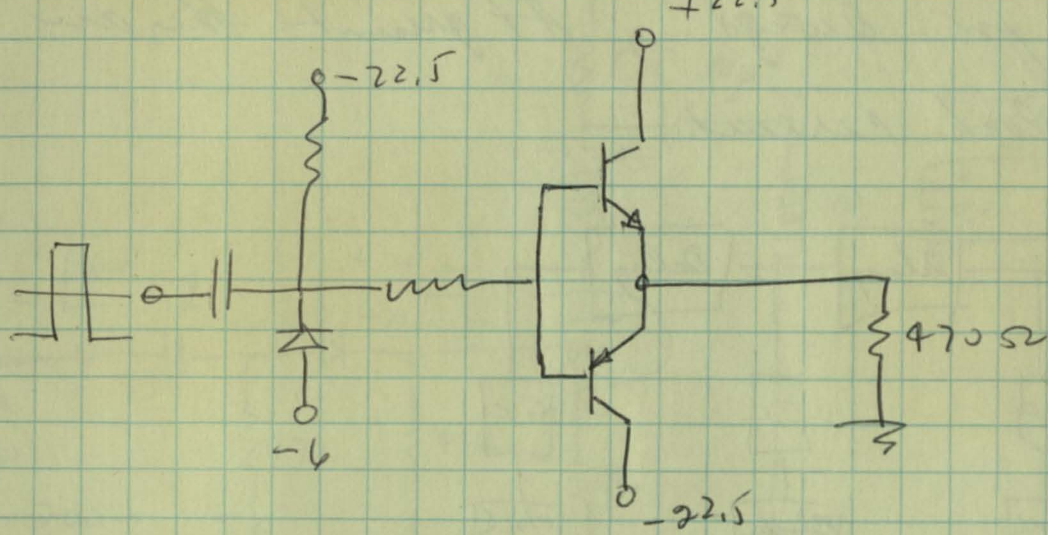
← ②

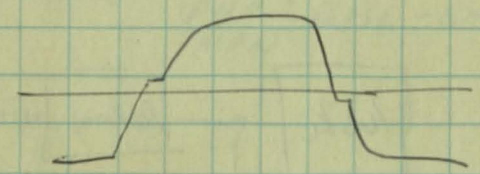
← ①

The spike on ①, ③, ④ is due to the saturation of the core.

11/24/58 Cont.

Did some work on the complementary E.F.
Tried loading the output of the Comp E.F.
with 470 Ω



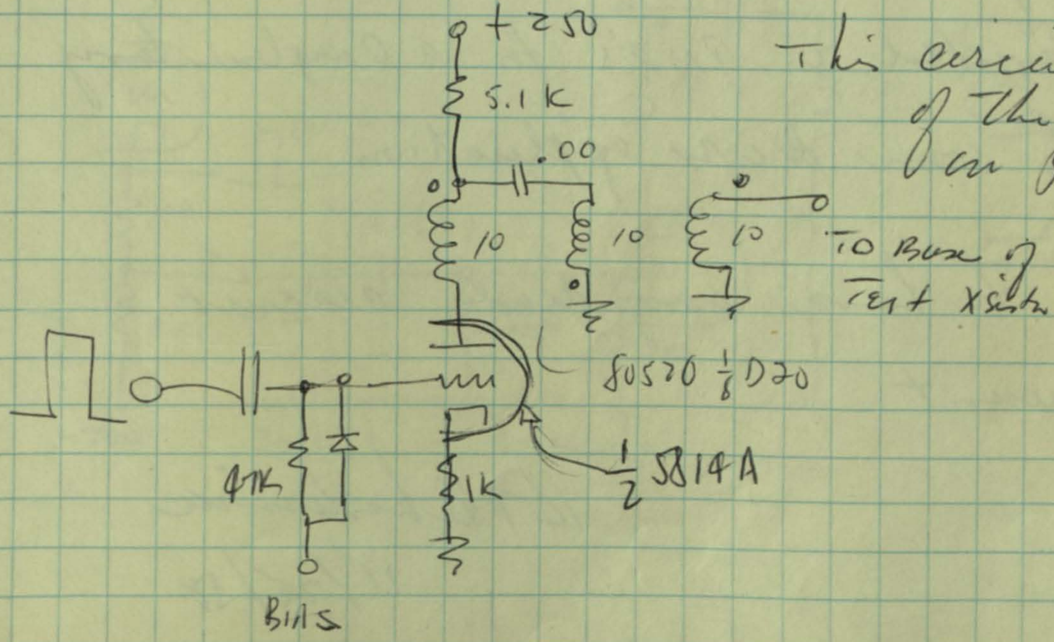


The output was "notched" as the input passed
through zero – will look into methods
of biasing the transistors in the active region

R T Kilcher 11/24/58

11/25/58

Had D. Ferris work on the AVCES Test circuit.

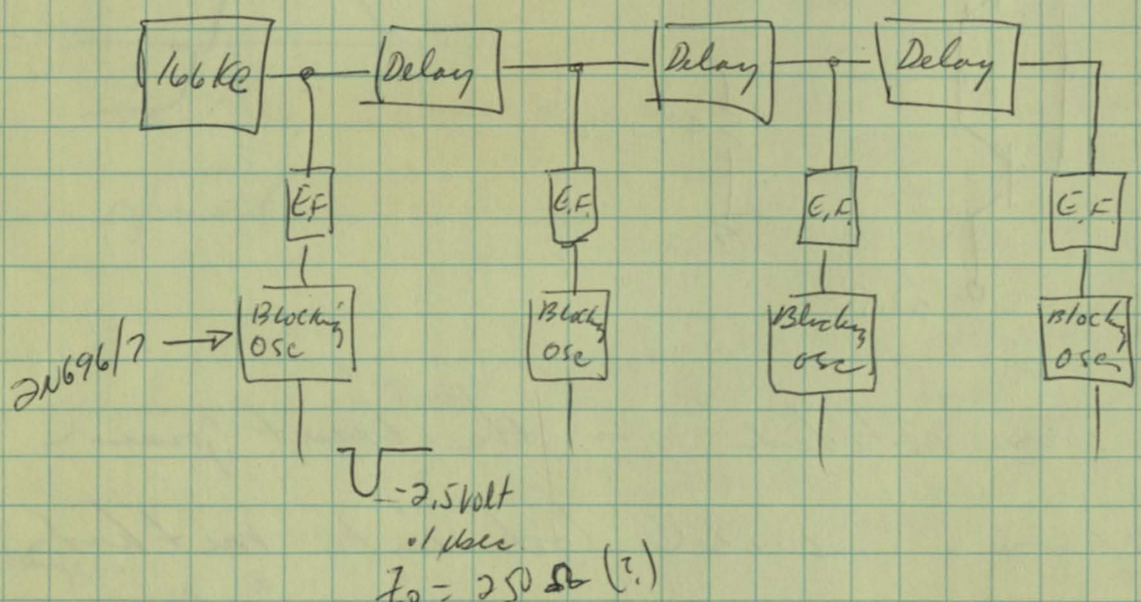


This circuit is the tube version of the amplifier described on page 76.

Circuit operated satisfactorily, but will look into current limiting methods.

11/25/58 Cont.

Visited IBM San Jose with Gene Kegarts. Met with Joseph Belet, Harry Kahn, Walter Bennet, Cliff Stidger, and the dept mgr, Joseph Fernandez. They are responsible for Test and check-out Equip't for Owego. At present they are working on a clock circuit.



B.O. Transformer: P.I.C. 8711

They want to use PNP's at the B.O outputs because with their present transformer, they are unable to invert the pulse (winding).

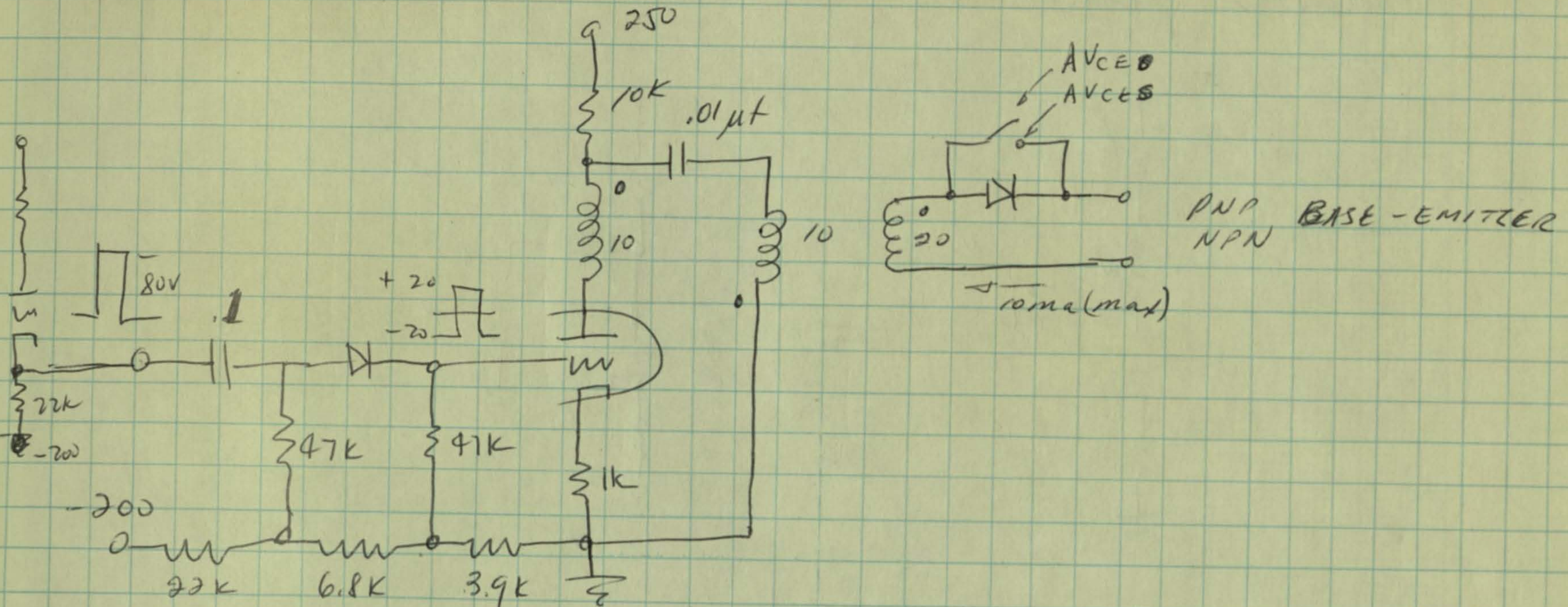
They are also interested in PNP's for a complementary emitter follower for some driver application

They didn't seem to have any real circuit problems at present.

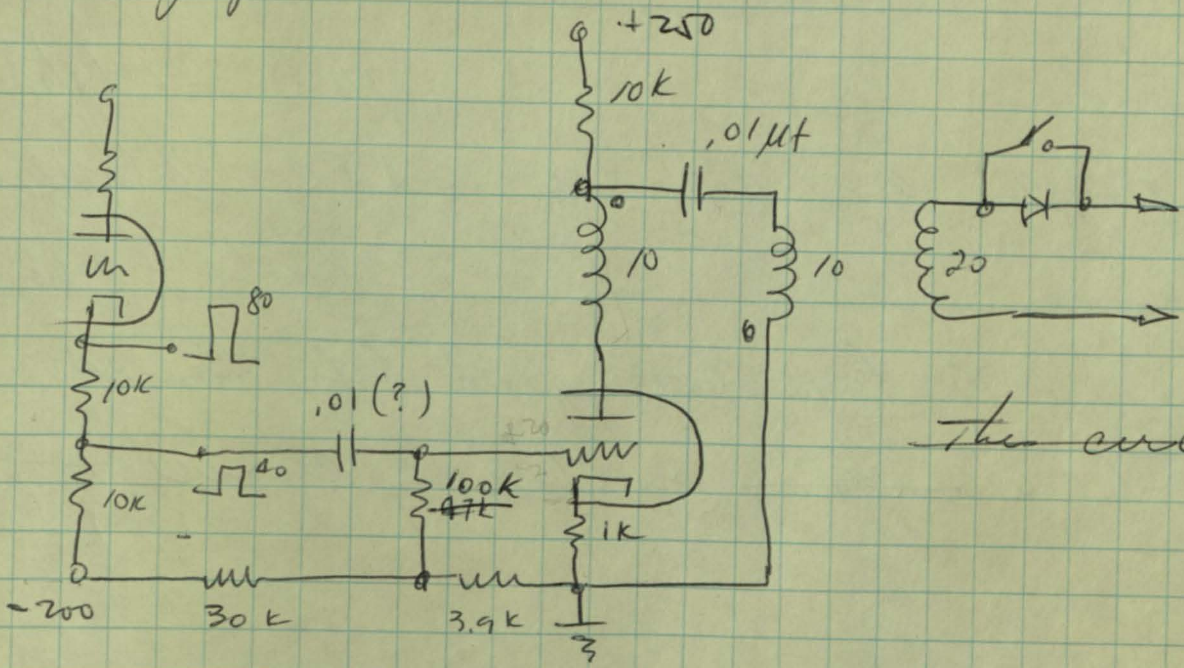
R T Kekarkanian
11/25/58

11/24/58

Resumed work on the AV_{CES} test circuit. The circuit now looks as follows:



The output circuit is limited to approximately 10 ma. The input clipping circuit loaded down the preceding stage. To reduce this loading, the following circuit is proposed

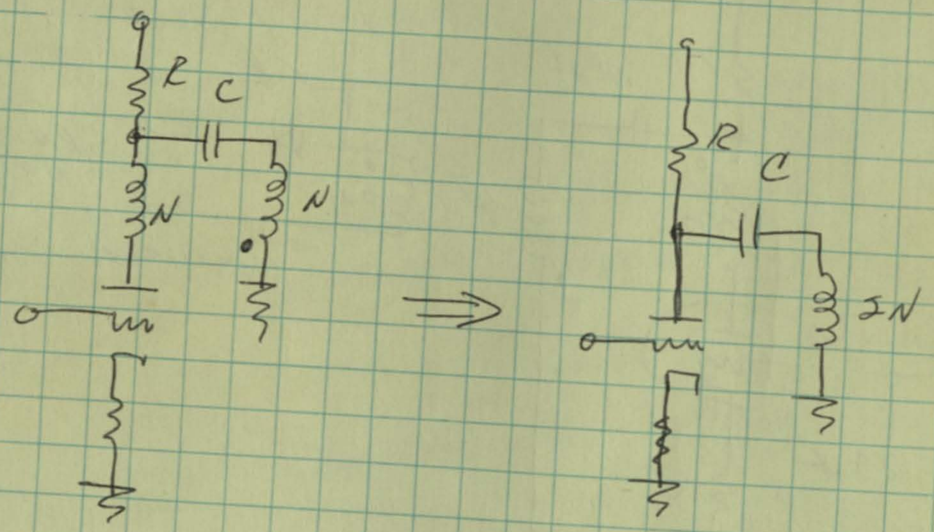


~~The circuit~~

R T McKinshin 11/26/58

11/24/58

Another modification on this circuit (and on the similar transistor circuits) is



The circuits are equivalent in operation. The reset mmf in the charge cycle will differ because of the difference in the number of turns.

R.T. Kirkham 11/26/58

12/1/58 – 12/5/58

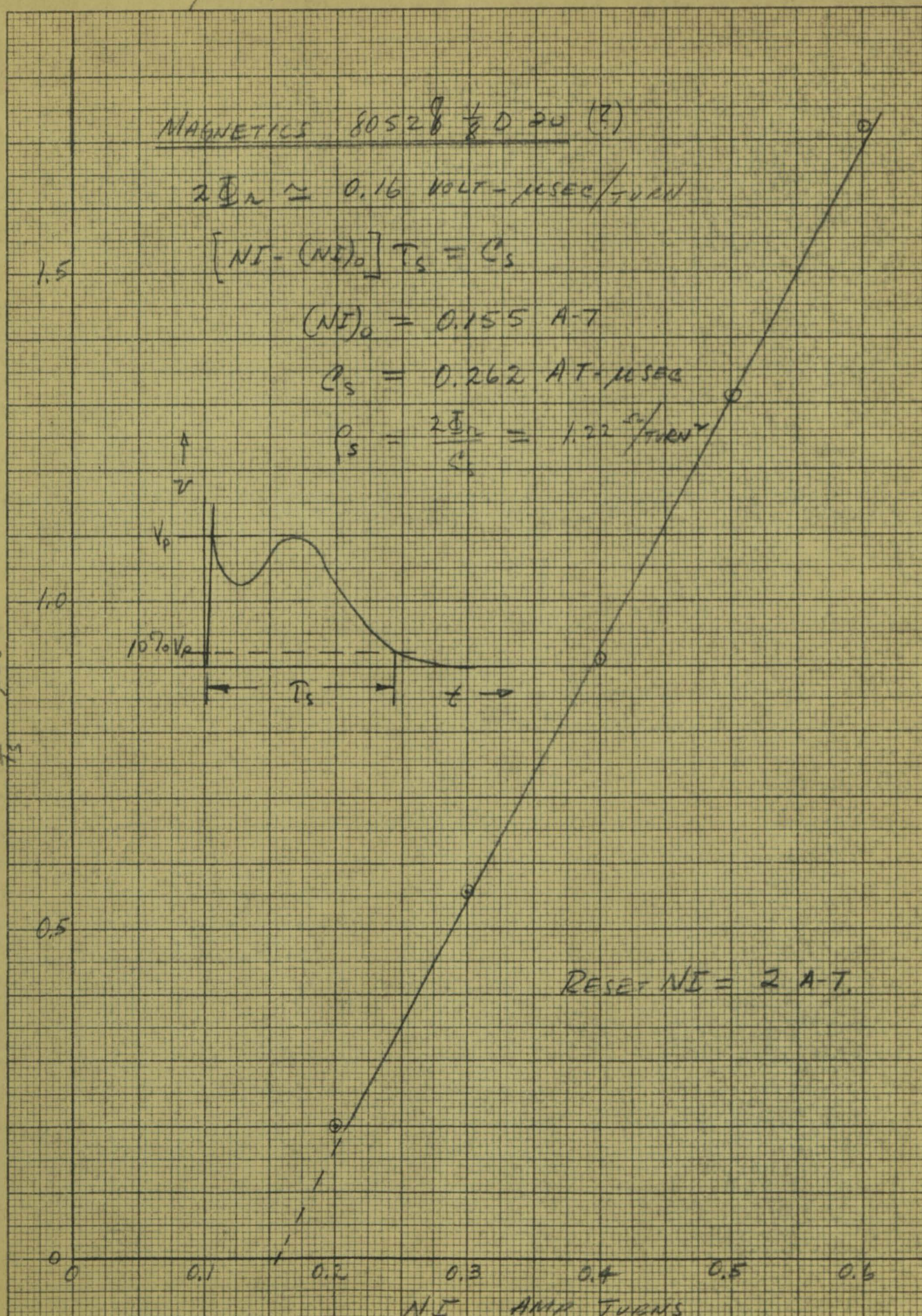
Visited IBM Kingston and attended EJJC Philadelphia

RT Kirkham 12/8/58

Received some Q-79 tape cores from Bill Lanier, IBM Kingston. Took a ~~switchin~~ switching curve ⟶ of the core.

RT Kirkham 12/8/58

KINGSTON

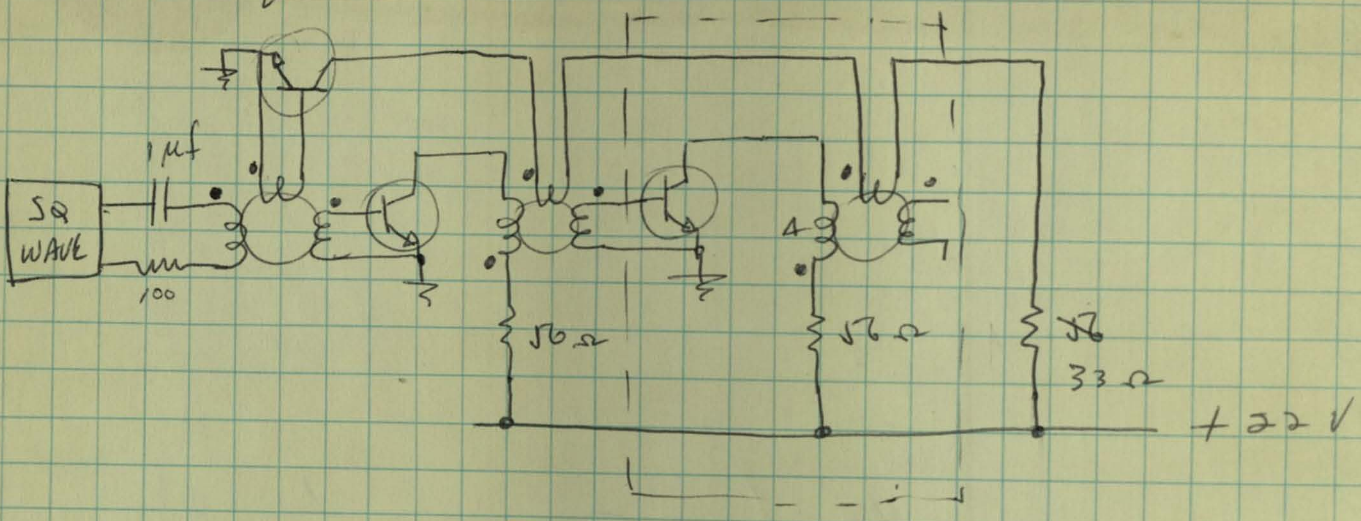


12/8/58 RTK

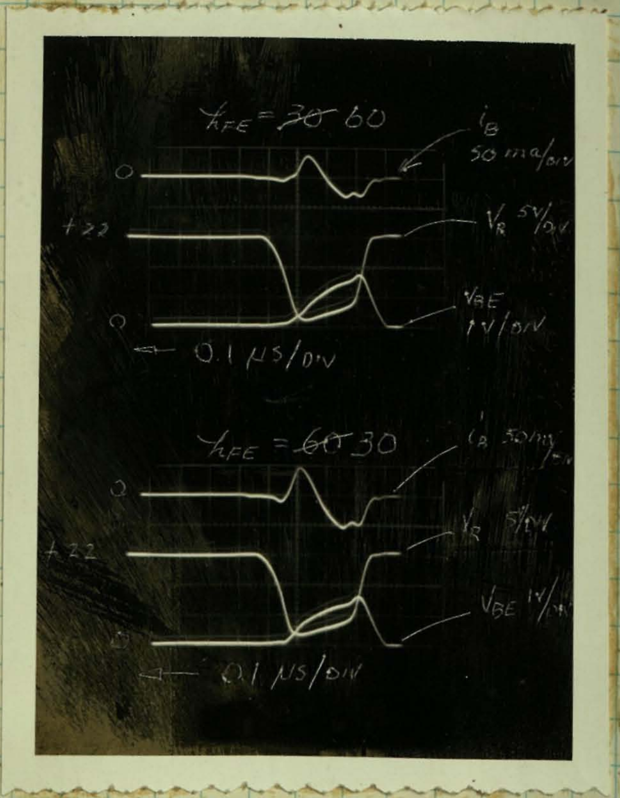
NI	$\frac{V_p}{N}$	T_s	$\frac{1}{T_s}$
.2	53 mv/turn	5 μsec	.2 μsec^{-1}
.3	128	1.8	.555
.4	205	1.1	.91
.5	290	0.76	1.31
.6		0.58	1.72

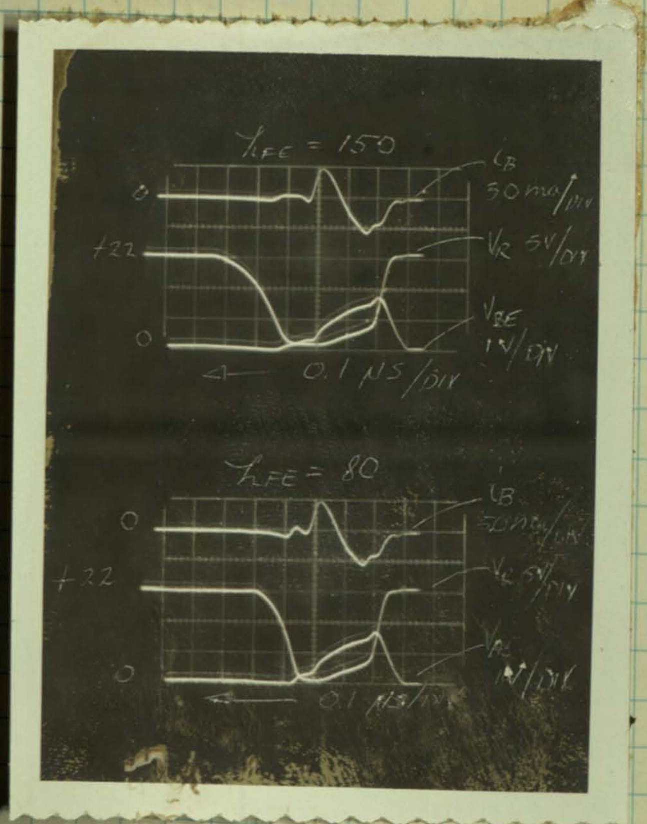
12/10/58

Set up the following portion of IBM Kingston circuit



Observed the current & voltage waveforms of ~~all~~ the stage enclosed by the dashed line. Took the following pictures for transistors having h_{FE} = 30, 60, 80, 150.





R T [illegible] 12/10/58

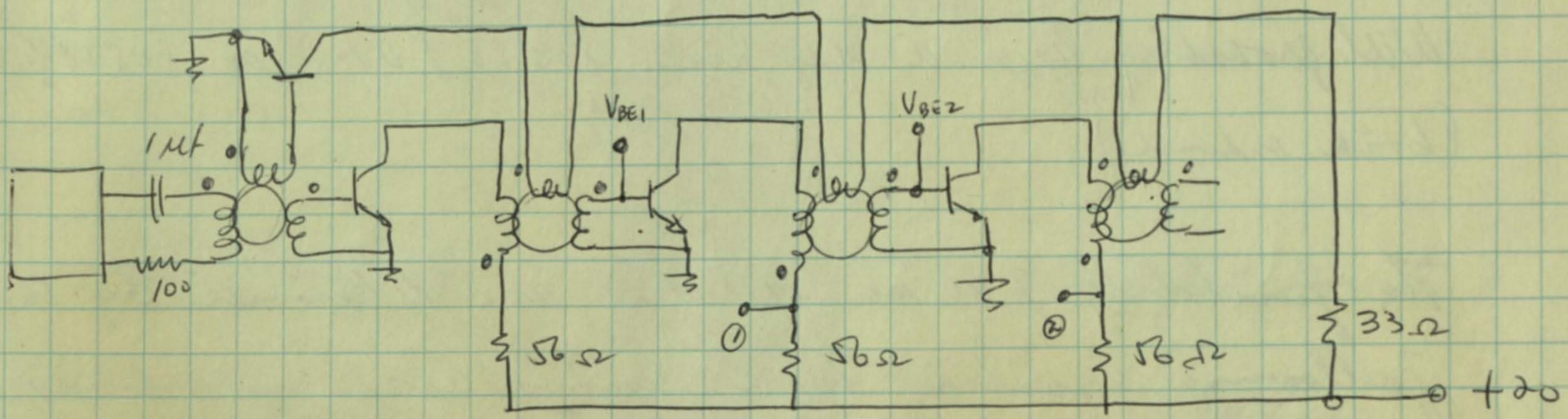
12/10/58 Cont

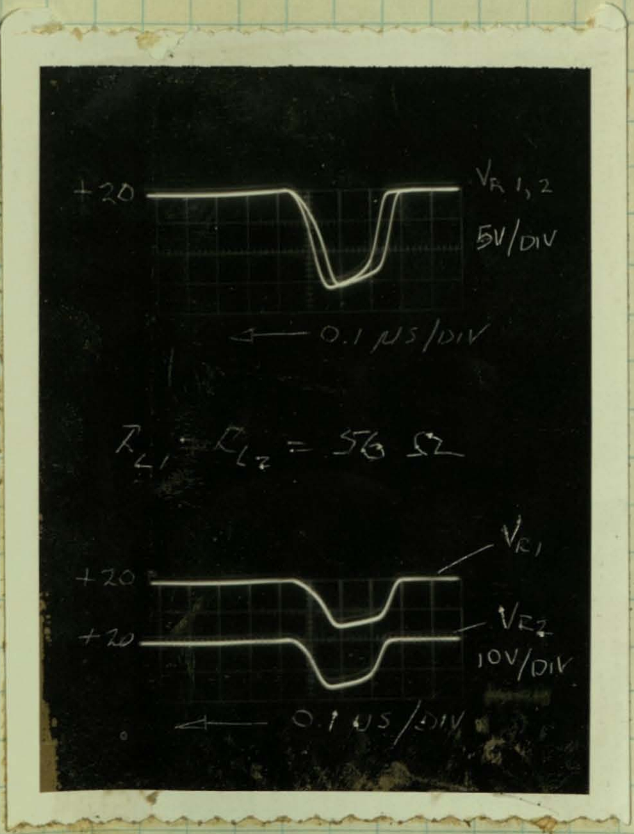
Will add another stage following the one observed to determine the effects of loading on the delays and pulse shrinkage per stage -

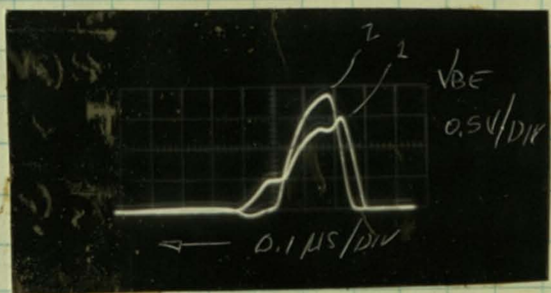
[signature] 12/10/58

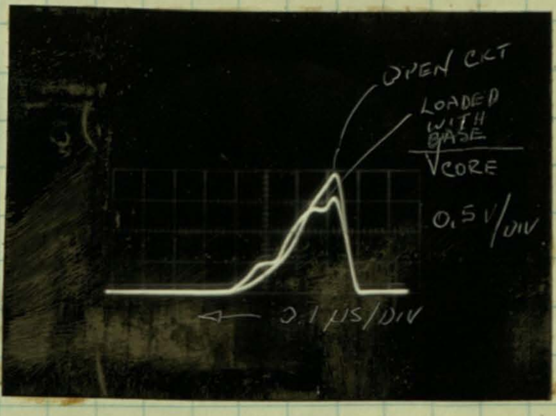
12/11/58

Added another stage to the core transistor circuit.







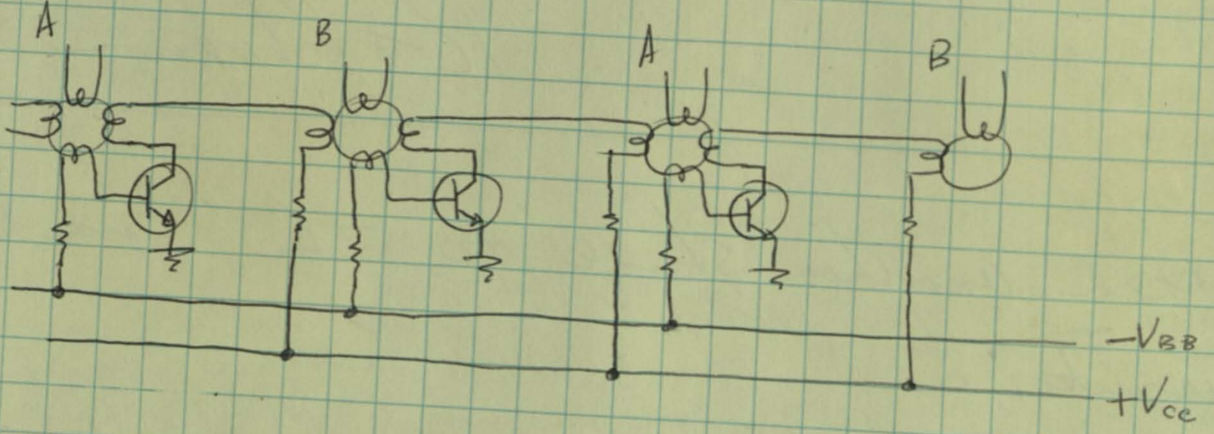


[signature] 12/11/58

12/15/58 - 12/16/58

Worked on the design of a 10 mc shift register for the next 2N697 data sheet.

The following circuit is being considered



Will probably use a mag inc. 80528 1/8 D10 or 80528 1/8 D5 (both ordered).

The feasibility of 10 mc operation was determined by the following equation for a loaded core.

$$T_s = \frac{\left(\frac{R_1}{R_2}x^2+1\right)N^2\Phi + R_1 C_s}{NV - R_1 (NI)_0} \qquad \text{(Page 60)}$$

N for minimum T_s:

$$N_m = \frac{R_1 (NI)_0}{V} \pm \sqrt{\frac{R_1 (NI)_0}{V} \pm \frac{R_1 C_s}{\left(\frac{R_1}{R_2}x^2+1\right)\Phi}} \qquad \text{(Page 66)}$$

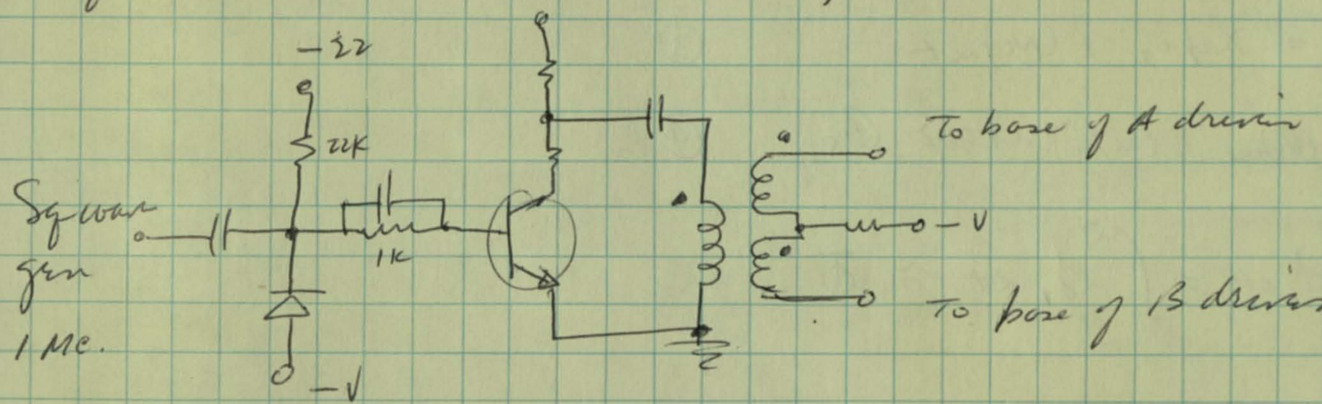
$$\simeq \sqrt{\frac{R_1 C_s}{\left(\frac{R_1}{R_2}x^2+1\right)\Phi}}$$

Ray T. Kikoshima 12/16/58

12/16/58

To me operation appears feasible providing that a cores with 5-8 maxwells capacity are used.
When the cores are received and the constants are determined, the circuit will be designed and breadboarded.

The following A-B driver is being considered.



The circuit was breadboarded and was not fast enough
Will continue work on the driver circuit

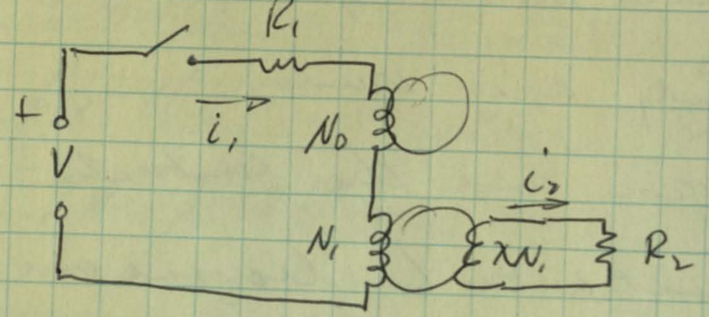
R T [signature]
12/16/58

12/17/58

Because the feedback circuit will be used (P. 96), the equation for the switching time of a core for the special case was derived using the same analysis as for the case on page 60

Roy T [signature] 12/17/58

12/17/58 cont.



$$V = R_1 i_1 + N_0 \dot{\phi}_0 + N_1 \dot{\phi}_1 \qquad (1)$$

$$X N_1 \dot{\phi}_1 = R_2 i_2 \qquad (2)$$

$$N_1 i_1 = X N_1 i_2 + (Ni)_{net} \qquad (3)$$

$$\int_0^{\tau_s} [(Ni)_{net} - (Ni)_0] \, dt = C_s \qquad (4)$$

$$\int_0^{\tau_s} \dot{\phi}_0 \, dt = \int_0^{\tau_s} \dot{\phi}_2 \, dt \cong \Phi \qquad (5)$$

From (1) thru (5) above, combining and integrating,

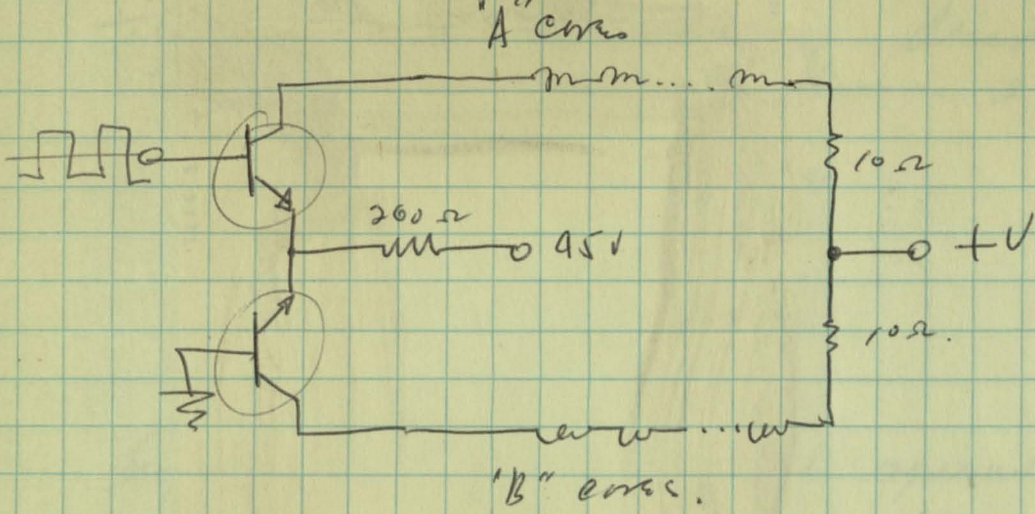
$$T_{s_1} = \frac{\left[\frac{R_1}{R_2} X^2 + 1\right] N_1^2 \Phi + N_1 N_0 \Phi + R_1 C_s}{N_1 V - R_1 (Ni)_0} \qquad (6)$$

$$T_{s_0} = \frac{(N_0 + N_1) N_0 \Phi + R_1 C_s}{N_0 V - R_1 (Ni)_0} \qquad (7)$$

Will try current steering for the A and B Advance drivers.

R T Kekisian 12/17/58

12/17/58 (cont)

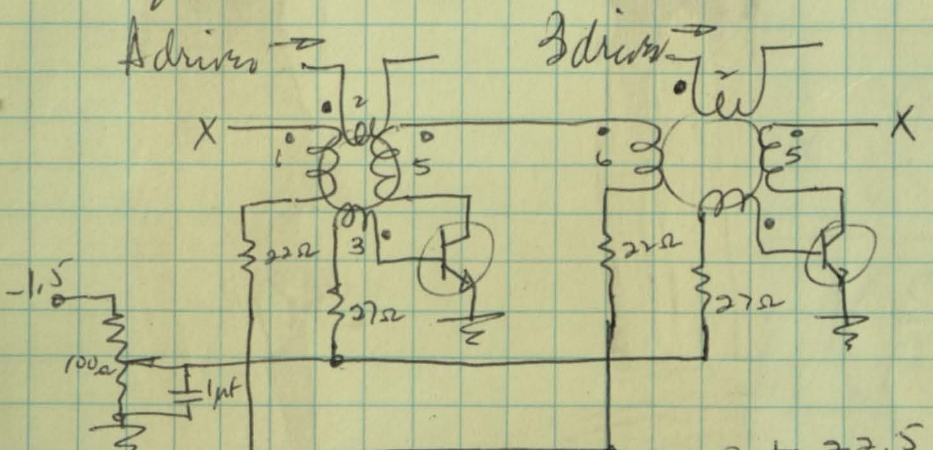


The above circuit was breadboarded.

[illegible signature] 12/17/58

12/18/58

Operated the following 2 stage (one bit) shift register.

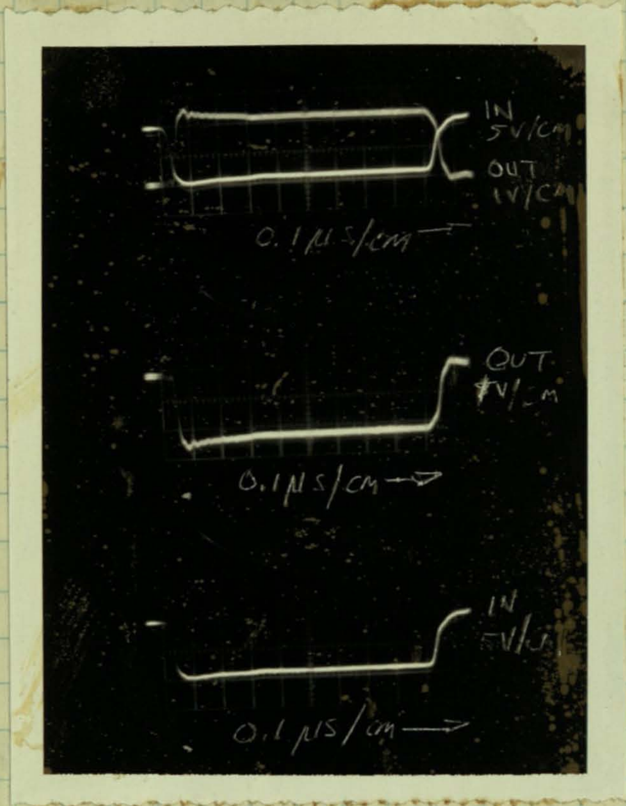


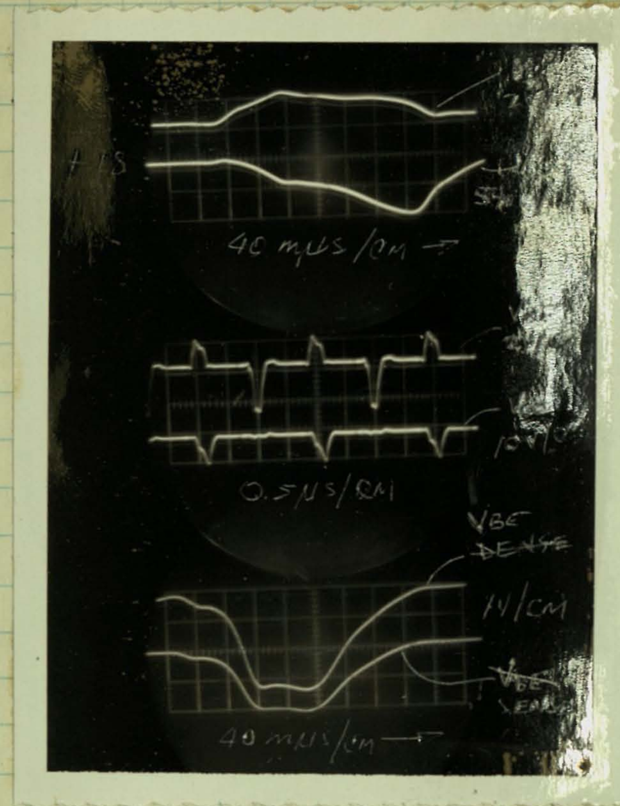
Cores: 80520 1/8 D10

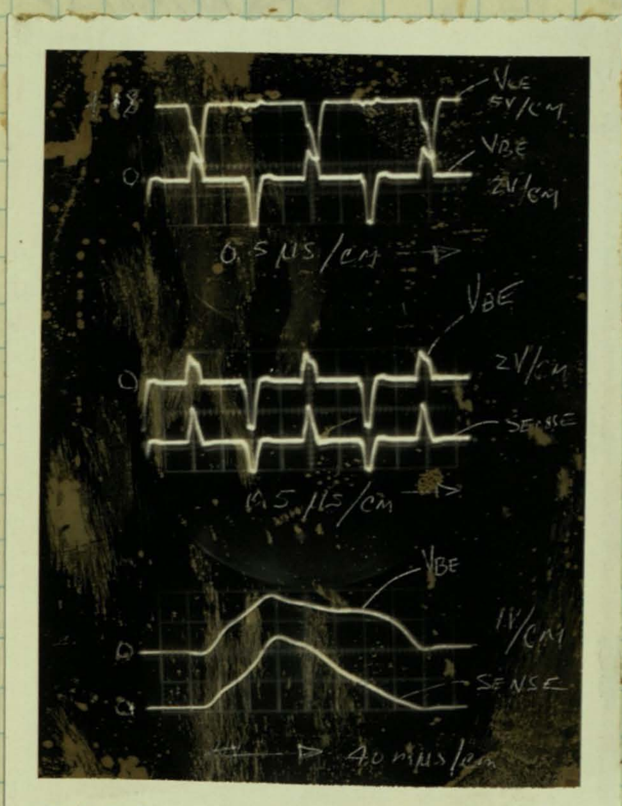
Tied the circuit at X–x and operated it as a ring. Took pictures of the waveforms at various points.

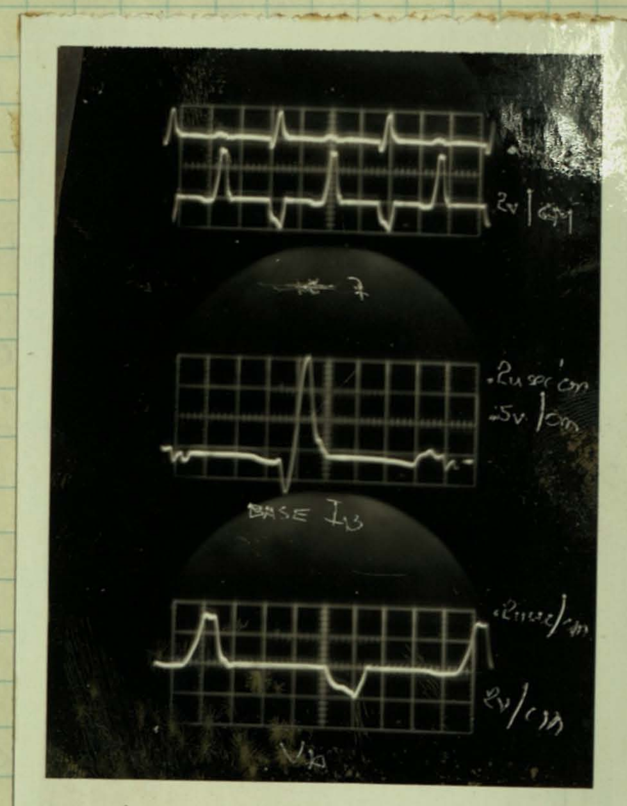
[illegible signature] 12/18/58

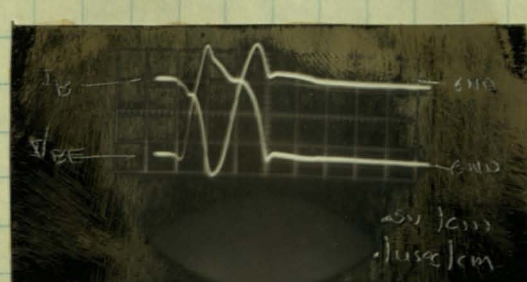
100 15/18/57 cont.











— across 27 Ω

12/18/58 Cont.

The current steering drivers operated with the following rise time etc.

$t_r = 19$ mμs $\quad V+ = 12$ Volts
$t_D = 22$ "
$t_f = 90$ " $\quad V- = -4.5$ Volts.
$t_s = 10$ "

Since this circuit will operate at a 2 mc bit rate operation at 10 mc with the 5 maxwell cores looks feasible.

By differentiating equation (6) on page 58 with respect to N_1 and setting it to zero, the number of turns for minimum T_s can determined

$$N_1(\min T_s) = \frac{R_1 (Ni)_0}{V} \pm \sqrt{\left(\frac{R_1(Ni)_0}{V}\right)^2 + \left(\frac{1}{\frac{x^2}{R_2}+\frac{1}{R_1}}\right)\left(\frac{C_s}{\Phi} + \frac{N_0 (Ni)_0}{V}\right)}$$

$$\simeq \sqrt{\left(\frac{1}{\frac{x^2}{R_2}+\frac{1}{R_1}}\right)\left(\frac{C_s}{\Phi} + \frac{N_0 (Ni)_0}{V}\right)}$$

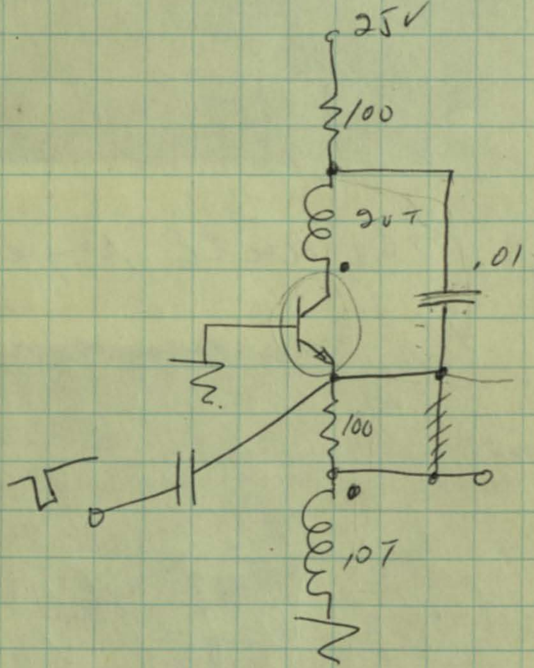
R T Kihoki[?] 12/18/58

12/19/58

Resumed work on the blocking oscillator study. Grounded base circuit are being considered.

12/22/58

Tried the following circuit.



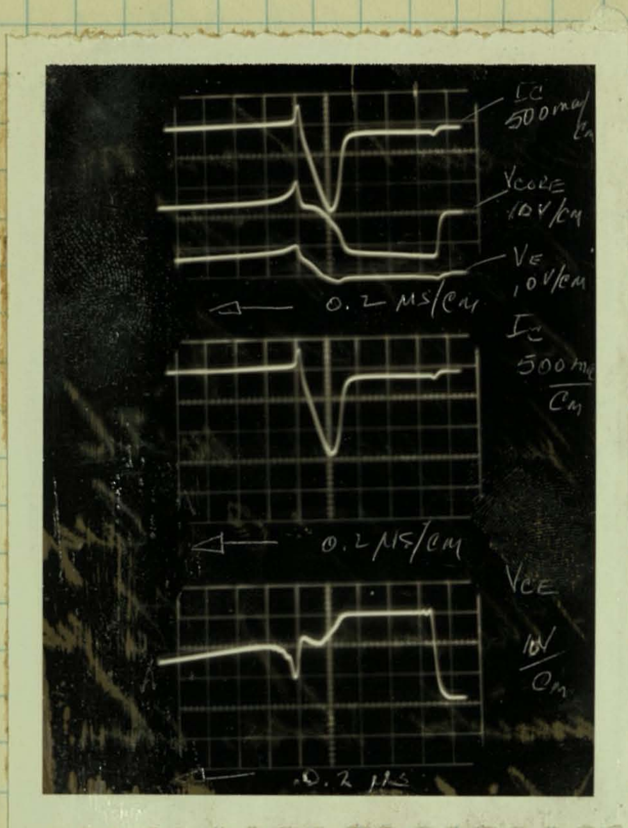
When the supply voltage is turned "on", the capacitor charges (the transistor is cut off) and the core is set to one remanance state. When a negative trigger pulse is applied, the transistor is turned "on" switching the core to a "1" state. The winding in the emitter circuit is such that it keeps the transistor "on" until the core saturates and the $\dot{\phi}$ goes to zero. The transistor then turns "off" and the core is reset by the capacitor charge current. The pulse width is approximately

$$T_w = \frac{2N\Phi_r}{V}$$

Pictures were taken of the various waveforms

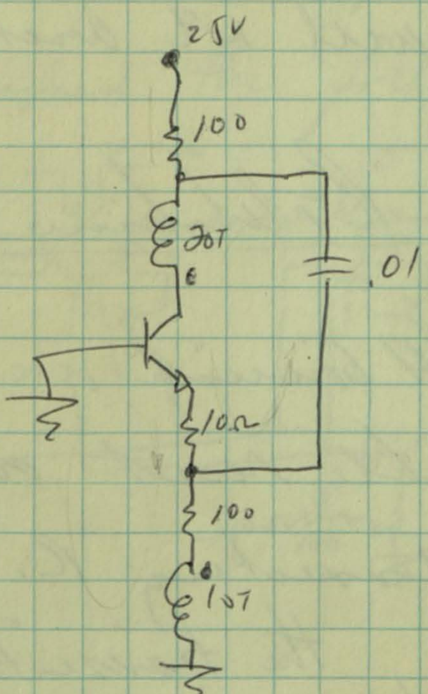
R T Kirkpatrick
12/22/58

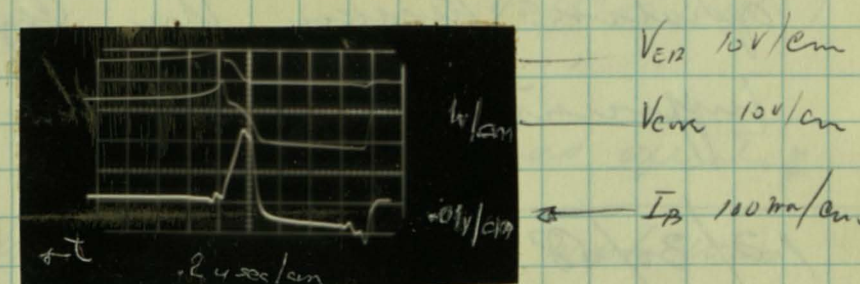
12/22/58



The picture of the collector current shows a peak current of 1.5 Amps when the core saturates. To reduce this peak, a ten ohm resistor was added in the emitter circuit.

This circuit appears to be better than any of the grounded emitter circuits tried. The rise time is shorter and not as dependent on the trigger pulse rise time.





[illegible signature] 12/22/58

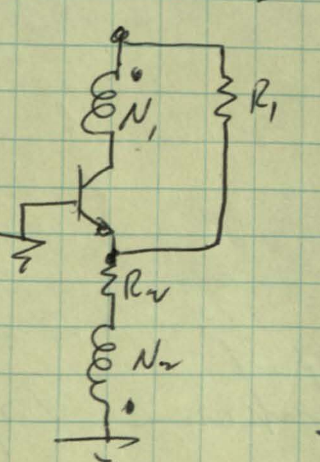
12/29/58

The operation of the grounded base circuit shown on page 103 depends upon the discharging of the capacitor so that the core can be reset by the charge current. For an output pulse with small droop, C should be large. But if C is large, it is not sufficiently discharged at the end of the pulse to reset the core. If the transistor stores, then the capacitor will discharge with high currents. Any attempt, therefore, to decrease the high currents after the core switches will make the circuit inoperative because the capacitor will not discharge sufficiently to reset the core.

R T Rubinstein 12/29/58

12/30/58

Discussed the problem with VH Grinich. He suggested trying a d.c. trickle reset on the core as shown. By connecting R_1 to



the top of R_2, the transistor will be pulled "off" harder. With $N_1 = 25$ and $N_2 = 10$, $R_1 = 1k$, $R_2 = 100$ the circuit operated with a rise time (max) of .0.1 μseconds.

R T Rubinstein 12/30/58

12/30/58 Cont.

The fall was very good and the top was flat with negligible droop. The slow rise time may be due to the trickle reset bias that must be overcome in going from "off" to "on".

R T Kihnhanen 12/30/58

Received cores from Magnetics, Inc. 80528 D3, D7, D14

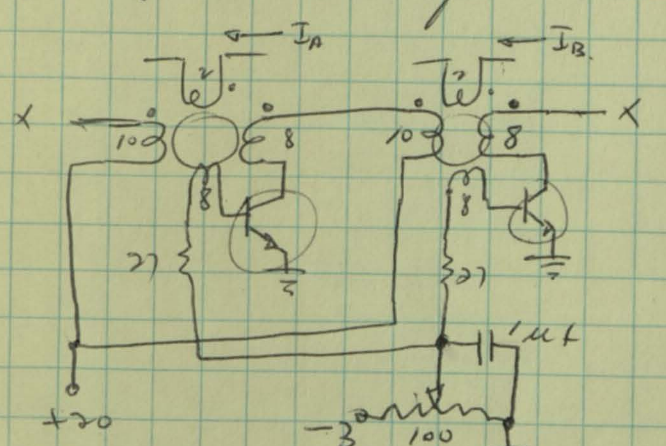
D. Ferris took switching curves (on next page)

Will use the 80528 D3 for the 10 mc shift register.

R T Kihnhanen 1/2/59

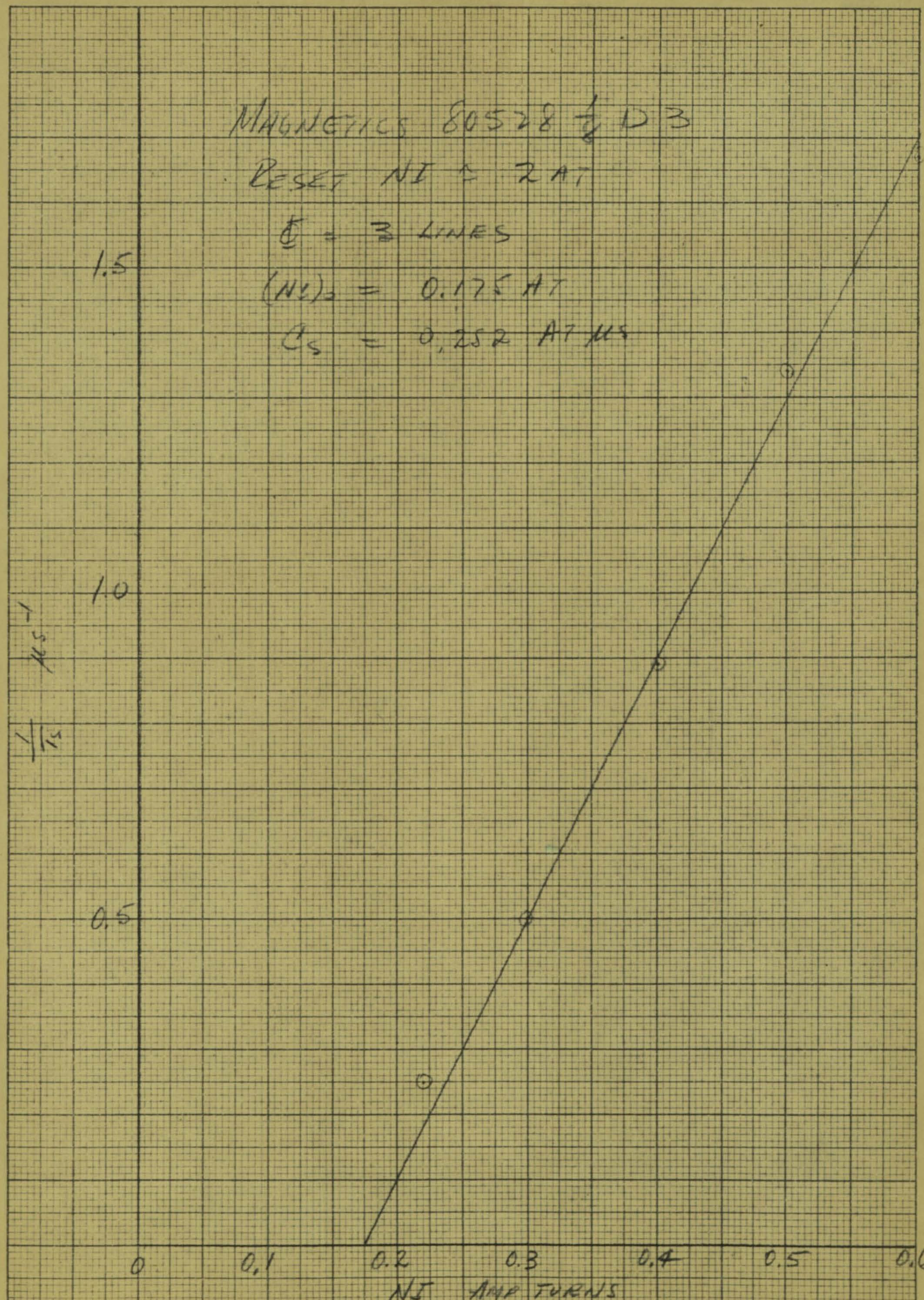
1/5/59 – 1/6/59

Designed the following cht

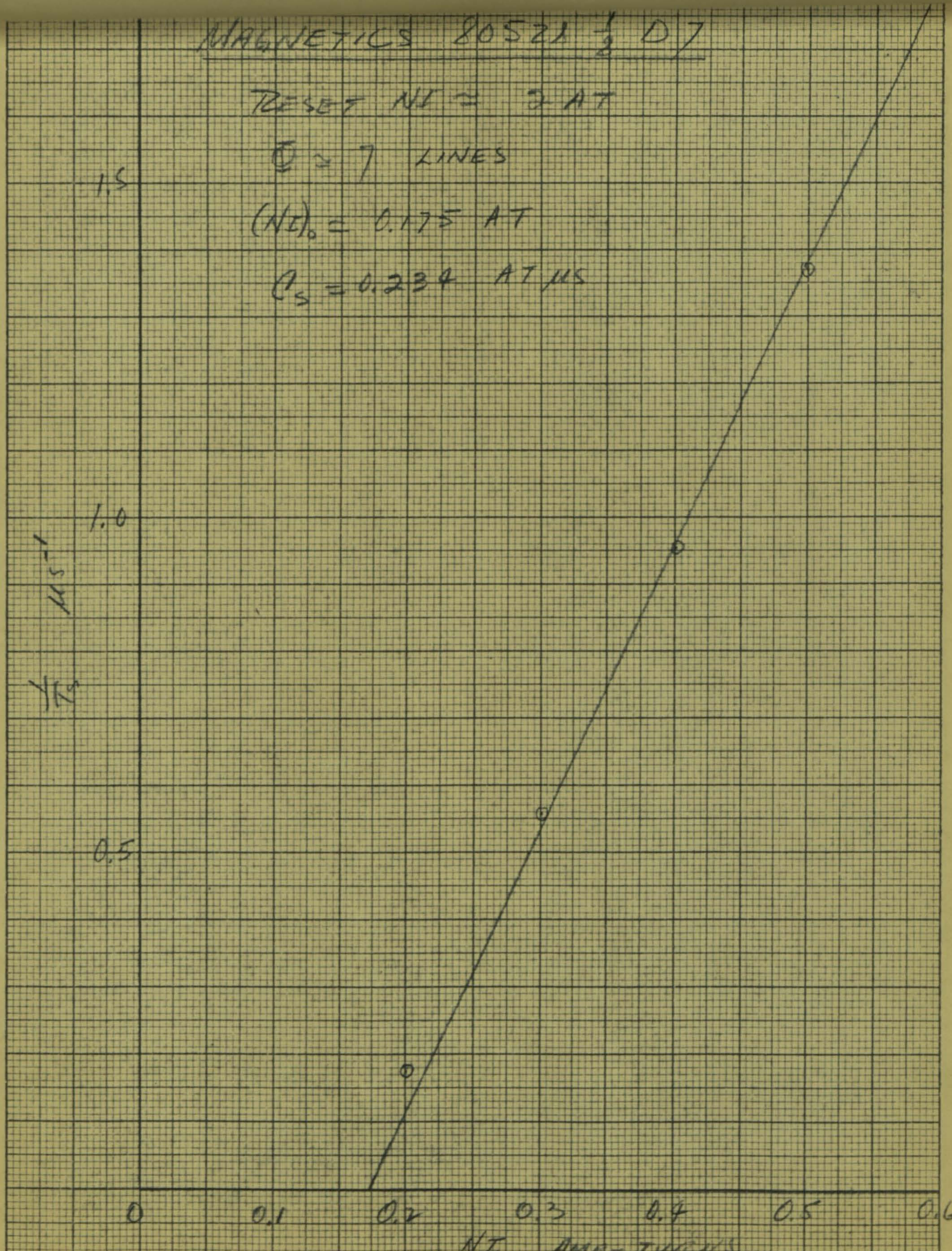


The circuit did not operate because the Drive mmf was not sufficient to switch the core at a fast enough rate to produce a peak voltage which would overcome the Base-emitter threshold voltage. The 2 turn drive windings were changed to 5 turns and the circuit operated.

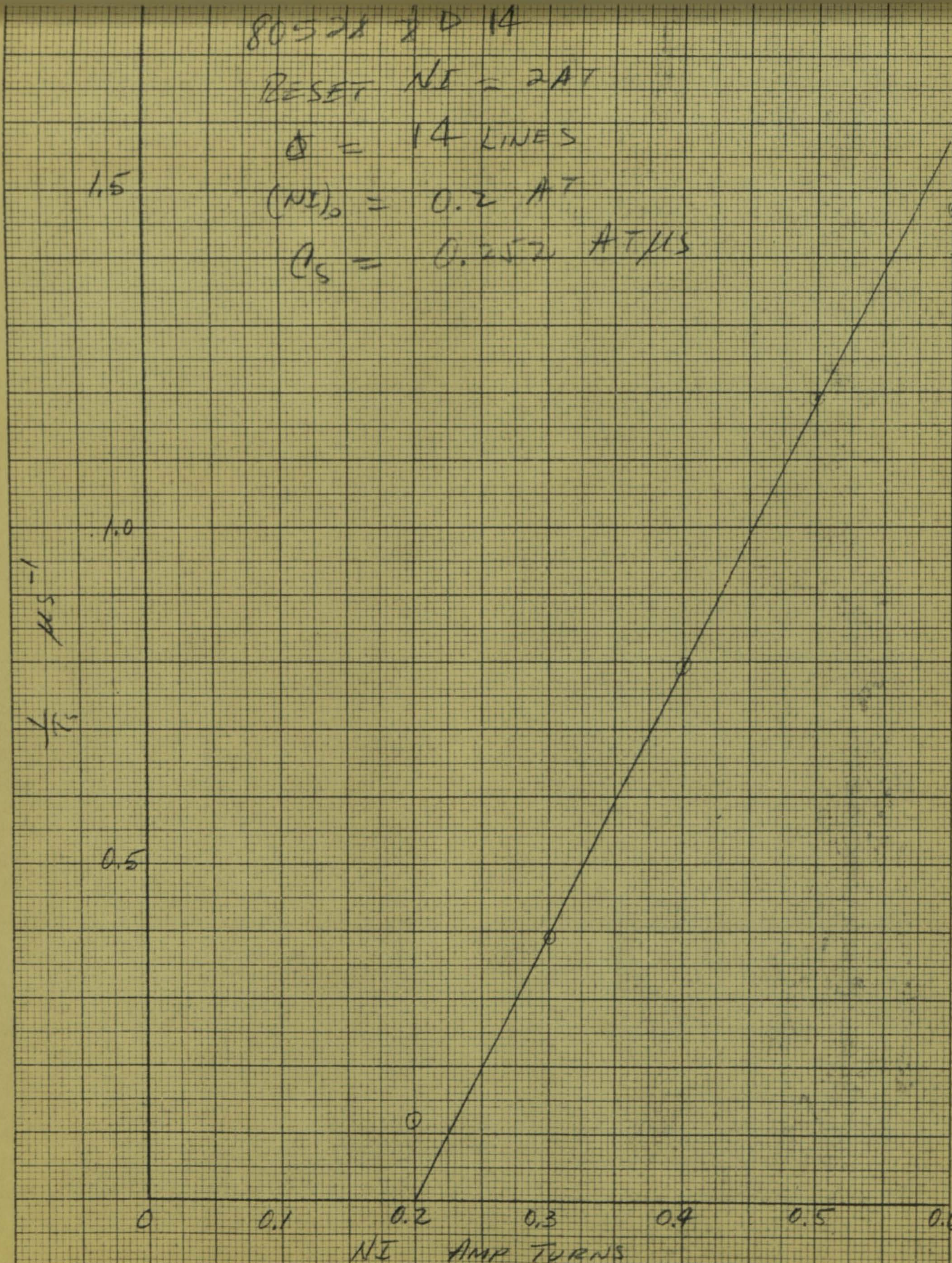
R T Kihnhanen 1/6/59


MAGNETICS 80528 1/8 D 3
RESET NI = 2 AT
Φ = 3 LINES
(NI)₀ = 0.175 AT
Cs = 0.252 AT μs
1.5
1.0
0.5
1/Ts μs⁻¹
0
0.1
0.2
0.3
0.4
0.5
0.6
NI AMP TURNS

RTK 1/2/59

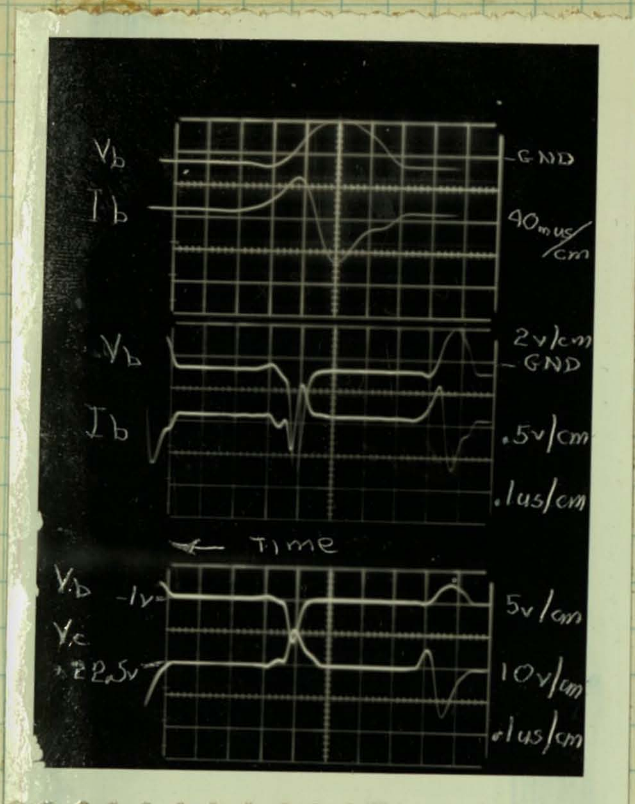

MAGNETICS 80521 1/2 D7
RESET NI = 2 AT
Φ ≈ 7 LINES
(NI)₀ = 0.175 AT
Cs = 0.234 AT μs
1.5
1.0
0.5
1/Ts μs⁻¹
0
0.1
0.2
0.3
0.4
0.5
0.6
NI AMP-TURNS

RTK 1/2/59

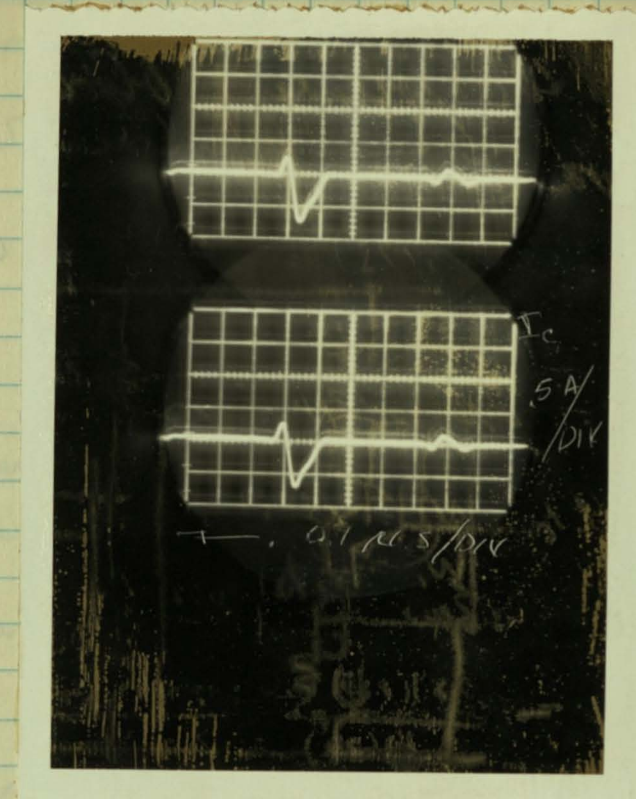

80528 2 D 14
RESET NI = 2AT
Φ = 14 LINES
(NI)₀ = 0.2 AT
Cs = 0.252 AT μs
1.5
1.0
0.5
1/τs μs⁻¹
0
0.1
0.2
0.3
0.4
0.5
0.6
NI AMP TURNS

1/6/59

Pictures were taken of the various waveforms —

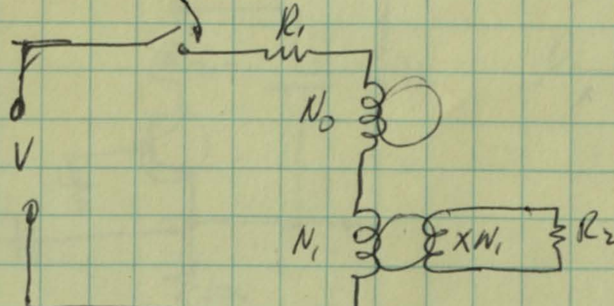


≈ 20ma/cm



The circuit will operate at a 5 mc bit rate but will not reach 10 mc. The speed determining factor now is the transistor rather than the core.

The design shown on page 105 requires a considerable amount of collector current. Calculations were again made to reduce the current.



$$T_{s_0} = \frac{(N_0+N_1)N_0\,\Phi + R_1 C_s}{N_0 V - R_1 (NI)_0}$$

$$T_{s_1} = \frac{\left(\frac{R_1 X^2}{R_2}+1\right)N_1^2\,\Phi + N_1 N_0\,\Phi' + R_1 C_s}{N_1 V - R_1 (NI)_0}$$

[signature] 1/6/59

 1/6/59

$$N_0 + N_1 < \frac{V\tau_s}{\Phi} = \frac{25(.04)}{.03} = 31$$

$$\left[NI - (NI)_0\right]\tau_s = C_s$$

$$(NI - .175) = \frac{.252}{.04} = 6.3$$

$$NI = 6.1$$

for $I = 0.5$ $N = 12$

Let $N_0 = 12$
$N_1 = 10$

$$\tau_{s_0} = \frac{(22)(12)(.03) + 2.52}{12(25) - 1.75} \approx .035\ \mu s$$

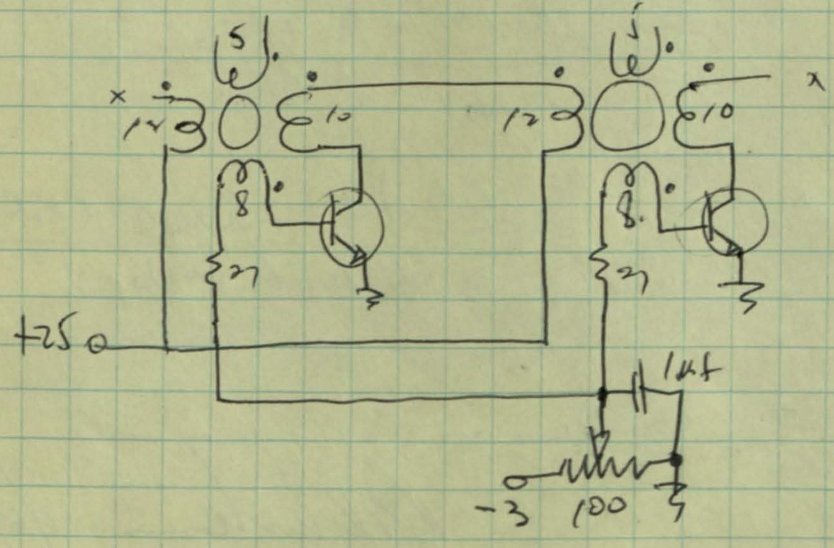
$$.04 = \frac{\left[\frac{R_1}{R_2}x^2 + 1\right]100(.03) + 120(.03) + 2.52}{250 - 1.75}$$

$$10 = 3\left[\quad\right] + 3.6 + 2.52$$

$$\frac{x^2}{R_2} = .03$$

for $x = 1$ $R_2 = \frac{1}{.03} = 33\ \Omega$

Circuit Now appears as follows

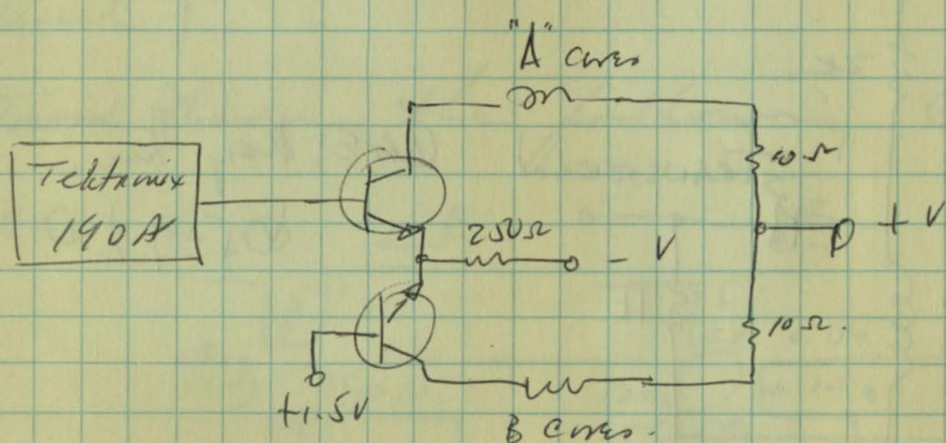


R. Kikuchi(?) 1/6/59

1/7 — 1/9/59

With the circuit as shown on page 108, tried driving the current steering driver with the Tektronix 190A

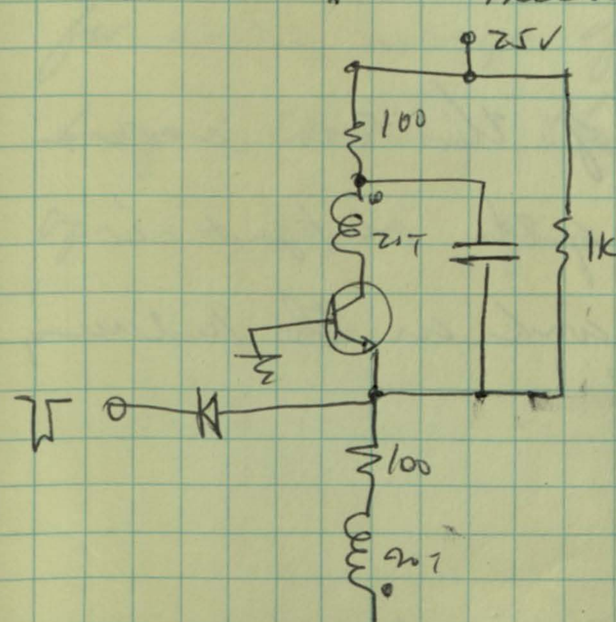
Circuit operated satisfactorily



The shift register circuit wiring was cleaned up and the power supply lines were bypassed. The operation at 5 mc appears stable.

1/9/59.

Resumed work on the Bulova Blocking oscillator circuit. Tried the following circuit.

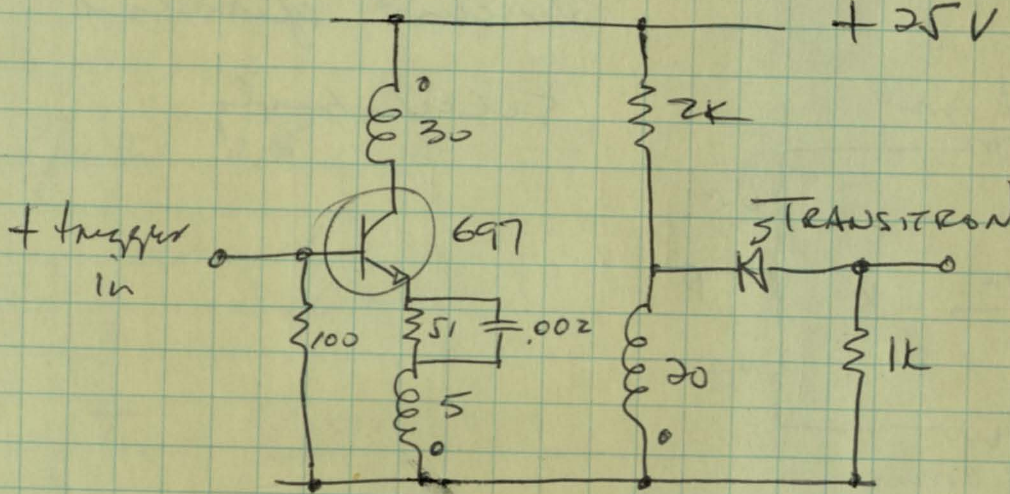


The droop is specified at less than 15%.

R T Kihoskimi 1/9/59

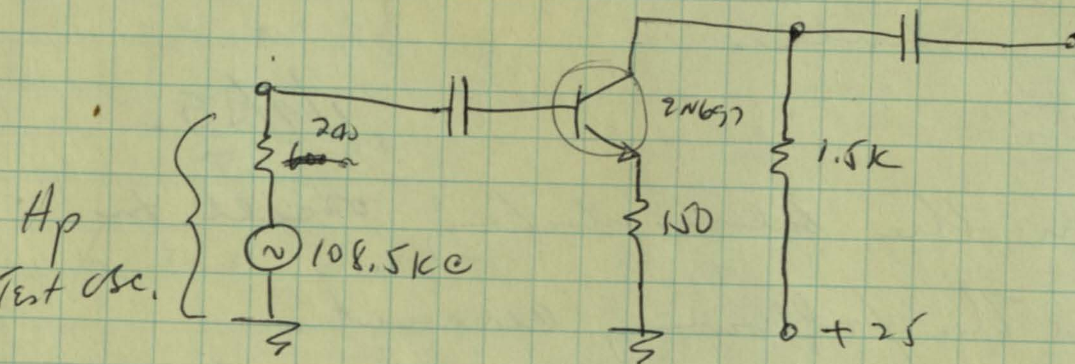
1/12/59

Tried the following blocking oscillator circuit for Bulova.



Cer E! May Inc. 80529 ¼ D 30

This circuit appears to be the best for this application. Also tried Bulova's triggering circuit.



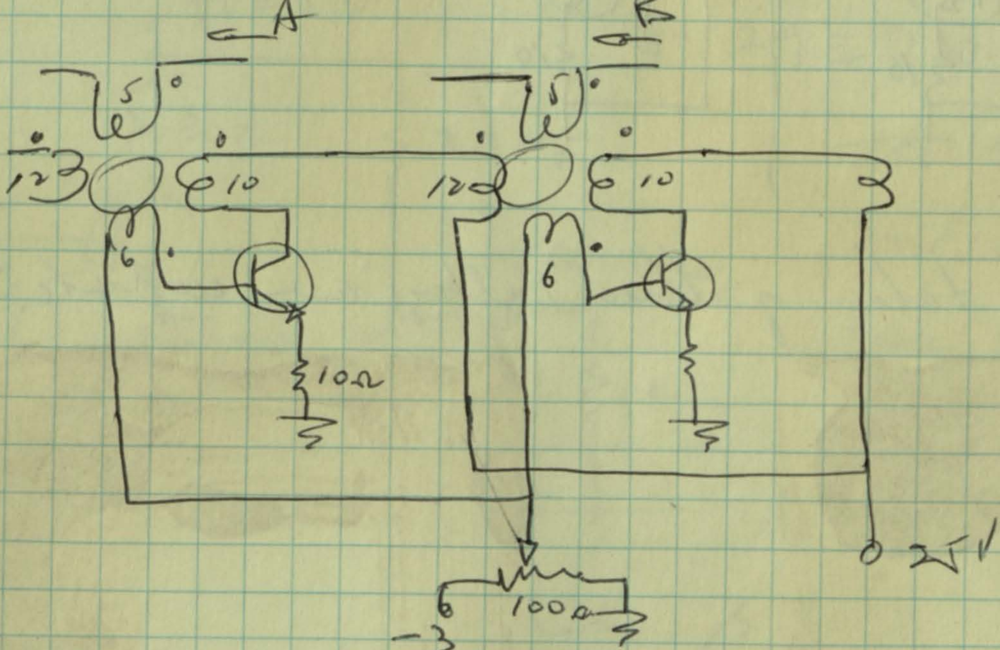
The b.o. triggered on any point of the sine wave — even at the top. The rise time of the output is approximately 50 mμs. Will work on ~~the~~ reducing this to 30 mμs.

R. T. Kikuchi 1/12/59

1/12/59.

Worked on the 5 mcs shift register. The operation of the circuit as shown on page 108 was marginal especially with 2N697's (high h_{FE} units).

~~Found~~ Made the following changes

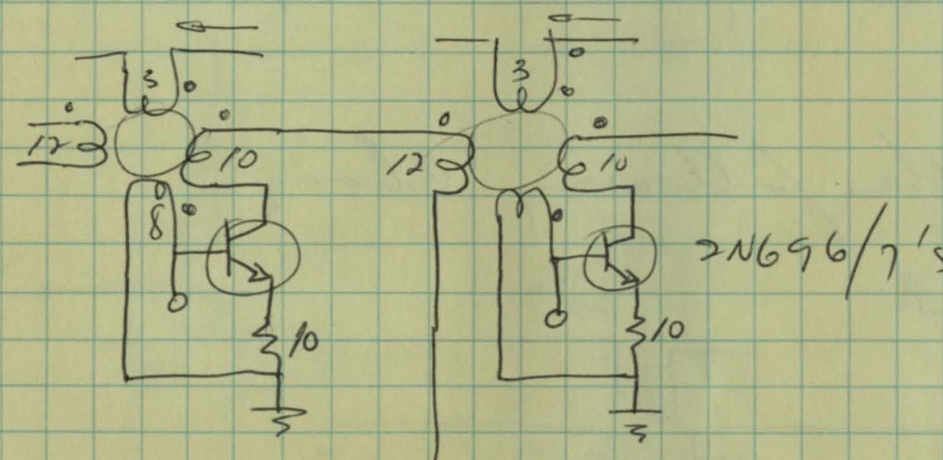


The operation of the above circuit was very stable for wide swings of voltage, drive & bias. Will try reducing the base input turns to 5 turns and operate with zero bias -

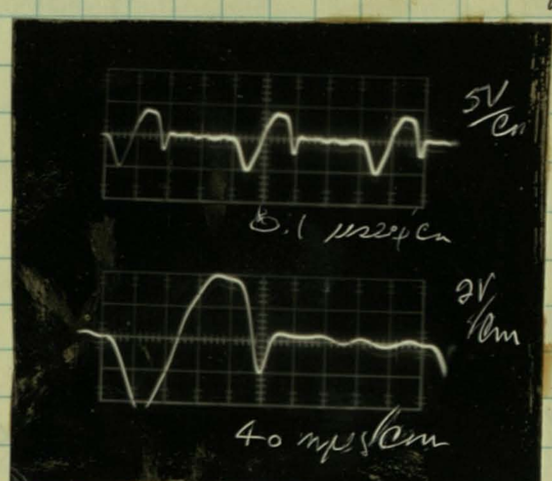
[signature] 1/12/59

1/13/59 - 1/14/59

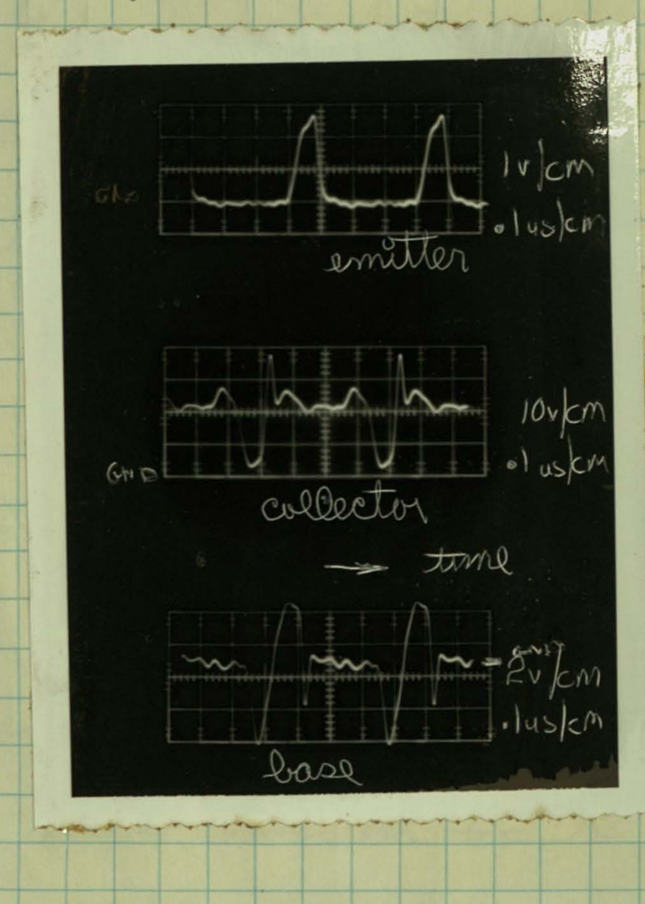
After discovering an error in the wiring of the core-transistor shift register, the circuit was changed to the following;

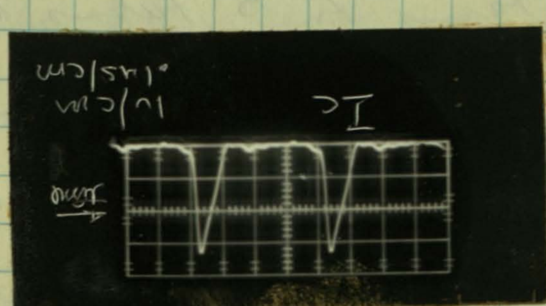


Pictures were taken of the voltage and currents.



Output





1.00 ma/DIV

0.1 μsec/DIV

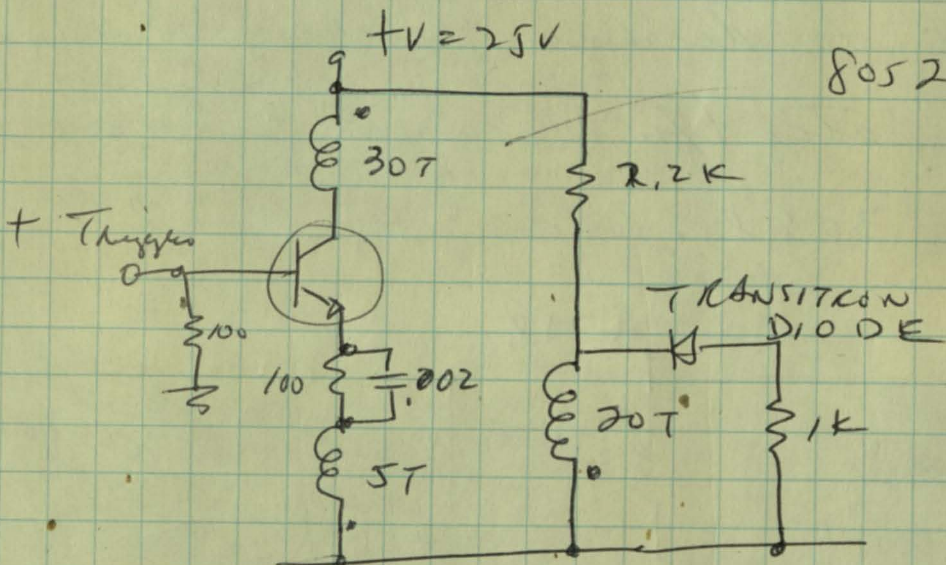
I_C

[illegible]

1/13/59 - 1/14/59

The circuit was very stable and operated with wide variation of the voltages and drive.

Worked on the blocking oscillator circuit for Bulova.



80529 1/4 D30

The circuit would not meet the rise time spec (< 50 mμs, typical 30 mμs)

Obtained sample transistors from Motorola. The rise time and width were measured for each sample

Batch 792-1788 1/7/59

ABA

	tr	width
1	55 mμs	1.05 μsec
2	65	
3	60	
4	65	
5	55	
6	65	
7	63	
8	53	
9	65	
10	60	

ACA

	tr	width
1	65	1.05
2	63	
3	65	
4	58	
5	63	
6	70	
7	65	
8	63	
9	70	
10	70	

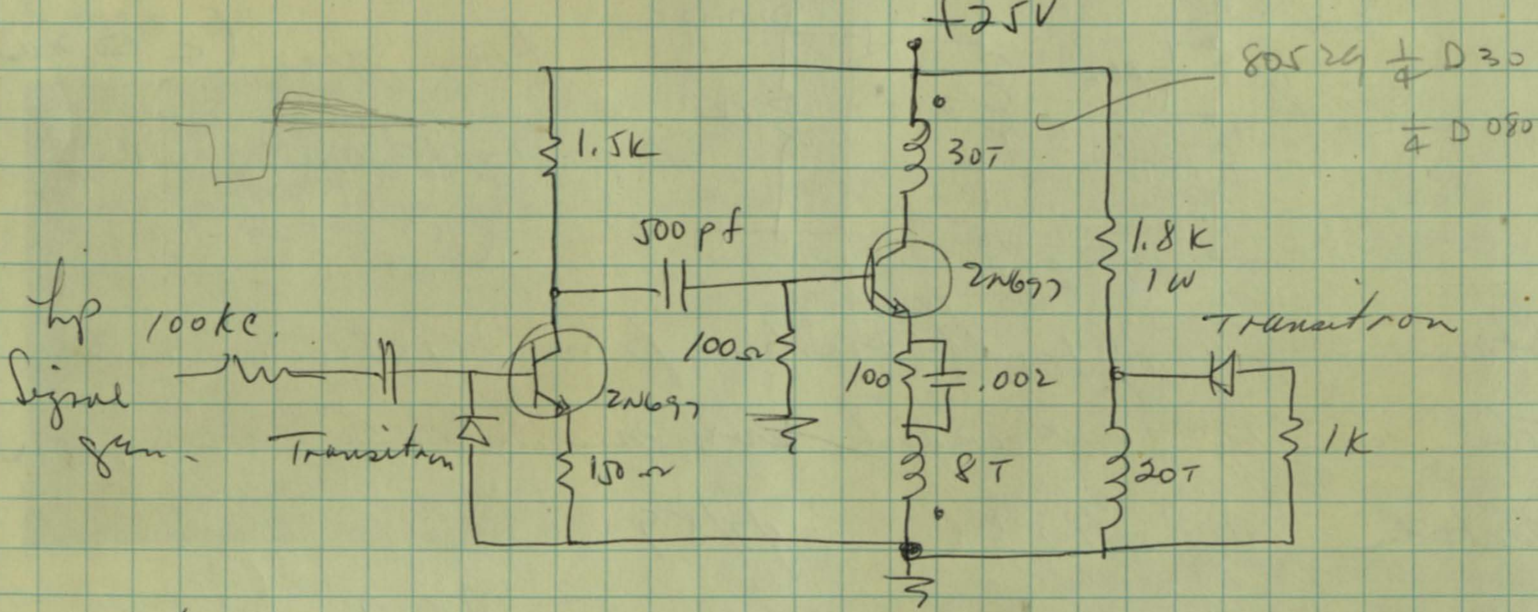
R T Abraham 1/14/59

1/14/59
The results show that the rise times are generally longer for the lower β unit, as expected.

R T Kikoshima 1/14/59

1/16/59

Tried various methods to decrease the rise time. The optimum turns ratio (for minimum rise time) was found to be 30:8.



The rise time is now approximately 30 mμs. Will make temperature tests and obtain data.

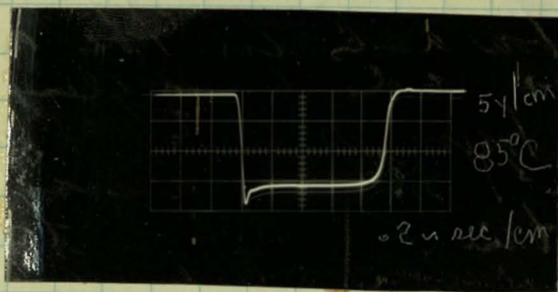
R T Kikoshima 1/16/59
1/19/59

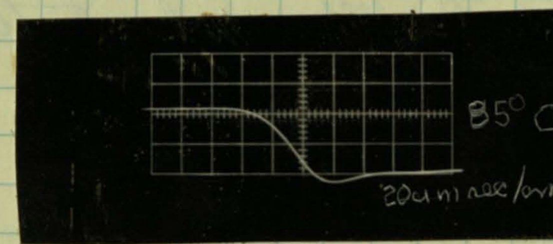
Ran temperature test on the above circuit

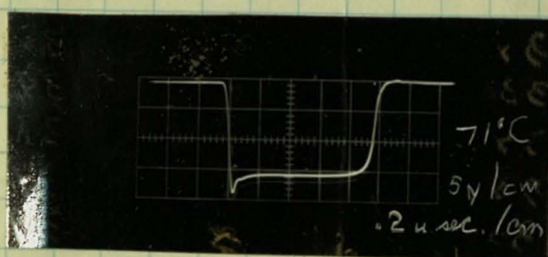
R.T. Kikoshima

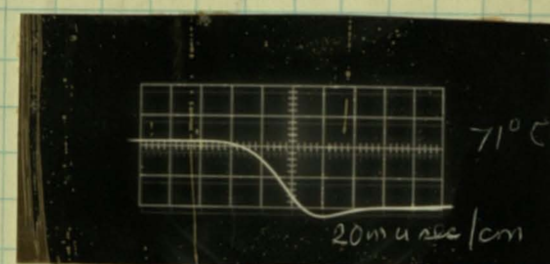
1/17/57.

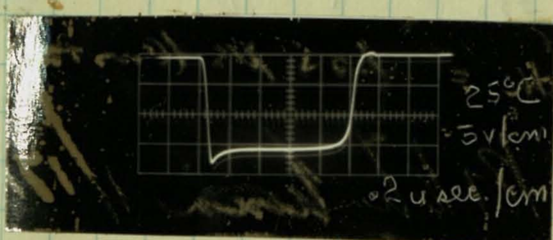
CRT WAS NOT LINED UP WITH GRATICULE

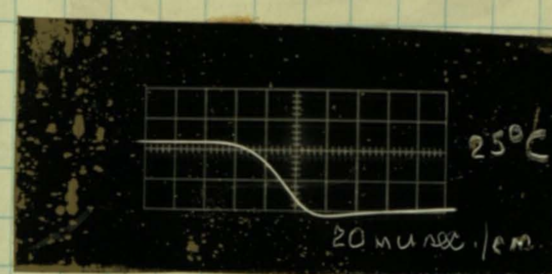


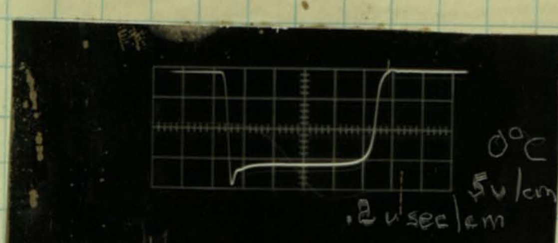


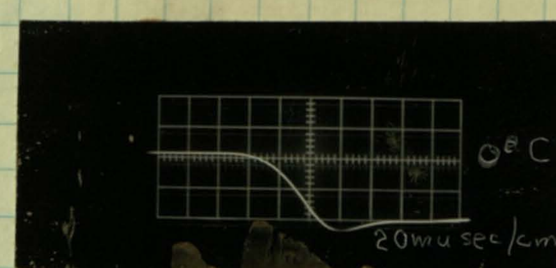


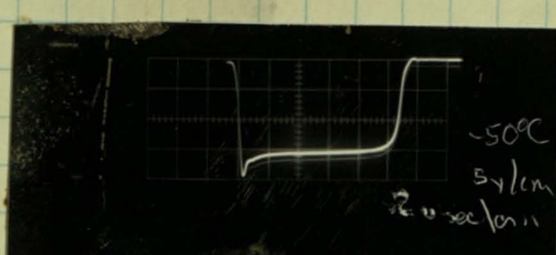


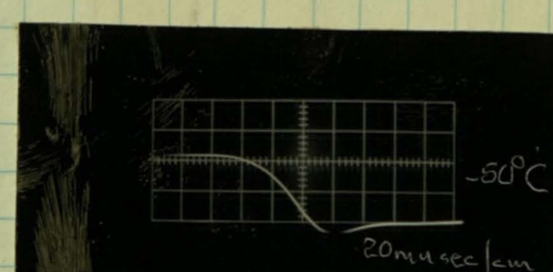








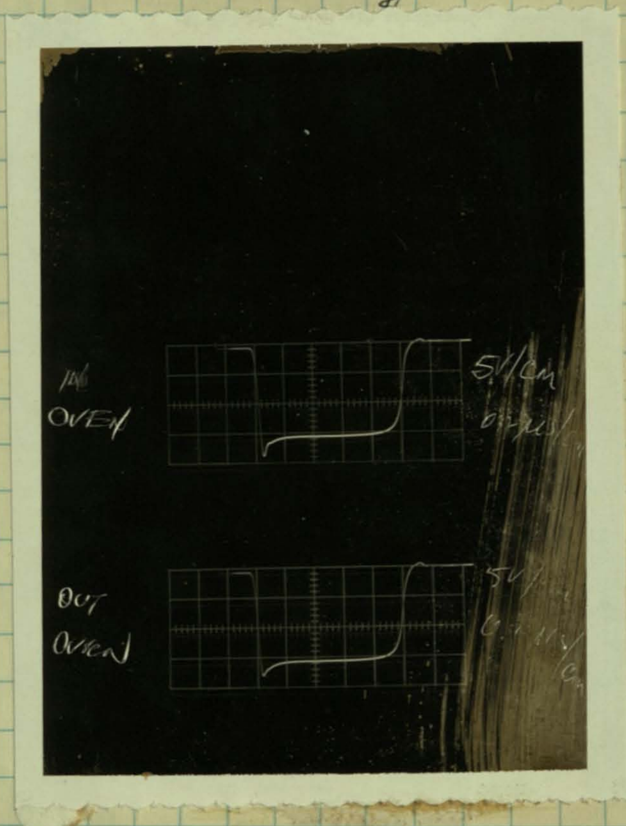




[illegible] 1/17/57

1/17/59

The increase in the overshoot is due to the added lead length when the breadboard is in the oven.



Results of trying 20 units

ABB	t_{rise}	ACB	t_{rise}
1	32 mµs	1	32 mµs
2	34	2	33
3	32	3	32
4	33	4	34
5	32	5	38
6	32	6	31
7	30	7	34
8	32	8	32
9	30	9	32
10	33	10	30

t_{width} = 1.05 µs (Constant)

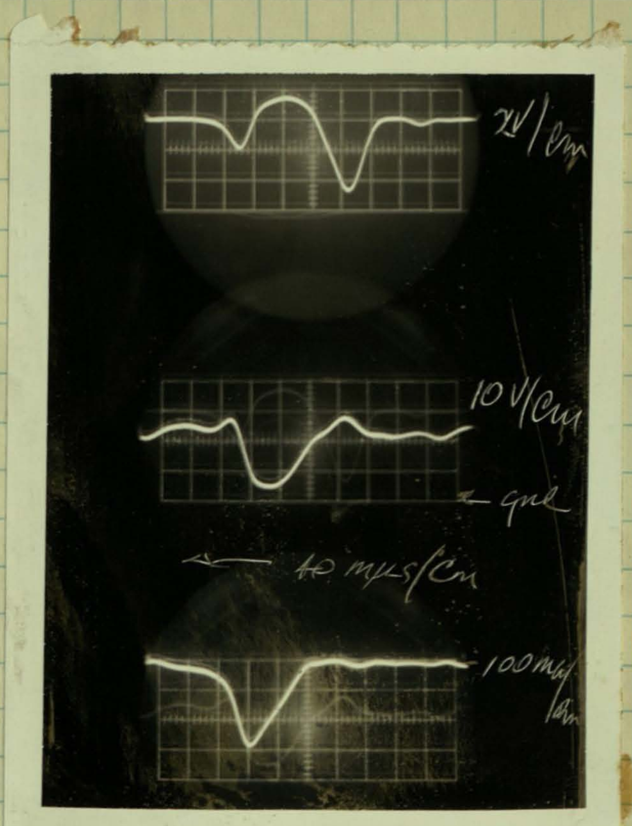
[signature] 1/17/59

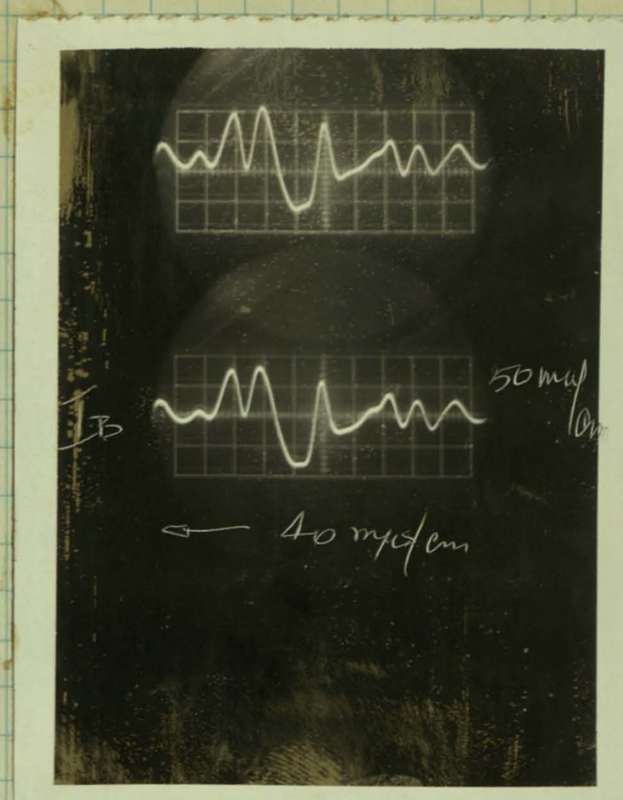
1/20/59

V_{BE}

V_{CE}

I_C



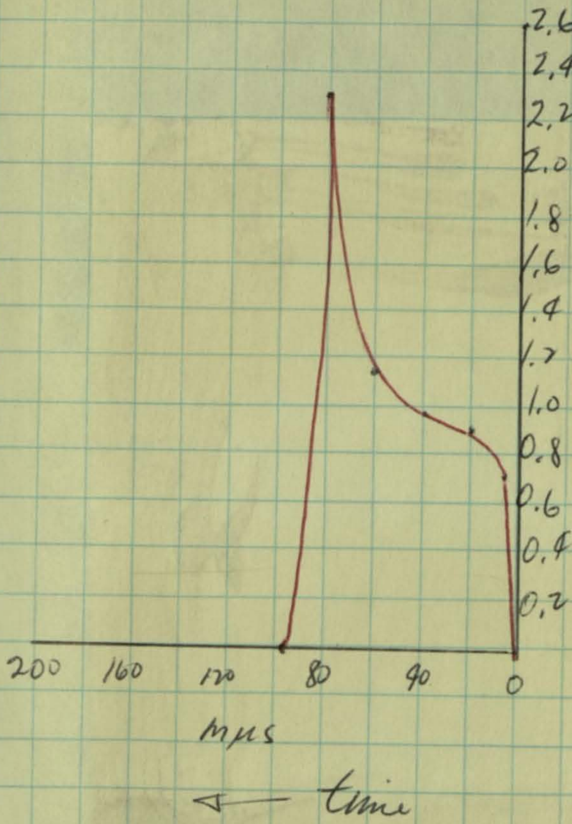


I_B

1/20/59 [signature]

1/20/59

Set up the 5 mc ~~ring~~ shift register as a one bit ring and took pictures of the I_B, I_C, V_{BE} and V_{CE} to get an idea of the power dissipation.



t	V_{ce}	I_c	P_c
20	11	.08	.88
40	6	.160	.96
60	5	.230	1.15
80	8	.290	2.32
96	0	–	0

Peak Base dissipation ≃ (1.5V)(80 ma) ≃ 120

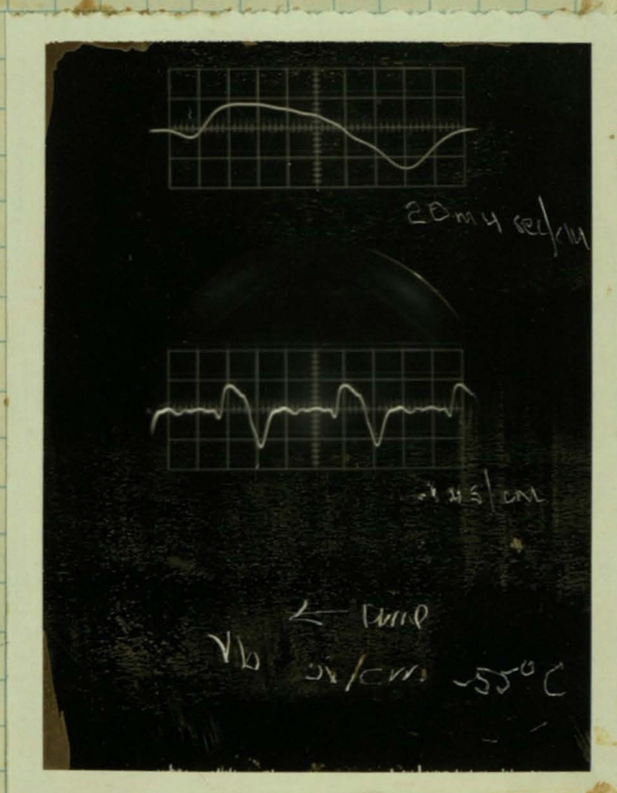
The average collector dissipation over a period of 100 mμs is approximately 500 mw. The total transistor dissipation is approximately 550 to 600 mw when the shift register is packed (all "1's")

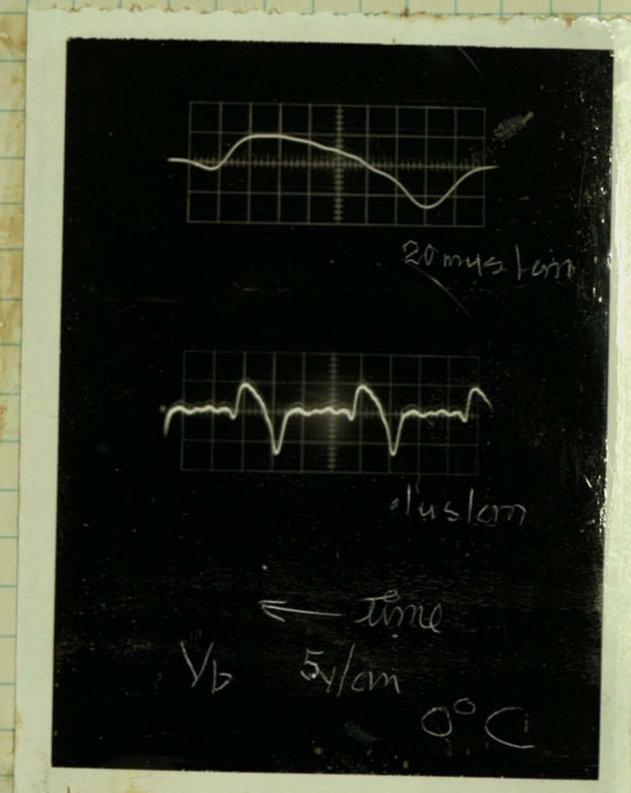
Will run temperature tests tomorrow

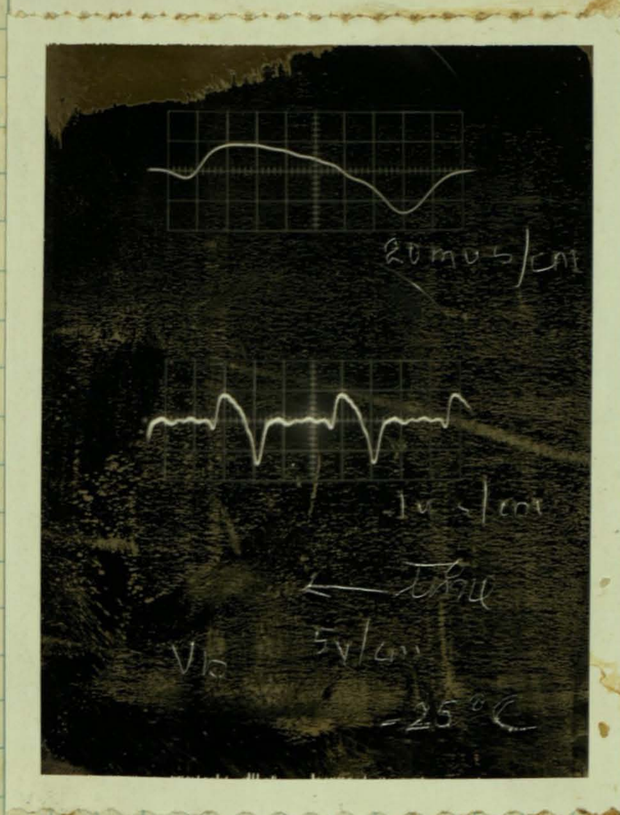
R [signature] 1/20/59

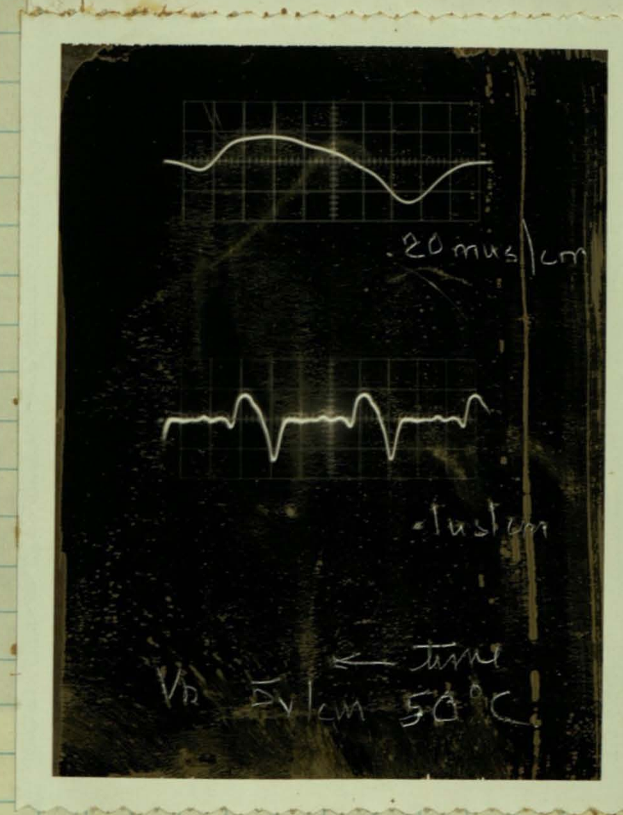
 1/21/59.

Ran a temperature test on the 5 mcs core transistor shift register circuit shown on page 112. The 4 stages were ring connected and placed in the oven. The current steering driver circuit was not ~~given~~ given the temperature test.

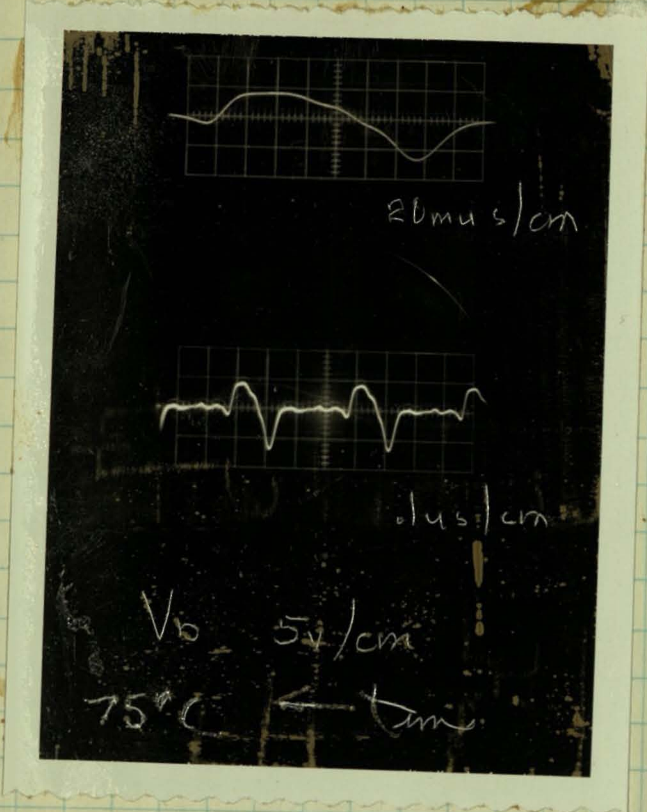


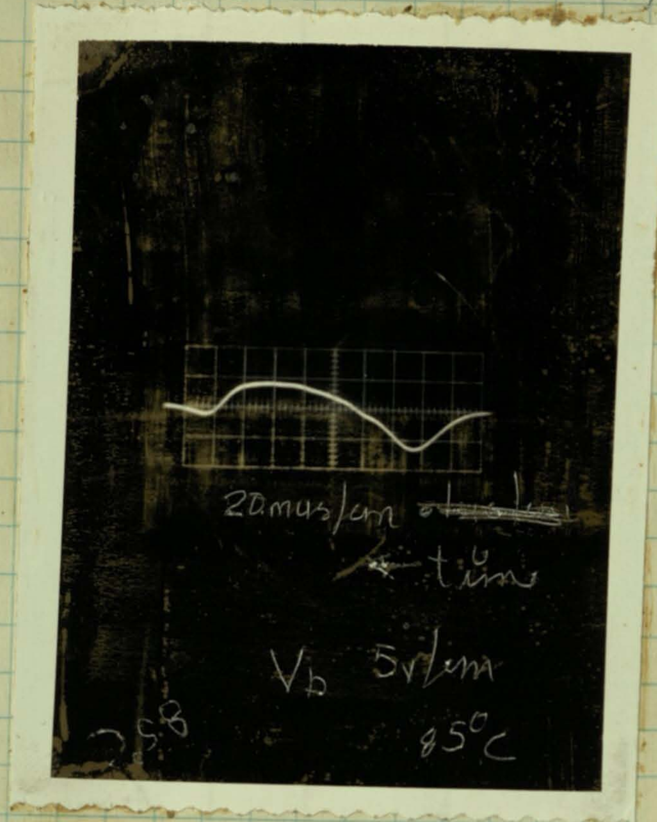






[illegible] 1/21/59



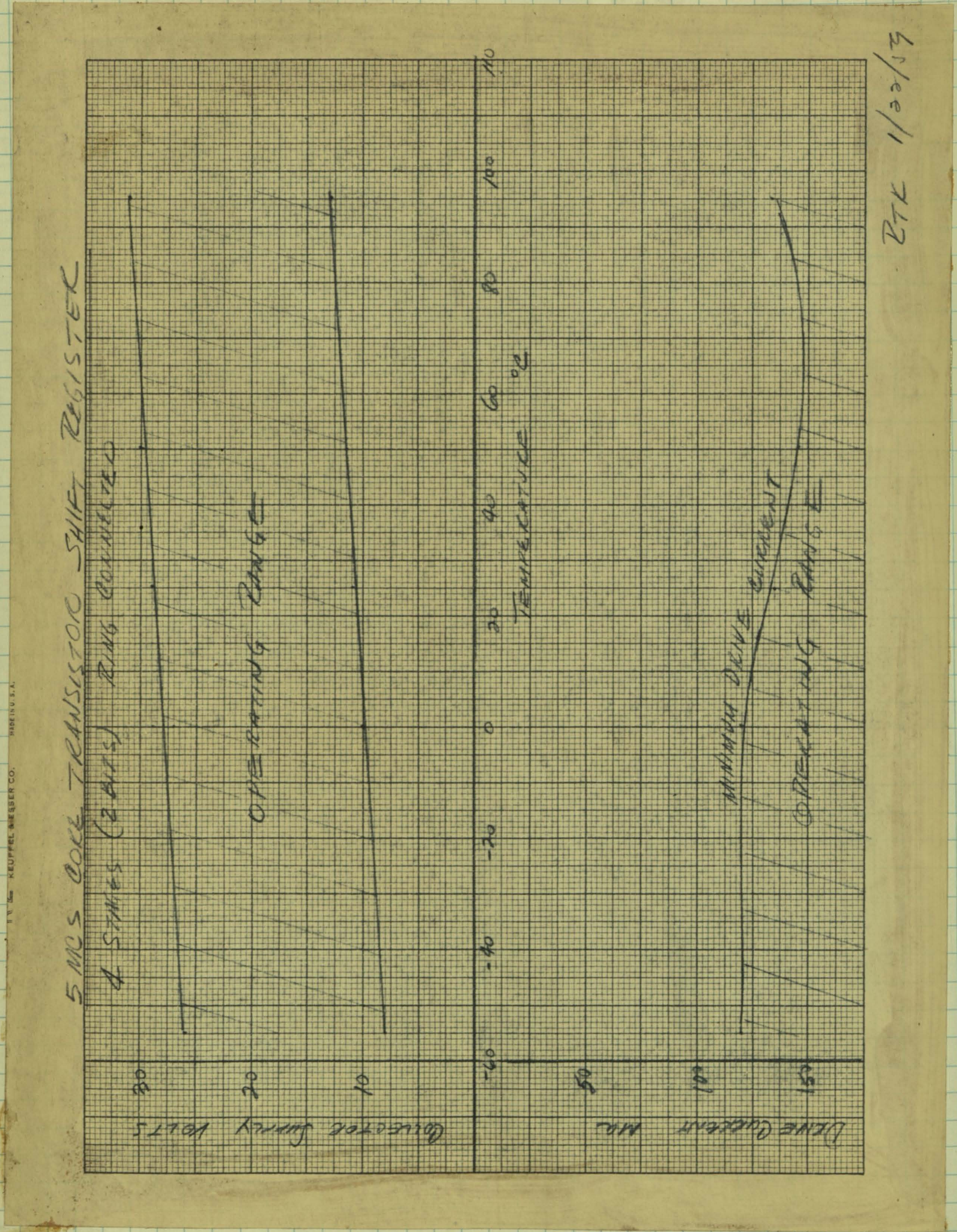


There was no apparent change in the operation over the temperature range − 55° to + 85° C

The operating range of the collector supply voltage and the drive current was determined for the temperature range − 55° C to + 95° C. The results of this test is shown on the following page. The operating range is wide and the circuit appears to be very stable throughout the range.

R C [illegible] 1/21/59

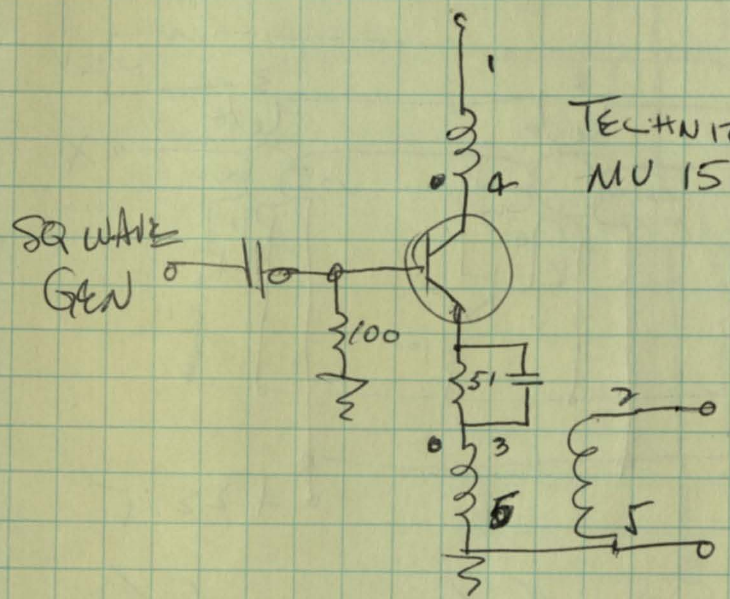
 1/22/59

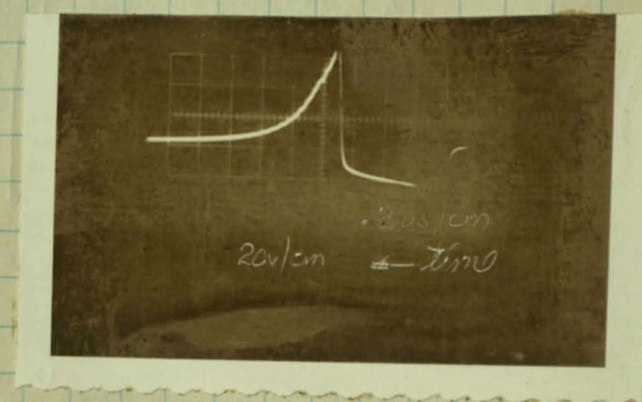

5 MCS CORE TRANSISTOR SHIFT REGISTER
4 STAGES (2 BITS) RING CONNECTED
OPERATING RANGE
TEMPERATURE °C
MINIMUM DRIVE CURRENT
OPERATING RANGE
COLLECTOR SUPPLY VOLTS
DRIVE CURRENT MA.
-60 -40 -20 0 20 40 60 80 100 120
30 20 10
50 100 150
RTK 1/22/59
KEUFFEL & ESSER CO. MADE IN U.S.A.

1/22/59

1/22/59

To get an idea of the performance of linear pulse transformers in a blocking oscillator circuit, the following circuit was breadboarded.





The best rise time was about 50 mμs. The output would not meet Bulova specs for rise time and droop.

Tried five AAB units in the square loop core blocking oscillator.

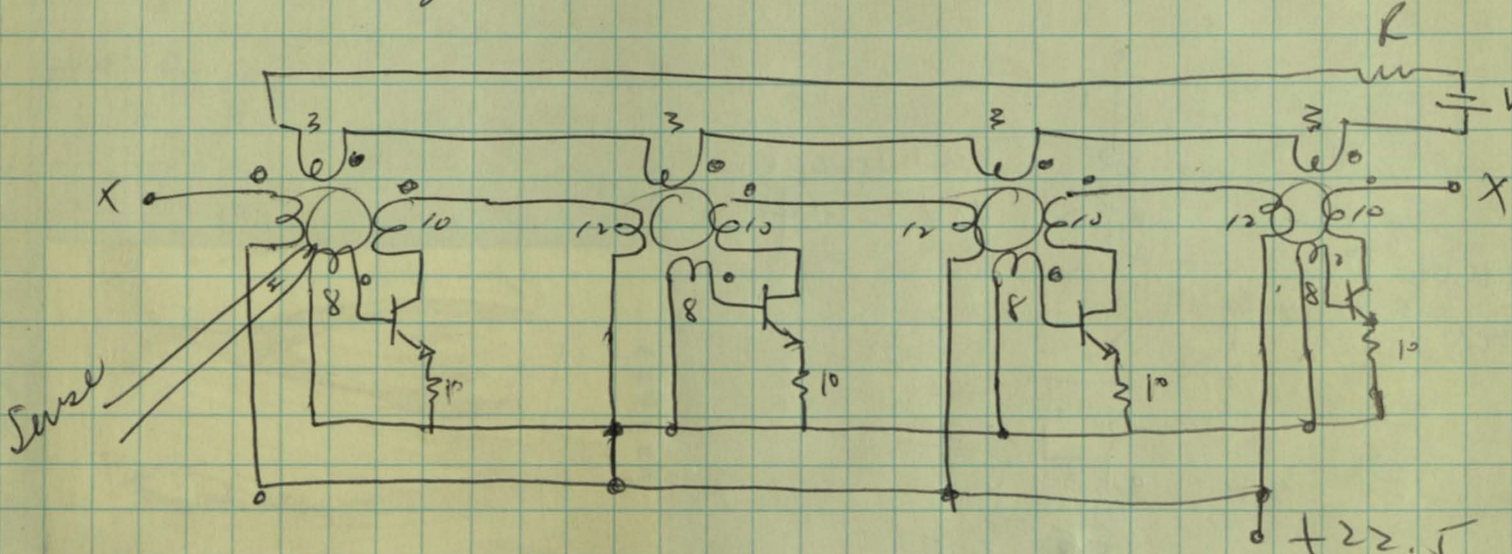
Sample	t_r
1	30 mμs
2	30
3	30
4	30
5	30

The ~~rise~~ time for ~~[illegible]~~ ranged from 30 - 35 mμs for a total of 25 units (AAB, ABB, ACB).

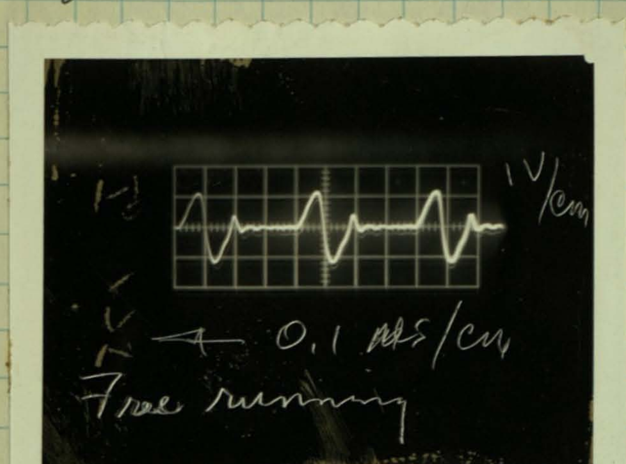
[signature] 1/22/59

1/23/59

By applying a D.C. Bias to the drive winding of the shift register, a Free running ring was developed.



A picture of the sense output was taken for a $I_0 = \frac{V}{R} = 175$ ma



The natural frequency is 5 mc.

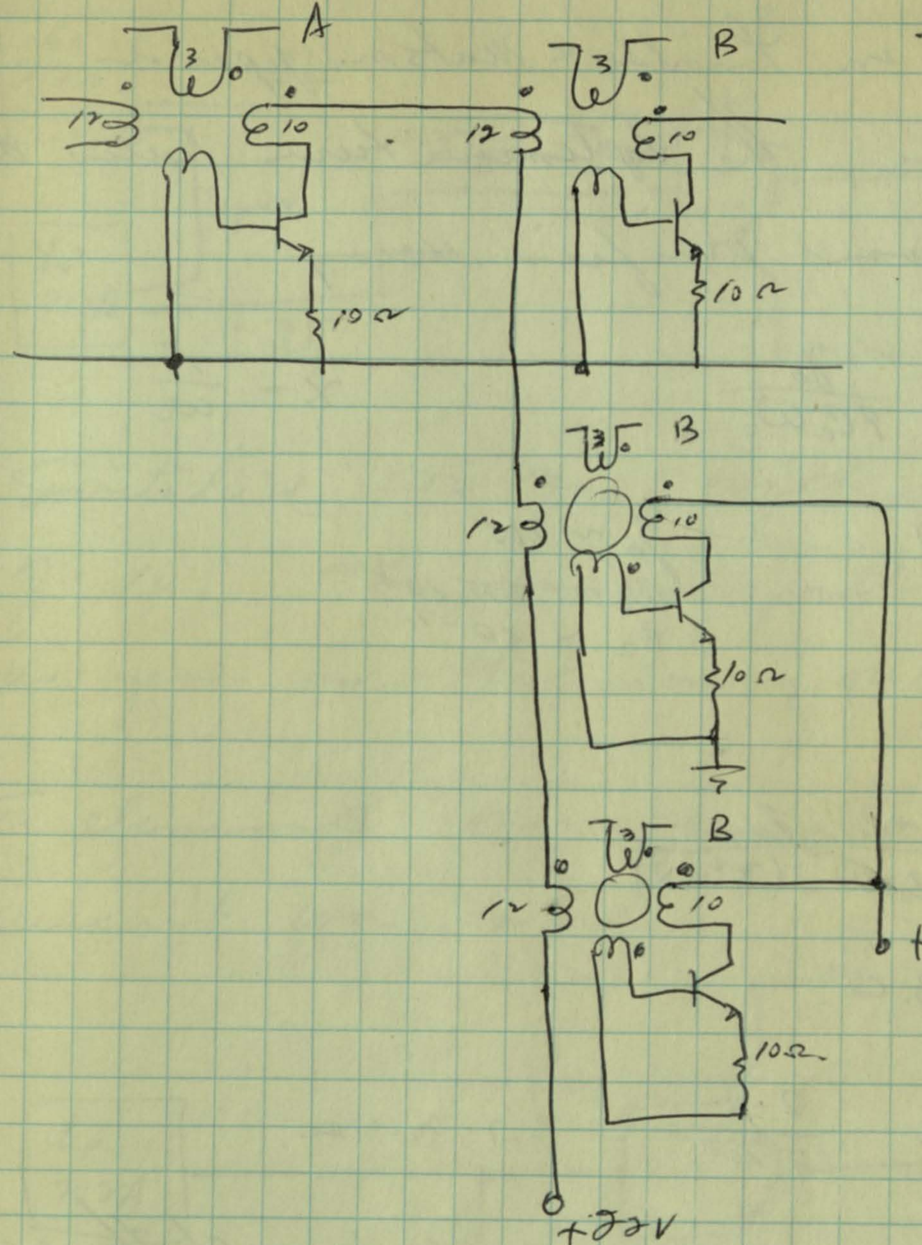
R T Kirchner 1/23/59

1/26/59 — 1/30/59

Tried branching out of the shift register as shown on next page.

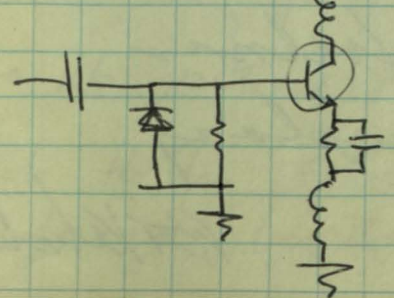
R T Kirchner

1/26/59 – 1/30/59



There was a lot of noise in the circuit on the ground bus and supply voltages. D Ferris revised the circuit. The circuit was unstable at 5 mc because of the increase in the transfer time caused by the two added windings in the collector circuit. Reducing the frequency slightly stabilized the operation.

Tried adding a diode to the base circuit of the blocking oscillator to see if it would improve the rise time. No improvement was noted.



R. [illegible]

1/26/59 — 1/30/59

Using the equations in Linvill & Mattson's paper on blocking oscillators, the ~~opt~~ optimum turns ratio determined experimentally was verified. ~~theory~~

$$x_m^3 + x_m^2 = \frac{g_b}{4C_c\omega_0} \qquad x = \frac{p}{\omega_0}$$

for the 2N697

$g_b \sim 0.05$
$\omega_0 \sim 2\pi\, 10^8$
$C_c \sim 10^{-11}$

$$x_m = 1$$

$$n = 1 + \frac{g_b}{2C_c\omega_0(x^2+x)}$$

$$n = 3.6.$$

$$t_r \approx \frac{2.3}{p_0} \approx \frac{2.3}{2\pi\, 10^8} = 3.7 \text{ m}\mu\text{sec.}$$

The results are in good agreement with the exception of the rise time. The calculated rise time is much lower than that obtained experimentally by a factor of 10.

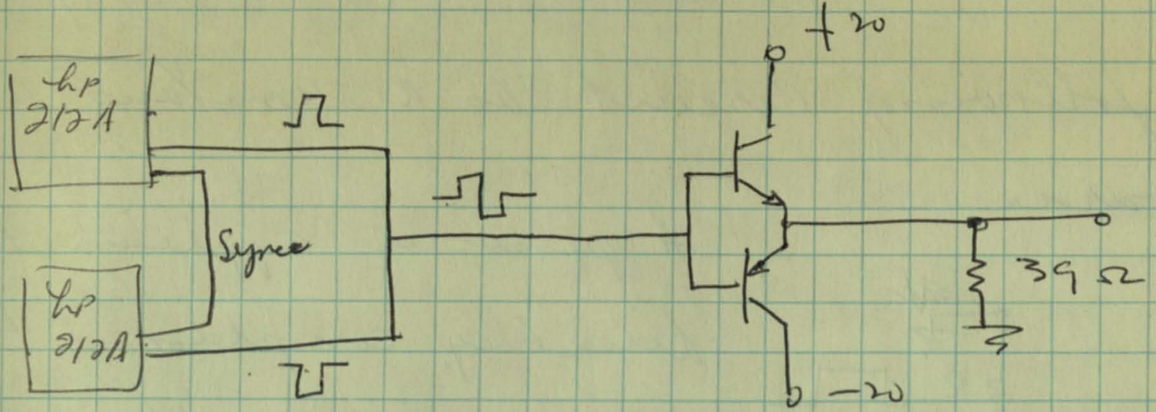
R T [signature]
1/30/59

2/3/59

Tried a complementary emitter follower circuit for the IRE Show display.

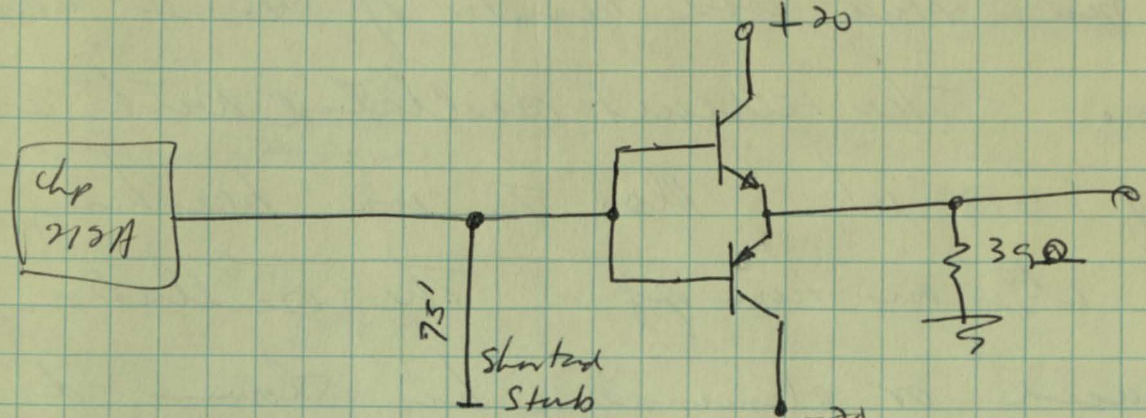
R T [signature] 2/3/59

2/3/59 Cont



Switched 500 ma with a current gain of 10. The rise and fall time were about as good as that coming out of the 212 A's

To eliminate one generator the following circuit was tried



The reflected signal was fairly good. Will continue work on this circuit.

R T [signature]
2/3/59

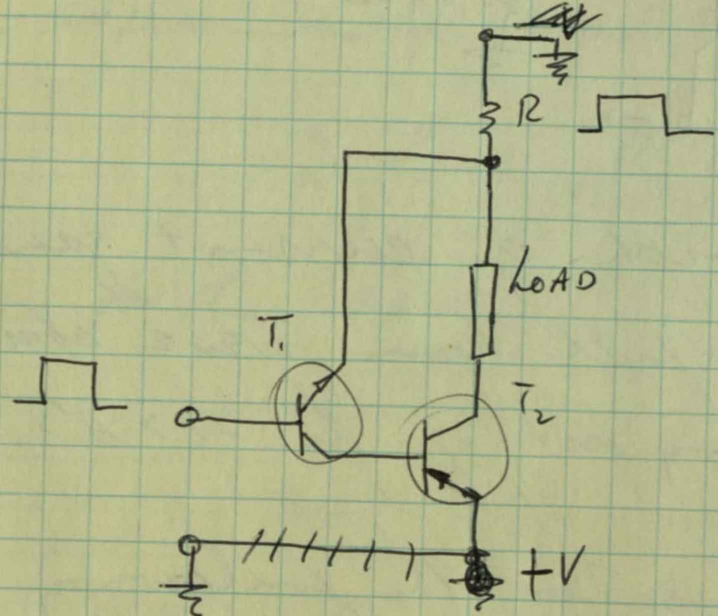
2/9/59

Since the generator end is not matched (especially in the zero db position) signals were being reflected from the stub to the generator and back to the load. This was reduced by adding a series resistor in the generator end

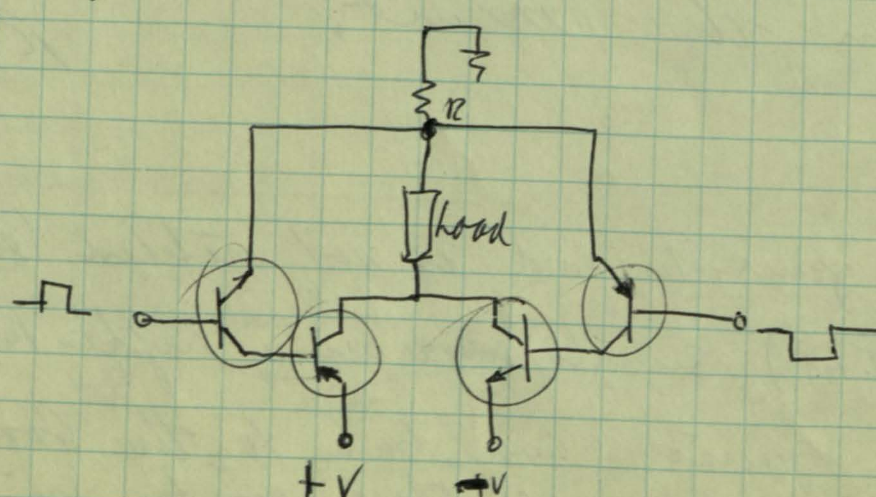
R T [signature] 2/9/59

2/5/59 - 2/6/59

Tried the following circuit as a constant current pulse source -



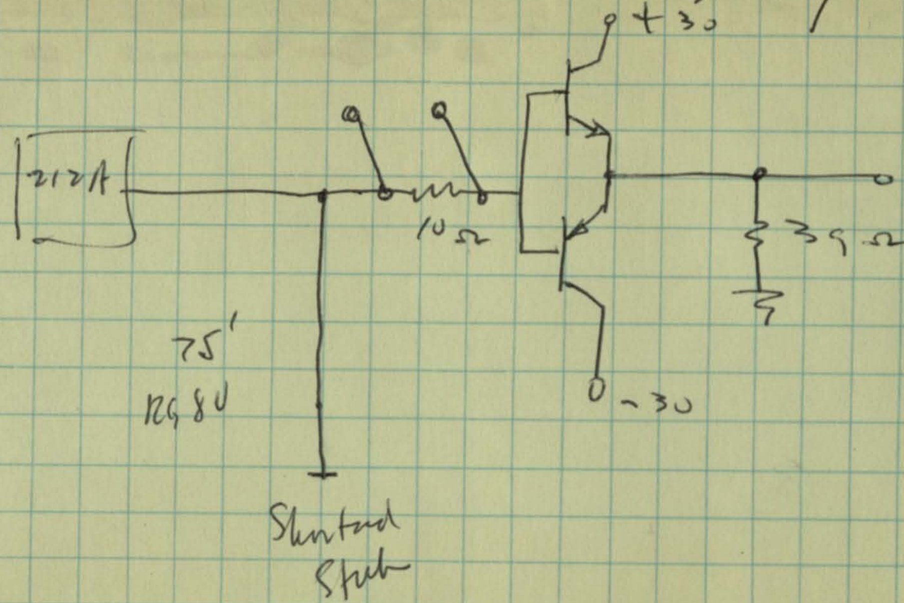
A pulse is applied to T_1, directly coupled to T_2. Current flows thru the load and the feedback resistor, R. The emitter of T_1 is returned to the resistor R ~~but~~ resulting in negative current feedback. The circuit regulated pulses of 500 ma thru load resistor of 90 Ω changed to 0 ohms. The circuit oscillated with an inductive load of 6.2 μh. Also T_2 was breaking down from the $L\frac{di}{dt}$ on turn off - The oscillations can be reduced or eliminated by slowing down the circuit response. The circuit can also be operated in push-pull.



R T Kiboshkin 2/6/59

2/23/59

Worked on the I.R.E. Show Display.



One of the 53/54 G plug in unit for the scope was found to pass slivers on A-B (with A = B) with fast (20 mus rise time) pulse. Another unit was tried and gave better results (still without complete cancellation. Some adjustment in the plug-in might help.

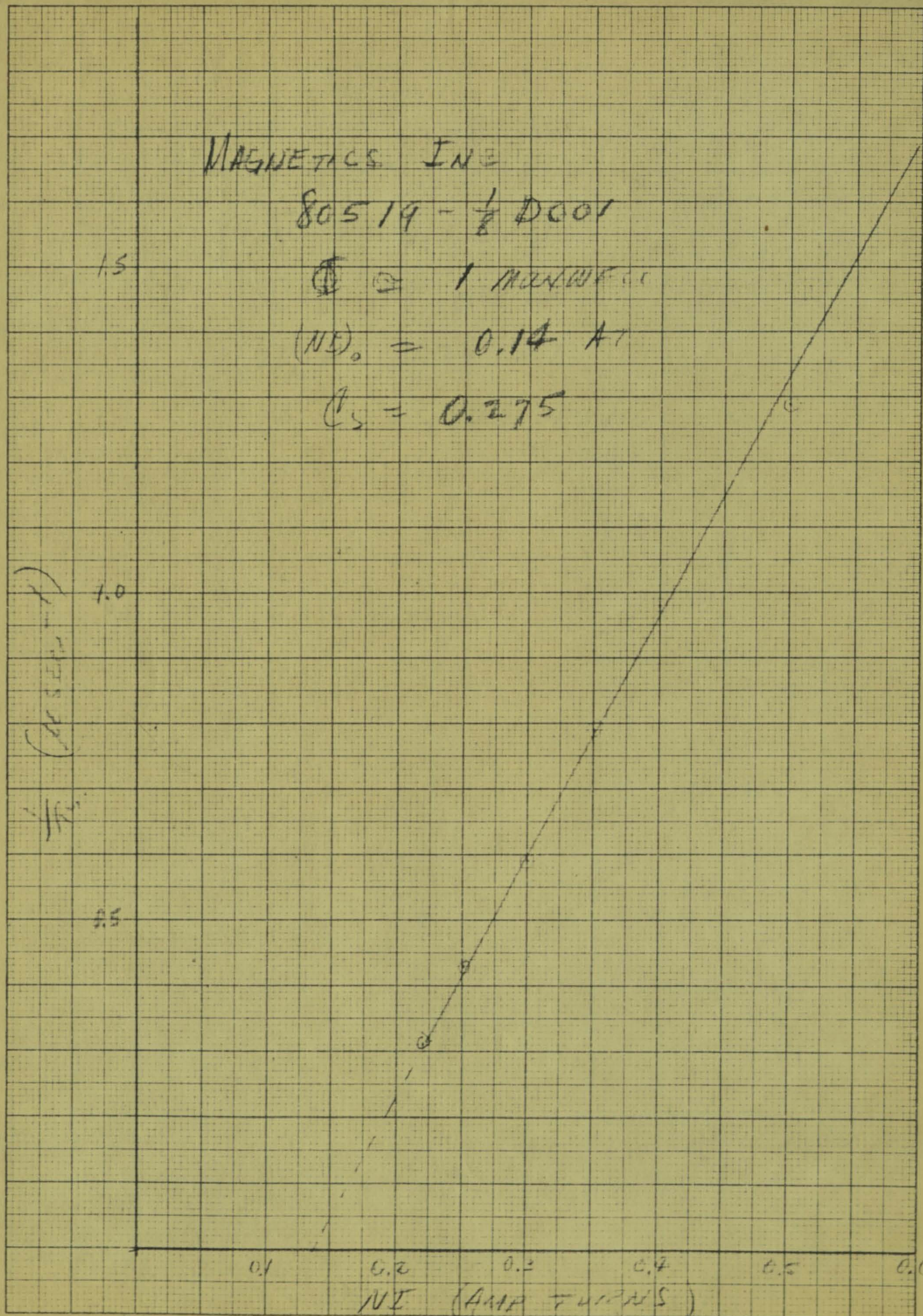
[signature] 2/23/59.

2/24/59

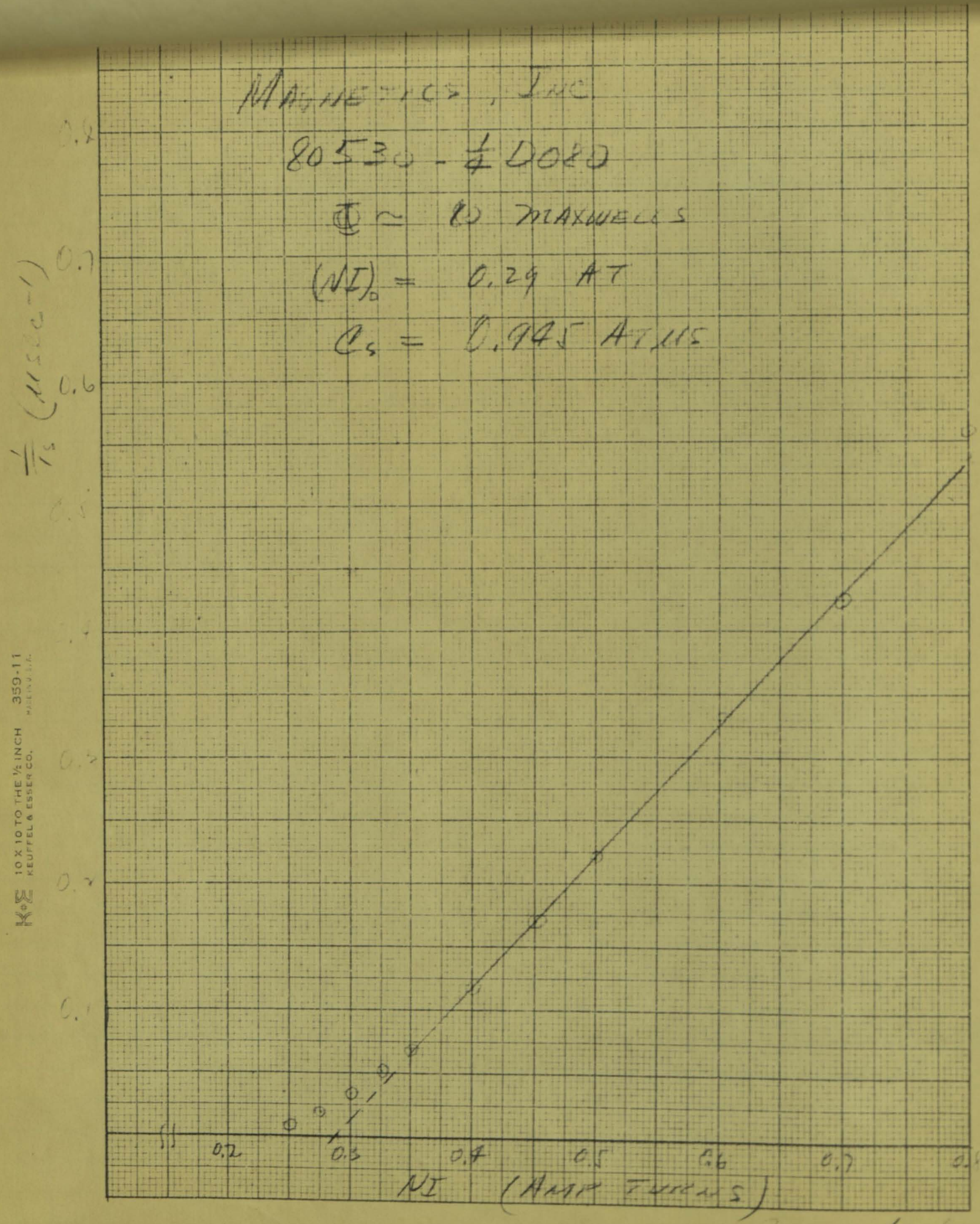
Tried a different 53/54 G plug in unit. Cancellation was much better. Adjusting tools have been ordered for the coil slugs in the plug in

[signature] 2/24/59

 2/26/59


MAGNETICS INC
80519 - 1/8 D001
(NI)₀ = 0.14 AT
= 0.275
1.5
1.0
0.5
0.1
0.2
0.3
0.4
0.5
NI (AMP TURNS)

2/26/59


Magnetics, Inc
80530 - 1/4 D080
Φ ≈ 10 maxwells
(NI)₀ = 0.29 AT
Cs = 0.945 AT μs
1/τs (μsec⁻¹)
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
NI (Amp Turns)

RTK 2/26/59

2/26/59

D. Ferris took switching curves of the bobbin cores received from Magnetics.

[signature]

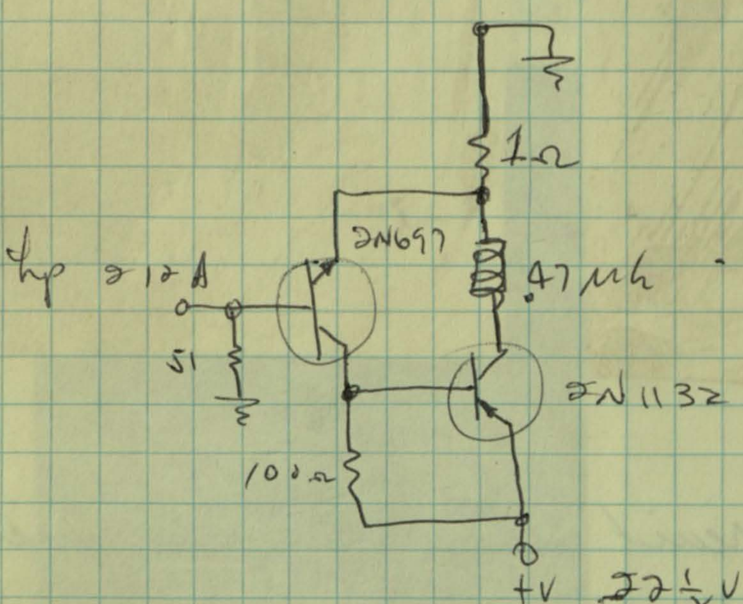
3/3/59

Attended WJCC in San Francisco.

[signature]
3/3/59

3/11/59

Tried the constant current circuit again (page 126).



Switched 500 ma thru the .47 uh choke with a rise time of 0.15 μs.

$L\frac{di}{dt}$ peaks were ± ~18 volts.

The current was well regulated as was previously observed. Will continue work on the circuit.

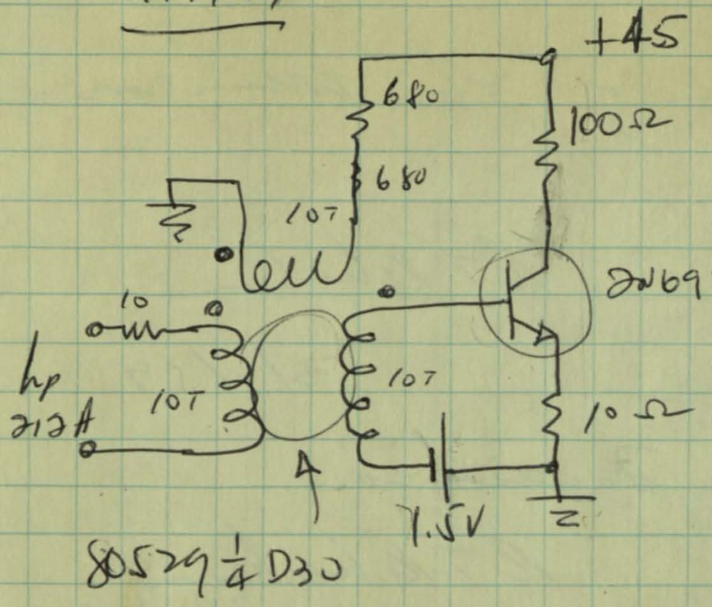
[signature]
3/11/59.

3/17/59

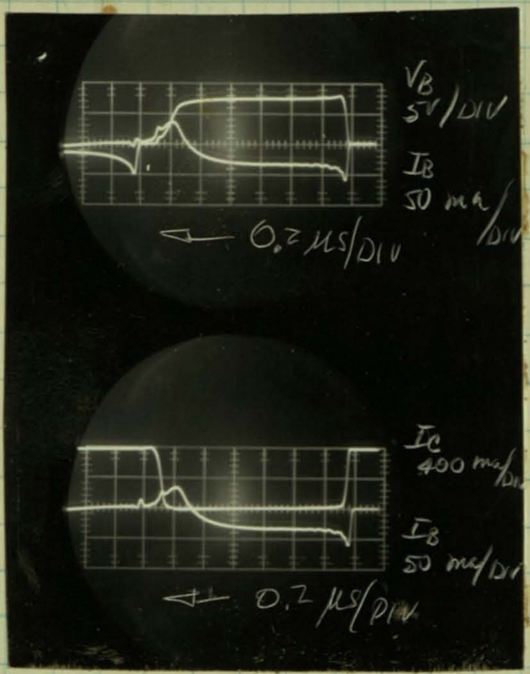
Tried a core-driven saturated circuit as a core driver. The circuit is as shown on the next page

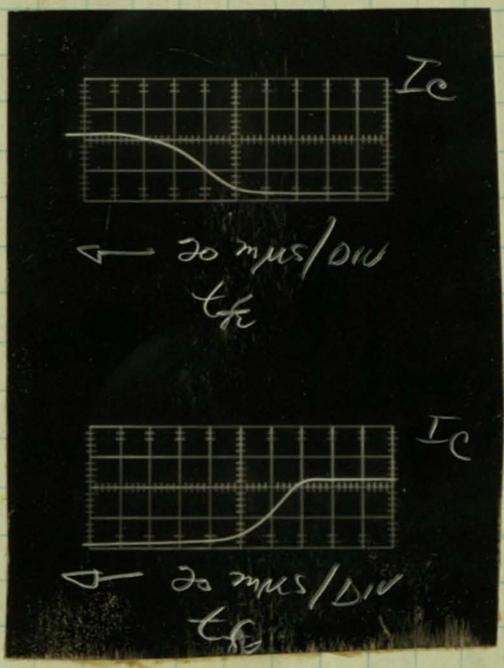
[signature] 3/17/59

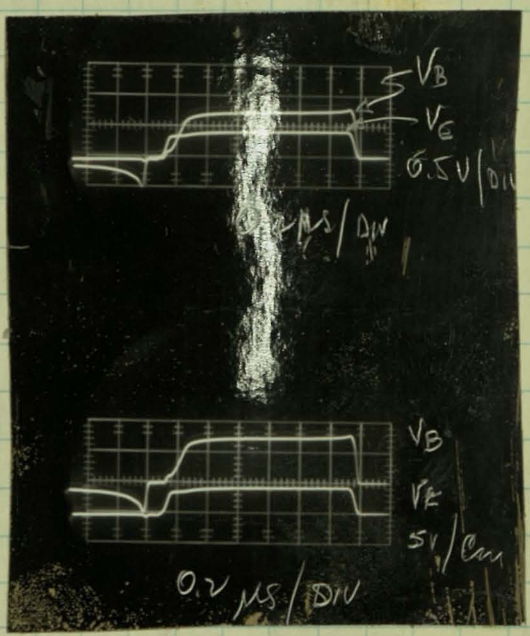
3/17/59



The core was allowed to saturate. Pictures were taken of the currents and voltages in the circuit







The main disadvantage to the circuit is the change in width with Transistor β. The width increased by 0.2 µsec when the transistor was changed from a β of 50 to a β = 150. The fall time was greatly reduced when the core was not allowed to saturate. This may be a possible improvement on the speed of the circuit

[signature] 3/17/59

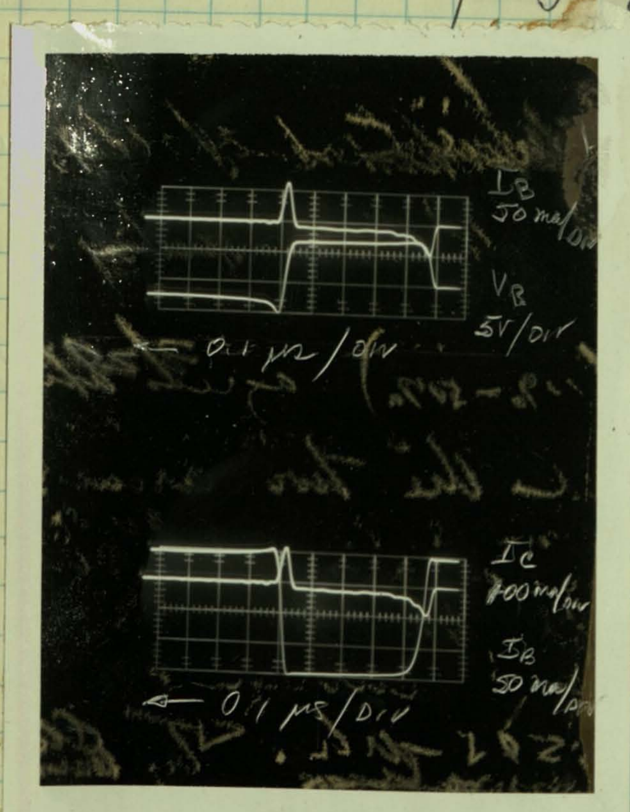
3/~~20~~ 18/59

Found an error in the rough draft of the shift register report in the calculation of the input turns. The error was corrected by calculating the input turns for minimum switching time rather than for a specified switching time.

R. T. Kihankanian
3/18/59

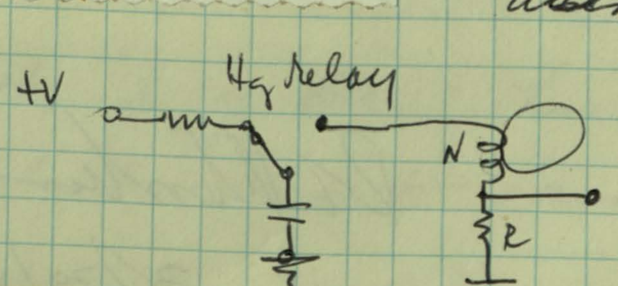
3/20/59

Took pictures of the driver circuit shown on the preceding page with the core unsaturated.



The transistor is just in saturation. The fall time has been reduced to about 30 mμs.

The dead core inductance of a Telemeter Magnetics 50-T1 core was measured using the following circuit.



A step of voltage was applied and the rise time of the current was measured

R. Kihankanian 3/20/59

3/20/59

The rise time was measured for $V = 5$ volts, $R = 10\ \Omega$ and $N = 10$ turns.

$$t_r = 122\ m\mu s$$

$$t_{(10\% - 50\%)} = 32\ m\mu s.$$

Using $t_r \simeq 2.2 \frac{L}{R}$

$$L = \frac{(.122 \times 10^{-6})(10)}{2.2} \simeq 0.55\ \mu h$$

$$\frac{L}{N^2} \simeq 5.5\ m\mu h / turn^2$$

Taking $V = 1$ volt, $t_r \simeq 130\ m\mu s$ which agrees with the above.

Also the mid point check $(t_{10\% - 50\%})$ agrees with the 10 - 90 % point

$$L = \frac{R\, \Delta t(10\% - 50\%)}{0.588}$$

$$= \frac{(10)(32)}{0.588} \simeq \underline{0.545\ \mu h.} \leftarrow \text{Ok}$$

R. T. [signature]

3/20/59

3/20/59

Also made a rough calculation of the flux capacity of a 50 T# core. From the curve on page 18, for a read and write mmf of 0.5 amp turns, the peak output volts/turn is 70 mv/turn and the switching time is 0.85 μs. Assuming the output to be sinusoidal,

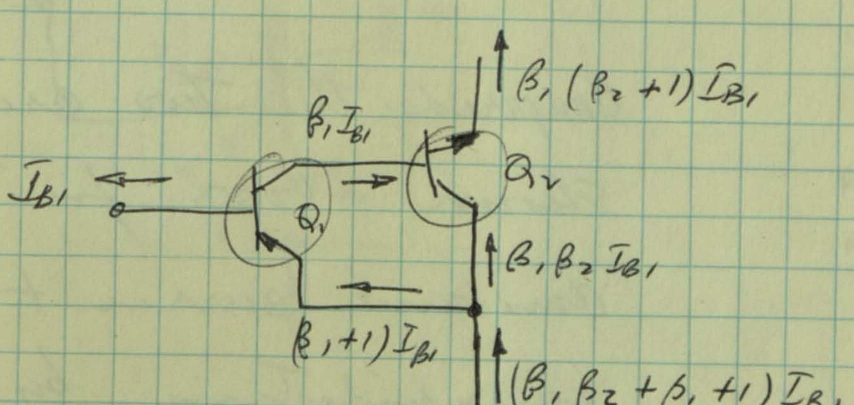
$$\Phi = 2\Phi_N \simeq (70 \times 10^{-3})(.85 \times 10^{-6})\left(\frac{2}{\pi}\right)$$

$$\simeq 3.8 \times 10^{-8} \text{ volt sec/turn}$$

R T Kikoshima 3/20/59

3/23/59

Continued work on the PNP-NPN compound constant current driver.

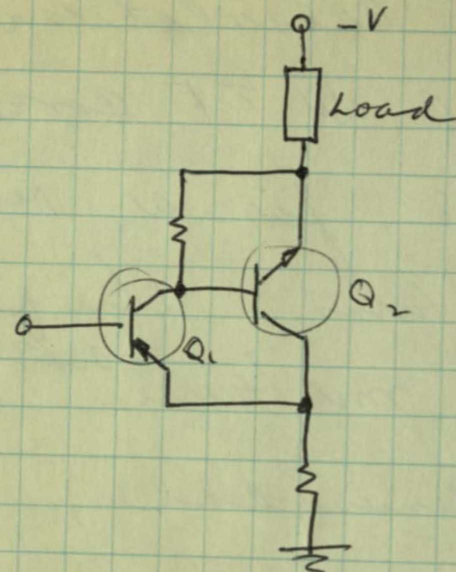


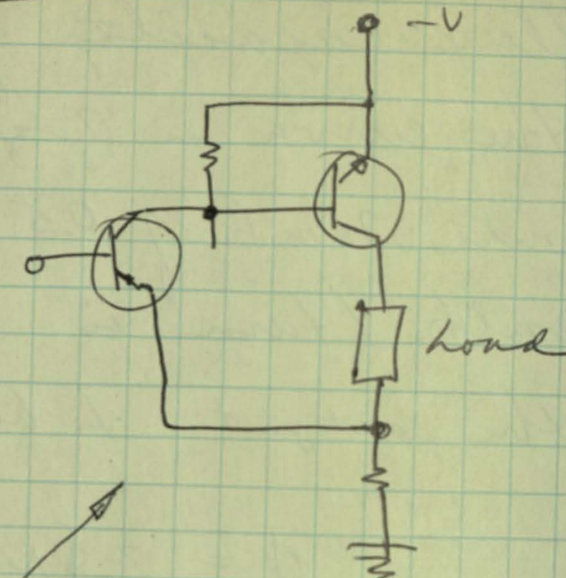
G. F. Abbott, Jr of B.T.L. has applied this circuit to constant current and constant voltage drivers.

R T Kikoshima 3/23/59

3/23/59

Hatts constant current circuit is as follows.

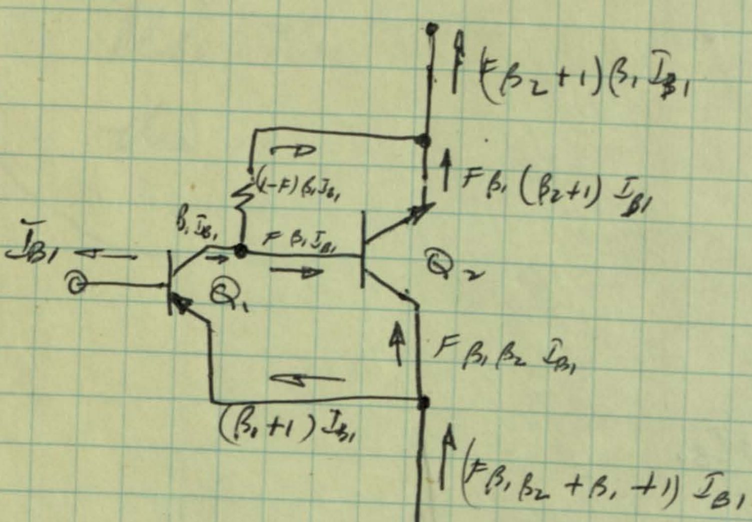




the constant current driver shown on p 126 and p 129 is as shown.

Will make a comparison of these circuits

[illegible] 3/23/59

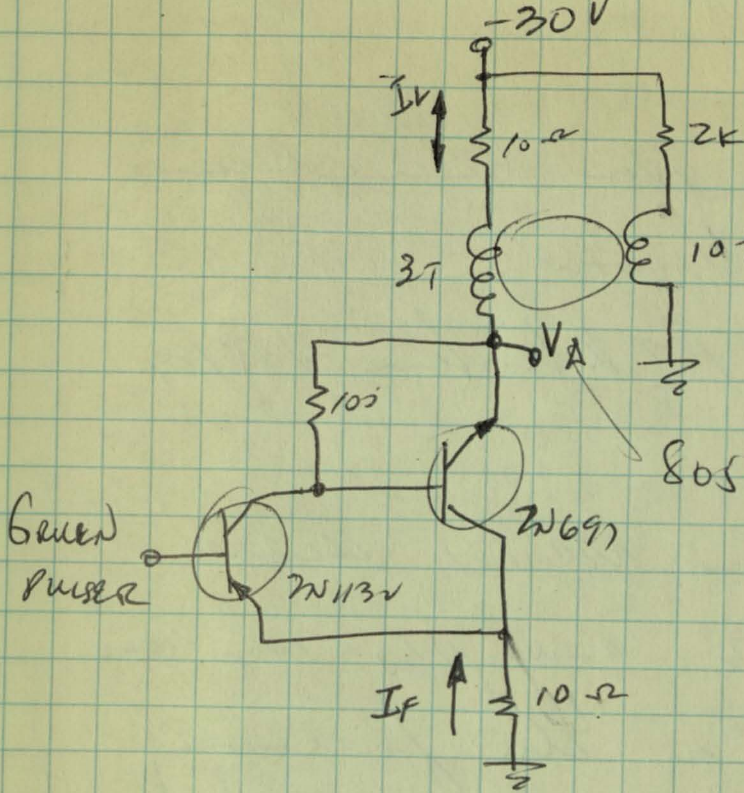


3/24/59

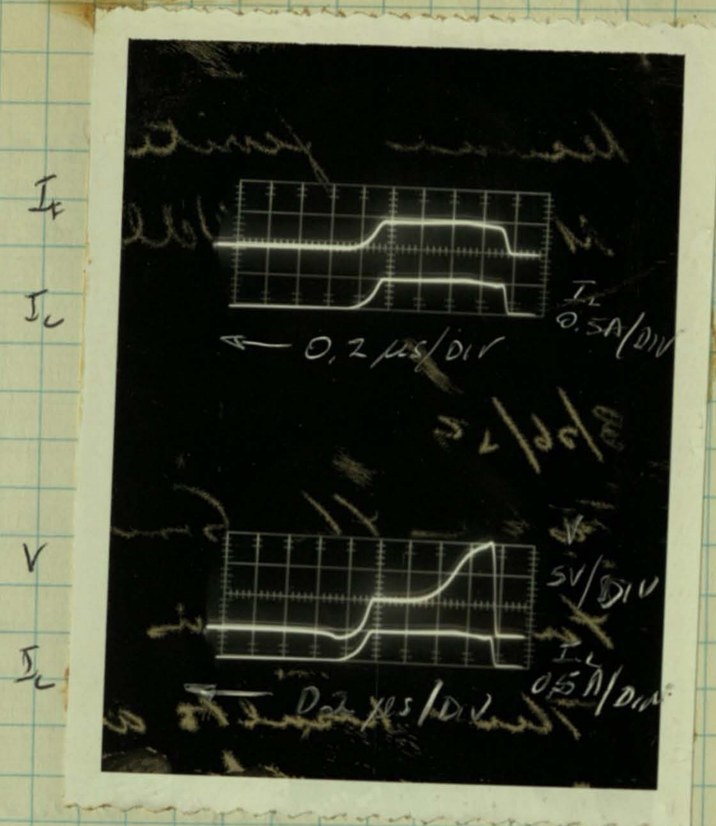
Compared the two circuits shown above for their constant current capabilities by using a Square loop core for a load.

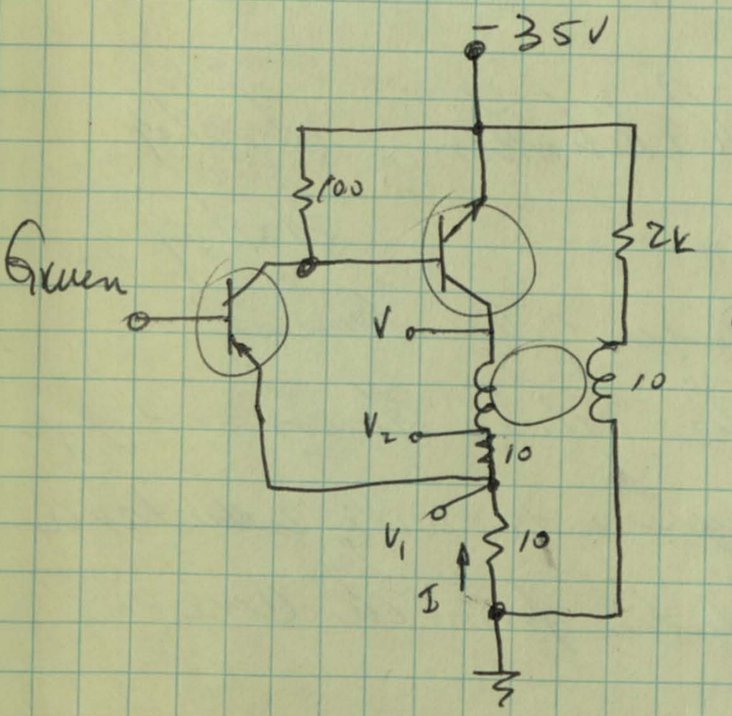
[illegible] 3/24/59

3/24/59

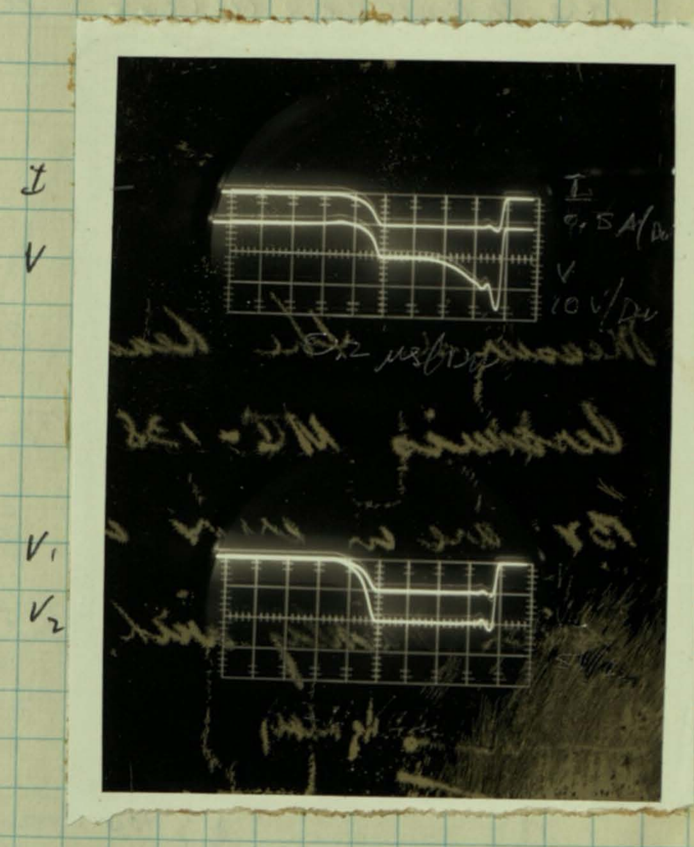


80524 ¼ D30





80524 ¼ D20



The second circuit appears to have slightly better constant current characteristics

[illegible signature] 3/24/59

3/25/59

Received ferrite memory cores from General Ceramics MC 138. Will test them tomorrow.

R T Kibrashian 3/25/59

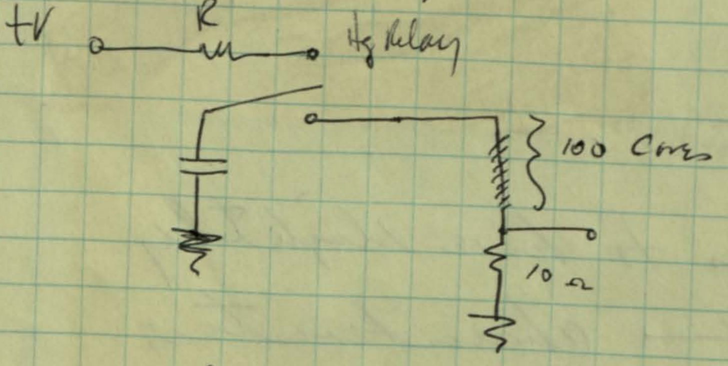
3/26/59

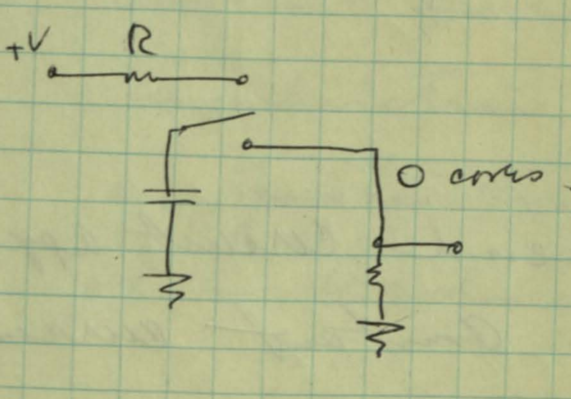
Tested the General Ceramics MC 138 under two conditions: $NI_W = NI_R$ and NI_W = 1 amp turn. The results are plotted on the following page. These results are in agreement with the manufacturers data sheet.

R T Kibrashian 3/26/59

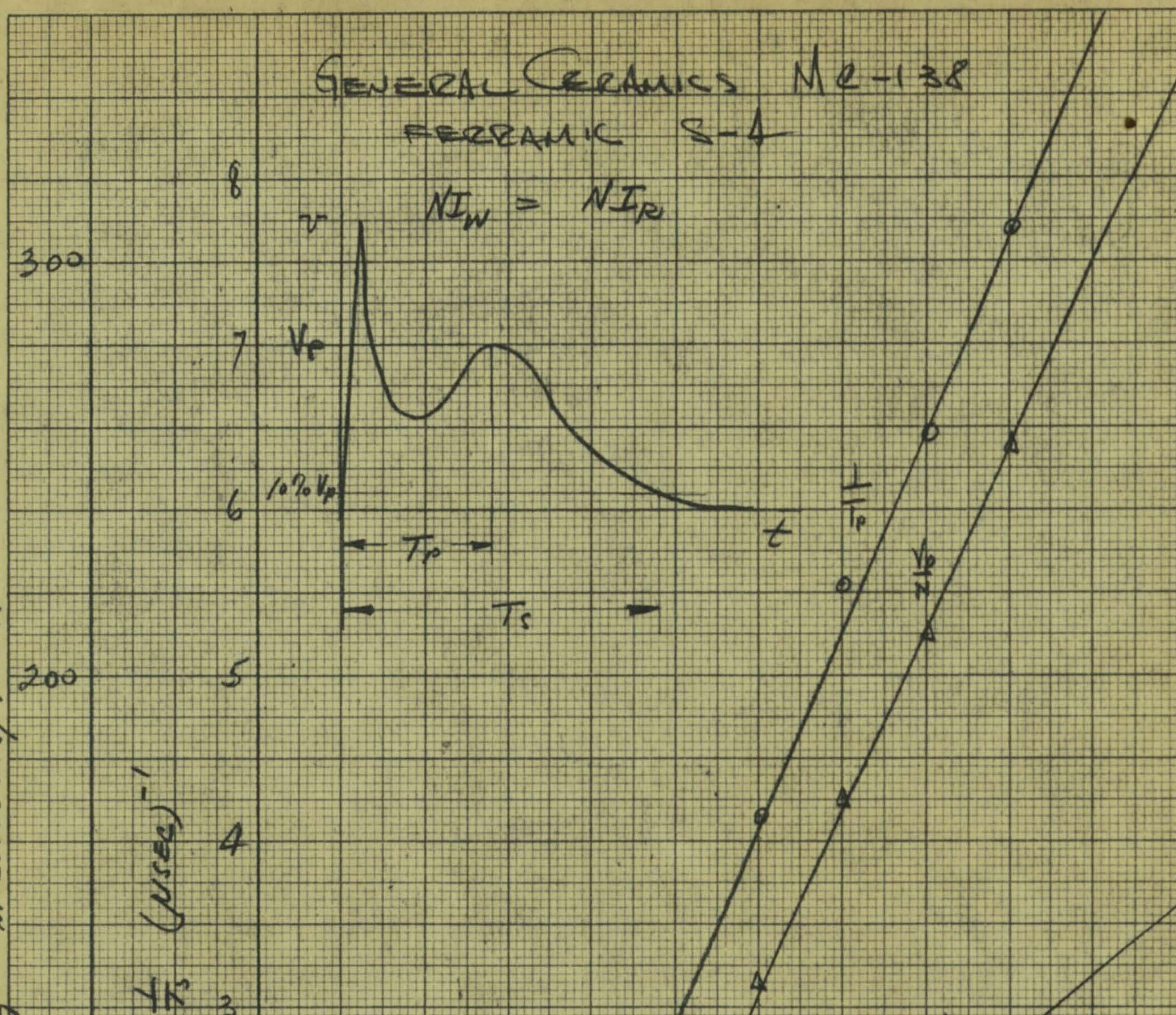
3/31/59

Measured the dead core inductance of the General Ceramics MC-138 cores. The values shown on page 132 are in error in that it represents wire inductance ~~with~~ mainly with little contribution from the core,

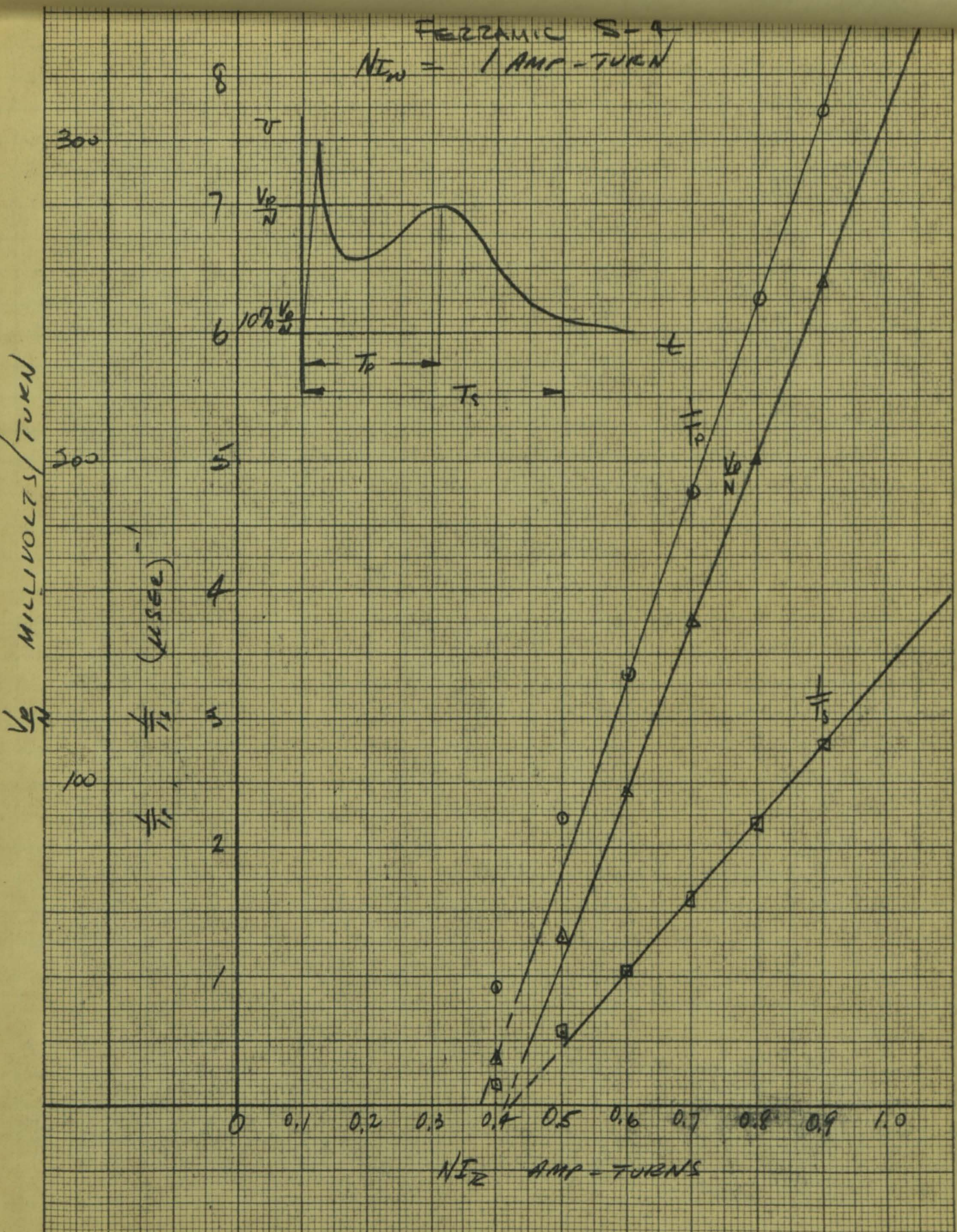




The rise time of the current was measured for 100 cores and 0 cores.


GENERAL CERAMICS MC-138
FERRAMIC S-4
NI_W = NI_R
v
V_P
10% V_P
t
T_P
T_S
1/T_P
V_P/N
1/T_S
V_P/N MILLIVOLTS/TURN
1/T_S, 1/T_P (μSEC)^-1
300
200
100
8
7
6
5
4
3
2
1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
NI_R AMP-TURNS

RTK 3/26/59


FERRAMIC S-4
NIw = 1 AMP-TURN
MILLIVOLTS/TURN
(μSEC)-1
NIR AMP-TURNS
1/Tp
Vp/N
1/Ts
10% Vp/N
Tp
Ts
t
v
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0
1 2 3 4 5 6 7 8
100 200 300

RTK 3/26/59

3/31/59

		250 ma	500 ma
t_r	100 cores	120 mμs	120 mμs
t_r	no cores	100 mμs	100 mμs.

$$2.2\frac{L}{R} = t_r$$

L_1 (100 cores) $= \frac{1.2}{2.2} = 0.545$ μhenries

$L_2 = \frac{1.}{2.2} = 0.455$ μhenries

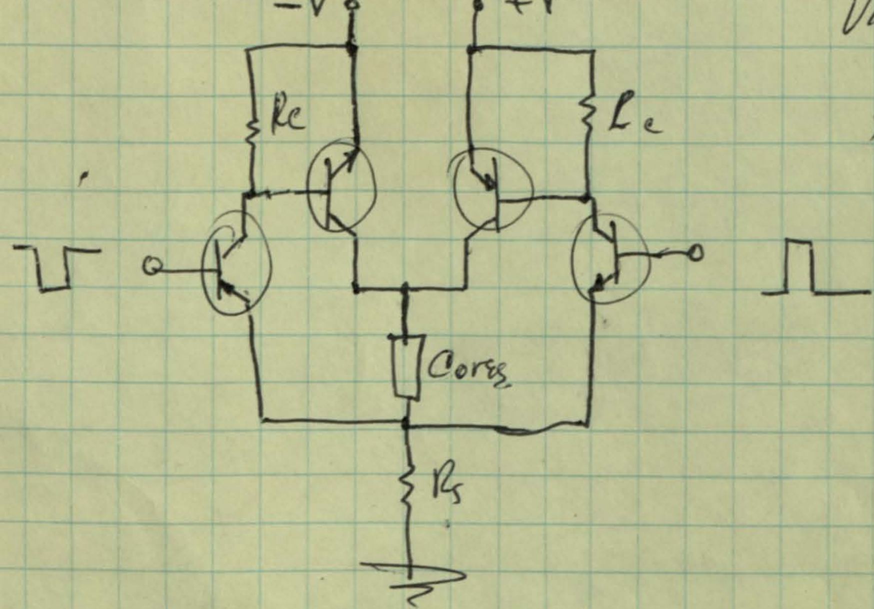
$L_1 - L_2 = .090$ μhenries / 100 cores

L_c = 0.9 mμh / core.

R T Kukutman 3/31/59

4/2/59

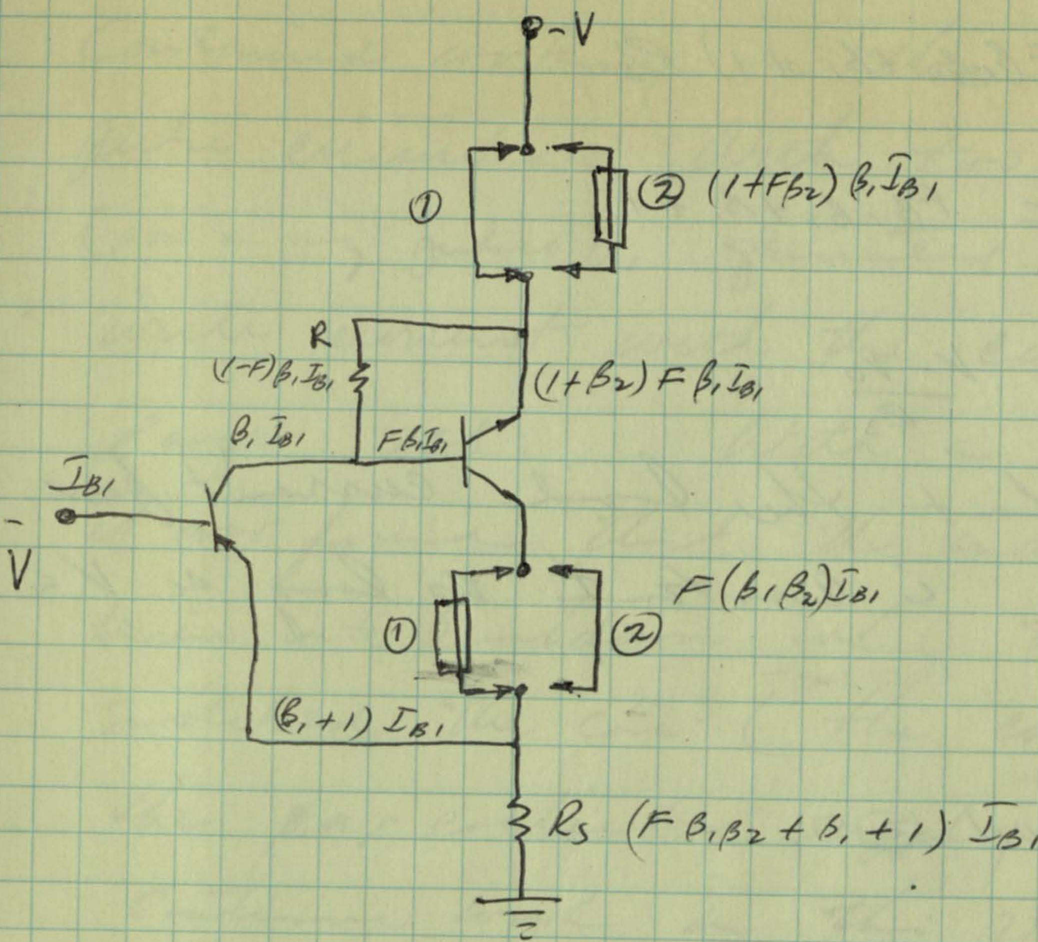
Will build a bidirectional core memory driver as shown on Page 126



VH Grinich suggested reducing the size of the Rc (now using 100 Ωs) to give better fall time

R T Kukutman 4/2/59

4/3/59



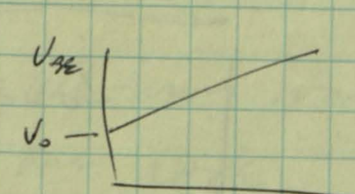
Considered the load in two positions shown above.

For position ①:

$$V_{BE_1} = V - (F\beta_1\beta_2 + 1) I_{B_1} R_s$$

$$= V - \left(\frac{F\beta_1\beta_2 + \beta_1 + 1}{F\beta_1\beta_2}\right) I_L R_s \quad \text{where } I_L = F\beta_1\beta_2 I_{B_1} \quad [1]$$

Assume that



$$V_{BE_1} = m I_{C_1} + V_0$$

$$V_{BE_1} = \frac{m I_L}{F\beta_2} + V_0$$

$$= \frac{m\beta_1 I_L}{F\beta_1\beta_2} + V_0 \quad \text{-------} \quad [2]$$

Equating [1] and [2] and solving for I_L

$$I_L = \frac{F\beta_1\beta_2(V - V_0)}{m\beta_1 + (F\beta_1\beta_2 + \beta_1 + 1)R_s} \quad \text{----} \quad [3]$$

4/3/57

If $m\beta_1 << (F\beta_1\beta_2 + \beta_1 + 1) R_s$

and $F\beta_1\beta_2 \simeq F\beta_1\beta_2 + \beta_1 + 1$

Then

$$I_L \simeq \frac{V - V_0}{R_s}$$

which shows that the load current for connection ① is constant as long as V is constant.

For LOAD IN POSITION ② :

$$V_{BE} = V - (F\beta_1\beta_2 + \beta_1 + 1) I_{B1} R_s$$

$$= V - \frac{F\beta_1\beta_2 + \beta_1 + 1}{F\beta_1\beta_2 + \beta_1} I_L' R_s \simeq V - R_s I_L' \quad [1]$$

$$\text{where } I_L' = (F\beta_1\beta_2 + \beta_1) I_{B1}$$

Again assume $V_{BE} = m\beta_1 I_{B1} + V_0$ [2]

Combining [1] and [2] and solving for I_L'

$$\boxed{I_L' = \frac{V - V_0 - m\beta_1 I_{B1}}{R_s}} \quad [3]$$

Since the load current is dependendant on I_{B1} it is not constant. This agrees with the experimentally observed results.

R T Rikenbaum 4/3/57

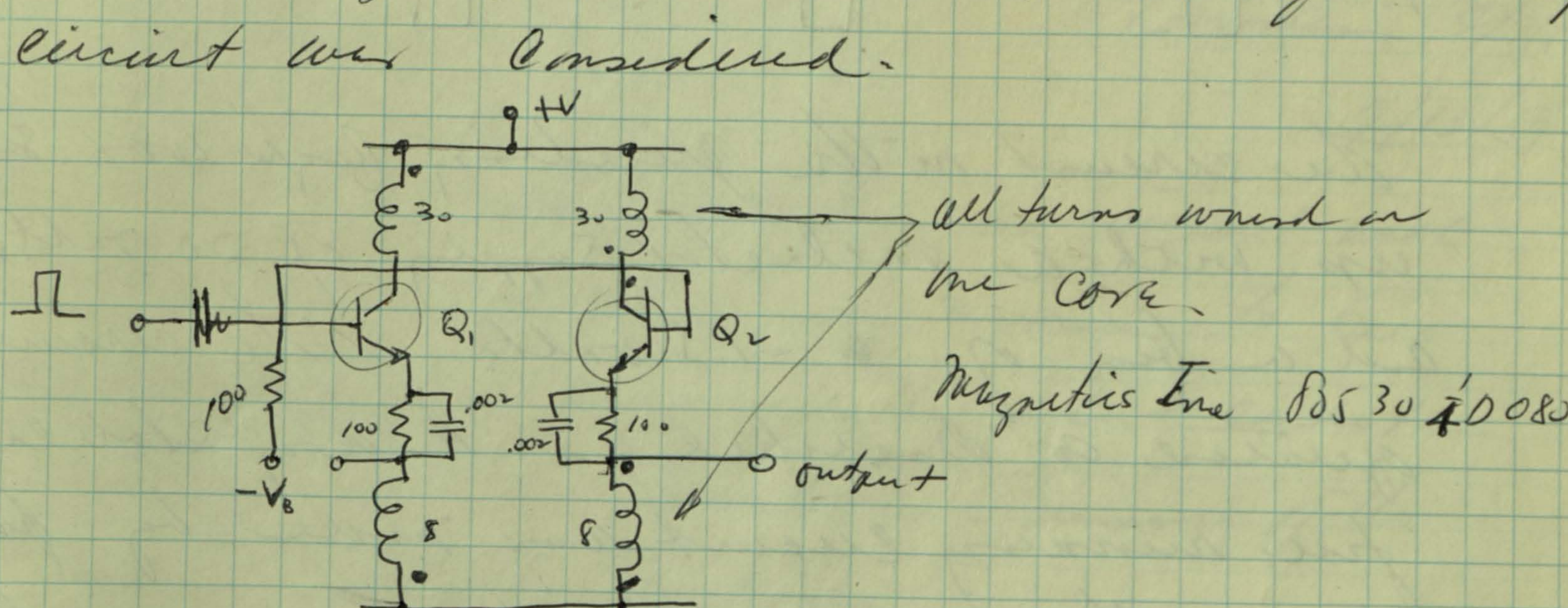
4/7/59

Continued working on the constant current pulse circuit. With two pulse generators (pos + neg pulses), generated a read and write current with the circuit as shown on page 138. With a core in a load it was found that the inactive PNP was driven into breakdown when the active one switched the core (the core voltage adds to the pnp collector supply voltage. Will continue work on this problem.

R. T. Kikushima 4/7/59

4/8/59

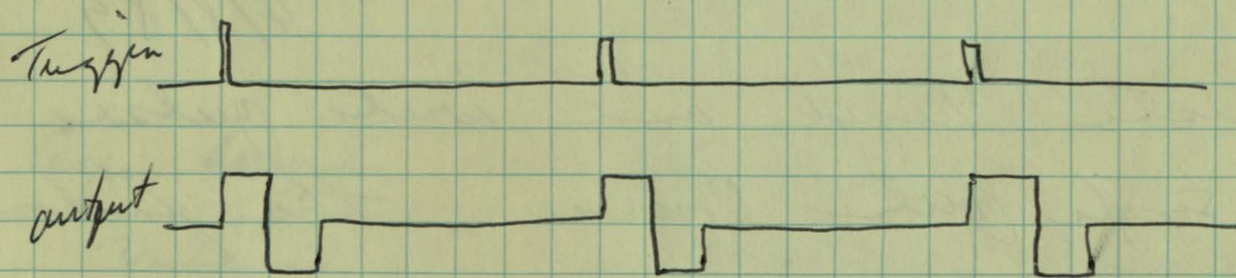
To generate read and write pulses from a single pulse source, the following circuit was considered.



R T Kikushima 4/8/59

4/8/59

~~The~~ If both transistors are identical, (also, if all the external components are identical), then pulse applied to the bases of the transistors will have no effect. However, if there is any unbalance, the current will be greater in one side and the core will be driven into saturation. When the trigger input pulse is removed, the ~~xxx~~ the voltage on the windings caused by the ~~flux~~ change from saturation to remanence is of the polarity to trigger the other side of the circuit.



The circuit on the preceding page was set up with a collector supply of 20 volts and a bias of -1.5 volts. The circuit operated as described. A very stable free running circuit was made by forward biasing the bases. The frequency is dependent on the supply voltage and the flux capacity of the core, that is 4/8/59

$$\frac{T}{2} \approx \frac{2N\Phi_r}{V}$$

where T = period

N = number of collector turns.

Φ_r = remanence flux

V = collector supply volts.

R T Vikashanian 4/8/59

4/9/59

Discussed Coincident current and linear selection core memories with V H Grinich. It was decided to start work on the linear selection memory drive circuits with I. Haas.

R T Vikashanian 4/9/59

4/13/59

After discussing the IBM Kingston circuit with V Grinich a phone call was made to Geo Center to find out exactly what conditions they were concerned about. Summary of the call is on the next page.

R T Vikashanian 4/13/59

PHONE CALL TO GEO CANTAC [illegible] ON 4/13/59

CONDITION:

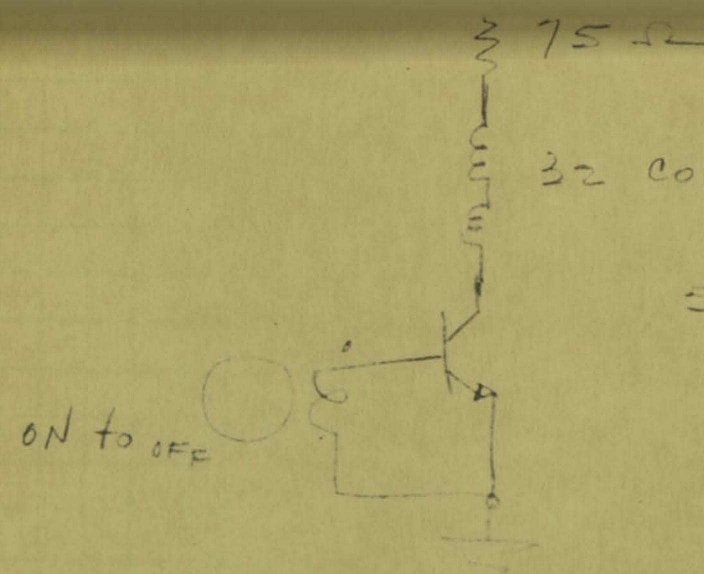
TRANSISTOR IS GOING FROM "ON" TO "OFF".
THE 32 CORES IN THE COLLECTOR ARE NOT BEING SWITCHED. THEY ARE INHIBITED AND OPERATING IN THE SATURATED REGION. (CANTAC SAID THAT THEIR ACTUAL LIMIT ON THE NUMBER OF CORES IS 15 AND NOT 32.)
THE −4 VOLTS ON THE BASE IS FROM THE INPUT CORE FROM SATURATION TO REMANENCE.

INFORMATION DESIRED.

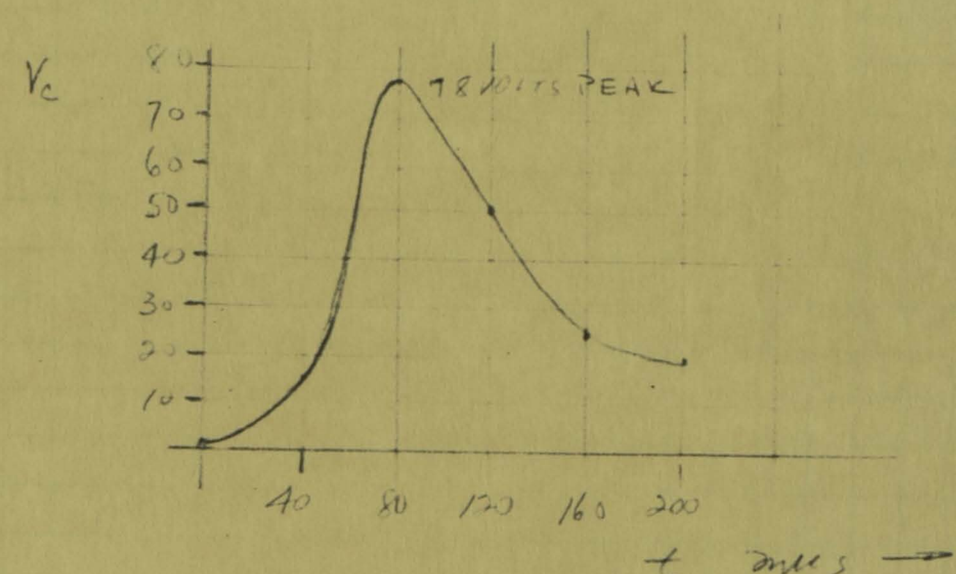
HOW WILL THE FOLLOWING EFFECT RELIABILITY?

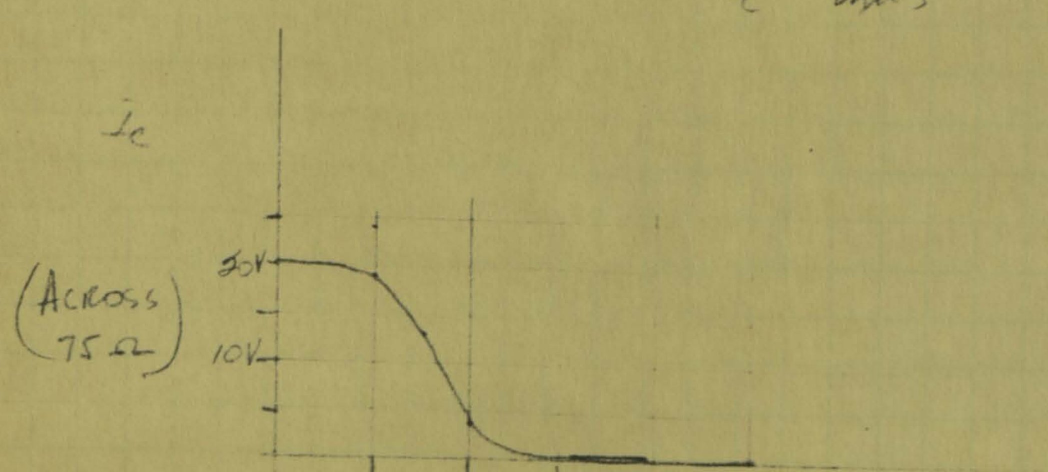
1. THE 10.4 WATT PEAK POWER SPIKE (FROM THE V_C & I_C CURVES)
2. THE CLAMPING OF THE SPIKE ON LOW BV_{CEO} UNITS

[illegible] 4/13/59



32 CORES NOT SWITCHED
(INHIBITED)
50 VOLT SPIKE

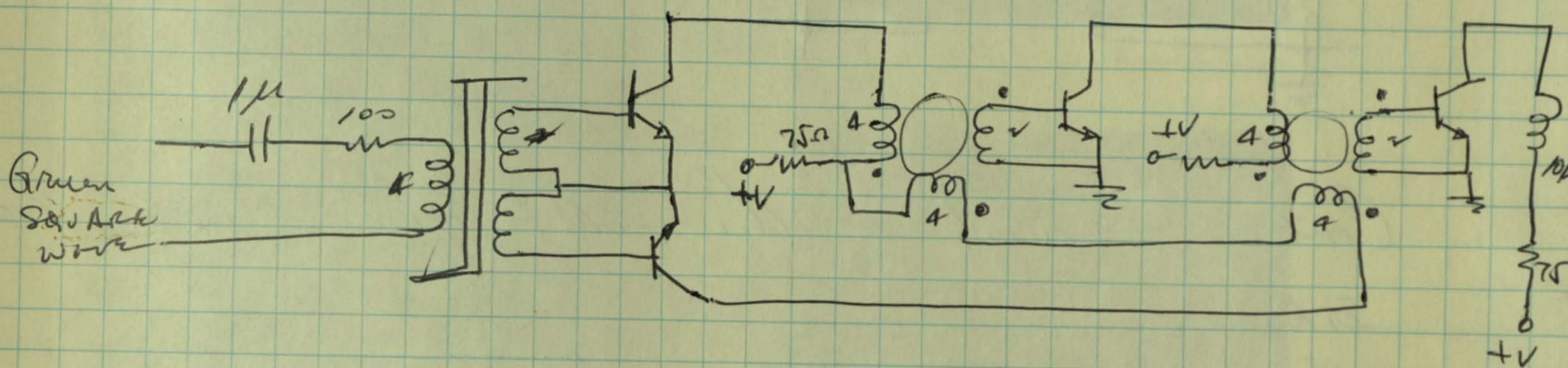




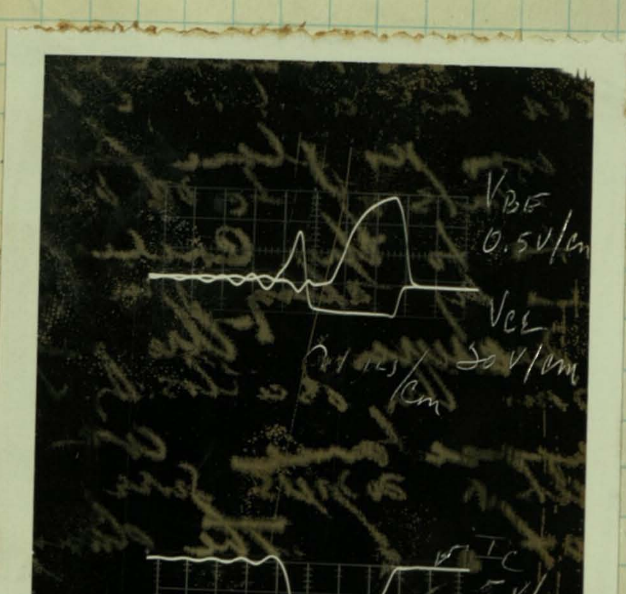
[illegible] 4/13/59

4/14/59

Started looking into the IBM circuit and the condition described on page 144. Set-up the following circuit.



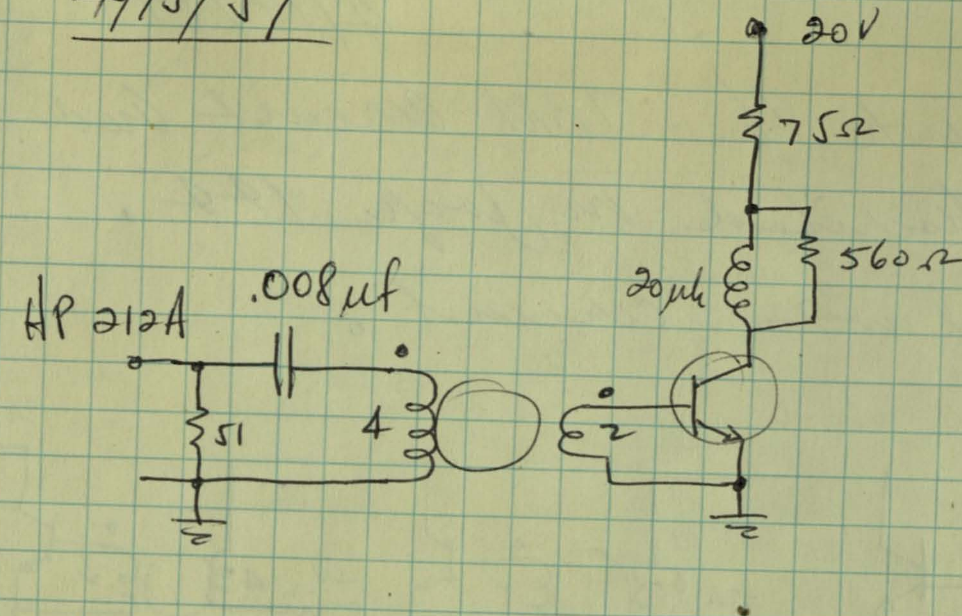
The circuit of interest is the last stage. The saturated core load was simulated with a 10 µh choke.



The $L\frac{di}{dt}$ peak on turn-off was approximately 30 volts. Increasing the inductance to 16 µh did not increase the peak. Will continue work on a circuit to give a higher $\frac{di}{dt}$ on turn off

[signature] 4/14/59.

4/15/59

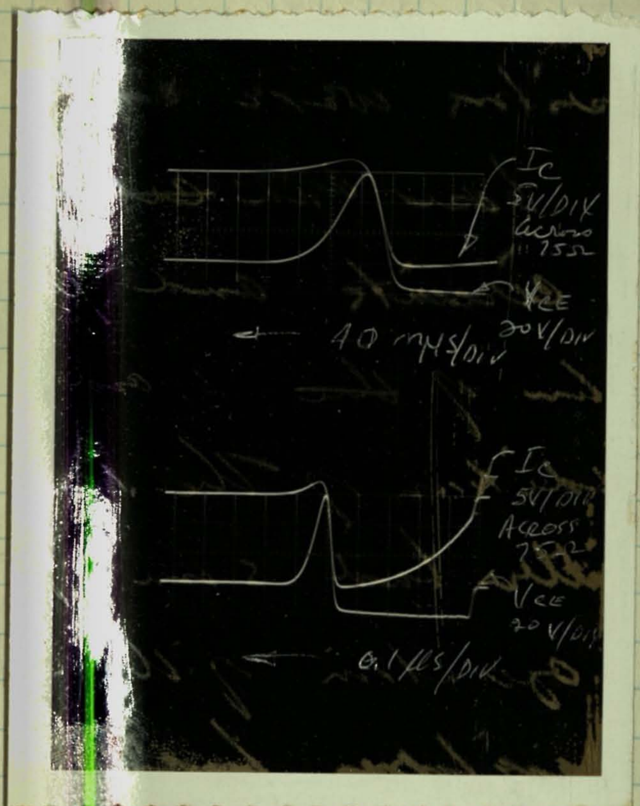


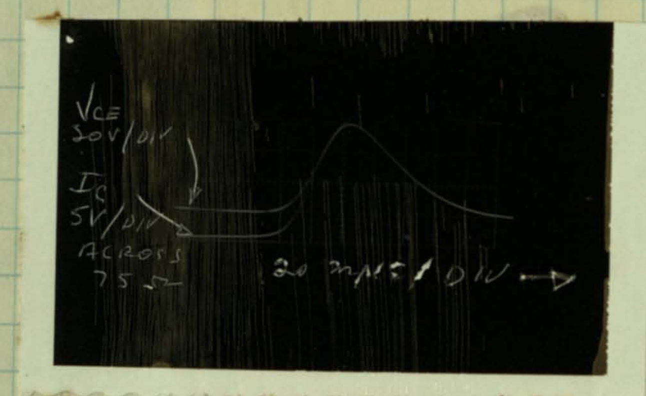
Continued work in the IBM Kingston circuit with I. Haas.
The test circuit was changed as shown. The core was set and reset by capacitor charge and discharge currents. Initially the ~~circuit was~~ 560 Ω resistor shunting the choke was omitted. This resulted in ringing on turn-off as there was no place for the coil energy to go except to the collector to emitter capacitance. By measuring the frequency of ringing, the total capacitance was found to be about 17 pf. The damping resistor was then added and the waveforms (current & voltage) looked approximately as the waveforms described by IBM.

R T [illegible] 4/15/59

4/15/59

Pictures of the current and voltages were taken

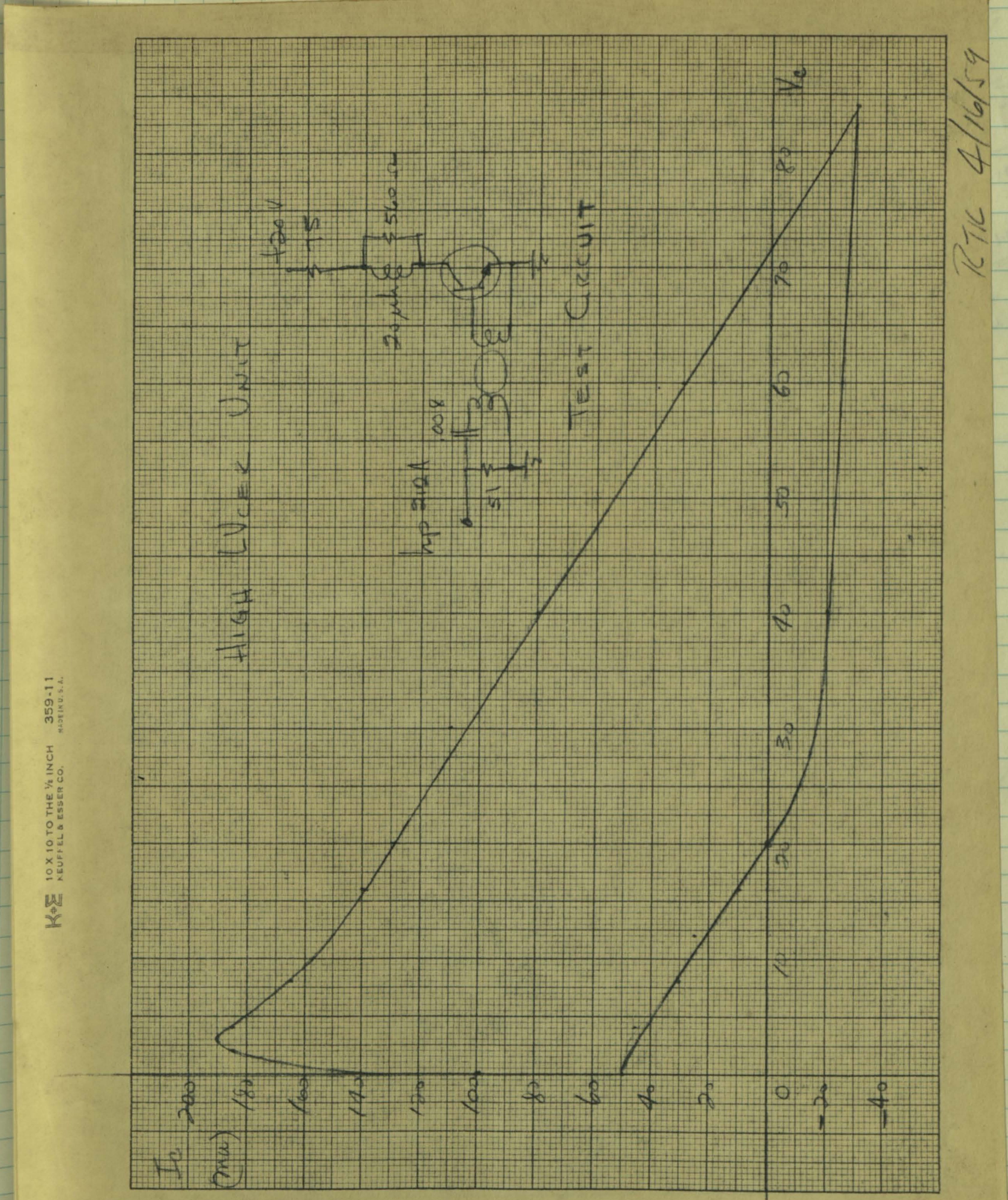




Observing also the base & emitter currents indicated that most of the current was going into the capacitance. Will make a closer observation of these currents.

Some low LVcer units were tried and definite clipping action was observed at approximately the LVcer voltages measured by I. Haas on the high speed plotter. The clipping action was more pronounced when the Vcc was increased (to 90 volts)

R T [illegible] 4/15/59



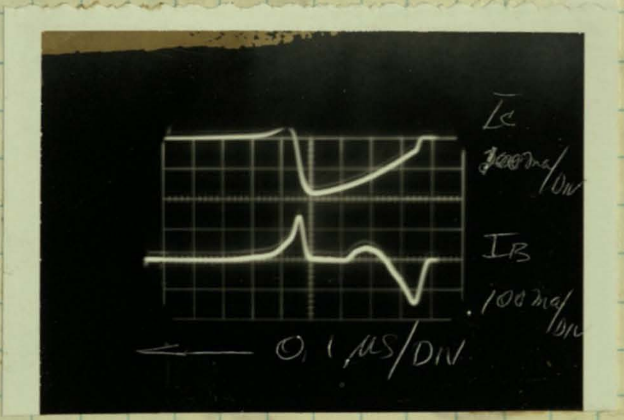
K+E 10 X 10 TO THE ½ INCH 359-11
KEUFFEL & ESSER CO. MADE IN U.S.A.
HIGH LVCEK UNIT
+20 V
75
20 μh
560 Ω
hp 212A
.008
51
TEST CIRCUIT
Ic
(ma)
200
180
160
140
120
100
80
60
40
20
0
-20
-40
10
20
30
40
50
60
70
80
Vc
RTK 4/16/59

4/16/59

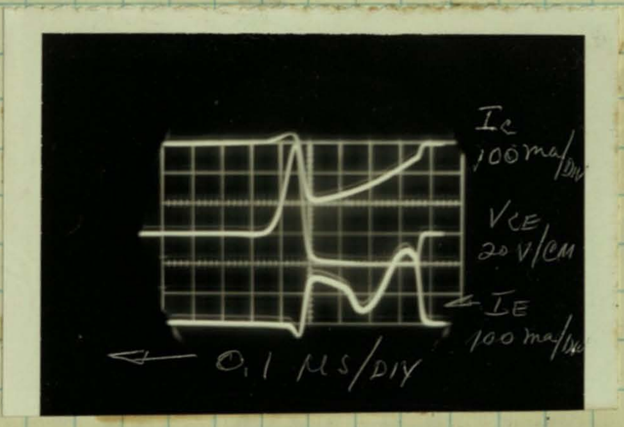
4/16/59

Continued work on the IBM Kingston Circuit.

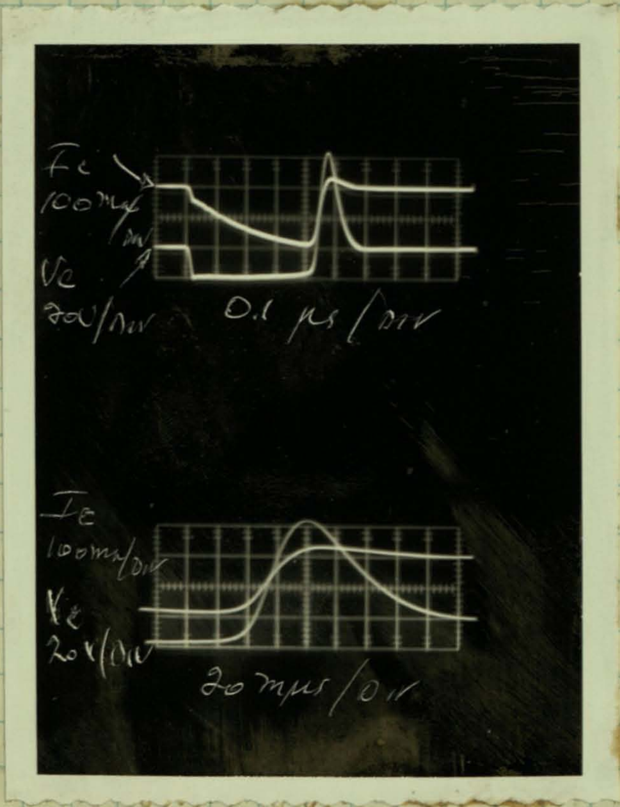
1 Ω current measuring resistors were added

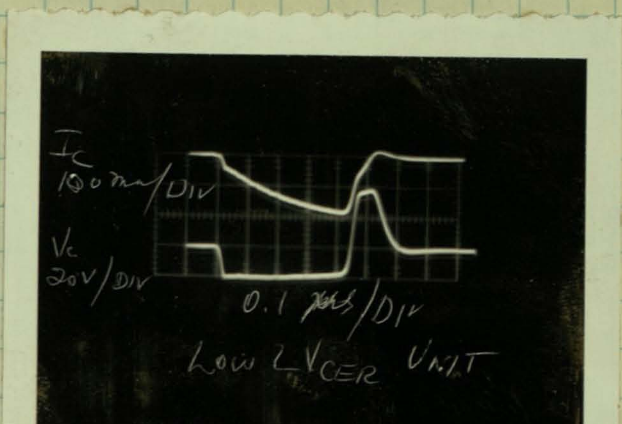


to the base and ~~collector~~ emitter circuits and pictures were taken of ~~the~~ I_B and I_E. The addition of the 1 Ω in the emitter had some effect on the operation of the circuit. The waveforms, however, give ~~a~~ reasonably accurate picture of the current.

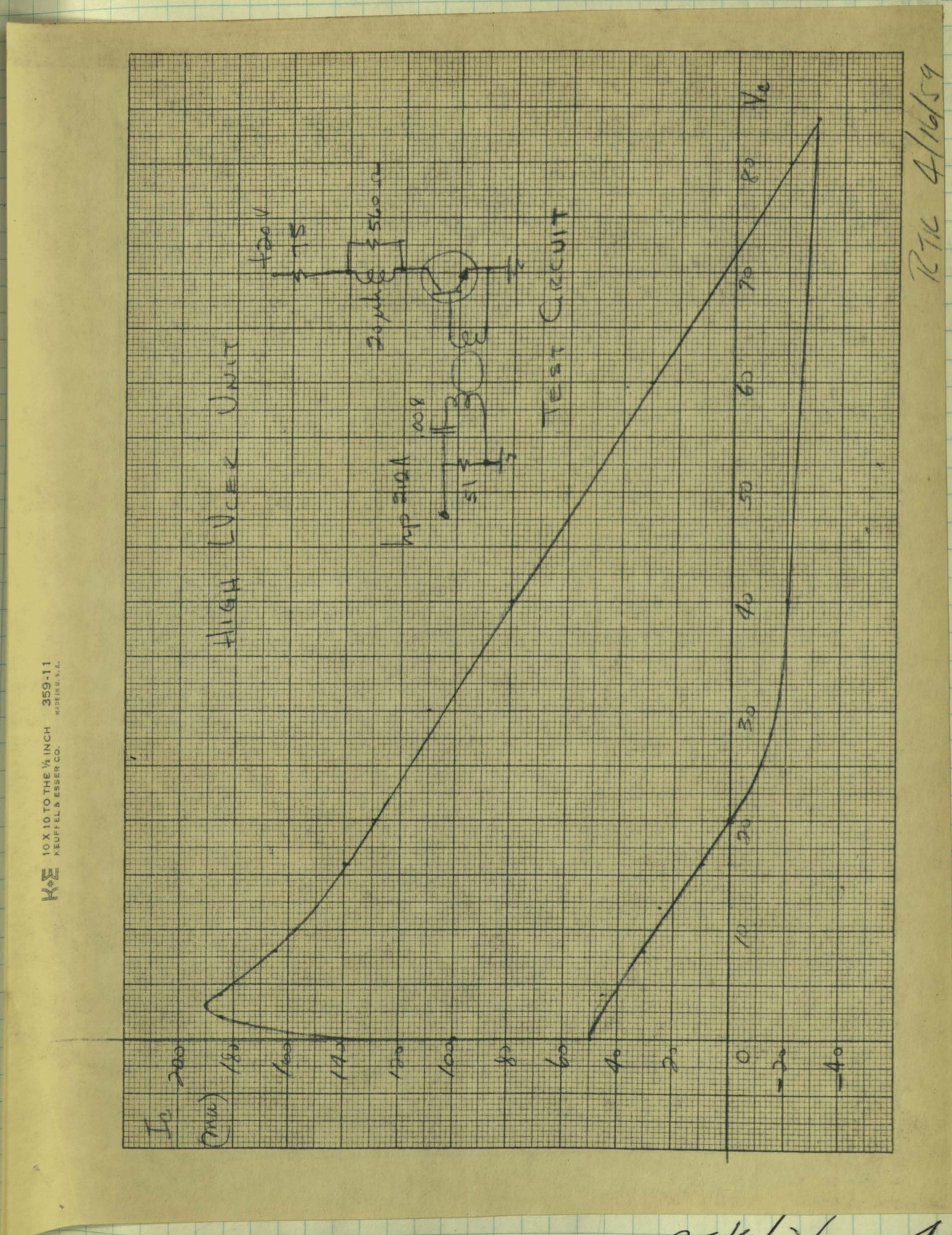


Pictures were taken of ~~two~~ a high LV_{CER} and a low LV_{CER} unit. Plots of I_C vs V_C were made by taking point by point from the oscilloscope display with a 20 mμs sweep.

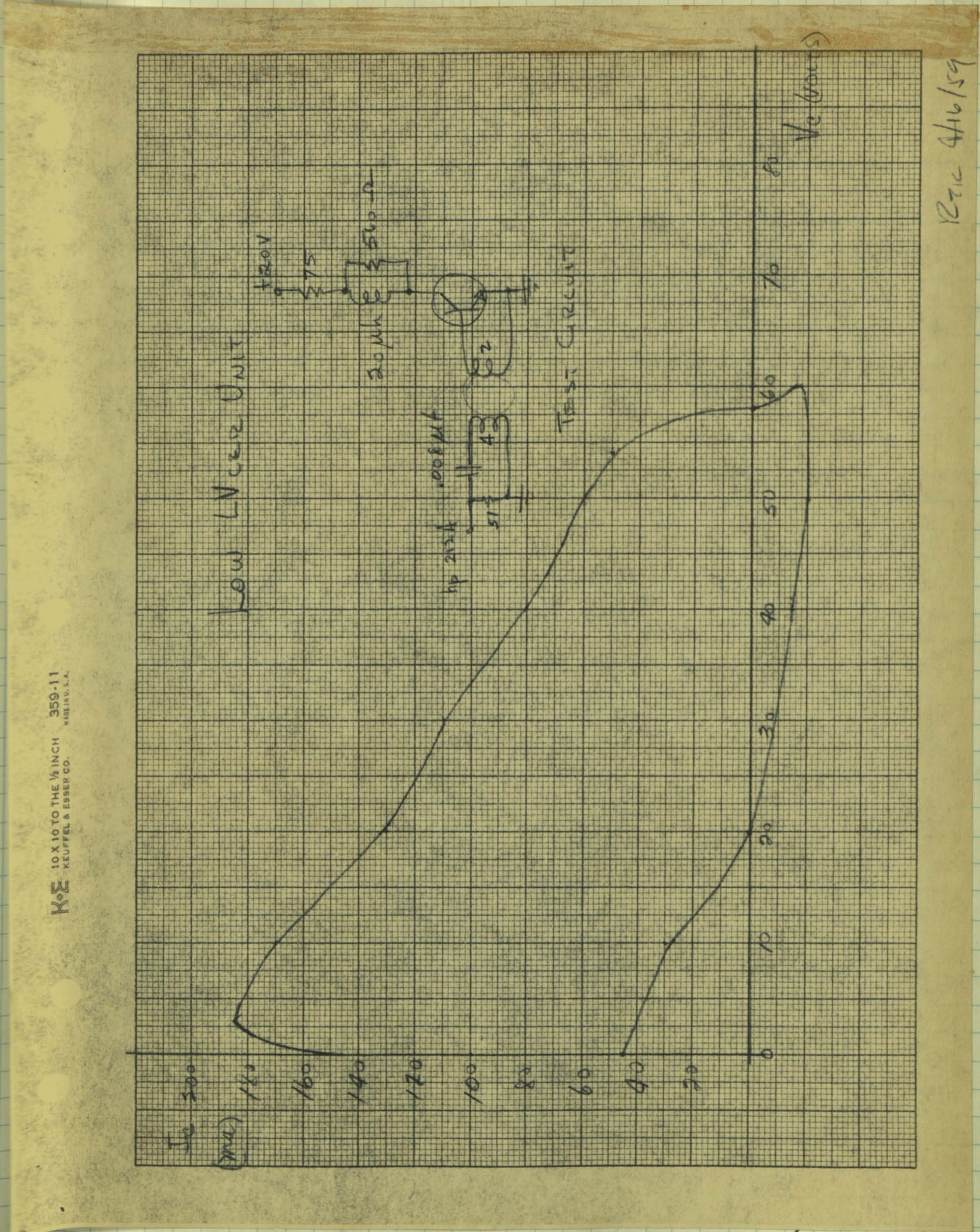




[signature] 4/16/59



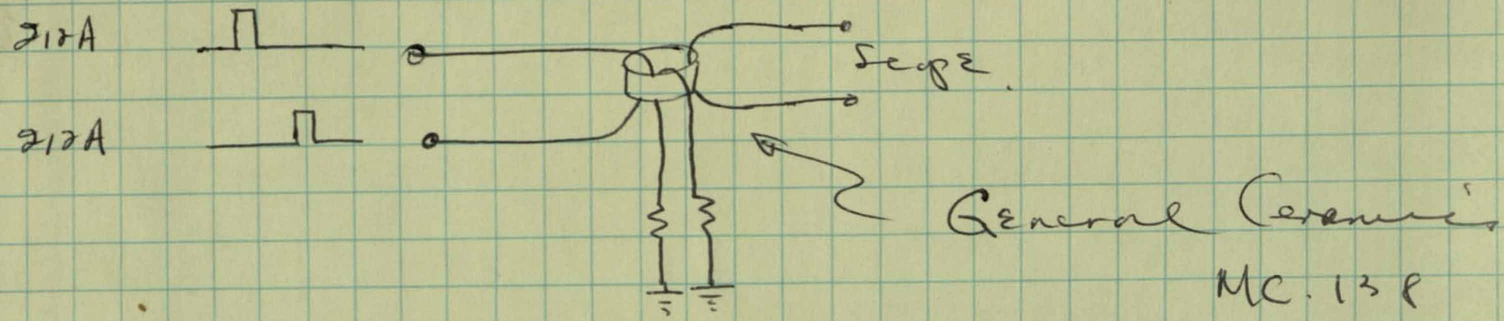
RTKkikana 4/16/59


K+E 10 X 10 TO THE ½ INCH 359-11
KEUFFEL & ESSER CO. MADE IN U.S.A.
Low LVceir Unit
Test Circuit
+20V
75
560 Ω
20 μh
hp 212A
.008 μf
51
Ic (ma)
Vc (volts)
0
10
20
30
40
50
60
70
80
200
180
160
140
120
100
80
60
40
20
4/16/59

R T [illegible] 4/16/59

4/22/59

Set up the following circuit for core testing



Took ~~of~~ a few spot checks on the data taken by Bob McMahon (Solid State circuit Conference 1958). Since the data obtained is in good agreement with McMahons, it will not be taken again.

Resumed work on the two transistor - one core blocking oscillator as shown on page 141. The circuit has a tendency to free-run. ~~when~~ Will continue work on this circuit so that it will operate as a stable flip-flop.

R. T. [illegible] 4/22/59

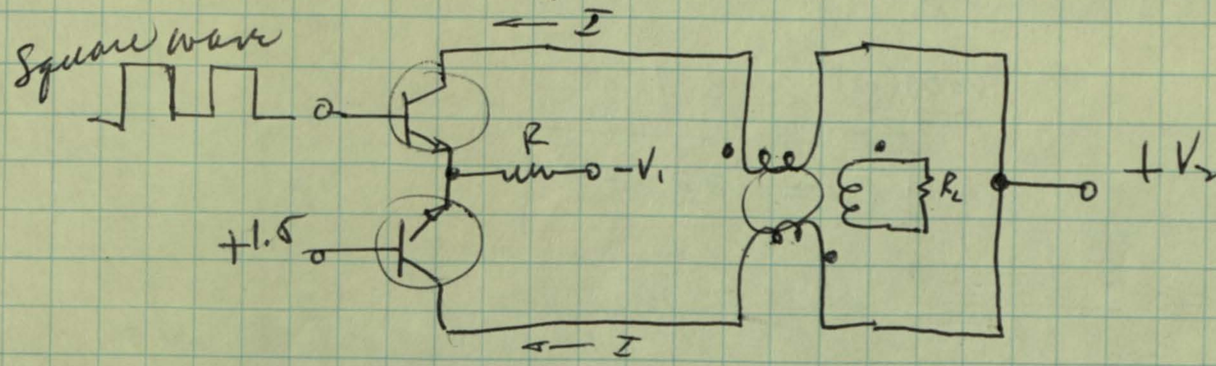
4/28/59

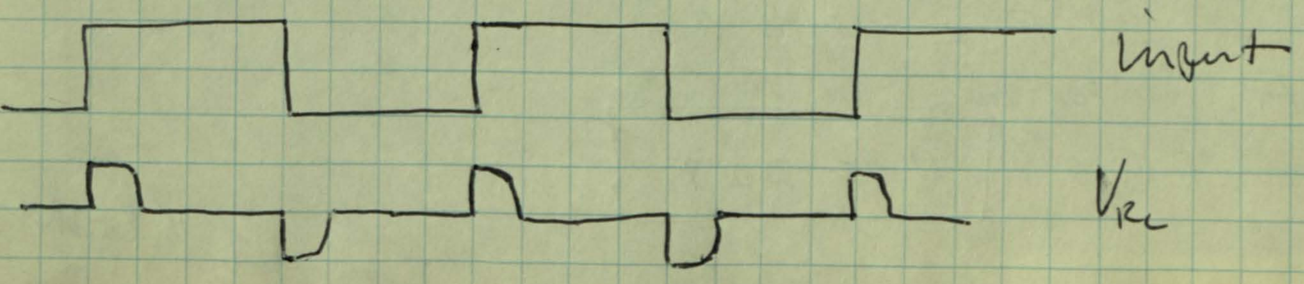
FT 4100's were tried in the 5 Megacycle shift register. 8 AB's and 8 AC's were tried in groups of 4. There was no significant increase in ~~off~~ speed. Operation was not as stable as with the 2N696 and 2N697's. It appears that the FT4100 will require more base drive (by increasing the base turns by 1, say). Since there will be no appreciable increase in speed, anyway, this will not be tried at this time.

R T [illegible signature] 4/28/59

4/29/59

Started work on a read-write pulse generator for use with the constant current core driver shown on page 126

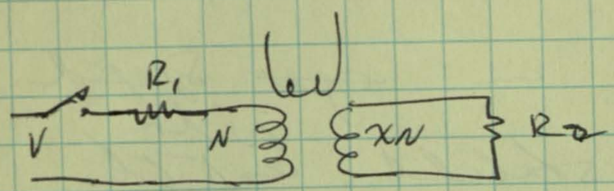




Design of Core circuit:

Core: Magnetics, Inc. 80529 $\frac{1}{4}$ D30

$C_s = 0.376$ AT μs
$F_0 = 0.15$ AT
$\Phi = 0.8$ volt μsec / turn.



We want 5 volts out with a pulse width of 1.5 μs

$$xN = \frac{VT_s}{\Phi} = \frac{(5)(1.5)}{(0.8)} \simeq 10T$$

$$T_s = \frac{\left(\frac{x^2}{R_2} + \frac{1}{R_1}\right) N^2 \Phi + C_s}{\frac{NV}{R_1} - F_0}$$

Since the source is a constant current, F,

$$T_s = \frac{\frac{x^2 N^2 \Phi}{R_2} + C_s}{F - F_0}$$

For small droop, $\frac{x^2 N^2 \Phi}{R_2} >> C_s$

Let $\frac{x^2 N^2 \Phi}{R_2} = 10 C_s$

$$\frac{(100)(.8)}{R_2} = 3.7$$

$$R_2 \simeq 22\ \Omega$$

$$F - F_0 = \frac{3.7 + .37}{1.5} \simeq 2.7$$

$$F = 2.8 \text{ AT}$$

Let I = 100 ma

$$N \simeq 30T$$

RT Kikoshima
4/29/59

TYPE 200 WAVEF

Each of the two groups of 50 knobs on the front panel of the **Synthesizer** adjusts a characteristic of a small segment of the total output waveform. Which characteristic—amplitude, slope, width, etc.—is determined by the plug-in generator being used with the **Type 200.**

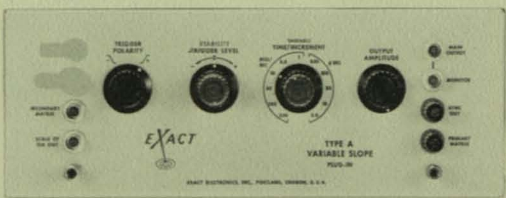
The plug-in generators furnish the versatility of triggering and lockout features as well as a wide range internal timing source necessary for the basic **Type 200.** The desired complex main output from the plug-in is then a result of combining the two independent **Type 200** increment outputs (primary matrix and secondary matrix).

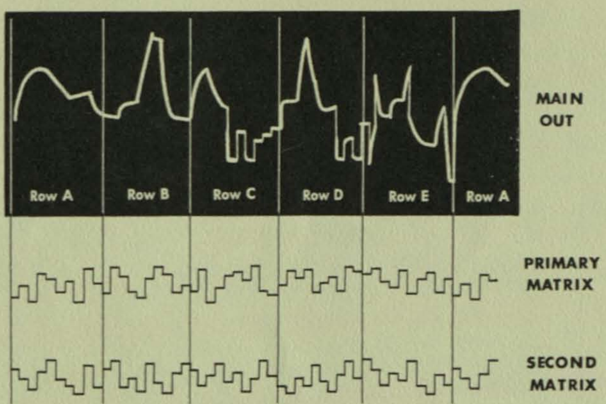
The ease and speed in producing nearly any waveshape needed gives this instrument application in every scientific field. A few are listed below:

COMPUTER PROGRAMMING — PCM-PTM SYSTEMS
BASIC RESEARCH — SPECTRUM SIMULATION
SERVO DESIGN & TEST — RADAR PULSE CODING
SPEECH AND SOUND SYNTHESIS
TELEMETERING CHANNEL SYNTHESIS

TYPE A VARIABLE SLOPE GENERATOR

PLU





The **Type "A"** plug-in produces a main output waveform having 10, 20, 30, 40 or 50 increments (segments) with independently variable amplitude and slope. Continuously variable timing over a wide range permits creation of sine waves, irregular waveforms, sawtooths and triangular functions, discontinuous waveforms, etc. Auxiliary outputs provide variable amplitude increments with the same time base as the main output.

MAIN OUTPUT

No. of increments	10, 20, 30, 40, or 50
Time/increment	1 sec. to 3.3 μsec.
Increment Amplitude	0-50 v variable
Increment Risetime	0.4 μsec
Time Jitter	1 part in 10,000/incr.
Amplitude Stability	.5% of max. ampl.
Slope limits (each incr.)	20% or $\pm$10 v, whichever greater
Waveform continuity	within 3%
Waveform power	50 v @ 10 ma
Overall waveform ampl.	var. over 3 to 1 range
Waveform ref. level	factory adj. 0

TRIGGERING

Internal	free running generator

MATRIX OUTPUTS

Increment Amplitude	0-10 v variable
Increment Risetime	0.2 μs

All other specifications same as MAIN output

GENERAL

Scale of ten out	40 v gate every 10th increment
Sync out	30 v amplitude
Monitor	Isolated output parallel to main output
Accessories included	Sync out cable, Main output coax

Price **$325**
f.o.b. factory

TENTATIVE

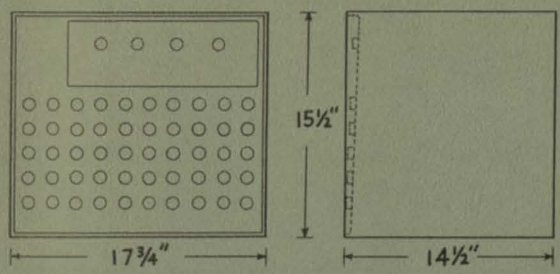
TYPE D CONTINUOUS WAVEFORM GENERATOR

The ouptut from this plug-in combines the features of slope and width. An output is produced which is an uninterrupted waveform composed of increments having independently variable width and slope. This unit will provide a trigger lockout feature and wide range continuous timing.

Tentative production	**August 1960**
Tentative price	**$300**

EXACT ELEC

ORM SYNTHESIZER



GENERAL SPECIFICATIONS

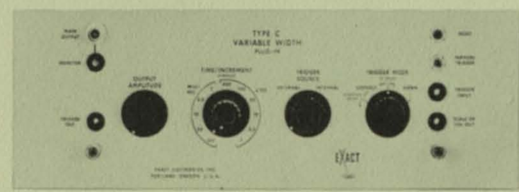
No. of increments	10, 20, 30, 40 or 50
Increment position	indicated by neon bulbs
Power req.	105-125 v 50-60 cps. 425 watts
Weight	58 lbs

TYPE 200 **$1575**
TYPE 200 RM **$1600**
f.o.b. factory

G-INS

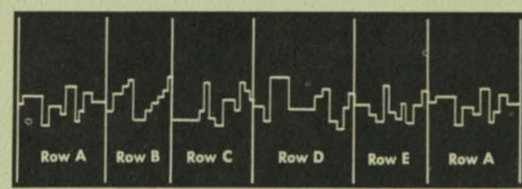
VARIABLE WIDTH GENERATOR

TYPE C



The **Type "C"** plug-in produces an output waveform made up of increments having independently adjustable width as well as amplitude. The number of increments in the total waveform can be controlled through a lockout-reset feature which permits internal or external sequence gating. Incremental pulse widths from 1 μsec to 1 sec. are available. A monitor jack is provided for parallel ocsilloscope observation.

MAIN OUT



TRIGGERING

In the LOCKOUT MODE the generator can be armed and, depending on the TRIGGER SOURCE, will either internally generate a pre-set number of increments or wait for additional external or manual triggering

Lockout by 10 count	re-arm for each row of ten incr.
Lockout by program count	re-arm for each total no. of rows (10, 20, 30, 40, or 50 incr.)
Normal Mode	No lockout feature
INT source	Free Running Generator at Time/Increment Rate
EXT. source	5 v at 1 μsec. RT
Manual (EXT.)	single shot

MAIN OUTPUT

No. of increments	10, 20, 30, 40, or 50
Time/increment	1 sec to 1 μsec.
Increment amplitude	0-50 variable
Time Jitter	1part in 10,000/incr.
Amplitude stability	0.2% of max. ampl.
Variable width ratio	1:10 per incr.
Waveform power	50 v @ 10 ma
Overall waveform amplitude	Var 3 to 1 range
Waveform ref. level	Factory Adj. to 0

GENERAL

Scale of ten out	40 v gate every 10th incr.
Sync out	+30 Volts
Monitor	isolated output

Accessories included: Sync out cable
Main output coax

Price **$300**
f.o.b. factory

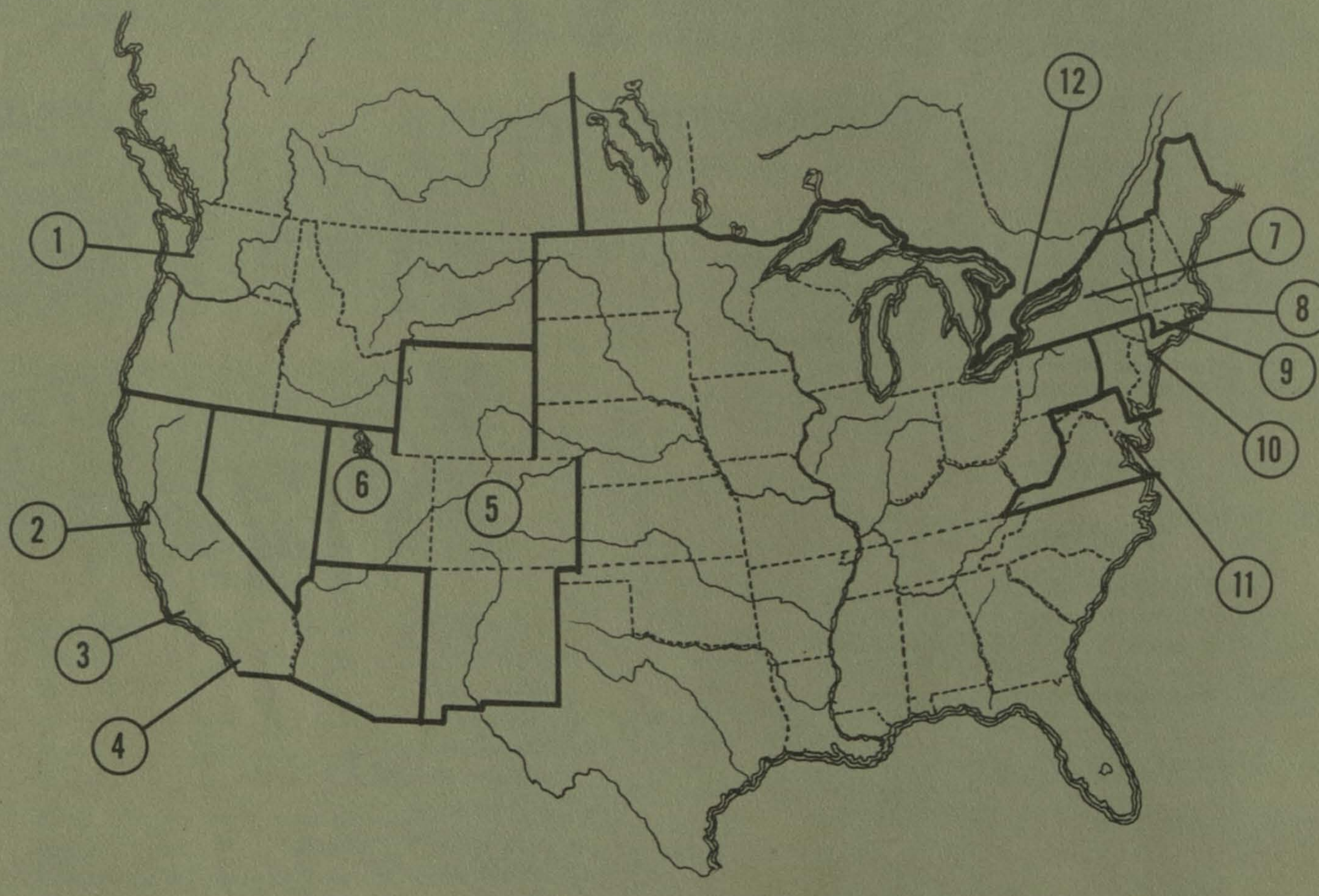
PLUG-INS

TYPE E PULSE TRAIN GENERATOR

This plug-in takes the two independent matrix outputs from the basic Type 200 and arranges them to run concurrently for a main output of 100 increments variable in amplitude and timing. This unit will be very useful in stairstep and pulse train applications.

Tentative production .... **August 1960**
Tentative price **$200**

TRONICS INC.



(1) Northwest & Western Canada
COMPTRONICS
Suite 123-124
No. 2 Hanford St.
Seattle 4, Wash.
Phone: MAin 4-5135

(2) Northern California
GERALD B. MILLER CO.
1334 Old County Rd.
Belmont, Calif.
Phone: LYtell 1-0365

(3) Los Angeles Area
GERALD B. MILLER CO.
1550 N. Highland Ave.
Hollywood 28, Calif.
Phone: HOllywood 2-1195

(4) San Diego & Arizona
GERALD B. MILLER CO.
P.O. Box 6544
Phone: ACademy 2-1121

(5) Colorado & New Mexico
HYTRONIC MEASUREMENTS
1295 So. Bannock St.
Denver, Colo.
Phone: PEarl 3-3701

(6) Utah & Wyoming
HYTRONIC MEASUREMENTS
2022 So. Main St.
Salt Lake City, Utah
Phone: INgersoll 6-4924

(7) Syracuse Area
TECHNICAL INSTRUMENTS INC.
916 Liverpool Road
Liverpool, New York
Phone: OLdfield 2-2534

(8) Boston Area
TECHNICAL INSTRUMENTS INC.
90 Main St.
Reading, Mass.
Phone: REading 2-3930

(9) Connecticut
TECHNICAL INSTRUMENTS INC.
1115 Main St.
Bridgeport, Conn.
Phone: FOrest 8-4582

(10) N.J. lower N.Y., Long Island Eastern Penn., & Delaware
R.E. WEBER CO.
15 Terry Lane
East Brunswick, N.J.
Phone: CIfford 7-5243

(11) Maryland, Wash. D.C. & Virginia
C.E. SNOW CO.
8218 Wisconsin Ave.
Bethesda, Md.
Phone: OLiver 4-1767

(12) Eastern Canada
ALLEN CRAWFORD ASSOC.
P.O. Box 214
Willowdale, Ontario, Canada
Phone: BAldwin 5-7391