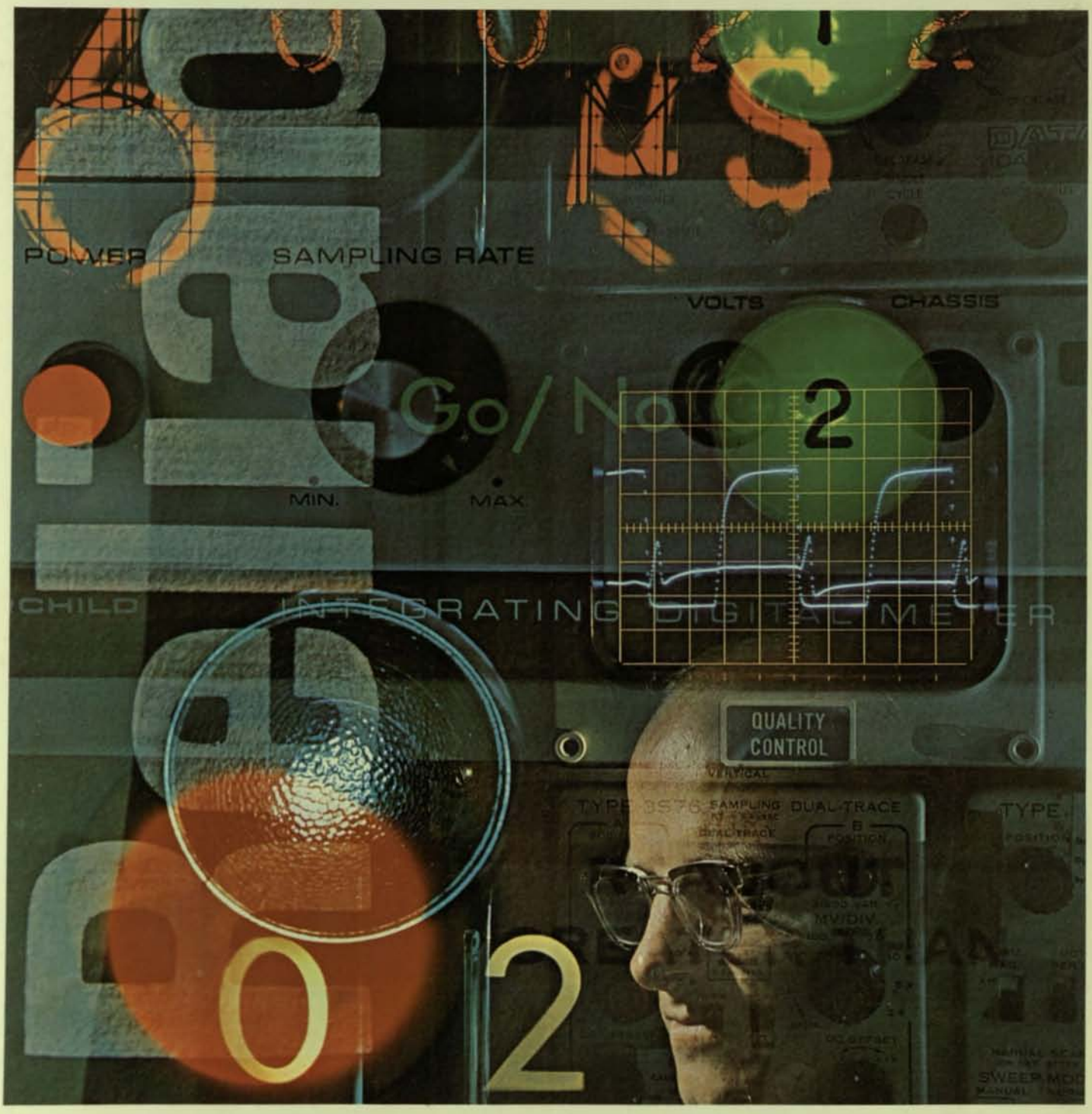
Fairchild Reliability



The UNIQUE Program

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The sunrise: inherently reliable—not because it happened once in some remote laboratory, but because it happens every day all over the world. Many separate factors combine to make it that way: the earth's rotation, gravitational fields, the frictionless vacuum of space; all of these are in part responsible for the final product—the inherent reliability of the sun.

This is the kind of reliability that Fairchild strives for. Not mere test hours accumulated in some laboratory, but the predictable culmination of many proven factors, time and time again, in one sure whole: an inherently reliable product.

Fairchild products are indeed reliable. They have to be. The failure of a single transistor or integrated circuit cannot be tolerated when the success of a space mission, the defense of the nation, or the life of an astronaut is at stake.

As the world's largest and most experienced supplier of silicon Planar* semiconductor devices, Fairchild is unquestionably in a position to supply aerospace and defense contractors with the reliable products their systems demand. Countless man-hours of the finest engineering talent in the country have been devoted to the elimination of common failure modes, and to the detection and resolution of others heretofore unsuspected. Planar II processing, EQR, and the C-B metal overlay have solved the problem of ion migration; the "field plate" has increased the voltage breakdown capabilities of Planar devices; ultrasonic bonding has significantly reduced bond failures; and heavy research in radiation resistance has resulted in a line of devices that can tolerate damaging effects of radiation—either from the Van Allen Belts, or from nuclear explosion.

Critical processes at Fairchild yield semiconductor products of inherent reliability. And exhaustive testing, under the new UNIQUE program, provides assurance that each device is indeed reliable. Taken together, they result in a product custom-tailored for the requirements of advanced systems design, bearing the name that for years has been synonymous with semiconductor progress and reliability—Fairchild.

*Planar is a patented Fairchild process.

The UNIQUE Program

What is UNIQUE?

Fairchild Semiconductor's UNIQUE Program is a full-scale manufacturing and testing program aimed at providing aerospace and defense contractors with readily available products that will meet the rigid specifications their systems demand. UNIQUE products are manufactured in separate facilities with special production forces, utilizing the Fairchild processes known to yield the most reliable product.

What Products are Available?

The UNIQUE Program includes those monolithic integrated circuits, transistors, and dual transistors that have demonstrated a degree of reliability consistent with the requirements of military specifications and the stated intent of the program. A detailed listing of UNIQUE products is available from all Field Sales Offices, or from the UNIQUE Program Office in Mountain View. Each quarter, as satisfactory reliability data is accumulated, additional products will become eligible for inclusion in the program, and will be added to the list accordingly.

What Does the Program Include?

The basic UNIQUE product, whether a transistor or an integrated circuit, includes processing on a separate line at Fairchild Semiconductor's new Aerospace and Defense facilities, stringent QA controls to ensure process integrity, 100% screening, traceability, and lot assurance through electrical, life, and environmental testing on a sample basis. Each UNIQUE product has a flow diagram that indicates the process steps involved and all applicable process specifications. Figure 1 is the flow diagram for CERPAK integrated circuits.

What Does it Cost?

There is no additional charge for the basic UNIQUE product. A reasonable charge for lot data and screening options, however, will be added to the basic device price, generally on a per lot basis.

Is UNIQUE Processing Available for Products Not Listed?

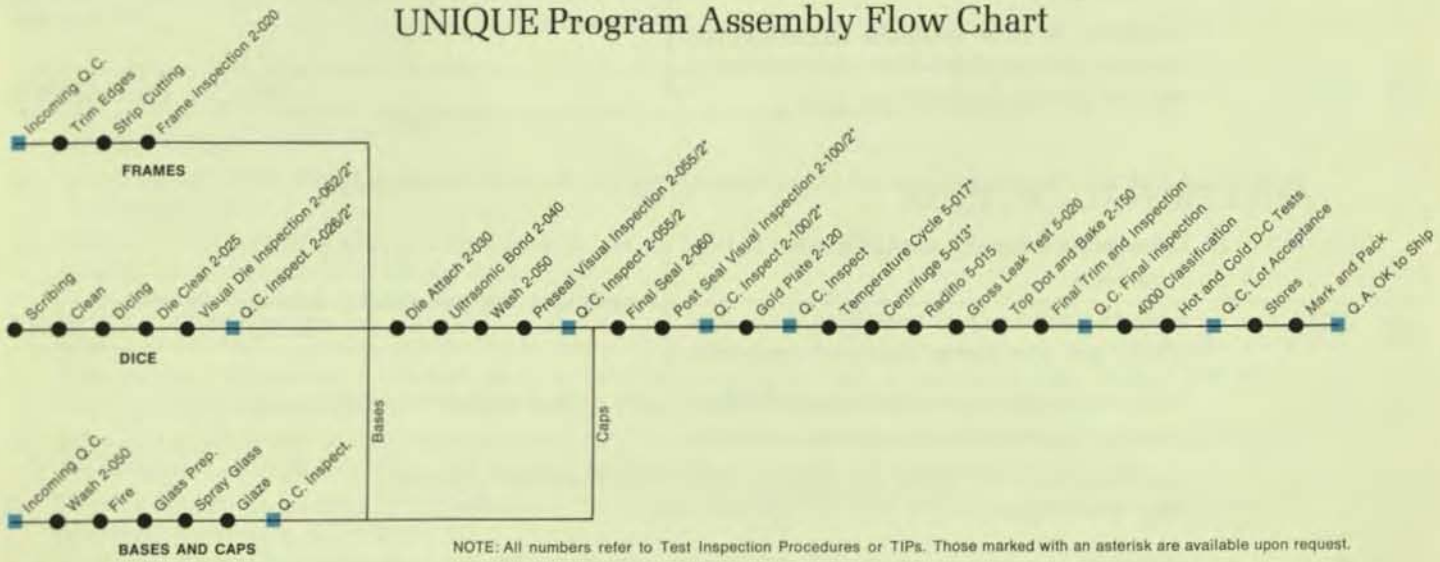
Fairchild Semiconductor will, in select situations, conduct special programs as a "Customer Special Test." Specifications, price, and delivery must be negotiated through the local Field Sales Engineer.

Additional Information

All inquiries regarding price, availability, and other specifics of the program should be directed to any Fairchild Field Sales Office, or to:

UNIQUE Program Office
Aerospace and Defense Department
Fairchild Semiconductor
313 Fairchild Drive
Mountain View, California 94040

UNIQUE Program Assembly Flow Chart



NOTE: All numbers refer to Test Inspection Procedures or TIPs. Those marked with an asterisk are available upon request.

Figure 1

UNIQUE Features and Options

Standard 100% Processing

The following processing steps have been implemented on all UNIQUE products to ensure device reliability. They are conducted on the most advanced test equipment available, according to rigid specifications explained in detail beginning on page 6.

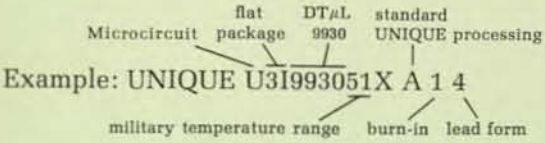
Delivery Code	Specified Processing	Purpose
A	the basic UNIQUE product, including:	
	traceability to original wafer lot	to identify all potential defects if any failure mode is suspected.
	Product Control Document	to save the customer the time and expense involved in drawing up his own specifications.
	100% pre-seal visual inspection	to screen out defects such as insufficient metallization, cracked dice, foreign materials, etc.
	100% post-seal inspection (ceramic packages)	to screen out sealing & plating anomalies.
	100% High Temperature Storage (Transistors only)	
	100% temperature cycling	to check thermal compatibility of dissimilar materials.
	100% centrifuge	to eliminate defective bonds or marginal die attaches.
	100% fine leak check 100% gross leak check	to eliminate defective package seals and insure package hermeticity to a very high level.
	100% electrical testing of key parameters.	to assure that product meets detailed electrical specifications.
	Group A electrical testing (sample). Group B life and environmental testing (sample).	to provide assurance that product is capable of withstanding various life and environmental stresses.
B	includes A plus generic Group B lot acceptance variables data and Group A attributes data	to provide documentation on performance characteristics.
C	includes A plus generic Group B lot acceptance variables data from specific lot, and Group A attributes data	

ADDITIONAL OPTIONS

1	burn-in (168 hours): units to meet Group A criteria:	to detect any potentially unstable devices.
2	burn-in (168 hours): variables data supplied; key parameter changes computed	
3	high temperature reverse bias (HTRB)—168 hours: units to meet Group A criteria	to detect surface impurities.
4	lead form per TIP 7-003; flat-package IC's only (See Fig. 6)	to facilitate installation
5	radiographic inspection (x-ray, 2 views) per TIP 8-005	to detect foreign materials inside package.

Ordering Instructions

UNIQUE processing and optional test routines are specified by adding the alphanumeric codes indicated to the basic Fairchild part number. For transistors, this is the regularly assigned 2N number; for integrated circuits, it is the ten digit product code provided on the price list and on all data sheets, designating package and temperature range in addition to the basic circuit.



Documentation Control

For those customers who need comprehensive documentation control to meet their contractual requirements, Fairchild provides a special Product Control Document with an assigned UNIQUE part number, thereby sparing the customer the time and expense involved in drawing up his own specifications. This document (see Figure 2) refers to a specific product specification, a general specication, a particular marking, and all standard UNIQUE options. No changes can be made without prior customer approval, and a revision letter will be attached to the document for change control. All specified deviations from UNIQUE processing must be approved by the Aerospace and Defense Products QA Manager in addition to the Production and Engineering Department Managers to assure that all changes are in accord with the intent of the program. Product Control Documents may be obtained from any Field Sales Office, or from the UNIQUE Program Office in Mountain View, California.

Fairchild UNIQUE

Product Control Document

Customer Name _____

Location _____

Customer Reference _____
(e.g., Drawing No. 248760 Rev. B)

NOTE: All blanks must be filled in and all "yes's" or "no's" answered.

S# _____
(Transistor)

SP# _____
(Special Products)

SL# _____
(Integrated Circuits)

UNIQUE PRODUCT SPECIFICATION _____
(e.g., 2N3965A or U3I993051X Rev. B)

GENERAL SPECIFICATION _____
(e.g., FSD 7000 Rev. A)

MARKING _____
(per General Specification Para. 3.5)

DELIVERY CODES	Yes	No
A. BASIC UNIQUE PART	___	___
B. BASIC UNIQUE PART, plus generic Group B Life and Environmental lot acceptance variables data and Group A attributes data.	___	___
C. BASIC UNIQUE PART, plus generic Group B Life and Environmental lot acceptance variables data from the specific lot, and Group A attributes data.	___	___

PROCESS OPTIONS	Yes	No
1. Burn-In for 168 hours at full rated power at 25°C for transistors; and at maximum rated voltage and 125°C for integrated circuits. All units to meet Group A electrical parameters after Burn-In.	___	___
2. Burn-In for 168 hours at full rated power at 25°C for transistors; and at maximum rated voltage and 125°C for integrated circuits. Variables data supplied and percent change in key parameters computed.	___	___
3. Burn-In for 168 hours **H**igh **T**emperature (+160°C) **R**everse **B**ias (75% of BV_{CBO}). All units to meet Group A electrical parameters after Burn-In.	___	___
4. Lead form on flat packages integrated circuits per Jig Number 253, TIP 7-003.	___	___
5. Radiographic Inspection (X-Ray, 2 views) per TIP 8-005.	___	___

Test Inspection Procedures

One of the most important aspects of the UNIQUE program is process control. All process and test procedures are regulated through comprehensive Test Inspection Procedures, or TIP's, maintained by the Quality Assurance Dept. of the Aerospace and Defense Products facility. Specific TIP numbers are included for reference on all UNIQUE product flow diagrams and control documents, and are available to individual customers upon request through the UNIQUE Program Office.

Traceability (TIP 2-005)

The main purpose of traceability is to facilitate the identification of potential defects whenever a failure mode is suspected. All devices are marked with a four digit date code that identifies the week and year of manufacture, and provides traceability to the original wafer lot. If wafers from more than one wafer lot are used in a given week's final assembly, a letter suffix is appended to the code.

Pre-seal Visual Inspections (TIP's 2-026, 2-055)

UNIQUE products undergo two 100% visual inspections followed by QC inspections prior to final seal. Before dice are approved for assembly, they are checked under high-power microscope for cracks, chips, presence of foreign materials, inaccurate photo-resist patterns, oxide deficiencies, and improper aluminum interconnects. Again after assembly, but before final seal, the devices are checked for these same anomalies, plus any others incurred in the assembly process, such as scratched metal or defective bonding. Integrated circuits undergo a third (post-seal) visual inspection (TIP 2-100/2).

High Temperature Storage (TIP 5-009)

All transistors are stored for 24 hours at 200°C.

Temperature Cycling (TIP 5-017)

Devices are subjected to a low ambient temperature of −65°C until stabilization, and then to a high temperature of +200°C. Cycling is repeated ten times, in accordance with MIL STD 750, Method 1051-C.

Centrifuge (TIP 5-013)/Pneupactor (TIP 5-024)

The normal centrifuge acceleration level for screening defective bonds is 20,000 G's for one minute in the Y_1 axis. An alternate test method utilizes the Fairchild pneupactor to accomplish the same end result. The pneupactor accelerates the device down a tube into a phenolic block. In this test, the force level is 25,000 G's for a pulse width of 25 μsec. in the Y_1 axis.

Fine Leak Check (TIP 5-015)

To ensure package hermeticity, Fairchild utilizes the RADIFLO method for leak detection to a level of 10^{-8} cc-ATM/sec. for transistors and integrated circuits. Under this test procedure, a radioactive tracer gas (Krypton 85) is forced into the package, and a scintillometer is used to detect the leak rate as a function of time, pressure and activity level of the gas. Testing is in accordance with MIL STD 202, Method 112-C.

Gross Leak Check (TIP 5-020)

Another test for package hermeticity is the hot oil bubble method, in accordance with MIL STD 202C, Method 112-A. This test is conducted by immersing the device in a clear hot oil and watching for escaping bubbles caused by gas expansion within the package.

Group A Electrical Testing (see Figure 3)

Actual sample size and test criteria are as outlined in each particular UNIQUE product specification, but, in general, conform to the following characteristics:

Transistors

1. All room temperature DC parameters are grouped and tested to a 1% overall AQL. If the sample fails, the lot is screened and re-sampled to the failed parameter with an individual AQL of 0.65%.
2. All AC and temperature tests are to an individual parameter AQL of 2.5%.

Integrated Circuits

1. All 25°C DC tests are grouped to a 10% LTPD.
2. All hot (70°C or 125°C) DC tests are grouped to a 15% LTPD.
3. All cold (−55°C or 0°C) DC tests are grouped to a 15% LTPD.
4. All AC tests are grouped to a 10% LTPD.

Table 1—Group A inspection.

Examination or test	Conditions		AQL 2N2060	Symbol	Limits		Unit
	MIL-STD-750 method	Specific conditions			Min.	Max.	
Subgroup 1			1.0				
Visual and mechanical examination	2071						
Subgroup 2			1.0				
The ratio of h_{FE1} to h_{FE2}		$I_C = 0.1$ mA $V_{CE} = 5.0$ Vdc		$\frac{h_{FE1}}{h_{FE2}}$	0.9	1.0	
The ratio of h_{FE1} to h_{FE2}		$I_C = 1.0$ mA $V_{CE} = 5.0$ Vdc		$\frac{h_{FE1}}{h_{FE2}}$	0.9	1.0	
Base voltage differential		$I_C = 0.1$ mA $V_{CE} = 5.0$ Vdc		V_{BE1}-V_{BE2}		0.005	Volts
Base voltage differential		$I_C = 1.0$ mA $V_{CE} = 5.0$ Vdc		V_{BE1}-V_{BE2}		0.005	Volts
Breakdown voltage, collector to base	3001 Condition D	$I_C = 0.1$ mA $I_E = 0$		BV_{CBO}	100		Volts
Breakdown voltage, emitter to base	3026 Condition D	$I_C = 0$ $I_E = 0.1$ mA		BV_{EBO}	7.0		Volts
Breakdown voltage, collector to emitter	3011 Condition B Pulsed[1]	$I_C = 100$ mA $R_{BE} \leq 10$ ohms		BV_{CER}	80		Volts
Breakdown voltage, collector to emitter	3011 Condition D Pulsed[1]	$I_C = 30$ mA $I_B = 0$		BV_{CEO}	60		Volts

Figure 3—Typical Example of Format

Group B Life and Environmental Testing
(See Figures 4 and 5)

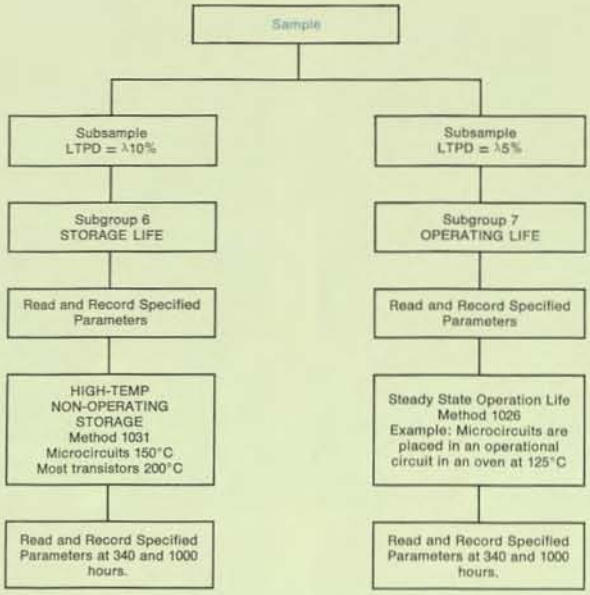
For purposes of lot qualification, a manufacturing lot is defined as six weeks' production. Finished units from each week's production will be held in Bonded Stores until the full lot is accumulated, at which time a sample will be drawn and subjected to environmental, operating life, and storage life testing. Individual product specifications will detail LTPD's, test conditions, and limits.

Transistors

In accordance with industry-accepted homogeneity principles, the qualification of a given gain or voltage class will qualify other gain or voltage classes. Qualification of the 2N3965, for example, will qualify the 2N3963 from the same manufacturing lot, as defined above.

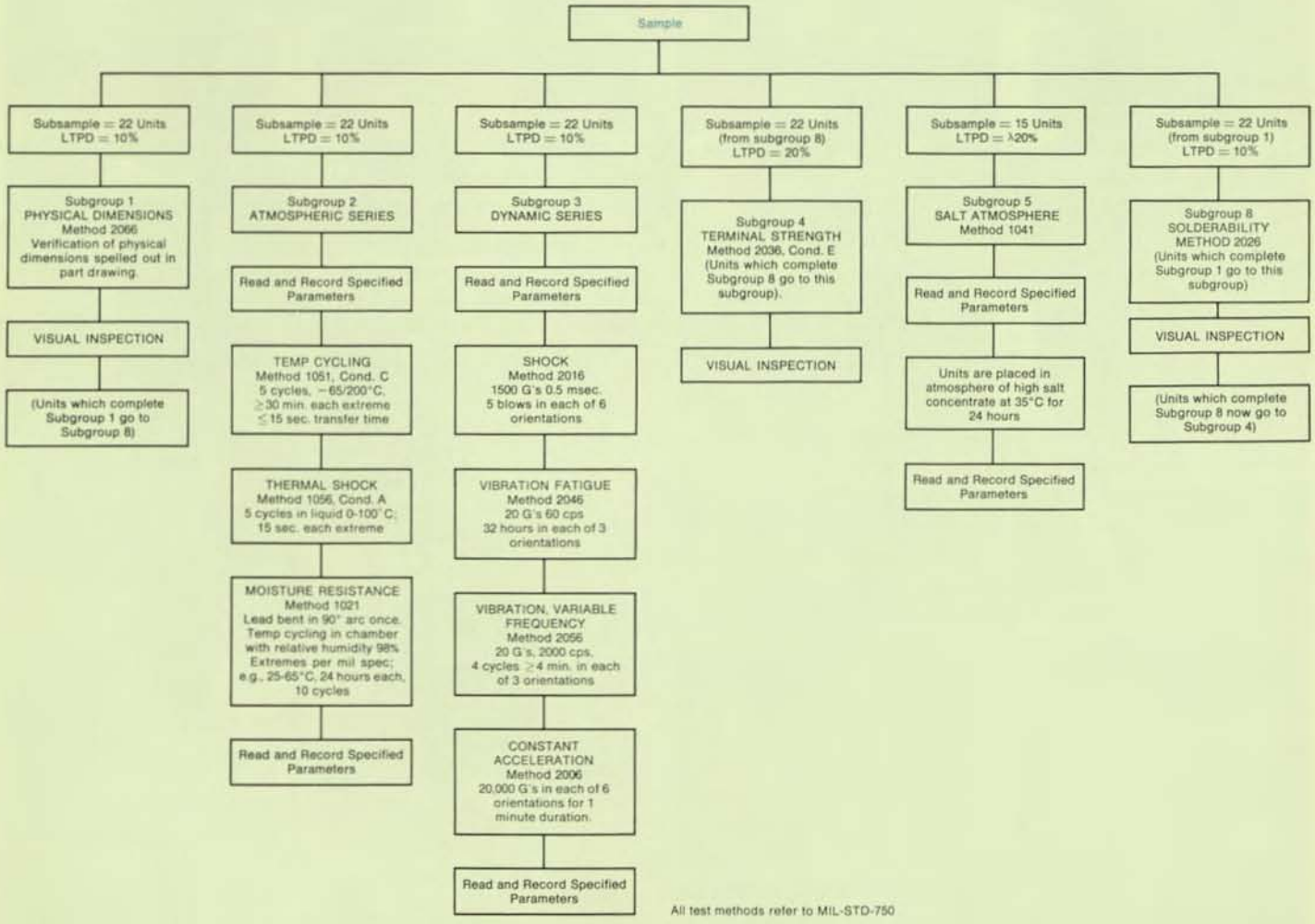
Integrated Circuits

Again in accordance with accepted principles, digital integrated circuit families will be subdivided into groups of similar functional and manufacturing complexity levels. Within each family (TTμL, DTμL, etc.) units will be grouped as gates, binaries, capacitor function, or multi-function elements. Qualification of one element from a group (the DTμL 9930 dual four-input gate, for example) will then qualify all other elements in that group (e.g. , the DTμL 9946 quad two-input gate, DTμL 9962 three-input gate, etc.) from the same manufacturing lot.



LTPD = Lot Tolerance Percent Defective; λ = Failure rate in % per 1000 hours

Figure 4—Group B Life Tests



All test methods refer to MIL-STD-750

Figure 5—Group B Environmental Tests

Burn-In

Three different burn-in options are offered. Two are for 168 hours at full rated power and 25°C ambient temperature for transistors, and maximum rated voltage, 125°C ambient temperature for integrated circuits. Under the first burn-in option, all units are guaranteed to meet Group A electrical characteristics after burn-in. Under the second, variables data is supplied, and percentage changes in key parameters are computed. The third burn-in option is 168 hours HTRB (160°C—75% of BV_{CBO}), with all units to meet Group A electricals after burn-in.

Lead Form (TIP 7-003)

Users of flat package integrated circuits may specify the lead form option, by which the leads of the package are carefully crimped and bent downward into the position in which they will ultimately be used. Jig No. 253 (see Figure 6) is used for this operation, which eliminates lead stress and any possible damage to the package.

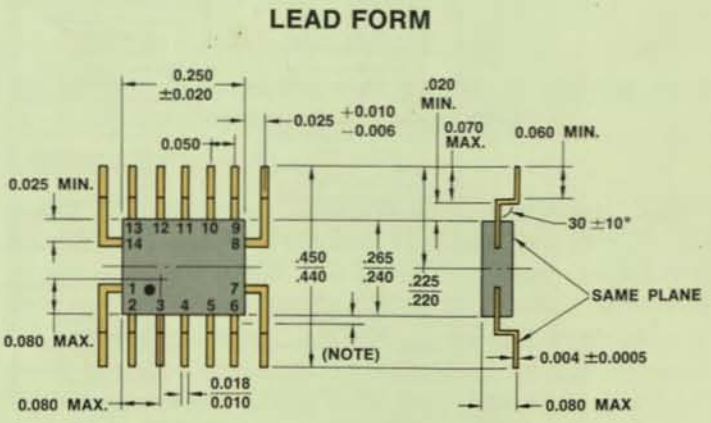
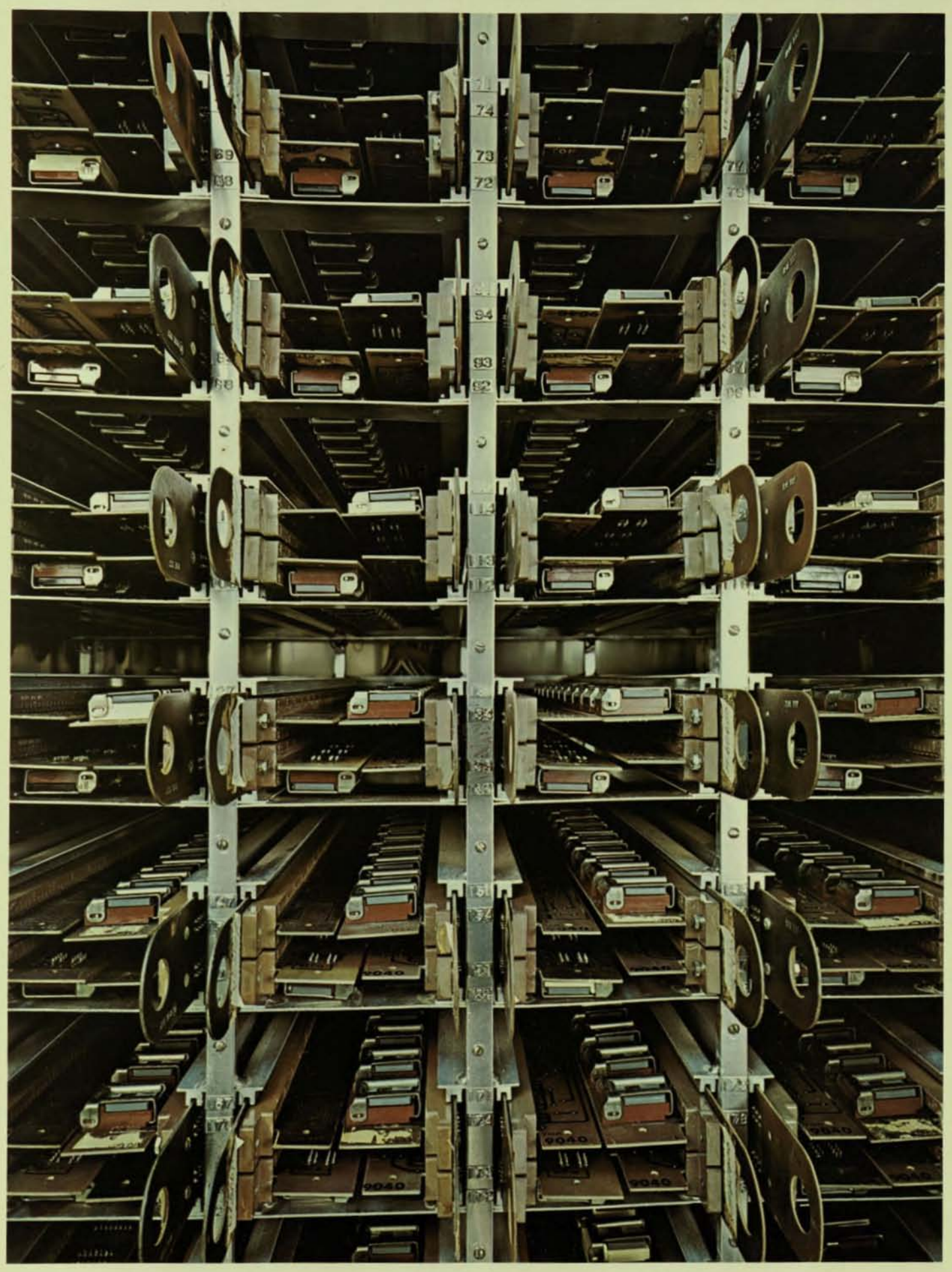


Figure 6

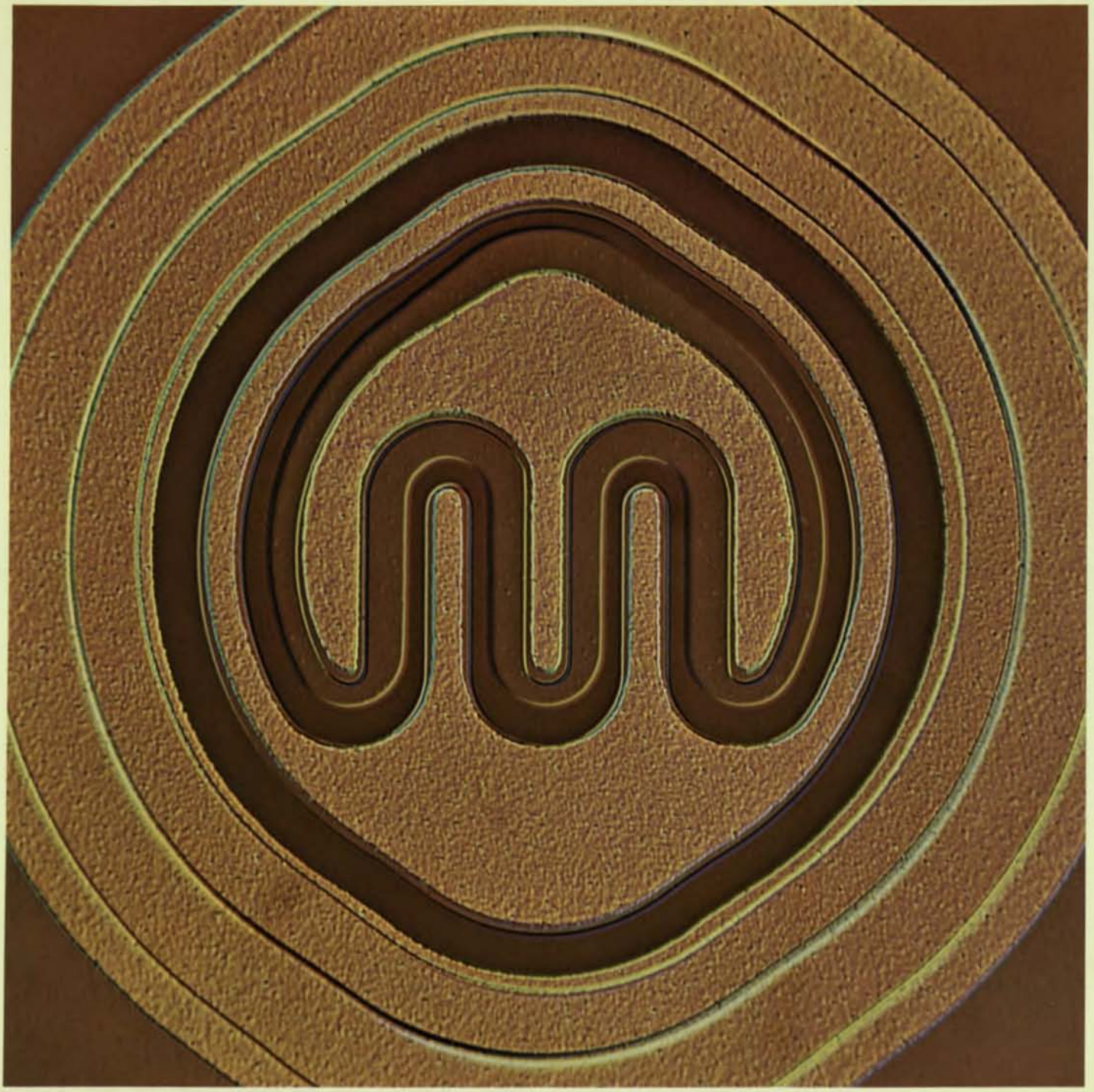


Critical Processes

Reliability is no accident, nor can it be tested into a product; it must be designed in from the start. From the first step in production to the last test in a UNIQUE program specification, the manufacture of semiconductor devices at Fairchild is painstakingly controlled to ensure a product whose reliability is beyond question. The processes used on UNIQUE's special production lines have all been developed through the extensive efforts of the Fairchild Research and Development Laboratories in Palo Alto, California, and are generally regarded as those most critical for inherent device reliability. Even a partial listing underscores the technological leadership for which the company is known and respected. Among those process improvements incorporated in UNIQUE are:

Planar Process
Planar II
Equipotential Ring (EQR)
Collector-Base Metal Overlay
Field Plate
Ultrasonic Bonding

These processes, and many others, listed on page 21, have been adopted for one reason: their contribution to the inherent reliability of a semiconductor device is a matter of record.



The Planar* Process

Most significant of these is the Fairchild-patented Planar process, by which all diffusions are made under layers of pure silicon dioxide, so that critical junctions are never exposed to the risk of atmospheric contamination. As a result, all characteristics which are sensitive to surface conditions—reverse leakage current, breakdown voltage, noise immunity, current gain, etc.—are vastly improved. The device is, accordingly, more reliable. The addition of an epitaxial layer to the basic Planar process results in further improvement of operating characteristics, and still greater reliability.

*Planar is a patented Fairchild process.

PLANAR II

An important evolutionary step toward increased electrical stability was signalled by Fairchild with the introduction of Planar II, a complex and highly proprietary process aimed at controlling the behavior of free positive ions in the protective oxide layer. Concentration of free ions in the oxide can lead to problems that result in unstable P-N junctions and catastrophic failure. Planar II keeps the number of these impurity ions to a minimum by using only ultra-pure materials and improved metallizing and bonding techniques, and by adding a few steps to the basic process resulting in a much purer oxide layer.

In a typical P-Channel MOS-FET (Figure 7a), free positive ions are randomly distributed throughout the oxide layer. If a negative voltage is applied to turn on the device, it repels the free electrons in the N material, forming a P-channel with resultant current flow from source to drain. Initially, such a voltage could be 5V.

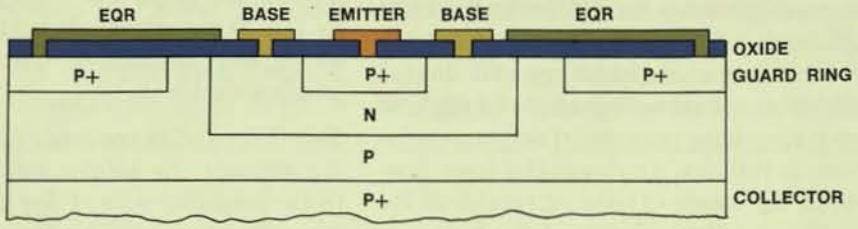
The negative voltage also attracts free positive ions, which concentrate near the metal-oxide interface. When a negative voltage is again applied, a much smaller voltage (about 1V) will form the P-channel, as the ions are already concentrated at the metal-oxide interface (Figure 7b).

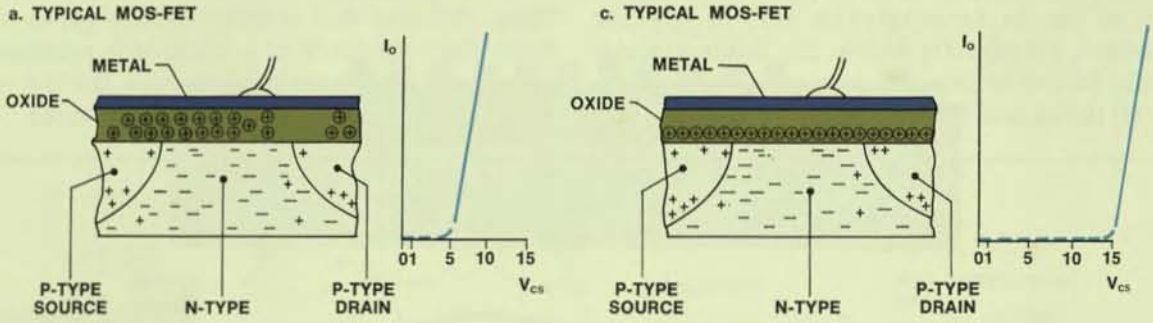
Conversely, if a positive voltage preceded the negative turn-on signal, a much higher voltage (15V) will be required to form the channel, since the positive ions are at the bottom of the oxide layer, and will be attracted to the top (Figure 7c). As a result, the threshold of the device is unstable and fluctuates between 1V and 15V, depending on the polarity of the previously applied signal.

Figure 7d shows how the Planar II process helps to alleviate the problem. In the Planar II device, the number of impurity ions is kept to a minimum, and the effect of their migrations is so small as to be negligible. The result is a threshold voltage that is stable, and a device of increased reliability.

EQR

Closely related to the Planar II process is the use of an equipotential ring (EQR) to prevent ion migration in PNP transistors. The EQR combats the formation of inversion layers (which might lead to channeling and device failure) by reshaping the electrical field distribution within the oxide layer to eliminate the lateral component. The result, again, is increased stability and reliability.





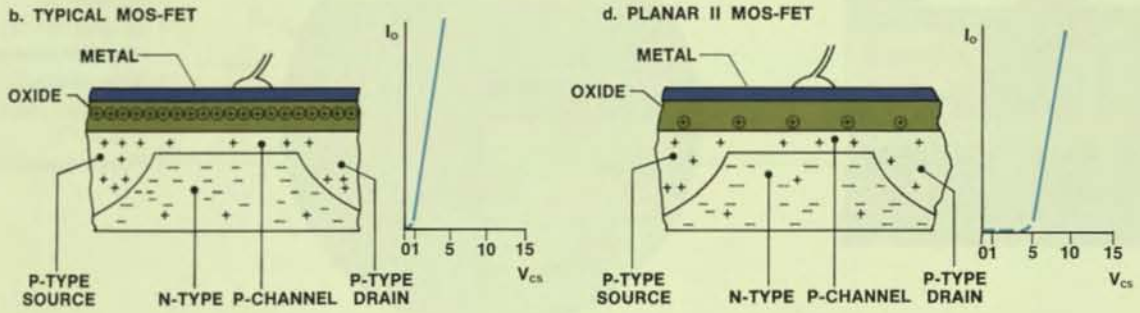
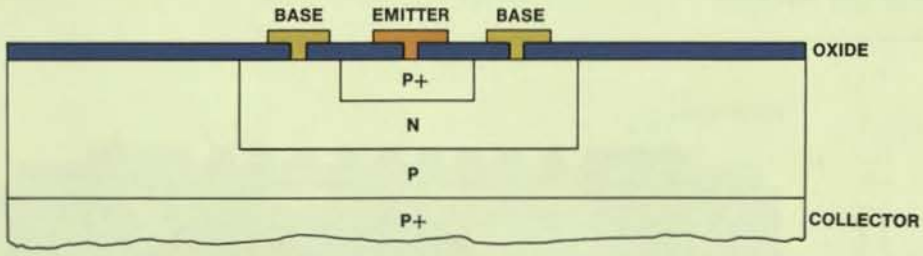


Figure 7



PNP TRANSISTOR

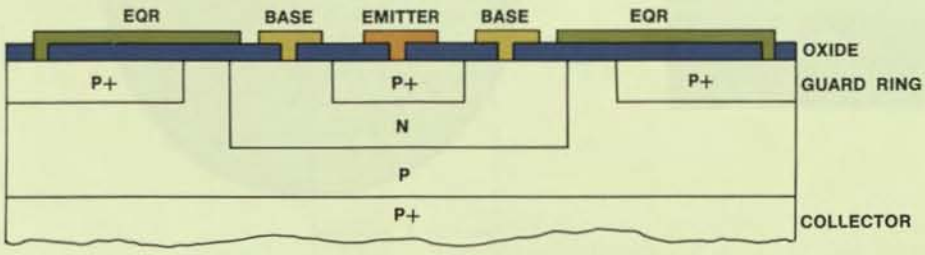


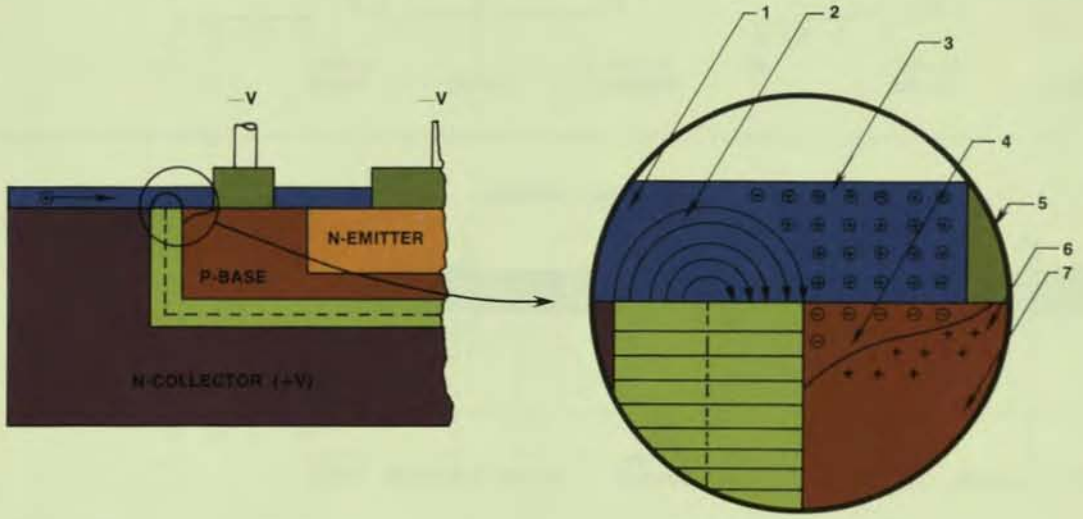
Figure 8

PLANAR II PNP TRANSISTOR WITH EQR

Metal Overlay

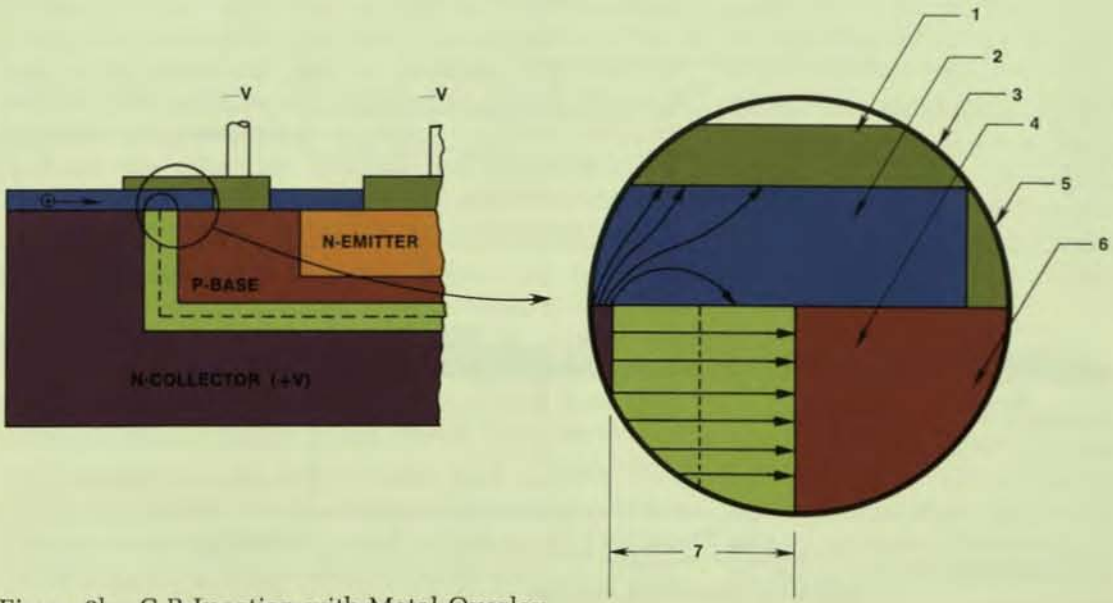
The collector-base metal overlay for NPN transistors is similar to the EQR, and is likewise used to inhibit ion migration, inversion layers, channeling, and device failure. Figure 9a illustrates the development of a channel caused by inverted P-type base material. The reasons for this development are as follows. Any impurity ions (contaminants) present in the oxide (1) are attracted to the base contact (5) by the negative polarity of the base bias for a reverse bias condition. When this migration has drawn a sufficient number of ions to the area of the collector-base junction (3), the total positive charge in that region of the oxide repels the mobile positive majority carriers (6) directly below the oxide surface. The immobile, locked-in negative ions create a net negative charge (4) in the area vacated by the mobile majority carriers. This region, formerly P-type, appears now to be N-type, and there is an inversion layer. Should it progress to the base contact, it will constitute a collector-base short, and, because of the channel, I_{CBO} will represent intolerable levels.

The C-B overlay prevents inversion layers in the following manner. As before, impurity ions are still attracted to the negative pole of the base (5, Figure 9b). However, since the base metallization extends over the C-B junction (3) and is negative, the positive contaminant ions are attracted directly to the metal itself, and the opportunity for them to build up over the junction no longer arises. Thus, the area that inverted before (4) is now stable. Since the occurrence of a channel is predicated upon a pile-up or concentration of charges, the C-B metal overlay effectively eliminates this failure mode.



1. SiO_2 passivation layer.
2. Electric field due to applied bias.
3. Ion pile-up.
4. Inversion due to excess negative charge.
5. Base contact.
6. Repelled majority carriers ("holes").
7. P-type base material.

Figure 9a—Typical C-B Junction

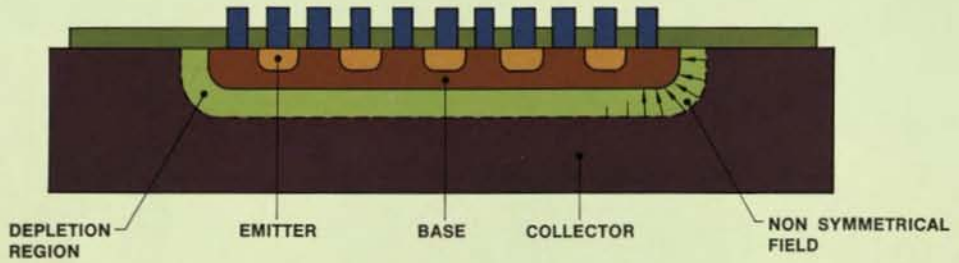


1. Contaminants (ions) in metal overlay, not in oxide.
2. SiO_2 passivation layer.
3. Collector-base metal overlay.
4. Stable area (no inversion).
5. Base contact.
6. P-type base material.
7. Junction depletion layer.

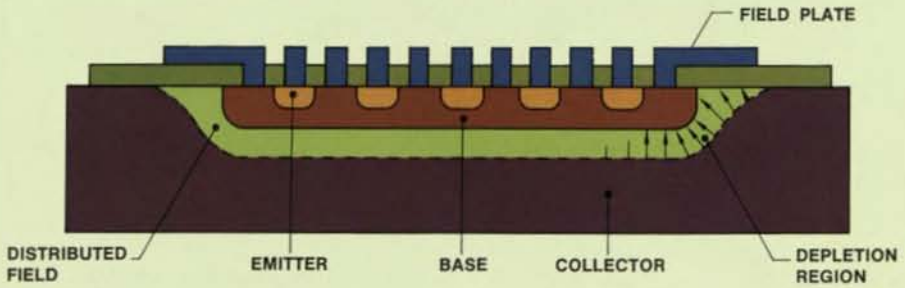
Figure 9b—C-B Junction with Metal Overlay

Field Plate

The voltage breakdown capability of Planar* junctions is somewhat limited by a concentration of the electrical field at critical points along the collector-base junction, occurring under reverse bias conditions. In an effort to distribute the field more evenly throughout this area, the outer peripheral base metallization has been extended to form a "field plate" that covers the entire C-B junction. Voltage breakdown capability is thereby increased.



CONVENTIONAL PLANAR TRANSISTOR



PLANAR TRANSISTOR WITH FIELD PLATE

*Planar is a patented Fairchild process.

Ultrasonic Bonding

Ultrasonic bonding is the most sophisticated bonding technique known today. It incorporates advanced technologies in acoustics and metallurgy to form a bond far more reliable than would be possible with any other process.

All metal atoms with unsatisfied bonds are capable of bonding to other atoms if they are brought into intimate contact. Thus, if two pieces of metal with absolutely smooth, clean surfaces are brought together, the unsatisfied bonds at the surface of each will create a true metallurgical bond between the two pieces.

This kind of bonding cannot occur in nature. There are three barriers that hinder its natural occurrence, and which must be remedied before the desired bond can take place.

1. The most finely polished metal surface is still quite rough on an atomic scale. Typically, there are irregularities with vertical excursions equal to 200 atomic layers on even the smoothest of metallic surfaces. As the attractive force between atoms is inversely proportional to the distance between them, bonding will occur only on the "peaks" of the surface, resulting in a very weak bond, if any.

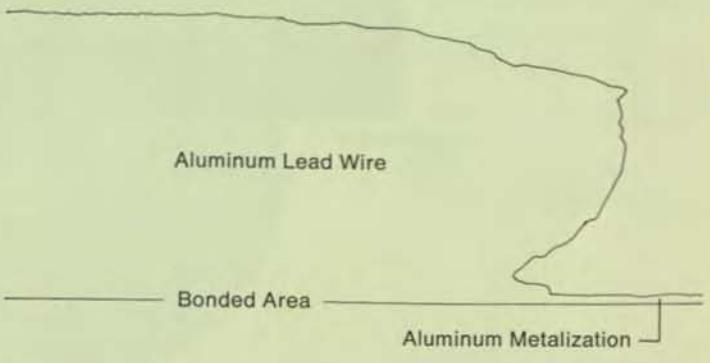
2. The attractive forces of surface atoms attract and hold oxygen from the atmosphere to form an oxide film on the surface, typically 200 molecules thick.

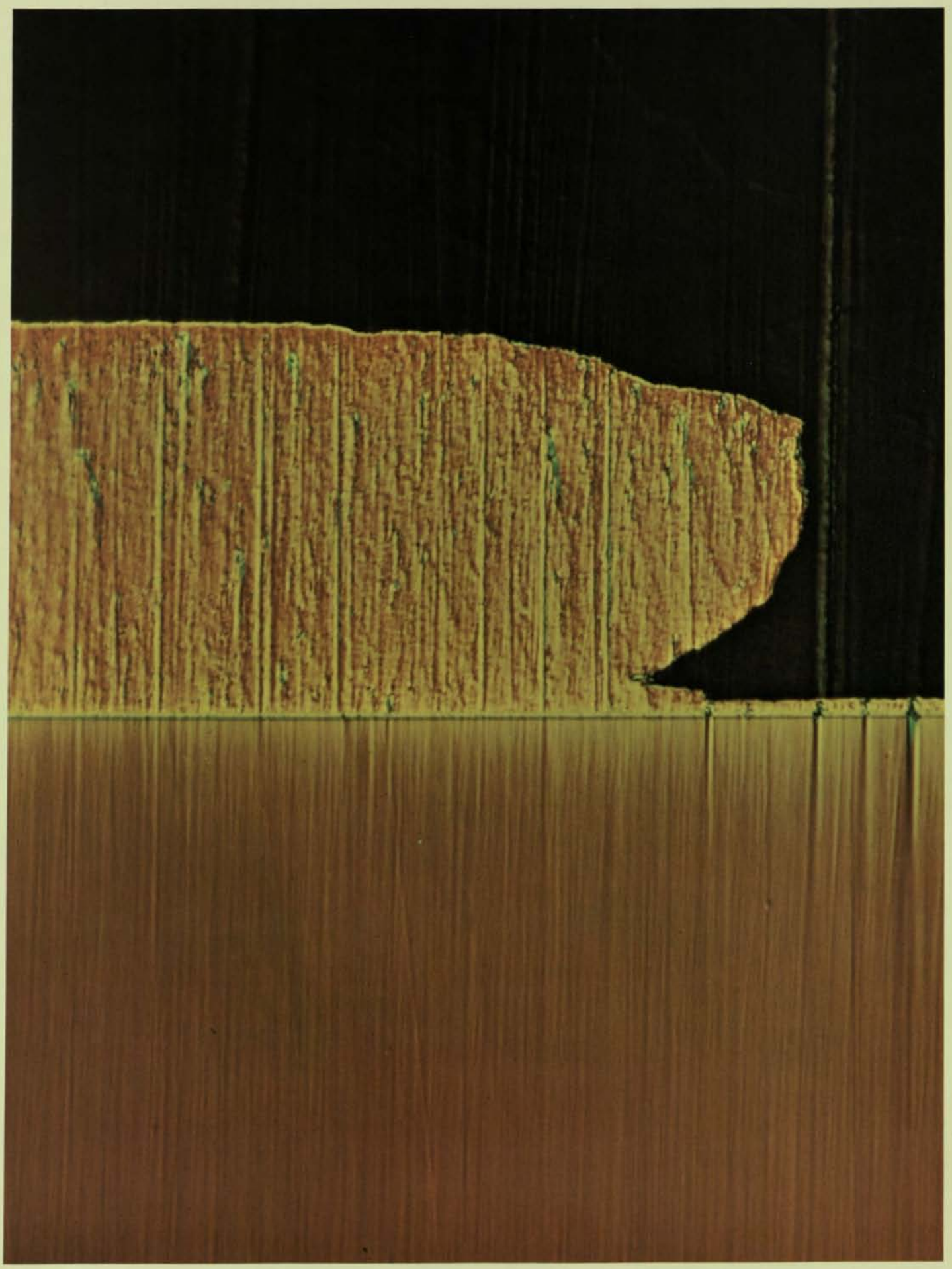
3. The unsatisfied bonds in the oxide in turn attract water molecules from the atmosphere, creating a film of moisture on the surface. While its thickness is dependent on relative humidity, it is never less than 2-3 molecules.

Ultrasonic bonding overcomes all three barriers by plastically deforming the interface between the two metals so that the films of moisture and oxide are dispersed, and the irregular surfaces of the two pieces are made to conform to each other. A large area of intimate contact is thereby formed between the adjacent pieces, and metallurgical bonding takes place.

The advantages of ultrasonic bonding are numerous: there is no contamination from foreign materials; heat generation is negligible; purple plague is avoided; there is little pressure, and the resultant bond is stronger and of smaller mass. Except where package configuration or metallization patterns prohibit its use, this advanced bonding technique is used on all Fairchild products.

750X magnification





Special Forces

State-of-the-art processes and exhaustive testing play an important part in the UNIQUE program, to be sure. But more important is the spirit of the program itself—a function of the people involved in all aspects of UNIQUE, from initial design through production to the marketing of what is, essentially, an intangible item: confidence in the final product. UNIQUE personnel are dedicated to the development of the most reliable devices in the industry. The end result of their sincere efforts cannnot be duplicated. At any cost.

Patent Information

The manufacture of semiconductor devices requires the use of several of the patents listed below—all held by Fairchild Semiconductor.

Patent No.	Filing Date	Description
2971139	6/16/59	Semiconductor switching device.
2981877	7/30/59	Metal-over-oxide interconnection technique.
3013955	4/29/59	Method of transistor manufacture.
3025589	5/1/59	Planar process—the fundamental process used in the manufacture of transistors and integrated circuits.
3064167	5/19/60	Planar construction techniques.
3108359	6/30/59	Double-diffusion process.
3108914	6/30/59	Transistor manufacturing process.
3117260	9/11/59	Junction isolation technique.
3150299	9/11/59	Intrinsic material isolation.
3156591	12/11/61	Epitaxial growth through a silicon dioxide mask.
3158505	7/23/62	Method of placing thick oxide coatings on silicon.
3158788	8/15/60	Dielectric isolation structure.
3183128	6/11/62	Method of making field-effect transistors.
3183129	7/15/63	Semiconductor formation technique.
3184347	7/19/62	Gold-doping technique.
3184657	5/18/65	Nested region transistor configuration.
3191070	1/21/63	Transistor AGC device.
3193418	10/27/60	Semiconductor fabrication technique.
3199002	4/17/61	Diffused lead crossovers.
3204160	4/12/61	Surface-potential controlled semiconductor device.
3212162	3/22/65	Semiconductor fabrication techniques.
3225261	11/19/63	High-frequency power transistor.
3227933	5/17/61	Diode and contact structure.
3243669	6/11/62	Surface-potential controlled semiconductor device.
3244950	10/8/62	Reverse epitaxial transistor.
3260902	6/10/64	Buried-layer epitaxial structure.
3262064	12/3/62	Temperature-stable differential amplifier.
3264493	10/1/63	Semiconductor circuit module for high-gain, high-input impedance amplifier.
3271640	10/11/62	Semiconductor tetrode.
3280391	1/31/64	High-frequency transistor.
3293087	3/5/63	Method of making isolated field-effect device.
3296040	8/17/62	Epitaxial growth through openings in oxide mask.
3303400	7/25/61	Semiconductor device complex.

Licensing agreements with 15 different companies permit them to utilize many of these patented processes in return for royalties and other legal consideration.

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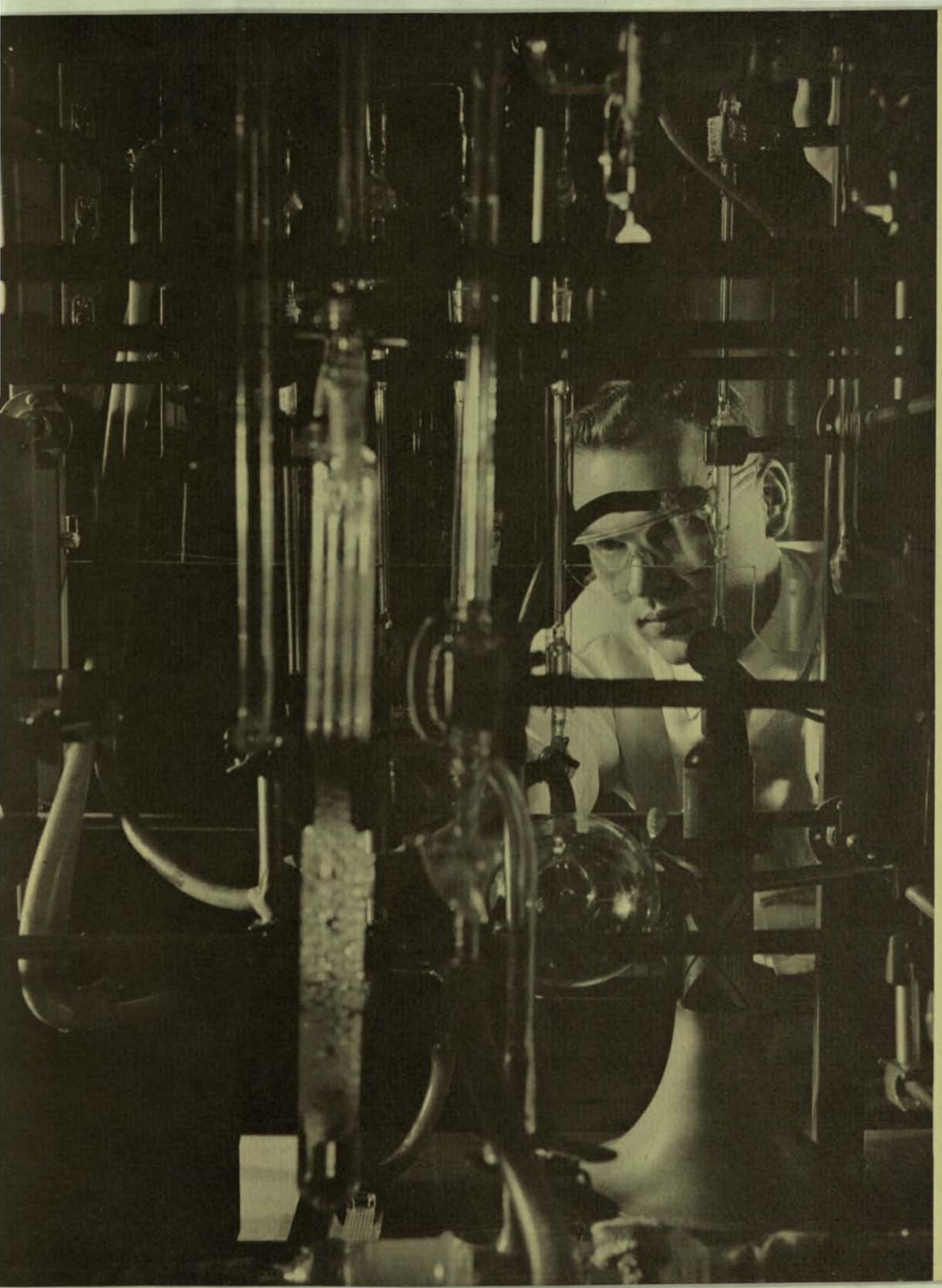
FAIRCHILD
SEMICONDUCTOR

FAIRCHILD
SEMICONDUCTOR ®

FAIRCHILD SEMICONDUCTOR II

This brochure is the second we have produced in the hope of establishing greater familiarity with our company, its products and its people. If you did not receive FAIRCHILD SEMICONDUCTOR I, we would be pleased to send you a copy. It concerned our products primarily, with something of the history of our company and the semiconductor field in general. It dealt with our locations in the San Francisco Bay Area, though these have again expanded and the diode plant which was just begun at that time is now a fully operative facility.

This, then, is an expansion of a theme. The photograph opposite illustrates the direction we have chosen . . . the inter-relationship of people and products. The engineer in the picture is taking readings on the flow meter of a diffusion furnace. Fairchild's mastery of the diffusion process led to its ascent as a major semiconductor manufacturer; its people were the source of that mastery. Their subsequent accomplishments in research, development, and improved manufacturing techniques, have kept us in the forefront of a stimulating, challenging industry.



ALL ABOUT PEOPLE . . .

Jack Sheets is Personnel Manager for the main transistor plant in Mountain View. With his counterparts in the Research and Development Laboratories in Palo Alto, and the Diode Plant in San Rafael, Jack is on constant lookout for "people with a plus." It is a part of his job to recognize the quiet applicant as the man who will some day dream up a Micrologic element, to analyze the capabilities of new talent and to channel it towards successful productivity.

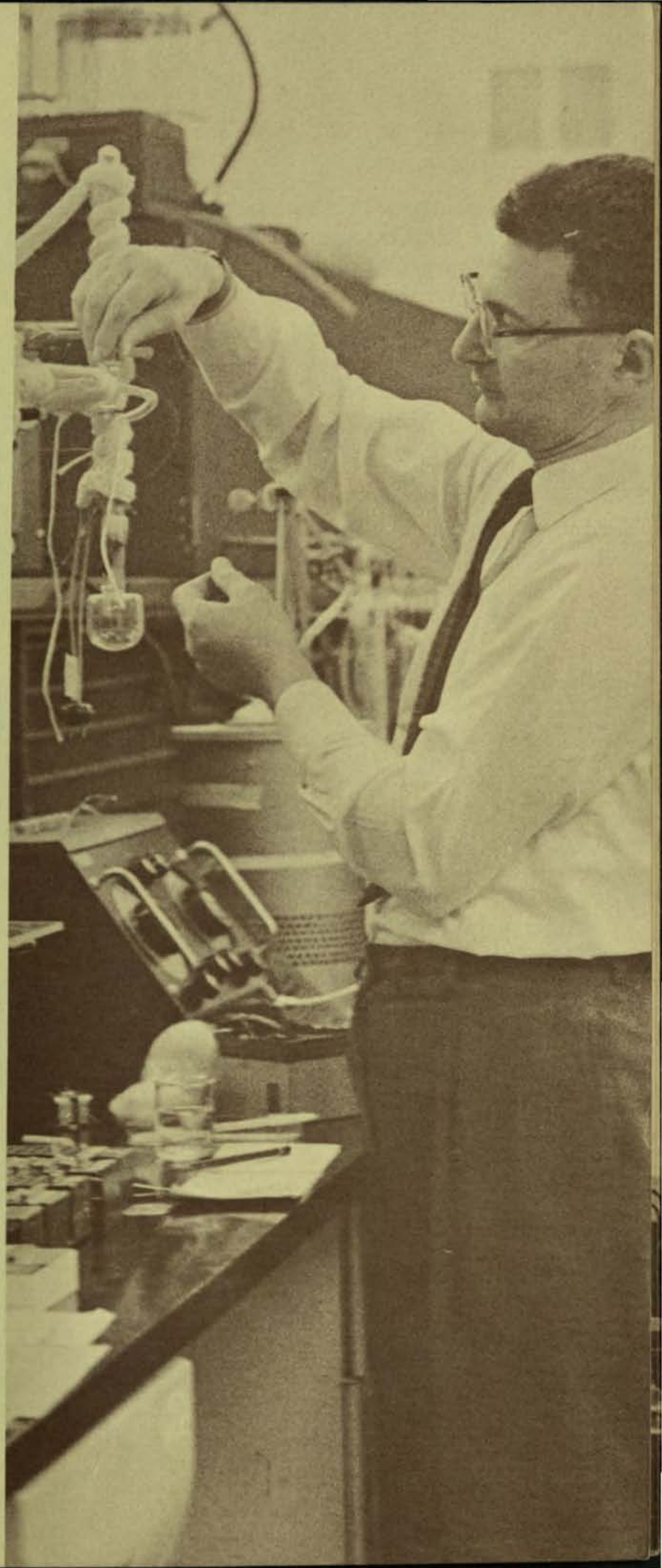
In addition to administering the varied personnel functions of a growing company, Jack constantly keeps his finger on the pulse of in-plant activity. He knows his people. His belief is a personal and professional conviction that that's what it's all about.

WITH AN ENDLESS CURIOSITY

Pride in accomplishment could be a deterrent if it weren't for curiosity. Dr. Bernard Rabinovitch of our Research and Development laboratories could easily be proud and rest on his laurels. At sixteen he was blitzed out of his native London. He proceeded with distinction through the University of London, Cambridge, Harvard, The Illinois Institute of Technology and The University of Chicago.

Life in the academic world was good; there was much cause for contentment. But curiosity and the challenge of a dynamic company in a new and competitive field drew him into industry.

He is not the "typical" man of science. His curiosity and innate abilities have been refined through intense study and application to lead him towards a better understanding of technological processes, old problems and new phenomena. He and his associates, nearly twenty percent of Fairchild's total employment, provide much of the impetus to future growth through the development of ever new, ever improved products and processes.

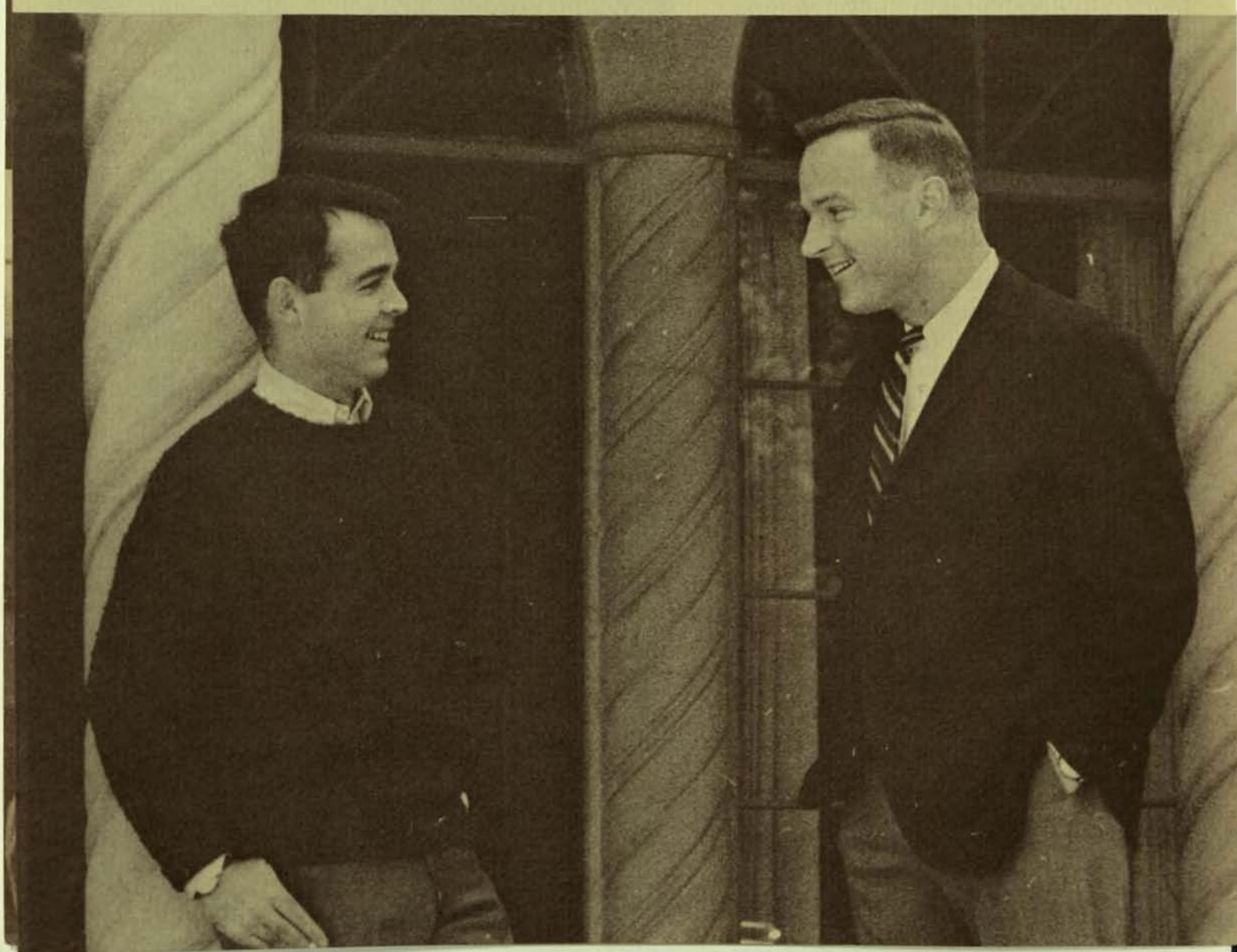


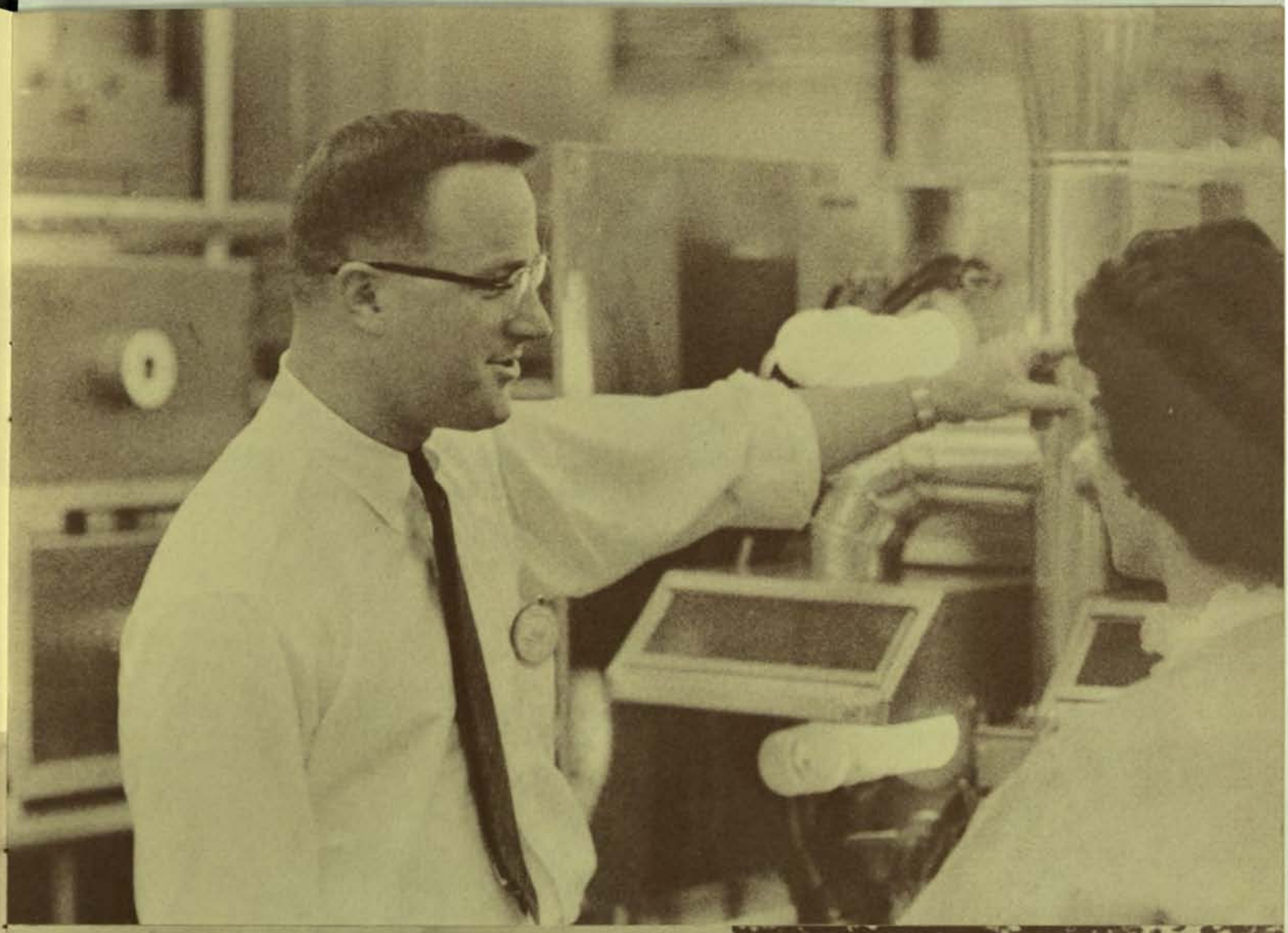
A MAN OF MANY PARTS

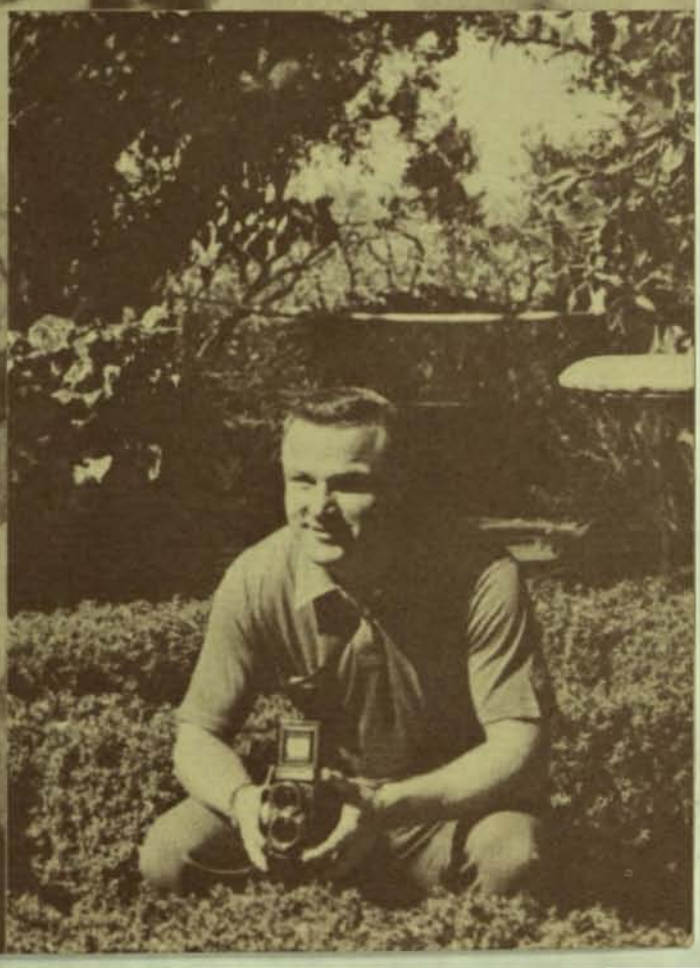
Richard Ellington Cole received his B.S. in Chemical Engineering from Purdue. On the completion of his M.B.A. from Stanford, he joined Fairchild as a Production Management Trainee. With a thorough background in all phases of wafer fabrication . . . masking, diffusion, and die sort . . . he soon progressed to Production Supervisor and has recently been appointed a Product Engineer.

During his two years of duty with the Navy, he served as a Lieutenant j.g. and participated in the Bikini H-bomb tests and as Navigator on a destroyer in Formosa waters. He is a personable man, well liked by his colleagues and respected by those who report to him. The fact that he is an investor in the stock market further emphasizes his serious nature and concern for the future.

But Dick has a lighter side, too; he is extremely active. He is an enthusiastic bridge player, Captain and Coach of the Fairchild basketball team, Coach of both the men's and girls' softball team, a golfer, swimmer, pianist, and plays tennis to boot. His energy, complemented by his sense of direction integrating his many parts into a purposeful, unified whole, has keyed his strong advance.







WHO KNOWS NO HANDICAPS

Donna Sue Brown is a stand-out operator in a stand-out group. She is one of the five deaf-mute girls who work on the production lines at Fairchild.

Donna's performance in die-attach is far above average. She has several reasons for working, all involving her family. She wants to help her husband; they have two children and are buying a home.

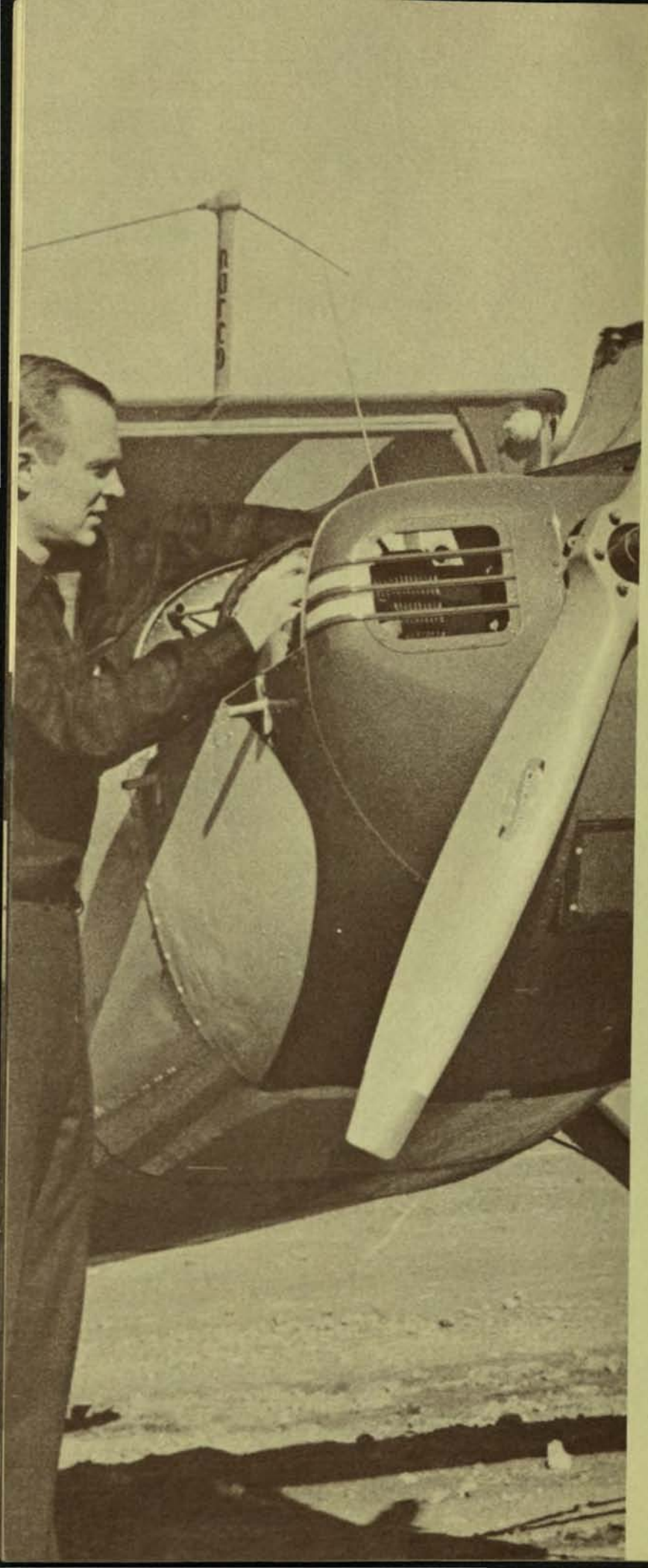
She has no problem communicating and does not know the meaning of the word "handicap." Using her hands gives her great satisfaction. When she isn't "talking," she sews.

WHO KNOWS NO BOUNDARIES

When Bill Bailey, Transistor Product Engineer serving as consultant to the Manufacturing Manager, was assigned for six months to Societa Generale Semicondutorri, Italy, it was truly a case of "Bill Bailey comin' home." An avid and accomplished skier who has tried almost every major ski resort in the Western World, Bill bypassed Italy on his latest European skiing tour. He has long wanted to return to fill the gap.

At S.G.S. he will serve as Senior Process Engineer to help our Italian affiliate set up production lines for silicon Planar devices. Bill is well versed in all phases of transistor manufacture. At Mountain View he has been trouble-shooting on the line to improve processes and production yield.

Even his outdoor life knows no boundaries. When the skiing slopes are dry, he is climbing them. He enjoys hiking and camping. His swimming has extended to body surfing and skin diving.



WHO REACHES HIGH

Flying, one of his many hobbies, symbolizes Dick Fouquet's goals in life. His background, filled with accomplishment, is evidence of his climbing spirit. However, attainment without contest is not in keeping with his nature; he wants to be on the winning team most especially when the other side offers serious competition.

At Harvard he received his B.S. in Chemistry and at Stanford his M.B.A. He was a Lieutenant in the Navy, assigned to Far Eastern Intelligence. He speaks four languages, is a creative color photographer, and plays classical piano. He competed in National Intercollegiate swimming championships. Like many another Fairchilder, he is an enthusiastic skier.

At Fairchild, Dick holds the title of Senior Industrial Engineer. All production processes, other than assembly, in the manufacture of transistors are his responsibility. His task is to assist production in obtaining the highest quality transistors for the lowest cost. It calls for constant effort to increase yield and to improve manufacturing efficiency. It is the type of challenge on which he thrives.


ACIDS

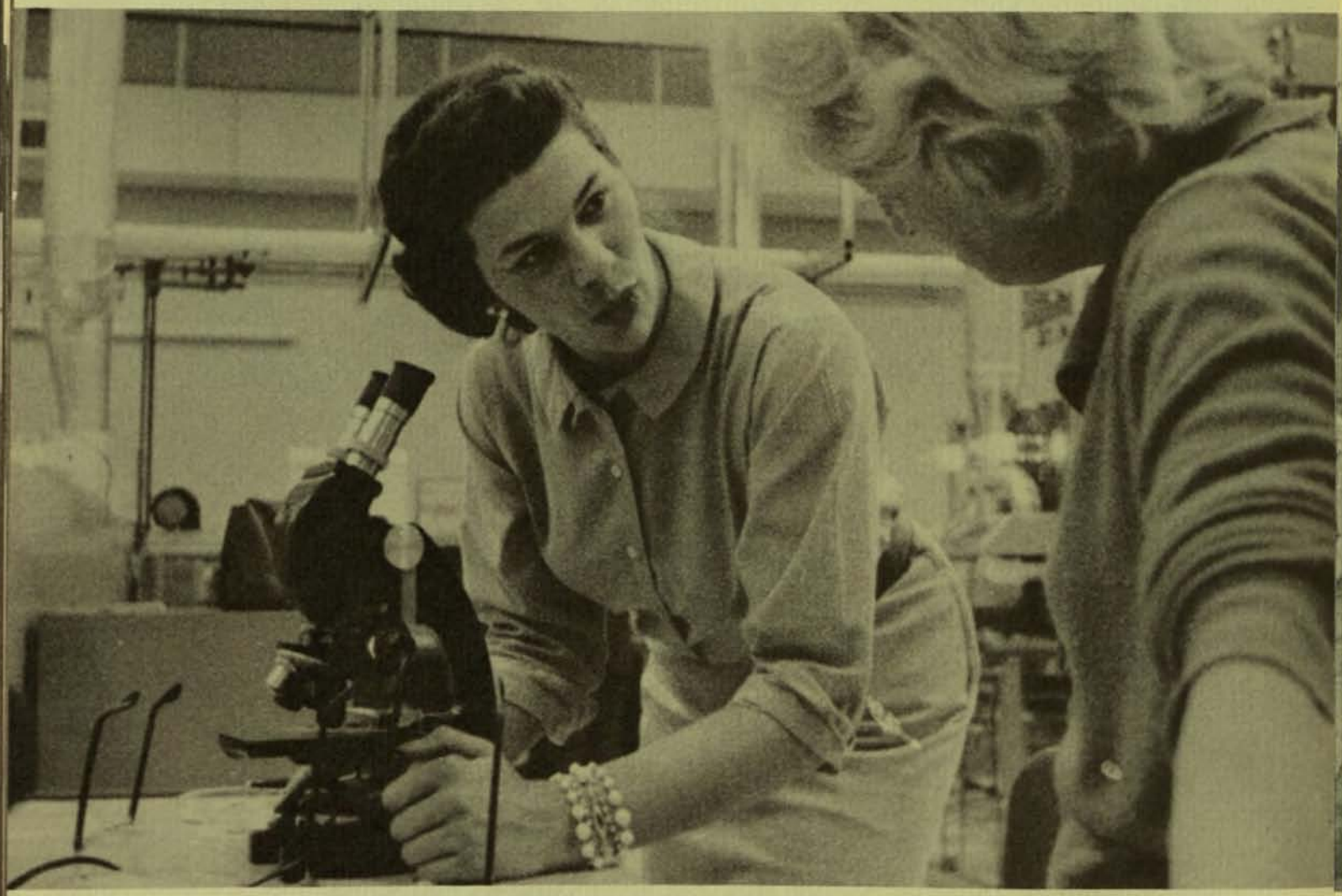

1340
ICBO
Atlantis
IEDO

FROM OTHER EXPERIENCE . . .

Lee Steward had previous experience as a bookbinder, stenographer, chorus girl and private investigator. Yet she longed to work in electronics because it was a new industry that stirred her imagination with hints of a stimulating future. She applied for employment at the Diode Plant in San Rafael. In her application she listed as related experience "Plugging in the electric percolator."

She was among the first dozen people hired at the Diode Plant when her aptitude revealed high manual dexterity, keen vision and intelligence. She learned to perform every phase of manufacture and was soon promoted to Supervisor-Inspector in Quality Assurance. Her technical ability is rated high. Her efficiency draws a great deal from her compatibility with those whom she must assist and instruct.

Lee lives with her daughter in a lagoon apartment in San Rafael. They often fish from the porch and take a boat to go shopping, to bowl, to eat out or to explore the lagoon and canals. Her leisure is occupied by reading, playing chess and making mosaics. Lee's versatility in both work and in play stems from her unbounded interest in the new, the unknown, the stimulating.

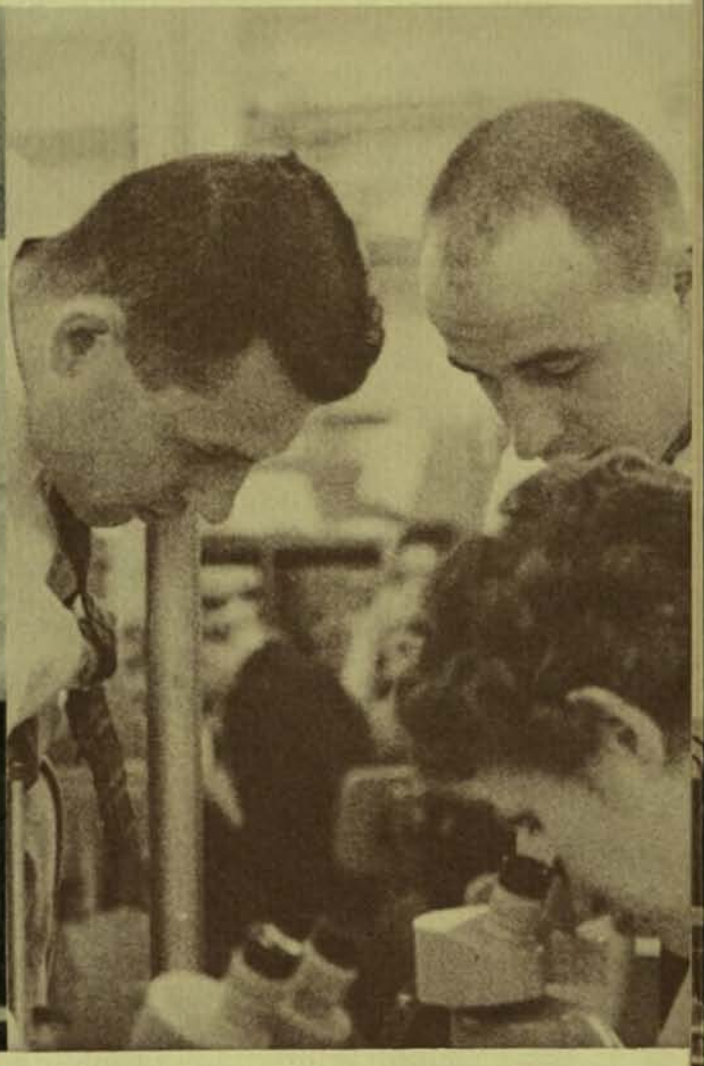


. . . ASSIMILATION

Jack Ehlers has always taken advantage of his experience; by analysis and planning he has been able to extract the maximum benefit. This trait took root during his Boy Scout days when he was an active Eagle Scout. He doesn't count on luck or wait for something to happen. Jack makes things come to being, and also makes certain that there is adequate activity during his leisure as well as working hours.

He made a careful survey and a trip from Rochester, N.Y., at his own expense to explore his future in the Bay Area. It brought him to Fairchild. He began as Pre-Production Engineer and Administrator. He received many and rapid advances. Presently he is manager of Reliability Engineering. He coordinates a factory-wide reliability improvement effort for the Autonetics Minuteman contract.

In his spare time he likes to play tennis, enjoys woodworking and listening to Beethoven. Jack also attends night school on a Certificate Program for Business and Management limited to technical personnel. He is also working toward an M.B.A. With his wife, he works on mosaics, goes camping and skiing; Betsy plays the guitar while he plays the recorder, a 16th Century flute. Series tickets to the theatre, actors workshop and concerts fill out their busy schedule.

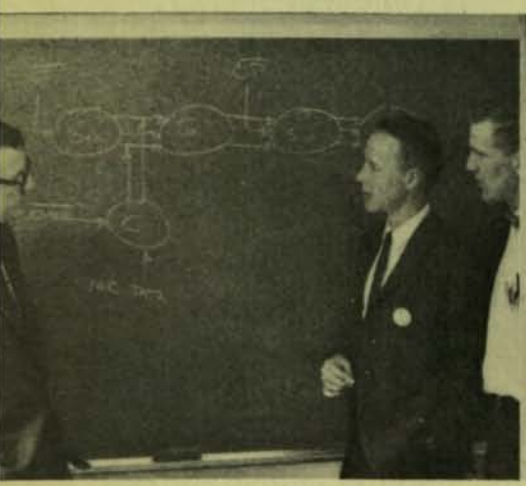


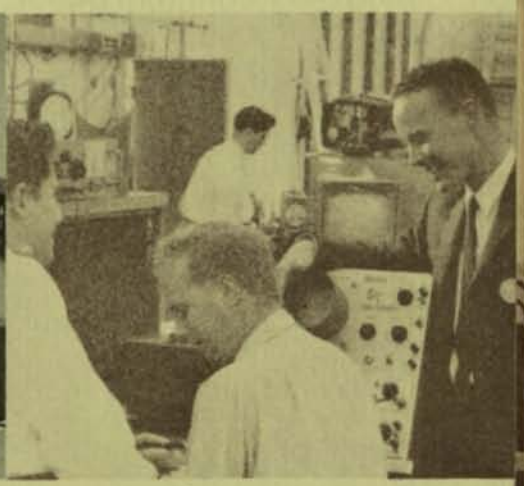
AND A DRIVE TO CONTRIBUTE

Dick Anderson is the youngest (26 years old) of the team of engineers who work on the development of Micrologic. His drive to contribute is equal in fervor to his curiosity of the unknowns in electronic technology.

Fairchild's research program required men with electrical engineering background in computers. Dick had studied at Stanford on a Halloway N.R.O.T.C. Scholarship. He received his M.S. degree and was commissioned Ensign, U.S.N. His Navy assignment took him to Washington where, in the Department of Defense, he obtained the experience in computer logic design required by the Micrologic Development Program.

His serious and technical mind is complemented by his love of skiing and folk dancing. His drive to serve is carried beyond professional considerations. He has become an active member of the Sierra Club, dedicated to preservation of the natural beauties in the Sierra Nevadas.



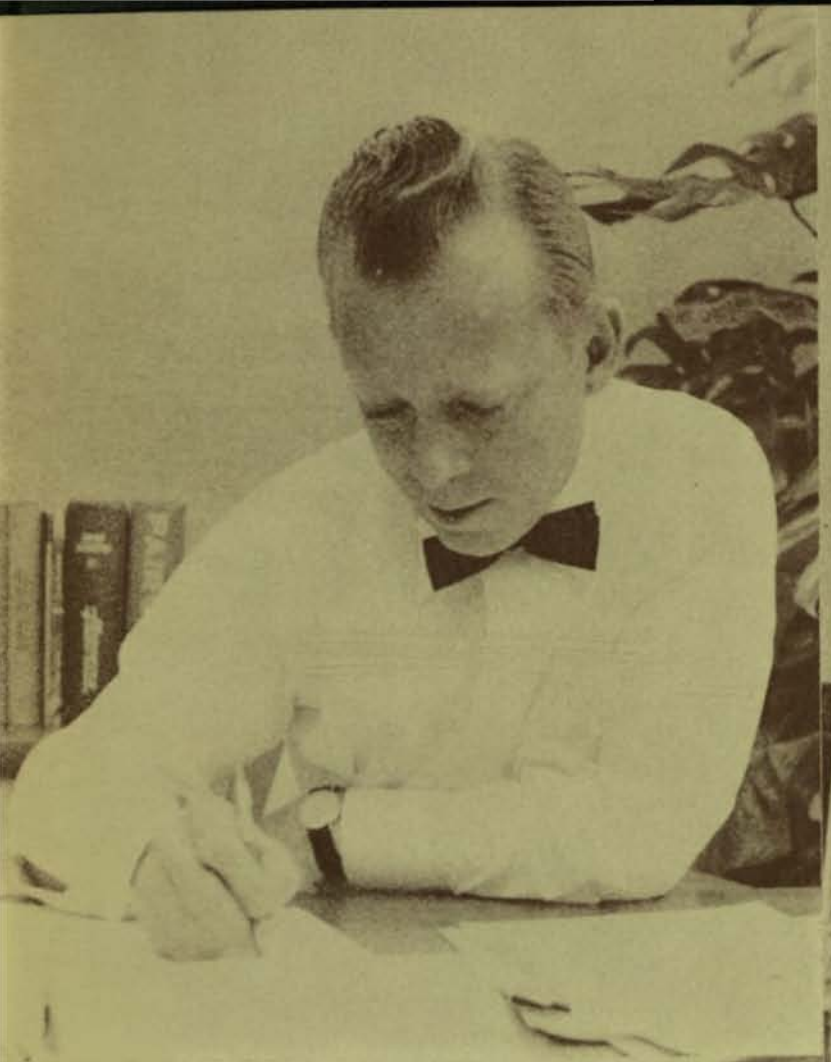


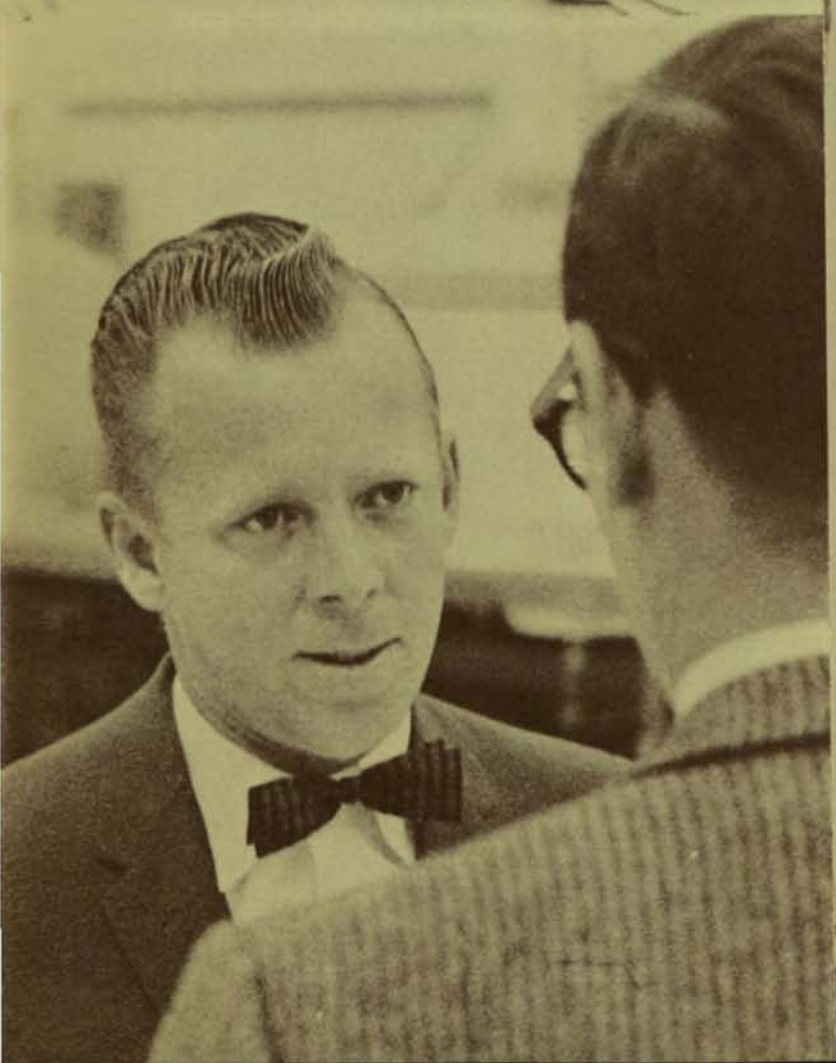
A MAN OF ENERGY

Don Rogers has been Diode Sales Manager since Fairchild began marketing the devices early in 1960. Prior to that time, he was Western Regional Sales Manager and one of Fairchild's star salesmen. According to Don, it was easy.

Don's lifelong love of the sea is reflected in his sailing ability, and in the location of his home. At the top of Tiburon Hill, its glass walls overlook San Francisco Bay, the Pacific Ocean directly through the Golden Gate, and offer a fantastic view of San Francisco's nighttime skyline across the waters.

He is constantly on the go. A favorite sport is "wearing out the young ones" on customer field trips. But he has times of solitude as well. Playing the electric organ at home with his family and occasional moments of just looking at the view renew the energy which has earned him the reputation of a human dynamo.





ALL ABOUT PEOPLE WITH AN ENDLESS CURIOSITY. A MAN OF MANY PARTS WHO KNOWS NO HANDICAPS, WHO KNOWS NO BOUNDARIES, WHO REACHES HIGH. FROM OTHER EXPERIENCE, ASSIMILATION AND A DRIVE TO CONTRIBUTE. A MAN OF ENERGY.

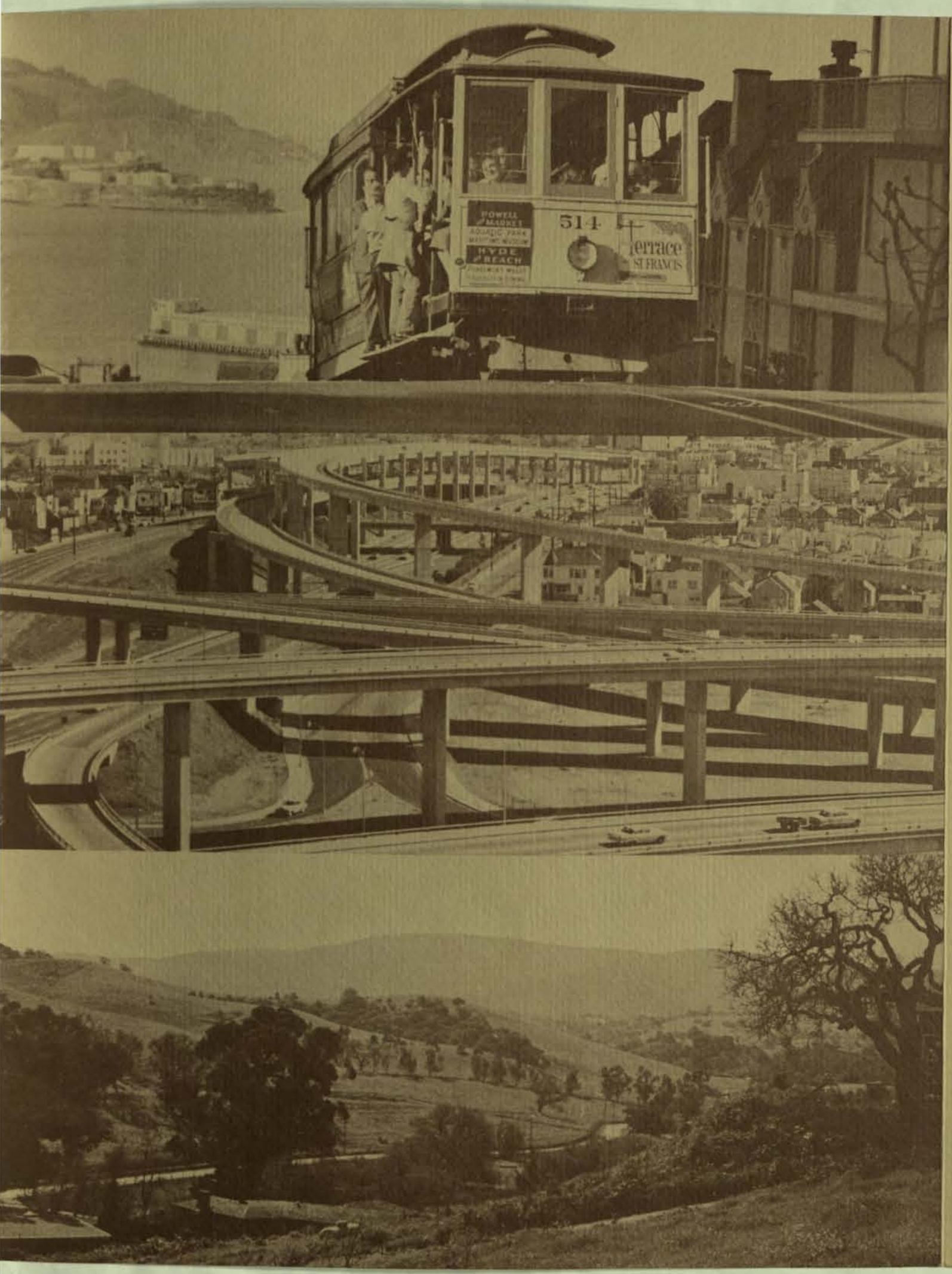
Such is a composite picture of "the Fairchild man." It has been illustrated through but ten people. It is composed of the 1500 who pursue their craft in a corporate endeavor.

The results of their labors are Fairchild semiconductor products; transistors, diodes, Micrologic elements . . . and now transistor test equipment. The semiconductor devices are all of the highest order of diffused silicon. The test equipment was developed because there was none available capable of testing the advanced devices we produce. Quality and reliability are the essence of our pride in our products.

It is all a reflection of people; people of ability, people who care, people "with a plus."

MICROLOGIC

FAIRCHILD SEMICONDUCTOR CORPORATION
545 Whisman Road / Mountain View / California
YOrkshire 8-8161

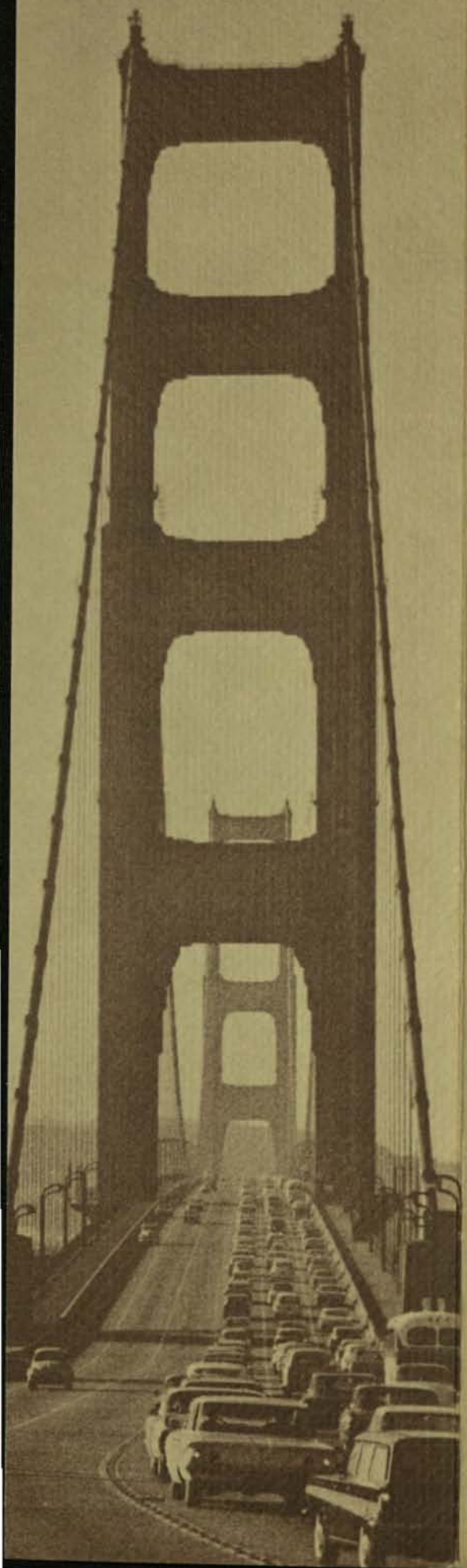


The San Francisco Bay Area is the home of our people. It is warm, vital and progressive; it has international allure. Our environment is rich in natural beauty.

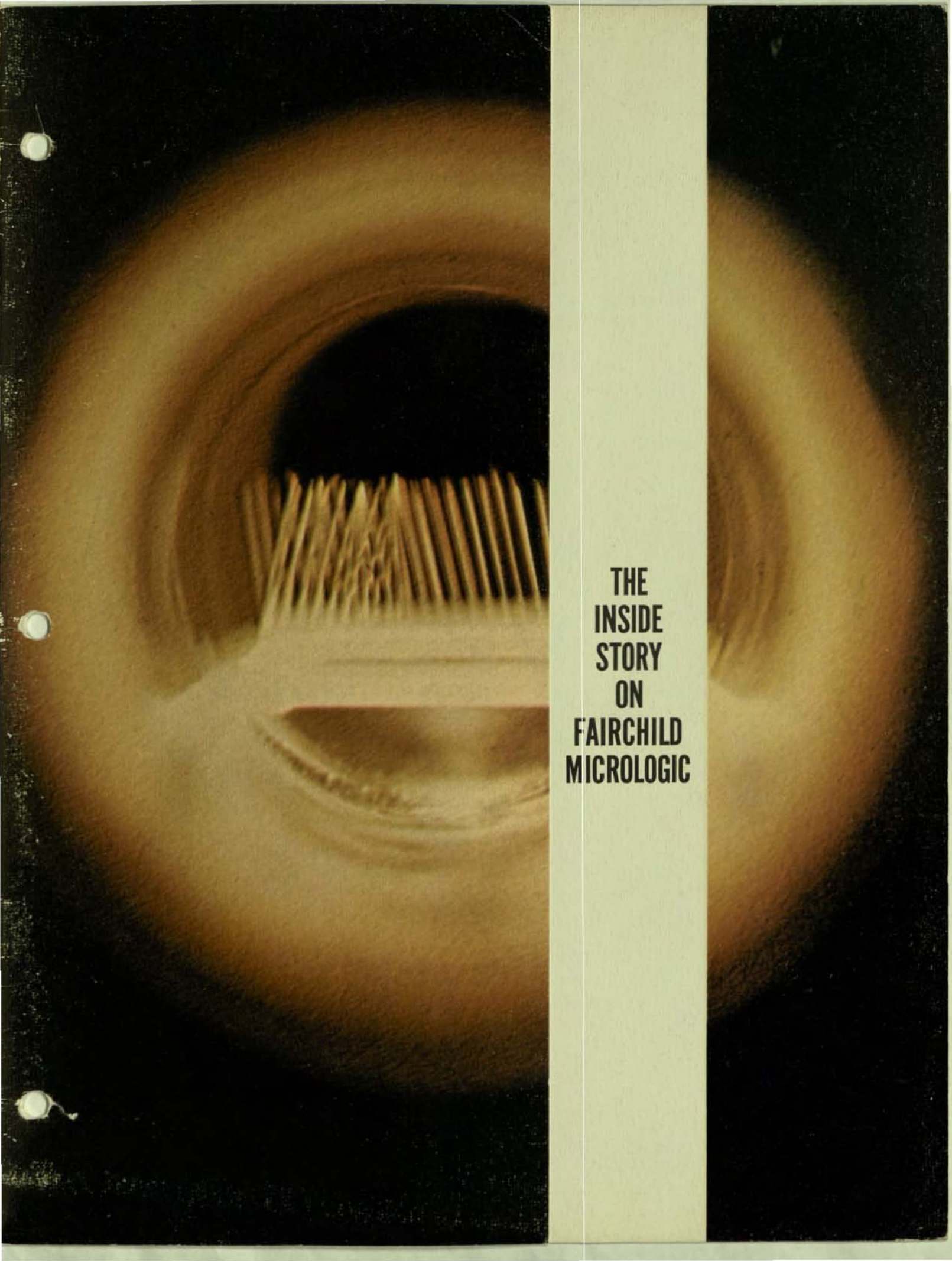
The Golden Gate Bridge is a link between our San Rafael and Peninsula facilities. The Alemany intersection is the gateway to the Peninsula area. We are protected by rolling hills.

The post-war industrial growth of this area has been phenomenal; it has taken a strong lead in electronics. Fairchild Semiconductor Corporation was founded here, grew here, and is now one of the chief technological, industrial attractions.

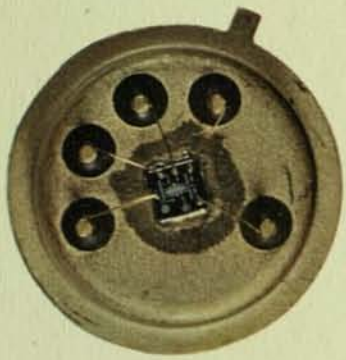
CREATIVE ENTERPRISE LITHO IN U.S.A.

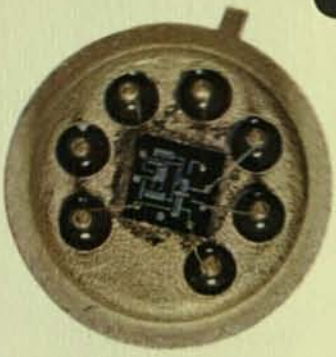


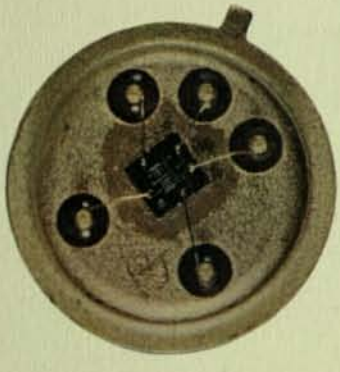
GINGER



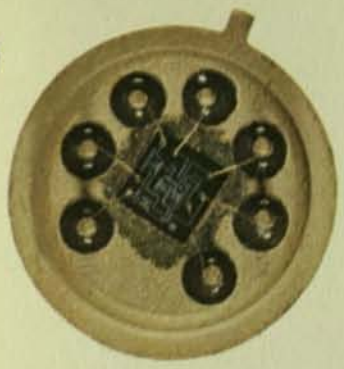
THE INSIDE STORY ON FAIRCHILD MICROLOGIC







ACTUAL SIZE

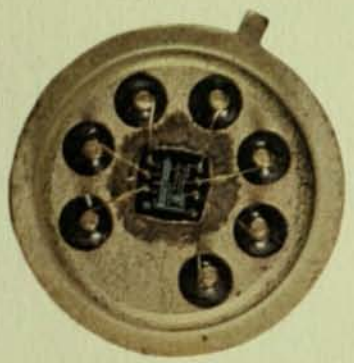


Micrologic elements are a compatible set of miniature logic circuit blocks, each built into a single, monolithic chip of silicon about 1/16 inch square. Micrologic circuits are a modified form of DCTL — direct-coupled transistor logic. DCTL was chosen for five reasons: (1) fewest number of components, (2) fewest kinds of components, (3) non-critical component values, (4) low power consumption, and (5) low supply voltage.

This family of functional elements can be used to fabricate a low cost, highly reliable computer logic section using no other components. They will operate at 1 mc (50 nsec stage delay) clock rates over a temperature range of —55° C to + 125° C.

This brochure will guide you through the manufacture of a typical Micrologic element — the Half-Shift Register — from the crystal to final inspection. The story is told for just one reason: it demonstrates Fairchild's production capabilities in the field of integrated circuitry.

THE INSIDE STORY ON FAIRCHILD MICROLOGIC

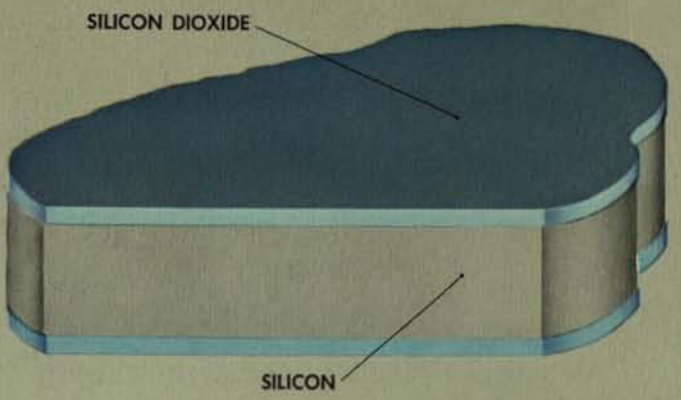


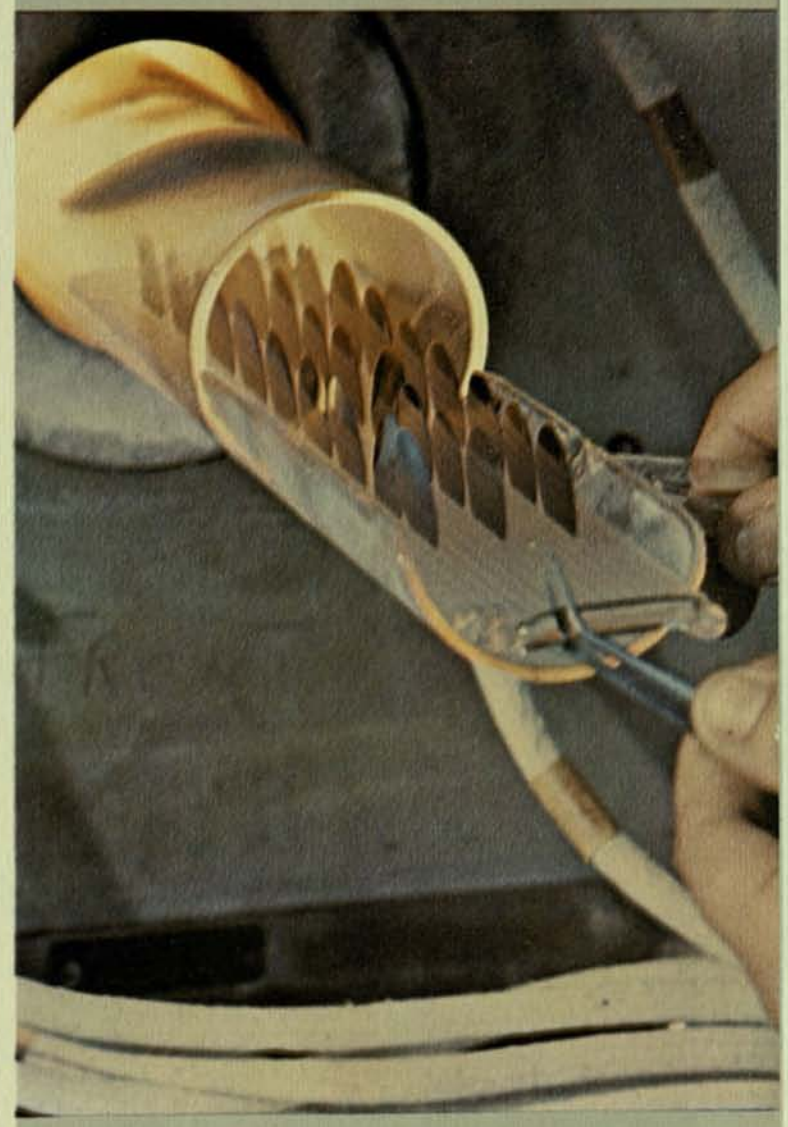
CRYSTAL GROWING

The starting material for Micrologic elements is the same high-purity silicon which is grown by Fairchild and used in its transistor production. The crystals are carefully selected for low dislocation and imperfection counts of the crystalline structure. The silicon crystals are grown by the Czochralski method: a small perfect seed crystal is lowered into molten silicon, and slowly pulled out to form a crystal about six inches long and one inch in diameter. For Micrologic, the crystal is grown with a phosphorus impurity to make it n-type.

CUTTING AND LAPPING

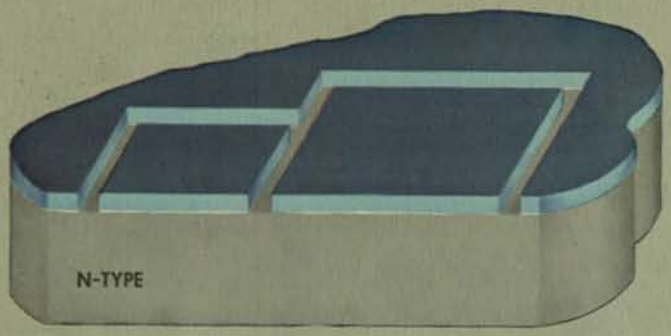
A diamond saw is used to cut the crystal into wafers, approximately eight thousandths (.008) of an inch thick. Each wafer is then lapped flat, using very fine grit abrasive. Next, a chemical etching results in a final thickness of about three thousandths inch (.003), and a smooth shiny surface. These steps are the same as those used in the preparation of Fairchild Planar transistor wafers.

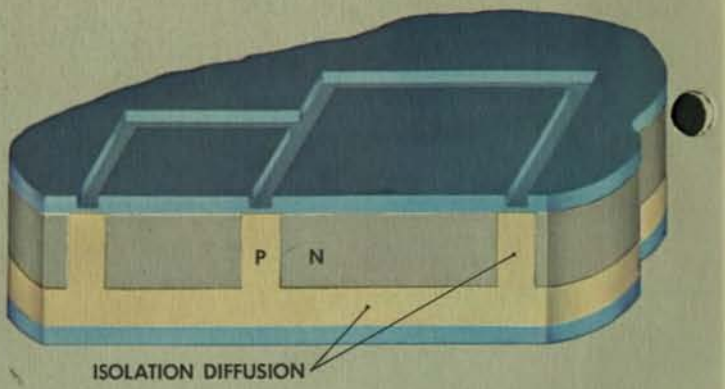


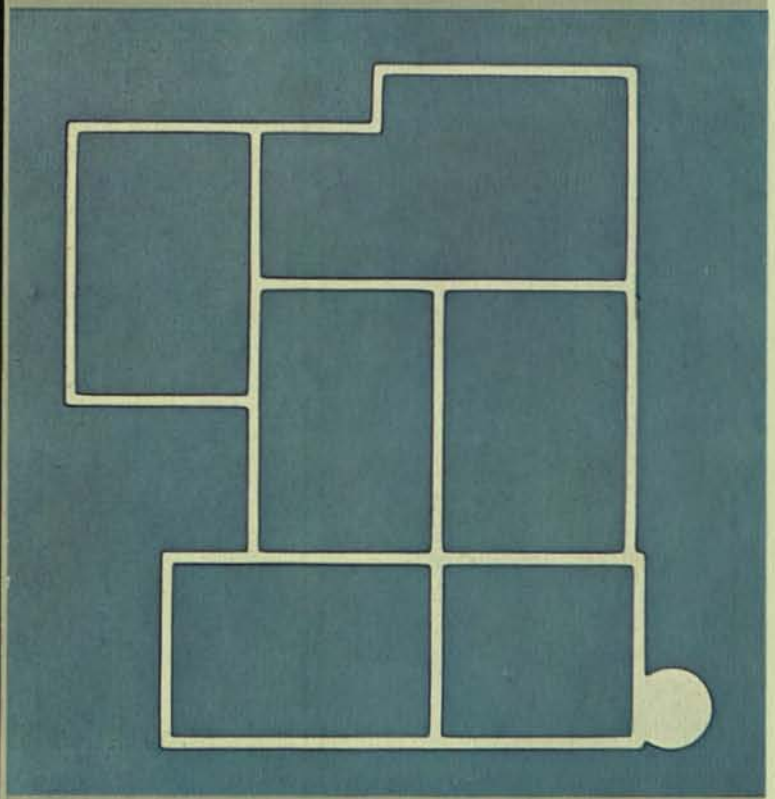


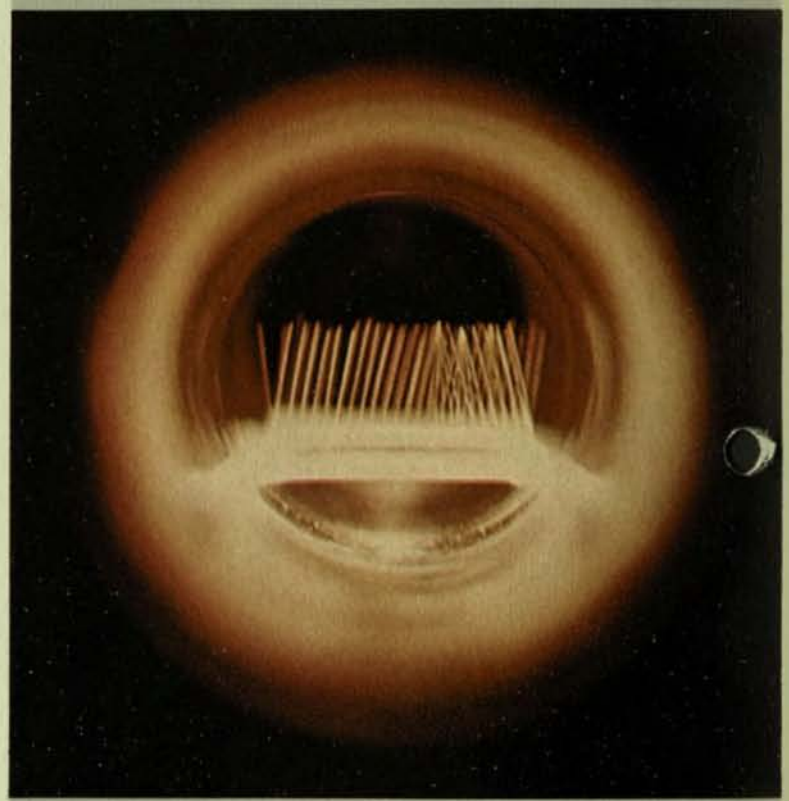
OXIDE GROWTH

Many wafers of silicon — representing thousands of potential Micrologic elements — are placed into a furnace containing an oxidizing atmosphere at 1200° C. Oxygen penetrates the crystal lattice at the surface of the wafer and combines chemically with these surface silicon atoms to form the inert, stable compound SiO_2 (silicon dioxide). Through this process, standard at Fairchild, the silicon wafers are virtually encapsulated and the surfaces are passivated. This one step — the beginning of the planar process — is the key to reliability and production economy.







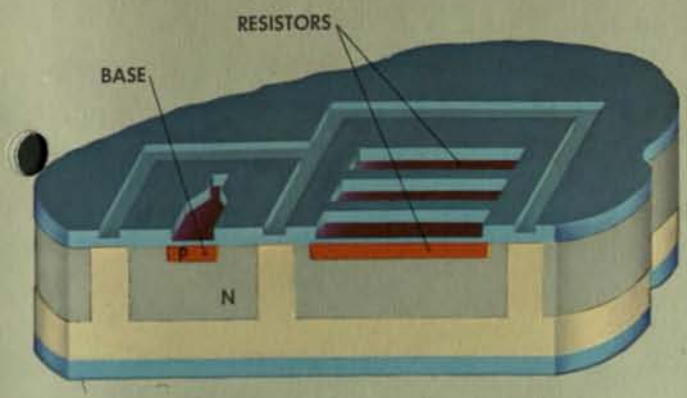


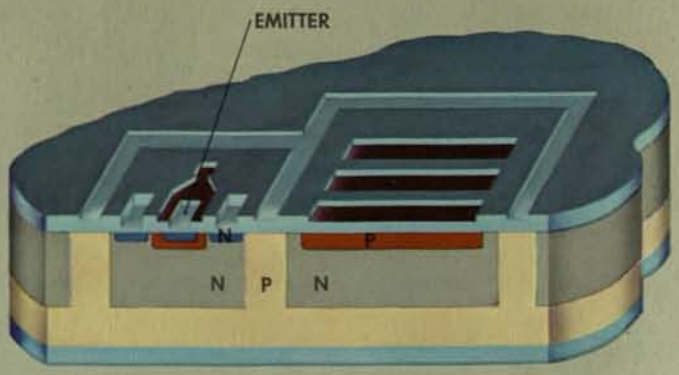
ISOLATION MASKING

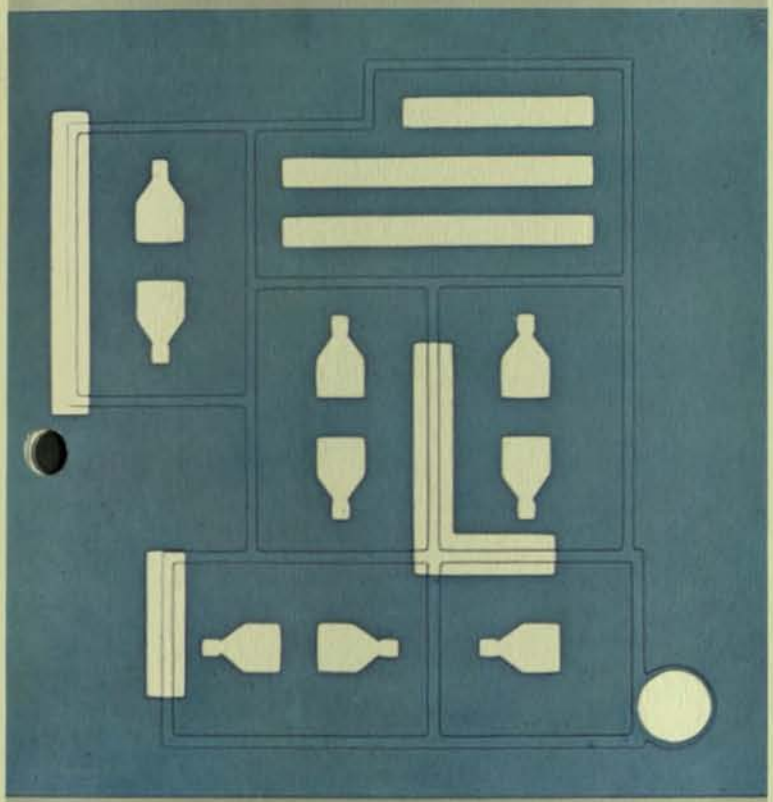
The following steps are performed in order to isolate electrically the individual transistors and resistors from one another. The wafers are coated with a photosensitive material in a darkroom. This material is exposed to light through a high-resolution mask. The portions not exposed are soluble and are easily removed by a solvent rinse. Then, an etch is used to dissolve the silicon dioxide from the areas not protected by the film of photosensitive material. In this way, a thin band, or "windows" surrounding the transistor areas, are photo-engraved through the protective silicon dioxide.

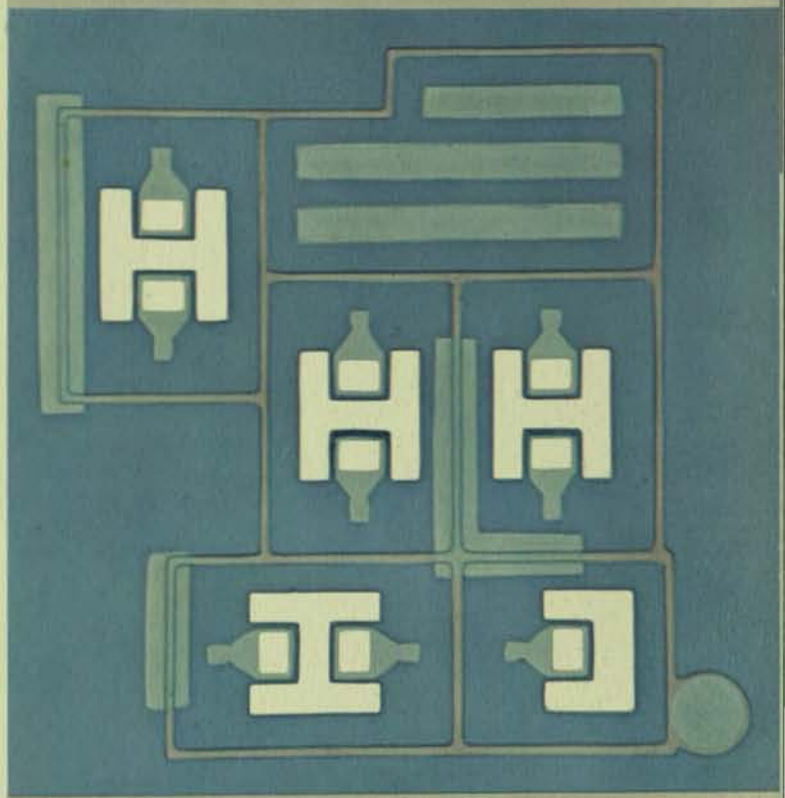
ISOLATION DIFFUSION

The wafers are placed into a special, high-temperature furnace where the atmosphere contains boron in a gaseous state. The boron impurity diffuses into the surface of the silicon wafer only where it has been exposed by the preceding photo-engraving steps. Even at elevated temperatures the silicon dioxide protects the underlying silicon from the dopants. The temperature is then raised to 1300°C; oxygen is introduced, and the boron impurity diffuses simultaneously from both sides of the wafer to meet in the middle, leaving pockets of the original n-type material which will become the collector regions of the transistors. These regions are separated from one another by the presence of the diffused isolation. In areas where the original silicon dioxide was etched away, a new layer is formed by surface oxidation during the diffusion.







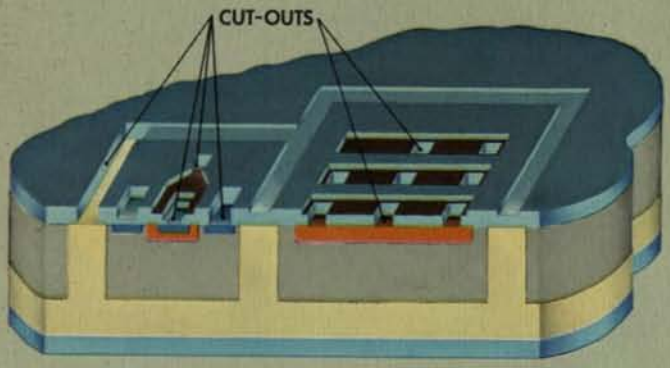


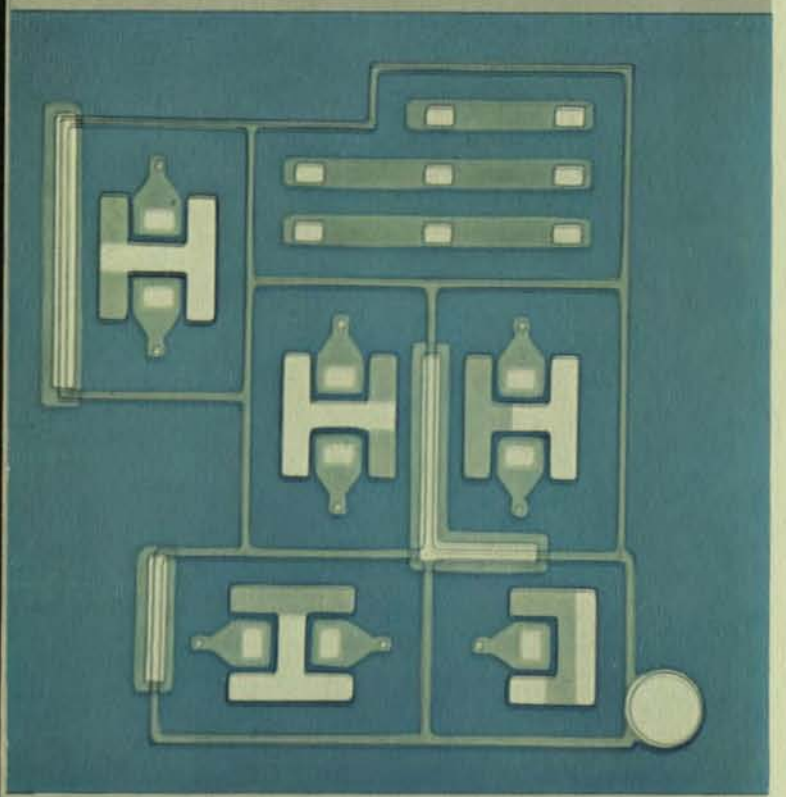
MASKING AND BASE DIFFUSION

The wafer is again masked and etched for the simultaneous diffusion of the base region and resistors. Once again boron is used as the diffusing impurity in this high-temperature diffusion. The base region is diffused into the n-type starting material to form the collector-base diode of each transistor as well as all the resistors in the circuit. As the diffusion progresses, the oxygen atmosphere in the furnace re-oxidizes the cutout portions of the wafer surface and seals them against contamination or injury. As the diffusion progresses downward into the wafer, it also proceeds laterally, diffusing into the silicon covered by the original protective oxide. The doping level of the base of the Micrologic transistor is such that the resistivity of the diffusion is compatible with the resistivity required for the formation of the resistors.

EMITTER MASKING AND DIFFUSION

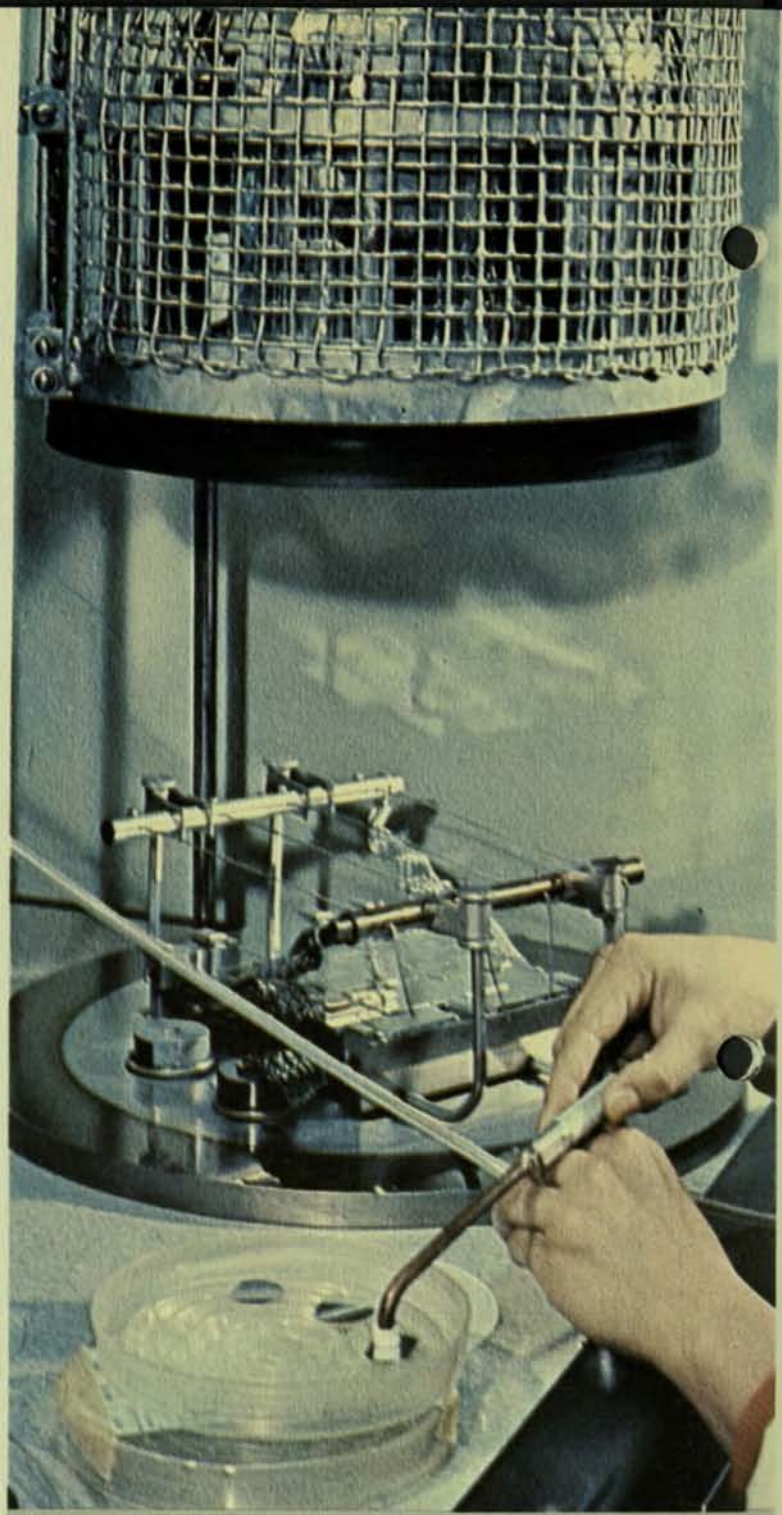
Another precisely indexed masking step is performed to remove oxide for the emitter diffusion and for the top-side collector contacts. In another high-temperature step, phosphorus — and n-type impurity — is deposited on the surface. Diffusion then takes place at about 1200°C. Again silicon dioxide forms as the diffusion progresses, covering the photo-engraved area and sealing the surface. Side diffusion carries the junction underneath the protective layer. Notice that in each case the diffused region ends underneath an oxide which existed previously. This oxide permanently protects the actual junctions of the device against exposure to the outside environment.





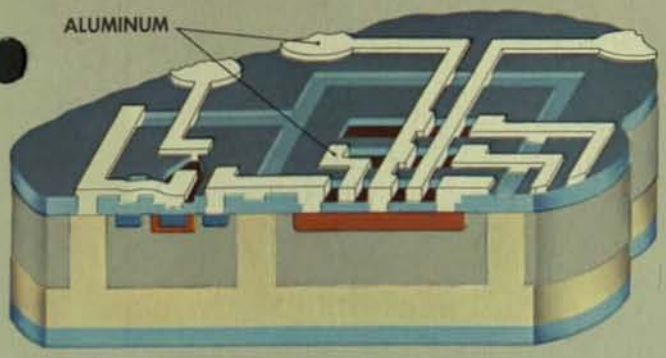
EXPOSURE OF CONTACT AREAS FOR INTERCONNECTIONS

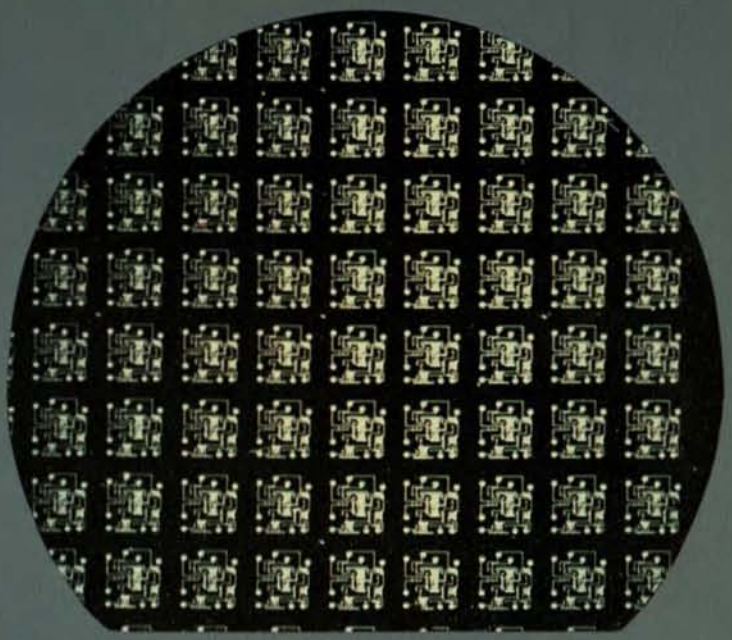
At this point the transistors and resistors of the Micrologic circuit are completed. They must now be connected together into the desired logic circuit. This is done by evaporating metal interconnections onto the surface of the silicon wafer. Before this can be done, however, a hole must be photo-engraved over the appropriate regions of the devices so that the evaporated metal can make contact. This is done in a masking step similar to the others.

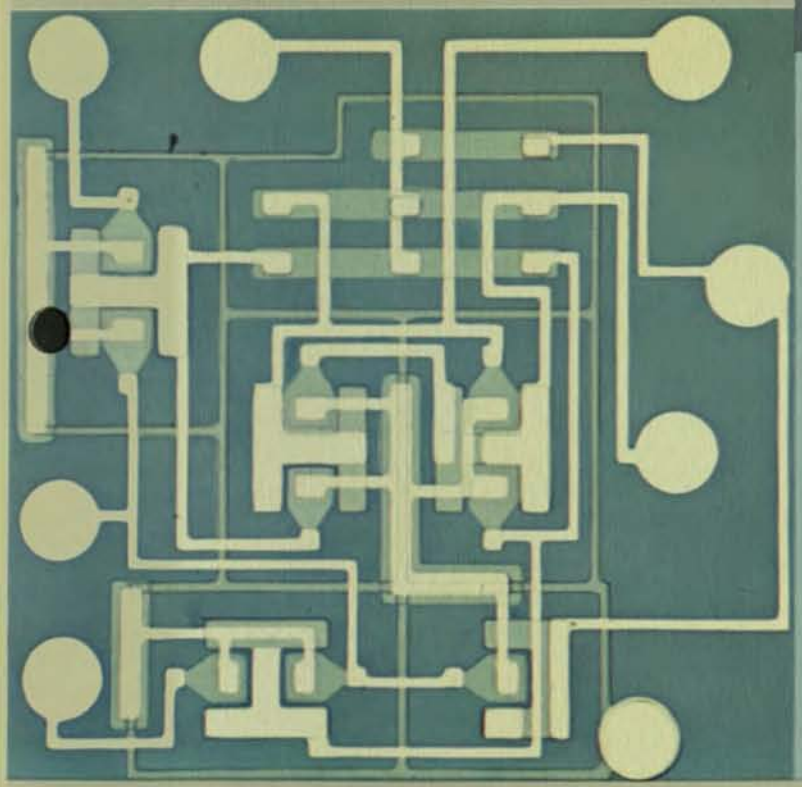


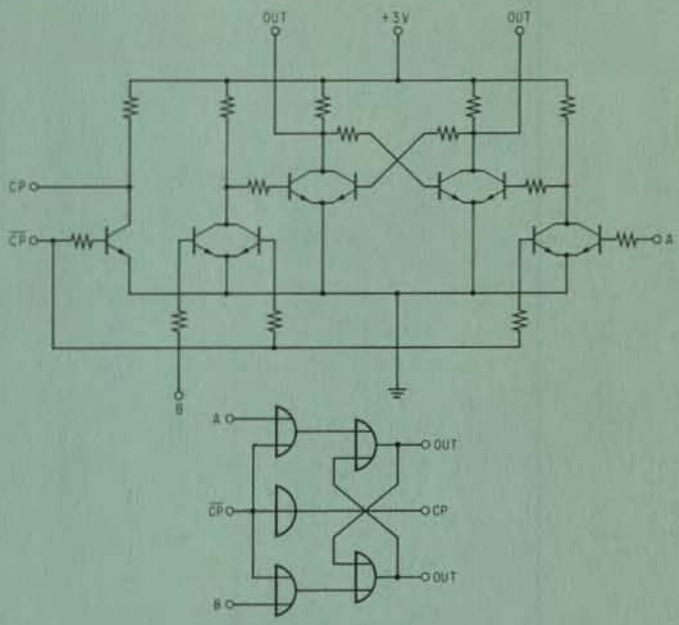
METALIZATION

The wafers are now placed into a high vacuum chamber containing a metal evaporating set-up. Aluminum is boiled from a hot tungsten filament forming an atmosphere of metal and other gases. The evaporated metal deposits in a thin, even coat over the entire wafer surface. Many wafers, comprising hundreds of Micrologic units, may be processed at one time in this fashion.





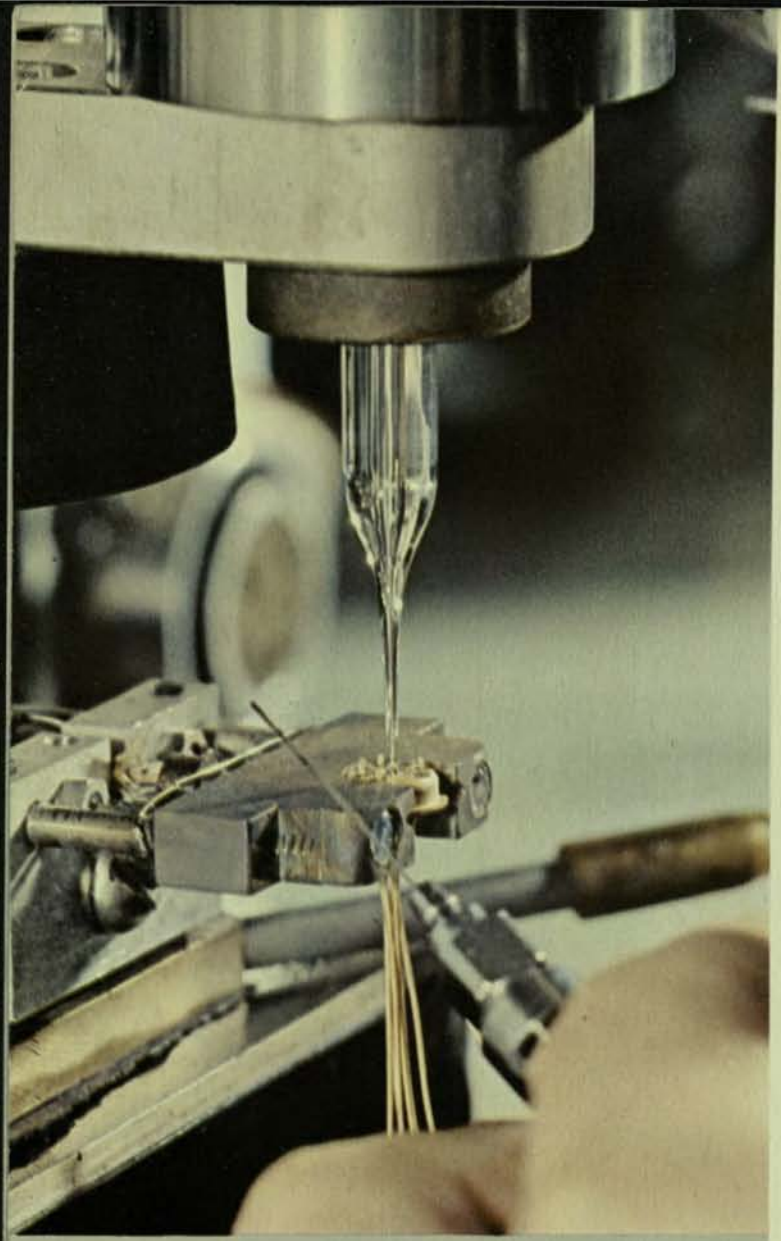




METAL INTERCONNECTIONS

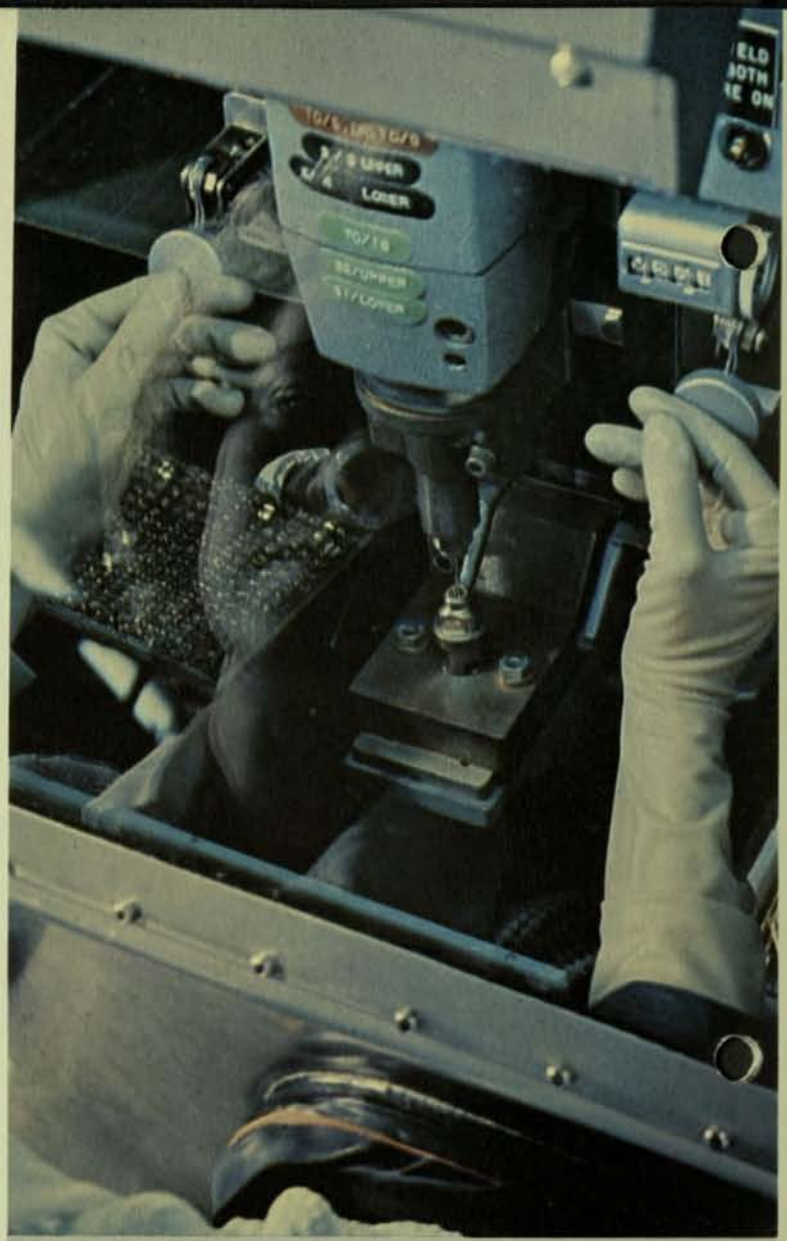
In another precise photo-engraving step, the aluminum layer is masked and selectively etched to leave a pattern of interconnections between transistor and resistor elements in the logic circuit. The Micrologic Half-Shift Register wafer is now complete as shown in the upper right figure and needs only to be cut into individual circuits and packaged. Up to this point, all operations have been done on many wafers at a time. The elimination of the handling of each device separately is a major factor in the reduction of production costs. This batch processing also increases the reliability and compatibility of the devices.

Compare the electrical schematic of the lower right figure to the color photomicrograph of the finished element. Notice the flip-flop section in the center of the picture, with the metal interconnections from the collector of one side to the base of the other. The collectors of each gate may be seen connected to the base of each flip-flop. All connections to the outside — inputs, outputs, power supply and ground — are brought out to the periphery of the element as large, circular aluminum pads, for easy, reliable connections. The power supply pad on the device may be traced to the center-tap on the 1200 ohm resistor, and from there through 600 ohms to each collector. All emitters have been tied to the isolation, which acts as the common ground.



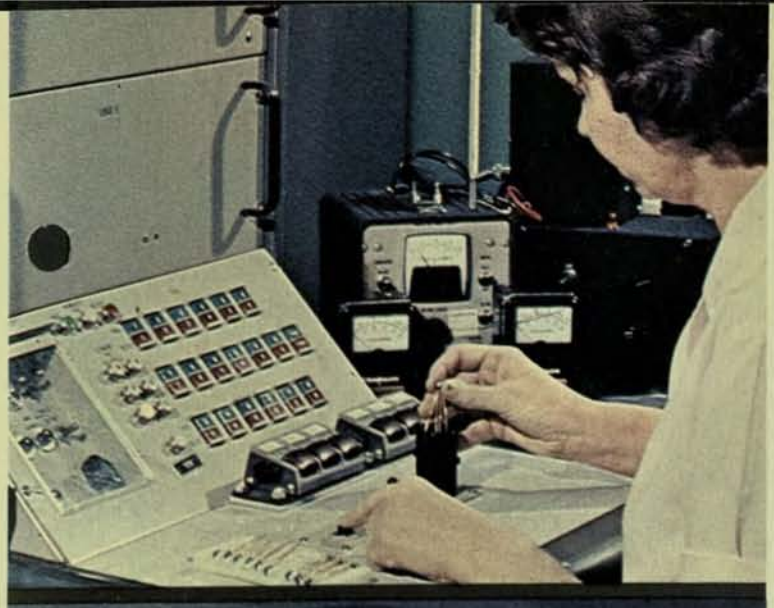
MOUNTING THE DEVICE

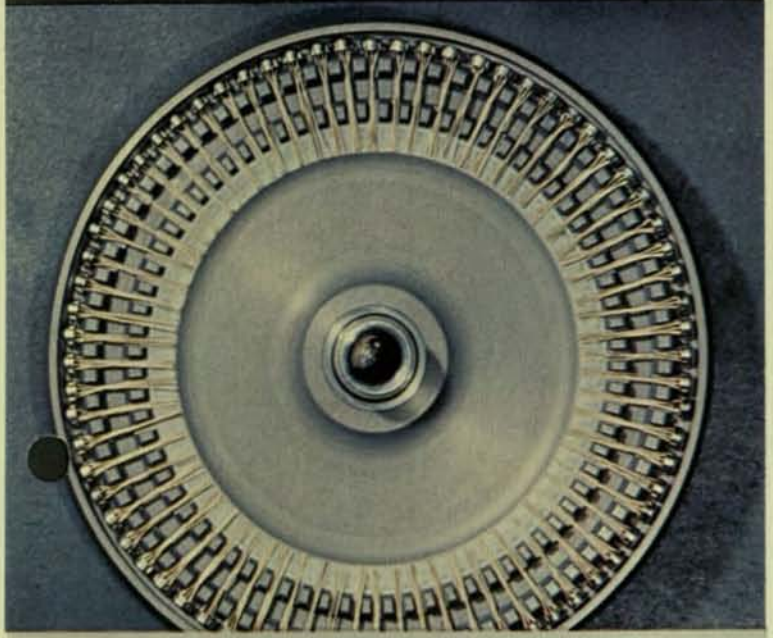
As another extension and modification of the standard Fairchild Planar process, the Micrologic elements are then packaged in a TO-5 type header with eight leads. The packaging operation uses techniques whose reliability has been verified extensively on transistors. The wafer is cut into small pieces using a technique very similar to the cutting of glass. A diamond scribe is used to make fine scratches on the surface of the wafer between the circuits. The wafer is mechanically separated along these lines into uniform square dice. The dice are then cleaned thoroughly, dried and inspected for defects under high-power microscopes before expensive hand labor is incurred. The die is then eutectically bonded to the center of a TO-5 type eight-lead header and proceeds to a lead bonding station. Using a capillary ball-bond, proven through four years of production experience at Fairchild, a fine gold wire is attached to each of the input, output and supply pads of the device. Each lead is held against a header post and securely spot-welded.



INSPECTION AND CAPPING

Following lead-weld, a final optical inspection is conducted to guarantee that the die has not been damaged in any manner during its packaging operation. Having passed this inspection, the unit is washed, dried and given a vacuum bake to remove moisture. Then, in the same chamber, a can is welded onto the header, covering and sealing the package. All steps from dicing through final seal are identical to those used to make standard Fairchild transistors. Micrologic elements or Planar transistors can share the same production line at any time.





ENVIRONMENTAL TESTING

After final seal, each Micrologic element is subjected to a number of tests to insure its reliability. They are subjected to mechanical shock tests, temperature cycling, and centrifuge acceleration tests. Elements which pass these tests are subjected to rigorous electrical testing. All Micrologic elements are 100% tested and sorted on Micrologic Mark II semi-automatic parameter testers. These machines check all measurable DC parameters and also perform a thorough worst-case functional operation test. Even after their final electrical tests, devices are continually sampled by Quality Control to confirm their conformance to rigid specifications. Each week a sample of devices is placed on a 125°C operating life test in a continuing evaluation program.

Finished units are supplied to Production Control for packing. They are placed in boxed stock for shipment to customers. The Micrologic Engineering Section of the Applications Department is available to help customers with logic applications.

The advanced technology discussed here is not limited to Micrologic. It may be directly applied to all other types of circuitry. Fairchild Semiconductor is equipped and able to offer custom integrated circuitry in quantity to your specifications. Our engineers invite your toughest circuit and applications problems for their study and solution.

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GINGER

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FAIRCHILD SEMICONDUCTOR NATIONAL SALES CONFERENCE '65 SAN JUAN, PUERTO RICO

The San Jeronimo Hilton still stands where one hundred eighty-four dedicated individuals met for the seventh annual Fairchild Semiconductor National Sales Conference. All were dedicated, and at least in part, to the same purpose. After five grueling days and seven grueling nights of earnest sales sessions, we left the lovely island with a new understanding of salesmanship, pricing, competitive bidding and the quick close. Several achievements deserve recognition: A special award for interior decoration (mobile division) to Colman Daniel and Jack Cooper. A signed copy of "The Old Man and the Sea" to Bob Pack and John Grey for their efforts on the briny. An assigned risk insurance policy to the Mountain View Volley Ball team for their bravery in (attending) the finals. An underwater compass for Bob Simko and an automatic pilot for Arnie Popky. But let us dedicate this tome to the man whose performance exemplifies all that made the conference possible, to Don Clarke, Salesman of the Year. For salesmanship in its fullest measure is the subject and object of it all.

Arrival....

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OLD SAN JUAN

SAN JERONIMO HILTON

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RICHARD HODGSON, PRESIDENT, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TOM BAY

DON VALENTINE

CHARLIE SPORCK, RICHARD HODGSON,
DON VALENTINE

ROBERT NOYCE, THOMAS BAY, GORDON MOORE,
DONALD YOST

Cocktails....

LOU LYONS, FRAN KRCH, BOB PETTIT, JERRY LARKIN

VINCE SABELLA, GORDON MOORE, MEL PHELPS, LEN SCHLEY, BILL SEIFERT

JIM CARR, BOB SIMKO

PETER TAGG, JIM MARTIN, G. VOLTINI, RALPH LEE

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JOHN O'DONNELL, KEN NORVELL, DICK SCHULKE

BILL EARNST, GEORGE GIBSON, MARTY JORDAN, RON HAMMER

BILL SLATER, COLMAN DANIEL, PETE ONSTAD, DICK GRANT, JOE PATRIDGE, JERRY CAMPBELL, CARL STEFFENS, JOHN LAMBROS

GEORGE BOHMAN, BERT McCARTHY, BILL WELLING

Banquet Dinner

AL MATTAL, JERRY LARKIN, BUCK ROGERS,
HOWIE SHAREK, JACK LEVIN, DON CLARKE,
KEN BERKLEY

LOU LYONS, LEE WETMORE, TERRY JONES,
JIM LUCY, JIM JOHNSON

MARSHALL COX, VINCE SABELLA,
JIM HONSBERGER, G. BADEWITZ, TOM COUGHLIN,
DON HALSEY, STEVE SCHWEBER, FRANK BROWN

KEN NORVELL, BILL FOCKELMANN, JOHN READY,
RAY SNIDER, LARRY ZISMAN, DICK SCHULKE,
JOE NEMANICH

BERT McCARTHY, BOB LEEPER, HAROLD POWELL, PETER TAGG, BOB PETTIT, JIM CARR, DICK MORGAN, WAYNE MONAHAN

DEL LA FACE, RON SMITH, GENE CANNY, BEN TAYLOR, RON HIMBURG, BOB HOFFMAN, BILL RICHMOND

TOM LITTLEFIELD, WARD GEBHARDT, JOHN HALL, BOB SIMKO, ARNIE POPKY, MARTY JORDAN

RALPH LEE, CARL STEFFENS, JESS CUNNINGHAM, DON McKENZIE, FRANK CATTERTON, TOM KLEINTANK, DON BOYLE

JIM BOURCY, CLOYD MARVIN, BERNIE MARREN, PAUL CARROLL, FLOYD KVAMME

JACK GIFFORD, TOM HYNES, JOE PATRIDGE, COLMAN DANIEL, CHAZ HABA, BOB GOODMAN

JACK COOPER, KEN TWETEN, BOB MAJOR, TIM CRONIN, DICK GRANT

ROGER SAPP, JERRY SANDERS, DICK KOEBLER, JACK ORDWAY, BOB VUGLAR, JACK MACINTOSH, EARL CHISWELL, PETE PAPAS

ART NANOS, JACK LASKIN, JIM MOSER, GENE McCLENNING, GARDNER DE SPAIN, CARROLL O'MACK, CHUCK SLOAN, MIKE NEWBERGER

Native Buffet Dinner

JOHN HALL, DON VALENTINE, and CATCH

JIM BOURCY, RAY SNIDER, LON LYONS, AL MATTAL, JOHN LAMBROS, AND JOHN'S SECOND CATCH

HOWIE SHAREK, DON VALENTINE, FRED BECK

BOOT CAMP

FRED BECK, JACK COOPER, DON VALENTINE, COLMAN DANIEL

JOE PATRIDGE, MRS. BUCK ROGERS

JOHN HALL SPLASH DOWN AND . . . RECOVERY

JOE PATRIDGE, COLMAN DANIEL, BILL CHAPMAN, FRED BECK, CHAZ HABA, JOE COSTELLO, HOWIE SHAREK

BILL SLATER, TOM BAY, LARRY MALONEY, BOB MAJOR, PETE ONSTAD, RON SMITH, JOE OBOT, RALPH LEE

RAY SNIDER, KEN NORVELL, FRANK BROWN, BILL FOCKELMANN, BOB ZARKO, JIM BOURCY, JIM JOHNSON, LEROY SUNDQUIST

BOB SIMKO, RON HAMMER, BOB GRAHAM, DEL LA FACE, JOHN LAMROS, VINCE SABELLA AND FRIEND, DAVE CONWAY

THE STEEL BAND

"LET ME ENTERTAIN YOU . . ."

TOM ANTHONY AND FRIEND


35X





















Candids....

G. BADEWITZE
HOWIE SHAREK
VIC GRINICH
INSTRUCTOR

UNDERWATER DEMOLITION TEAM

JIM MARTIN, BILL WELLING, BOB VALENTINE
TOM ANTHONY

JOHN READY, JERRY LARKIN, MAURI MORIN,
BOB GOODMAN, TOM HYNES, VERN OLSEN,
BOB HOFFMAN

RALPH LEE, HAROLD POWELL, JOHN O'DONNELL,
JOHN BUSACKER

BOB PACK, ARNIE KATZ, STAN GOODMAN,
JACK LASKIN, STEVE SCHWEBER, BILL EARNST

JERRY OBERLY, DON VALENTINE, JERRY SANDERS,
JACK GIFFORD

JIM LUCY, BILL DRESSER, AL MATTAL

DON CLARKE, DAVE HAUN, JOE COSTELLO,
JOHN GREY

ROGER SAPP, DICK SCHULKE, LARRY MALONEY, JACK MACINTOSH, BILL DRESSER, JOHN READY, DICK KOEBLER, JIM LUCY, BOB VUGLAR, DON YOST

JACK HYER, JOE NEMANICH, GORDON MARSHALL, LEN SCHLEY, KEN NORVELL

JOE COSTELLO, KEN TWETEN, JACK COOPER, FRED BECK, MIKE NEWBERGER, CARROLL O'MACK, TONY HAMILTON, JOHN GREY

GORDON MARSHALL, BOB TERRY

JACK GIFFORD, VIC GRINICH, CHAZ HABA, DEL LA FACE, JOHN LAMBROS, RAY SNIDER, BILL FOCKELMANN

CHRIS COBURN, RICHARD HODGSON

TERRY KILDUFF, MARSHALL COX

JOE PATRIDGE, BILL WELLING

ROBERT NOYCE

BILL DRESSER, LARRY MALONEY, LEN MILAUSKAS, TOM ANTHONY, JACK HYER, EWALD SPEDDEN, BOB VALENTINE, GEORGE BOHMAN

BOB SKURKO, CHRIS COBURN, JAY FARLEY, NICK DROOGAS, G. VOLTINI

GARY LOGAN, FRAN KRCH, JOHN RICHARDSON, GORDON MARSHALL, ED FARRELL, BILL WELLING

HERB RICHMAN, BILL SEIFERT, MEL PHELPS, JOHN RICHARDSON, TOM SCHNORRENBERG, FRANK LONERGAN, DAVE HAUN, MAURI MORIN, BILL EARNST

GENE BENNETT, AL JONES, GENE HALEY, DON ROGERS, JOHN LAMBROS, JERRY OBERLY, BEN ANIXTER

BILL CURRY, RON HAMMER, JOE OBOT, BOB ZARKO, NILS ATTEMANN, BILL O'HARA, BILL CHAPMAN

LEROY SUNDQUIST, PETE ONSTAD, BOB GRAHAM, BOB HOLDEN, JIM WILSON, FRED BECK, ED TURNEY

TERRY KILDUFF, JIM MARTIN, GEORGE KORPONTINOS, DON SMITH, STAN GOODMAN, ARNIE KATZ, LEN SCHLEY

BILL SIMPSON, JOHN O'DONNELL, PAUL KAUFMAN, DAVE CONWAY, GEORGE GIBSON, JOHN GREY, BOB PACK, TONY HAMILTON

The Sessions

CHARLIE SPORCK, BOB PACK

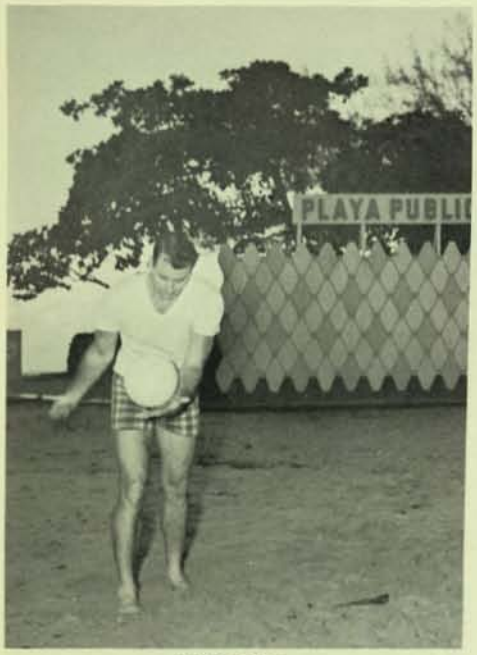
GORDON MOORE

DON VALENTINE,

BOB GRAHAM

BUCK ROGERS

Volleyball



ED FARRELL

DICK GRANT

FRED BECK, DON VALENTINE

MARSHALL COX

DICK GRANT, DON VALENTINE, HOWIE SHAREK, JACK GIFFORD, MARSHALL COX

JIM MARTIN, LEN MILAUSKAS, JACK ORDWAY, MARSHALL COX, JIM LUCY

MARSHALL COX, ROGER SAPP, LEN MILAUSKAS, JIM MARTIN

GARY LOGAN, TOM COUGHLIN, FLOYD KVAMME, ED TURNEY, CHAZ HABA, RON SMITH

ED FARRELL, FRED BECK, DICK GRANT, JACK COOPER

HERB RICHMAN, JIM MARTIN, RON SMITH

BOB GRAHAM, TOM COUGHLIN, JOHN LAMBROS

FRED BECK, JACK COOPER, ED FARRELL

DICK GRANT, BILL WELLING, JACK COOPER, DON VALENTINE

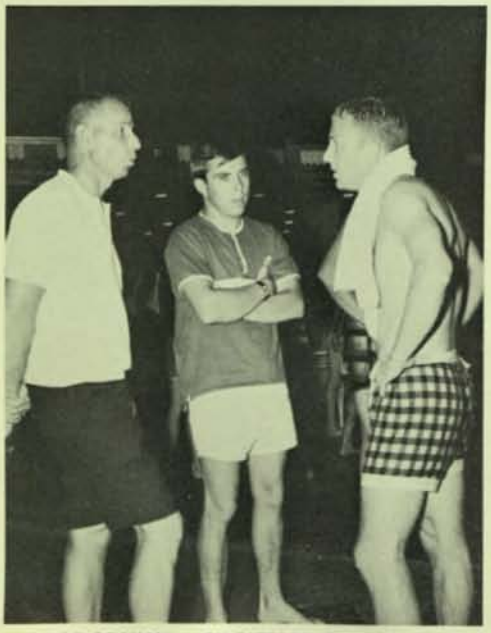
DON VALENTINE, BILL WELLING

Swimming Relays

BEN ANIXTER, CHARLIE SPORCK

ED TURNEY, CHARLIE SPORCK, BEN ANIXTER,

DON VALENTINE, CHARLIE SPORCK, TOM BAY, BEN ANIXTER

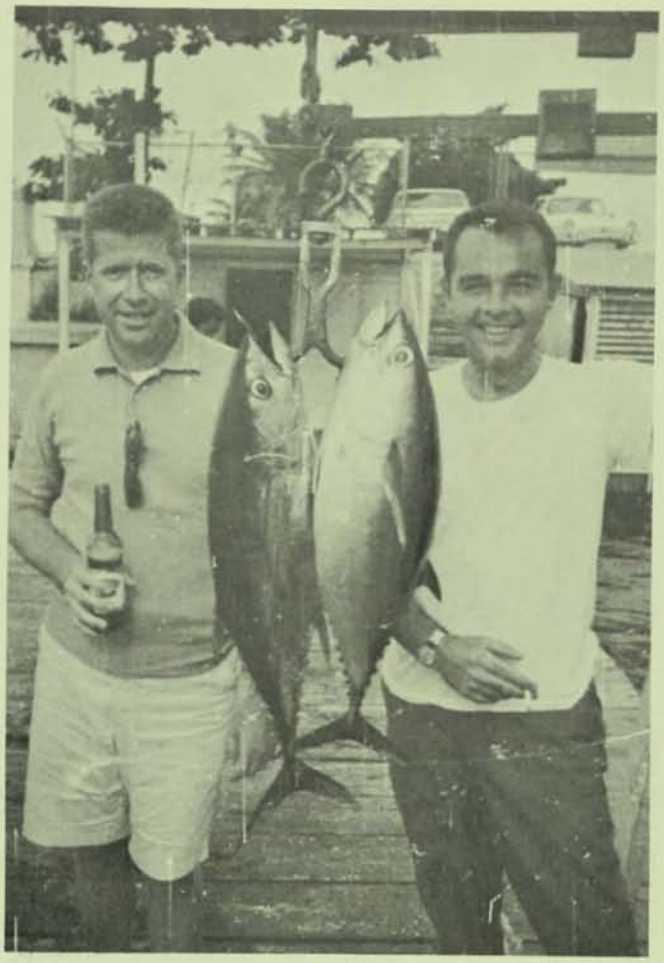


BOB GRAHAM, JACK GIFFORD, BEN ANIXTER

DAVE HAUN, JIM MARTIN, JERRY SANDERS

DON VALENTINE, CHARLIE SPORCK, RON HAMMER

Deep Sea Fishing



THE CHAMPS

THE LUCKY SHIP

EVERYBODY SAID IT COULDN'T BE DONE

$1.00 EACH . . . FROM THE FISH MARKET

JACK GIFFORD, FRED BOARD

Championship Awards

ROSTER OF CHAMPIONS: NATIONAL SALES CONFERENCE 1965

Volley Ball: FRED BECK — Hamilton Electro Sales
JACK COOPER — Hamilton Electro Sales
ED FARRELL — G. S. Marshall
DICK GRANT — Hamilton Electro Sales

Swimming Relay: BEN ANIXTER — Marketing, Mtn. View
BOB NOYCE — Group Vice President, Mtn. View
CHARLIE SPORCK — General Manager, Mtn. View
DON VALENTINE — National Sales Manager, Mtn. View

Golf: BEN ANIXTER — Marketing, Mtn. View
DICK GRANT — Hamilton Electro Sales

Deep Sea Fishing: JOHN HALL — Marketing Services Manager, Mtn. View
DON VALENTINE — National Sales Manager, Mtn. View

Tennis: JACK HYER — Hyer Electronics

Departure....

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