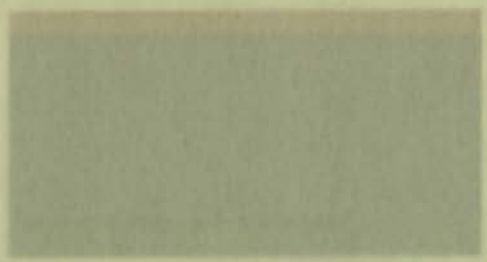
FAIRCHILD PLANAR PROGRESS REPORT



■ The first Planar transistor was introduced by Fairchild at the I.R.E. show in March, 1960. It set new standards of reliability, performance and yield—the latter especially important in the economics of production. Important since that date with the growth of silicon semiconductor devices in general, it also opened the way for production of integrated circuitry.

Combined with such techniques as epitaxial growth of crystals and specialized geometries, it has led to product refinements and parameter combinations otherwise unobtainable. It has enabled silicon—with its more favorable temperature characteristics—to match and outdistance the performance of germanium.

The Planar process and extensions of its technology have a potential still being explored.

FAIRCHILD PLANAR PROGRESS REPORT

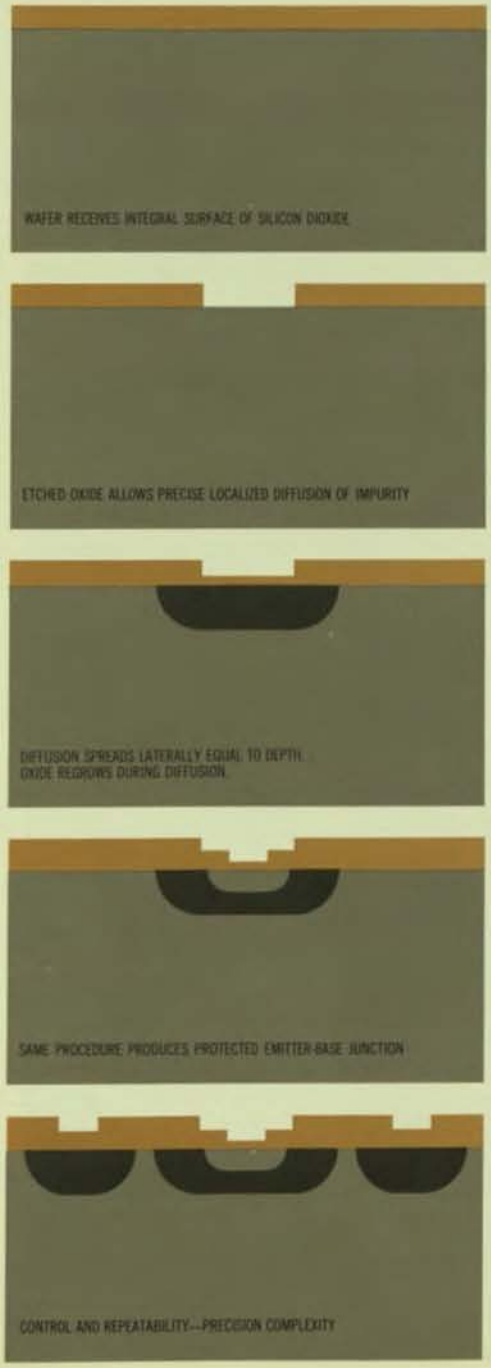
■ The first Planar transistor was introduced by Fairchild at the I.R.E. show in March, 1960. It set new standards of reliability, performance and yield—the latter especially important in the economics of production. Identified since that date with the growth of silicon semiconductor devices in general, it also opened the way for production of integrated circuitry.

Combined with such techniques as epitaxial growth of crystals and specialized geometries, it has led to product refinements and parameter combinations otherwise unobtainable. It has enabled silicon—with its more favorable temperature characteristics—to match and outdistance the performance of germanium.

The Planar process and extensions of its technology have a potential still being explored.

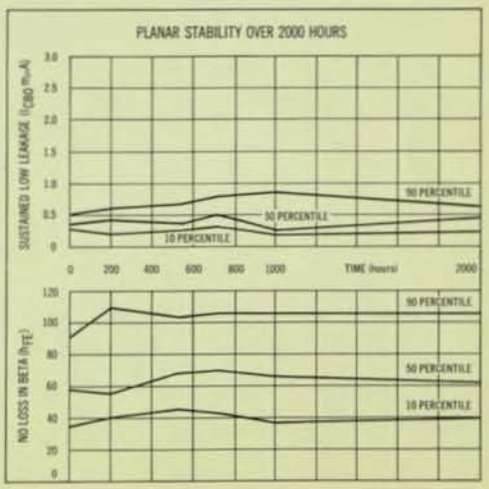
The advantages of the Planar process are derived from the first diffusion. Silicon wafers—from which diodes, transistors or microcircuits will be manufactured—are placed in an oxidizing atmosphere at 1200°C. A hard, silicon dioxide surface formed on the wafer is the key to Planar construction. It passivates the surface of the device and prevents contamination and associated parameter drift. It insulates the surface of the device and allows direct deposition of metal without electrical interference. As successive mask/etch/diffusion steps are performed, the wafer assumes the electrical characteristics gained from precisely controlled variations in collector, base, and emitter areas and junction perimeters. The Planar process assures uniformity, stability, and reliability. Important in simple devices, it is the key to production capability in complex integrated circuitry.

Uniformity: Diffusion of as many as two thousand individual dice in a typical wafer and hundreds of wafers in the same batch diffusion is coupled with the controlled timing, atmosphere and temperature of Fairchild Planar processing to produce devices of outstanding uniformity and optimum specifications with high yields.



Stability: The performance graphs illustrate the stability of Fairchild Planar devices over two thousand hours.

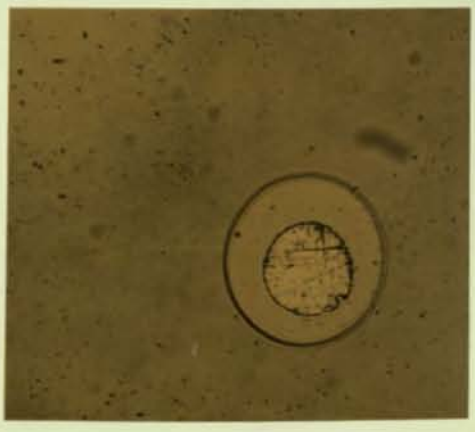
Reliability: The integral silicon dioxide surface of every Planar device is the key to Planar reliability. Each junction is formed beneath the oxide, thus never exposed to surface contaminants, microscopic particles or atmospheric variables which can cause degradation in devices with exposed junctions. Providing a large lead-attach area with electrically small devices permits the use of larger diameter lead wires and more reliable lead bonding in Micro-Planar devices.

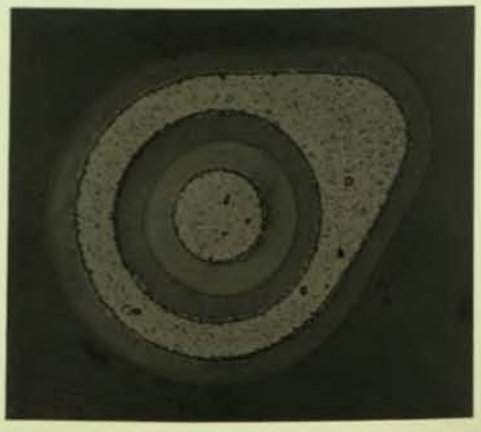


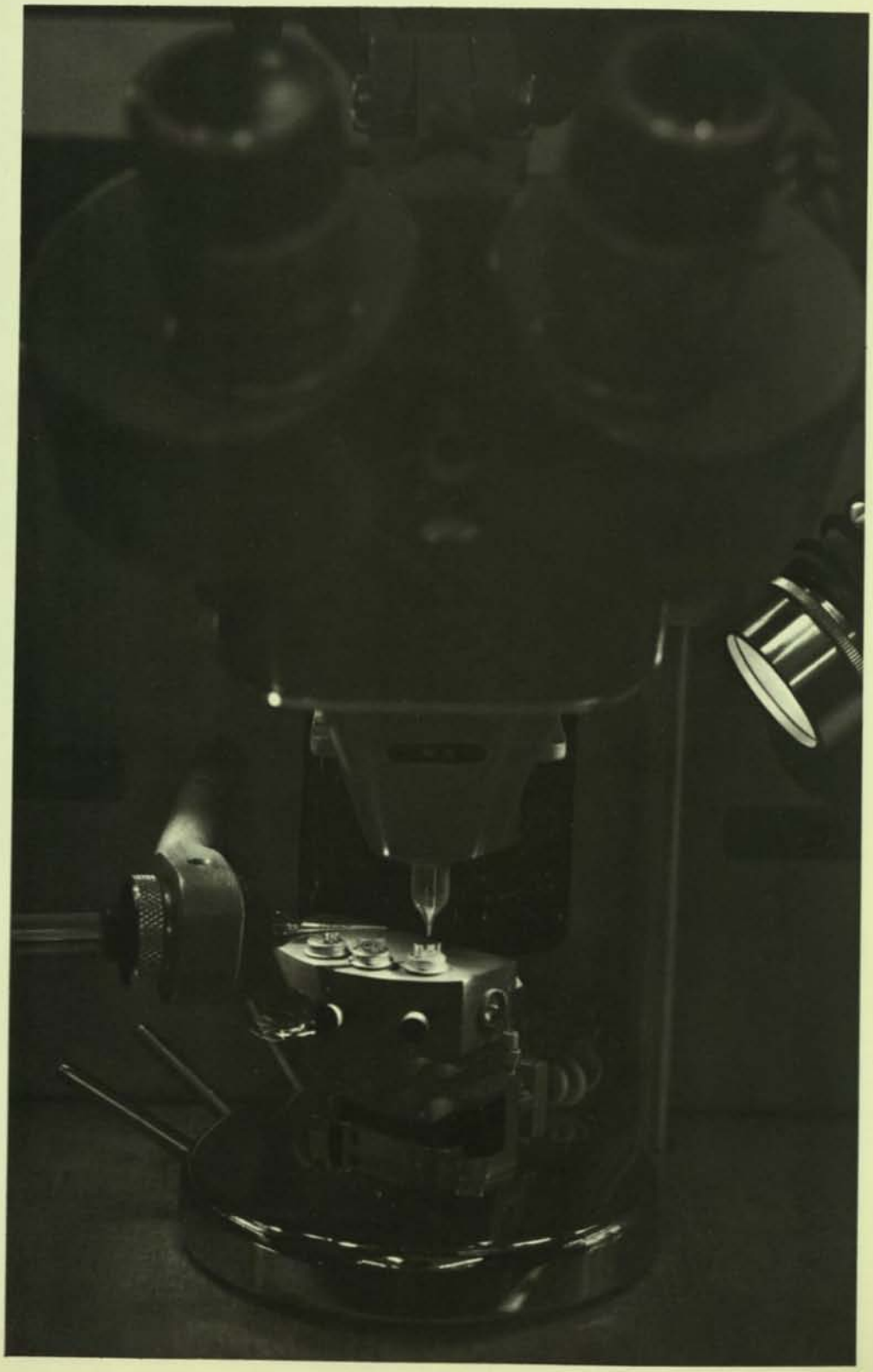
Planar Diodes exhibit a combination of electrical characteristics which cannot be duplicated through any other manufacturing technique: Fast switching speeds, high conductance, low capacitance, low leakage and high reverse voltages have been optimized in three basic diode types which encompass the specifications of a wide variety of competitive devices. From the basic diode types, FD 1, FD 2, and FD 3, Fairchild is able to ship to every major diode application. The uniformity and stability of these diodes has made them ideally suited to applications requiring matched pairs and quads. Combining Planar and epitaxial techniques has extended the range of diodes into very high conductance types. The new Adam package, featuring hermetic glass-to-metal seals and all-soldered connections, is available with all Fairchild Planar diodes where the application calls for miniaturization.

Transistors: With the introduction of the Silicon Planar 2N709, Fairchild broke the germanium speed barrier and there is no type of transistor available which cannot be made and made better through Planar processing. Planar and Planar epitaxial transistors have an exceptional combination of speed, power and low-saturation resistance. The stability, uniformity and reliability of Fairchild Planar devices dominate the application of all types of transistor—general purpose, amplifiers and switches. Amplifiers: high voltage, small signal, RF, VHF, UHF and power. Switches: high speed, high current, saturating and non-saturating. The precise control of the process which enabled Fairchild to produce these devices has also enabled the company to introduce similar types for industrial-commercial applications and to enter the entertainment market with a competitive edge—silicon's high performance at prices competitive to germanium.

Epitaxial techniques have been combined with the Planar process wherever it has offered an advantage in device performance. Particularly where higher currents are the object, and the combination of the two techniques has enabled Fairchild to produce small, high speed devices which still have the capability of handling high currents.

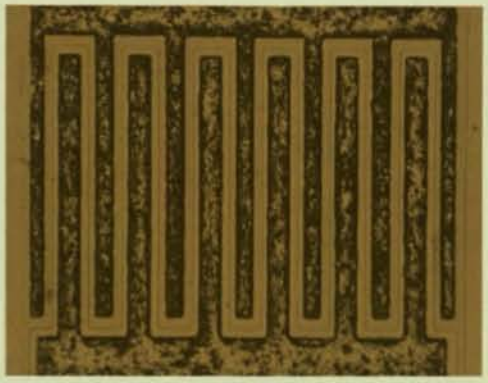


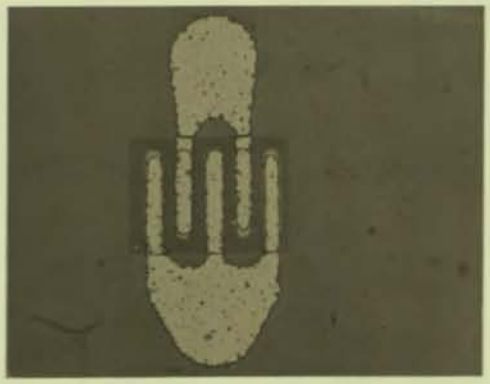




Geometries: Within the framework of the Planar process, the geometry or pattern of the diffusions and hence the junctions can be manipulated significantly, thus altering the electrical characteristics of the device. The original Planar transistors had the familiar 'teardrop' configuration shown on the previous page. The interdigitated geometry common to power devices and Fairchild's new 'trident' geometry feature long emitter-periphery to emitter-area ratio which results in good high current performance and low capacitance with high operating speeds and frequencies.

Multiple Assemblies: A unique advantage of the Planar process is demonstrated in a line of special products—multiple chip devices within a single package. Fairchild has had an established production line making special products for three years. The high yields of the Planar process made multiple assemblies economically feasible. The stability and uniformity of Planar devices makes it technically practicable to combine them with guaranteed matched electrical characteristics. Better thermal tracking between devices in one enclosure, in addition to Planar reliability, assures improved circuit reliability. This product line has helped designers achieve greater circuit performance and reliability especially where it is not economical to develop an integrated circuit for the application, but where reduced size, fewer interconnections and greater reliability are major considerations. The same chips which comprise Fairchild's basic product line are used in the manufacture of multiple assemblies. They are available in hundreds of configurations and in a variety of packages.





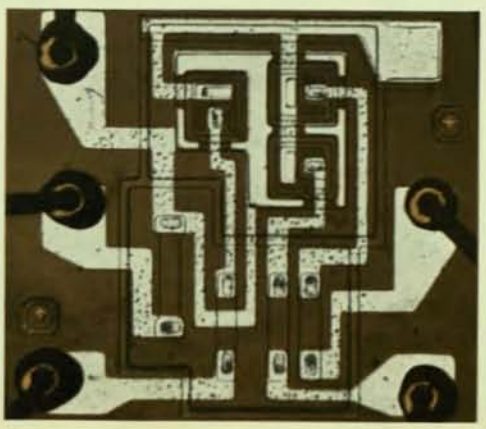
Micrologic: Within a year after introducing the Planar process, Fairchild produced the first practical microcircuit—integrating transistors and resistors, plus all the necessary interconnections, in a single, monolithic chip of silicon. A full spectrum of highly developed semiconductor skills was utilized: precision optics and mask-making; the Planar diffusion process; metal-over-oxide; mounting and lead bonding; testing and test equipment design and production.

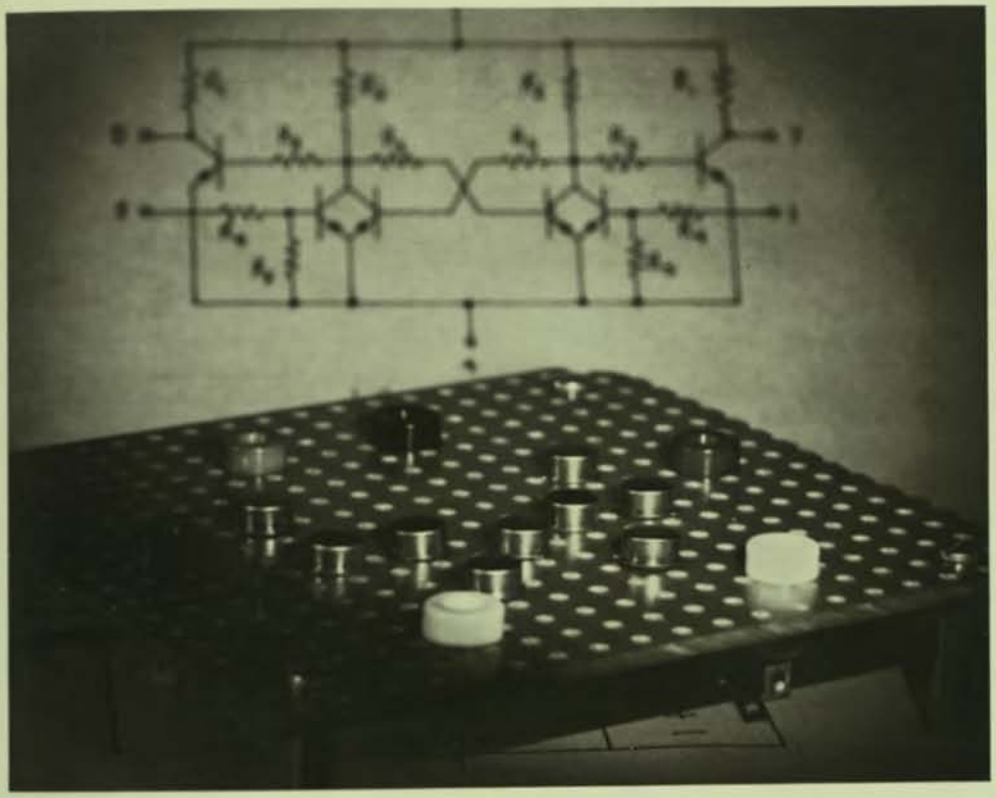
Fairchild's first offering was Micrologic —six compatible computer building blocks. This family of devices is sufficient to handle all of the logic-function requirements of a digital machine operating at bit rates up to 1 mc; no other components are required in the logic section of such a machine. The result is a smaller machine—requiring less power —which can be designed in less time—and cost far less to manufacture.

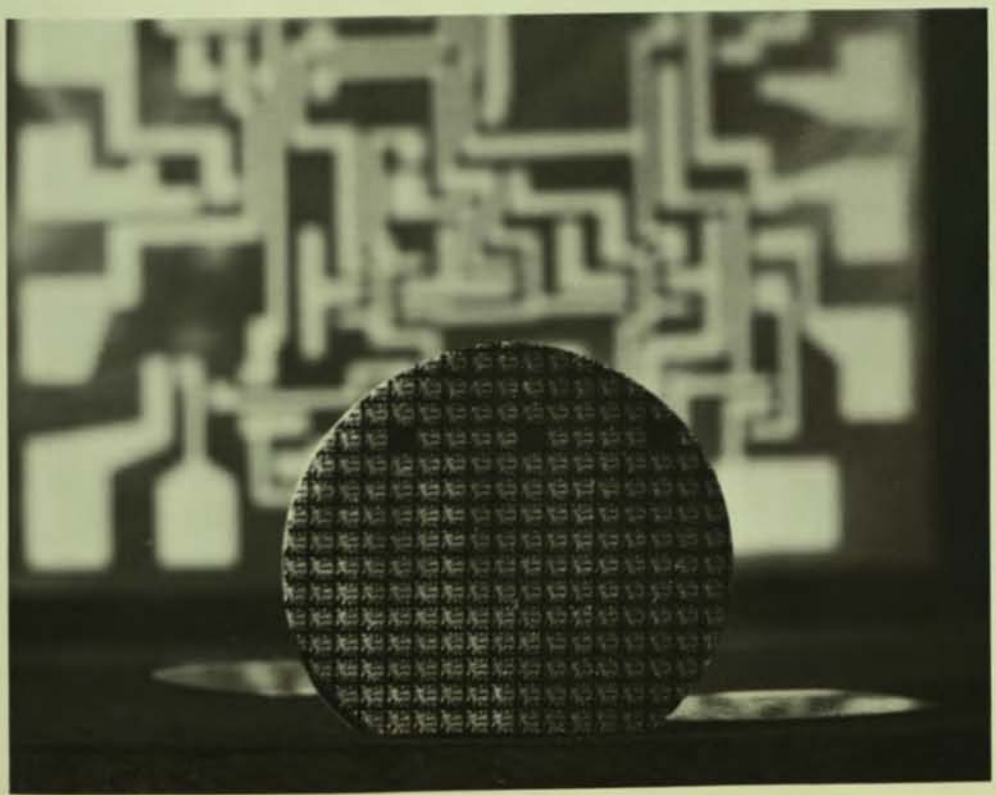
Micrologic utilizes modified DCTL (Direct Coupled Transistor Logic) circuitry and is designed to operate in a full military environment over a temperature range of −55° to plus 125°C. Worst-case propagation delay is 50 nanoseconds stage delay over the full temperature range.

Micrologic, and microcircuitry in general, offers the systems builder major reliability, and cost advantages besides the obvious one of decreased size. Improved reliability stems from many factors: The number of soldered connections may be reduced to one tenth the number required by standard components; power consumption is greatly reduced so less heat is generated; fewer dissimilar materials come into contact.

The improved cost picture stems from the major savings which can be realized in the use of Micrologic as opposed to the best contemporary single layer (printed circuit board) computer packaging techniques. With Micrologic, volume can be cut to one twentieth. Design time is one twentieth to printed circuit masters. The power requirement is one fourth—for equal speed and temperature ranges. Micrologic elements are handled exactly as transistors and can reduce the assembly costs to one tenth! And as the use of Micrologic has extended, the cost of the units versus the production volume relationship has brought the individual unit cost down. In total, these factors are expected to bring the cost of the logic section of a computer down to twenty or thirty percent of present costs. And all of these things are accomplished without sacrificing performance.



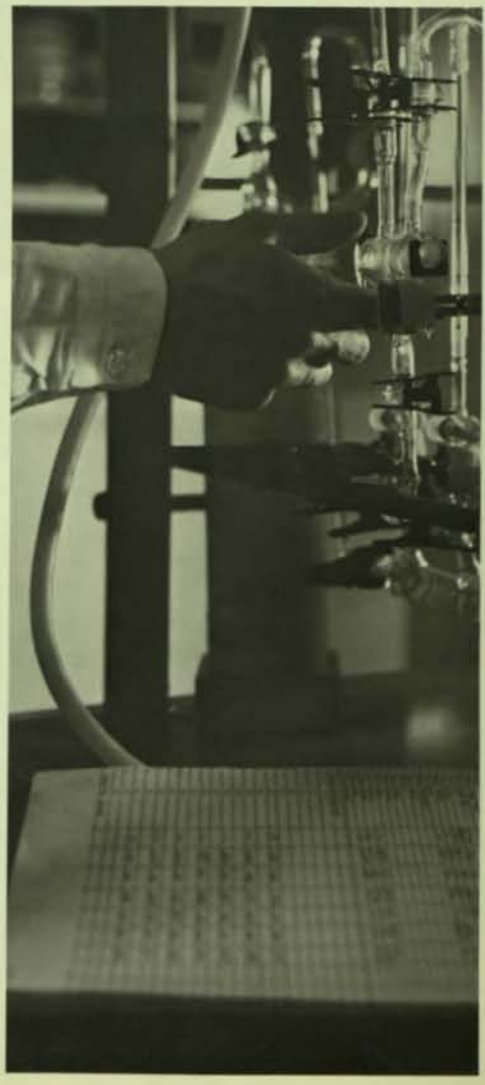




Custom Microcircuitry is a natural outgrowth of Fairchild's standard Micrologic product line. It derives from the development of successful, standard production microcircuits and the inherent flexibility of the Planar process. Within the broad framework of custom microcircuitry, there are two distinct groups—production circuits and Research and Development circuits. In designing custom microcircuits, the basic elements from which the designer works are discrete components, packaged separately and individually characterized with complete electrical data. The transistors, diodes, resistors and capacitors are available with complete specifications and breadboard for the designer to assemble an electrical mock-up of the circuit ultimately to be produced as a single silicon chip. When the design and specifications have been thoroughly proven, Fairchild begins its production cycle. The finished microcircuits—delivered in twelve weeks from acceptance of the schematic—are mass produced according to standard Fairchild procedure. This includes subjecting samples of each batch to a comprehensive quality assurance program. Fairchild also designs and builds special electrical equipment for inspecting the finished units. The custom microcircuits are manufactured in the same manner as Fairchild's Micrologic product line; the designer benefits from the advantages of having his own design built in microcircuitry and has the assurance of Fairchild's successful two years' experience in volume microcircuit production. The same equipment, the same highly skilled personnel and the same unique processes are employed.

FAIRCHILD
SEMICONDUCTOR

Fairchild is now extending microcircuitry techniques to include the integration of NPN, PNP and field effect transistors within a single substrate. The technologies are in hand enabling Fairchild to produce microcircuits with operational and functional characteristics unattainable with the use of discrete components. Ultimately, these new devices will hold a relationship to present transistors similar to that which transistors now hold to vacuum tubes. The marriage of thin film and Planar epitaxial technologies in an integrated device is a technique which allows the fabrication of circuits in smaller devices, resulting in lower systems cost and improved systems reliability. Circuits of this type have the potential of greater switching speeds, frequencies and operation at higher currents—all with greater packaging densities. These are State-of-the-Art integrated circuits, a direct outgrowth of Fairchild's Planar process, the process which has brought about true versatility and economic practicality in silicon.



FIELD SALES OFFICES

Sherman Oaks, California
Oak Park, Illinois
Plainview, L. I., New York
Minneapolis, Minnesota
Detroit 28, Michigan
Huntsville, Alabama
Orlando, Florida
Jenkintown, Pennsylvania
Washington 6, D. C.
Syracuse, New York
Bedford, Massachusetts
Palo Alto, California
Englewood, Colorado
Scottsdale, Arizona
Seattle 4, Washington
Poughkeepsie, New York

FAIRCHILD SEMICONDUCTOR ■ A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

■ 545 WHISMAN ROAD/MOUNTAIN VIEW, CALIFORNIA/PHONE 415-968-8161/TWX: 415-969-9165

4-15/3-63/PRINTED IN U.S.A. © 1963

FAIRCHILD SEMICONDUCTOR ■ A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

■ 545 WHISMAN ROAD/MOUNTAIN VIEW, CALIFORNIA/PHONE 415-968-8161/TWX: 415-969-9165

RELIABILITY '65

PREDICATIONS AND MEASUREMENT

RELIABILITY '68

The reliability of our product is a fundamental and universal concern at Fairchild Semiconductor. In this brochure you will find documentation of Fairchild reliability, details on the tight manufacturing control and test procedures we use to assure it, and a resume of the Fairchild FACT program.

Because in the final analysis reliability begins with design, we have included a separate section detailing the development of the Fairchild-patented Planar process and technological refinements which help us build reliability into all our products.

Table of Contents

View through operator's microscope of a Micrologic wafer in the process of 100% electrical testing of all dice on the wafer.

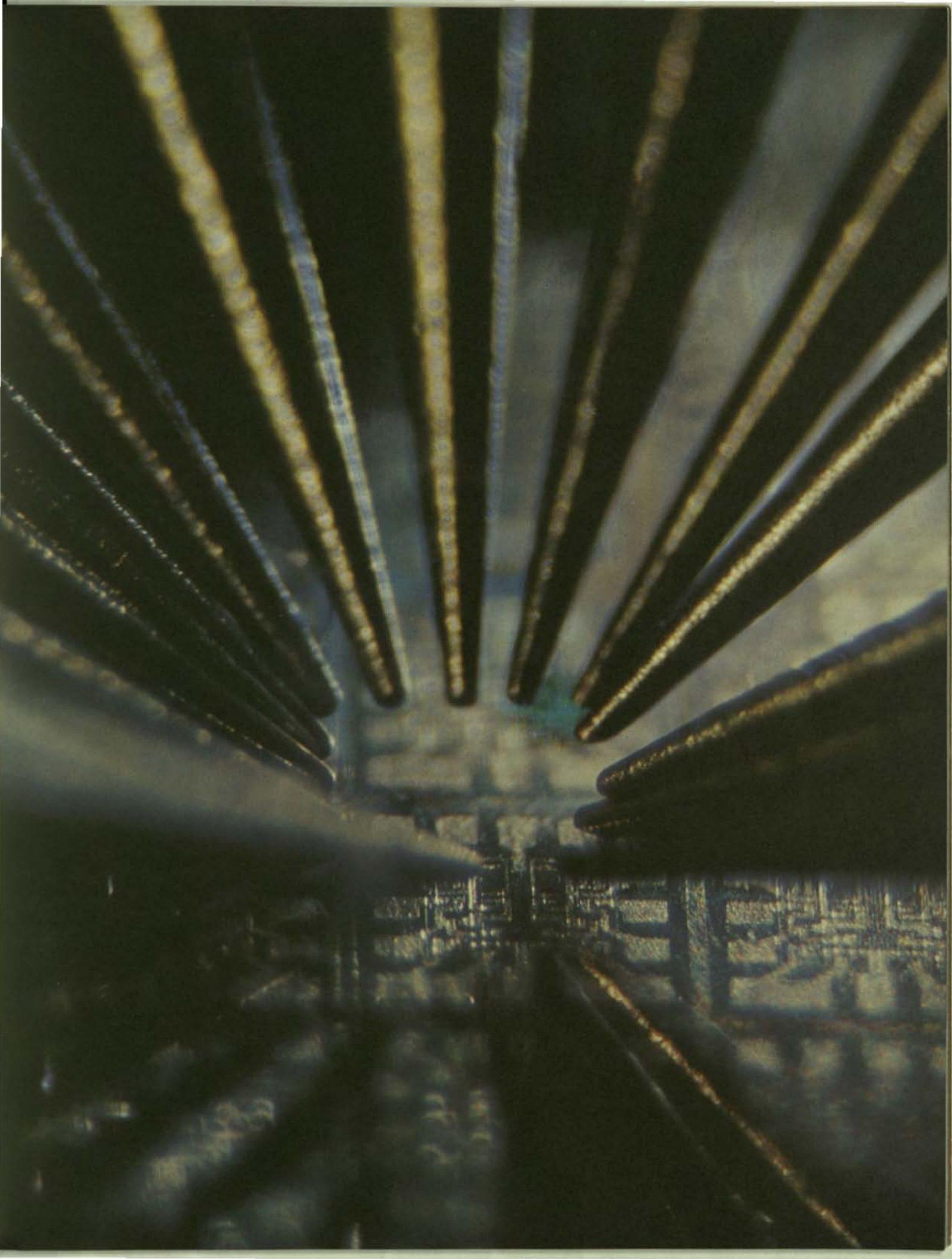


FIGURE 1
Microcircuits — Epitaxial Extended Life Test

Ring Counter – Rings are monitored daily to assure continuous operation

Date Placed on Test	Element Sample Size	Hours per Day	Test Conditions	Total Test Hours Accumulated
February 4, 1964	Three-Input Gate TO-5 μL903 2018 Units	48,432	V_{CC} = 3 Volts T_A = 125° C	17,556,600 (362.5 Days of Continuous Operation)
March 18, 1964	Three-Input Gate TO-5 μL903 922 Units	22,128	V_{CC} = 3 Volts T_A = 125° C	7,680,796 (119.5 Days of Continuous Operation)
April 17, 1964	Three-Input Gate TO-47 SL 1091 205 Units	4,920	V_{CC} = 3 Volts T_A = 125° C	1,424,340 (289.5 Days of Continuous Operation)
April 17, 1964	Dual Two-Input Gate TO-5 $MW_{\mu}L$ 910 184 Units	4,416	V_{CC} = 3 Volts T_A = 125° C	1,278,432 (289.5 Days of Continuous Operation)
September 15, 1964	Dual Four-Input Gate TO-5 $DT_{\mu}L$ 50 Units	1,200	V_{CC} = 6 Volts T_A = 125° C	168,000 (140 Days of Continuous Operation)
October 6, 1964	Dual Four-Input Gate TO-5 $DT_{\mu}L$ 100 Units	2,400	V_{CC} = 6 Volts T_A = 125° C	285,600 (119 Days of Continuous Operation)
December 20, 1964	Dual Four-Input Gate TO-5 $DT_{\mu}L$ 147 Units	3,528	V_{CC} = 6 Volts T_A = 125° C	112,896 (32 Days of Continuous Operation)
TOTAL January 31, 1965	3,626 Units	87,024	27,895,664 No Failures F. R. 0.0030%/1000 hours at 60% confidence F. R. 0.0082%/1000 hours at 90% confidence	

Reliability in Operation

4

No failures in 77.9 million hours extended life tests

The exceptional reliability of Fairchild products has been documented repeatedly. MIT's Instrumentation Laboratory, working on the Apollo program, has conducted operational life tests on Micrologic elements totalling over 50 million hours without a single failure. Additional microcircuits are on test at Fairchild, and as of January 31, 1965, the two programs had accumulated more than 77.9 million element-hours without a single failure, generating a combined failure rate of 0.0012% per thousand hours at a 60% confidence level (0.0030% per thousand hours at 90% confidence).

Fairchild devices have also scored an impressive record for performance in missiles and satellites. The Vela nuclear detection satellite is one example. When it was launched in October, 1963, its lifespan was estimated at six months. In February, 1965, sixteen months later, it was still operating perfectly, monitoring radiation levels in outer space. Among its components are more than 1 thousand transistors and 3 thousand diodes manufactured by Fairchild.

Major missile and satellite programs featuring Fairchild devices are the Mariner II, Gemini, Injun I, Injun III, Apollo, Vela, Surveyor, OGO, Snycom, Hawk, Sprint, Pershing, Titan, Ranger, Minuteman, and Polaris.

Failure rate of 0.0012% per 1000 hours for microcircuits at 60% confidence

Fairchild integrated circuits have demonstrated the following failure rates on operating life tests:

1. The Martin Co. in Orlando, Florida, operated Fairchild integrated circuits in a ring oscillator for 1 million element-hours at 25°C and 1 million element-hours at 75°C without a failure. Failure rate = 0.045% per 1000 hours at 60% confidence (0.114% per 1000 hours at 90% confidence).

Indicator lights on a typical temperature-cycling chamber in the reliability laboratory at Fairchild.

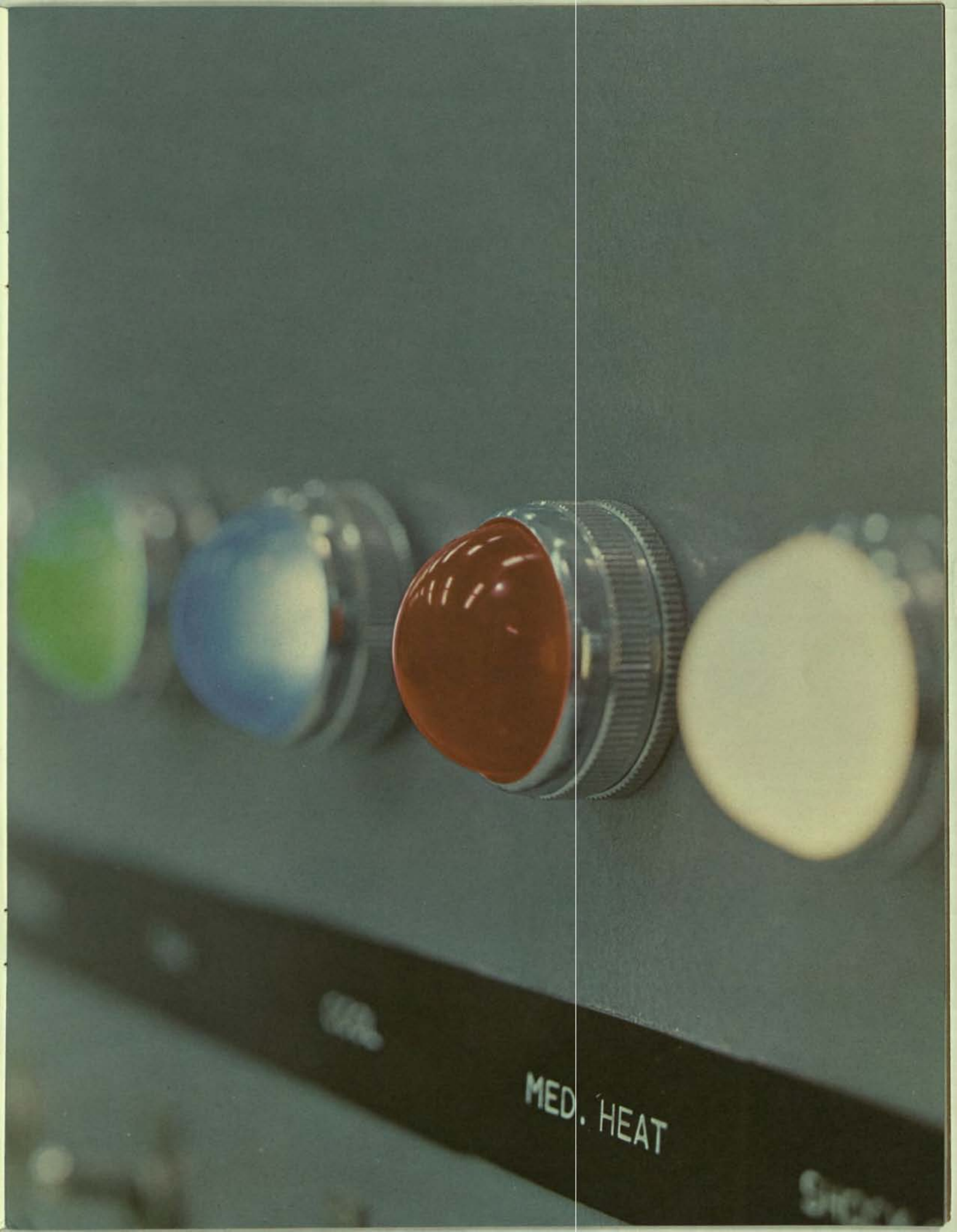

MED. HEAT

FIGURE 2
High Stress Tests
μL903 Gate TO-5 Package

Subgroup and Test Conditions	Sample Size	Bonds Stressed	Per MIL-STD 750 Para. No.	Stress Level (KG's)	Temperature (° C)	No. of Failures				
						After Each Stress				
						A	B	C	D	E
1. Centrifuge (Y_1 orientation only) (Each sample stressed at same G level 5 times)	18	108	2006	20	—	0	0	0	0	0
	18	108		40		0	0	0	0	0
	18	108		100		0	0	0	0	0
	18	108		161		4	0	1	0	0
	18	108		202		2	1	0	0	0
2. Thermal shock, 10 cycles. (Sample subjected to test 5 times, or 50 cycles)	10	60	1056	—	−65 to 200	0	0	0	0	0
3. Shock test. (Each sample subjected to 30 blows 5 times (150 blows) at the same G level.)	10	60	2016	3	—	0	0	0	0	0
	10	60		6		0	0	0	0	0
	10	60		12		0	0	0	0	0
						After Each Readout				
						0	250	500	1000	
4. Storage and centrifuge. (Units centrifuged and readout at 0, 250, 500, and 1000 hours.)	10	60	1031 & 2006	40	25	0	0	0	0	
	10	60		40	150	0	0	0	0	
	10	60		40	200	0	1	0	0	
	10	60		40	300	0	0	0	0	

2. Extended life tests, in house at Fairchild, on nonepitaxial units manufactured before 1963. Failure rate = 0.0084% per 1000 hours at 60% confidence (0.022% per thousand hours at 90% confidence).

3. Extended life tests, in house at Fairchild, on epitaxial material produced during 1964. Failure rate = 0.0033% per 1000 hours at 60% confidence (0.0082% per 1000 hours at 90% confidence). (0 failures in 27.8 million hours)

4. MIT Instrumentation Laboratory tests of circuits for Apollo. Failure rate = 0.00185% per 1000 hours at 60% confidence (0.0047% per 1000 hours at 90% confidence). (0 failures in 50 million hours)

5. The combined failure rate of (3) and (4) above for current epitaxial microcircuits was 0.0012% per 1000 hours at 60% confidence (0.0030% per 1000 hours at 90% confidence).

Figure 1 details the extended life tests on Fairchild microcircuits manufactured during 1964. As of January 31, 1965, no failures had occurred in 27,895,664 element-hours!

Figure 2 lists results of typical high-stress tests performed by Fairchild's Reliability Laboratory. Centrifuging produced no failures until the 161 thousand G level. (Military specifications normally require 20,000 to 40,000 G's.) Only 1 failure occurred in a sample of 40 units stored at 200°C for one thousand hours and centrifuged 4 times during that period at 40,000 G's. No failures occurred in another 40-unit sample stored at 300°C for the same period and subjected to the same stress.

Failure rate of 0.00001% per 1000 hours for diodes at 60% confidence

Figure 3 lists results of high-temperature storage tests conducted on three diode families. Since the number of failures found in any of the families was very low, the failure rates computed here are primarily a function of the number of element-hours accumulated. High-temperature (150°C) storage tests for 600,000,000 element-hours with the FD-100 produced no failures, generating a failure rate of 0.00001% per 1000 hours at 60% confidence (0.00038% per 1000 hours at 90% confidence).

Temperature cycling and burn-in area of reliability laboratory at Fairchild.

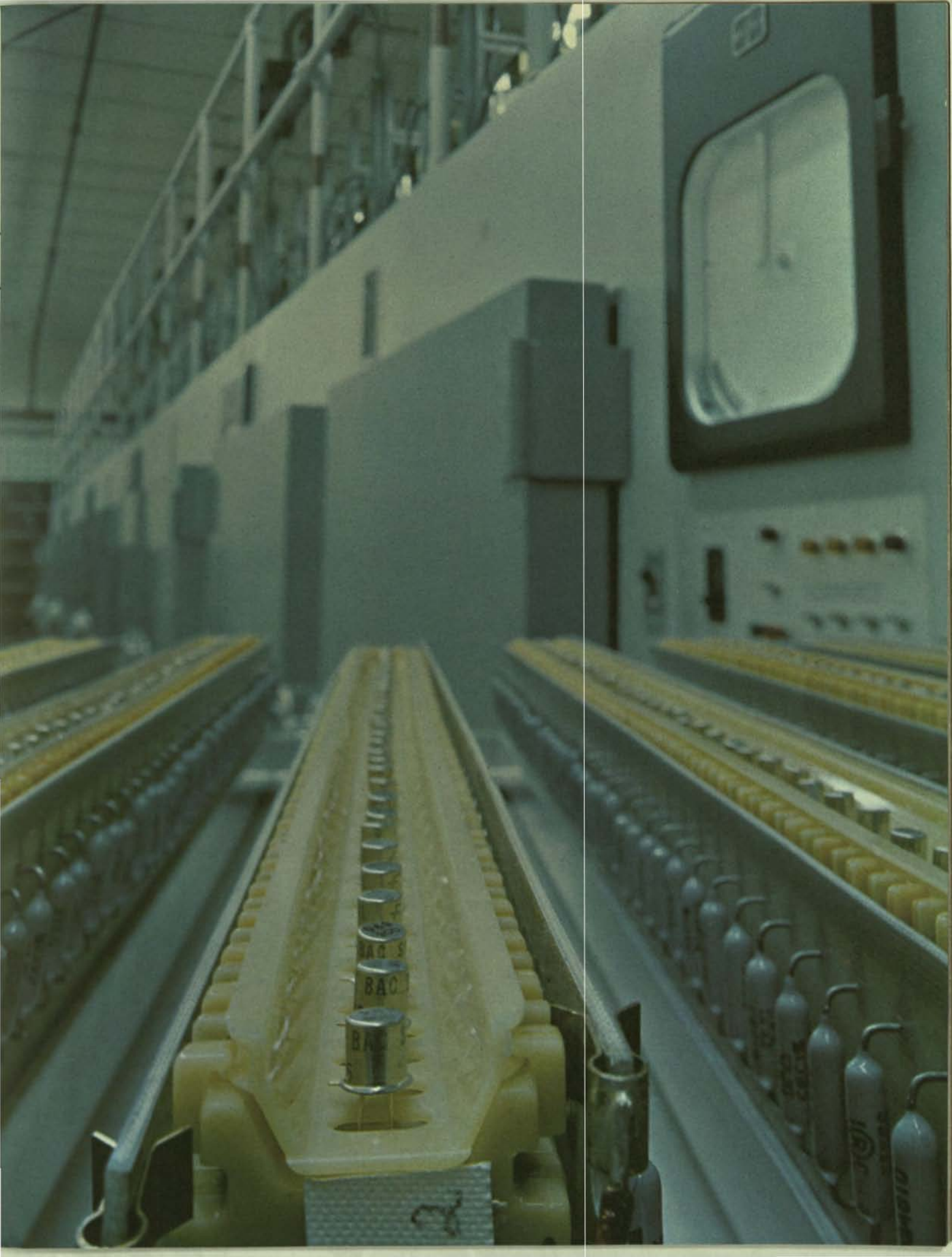


FIGURE 3
High-Temperature Storage Tests
on Three Representative Diode Families

	High-temperature Storage (150° C)		
Family	Sample Size	Element Hours	Failure Rate* (%/1000 hours)
FD-100	90,209	600,000,000	0.00001
FD-200	8,320	12,500,000	0.008
FD-600	8,320	12,500,000	0.008

*At 90% confidence

Failure rate of 0.002% per 1000 hours for transistors at 60% confidence

In extended operating life tests on a typical device in connection with the Minuteman program a total of 84.6 million transistor-hours generated a failure rate of 0.002% per 1000 hours at 60% confidence (0.005% per thousand hours at 90% confidence).

Operating life tests conducted during 1964 on 10,825 transistors of many different types accumulated a total of 21,809,249 element-hours, generating a failure rate of 0.039% per 1000 hours at 60% confidence (0.053% per thousand hours at 90% confidence).

Same order of reliability for Fairchild consumer products

The epoxy consumer products have demonstrated the same order of reliability as Fairchild military products. The SE6001-2N3566 family, for example, has had no failures in the last ten consecutive lots on storage life at 125°C or on operating life test at 300 mW. This represents nearly 250,000 hours without a failure.

Their solid construction makes the epoxy units virtually immune to mechanical shock and vibration. Shock tests up to 15,000 G's have yielded no failures. There have been no failures to date under the rigorous Fairchild FACT program (see Page 20 and Figure 9) on dynamic tests (shock 3,000 G's, plus vibration fatigue, plus vibration variable frequency), and in addition all lots are subjected to and consistently pass atmospheric tests consisting of thermal shock, temperature cycling and moisture resistance in accordance with MIL-STD-750.

It is important to note that all failure rates cited are actual failure rates, without acceleration factors.

Transistors mounted in a production centrifuge. Fairchild devices receive this test during the manufacturing cycle.

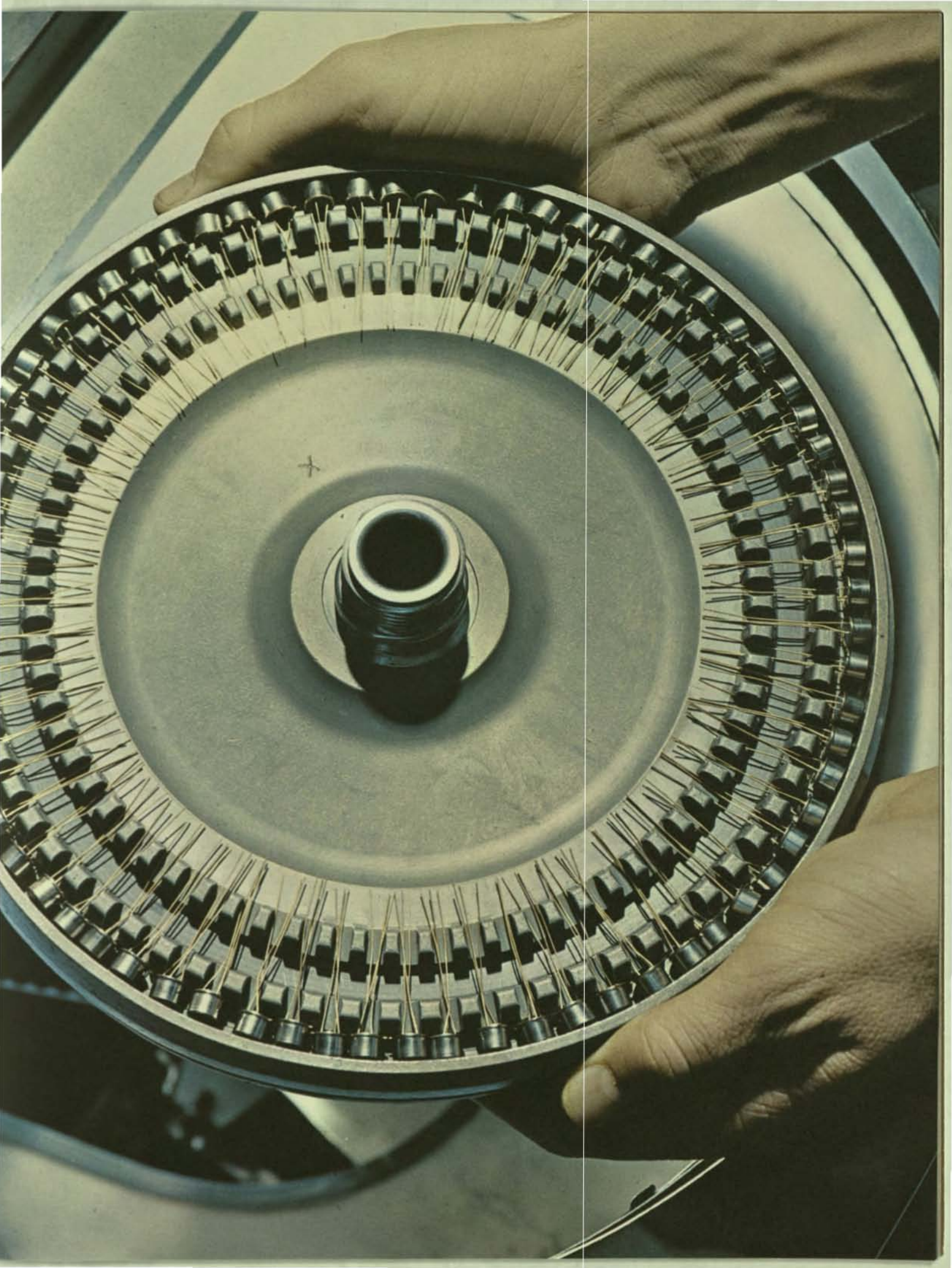
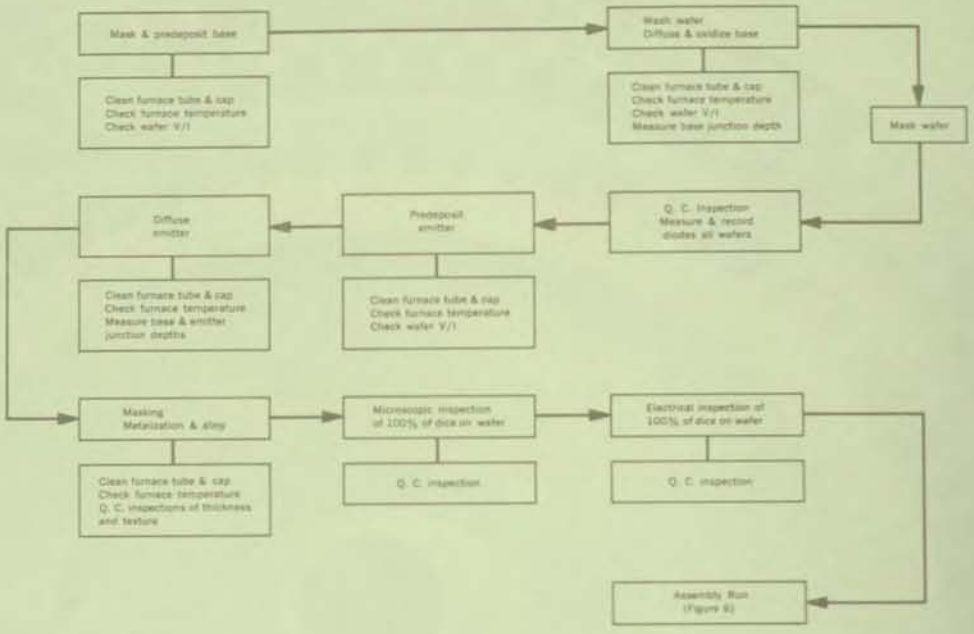


FIGURE 4
Wafer Fabrication



Maintaining Reliability by Tight Process Control

10 Thus the problem is not how to make a reliable product. Fairchild products are reliable. The question is how to maintain reliability. The answer, since we know our processing techniques produce a good product, is tight process control. We have written specifications; we check each step to make sure the operators are following the specifications; we 100% visually and electrically test all units frequently during processing and assembly; we make control charts to compare today's data with those of yesterday, last month and last year; when devices do not meet the exacting Fairchild standards, we submit them to a thorough defect analysis to pinpoint the problem; and we take corrective action.

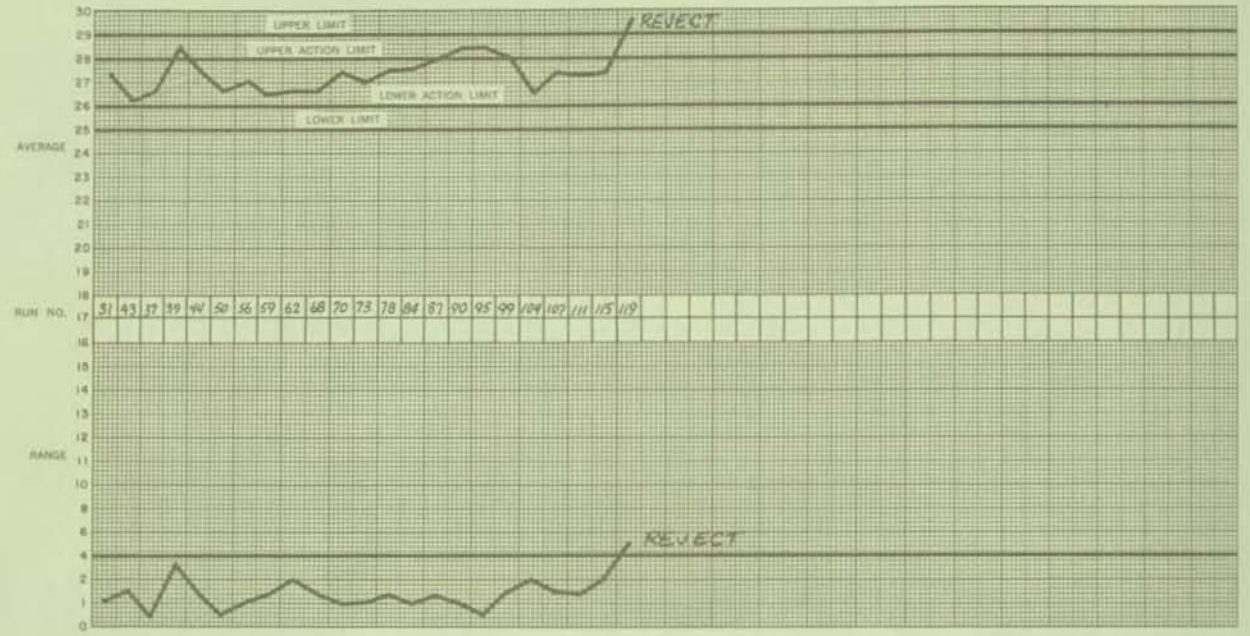
Wafer fabrication

Figure 4 shows the typical procedures followed in wafer fabrication and routine step-by-step cleaning and checking done to assure continuity of process. At each step the furnace tube and cap are cleaned according to specification, furnace temperature checked, and the wafer measured to determine surface leakage. These V/I calculations are plotted on control charts and compared graphically with limits set by specification (see Figure 5). In this way the slightest process deviation is corrected as soon as it occurs.

Wafers of identical resistivity are processed together. This is done because the electrical parameters of final units are determined by wafer resistivity – wafers of the same resistivity producing a tight parameter distribution. If wafers were chosen at random, even from the same crystal, parameter spread in finished units would be so wide that any slight change in "typical" values might pass unnoticed. Thus it is essential to isolate identical-resistivity wafers and process them together.

Operator's view of planar transistor on completed wafer.

FIGURE 5
Typical diffusion control chart.



100% visual and electrical inspection of all dice on each wafer

All dice on each wafer are 100% visually inspected by manufacturing personnel according to carefully detailed specifications, and samples of their work are inspected hourly by Quality Control inspectors to make sure the specification is met. At the wafer test station each die on the wafer is electrically inspected, and the electrical inspection is sample-checked hourly by Quality Control inspectors to ensure process stability. Control charts comparing typical parameters with specified limits quickly reveal any errors in process or machine calibration.

Assembly

Similar tight process control is exercised in the assembly of every product type – diodes, transistors, and microcircuits. The techniques which produce the most reliable product depend on the characteristics of the family and may vary slightly with the product, but on all assembly lines in every Fairchild plant the same principles apply: (1) strict adherence to written specifications; (2) step-by-step monitoring to screen imperfect units and remove their cause; and (3) immediate feedback to correct the slightest process deviation. Figure 6 shows the steps followed in the assembly of all products. Note that after die attach, lead bond, and lead weld, samples of each operator's work are tested by Quality Control inspectors and a control chart of her work plotted as illustrated in the photograph on the facing page.

100% environmental tests on all units after assembly

At the end of the line all units undergo rigid environmental tests listed in inserts to the data sheet for each product type. The tests are designed to stress the structure and package of the units so that substandard units will be rejected by the 100% electrical classification tests that follow. Figure 7 describes the tests. All units are subjected to temperature cycling, dynamic tests (shock at 30 to 60 KG's or centrifuge at 20 KG's), a hermeticity test such as the Joy bomb, oil bath, or Radiflo, and aging for more than 24 hours at 200°C. In all cases the 100% processing is designed to segregate mechanically substandard units.

Control chart of operator's quality posted at operator's position.

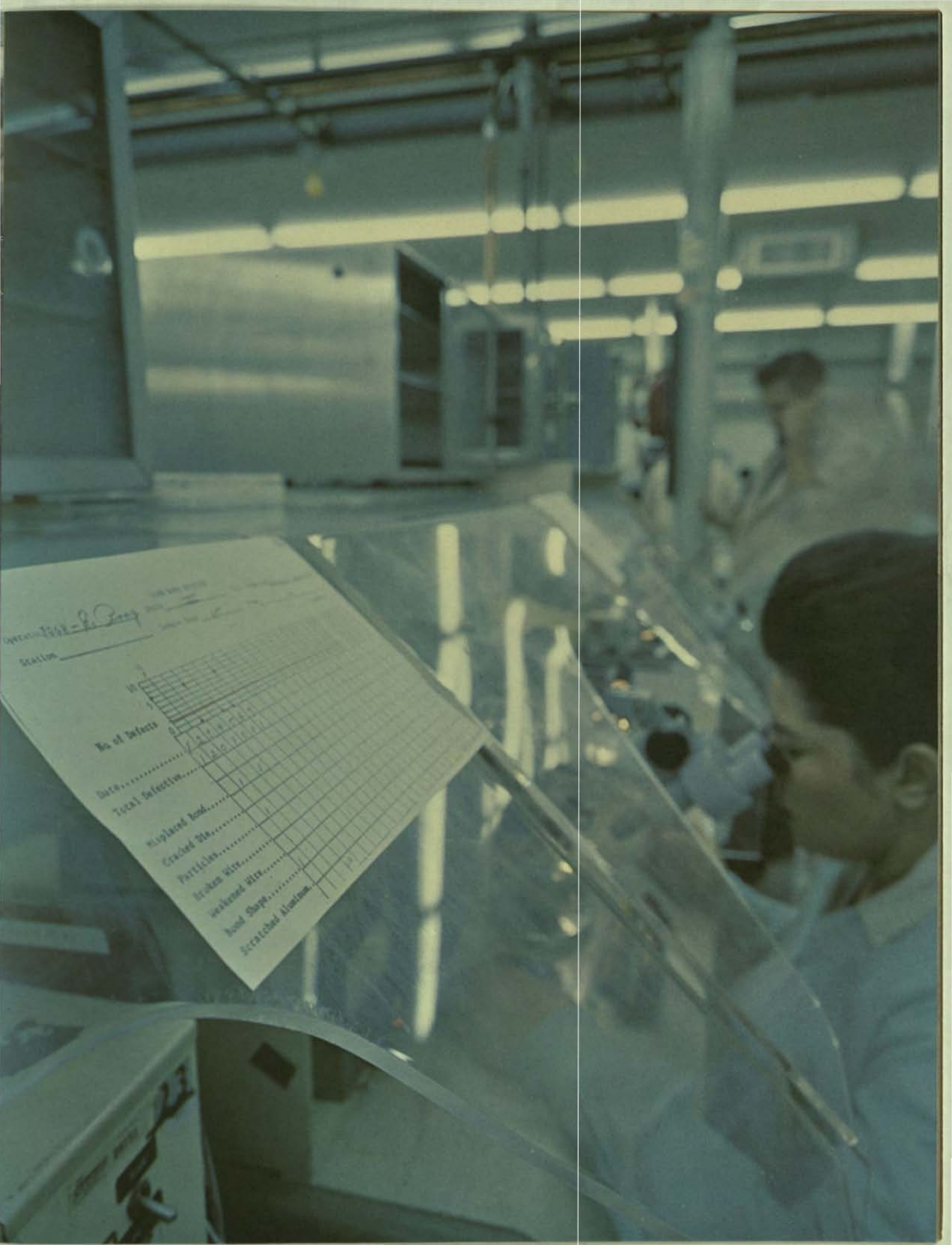
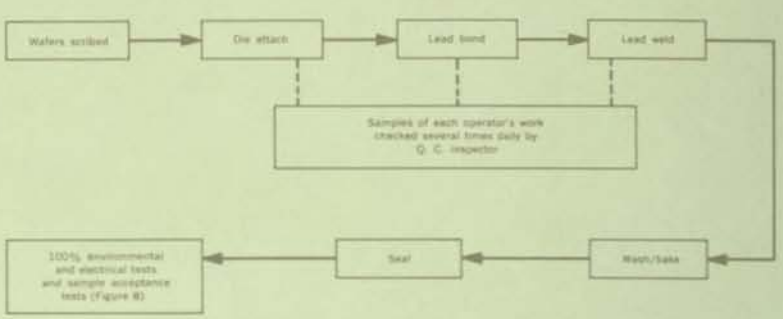

Station
No. of Defects
Date
Total Defective
Misplaced Bond
Cracked Die
Particles
Broken Wire
Weakened Wire
Bond Shape
Scratched Aluminum

FIGURE 6
Assembly Run



14 **100% electrical classification tests on all units after assembly**

Before an assembly run undergoes 100% electrical classification, test equipment is checked to assure proper calibration and programming, and a random sample is classified. From this sample, data are recorded and analyzed. Any fallout devices are studied to determine the reason for deviation from specifications. If necessary, units are sent to the Defect Analysis Department for a thorough analysis to ensure that product engineering has constant feedback relative to fallout or possible fallout trend.

If the sample reveals no inconsistencies, 100% of the units in the run are then electrically classified. As many as 100 different electrical tests may be performed at this time.

Transistors and special devices such as matched units are tested on the Fairchild 200 tester, which tests 1500 transistors per hour and checks its own calibration before each test. Microcircuits are tested on the Fairchild series 4000 tester, a very rapid (17 msec per test), completely digital machine with a magnetic disc for storing programs.

Fairchild integrated circuits mounted in Fairchild-developed universal carriers sliding into the automatic Fairchild series 4000M tester. This machine tests both flat and header-type packages with up to 20 active leads at a rate of 60 Go/No-go decisions per second. Final electrical classification and testing of microcircuits is done on this machine.

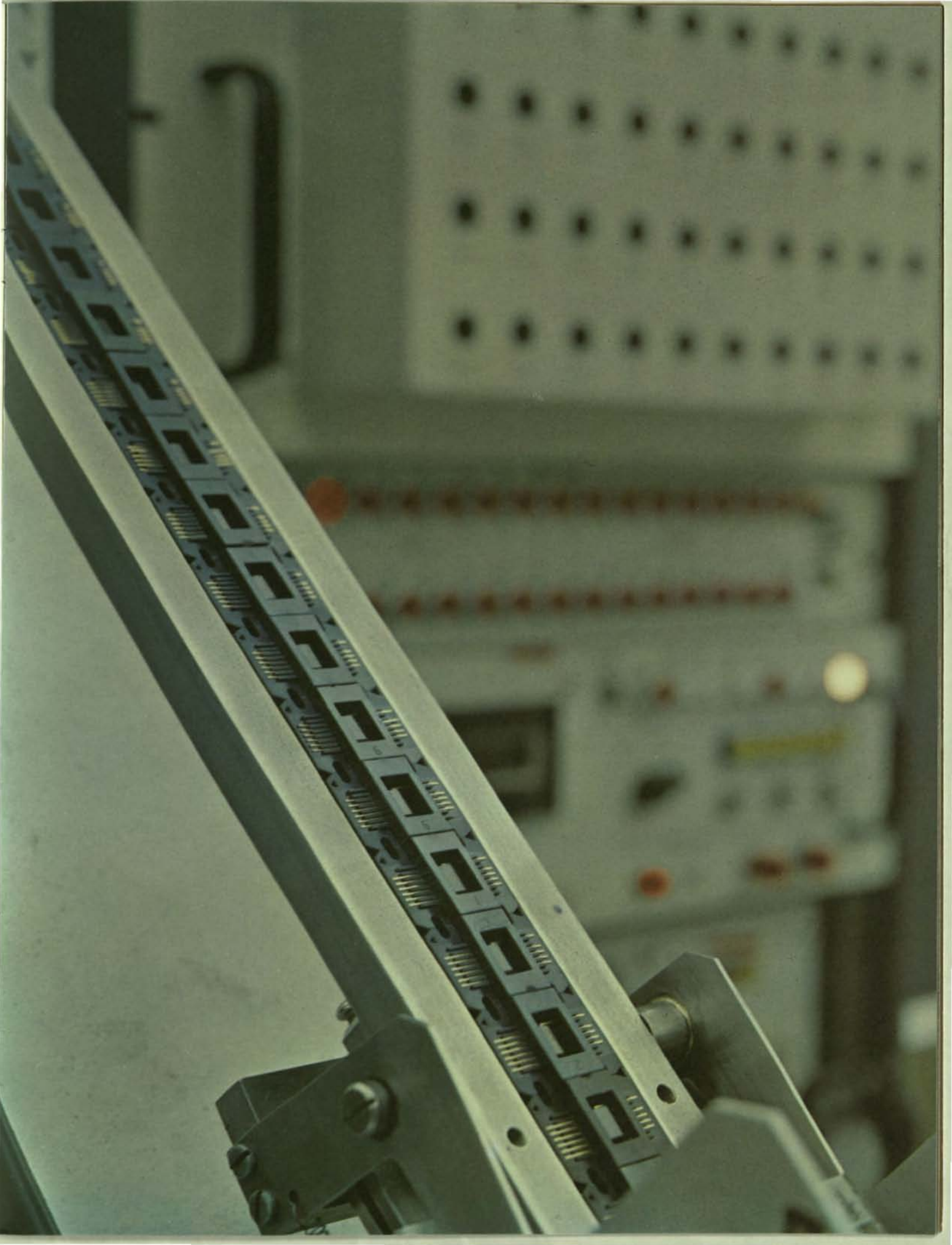


FIGURE 7
100% Environmental Tests

A. Temperature cycling (to stress hermeticity)

Device is subjected to temperature extreme (e.g., −65°C), allowed to stabilize, returned to room temperature, subjected to opposite extreme (e.g., 200°C), and returned to room temperature; usually 2 cycles, 15 minutes at extremes, 5 minutes transfer time (see data sheet).

B. Dynamic tests (to stress bonding/welding)

1. High-impact shock. Units are shot from Fairchild-designed pneumatic air guns ("Pressjectors") against a nylon plate with a steel backing. G levels on impact: 30 to 60 KG's.

2. Centrifuge. Device is centrifuged at acceleration of 20 KG's for 1 minute.

C. Leak tests (to check package)

1. Joy bomb. Device is placed in a chamber with water and detergent. Gas is pumped in under pressure to force liquid into the can if possible.

2. Oil bath. Device is immersed in hot oil. Any slight opening in the package produces a bubble in the oil.

3. Radflo. Device is subjected to radioactive gas under pressure and checked for signs of radioactivity. Limits are allowed to vary from 10^{-6} cc/sec for some products to 10^{-9} cc/sec for others.

D. Aging

Device is baked at 200°C for more than 24 hours.

16 **Training and motivation of operators**

Because in the final analysis the quality of the manufacturing process depends on the performance of each line operator, all Fairchild operators are thoroughly trained and motivated to produce consistently high-quality products. New operators undergo training periods averaging two weeks and must meet rigid quality standards before taking their place in the line.

Each operator's work is checked several times daily by a Quality Control inspector and a control chart of her quality is kept beside her position. If her performance falls below the quality standard, she is sent back for retraining as a new operator. Periodic salary reviews are based on the quality of her work. In addition, operators are encouraged in every way to take pride in their craftsmanship. They learn from experience as well as from observation that only personnel of high caliber can perform the delicate operations involved in the manufacture of semiconductor products. They are constantly reminded by posters, periodic lectures, and training movies that Fairchild products are used in missiles and satellites in which reliability is essential to national prestige – perhaps to national survival.

Classification indicator on the Fairchild series 200 tester. Any combination of 24 tests is possible with this tester in any sequence using only 4 plastic punched cards. The test rate with all 24 tests in use is approximately 1500 transistors per hour.

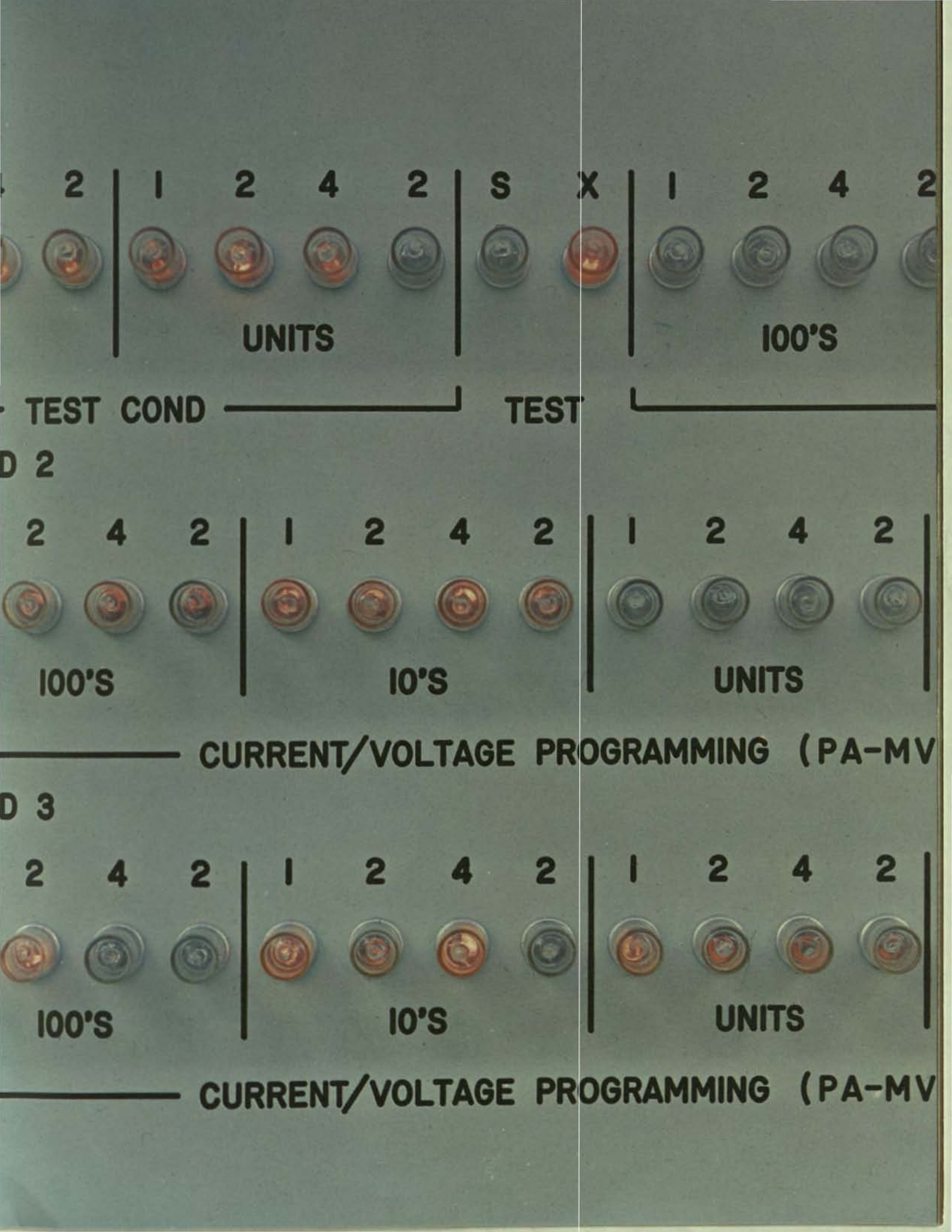
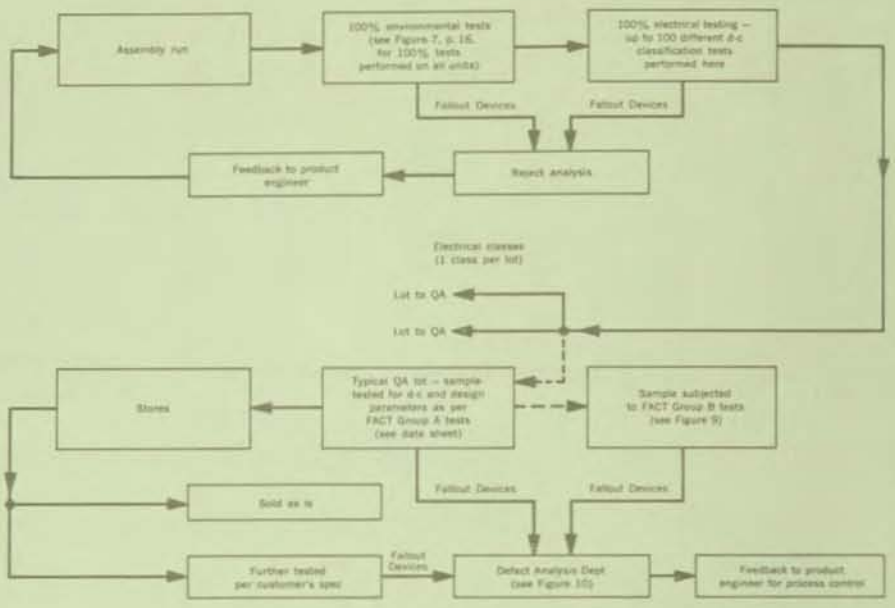

2
1 2 4 2
S X
1 2 4 2
UNITS
100'S
TEST COND
TEST
D 2
2 4 2
1 2 4 2
1 2 4 2
100'S
10'S
UNITS
CURRENT/VOLTAGE PROGRAMMING (PA-MV
D 3
2 4 2
1 2 4 2
1 2 4 2
100'S
10'S
UNITS
CURRENT/VOLTAGE PROGRAMMING (PA-MV

FIGURE 8
Standard Fairchild Tests



Assuring Reliability by Comprehensive Testing

18 In addition to Quality Control inspections after each step in the processing and assembly and 100% testing at the end of the line, we also rigorously test incoming direct materials as a matter of routine. Tests performed on incoming direct materials include:

1. Chemical and spectrographic analyses of wire and preform;
2. Functional tests to duplicate the actual environment experienced in manufacture;
3. Checking of wire tensile strength by the Instron Tester;
4. Checking of all dimensions spelled out in the blueprint.

Routine lot acceptance tests

Test facilities at Fairchild include over 225,000 sockets for operating life tests, many high-temperature storage chambers, each capable of storing hundreds of thousands of devices, and complete equipment for environmental testing: shock and vibration equipment, temperature cycling, thermal shock equipment, moisture resistance chambers, lead fatigue and lead tension equipment, Radiflo, etc. All units, regardless of where they are assembled, are subjected to the same rigorous Quality Assurance tests (see Figure 8). Each lot, identified by product type and electrical characteristics, is electrically sample-tested on the Fairchild 500 series tester, a direct-reading, data-logging instrument with a unique digital measuring technique which permits an unusually high degree of repeatability and accuracy. Not only are the parameters previously 100% tested rechecked at this time, but additional a-c and design parameters considered in the industry to be the most critical are also tested in accordance with MIL-S-19500 and MIL-STD-105.

After these routine sample acceptance tests the lot is either placed into stores or sent back for 100% rescreening if it exceeds the required LTPD or AQL.* Depending on the customer's requirement, lots available for sale are (1) sold without further tests, (2) electrically screened (if the customer requires a tighter parameter spread), or (3) electrically screened and also given further high-reliability processing, such as burn-in, x-ray, etc. Approximately 100,000 units are burned in and individually tested each month for use in missile and space systems.

*LTPD — Lot Tolerance Percent Defective
AQL — Acceptable Quality Level

Lead tension equipment capable of exerting up to 150-oz pull on each lead.

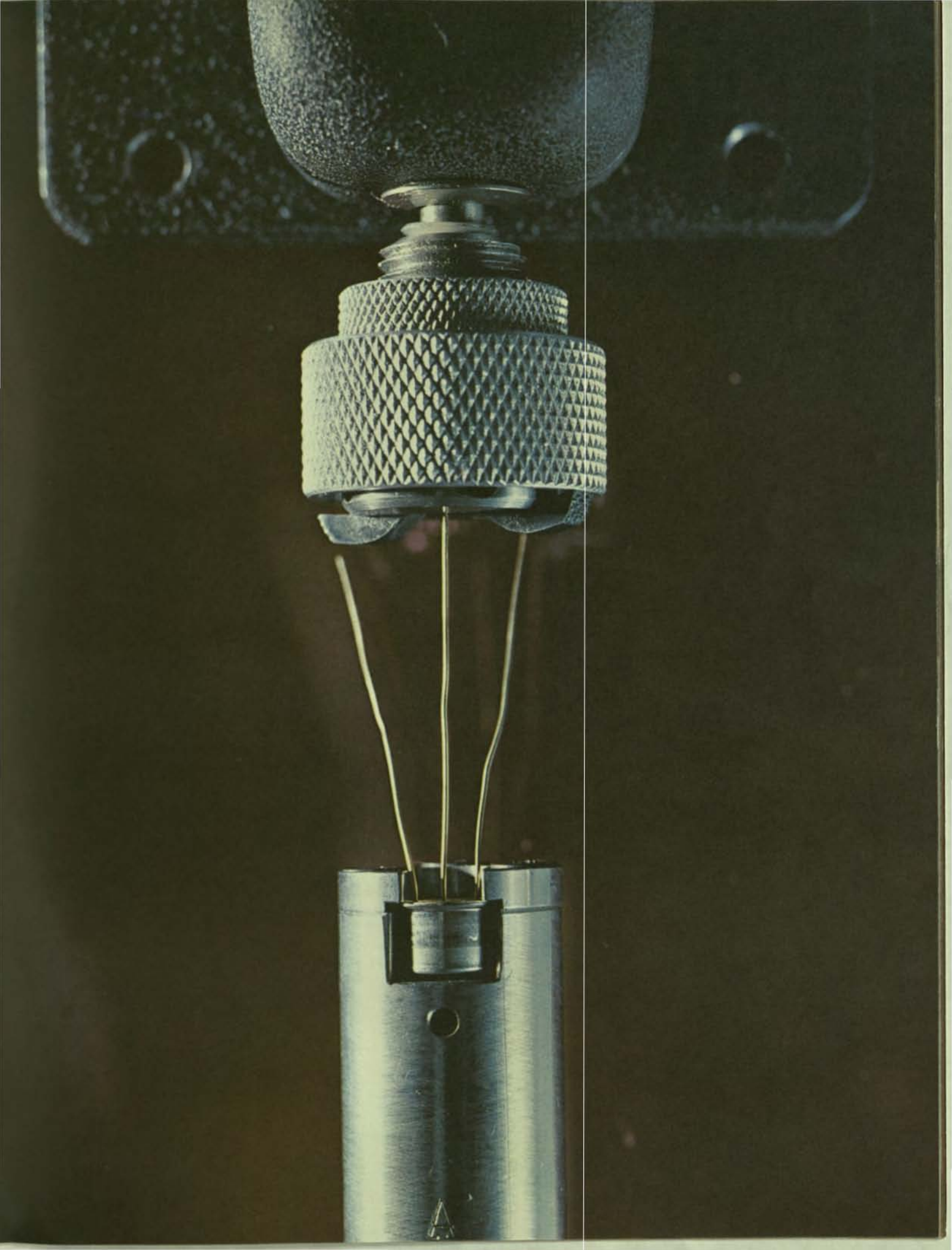
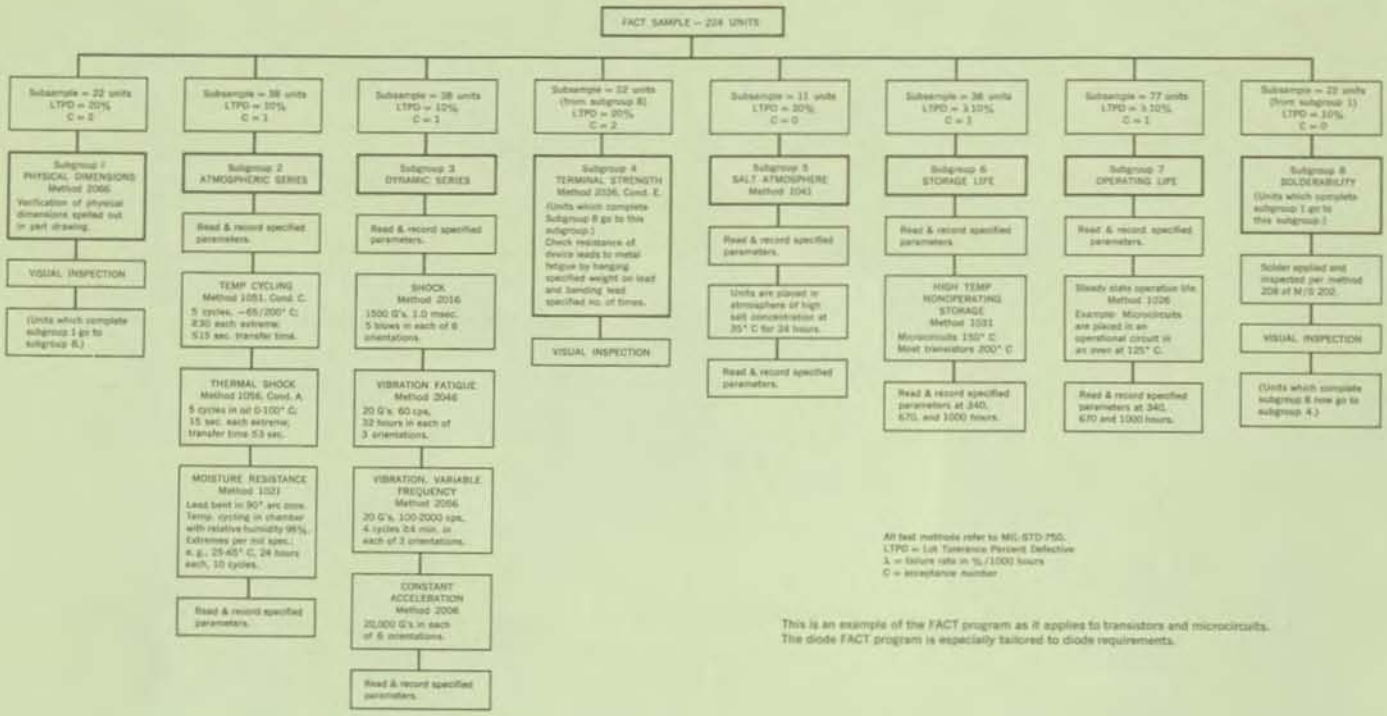


FIGURE 9
Fairchild Assured Component Test (FACT) Program



All test methods refer to MIL-STD-750.
LTPD = Lot Tolerance Percent Defective
λ = failure rate in %/1000 hours
C = acceptance number

This is an example of the FACT program as it applies to transistors and microcircuits. The diode FACT program is especially tailored to diode requirements.

20 This is true 100% high-reliability processing, since parameters (typically 5 but can be many more if the customer desires) of each unit are measured before and after burn-in and the data are included with each device shipped. Testing is done on the Fairchild 500 series tester, which punches IBM cards for each unit. It has been estimated that on some contracts Fairchild ships anywhere from 10 to 50 pounds of reliability data for each pound of devices sold!

The FACT program — comprehensive lot reliability verification

Procurement specifications which call for a special, complex series of tests sometimes cause shipment delays and extra costs. The Fairchild FACT program fulfills the requirement for reliability processing without special handling; it provides our customers with comprehensive lot reliability verification at minimum cost and without delay.

Most special procurement specifications call for various 100% environmental and electrical tests performed as a matter of routine at Fairchild, plus additional sample tests such as operating life, shock, salt atmosphere, etc. Under the FACT program we list all 100% environmental and electrical tests with the data sheet pertaining to each device, giving guaranteed parameter values. In addition we take samples from every week's production of each device after it has passed the 100% environmental and electrical tests and routine Quality Assurance tests, and we perform the Group B inspection shown in Figure 9. The FACT program, recently revised, has shortened the test time and tightened the test conditions. The quality conformance inspection is in strict accordance with MIL-S-19500. The tests performed are those set forth in MIL-STD-750, and in most cases the test conditions and limits are more stringent than specified in the pertinent military specification. Notice in Figure 9 that specified parameters are read and recorded before and after operating life tests and various stress tests. The parameters chosen (see data sheet for specific parameters chosen for each device) are those

Fairchild data sheets with the FACT program offer a complete procurement specification which can be referred to as a purchase contract.

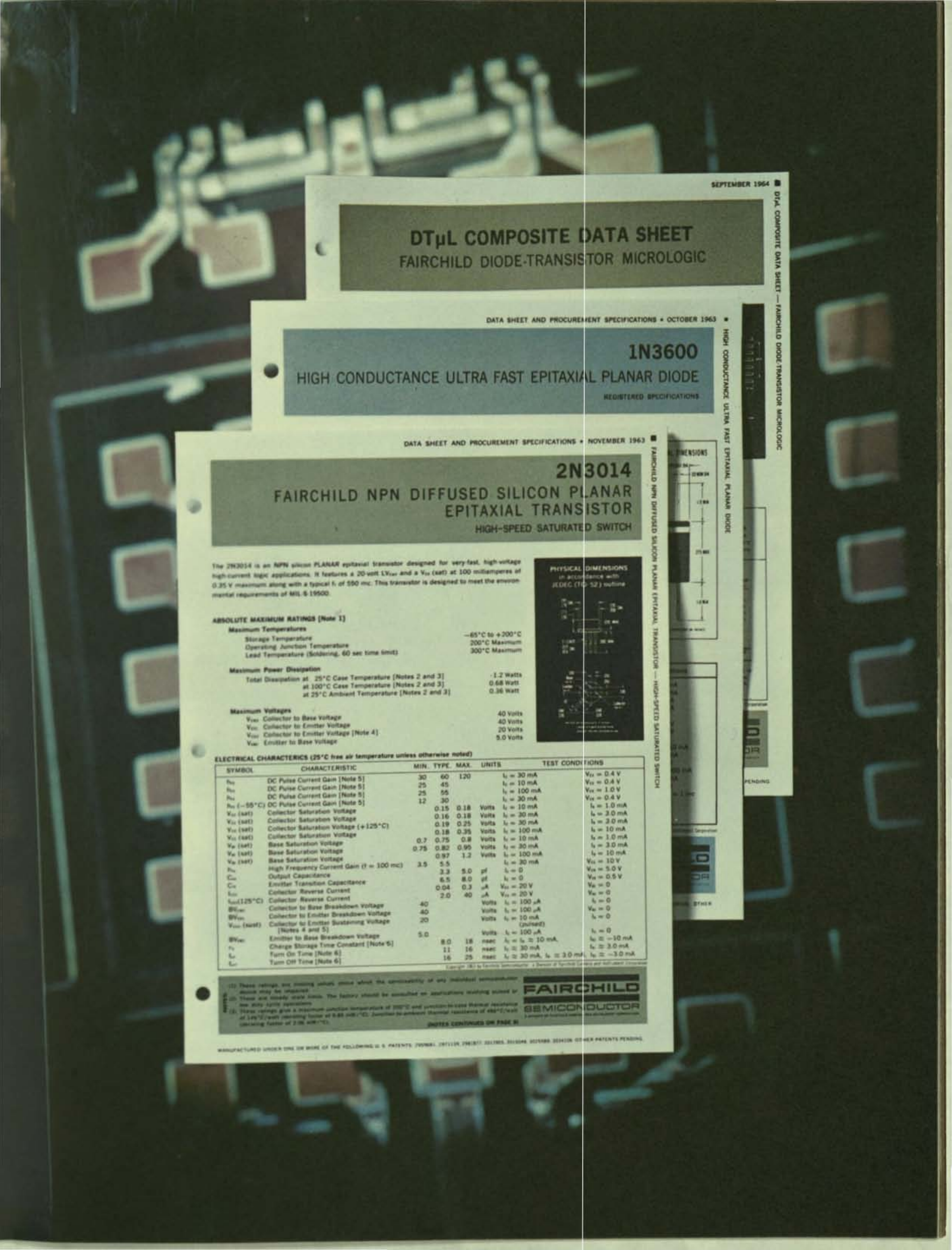
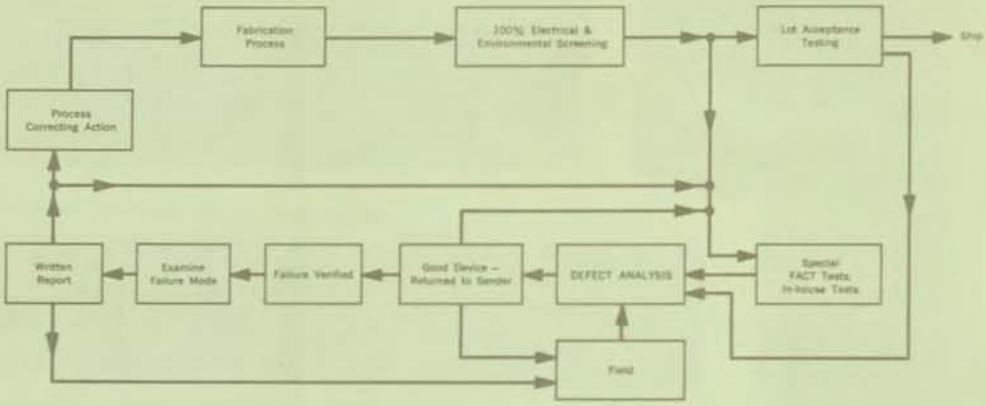

SEPTEMBER 1964
DTμL COMPOSITE DATA SHEET
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC
DTμL COMPOSITE DATA SHEET — FAIRCHILD DIODE-TRANSISTOR MICROLOGIC
DATA SHEET AND PROCUREMENT SPECIFICATIONS • OCTOBER 1963
1N3600
HIGH CONDUCTANCE ULTRA FAST EPITAXIAL PLANAR DIODE
REGISTERED SPECIFICATIONS
HIGH CONDUCTANCE ULTRA FAST EPITAXIAL PLANAR DIODE
DATA SHEET AND PROCUREMENT SPECIFICATIONS • NOVEMBER 1963
2N3014
FAIRCHILD NPN DIFFUSED SILICON PLANAR
EPITAXIAL TRANSISTOR
HIGH-SPEED SATURATED SWITCH
FAIRCHILD NPN DIFFUSED SILICON PLANAR EPITAXIAL TRANSISTOR — HIGH-SPEED SATURATED SWITCH
PHYSICAL DIMENSIONS
ABSOLUTE MAXIMUM RATINGS (Note 1)
Maximum Temperatures
Maximum Power Dissipation
Maximum Voltages
ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)
SYMBOL
CHARACTERISTIC
MIN.
TYPE.
MAX.
UNITS
TEST CONDITIONS
FAIRCHILD
SEMICONDUCTOR

FIGURE 10
Tight Process Control Through Defect Analysis and Feedback



considered in the industry to be the most critical, providing the best measure of device reliability. The FACT data supplied to the customer verify the fact that the line has been running smoothly and on a continuous basis. Thus the customer can maintain a high degree of confidence that the devices are in fact high-reliability units.

Options

The FACT program offers a variety of options which meet almost any high-reliability requirement, including 100% burn-in on all devices purchased by the customer. These options provide high-reliability testing with optimum delivery and minimum cost.

Defect analysis and feedback

An essential step in tight process control is the analysis of any out-of-tolerance units that may occur in lot acceptance and FACT test programs, and, on rare occasions, in the field,* in order to determine failure modes and permit corrective action by the product engineers. Figure 10 shows the vital function performed by the Defect Analysis Department at Fairchild. This department is equipped with all needed equipment: an infrared scanner, curve tracers, electrical test jigs, photographic equipment (both color and black and white), microscopes, microprobes (to probe the die when electrical connections have been severed), and equipment for potting, sectioning, staining and etching units.

*Of the 40 million devices sold between the months of August and December, 1964, 0.00012% were returned to the factory because of device defects.

Also, Research and Development facilities, including an electron beam microscope, are available for defect analysis. In addition to the regular analysis of all units submitted to it, the Defect Analysis Department does literature researches and maintains contact with suppliers to keep up to date on techniques and equipment for analysis. Each device is either (1) found to be still good and therefore returned to the originating department or (2) if the failure is verified, subjected to a thorough analysis to discover the cause. Was the failure due to an inherent defect in the device or was it due to misapplication of the device? Was the damage electrical or physical? Etc. In each case a detailed report is written and submitted, with photomicrographs of the device, to the line engineer for corrective action as well as to the originating department.

Fairchild series 500C tester with tape programming option, which increases the number of parameters that can be tested in any sequence and in any combination from 12 to a number limited only by the length of the tape, at 1 test per inch. Test results are available in direct digital reading display and digital outputs, which can be adapted to drive optional readouts such as printout, typeout, and card punch.

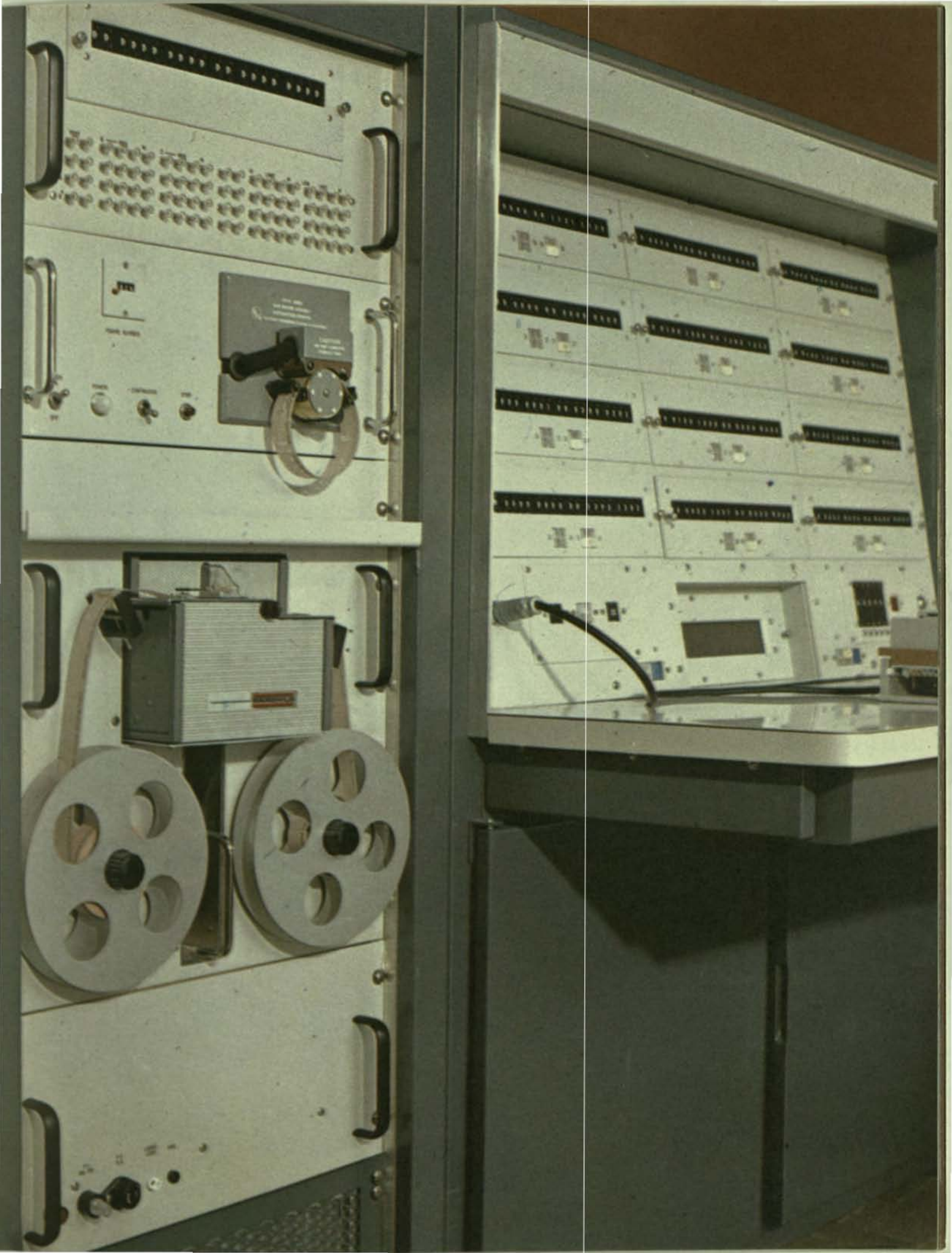
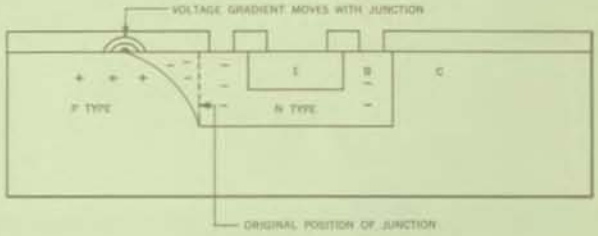


FIGURE 11
Cross-sectional view of pre-PLANAR II PNP transistor showing inversion layer.



Designing Reliability into the Product

Since its beginning as the first large-scale producer of silicon transistors, Fairchild has led the industry in developing and improving reliability and performance by improving the basic product design. Shortly after the silicon mesa transistor had become accepted as the most reliable transistor available, Fairchild made a second giant evolutionary step: the Planar process. This process was – and is – an invaluable tool for solving problems in transistor technology, opening up areas of development previously impossible. One of its most fruitful outgrowths has been the monolithic integrated circuit – another Fairchild "first." A new order of reliability for circuit functions was established by this development – comparable to that of a single transistor.

The steps involved in making a transistor by the Planar process are essentially the same as those required to make a diode or integrated circuit, differing primarily in the number and order of diffusions. Aside from refinements such as the addition of an epitaxial layer, this Planar technique is the same as that used today in manufacturing all Fairchild semiconductor devices. The secret of the vast increase in reliability introduced by the Planar process lies in the fact that all junctions are formed beneath the oxide layer and are never exposed to atmospheric contaminants. As a result all characteristics which are sensitive to surface conditions – reverse leakage current, breakdown voltage, noise figure, current gain, and therefore reliability – are vastly improved.

The third giant evolutionary step made by Fairchild in improving reliability was the public introduction in autumn 1964 of Planar II, a complex and highly proprietary method of growing stable oxides. This process makes it possible to produce PNP's with voltage breakdowns in excess of 200 volts and reliability figures equalling those of the finest NPN transistors. It also makes possible mass production of practical MOS FET's (such as the Fairchild FI 100) capable of withstanding electric fields of the order of 2 million volts per centimeter without dielectric charge migration.

Cross-sectional view of silicon chip enlarged 200X showing a typical gold ball bond.

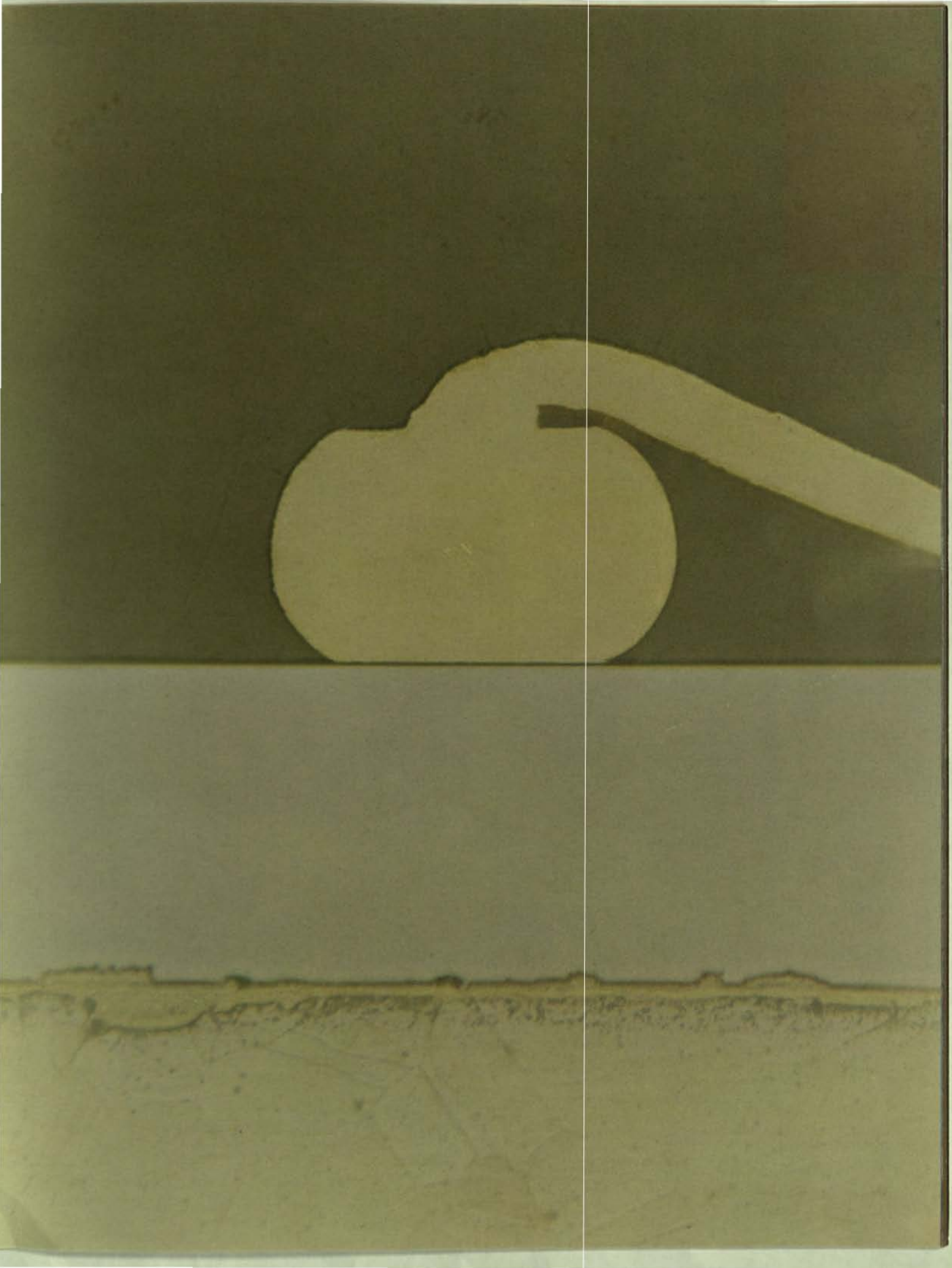
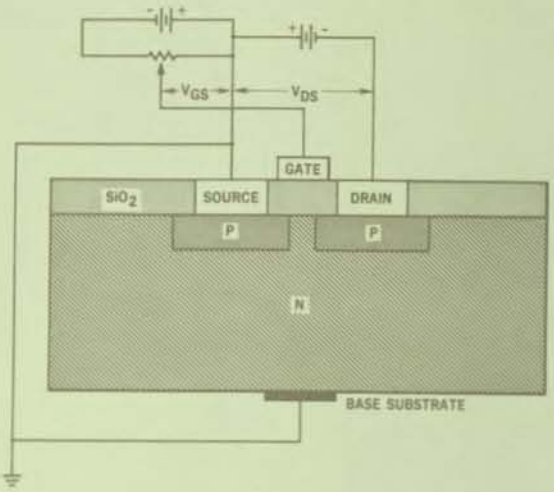


FIGURE 12
Cross-section of P-type MOS FET with correct biasing polarity.



The problem in PNP's solved by PLANAR II is briefly summarized as follows:

In a diffused transistor the collector is very lightly doped compared to the base and emitter. This is particularly true of high-voltage transistors, in which very light collector doping is used to increase the voltage breakdown characteristic. The oxide layer in the ordinary Planar device is not a purely passive coating but tends to be quite heavily loaded with mobile positive ions. The voltage gradient across the junctions in the silicon beneath the oxide extends into the oxide and causes the ions to cluster about the junction at the interface.

The positive ions affect the majority carriers in the silicon and can actually invert the polarity of lightly doped P-type material to N-type.

This fact causes no particular problem in the NPN transistor. Its N-type collector merely appears more heavily doped than would be expected and its P-type base is too heavily doped initially to be inverted; but, it can be a serious problem in a PNP as shown in Figure 11.

If inversion takes place adjacent to the collector-base junction, in effect the junction is extended, causing increased leakage and reduced breakdown voltage. When the junction moves along the interface, the force field – and thus the ions – moves with it. As the junction "creeps" along the interface, leakage continues to increase. The new junction formed between the inverted N and the non-inverted P portions of the collector has very poor electrical characteristics and, if large enough, renders the device useless. Inability to control the inversion layer (known as a "channel") in pre-Planar devices made it difficult to build high-yield, reliable PNP transistors.

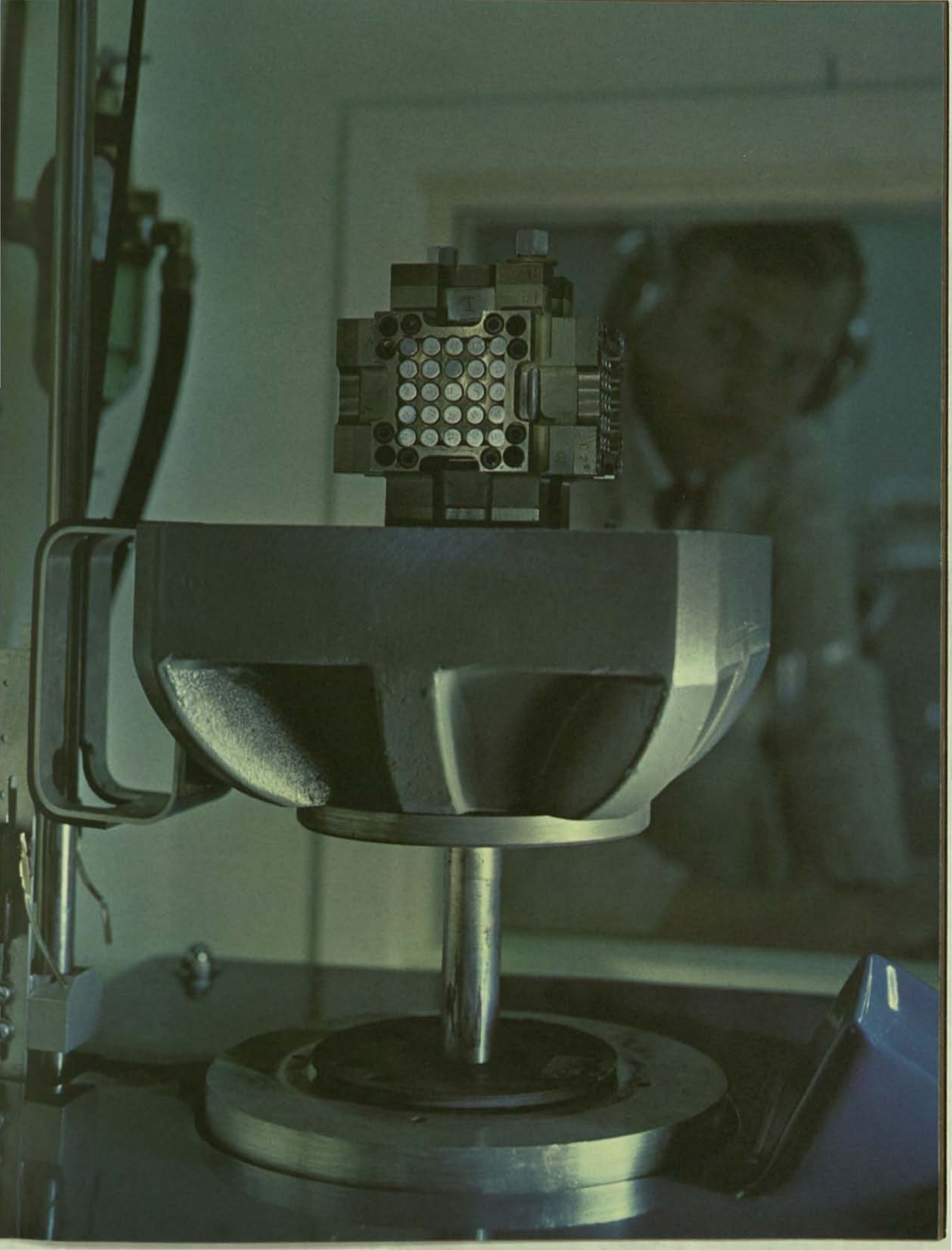
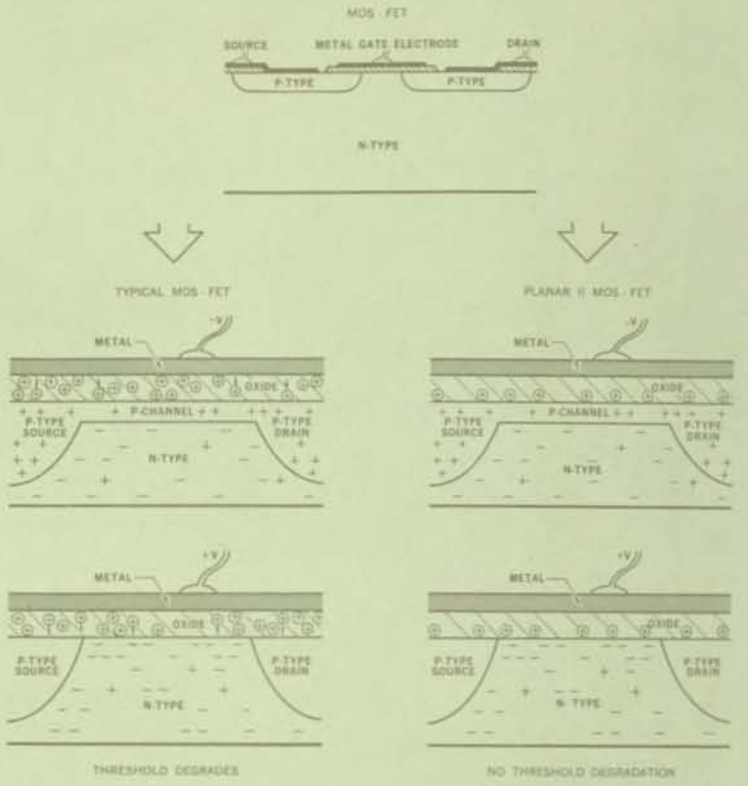


FIGURE 13
Comparison of PLANAR II MOS FET with pre-PLANAR II type.



28 A similar problem exists with the pre-PLANAR II MOS FET. Figure 12 shows a cross section of a P-type MOS FET with correct d-c biasing polarities. In this MOS FET a negative gate voltage V_{GS} produces a P-type channel in the N-type silicon beneath the gate so that current can flow from source to drain.

Unfortunately V_{GS} induces a voltage gradient across the oxide. The resulting changes in gate threshold voltage and capacitance due to ionic drift in the oxide are depicted graphically in Figures 13, 14, and 15. Note that in the PLANAR II device ions are completely immobilized and oxide stability increased by three orders of magnitude (100V change versus 0.1V change). Among the advantages are:

1. Complete elimination of channel development;
2. Stability at operating junction temperatures of 175°C;
3. Stability at storage temperatures of 200°C.

Process refinements:
Gold ball bond

The experience gained in manufacturing Planar devices naturally led Fairchild engineers to the development of new processing techniques and new test equipment. The gold ball bond, used in Minuteman transistors and today a standard technique throughout the industry, is one example. Before the invention of this type of bond the gold lead was commonly

Devices mounted inside a heated salt-mist chamber (subgroup 5 of FACT program).

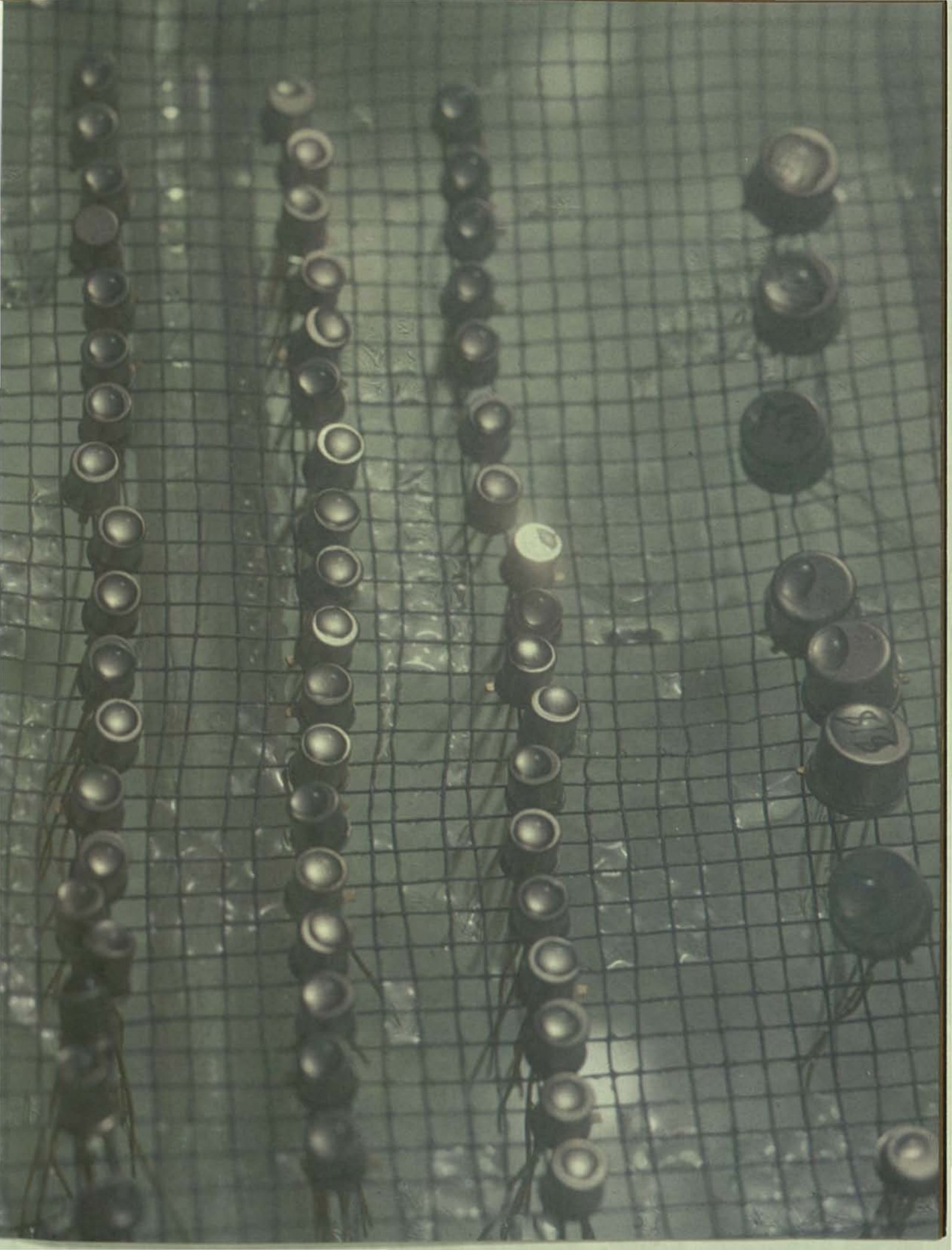
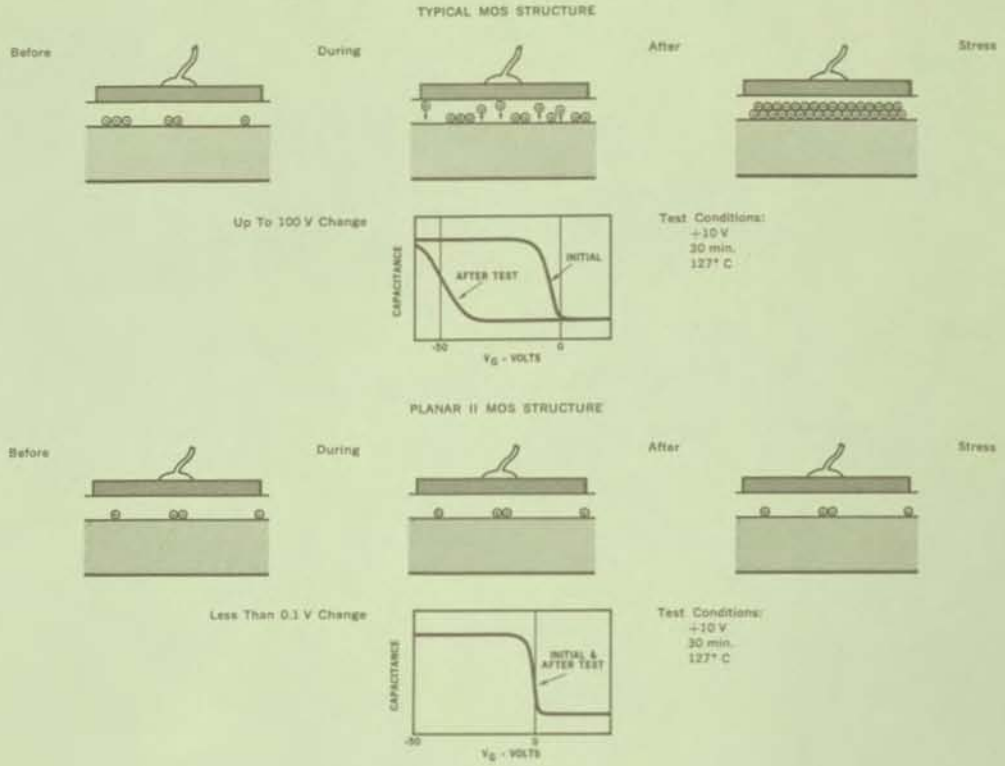


FIGURE 14
The Physics of PLANAR II oxide stability demonstrated in a metal oxide capacitor.



applied to the bonding pad by a wedge-shaped tool under heat and pressure, which tended to deform and weaken the lead. The "gold ball" bond is so called because a ball formed of melted gold at the tip of the wire is pressed against the chip by a capillary needle. This type of bond is more resistant to shock, contacts a larger area of the bonding pad, and permits the use of a larger wire.

Ultrasonic bond

A recent development at Fairchild is an adaptation of the ultrasonic bond for bonding aluminum leads. Among its advantages over the aluminum wedge bond are that it (1) does not appreciably weaken the aluminum or reduce its cross-sectional area, illustrated in the photograph on the facing page, and (2) requires no external source of heat. It is used in SCR's, power transistors, and in all flat-package integrated circuits.

Metal-over-oxide

Another major advance in processing techniques was the Fairchild-patented metal-over-oxide technique. This is a method of evaporating aluminum over the oxide in strips from the base and emitter to form large pads on the periphery of the chip, to which the leads are bonded. This method increased the reliability of all product families by providing a larger target for the bonding operation than the base and emitter stripes themselves. It was of particular importance in the development of high-speed, high-frequency devices, which require the smallest possible base and emitter areas.

Aluminum leads bonded by wedge bond (top) and ultrasonic bond (bottom).

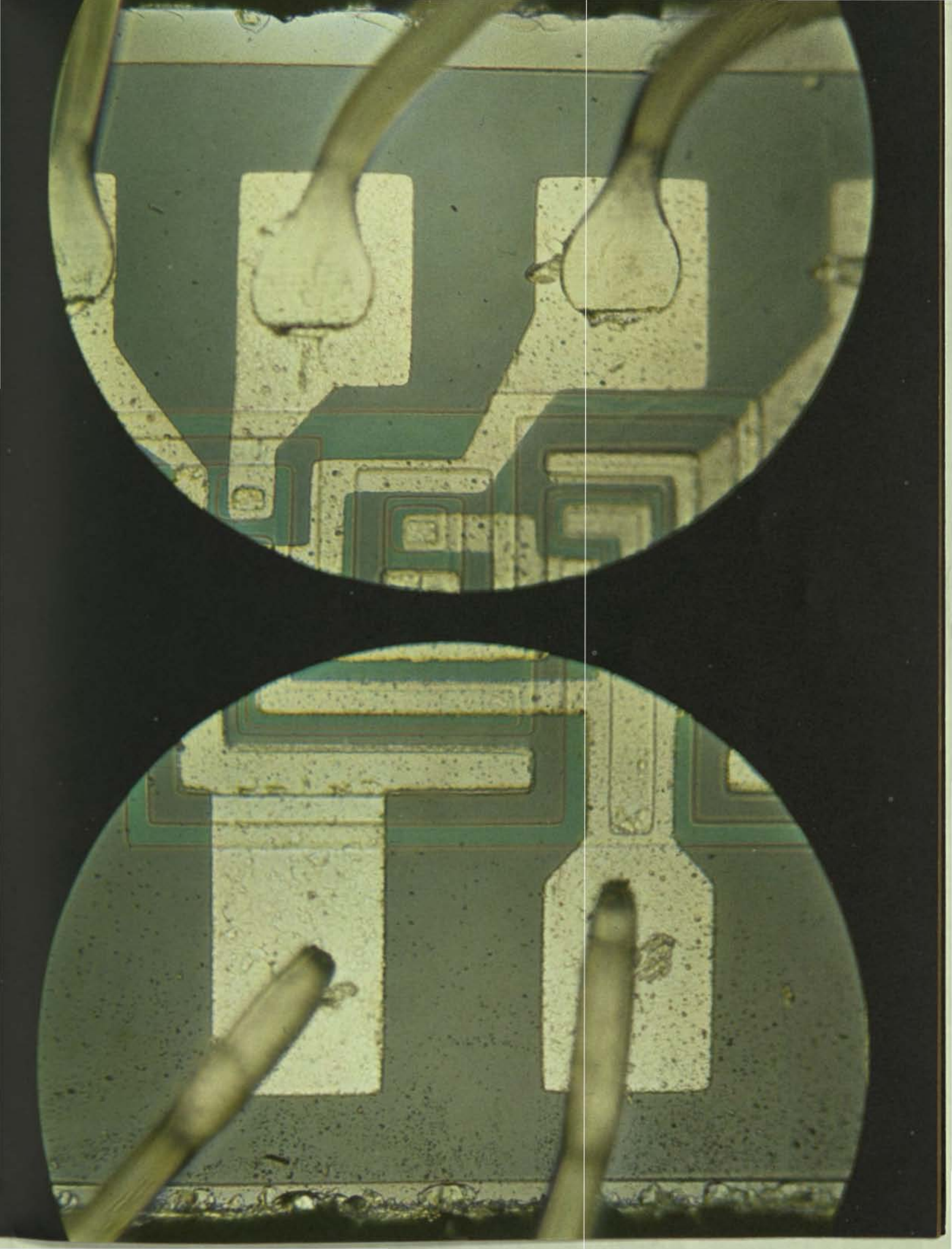
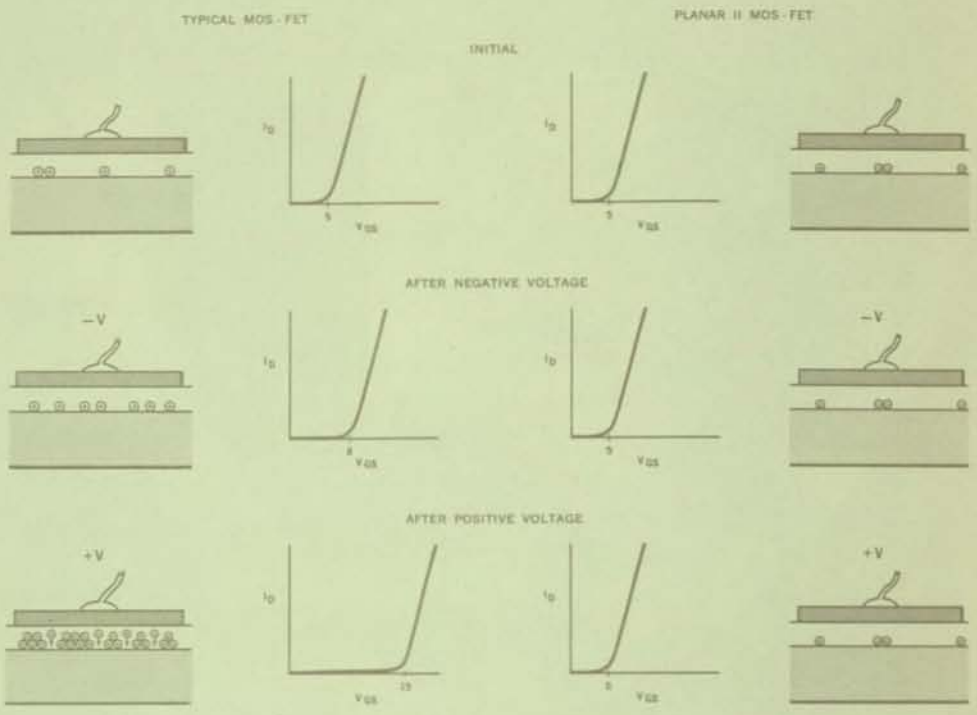


FIGURE 15
Threshold voltage is a function of ion migration.



Reliability is More Than Statistical Data

32 Statistical calculations of failure rate express reliability, but people create it: People in Research and Development who design devices with inherent stability; people in Manufacturing who rigidly follow procedures known to produce reliable products; people in Instrumentation who custom design equipment for testing every unit repeatedly during its manufacture; people in Quality Assurance who painstakingly check all phases of production from incoming materials, through manufacture, to end-of-line testing, in order to eliminate the slightest deviation as it occurs; people in management who focus attention on reliability. Fairchild is rich in creative, dedicated people. And these people, who invented and use the Planar process, continue to lead the industry in discovering and using new technological tools for building reliability – a tradition at Fairchild Semiconductor.

PLANAR, A PATENTED FAIRCHILD PROCESS. μL, DTμL, TTμL, MWμL, μLogic: FAIRCHILD TRADEMARKS. © FAIRCHILD SEMICONDUCTOR, A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT

FAIRCHILD

SEMICONDUCTOR

FAIRCHILD SEMICONDUCTOR, 313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA

Printed in U.S.A.

1988

The New York Times
SAN FRANCISCO BUREAU
925 FOX PLAZA BUILDING
SAN FRANCISCO, CALIFORNIA 94102
(415) 861-8662

Dear Bob -

Nice talking to you the other night. Here's the Fairchild story, as requested, which ran on the Business Page on Saturday, April 16. Hope you like it.

Regards,
Andy Pollack
S.F. Correspondent

ANDREW POLLACK

WEST COAST CORRESPONDENT
The New York Times
ONE EMBARCADERO CENTER
SUITE 1310
SAN FRANCISCO, CA 94111
415-362-3912

The New York Times/Terrence McCarthy

Founders of the Fairchild Semiconductor Corporation who gathered Thursday evening, from left: Victor Grinich, Jay Last, Jean Hoerni, Julius Blank, Eugene Kleiner and Sheldon Roberts. Seated, Robert N. Noyce, left, and Gordon Moore.

Fathers of Silicon Valley Reunited

By ANDREW POLLACK

Special to The New York Times

PALO ALTO, Calif., April 14 — When the eight men stepped onto the stage here, the crowd erupted into applause. The men, now aging and gray, had, in their day, been among the first of their kind — young technological whizzes who started a company, became fabulously wealthy and helped spark the electronics revolution.

The men were the founders, in 1957, of the Fairchild Semiconductor Corporation, a company that, more than any other, gave birth to what is now known as Silicon Valley. Last year, after a proposed sale to Japan's Fujitsu Ltd. caused a controversy, Fairchild was sold to the National Semiconductor Corporation.

With Fairchild now disappearing as a separate entity, the former employees gathered in a hotel ballroom here this evening for a final farewell, a celebration that was part reunion, part wake. More than 1,000 "Fairchildren" showed up.

"If you look back and see what has happened because of what you folks did, it is absolutely astounding," Robert N. Noyce, Fairchild's first leader, told the crowd.

"Like many people here, Fairchild changed my life," said Lyle Ronalds, a former salesman who came from Australia.

Fairchild was the first major company in the area

Continued on Page 21

Fathers of Silicon Valley Reunited

Continued From First Business Page

south of San Francisco to make semiconductors, the silicon chips that are used in computers, robots, missiles and all other electronic gear. Its founders, led by Robert N. Noyce, invented a key process that is still used to make such chips. Because of that invention Dr. Noyce is considered the co-inventor of the integrated circuit.

Fairchild served as a training ground for many of the leaders of today's electronics industry, who then went off to start their own companies. The companies include such stars as Intel, Advanced Microdevices, National Semiconductor and LSI Logic.

'Exploded Like a Seed Pod'

Fairchild "exploded like a seed pod and scattered the germs of new firms throughout the valley," Michael S. Malone wrote in his 1985 history of Silicon Valley, "The Big Score." Indeed, if one were to draw a family tree of Silicon Valley today, there would be hundreds of companies that had Fairchild at their roots.

To many here, Fairchild meant a hearkening back to simpler times in the 1950's and early 1960's when engineers wore crew cuts, technology was primitive and American know-how reigned supreme. It was a time of great hope.

"People really didn't know what it was going to amount to, but everyone knew that I.C.'s were going to be really big," said Robert K. Waits, referring to integrated circuits. Now an engineer at the Digital Equipment Corporation, he worked at Fairchild from 1960 until 1973.

Symbol of Decline as Well

Today the semiconductor industry is international, with huge sums of money and politically negotiated trade agreements meaning as much as technological innovation. And if Fairchild symbolizes the birth of the American semiconductor industry, it also symbolizes its decline. By the time it was sold last year, Fairchild had become a technological also-ran, its strength having been depleted by poor management and by numerous defections of its top engineers to new companies.

By 1968, virtually all the top management had left, and new management was brought in from rival Motorola Inc. The new management, headed by Lester Hogan, became known as "Hogan's Heroes." The most ambitious of these heroes, Wilfred C. Corrigan, ousted Mr. Hogan in 1974 and ran Fairchild until 1979, when he sold it for $425 million to Schlumberger Ltd., a French oilfield services concern.

Fairchild continued to decline under Schlumberger, losing hundreds of millions of dollars and earning the nickname "Schlumchild." In 1976, Schlumberger tried to bail out by selling most of its stake to Japan's Fujitsu Ltd. The agreement collapsed after protests from American industry and Government officials, who feared transferring key technology to Japanese competitors, and National then bought it last October for $122 million.

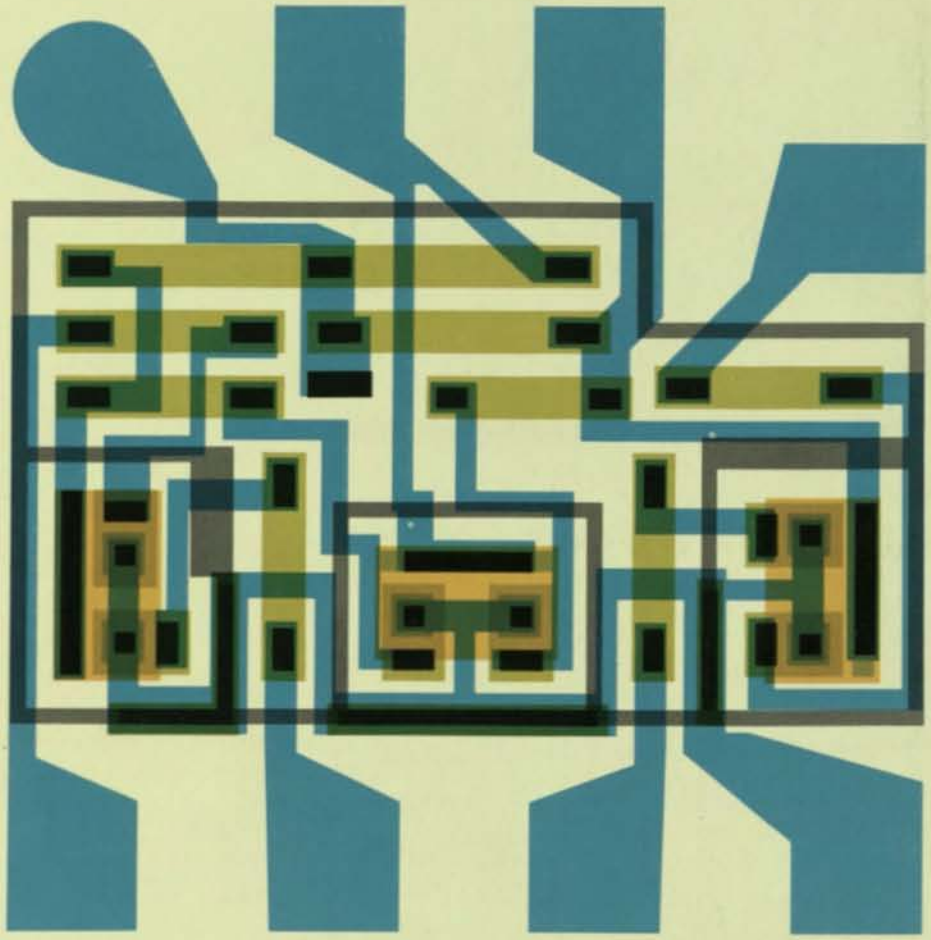
To keep the name alive, National today named a new corporate laboratory the Fairchild Research Center.

"Fairchild's spirit lives on within National," Charles E. Sporck, National's president and a Fairchild alumnus, said in dedicating the building.

Job hunting? Check today's Times.

FAIRCHILD EPITAXIAL MICROLOGIC

[redacted]



This brochure describes the process used to produce the most advanced, completely integrated silicon microcircuits available for computer logic applications—Fairchild's EPITAXIAL MICROLOGIC.

Epitaxial Micrologic replaces its predecessor, non-epitaxial Micrologic, because it is faster, more rugged and less expensive. The graphs on the left show significant epitaxial performance superiority. It is more immune to extraneous computer noise, more stable throughout the temperature range—55°C to 125°C, and it exhibits much improved saturation characteristics. Although its development embodies the latest technologies, it is available in production quantities.

The difference between Epitaxial Micrologic and non-epitaxial Micrologic involves both process improvements and performance improvements. This brochure follows the manufacturing process of a typical element, illustrating both sources of improvements.

FAIRCHILD
SEMICONDUCTOR

PROCESS INTRODUCTION

The process used to manufacture Epitaxial Micrologic elements is an extension of the Planar* Processes developed by Fairchild to produce Silicon transistors. The elaborations on the original process are pointed out in the following description. The successful integration of many disciplines into an economical and productive process is a major factor contributing to the performance of Fairchild Epitaxial Micrologic.

*PLANAR: A PATENTED FAIRCHILD PROCESS.

CRYSTAL GROWING

The starting point is the growth of high purity silicon crystals by the Czochralski method: A small, perfect seed crystal, carefully selected for low dislocation and imperfection counts, is lowered into molten silicon, and slowly withdrawn under precise control, forming a large single crystal about six-inches long and one-inch in diameter. For Epitaxial Micrologic, the crystal is grown with a boron impurity to make it P-type, rather than the N-type starting material of non-epitaxial Micrologic.

WAFER FORMING

The crystal is sliced with a diamond saw into many wafers each approximately 12 thousandths (.012) of an inch thick. The cut wafer is then lapped flat, using a very fine grit abrasive, and chemically etched to form an extremely smooth shiny surface. The thickness of the finished wafer is about five thousandths (.005) of an inch. Non-epitaxial Micrologic devices require even thinner finished wafers due to the necessity of diffusion from both surfaces. Epitaxial techniques side step this requirement so that thicker, less fragile wafers are produced. The added thickness strengthens the individual wafers resulting in lower wafer loss during the manufacturing process.

OXIDE GROWTH

Many wafers of silicon—representing hundreds of potential Micrologic elements per wafer—are inserted into the grooves of a quartz boat and placed into a furnace containing an oxidizing atmosphere at 1200°C. Oxygen penetrates the crystal lattice at the surface of the wafer, combining chemically with surface silicon atoms to form SiO_2 (silicon dioxide) an inert, stable "glass" which encapsulates and passivates the wafer surface. This step is the key to the reliability and production economy attained through the Planar process.

FAIRCHILD
SEMICONDUCTOR

COLLECTOR CUTOUT

The passivated wafer begins to take the form of an integrated circuit with the collector cutout step. The wafer is coated with a photosensitive material in a darkroom, and then exposed to light through a high resolution mask. Those portions not exposed are soluble and easily removed with a solvent rinse. At this point, an etch is used to remove the silicon dioxide from those areas not protected by the film of photosensitive material. In this way, cutouts for collector diffusion are photo-engraved through the protective passivating silicon dioxide layer.

N+ COLLECTOR DIFFUSION

The wafers are placed into a special high-temperature furnace whose atmosphere contains gaseous phosphorus. The temperature is raised and the phosphorus impurity diffuses into the exposed silicon, forming a highly doped N+ region. This N+ diffusion is necessary to create a very low transistor collector resistance.

EPITAXIAL LAYER GROWTH

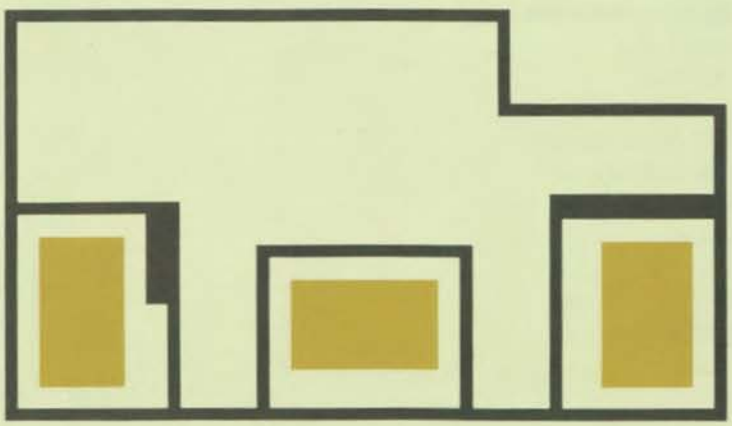
With N+ material diffused within the P substrate, the next step is the growth of the epitaxial layer. This is accomplished in the following manner: First, the passivating surface of silicon dioxide is removed by etching with hydrofloric acid. The wafers are then placed within a thermal reaction chamber where volatile gases are introduced and through chemical reactions, N-doped silicon is grown on the wafer surfaces. Under these conditions, the growing layer assumes the same crystal orientation as the substrate wafer and becomes an addition or extension of this material. The thickness and resistivity of this epitaxial layer affect the speed and saturation parameters of the finished device. After the epitaxial growth, an oxide is grown on the wafer as before, forming a new passivation for the rest of the manufacturing process.

The design developing on the facing page is a simulated mask for the progressing photo etching process.

FAIRCHILD
SEMICONDUCTOR

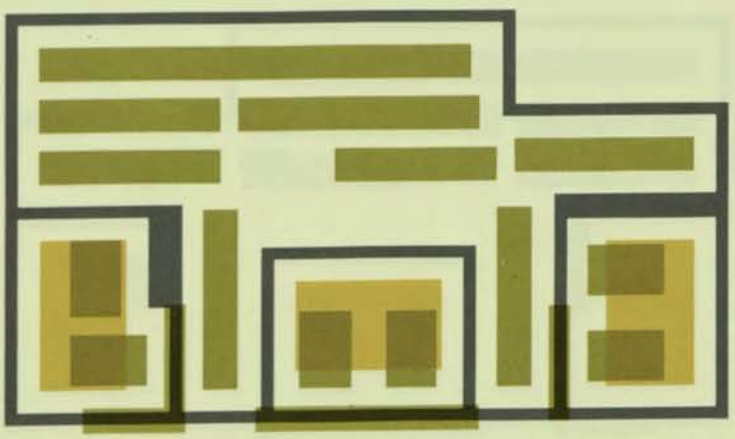
ISOLATION MASKING AND DIFFUSION

The process now returns to steps similar to the non-epitaxial Micrologic process. Isolation masking and diffusion are performed to electrically isolate transistors and resistors from one another. Bands are etched through the silicon dioxide surface to prepare for the isolation of individual circuit parts. The wafers are then placed into a furnace operating at controlled high temperature in an atmosphere of boron (P-type dopant) for isolation diffusion. The dopant diffuses through the exposed epitaxial N-type layer, forming a highly concentrated P-type region extending through to the P-type substrate. During the diffusion, the silicon dioxide layer regrows over the masked area. In this manner, isolated pockets of N-type material which will become the collector regions or resistor regions, are formed.



BASE MASKING AND DIFFUSION

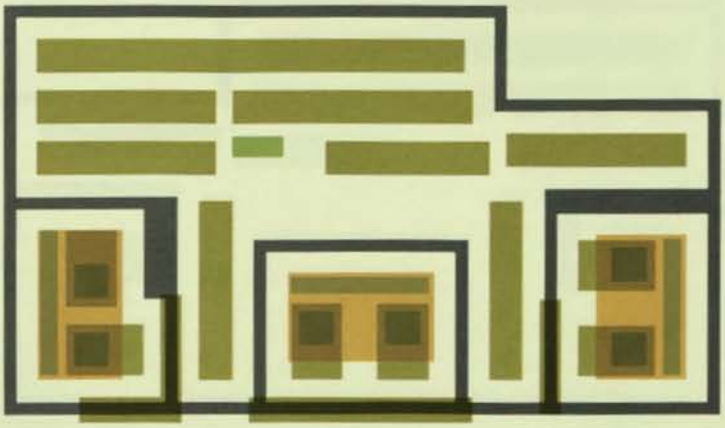
The wafer is again masked
and etched for the simultaneous diffusion
of the base region and resistors.
Once again boron is used
as the diffusing impurity in this
high-temperature diffusion.
The base region is diffused into the N-type
epitaxial layer to form the
collector-base diode of each transistor
as well as all the resistors in the circuit.
The oxygen atmosphere in the furnace
re-oxidizes the cutout
portions of the wafer surface and
seals them against contamination or injury.
As the diffusion progresses
downward into the wafer, it also
proceeds laterally, diffusing into the silicon
covered by the original protective oxide.



FAIRCHILD
SEMICONDUCTOR

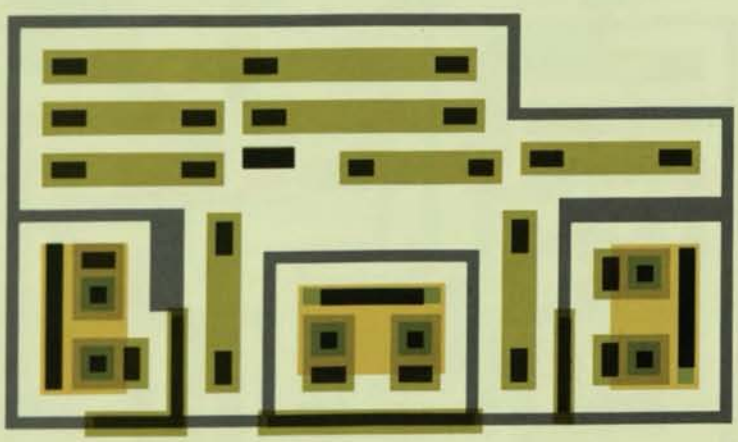
EMITTER MASKING AND DIFFUSION

Another precisely indexed masking step is performed to remove oxide for the emitter diffusion and for the top-side collector contacts. In a high-temperature step, phosphorus (an N-type impurity) — is diffused into the surface at 1200°C. This impurity forms the emitter region. Again silicon dioxide forms as the diffusion progresses, covering the photo-engraved area and sealing the surface. Side diffusion carries the junction underneath the protective layer. Notice that in each case the diffused region ends underneath an oxide which existed previously. This oxide permanently protects the actual junctions of the device against exposure to the outside environment.



EXPOSURE OF CONTACT AREAS AND METALIZATION

At this point the transitors and resistors of the Epitaxial Micrologic circuit are complete. They must now be intraconnected to form the desired logic circuit. This is done by evaporating metal onto the surface of the silicon wafer using the Metal-Over-Oxide process*. Before this can be done, however, a hole must be photo-engraved over the appropriate regions of the devices so that the evaporated metal can make contact. This is done in a masking step similar to the others. The wafers are now placed into a high vacuum chamber containing a metal evaporator. Aluminum is boiled from a hot tungsten filament forming an atmosphere of metal and other gases. The evaporated metal deposits in a thin, even coat over the entire wafer surface. Many wafers, comprising several thousand Epitaxial Micrologic units, are processed at one time in this fashion.

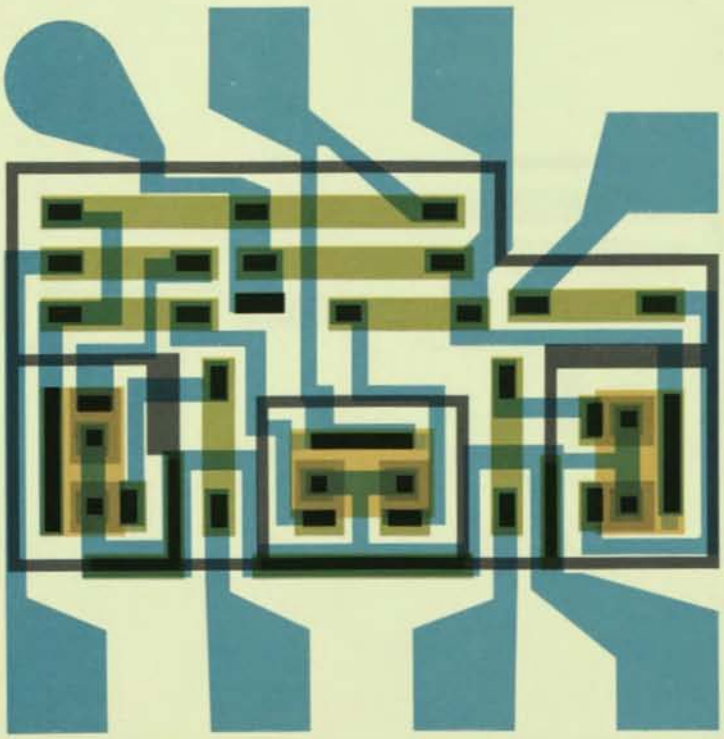


*METAL-OVER-OXIDE: PATENTED FAIRCHILD PROCESS.

FAIRCHILD
SEMICONDUCTOR

METAL INTRACONNECTIONS

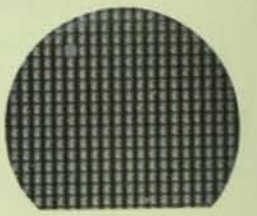
In another precise photo-engraving step, the aluminum layer is masked and selectively etched to leave a pattern of intraconnections between transistor and resistor elements in the logic circuit. The wafers are placed in an alloying oven so that the aluminum intraconnections can be firmly attached to the silicon dioxide surface. The Epitaxial Micrologic wafer is now complete as shown in the figure and needs only to be cut into individual elements and packaged. Up to this point, all operations have been done on many wafers at a time. The elimination of the handling of each device separately is a major factor in the reduction of production costs. This batch processing also increases the reliability and compatibility of devices. All connections to the outside—inputs, outputs, power supply and ground—are brought out to the periphery of the element as large aluminum pads, for easy, reliable connections.



MOUNTING, INSPECTION, CAPPING AND FINAL TESTING

The wafer is cut into small pieces using a technique very similar to the cutting of glass. A diamond scribe is used to make fine scratches on the surface of the wafer between the circuits. The wafer is mechanically separated along these lines into uniform, square dice. The dice are then cleaned thoroughly, dried and inspected for defects under high-power microscopes before expensive hand labor is incurred. The die is then soldered to the center of a header using a high temperature alloy preform and proceeds to a lead-bonding station. Using a capillary ball-bond, proven through four years of production experience at Fairchild, a fine gold wire is attached to each of the input, output and supply pads of the device. Each lead is held against a header post and securely spot-welded. Following lead-weld, a final optical inspection is conducted to guarantee that the die has not been damaged in any manner up to this time. After passing this inspection, the mounted device is thoroughly cleaned and a cap is welded to the header, completing the assembly. Epitaxial Micrologic can share the production line with Planar transistors at any time, since the processes are identical from dicing through final seal. This packaging operation uses techniques whose reliability has been verified extensively on Planar transistors and non-epitaxial Micrologic. After final seal, each Micrologic element is subjected to a number of tests to insure its reliability. They are subjected to mechanical shock tests, temperature cycling, and centrifuge acceleration tests as well as rigorous electrical testing. All Micrologic elements are 100% tested and sorted on Fairchild Series 4000 integrated circuit testers. These machines check all measurable DC parameters and also perform a thorough worst-case functional operation test. Finished units are supplied to Production Control for packaging in boxed stock for shipment to customers. Even after their final electrical tests, devices are continually sampled by Quality Control to confirm their conformance to rigid specifications. Each week a sample of devices is placed on a 125°C operating life test in a continuing evaluation program.

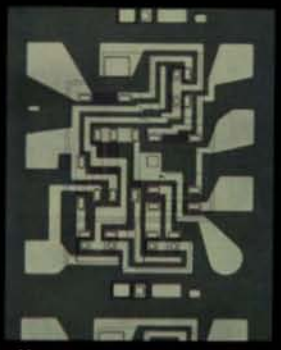
FAIRCHILD
SEMICONDUCTOR



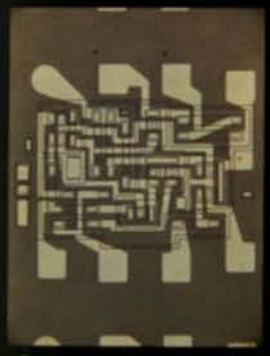
HISTORY

The first production integrated microcircuits were silicon Planar* devices, introduced by Fairchild in 1960. Because these units were manufactured for digital computer logic applications, they were called Micrologic and abbreviated "μL"*. By 1961 the Micrologic family had grown to six basic mutually compatible integrated circuit elements. These consisted of a buffer element ("B" element), a counter adapter element ("C"), a flip-flop element ("F"), a gate element ("G"), a half-adder element ("H"), and a half-shift register ("S"). Using a modified form of direct-coupled transistor NOR logic known as RTL (resistor transistor logic) NOR logic, this family of Micrologic permitted the synthesis of all computer logical functions. The evolution of Epitaxial Micrologic increases this basic family of elements with the addition of two more devices. These are a 4-input gate element ("G_1"), and a dual 2-input gate element ("D"). Photomicrographs of the Epitaxial Micrologic family are shown on the facing page. The higher circuits per wafer ratio of Epitaxial Micrologic on finished wafers is shown in the photographs above. Although Micrologic offered the solution to routine design problems, the demand for special integrated circuit devices stimulated the creation of the custom microcircuits group. Through this facility, Fairchild engineers are able to offer the capability of design and production of special microcircuits manufactured to customer specifications. The epitaxial techniques are also available for these custom microcircuits.

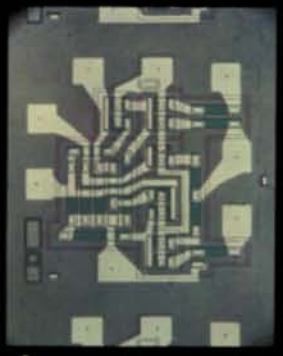
B



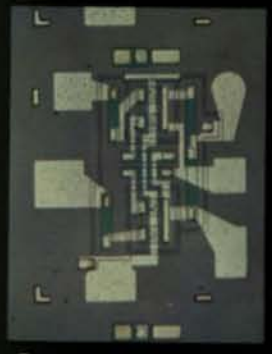
H



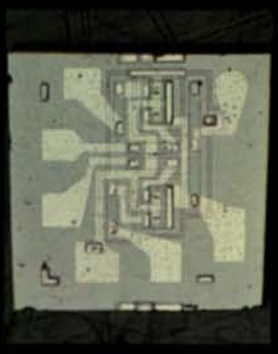
C



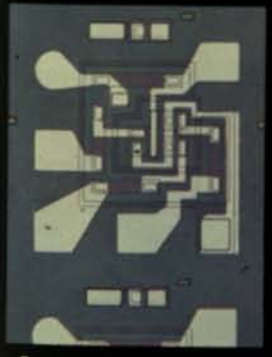
S



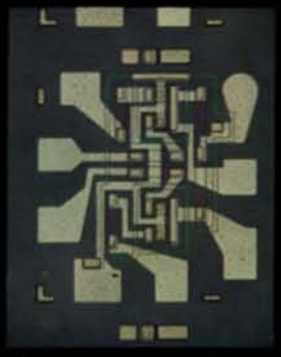
F



G_1



G



D

FAIRCHILD

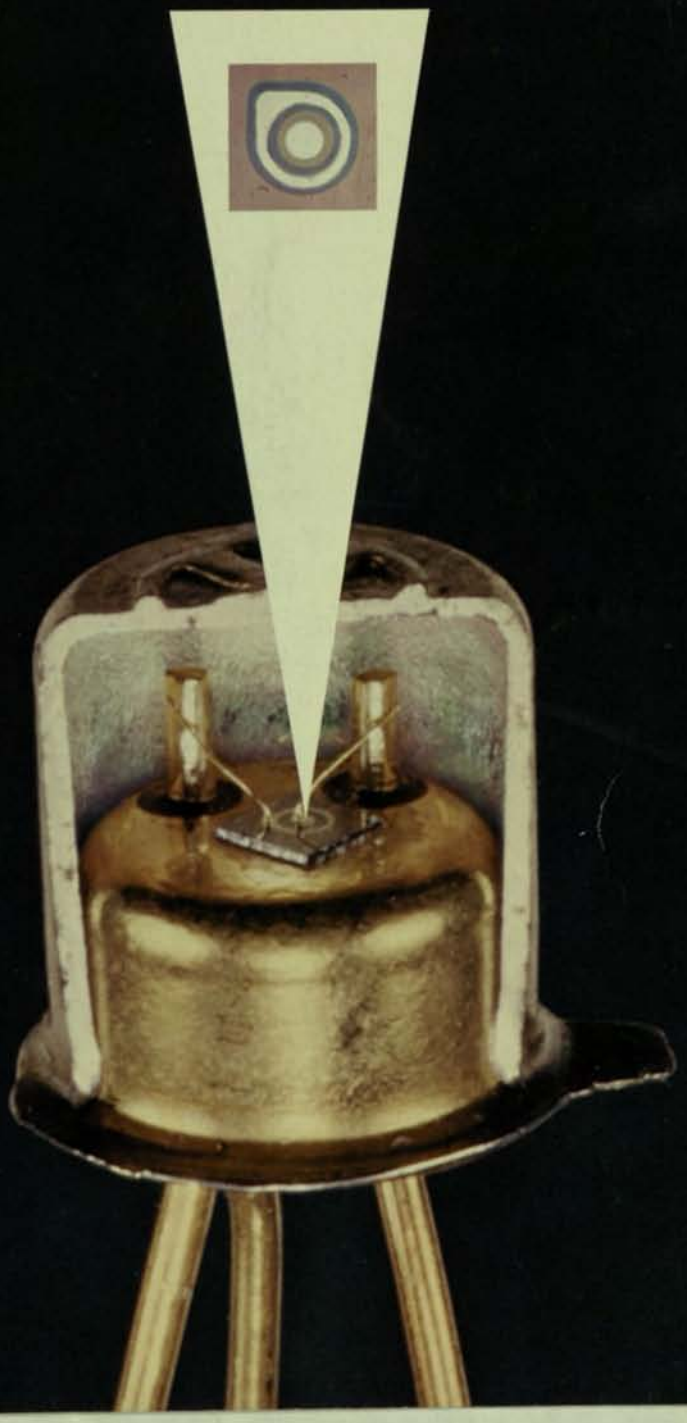
SEMICONDUCTOR

FAIRCHILD SEMICONDUCTOR / 545 WHISMAN ROAD, MOUNTAIN VIEW, CALIFORNIA / 962-5011 / TWX: 415-969-9165

μL AND μLogic TRADEMARKS OF FAIRCHILD SEMICONDUCTOR A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION. A-64/B-63/PRINTED IN U.S.A. ©1963

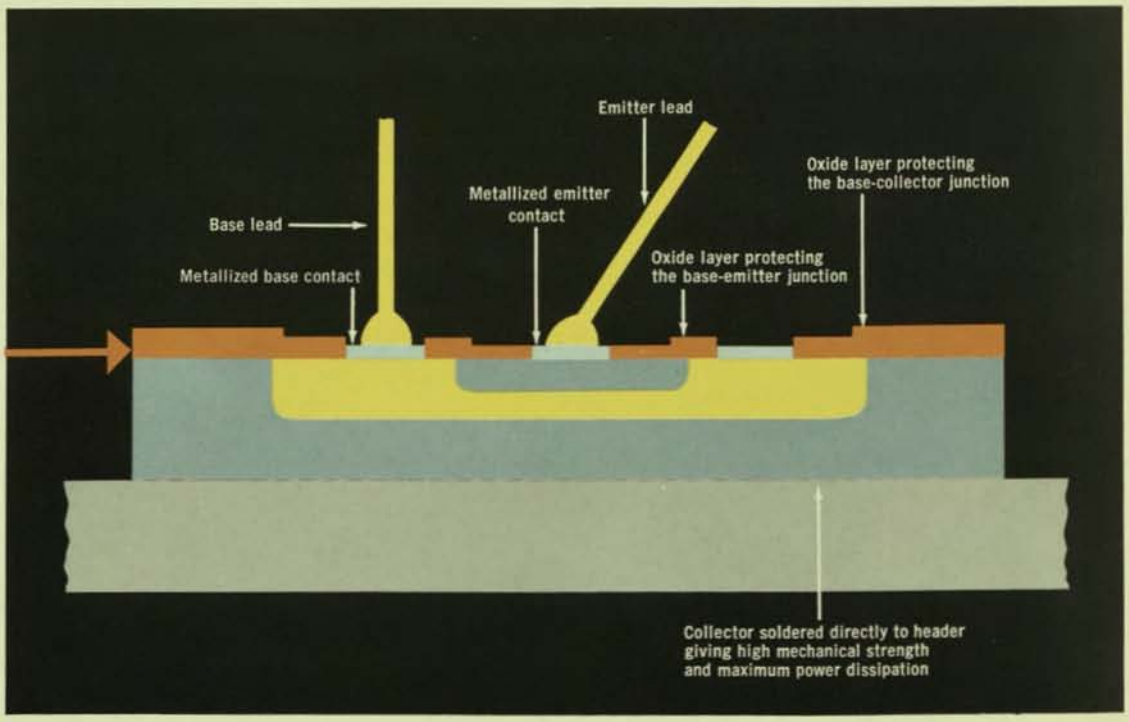
THE MOST SIGNIFICANT SEMICONDUCTOR DEVELOPMENT SINCE THE DIFFUSED SILICON MESA

THE FAIRCHILD PLANAR STORY



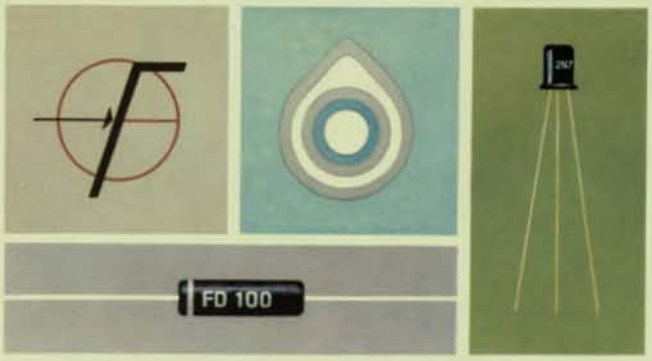
FAIRCHILD SILICON PLANAR TRANSISTORS AND DIODES

Offering stability to a degree never before attainable



THE PASSIVATED SURFACE
an integral silicon oxide coating completely protecting the junctions against contamination during manufacture and against change with time.

COPYRIGHT 1960 BY FAIRCHILD SEMICONDUCTOR CORPORATION



achieved by 100% oxide protection of junctions

By a unique process revealed in this brochure, Fairchild has passed a milestone in semiconductor technology. The transistors and diodes now in large-scale production by this method offer unprecedented stability—performance unchanged by time, use, environment, or even exposure to foreign matter. This protection and the resulting stability actually reduce the cost of manufacture. And the versatility of the process permits the specifying of planar replacements for almost every transistor and diode in present use.

THE 4 REASONS WHY PLANAR TRANSISTORS AND DIODES ARE DESTINED TO SUPPLANT THE MAJORITY OF OTHER TYPES

RELIABILITY
Reliability statistics already accumulated on Fairchild's planar types excell those obtainable with any prior types. The reasons derive logically from Fairchild's processing steps and the 100% surface protection of the finished devices.

PERFORMANCE
Broadened operating range and extremely low leakage are combined with the speed and power capabilities of the conventional type mesa transistors and diodes. As well as permitting exciting new applications, planar types are available as replacements for existing transistors and diodes *with no circuit changes required.*

COST
On a performance-per-dollar basis, planar types are more than competitive even at the present state of manufacturing technology. Very high yields are made possible by "planar self-protective manufacture" and will lead to much lower prices in the future – competitive even with germanium and low-performance silicon.

ADAPTABILITY
Fairchild's planar manufacturing technique – because of its high yields – and because of the inherent versatility of the structure – lends itself ideally to such advances as multiple transistors, multiple diodes and integrated circuitry. It is also the best way to make universal transistors and diodes that serve broad needs with few types.

The PLANAR PROCESS

and how it builds in an unprecedented degree of reliability

The way it is made tells why a planar transistor or diode will be far more stable and reliable than any other type. Use and statistical studies confirm this.

PROTECTION FROM START TO FINISH

One planar transistor on a silicon wafer is followed through the various steps in which the junctions, surface and contacts are formed. Photographs are magnified 128 times.

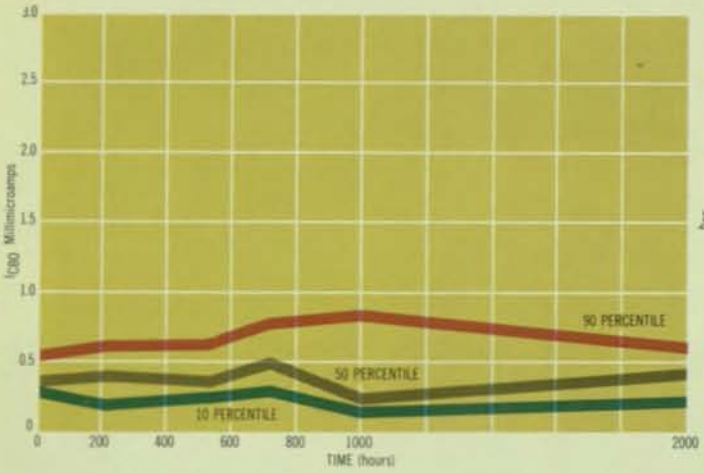
All photographs unretouched — colors are interference colors.

The entire silicon wafer surface receives protective oxidation before any of the diffusion steps that will form the base and emitter junctions.

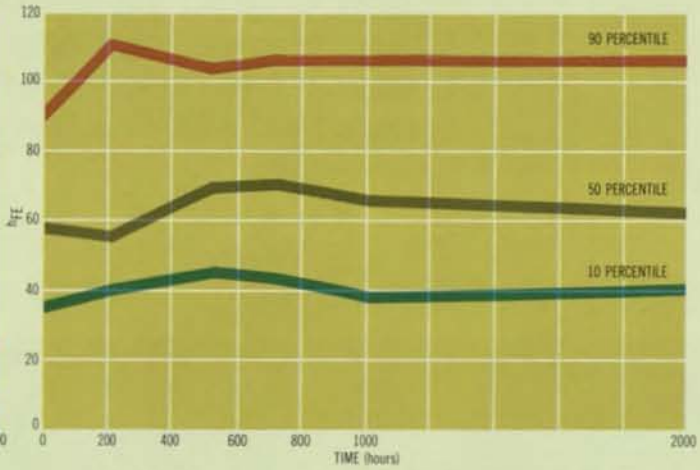
A window is etched through the oxide to prepare for base diffusion. Surrounding oxide has been masked against etching by a photo lithographic technique.

Base impurity enters through the exposed area. The base collector junction is formed by diffusion under the original oxide at a protected location. New oxide forms over exposed base area.

STABILITY – THE MOST IMPORTANT KIND OF RELIABILITY Planar transistors and diodes because of their protected junctions give the circuit designer the most important assurance he can ask – that performance parameters will stay put – so that this circuit will continue to function as intended – for an indefinite length of time, and through all the environmental extremes considered in its design.



SUSTAINED LOW LEAKAGE – The life test shown above was conducted at 200° C storage to increase any effects of time. Note that the leakage values are in fractions of millimicroamperes, hence the apparent small changes are fractions of extremely small values.



NO LOSS IN BETA (h_{FE}) – A random thousand 2N1613 (Planar 2N697) units subjected to 2000-hour life test at 200°C. Graph shows that beta distribution actually has a slight upward shift with time, stabilizing after 1000 hours and affording a large design safety factor.

A smaller window is etched through the second oxide coating to prepare for emitter diffusion. Precision masking at various stages maintains exact relative positioning of areas.

Emitter impurity diffuses through the exposed area. Again, due to the concurrent lateral diffusion, the emitter-base junction is placed under the second oxide at a protected location.

Base and emitter contact areas are etched through the oxide coatings. Precision masking keeps etching well away from junctions. Protective oxide over junctions remains undisturbed.

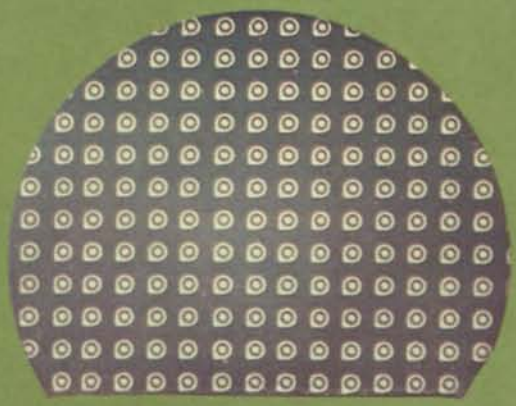
Metallizing of base and emitter contacts completes the processing of the wafer prior to separation into individual dice. At no step have the junctions been exposed to contamination.

PLANAR YIELD

the key both to lower cost and to new, advanced

Fairchild's planar process characteristically yields in excess of 90% finished units meeting very high specifications. (50% yield has been good by other methods.) The economic advantage is huge—first to provide high-performance, high-reliability units at reasonable cost—ultimately to supplant even the low-performance types as these lose their price advantage. Increased volume can only snowball the effect.

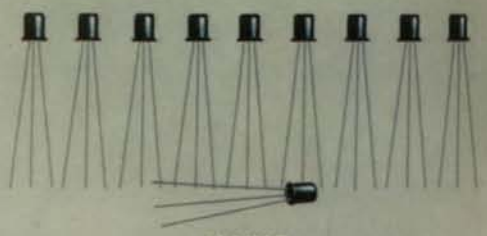
THE EXTRAS IN THIS WAFER ARE THE SECRETS TO LOW-COST TRANSISTORS



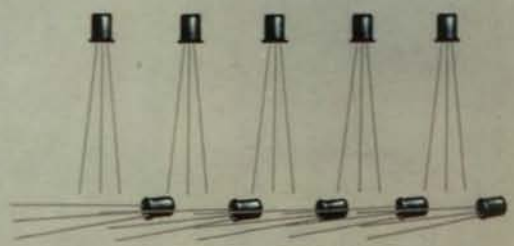
It took extra steps and extra precision to manufacture this planar wafer — an apparent extra cost. But because of the passive oxide that protects the sensitive regions of the transistors on this wafer, more of these structures will survive to meet rigid specifications.

A COMPARISON OF REJECT BURDENS

The transistors or diodes that pass specifications obviously must carry the cost burden of those that fail. A comparison of planar yield with "good" yields by other processes is shown.



PLANAR
(9 to 1)

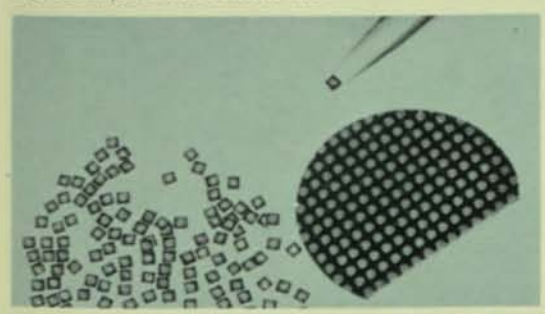


TYPICAL OTHER
(5 to 5)

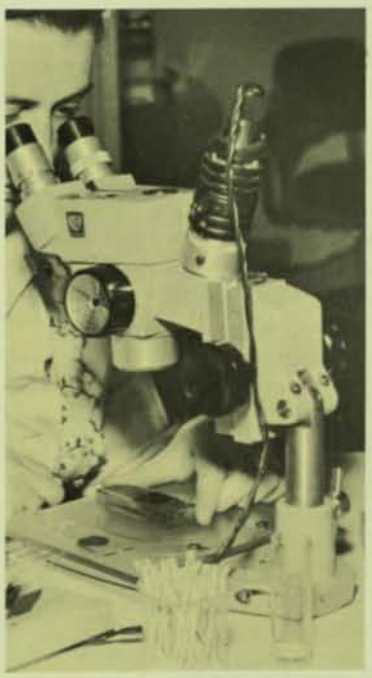
devices

A REVEALING DIVISION OF COST IN FAIRCHILD'S PLANAR MANUFACTURE

In the wafers thousands of potential transistors or diodes are handled together. They receive the extra steps necessary for surface passivation. Simultaneous processing makes these valuable extra steps a small part of total transistor cost.



Once the dice are cut apart, the manufacturing steps become more costly because of individual handling. Protection against some of the normal production hazards is built in, making subsequent steps easier.



Assembly steps are the costly ones. But the costs are similar whether the transistors are low performance types or high. Three things count. The first two are the scale of production and degree of automation. The other is yield — the final acceptance rate.

HIGH YIELDS NOW MAKE MULTIPLES FEASIBLE

Advantages

- Closely matched twins, triplets or quads can be tied together in one package.
- Functional multiples with a common electrical connection can be packaged together reducing external soldered connections.
- Higher packaging density is made possible.

The Arithmetic of Practicality

Using a four-transistor quad as an example, simple arithmetic shows the vital part played by planar high-yield manufacture in making such devices feasible.

By planar (90% yield of single transistors)
.90 x .90 x .90 x .90 = 65% yield of quad assemblies

By other processes (50% yield of single transistors)
.50 x .50 x .50 x .50 = 6% yield of quad assemblies

The photo shows a Fairchild two-transistor chopper in one TO-5 package, the first of a family of Fairchild multiple transistors and multiple diodes to come. The same planar advantages are essential to future development of integrated circuits.

"HARDWARE" *to the tightest specifications and*

Fairchild silicon planar transistors and diodes embodying all the claimed advantages of performance and reliability are available now. The selection is broad and will increase further.

SILICON PLANAR TRANSISTORS

The most significant combination of performance parameters ever offered is available now in Fairchild planar transistors. They can fulfill the most demanding requirements — also simpler needs, of course.

PERFORMANCE PROFILE OF PLANAR TYPES

(These figures do not represent ultimates; they are performance available or imminent as of November 1960. Full data is available on all types.)

2N 708

SPEED — 400 megacycles gain-bandwidth product... in a planar transistor that also has power dissipation of *1 watt* at 25°C case temperature

2N 699B

POWER — 5 watts dissipation in TO-5 package... in a planar transistor that also has gain-bandwidth of 120 mc. *(Planar power transistors also planned)*

2N 1613

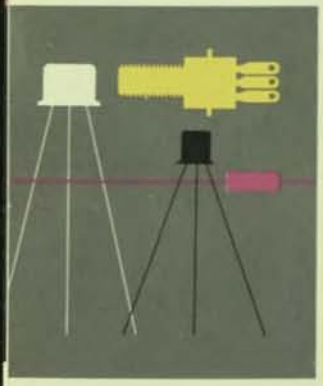
LOW LEAKAGE — 0.0008 μA typical at 25°C... and 10 μA maximum at 150°C in a general purpose planar at $V_{CB} = 60V$

2N 1613 2N 708

TIGHT SPREAD OF "ON" BASE VOLTAGE ... This permits close matching of transistors for differential usage and simplifies dc logic chain designs

2N 1613

BROAD CURRENT RANGE — I_C from 100 μA to 500 mA... 5000-to-1 range all in one planar transistor with guaranteed h_{FE} greater than 15 at both extremes



A planar/mesa performance comparison (2N 1613 versus 2N 697)

The following apply to a planar "immediate superior" and the specific mesa type it replaces.

Maximum dissipation	Planar 50% higher	Gain-bandwidth	same
Maximum V_{CBO}	Planar 25% higher	Switching speeds	same
Maximum V_{EBO}	Planar 40% higher	V_{CER}	25% higher
Low current h_{FE}*	Planar very superior	$V_{BE\ SAT}$	same
I_{CBO}	Planar 100 times lower	$V_{CE\ SAT}$	same
C_{ob}	Planar 30% lower	h_{FE} (@ 150 mA)*	same
I_{EBO}	Planar 10,000 times lower		

In addition, the noise figure is considerably improved.

*h_{FE} is useful and specified over a broader current range on the planar types.

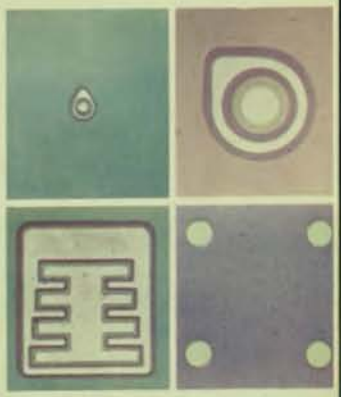
for the broadest requirements

PLANAR TYPES REPLACE MANY TRANSISTORS DIRECTLY

One or two planar transistor types replace many mesa, grown diffused, grown and alloy transistor types. Use planar transistor types which provide higher power dissipation and higher f_T and/or f_{max}[1] as replacement types[2] for the following transistors:

2N 117	2N 335	2N 472	2N 560	2N 756	2N 1077	2N 1212	2N 1386	2N 1586
2N 118	2N 335A	2N 473	2N 696	2N 757	2N 1149	2N 1247	2N 1387	2N 1587
2N 118A	2N 335B	2N 474	2N 697	2N 758	2N 1150	2N 1248	2N 1388	2N 1588
2N 119	2N 336	2N 474A	2N 698	2N 759	2N 1152	2N 1249	2N 1389	2N 1589
2N 120	2N 336A	2N 475	2N 699	2N 760	2N 1153	2N 1267	2N 1390	2N 1590
2N 160	2N 337	2N 476	2N 699A	2N 761	2N 1154	2N 1268	2N 1417	2N 1591
2N 160A	2N 338	2N 477	2N 702	2N 762	2N 1156	2N 1269	2N 1418	2N 1592
2N 161A	2N 347	2N 478	2N 730	2N 770	2N 1157	2N 1270	2N 1479	2N 1593
2N 162A	2N 348	2N 479	2N 731	2N 772	2N 1196	2N 1271	2N 1482	2N 1594
2N 332	2N 349	2N 479A	2N 745	2N 1060	2N 1199	2N 1276	2N 1528	2N 1631A
2N 333	2N 470	2N 541	2N 746	2N 1074	2N 1205	2N 1277	2N 1564	2N 1644A
2N 333A	2N 471	2N 542	2N 754	2N 1075	2N 1206	2N 1278	2N 1565	2N 2503
2N 334	2N 471A	2N 543	2N 755	2N 1076	2N 1207	2N 1279	2N 1566	

[1]Compiled from "Derivation and Tabulation Associates Ind." [2]Specific applications determine the degree of electrical and/or mechanical interchangeability.



PLANAR CONFIGURATIONS
Top left – High-speed switching transistor (2N708)
Top right – General purpose transistor (2N1613)
Bottom left – Power transistor
Bottom right – Diode (FD 200)

SILICON PLANAR DIODES

The more advanced silicon planar diodes offer desirable combinations of performance parameters difficult or impossible to attain by other manufacturing techniques. On standard specification, the passivated surface offers a bonus in extra reliability.

THREE TYPES WITH ADVANCED PERFORMANCE

This represents state-of-the-art performance available as of November 1960.

Ultra-fast – the FD100

For use in advanced computer logic application

2 mμsec. max. rev. recovery time	@ If = 10mA, Vr = 6V
10mA minimum forward conductance	@ 1 volt
2.0 μμf maximum capacitance	@ VR = 0V, f = 1mc
75V minimum breakdown voltage	

Ultra-fast, high conductance – the FD200

"Universal" type for switching and general purpose applications

100mA min. forward conductance	@ 1 volt
50mμsec. max. rev. recovery time	@ If = 30mA, Ir = 30mA
200V minimum breakdown voltage	
5 μμf maximum capacitance	@ VR = 0V, f = 1mc

General purpose, high conductance, low leakage – the FD300

"Universal" type for all applications where speed is not critical

Over 200mA forward conductance	@ 1 volt
0.005 μA maximum leakage	@ —125V, 25°C
Under 6 μμf capacitance	@ VR = 0V

OVER 200 STANDARD SPECIFICATIONS FULFILLED BY PLANAR DIODES

These include the most widely used high performance silicon diodes – and others that prior to Fairchild's planar introduction were difficult to obtain because of production problems encountered in other processes.

Some of the most popular types available with planar reliability are listed below. Switching diodes in the planar line are available with recovery time as low as 2 millimicroseconds.

1N 251 (JAN)	1N 662 (Sig C)	1N 843
1N 457 (JAN)	1N 663 (Sig C)	1N 903
1N 458 (JAN)	1N 837A	1N 904
1N 559 (JAN)	1N 840	1N 905
1N 643 (Sig C)	1N 841	1N 914 (USN)
1N 658	1N 842	1N 916

THREE QUESTIONS ANSWERED

1. AREAS OF APPLICATION

- For direct use in any circuits designed around silicon mesa types.
- In lieu of high-performance germanium types in circuits now being designed for future manufacture (since lower prices are anticipated for planar silicon devices).
- To solve problems of heat, packaging density, circuit simplification, reverse leakage, long term stability or reduction of the number of device types required.
- In circuits requiring much less than planar performance – but which can benefit from reliability and design simplification. A projection of future planar prices versus your own production timetable can save your product from early obsolescence.

2. AVAILABILITY OF TECHNICAL DATA

Detailed specification sheets are available on each planar type now in production and will be issued on new types as they are released.

Circuit application data is available showing effective circuits to take full advantage of the performance characteristics of planar devices for a wide range of needs.

Technical papers are available on various fundamental investigations by Fairchild research and application personnel.

Fairchild's sales engineers or the application engineering department in the Mountain View home office can supply any of the above.

3. CONVENIENT SOURCES OF FAIRCHILD PLANAR TRANSISTORS AND DIODES

Local distributor stocks in the major electronic manufacturing areas enable quick delivery. Up to 999 units of any type can be furnished at factory prices. See back cover for your nearest distributor.

Large production orders for quantities over 999 are processed by Fairchild's field offices in a number of areas of the country.

Government source inspected sales on Fairchild types with MIL approval can be placed through Fairchild field offices.

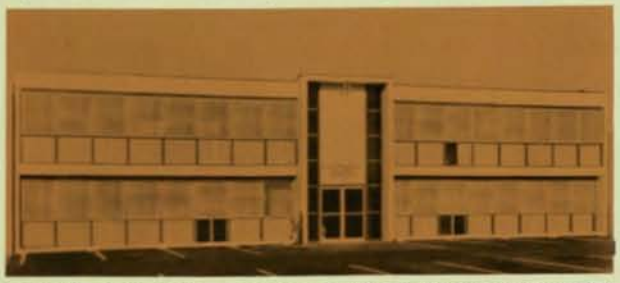
FAIRCHILD GROWTH

The reflection of product acceptance

Fairchild's main office and transistor manufacturing plant, occupying 68,000 square feet in Mountain View, California. This expanded facility was necessitated by production requirements less than one year after Fairchild's first product announcement. Further expansion of this facility is planned for early 1961.

The research and development center in Palo Alto occupying Fairchild Semiconductor's entire original plant facility of 17,000 square feet plus a 10,000 square foot addition. A completely new 60,000 square foot research and development building will be started in early 1961.

Quarters for Fairchild's Minuteman reliability program, occupying 7,800 square feet in a second Mountain View location.



Fairchild's Instrumentation Department moved from the main plant to 7,700 square foot quarters in Palo Alto, California.

Fairchild's 52,000 square foot diode plant in San Rafael, California, was occupied in November 1960.

FAIRCHILD DISTRIBUTORS

1 to 999 units at factory prices

ALMAC ELECTRONICS CORPORATION
6301 Maynard Ave., Seattle 4, Washington
PArkway 3-7310

ATLAS ELECTRONICS INC.
774 Pfeiffer Blvd., Perth Amboy, New Jersey
HIllcrest 2-8000

CRAMER ELECTRONICS INC.
811 Boylston St., Boston 16, Massachusetts
COpley 7-4700
WUX: FAX Boston, Massachusetts

DENNY-HAMILTON ELECTRONICS
1862½ Bacon St., San Diego 7, California
ACademy 4-3451

HAMILTON ELECTRO SALES
11965 Santa Monica Boulevard
Los Angeles 25, California
EXbrook 3-0441, BRadshaw 2-9154
TWX: W LA 6637

KIERULFF ELECTRONICS INC.
820 West Olympic Boulevard
Los Angeles 15, California
RIchmond 8-2444, TWX: LA 46

PHILA ELECTRONICS INC.
1225 Vine St., Philadelphia 7, Pennsylvania
LOcust 8-7444

SCHAD ELECTRONIC SUPPLY, INC.
499 South Market St., San Jose 13, California
CYpress 7-5858

SCHWEBER ELECTRONICS
60 Herricks Road
Mineola, Long Island, New York
PIoneer 6-6520, TWX: G CY NY 580-U

SCHWEBER ELECTRONICS
Silver Spring Division
8710 Georgia Ave., Silver Spring, Maryland
JUniper 5-7023

SEMICONDUCTOR DISTRIBUTOR SPECIALISTS, INC.
5706 West North Ave., Chicago 39, Illinois
NAtional 2-8860

VALLEY ELECTRONICS INC.
1735 East Joppa Road, Baltimore, Maryland
VAlley 5-7820, TWX: TOWS 564

VALLEY INDUSTRIAL ELECTRONICS, INCORPORATED
1417 Oriskany Street W., Utica, New York
RAndolph 4-5168, WUX: FAX Utica, New York

WARD TERRY AND COMPANY
Electronics Parts Division
P. O. Box 869, Denver 1, Colorado
AMherst 6-3181

FAIRCHILD FIELD SALES OFFICES

For production orders of 1000 units or more

PALO ALTO, CALIFORNIA
378 Cambridge Avenue, Suite M
DAvenport 1-8780

LOS ANGELES, CALIFORNIA
8833 Sunset Boulevard
OLeander 5-6058, TWX: BV 7085

GARDEN CITY, L. I., NEW YORK
600 Old Country Road
PIoneer 1-4770, TWX: G CY NY 5391

OAK PARK, ILLINOIS
6957 West North Avenue
VIllage 8-5985, TWX: OAK PARK 2820

WASHINGTON 6, D. C.
809 Cafritz Bldg., NAtional 8-2590

MARBLEHEAD, MASSACHUSETTS
119 Rockaway Ave., NEptune 1-4436

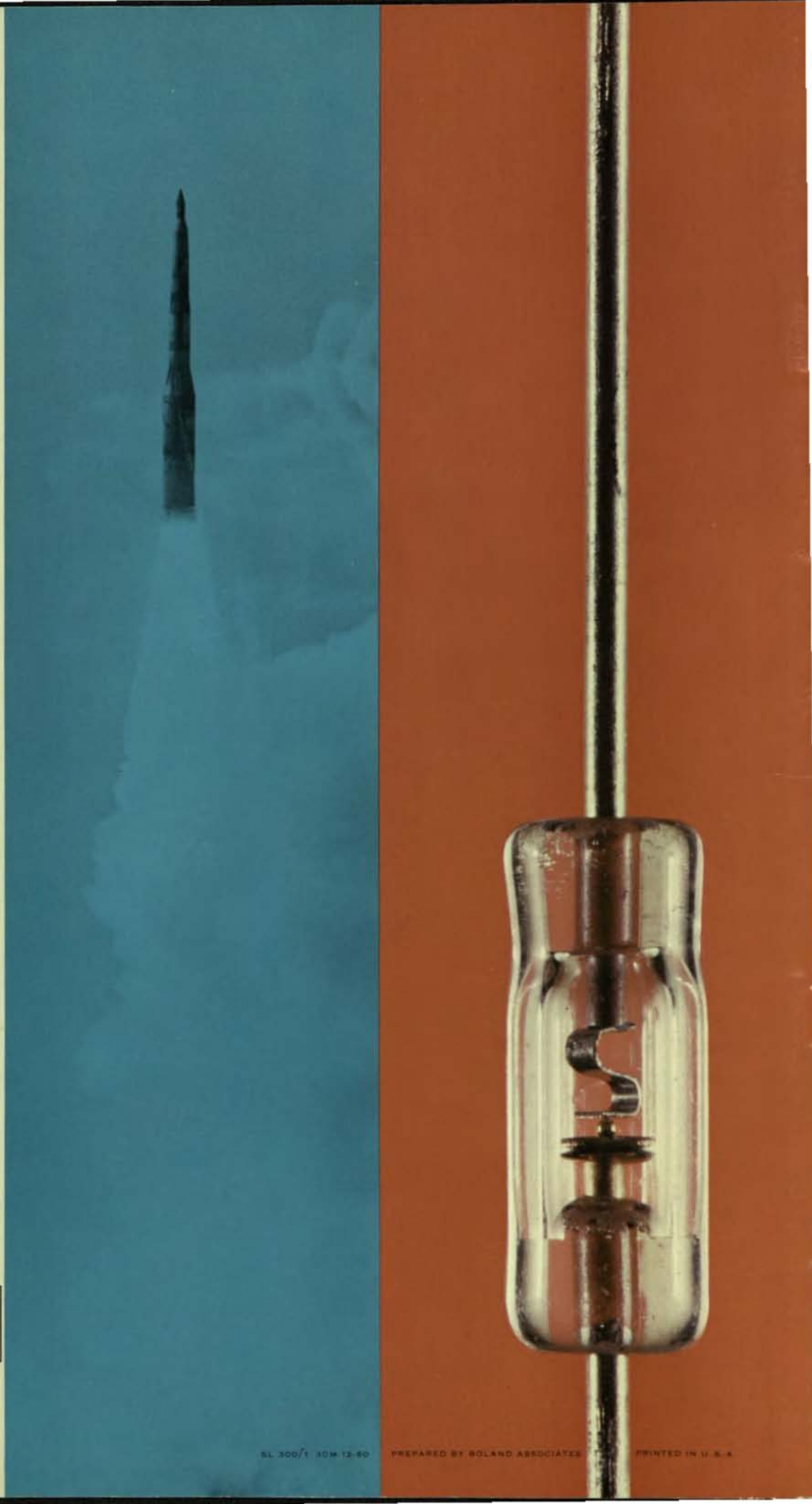
JENKINTOWN, PENNSYLVANIA
100 Old York Road
TUrner 6-6623, TWX: Jenkintown PA 1056

SYRACUSE, NEW YORK
731 James Street, Room 304
GRanite 2-3391, TWX: SS 94

ORLANDO, FLORIDA
618 E. South St., Suite 21, CRestwood 7-5610

FAIRCHILD
SEMICONDUCTOR CORPORATION

Transistors: 545 Whisman Road, Mountain View, Calif. YOrkshire 8-8161. TWX: MN VW CAL 853
Diodes: 4300 Redwood Highway, San Rafael, Calif. GReenfield 9-8000. TWX: SRF 26
A Wholly Owned Subsidiary of
Fairchild Camera and Instrument Corporation



SL 300/1 10M 12-60 PREPARED BY ROLAND ASSOCIATES PRINTED IN U. S. A.

suggestion award

Presented to

Hazel White

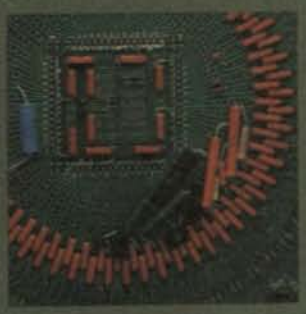
In recognition of a valuable
contribution to the company

October 22, 1973
Date

Thomas A. Longo
General Manager

FAIRCHILD
SEMICONDUCTOR

FACTS ABOUT FAIRCHILD



FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

Fairchild Camera and Instrument Corporation develops, manufactures and sells semiconductor devices and automatic test equipment. The company is a subsidiary of Schlumberger Limited, an oilfield services and electronics company headquartered in New York and Paris.

Fairchild's solid-state components – including integrated circuits, microprocessors, discrete devices and hybrid products – employ virtually every major semiconductor technology. They are used in aerospace, communications, automotive, computer, consumer and industrial products.

The company produces a broad range of test equipment for evaluating all types of semiconductor devices and circuit board subassemblies. Semiconductor companies and equipment manufacturers use these highly automated systems for engineering development, production and final testing, and incoming inspection. The Automatic Test Equipment Group operates a worldwide service and training network for its customers.

Headquartered in Mountain View, California, Fairchild has manufacturing facilities in ten other countries and sales and distribution outlets around the world. The firm employs more than 20,000 people.

The Company was founded in 1920 by the late Sherman Mills Fairchild, an American industrialist, inventor and scientist who was Board Chairman when he died in 1971 at the age of 74. He founded a number of companies and for many years was a director of IBM.

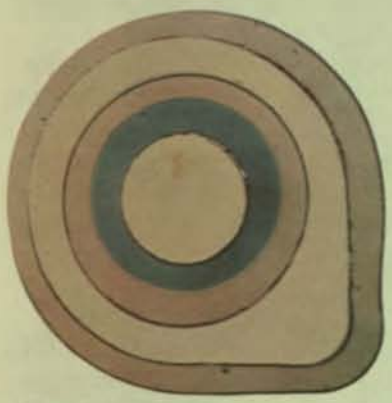
In its early years the company was known as Fairchild Aerial Camera Company. Its products were based on Mr. Fairchild's inventions, which include a between-the-lens camera shutter, the closed-cabin airplane, the folding-wing airplane and hydraulically operated aircraft brakes and landing gear. In 1936, aviation product areas were split off to form a new company, now known as Fairchild Industries. The aerial camera and electronics businesses were renamed Fairchild Camera and Instrument Corporation in 1944.

In the late 1950s, Fairchild sponsored a small group of young scientists in California in the development of a new process for manufacturing transistors. These scientists touched off a revolution in the newly born transistor industry with the planar process, which allowed mass production of devices that met users' most stringent requirements. Today planar technology is the fundamental method for producing transistors and integrated circuits, and is still regarded as the most significant achievement in semiconductor technology since the invention of the transistor.

During the 1960s, Fairchild built multimillion dollar plants in the United States and the Far East to serve the burgeoning semiconductor industry. The company has continued to develop new designs and process technologies which have allowed the density of circuit integration to double every year or two. Today's silicon "chips" now contain as many as 150,000 components on a piece of silicon no larger than the first, single-element transistors.

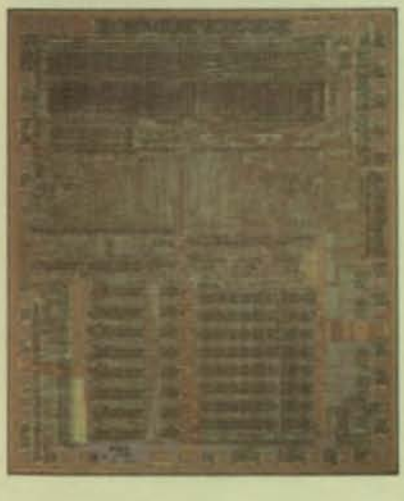
Another source of Fairchild's growth stemmed from test equipment that the company developed for use on its own semiconductor manufacturing lines. In 1961 the company began selling this equipment to other firms in the industry, and is now a leading producer of test systems for digital, analog and mixed signal semiconductor devices and circuit board assemblies.

In 1979, Fairchild became a subsidiary of Schlumberger, a world leader in oilwell logging services, electronics and measurement products. Schlumberger provides the petroleum industry with information essential to discovering and producing oil and gas economically. The company provides drilling and production services, energy measurement and control equipment, instruments and components.



In 1959, Fairchild produced the first planar transistor, a semiconductor device that marked the beginning of an age of high technology in electronics.

Introduced in 1981, Fairchild's F9445 is the fastest single-chip microprocessor available. Utilizing Isoplanar Integrated Injection Logic ($I^2L^®$), the 20 MHz version of the F9445 can perform a 16 x 16-bit multiplication in 3.5 microseconds.



Fundamental research has been key to Fairchild's accomplishments in the past and is recognized as an essential activity for future success. The company's broadest goal–to be the technological leader in the electronic components and automatic test equipment industries–demands a serious commitment to research.

Fairchild's Advanced Research and Development Laboratory in Palo Alto, California, is dedicated to the development of advanced solid-state physics and other technologies related to the semiconductor and testing industries. Its professional staff is made up of more than 200 physicists, engineers, chemists, mathematicians and computer scientists most of whom hold advanced degrees from universities throughout the world.

This laboratory provides the appropriate environment for technical innovation. Because major breakthroughs in these complex technologies usually evolve over a number of years, scientists are encouraged to work for long-range results. They are backed by the company's willingness to take calculated risks in order to achieve the greatest returns.

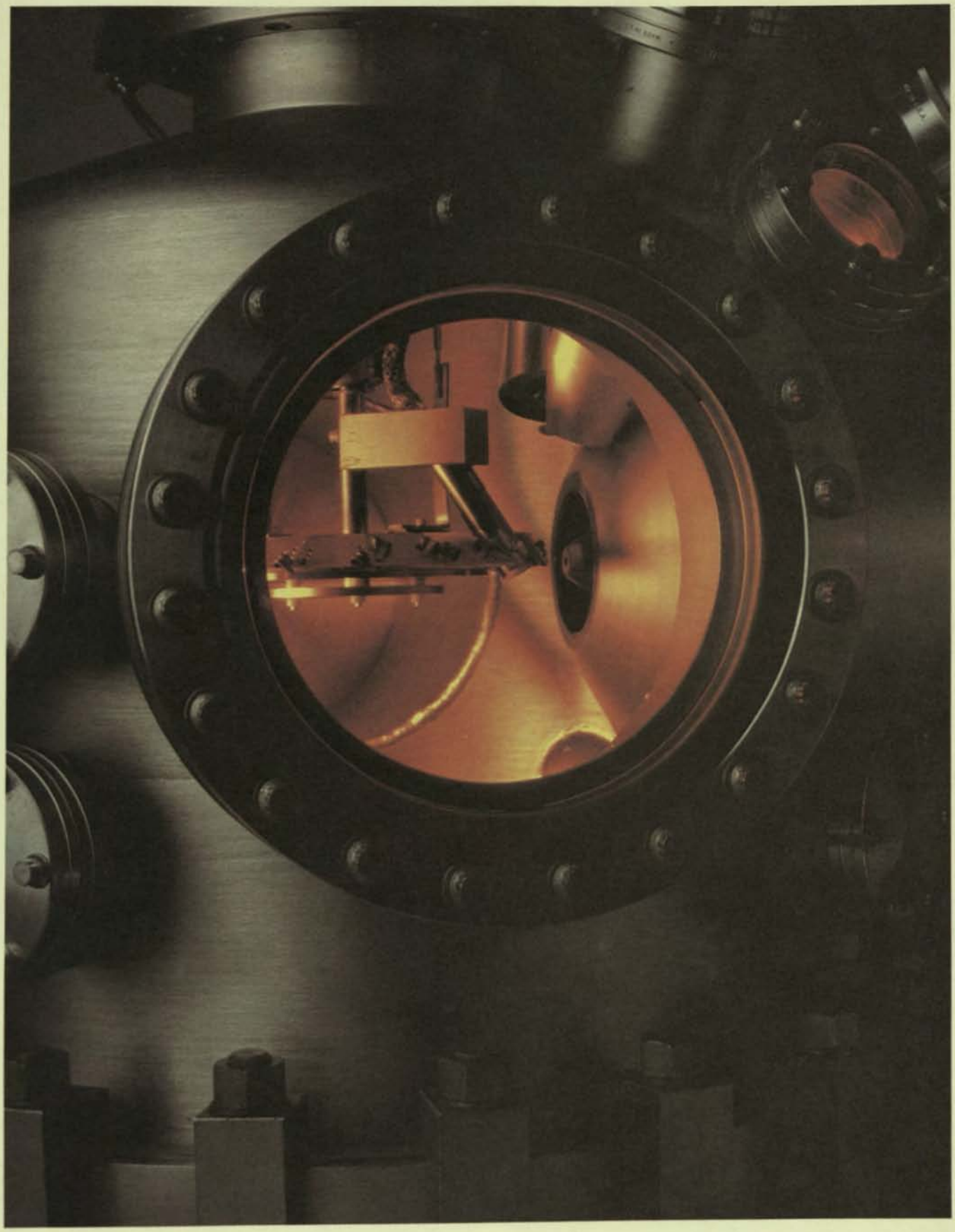
Many of Fairchild's most successful products were developed in Palo Alto: Isoplanar™ technology, 100K subnanosecond ECL (emitter-coupled logic) and CCD (charge-coupled device) imaging technology.

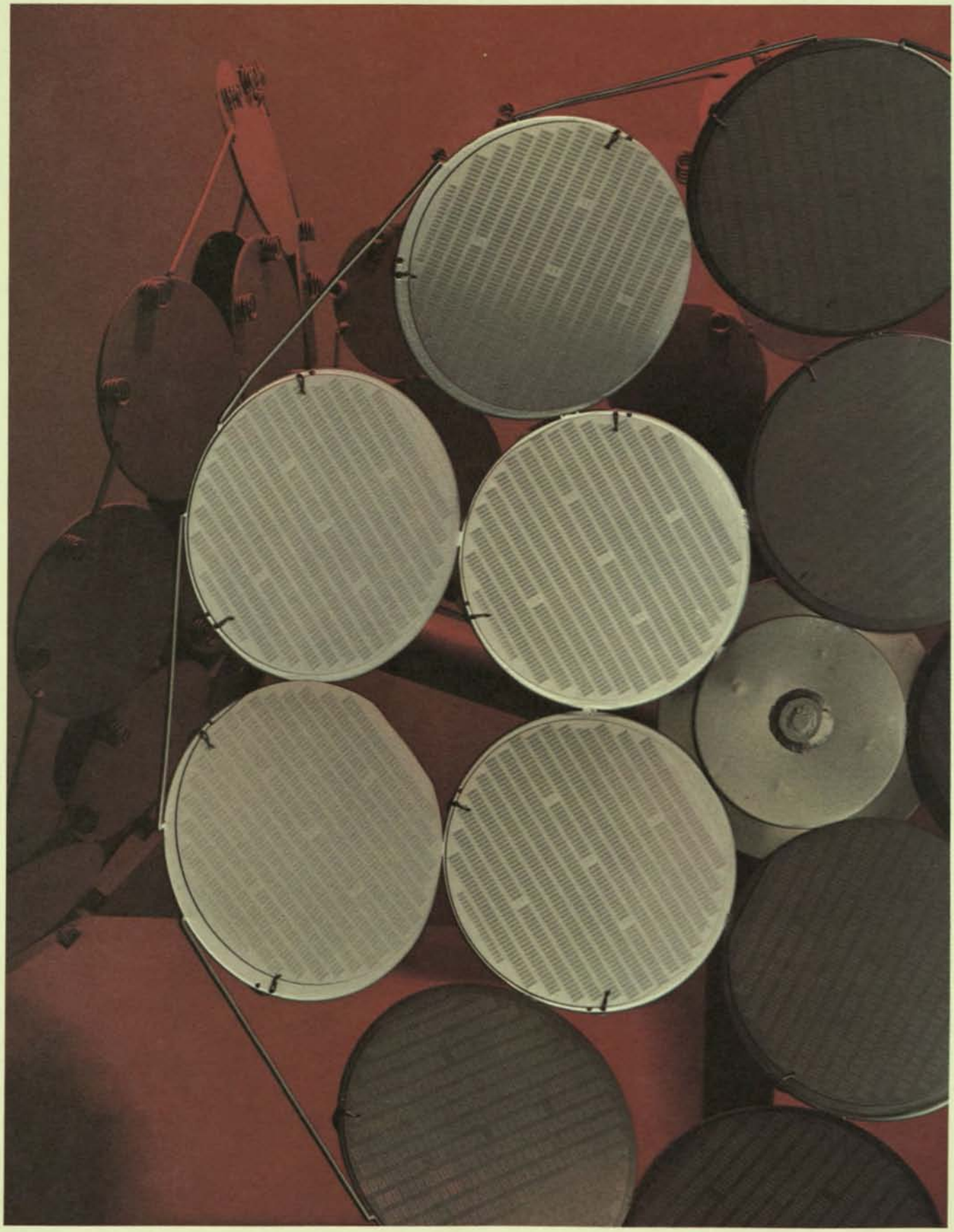
A multi-year capital investment program begun in 1979 is equipping this facility to continue work on technologies for the '80s and '90s. A new VLSI (very-large-scale integration) lab being constructed over several years incorporates wafer stepper lithography and plasma etching equipment needed to develop 256K (262,144 bit) and million-bit random-access memories. The Advanced Research and Development Laboratory also recently acquired a 40 megahertz electron beam mask maker, the most advanced of its kind in the world.

Investment in facilities and in additional staff will strengthen other current and planned programs in Palo Alto: computer-aided design (CAD), which is investigating revolutionary modeling and simulation techniques; applications of artificial intelligence to circuit design and testing; advanced logic, gate array and microprocessor technology, which should yield high-density, very fast integrated circuits; advances in CCD technology directed at developing solid-state image sensing devices; development of solid-state telecommunications circuits; and exploration of advanced silicon materials.

These broad studies are supported by development engineering and applications activities. New technologies are advanced to a pre-defined level of capability, then are transferred to a manufacturing operation. Such long-range projects, however, are complemented by many shorter term programs initiated and carried out completely within the operating groups. Engineering at this level accounts for a sizeable portion of Fairchild's total investment in research and development.

The auger spectrometer enables the analysis of the surface of a material without penetrating more than the outer layers. Important in semiconductor manufacturing, this electron-beam analytical tool can detect small amounts of impurities on the surface of a wafer.





Between 1965 and 1980, semiconductor technology progressed so rapidly that circuit density doubled every year. As circuit complexity approaches a half-million components on a silicon chip less than a quarter of an inch square, automated control of virtually every design and manufacturing step is required.

In 1960, a circuit designer would have initiated a new product design with a hand-drawn piece of artwork which depicted the handful of transistors, diodes and resistors that made up an integrated circuit. Today, designers of microprocessors, high-density memories and high-speed logic circuits use a sophisticated system of computer-aided design tools.

Circuit patterns are converted to digital coordinates and recorded on computer tapes. These tapes provide data to computer-driven layout machines, then to simulators which model expected performance of new circuits, and finally to machines which use an electron beam to etch circuit patterns on a set of glass masks. Many patterns in LSI (large-scale integration) are only two microns in width (one micron equals about 1/25,000 of an inch).

Similarly, Fairchild's manufacturing processes utilize computer-controlled equipment which contains the complete "recipe" for a particular circuit. Twenty years ago, wafer fabrication operators judged the color of the wafers with the naked eye to determine whether process steps were done according to specifications. (Color is related to surface oxide thickness, which, in turn, is related to process time.) Today, surface oxides are measured in angstroms (there are approximately 250 million angstroms in an inch), and dopants are implanted a few ions at a time. Such precision can only be achieved with a high degree of automation.

Fairchild manufactures devices that belong to every major area of semiconductor technology: diodes and transistors, TTL (transistor-transistor logic), digital logic circuits, bipolar and MOS (metal-oxide semiconductor) memories and microprocessors, and advanced CCD (charge-coupled device) circuits that can be used both as image sensors to create a television picture signal and as serial memories.

The company also produces analog devices, such as operational amplifiers and solid-state analog to digital converters, and optoelectronic sensors and displays, such as large-area liquid crystal alpha-numeric panels.

Semiconductors have become truly pervasive during the last decade. The entire computer industry is based on solid-state technology and accounts for about 70 percent of Fairchild's semiconductor business. Modern offices are rapidly acquiring electronic equipment and systems that likewise depend on semiconductors. And every modern home is full of solid-state components, from television sets and audio and video equipment, to pocket calculators, cameras, watches, home appliances – even toys.

This trend is accelerating rapidly, and some market areas, such as that for telecommunications equipment, have still to reach their full potential. In the future every home, office, business and factory will have systems such as small computers linked by telephone lines or microwave receiving stations to virtually unlimited information resources around the world.

With its leadership in silicon technology and processing capability, and demonstrated commitment to fundamental research, Fairchild will play a significant role in the development of these advances.

Sputtered aluminum is essential in providing the high-quality interconnection of transistors on Fairchild's integrated circuits. This structure, when placed in a vacuum chamber, rotates in a planetary motion, assuring even deposition of the metal on every wafer.

Fairchild's automatic test systems business evolved from equipment the company developed for testing its own semiconductor devices in the early 1960s. Though the company's principal products were, by today's standards, relatively simple, the equipment to adequately test them was not available commercially. As a result, Fairchild designed and built its own testers, eventually creating a major new business for the company.

Today, Fairchild's Automatic Test Equipment Group supplies leading semiconductor and computer manufacturers with systems for testing components and printed circuit board subassemblies. The rapidly expanding marketplace for test equipment also includes a variety of industries which use electronic components in their products: telecommunications, automotive, consumer electronics, military electronics and high technology equipment companies.

As the density and speed of semiconductor devices increases, it is both more important and more difficult to assure their reliability. So many functions now can be packed onto one chip that, often, if the chip fails, the system fails. On the other hand, thorough testing of the millions of interconnections on typical large scale integration (LSI) devices would take years.

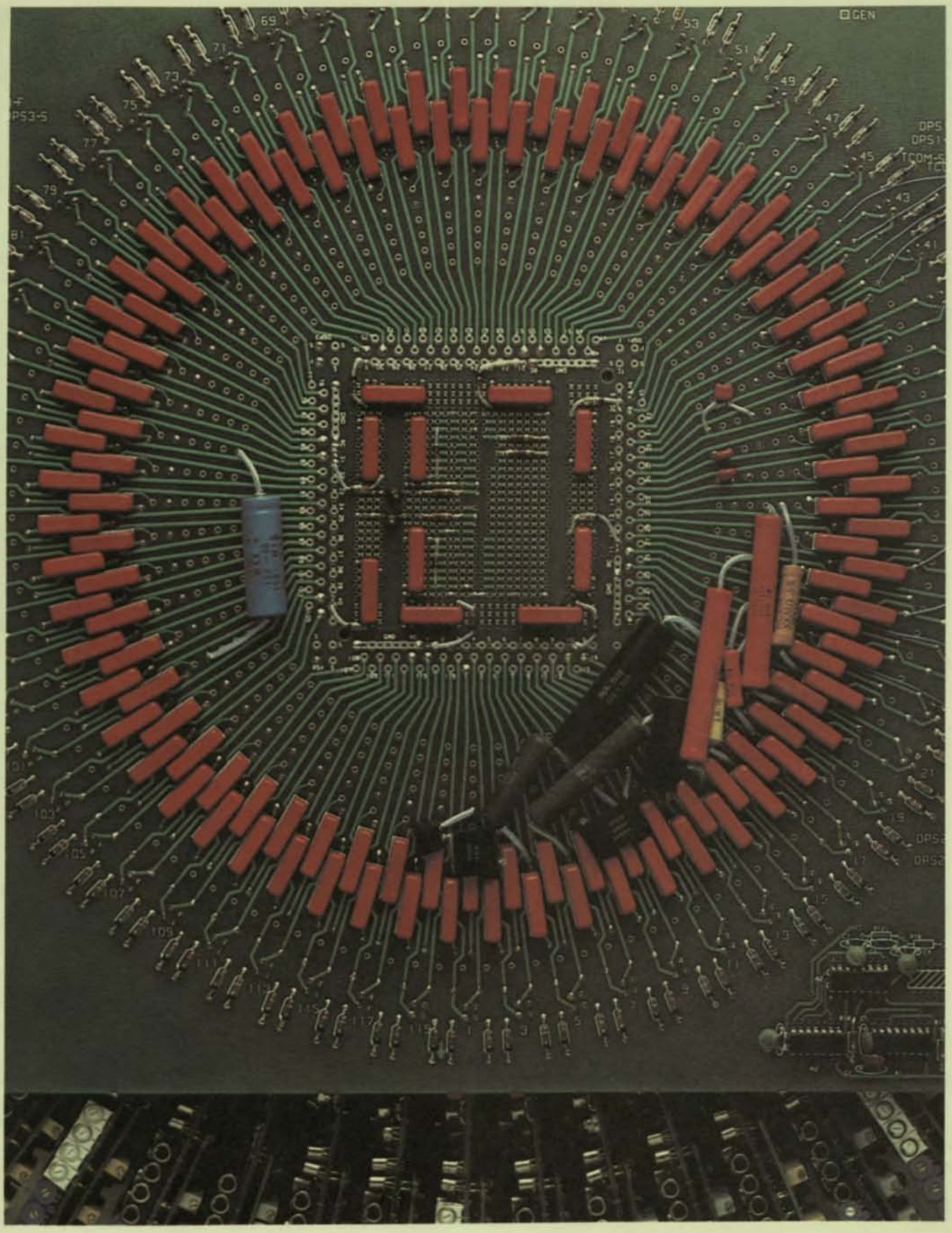
Fairchild is leading the industry in developing solutions to these problems, including the use of software to upgrade the performance of existing hardware. Products of the Component Test Systems Division are largely modular in design and include systems devoted to general purpose LSI testing; specialized memory testers; systems for VLSI (very large-scale integration) and very high speed circuits that represent the leading edge of technology; and testers for mixed signal and analog LSI devices.

In the future, techniques employed in board-level testing, such as automatic test program generation, may also be applied to component testing. Semiconductor and test equipment designers may combine their efforts so that a portion of the integrated circuit itself will be devoted to self-testing and self-diagnosis. Fairchild is also developing automatic tester controls which will reduce the burden on test operators.

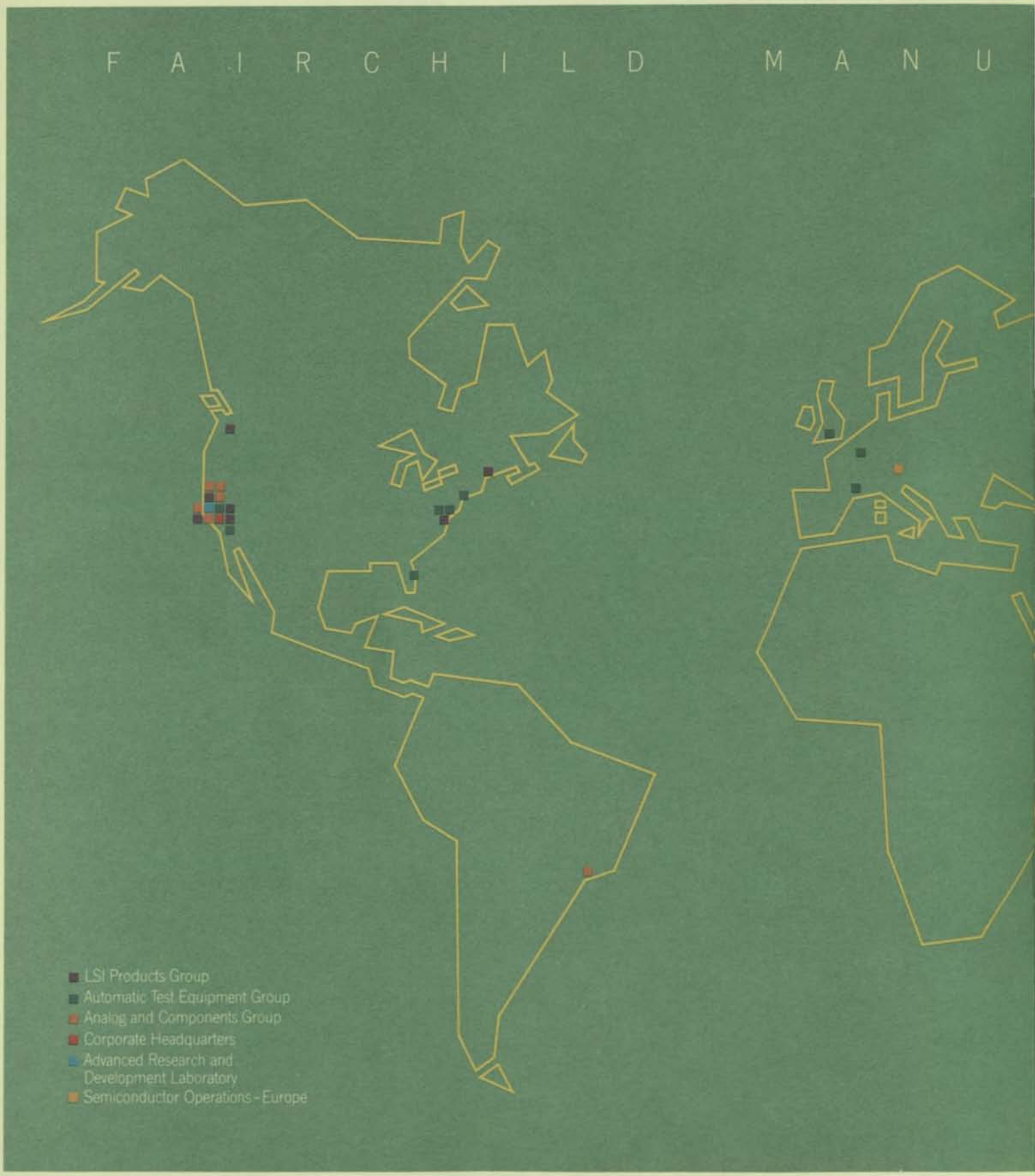
Printed circuit board testing has also grown significantly during the last decade. The large electronics assembly market is demanding testers which keep up with the increasing variety and complexity of devices on printed circuit boards, as well as software which simplifies test programming operations.

Products of Fairchild's Subassembly Test Systems Division meet the requirements of both types of board testing: in-circuit, which tests each component individually; and functional, which tests the function of the entire board.

This 60-pin performance board is used in Sentry V and VII, Series 20 and 60, and Sentinel test systems. It helps in the testing of integrated circuits in the production and incoming inspection and engineering areas.


GEN
69
71
73
75
77
79
81
53
51
49
47
45
43
41
DPS
DPS1
DPS2
DPS3
103
105
107
109
111
113
115
117
1
3
5
7
9
11
13
15
17
19
21

F A I R C H I L D M A N U



F A C T U R I N G

Corporate Headquarters

Fairchild Camera and
Instrument Corporation
464 Ellis Street
P.O. Drawer 7281
Mountain View, CA 94039
415-962-5011
415-962-2011

Advanced Research and Development Laboratory

4001 Miranda Avenue
Palo Alto, CA 94304
415-493-7250

3420 Hillview Ave.
Building 8
Palo Alto, CA 94304
415-493-7250

LSI Products Group

464 Ellis Street
P.O. Drawer 7281
Mountain View, CA 94039
415-962-5011
415-962-2011

Divisions

Bipolar Division
464 Ellis Street
P.O. Drawer 7283
Mountain View, CA 94039
415-962-5011
415-962-2011

11413 Meridian South
Puyallup, Washington 98373
206-848-3558

Static random access memories (RAMs), programmable read-only memories (PROMs), emitter-coupled logic (ECL) circuits, 100K ECL.

Gate Arrays
1801 McCarthy Blvd.
Milpitas, CA 95035
415-942-2500

Gate arrays (CMOS, ECL, TTL).

Digital Division
333 Western Avenue
South Portland, ME 04106
207-774-6211

Transistor-transistor logic (TTL) circuits, Schottky (TTL) circuits, Fairchild Advanced Schottky TTL (FAST) circuits, 10K ECL circuits.

MOS Division
101 Bernal Road
San Jose, CA 95119
408-224-7000

Static random access memories (RAMs), dynamic RAMs, erasable programmable ROMs (EPROMs), complementary metal-oxide semiconductors (CMOS).

Microprocessor Division
3420 Central Expressway
Santa Clara, CA 95051
408-773-1000

All Angels Hill Road
Wappingers Falls, NY 12590
914-297-0161

8-bit MOS microprocessors, 16-bit MOS microprocessors, 16-bit bipolar microprocessors, support circuits, design aid systems, microprocessor software, read-only memories (ROMs).

Foreign Manufacturing

Fairchild Singapore Pty., Ltd.
No. 11 Lorong 3
Toa Payoh, Singapore 12
Republic of Singapore
253-1066

P.T. Fairchild Semiconductor
KM 27.3, JL Raya Bogor
Ciburbut-Gandaria
Jakarta, Indonesia
870929

Domestic Marketing Locations

Northeast Region
5 Speen Street
Framingham, MA 01701
617-872-4900

Midstates Region
500 Park Blvd.
Suite 575
Itasca, IL 60143
312-773-3300

North Central Region
4570 West 77th Street
Suite 356
Edina, MI 55435
612-835-3322

Southern Region
1702 Collins Blvd.
Suite 101
Richardson, TX 75081
214-234-3391

Northwest Region
3333 Bowers Avenue
Suite 299
Santa Clara, CA 95051
408-987-9530

Southwest Region
15760 Ventura Blvd.
Suite 1027
Encino,CA 91436
213-990-9800

Analog and Components Group

464 Ellis Street
P.O. Drawer 7281
Mountain View, CA 94039
415-962-5011

Divisions

Linear Division
313 Fairchild Drive
P.O. Drawer 7282
Mountain View, CA 94039
415-962-4011

Operational amplifier circuits, comparators, interface circuits, television signal processing circuits, audio circuits, voltage regulators, telecommunications circuits.

Optoelectronics Division
3105 Alfred Street
Santa Clara, CA 95050
408-987-9000

Infrared sensors and emitters, LED lamps and displays, LCD displays, fiber optic connectors, optical couplers.

Hybrid Products Division
369 Whisman Road
Mountain View, CA 94043
415-962-5500

Ignition modules, voltage regulators, hybrid circuits.

Discrete Division
4300 Redwood Highway
San Rafael, CA 94903
415-479-8000

Diodes, diode arrays, transistors.

Materials Division
33 Healdsburg Avenue
Healdsburg, CA 95448
707-433-6541

Silicon wafers.

Foreign Manufacturing

Fairchild Semiconductor (HK) Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
3-890271

Fairchild Semiconductor Ltd.
219-6 Kari Bong Dong
Kuru-Ku
Seoul, 150-06, Korea
2-855-6751-5

Fairchild Philippines
P.O. Box 981
Cebu City,
Cebu, Philippines
8-50-41

Fairchild Semiconductores Ltda.
RUA Oswaldo Cruz, 505
CAIXA Postal 948
13100 Campinas SP, Brazil
192-416655

Domestic Marketing Locations

Northeast Region
5 Speen Street
Framingham, MA 01701
617-872-4900

Central Region
7702 N. Shadeland
Castle Point #205
Indianapolis, IN 46250

Southeast Region
Executive Plaza
Suite 511
500 Wynn Drive
Huntsville, AL 35805
205-837-8960

Western Region
1570 Brookhollow
Suite 206
Santa Ana, CA 92705
714-557-7350

Foreign Marketing Locations

Fairchild Semiconductors Ltd.
CAIXA Postal 30407
RUA Alagoas, 663
01000 Sao Paulo SP, Brazil
11-66-3645

Semiconductor Operations Europe

Fairchild European Headquarters
11, Boulevard DeLa Tour Maubourg
75007 Paris, France

Mailing address:
42, rue Saint Dominique
75007 Paris, France
1-555-9123

Fairchild Electronics G.M.B.H.
8090 Wasserburg
AM Burgfried 1
West Germany
(8071) 1030

Fairchild Camera and
Instrument (U.K.) Ltd.
European LSI Design
and Application Centre
Shire Hall
Shinfield Park
Reading, Berkshire
United Kingdom
(734) 875-444

Marketing Locations

Fairchild Camera and Instrument
(UK) Ltd.
230 High Street
Potters Bar
Hertfordshire, ENG 65 BU
United Kingdom
707-51111

Fairchild Camera and Instrument
(France) SA
121 Avenue d'Italie
75013 Paris, France
1-584-5566

Fairchild Camera and Instrument
(Deutschland) GmbH
Daimlerstrasse 15
8046 Garching-Hochbruek
Munich, West Germany
89-32003

Fairchild Semiconducttori SPA
Viale Corsica 7
20133 Milan, Italy
296001-5

Semiconductor Operations Asia

Fairchild Asian Headquarters
Dai-Ichi Seimei Building
7-1 Nishi Shinjuku 2-Chome, 14th Floor
Shinjuka-KU, Tokyo 160
Japan

Marketing Locations

Fairchild Japan Corporation
7th Floor Pola Shibuya Building
15-21, Shibuya 1-Chome Shibuya-KU
Tokyo 150, Japan
81-03-400-8351

Fairchild Semiconductor Products Ltd.
135 Hoi Bun Road
Kwun Tong
Kowloon, Hong Kong
852-3-890271

Automatic Test Equipment Group

1601 Technology Drive
San Jose, CA 95115
408-998-0123

Divisions

Component Test Systems Division
1601 Technology Drive
San Jose, CA 95115
408-998-0123

General Purpose LSI
1601 Technology Drive
San Jose, CA 95115
408-998-0123
Component test systems.

Xincom
1800 Tapo Canyon Road
Simi Valley, CA 93063
805-583-5290
Memory test systems.

Subassembly Test Systems Division
299 Old Niskayuna Road
Latham, NY 12110
518-783-3600

Faultfinders
299 Old Niskayuna Road
Latham, NY 12110
518-783-3600
In-circuit printed circuit board test systems.

Mechanical
One Fairchild Square
Clifton Park, NY 12065
518-877-7042
Test fixtures and probes.

Titusville
1400 White Drive
Titusville, FL 32780
305-267-7212
Clip access digital test systems; PCB interconnect analyzers.

Series 70
3 Suburban Park Drive
Billerica, MA 91821
617-663-6562
Functional printed circuit board test systems.

Automatic Test Equipment–Europe
12, Place des Etats-Unis
92120 Montrouge
France
657-1107

Membrain
23 Cobham Road
Ferndown Industrial Estate
Wimborne
Dorset BH217PE
England
44-202-893535

Functional printed circuit board test systems.

Component Test Systems–Europe
Rue du Vercors
Zone 1 La Chauvetiere
42100 St. Etienne
France
33-77-579115

Component test systems.

Automatic Test Equipment–Japan
Tomioh Building, 1st Floor
4-1, 2-Chome, Shibazaki,
Tachikawa, Tokyo 190
Japan
425-27-5811

Memory test systems.

Automatic Test Equipment Training Centers

3 Suburban Park Drive
Billerica, MA 01821
617-663-6562

299 Old Niskayuna Road
Latham, NY 12110
518-783-3600

1601 Technology Drive
San Jose, CA 95115
408-998-2361

1800 Tapo Canyon Road
Simi Valley, CA 93063
805-583-5290

6B-7B, Block 15
996, Bendemeer Road
Kallang Basin Industrial Estate
Singapore 1233
65/2966155

Albert Schweitzer Strasse 66
8000 Munich 83, West Germany
49-89-672061

Domestic Marketing Locations

2002-D Greentree Executive Campus
Route 73
Marlton, NJ 98053
609-983-3100

1002 E. Algonquin Road, Suite 104
Schaumburg, IL 60195
312-397-8480
312-397-7505

1601 Technology Drive
San Jose, CA 95115
408-998-0123

900 Plano Park Way, Suite A
Plano, TX 75074
214-422-7200

505 Northern Boulevard
Great Neck, NY 11021
516-466-6393

17682 Mitchell North, Suite 100
Irvine, CA 92714
714-549-7885

Foreign Marketing Locations

23 Cobham Road
Ferndown Industrial Estate
Wimborne
Dorset BH217PE
England
44-202-893535

4, Avenue des Bosquets
78180 Montigny Le Bretonneux
France 1
33-3-043-0609

Albert Schweitzer Strasse 66
8000 Munich 83, West Germany
49-89-672061

Tomioh Building, 1st Floor
4-1, 2-Chome, Shibazaki,
Tachikawa, Tokyo 190
Japan
0425-27-5811

6B-7B, Block 15,
996, Bendemeer Road,
Kallang Basin Industrial Estate
Singapore 1233
65-2966155

Schlumberger Limited

277 Park Avenue
New York, NY 10017
212-350-9400

Schlumberger Limited
42, rue Saint Dominique
75007, Paris, France
1-555-9123

FAIRCHILD

A Schlumberger Company

Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, CA 94039