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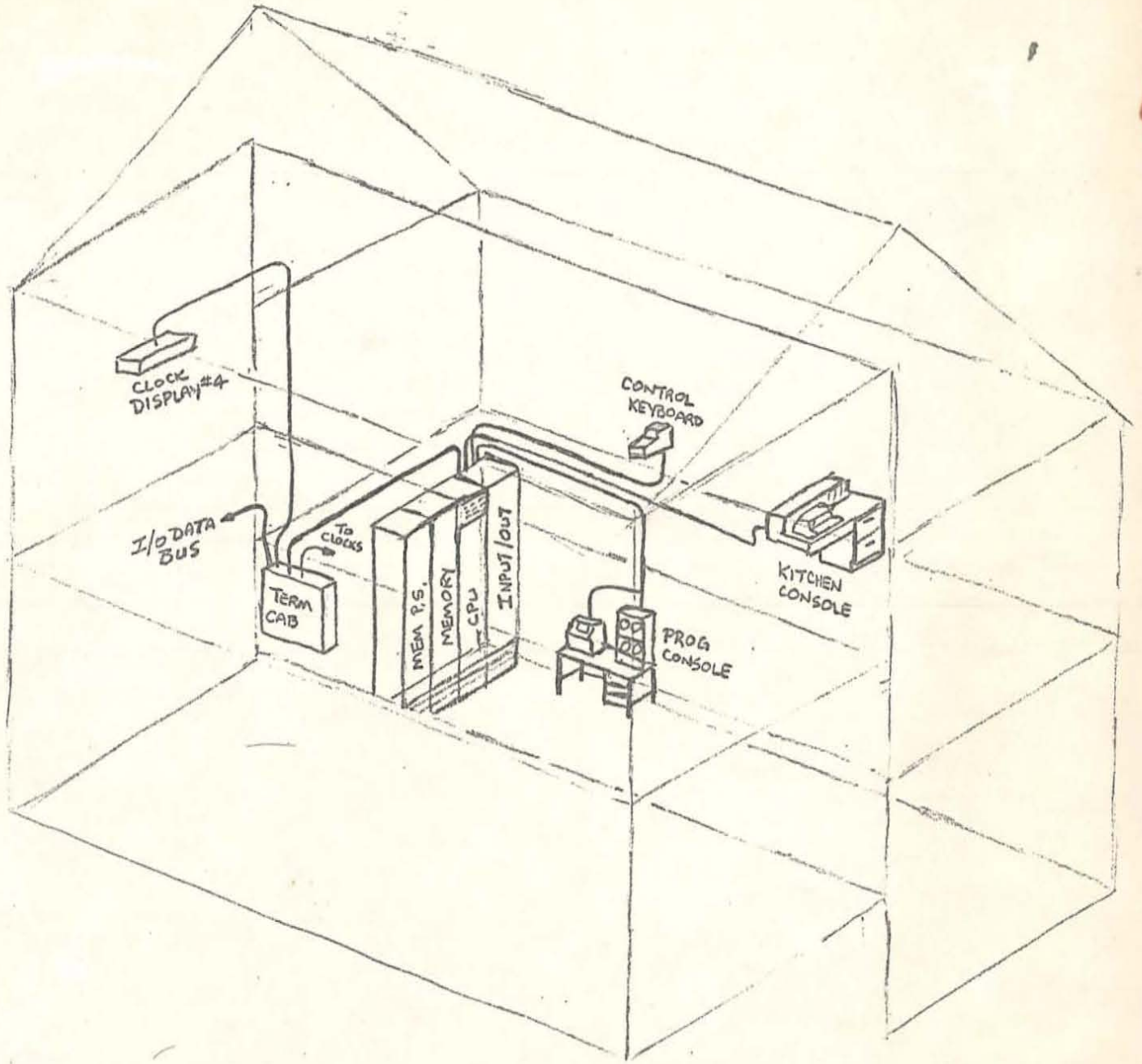
ELECTRONIC COMPUTING HOME OPERATOR - Designed by James F. Sutherland



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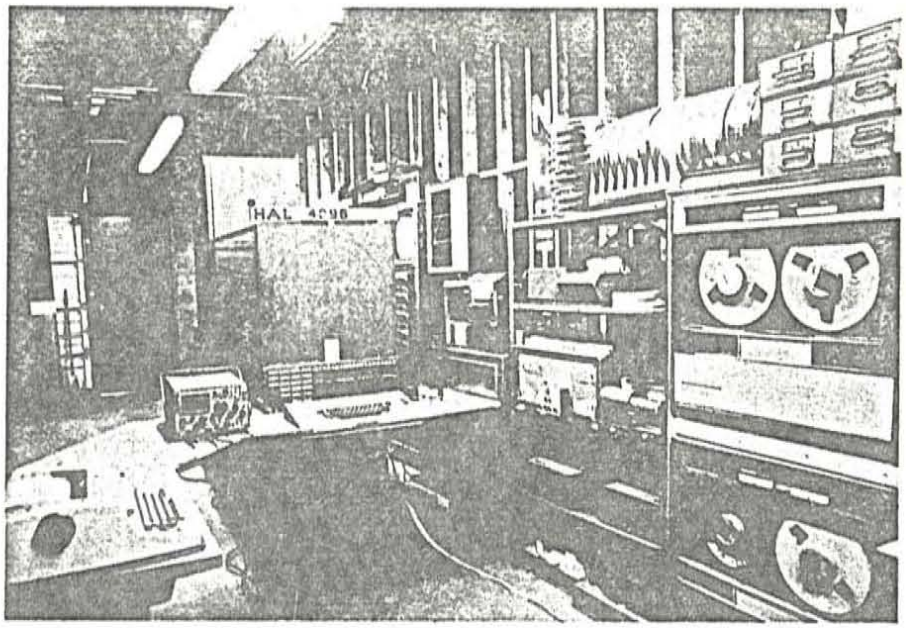


Photo 1: Hal Chamberlin's home built HAL-4096 computer system, built in 1972. This system, which is still in service handling IO for an IMP-16 microcomputer system, features TTL logic, a 16 bit word length, 16 registers, 4 K bytes of magnetic core memory (a surplus IBM 1620), and priority interrupt.

The First Ten Years of Amateur Computing

Sol Libes
President, Amateur Computer Group of New Jersey
995 Chimney Ridge
Springfield NJ 07081

If one could find a specific date for the birth of personal computing, it would be May 5 1966.

Most people I meet are under the mistaken notion that personal computing started only two or three years ago, with the introduction of the Altair 8800 by MITS. Nothing could be further from the truth. In fact, the amateur computing hobby was then almost ten years old.

I therefore decided to write this article to set the record straight, give credit to the early pioneers in this hobby and shed some light on the early history of microprocessors.

If one could find a specific date for the birth of personal computing, it would be May 5 1966. For it was on that date that Steven B Gray founded the Amateur Computer Society and began publishing a quarterly called the *ACS Newsletter*.

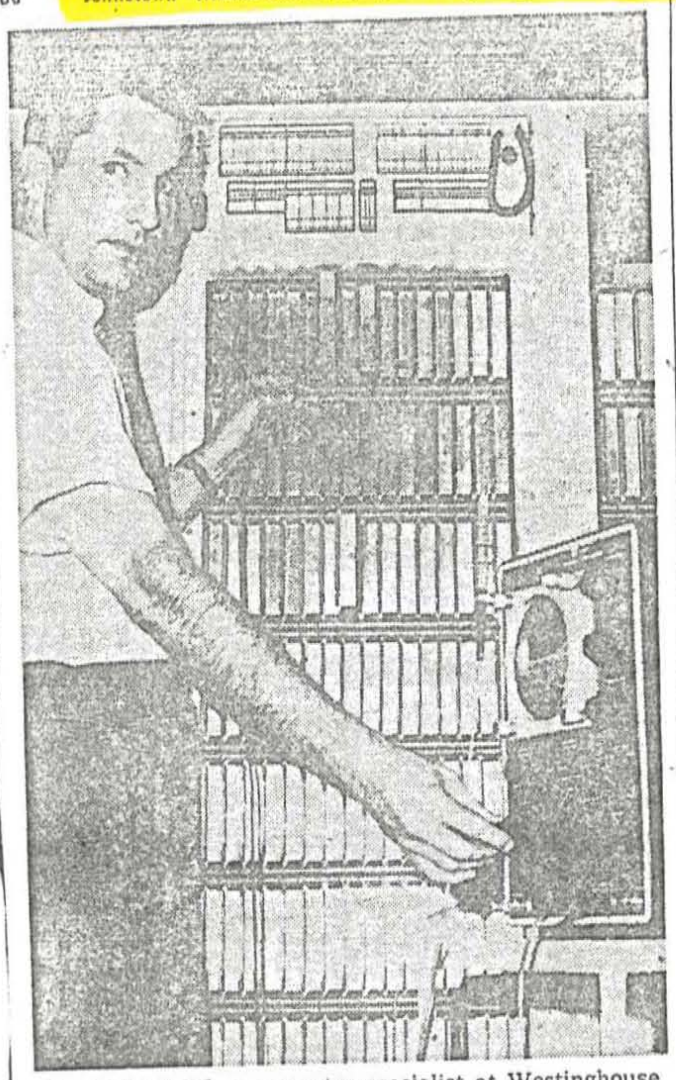
The newsletter exchanged information on where to get surplus computer gear, how to build not too complicated circuits, where to get integrated circuits, tips, experiences and where to get help. By the end of 1966, the Society reported that it had over 70 members.

1966 also saw the publication of the first books on how to build a home computer. Typical was *We Built Our Own Computers* by A B Bolt and published by Cambridge University Press.

In January 1968, a survey in the *ACS Newsletter* reported that two amateurs had their home built systems up and running and that many others were actively working on their systems. The survey indicated that programmable memory sizes ranged from 4 to 8 K with some as high as 20 K, all magnetic core of course. Teletypes and Flexowriters were popular for IO. Clock speeds ranged from 500 kHz to 1 MHz, with the average 500 kHz. Most used discrete transistors, and a few reported using those new and hard to come by RTL integrated circuits. Instruction sets were small, ranging from 11 to 34 instructions. Word sizes were from four to 32 bits, with 12 bits the typical number. Registers ranged from two to 11, with three most common. Most reported that they had been working on their machines for about two years.

The April 1968 issue of *Popular Mechanics* reported on ECHO IV (Electronic Computing Home Operator), a home built computer constructed by Jim Sutherland. It had four registers, used a 15 bit word, had 8 K bytes of core memory, 18 instructions and a clock speed of 160 kHz.

In December 1968 Don Tarbell (now



Jim Sutherland, a computer specialist at Westinghouse Electric Corp., checks over the computer built at his suburban Pittsburgh home. After programming, the computer will take charge—and tell Sutherland and his wife what's needed in groceries, how to handle the household budget and even predict the weather.
(AP Wirephoto)

Computers Seen as Boss of Household

By BOB VOELKER

PITTSBURGH (AP) — Tired of having people tell you what to do? Brace yourself--for the worst.

A new commanding voice is being heard across the land. It's only a whisper now. But someday it might be roaring at you in your home.

It's a computer.

Nowadays, computers aren't bothering you. There are only a relative handful around; and they're busy doing things like running steel mills and chewing up mountains of banking data.

"Mother's Little Helper"

But they have a fiendish eye on your home--with invasion in mind. They'll probably sneak in under the innocent-sounding guise of "mother's little helper."

Jim Sutherland, a computer specialist at Westinghouse Electric Corp., is among those who foresee the invasion. Matter of fact, he's aiding and abetting it.

Sutherland, 33, has built a computer in the basement of his suburban Plum Borough home. Now, he's busy programming it; that is, telling it what he wants it to do.

Later, the computer will take charge--and tell Sutherland and his wife what to do.

Household Bookkeeping

Initially, Sutherland is setting up programs to handle household bookkeeping and to prepare shopping lists.

He says home computers eventually will:

--keep an inventory of groceries on hand--and tell you what to buy.

--keep track of family finances--and tell you what luxuries to cut out.

--predict the weather--and tell you to wear an overcoat.

--keep track of your diet--and tell you to lay off the booze.

No Talking Back

There's no talking back to the computer. All you can do is listen--and squirm.

Sutherland, who dubbed his computer ECHO-IV for Electronic Computer for Home Operations, says:

"Actually, the number of things ECHO-IV will do around the home is almost unlimited.

"For instance, I plan to eventually hook up television sets to the system. When my wife, Ruth, or one of our three children wants to leave a message for other members of the family, they'll simply type it into the computer which will display the message on the TV screens."

Could Aid Golfer

Sutherland says a computer could be set up to tell a golfer what's wrong with his swing. He would swing at a stationary ball, and the computer would say something like:

"You didn't keep your head down, you jerk."

He predicted computer magazines will be published some day telling about new challenges and successes and presenting "game" problems.

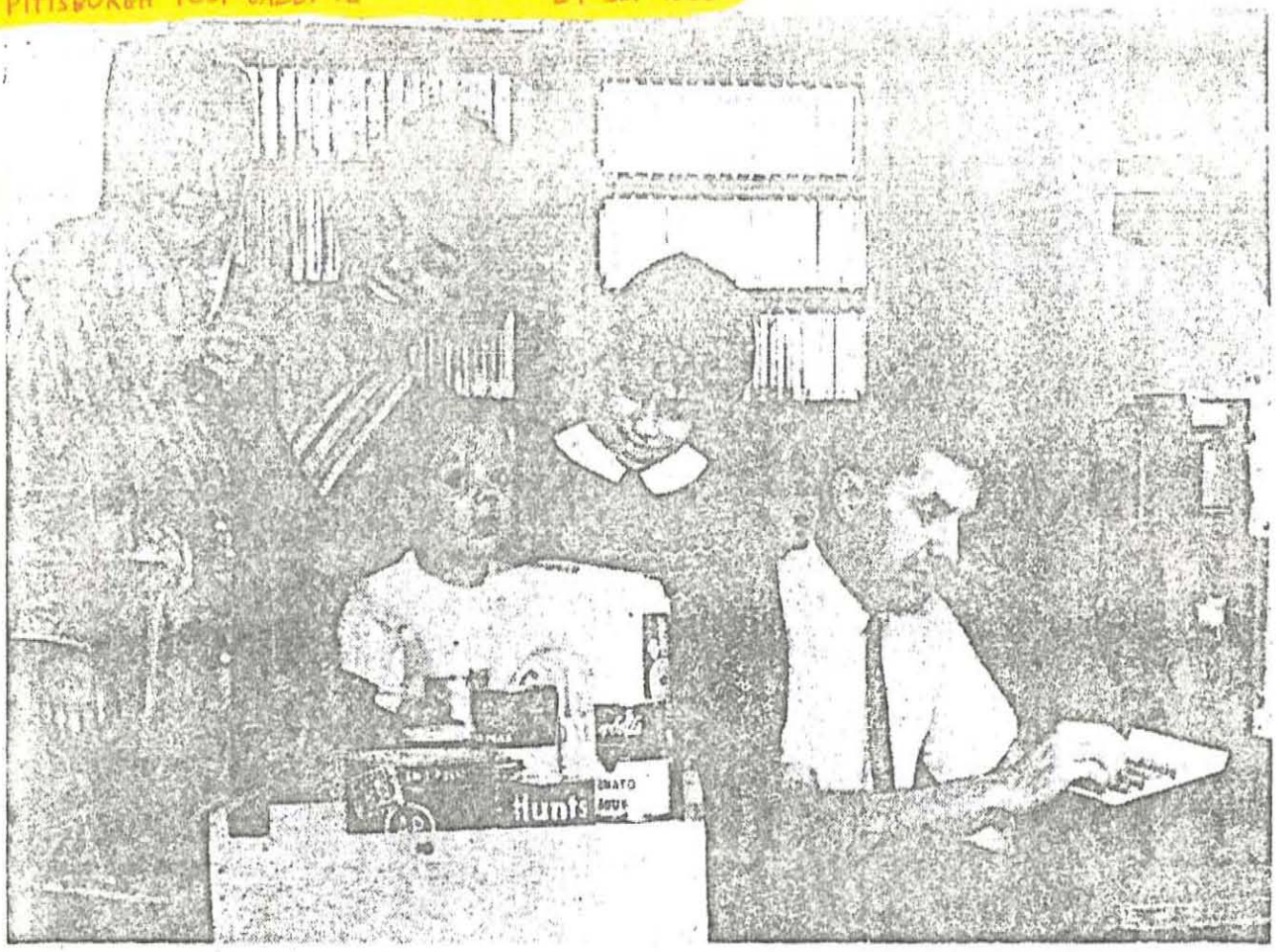
He predicts computer tapes and records will be available much like today's recording tapes and records. A person will buy a tape, say for bookkeeping, then program into it his own personal data.

Sutherland put together his computer from obsolete parts and some equipment borrowed from Westinghouse. He estimates such a computer is worth about $10,000.

In time, he says, the cost will be reduced considerably. He feels people will start tinkering with home computers when the cost becomes comparable to that of early model color television.

Then, the invasion starts in earnest.

PITTSBURGH POST-GAZETTE 24 SEP 1966



—Post-Gazette Photo

While Jim Sutherland checks his homemade computer, daughter Sally is buttoned up for rain by her mother. Jay and Ann look over food, one of many household items managed by selective device ECHO-IV.

ECHO TO DO 600 HOUSEHOLD TASKS

Computer Carries Family Load In Engineer's Suburban Home

By DENNIS CASEY
Post-Gazette Staff Writer

Days of compiling shopping lists for trips to grocery stores are never over for Mrs. Ruth Sutherland, who will find out exactly what foods she needs by asking the computer her husband built in their Plum Borough home.

And if you think that sounds "1984ish," get a load of this: The computer, which look innocuous enough in the Sutherlands' basement, will keep track of family finances, predict the weather, run digital coded computer clocks, turn television sets and radios on and off, print recipes and control the house temperature.

And all that is just a start, according to James Sutherland, 33, whose family lives in a split-level home at 4837 Havana Drive. Sutherland, a Westinghouse Electric Corp. computer systems engineer, plans for his machine eventually to perform 600 tasks in the house.

For Jim, the computer is the culmination of a year's labor of love, during which he used discarded computer components and spare time to work on the machine. "I started it mostly just as a hobby," he said. "It was a way to unwind after coming home from work."

Jim designed the computer from scratch, making schematic sketches and mooching obsolete computer components from his company. "They were glad to give them to me," he said.

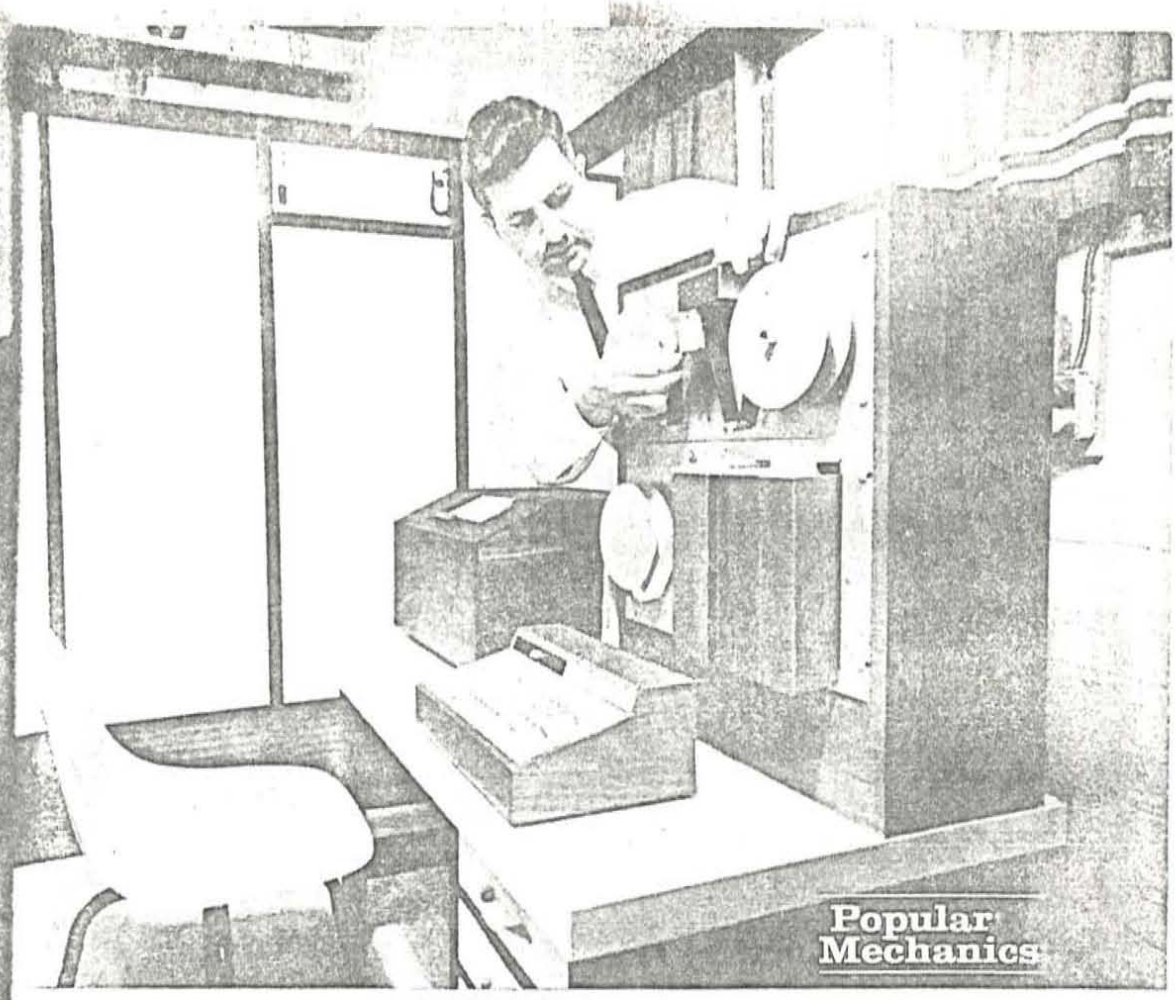
The computer, which Jim dubbed with the acronym ECHO-IV (Electronic Computer for Home Operation), stands about six feet high and takes about seven feet of floor space at one end of the family's basement.

Jim figures that to program the computer completely (which he explained means "give it directions on what to do") will take him about ten years of work in his spare time.

Clocks in the Sutherland home already are set up to run from the computer, as does one in the living room. It is a clock without hands or the conventional arabic numerals. It consists of sets of lights, which flash on and off.

"The kids could read this before regular clocks," he mused while glancing up at it. "We have one regular clock – that's in the kitchen stove, so we couldn't do too much about it."

Jim has two daughters, Sally, 6, and Ann, 10, and a son, Jay, 19 months. Jim said his son shows a penchant for computers as he plays around ECHO and drags pieces of wiring around with him. It's easy to imagine Jay 15 years from now asking the computer if he can use the car for an evening or will the conversation be a helicopter [illegible]



HOMEMADE PROGRAMMER'S DESK contains keyboard, page printer, paper tape punch and paper tape reader

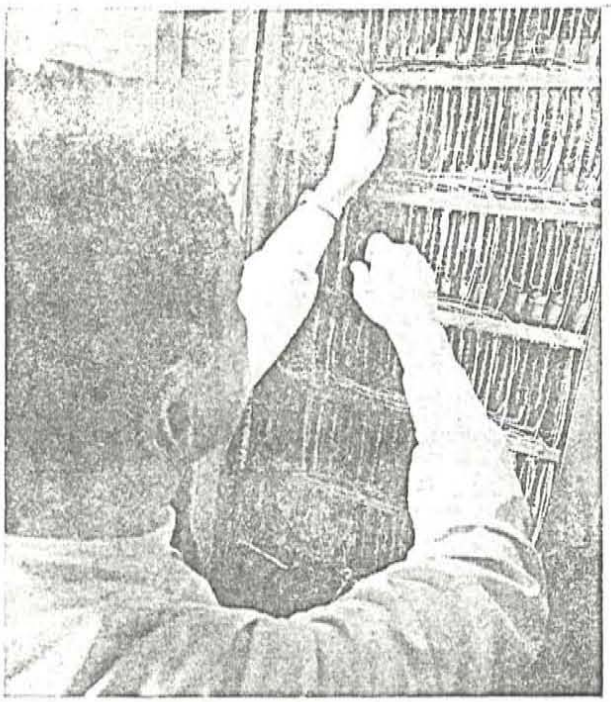
A Computer in the *Basement?*

Jim Sutherland's home-built computer is not very sophisticated by today's standards—or tomorrow's. But as it takes on more tedious household tasks, it's proving what can be expected of the future home computer

By GLENN INFIELD

THERE HAVE BEEN many predictions that the home of tomorrow will be radically different from the home of today, because it will be run by a computer. But no one knew precisely what a computer could do in the home until Jim and Ruth Sutherland of Pittsburgh, Pa., designed, built and programmed "ECHO IV." ECHO means Electronic Computing Home Operator, and building it has been a family affair.

Jim is a computer-systems design engineer with Westinghouse Electric Corp., and his wife, Ruth, is a home economist. Their home-computer venture began two years ago when, as a hobby, Jim started buying obsolete computer parts and sketching logic circuit diagrams. Actual wiring of 11 printed-circuit module mounting panels began as soon as the design stage was completed. Within the year, ECHO was running simple programs but was limited by an inadequate input-output



SUTHERLAND goes over the intricate wiring required to build ECHO. Each of four units has such a panel

capability. To overcome that handicap, Jim produced a programmer's desk consisting of a keyboard, page printer, paper tape punch, and paper tape reader in oiled walnut enclosures.

Before the end of the second year what was formerly the family basement playroom had been taken over by the home computer and its peripheral equipment and Ruth was wondering, "Will it replace *me*?"

She isn't worried about this now, since she has learned that *home* computer programs must first be flowcharted by someone who knows *homemaking*. Flowcharts define the job graphically, so that the programmer and the user can understand each other.

Usually, shortcuts and time-saving features show up when the flowchart is prepared for a task prior to translating it into computer language. Later, if program revisions are needed, the flowchart provides a quick review of how the program operates. Changes and/or corrections in the flowchart can easily be inserted into the program listing of instructions.

The Sutherlands feel that if the homemaker programs some of her own

RUTH SUTHERLAND programs computer which can control temperature, set clocks, tabulate home bills

tasks, she will better understand how the computer operates and become skilled in determining best household applications.

Simple keyboard entry and printer output routines were the first ECHO programs the Sutherlands wrote. These were followed by the paper tape input and paper tape punching routines. Subsequently these programs permitted other, more complicated programs to be entered into the computer, verified on the printer, and stored permanently on paper tape. Jim is now devoting his time to writing such programs as multiply, divide, multiple precision add, subtract, and message writer routines.

As more jobs are loaded into ECHO,

INPUT-OUTPUT UNITS are made from an electric typewriter keyboard and a surplus teletype printer

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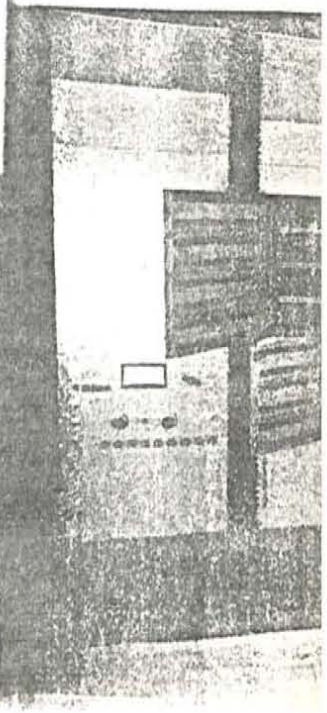

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its core memory storage capacity of 8192 words may be exceeded, and that's when Jim will begin building some magnetic-tape auxiliary bulk memory units. The computer understands 18 commands—or machine language instructions—which can be arranged into computer programs and stored in memory for future use. Some of the larger programs will be stored on paper tape and loaded into the computer when needed.

Now that the basic routines are running in ECHO IV, the Sutherlands are planning to delegate the chores of bookkeeping to the computer. Tabulating monthly budgets and accounting for monthly expenditures is a time-consuming job that ECHO will reduce to simple end-of-the-month routine. Specifically, when April 15 rolls around, income-tax deductions can be identified and grouped so that tax forms can be filled out readily.

One important task which ECHO performs reliably is the updating of the hour portion of binary-coded decimal clock displays found in four different rooms of the Sutherland home. Jim designed and built the timepieces several years ago, and even though the clocks have no hands, the children learned to tell time by them before they understood ordinary clocks.

ECHO will also be programmed to keep track of real time so that events can be scheduled up to a year in advance with one-second accuracy. Ruth isn't interested in running their home on a second-by-second schedule, but she feels Jim won't be able to make excuses about forgetting birthdays and anniversaries ever again.

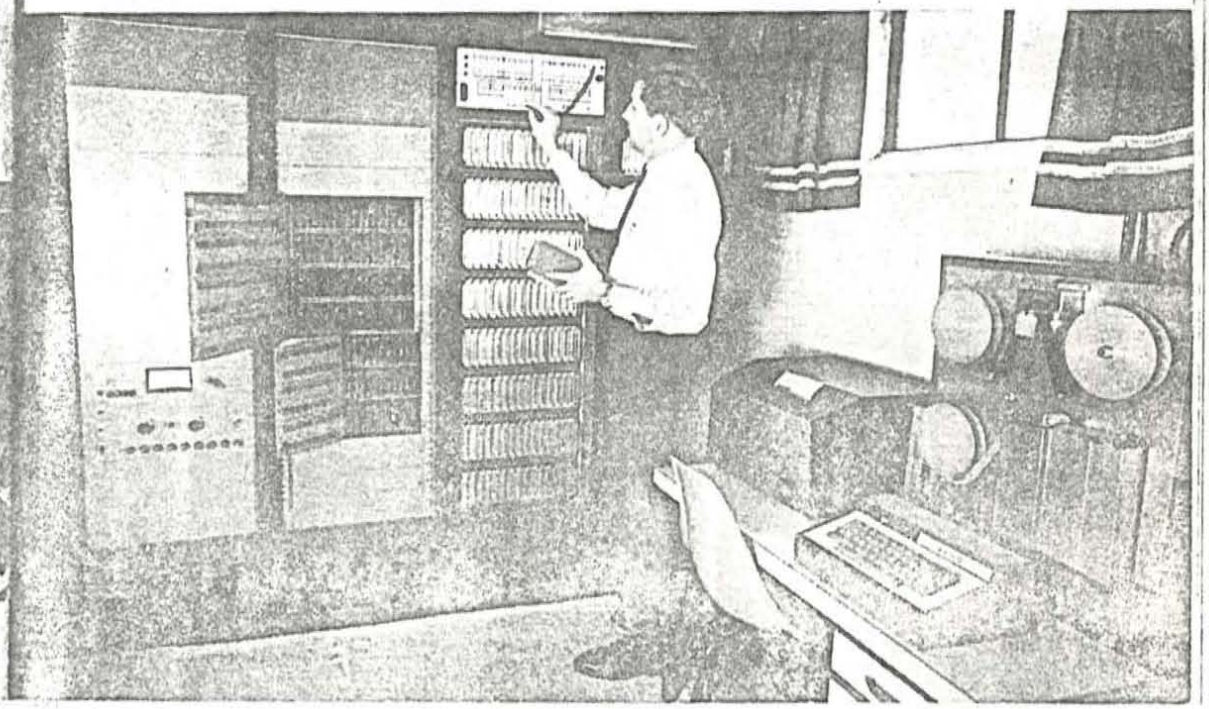
Ruth believes that the kitchen is where the computer will really perform well and save time in routine jobs. Recipes will be increased or decreased proportionately to provide any number of servings, with the necessary shopping lists printed out automatically.

"To be really effective," Jim says, "the computer must know how much and what kind of food is on hand so allowances can be made in shopping lists."

Jim plans to modify the kitchen cabinets to allow ECHO to take inventory automatically. Later, as more complex programs are tried, the computer will

(Please turn to page 209)

ECHO with two of the front panels removed. Computer takes about 20 square feet of basement floor space



COMPUTER IN HIS BASEMENT

(Continued from page 79)

generate balanced menus with specific calorie and nutrient content, from which the family can select their meals in advance.

ECHO provides the Sutherlands with a proving ground for experimental family games. The Sutherland children—Ann, 11; Sally, 7; and James Scott, 2—are looking forward to programming and playing games on the computer. As television displays are added to the system, many new games involving logic and strategy will provide family entertainment.

Recently Jim connected his color TV to a controller that will eventually allow ECHO to regulate the TV schedule. For instance, on a school night, the children might have to answer correctly some key questions via the keyboard before ECHO will switch on the set. The antenna rotator will also be controlled by ECHO to insure proper alignment of the antenna with the corresponding channel number entered through a control keyboard. This way, one manual entry directs both set and antenna to the desired channel.

Automatic temperature control

Jim will experiment with the computer as a temperature-controlling device for the home. After interrogating weather instruments on the outside of the house, the computer will be programmed to compensate for weather changes and make automatic temperature and humidity adjustments on the inside. Purely for his own interests, he hopes to use ECHO as an aid in short-term local weather prediction. Jim has a degree in meteorology from Penn State University, which was received while he was on active duty as a weather officer in the U.S. Air Force. He and Ruth also hold degrees from the University of Missouri which Jim attended through a Westinghouse scholarship won in a National 4-H Farm and Home Electric contest.

The Sutherlands are pioneers in the field of home computers and undoubtedly will discover that the best computer applications will evolve through everyday experiments. Although many of the uses planned for ECHO sound impractical and impossible, Jim notes that many of today's computers and their uses would have sounded farfetched to people 20 years ago.

For instance, at age 15, Jim constructed a model electrified farm to show various farm groups how they could do more work with the aid of electricity. "Several national magazines carried stories on the project; the one I value most appeared

(Please turn to page 229)

BIG RISE OF LITTLE SINKERS

(Continued from page 220)

visibility, however, marine scientists and others with business in the deep are glad to pay substantial sums to use the small subs. The Navy, for one, leases a number of them for work on the development of military undersea techniques—submarine communication, detection and weaponry. Others use them as workboats for undersea construction, surveying, salvage, mineral prospecting and inspection of underwater equipment such as cables.

Daily rent $300 to $10,000

What does it cost to hire one? Prices vary, depending on the size, payload and depth capability, but a rough rule of thumb is $1 or $2 per foot of depth. The smallest, shallow-diving subs rent for $300 to $500 a day, but you could pay as much as $5000 to $10,000 a day for the deeper-diving vessels.

Obviously, it's too expensive for joy-riders, so the money goes for jobs that are worth doing and worth risking in the harsh, alien, unforgiving deep seas.

Remarkably, not one life nor one small sub has been lost to date. Let's hope no one gets overconfident. ★★★

COMPUTER IN HIS BASEMENT

(Continued from page 209)

in March, 1949, in *Popular Mechanics*," Jim reminisces.

In that same issue, there was an article describing the first electronic computer built by Echert and Mauchley at the University of Pennsylvania. One of the predictions made then was that "Computers in the future might have only 1000 vacuum tubes and perhaps weigh only one and one-half tons."

However, since that time, transistors have replaced tubes and today's integrated circuits are replacing transistors. To illustrate the radical reduction in size which has been made possible by molecular electronics, one need only note that space-age computers now weigh only a few pounds.

"Computers are capable of being programmed to perform important household tasks today, but when we look ahead 20 years, even our wildest expectations will probably seem pale when compared to what ECHO, 1987 version, may be doing for us." One thing is certain, the Sutherland family of Pittsburgh will know from firsthand experience how to get the most from an ECHO "genie." ★★★

ACS NEWSLETTER

a publication of the
AMATEUR COMPUTER SOCIETY

Number 8 January 1968

COMPUTER SURVEY RESULTS

SEE PAGE 4

ACS COMPUTER SURVEY RESULTS

Although not many ACS members sent in the computer survey forms, those who did are, not surprisingly, the furthest along with their machines. Two have finished.

Memory

Most of those who answered the survey are using core memory, with sizes ranging from 4K to 20K words; the majority are equally divided between 4K and 8K.

One member uses a delay line for memory, containing 512 words. Another uses a delay line (2K bytes), drum (8K bytes) and core memory (4K bytes); 4-bit bytes.

For his small machine, one member uses flip-flops for memory. Another uses punched paper tape, having convinced himself that "tape would eliminate the memory limit."

Input

Teletype is the most common input device. One member, however, uses a Flexowriter. Another uses punched cards, keyboard, magnetic tape, paper tape, and keyboard switches.

Output

Again, Teletype is the most common output device. Others include a Kleinschmidt printer, paper tape punch, IBM Selectric typewriter, lamps, and Nixie tubes. One member uses magnetic tape, paper tape, Selectric typewriter, printer and lamps. And the member with the Flexowriter also uses it for output.

Clock

Clock speeds include 100K, 160K, 250K, 500K, and 1Mc, with one given as 10-100K. The average is 500K.

Serial or Parallel

The situation is about equally divided into thirds: one-third serial; one-third parallel; one-third combinations such as serial character, parallel bit.

Transistor Types

A wide range here, of course. One uses only 2N404. Another, 2N2923, 2N3721, 2N2711 (npn) planar. A third, 2N2923, 2N2925, 2N3906. A fourth, MPS3640, MPS3646, and 2N3641 in core drivers.

Integrated-Circuit Types

(1) uses Fairchild RTL (67¢ FF, 36¢ dual 2-input gate, 36¢ buffer). (2) Fairchild RTμL and CTμL. (3) Motorola RTL (700P series). (4) Motorola and Fairchild RTL.

Card Types

None of those replying use surplus IBM or Univac cards, although one uses surplus Westinghouse RTL NOR gates. Another is considering Wyle modules. A third designs and etches his own PC cards. A fourth makes his cards from Vector boards. A fifth uses Ransom, SEI and Autonetics cards. A sixth uses Teletype etched boards, with his own circuits.

Number of Instructions

Generally speaking, beginning com-

puter amateurs hope to use a large number of instructions, from 50 to 100. Those who have gotten fairly well into the construction use no more than between 11 and 34. The one exception is a member who has spent $1,000 and two years on his machine, and has (or has projected) 67 instructions. The average number, counting all those reported, is 44. Leaving out those over 50, the average is 22.

Data-Word and Instruction Lengths

The data-word lengths specified range from 4 to 32 bits, with the average around 12 bits.

The instruction lengths also range from 4 to 32 bits, with an average of about 12 bits also.

Add Speed

The range of add speeds is from 8 μsec to 10 msec, with in-betweens of (1) 24 μsec, (2) 216 μsec, (3) 100-500 μsec, depending on the length of the binary number, (4) 8 μsec for one memory reference, but circuitry will operate in 1 μsec, (5) 30 μsec add speed, 4 msec memory cycle time with a magnetostrictive delay line, (6) 20 μsec with one number in accumulator, 25 μsec with both numbers in memory, (7) 32 μsec per pair of decimal digits, (8) 1 to 10 msec.

Number of Registers

The range of number of registers is from 2 to 11, with 3 the most popular. One member has 2 memory, 2 data, 1 op code and 5 address registers.

Special Features

Here are some of the special features reported. Not all of these features have yet been translated into hardware; some are only in the planning stage, or partially breadboarded.

(1) Over 100 Sylvania bulbs in strip sockets will monitor the major registers, etc. CRT displays planned. When completed it will be far more versatile than DEC's PDP8 line.

(2) Data-word length 16-32 bits (32-64 for floating). Planning modular op-code decoders (i.e., basic repertoire plus floating arithmetic, hardware stack operations, etc.). Basic structure is bus-oriented.

(3) Has D/A converted output to drive motor position. Machine has two 8-bit registers, one 15-bit accumulator.

(4) Variable-length instructions, variable-length indirect address fields.

(5) Contents of memory address zero and A register are swapped every cycle (inhibited on some instructions). Therefore one register serves as accumulator and program counter. Memory address 1 serves as index register.

(6) Double precision arithmetic; fixed and floating-point numbers; link on all arithmetic registers; full comparator; AND, OR, Exclusive OR registers for logical computations; data bus allows bi-directional transfer between any two registers.

(7) Will use IBM 1620 software, modified to use USASCII code and to get around unimplemented instructions.

Cost

As to "Cost so far," the range is from 0 to $1500, with an average (among those reporting a cost) of $650.

For "Estimated cost when complete,"

the range is from $300 to "over $10,000." with an average of $2,100. Without that "over $10,000" estimate, the average is $1,100.

Wiring

The large majority, over 80 percent, use fixed wiring.

How Long Working On It?

The range of time spent so far ranges from "one month on the present model" to 4 years, with an average of 2 years.

Size

Here are some present sizes: 3-foot relay rack; 6' x 7' x 18"; 35" x 25" x 20"; 1 work bench; 1 board complete; 30" x 36" x 40"; three 19" five-foot racks; 38" x 60" x 12" & TTY. The "Estimated size when complete" is usually just the same.

Education

Most of those responding have at least one technical degree, including BSEE, MEE, BA in Math, PhD EE, "BA and BS and working on MS," and several students.

Because the great majority of those sending in the survey have technical degrees, and because those who sent it in are among those who have advanced the most with their computers, it seems that lack of a technical education is holding back many ACS members from pushing ahead with their machines, or perhaps from just getting started. Unlike amateur radio, there just isn't enough circuit-level information available on how to build computers.

Other Information

(1) Presently supervising 5 Explorer scouts who are doing much of the construction work, such as building PC cards. I became an Explorer advisor at my company's post to get more hands on the project and to force me to get on the ball and make some progress.... I am going to debug the power supply transients and add a line filter. RTL has low noise immunity and my first wired-up register is dropping and gaining extra bits.

(2) Wish disks and line printers were cheaper! Fortunately, I can build my own software -- assembler, compiler (FORTRAN and/or ALGOL) and operating system.

(3) Teletype controller and memory operational. Can presently transfer data from TTY to register to memory and back. Delay-line memory stability problems solved -- successfully retrieved data after eight hours. Using 8½" x 17" Vectorboard with AA pattern, strengthened by chrome-plated angle. Dual Inlines mounted by alternately bending pin pairs inward and outward. Wiring directly soldered to ICs, using #22 wire with high-temperature-resistant insulation.

(4) This has been an evolutionary process without a fixed idea of exactly what the final product would be. Now I have outrun myself in some ways. For example, I know how to get back and forth from memory to TTY. Also, how to add binary numbers. I don't know how to turn TTY characters into binary numbers in any simple manner. I would appreciate any clues you might have on the subject. (ANY MEMBERS ABLE TO HELP HIM ON THIS?)

Interested in Computers Since...

Those who put down a date gave: 1951, 1955, 1957, 1965. Those who put down an age gave: 13, 14, 15, 18, 20, 21. Those who gave the number of years gave 3, 3, 9 and 17 years.

COMPLETED COMPUTERS

Only two ACS members have reported being anywhere near completing their computers:

ECHO-4

Jim Sutherland's ECHO-4 computer, reported briefly in ACS Newsletter 6, is 7 feet long, 1½ feet deep and 6 feet high. It took Jim a year to build it and will take 10 years to program. He says the CPU is complete, but the input/output system is still growing.

ECHO-4 uses 2N404 transistors and RTL NOR logic elements. The NOR gates were used in process control systems built by Westinghouse about 8 to 10 years ago and were declared scrap. They are mounted on etched circuit boards with 35-pin Elco connectors. A total of 120 boards were used in the entire system (input/output control, arithmetic units) but only 16 types of boards were used, so spare boards do not take up much room.

The memory unit, an Ampex 4096-RQ-30A, came from an obsolete process control computer. Memory cycle is 6 usec, but since the NORs require from 1 to 3 usec to switch, the add time suffers (add speed is 216 μsec).

Between instruction accesses, the memory is available as a refreshing buffer for a CRT display, which is planned but not built yet.

Jim says a story about ECHO-4 is tentatively scheduled for the April 1968 issue of Popular Mechanics. He says it doesn't go into much construction detail, "but the pictures should be interesting."

ECHO-4 has 4 flip-flop registers, and three (P, A and X) in core memory. There are 8,192 words in core memory, each 15 bits long. Clock speed is 160 Kc. There are 18 instructions, 4 bits long.

Special features: one's complement adder with end-around carry. Overflow and carry designators are stored in upper two bits of Program counter (location 0 of core memory). Interrupt automatically stores P and takes next instruction from specified SAVE routine entry. Using 15-pps sync derived from real-time clock. One index register, and also indirect addressing, can be specified by setting flags in the instruction word.

Input: alphanumeric keyboard, six control keyboards, 8-channel paper tape reader, 15 interrupts, 75 contact closures.

Output: Kleinschmidt printer, 60 contact closures, 8-channel paper tape punch, 4 digital clocks.

Interconnections are wire-wrapped.

By the way, ECHO stands for Electronic Computing Home Operator.

EL-65

Hans Ellenberger, who lives in Switzerland, worked a year on his computer and finished it in 1965. A small desk-top machine, looking a little like a Wang calculator with a separate keyboard, EL-65 has a keyboard input and Nixie-tube readout. Size is 40 by 40 by 20 centimeters.

A serial-type computer, EL-65 has 3 registers, 30 words in flip-flop memory, and 15 instructions. The transistors are AC122 (AF pnp germanium) "because of price."

Addition and subtraction times are 1/50 second. The longest multiplication and division times require 1.3 seconds. In addition to these four basic functions, EL-65 can also perform negative multiplica-

tion, and accumulate products.

The cost of materials alone was 1500 Swiss francs, which is about $345. Hans tried to market his computer, calling it "der erste Schweizer Pult-Elektronenrechner," meaning the first Swiss desk-top electronic calculator. But the sales price of 6000 SF ($1380) seems to have put it beyond the means of most Swiss and also it may have been too much of a novelty on the market. As Hans notes, "It seems almost impossible for an amateur to build a computer that can compete with commercial machines. (The amateur who can do that would be, before long, employed by a computer company.)"

Hans is working on a new model, with 16 registers, using Philips LTC cores, and ICs by Fairchild (RTL epoxy), TI and Philips.

MAGAZINE ARTICLES

Low-Cost Counters

The February Popular Electronics contains a construction article (pp 27-32) on a decimal counter with readout, which the magazine believes to be a price breakthrough, as the decade costs only $12, complete with counter, drivers and ten lamps. Parts are available from a Texas company at $12 a decade, including a PC board. A power-supply schematic is given. The maximum rate is 10 Mc, although the unit has been used up to 18 Mc.

Later issues will feature items based on the counter: an "Electronic Stop Watch," which is an EPUT (events per unit time) counter; a digital voltmeter; digital multimeter; and a frequency counter.

The ICs used are all Motorola: two MC790P dual JK flip-flops, and one each of the MC724P (quad, two-input) and MC715P (dual, three-input) NAND/NOR gates. And seven transistors.

An interesting coincidence is the appearance by the same author of an Electronics article (Jan. 22, pp 74-76), "For low cost, count on RTL," which compares the $12 decade with a $10 digital display that uses a milliameter with a special scale, calibrated from 0 to 9, and a biquinary 1-2-2-4 code.

The authors says in his last paragraph that the in-line counter is superior in readability, but the meter design is cheaper and smaller.

Basic Digital IC Circuits

Over a dozen simple digital circuits are given in "30 Basic IC Projects," in Radio-Electronics (Jan. 1968, pp 50-53). This second part of a two-part article uses the Fairchild µL914 as the basis for inverters, pulse-enabling and disabling gates, NOR/NAND and OR/AND gates, square-wave generators, one-shot, Schmitt trigger, flip-flop, and others. All that's needed is a 914 and a few resistors and capacitors, plus diodes for the generator.

The article on the following pages (pp 54, 55, 62) describes how to "Build a Low-Cost IC Signal Generator," with the same µL914, to provide square waves from 5 cps to 50 Kc.

The first part of the IC article appeared in the December 1967 issue (pp 43-45), and covered the basic description of the µL914, giving circuits for linear applications such as emitter followers and amplifiers.

Wireless World Digital Computer

The four-part article on building a small computer, described in the

The Amateur Computer Society is open to all who are interested in building and operating a digital computer that can at least perform automatic multiplication and division, or is of a comparable complexity.

For membership in the ACS, and a subscription of at least eight issues of the Newsletter, send $3 (or a check) to:

Stephen B. Gray
Amateur Computer Society
260 Noroton Avenue
Darien, Conn. 06820

The Newsletter will appear about every eight weeks.

previous Newsletter, has a fifth part now, completing the series. The December Wireless World (pp 601-605) covers the operation of the machine, with coding examples.

Using Miniature Relays?

An interesting comparison of major characteristics of miniature relays appeared in a new-product item in the January 8 Electronics (pp 171-172). Comparisons are made between crystal-case relays, mercury-wetted and dry reed relays, and solid-state switching devices. Each of the four types is said to provide certain advantages. "If speed is needed more than isolation, solid-state switches should be used. When cost is the prime factor and high isolation is also required, the reed relay is the best choice." The new product is a line of dry reed relays, made by Hi-G Inc. (Windsor Locks, Conn.) which sell for about $2, compared with about $8 for solid-state switches.

Would you believe a relay in a TO-5 transistor can? They're described in the January EEE (pp 20 & 24). Not cheap, though; over $20.

BREADBOARDING INTEGRATED CIRCUITS

Wade White says he breadboards in-line ICs with a board that holds 15 of the 14-pin packs, from J.R. Anderson Enterprises, Inc. 3691 Lee Road, Cleveland, Ohio 44120. The board, type MC-1, costs $4.85 for 1-9, $4.50 for 10-24, and $4.25 for 25-49.

No holes are drilled in the board. The components are soldered to the top, for easy removal or change. Size is 3/32" x 8-5/8" x 5-49/64".

For permanent mounting of 12 of the 14- or 16-pin ICs, Wade uses an M-96003-PG board from Dyna Sales Co., 962½ S. Atlantic Blvd., Los Angeles, Calif. 90022. Phone (213) 268-1175, ask for Milt Hollingsworth.

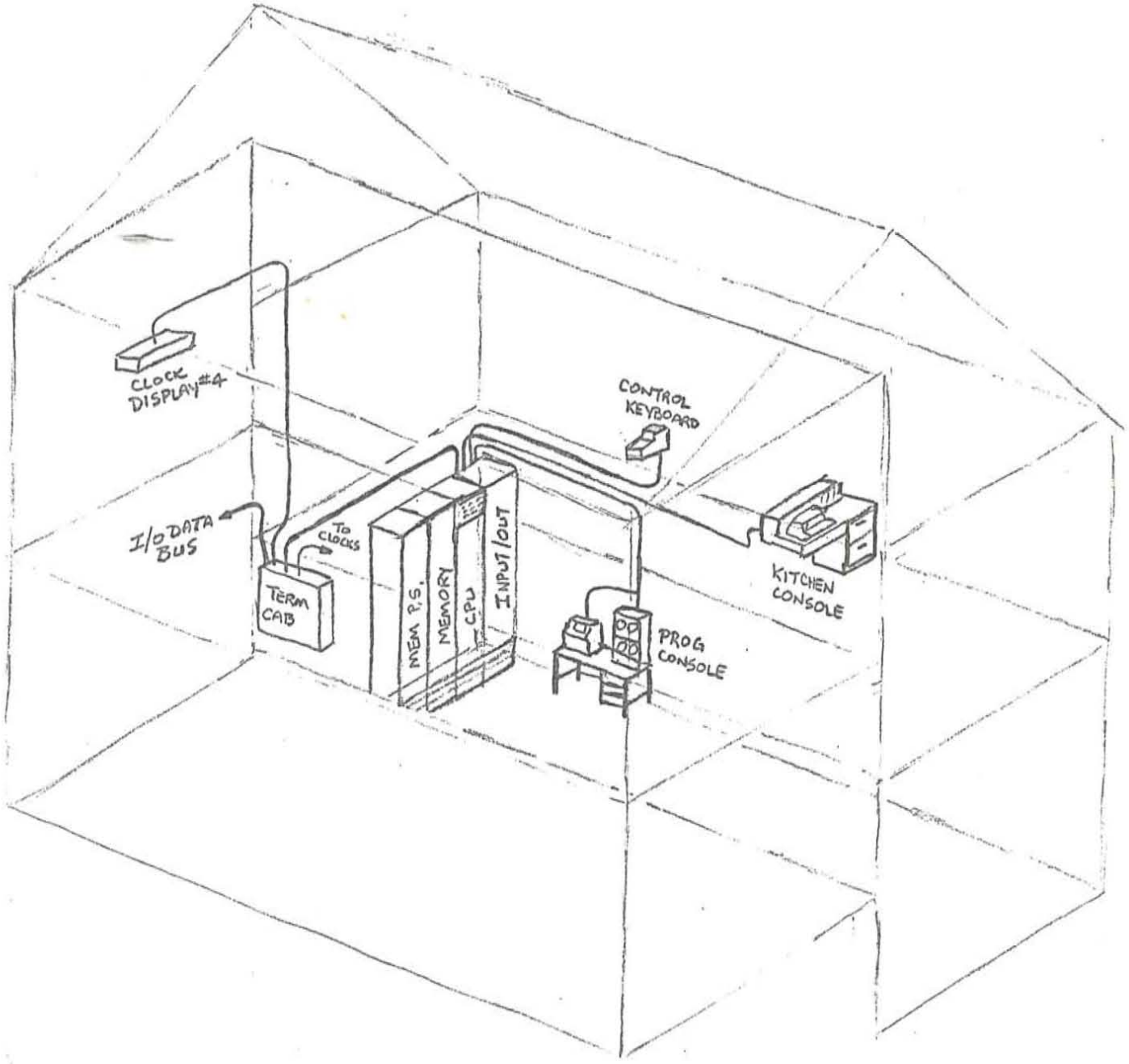
For TO-5 and flat-pack ICs, use board M-96002-PG. The boards have holes drilled for mounting components, and pins to fit a 22-contact connector (Amphenol series 143). The connector costs about $1.55 new, but can be bought surplus for much less.

Price for either board is $6.95, with a discount of 5% for 5-14, 10% for 15 or more.

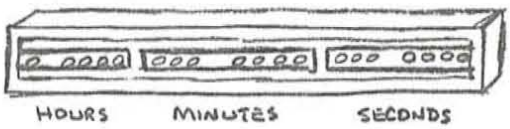
Wade also notes that the Vero IC board kit listed in Newsletter 7 at $40, is available from Dyna Sales for $29.95, as item MC-10.

NEXT ISSUE

If any of you who have gotten into the construction of your machines fairly well would like to write up your experiences for the Newsletter, several pages are available for the gory details. Tell us all about your problems, solutions, discoveries, failures, components, and your future plans.



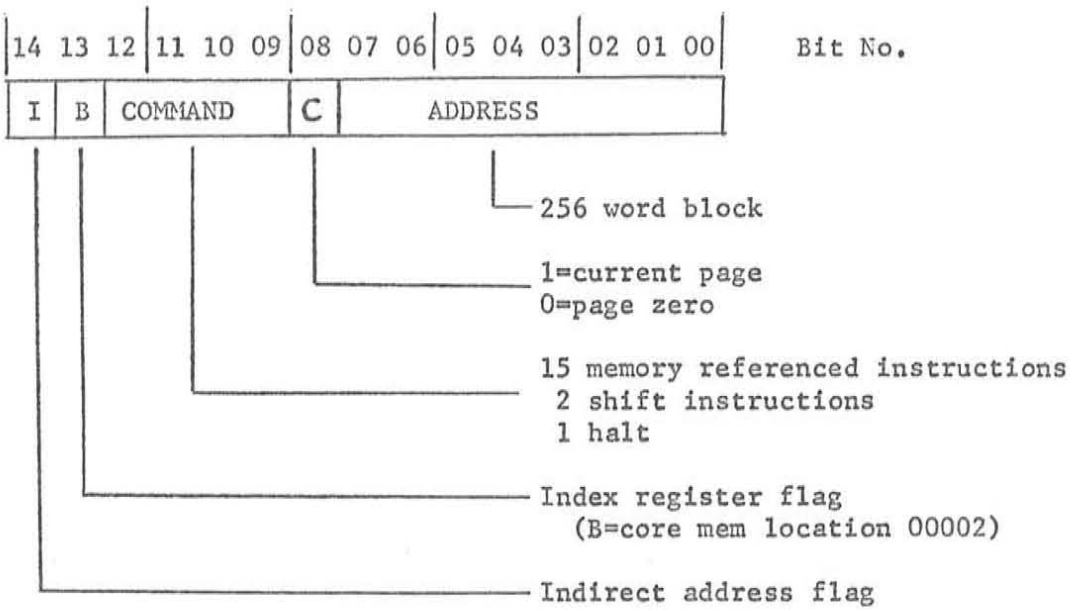
ECHO IV SYSTEM DIAGRAM



DIGITAL CLOCK DISPLAY

J.S. 2-14-71

ECHO IV INSTRUCTION FORMAT



ASSIGNED CORE MEMORY LOCATIONS

00000 = P = Program Counter
00001 = Zero constant loc
00002 = B = Index Register
00003 = A = Accumulator
00004 = Interrupted program return
00005 = First instruction of Interrupt Executive

Bit 14 of Program Counter is Endaround Carry (E) designator
The E designator is set if carry out of adder bit 14 occurs during ADD. The E designator is cleared otherwise near end of ADD instruction execution.

The overflow designator (OV) is set if:
1. Bit 00 of accumulator equalled 1 before right shift
2. Sign of sum is different from sign of like-signed terms

Address modification occurs in the following order:

Indirect address is fetched BEFORE content of Index Register is added

COMMAND DEFINITIONS

Code	Mnemonic	Definition
01	JMP	Jump to Y + 1
02	JOV	Jump to Y + 1 if OV = 1
03	COM	Complement contents of Y
04	DCS	Decrement contents of Y and skip next instruction if contents of Y = minus one after decrement
05	SIP	Store incremented P in Y
06	ENB	Enter B with contents of Y
07	ENA	Enter A with contents of Y
10	OUT	Output from A to channel address
11	INP	Input to A from channel address
12	JAN	Jump to Y + 1 if bit 14 of A = 1
13	JAZ	Jump to Y + 1 if A = positive zero
14	STA	Store A in Y
15	ADD	Add contents of Y to A
16	EOR	Exclusive OR contents of Y with A
17	AND	And contents of Y with A
00000	HLT	Halt
40000	LSH	Left shift A, Bit 14 replaces bit 00
00400	RSH	Right shift A, Bit 00 enters OV designator

INPUT CHANNEL ASSIGNMENTS

Channel number is defined by bits 00 through 05 of effective address

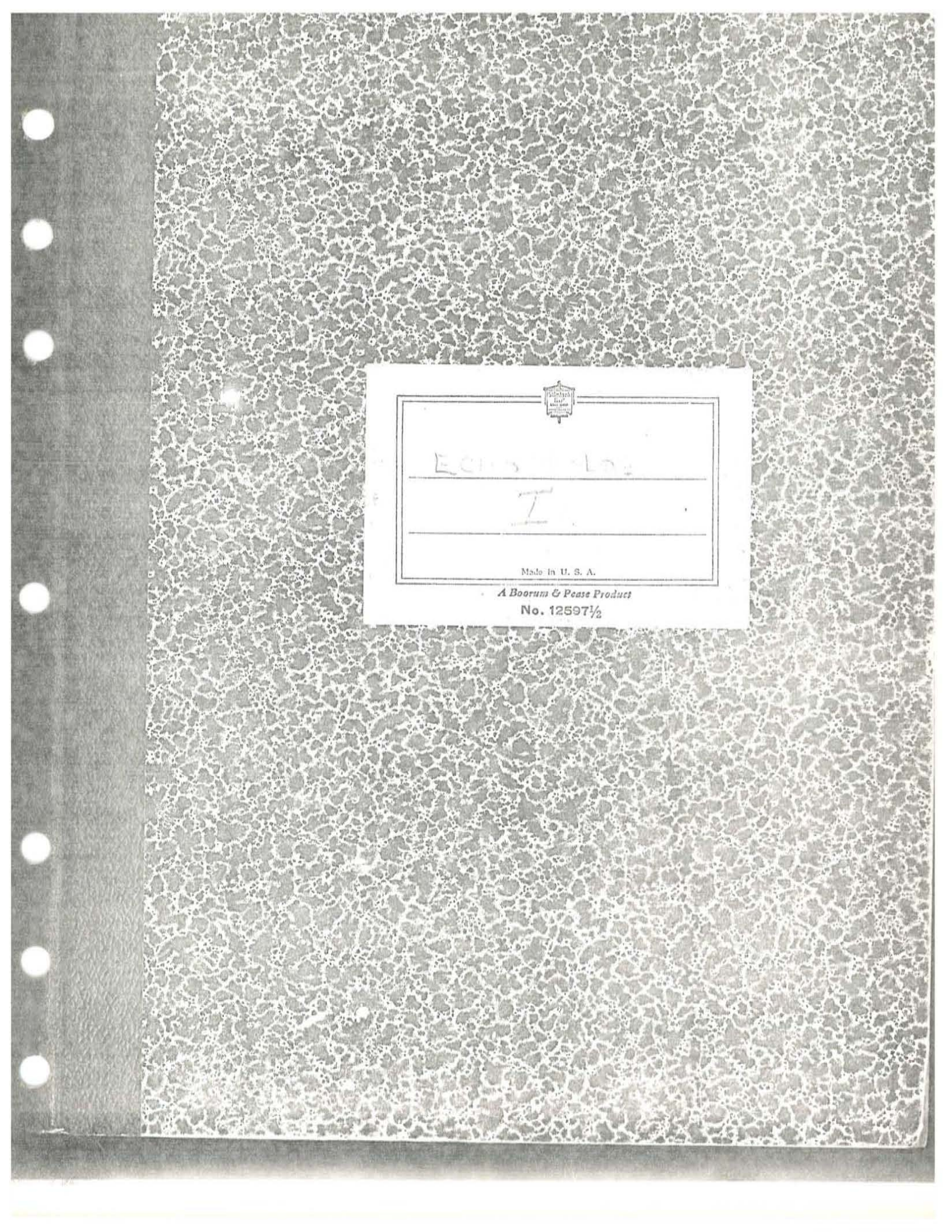
Channel No.	Function
00	Interrupt word, 15 bits including SYNC
10	House trunk on low order 6 bits, Kitchen keyboard on high order 8 bits
20	Real-time clock, minutes and seconds in BCD
30	Contact-closure inputs
40	Magnetic tape storage unit (future)
50	Paper tape reader
60	unassigned
70	unassigned

OUTPUT CHANNEL ASSIGNMENTS

00	Programmer's printer/punch on low order 6 bits
10	House trunk DATA character on low order 6 bits
20	unassigned
30	Contact-closures,,31 to 35 designate 5 words, 15 bits/word
40	House trunk ADDR selector on low order 6 bits
50	Magnetic tape storage unit
60	Kitchen console printer on low order 8 bits
70	unassigned

ECHO-IV Logbook Summary

Date	Problem	Solution
Aug 1966	Machine stopped occasionally due to power line transient spikes from fluorescent lamp in bathroom.	Installed power line filter on ECHO-IV
Mar 1967	Burned out two print coils on printer print solenoids	Rewound the coils
Apr 1967	"Programs fairly well goofed up, Jay (2 yrs old) had been playing with keyboard".	Talk with Jay
Apr 1967	Need variable speed clock to check operational margins.	Adjustable clock speed feature added
Aug 1967	Temperature variations in basement causing amnesia in core memory.	Keep doors to garage closed
Oct 1967	Machine turned itself on and did not shut down.	Run machine for three minutes each hour to reach stability
Nov 1967	Rapped all card handles and found two intermittent cards	Replaced with spares
Dec 1967	Found loose wire termination on memory power supply contactor.	Recrimped wire and tightened termination screw
Jan 1968	Found that the interrupt executive routine was getting interrupted.	Corrected logic
Oct 1968	Cold temperatures affecting machine	Added heaters to memory cabinet, left logic power on continuously, added blower to power supply cabinet
Nov 1968	Memory power supply contactors failing after two years of operation of once per hour.	Added thyristor power control
Dec 1968	Intermittent fuse holder in the memory drive chassis	Replaced fuse holder
Jan 1969	Jay left garage door open, memory messed up.	Ducted warm air from cabinet 4 to cabinets 2 and 3


I
Made in U. S. A.
A Boorum & Pease Product
No. 12597½

4/14/66 INHIBIT = 29V DRIVE = 35.5V

Instructions verified: ENA, ENB, STA, DCS, JMP, E⌀R, LSH, RSH, HLT JAZ,

Yet to be verified: AND, ADD, JAN, OUT, INP, ~~ESE~~ SIP, COM, JSV

4/15/66 Machine runs from cold start
INHIBIT = 29V (setting 349)
DRIVE = 37V (setting 608)

4/16/66 E & ⌀ fixed and verified

4/17/66 ON AT 1230hrs 1310 Stop loc 10700 dropped Bit 10

4/24/66 Loc 5172 dropped bit 14

5/29 INH = 3.5 setting DRIVE = 6.5 setting

5/31 Bit 8 not being read back to ZR in ENA LOCKED
CHANGED XGF IN Loc 1H and trouble disappeared.
other possible causes: 1G, 1E, 1F, 4C
Failed again, 1G Replaced, still Failed, 4C replaced, trouble disappeared when restarted after 15 minute cool off
Changed power control panel so that the P relay NO contact is usually closed to enable the Memory START circuit when Switched Neutral is applied. This way, only 1 CCO IS needed to make the system seal in and run.

6/1 INTERRUPT f-f gnded at SH13 with Jumper wire

6/7 Bit 4 seems to come on if another bit on trunk is a one

6/2 HLT stored in loc 15, 16, 17 of core test

6/4 Found open 1K resistor on XDA card in slot 6C output #13 temporarily replaced with 1K ww ohmite

XGB in Loc 4C which was replaced on 5/31 was put back into system, RUNS OK

with 77776 test pattern, system is sensitive to -5% on +4V in core memory

6/9 delay added to closing the UAS, UTR, UZR, STARTS OK

6/10 +4V margin switch in -5% position causes Bit 0 of Location 7667 be dropped.

6/12 within 5 minutes after START, 00000 pattern, Core test picked up a one in Bit 4 (20_8) and stopped at HLT in 21.

INCREASED INHIBIT SETTING TO 5.0 Line Volt = 115

6/13 Core test changed so that 00000 and 77777 are the two test pattern

Core cleaned and JMP 0 loaded into loc 1

6/14 Picked up bit 4 and Test stopped after about 5 Minutes

Changed all load gates to Z register, and bit 4 still picks up in the locked ENA mode.

Changed the XGF in loc 1G and trouble went away. 1H could also cause trouble. Replaced the original card into 1G and restarted the test.

BIT 9 coming on intermittently IN ZR when running in locked ENA

6/29/66 LOADED NEW COMBINED CORE TEST
ADD FILTERS TO INPUT DATA LINES

7/2/66 GDH at 4M had open NOR (- all the time) at Term 29
This prevented loading of IR

7/7/66 Bit 14 either dropped or added

7/9/66 ADD, JOV, OUT, INP CHECKED OUT OK COM inst previously checked OK

Power Supply moved up 8 3/4 inches and recommended, All OK

8/12/66 checked trunk to workbench timing of load pulses and data on the output data lines.

1. Bit 5 of X reg is cleared during INP and therefore the output driver pulls the line negative. This prevents the inputting of a Zero into bit 5. Solution: set bit 5 of X reg to "1" during early portion of E sequence during INP.

2. Noticed that machine is sensitive to inductive spike when bench lamp turned OFF. Causes machine to stop.

3. Input data gates on input chan 1 (TRUNK) for bits 6-14 should be driven with -12 Volts to insure that input character will be right Justified and bits 6-14 cleared.

8/13/66

Added +12 to unused inputs on Chan 1
Added CLEAR XR3 at time S2 during IJP instruct
Wired RC noise suppressor across workbench power switch
R = 5Ω C = 1 μf

(−) 37 Volt power supply in memory still sags to −30 volts when first turned on after having been off for more than 24 hours. Trouble not due to excessive current (≈ 12 Amps) must be a leaky electrolytic capacitor which must reform each time power is restored after long period of inactivity.

Looks like it would be a good trade to replace ESC with SIP (Store Incremented PC). This would simplify the return jump function.

1G

9/10/66 Changed logic to make SIP inst.
Corrected OV logic
Bit 5 intermittently going on and off during locked ENA
(Memory voltage up to Normal)

Trouble with Bit 5 due to defective RA-L card in memory DIGIT PLANE PACK slot A09 (Z). This card was swapped with B09 to move defective bit to bit 0 of high address (above 7777_8)

Memory test located at $110 - 165_8$ runs OK if size in location 132 and 165 is set to 7577_8

9/13/66 CORE TEST — BIT 4 of loc 3172_8 was dropped !!!!
+4V Margin switch on Mem P.S. was raised to +5% and trouble disappeared.

9/15/66 CORE TEST with +4V margin set 5% LOW

RA-L CARD IN		LOC FAILED		BIT FAILED	detection section
489	IN B09	7660		0 dropped	Z
489	IN B09	6677		0 dropped	Z
489	B08	17272		2 dropped	Z
489	B08	17272		2 dropped	Z
132	B08	7475		0 dropped	
"	"	12172		2 dropped	Z
364	"	17777	(solid failure)	2 dropped	Z

B09 replaced by 132, B08 put in B08

With +4V Margin switch set AT NORM, CORE TEST RUNS OK

9/16/66 Loc 7575 bit 14 dropped (B09H suspect)

9/19/66 corrected wiring in OV set circuit, Bootstrap runs ok Now
Core test loaded to run test between 00200_8 and 17377_8

9/22/66 INDIRECT JMP CAN'T BE EXECUTED PROPERLY IN UPPER BAY OF CORE. P is set to 00000
DIRECT JMP IS OK IN UPPER BAY
BOTH TYPES OF JUMPS OK IN LOWER BAY

Trouble was fixed by separating the LZR and LTR during I sequence into 2 times! TR12 was being cleared during LTR which changed LDA and LDB signals during transfer.

10/15/66 Worked on Printer. Bit 4 comes on when executing Locked ENA

11/3/66 Bit 10 dropped in Prog. counter occasionally
also Bit 8 dropped at same time Bit 7 picked up.

11/16/66 Bit 10 dropped occasionally RA-L CARD located in slot B09 (NO serial NO.) was replaced by Serial NO 510
Machine starts automatically OK.

11/21/66 JAN ~~Always doesn't~~ Jmp on NEG $\overline{XR14}$ was missing from IR17 pin
OK NOW

12/29/66 BIT 10 dropped steadily when in locked ENA
MDR DOOR OPENED AND TROUBLE WENT AWAY
CARD # A12 contacts cleaned with eraser and replaced.

1/1/67 Bit 8 seemed to drop BIT 7 seemed to be picked up.
Bit 11 drops when cold

1/2/67 Trouble with Bit 11 traced to XGG in slot IF #19 (output #3)
Replaced with spare XGG. RUNS OK NOW

1/7/67 STOPPED WITH 17200 IN P, 17402 IN Loc 1
Bit 7 could be dropped from JMP 17377
↕
17177

WORST CASE CORE TEST

$$WP = A_7 A_1 \bar{A}_0 + A_7 \bar{A}_1 A_0 + \bar{A}_7 \bar{A}_1 \bar{A}_0 + \bar{A}_7 A_1 A_0$$

202 201 0 3

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 MASK = 00203

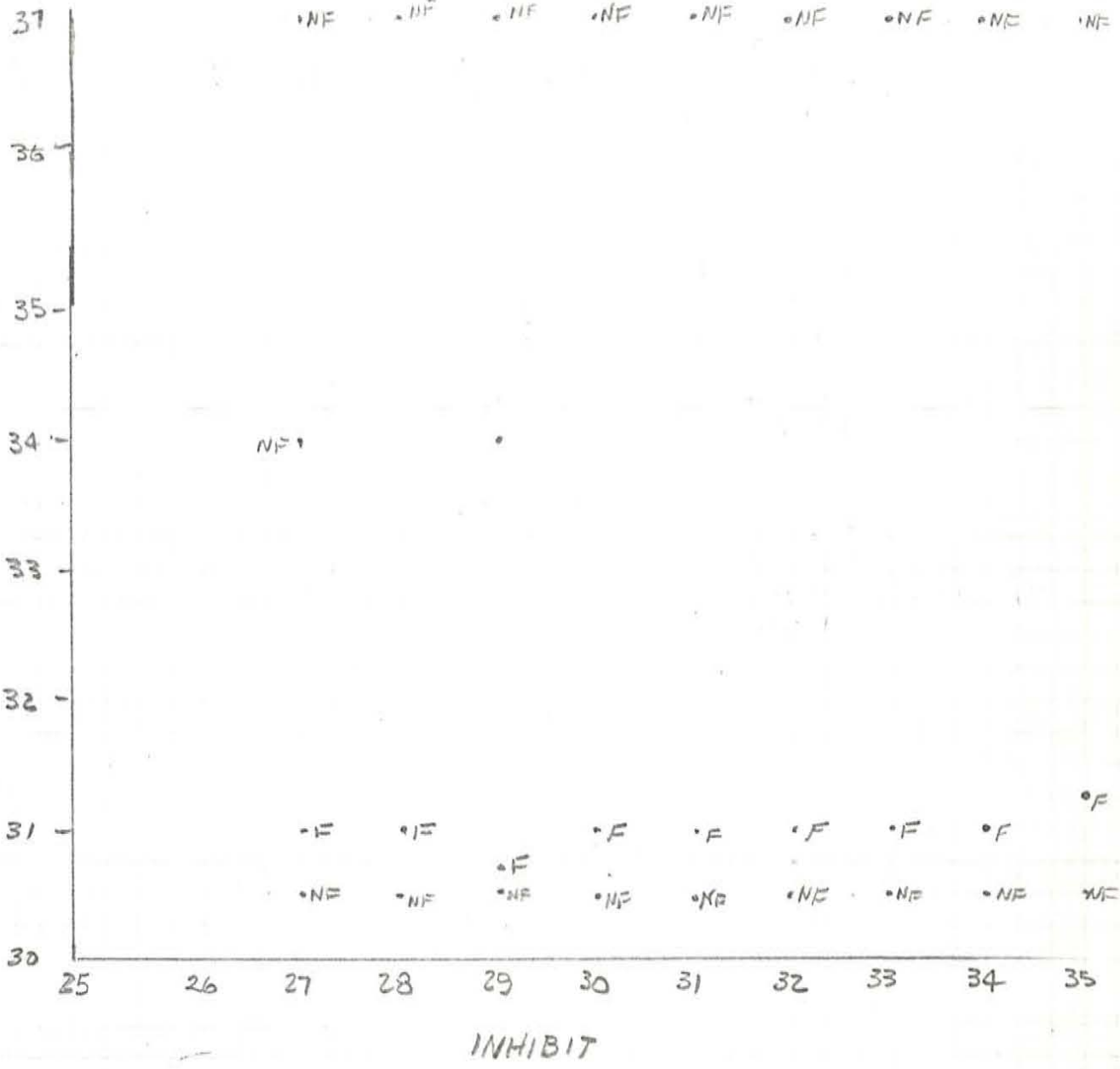
```
WRITE ---> ENA  SIZE          17401    7431
           STA  B                 2    14002
RET  ----> JMP  PATCH             3    14416
           AND  MASK              4    17432
           STA  ADDR              5    14441
           EOR  TEST1             6    16433
           JAZ  ONES              7    13425
           ENA  ADDR             10    07441
           EOR  TEST2             1    16434
           JAZ  ONES              2    13425
           ENA  ADDR              3    07441
           EOR  TEST3             4    16435
           JAZ  ONES              5    13425
           ENA  ADDR              6    07441
           EOR  TEST4             7    16436
           JAZ  ONES             20    13425
           ENA  ZERO              1    07440
           STA  i,5,B             2    74445
END  ----> DCS  B                 3    04002
           JMP  RET               4    14002
           HLT                    5    00000
ONES ----> ENA  ONES              6    07437
           STA  i,10,B            7    74445
           JMP  END              30    14222

           SIZE      17367        1
           MASK        203        2
           TEST1       202        3
           TEST2       201        4
           TEST3         0        5
           TEST4         3        6
           ONES      77777        7
           ZEROS         0       40
           ADDR      (   )        1
PATCH      ENA  B                 2    07002
           ADD  con10             3    15445
           JMP  403               4    14403
                                 10    5
```

RELOCATION OF CORE PROGRAM

INPUT PARAMETERS, SIZE OF BLOCK
FIRST PRESENT LOC = FPL
FIRST NEW LOC = FNL

BEG 17764	ENB SIZE	6772
5	ENA L,B FPL	67773
6	STA L,B FNL	74774
7	DCS B	4002
17770	JMP BEG	17764
1	JMP KB INPUT PROG	41775
17772	SIZE	
17773	FPL	
17774	FNL	
5	KB INPUT	17377
17776	00531	
7	77377	



INITIALLY, $V_D = 34.0$ $V_I = 29$

1/17/67 RA-L CARD IN MEM DPA slot 9 was replaced and bit 4 no longer picked up.

1/18/67 Stopped with bit 11 dropped and P = 13400 instead of 17400

Bit 11 dropped in P P = 13400 instead of 17400

1/20/67 Plated fingers of ID-A And top half of RA-L cards in digit plane Pack (DP) of memory were cleaned with eraser, in attempt to clear up the dropping of bits 7 & 9 during JMPi from 17546

1/21/67 Swapped bits 7&8 for 5&6 in high bank of own RA-L cards

Replaced XGB IN Loc 4C (Unload gate in AD)

STOPED AS BEFORE

Prog relocated so that the initial loop is at 7000 instead of 17000

1/22/67 Autostart at 1:00 OK
2:00 False start Pleft equal to 7301
7377
7277 bit 6 dropped

Stopped with P = 7200
377 became 177
bit 7 dropped

3:00 OK

4:00 stopped P = 7370 bit 2 is dropped
Also bit 2 is dropped in upper half

Load Z gate in slot 2F changed out

Loc 7547 = Stop for 59 Minute restart
17547 = Stop

1/23/67 loaded Turn off prog at 17600
Stops at 1563 (almost as soon as startup)

1/27/67 Relay K3 in Memory Seq rebuilt so that NC contacts are OK to allow START

Set for Turn on at 30 minutes
" " Turnoff at 31 minutes

2/12/67 stopped at 153_8

2/12/67 stopped at 1563_8 loc1 = 17403

2/17/67 Stopped at 1563_8 Loc1 = 17601

stopped at 1563 Loc1 = 17401

2/21/67 Stopped 10412 A = 00020 (Bit 4)

HLT 23 loc1 = 10541

2/26/67 Stopped 13400 Loc1 = 467
A = 0

stops at 411 ov=1.

bit 9 on in A

When turned on at MC, Bit 1 of trunk follows bit 7 of T reg. (FIXED ON 3/16)

When restarted, P= 37752 or 37772 instead of 17552

Note that when loc 10000 contains 77777 then the P can pick up ones, it seems that the register selection is not initialized on startup and if 10000 ≠ 0 then Reg B is adding noise to data bus

2/27/67 stopped

1) P= 1445 with E≠0=1 A = 12524

2) stopped P= 1411 A = 1000 (BIT 9)

3 stopped 413 A = 777

2/23 Stopped P= 10411 A= 10150

3/8 Stopped P= 10411 A= 1000 (BIT9)

3/9 Stopped P= 10421 A= 00077 OV=1 (FIXED 3/10)

3/10 " P= 403 A= 200 (BIT7)

" 00421 A= 00077 OV=1 (FIXED 3/10)

" 17354 A= 77777 OV=1

DRIVE SET TO 35V

3/12 STOPPED P=7312? A= 77776 OV=1

" 403 A= 200 (BIT 7)

403 A= 200 BIT 7

411

DCS 3 decrementing P instead of Loc 3

3/16 lamp TR bit 1 — T REG Bit 7 crosstalk traced to maintenance panel wiring was punched through and tying 100K resistor mixer. Probably not the cause of random troubles.

STOP OV=1 P=411 A=20 (BIT4) " (fixed 3/17)

OV=1 P=421 A=77

Bit 6 was not being complemented, XGF card in loc 2G was replaced. Prog runs OK now.

STOPPED OV=1 P=10411 A=20 (BIT4) (fixed 3/17)

MACH. WILL STILL NOT START CORRECTLY IF LOC 10000 = 77777

3/17 STOP OV=1 P=10411 A=20 BIT (4) (Fixed 3/17)

Bit 4 was bad on Right shift Gate from Adder → trunk card replaced (XGB in slot 4E)

ENA WAS NOT BEING LOADED PROPERLY

ENA 474 brings 400_8 into Accum instead of pattern which is stored at 474

ENA E SEQ TR seems to be getting cleared in 0 or 1 STEP AND THEREFORE 474 is lost

loc 6G (2EB) driver was rewired so that signals E, SS1 S3 S5 are solid and not marginal.

3/18 STOP P=10411 A = 10150 OV = 1 COMPARE WITH 12525
SYNC disable but keep arm
ENA SEEMS TO BE ENTERING A with C(P) instead of with operand.

3/20

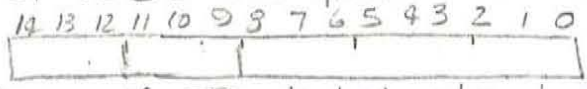
STOP	P= 7324	OV=1	A=0
"	1411	1	10150
"	1421	1	10147
"	1426	1	7353

3/21 1. DRIVE VOLTAGE INCREASED TO 36V
2. MEM TRIG DISABLED WITH GND JMPR To Prevent extra memory cycles

TYPER DRIVE CIRCUITS MODIFIED TO GIVE INDIVIDUAL dropping resistors in the 5 coils

3/22 The CLR TR driver control (4K) XGD was replaced. to prevent the TR From being cleared before the instruction is executed.

SYMPTOM OF JMPING To 1563 when indirect address of 7563 was given



This could happen if TR is being cleared during F seq.
∴ 4K module probably ok. so 4K put back.

MODULE 7J Replaced, but same symptom as above

Modules in 5T, 5S removed, and contacts were spread. long nose pliers reset the contacts.

Rest of CAGE 5 was reset, prog still stopped
CAGES 4, 6, & 7 were reset

3/23 STOPPED AT P= 426 OV=1 about 5 sec after start.

STOP P= 403 A = 200

SCOPE HOOKED TO CLR TR (5P12) MACH TURNED OFF

FOUND PSN SOLDERED CONN. ON 5T28 WHICH poor joint.

3/23

STOP A = 00004 P = 1411 OV = 1
(SAME ERROR AS THE ONE IN BOOTSTRAP
WHERE 1⊕1 GAVE A 1 INSTEAD OF 0)

STOP A = 10150 P = 1411 OV = 1

STOP A = 10,150 P = 1411 OV = 1

Bit 2 in high bank is being dropped
Bit is OK in Low bank ∴ Memory is at fault

3/24 STOP A = 10147 P = 1421
A = 0 P = 13461 OV = 1
STOP +15sec A = 77776 P = 10426 OV = 1
STOP 5 secs A = 10147 P = 10421 OV = 1
3 secs A = 57353 P = 426 OV = 1
A = 10147 P = 10421 OV = 1

3/27 SPARE RA-L card was placed in BITS 13 & 14 of HIGH BANK
BITS 2 & 3 in high bank were replaced by previous 13-14
Original Bit 2 & 3 RA-L card (tape marked BB) held in spares

XGC Card in Slot 1E replaced this card unloads high bank MEM BUFFER onto TRUNK LINE

CARDS IN CAGES 2 & 3 were individually inspected and contacts were reset.

3/29/0300 STOP P = 4
STOP again (when restarted) P = 17405 Loc 17405 = 00004
Should be 02406
loc 17405 reloaded to 02406 and test restarted OK

STOP A 10147 P = 421 OV = 1

14	1 0 1 0 1 0 1 0 1 0 1 0 1	
15	0 1 0 1 0 1 0 1 0 1 0 1 0	
16	1 1 1 1 1 1 1 1 1 1 1 1 1	67627
17	0 0 0 0 0 0 0 0 0 0 0 0 0	10150
20	1 1 1 1 1 1 1 1 1 1 1 1 0	10147
21		

```
                0 0 1 0 1 0 1 0 1 0 1 0 1 0 1      CK1
                0 0 1 0 1 0 1 0 1 0 1 0 1 0 1      PAT 2
                0 0 0 0 1 0 1 0 0 1 1 1 1 1 0      02475
ACTUAL          0 0 1 0 0 0 0 0 1 1 0 1 0 0 0

                  X               X X   X
```

LOOKS LIKE BIT 1 IN HIGH BAY IS BEING LOST OCCASIONALLY SO THAT PAT2 (LOC 472) IS NOT BEING USED. INSTEAD LOC 470 is used by EDR at loc 7,

```
74  14          1 0 1 0 1 0 1 0 1 0 1 0 1 0 1      CK1
75  15          0 0 1 0 0 0 0 1 1 1 1 1 1 1 1
                1 0 0 0 1 0 1 1 0 1 0 1 0 1 0
    16          0 0 1 0 0 0 0 1 1 1 1 1 1 1 1      PAT.
    17          1 1 0 1 1 1 1 0 0 0 0 0 0 0 0

                1 1 0 1 1 1.0 1 1.1 1 1 1.1 1 1 /  67377
```

NOT CONCLUSIVE

3/31/1300	STOP	P= 10421	A= 10147	
4/1/0230	STOP	P= 27324	A= 0	OV=1
4/1/1200	STOP	P= 27361	A= 15646,	OV=1
1300	STOP	P= 27324	A= 0	OV=1
		P= 403	A= 200	

Machine stopped in DCS instruction as before. The BAD NOR on 5728 was replaced. This is same problem as before on 3/23

4/2/7 STOP P= 4 Loc 1 = 17557 MACH RUN / MAINT

When restarted, machine stopps with P= 17605

STOP P= 14436 A= 14436 OV 1 = 14225

4/2/1600 STOP P= 30440 A= 00004 OVF 1

With restart machine stops with P= 17605

AND should have left all zeros

∴ BIT 2 "AND" circuit is intermittent

All HLT inst in 0400 2d 10400 test were completed to DCS P inst.

STOP P= 17357

3

4/3/1700 STOP A = 7777₈ P = ②7352 OV = 1 loc 1 = 10424
Restarted with phase left out (NO SYNC INT)

4/4/0000 STOP A = 0 P = 16405

Loc 5 has been changed, therefore octal dump prog at 16400 was entered and stopped at 16405 because rSync had been disabled.

Since loc before 16400 contain zeros, program was jumped into with Jmp instruction

4/4/0400 STOP A = 60000 P = 27367 OV = loc 1 = 10403

STOP with P = 17605 when put into Inst. Step, and STARTED at 17577, executes INP inst at 17600 and then goes to P sequence. At end of P Sequence, The X register contains 17604 instead of 17600 trouble is either in unload gate of adder or load gate to XR associated with bit 2

4/6/67 UNLOAD GATE ON AD Resocated in socket (loc 4C)

4/7/67/100 STOP P = 17605 when running in phase step thru program, bit 2 of X reg was initially on during SI - All other stuff then it went off as it should.

Both input track gates on XR were replaced since it wasn't possible to tell which one is at fault. loc 2C & 2D

3

STOP P = 00531

STOP P = 17605 A = 20664

4/7/67 Bit 2 of XR was seen on during P seq of 17600 → 17603
Trouble must be in XR bit 2 flip-flop.

GITH card in Slot 2K replaced to try correcting XR problem above

4/9/67 STOP P = 17400 A = 30470 loc 1 = 0 OV = 0
ZR = 17377

IR = 2 (JOV, i) Mode = AUTO, got chec INT RUN
P SEQ SEL

4/3/67 1500 STOP IN E SEQ. clock not running, but still in AUTO
All phases off suspect GHH card in 7K

Card in slot 7K replaced by suspect card removed from loc where input 23 was intermittently bad. Input 23 is not used in the 7K circuit.

1550 Elements with outputs #10 #17 were replaced and original GHH card inserted into 7K

STOP 4/10/1000 P = 20415 A = 52525 I = 00000

STOP P = 4 A = 00000 I = 00000

4/13/67 Computer programs were fairly well cooled up. JAY had been playing with keyboard.

4/14/2100 STOP P = 27357 A = 10147 OV = 1

STOP P = A = 436 OV = 1
SEQ = A, yet clock is off
IR = 13
ZR = 20440
MACHINE STARTS WHEN START BUTTON PUSHED

STOP SEQ = P Yet clock is off IR = 3

STOP A = 0 P = 4

STOP A = 400 P = 37367

4/16/2100 STOP SEQ = AUTO - E YET CLOCK NOT RUNNING
restarted with START switch

4/17/1900 STOP SEQ = AUTO - E CLOCK OFF
XR = 10534
ZR = 10003 OV = 1
Loc 10570 = 30535
restarted with START switch

TRAP INSTALLED ON THE 3 STOP GATES WHICH SET STOP GATE "ON"

4/19/0900 Wed stop P = 423 A = 12134 L570 = 423

4/20/0000 Thurs stop P = 423 A = 12134 L570 = 423

4/20/0003 Thurs. stop P = 423 A = 5056 L570 = 423
(RESTARTED WITH PROBE OUT)

4/20/0700 STOP P=0 A=01001 (JMP to 2
loc 2 = 00413 (RSH A)
457 = 20456
10457 = 30456

4/20/1800 STOP P=16405 A=0 570 = 20556
10570 30556
Looks like bit 9 dropped from address

4/22/1500 After sync was enabled,
STOP = 10422 (DCSP) A = 2134

10570 = 10423
570 = 20556
1 = 10413

4/22/1600 STOP 10422 A = 2134
10570 = 10423
570 = 20556
1 = 10413

4/22/1700 STOP 10422 A = 12134
1 = 413
10570 = 30556
570 = 423

4/22/1900 STOP 427 A = 12134

10570 30556
570 423
1 = 413

SYNC DISABLED

4/24/0900 MON ST
STOP P = 30512 A = 76001 I

10570 = 30513
570 = 20556
1 = 10377

Restarted OK

4/24/0900 MON
STOP P=4006 A=0

10570 = 30557
570 = 20436 ←
1 = 10377

IF SUSPECTED TROUBLE OF 3/29 occurred on 4/22

```
0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1     CKI
0 0 1 0 0 0 1 0 0 0 0 0 1 1 1 1 0     10417
0 0 0 0 1 0 0 0 1 0 1 1 0 1 0 1 0     result = 2132
```

75651

0Φ1

ΦΦ1'ΦΦΦ'1 1Φ'ΦΦ1'ΦΦ1 10411, 10413, 10451, 10453

SINCE Trouble occurs in both high & Low bays of core, then TR bit 1 seems to be dropping fm operand

If unload cycle fm TR bit 1 is intermittently allowing the trunk to be a (-) level during transfer, then a "0" will be set into ZR during step 6 & 7 of F

4/27/67 STOP P = 24001 A = 400 I = 10377
570 = 412
10570 = 30556

WITH SYNC → STOP P = 00422 A = 12134

570 = 423
10570 = 30556
I = 413

4/27/67/2142 (THURS) .0036 CAP ADDED TO CLOCK TO SLOW MACHINE DOWN TO ABOUT HALF NORMAL SPEED

STOP P = 00004 A = 52524

570 = 20426
10570 = 30556
I = 10435

SYNC ENABLED ↓

4/29/1700 SAT New 3-speed Clock board added to loc 7R
high 65 μsec/SEQ
NORM 80
LOW = 160

5/2/1100 TUES STOP P = 20440 A = 441
C(P+1) = DCS 3
570 = 20441
10570 = 30556
I = 10457

SINCE AUTO was set
CLOCK RUNNING

SYMPTOM: DCS 3 was interpreted DCS 0

5/3/0100 Wed STOP DCS P

P= 40423 A= 1410

570= 20423
10570= 30556
1= 10433

CLOCK SET TO LOW SPEED AND RESTARTED AT 17552

STOP 5/5/67 FRI STOP P= 33 A= 32

SYNC enabled and restarted

17777 = 75475 instead of 77377

5/5/67 STOP P= 442 A = 67340

SYNC disabled and restarted

570 = 30441
10570 = 30556
1 = 553

STOP SER = A, clock = 0 #15 lamp is off

STOP P= 512 A = 77277

570 = 20513
10570 = 30556
1 = 552

DDT 1

```
SIP
ENA i   PAT
SIP
STA     TEMP 1
SIP
LSH     A
SIP
STA     TEMP 2
SIP
RSH     A
SIP
STA     TEMP 3
SIP
EOR     PAT2
SIP
STA     TEMP 4
SIP
JAZ i   ————————  o should take Jmp.
SIP
STA     TEMP 5
SIP
DCS     P
SIP
HLT
  TEMP  1
  TEMP  2
  TEMP  3        Modified to complement
  TEMP  4
  TEMP  5
  PAT
  PAT2
  PROG STORE
```

STOP P = 632 A = 57152

SYNC ENABLED

T1 = 52525
T2 = 25253
T3 = 12525
T4 = 0
T5 = 77777
T6 = 57152
640 = 20627

STOP P = 10632 A = 16620

SD I = 10611

10650	52525
1	25253
2	4304
3	16621
4	61156
5	16621

SE P = 10632 A = 77777

I = 10611

10650	52525
1	65253
2	65252
3	77777
4	0
5	77777

COM A 03003) was changed & located at 10611
30623

Bit 14 is being dropped in upper bay of core
picked randomly

Slow clock — Bit 14 flickering on & off in ZR when in locked. ENA when top bay is used. This points To either the load ZR or the unused left half MD

RA-L changed in Memory

Bit 7 being dropped during transfer fm TR → ZR in Jump instruction (F sequence)

NOR #4 ON 7K was replaced to correct problem of 5/5/67

SUN 5/6/67
STOP P = 10632 A = 37776

10640 =	30627
10650	52525
1	25253
2	12525
3	0
4	77777
5	0
1	10610

5/6/67 1235 SUN
Restarted with

(SDN)

STOP 1300 P= 613 A= 25252 I = 10610

640 607
650
1
2
3
4
5
} OK

CHANGED PROG LOC

600	20627
610	52525
611	25253
612	25253
613	0
614	77777
615	0

5/8/67 MON
UNLOAD GATE FROM AD repaired (BIT 5 replaced)

Restarted (SEN) STOPPED AT 0100 with P= 1605 (JMP SELF)

Looked like it must have dropped bit 9 in the Jmp address. Quite likely a JMP,C,1 in loc 5. DID NOT JMP OUT OF 0600 or 10600 PROGS

Restarted (SDN)

STOPPED P = 16400 (16400 = 0) Both 640 and 10640 (trap P-store loc) contain proper add. therefore the last Jmp. fm 10600 prog (JMP,C must be dropping bit 9 in address

Restarted (SDS)

5/10/67 Unload signal driver delays were modified on scheme 8 so that less delay is provided at beginning of gating period Ran out of wire. UAD (straight) installed however.

(SDF)

5/11/67 STOP P= 10632

53 = 00000
10654 = 67157 ($\overline{10620}$)
10655 = 77773

3

With SYNC ENABLED,
CLOCK FAST

STOPS ALMOST IMMEDIATELY P = 10632 A = 16621

STOPS Almost Immed P = 632 A = 12621

I = 611

652 = 304
653 = 12621
654 = 65156
655 = 12621

on fast clock, either bit 2 or bit one is being picked up in operand address of STA

(SDN) STOP 5/12/0600 Bit 12 was dropped from effective address on indirect JAZ at 677. instruction changed so that address is now stored in page zero instead of current page. If bit 12 continues to be dropped, then the program in upper bay 10677 should be activated

STOP 5/12/1000 Bit 9 was dropped from effective address on a JMP at 677 to (17547+1) it went to 16550 and stopped.

3

STOP 5/13/0830 A = 12525 P = 634
40 = 10613
Dropped bit 12, picked up bit 2
BLOCK WIRING CHANGED SO THAT MACHINE RUNS ON ALL MARGINS

CLOCK RANGES FAST 65
NORM. 86
SLOW 130

5/13/1235 (SEN)

5/13/1400 PUNCH TESTS OK (about 60 char/sec)

46	ENA CHAR	07060
47	AND 777	17064
50	JAZ 41	13040
1	ADD ONE	15061
2	STA CHAR	14060
3	OUT 20	10020
4	ENA DEL	07062
5	ADD DEL	15062
→ 6	JOV BEG	02046
7	JMP -2	01054
60	CHAR	—
1	ONE	1
2	DEL	1000
3	577	577
4		

5/14/1200 HANGUP PAT 2 777 at 636 had dropped bit 4 and picked up Bit 5

Restarted

5/14/1500 Stop with P = 702 (HLT) either JMP i at 701 ignored or wrong address Jmped to.

IGNORES i JAZ AT 677, it seems to merely go to next instruc.

Stopped SEQ = P CLOCK = 0 IR = 0 i = 1

XR = 52525

Restarted with START lights 13 & 14 were out on TP 1

5/15/67 MONDAY INSTALLED PUN/RDR ON PROG DESK (LUBRICATED)

(SEN) CHANGED STOP F-F WIRING To Try to fix HANGUP PROB.

5/16/0200 STOP P = 634 750 = 0 PAT 4 PAT 2 OK

1 = 10611 1 = 0

2 = 0

3 = 12525

4 = 65252

5 = 12525

LOOKS like wrong eff addr used for ENA i at 601 and ZERO WAS BROUGHT INTO A.

5/15/2030 TUES CHANGED GHH AT 35

MACH DUMPS OK ON FAST CLOCK

(SEF)

5/17/0300 Wed

STOP P= 14 A = 60776 40 = 20627

1 = 00662 750 = 52525
1 = 25253
2 = 12525
3 = 0
4 = 77777
5 = 0

XGF CARDS ASSOCIATED WITH LOADING OF
XR & ZR & Complementing of AD
were changed out with new sets

SLOTS 2C, 2D*, 2E*, 2F, 2G* *found defective later
(CARD IN 2F had NOTE, "OUTPUT 27 BAD")
This would have affected bit 12 in ZR

(SEF) Restarted

When running with fast clock, the KB loader changes
Location 17573 to 67 from 37
17577 to 37 from 00000

5/17/0800 STOPPED P= 16550 Bit 9 was dropped from eff address during
40 = 00674 JMP at 677 to 1754
TR gates in 1J, 1K replaced
A = 66262

(SEF) RESTARTED

P = 16550 dropped bit 9 (see 5/19/67)

Stop 40 = 663 XGG card in slot 1F replaced

A = 4023 (unload gate for DA)

1 = 667

(SEN) 10:00 5/18/67

Stop P = 634 A =

750 = 0
1 = 25253
2 = 12525
3 = 0
4 = 77773) ?
5 = 00004) ?

complement gate seems to drop bit 2 since the inverter on XGF card in slot 2G was changed recently, It was replaced by repaired XGF

5/19/67 Stop P = 13530 A = 40005 40 = 635

lamp bit 7 in ZR seems to be slightly turned on. (Low voltage on Z7 when running in AUTO LOCK)

750 52525
1 25257 → LSH
2 12525 → RSH
3 37776
4 777777
5 40005

later

XGF in 2E replaced, lamp seem OK

(SEN)

STOP P = 3 J = 0 40 = 677

1 = 17550

B = 0

JMPi 647 went to same location with zero

750
1
2
3
4
5
OK

7547

All NON Prog loc in 400-777 block set with trap loc

Loc 400 → 577
Cont 1100 → 277

Cont Loc 704 → 747 + 756 → 1000
1704 1747 1756 → 2000

STOP 5/19/67 P= 10635 A= 1400 4= 10635 ← BIT 8 & 9 picked up

Adder dropped bit 9 when entering XR fm A

Adder as if Bit 9 dropped when entering XR from A during SIP

ENA OC	10750	=	52525
LSH	1		14253 dropped bit 9
RSH OC	2		12025 misg bit 8
EOR	3		400 bit 8
Com OC	4		76377 msg bit 8 & 7
Com	5		400 bit 8

card (XGF) in 2D replaced

STOP 5/20/67/0900 P= 3 A= 0 40= 10677 MISSED TRAP

5/20/67 Bit 2 being dropped during trans fm DA → ZR

card (XGG in 1F replaced)

5/20/67 SAT NOON Stopped (SEN) Bit 9 dropped as before in XR

GHH in 2T replaced

5/21/67/2100 SUN NIGHT (SEF)

5/22/0600 MON P= 10635 A= 71574 40= 10634

Load Z gates in 2E, 2F replaced ↗ ↗

18XIE X3G

Looks like internal clock may have tripped up on FAST margin

10750 =	63325	OK
1	46653	
2	63325	Should have been 2
3	716	OK
4	75356	NO
5	71574	NO

Stop 5/23/67 TUES
10:00

STOP P=4001 A=67156 10=10634
XR=77777
SEQ P&F both on 10750 - 55 OK

(SEN)

5/25/0000 Thurs. STOP AUTO SEQ ON, F SEQ, All clock lights off

* HF not SET (males 7D, 7C or 6S suspicious)
CLOCK NOT RUNNING, STOP MAY HAVE BEEN SET, SINCE STARTED OK
When running, signals are on margin.

SINCE F was set & clock stopped, and F gets set on during 55.50 both off (normal stop state) The HF should not have been expected to be on. Trouble is entirely the clock or STOP logic.

GHH IN Loc 7K (STOP F-F) replaced by spare.
element on Output 17 looks like bad soldered joint.

5/25/1800 Thurs. STOP SAME AS MORNING

(SEN) GHH IN LOC 7K PUT BACK
XGF IN LOC 6N replaced.

5/26/1900 (SEF)

=41

		ENL	CWJ2	07060
PUN ON	2	OUT		10032
OR OFF	3	JMP .		41044
BIT 0 = ON/OFF	4	577		577

BASIC PUNCH TEST

=70 OUT 20 ACC = 77777
71 JMP SELF

=5 JMP 67

SWN 5/28/1200 STOP

P = 10633 A = 71600 40 = 10634

10750 = 63325
1 = 46653
2 = 63325
3 = 71600
4 = 6177
5 = 71600

1 = 46

SIMILAR TO FAILURE ON 5/22 SEF WAS RUNNING

TUES 5/30/ AM DAY (SEN) XCA Counter substituted for original spare GMM element center in clock circuit. Clock now runs with margin set for 3 μsec per phase.

Program runs ok at Fast margin (5 μsec) but Keyboard input program will not input the correct data.

THURS 6/8/67 0300 STOP P = 405 A = PAT (52525) 1 = 476

WITH NEW CONFIDENCE PROG

		should be
111 = 00000		52525
112 = PAT2 (12525)		25252
113 = 25252		

Temp loc (111, 112, 113) are set like they would be at the end of test 11 or test 12

400 (ENA PAT) was executed
Instruction at Loc 401 (STA 111) was not executed
402 (RSH) was not executed
403 (STA 112) was not executed
404 may have been

→ looks like bit 2 was picked up in T Reg.

Restarted (SEN) 400 became 404

Thurs Afternoon P = 4002 A = 1 I = 547
she cc

111 = 77777
112 = 77777
113 = 00000

on High Margin

P = 20437 A = 2

111 = 77776 failed to com
112 = 77775 A
113 = 2 may have skipped 2 instead of 1 instruct

P = 20430 A = 25252

111 = 1
112 = 52524 skips 2 instead of one instruction
113 = 25253

Test.		Temp 1	Temp 2	Temp 3	A
	1	PAT	25252	LSH PAT2	25252
	2	LSH PAT	0	LSH PAT2	0
	3	LSH PAT	0	LSH PAT2	77776
	4	PAT	77777	0	77776
	5	1	77777	0	0
	6	77777	77777	0	77777
	7	0	0	0	0
	8	77777	1	0	0
	9	PAT2	PAT2	LSH PAT2	0
	10	77777	PAT2	LSH PAT2	0
	11	0	PAT2	LSH PAT2	0
	12	0	PAT2	LSH PAT2	

FAST CLOCK P = 440

Temp 1	1	DCS NOT coming up with NEG ZERO when adding 77776 to 1
2	0	
3	77777	
A	77777	

STOP FRI JUNE 9 0100

P = 440 A = 1 1 = 474

111 = 25252
112 = 777.77
113 = 1

OV = 1

			A
Loc 431	is	executed (com A)	1
432	is	not	STA TEMP1
433	is	not	DCS A
434	is	not	STA TEMP2
435	is	NOT	com A
436	is	executed	STA TEMP3 1

Similar to stop in 6/8, four locations are skipped over. Bit 2 coming on in the TR causing trouble.

Since trouble did not affect the data going through A, we can assume that adder is OK

So far, it looks like BIT 2 coming ON and not affecting other addresses when BIT 2 already on.

Trouble has to be in P seq since it has already occured by F seq when instruction is brought in.

TR branch unload gates replaced which is used in step L4.5.

→ XGF in LOC 1K replaced

Stop Fri June 9 0200

P = 20510 A = 20510

111 = 77777
112 = 12525 PAT2
113 = 25252

SOLID HANG UP original card in loc 1K repaired and replaced back into 1K

STOP P = 440 A = 1

111 = 25252
112 = 77777
113 = 5

trouble now points to unload code on AD since STA Temp 3 at loc 436 picked up bit 2
2nd stop is just like earlier stop this morning

→ 4C repaired (output # 22)

STOP P = 476 A = 4 OV = 1

111 = 12525 PAT2
112 = PAT2
113 = 25252

→ one output # 11 on 3L replaced

If this doesn't fix bit 2 problem, the next thing to do is to replace card 3D, 2K, 2C, 2D 2E, 2F

STOP P = 414 A = 65252

111 = 65256
112 = 65252
113 = 25252

→ card in slot 3D was repaired only NOR not replaced which affects bit 2 was output # 7

Still can't run fast clock margin

STOP P=454 A=1

111 = 77777
112 = 77777
113 = 0

elements yet to be replaced,

more suspect than →	2D7	2K24
	~~2C7~~	2K27
	2E7	2K13
	2F7	3D7

STOP 0500 hrs. same trouble as before.

→ card 2C (XGF gate to XR) replaced

(SEN) element with output #7 on 2C had open connection between output and PSN (should be 2K)

7/3/67 P=3 loc 1 = 1 loc 100 = 400
Loc 3 = 0

111 = 77777
112 = 1
113 = 0
114 = 0

SEN loc 502 was cleared to zero

*7/7/67 STOP P=1 A=0 loc 1 = 1

100 = 1400

Turnoff (764) = 40025 (OK)
Turnon (761) = 531 (OK)

HAPPENED AT 1:00 AM

111 = 0
112 = 12525 PAT2
113 = 25252 LSH PAT2

SDN

* 7/8/67 SAME STOP AT 0100 HRS AS LAST NIGHT

* PROG BUG DUE TO [illegible] ARRAY

SEN

7/8 when clock set to fast margin, the confidence prog will only run INST step and not AUTO. It seems that the SEQ SELECTOR does not settle between P and F in time for TO events to be correctly executed.

Temp 1 = 1
2 = 52524
3 = 25253

SKIP WAS BEING SET TO 1 and then later 2 to make a skip of 3. Wiring corrected.

MACHINE RUNS CONFIDENCE PROG AT FAST MARGINS NOW

SEF

SDF

7/14 EARLY MORN P = 455
A = 77331
111 = 0
112 = 77331
113 = 0
100 = (3) 3776
3 o'clock

1 = 1000
2 = 77331
4 = 1000

IN TEST PROGRAM 7,

Loc		
446	ENB	A
447	COM	B
450	ENA	B
451	STA	TEMP1 (111)
452	AND	ZERO
453	STA	TEMP2 (112)
454	JAZ	Jmp should be taken

Looks like B was loaded with 446 instead of C(A)

∴ when B was complemented, It would equal 77331
then ENA B would make A = 77331

7/16 SUN 500 PM P = 2 S = 41001
STOP HLT A = 63177

(SDN) 111 = 0 200 = 46376
112 = 12525
113 = 25252

10:00 PM HLT
XR = 70137

P = 2 100 = 60276
A = 70137
111 = 0
112 = 12525
113 = 25252

Program loc in Clock INC program bad

RESTARTED
SDN

8/2 WED 600 AM A = 1075 ? HLT except TR≠3
P = 1075
111 = 0 XR = 1075
112 = 12525 ZR = 0
113 = 25252 TR = 0
Looks more like a USER hangup than HLT. SEQ = E
MODE = SEQ STEP
INST = HLT

When restarted, stop 415 111 = 25253
112 = 1
A = 1 PAT2 had dropped a bit 0

Loc (770) PAT2 restored to 12525

SEN Restarted OK RUNS OK ON FAST & SLOW clock

5 MIN LATER WHEN MANUAL STARTED RESTARTED OK

STOP A = 0 X, Z, T = 0
P = 1145
111 = 0
112 = 12525
113 = 25252

WED 8/12
0600

A = 0
P = 1144
111 = 0
112 = 12525
113 = 25252
FLAG 777 = 5010

XR = 0
ZR = 0
TR = 0
SER = E
MODE = SEQ STOP
INST = HLT
CLOCK:

BIT 14 was dropped

0215 TUES 8/14

A = 0
P = 00004
111 = 77777
112 = 77777
113 = 77777
777 = 0
1 = 4
4 = 4
5 = Jmpi 1

100 = 3

XR =
ZR =
TR =
SEQ =
MODE =
INST =
CLOCK =

LAST clock output was at 12:00

Relay R on Power Control Panel may have to be replaced or blown will have run all the time in cab 4

mach was warm since it had been running for 1 hr 1.5 minutes and AUTO mode was being forced by MEM OK signal. After mach was coxed down, it was restarted.

0600 THUR 8/16 DCS P loop

A = 0
P = 506
1 = 60462
4 = 60462
5 = 41077
100 = 05376
111 = 0
112 = 12525
113 = 25252
77 = 1200
777 was NOT read

RESTARTED AT 377
OK, NO LOCATIONS CLOBBERED

EVEN THUS - A = 0
JAZ i NOT TAKEN

1. Did not pull A fm. Core
2. Did not recognize all zeros
3. Took wrong jmp address.

JAZ i test to detect missing of indirect bit

10 PM FRI 8/17 Debugged program which loads character into buffer.

MON AUG 21 0700 Turned on, scaled in, but failed to increment Hours

DCS P

0 = 415
1 = 60462
2 = 1
3 = 12524
4 = 60462
5 = 41077
100 = 6376
111 = 0
112 = 12524
113 = 25252
77 = 1200
777 = 6376
10000 = 0

XR =
ZR =
TR =
SEQ =
MODE =
INST =
CLOCC =
OV = 0

767 = 52525
770 = 12524 should be 5 (MUST HAVE BEEN DOCKED)

Prog 406 7747 should have been 7767

Bit 4 was dropped from address portion of instruction after loc 406 & 770 were corrected, Restarted OK

WED AUG 23 5 PM DCS P

0 = 453 with OV set
1 = 60470
2 = 77331
3 = 1
4 = 60470
5 = 41077
100 = 45376
111 = 77777
112 = 1
113 = 1
77 = 1200
777 = 45376
10000 = 0

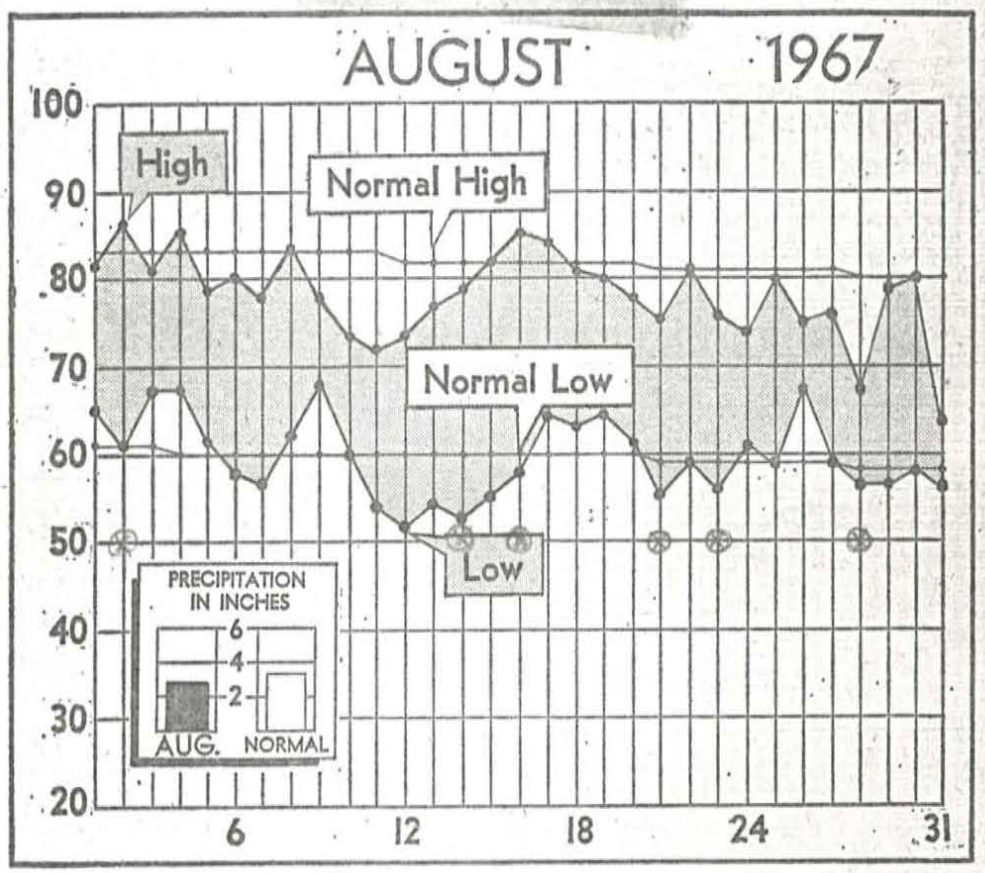
Restarted OK at 377

DRIVE SETTING INCREASED FROM 7/0 to 9/0

P=607
1 = 60
2 = 12
4 = 6
5 = +1077
100 = 4376
111 = 0
112 = 12525
113 = 25252
77 = 1200
777 = 1376
10000 = 0

MACHINE VERY COLD SINCE WINDOW WAS OPEN

Loc 0-2000 stored at 11000 - 13000 for safekeeping.



AUGUST WAS COOL IN PITTSBURGH, records show, as the temperature reached the normal highs on only seven days and exceeded these marks just four times. Hottest day of the month was Aug. 2, when the temperature nudged up to 86 degrees. Lowest daytime temperature was yesterday, when the mercury reached 66 degrees. For the most part temperatures averaged in the high 70s and dipped into the low 50s at the bottom points. Rainfall for the month was below normal, amounting to 2.67 inches as compared with the normal 3.31 inches.

SEP 4 KLENSCHMIDT LUBRICATED AND ADJUSTED

LTRS STILL DO NOT LINE UP EXACTLY WITH FIGS.

SEP 11/12 12 midnite Window was left open at Computer stopped, restarted OK

SEP 15 0600 hrs STOP P= 2023
A= 25252
100 = 5376
5 = 41077
111 = 25253
112 = 0
113 = 25252
FLAG 777 = 5376

As little as 3 MEG res to gnd at PWC TB3/4 will start machine. or keep it running. CCO bit 7 is open and so is TRUNK I/O DISABLE, "5" is displayed on clocks.

Possibly bad relay on bit 7 of word 31 which doesn't let machine stay on long enough.

PATCH ADDED AT LOC 554 - 555 TO SAVE CUR TIME at 110_8

SEP 18 0200 STOP P= 20546 MIN : SEC 59 : 02

110 = 66202 time turned ~~off~~ (
526 = 40025 time turned ON
09 : 15

100 = 02376 yet machine is off
5 = 41077

Restarted at 1061 OK

SEP 18 1000 Stayed on in DCS loop

P = 2101
A = 77777
S = 41077

100 = 20376
110 = 64424 52:14
526 = 50200 21:00

Restarted at 1061 OK

111 = 12525
112 = 12525
113 = 25252

diode removed from turn on circuit on system 33
To attempt to prevent false turn on

SEPT 28 THURS 1700 hrs. HLT 2d machine was running

A = 0000 ϕ = 0 E = 0

→ P = 125
S = 41001

110 = 40010 current time 8 SEC After hour
526 = 66325 time on 59:55 OK

111 = 12525
112 = 12525
113 = 25252

B = 16
4 = 62075

100 = 45376

Restarted OK at 1061 2d Loc S = 41077

At 2158:50 COMP CAME ON, TURNED OFF AT 21:59:00
did not come on at 22:58:50 or 22:59:50

P = 2053

100 = 51376

110 = 66200 59:00
526 = 40025 00 15

→ didn't stop when turned off at 21:00:15

OCT 8, Made modification in Power Control Panel to hold Master Clear on until power is shut down to prevent machine from restarting prematurely during turn-off.

OCT 9 Stopped SEQ = 0 A = 0 HLT = 0

P = 262
5 = 41001
1 = 22022
4 = 22022

110 = 40010 00:10 stopped 8 sec after
526 = 06324 59:54 time on OK

100 = 41376

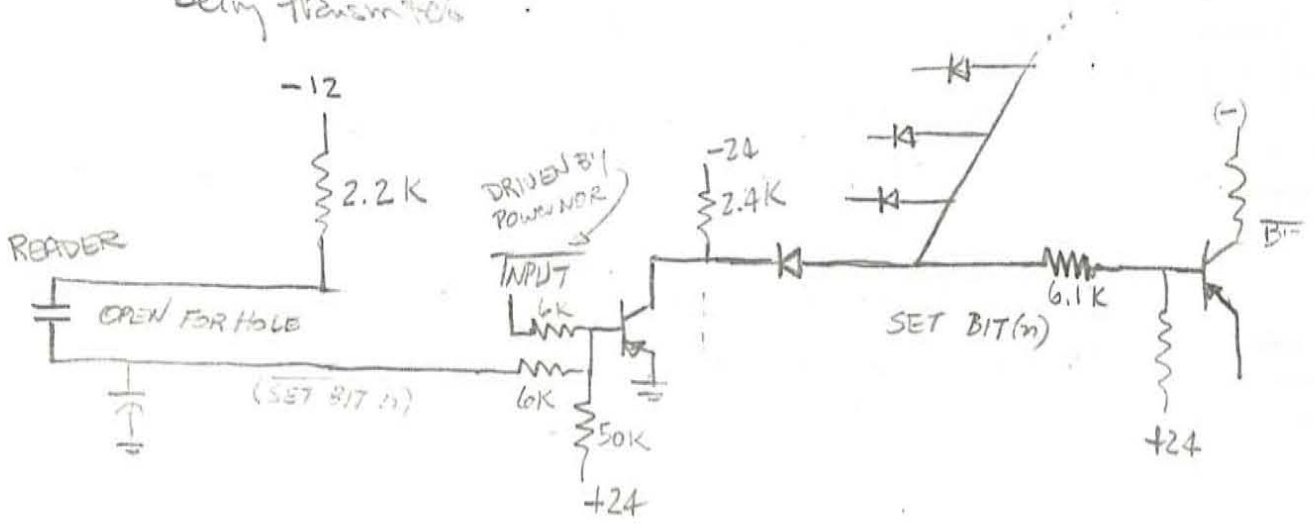
111 = 25253
112 = 0
113 = 25252

SAME AS 9/28

10000 = 0

looks like a 1261 was executed (JMP 261)

OCT 9 Reader adjusted as still reads extra holes when reading channels 6, 5, 3 when 7 holes are being transmitted.



OCT 10 Malik read 4 o'clock at 5:00 clock

P= 2014
5= 41077
1= 20544
4= 20540

110 = 66200 59:00 stopped at 59:00
100 = 44376
526 = 40025 00:15 started at 00:15

did not stop properly at +15 sec

OCT 10 Reader input problem solved by addin 15 capacita to the common input data lines to neutralize the line-line capacitance. RUNS COPY TAPE OK NOW.

OCT 11 RELAY ADDED IN CPU CABINET WHICH GNDS THE MEMORY START PULSER (PIN 1D32) WHEN POWER IS TURNED OFF BY CCO

Reader input card bits 8-14 were disabled by wiring (-)12V to them so that only the lower 8 bits of the reader word come in "1's"

OCT 13 Stopped right after changing fwa 12 to 1

A = 6016 P = 22015
526 = 66324 59:54
110 = 40000 00:00
111 = 31267
112 = 6016
113 = 25252

OCT 14 HLT Decode NOR (MIC) WAS REPLACED ON XKA BOARD IN SLOT 6L because the connections Looked like dirty soldered joints.

OCT 16 HLT

P = 114 with OV = 1
5 = 41077
1 = 543 with OV = 1

526 = 66324 59:54
110 = 40023 00:13

111 = 0
112 = 12525
113 = 24252
↑ should be 5, bit 9 dropped

restarted OK

Core loc 0 - 3000 cleared and restored to eliminate half set cores

OCT 14 HLT P = 114

110 = 40023 00:13 off
526 = 66324 59:54 ON

100 = 11376 (9 O'clock)

Restarted OK

Loc 776 was cleared and this prevented proper incrementing of clock

C(776) is only used as operand in one location (711) EOR 16 776

it is true that if 16 became 14, then loc 776 would be cleared by STA

This imply BIT 10 dropped

IF ENA 113 become SIP 113
(7) (5)

OCT 20 RAN THROUGH HLT AGAIN

SOLIDLY IGNORED HLT, So trouble was definitely traced to GHH card in Slot 7D which was not coming on during Step 3 to turn mode f-f to SEQ STEP.

NDR REPLACED, AND CARD PUT BACK INTO ECHO

OCT 24 MACHINE FAILED TO COME ON AT 0600 to increment clock light
Everything in memory OK in the clock program.
loc 100 = 5531 which looked like the time had be set correctly at 0500. lights on alarm clock (in this case "59") are needed to know whether ccd were set correctly.

Machine was cold, as this may have affected the setting of the ccd at 0500.

Restarted OK at 1061

Loc 10000 = 20564, this was cleared to zero through keyboard.

After 5 startups and shutdowns, the loc 10000 still = 0

OCT 27 FRI AT 0700, MACH DID NOT TURN ON.

P = 20563 (where it should have been)
100 = 4653 (6:59)
Restarted OK as 100 incremented to 7:59

→ INTERMITTENT ELEMENT IN I/O CABINET SEEMS TO BE DROPPING/ADDING BIT TO OUTPUT WORD TO COMPARITOR.

OCT 27
Midnite

CAME ON, STOPPED

P = 5074

107 = 5074
73 111 = 52525
74 112 = 52524
75 113 = 25273

A = 25273

PAT =
PAT2 =

C(74) = C(73) − 1

Prog entered before STA 73

5055	DCS A		77776..after DCS
5056	DCS P		
5057	SIP 7_{10} (107_8)		
5060	COM A		
5061	SIP 107_8		
5062	STA 111	was	52525
5063	SIP 107_8		
5064	DCS A		52524
5065	SIP 107_8		
5066	STA 112		
5067	SIP		
5070	COM A		25253
5071	SIP	should was	
5072	STA 113		25273

↑ PICKED UP bit 4 (added 20_8)

✓ 5037 brought PAT into A (52525)
✓ 5040 SIP 107_8
5041 EOR 115 NEZERO this was never executed since 52525 was stored at Temp 1

∴ Bit 4 was picked up in the prog counter And caused 5061 to be executed.

when ECHO turns off, 53_{16} is output. Since Bit 4 is on, this does not explain the hangup of OCT 24, 27
Also, CCO chan = 30, bit 4 not at fault in address

STA 111, 112, 113 were executed correctly so bit 4 addition did not affect address of where data is stored.

DATA was affected since bit 4 was added during STORE INSTRUCTIONS

SAT OCT 28

JUMPED OUT OF PROG

107 = ② 5010 P = 4001 A = 65252

5 = 41077 111 = 52525
112 = 65252
113 = 0

~~DES~~ OCT 31

At 0600, clock showed 3

COMPARE RELAYS WERE SET PROPERLY TO 59

Machine started OK at 0700 and incremented 3 → 4

Machine then hung up at 563 when manually started. restarted with START Button.

Clock reset to proper time.

SHUTDN prog entry changed so that TIMECK Bids for SHUTDN instead of jumping directly to it.

NOV 10 0700 HLT A = 77777 E&O = 0

P = 1367 5 = 41077

100 = 6376

(00:14) 110 = 40024 526 = 66322

111 = 00000 (59:52)

112 = 25252

113 = 00000 107 = 5217

1366 ≠ 1064 ∴ NOT BID FOR

Restarted OK

Picked up

1	3	6	7
001011110111			

-this address must be in our loop

Possible addresses generated by one bit change

1366	NO
1365	NO
1363	NO
1377	NO
1347	NO
1327	NO
1267	NO
1167	NO
1767	NO
367	NO
3367	NO
5367	NO

NOV10 0900 CAME ON AT 59:59, didn't increment time clock

HANG UP (DCS)

P= 5164

111 = 77777
112 = 21
113 = 00000

E ≠ Ø = 1

110 = 59:55

107 = 5164 OK

A = 20

BIT 4 seems to be picked up in P and A

NOV 11 Found that GHH Card in Slot 2M was intermittently solid failure on Bit 4 of 2 register. I knew it couldn't be in the memory since the bit was coming up in both HI and LO Banks of core, NOR elements with outputs on 13 and 27 were replaced on the GHH and it was replaced into slot 2M. The spare GHH card worked from 5 until 9 without error, when placed in slot 2M

NOV 14 CCO output turn on time: 59:59

P= 1013

SINCE MACHINE HAD

100 = 43531 (59:~~58~~)
107 = 25217
110 = 0
110 = 66331 (59:59)
112 = 25252
113 = 0
526 = 66322 (59:52)

NOV 21 ① SEEMED LIKE INTERRUPT WAS JUMPING TO 25, INSTEAD OF 5

GHH CARD IN SLOT 5S WAS REPLACED

② XGB SPARE REPAIRED AND TESTED OK IN SLOT 2C

NOV 22 2 GHH boards were repaired and tested, placed in spare storage

2 XGF boards were put in slots 2D & 2E to check out before placing in spare storage.

9 o'clock stopped at loc 26

GHH at 5S replaced with spare to see if CLR TR element was bad.

NOV 24 MACH OK GHH which was removed from slot 5S was put in slot 3S (BIT 13 Addr) to see if will fail intermittently. Bit 13 should not affect addressing, but will show up in diagnostic

Original card in 3S placed in desk standby

MACH STOPPED AT 200 with BIT 13 on in A

Original 3S card put back in 3S, 2d defective GHH will be repaired.

NOV 25 HLT stop

(After INC the clock to 9 o'clock OK)

Z = 60022 E = 1 O = 0

X = 20 P = 60022

5 = 41077

107 = 65164 110 = 40070

526 = 59152

Restored OK

111 = 77777

112 = 1

113 = 0

NOV 26 DCS start 5143

Run for 2 seconds before C.C.

111 = 77577
112 = 77400
113 = 77401

→ ORIGINAL XGF CARD IN SLOT 2E reinserted.
Spare XGF which had been placed in slot 2E on 11/22/67 was removed as marked

→ ORIGINAL XGF CARD IN SLOT 2D reinserted

SPARE XGF WHICH HAD BEEN PLACED IN SLOT 2E on 11/22/67 was removed and marked.

Restarted OK

NOV 27 DCS Stop 5143
7 O'clock PM

P = 65143
5 = 41077

110 = 59:54
107 = 65143
111 = 77777
112 = 00000
113 = 7523

P = 7523

4 = 1 = 25032

TEST CARD SLOTS

	QUANT	TEST SLOT	
XGA	1		
XGB	6	4D	
XGC	14		
~~XGD~~	10		
XGE	4		
XGF	19		
XGG	2		
XKA	2		
XDA	4		
2DD	1		
2EB	4		
2TA	1		
GAH	20		
GDH	19	3J	Bit 12, 13 of adder
GHH	30	3S	Bit 13 of X + Z
DAH	4		

Found bad XGF at slot 1H (Bit 4)

When Hammer was Cage G, machine stopped at (3)5193

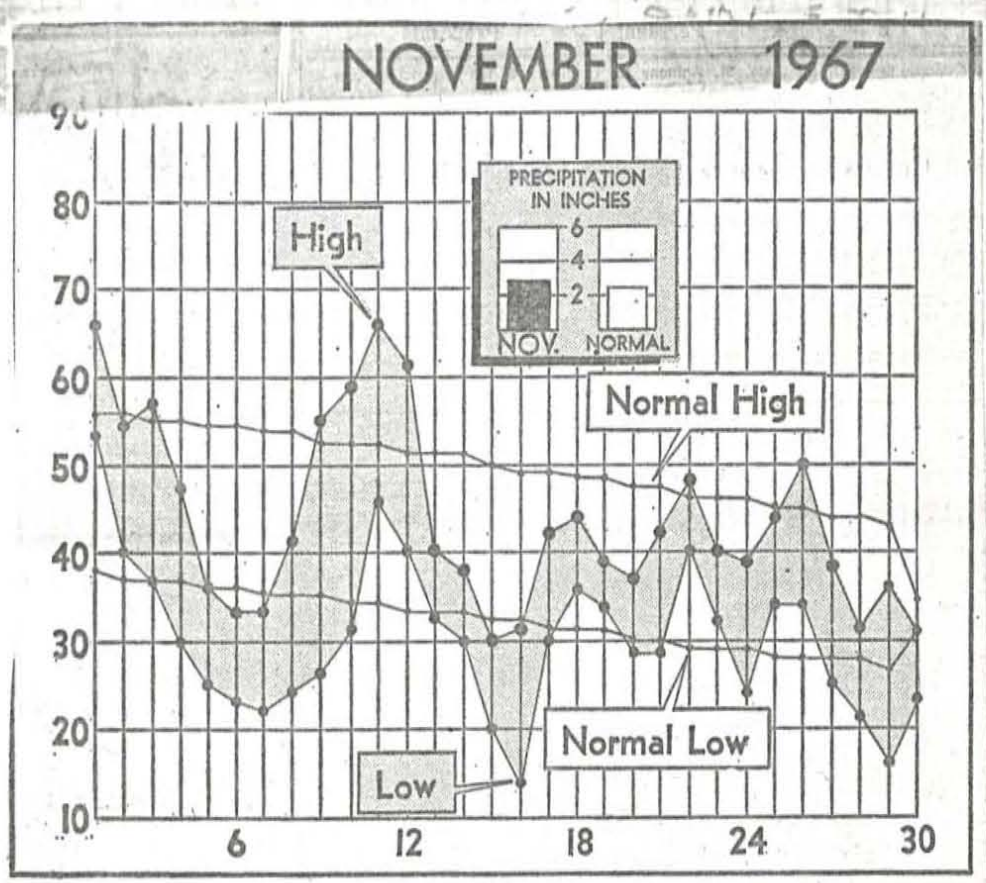
(fast clock) 5 = 41077 111 = 25253
3 = 40614 112 = 0
113 = 0

By Rapping card handles with screwdriver handle, two intermittent cards were smoked out

2EB in slot 6G Clock $\overline{50}$, $\overline{51}$, 52, 53, $\overline{55}$
XGB in slot 1L (unload TR) (BIT 11 bad)

→ MACHINE LEFT ON FAST CLOCK MARGIN TEST PLUG

NOV 27
(MONDAY)



SUB NORMAL TEMPERATURES generally prevailed during the month just ended with a four-day span (Nov. 9-12) providing substantially higher-than-usual temperatures for a November here. The mercury reached 66 on Nov. 11—the day of the Veterans Day parade—but within five days sank to the month's low of 14 degrees. Precipitation was normal for the month until yesterday's snow added three-quarters of an inch for a total of 2.96 inches, as compared to the normal 2.24.

TUES DEC 5, 1967

HLT XR = 50376 P = 70377

ZR = 60377

Ruth turned machine off yesterday while stopping first 2nd half set a dummy location.

corrected 3 locations in clock shutdown prog.

loc 500 - 777 are checked OK

WED DEC 6, 1967

P = 5214 A = 0

107 = 5214
110 = 1448 minutes
111 = 0
112 = 25252
113 = 0

526 = 00:38 seconds after hour.

MON Dec 11, 1967 7:00 PM

HLT ZR = 60000 EAO = 1
XR = 71460 5 = 41077
P = 60201 1 = 64207

201 = 0 526 = 59:53

HRS were properly incremented

107 = 25133
110 = 00:10 sec
111 = 77777
112 = 00000
113 = 00000

8:00 DCS Stop. P= 5013
A= 67653

526= 59:52 107= 5013
110= 40002 00:02
111= 57526 } RIGHT SHIFT
112= 67653 }
113= 0

Slowed to NORMAL CLOCK.

Original XGB removed from IL was repaired and replaced.

FRI DEC 15 5 o'clock PM HLT

XR= 10400 E$O=0
ZR= 20000

→ P seq was on HLT was ~~off~~

P= (5016) 5= 41077

107= (5055)
→ bit 5 was dropped in the instruction counter 110= ~~40000~~ 00:00
111= 65252
SEQ Step was set 112= 37777
113= 40000
526= 66322 59:52

7:0 Clock HLT

P= 20205 1= 267
XR= 72653

107= 5143
110= 40000 00:00
111= 72651
112= 72652
113= 72653
526= 66322 59:52

DEC 15 9:30 Loc 10000 was NOT = 0 and PWFS getting messed up on startup.
RATTLED CARDS, still runs OK

HLT 10:90 Bit 0 was dropped in the address of operand in loc 5064

DEC 16 Repaired wiring to connection on K105 relay in memory. It had come loose and was so hot it burned sleeving and insulation off

DEC 21
1. Reloaded exec prog.
2. Relocated CONFIDENCE Prog into upper core bay
3. RUNS OK

DEC 22 DCS P

A = 62323
P = 35465

5 = 41077
110 = 44506

526 = 66322 59:52

111 = 62321
112 = 62322
113 = 62323

→ Looks like bit 7 dropped in low bay.

DEC 22 DCS P

A = 62323
P = 35465

5 = 41077
110 = 00:06
526 = 59:52

111 = SAME AS BEFORE
112
113

SLOW CLOCK

DEC 23 12 Midnite HLT

P = 20002
A = 55532

5 = 41001
1=4= 35453

NO SIP
107 = ~~25031~~

110 = 40000 00:00

526 = 59:52

Clock change at Midnite OK.

Necessary to Bootstrap before restart

3:00

P= 261

A=

5= 41001
1=4= 552

NO SIP
~~107 25031~~
110 00:10
526 59:52

111 77765
112 25240
113 0

clock change at 0300 hrs ok

Restarted OK.

DEC 26 HLT 10:00 AM

P= 62
A=

5 = 41077

110 = 00:02
111 = 77765
112 = 25240
113 = 00000
526 = 59:50

→ DRIVE REDUCED TO 34.0 V (40 set)

→ SET Clock FAST

RA-L card with bits 8 & 9 swapped with the one in bit 28-29 (13 & 14 in high bay)

HLT P= 222

Replaced 8 & 9 block and swapped bits 14 & 15 with 28 & 29

Dec 25

8:00 HLT P= 205 5=41077
A= 41001
111=77765
112=25240
113=0

Restart OK

PAT OK

HLT P= 113
A= 23

5= 41077

111 : 77765
112 : 25240
113 : 0

110 = 00:06
526 = 59:52

HLT P= 165
A= 164

5= 41077

HLT P= 065

5= 41077

XGF IN LOC 6H (gate which loads IR from EDS)
was replaced

STILL STOPS, Looks like indirect instruction not executed indirectly

7D, 7E, 7F, 4V,

↑
Chayd ist

DEC 26 1:00 DCS

P = 35442

A = 15435

5 41077
110 00:00
111 1
112 77777
113 62342
526 59:52

Restarted OK at 1061

GHH IN SLOT 7E was replaced by all new NDR CARD

11:00 HLT
P = 62

INDIRECT FAILED

4V28 Replaced.

DEC 27 9:00 DCS

P = 35416
A = 62415

5 = 41077
110 = 59:52
111 = 60267
112 = 62416
113 = 25252
526 = 59:52

6:30 HLT

P = 15223
A = 0

111 = 1
112 = 76777
113 = 0

BIT 9 bad on the Z reg load seems

→ XGF in 2E replaced with spare. (changed back later)

→ XGF in 1J replaced with spare. this one is the one which loads TR during indirect transfer (put back later)

bit 9 seems to be dropping

→ GDH in loc 1N was replaced (BIT 9 of TR) (changed back)

HLT

P = 15223
A = 0

5 40077
111 0
112 12525
113 25252

CLOCK set for normal speed.

HLT

P = 201
A = 52525

111 = 52525
112 = 65252
113 = 25252

1 = 14025 ?
4 = 21067
5 = 41007

All original cards put back, spares retrieved and Attest concentrated in the unload ZR area (bit 9)

→ XGB IN 4N replaced

for shakedown at high speed clock,

4F and new 4N card were swapped

4F ↓ complement unload

4N ↑ Unload Z

DEC 28 900 PM

HLT
P = 62
A = 26

RESTART OK

110 00;03
111 = 0
112 = 12525
113 = 25252

→ Still NOT UNLOADING Z PROPERLY

→ CLOCK SLOWED

→ CLOCK SPEED UP

→ GHH IN 4H (CLR ZR 8-12) replaced by spare.

→ could be causing loss of ZR bit 8 in indirect Jmp.

DEC 30

DATA (30) lines were reterminated at the 1E and 1F slots to eliminate the source of trouble in the bit 9 mystery.

CARD IN 1L was changed out with a spare since the current problem with BIT 9 seems to have cropped up after previous repair work on XGB in 1L.

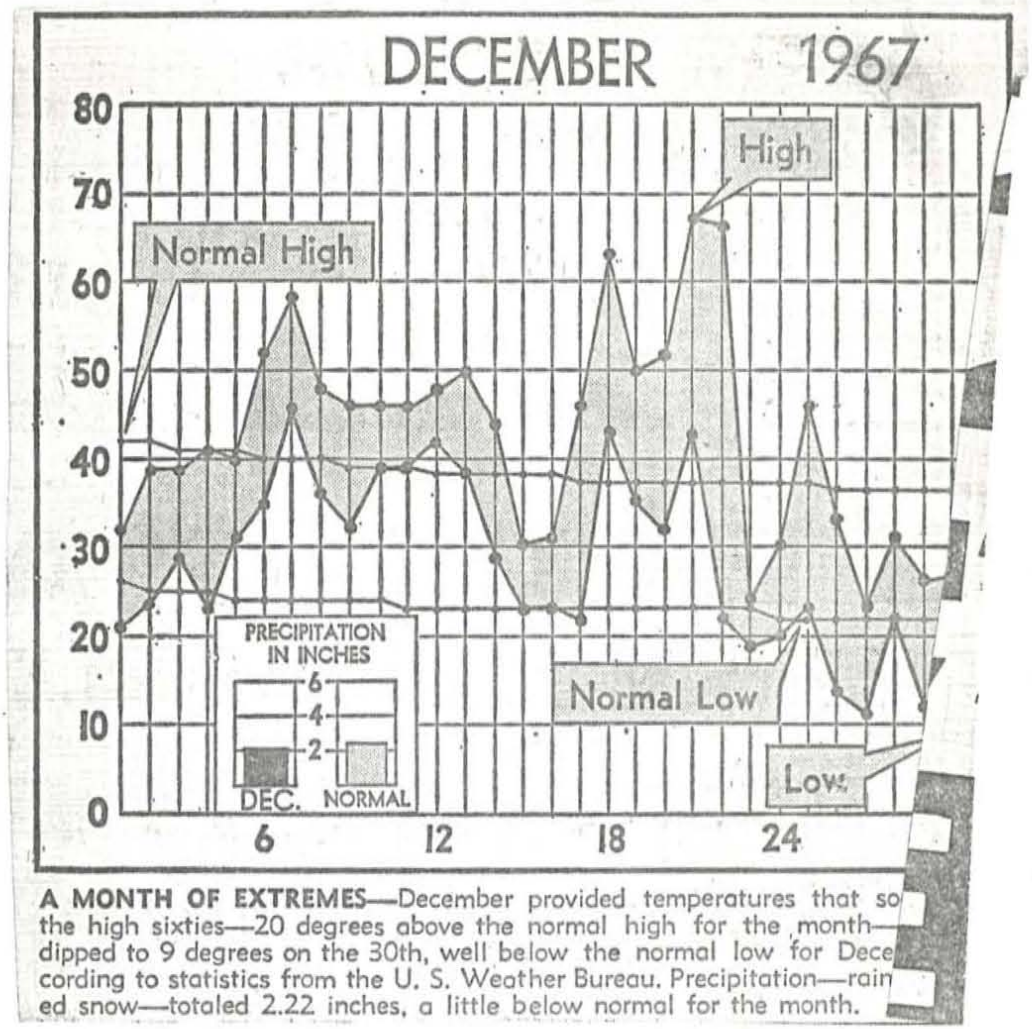
CORE DRIVE INCREASED TO 340 VOLTS (510)

DEC 31 0400 HRS HLT Bit 9 dropped

ON MAINTENANCE PANEL BIT 9 of Addr did not follow bit 9 of ZR. Therefore, addr at fault.

→ GDH at 3G replaced.

ISTOP A 1:00 PM bit 3 was set on in two instructions. of clock prog. Bit 283 in MDR (Replaced by spare FF-L



A MONTH OF EXTREMES—December provided temperatures that so the high sixties—20 degrees above the normal high for the month—dipped to 9 degrees on the 30th, well below the normal low for Dece cording to statistics from the U. S. Weather Bureau. Precipitation—rain ed snow—totaled 2.22 inches, a little below normal for the month.

JAN 4 HLT

ZR = 33152
XR = 576
B indicator was set

HRS NEVER CHANGED FROM 7 to 8

P = (2) 0004
4 = (2) 0002
1 = (2) 0002
5 = 41077
2 = 000555

111 = 0
112 = 12525
113 = 25252

RESTARTED AT P = 1061 OK

CORRECTED LOC 1008 to 8.00
TURNED OFF

JAN 7 HLT ZR = 20000 OV = 1
XR 200

P = 35640
1 = 21067
2 = 1067
3 = 0
4 = 21067
5 = 41077

110 = 00012
111 = 1
112 = 77777
113 = 0

→ PICKED UP BIT 7 in P and A

→ CLOCK SLOWED TO NORMAL SPEED

JAN 9 FF-L IN MDR Bit 6-7 was replaced. ←

JAN 10 this was to fix previous prob with Bit 6-7

→ Bit 7 Failed by coming on in P&A again
Memory probably not at fault

→ Turn off time increased to 01:000 so that more chance for bit 7 prob to occur

if bit 7 is picked in turn off prog it will jump to 7540 - 7550 from 540-550 (zeroed)

if bit 7 is picked up in 15400 - 15520 prog it will jump to 15600 - 15720 (zeroed

in either case machine will stop.

JAN 21 SUNDAY DCS STOPPED AT 10:00 AM

P = 15440
A = 77772
B = 1067
4=1 = 21112
5 = 41077

526 = 59:50
110 = 59:57
111 = 62350
112 = 62347
113 = 77772

Restarted at 1061 OK

62350 = $\overline{15427}$

NEXT TIME, BE SURE CHECK ALL THE ENTRIES IN THE BID TABLE 2140 - 2177 to SEE IF IMPROPER BID WAS MADE.

1111 SIP
1112 JMP
1113 JMP

} NO INTERRUPT SHOULD BE ALLOWED HERE, OR IN the OUT/INP SEQ

Logic for INT disable was checked, and JMP can be interrupted. This must be changed

STOPPED HLT ZR=20000 XR=0
P = 35715

111 = 0
112 = 12525
113 = 25252

4=1 = 15424
2 = 1
5 = 41077
110 = 00:11
526 = 59:52

RESTARTED OK
1061

NO BID IN TABLE FOR 15715, so Bit 7 Must have been

→ XGB in IL changed

IN & IK are also suspect

62

JAN 23 0800 DCS STOP
P was Not Saved.

2 = 1067
→ 4 = 01112
5 = 41077

526 = 59:52
110 = 59:54
A = 5033

111 = 07633
112 = 55316
113 = 05034 + 1 2252
62352 +
50362 −
03620 EOR

RESTARTED OK
1061

JAN 23 1930 hrs, INP, JMP & OUT WERE WIRED TO BE NOT INTERRUPTABLE.

OCTAL DUMP DEPENDS ON JMP BEING INTERRU
JMPs CONVERTED TO JAN IN DUMP

9190 HLT BIT 7 ON IN XR

P = 7741
541 should have been set

~~replaced.~~

Looks like LXR adds bit 7
gate or XR7 bad.
→ 2C & 2D (XGF load gates XR)
replaced.

JAN 24 1800 hrs. DCS

P = 15477 A = 2524 = 75253

111 = 30213
112 = 10001
113 = 22526

110 = 59:59
526 = 59:52
4 = 1 = 15403
5 = 41077
2 = 0

START OK 1061

TEMP 3

12525
22526

0 1 0 1 0 1 0 1 0 1 0 1 1 0
0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 AND
0 0 0 0 1 0 1 0 1 0 1 0 0

02524 should have been in A (it was)

∴ address 15521 } was correctly accessed
113 }
3 }
15474 }
15475 }
15476 }
15477 }

TEMP 2

10001

0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 10001 ADD
0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 12525

0 1 0 0 1 0 1 0 1 0 1 0 1 1 0

22526 should have been in TEMP 3 (it was

15473 } was correctly accessed
15472 }
112 }

TEMP 1 30213

0 1 1 0 0 0 0 1 0 0 0 1 0 1 1
0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 AND

0 0 1 0 0 0 0 0 0 0 0 0 0 0 1

10001 should have been in TEMP 2 (it was

15470 }
15471 } were correctly accessed
111 }

ILLEGAL ENTRY → 15467 was not executed before 15470
15470 was executed

"A" contained 30213 when illegal entry occured
12525
15466 = address of JAZ vector

SUN JAN 28 | DCS 15465

Clock norm P = 15465

5 = 41077
4 = 1 = 15412
2 = 0
3 = 62323

No strange bids in BIDTAB

Restarted OK at 1061

110 = 59:53 (66323)
526 = 59:52 (66322)

→ DRIVE SETTING REDUCED from 610 → 550

111 = 62321
112 = 62322
113 = 62323

			A
	15455	JAZ	00000
enter either A →	15456	DCS P	
here or here B →	15457	COM A	77777
	15460	STA	TEMP1
	15461	ADD	1

62321 = 15456

ENTRY PROBABLY AT A since COM A would have generated 62321 if 15456 was in Accumulator.

→ Looks like Both P and A were set to 15456 when JAZ was executed. This is difficult to explain

15456 was probably left in a register (Hardware) when JAZ was completed. This may not have been wiped out by C(A) during sequence of COM A, and therefore became effective in the C(A)

SINCE A = 00000 it could have been accessed and added to 15456 and still leave 15456.

→ ∴ LOOKS LIKE CLEAR XR DID NOT WORK DURING COM A

THIS EPLAINS JAN 24 TROUBLES ALSO

JAN 29 DCS 0500 HRS E=0=1

P= 15476

111 = 12525
112 = 1
113 = 12525

A = 12525
4=1 = 75473
2 = 0
5 = 41077
110 = 00:04
526 = 59:52

RESTARTED OKAT
1061

INVOLVED IN CLR X':

	5V*	4R	5T*
	2EB	XGC	GDH
ELEM #	30	17	15

*=Most likely

→ XGC AT 4R replaced by spare

JAN 29 DCS 0800 PM E=1

P= 15475 A = 12525

110 = 59:52
526 = 59:52

111 = 12525
112 = 1
113 = 12525

1 = 75471
4 = 75473
5 = 41077
2 = 0

Restarted OK

→ Orig XGC at 4R put back

→ Spare GDH Put in 5T

JAN 30 HLT ZR = 0 XR = 00001

P = 1226

110 = 00:59
526 = 59:52

111 = 0
112 = 12525
113 = 25252

2 = 77776
1 = 1221
4 = 43356
5 = 42204

NO SCREWEY BIDS IN BIDTABLE

Restarted OK at 1061

→ drive increased to 610

FEB 6 THUR HLT ZR = 60000 XR = 52 0700 hrs

P = 63277

342 = 00:19
526 = 59:52

111 = 0
112 = 12525
113 = 25252

1 = 62063
4 = 63270
2 = 4363
5 = 42112

Restarted 1061 OK
BIDTABLE OK

FEB1 THURS DCS ZR = 35431 2000HRS
XR = 77776

P = 35431

342 = 59:59
526 = 59:52

111 = 25252 OK
112 = 77777 OK
113 = 62352 = 15425

4=1 = 35436
2 = 1067
3 = 62351
5 = 41077

RESTARTED OK AT 1061

→ CLR X did not occur during ESEQOF COM A INSTRUCTION

FEB 2 1900 HLT ZR = 0
XR = 37737

P = 222

342 00:59
526 59:52

111 = 0
112 = 12525
113 = 25252

1 21070
2 1067
4 21070
5 41001

Restarted OK
AT 1061

→ CLOCK SLOWED

Feb 3 HLT 1400hr. did not time in Scelin

P = 1226

526 = 59:59
342 00:59

5 = 42204
4 = 1772
1 = 1216
2 = 1236

Restarted at 1061
Stop at 563 (TURN OFF)
Restarted OK

Feb 3 1805 Hrs

HUNG UP TEMP INDCS LOOP, tha HLT

P = 125

111 = 30213
112 = 10001
113 = 2525

5 = 41077
1=a = 21070
2 = 0

342 = 40031 00:19
526 59:52

9:00 Clock
HLT

FE33

XR = 42074
ZR = 20000

O = 1 E = 0

P = 21660
Z = 1657

111 = 0
112 = 12525
113 = 25252

Restated at 1061

at 1062, there is an ENB; CURENT
1063 SIP, B 0
1064 JMP, B 0

→ Since B = 1657, JMP, B, 0 will go to 1660

HOW DID B get set to 1657?

C(CURENT) = 1067, 515, 576, 555, 1053
1061 1061 1061 1061 1061
2150 1576 1657 1635 2134

→ XR was not cleared during ENB at 1061

~~→ ZEB in Slot 5V (CLR XR drive) was reseted in connector.~~

→ 5V & 5M swapped. If output #30 fails in Slot 5M, Com gate will not open.

→ NORM CLOCK

1:00

DCS

P = 35465

RESTART OK 1061

1 = 35505
2 = 62324
3 = 62323
5 = 41007

392 = 00:07
526 59:52

111 = 62321
112 = 62322
113 = 62323

15456

→ XR NOT CLEARED DURING Com A at 15457 69

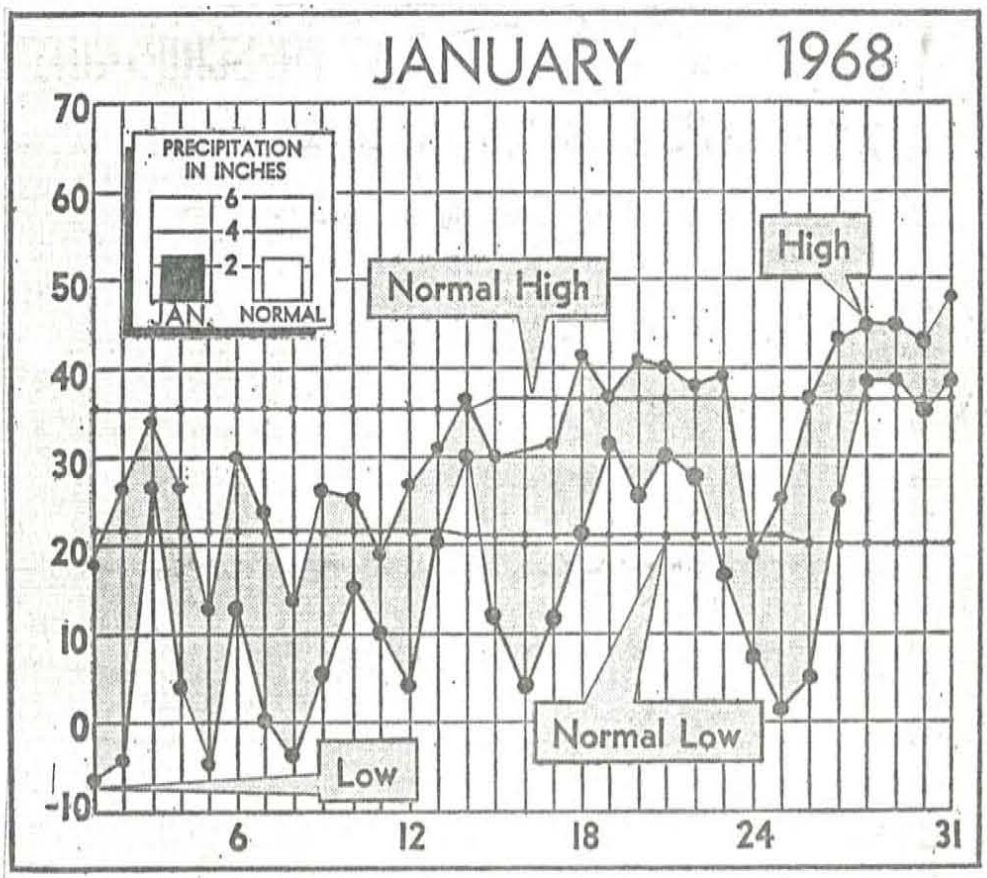
Feb 4 2200hrs Halt P=2 1637

XR= 42074
ZR= 20000
4=1 = 35450
2= 1636
5= 41077
526= 59:52
342= 00:04
111= 0
112= 12525
113= 25252
1636= 1064

bit 5 would not stay set in MAINTENANCE CONTROL

SAME PROBLEM AS FEB 3 2100 hr.

→ XR NOT CLEARED DURING ENB



JANUARY GOT BETTER as the month wore on where the weather was concerned. The mercury dipped to 10 degrees or below on nine of the first 12 days of the month, including four readings below zero. The first and last days provided the low (-7) and high (49) readings of the month. Total precipitation for the month was 2.85 inches, compared to the normal 2.97 for a January here. Contributing to the total was 15.4 inches of snow, which melts down to 1.54 inches of water.

Feb 6 wire replaced from 4R17 — 5V27 (CLR XR)

Feb 7 DCS 1800 HRS

P = 15415 A = 62416

B = 1067

111 = 20267
112 = 62416
113 = 25252

1=4 = 21112

526 = 59:50
342 = 59:55

5 = 41077

→ Restart OK at 1061

PAT = 52525
15406 add
70133

1 1 0 0 0 0 0 1 0 1 1 0 1 1 1 ①
6 | 0 | 2 | 6 | 7

20267 0 1 0 0 0 0 0 1 0 1 1 0 1 1 1
62416 1 1 0 0 1 0 1 0 0 0 0 1 1 1 0

52525
15407 ORED in that. before adg

57527

1 0 1 1 1 1 1 0 1 0 1 0 1 1 1 ①

LSH 1 1 1 1 1 1

3 7 2 5 7

20267
RSH 10133
⊕PAT2 12525
22416

ENA PAT actually entered
A with PAT + XR
∴ XR WAS NOT CLEARED during ENA

71

Feb 7 ~~GATE IN 7F replaced~~

→ 2EB IN 6G replaced with original one removed in NOV 26

→ other 2EB PUT BACK INTO 6G
→ CLR X from 2EB to 15 ff of XR wiring replaced.

Feb 9

LOC 2150 was set = 1064 causing proy to hang-up Shd be 27363

→ CLOCK set high margin

1000 hrs DCS P= 15431 A = 5033

Restarted OK

111 = 7633
112 = 55316
113 = 5034

4=1 = 530
2 = 1067
5 = 1077

$$\begin{array}{r} 15420 \\ 52525 \\ \hline 70145 \end{array} = \overline{07632}$$

→ during ENA, XR WAS NOT CLEARED

→ NEW WIRE INSTALLED FROM 4R16 — 5T15 (Schem 7)

1700 HRS DCS P= 15415 B= 1067

111 = 60267
112 = 62416 = A
113 = 25252

$$\begin{array}{r} 52525 \\ 15406 \\ \hline 70133 \end{array}$$

1	1	0	0	0	0	1	0	1	1	0	1	1
	6		0		2		1		6		7	

→ XR still not cleared duri ENA

→ XGC IN 4R replaced ← — — STARTED ALL THE P=0 Prob.

→ CLR XR PULSE LENGTHENED TO LAST ENTIRE E SEQ

Feb 12 HLT A lost

P = 20022 B = 1067 4=1 = 20001 5=41077

111 = 77777
112 = 77777
113 = 00000

526 = 59:52
342 = 59:53

NO Bad bids

Location 20 = 1064
21 = 1

Restarted at 1061 OK

Feb 12 HLT XR = 41205

P = 20002

111 = 0
112 = 12525
113 = 25252

B = 2
4=1 = 35412
5 = 41077

526 = 59:52
342 = 00:04

CLOCK was not inc properly Loc 710 had been changed to 17777 ← 5 ∴ bit 1 was picked up.

Feb 22 bit 1 solidly picked up in low bay when more than 13 ones were in the word.

→ DRIVE setting was reduced to 400 (34 Volts cold start 20°C
33 Volts at 30°C.
1 Volt / 10°C

Feb 26 HLT at 1:00 PM

XR = 12525 OV = 1

ZR = 60000 EXECUTE SEQ

AD = 72525

P = 60002

111 = 12525
112 = 12525
113 = 0

2 = 00000
1=4 = 35456
5 = 41087

526 = 59:52
342 = 00:06

56 = 0

Restarted OK at 1061

FEB 27 HLT AT 12 Midnite

XR = 00000

ZR = 60000 OV = 1

AD = 60000

P = 60002

2 = 00000
4=1 = 35446 46 = 0
5 = 41087

111 = 77777
112 = !
113 = 0

526 = 59:52
342 = 00:04

Restarted OK at 1061

TEST 8 has 111, 112, 113 set as above

JAZ 15466 is at loc 15465

→ CLOCK SET SLOW MARGIN TO TEST GATING

Feb 29 HLT after changing HRS to 0700

XR = 53611 EEOV = 0

ZR = 00002

P = 00022 21 = 00001

526 = 59:52
342 = 00:03

4:1 = 75463

111 = 0 2 = 1067
112 = 12525 5 = 41077
113 = 25252

→ Restarted OK, SYNC DISABLED

FEB 29 HLT after changing HRS to 1100

AD = 41531 OV = 1
XR = 21531

ZR = 20000 4:1 = 557

P = 20563 2 = 555

526 = 44:45 5 = 40077
342 = 06:20

NOT LOGGED SINCE SYNC WAS NOT RUNNING

100 = 21531 (59)

111 = 0
112 = 12525
113 = 25252

UNLOCKED AT 45:13
OFF AT 46:01
} CKB PRINTOUT

720Ω shunt – 500Ω series

Temperature sensitive resistor = 1000Ω when temp = 35°C

	TEMP	V	SETTING	
	30°C	34.0	340	too low for loc 11774 to be read 37777
SET AT 1730 hrs Apr 13 →	35°C	35.0	420	
	28°C	36.5	420	

APRIL 14 Midnight HLT

ZR = 0 5 = 41077

VR = 231 Z = 1067

P = 00001

121 = 15723 (JMP i ENTRY)

111 = 77777

112 = 00000

APRIL 14 1600 hrs. DCS DRIVE = 35.2 volts

ZR = 75777

111 = 77777

112 = ~~40333~~ 00000

121 = 15723

Loc 1900 was cleared manual

Reboot stepped and restarted OK

Apr 14 2000hrs. HLT

ZR = 0
XR = 231

111 = 77777
112 = 00000
121 = 15723

P = 00001

10000 = 0
1 = 0

restarted at 1001

→ Chan 0 input buffer card removed

2300 hrs HLT

ZR = 0
XR = 40001

111 = 77777
112 = 00000
113 = 15723

P = 00001
1000 = 0
1 = 0

→ Chan 0 input buffer put back

APR 15 1000 HRS HLT

ZR = 0
XR = 00062

121 = 15723
111 = 112 OK

P = 00001
1000 = 0
17777 = 16414
5 = 41077
2 = 1067

After running 3 hrs Temp = 41°C, V_{drive} = 34.2

→ XKA INST DECODE & CHAN 0 removed temp. replaced

APRIL 15 1500 HRS HLT

ZR = 00000
XR = 40061
AD = 40001

111 } OK
112 }
121 = 15723

P = 00001
1000 = 0
17777 = 0
5 = 41077
2 = 1067

→ XGC in Location OJ replaced since it grounds $\overline{INP}$

APRIL 16 0600 HRS HLT V_d = 75.5

ZR = 0000
XR = 00227
AD = 00227

111 = 77777
112 = 10000
121 = 15723

P = 11701
1000 = 0
17777 = 0
5 = 41077
2 = 1067

11700 = 0000
1114 = 15700

→ Restarted OK at 15700

→ CHAN 0 buffer still removed

April 16 1000 HRS HLT off Seq Step off.

ZR = 00000
XR = 00000
AD = 00000

All other lights off except seq

P = 00001
5 = 41077
2 = 1067

→ XGG (Unload DA gate) in slot 1F replaced

→ CHAN 0 Gate put back in

APRIL 17 0300 hrs. HLT

ZR=0
XR=6

P=00001

ALL AS BEFORE

T= 35°C V_D= 35.0V

0600 HLT P=00001

ZR=00000
XR=26351 59:69

AAB
Next time, read Time OFF

April 17 1600 hrs HLT

ZR 00000
XR 00040
AD 00040

TR. 5 on

P= 16764
Z= 1067
5= 4.1077
AAB

TIME OFF (342) = 10:28
↑
Bit 11

15700 + 1064

restarted ok at 1067 → failed to CLR ZR in step 0 of P sequence

April 17 1900 HLT stopped right after inc clock

ZR= 40000
XR= 00000

P= 1516
AAB

1115
537
1654

April 17 2230: orig OJ card ⟹ 4R (XGC)

APRIL 17 MIDNITE HLT start 00:40

ZR = 0 P = 00001
XR = 26237
AAB

→ TRIAL OF XGD IN SLOT OK } CLR Z
→ XGC " " OM }

0300 hrs. HLT

ZR = 0 P = 00001
XR = 77777

121 = 15705

112 = 0 111 = 77777

JAZ WENT TO 77777+1 when XR contained 77777
ac ≠ 0

→ GHH IN LOC 5G replaced.

→ ORIG XGD put back in slot OK
→ ORIG XGC put back in slot OM

April 18 0800 hrs. HLT

ZR 00000 TR, 5 on P = 00001
XR 77777 Seg E on
AD 77777 old.

111 & 112 OK
121 = 15703

APRIL 19 0700 hrs HLT

ZR = 0
XR = 0

P = 11722
121 = (15716)

→ ZR UNLOAD GATE BIT 11 bad

ORIG OR gate Trial in AN (UNLOAD ZR)

April 19 0800 hrs HLT

ZR = 0
XR = 0
AD = 0

P = 00001
AAB

STARTED AT 1061 OK Loc 1 CLEARED OUT

2000 hrs. HLT

ZR & XR = 0

P = 00001
111 & 112 OK
121 = (15707)

TEMP = 39°C

APRIL 20 SAT AFTERNOON — WIRED IN RELAY TO DISABLE -24V to computer if 115VAC to fans is OFF

Temp = 35°C

WIRED -24V low voltage checker in to test at 0, .9V, 1.8V, 2.7V down from normal 24 volts.

Part of interrupt rec was clobbered when -12AV was accidentally shorted

Changed data couplers on all 15 bits of MDR so machine would run on reduced voltage and all clock speeds.

APR 23 2200 hrs HLT after latch, before clock was incremented (75 hours)

ZR = 0
XR = 66130

P = 00001
AAB

B = 1067
5 = 41077

STARTED OK AT 1061

1 (101) (1000) (101) (1000)

→ ~~A5 IF SEAL ON DIODE WORK~~

APRIL 24 1000 hrs HLT

ZR = 00000
XR = 77777
AD = 77777

P = 00001

Tr 5 on Seq E on

B = 1067
5 = 41077

111 = 77777
112 = 0
121 = 15705

Restarted OK

→ GHH (TRIAL) MOVED FROM 5G to 1V
→ orig GHH put back in 5G

APRIL 25 Midnite HLT

ZR, XR, AD = 0

P = 15715 BIT 11 dropped
121 = 15713

Restat OK

APRIL 25 0100 HLT
ZR = 0
XR = 77777

P = 00001
121 = 15703

THAT'S A STA INSTRUCTION

4/25 0700 HRS
→ ORIG XKA in 6L PUT BACK IN

APRIL 25 1600hrs HLT

XR = 22131
ZR = 0

P = 11701
121 = 15723

~~GHH IN 7C replaced by TRIAL GHHH~~ This is to fix I sequence trouble noted when -24 was lowered by 10%

~~GAH IN 6T replaced by TRIAL GAH (I Seq)~~

→ GHH IN 7D replaced by TRIAL GHH (this element sets I Seq at 50 and 55 time)

APRIL 26 0700 HRS HLT (did not increment hours. did Latch on

ZR = 0
XR = 62131

P = 10701 BIT 11
121 = 15723

restarted at 15700 OK

April 26 800 hrs HLT

ZR = 0 0 0 0 0
XR = 7 7 7 7 7
AD = 7 7 7 7 7

P = 00001
TR 5
AAB

Restarted OK

APRIL 29 0400 HRS HLT

ZR XR = 0

P = 11711
121 = 11711
111 = 77777
112 = 0

→ XGB IN 4C Replaced (unload AD)

April 29 0900 HLT

XR ?????
AD ?????

P = 00001

121 = 15705

2100 HRS HLT (after inc HRS)

ZR = 0
XR = 77777

P = 00001

121 = 15703

TEST PROG CHANGED SO THAT 77775 instead of 7777 is used for test pattern

APR 30 0500 HRS HLT

ZR = 0
XR = 0

P = 00001

121 = 15707 (EOR)
111 = 77775
112 = 00000

7777$_0$, 7777, 4, 1 SNI = 0

NEW PROG

APRIL 3 2200 HRS HLT

ZR = 60000
XR = 77775

P = 60001

121 = 75705 (JAZ NOT TAKEN)
A = 77775
111 = 77775

7777$_6$, 1 SNI 0

→ 2EB IN 5V REPLACED TEMP

HLT

ZR 20000
XR 42453
AB 62453

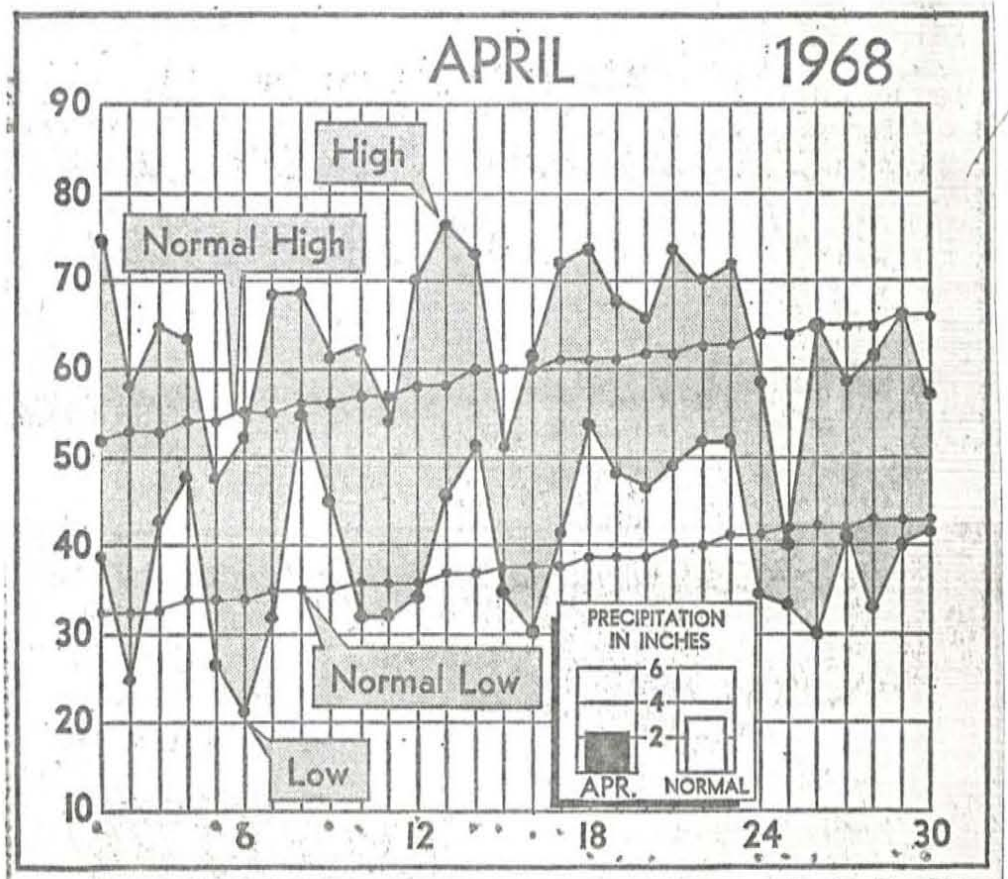
P = 20001
121 = 35707 (ENA TEMP 2)
111 = 77775
77776 f1 = 0

1900 hrs.

HLT

ZR = 20000
XR = 77775

P = 20001
121 = 35705 (JAZ NOT TAKEN)
111 = 77775



APRIL SHOWERS DIDN'T COME OUR WAY the way they normally do. The Pittsburgh precipitation was 2.27 inches last month compared to the usual 3.08 inches. A low of 21 degrees was reached on April 6 and a high of 77 April 13.

MAY 2 0200 HALT

ZR=20001 P=26001
XR=270 121=35717 (JAZ i 15700)

→ ORIN 2EB IN 5V PUT BACK

May 2 0900 HLT

ZR = 20000 P= 20001
XR = 77775
AD = 17776

→ 1800 HRS. GDH IN 4L replaced by BLACK SPARE
RAN OK 20 MINUTE CONTINUOUS TEST

2200 HRS HLT

ZR = 20000 P= 20001
XR = 20507 121 = 35711 (ADD)

→ XGD IN 7P replaced

May 3 1400 HRS HLT

XR = 20000 P= 20001
ZR = 40051 121 = 35717 (JAZ i 15700)
AD = 60051

→ 1V (GHH) & 1R (GDH) replaced

APRIL 3 2000 HRS HLT

Z = 20000 P = 20001
X = 11514 121 = 35711

→ 2PD Card in loc 1D replaced
→ XGD 1C replaced

2100 HRS HLT
P = 20001
Z = 20000 121 = 35715 (ENA POWER)
X = 13534

1200 mid HLT

ZR 20000 P = 20001
XR = 66063 121 = 35711

MAY 7 HLT 1800 HRS P = 20001

ZR = 20000
XR = 0 121 = 35717

→ TRANS OF AD ⇒ TR timing changed
→ 5.1K PULL-up added to MEM START SINCE 3 times, the system stopped when scope probe was hooked to MEM START.
NOTICED THAT 100-Ω additional parallel load resistance to -12V on START gave -4V pulse

→ STILL ON FAST MARGIN

May 8 1100 HLT

ZR 20000 TRunk 5 13 on
XR 40262
AD 60262

MAY 8 2200

→ SLOWED TO NORM

→ GNDED PANELS IN A&C UNIT

→ ADDED 100Ω pullup to IDD in ID

MAY 9 MIDNITE HLT P= 35720
121 = 75715
111 = 77775

MAY 9 0500 HLT SAME AS MIDNITE, ZR & XR = 60000 00000

→ ORIG IDD (without 100Ω pullup added) put back in to SAT ID

0600 HLT

ZR = 20000
XR = 77776

P = 20000
121 = 35705

10000 was 7777, so it was CLRED to 00000

5/9 1900 HLT

XR = 6531
ZR = 20000

P = 563
121 = 35717
2 = 555
5 = 41077
1 = 0

5/10 0300 HLT
XR = 6260
ZR = 20000

P = 20000
121 = 15711

MAIN 0200 hrs HLT P = 20001

ZR = 20000
XR = 77776

121 = 35703
111 = 77775
2 = 1067
5 = 41077
17777, 17776, 1 still = 0

→ Loc 4 wired so that it saves P during INT INSTEAD OF 1

Prog changed. COPY TAPE, STOP COPY WORKS
CONTROL KB WORKS.
Original CONF prog reinstated

~~TEMP running on the spare 200 since primary 200 was ZAPPED during probe tests~~ (REPAIRED AND REINSTALLED PRIME)

→ WRITE A & WRITE B ON SCHEME 2 WERE enabled at S3 · $\overline{S5}$ instead of S3 · $\overline{S4}$

YET TO DO:

1. Add relay to SEQ STEP so MACH will TURN OFF AUTOMATICALLY WHEN HLT executed.
2. TEST OUT A set of BS modules (BLACK SPARES)

MAIN 1300 hr HLT P = 60001

ZR = 60000
XR = 00000

111 = 77777
112 = 00001
113 = 60000

Restarted OK at 1061

342 = 59:56

→ Loc 15465 JAZ seemed to GO TO Loc Zero

2300 hrs HLT P = 20001

ZR = 20000
XR = 25252

2 = 0
1 = 0
5 = 41077

111 = 12525
112 = 12525
113 = 25252

342 = 59:59

→ 2 extra diode added to TDA card in memory slot 6

MA413 0500 HRS HLT P=00001

→ CLOCK INCREASED TO FAST

→ GAH's in 6S and 6V replaced since HP was not being set

FIXED Illegal stop at 00001

→ Put recovery prog at Loc 16, 17 which records number of P=0 errors in loc 15 and then recovers the exec at 1061

DCS STOP P= 75476

A= 00000

T= 39°C

111 = PAT2
112 = PAT2
113 = LS PAT2

→ CLOCK SLOWED DOWN

WHEN +4V BIAS IS REDUCED BY 10% IN MEMORY

DCS stop P= 75427

A= 7 ← BIT 3 dropped

111 = 25242
112 = 77767
113 = 00010

Loc 21 was = (1001
115 (NELEKA) = 00010 instead of 77777

Black Space removed from loc 4L. 4L ⇐ IR ⇐ ORIG IR

XGB in OS ⇐ ORIG 4C

SAT MAY 18 only IV and 7G GIH's put back where they belong. BS ⇐ 7G ⇐ IV ⇐ ORIG
BS was placed into plastic bag for storage.

FRI · MAY 24 Clock stopped at 12 NOON
CCO turnon set 59 min after hour OK

526 = 59:52
342 = 00:59

BIDDING TABLE OK
1053, 555 1067

111 = 0
112 = 12525
113 = 25252
2 = 555.
5 = 41001
4 = 565
15 = 77777

→ AS IF BID COUNT GOT OUT OF STEP

→ Probably due to AC power outage while running

SAT MAY 25 Added two new power control features.

1. If hangup is encountered, MACH will now turn off power and not turn back off
2. OUT on Channel 7 once each SYNC period causes the KEEPGON circuit to perform.
3. If AC power fails during time mach is on, it will set lockout bistable and will not restart until manually bistable is reset.

Wed May 29 DCS + AUTO off

ZR 85431
XR 77776
AD 77777
TR 77611

SK 0+1 on
MR 4 on
seq. PF E

Only all on
tests 543 fault 210

A = 77777 P = 35431
111 = 25253 (LSH PAT) or PAT+1
112 = 77776
113 = 00001

Machine had been set to run only 15 sec since MONDAY NITE (MAY 27)

→ bit Zero of unit 115 was DROPPED

→ DRIVE INCREASED TO 500

JUNE 2 0200 SUN DCS P = 15431
A = 40000
5 = 41077

111 = 65253
112 = 37776
113 = 40091

115 = 37776 instead of 77777

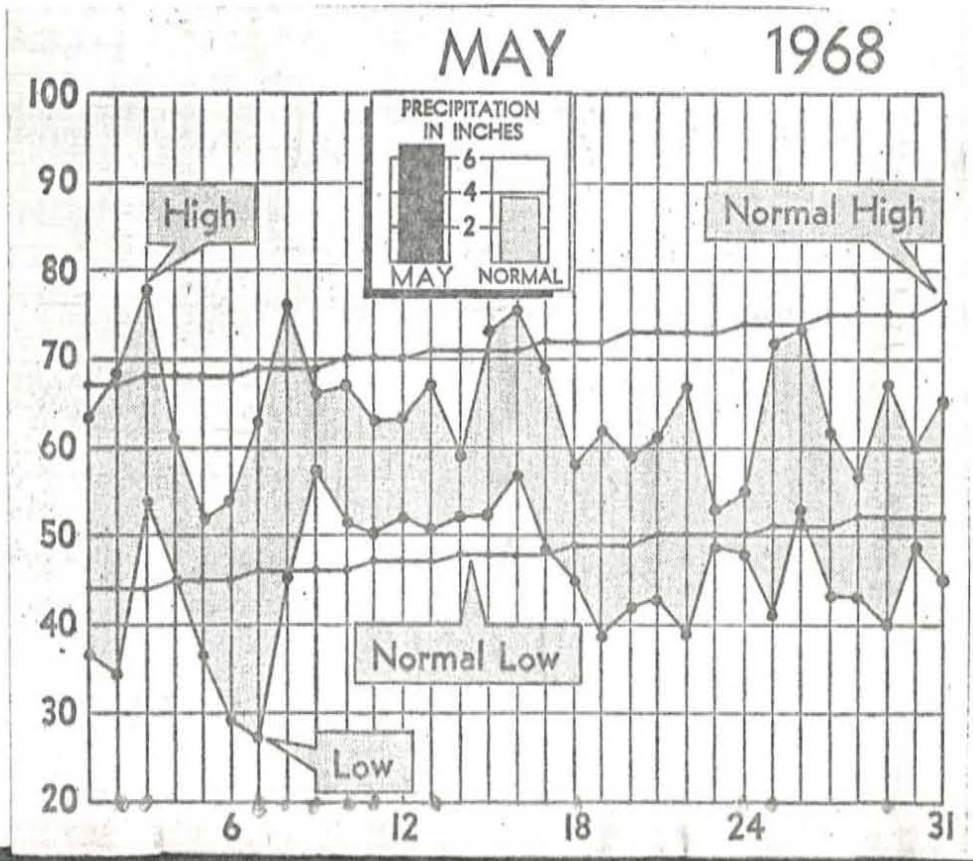
10115 = 37777

After 2 hours of running Temp = 38.5°C

V drive = 35.8 Volts (setting of 500)

→ V drive increased 36.5 (setting 550)

Shift this - Both crew SD [illegible]



June 12 0900 HRS Marlin clobbered several locations
Turned off with ALL HOUR LIGHTS ON.

→ Mem DRIVE increased to 600 (37.0 V)

JUNE 20 0135 HRS DCS 15417

111 = 21253
112 = 02000
113 = 25252

114 = 0
115 = 77777

2 = 1067
5 = 41077

10000 = 0

RestrAd OK at 15400

→ BIT 10 WAS dropped UP either in 10 ENA, 10→11 LSH, or 11 STA

JUNE 22 SAT 1600 HRS P = 15434

A = 1777
B = 1067
5 = 41077

111 = 27252 LPAT2
112 = 75777
113 = 02000

→ Bit 10 was dropped in ENA, at loc 15421

ENA PAT	52525
EOR NEGZRO	77777
STA TEMP1	25252
EOR PAT	177777
STA TEMP2	77777
Comp A	00000
STA TEMP3	00000
DCS A	77776

27252

JUNE 23 Sun 0900 hrs

526 = 59:52
342 = 59:52

114 = 0
115 = 77777

P = 15476
A = 12525

111 = 12525 PAT2
112 = 1
113 = 12525 PAT2

2 = 0
5 = 41077

Restrt OK

June 24 - Monday

→ IN BIT 10, BLACK SPARES PUT INTO [3H & 2V], this leaves (4C), (3M), [2E, & 2F] ← Replaced 9/6/68 THIS CURED BIT 10 Being dropped 6/22 ? 9/4/68 No 9/19/68

Replaced 9/19/68 July 6 - Sat ← replaced 9/4/68

[3H] Black Spare replaced by original GDH removed on June 24.

Originals to be restored in original Slots

1XGD	1C	April 23, 68
XGG	1F	April 16. 68
2DD	1C	April 23, 68

July 8 MON - DCS P STOP

P = 15431

111 = 272252

BIT 10

3H WAS THE DEFECTIVE CARD (GDH)

Black Spare GHH removed fm 2V & orig GHH put BACK

GDH Removed fm 3H & replaced by Black Spare.

ETHER adpt 7, 11, 15, 19 bad.

July 9 TUES 12 Midnight DCS Stop

P = 15431

111 = 25252 A = 1777

112 = 75777

113 = 0 342 = 00:07 SEC

2V BLACK SPARE PUT BACK

FAST CLOCK

July 10 DCS + auto off

TR 77677
ZR 35467
XR 77777
AD 77777

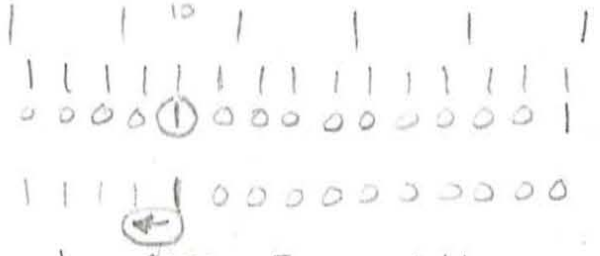
Seg PFE on
SK 1+3 on
I4 4 on
Clock all on

342 = 00:14

P = 15466

A = 76001

111 = 77777
112 = 76000
113 = 76001



1. CARRY from 10 → 11 missing or bit 10 dropped when 77777 → Z or X

July 12 DCS

P = 1552D

111 = 0
112 = 12525
113 = 25252

A = 35516 = B

5 = 41077

MEM AMBIENT = 40 °C

P = 15455

342 = 00:59

111 = 77777
112 = 0
113 = 0
B = A = 0

With FAST CLOCK, JA2 NOT taking Jump when A = 0

HAPPENED AGAIN SAME WAY AT 0800 (FAST CLOCK)

CLOCK NORM

SAT Jul 13 No start at 2100 hrs

P = 2410
A = 0
5 = 21205
4 = 21070
2 = 5
342 = 00:59
100 = 50376

111 = 0
112 = 12525
113 = 25252

Restarted OK after about 8 starts

Low Block → UP
← BACK OK

P = 13516
A = 0
B = 15
5 = 21205
4 = 15410

111 = 52525
112 = 65252
113 = 25252

Restarted OK

KEEP RELAY CONTACTS Temp Sensor with wire jumper

PWR CONTROL CIRCUIT MODIFIED [illegible] OK

Thurs Jul, 18 No start at 0700 hrs

P = 15412
A = 25253

111 = 25253
112 = 65252
113 = 25252
342 = 59:52
100 = 6376

Bootstrap OK
Temp = 31°C

T. July 13 [illegible] / AT 1200

P = 527
A = 26323

140 = 213[illegible]
111 = 0
112 = 12525
113 = 25252

342 = 59:59

Restarted OK
TEMP = 32.5°C

SAT July 20, did not start at 0600.
tried to start at 7, & 8

P = 16
5 = 0
2 = 0
4 = 414

EVERYTHING IN MEMORY PRETTY WELL CLEARED

TUES July 30 2000 hrs
P: 15431

A = 51544

5 = 41077
Z = 1067

111 = 25252
112 = 26232
113 = 51545

Restarted OK at 15400

342 = 00:59
100 = 47576

Aug 11 sys stop [illegible]
ZR 20000
ZR 01[illegible]
AD 21001

HLT off

P: 20001 (Loc 0

342 = 59:59
526 = 50:52

111 = 0
112 = 12525
113 = 25252

(DEF INT TO 650) → Bit 5 dropped in Loc 574

Loc 575 = 41604 ~~SH 1774~~

SH 41766

bits 6, 5, 4, 1 dr[illegible]

AUG 22 0300 HLT

XR = 0
ZR = 20000
P = 1133
[illegible] = 15

111 = 77777
112 = 77777
113 = 00000

4 = 15446
5 = 41004

Ro[illegible] [illegible] at 1133 OK

342 = 0059

HLT [illegible] spurious, [illegible]
[illegible] set

AUG 25 SUN 0600 HLT P = 1050

XR = 77777
ZR = 20000

5 = 41077
2 = 1047

111 = 00000
112 = 12525
113 = 25252

CURCHI ([illegible] 1047)
WAS 21064 AS IF A BID HAD BEEN PLACED
FOR [illegible] INSTEAD OF i CURCHI BID TABLE
did not CONTAIN 1047. NO OTHER LOCATIONS
WERE CLOBBERED

COLD DAY

AUG 26 did not come on at 10:00

P = 26 then 0000

→ DRIVE VOLTAGE IS ONLY 30.00 Volts

→ loc 1274 was altered unexplainably by losing bit 0

2:00 pm Sept 4 HLT off sg off

ZR 00001
X 1 40222
AD 40223

probe Sg step
Man T L
Turn off

P = 2 when turned ON at 1800 hrs. Mem power OK

111 = 0
112 = 12525
113 = 25252

342 = 00:21

Loc 3163 in bid table = 00001
which was CURCNT :. Imped to 00002

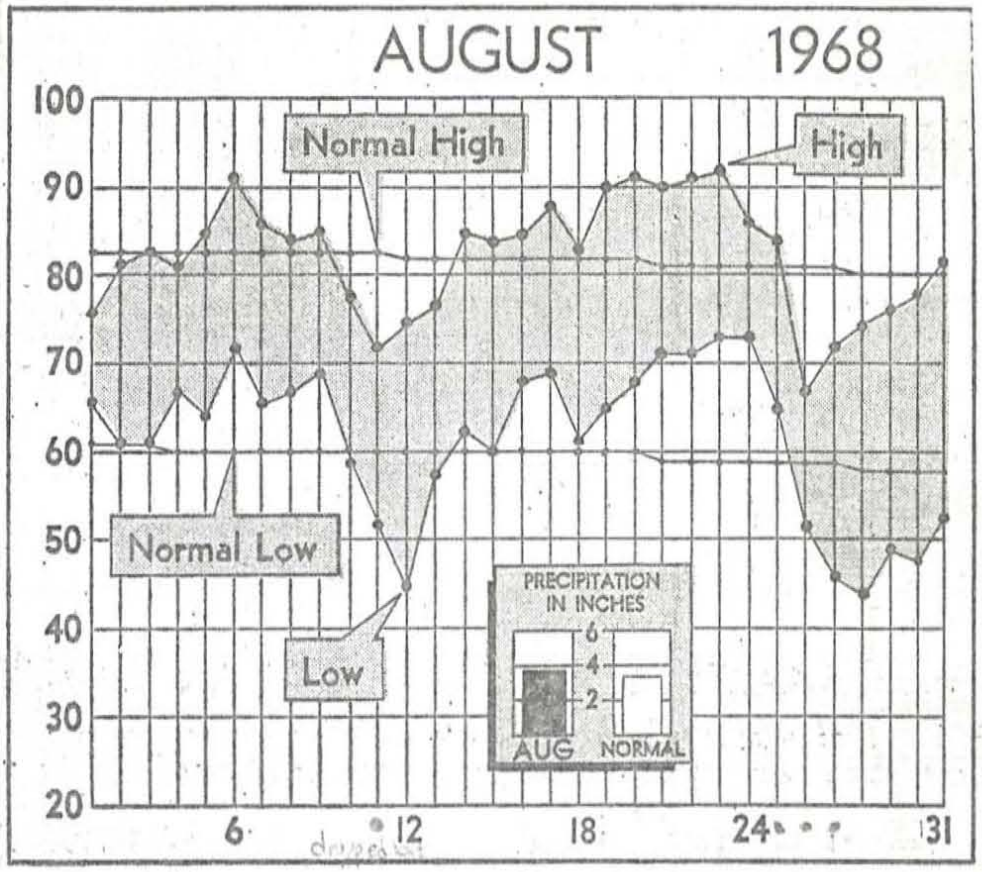
Sept 6 DCS P 15431

111 = 37252
112 = 75777
113 = 02000

A = 1777

BIT 9 picked up during EOR.

2E & 2F REPLACED



ENDING ON A PLEASANT NOTE. August had more than its share of heat and humidity as the mercury reached 80 degrees or above on 21 days and climbed above 90 six days. But all the misery was offset last week by cool nights and warm, dry days as an Aug. 27 record low of 46 was set and the Aug. 28 record low of 44 equalled. A shade of under four inches of rain fell, compared to a normal 3.31 inches for August.

Sept 4 DCS P 15431 A = 1777

111 = 27252
112 = 75777
113 = 02006

BIT 10 Picked up when NEZERO ⊕ PAT
WOULD BE DROPPED WHEN ENTERING NEW.

~~ORIG 2V PUT IN BACK AND BLACK SPARE GIVEN~~
~~PUT INTO SLOT~~ 2J

BLACK SPARE PUT INTO 3M original 3H put back

Sept 9 ZR 66401
AR 77777 [illegible]
AC 7[illegible]

Auto [illegible] DCS [illegible]
PF [illegible] in Seg [illegible]

A = 57775   P = 15416

342 = 00:21   111 = 25253
112 = 0
113 = 75252

Restarted OK at 15400

→ Memory seems OK

→ "A" should have been Zero since 112 = 00000

Sep 13 ZR 60000
AR 77777
AD 60000

HLT & Seq Stop off

P = 66411

B = 76   5 = 41077
4 = 543
111 = 0
112 = 12525
113 = 25252

342 = 00:01

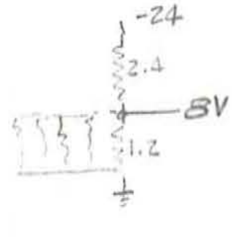
→ BIT 2 was dropped in Loc 1061 and 1062

1401 lost bits 2 & 3

→ LIGHT BULB PLACED IN MEM CAB

SAT SEPT 14

I SEQ & F SEQ ARE NOT STAYING CLEARED during auto restart if AUTO allowed to come on. SEQ STEP was forced to ground by probe, and F does not come on spuriously. If the I connection to pin 7M4 is removed, F comes on, if I is left connected to 7M4, then I comes on.



A CLAMPING DIODE (429) WAS INSTALLED on "MC" to prevent it going positive during startup transients.

STARTS OK NOW. → LAMP STILL IN MEM

Mon Sept 16 0500 hrs DCS P=15431

A = 52524 = PAT-1
B = 1067
5 = 41077

111 = 25252 = $\overline{PAT}$
112 = 25252 = $\overline{PAT}$
113 = 52525 = PAT-1

342 = 55152
100 = (01)376

→ Restarted at 15400 OK
MACHINE CLOCK SLOW set

→ EOR AT 15424 did NOT PRODUCE NEZERO FROM PAT ⊕ $\overline{PAT}$. $\overline{PAT}$ resulted and was stored in Temp2 (112)

EOR AT 15422 Did work correctly since PAT ⊕ NEZERO = $\overline{PAT}$ stored at Temp1

Thurs Sept 19 0100 HRS DCS P= 15431

A= 1777

111 = 25252
112 = 75777
113 = 02000

All this while running on SLOW clock, and no interrupt

Bit 10

CLOCK put in NORM, NO INTERRUPT

XGB IN 4C replaced temp by RED spare until 4C can be repaired (more likely 17 will be replaced)

(Red spare had previously thought to be bad bit 8)

IF THIS WORKS, then BLACK spare in 3M can be relieved (9/4/68)

Thurs Sept 19 0800 HRS

→ ORIG "4C" card repaired (Bit 10) to be replaced in slot 4C

SAT SEPT 21 DCS 15406

A = 65252

JOV NOT EXECUTED

111 = 52525
112 = 45252
Should be 6

RSH dropped Bit 19 → 18

Sept 21 HLT XR = 00000
ZR = 20001
OV = 1

P = 20002 Loc 1 = 0

111 = 00000
112 = 12525
113 = 25252

→ Mem Drive reduced to 6,00

MACHINE DON'T TURN OFF AT 10:00 (Loc 764 = 64331
Should be 40200)

→ Cable 4C changed (XGB)

SUN Sept 22 DCS 15517

111 = 00000
112 = 12525
113 = 25252

A = 20000
B = 00001
1 = 00000
15400 = 00000

MEM TEMP = 110

SUN 9/22 NO STARTUP AT 0900 P = 20563

→ SYNC REMOVED

→ 4C & 4E SWAPPED

SUN SEPT 22 MEMORY POWER SUPPLY WENT OFF (RED) after changing clocks to 1300 hrs. Plus about 1 min'ste of operation

CONTACTS Cleaned on K101, RC protective circuit resoldered on K101, K104

FUZE Socket F102 burnished to prevent intermittent

MON SEPT 23 DID NOT COME ON AFTER 1300 hrs

CCO TURN ON MUST HAVE BEEN ALTERED

P = 15517

MUST HAVE HUNG UP ON JAZ (A=0) at loc 15517 at 0400 before changing cco or cco did not seal in. Mem Power supply may have failed at that time.

→ Bootstrapped and restarted

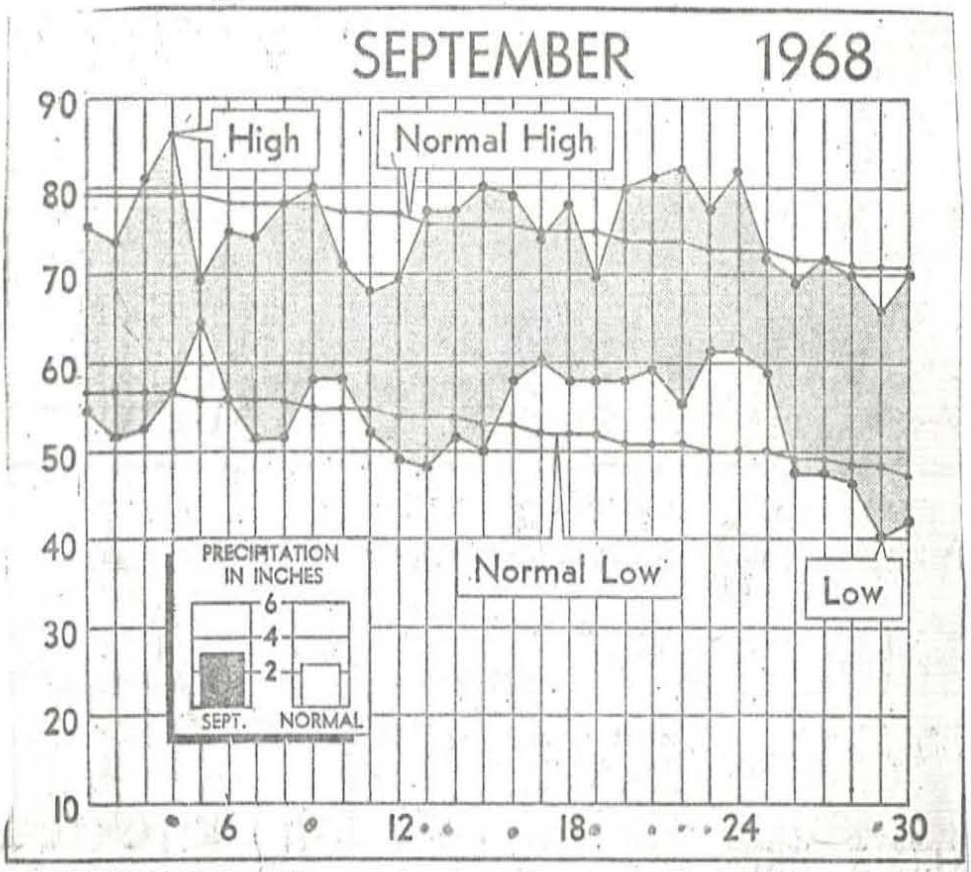
SUN Sept 29 MACH OFF via 1544.

342 = 59:52 TURNON = 59:52

111 = 00001 A = 0
112 = 77777 2 = 1067
113 = 00000 5 = 41077

OFF Loc 15432

→ TROUBLE CAUSED BY THE KEEPGON Relay not staying energized



A PLEASANT SEPTEMBER was enjoyed, weatherwise, by Pittsburghers as temperatures ranged generally from the lows in the 50s to highs in the 70s and 80s. The mercury hit a high of 86 on Sept. 4 and dipped to a low of 40 on Sunday. Rainfall totalled 3.08 inches, compared to a normal 2.54 inches for September.

OCT 2

auto DCS off

ZR 35431
XR 77776
AD 77777

Check trunk on

P = 15431

111 = 27252
112 = 75777
113 = 02000
342 = _____
526 = 59:52

A = 76000

Bit 10 Picked up during EPR

Loc				
15421	ENA	PAT	change to	ENA NEZERO
15422	EPR	NEZERO		EPR PAT

Oct 3 1800 hr.

→ Bit 9 was picked up in loc 100 which made clock set to 7:00 instead of 6:00 at 6:00 explained by following (clock increment twice once at 00:00 and once at 00:40

1900 hr.

→ EDR 00100 with 0000 produced Zero (explained by following)

→ OP code $16_8 \Rightarrow 14_8$ when bit 10 was dropped this made EDR become STA and loc 762 in clock prog was altered.

→ XGG IN loc 1F changed (unload DA gate)

→ MEM CAB HTR THERMOSTAT SET AT 70°

OCT 5 HLT P= 21 Bit 2 dropped at loc 3173 Bid

XR= 66123 5= 41077

ZR= 20000

OCT 6 HLT

ZR= 20000 P= 20002

XR= 00000 5= 41077

111= 00000 113= 21252

112= 10525

FF-E Serial # 490 removed fm
Bit 10 slot of DATA REG IN MEM

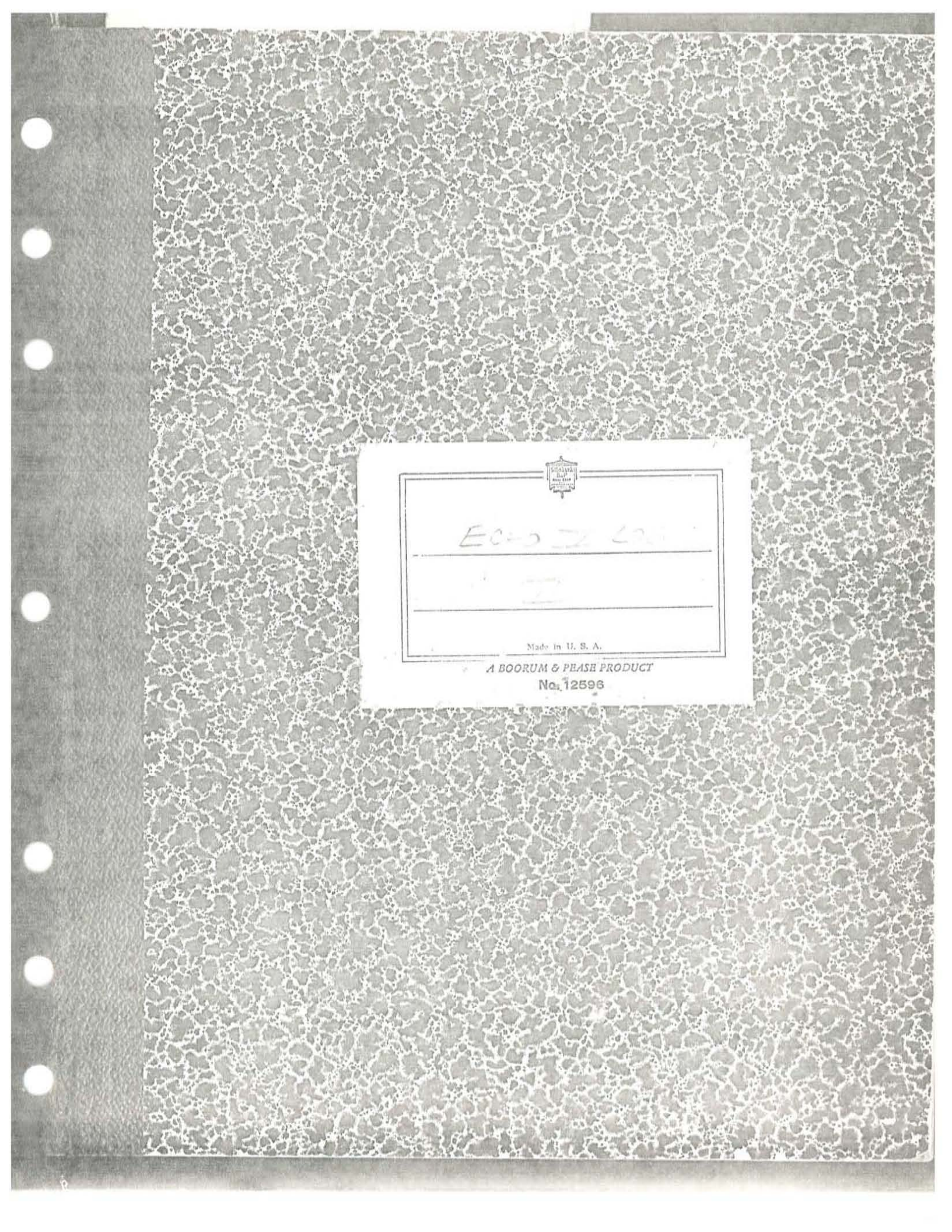
THIS BOOK CLOSED 10/19/68

PROG TO PRINT OUT CHAR
(ASSUME TYPER ALREADY TURNED ON)

```
17001   ENBi CHAR          46405
    2   ENA  TABL, B       27500
    3   OUT  TYPER         10000
    4   JMPi RET           41406
    5        CHAR          17575
    6        Time check    17577
```

TABL

```
17100   000000          17140   000000
    1        3              1       15
    2       31              2       21
    3       16              3        0
    4       11              4       11
    5       01              5        0
    6       15              6       32
    7       32              7        2
   10       24             50       13
    1        6              1       17
    2       13              2       22
    3       17              3        0
    4       22              4       14
    5       34              5        3
    6       14              6       34
    7       30              7       35
   20       26             60       26
    1       27              1       27
    2       12              2       23
    3        5              3        1
    4       20              4       12
    5        7              5       20
    6       36              6       25
    7       23              7        7
   30       35             70        6
    1       25              1       30
    2       21              2       16
    3       36              3  ON    0
    4        4              4  Line fees  2
=   5  FIG  33         TAB  5  OFF  40
BS  6  LETR 37         ¢    6       0
120 7       10              7       31
```


Made in U. S. A.
A BOORUM & PEASE PRODUCT
No. 12596

OCT 19, 1980 – Saturday

New Power Cont. Pnl installed in Cabinet 4. Has option for either running MF logic continuously or on-off with memory. Power input to DC supply changed from 220 to 120. This should work for up to 30 Amps DC output.

Yet to do:

done 1. Reconnect memory fans to memory power

done 2. Put longer plug on maintenance panel AC power cord so that it can reach to memory blower receptacle.

done 3. Build quieter blower assembly for cabinet 4 using Boxer (66 CFM)

4. Build blower assembly for cabinet #3 using 2 boxer fans.

5. Exhaust cabinets 1 & 2 into house cold air return.

6. Build baffles around memory blower assemblies to prevent air leakage.

Drive Set at 5.00 = 37 Volts. Temp: 78°F

HLT 10/25/68 FRIDAY MIDNITE

ZR = 20000

XR = 00000

P = 20005

5 = 0

111 = 0

112 = 10525 (2) BIT 10 dropped

113 = 17252 (5)

342 = 00:37

drive increased to 6,00

HLT 10/28 Mon Morn 0730 hrs

XGF in Loc 1H had bad bit 3, replaced

restarted by bootstrapping

HLT 10/29 TUES NIGHT 2300 hrs

BIT 10

ZR = 20000

XR = 0

P = 20005

111 = 75777

112 = 10525

113 = 21252

Card in memory data pack bit 0-1 swapped with 2-3
dropping solidly when margin -4.6 & +4V low
with -24V +24 High

after swap, bit 2 still drops.

RA-L bit 0-1 & 2-3 were swapped
trouble moved to bit 0-1

with middle margin switch high 2d data
margins normal Bit 0-1 OK, so outer two
were set Low to get some extra margin
and inner two set norm
Found that KEYBOARD program could not run unless
margin switches were all set NORMAL

→ Swapped cards 01 & 2-3 were left in swapped positions
→ Drive was set to 6.0
→ FF-L card for Bit 10 was replaced

→ Power Supplies in memory should be checked
for defective filter cap which may be causing too
much ripple.

Seq. off 4LT

Z - 20000

XR - 00000

A-D - 00001

111 = 0

112 = 10525 (bit 10 dropped)

113 = 21252 " "

OCT 31/NOV 1 1968

→ ID-A card for bit 10-11 replaced

BIT 10 STILL DROPPED AT 0100 HRS

→ XGG IN LOC 1F repaired to correct the dropping of BIT 10 (bad solder joint in NOR package at collector end of 2.37K load resistor) Top of package removed and joint was re-soldered.

NOV 3 SUNDAY DID NOT INC HRS AT 0600, shut off, tried to come on at 0659:50

→ Mem power fail lamp came on at first P=0 (mem not cycling)

→ RWS-A card in location B11 of drive pack was shorted (PIN 5) so new spare was installed

Mem OK, restarted at 1900 hrs 11/5/68

→ STILL WILL NOT RUN when +4V margin switch is moved high or low (Bit 10 picked up in loc 1220)

drive out = 6.0 INHIBIT = 3.8

2000 hrs.

HLT ZR = 20000 XR = 50376

P = 720

→ Locatic was incorrectly initialized by bootstrap.

SUN NOV 10 – HLT would not restart at 12:00 or 1:00

P = 563

MF turned off at 1:05 by bidding for Turnoff program.

MON NOV 11 – Prog simplified so that only CONF And Time prog are running. JMP i stored P ignores interrupts

TUES NOV 12

occassionaly skips an hour, then comes back as if an instructi is skipped

bits 01 swapped with Bits 28-29 in RL-A 2d ID cards.

STILL SKIPPED INC HOURS AT 2200 hrs.

FF changed 0-1 ⇔ 28-29

FRI NOV 15 LOST AN HOUR between 8:00-4:00

Clock Reset to 5:00 at 5:00 PM

Fri Evening NOV 15, CONF PROG WRITTEN INTO LOW BAY OF MEM (Begin 6000) to test both bays. Program is linked as follows:

TimeCK ⇒ LOWCONF ⇒ HighCONF

SAT NOV 16 — INSTALLED SOLID STATE CONTROL IN PLACE OF K101 (K102, 104, 105 yet to go)

MON NOV 18 - Completed installation of solid state controls on all 4 power circuits in memory (K102, 104, 105 done)

NOV 27 — INHIBIT SET 3.0 = 29.0V
DRIVE SET 4.5 = 37.0V initially

NOV 28 Exhaust Manifold fixed on cab #2
Bit 10 picked up in loc 21 when operating with +4V on high margin

DEC 2 - MON - OVER/UNDER voltage protection cards removed from memory power supply control

HLT & E on All others off

Wed Dec 4 Seq. Step (4-f) Clock did not change hour from 6 to 6:00 p.m

Man to left - little switch to center then off

Thur Dec 5 repaired memory system

RWS-A card in slot B5 of drive pack was shorted to ground at pin 4 (Read/CLEAR) select spare was put in its place

This failure was similar to RWS-A failure on 11/3/68

FRI Dec 6 0400 did not come on P = 563 OK

→ removed the sensitive relay trip from Memory. Noticed that fuse F2 indicated faintly during Startup. when fuse was removed, it was found that end was not making good contact with fuse holder contact, fuse holder should be replaced.

MON Dec 9 Did not come on at 3:00 PM

P = 617 111 = 0
112 = 0
113 = 0

Reset loc 100 to correct time

Restarted at 564 OK and went thru complete cycle

Bid for shut down 571

Sat Dec 14 reloaded old exec OK, noticed that bit 3 of P was coming on if it was only bit supposed to be off in low-bay world. For instance 77767 ⇒ 77777. FF-L card for bits 2 & 3 was swapped with FF-L in bits 9 & 10

→ Locations 400 through 2777 cleared in image & working core

→ 9:00 Dec 19. Auto off DCS off

ZR 35441
XR 77776
AD 17777 − 35441
pick seq st.
P= 35441 111=0
112=77777
3=113=00001

Restarted OK Loc 3544 was changed in core from 13677 to 17677

→ Bit 11 was picked up.

→ drive was reduced to 3.5

FRI DEC 20 DCS P = 35441
A = 00001

111 = 0000
112 = 77777
113 = 00001 bit 11 of 3544 was dropped

→ Memory cab heat lamp was on
exhaust temp = 25°C
Drive voltage = 35.0 with 3.5 setting
drops bit 1 → 34.0 with 2.5 set (new)
→ finally set for 36.0 " 4.0
Clicks up bit 11 if V = 37 Volts.

→ drive set at 3.5 (35.5 Volts) to prevent picking up BIT 11 in locati 3671, 3672, 3675, 3676

→ Remote Sensing on -37V Supply put back like it originally was by Anpex
→ Drive 37.0 V at startup 72°F = 6.0 setting
→ Memory voltage ± sensing cards installed
→ Upper fan in cab ± 2 disconnected (exhaust Temp level
→ set at 31°C = 87°F when ambient = 22°C = 71°F)
with setting = 6.0, V-31 = 36 volts with outlet temp = 87°F

SAT DEC 28 CLOCK DIDN'T RESTORE AT 0700 PM

Loc 3544 picked up bit 11

→ drive reduced to 5.5.

→ Mon Dec 30 DCS + AUTO OFF

ZR	35441	11 = 00001
XR	77776	12 = 77777
AD	35431	13 = 00001
		3 = 00001

Thurs Jan 2 Drive restored to 6.0 RA-L

~~said~~ bits 10-11 WAS SWAPPED WITH 12-13. Before swap, bit 10 was picked up in manual single step at location 76 only. (ultra + 4ust margin were set -10%, it worked OK)

ON RA-L ~~disk~~ which were in location bits 2-3, 10-11 had discolored Tantalum .16 μf 10VNP capacitors. These four will be replaced. (but were still not replaced by May 27, 1969)

Friday Dec 13, 1968 (+4 margin reduced by 10%)

to prevent bit 10 from coming on in loc

20, 21, 25, 74, 76

following locs were swapped with no success

INHIBIT

RWD

RWS

DDA

Mon Jan 6 Clock did not advance at 2000 hrs.

loc 3700 had picked up bit 9

making 15777 instead of 14777

Octal load prog'm had two bad loc:

loc 17532 was 24064 instead of 4564

17542 " 17542 " " 41562

FRI Jan 17 DCS AUTO OFF 5:00 clock

ZP	35441	P = 35441
XP	77776	A = 00001
AD	35441	111 = 00000
		112 = 77777
Turn on = 59:53		113 = 00001

loc 3700 WAS 15777 SHOULD BE 14777 PICKED UP BIT 9

Same as DEC 30, 1968, DEC 19, DEC 20, JAN 6

JAY had left outside door open in basement got too cold (≈ 40° F)

2/15/69 +4V margin set to NORMAL

3/14/ Door open auto off DCS off

ZR 35431 9.10

XR 77776

AD 35431 Loc 115 dropped bit 9

3/14 Air ducted from Cab # 3 & 4 to # 2

Inlet air = 21°C 70°F $\Delta T = 5°C$ with

outlet air = 26°C 79°F machine not running

3/19 HLT off Seq Skip c/o

ZR 20001 P = 20014

XR 77777 111 = 0

AD 20001 112 = 12525

113 = 25252

5 = 41077 13 = 24964

= 4067 2 = 13

3176

loc 3175 CURRENT = 1777

3176 13

Sun Mar 23 0900 home from Church
Clock says 2.0'clock (not or 7 hrs)
outdoor temp = 30.5°C

HLT ZR 20001 P=14 A=23530
XR 77777 5=41016
5 3522 111 = 0
3174 3523 112 = 12525
3 13 113 = 25252
2 1776
1 4064

Wed auto + DCS off
ZR 75477 A= 12525
XR 77776 P= 15477
AD 75477 111= 52525
Temp = 30.5°C 112= 12525 Pat 2
DRIVE = 630 113= 52525

FRI DCS P= 15477 A= 12525
111= 25253
112= 65252
113= 25252

P = 15477

INTERRUPTED AT (15432)
Yet re-entered at 15475

A = 1
111 25252
112 77777
113 0
4 = 15474
SAVA 533 = 1
SAVB 534 = 0

P = 15477

Prob (15422)
before 15423
INTERRUPTED AFTER 15414
Yet reentered at 15475

A = 25252
111 = 25253 Lsh PAT
112 = 0
113 = 25252
4 = 15474
533 = 25252
534 = 0

P = 15477

INTERRUPTED AFTER
CONFID, yet re-entered
at 17575

A = 73174
111 = 0
112 12525
113 25252
4 = 15474
533 = 73174
534 = 0

SJP BIDENT
JMP LOCK

~~Lock~~

7004 ENA 4
14546 STA SAVENT
1 JMP BIDENT

DCS P = 15430

4 = 15421
A = 25251
533 = 25252
111 = 0
112 = 52525
113 = 25252
534 = 664
700 = 571

P = 15415

A = 12525
J = 15407
533 = 52525
111 0
112 12525
113 25252
534 664
700 571

35 5 17

INTERRUPTS 446 stored at loc 4

Mon 10 0 clock

ZR 35511 P = 15507

XR 77777 A = 20000

AD 7777 4 = 15446

111 = 20000

112 12525

113 25252

restarted OK at 15400

TUES 10 0 clock

ZR 35511 P = 35507

XR 77777 A = 76643

AD 35505 35515 4 = 15504

NORM PAT prior to entry CONF { 111 = 0 ; 112 = 12525 PAT2 ; 113 = 25252

restarted OK at 15400

(533) SAVA = 20000

(534) SAVB = 664

2 = 664

Appears that Bit 13 being picked up in low bay

→ drive reduced to 550 (34.5V)

(TEMPERATURE AT OUTLET = 33°C)

XR 35467
ZR 77777
AD 77777

P = 35466
A = 00001
4 = 35432
Z = 0

534 = 00001 533 = 00001
111 = 57777
112 = 40001
113 = 0

Attn was not recognized from Prog. KB because loc 661 was not 77777 or 00001, and check was not made for Attn.

SUN 4/13/69 DCS

P = 35431
A = 377
4 = 3547
533 = 24
2 = 664

111 = 25252
112 = 77377
113 = 400

Fri 4/18/69 Bit 6 seems to be picking up
→ drive increased to 700

SAT 4/19/69 Bit 12 picked up in A P = 15415
111 = 5253
112 = 10000
113 = 257577

3pm auto · DCS off

XR 35511
ZR 77777
AD 77777

P = 15507
A = 20000

Bit 13 picked up

111 = 0
112 = 12525
113 = 25252
533 = 0
4 = 15463

restarted OK

MON 1900hrs P = 15415 A = 10000

4 = 15415

BIT 12 picked up in A

111 25253
112 10000
113 25252

2pm auto · DCS

XR 35521
ZR 77777
AD 77777

P = 15517
A = 20000
4 = 15505
111 = 0
112 = 12525
113 = 5252
533 = 0

dropped bit 13

4/26/69 Saturday

1. Found bad NOR GHH in slot 35 (Bit 13 of XR) would not stay set.

2. Lowered Drive to 550 so that Inc 663 would DCS OK. Bit 9 seemed to stay set to one when Drive was too high. Other locations were OK (Drive later set to 650

4/26/69

ZR 35431
XR 77776
AD 77777

P = 15430
A = 40000 ⇒ 00000
4 = 3541
533 = 0
111 = 25252
112 = 37777
113 = 0

→ DRIVE REDUCED To 500 when bit 9 was dropped

Raise drive to 600
→ Turn on time = 55:50
Turn off time = 00:15

→ Cores were initialized by ENA from each core location to eliminate Halfset cores.

4/29 800 o'clock evening

→ Picking up bits in reading location 15521 so drive reduced to 550 and cores reinitialized by ENA.

4/30 0300 next morning
dropping bit 8 in ZR when continuously reading loc 15521

→ reduced drive to 500 and cores were then reinitiallized by ENA prog.

4/30 0600 dropped bit 8 of loc 15403 which caused it to look like HLT.
Loc 15403 was still 400 however, so it pointed to data gotten outside memory
Problem only occurs on gating from high bay locations

→ Swapped FF-L cards for bits 5&6/7&8 in high bay

Lost bits 4 & 6 in A . with stop at 15414

111 = 25253

112 = 12405

113 = 25252

9:00 Am Apr30 Seq Stop + HLT .

XR 20000 P = 377

ZR 00000 4 = 35516

A-D 20000 533 = 0 534 = 664

B = 1

111 = 0

112 = 12525 no BAD BIDS IN BIDREG

113 = 25252 15403 = 0 instead of 400

→ Found bad unload NOR on XGG in slot 1E which was causing Bit to be dropped from high bay. This was replaced with new NOR element

→ DRIVE still set at 500

Apr30 8:00

May 1 auto. DCS B=664

X 35511 A = 65252

Z 77776 111 = 0

AD 77777 (35511) 112 = 77777

113 = 1

533 = 65614

→ drive increased to 600

0700 o'clock

STOP X = 26041 P = 3555

Z = 20000

dropped bit zero in getting
loc 3526 (Jmp 555)

P = 15431 111 = 25252

A = 07777 2 37777

3 0

Loc 15522 → 15521 both = 12525

→ dropped bit 14

5/2/69

→ 2EB in Loc 5V replaced (UDB)

SUN 5/4/69

→ Drive reduced to 550

SUN 5/11/69 ontime was only 15 seconds 2 times this evening

1100 o'clock DCS stop P = 15031

14 25252 A = 37777

12 37777

113 0

→ TIME corrected and core replaced by using EVA;

DCS stop 8 o'clock MAY 13 TUES

P = 15031 (BIT 14)

A = 37777

111 = 25252

112 = 37777

113 = 0

Machine was turned on for about 1 minute at 6:00

Loc 15522 seemed to not want BIT 14 set

MAY 20, 2100 hrs. DCS 15520 A = 0

111 = 0

4 = 15517 112 = 12525

113 = 25252

2200 hrs. 533 = 0

Sun May 25 D 15465 A = 1

4 = 15406 111 = 77777

533 = 65252 112 = 1

RESTARTED OK 113 = 0

2200 hrs. SUN STOP Z = 20000

P = 504 111 = 77777

4 = 15466 112 = 1

533 = 1 113 = 0

RESTARTED OK

auto - DC8 - Cold

ZR 75467
XR 77777
AD 77777 - light 75467

P = 15465
A = 1
4 = 717

Mon May 26 Added INITCORE To Shutdown routine
(Loc 301-310)
- seq Skp + Hlt

ZR 20000
XR 00000 STOP P = 504
AD 20000

SKIPPED THE JMP at 503

A = 15466 111 77777
S_{23} = 1 112 1
113 0

MAY27 1969
→ RA-L card in memory bit 0/1 Removed
15/16 put into 0/1 slot
Card which previously was marked "No IS ... Z
was put into 15/10

DRIVE SEMI AT 6.0

⇒ RA-L card in bit 2/3 still has brown deposit all others have porcelain ends.

Noticed that Locations 4470 thru 4477 were disbleared when the Keyboard Interp Program was checked

Halt circuit/drivers were checked using scope at all connections of the decode. found suspicious [waveform] at selector in slot B1 (Φ7pΦ) → card was replaced. Also noticed excessive hiss [waveform] signal on ΦpzΦ selector during read.

SAT MAY 31 DCS P=15510 A=40000
4=15466 111=40000
533=1 112=12525
113=12525

7 o'clock
4=15413 Sprocket hole seen 12
P=15416 533=12525
111=25253
112=12525=A
113=25252

(Ultra? SYN)

JUNE 1
Monitor DCS

(15507)
75507

111 = 40000
112 = 25252
113 = 12525

A = 40000

END AROUND Carry was not set when SIPA was executed at 15503, but it was set when EOR P was executed at 15505

0200 hrs closing 10 o'clock AM
clock was correct at Midnight

SUN NITE 10:00 Noticed that when -24 was reduced to low margin, the OD program ran with no hesitation, but at normal -24, it ran jerkily.

→ Left at low margin
→ Opened window
→ Reduced mem drive to 610

Tue. Morning Jim's Console OD [illegible]

ENA [illegible] at 16542 was picking up bit 0 when loading A and 16550 this caused '143 to be written on top of contents 16551 (previously ENB)

This happened with Low-24 margin and Cold temp (window was open.)

→ Cleared up when bootstrapped and -24 put to NORM.

TUES EVE

Loc 3721 had 15777 instead of 14777

Restored with SYNC PROBE OUT

Fri - ZR 75437

XR 77777

AD 77777 75435

Restarted OK

SAT 6/7/69 DCS

2300 hrs

restarted OK.

P=35464

A= 1

111 = 77777

112 = 1

113 = 0

P= 15414

A= 25252

111= 25253

112 = 25252

113 = 25252

Monday

Loc 100 had 20 o'clock (A) shift scale

Here had 5 o'clock (P)

Bit 14 was dropped also

	Should have Been	Was	Error Comment
11 o'clock	61	61	
12	62		add 70, make 11
1	1		CLR 62, make 20
2	2		
3	3		
4	4		
5	5		
6	6	43	
7	7		

Wed ZR 15417 auto JMS

XR 77777

AD 15417 77777

P = 00001 ← Probably resulted from bad shift.

A = 17527

111 = 12004

112 = 17527

113 = 25252

Restart's OK

(TEST 2)

11:00
SAT MORN PCS
JUNE 14

P = 35444
A = 4564

111 = 77777
112 = 77777
113 = 0

(TEST 6)

4 = 665
533 = 65523

Restarted OK

JUNE 14 12:00 STOP P = (2)0012
A = 20001

(TEST 2)

111 = 0 ← IF loc 15522 became 15523 then it is possible that ZERO [illegible]
112 = 12525
113 = 25252

Restarted OK

[illegible] bit 14 [illegible] one [illegible], bit 8 may have dropped

June 14 15:00 STOP P = 0

(TEST 2)

111 25253 [illegible]
112 37776 37777 = 0
113 25252

[illegible] = P+12
10 101 010 101 [illegible]
11 111 111 111 110

→ SYMPTOM = P skipped [illegible] in Loc 15412
or RSH was not executed, but [illegible]
picking up the bit in [illegible] could explain
[illegible]

JUNE 14 1700hrs STOP

ZR = 20001 P = 15460

111 = 77777

112 = 0

113 = 0

June 15 stop 1100P

ZR = 20000 111 = 000000

112 125252

113 25252

June 16 0300 DCS

→ Clock set Low margin

June 17 0600 DCS P = 15465

A = 00001 111 = 77777

112 = 1

113 = 0 correct

→ Sometime between STA 113 at loc 15464

and JAZ +2 at loc 15465

the Accum picked up bit zero

July 4, 1969 found that gate for [illegible] of Tropel

was vibration sensitive, [illegible]

→ +24V bus on P.S. has Variac now

it is set to 24V (had been 26V)

while printing out on KITTEN, Made used DCS

P = 15512 | 111 = 0
A = 0 | 112 = 12525
113 = 25252

533 = 0
4 = 15500

→ Looks like interrupted program returned to P+1 instead of P

Sun Night 11:00 July 6 did not sustain start at 11:00
P = 51777 | 4 = 35523
A = 0 | 533 = 0
111 = 0
100 = 60525 | 112 = 12525
Restarted OK | 113 = 25252

Sun Mom July 13 Clock did not inc past 0300 hrs.
P = 0032 | 4 = 410 | 111 = 0
533 = 0 | 112 = 10400
Wall block was out, and EAC to was cold. | 113 = 21252
dropped bit 11

many locations were clobbered. in SYNC (400 →)
→ restarted without SYNC plugged in

Mon Morning July 14 4:40 (clock reads 4:40)

STOP Z = 24031 111 1
X = 3476 112 77777
P = 15436 113 0

4 15416
533 0

restarted OK

SYNC NOT RUNNING

Mon Aft July 14 at 5:00 clock

Stop Z = 20300 111 77777
X = 0 112 7777
P = 213 113 0

clock = 2:00
100 = 42376

→ Reinitialized Core. and restarted

MonEle STOP Time = 7 o'clock

Z = 20025 111 = 77777
X = 09020 112 = 0
P = 15461 113 = 0

Since SEQ STEP WAS BEING SET ACCIDENTALLY TO

→ Card was repaired (output 13)

auto

ZR 75437 111 = 77777
XR 77777 112 = 1
AD 75437 − 77777 113 = 0

P = 75463 (15463)
A = 1
→ CLOCK SLOW MARGIN

ZR 35431
XR 77776
AD 35431 (77777)

Tues July 15 10:00 HLT
Z = 156 111 = 52525
X = 312 112 = 65252
P = 15410 113 = 25252
→ SLOW CLOCK & LOW PSN

Wed EVE July 16 Grounded temporarily 4R14 which
→ may be clearing TR dum F Sq.
→ Clock 2d PSN ADRM

Seg. Step - auto off

ZR 20000
XR 00010
AD 20000

July 18 HLT

ZR = 20276 P = 15404
XR = 2000 15404 = 14112
A = 0

Loc 276 = 2000

111 52525
112 12525
113 25252

→ GHH in Loc 6F replaced — the clock was stopping with step 1, 2, 3 on when clock was fast margin

12:15 Seg St. + HLT - off temp 30.6 degrees

ZR 20000
XR 77777
AD 20000

111 77777
112 77777
113 0

P = 5b
5b = 0 restarted OK

→ Press TR signal circuit with CRT refresh cycle temp disabled by grounding OG26 & OG28

STOP ~~July 21, 1969~~ 1900 hrs.

~~Z = 20000~~

~~X = 47525~~ (Norm stop

"ON" switch left ON at 1900 hrs.

Tues July 22, 1969 Programs were re-initialized Jumper removed from the CLR TR gate installed on July 16 so that INTERRUPTS could work. Disabling Jumper on transfer K cont → TR for CRT refresh still there.

Temperature = 23°C

Time

ZR 00030

XR 15454

AD 35501

com + dist stop off

For none in clocks

31

P = 15452

Restarted OK 100 = 11° clock

Tri.

AUTO - DCS off

ZR 30001

XR 15404

AD 35405

P = 15404

A = 65252

111 = 52525

112 = 65252

113 = 25252

AR 4 on
ZR 35441 Sq. PFE on
XR 77776 clock all fine on
AD 77777 (35441)

MON AUG 11, 1969

INTERMITTENTLY IGNORING INPUT from PKB
Cause – Shift instruction dropping bit 4
Solution – Set pin 20 on XGB in slot 4D and then dipped it with conductive paste

Tues Aug 12, 1969

→ XGB in slot 4D replaced since problem did not come back.

Wed Aug 13 1969 XGC in Slot 11V has bad element output pin 26, replaced with an XGC which had been removed from 4R on 1/29/68

SUN AUG 17 1969 Returned home after being away 48 hours.

1. DRIVE (37V) in memory took 30 minutes to come up to 36 volts from 30V.
2. Bit 10 of X reg would not stay set to "1" unless Sw 6 other bits were also set.

After testing up trouble disappeared

(found Solder blob on pins 24-25 of 2V on 9/30/[illegible])

Sept 1 Block Spare GHH in slot 2V replace
Clocks had been hung up on 10:00 and
not incrementing P was set to 1606 at
8:00

$$\begin{array}{r} 1606 \\ \underline{1564} \\ 22 \end{array} = 18 \text{ hours is too long}$$

except that Some of the loc. between 1564
and 1606 were valid instructions.

```
10000 00000
                                10:00   11      12      1       2
01560 00000 00000 00000 00000 00000 00000 00000 00000
01570 02000 02000 02000 02000 02000 02000 02000 02000
01600 00000 00000 00000 00000 00000 35432 00000 00000
        3     4     5     6     7     8 → 8:00
      1600    1     2     3     4     5     6
```

Loc 1570 - 1600 are now cleared.
loc 1605 is Cleared

SEPT 8 - CLEANED AND OILED BLOWER IN #4
CAB. MTD IT BACK WITH ONLY 2
SCREWS SO THAT IT WILL BE
EASY TO TAKE OUT NEXT TIME.
OIL HOLES SHOULD BE ON TOP.

WIRED IN THE CCO WORD 32, bits 1-12
to the TB2 of the Terminal cabinet

Sept 9 - 0600 hours.

1. At 0555 hrs Jupiter came on for only 10 seconds.
2. Temp in Terrarium = 23°C 6' above floor
3. Loc 400 - 410 were clobbered
4. loc 100 was calling for 9:00 PM (this explains why the clocks had gone to 10:00 after an hour's increment on cold mornings before.
5. Also loc at 10400 - 10410 were clobbered. SHD HAVE BEEN

10400 =	43	77
1 =	4000	14533
2 =	1000	11000
3 =	2041	12461
4 =	7020	7020
5 =	4000	14505
6 =	1000	1504
7 =	4000	4010
10 =	1001	1521
11 =	3010	3010

6. Prog printer motor came on when first restart was attempted after the 10 sec auto-run.
7. Temp came up to 25°C when curtains were opened, and North window was closed.
8. Liv Room thermostat was set on 62°F furnace was not running.

```
03500 03521 07017 10040 07475 10010 07017 10040 07377
03510 14514 07020 14377 41500 00000 00743 07115 14117
03520 05500 01500 01523 00743 07030 10060 01555 11020
03530 12531 01521 14537 07115 14116 10070 41523 54125
03540 07047 52765 11020 16762 13677 11020 16763 13701
03550 11020 16764 13571 41766 03523 00000 07100 17760
03560 16761 14100 10031 00000 07100 17760 16757 14100
03570 10031 01526 07554 45015 41015 41766 00000 63577

03700 14777 41766 07777 13704 41766 07100 15756 14100
03710 17775 16776 13722 07100 16773 17774 13727 01742
03720 10031 14777 41766 07100 17772 15771 14100 01717
03730 07100 17772 15756 01724 07754 14005 45755 63777
03740 07753 14005 01571 07100 17760 16757 01717 17000
03750 00000 00000 00000 41077 41004 17000 01000 00376
03760 77000 00525 66330 00000 40025 17412 00740 52525
03770 12525 20000 60777 23000 37000 17000 12000 05376
```

Dumped 9/9/69 after 2nd restart

Sept 16, 1969

Stopped mysteriously in (INST) step ← IMPOSSIBLE

P = 507 (JAZ instruction)

Restarted OK at 504

Sq. step HLT off

ZR 40000

XR 44525 JAY PUSHED BUTTONS ONCE

AD 04523 AFTER MACH STOPPED, BEFORE POWER WAS SWITCHED OFF

Thurs. Sept 13, 1969

At 0600, the clocks said 0130, the last time displayed after turned off at KITCON. No restarts had occurred during night.

Sq. step on

ZR 00777

XR 13777

AD 13777

TR 67777 all instructions on

P = 571

Not goal, bids in bin below

Restarted OK at 3563

Sat Morn,
Was turned on by CKB, machine went into
tight loop 446 – 450 Loc 4 had 445
which looked like ready

Monday, Sept 22, Replaced XGE module in
location 7S to prevent Loop at loc 450
(the first location after clearing INT lock
IN the exec program)
ØUY should be inhibiting interrupts per
the login diag. (7S18 has wire)

SAME TROUBLE, 7S orig put back
→ 7M replaced

ZR 00000 HLT off CKB was used
XR 00000 E on after Complex test
AD 00000 Stupid

HLT off

ZR 20000 P = 463 (462 OK)
XR 77777 Loc 541 = 2715
AD 20000 PRev bid in table was 2600

Loc 463 was cleared to Zero., when it was
corrected, machine started OK at 3540.

Sep 29, Monday 0300 hrs.

Seq E IR = 1 INSTR = JMP

SEQ STEP SK = 1

ZR = 473

XR = 441

P = 473 LOC 473 = 1445

LOC 4 = 3551

Restated at Loc 473 OK

No core location in error display

→ Looks like SEQ STEP came in incorrectly during JMP

Sep 29 0700

Came on ok at 0655 hrs.

SEQ F IR = 1 INST = JMP

INST STEP SK = 0

ZR = 1

XR = 445

TR = 446

AD = 446

P = 446

→ Started ok at 444 Similar to above prob

00 517 auto ip
00 447
01 777

Loc 541 = 445

Started at Loc 3540 OK

Sept 30 Trcs 0200 hr.
Stopped with INST STEP SEQ = F
IR = DCS (4)
P = 531

Restart OK at Loc 530

→ { GAH IN 6T
XGA IN 5C } Replace to Solve the INST STEP – SEQ STEP problem

TO BE REPAIRED

Sept 30

40 517
40 447
41 577

P = 451
541 = 445

→ GAH IN 5H replaced
NEXT TRY GAH IN 5E

PROB OK 1-20-70

OCT 5 P = 450   541 = 445

Loop with 4 = 3312

Oct 6 20000   HLT - Seg. off
051 00
251 00

00000 no lug HLT off
10000
10000

541 = 2716
4 = 2716 ←

OCT 8 Replaced GHH in 5E To prevent locked with cleared premature
1. Put RC suppression on TV station changer to prevent hangup
2. Changed TV program so that it is [illegible] Bidder

Oct 9 Stp P = 447
4 = 445 = 541

OCT10 P = 717
4 = 717
541 = 657

OCT11 SATURDAY - Added extra brace to TV antenna mount
added Shutter to exhaust fan in back
of computer in basement wall

→ swapped XKA in Slot 11F to
coirect the false clear lookout
"KEPGON" signal

Seg Step # HLT off LOVE YOU OY
ZR - 20000
XR - 11527
AD - 31527

OCT 14 STOPPED P = 446
4 & 541 = 445

PROB OK 1-20-73

→ XGF IN SLOT 11E SWAPPED

OCT 17 Loop 4 = 445
541 = 445

OCT 17 loop 4 = 571
541 = 571

Loop 4 = 717
541 = 657

Looks like TR may be indeseriminately be set to 4.
→ 5R replaced
(to be replaced NEXT OH, OK element)

Loop 541 = 657

OCT 19 LOOP 447, 450, 467, 446

541 = 4 = 466

OCT 22 FAN IN [illegible] STOPPED. [illegible] SHUT DOWN
POWER. [illegible] WAS [illegible] WITH DOW
CORNING 200 FLUID DIMETHYLPOLYSILOXANE
AND RE-INSTALLED

DYNACOOL MFG INC.
West Hurley, N.Y.
[illegible] C-329
[illegible]
1000 RPM

A4

→ CIRCULATING FAN IN CAB 4 REPLACED BY DUAL ROTRON SAUCER FAN ASSEMBLY WIRED FOR 110V. EACH FAN GETS 60 Volts WHEN POWERED BY 120 VAC. PLUG at rear of Assembly Supplies 120 Volts.

→ Filter in CAB 4 was very dirty. Can It was cleaned and reinstalled. THIS FILTER SHOULD BE CLEANED ONCE A MONTH

OCT 25 - Clock did not increment - loc 3700 picked up bit 9

→ Air flow barrier installed in cabinet 2 to keep sudden air temp change from affecting memory

Sys. Stop Halt Off

ZR 00000
XR 11527
AD 11527

Y R 007

Nov 12 0530 hrs hanger loop 445
interrupts during interrupt program

00777 Quits OFF
00777
01777

Nov 14 40000 INTERRUPTED AT 571
11527 loc 4 + 451 = 571
51527

Nov 21 Sync Pulse off loc 4 = 571
391 = 571

Nov 21 NOTICED CLOCK WAS WRONG
LOC 3700, 3721, 3745 has picked up
Bit 9.
Restarted OK after Correction
Drive moved to 550

Nov 21
Drive set over to 550
Picked up one in Bit 9 in loc 3700 & 3721
Drive moved to 550

NOV 24 [illegible] COLD – CLOCK STOPPED
ADJUSTED AT 100
BIDDER TABLE WAS FULL OF BIDS for
3200
IDLE #11 (604) was placed in table and
mach running OK.

While single stepping through prog counter, Sync bit
Acc hang up (loc 4 = 641) occurred
[illegible] at loc 35400
Also loc 541 = 641

Nov 24 00177
00657
00177 [illegible]

Nov 24 Loc4 & 541 = 655
P = 450

——▷ Sense amp for bit 9 was replaced

Nov 26 no lights on HLT off
Would not turn off by Holding
down upstairs

Nov 29 2 PM TURNED ON OK

HLT ZR = 0

XR = 26007

P = 1064

4 = 665

· current P = 3523

Restarted OK at 3540

TV wouldn't change channels turn off

Cause - bit 9 was set in POZE 20 (Loc 20)

Nov 30 1 AM Machine down turn off

P = 1401

loc 20 = 01000

contacts on RA-L card for bit 9 look dirty

→ conductive epoxy applied to card contacts

2, 4, 5 in position for bit 9, of previous

card replaced on 11/24/09

Nov 30 1 PM Machine was turned on at 11:00

and not turned off. Typer motor was

running ad case was hot. Pulled plug

to allow motor and frame to cool down.

Restarted at 3540 OK.

Dec 1 00777 HLT

60777

01777

DEC 4 03777 loc 3546 picked up bit 9

23777 command was changed to

37777 EDR POZERO

so that fewer "1" in word

DEC 5 { loc 4 = 447 (interrupted)

40053 B = 41002

00076 P = 41004

10131 No. Bids

Dec 8 HLT Picked up bit 9 and went to 1664

77777

77777

77777

Dec 8 set the thermostat inside men cab for 80°F

Dec 13 1. Replaced FF-L card in Memory bit 4 #5 because it was sensitive to rapping with screwdriver handle.

2. Replaced XKA in loc 6L because $\overline{OUT}$ was intermittent

THIS CAUSED OUT SEQUENCE TO BE SKIPPED

3. Repaired printer control logic in Kitem NOR 6J was replaced. $\overline{ISR}$ was not being raised

→ DRIVE REDUCED TO 5.0

Bit 7 dropped at 9:00

→ reinitialized and restarted

Dec 20 Picked up [illegible] in loc 3764

→ Reduced Drive to 450

Dec 21 [illegible]

Added Dedicated Light

10577 auto off -
00447
41577

00777
77771
01777

ZR- 00000
11527
11525

20016
00000
20016

20016
00000
20016

Seq Stp. off
SEQUENCE LITE ___ ON
INSTRUCTION . HLT OFF
IR all off | 0000 | ON
ZR off
XR 21527 (NORMAL P = 3563)

20477
20447
21577

20477
00447
21577

SAT MAR 21, 1970

Bit 12 Sense Amp (Labeled All) drops a bit 12 in loc 72: when cycled rapidly. When sense amp card was moved to Bit loc 10, it dropped Bit 10 in loc 660

Cards (Sense Amp) are sensitive to +4V margin
Sme pick up with increase by 5%
other drop " decrease " "

bit 10 dropped in loc
3224
3204
3260
660

Did not change to 2
00477
00447
01577

00617
00677
01777

following locations cannot store a "0"
in bit 9 if all other bits are 0

0020
0120
0220
0320
0620
1020

Sat April 11, 1970

Some execs were clobbered in core memory during the checkout of new sense amp card. found that disturbance on Bit 9 worse than anybody else. Change 35.7 ohm sense offset res to 65.9 Ω runs ok. Restored the clock program to come in at T+55 minutes and run till 10 secs after hour. Bit 9 was coming ON in P with all other bits were off. otherwise, it was ok

SAT APR 18, 1970

Checked out newest version of the sense amp in the Argos memory. Works ok. +6V margin switch still causes Bit 9 to come on. New SK ~~4010~~ 4110-1 is in the 1-1 Bit 9 to

5p

Resistors used on SK4170-1 were

24.3KΩ (3 per dual sense amp card)

75 Ω

511 carbon

IN3016B Zeners

711 Sense Amps

944 with pull up resistor = 2K

MAY 11, Monday.

1. Found that memory loc from 400_8 to 3000_8 had been shifted down by one location, and that bit 9 was usually missing. Wrote short program to relocate this block up by one location. Entire Block must now be checked for Bit 9 omissions.
2. Replaced sense amp for Bit 10 with new type sense amp card, since it was being dropped in location 465 (all other locations around there could accept a "one" in bit 10)

June 7 swapped R/W Driver card for address bits 4 and 3 S43 210

loc 20_8 seems to be picking up a false ONE even though it is not addressed. It appears to be half set until data is read into a few times.

ZR 00000 Sq. Step not off
XR 07366
AD 07366

June 20, Sat 1970.

Took blower motor apart (cab 4) and cleaned it, oiled with Sewing Oil and Teletype oil

Last cleaned in October 1969 (8 months ago. (Blowers should be cleaned every 6 months)

Used DOW-CORNING 200 fluid on both bearings after cleaning thoroughly with Degreaser to remove hard dry grease deposit

ZR 20000
20366
40366

after Rick Sq. Step - all lights a bit on before

IR 20724 ENDM
XR 00002
AD 20724

Mon July 13, 1970 INSTALLED NEW BLOWER IN #4 cabinet. Should be oiled with #20 NOE Oil on New Years Day

Sun Oct 25, 1970 Cleaned blower filter in cab #4

Mon Nov 9, 1970 Bit 14 dropped in loc 5
∴ Jmp 1 to loc 16 became Jmp to 16

MON MAR 22 1971 Mach did not start at 0800 PM because the contacts of X relay (ⓦ BF Silver contacts) in power control panel were not making contact. After recycling relay several times, -12V was switched thru to logic. Symptms were that 2EB drivers were not holding transfer buses to +5 logic "1" and all register lights were on at the maintenance panel.

Bit 14 was set in loc 100 which caused alarm not to go off this morning

TUE MAR 23 CLEANED Relay X1 contacts with emery paper and doped them with conductive epoxy grease to preserve good contact on (-)12 and (-)24 volt power to CPU

April 3, 1971

Present locations used in block 400 — 777 which must be relocated before new exec can be put in that block

740 — 744
665 — 667
755 — 756

April 15, 1971
2000 hours

Machine didn't turn off automatically at 3:00:20

1. The Z register bit 14 appeared to not stay set when manually loading a "1" into memory.
2. The same trouble appeared on the high addresses of memory, so, memory itself not at fault.
3. Ran the ENA, DCS, Jmp loop to insure no half-set cores. (prog would not stop at end of DCS loop.)
4. Bit 14 still could not be set in Z
5. Ran program on manual clock, bit 14 seemed to be set ok on slow transfers.
6. Ran program on normal clock, and it worked ok. (stopped at end of DCS loop)
7. Looks like DCS check for all ones in Z register failed because Bit 14 was not being set
8. Restarted clock and found no loc were destroyed by ENA loop prog, therefore, the normal MEM+CPU

transmission was OK. The trouble with Bit 14 must have been in the Z register flip-flop or in the gates to Z register.

this cause would explain several recent problems with Bit 14.

1. Failure to clear bit 14 with EDR at MidInt in the time increment prog.
2. Failure of JMZ instruction sometimes

April 16, 1971

Same problem with Bit 14 as on April 15
changed XGF card (input Gate) in slot 2F and trouble disappeared, Bit 14 could not be set where the original XGF card was placed in slot 2F. Card will be repaired (output = 30 bad)

April 29, 1971

Made repairs to +6 Volt power supply in Core Memory Voltage now about 4.6 Volts (R 33 was jumpered out in control panel to permit Relay for +6 V in sequence to pick up) Running with modified RA (read amp) cards in slots for bits 0, 1, 2, 3.

CORE NOW RUNS UNDER ALL MARGIN SWITCH COMBINATIONS

Finished 13 more modified RA boards for further additions on a one for one basis

Noticed that bit 14 in lower half core is dropped when transmitting

MAY 24, 1971

Bit 14 still is being dropped in Z register when in Mon Lock ENA. The "repaired NOR" was replaced on the Apr 16, 1971 repaired board and re-installed into slot ZF.

RA cards for Bits 8, 9, 10, 11 in lower stack were replaced by modified cards with IC sense amps installed.

MAY 25, 1971

Bit 14 still being dropped in Z register as before. XGF card in slot ZE was repaired by replacing NOR gate associated with bit 14 (output # 30)

May 26

Machine stopped at 11:00 this morn. Card in slot ZC is sensitive to vibration and it was replaced

MAY 27 1971

Added 3 more rebuilt RA cards to memory. The cards now in slots B8 and C8 will be the two extra spares since they have wire jumper corrections

MAY 29 1971

[illegible] Transmitter [illegible] [illegible] [illegible] [illegible] [illegible] [illegible] Beyond [illegible] [illegible] [illegible] [illegible] [illegible] Nap-down [illegible] to [illegible] it doesn't stick

JUNE 10

AND & EOR loc at 3557 are not executed correctly, ADD is OK
Program can be started at 3515, and run to stop at 3560, answer correct in Accumulator, but if machine is allowed to run to complete, then Accum = 61... instead of 17...

June 12

1) Sequence hanging up in Step 0
2) Core was cleared except for loc 3700-3777
3) Clock prog was loaded into 3700-3777

June 13 Bit 6 of word 31 cannot be set. (Relay letters OK)
trouble probably with bit. driver

July 14 Stopped at 2:00 AM
XR = 25643
Seq step, E P = 3752
IR = 0, HLT
Halted current output time and turn off to CC0

July 27 0100 hrs stopped on HLT, P = 3640
restarted at 3740, increments disc counter,
no trouble occurred at time of interrupt,
after interrupt, resumed OK.

Aug 3, 1971

Bit 5 of TR was getting cleared randomly and causing among other things STA 3767 to become STA 3727.

→ Boards in Slots 0G and 0H associated with K counter interface were removed to see if this problem caused by them randomly setting or clearing bits of TR.

Cards 0G and 0H were very dirty — contacts were BLACK.

AUG 3, 1971 (0700 hrs)

→ same problem as before, bit 5 was dropped in TR causing loc 3727 and 3767 to be destroyed

→ GDH in slot 1P was changed out with BACC spare

Noticed that bit 0 of TR was being picked up w/ Low bay of core only.

→ swapped data gates from DA → DB, no effect

→ Replaced RA-L card in Memory bit 0#1, OK now

Aug 21, 1971 Mach stopped at 2000 hrs.
Auto, P ±B 1111
17 = AND

ZR = 77777
XR = 77777 P = 0
TR = 5100 A = 66230

Found no-stacked connector in Memory Read Amp, repaired & reinserted

Sept 6 Noticed that slight touch on START switch handle caused the machine to stop. Bad contacts were burnished and connector epoxy was replaced to stop. This sort of stop could explain intermittent stops and loss of time noticed earlier.

Sept 11, 1971 Replaced the Silver contact switches on Maintenance panel with Push Button / Mercury Wetted Relays. The TEC push buttons have Gold over Nickel Contacts, and the two indicators are LED (Light emitting diodes) this will be a good test of these switches.

Sept 12 1971
Stopped at 1700 hrs. HLT 0V
ZR 20000 P = 0.0001
XR 17776 bc = 0
AD 37776

Restarted OK at 3733
Rapped all Card handles, lowered PSN, PSP MARGINS
NO failure
Ran Memory cards and found that Bit 8 ff-L

IN Slot 13 of DATA CAGE (Bottom Cage in 2nd cab.) was sensitive to RAPPING front edge, changed card with spare Same problem, so the Socket must be defective,

Sept 20, 1971
Stopped with P= 1 restarted OK at 3733

Oct 1 1971
Machine stopped in A sequence with step "0" on all 1 through 5 off. for about 5 seconds and then proceeded

Oct 6 1971
Changed out GAH in loc 6D to fix of Oct 1 1971 observation. Card in loc 6D controls seq. step 1

Garage door left open - Loc 3714 picked up bit 9
Clock did not roll over to 1:00 after midnite
Noticed that bit 9 would come up in Loc 3714
Whenever loc 3767 with bit 9 set was accessed
→ Lowered drive from 6.00 to 5.00
trouble disappeared

Oct 17, 1971

Changed dropped bits in P.

1. Lowered INH to 4.5 for 5.0
2. Grounded the pins 4R14, 0G26, 0G28 to prevent TR from being cleared by logic no longer needed (Interrupt & CRT)

Oct 21, 1971

Grounded pin 0H26 (MEM TRIG of CRT buffer) to prevent Prog Counter from getting mis set.

Oct 23, 1971

Raised INHIBIT back up to 5.0
Lowered +24V margin to 50%
−24 margin to 20 volts.
Changed out GAH in Loc 6D

Changed out GHH in Loc 5R

OCT 20, 1971 Wed.

Replaced two NORS on GHH (Slot 5R) and replaced.
Replaced another GHH to provide two Black banded Spares.

OCT 21, 1971

Stopped at 0500 hrs Loc 3610 cleared to 00000
Should have been 41612

→ Clock slowed.

OCT. 27

Original GAH replaced back into slot 6D

CLOCK NORMAL SPEED

OCT 27

Stopped P = 3375

loc 13 = 73536

Stopped P = 66274

Stopped P = 04054

loc 13 = 77323

Replaced 11/8 Loc 5P (GAH) swapped with Black spare

After 20 hrs. Loc 13 = 77462

Loc 5T (GDH) swapped with SPARE

4L (GDH) swapped with Black Spare

Stopped because Loc 1 was executed

Replaced 11/3/71 Loc 4V (GHH) swapped with Black Spare

Stopped because loc 1 was executed

Replaced 11/3/71 Loc 3F (GDH) swapped

Stopped because loc 1 was executed

Loc 5R (GHH) Swapped
output 5R10 suspected if causing TR_{8-13}
to be cleard wh it shold not be

Loc 3733 contained 3733 instead of 1724
preceding inst was 15765
5IP

OCT 30 1971
Stopped on INITIAL TURNON AT 21665

Φ should have been	was
3735	3214
	6373
3755	3214
3753	3763
3753	3214
3735	
3756	1

Nov 7, 1971 MACHINE HAS BEEN DISABLED FOR ONE WEEK.
→ Modified the power supply in memory (-37V) to reduce the chance for its oscillating. (lowered loop gain) Add 2.7 K resistor between Collector of Q5. and base of Q4 on Scheme 11627
MACHINE RESTARTED WITHOUT PROBLEM

NOV 8 Steps at Loc 0

Replaced spare cards previously changed on 10/27

Stepped with P = 4054
" " P = 3634 Loc 13 = 77740
A = 40101 P 3644 " 77773
3146 77374
3610

1644 1645
4205 7570
44521 44522
45211 45211
23011 45322
45472
5625

40000 40301 76265
#1 66244 B=66244 65527 77775
- 66244

#2 17776 0 7734 77775
0 0 10041 77760
#3 37000 0 11322 77354

3735 → 1

3736 → 1

NOV 10, 1971

3R ≠ 3K swapped out with good spare

stopped #1 Looks like instruct was INDEXED

110 110 010 100 100 (B)

① ~ 111 111 010 110010 ← 1 (P)

110 101 101 010 111

stop #2 drive decreased to 5.5

→ { 4M (GDH) ≠ 4V (GHH) swapped
drive slt look to 6.0

#13 output noted marginal spec (3c, usu)

	B	P	13
Stop	26046	25726	77760

AND failed to give right answer 77000 • 00377

lower half of AD was 377 should have been 77

Stop #3

Changed 2EB in slot 5M (AND)

2252 contains 10040

Test program

Loc 310 = compare word

beg = 301

B contains address where compare word was found.

A = 0000 P = 77701 B = 0

following Loc contain 77700:

4055 = (DKBCHR)

NO Loc contain 77701

Looks like TR not being cleared at end of E seq.

5T (GDH) replaced)

5S (GHH) "

NO AND, EOR, ADD, STA (No space for XKA in Loc 6L

Reseated card into connector, trouble disappeared

A = 37000

P = 65441

B = 0

Nov 12, 1971

Reduced -24 to low margin

TURNED OFF MACH

DEC 2 1971 - TURNED MACH BACK ON

DEC 8 1971 - STOPPED AT 0400 hrs. with 4HR clock

NOT INCREMENTED

E SCLQ

ZR= 40000

XR= 49003 all other lamps out

AD = 00004

P= 40005

B= 43761

I= JMP to 7

DEDTIME LOC (4060) = 11571

Loc 13 = 77725 (set back to 77776)

Restarted at 3733 OK

Dec 11 Adder is OK at all clock speeds, but...

the following program doesn't decrat properly

```
ENA, I, 2
DCS     2
JMP   - 2
HLT
JMP   - 4
```

step over dec 012

1 1 1 1 1 1

NO apparent decrement for bit 8 to 9 at fast and normal clock

Dec 12, 1971

IR decode had intermittent loss of upper group of inst. (outputs 10) Replaced card 45 (output ± 2 intermittently open) with spare. plan to repair old 45 card by replacing NOR 2s then replacing board into computer.

Repaired and replaced ON Dec 12, 1971

Also caught the machine hanging up in E and P seq with Clock phase 0 on and 1, 2, 3, 4 & 5 off

Dec 14, 1971

Problem with machine Jumping to loc called out by C (Accumulator) still present.

→ Repaired Power NOR XDA card (NOR 25 output)

→ Sequence hanging up semi-solid in Step 0, replaced GAH seq advance slot 6D with spare. outputs 20 & 26 Suspect

Dec 16, 1971

Bit 14 being dropped in some words, so memory line to 65

DEC 18 NEW INTERMITTENT, NO MEM LOC MESSED UP,
Program seems to skip interrupts (Bit 14 on chan)

Variables : most sens.	Clock	Slow Normal	Fast
least sensitive ⟷ 24V		Low	High (WORKS)
Medium + 24V		HIGH	Low (NO WORKS)

Accumulator does not get stored in ADD (Seq E-10,11) in following program:

```
ADD   300      loc 300 = 00001
JMP   -1
```

when worst conditions were set, lights on Maint panel showed that Accum was NOT being incremented

```
DCS   3        works OK, so Treg f-f
JMP   -1       and mem address gates are OK
```

```
LSH            doesn't work under worst
JMP   -1       case cond, and it has
               a double width set TIR=3
               in the xecute seq.
```

→ INSTEAD OF STORING ADDER INTO Accum (Loc 3) data is being stored into loc 2 (B register)

∴ Bit 0 of TR is not being set all the time in Step 9 of the E seq used for commands which store into Accumulator

12/18/71 Continues

→ Found bad GDH in slot 1R which was sensitive to power supply and clock margin NOR output 29 bad

12/26/71

STOPPED AT 0900 HRS SEQ STEP CLOCK = 00000

TR = 0 SEQ = E

ZR = 20000

XR = 00100 P = 00101

0 = 1

Restarted OK at 3733

1/2/72 0600 HRS Garage door was left open, bit 10 was picked up at loc 3612 which caused machine to jump to OCTAL dump continually for MONITOR. Fixed up loc 3612 at location IN Clock prog. which also picked up BIT 10 (00000)

Restarted OK at 3733

1/2/72 GHH in loc 5G replaced since symptoms point to JAZ NOT DETECTING A ONE IN BIT 2 or 3 IGNORE ABOVE SYMPTOMS, 5G put back since IT was determined that UC char was being transmitted by typer logic into CHAN 10 as zero

1/3/72 BIT 11 of TReg was comming on intermittently

→ GDH in loc 1M was replaced.

Symptoms point to BIT 11 NOT getting cleared during EIA last half when TR is set = 3

→ XGF in loc 1J was replaced

2/6/72

→ XGF in loc 1J was replaced because bit 12 was not being gated from bus into TR during ADDER→BUS→TR transfer in Step T11 and T12 of Sequence P.

Noticed that decrement instruction does not work for small locations like B. Works ok for loc 377. Following program was used for test:

10	DCS	T	When T=2, borrow seems to
12	JMP	-1	not progress between bits 7 & 8
			When T=377 DCS works fine

Cannot explain the above observation

2/7/72

XGF put into Loc 1J for 2/6/72 had intermittent bad bit 10

→ New XGF put into loc 1J

March 18, 1972

Setting of memory drive was at 7.0 and bit 10 was being grown in several locations.

Loc 6060 had picked up bit 10

6101 " " " " "

March 22/23 1972 Midnite

Bit 14 in both upper & lower bays was not coming on in Z when doing Locked ENA. Suspected bit 14 output gate of adder (card XGB in slot 4C) swapped with card in slot 4D and Bit 14 worked OK. Soldering on Bit 14 NOR of 4C looked marginal. Heated up the pins on circuit side with soldering gun and replaced the original 4C card back in slot 4C. Ran OK, restarted OK

MAY 10, 1972 Clocks did not advance after 2:00 PM

Basement cold, lowered drive to 5.00

```
6.[a3700.4000.[c[d
03700 14777 01733 07777 13704 01733 07767 15765 14767
03710 17775 17776 13722 07767 16773 17774 13727 07767
03720 10031 14777 01733 07767 17772 15771 14767 01717
03730 07767 17772 15765 01724 11020 16762 13677 11020
03740 16763 13701 10070 01600 01667 07767 17766 16761
03750 14767 10031 00000 07767 17766 16764 14767 10031
03760 01733 00526 66330 02000 00376 01000 77000 42376
03770 77777 20000 60777 23000 37000 17000 12000 00000
```

16776 bit 9 picked up

00000 bit 10 picked up

June 4, 1972 Replaced GDH in loc 1M to fix bit 11 of Freq which was accidentally being left on during the CLR TReg 8-12 time.

June 13 Turned ECHO on after being off for 2 days. Found that bit 10 in lower bay of core was coming up "1". Moved RA (read amp) card to bit 12, 13 in high bay of core. Trouble moved with card. Replaced RA card in bit 12, 13 of high bay with spare which says "bit 0 comes up 1 something". Runs OK

June 28, 1972

Tried to start machine after being off for 3 days. Found that -37 volt power supply in memory was only 30 volts. Changed 2.7K series resistor in base of Q4 circuit to 1.5K. Works OK now

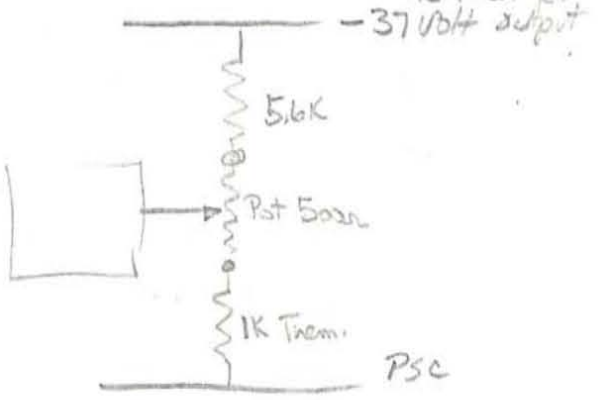
June 29, 1972 Stopped at 0300 hr.

Seq F, I & E are ON P = 00001
Chk all off Loc 1 = 0
AUTO mode
IR = 7 Inst decode = ENA
TR & XR = 00000 ZR = 77777
AD = 00000

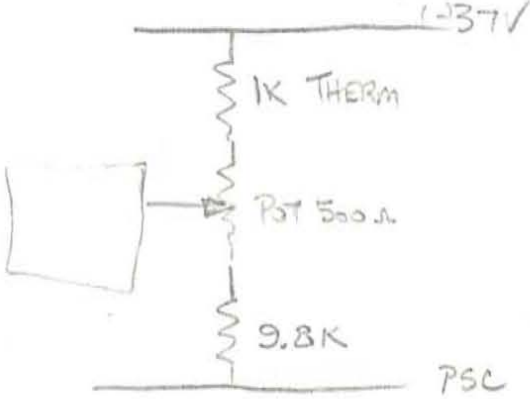
July 3, 1972

Since the -37 volt P.S. in memory system seems to oscillate when first turned on after being left off for several days, I decided to replace the regulator circuit. It was originally made of descrete components. The new regulator is a µA723. The 10 turn drive adj pot and Thermister were rewired as shown below to provide control range of 32 - 37 volts. Drive voltage was set to 34 Volts. with dial setting of 7.5

old Circuit for drive pot



NEW Circuit



AUG 7, 1972 – back from vacation trip to Washington

Bit 12 of Tregister would not stay set to ONE

GDH in slot 1M was replaced. Either output 15 or 29 is bad.

Power supply in memory came on fine after being off for 25 days.

NOV 11, 1972 No Hardware failures. Corrected Logic error in B seq by adding reset to XR_{14} from B seq. to keep from adding an end-around carry into effective address

NOV 22, 1972 Picked up bit 9 in loc 3740, 3700, 3711, 3601 because garage door was left open and basement got cold. Restarted OK. Drive dial still set at 7.5

NOV 23, 1972 Seems to occasionally get into a tight loop within the 3734-40 area and does not Jump to check the Sync interrupt. Clocks are incrementing OK, but the machine runs for longer time than it should because Decrement of Leadtime is not being performed 60 times each seconds.

→ Decoder XKA in slot 6L was removed and resoldered at NOR output pins, and replaced back in slot

Nov 29 ECHO gets out of prgm into tight loop, then proceeds OK back to running math. bit 12 of X Reg seems to disappear on Mant panel when freq of Zing changed to high pitch. Doesn't seem to be a function of memory drive voltage, clock time, PSN or PSP margin switch adjustments

Nov 30 Found out that JAZ is OK by exhaustively checking all possible single bit combinations. Saw that bit 6 of T register was hanging on during jump instruction at loc 3743 (1600) it seems that ECHO is jumping to location 3701 instead of 3601 and causing tight loop to occur.

→ Replaced transistors in 3 NOR packages and put same card (GDH) back into Slot 1P in CPU cage. The previous NORs were "red dotted" from Buffalo, and therefore they may have been "Slow NORs". Used NA-1 transistors. Since problem seemed to occur when temperature dropped, it may have been caused by bad resistor on 1P card, so if trouble persists, I'll change NOR packs associated with bit 6

Prob still with us...

Symptms:

1. Tight loop caused by Jmp to 3601 being done as if it were Jmp to 3702
2. Numeric print prog. Jmps into turn off power to computer routine. (enters loc 3660 or 3744 accidently) — Prog error due to INDIRECT ENA INSTEAD OF DIRECT
3. Message dump program fails to INCREMENT DUTCNT properly. for example: 6777 + 1 = 10000

~~Not~~ DEC 2 IN upper bay: bits 13, 0, 1, 2

lower bay bits 10, 8, cannot be cleared in reading/writing memory through Z register

Swapped XGG gates to memory in slots 1E ⇄ 1F and same bit pickup occured as above

Problem is sensitive to +24V margin setting. (fails with PSP set low)

+6V in Memory only reads 4.6 Volts

Dec 2 Made following changes to Memory System

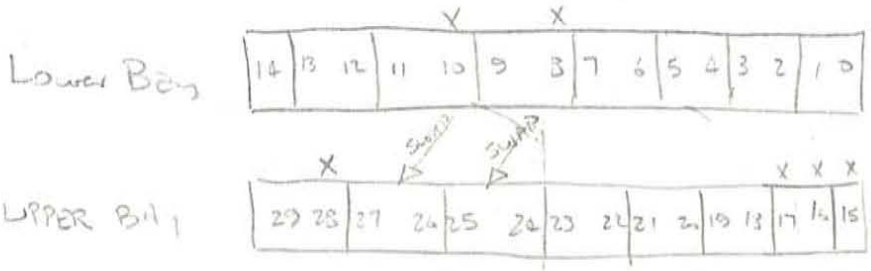
1. Moved Strobe timing downstream by 200NS.
2. Raised +6 (4.6 Volts) to be 5.4 volts
3. Increased drive setting to 9.0 (37 Volts)

→ Still have trouble with Jmp to 3601 being executed as Jmp to 3702

Dec 4 Picking up bits, so drive reduced to 7.5
changed Deadtime preset to 17000 from initial
count of 37000 so that it would decrement to
zero and turn off machine.
Loc 3740 had picked up bit 9

Dec 6 Lowered +6 back to 4.6 volts

JAN 1, 1973 RA-L Amp



JAN 8, 1973 Swapped back like they were before JAN 1, 1973

JAN 2, 1973 NOT INPUTTING ON CHAN 20 (CLOCK CHAN)
Replaced XKA char decoder in slot 11F
output pin 21 is driven for channel 20

JAN 15 1973
Same problem as 1/2/73 found that
swapping XGC in slot 11K was not
allowing input channel 20 be selected.
Swapped with XGC in slot 10T (bad output
would not hurt since input from magtape
would be not selectable)

Feb 18: 2:00 AM
Tight loop in clock progr — 3740, 3741, 3702 ok
because door to garage was left slightly open
and bit 9 of loc 3740 (EOR with Zero
became AND with Zero) so JAZ 3702 in
loc 3741 was always being taken.
9:00 AM Corrected the loc 3740 and restarted
OK.

April 7, 1973 Turned off power to CPU & CLOCK to reduce electrical load. Typer in Kitchen still receiving ⊖24 volts to run motor control & MOTOR light.

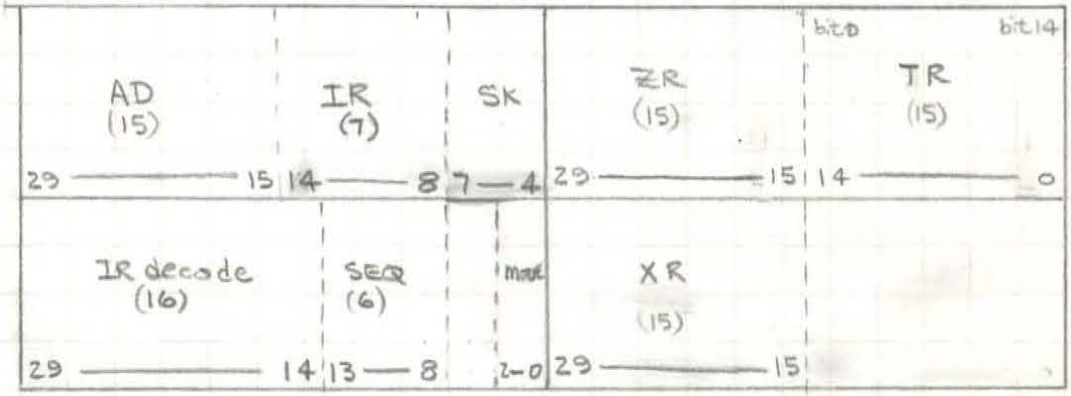
OCT 2, 1974 Replaced XDA in slot 6J

WESTINGHOUSE ELECTRIC CORPORATION

D		B		A		C	
IR	SEQ-Mem	AD	IR-SK	ZR	TR	XR	SWITCH
1	2	3	4	5	6	7	8

CONN

REAR VIEW



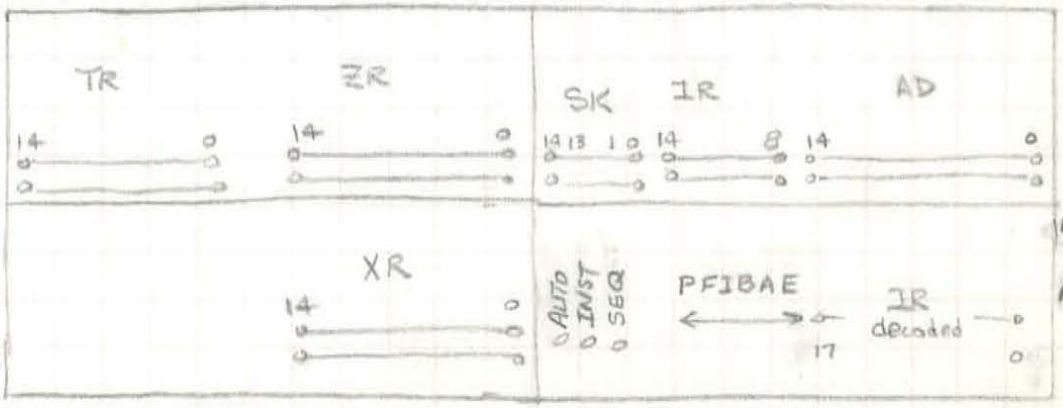
U = UPPER = complement → lamp on = 0 Volts
L = LOWER = TRUE

A & C Page 2, 3, 4, 29, 31, 33, 34, 35, 36, 37, 38, 40, 41, 42, 43, 44
45, 46

B Page 30, 31, 33, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46
D 27, 26, 28, 24, 25, 13, 23, 12

8 CONN TOTAL

A - 2 CONN B - 2 CONN C - 2 CONN D - 1 CONN POWER - SWITCH - 1 CONN

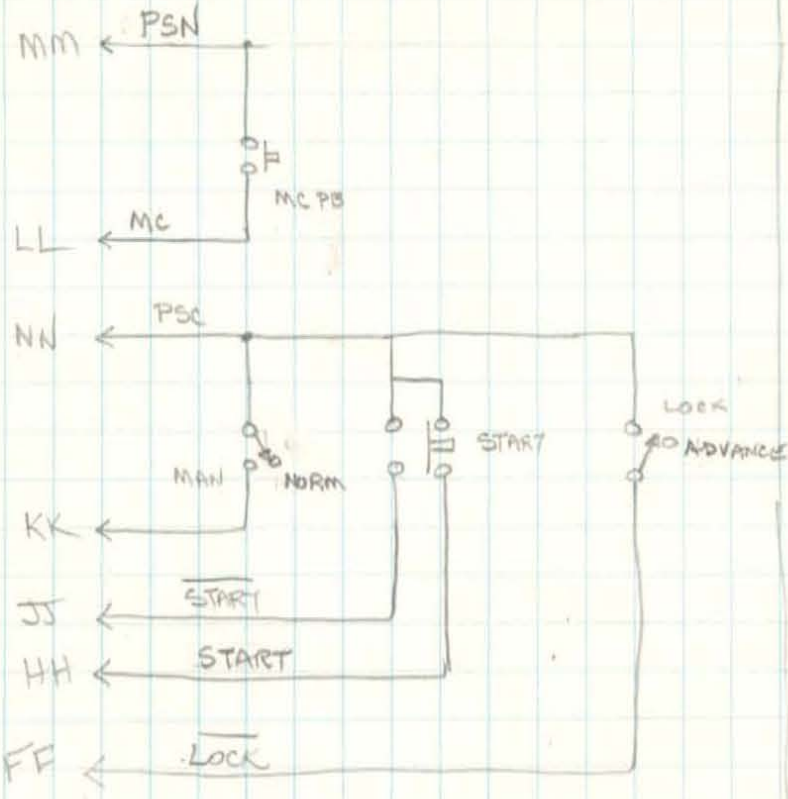


FRONT VIEW

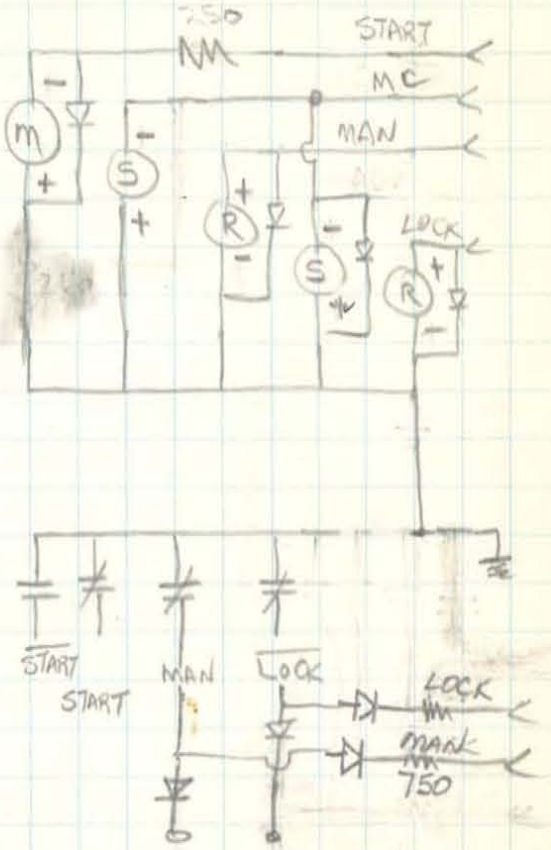
SKETCH SHEET
FORM 28577

WESTINGHOUSE ELECTRIC CORPORATION

CONN	X1	X2	X3	X4	X5	X6	X7	X8		
A	HLT	P		IR14	ZR14	TR14	XR14	$\overline{S5}$	C7U	
B	JMP	F	$\overline{AD14}$					$\overline{S4}$	C6U	
C	INT	I		IR13	ZR13	TR13	XR13	$\overline{S3}$	C5U	
D	COM	B	$\overline{AD13}$					$\overline{S2}$	C4U	
E	DCS	A		IR12	ZR12	TR12	XR12	$\overline{S1}$	C3U	
F	ESC	E	$\overline{AD12}$					$\overline{S0}$	C2U	
H	ENB			IR11	ZR11	TR11	XR11	C14U		SPARE
J	ENA	AUTO	$\overline{AD11}$					C13U		TL5
K	JOV			IR10	ZR10	TR10	XR10	C12U		TL4
L	OUT	INST	$\overline{AD10}$					C11U	future	TL3
M	JAN			IR9	ZR9	TR9	XR9	C10U		TL2
N	JAZ	SEQ	$\overline{AD9}$					C9U		TL1
P	STA	—		IR8	ZR8	TR8	XR8	C8U		TL0
R	ADD		$\overline{AD8}$					C7U		
S	EOR			SK14	ZR7	TR7	XR7	C6U		
T	AND		$\overline{AD7}$					C5U		
U				SK13	ZR6	TR6	XR6			
V			$\overline{AD6}$					ZING2		
W				SK1	ZR5	TR5	XR5			
X			$\overline{AD5}$					ZING1		
Y				SK0	ZR4	TR4	XR4			
Z			$\overline{AD4}$	—						
AA					ZR3	TR3	XR3			
BB			$\overline{AD3}$							
CC					ZR2	TR2	XR2			
DD			$\overline{AD2}$							
EE					ZR1	TR1	XR1			
FF			$\overline{AD1}$					$\overline{LOCK}$	23	
HH					ZR0	TR0	XR0	START	12	
JJ			$\overline{AD0}$		—	—	—	$\overline{START}$	12	
KK								MAN	sheet 10	
LL								MC	8D	
MM								PSN		
NN								PSC		
TT								VOLUME		
PP	$\overline{Block}$									

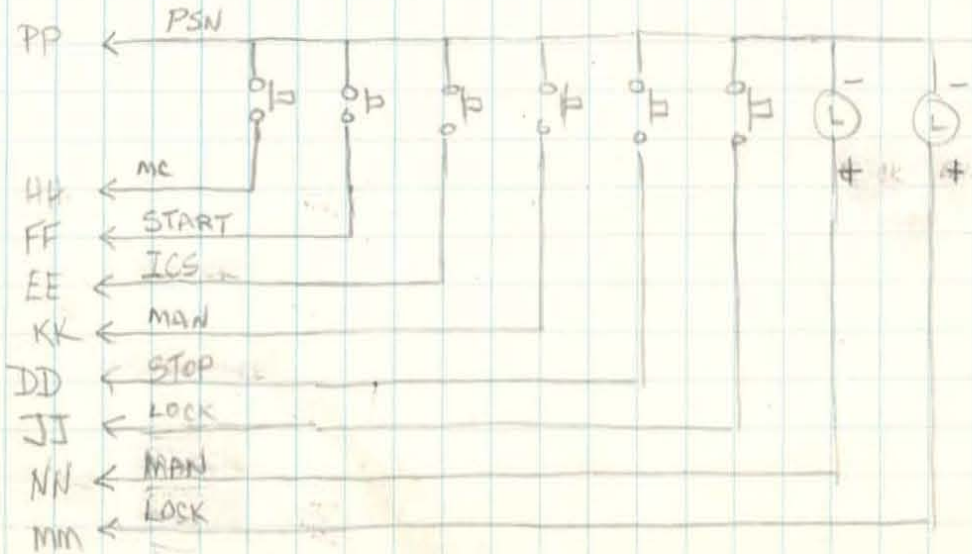


ORIGINAL SWITCHES ON MAINT. PNL.



RELAY

NEW PB/RELAY ARRANGEMENT
MAINTENANCE PANEL



WORK SHEET
WESTINGHOUSE FORM 8295 E

← = low
↓ = high

Scheme 2
Sheet 1

	1V24	1V16													
	1V27	1V18													
	1R28	1V19													
	1V13	1V20													
	1V17	1C12	1C30	1C31											
	1C15	1D30													
	1T17	1V14	1C19	6R29											
		1C20	1C24												
	1C7	1D4	1C28												
	1C11	1D20	1C29												
	1R11	1T19	7P12												
	1R15	1T20	7P14												
	1R19	1T21	7P13												
4N BUS	1D10	1D33													
12N BUS	1D13	1D34													
	7L10	7L8	7L30	7L32											
		7L16	7L18												
	7L19	7L9	7L23	7L25											
		7L7	7L5												
	6N14	7L4													
		7L6	6R19												
	1T24	1S4													
	1T27	1S11													
ZING	7L26														
ZING	7L21														
	7N17	7P15													
		6R16													

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 03
Sheet 2

TR14	1M7	1M22	A00U												
		1L5	X6B												
TR13	1M11	1M26	A01U												
		1L6	X6D												
TR12	1M15	1M33	1C10	4P29											
		1L7	1T30	X6F	A02U										
TR11	1M19	1M32	A03U												
		1L4	X6J												
TR10	1N7	1N22	A04U												
		1L8	X6L												
TR09	1N11	1N26	A05U												
		1L9	X6N												
TR08	1N15	1N33	A06U												
		1L10	X6R												
TR07	1N19	1N32	A07U												
		1L11	X6T												
TR06	1P7	1P22	A08U												
		1L27	X6V												
TR05	1P11	1P26	A09U												
		1L28	X6X												
TR04	1P15	1P33	A10U												
		1L29	X6Z												
TR03	1P19	1P32	A11U												
		1L35	X6BB												
TR02	1R7	1R22	A12U		1R7	OK11	1A4/T								
		1L31	X6DD												
TR01	1T13	1R26	A13U		1T13	6R28	OK15	1A4/U							
		1L33	X6FF												

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 03

Sheet 3

TR00	1T10	1R33	A14W		(1T10)	6RZ0	0K19	1ØA/V								
		1L34	X6JJ													
PSC	1L32															
TR14	1M20	1M4			(1M20)	1ØA/A										
		X6A	A00L													
TR13	1M24	1M8			(1M24)	1ØA/B										
		X6C	A01L													
TR12	1M29	1M13		X6E	(1M29)	1ØA/C										
		1C6	1T25	A02L												
TR11	1M28	1M16			(1M28)	1ØA/D										
		X6H	A03L													
TR10	1N20	1N4			(1N20)	1ØA/E										
		X6K	A04L													
TR09	1N24	1N8			(1N24)	1ØA/F										
		X6M	A05L													
TR08	1N29	1N13			(1N29)	1ØA/H										
		X6P	A06L													
TR07	1N28	1N16			(1N28)	1ØA/J										
		X6S	A07L													
TR06	1P20	1P4			(1P20)	1ØA/K										
		X6U	A08L													
TR05	1P24	1P8			(1P24)	1ØA/L										
		X6W	A09L													
TR04	1P29	1P13			(1P29)	1ØA/M										
		X6Y	A10L													
TR03	1P28	1P16			(1P28)	1ØA/N										
		X6AA	A11L													

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 03
Sheet 4

TR02	1R20	1R4		1R20	1DA/P											
		X6CC	A12L													
TR01	1R24	1T5		1R24	1DA/R											
		X6EE	A13L													
TR00	1R29	1T4		1R29	1DA/S											
		X6HH	A14L													
	1J20	1M6														
	1J21	1M9														
	1J23	1M12														
	1J25	1M17														
	1J27	1N6														
	1J31	1N9														
	1J30	1N12														
	1K20	1N17														
	1K21	1P6														
	1K23	1P9														
	1K25	1P12														
	1K27	1P17														
	1K31	1R6														
	1K30	1T11														
	1K29	1T6														
	1J8	1J19														
		1M23														
	1J7	1J22														
		1M27														
	1J10	1J24														
		1M35														

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 03
Sheet 5

1J12	1J26						1S27	5N29						
	1M34													
1J14	1J28													
	1N23													
1J16	1J35													
	1N27													
1J18	1J33													
	1N35													
1K8	1K19													
	1N34													
1K7	1K22													
	1P23													
1K10	1K24													
	1P27													
1K12	1K26													
	1P35													
1K14	1K28													
	1P34													
1K16	1K35													
	1R23													
1K18	1K33													
	1R27													
1J29	1K32													
	1R35													
5N19	6R30													
	6R21													

WORK SH..T
WESTINGHOUSE FORM 8295 E

Scheme 04
sheet 6

PSC • 1F32															
T14	1E16	1F16	1H6	2E33	4D14	4E24	6H5								
		1L13	1J6	2C33	4C13	4F13	4N13								
T13	1E14	1F14	1H5	2E35	4D15	4E13	6H11								
		1L14	1J5	2C35	4C14	4F14	4N14								
T12	1E12	1F12	1H9	2E28	4D16	4E14	6H15								
		1L15	1J9	2C28	4C15	4F15	4N15								
T11	1E19	1F19	1H11	2E26	4D17	4E15	6H19								
		1L16	1J11	2C26	4C16	4F16	4N16								
T10	1E21	1F21	1H13	2E24	4D18	4E16	6H24								
		1L17	1J13	2C24	4C17	4F17	4N17								
T09	1E23	1F23	1H15	2E22	4D12	4E17	6H28								
		1L18	1J15	2C22	4C18	4F18	4N18								
T08	1E25	1F25	1H17	2E19	4D19	4E18	6H33								
		1L12	1J17	2C19	4C12	4F12	4N12								
T07	1E24	1F24	1H19	2E17	4D26	4E12									
		1L19	1K6	2C17	4C19	4F19	4N19								
T06	1E22	1F22	1H22	2E15	4D25	4E19									
		1L26	1K5	2C15	4C26	4F26	4N26								
T05	1E20	1F20	1H24	2E13	4D20	4E26									
		1L25	1K9	2C13	4C25	4F25	4N25								
T04	1E11	1F11	1H26	2E11	4D21	4E25									
		1L20	1K11	2C11	4C20	4F20	4N20								
T03	1E13	1F13	1H28	2E9	4D22	4E20									
		1L21	1K13	2C9	4C21	4F21	4N21								
T02	1E15	1F15	1H35	2E5	4D23	4E21									
		1L22	1K15	2C5	4C22	4F22	4N22								

WORK SH .T
WESTINGHOUSE FORM 8295 E

Shame 04
Sheet 7

To1	1E17	1F17	1H33	2E6	4D24	4E22									
		1L23	1K17	2C6	4C23	4F23	4N23								
Too	1E18	1F18	1H32	2E32	4D13	4E23									
		1L24	1J32	2C32	4C24	4F24	4N24								
	1H8	1G6													
	1H7	1G5													
	1H10	1G9													
	1H12	1G11													
	1H14	1G13													
	1H16	1G15													
	1H18	1G17													
	1H20	1G19													
	1H21	1G22													
	1H23	1G24													
	1H25	1G26													
	1H27	1G28													
	1H31	1G35													
	1H30	1G33													
	1H29	1G32													
PSC	1H4	1G4													
SCHEMS 5 ↓															
CINH	6C24	3R21	3V21	2V21	2R21	2P21	2L21	2K21	4H33						
		3S21	3T21	2T21	2S21	2N21	2M21	2J21	2H21						

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 05
Sheet 8

												TB3/6			
MC	6C5	6C6	6C17	6C27	6J22	7C26	7G18	5C30	5S5	5D8	5F29	X8LL	6C5	6S9	
		6F4	6F22	6J34	6J31	7D30	7G31	5S16	5S29	5D11	5D7				
														5K25	
	7T8	6J8												5K27	7C20
Clock	7R16	7T18													
	7T9	5J28													
PSC	6D9														
6J14	~~6C25~~	6D21	6E22	6E24											
		6D25	6E6	6E4											
5J25	~~6C24~~	6D32	6E14	6E32											
		6E19	6E33	6E5											
SO	6C15	6D24	5E4	5G33	4J16	IOC/X			6C15	4S33					
		6D17	5E5	7H18	5T17					4M18	4L18				
	6D23	6C10													
SI	6C13	6D35	4M27	4L22											
		6E7	5S22	4R35											
	6E10	6F6													

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 05
Sheet 9

PSC	6E9	6E30														
	6F10	6G23														
	6E12	6F23														
	6F24	6G15														
	6E15	6C18														
S4	6C16	6E21	5E30	4J29	6R17	IDC/S		6C16	6C32							
		6C20	5C19	4M17	1V29											
	6E20	6C31														
S5	6C26	6E28	5G31	7H16	4M6	4L14	IDC/T		6C26	5R6						
		6E35	5G18	5L19	5T16	4S35	OH32		6F15	6F29						
	6E27	6D19														
		7J11														
	6D18	6G31														
	6D20	6D31														
	6D26	6G27														
	6D29	6D28														
S2	6D27	6E8	1V28	X8D		6D27		IDC/Y								
		6F7	5S23	C4U												

WORK SH..T
WESTINGHOUSE FORM 8295 E

Scheme 05
Sheet 10

	6E13	6C8														
S3	6C14	6E17	5L18	5R12	4L13	4L23			(6C14)	4M26	OH30	7D15				
		6F25	5G6	5R23	4M5	X8C	C5U					6F11	6F31			
	6E18	6C21														
S4	6C23	6C19	5N35				6C23	OH31	5R4	1C9						
		6E25	5G16	X8B	C6U			7M16	7M5	1C5	IOC/DD					
	6E23	6E31														
	6E26	6G11														
	6E29	6C7														
S0	6G34	7H28		X8F		6G34	OG25	4H15	4H25	6D22	6C9					
		4R34	1V22	C2U			OH29	1V7	7M6							
S1	6G30	5E6	5L30	4P34	4J18	6C30			(6G30)	6C11	C3U					
		5E11	5J30	3M14	4L27	OJ6	IOC/BB			6D34	X8E					
S5	6G12	5C20			4L26		1T29	1R32	1V11	1V8	X8A/C7U	6G12	4S34	7M15	6E34	
		5E31	7H30	4M13	4L35	4J30	1T23			4H12	4H26		6R18	OG24	(6C35)	
S2	6G24	5G4	5R22	5R11	1T28	1T22	IOC/CC		(6G24)	6D33						
			4L17	4R35	5N34	1V23	OJ25			6E11				IOC/AA		
S3	6G16	5L31	1V5	1R30	4S32		6E16	6C4	(6G16)		IOC/Z					
		4L33	4P35	1C8	1C4	OG31	OG30	5J		7M11	7M17					
NORM-MN	5F8	6P22														
		6P28	X8KK													
	6P24	7R15														
	6P27	7D10														

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 06
Sheet 11

HP	6S10	6S22	6D7													
	6V10	6S7														
PSC		6S30														
		6T9	6T30													
$\overline{HP}$	6S20	6S5	0J13													
		5T18	7C11													
	6V20	6S21														
HF	6S12	6S25	7L17	7L20	1S28											
	7C10	6S11														
	7D10	6S24														
$\overline{HF}$	6S23	6S6	7E33	7F25												
		7D26	7D20	0J10												
	6V12	6S8														
	6V23	6S31														
	6S13	6S35														
		6N35														
$\overline{HI}$	6S26	6S4														
	6N31	7G15														
		7E12	7E26													
	6V13	6S16														
	6S15	6S33														
	6V26	6S28														
$\overline{HB}$	6S27	6S14	6R12													
		7E19	7F30													
	6V15	6S19														
HA	6S18	6S34	0H23		6S18	4R20										

WORK
WESTINGHOUSE FORM 8295 E

Scheme 06
Sheet 12

	6V27	6S32														
HA	6S29	6S17														
		7G7														
	7F10	6T8														
LOCK	6T13	6T14				(GT13)	7J19	7N13		X8FF	7M22	7N8				
	7F13	6T16						7N15	(HE)	7N14	5G30					
HE	6T15	6T4	DJ31	I&C/W												
		7C30	5T18													
	5J14	6V9	7F8	7D7										7HZ7	5J8	
		6V30	7F12	7C8												
AUTO	6T18	7G19	D00U				(6T18)	5CZ8								
		7G22	X2J													
INST	7G17	7G25	X2L	D01U			(7G17)	7P17								
		6N17	6T17													
SEQ	7G24	7G16	X2N	D02U			(7G24)	7P16								
		6N15	6T19													
SEQ STEP	6N16	5J27														
		5J20	6V34													
INST STEP	6N18	6N32														
		6T21	6V17													
START	6N20	6N22	6P23	X8JJ												
		6T22	5J31													
START	6N21	6N19	6P29	X8HH												
		6N34	5J21				7K19	7J9								
	5J26	6V33	6V25	6V5	6V6	7F5	7C6									
		6V35	6V21	6V4	6V14	7F6	7D4									
MEMOK	7G23	7G21	TB3-7													
	AR16															

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 06
Sheet 13

P	6T10	6V7													
		6J30	6F19												
	6T29	6J21	4P33												
		5R25	4M30												
$\overline{P}$	6J24	6V22	5R14				1R34	X2A		6J24	0G29	0H33	0H27		
		6T34	6T5	5L29	4J19	4P7	4R24	D08U			0G23	0G32	6V19	4R27	
F	7C24	7C7													
		6J29													
	6T27	6T7			6T27	0J26									
		4L10													
$\overline{F}$	6J25	7D6	5G19	5J34	4P25	4M12	D09U		6J25	6T33	4V29				
		7C22	5E12	5T31	4R13	4L25	X2B			5R7	5T32				
I	7G27	7C23	4L9	1S29											
		6T6	6V11												
$\overline{I}$	6T12	6V24	X2C	D10U		6T12	5S8	7M4							
		7G28	4P21												
B	7D27	7E4	4S21												
		6V8	6T35												
	6T23	7G29	5R32	3R32											
		7C25	5S25												
$\overline{B}$	7E10	7D28	X2D	D11U		7E10	4S30								
		6T25	6V31												
	6T26	4M25	4L31												
		4P15	4L21												

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 06

Sheet 14

A	6J26	6J17	7D29	5R35	1V25			6J26	7G30	4S12	0J21				
		6V16	7C32	4P30	4P31										
A	6J16	6J27	4L4	5F26	4M4		D12U								
		6V28	5N15	4L12		1V30	X2E								
E	6J23	6J35		7D31	7G33	1S30									
		7F21	7F7	7C35	5P19										
E	7F17	6G5							6D16	7M12	6J20	7F11			
									6G6	7M18	0M4	X2F	D13U		
	6G6	5N25	5N7	5N32	5L16	5G7	5D21	4H5	4P12	4P6	4R12	4R18	6N13	1V4	
		5N16	5N12	5T5	5T21	5E7	5E29	4H22	4J31	4P18	4R7	1V12	7D14		1DC/V
	7C27	6J32													
	7C13	6J28													
	7D24	6T11													
	7D17	7E6													
	7E13	7E7													
	7E17	6J18													
	7E24	6J19													
	7E27	5F30													
		5F27													
	7F24	7F20													
	7F27	7F19													
	7G10	7F18													
	7G13	7F16													
	5J23	7G12	7F22	7E30	7E5	7D18	7C28								
		7G4	7F28	7E23	7E16	7D23	7C5								
	5J16	7G14	7F23	7E31	7E11	7D19	7C29							7H17	5J17
		7G6	7F29	7E25	7E18	7D25	7C12								

WORK SH. .T
WESTINGHOUSE FORM 8295 E

Scheme 06
Sheet 15

6T20	7F14
10V18	7K7
6V29	7K6
7K10	7K20
STOP 7K17	7K8
	7J8
7D13	7G20
	5C29
6D10	4M16
$\overline{HP}$	4L16

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 07
Sheet 16

	4P8	4V4	
	4P9	4V6	
	4P11	4V7	
	4M7	4V8	
	4P14	4V9	
	4V10	4T31	
LXR	4T34	2C34	2D34
		2C4	2D4
	4V24	4P16	
		4K20	
	4P17	4M8	
	4M15	4M9	
	4M11	4T27	7J28
	4P19	4M10	
	4M19	4V5	
		4V18	
	4S28	7J30	
	4M24	4V20	
		4V14	
	4P22	4V21	
		4M31	
	4V13	4T23	7P11
	4V17	4T15	5K19
	4M29	4T11	

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WESTINGHOUSE FORM 8295 E

SCHEME 07
Sheet 17

LZR	4T30	2E34	2F34												
		2E4	2F4												
LTR813	4T24	1J4													
LTR07	4T16	1K4													
		1K34	1J34												
LIR	4T12	6H4													
	4R8	4T5													
	4M28	4R6	0K20												
	5T7	4M32													
CLRZ	4T6	2H30	2L30	2M30	2R30	2S30	3V30	3T30							
		2J30	2K30	2N30	2P30	2T30	2V30	3S30	3R30						
	5T11	4R5													
CLRZ8-14	4R9	3R33													
		3S33													
CLRZ81-4 SETZR0	4H24	2M31	2K31	2L31											
		2H15	2J31												
CLRZR8-12	4H13	3T31	2T31	2S31											
		3V31	2V31												
	4R11	5V31													
SETXR7776	5V34	2H25	2L7	2M7	2R7	2S7	3V7	3T7							
		2J7	2K7	2N7	2P7	2T7	2V7	3S7	3R7						
	5T15	4R16													
CLRXR	5V30	2H26	2L26	2M26	2R26	2S26	3V26	3T26		*	5V30	wired to	3R26		
	(3R26)	2J26	2K26	2N26	2P26	2T26	2V26	3S26	3RZ6						
CLRZR13457	1V10	2R31	3R31	3S31											
		2P31	2N31												

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WESTINGHOUSE FORM 8295 E

SCHEME 07
sheet 18

	5T20	5S26														
	5T24	5T22			5T29	0K7										
	5T29	5S32														
	5S10	5S35	6R24													
	5T28	4K26	7J24													
	5T19	5S11	7J31	7J33												
		5S20	5S30													
	5S24	5S12	4K24													
		5S18	5S33													
	4L7	4K25														
	4R14		5S34													
		5S19	5S15													
	5S13	5P5														
	5S17	5P6														
		5P4														
	5S27	5P14	6R11													
	5R10	5S28														
PSC		5P9														
CLR TRIB 14	5P10	1M21														
		1M25														
1 (CLR TRO-7)	5P12	1N30	1P31	1P30												
		1P21	1P25													
2 (CLR TRO-7)	5P13	1R21														
		1R25	1R31													
CLR TRB-12	5P15	1M31	1N21	1N31												
		1M30	1N25													
	7M21	7M9			7M21	7J16										
		5G9	4K27													

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 07

Sheet 19

(STR4)	5R13	0K9													
STR2	5R24	4K29													
		1T12													
	5P18	5R26													
	4L11	4K31													
	4V27	4K33													
	4S29	5S21	6R15												
		5S14	6R8												
	4S24	4S31													
	4S7	4P10													
	5K15	5F9													
		4M34													
	0M8	0K22													
	5T15	6D14													
	6D15	5V27													

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WESTINGHOUSE FORM 8295 E

SCHEME 08
Sheet 20

	4P26	5P22	7P21												
	4L15	5P21	7P22												
PSC	5P30														
	5P20	OL35													
UDA	5V24	1F31													
	4P28	5P25	4P32	7P25											
	5P23	OL28													
UDB	5V16	1E31													
	4L19	4L30	7P35												
	5N9	4L32	7P31												
	5L24	5N5													
		4K28													
	4L20	4L34	7P33												
	4L28	OL5													
UAS	5V12	4C30													
	4L24	5P35	7P30												
	4L29	5P31	7P32												
	5P26	OL14													
UTR	5V6	1L30													
	5N11	5P33	7531												
	5L10	5N10													
	5N14	5P28	H-4V15	4V19	6R7	7533									
	5P27	OL8	7P7	5K20											
UZR	5M34	4N30													
	5N17	5P34													
	5P29	5M27													

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SCHEME 08
Sheet 21

$\overline{UAC}$	5M30	4F30														
	5N22	5L5														
		5K7														
	5L13	5M23														
	5N26	5K11														
		4M21														
	4M20	5M15														
$\overline{UAL}$	5M16	4D30														
$\overline{UAR}$	5M24	4E30		5M24 ⊕ 5N6												
	5L27	5J5														
	5L17	5K18	7P6	7P8												
	7M10	7M8	4V11	7S29												
		5K21	4V16													
$\overline{SK \rightarrow ZR}$	5J15	3N30	4J23													
		3N31	3P34													
	OL10	OL6														
	OL12	5V11	7P29													
	OL15	OL17														
	OL18	5V5	7P28													
	OL13	OL21														
	OL20	5M31	7S28													
	OL26	OL34														
	OL27	OL25														
	OL29	5V23	7P20													
	OL23	5V15	7P24													
↓ Scheme 9	4S15	4R21														

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WESTINGHOUSE FORM 8295 E

SCHEME 09

Sheet 22

	5G13	5G8													
STR31	5G10	1T7													
		1T14													
STR32	4R19	1T9													
		1T15													
STR4	5J24	5F10	6K9	6J9											
		1R5	6P12												
	5G24	5H5	5F21												
		5F14	5F19												
PSC	5H9														
XR=ZERO	5H10	1R9													
	5H12	5H4													
	5H13	5H11													
		5G28													
SYNC	5H8	5G29													
	5G27	5H22													
	5H23	5H21													
		5H6													
	5G17	5H24													
	5H26	5H17	5G34												
		5H33	5G20												
	5H20	5H19													
		5H25													
INTERLOCK	5H15	5F4	4R15	4R30											
		5F6	5R5												
INTERLOCK	5H18	5H14													
		4F24	4R23												

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WESTINGHOUSE FORM 8295 E

SCHEME 09

Sheet 23

	5E13	5H31											7M14	7N11	
	5H27	5H35	7P19											7J21	
	5H29	5E8	7M28	7S19									7M19	7M27	
	5E10	5H28												7N9	
PSC	5D30												7N19	7P18	
	5D20	5D28	5C11											X1PP	
		5C18	5C23										4R26	5K32	
SK13	5D10	5D24	X4U	B05L		5D10	7J20							7J13	7C18
SK13	5D23	5D5	B05U	X4V		4J22	5K29	6F34				INTLOCK	7H10	7M29	
		4J22	X4V											7C16	
SK14	5D12	5D35	X4S	B04L		5D12	7M26					INTLOCK	7C17	7H9	
SK14	5D26	5D6	B04U			3P32	6F12								
		3P32	X4T												
SK01	5D13	5D33		B06L		4R25	5K28	5D16							
		4R25	X4W												
SK01	5D27	5D4	B06U												
		3N33	X4X												
SK00	5D15	5D34	X4Y	B07L		5D15	7J15								
SK00	5D29	5D14	X4Z	B07U											
		5F28	3N32												
	4R22	5D32													
	4J27	5D31													
	5E27	5D25													
	5E17	6P16													
	5E24	6P18													
	4J17	5K30	7J12												
	5N8	5K31													
	6P17	5E34													

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WESTINGHOUSE FORM 8295 E

SCHEME 10
Sheet 24

	6L9	5M11															
	6L10	5M5															
PSC	6N4	6K30	6M4				OUT	6L17	6M28	XIK	D21U		6M28	0J29	0K6		
ADD	6N10	5L25	4V25	1C17			JOV	6L24	6M26	6R4	4S25				7S18		
		5H32	5G12	XIR	D16U			6L27	6M24	6R5	4S26	6N11	7M35				
STA	6L13	6M32	1C18	XIP	6L13	7M31		6L26	6M22								
		5T25	5L26	D17U				6L12	6N28								
JAZ	6L14	6M33	XIN	D18U				6N12	4P4								
		5T10	5L4														
JAN	6L15	6M35	XIM	D19U													
		5T9	5L6														
JOV	6N30	5T8	4L6			7J26	4S4										
		5S7	5L8	XIC	D27U												
ENA	6L30	5T12	4V26	1C25	6L30	7M33											
		5L32	5G14	XIJ	D22U												
ENB	6L28	5T13	4L8	1C21	6L28	7S20											
		5L35	4V32	XIH	D23U												
SIP	6N7	5S6	4K30	1C22		7J25	0K5										
			4L5	XIF	D24U												
DCS	6N8	5H34	XIE	D25U				4V35	4K32								
		4V35							1C27	5T26							
COM	6L25	6M19	4K21	1C23													
		5T14	5T27	XID	D26U												
INP	6L16	5L9	XIL	D20U	1T16	0J32											
		5G15	1T16			0K25	7S17										

SCHEME 10
Sheet 25

JMP	6L22	5L7	D28U			1T18	7N18	7S16							
		1T18	X1B												
MIC	6L21	6M17	D29U			6M17	6R25	5T34							
			X1A				5T35	4S5							
ADD	6N27	6N9	7M20												
		5E28	4J33												
STA	6M29	5T4													
JAZ	6M30	1R8													
JAN	6M31	1R16													
OUT	6M27	I&C/P													
JOV	6M25	6N33			6M25	7M13									
		1R12													
SIP	6M23	6N5	4H13	1V6											
		5L20	4H11												
DCS	6M21	6N6													
		5D22	4R10												
COM	6M20	5N18													
MIC	6M18	7D12	5K13	5N21											
		5N30	5N24	1S22											
PSC		6L35													
	6K10	6H32			6K10	7S16									
		X4A	B08L												

(MIC) 1S24 6R31

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SCHEME 10

Sheet 26

IR14	6H29	6K7	5N27	X4B			6H29	5T33									
		6N24	7D22	B08U				4V28									
IR14	6N23	5N23	7D21	7D5													
		7F35	7E29	X4A													
IR13	6K20	6K6	7D16														
		6N26	7E14	X4D	B09U												
IR13	6K12	6K22	X4C	B09L			6K12	5S9	7J27								
			5P17														
	6N25	7G11	7E32														
		7F32	7E34														
IR12	6J13	6J5	7E22	7E28			6J13	4S16									
		6L5	7E20	X4F	B10U												
IR12	6J15	6J6	7F31	7F26			6J15	7J29	5S4	4S27	5K24						
		6L34	7G5	X4E	B10L												
IR11	6K23	6K4	X4J	B11U													
		6M5	6L33														
	6M8	6L6															
IR11	6K13	6K25	X4H	B11L													
		6M6	6L20														
	6M7	6L19															
IR10	6K26	6K14	X4L	B12U													
		6M11	6L32														
	6M10	6L7															
IR	1S17	5K14															

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SCHEME 10

Sheet 27

IR10 { 6K15 • 6K35 (X4K) • B12L
6M9 • 6L23
6M12 • 6L18

IR09 { 6K18 • 6P6 (X4N) • B13U
6M15 • 6L31
6M14 • 6L8

IR09 { 6P10 • 6K17 (X4M) • B13L
6M13 • 6L29
6M16 • 6L11

IR08 6K27 • 6P5 (6K27) ▲ 5K4
X4R • B14U
IR08 6P13 • 6K33 B14L (6P13) ▲ 7D11 • 5K8 ▲ 1S18
5R8 X4P
6H7 • 6H6
6K5
6H8 • 6H34
6H12 • 6H9
6K11
6H10 • 6K21
6H16 • 6H13
6J7
6H14 • 6J10
6H20 • 6H17
6K8

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Scheme 10
Sheet 28

6H18	6K24														
6H23	6H22														
	6K16														
6H21	6K31														
6H27	6H26														
	6P4														
6H25	6K19														
6H30	6H35														
	6P11														
AND 5M12	5L22	4J6	7H12	3C4	3C21	3E4	3E21	3G4	3G21	3J4	3J21	3K31	3L4	3L30	
	5G5	4V22	4H7	4G12	3D4	3D21	3F4	3F21	3H4	3H21	3K4	3K21	3L16	3L25	
	3M12	3M31	3N8	D14U											
	3M21	3N16	1C26	X1T											
EOR 5M6	5L23	3V19	3T19	3K17	3J32	3H17	3G32	3F17	3E32	3D17	3C32	2J19	2K19	2N19	
	5G11	4V23	3S19	3R19	3J17	3H32	3G17	3F32	3E17	3D32	3C17	2H19	2L19	2M19	
	2P19	2T19	2V19	D15U											
	2R19	2S19	1C16	X1S											
(B) 4S20	6C28														
(B) 6C25	6L4														
(IR12) 4S19	5T30														
6H31	6K28														

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WESTINGHOUSE FORM 8295 E

SCHEME 11

Sheet 29

	2C29	2D32														
		2H23														
	2D29	2H4														
XR00	2H24	2H6	X7HH	C29L		(2H24)	AIDD/S									
		3C5	5G22													
XR00	2H10	2H22	C29U			(2H10)	AIDD/X									
		3C8	X7JJ													
	2E29	2F32														
		2H29														
	3N28	2H12														
	2F29	2H5														
PSC	4N32															
ZR00	2H13	2H28	4N34	X5JJ												
		3C9	3P6	A29U												
ZR00	2H27	2H11	X5HH	A29L												
		3C6	3P19													
V00	3C7	3C13														
		2H16	4G35													
W00	3C11	3C12	2H18													
		3K22	4G32													
	2H17	3K23														
		3C14	3C16													
	3C19	3K26														
	3C15	3K25														
COT00	3K20	3C34														
		2J20														

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WESTINGHOUSE FORM 8295 E

Scheme 11
Sheet 30

ADDD	3K24	2G32	[illegible]	X3JJ		3K24	5N4								
		4C34	4D34	B29U											
	2G29	4F34													
		5C4													
PSC	4C32	4D32	4E32	4F32											

SCHEME 12

Sheet 31

	2C8	2D6														
		2J23														
	2D8	2J4														
XR01	2J24	2J6	X7EE	C28L		(2J24)	IDD/R									
		3C22	5G23													
XR01	2J10	2J22	C28U			(2J10)	IDD/W									
		3C25	X7FF													
	3N29	2J12														
	2E8	2F6														
		2J29														
	2F8	2J5														
ZR01	2J13	2J28	4N33	X5FF												
		3C26	3P5	A28U												
ZR01	2J27	2J11	X5EE	A28L												
		3C23	3P22													
V01	3C20	3C33														
		2J16	4G26													
W01	3C24	3C31	2J18													
		3K33	4G25													
	2J17	3C30														
		3C35	3K35													
	3C28	3K32														
	3C29	3K30														
C0T01	3K29	4G9														
		3D18	2K20													
AD01	3K28	4C33	2G6	5C5												
		4D33	4E33	X3FF	B28U											

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SCHEME 12

Sheet 32

2G8 4F33

SCHEME 13

Sheet 33

2C7	2D5													
	2K23													
2D7	2K4													
2K10	2K22	C27U			(2K10)	I0D/V								
	3D8	X7DD												
2K24	2K6	X7CC	C27L		(2K24)	I0D/P								
	3D5	5G25												
2E7	2F5													
	2K29													
2F7	2K5													
2K13	2K28	4N31	X5DD											
	3D9	3P9	A27U											
2K27	2K11	X5CC	A27L											
	3D6	3P24												
3D7	3D13	4G23												
	2K16	4G8												
3D11	3D12	4G7	4G22											
	3L5	2K18												
2K17	3D16													
	3D14	3L6												
3D15	3L8													
3D19	3L9													
3L7	3D34													
	2L20													
3L11	4C31	2G5 H	5C10											
	4D31	4E31	X3DD	B27U										
2G7	4F31													

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WESTINGHOUSE FORM 8295 E

SCHEME 14

Sheet 34

2C10	2D9													
	2L23													
2D10	2L4													
2L10	2L22	X7BB			2L10	I0D/U								
	3D25	C26U												
2L24	2L6	X7AA	C26L		2L24	I0D/N								
	3D22	5G26												
2E10	2F9													
	2L29													
2F10	2L5													
2L13	2L28	4N35	X5BB											
	3D26	3P11	A26U											
2L27	2L11	X5AA	A26L											
	3D23	3P26												
3D20	3D33	4K18												
	2L16	4G6												
3D24	3D31	4K17	4G14											
	2L18	4G4												
2L17	3D30													
	3D35	4G15												
3D29	3L12													
3D28	3L13													
4G10	4G11													
4G24	4G5													
	4K19													
4G13	4K12													
	3E18	2M20												

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WESTINGHOUSE FORM 8295 E

SCHEME 14
Sheet 35

3L15	4C35	2G9[H]	5G12											
	4D35	4E35	X3BB	B26U										
2G10	4F35													

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SCHEME 15

Sheet 35

2C12	2D11													
	2M23													
2D12	2M4													
2M10	2M22	C25U			2M10	IDD/T								
	3E8	X7Z												
2M24	2M6	X7Y	C25L		2M24	IDD/M								
	3E5	5G32												
2E12	2F11													
	2M29													
2F12	2M5													
2M13	2M28	4N29	X5Z											
	3E9	3P13	A25U											
2M27	2M11	X5Y	A25L											
	3E6	3P28												
3E7	3E13													
	2M16	4G34												
3E11	3E12	4G33												
	2M18	3L17												
2M17	3E16													
	3E14	3L18												
3E15	3L21													
3E19	3L22													
3L19	3E34													
	2N20													
3L20	4C29	5C13 HOL	2G11											
	4D29	4E29	X3Z	B25U										
2G12	4F29													

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WESTINGHOUSE FORM 8295 E

SCHEME 16
Sheet 36

2C14	2D13													
	2N23													
2D14	2N4													
2N10	2N22	C24U			(2N10)	IDD/AA								
	3E25	X7X												
2N24	2N6	X7W	C24L		(2N24)	IDD/L								
	3E22	5G35												
2E14	2F13													
	2N29													
2F14	2N5													
2N13	2N28	X5X	A24U											
	3E26	4N28												
2N27	2N11	A24L												
	3E23	X5W												
3E20	3E33													
	2N16	4G31												
3E24	3E31	4G30												
	2N18	3L26												
2N17	3E30													
	3E35	3L27												
3E29	3L31													
3E28	3L33													
3L24	2P20													
	3F18	4G21												
3L29	4C28	5C14	2G13											
	4D28	4E28	X3X	B24U										
2G14	4F28													

WORK S. .T
WESTINGHOUSE FORM 8295 E

SCHEME 17

Sheet 37

2C16	2D15													
	2P23													
2D16	2P4													
2P10	2P22	C23U			2P10	I&D/Z								
	3F8	X7V												
2P24	2P6	X7U	C23L		2P24	I&D/K								
	3F5	5F22												
2E16	2F15													
	2P29													
2F16	2P5													
2P13	2P28	X5V	A23U											
	3F9	4N27												
2P27	2P11	A23L												
	3F6	X5U												
3F7	3F13	4G29												
	2P16	4G20												
3F11	3F12	4G28	4G19											
	2P18	3L32												
2P17	3F16													
	3F14	3L34												
3F15	3M4													
3F19	3M5													
3L28	3F34													
	2R20													
3M7	4C27	2G15*	5C22											
	4D27	4E27	X3V	B23U										
2G16	4F27													

WORK S[illegible]T
WESTINGHOUSE FORM 8295 E

SCHEME 18
Sheet 38

2C18	2D17													
	2R23													
2D18	2R4													
2R10	2R22	C22U			2R10	IDD/Y								
	3F25	X7T												
2R24	2R6	X7S	C22L		2R24	IDD/J								
	3F22	5F11												
2E18	2F17													
	2R29													
2F18	2R5													
2R13	2R28	X5T	A22U											
	3F26	4N11												
2R27	2R11	A22L												
	3F23	X5S												
3F20	3F33	4K14												
	2R16	4G18												
3F24	3F31	4H8	4G16											
	2R18	4K13												
2R17	3F30													
	3F35	4H9												
4G17	4H6													
4G27	4H4													
	4K15													
4H10	4K8													
	3G18	2S20												

WORK S. .T
WESTINGHOUSE FORM 8295 E

SCHEME 18

Sheet 39

3M11	4C11	2G17"	5C24											
	4D11	4E11	X3T	B22U										
2G18	4F11													
3F28	3M9													
3F29	3M8													

WORK S[illegible]T
WESTINGHOUSE FORM 8295 E

SCHEME 19
Sheet 40

	2C20	2D19							3M19	4C10	2G19 H	5C25			
		2S23								4D10	4E10	X3R	B21U		
	2D20	2S4							2G20	4F10					
XR8	2S10	2S22	C21U			2S10	IOD/BB								
		3G8	X7R												
XR8	2S24	2S6	X7P	C21L		2S24	IDD/H								
		3G5	5F12												
	2E20	2F19													
		2S29													
	2F20	2S5													
	2S13	2S28	X5R	A21U											
		3G9	4N10												
	2S27	2S11	A21L												
		3G6	X5P												
	3G7	3G13													
		2S16	4K10												
	3G11	3G12													
		3M13	2S18												
	2S17	3G16													
		3G14	3M14												
	3G15	3M16													
	3G19	3M17													
	3M15	2T20													
		3G34													

ODING FORM FO IRROUGHS B ALGOL
ORM 34235 A

Westinghouse Electric Corporation

☐ PUNCH ( ) ☐ PUI SYNTAX CK.
☐ ORIG. PROGRAM ☐ PROGRAM CORRECTIONS

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.	SH
						SCHEME 20	4

BEGIN LINES AT INDICATED COLUMNS, ONLY

REF.

```
2C21 • 2D22                          3M24 • 4G9  2G22H • 5C26
       2T23                                  4D9 • 4E9   X3N   B20U
2D21 • 2T4                           2G21 • 4F9
2T10 • 2T22  C20U        (2T10) IØD/cc
       3G25 • X7N
2T24 • 2T6   X7M  C20L   (2T24) • IØD/F
       3G22 • 5F13
2E21 • 2F22
       2T29
2F21 • 2T5
2T13 • 2T28  X5N  A20U
       3G26 • 4N9

2T27 • 2T11  A20L
       3G23 • X5M
3G20 • 3G33
       2T16 • 7H23
3G24 • 3G31  7H22
       2T18 • 3M22
2T17 • 3G30
       3G35 • 3M23
3G29 • 3M25
3G28 • 3M26
3M20 • 4H19
       3H18 • 2V20
```

ODING FORM FO IRROUGHS B ALGOL
ORM 34235 A

Westinghouse Electric Corporation

☐ PUNCH ☐ PU SYNTAX CK.
☐ ORIG. PROGRAM ☐ PROGRAM CORRECTIONS

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.	SH
						SCHEME 21	4

BEGIN LINES AT INDICATED COLUMNS, ONLY

REF.	
2C23	2D24
	2V23
2D23	2V4
2V10	2V22 C19U
	3H8 X7L
2V24	2V6 X7K C19L
	3H5 5F15
2E23	2F24
	2V29
2F23	2V5
2V13	3H9 X5L A19W
	4N8 2V28
2V27	2V11 A19L
	3H6 X5K
3H7	3H13 7H26
	2V16 4H21
3H11	3H12 4H20 7H25
	2V18 3M33
3H15	3M30
3H19	3M32
2V17	3H16
	3H14 3M35
3M29	3H34
	3V20
	3M28 4C8 2G24 5C27
	4D8 4E8 X3L B19U
	2G23 4F8
	(2V10) I0D/DD
	(2V24) 'I0D/E

ODING FORM FO URROUGHS B ALGOL
ORM 34235A

Westinghouse Electric Corporation

PUNCH PU SYNTAX CK.
ORIG. PROGRAM PROGRAM CORRECTIONS

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.	SH
						SCHEME 22.	2

BEGIN LINES AT INDICATED COLUMNS, ONLY

```
REF.  1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73
2C25  2D26                                  4H17 • 7H11
      3V23                                  7H24 • 7H5
2D25  3V4                                                 4K11
3V10  3V22  C18U          (3V10) IØD/EE     3N7 • 4C4  2G26 • 5C35
      3H25 • X7J                                          4D4 • 4E4  X3J  B18U
3V24  3V6   X7H  C18L     (3V24) IØD/D      2G25 • 4F4
      3H22 • 5F23
2E25  2F26
      3V25
3V13  3V28  X5H  A18L
      3H26 • 4N4
3V27  3V11  A18U
      3H23 • X5J
3H20  3H33  7H35
      3V16 • 4H18
3H24  3H31  7H14 • 7H32
      3V18 • 4H16
3V17  3H30
      3H35 • 7H15
3H29  3N4
3H28  3N5
1H13  4K6
      3T20 • 3J18
2F25  3V5
```

ODING FORM FO IRROUGHS B ALGOL
ORM 34235 A

Westinghouse Electric Corporation

☐ PUNCH ( ) ☐ PU SYNTAX CK.
☐ ORIG. PROGRAM ☐ PROGRAM CORRECTIONS

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.	SH
						SCHEME 23	2

BEGIN LINES AT INDICATED COLUMNS, ONLY

REF.	
2C27	2D28
	3T23
2D27	3T4
2F27	3T5
3T24	3T6 X7E C17L (3T24) I∅D/C
	3J5 • 5F16
2E27	2F28
	3T29
3T13	3T28 X5F A17U
	3J9 • 4N7
3T27	3J11 A17L
	3J6 • X5E
3J7	3J13
	3T16 • 4H31
3J11	3J12 4H30
	3T18 • 3N9
3T17	3J16
	3J14 • 3N10
3J15	3N12
3J19	3N13
3N15	4C7 2G28H • 5C15
	4D7 • 4E7 X3F B17U
4G27	4F7

3N11 • 3J34
3S20

3T10 • 3T22 C17U (3T10) I∅D/FF
3J8 • X7F

ODING FORM FO[illegible]URROUGHS B[illegible] ALGOL
ORM 34235 A

Westinghouse [illegible]ectric Corporation

☐ PUNCH [illegible] ☐ PU[illegible] SYNTAX CK.
☐ ORIG. PROGRAM ☐ PROGRAM CORRECTIONS

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.	SH
						SCHEME 24	4

BEGIN LINES AT INDICATED COLUMNS, ONLY

REF.	
2C31	2D35
	3S23
2D31	3S4
3S10	3S22 X7D C16U (3S10) IOD/HH
	3J25 • 1R13
3S24	3S6 X7C C16L (3S24) IOD/B
	3J22 • 5F17
4J24	3S12
2E31	2F35
	3S29
2F31	3S25
3S13	3S28 X5D A16U
	3J26 • 4N6
3S27	3S11 A16L
	3J23 • X5C
5J20	3J33
	3S16 • 4H29
5J24	3J31 4H28
	3S18 • 3N17
5S17	3J30
	3J35 • 3N18
5J29	3N21
5J28	3N22
4N19	3K18
	3R20
	3N20 • 4C6 2G35 • 5C16
	4D6 • 4E6 X3D B16U
	2G31 • 4F6
	6F17 • 6F5
	6F33
	6F27 • 3S25
	6F13 • 3R25

CODING FORM FO[R] [BURROUGHS B] ALGOL
FORM 34235A

Westinghouse Electric Corporation

☐ PUNCH 8 ☐ PUN SYNTAX CH
☐ ORIG. PROGRAM ☐ PROGRAM CORRECTIO

TITLE	ANALYST	PHONE	DATE	PROGRAM NO.	DECK NO.	C.S. NO.
						SCHEME 25

BEGIN LINES AT INDICATED COLUMNS, ONLY

REF.	
2C30	2D33
	3R23
2D30	3R4
3R10	3R22 C15U (3R10) 5E22 1R17
	3K8 X7B
3R24	3R6 5E16 X7A (3R24) 1ØD/A
	3K5 5F18 C15L
3P29	3R12
2E30	2F33
	3R29
2F30	3R5
3R13	3R28 X5B A15U (3R13) 5E23
	3K9 4N5
3R27	3R11 X5A A15L
	3K6 5E18
3K7	3K13
	3R16 4K5
3K11	3K12 4K4
	3R18 4J7
3R17	3K16
	3K14 4J8
4J10	4J28 2H20
	4K16 3C18
3K15	3N25
3K19	3N26
4H27	4J4
	4K7
3N24	4C5 4E34 5E19 X3B B15U
	4D5 4E5 2G33 5C17
IDD/JJ	2G30 4E5
	5E25

WORK S_ _T
WESTINGHOUSE FORM 8295 E

SCHEME 26

SHEET 47

	0J19 • 0J18														
	0J9 • 0H6 • 0M29														
	0J17 • 0J33														
	0J20														
	0J28 • 0H24 • 0K24														
	0J11 • 0H7 • 0M33														
	0H22 • 0J5														
	0J14 • 0H12 • 0M31														
PSC	0G34 • 0G35 • 0H34 • 0H35 • 0J34 • 0J35														
	0G28 • 0G21	1M14 • 1M18													
	1M5 • 1M10														
	0G26 • 0G18	1N14 • 1N18													
	1N5 • 1N10														
	0G19 • 0H21														
	0H15 • 0H18														
	0G17 • 0G15	0G6													
	0G7 • 0G12														
	0J8 • 0J12	I0C/R													
	0J7 • 0J15														
CRSTROBE	0M28 • I0C/D														
	0M9 • 0K31														
DECK	0G22 • 0C18														
	0F9 • 0G13														
	0E28 • 0G10 • 0F18														

WORK S. _ _ r
WESTINGHOUSE FORM 8295 E

SCHEME 26

SHEET 48

OE9	•OG5	•OE19														
OD28	•OG4	•OE18														
OD9	•OH20	•OD19							SEE	SH 2,3	1A, 12	11 13	24 8	10 9	16 4	
OC28	•OH16	•OD18									29 31	33 34	35 36	37 38	40 41	
OC9	•OH13	•OC19									42 43	44 45	46			
OH14	•OK16															
OH17	•OK12															
OH19	•OK8															
OG8	•1P18															
OG9	•1P14															
OG11	•1P10															
OG14	•1P5															
OH26	•1V21	▲OK29														
OH28	•4V12	IΦC/E		(OH28)	•7P26											
	5K16	•5P24														
OH11	•IΦC/A															
OH9	•IΦC/B															
OH8	•IΦC/C															
INP OJ26	•IΦC/N		(OJ26)	•OM6												
(52)	•OJ22	•OG27														
		•OG33														
SCHEME 27 ↓																
55 IΦC/AA	•1055															
51 IΦC/BB	•1151B															

WORK S_ _T
WESTINGHOUSE FORM 8295 E

CAGE O SCHEME 27 & 28

SHEET 49

ECH0	OV32	IDC/F							(-)12V	OT4	OT10	OT5	OT11	OT27		
ECH1	OT32	IDC/H								OT6	OT8	OT7	OT9			
ECH2	OS32	IDC/J														
ECH3	OR32	IDC/K														
ECH4	OP32	IDC/L														
ECH5	ON32	IDC/M														
PSC	OV30	OT30	OS30	OR30	OP30	ON30										
SZR14	OV19	OT19	OP19	ON19												
		OS19	OR19	3R14												
13	OV12	OT12	OP12	ON12												
		OS12	OR12	3S14												
12	OV18	OT18	OP18	ON18												
		OS18	OR18	3T14												
11	OV17	OT17	OP17	ON17												
		OS17	OR17	3V14												
10	OV16	OT16	OP16	ON16												
		OS16	OR16	2V14												
9	OV15	OT15	OP15	ON15												
		OS15	OR15	2T14												
8	OV14	OT14	OP14	ON14												
		OS14	OR14	2S14												
7	OV13	OT13	OP13	ON13												
		OS13	OR13	2R14												
6	OV26	OT26	OP26	ON26												
		OS26	OR26	2P14												
5	OV25	OT25	OP25	ON25												
		OS25	OR25	2N14												

WORK S _ r
WESTINGHOUSE FORM 8295 E

CAGEO SCHEME 27 & 28

SHEET 50

4	OV20	OTZ0	OPZ0	ONZ0						1SECINT	OV34	OS11	OS11 ALREADY GOES TO IDT/S				
		OSZ0	ORZ0	2M14													
3	OV21	OTZ1	OPZ1	ONZ1													
		OSZ1	ORZ1	2L14													
2	OV22	OTZ2	OPZ2	ONZ2													
		OSZ2	ORZ2	2J14													
1	OV23	OTZ3	OPZ3	ONZ3													
		OSZ3	ORZ3	2J14													
0	OV24	OTZ4	OPZ4	ONZ4													
		OSZ4	ORZ4	2H14													
IN	11S17	10S7															
		10C20															
$\overline{RDO0}$	RDR/A	ON34															
		ON5															
$\overline{RDO1}$	RDR/B	ON33															
		ON6															
$\overline{RDO2}$	RDR/C	ON31															
		ON7															
$\overline{RDO3}$	RDR/D	ON35															
		ON4															
$\overline{RDO4}$	RDR/E	ON29															
		ON8															
$\overline{RDO5}$	RDR/F	ON28															
		ON9															
$\overline{RDO6}$	RDR/H	ON27															
		ON10															
$\overline{RDO7}$	RDR/J	ON11															

WORK S. .ET
WESTINGHOUSE FORM 8295 E

CAGES 10 & 11 SCHEME 27 & 28

SHEET 51

	10T8	10C5													
ECH0	10C15	10C/F													
	10T22	10C6													
ECH1	10C13	10C/H													
	11K11	10C4													
ECH2	10C14	10C/J													
	11K9	10C17													
ECH3	10C16	10C/K													
TN	10C23		10T6	10T12	11S25	13V5								Add 11S25	←
		10T7	10T25	11K12	11K7										
	10T11	10C28													
ECH4	10C25	10C/L													
	10T9	10C30					10T9	11S13							
ECH5	10C24	10C/M													
PSC	10F9	10F30	10G9	10G30	10H9	10H30									
	10D8	10E6													
		10F22													
	10D7	10E5													
		10F25													
	10D10	10E9													
		10F35													
	10D12	10E11													
		10F33													
	10D14	10E13													
		10F34													
	10D16	10E15													
		10G22													

WORK SHEET
WESTINGHOUSE FORM 8295 E

CAGES 10 & 11 SCHEME 28

SHEET 52

10D18	10E17													
	10G25													
10D20	10E19													
	10G35													
10D21	10E22													
	10G33													
10D23	10E24													
	10G34													
10D25	10E26													
	10H22													
10D27	10E28													
	10H25													
10D31	10E35													
	10H35													
10D30	10E33													
	10H33													
10D29	10E34													
	10H34													
10K8	10J31													
10J15	10J19	10E4	10E32											
	10D4	10D32												
10E8	10F7													
10E7	10F11													
10E10	10F8													
10E12	10F16													
10E14	10F19													
10E16	10G7													

WORK SHEET
WESTINGHOUSE FORM 8295 E

CAGES 10 & 11 SCHEME 28

SHEET 53

10E18	10G11
10E20	10G8
10E21	10G16
10E23	10G19
10E25	10H7
10E27	10H11
10E31	10H8
10E30	10H16
10E29	10H19
10F20	10F5
10F23	10F6
10F26	10F4
10F27	10F14
10F29	10F17
10G20	10G5
10G23	10G6
10G26	10G4
10G27	10G14
10G29	10G17
10H20	10H5
10H23	10H6
10H26	10H4
10H27	10H14
10H29	10H17

WORK S[illegible]ET
WESTINGHOUSE FORM 8295 E

CAGES 10 & 11 SCHEME 28

SHEET 54

CR14	10F10	10F21
		11D34
CR13	10F12	10F24
		11D33
CR12	10F13	10F31
		11D35
CR11	10F15	10F28
		11D25
CR10	10F18	10F32
		11D22
CR9	10G10	10G21
		11D17
CR8	10G12	10G24
		11D14
CR7	10G13	10G31
		11D4
CR6	10G15	10G28
		11D6
CR5	10G18	10G32
		11D5
CR4	10H10	10H21
		11C34
CR3	10H12	10H24
		11C33
CR2	10H13	10H31
		11C35

WORK S ET
WESTINGHOUSE FORM 8295 E

CAGES 10 & 11 SCHEME 28

SHEET 55

$\overline{CR1}$	10H15	•10H28													
		11C25													
$\overline{CR0}$	10H18	•10H32													
		11C22													
TR→CR	10C/E	•10K6													

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 30
SHEET 56

$\overline{\phi A0}$	10L21	10L16	TKL/K*												
$\overline{\phi A1}$	10L20	10L17	TKL/M*												
$\overline{\phi A2}$	10L14	10L18	PUN/S												
$\overline{\phi A3}$	10L15	10L19	11H7	11H15											
		11J4	11J32	11H25											
$\overline{\text{ADD STROBE}}$	10J21	10J16	TKL/N*												
$\overline{\text{IN STROBE}}$	10J20	10J17	TKL/L*												
	10M28	10M18													
	10M26	10M15													
	10M22	10M12													
	10M19	10M7													
		10T33													
	10K19	10M6													
	10K11	10K15	10528	11T9											
	10M17	10L5													
	10M14	10L4													
	10M11	10L29													
	10M9	10L31													
	10M8	10J5													
$\overline{\text{IN}}$	10K14	10J4	11S25												
	10K23	10S11													
		10C27													
	10K26	10K18													
$\overline{\phi A}$	10C26		10M24	10M30											
		10K20	10M20	10M31	13V12									13V12 NOT INSTALLED YET	
XR→TL	10K17	11C9													
PSC	10K34	10K35	10M34	10M35	10T34	10T35	11E4	11K34	11K35	11L34	11L35	11F34	11F35		

WORK S. .ET
WESTINGHOUSE FORM 8295 E

SCHEME 30

SHEET 57

	10K22	10K7														
	10K9	10J29														
LERT	10J14	10J18	TKL/J*													
	10T28	10T32														
		10V5														
	10T26	10T31	10T18	11S20												
		10T15	10T21													
	10V30	10V16														
	10V7	10T30														
									11S8	11S15						
CLR DR1	10T19	11N13	11N24	11N30						11T4	11T6					
		11N16	11N20						11S14	11S4						
CLR DR2	10T17	11N31	11M5	11M13						10V29						
		11M6	11M10						10V28	11S6						
CLR DR3	10T14	11M31	11M20	11M16					10V12	10V22						
		11M30	11M24						11S34	11S35	PSC					
	11E16	11F20						RDRADV	11T7	10T5						
	11E12	11F23														
	11E7	11F29														
	11E14	11E15														
		11F33														
	11E10	11E11														
		11F32														
	11E8	11E5														
		11F31														
PSC	11F34	11F35														
CLR HR	11S19	11H32														
		11H4	11H12													

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 30

SHEET 58

	11F30	11E33													
	11F28	11E35													
	11F27	11E28													
	11F26	11E26													
	11F25	11E24													
	11F24	11E22													
	11F22	11E19													
	11F21	11E17													
CHAN 0	11E18	10M33													
		10T4													
CHAN 1	11E20	10M32													
		10T24													
CHAN 2	11E21	10M25													
		11K10													
CHAN 3	11E23	10M21													
		11K5													
CHAN 4	11E25	10K21													
		10T10	13V4												←
CHAN 5	11E27														
		10T5	13V11												←
CHAN 6	11E31														
KEPGON	11S22	10TT	7N25	3R15										←	
CHAN 7	11E30	11S24													
S2	10C/CC	10K31													
S4	10C/DD	10K29													

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 31
SHEET 59

	11J29 • 11K31							11H9 • 11H10							
	11J30 • 11K30							11H14 • 11H20							
	11J31 • 11K24							11H22 • 11H31							
	11J27 • 11K20														
	11J25 • 11K16														
	11J23 • 11K13														
	11J21 • 11L31														
	11J20 • 11L30														
	11J18 • 11L24														
	11J16 • 11L20														
	11J14 • 11L16														
	11J12 • 11L13														
	11J10 • 11L10														
	11J7 • 11L5														
	11J8 • 11L6														
DR14	11K28 • 11M33														
	11P6														
13	11K26 • 11M32														
	11P5														
12	11K22 • 11M25														
	11P9														
11	11K19 • 11M21														
	11P11														
10	11K17 • 11M18														
	11P15														
9	11K14 • 11M15														
	11P17														

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 31

SHEET 60

DR8	11L28	11M12
		11P19
7	11L26	11M7
		11P22
6	11L22	11M4
		11P24
5	11L19	11N33
		11P26
4	11L17	11N32
		11P28
3	11L14	11N25
		11P35
2	11L11	11N21
		11P33
1	11L9	11N18
		11P13
0	11L8	11N15
		11P32
DR14	11M28	11K33
		11R6
13	11M26	11K32
		11R5
12	11M22	11K25
		11R9
11	11M19	11K21
		11R11
10	11M17	11K18
		11R15

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 31

SHEET 61

DR9	11M14	11K15													
		11R17													
8	11M11	11L33													
		11R19													
7	11M9	11L32													
		11R22													
6	11M8	11L25													
		11R24													
5	11N28	11L21													
		11R26													
4	11N26	11L18													
		11R28													
3	11N22	11L15													
		11R35													
2	11N19	11L12													
		11R33													
1	11N17	11L7													
		11R13													
0	11N14	11L4													
		11R32													
PSC	11N34	11N35	11K34	11K35	11L34	11L35	11H34	11H35	11F4	11F5					
PU05	10R21	10R16			(10R21)	IDT/BB	X8J								
		PUN/F	TKL/F												
PU06	10R20	10R17		(10R20)	IDT/U										
		PUN/H													
PU07	10R14	10R18		(10R14)	IDT/V										
		PUN/J													

* 7
TL05

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 31

SHEET 62

WD 07	11F9	11G31													
		11G33													
06	11F10	11G25													
		11G27													
05	11F12	11G21	11T31	11T33											
		11G23	11G22	11T35											
04	11F13	11G16	11T26	11T25											
		11G18	11G17	11T27											
03	11F14	11G12	11T22	11T21											
		11G14	11G13	11T23											
02	11F15	11G8	11T17	11T16											
		11G10	11G9	11T18											
01	11F16	11G4	11T13	11T12											
		11G6	11G5	11T14											
HR02	11H26	11H33													
		11F19													
$\overline{HR02}$	11H28	11H30													
		11F6													
HR01	11H17	11H21													
		11F18													
$\overline{HR01}$	11H19	11H18													
		11F7													
HR00	11H3	11H12													
		11F11													
$\overline{HR00}$	11H11	11H6													
		11E9													

WORK S ET
WESTINGHOUSE FORM 8295 E

SCHEME 32

SHEET 63

$\overline{TL00}$ / $\overline{PU00}$	10P21	10P16			10P21	1DT/W	X8P									
		PUN/A	TKL/A													
$\overline{TL01}$ / $\overline{PU01}$	10P20	10P17			10P20	1DT/X	X8N									
		PUN/B	TKL/B													
$\overline{TL02}$ / $\overline{PU02}$	10P14	10P18			10P14	1DT/Y	X8M									
		PUN/C	TKL/C													
$\overline{TL03}$ / $\overline{PU03}$	10P15	10P19			10P15	1DT/Z	X8L									
		PUN/D	TKL/D													
$\overline{TL04}$ / $\overline{PU04}$	10R15	10R19			10R15	1DT/AA	X8K									
		PUN/E	TKL/E													
	11511	10P5														
		10S15														
	1159	10P4														
		10S19														
	11K8	10P29														
		10S20														
	11N11	10P31														
		10S24														
	11N9	10R31														
		10S29														
	11C10	11S12														
	11C20	11S10														
	11D10	10S12														
	11D20	10S13														
	11C12	11S7														
	11C23	11S5														
	11D12	10S16														

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 32
SHEET 64

11D23	10S17
11C13	11K6
11C26	11K4
11D13	10S21
11D26	10S22
11C15	11N12
11C27	11N10
11D15	10S25
11D27	10S26
11C18	11N7
11C29	11N5
11D18	10S31
11D29	10S33

WORK S ET
WESTINGHOUSE FORM 8295 E

IDCONTROL CONN

SHEET 65

CR1→TL	IDC/A	11C30
CR2→TL	IDC/B	11D9
CR3→TL	IDC/C	11D30
CRSTROBE	IDC/D	10K25
$\overline{INP}$	IDC/N	11S16
		10S30
$\overline{OUT}$	IDC/P	10K32
		10S8
S1	IDC/R	10K27
S4	IDC/S	10K24
S5	IDC/T	
$\overline{E}$	IDC/V	10K12
		10S4
$\overline{HE}$	IDC/W	10K33
		10K30
S0	IDC/X	10K23
$\overline{S2}$	IDC/Y	10K10

WORK S ET
WESTINGHOUSE FORM 8295 E

I∅A DDRESS CONN

SHEET 66

TR14	A	10D6
13	B	10D5
12	C	10D9
11	D	10D11
10	E	10D13
9	F	10D15
8	H	10D17
7	J	10D19
6	K	10D22
5	L	10D24
		11E13
4	M	10D26
		11E9
3	N	10D28
		11E6
2	P	10D35
1	R	10D33

WORK S. ET
WESTINGHOUSE FORM 8295 E

ID ADDRESS CONN
SHEET 67

O	S 10D34													
E	T 11H24													
T	U 11H13													
D	V 11H5													

WORK S. ET
WESTINGHOUSE FORM 8295 E

I∅DATA CONN

SHEET 68

XR14	A	11J34													
		13G13													
13	B	11J33													
		13G17													
12	C	11J35													
		13G22													
11	D	11J28													
		13G26													
10	E	11J26													
		13G35													
9	F	11J24													
		13FZ6													
8	H	11J22													
		13F35													
7	J	11J19													
		13F34													
6	K	11J17													
		13G6													
5	L	11J15													
		11T11	13G9												
4	M	11J13													
		13F6													
3	N	11J11													
		13F9													
2	P	11J9													
		13F13													
1	R	11J5													

WORK S. ET
WESTINGHOUSE FORM 8295 E

I∅DATA CONN
SHEET 69

XR0	S	11J6						$\overline{XR13}$	HH	13G19						
		13F22														
$\overline{4}$	T	11C17						$\overline{XR14}$	JJ	13G15						
		13F5														
$\overline{3}$	U	11C14														
		13F11														
$\overline{2}$	V	11C4														
		13F15														
$\overline{1}$	W	11C6														
		13F19														
$\overline{0}$	X	11C5														
		13F24														
$\overline{7}$	Y	10R29														
		13G34														
$\overline{6}$	Z	10R4														
		13G5														
$\overline{5}$	AA	10R5														
		13G11														
$\overline{8}$	BB	13F33														
$\overline{9}$	CC	13F28														
$\overline{10}$	DD	13G33														
$\overline{11}$	EE	13G28														
$\overline{12}$	FF	13G24														

WORK SHEET
WESTINGHOUSE FORM 8295 E

CAGE 12 (CCP)
SHEET 70

WD01L	11G7	12J16					WD01H	11T15	12K34						
		12J34							12K16						
WD02L	11G11	12L16					WD02H	11T19	12M34						
		12L34							12M16						
WD03L	11G15	12N16					WD03H	11T20	12P34						
		12N34							12P16						
WD04L	11G19	12R16					WD04H	11T24	12S34						
		12R34							12S16						
WD05L	11G20	12J16					WD05H	11T29	12V34						
		12T34							12V16						
WD06L	11G24														
WD07L	11G29														
SR00	11R29	12J15	12R15	12T15											
		12L15	12N15												
01	11R14	12J13	12R13	12T13											
		12L13	12N13												
02	11R30	12J11	12R11	12T11											
		12L11	12N11												
03	11R31	12J9	12R9	12T9											
		12L9	12N9												
04	11R27	12J33	12R33	12T33											
		12L33	12N33												
05	11R25	12J31	12R31	12T31											
		12L31	12N31												

WORK S ET
WESTINGHOUSE FORM 8295 E

CAGE12 (CCØ)

SHEET 71

SR06	11R23	12J29	12R29	12T29													
		12L29	12N29														
07	11R21	12K15	12S15	12V15													
		12M15	12P15														
08	11R20	12K13	12S13	12V13													
		12M13	12P13														
09	11R18	12K11	12S11	12V11													
		12M11	12P11														
10	11R16	12K9	12S9	12V9													
		12M9	12P9														
11	11R12	12K33	12S33	12V33													
		12M33	12P33														
12	11R10	12K31	12S31	12V31													
		12M31	12P31														
13	11R7	12K29	12S29	12V29													
		12M29	12P29														
14	11R8	12K27	12S27	12V27													
		12M27	12P27														
RR00	11P29	12J2	12R2	12T2													
		12L2	12N2														
01	11P14	12J3	12R3	12T3													
		12L3	12N3														
02	11P30	12J17	12R17	12T17													
		12L17	12N17														
03	11P31	12J18	12R18	12T18													
		12L18	12N18														

WORK SHEET
WESTINGHOUSE FORM 8295 E

CAGE 12 (CCP)

SHEET 72

RR04	11P27	12J35	12R35	12T35													
		12L35	12N35														
05	11P25	12J19	12R19	12T19													
		12L19	12N19														
06	11P23	12J20	12R20	12T20													
		12L20	12N20														
07	11P21	12K2	12S2	12V2													
		12M2	12P2														
08	11P20	12K3	12S3	12V3													
		12M3	12P3														
09	11P18	12K17	12S17	12V17													
		12M17	12P17														
10	11P16	12K18	12S18	12V18													
		12M18	12P18														
11	11P12	12K35	12S35	12V35													
		12M35	12P35														
12	11P10	12K19	12S19	12V19													
		12M19	12P19														
13	11P7	12K20	12S20	12V20													
		12M20	12P20														
14	11P8	12K21	12S21	12V21													
		12M21	12P21														

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 33 & 34

Sheet 73

11V22	11V22	11V32													
		11V30					(KEEPGON)	7N25	7H8						
PWRON	TB3/4	TB4/9													
		12K14													
ATOLINT	11V26	TB4/8	TK2/H	TK3/H											
		IØT/cc	TK1/H												
	TB3/1	12K4													
-24V	TB2/13	TB4/1													
		11V1													
+24	TB2/1	11V2													
M1	12F26	12J14													
$\overline{M1}$	12F27	12J4													
		IØT/J													
M2	12F28	12J12													
$\overline{M2}$	12F29	12J5													
		IØT/K													
M4	12F30	12J10													
$\overline{M4}$	12F31	12J6													
		IØT/L													
M8	12F32	12J8													
$\overline{M8}$	12F33	12J7													
	(12E34)	-IØT/M													

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 33 & 34

SHEET 74

M10	12E26	12J32
$\overline{M10}$	12E27	12J22
		IDT/N
M20	12E28	12J30
$\overline{M20}$	12E29	12J23
		IDT/P
M40	12E30	12J28
$\overline{M40}$	12E31	12J24
		IDT/R
COMPUTER AUTO TURN ON	12J26	11V25
$\overline{S1}$	12H27	IDT/A
$\overline{S2}$	12H29	IDT/B
$\overline{S4}$	12H31	IDT/C
$\overline{S8}$	12H33	IDT/D
$\overline{S10}$	12G27	IDT/E
$\overline{S20}$	12G29	IDT/F
$\overline{S40}$	12G31	IDT/H

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 39

SHEET 7.5

	13N9	13P5													
		13P22									SEE	SHEET	68 &	69	
	13N12	13P6									FOR	XR & $\overline{XR}$	connections		
		13P24													
	13N18	13P4									SEE	SHEET	78 &	79	
		13P32									for	$\overline{MR}$	CONNECTIONS		
	13N24	13P14													
		13P33									SEE	Sheet	40-46	for MF	conn
	13N28	13P17									to	$\overline{XR}$(n)			
		13P31	13M6												
HA	13P10	13P11	13R5								SEE	Sheet	51,	56,	58
		13P25	13N10												
HB	13P12	13P8	13R14												
		13P34	13N16												
HC	13P13	13P16	13R20												
		13P28	13N22												
HD	13P15	13P19	13R26												
		13P35	13N32												
HE	13P18	13P21	13T4												
		13P7	13N4												
$\overline{HA}$	13P20	13N31													
$\overline{HB}$	13P23	13N5													
		13T31													
$\overline{HC}$	13P29	13N14													

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 39

SHEET 76

HD	13P27	13N20													
HE	13P26	13N26													
		13T11													
	13R8	13N15													
		13S5													
	13R9	13S22													
	13R13	13S6													
	13R12	13S25													
	13R19	13S4													
	13R18	13S34													
	13R25	13S14													
	13R24	13S33													
WRITE	13M23	13M31	13V16	13V18											
		13M34	13S30	13X32											
WRITE	13V19	13X31													
		MAG/X													
READ	13M28	13M25	13X30												
		13M27	13S9												

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 39
SHEET 77

(IN) 13V10	13R30															
	13M29	13M33														
(OUT) 13V14	13R32															
	13M22	13M24														
(HE) 13M8	13R4	13R22														
	13R10	13R16														
INIT 13M11	13M30	13S9	MAG/BB													
	13M32	13N34														
CLOCK 13T19	13P9															
	13X35															
SEEK	13V4															
	MAG/C															
GAP MAG/Z	13S19															
$\overline{\text{GAP}}$ MAG/Y	13M12															
	13M14															
HOLD 13R29	13T28	IOC/EE														
	13M4	13M10														
CLR SW MAG/AA	13T35															
$\overline{\text{FWD}}$	13T29															
$\overline{\text{CLOCK}}$ MAG/CC	13T16						$\overline{\text{CLOCK R}}$	MAG/DD	13T3							
	13T18															

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 39
SHEET 78

ØOR 13S10	13L35	13L20	13L24												
	13L6	13L12	13L34												
ØOW 13S20	13L33	13L17	13L15												
	13L27	13L25	13L5												
ØIR 13S12	13K35	13K20	13K24												
	13K6	13K12	13K34												
ØIW 13S23	13K33	13K17	13K15												
	13K27	13K25	13K5												
Ø2R 13S13	13J35	13J20	13J24												
	13J6	13J12	13J34												
Ø2W 13S29	13J33	13J17	13J15												
	13J27	13J25	13J5												
Ø3R 13S15	13H35	13H20	13H24												
	13H6	13H12	13H34												
Ø3W 13S17	13H33	13H17	13H15												
	13H27	13H25	13H5												
X→M1 13T21	13F4														
	13F32	13X34													
X-M2 13T26	13G4														
	13G32	13X33													
MC IDC/FF	13T33														

WORK S. ET
WESTINGHOUSE FORM 8295 E

SCHEME 40

SHEET 79

IDA MAG/KK	13C6					IDAR	MAG/LL	13C3							
						IDBR	MAG/JJ	13E3							
IDB MAG/HH	13D6					IDCR	MAG/FF	13F3							
IDC MAG/EE	13E6														
ODA MAG/SS	13V21					ODAR	MAG/TT	13VGND							
						ODBR	MAG/RR	13TGND							
ODB MAG/PP	13V26					ODCR	MAG/NN	13SGND							
ODC MAG/MM	13V28														
PSC 13D3	13C34														
	13D34	13E34													
$\overline{MR00}$ 13C29	13V22														
	13V24	IOA/SS													
$\overline{MR01}$ 13C24	13L7														
	IOA/RR														
$\overline{MR02}$ 13C18	13K7														
	IOA/PP														
$\overline{MR03}$ 13C12	13J7														
	IOA/NN														
$\overline{MR04}$ 13C9	13H7														
	IOA/MM														
$\overline{MR05}$ 13D29	13V30														
	13V32	IOA/LL													

WORK S ET
WESTINGHOUSE FORM 8295 E

SCHEME 40
SHEET 80

$\overline{MR06}$ 13D24	13L16														
	IDA/KK														
$\overline{MR07}$ 13D18	13K16														
	IDA/JJ														
$\overline{MR08}$ 13D12	13J16														
	IDA/HH														
$\overline{MR09}$ 13D9	13H16														
	IDA/FF														
$\overline{MR10}$ 13E29	13V33														
	13V35	IDA/EE													
$\overline{MR11}$ 13E24	13L30														
	IDA/DD														
$\overline{MR12}$ 13E18	13K30														
	IDA/CC														
$\overline{MR13}$ 13E12	13J30														
	IDA/BB														
$\overline{MR14}$ 13E9	13H30														
	IDA/AA														
13F8	13C4														
13F7	13C5														
13F10	13C10														
13F12	13C14														
13F14	13C16														
13F16	13C20														
13F18	13C22														
13F20	13C26														

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 40
SHEET 81

13F21	13C31													
13F23	13C30													
13F25	13D4													
13F27	13D5													
13F31	13D10													
13F30	13D14													
13F29	13D16													
13G29	13D20													
13G8	13D22													
13G7	13D26													
13G10	13D31													
13G12	13D30													
13G14	13E4													
13G16	13E5													
13G18	13E10													
13G20	13E14													
13G21	13E16													
13G23	13E20													
13G25	13E22													
13G27	13E26													
13G31	13E31													
13G30	13E30													
13H10	13C11													
	13H8													
13H14	13C15													
	13X15													

WORK SHEET
WESTINGHOUSE FORM 8295 E

Scheme 40
sheet 82

13J10	13C17													
	13J8													
13J14	13C21													
	13X19													
13K10	13C23													
	13K8													
13K14	13C27													
	13X23													
13L10	13C33													
	13X29													
13L14	13C32													
	13X28													
13H19	13D11													
	13H9													
13H21	13D15													
	13X14													
13J19	13D17													
	13J9													
13J21	13D21													
	13X18													
13K19	13D23													
	13K9													
13K21	13D27													
	13X22													
13L19	13D33													
	13X27													

WORK SHEET
WESTINGHOUSE FORM 8295 E

SCHEME 40
SHEET 83

13L21	13D32													
	13X26													
13H26	13E11													
	13X13													
13H28	13E15													
	13X16													
13J26	13E17													
	13X17													
13J28	13E21													
	13X16													
13K26	13E23													
	13X21													
13K28	13E27													
	13X20													
13L26	13E33													
	13X25													
13L28	13E32													
	13X24													

WORK S ET
WESTINGHOUSE FORM 8295 E