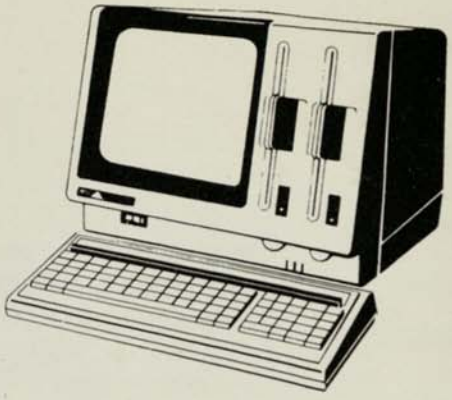
Advanced
Personal Computer



APC System Reference Guide

NEC
NEC Information Systems, Inc.
819-000100-1003
4-83

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FEDERAL COMMUNICATIONS COMMISSION RADIO FREQUENCY INTERFERENCE STATEMENT

"WARNING: This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A Computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide protection against such interference. Operation of the equipment in a residential area is likely to cause interference in which case, the user will be required to take whatever measures may be required to correct the interference."

Manufacturer's Instructions and User's Responsibility to Prevent Radio Frequency Interference

Manufacturer's Instructions

The user must observe the following precautions when installing and operating this device:

1. Operate the equipment in strict accordance with the manufacturer's instructions for the model.
2. Ensure that the unit is plugged into a properly grounded wall outlet and that the power cord supplied with the unit is used and not modified.
3. Ensure that the unit is always operated with the factory-installed cover set on the unit.
4. Make no modifications to the equipment which would affect its meeting the specified limits of the Rules.
5. Properly maintain the equipment in a satisfactory state of repair.

User's Responsibility

The user has the ultimate responsibility to correct problems arising from harmful radio-frequency emissions from equipment under his control. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures. All of these responsibilities and any others not mentioned are exclusively at the expense of the user.

1. Change in orientation of the receiving device antenna.
2. Change in orientation of the equipment.
3. Change in location of equipment.
4. Change in equipment power source.

If these attempts are unsuccessful, install one or all of the following devices:

1. Line isolation transformers
2. Line filters
3. Electro-magnetic shielding

If necessary, the user should consult the dealer, NEC, or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission to be helpful: "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

"Note: The operator of a computing device may be required to stop operating his device upon finding that the device is causing harmful interference and it is in the public interest to stop operation until the interference problem is corrected."

Contents

Contents (cont'd)

Contents (cont'd)

List of Illustrations

List of Illustrations (cont'd)

List of Tables

List of Tables (cont'd)

List of Tables (cont'd)

Preface

This system reference guide provides hardware design and interface information for programmers, engineers, designers, and others who need to know how the APC is designed.

Chapter 1, Hardware Overview, familiarizes you with the Advanced Personal Computer and defines the principal components and devices.

Chapter 2, Processor PCB, includes descriptions and technical information for the devices contained on the Processor PCB along with programming considerations where appropriate.

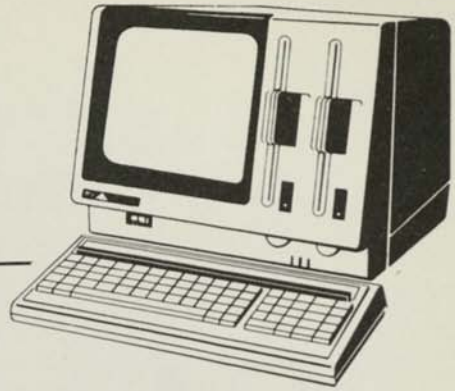
Chapter 3, Controller PCB, includes information similar to that in Chapter 2 for the devices contained on the Controller PCB.

Chapter 4, Power Supply, contains detailed specifications for the system power source.

Appendices A to F include hardware reference information such as IC data sheets, logic diagrams, and data summaries.

List of Abbreviations

A	Ampere
ALE	Address Latch Enable
APC	Advanced Personal Computer
APU	Arithmetic Processing Unit
AT	Abnormal Termination
BBM	Battery-Backed Memory
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CS	Code Segment
DCH	Device Control
DIP	Dual In-line Package
DMA	Direct Memory Access
DMC	Direct Memory Access Cycle
DS	Data Segment
EPROM	Erasable Programmable Read-Only Memory
ES	Extra Segment
FDC	Flexible Disk Drive Controller
FDD	Flexible Disk Drive
FIFO	First-In First-Out
FM	Frequency Modulation
GDC	Graphic Display Controller
HEX	Hexadecimal
Hz	Hertz
IC	Integrated Circuit, Interrupt Code, Invalid Command
ICW	Initialization Command Word
I/O	Input/Output
IP	Instruction Pointer
IRR	Read Interrupt Register
ISR	Read Inservice Register
KB	Kilobyte
LED	Light Emitting Diode
LSB	Least Significant Bit
LSI	Large-Scale Integration
MB	Megabyte
MFM	Modified Frequency Modulation
MHz	Megahertz
MOS	Metal Oxide Semiconductor
ms	Millisecond
MSB	Most Significant Bit
ns	Nanosecond
NT	Normal Termination
OCW	Operational Command Word
ODA	Output Device Adapter
PAL	Programmable Array Logic
PCB	Printed Circuit Board
POF	Power Off Control
RAM	Random Access Memory
ROM	Read-Only Memory
rpm	Revolutions Per Minute
SS	Stack Segment
SW	Switch
TTL	Transistor/Transistor Logic
USART	Universal Synchronous/ Asynchronous Receiver/ Transmitter
V	Volt
VFO	Variable Frequency Oscillator
W	Watt
μs	Microsecond



Chapter 1

Hardware Overview

The NEC Advanced Personal Computer (APC) has two basic components: a Main Unit and a Keyboard. The Keyboard, which cable-connects to the Main Unit, is common to all APC models. The Main Unit, which houses the Central Processing Unit (CPU), memory, visual display, sound output, and peripheral controllers, is available in three models: (1) a Monochrome Cathode Ray Tube (CRT) Display with one 8-inch Flexible Disk Drive (FDD), (2) a Monochrome CRT Display with two 8-inch FDDs, and (3) a Color CRT Display with two 8-inch FDDs. Several options and accessories are available to enhance performance or to adapt the APC for special applications.

Figure 1-1 is a block diagram of the APC. The Main Unit, the heart of the APC, has a CRT Display, one or two 8-inch FDDs, an ON/OFF switch, and several controls associated with the CRT Display. Three Input/Output (I/O) cable connectors are available at the rear of the cabinet.

The CPU, memory, and basic control logic are contained in the Main Unit on two quad-layered Printed Circuit Boards (PCB): a Processor PCB (G9PFBU) and a Controller PCB (G9PFCU). These PCBs plug into a mother board interface bus that has the space and power for up to three additional (optional) PCBs.

The Processor PCB contains as standard equipment:

- A 16-bit 8086 Microprocessor
- An 8288 Bus Controller with 20-bits of addressing, making one megabyte (MB) of memory accessible
- 128 kilobytes (KB) (standard) of Random Access Memory (RAM)
- 8 KB of Read-Only Memory (ROM)
- 4 KB of CMOS Battery-Backed Memory, which remains refreshed for at least two years without ac power
- A 4-channel Direct Memory Access (DMA) Controller

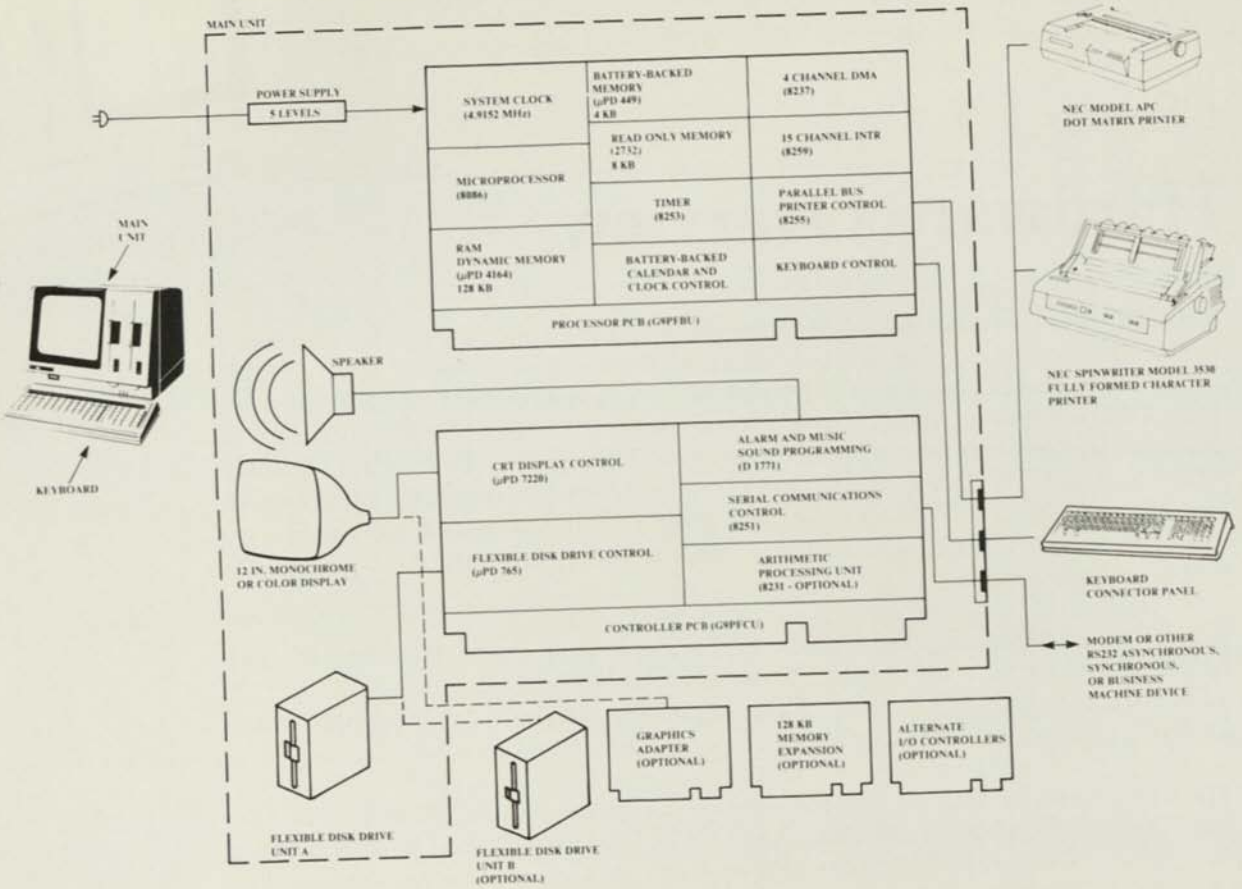


Figure 1-1 System Block Diagram

- A 15-channel Interrupt System
- Printer and Keyboard Controllers
- Calendar-and-Clock Controller, which keeps track of the month, date, day of week, hour, minute, and second, and runs on battery power when ac power is off, thus preserving the time/date setting.

The Controller PCB contains as standard equipment:

- CRT Display Control, which can generate 250 predefined characters and allows you to create and store on disk any number of sets of 256 other special characters

- Flexible Disk Drive Controller (FDC) to coordinate the reading of and the writing to one or two 8-inch flexible disks
- Alarm and Music Sound Programming System, which enables you to select alarm tones and generate music across two octaves, with selected tempos, volumes, and tone characteristics
- Serial Communications Adapter, which is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART), enabling the APC to communicate with almost any type of communications device.

The APC power supply is a 100-watt, 5-voltage-level switching regulator. It furnishes dc levels to all components — except to the CRT which has its own power unit — and has sufficient reserve capacity to handle future expansion. The power supply has a software-controlled Power-Off control (POF) circuit that enables you to turn off the system locally or remotely.

One or two 8-inch FDDs are integrated into the Main Unit. The FDC (NEC μPD765) can read from or write to dual-sided double-density disks (which store up to 1 MB of unformatted data) or single-sided single-density flexible disks (which can store about 260 KB of unformatted data). The disk drive is a compact, high-performance, energy-efficient design featuring direct drive by a dc motor. Head loading and positioning is microprocessor-controlled for greater accuracy and minimum wear and damage to the media surface. Variable Frequency Oscillation (VFO) is employed to improve data transfer.

The APC comes equipped with a 12-inch (diagonal) green-phosphor monochrome CRT or a 12-inch 8-color CRT. Either unit has a self-contained power supply. Both have a reduced glare surface and a high resolution screen. Standard alphanumeric characters are composed from an 8-by-19 dot matrix, allowing a display of 25 lines of 80 characters. Special symbols can be designed by the user with a dot matrix of up to 8-by-16.

The CRT Display has considerable versatility and provides you with capabilities for scrolling, partitioning (and scrolling within selected partitions), overbar, vertical bar, underscore, highlighting, blinking, and reverse video. The Color CRT Display has all these attributes plus a choice from eight colors.

With the special-character generator, you can design up to 256 characters dot-by-dot, which can be saved on disk as one or more special character sets. Using a dot matrix printer, these special characters can be printed and displayed, making the APC especially adaptable to users who use non-Roman alphabets or scientific symbols.

The APC also offers an optional Graphics Adapter based on the NEC μPD 7220. This self-contained single PCB plugs into the Main Unit and simplifies graphics applications, such as area shading, simulated movement, and solid or dashed lines, either straight or curved. By employing the Graphics Adapter with selected software packages, you can generate graphs, bar graphs, and three-dimensional pictures.

Also optional are two NEC printers. The Dot Matrix Printer provides rapid, high quality printing at a low cost. It prints in both directions at 100 characters per second on a 80-to-136-character column width. It prints special and graphic characters as well as standard alphanumeric characters.

The other printer is the NEC Model 3530 Spinwriter®, which produces high quality fully-formed characters. This printer features interchangeable print elements that contain up to 128 characters and are offered in several dozen type styles and symbol sets. It prints 35 characters per second at 10, 12, and 15 characters per inch or proportional spacing. It also prints bidirectionally and offers word processor functions, such as automatic underlining, shadowing, bold face printing, as well as several paper-handling accessories.

The standard APC comes equipped with 128 KB of RAM, which resides on the Processor PCB. With the optional memory-expansion kits, RAM can be expanded to 640 KB.

The asynchronous, synchronous serial I/O communications adapter is a standard feature of the APC. The interface is supported by the NEC 8251A Communications Controller, a USART, that is used as a peripheral and is programmed by the microprocessor to communicate using virtually any serial or parallel data-transmission technique, at programmable baud rates. For communications interface requirements beyond this standard controller, NEC offers special-purpose I/O Controllers on plug-in boards.

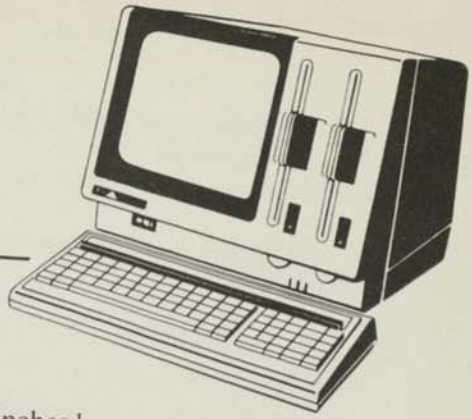
The Keyboard is not housed in the Main Unit; it attaches to the rear of the Main Unit with a single five-foot, coiled cable. The Keyboard has 109 keys, including a numeric keypad and 22 programmable function keys that facilitate data and word processing. Each function key has two shift-modes, making available 44 user-definable functions with one or two keystrokes.

NOTE

Only 32 of the 44 user-definable functions can be character strings.

PROCESSOR PCB

PROCESSOR PCB



Chapter 2

Processor PCB

The Processor PCB (G9PFBU) fits vertically in the Main Unit and is 11 inches long by 9½ inches high (see Figure 2-1). It is composed of four sandwiched layers, including the signal, ground, and dc-power internal planes. It plugs into the third slot of the card cage with a 100-contact edge connector on the bottom of the PCB.

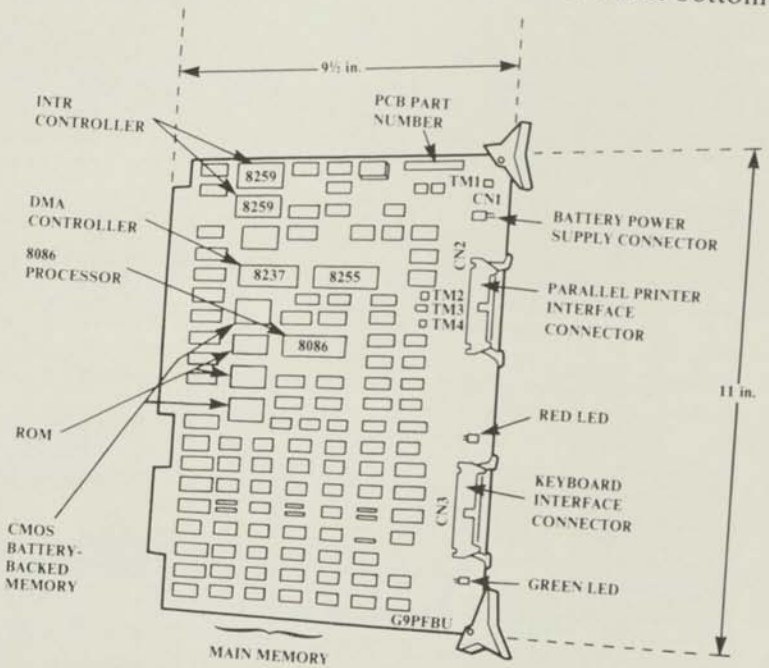


Figure 2-1 Processor PCB

As shown in Figure 2-1, three cable connectors are on the Processor PCB; two are 26-pin connectors and the third is a 2-pin header connector. The Keyboard interface uses one of the 26-pin connectors, while the other connector provides a parallel printer (or other such device) interface. Battery power is supplied by the 2-pin connector.

The principal functional components and their interrelationships are shown on the block diagram of the Processor PCB (see Figure 2-2). The major elements of the PCB consist of the following functional areas:

- An NEC μPD8086 microprocessor, which is
  1) Fully compatible with the Intel 8086 microprocessor
  2) Capable of addressing one MB of memory
  3) Driven by an NEC μPD8284 clock generator at 4.9152 MHz
- A 20-bit bidirectional address bus, 16 bits of which serve also as the data bus, and related buffers, controls, and ports
- A DMA controller to permit high speed data transmission between input/output devices without intervention of the microprocessor

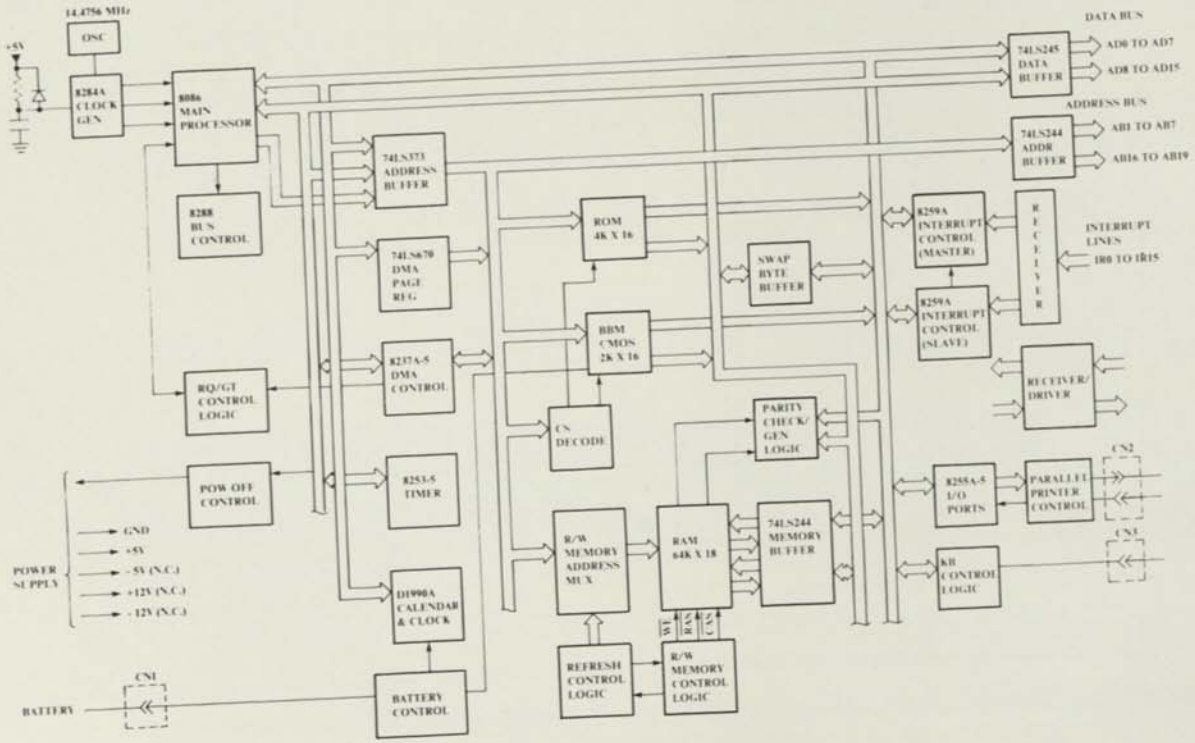


Figure 2-2 Processor PCB Block Diagram

- A 15-channel interrupt controller to govern access to the microprocessor and data bus
- 8 KB (4K x 16 bits) of ROM, which carry out self-testing and flexible-disk bootstrap loading.
- 128 KB of RAM organized into sixteen 64K x 1 dynamic-memory chips, plus two more for parity check
- 4 KB (2K x 16 bits) of CMOS Battery-Backed Memory (BBM)
- Keyboard control logic, which controls and conveys data from the Keyboard to the data bus
- Parallel printer control, which interfaces with a connector on the APC rear panel for connection of a printer or similar device
- Calendar and clock generator, supported by NEC μPD1990AC, which is battery-protected and generates day, month, day of the week, hour, minute, and second information.

2.1 MOTHER BOARD/CARD CAGE INTERFACE

The Mother Board contains five card-edge socket connectors, each having 100 contacts, 50 on a side (see Figure 2-3). All contacts are connected as a bus to each PCB socket.

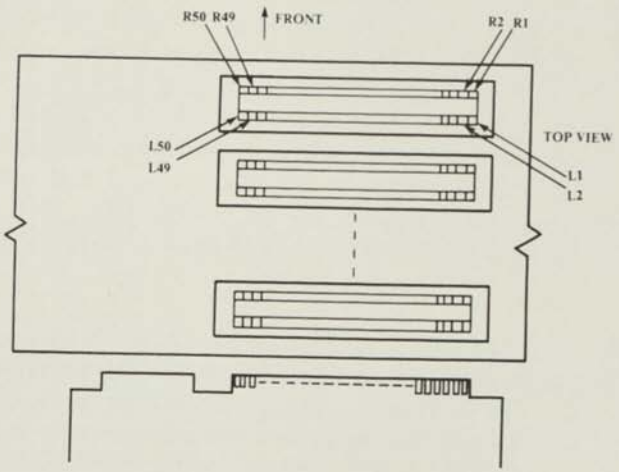


Figure 2-3 Mother Board/Card Cage Interface

Table 2-1 lists the contact assignments for each socket. All signals on these contacts are Transistor/Transistor Logic (TTL) compatible. Time relationships between various contacts in the card cage bus are shown in Figures 2-4 through 2-7. I/O equivalent circuits for the affected contacts and devices are shown in Figures 2-8 and 2-9.

Table 2-1 Card Cage Socket Contact Assignments

PIN NUMBER	NAME	READ/ WRITE	DESCRIPTION
R1, R50 L1, L50	GND		Signal Ground
R2, R49 L2, L49	+5 V		+5 Vdc Supply
R3, R48 L3, L48	+12 V		+12 V Supply
R47, L47	-12 V		-12 V Supply
R46, L46	-5 V		-5 V Supply
R4	POF	W	*Power Off Control.* Goes high to command power supply off.
R5, L5 R6, L7 R8 R9, L9 R10, L10 R12	IR0 to IR14	R	*Interrupt Request 0 Through 14.* These 15 lines carry interrupt requests to the processor. When an I/O device requires processor intervention, it signals the μPD8259A interrupt controller, which activates one of the 15 interrupt lines to the processor; the interrupt-request signal is maintained until acknowledgement from the processor. IR0 has the highest priority and IR15 the lowest priority. These lines are active Low.
R13, R14 R15, R16	DRQ0 to DRQ3	R	*DMA Request 0 Through 3.* These lines transmit requests by I/O devices for DMA service. These signals remain active until DMA acknowledgement is active on a corresponding DACK line. Channel assignments are 0 = CRT, 1 = FDD, 2 = Graphics, 3 = AUX.
L13, L14 L15, L16	DACK0 to DACK3	W	*DMA-Request Acknowledgement 0 Through 3.* These lines signify that the DMA controller has acknowledged the DMA request on a corresponding DRQ line. DACK lines are active High.

Table 2-1 Card Cage Socket Contact Assignments (cont'd)

PIN NUMBER	NAME	READ/ WRITE	DESCRIPTION
R20	TC	W	*Terminal Count.* This line carries to the I/O device a one-clock-duration pulse indicating that the terminal count for the DMA channel has been reached. This pulse is active High.
R21	PHI0	W	*System Clock.* The pulse of the clock is transmitted on this line; the clock period is about 200 nsec (4.9152 MHz) and its duty cycle is 33 percent.
L21	IRST	W	*Initial Reset.* When this line goes High, every device in the system is initialized. This line is activated at power on.
R22	IOW	W	*I/O Write.* A Low on this line instructs the I/O device to receive data from the data bus. Either the DMA controller or processor can activate the line.
L22	RDY	R	*Ready.* A High on this line indicates that data has been received by an I/O device or memory, or that preparation of data is complete. It is pulled Low by a device to lengthen I/O memory cycles, allowing slower devices to adjust to the I/O channel. NOTE There is an *Interval-Ready* signal within the G9PFBU PCB; it activates when memory access from the processor or DMA controller clashes with the memory-refresh cycle.

Table 2-1 Card Cage Socket Contact Assignments (cont'd)

PIN NUMBER	NAME	READ/ WRITE	DESCRIPTION
R23	IOR	W	*I/O Read.* A Low on this line instructs the I/O device to transmit its data to the data bus. This instruction can come from either the DMA controller or the processor.
L23	DMC	W	*DMA Cycle.* A High on this line indicates the processor has been inhibited, thus giving system-bus control to the DMA controller.
R24	MRQ	W	*Memory Request.* When this line is Low, it indicates the memory cycle is in operation. The line is inactive (High) during memory-refresh cycles.
L24	MR	W	*Memory Read.* This line instructs the additional memory to transmit its data onto the data bus. Either the processor or DMA controller can activate this signal, which is active Low.
R25	RFSH	W	*Memory Refresh.* When this line is Low, dynamic memory is refreshed.
L25	MW	W	*Memory Write.* When Low, this line instructs the selected memory to receive the data on the data bus. It is activated by either the DMA controller or processor.
R26	BHE	W	*Bus High Enable.* When Low, this line indicates that the most significant half of the data line is ready to be read. This line is not used during DMA cycles.
L26	ALE	W	*Address Latch Enable.* When activated by the processor or DMA control, the signal on this line latches the address on the bus.

Table 2-1 Card Cage Socket Contact Assignments (cont'd)

PIN NUMBER	NAME	READ/ WRITE	DESCRIPTION
R27	DT/R	W	*Data Transmit or Receive.* This line indicates data transfer direction. When High, direction is processor to I/O or memory; when Low, direction is I/O or memory to processor.
L27	CLK0	W	*Communication Clock.* This line, which is energized by the 8253-5 Programmable Interval Timer, conveys a synchronizing variable frequency clock to the communications control.
R30	A0	W	*Address Bit 0.* When this line is active (High), the memory or I/O device associated with the least significant half of the data is enabled to read or transmit its data.
R31, L30 R32, L31 R33, L32 L33	A1 to A7	W	*Address Bits 1 Through 7.* These seven lines address the memory or I/O device. These signals are latched.
R34, L34 R35, L35 R36, L36 R37, L37 R38, L38 R39, L39 R40, L40 R41, L41	AD0 to AD15	W	*Address and Data Lines 0 Through 15.* These 16 lines are bidirectional and time multiplexed to convey address or data to the address or data buses.
R42, L42 R43, L43	A16 to A19	W	*Address Lines 16 Through 19.* These four lines, used for addressing the memory, increase the number of address lines to twenty, allowing access to one megabyte of memory.

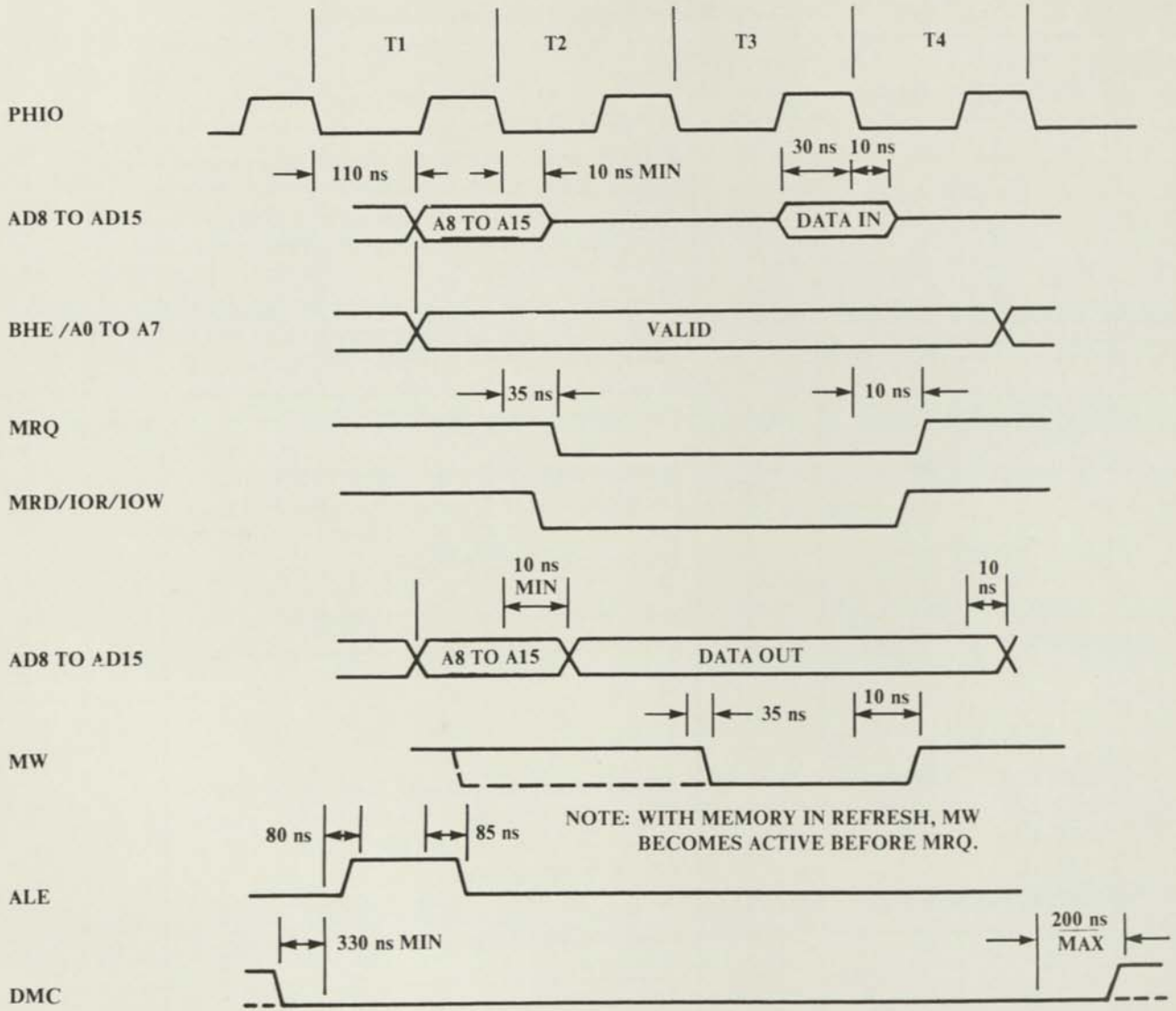


Figure 2-4 Processor Timing

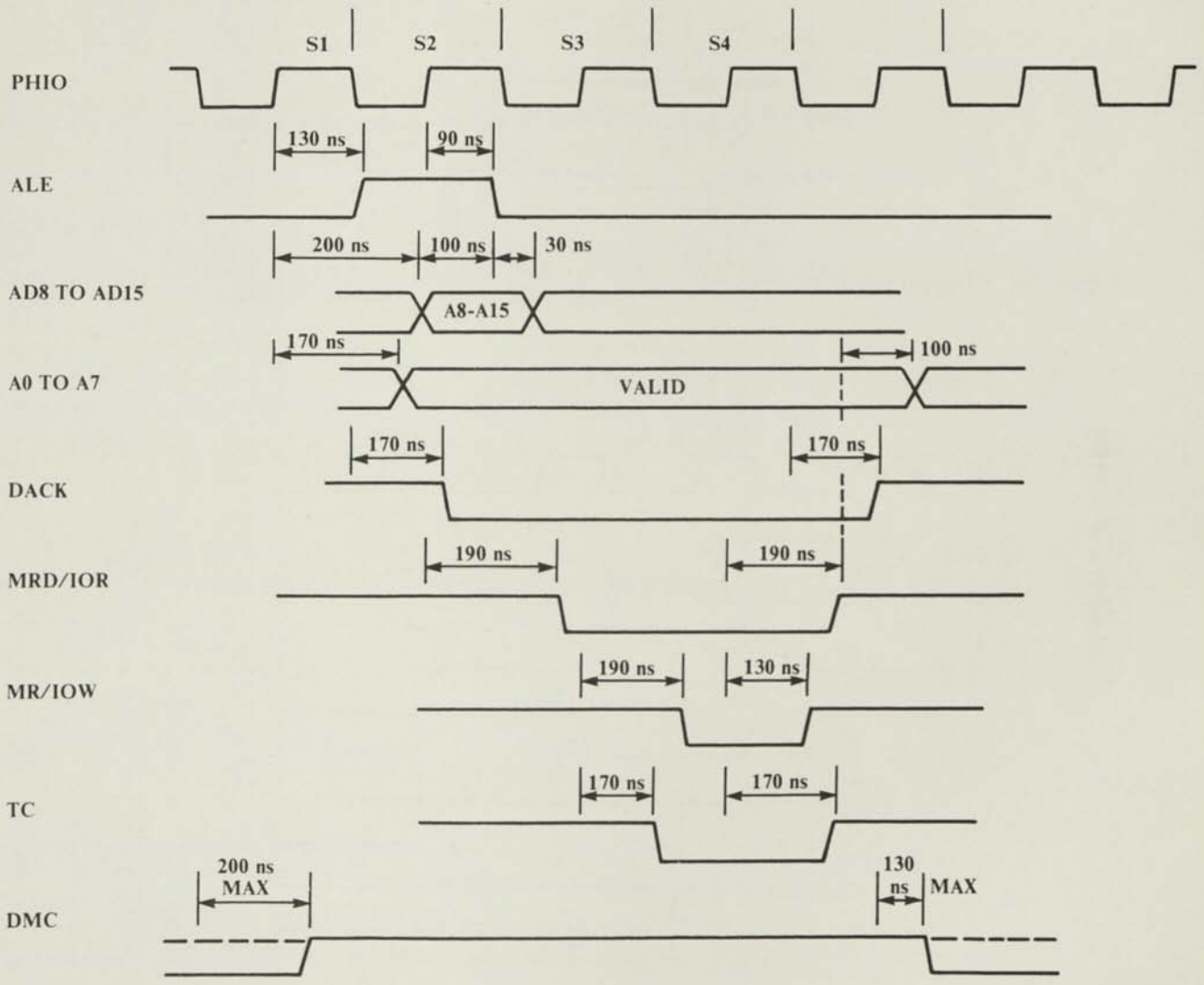


Figure 2-5 DMA Timing

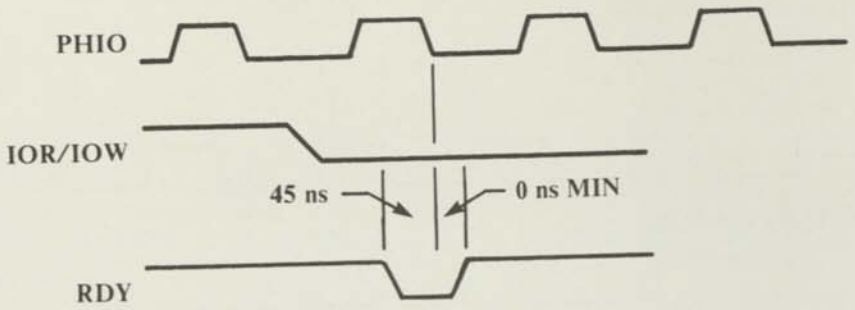
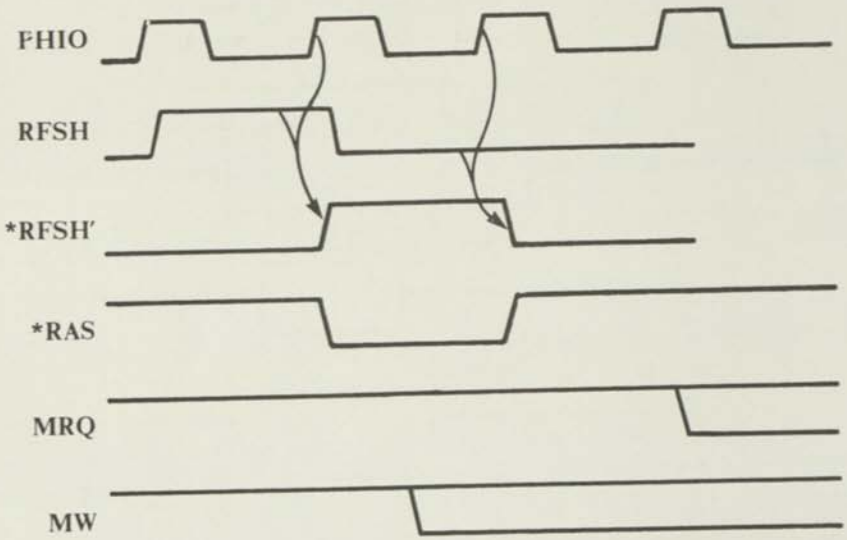


Figure 2-6 RDY Signal Timing



NOTE: THE *RFSH' AND *RAS SIGNALS ARE GENERATED IN THE MEMORY FROM THE RFSH SIGNAL.

Figure 2-7 RFSH Signal Timing

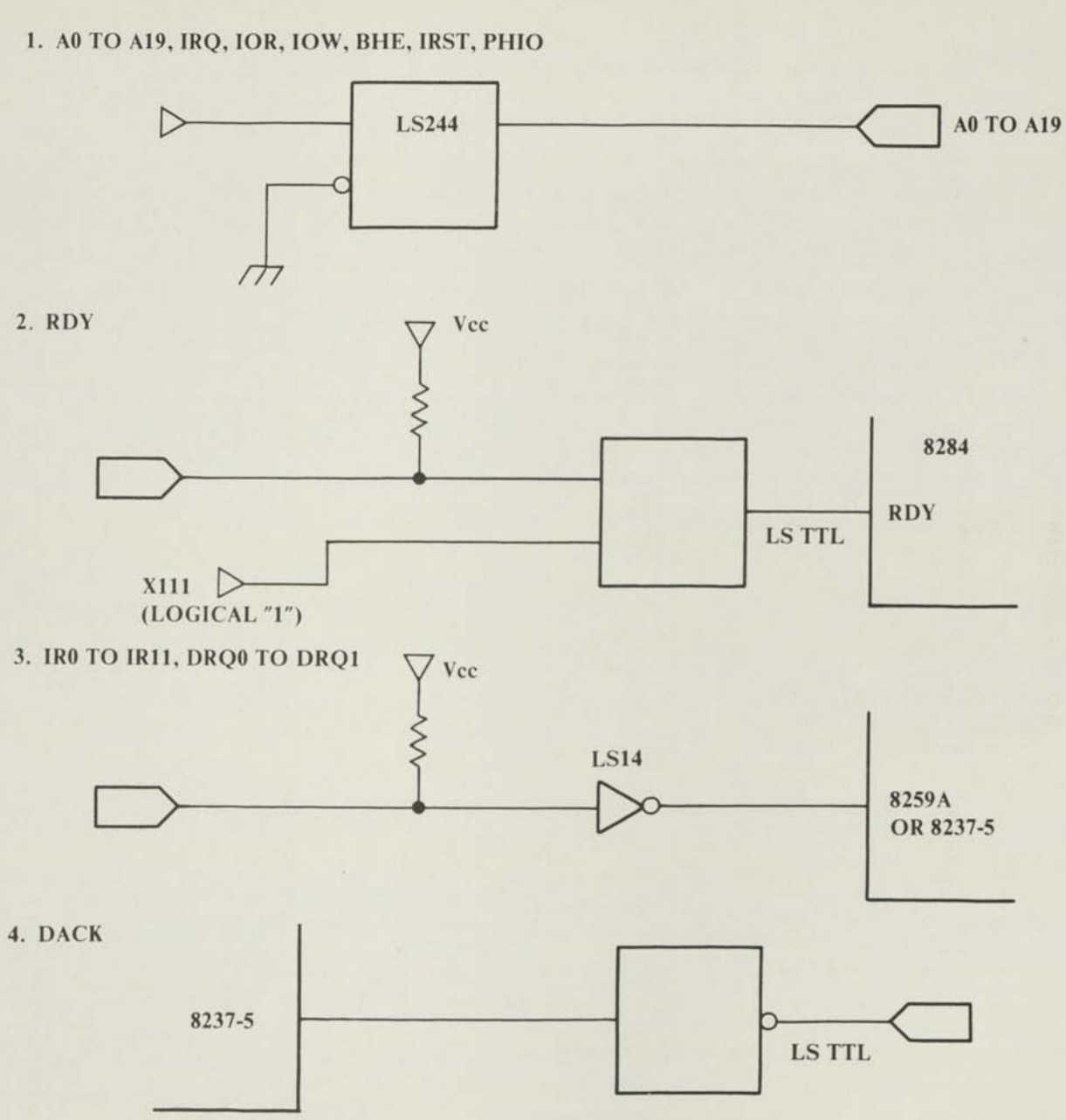
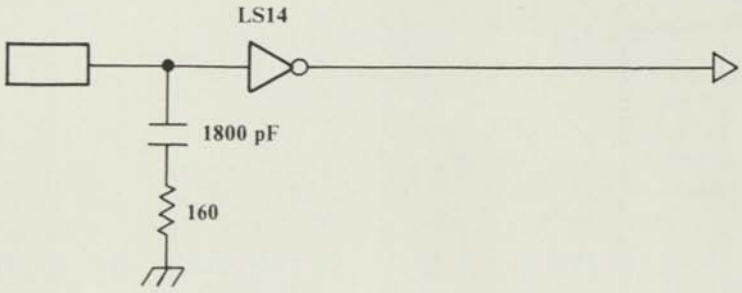
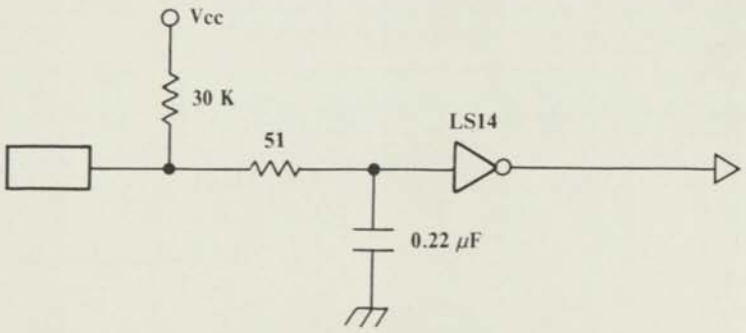


Figure 2-8 Processor Interface Circuits

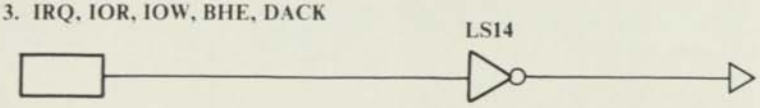
1. PHIO



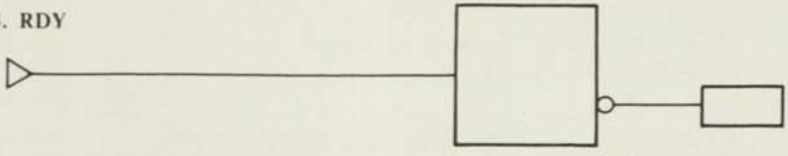
2. IRST



3. IRQ, IOR, IOW, BHE, DACK



4. RDY



5. IR0 TO IR11, DRQ0 TO DRQ1 (LS TTL)

Figure 2-9 Device Interface Circuits

2.2 MICROPROCESSOR

The functional heart of the Processor PCB is the NEC μPD8086 Microprocessor, an NEC-manufactured device physically and logically interchangeable with the Intel 8086.

The 8086 is a high-performance 16-bit CPU packaged in a single 40-pin Dual In-line Package (DIP) chip. It has a direct addressing capability to 1 MB of memory on a 20-bit address bus, of which bits 0 through 15 are time-multiplexed for the 16-bit data bus. It is driven at a 4.9152 MHz clock rate and is used in maximum operating mode (using an external 8288 bus controller).

In general, the 8086 processes a program by repeated cycling through four clock steps, T1 through T4:

T1 fetches an instruction from memory

T2 reads in any required operand

T3 executes the instruction

T4 writes any required result.

In the 8086, two separate processors perform these steps independently and simultaneously: (1) an execution unit that executes instructions, and (2) a bus interface unit that fetches instructions and queues them up for use by the execution unit.

All registers and data paths within the execution unit are 16 bits wide for fast operation. A 16-bit arithmetic-logic unit manages the general registers and instruction operands and maintains status and control flags. The execution unit is a strictly internal device and has no connection to the outside world. All instructions and memory access operations are accomplished by the bus interface unit.

The bus interface unit functions as a good secretary by anticipating the needs of the execution unit and lining up sequential instructions for ready access. These instructions are stored in an internal queue RAM with a capacity of six bytes. The bus interface unit is programmed to keep this RAM filled, fetching two bytes at a time from even addresses and one byte at a time from odd addresses. When the execution unit requests a memory or I/O read or write, the bus interface unit discontinues instruction fetching and responds to the execution unit request. If the instruction executed calls for control transfer to another location, the bus interface unit empties the queue RAM, fetches the instruction from the new location, and feeds it directly to the execution unit. Then the bus interface unit proceeds to refill the queue RAM from sequential instructions from the new location.

The 1,048,576 bytes of available memory space are addressed as if divided into logical segments of up to 64 KB each. The 8086 has direct access to four segments at a time, each of which has a base address carried in one of four segment registers: the Code Segment (CS), Data Segment (DS), Stack Segment (SS), and Extra Segment (ES). The Instruction Pointer (IP) register contains the present offset distance in bytes, which completes the logical address of the next address to be processed. The result of this memory organization is that the 20-bit physical memory address can be defined by a logical address consisting of two 16-bit bytes, the first specifying the base address of the selected segment and the second specifying the relative address within that segment, counting from the base address. To convert a logical address to a physical address, first shift the base address byte 4 bits to the left by multiplying it by sixteen, then add the result to the offset byte.

2.3 DIRECT MEMORY ACCESS

Because it bypasses processor intervention, DMA provides a much faster way of moving data between I/O devices and memory. Supported by the NEC LSI 8237-5 DMA Controller, DMA employs 16 address lines and 4 bits of page addressing, thus enabling it to address one megabyte of memory. Although the DMA is a synchronous device, it can interface with low-speed memory or I/O devices by using the external Ready line.

The four DMA channels are assigned as follows:

Channel 0 CRT
Channel 1 FDD
Channel 2 Reserved for graphic operations option
Channel 3 Future.

See Table 2-2 for a list of instructions and I/O addresses. Figures 2-10, 2-11, and 2-12 show the DMA registers.

Table 2-2 DMA Instructions

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
			7	6	5	4	3	2	1	0
Write Command	W	09	KS	DS	WS	PR	TM	CE	AH	MM
Write Mode	W	1B	MS1	MS0	ID	AT	TR1	TR0	CS1	CS0

Table 2-2 DMA Instructions (cont'd)

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS 7	6	5	4	3	2	1	0
Write RQ Register	W	19	—	—	—	—	—	RB	CS1	CS0
Write Single Mask	W	0B	—	—	—	—	—	MK	CS1	CS0
Write All Mask	W	1F	—	—	—	—	MB3	MB2	MB1	MB0
Read Status	R	09	RQ3	RQ2	RQ1	RQ0	TC3	TC2	TC1	TC0
CH0 DMA Address	R/W	01	A7 A15	A6 A14	A5 A13	A4 A12	A3 A11	A2 A10	A1 A9	A0 A8
CH0 DMA Count	R/W	11	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8
CH1 DMA Address	R/W	03	A7 A15	A6 A14	A5 A13	A4 A12	A3 A11	A2 A10	A1 A9	A0 A8
CH1 DMA Count	R/W	13	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8
CH2 DMA Address	R/W	05	A7 A15	A6 A14	A5 A13	A4 A12	A3 A11	A2 A10	A1 A9	A0 A8
CH2 DMA Count	R/W	15	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8
CH3 DMA Address	R/W	07	A7 A15	A6 A14	A5 A13	A4 A12	A3 A11	A2 A10	A1 A9	A0 A8
CH3 DMA Count	R/W	17	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8

Table 2-2 DMA Instructions (cont'd)

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS 7	6	5	4	3	2	1	0
CH0 Page Register	W	38	0	0	0	0	A 19	A 18	A 17	A 16
CH1 Page Register	W	3A	0	0	0	0	A 19	A 18	A 17	A 16
CH2 Page Register	W	3C	0	0	0	0	A 19	A 18	A 17	A 16
CH3 Page Register	W	3E	0	0	0	0	A 19	A 18	A 17	A 16
Read Temp Register	R	1D	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
Master Clear	W	1D	—	—	—	—	—	—	—	—

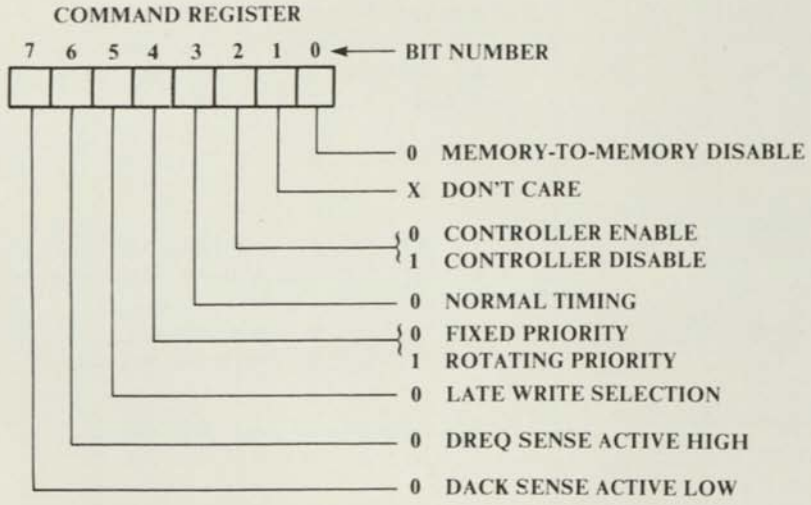


Figure 2-10 DMA Command and Mode Registers

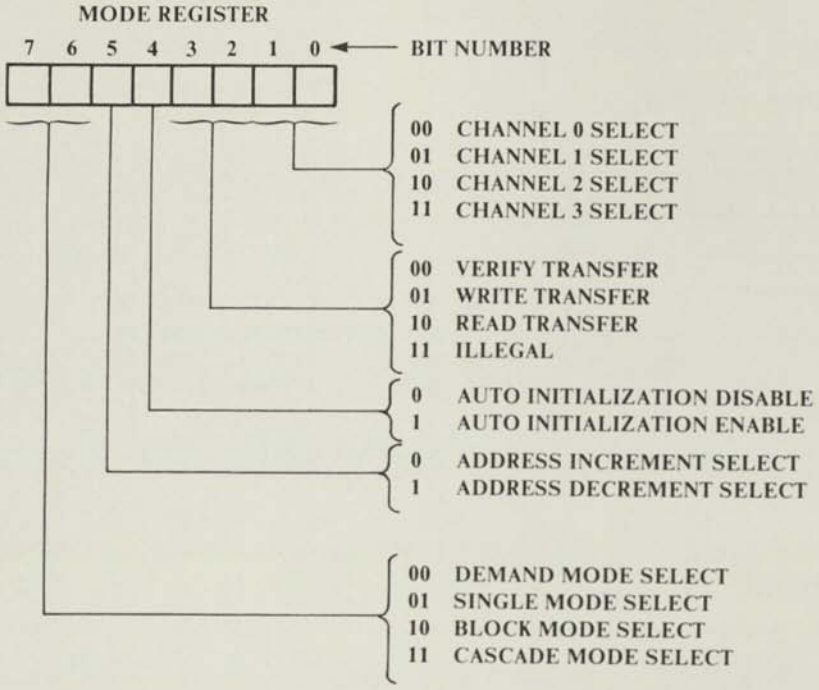
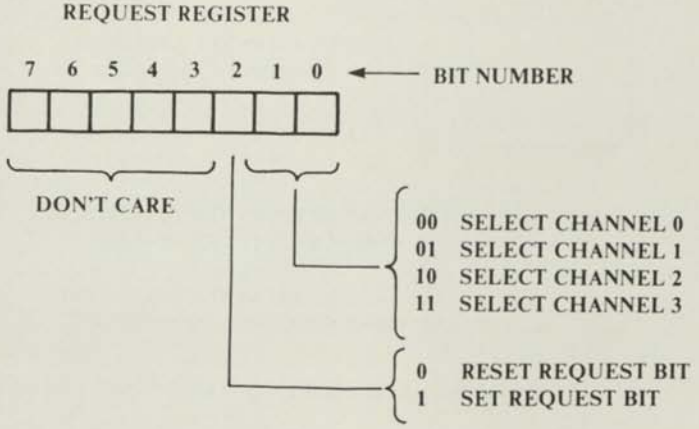
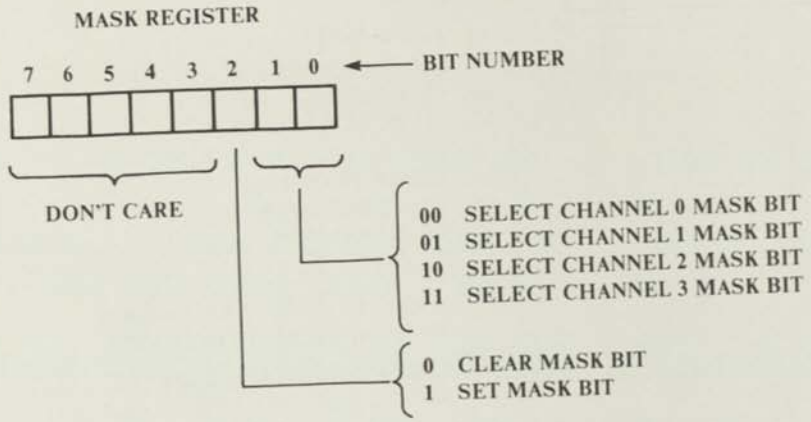


Figure 2-10 DMA Command and Mode Registers (cont'd)

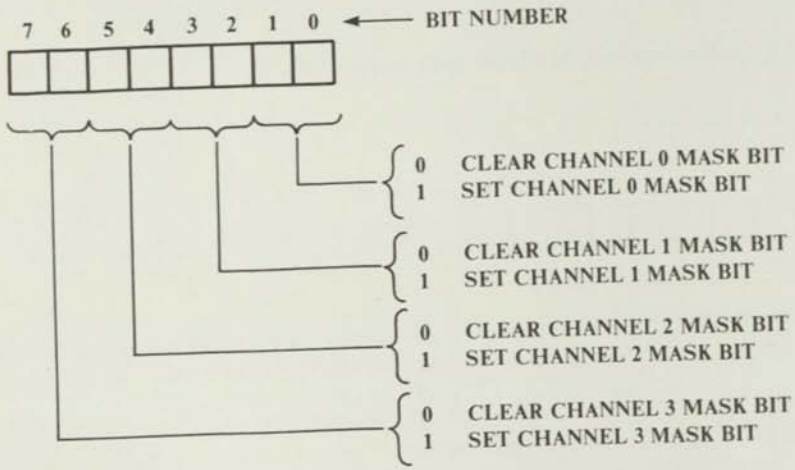


SOFTWARE REQUESTS WILL BE SERVICED ONLY IF THE CHANNEL IS IN BLOCK MODE.

Figure 2-11 DMA Request and Mask Register

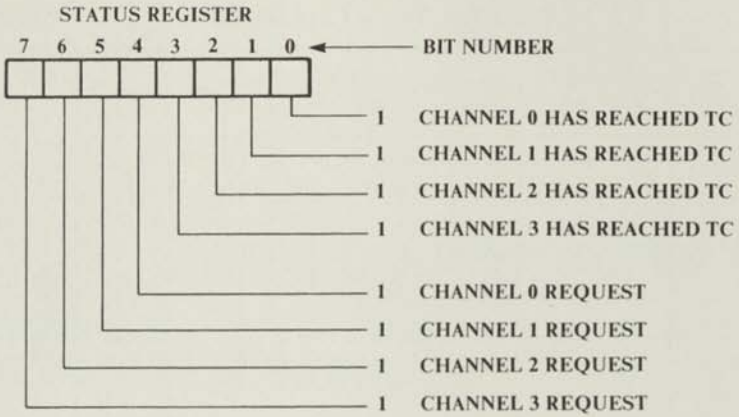


THE INSTRUCTION, WHICH SEPARATELY SETS OR CLEARS THE MASK BITS, IS SIMILAR IN FORM TO THAT USED WITH THE REQUEST REGISTER.



ALL FOUR BITS OF THE MASK REGISTER MAY ALSO BE WRITTEN WITH A SINGLE COMMAND.

Figure 2-11 DMA Request and Mask Register (cont'd)



THIS INFORMATION INCLUDES WHICH CHANNELS HAVE REACHED A TERMINAL COUNT AND WHICH CHANNELS HAVE A PENDING DMA REQUEST. BITS 0 THROUGH 3 ARE SET EVERY TIME A TC IS REACHED BY THAT CHANNEL OR AN EXTERNAL $\overline{EOP}$ IS APPLIED. THESE BITS ARE CLEARED UPON RESET AND ON EACH STATUS READ.

Figure 2-12 DMA Status Register

2.4 INTERVAL TIMER

The NEC μPD8253-5 Programmable Interval Timer has three timer counter outputs: Channel 0 is attached to interrupt-request Channel 3; Channel 1 is sent to the synchronous/asynchronous communications controller on the Controller PCB (see Chapter 3); Channel 2 is not used. Figure 2-13 is a block diagram of the interval timer. Table 2-3 lists the timer commands.

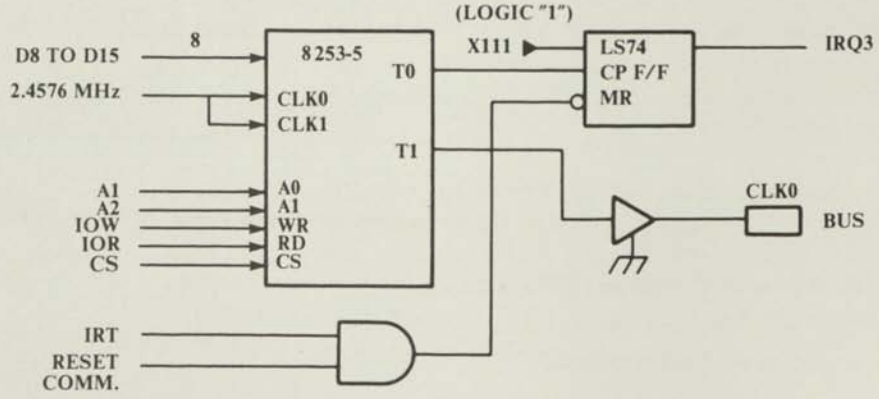


Figure 2-13 Interval Timer Block Diagram

Table 2-3 Timer Commands

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
			7	6	5	4	3	2	1	0
Load Counter 0	W	29	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Load Counter 1	W	2B	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Mode Set	W	2F	SC 1	SC 0	RL 1	RL 0	M2	M1	M0	BCD
Timer Reset	W	46	X	X	X	X	X	TM	X	X
X: Don't care.										

2.5 INTERRUPT CONTROL

This interrupt function is controlled by two 8259 Metal Oxide Semiconductor (MOS) devices; each can handle up to eight vectored priority interrupts, as shown in Figure 2-14. The first 8259 device (master) supports IR0 through IR6, with IR7 cascaded from the second 8259 device (slave), which supports IR7 through IR14. These 15 available interrupt lines are assigned to service specific devices in order of priority. Table 2-4 lists the interrupt lines.

There are two interactions between the processor and the interrupt controller. The first is the acknowledgement process, during which the processor transmits acknowledgement of the interrupt request to the interrupt controller. During the second process, the interrupt controller transmits a byte of data to the processor (see Table 2-4).

Control commands issued by the processor, consisting of Initialization Command Words (ICW) and Operational Command Words (OCW), are summarized in Table 2-5 and shown in Figures 2-15 and 2-16. Table 2-5 also includes poll mode, read interrupt register (IRR), read inservice register (ISR), and interrupt register words that are read into the data bus by the interrupt controller when so commanded.

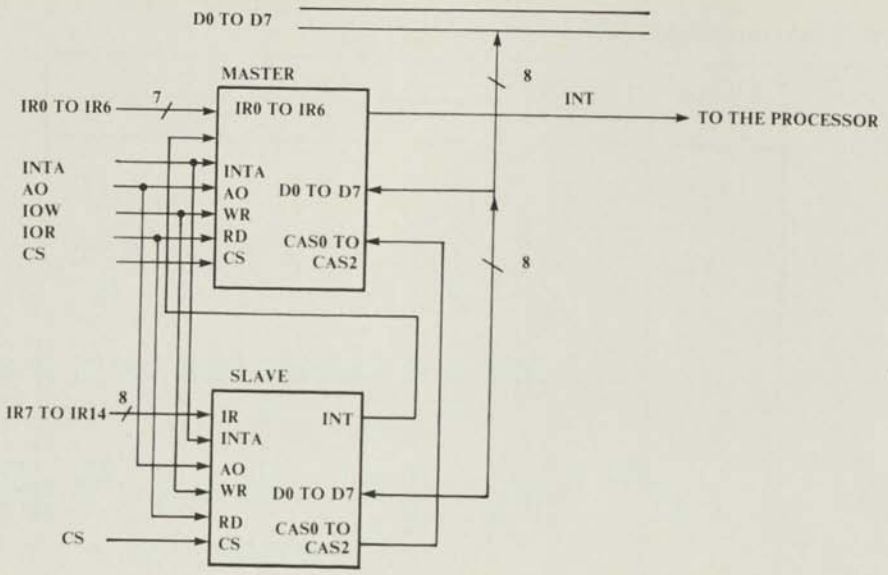


Figure 2-14 Interrupt Control Block Diagram

Table 2-4 Interrupt Lines

DEVICE	INTERRUPT REQUEST LINE	ASSIGNMENT	INTERRUPT VECTOR BYTE
Master	IR0	Not used	T7 T6 T5 T4 T3 0 0 0
	IR1	Communication	T7 T6 T5 T4 T3 0 0 1
	IR2	Not used	T7 T6 T5 T4 T3 0 1 0
	IR3	Timer	T7 T6 T5 T4 T3 0 1 1
	IR4	Keyboard	T7 T6 T5 T4 T3 1 0 0
	IR5	Not used	T7 T6 T5 T4 T3 1 0 1
	IR6	Not used	T7 T6 T5 T4 T3 1 1 0
Slave	IR7	Printer	T7 T6 T5 T4 T3 0 0 0
	IR8	Not used	T7 T6 T5 T4 T3 0 0 1
	IR9	Not used	T7 T6 T5 T4 T3 0 1 0
	IR10	CRT	T7 T6 T5 T4 T3 0 1 1
	IR11	FDD	T7 T6 T5 T4 T3 1 0 0
	IR12	Not used	T7 T6 T5 T4 T3 1 0 1
	IR13	Not used	T7 T6 T5 T4 T3 1 1 0
	IR14	APU	T7 T6 T5 T4 T3 1 1 1

Table 2-5 Interrupt Control Commands Summary

DEVICE	INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
				7	6	5	4	3	2	1	0
Master	ICW 1	W	20	0	0	0	1	0	0	0	1
	ICW 2	W	22	T7	T6	T5	T4	T3	0	0	0
	ICW 3	W	22	1	0	0	0	0	0	0	0
	ICW 4	W	22	0	0	0	0	0	0	0	1
	OCW 1	W	22		M6	M5	M4	M3	M2	M1	M0
	OCW 2	W	20	R	SL	EOI	0	0	L2	L1	L0
	OCW 3	W	20	0	ESM	SMM	0	1	P	PR	RIS
	Poll Mode	R	20	I	—	—	—	—	W2	W1	W0
	Read IRR	R	20		IR6	IR5	IR4	IR3	IR2	IR1	IR0
	Read ISR	R	20		IS6	IS5	IS4	IS3	IS2	IS1	IS0
	Read Mask	R	22		M6	M5	M4	M3	M2	M1	M0
Slave	ICW 1	W	28	0	0	0	1	0	0	0	1
	ICW 2	W	2A	T7	T6	T5	T4	T3	0	0	0
	ICW 3	W	2A	0	0	0	0	0	1	1	1
	ICW 4	W	2A	0	0	0	0	0	0	0	1

Table 2-5 Interrupt Control Commands Summary (cont'd)

DEVICE	INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS 7	6	5	4	3	2	1	0
	OCW 1	W	2A	M14	M13	M12	M11	M10	M9	M8	M7
	OCW 2	W	28	R	SL	EOI	0	0	L2	L1	L0
	OCW 3	W	28	0	ESM	SMM	0	1	P	RR	RIS
	Poll Mode	R	28	I	—	—	—	—	W2	W1	W0
	Read IRR	R	28	IR 14	IR 13	IR 12	IR 11	IR 10	IR 9	IR 8	IR 7
	Read IRR	R	28	IS 14	IS 13	IS 12	IS 11	IS 10	IS 9	IS 8	IS 7
	Read Mask	R	2A	M14	M13	M12	M11	M10	M9	M8	M7

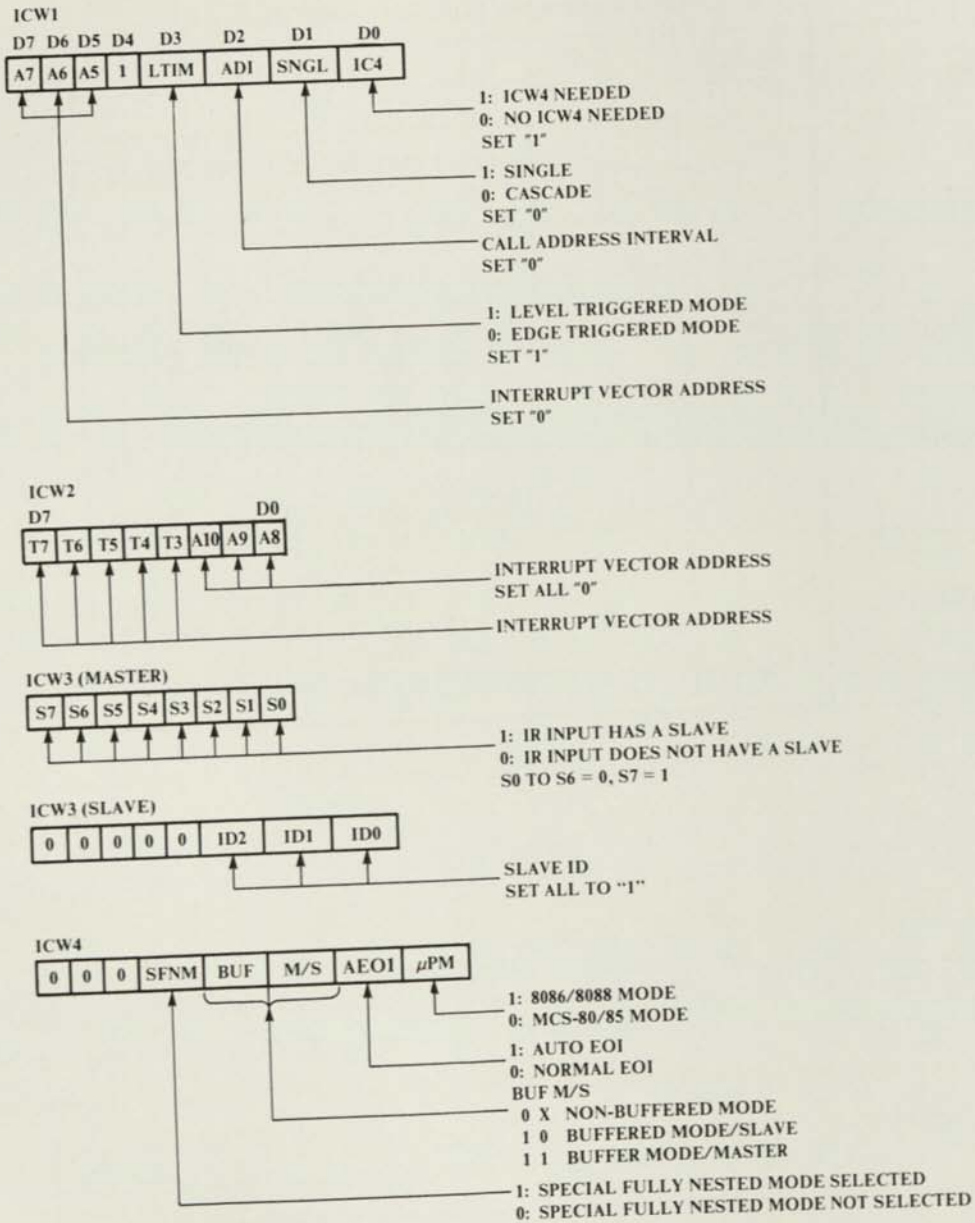


Figure 2-15 Interrupt Initialization Command Words

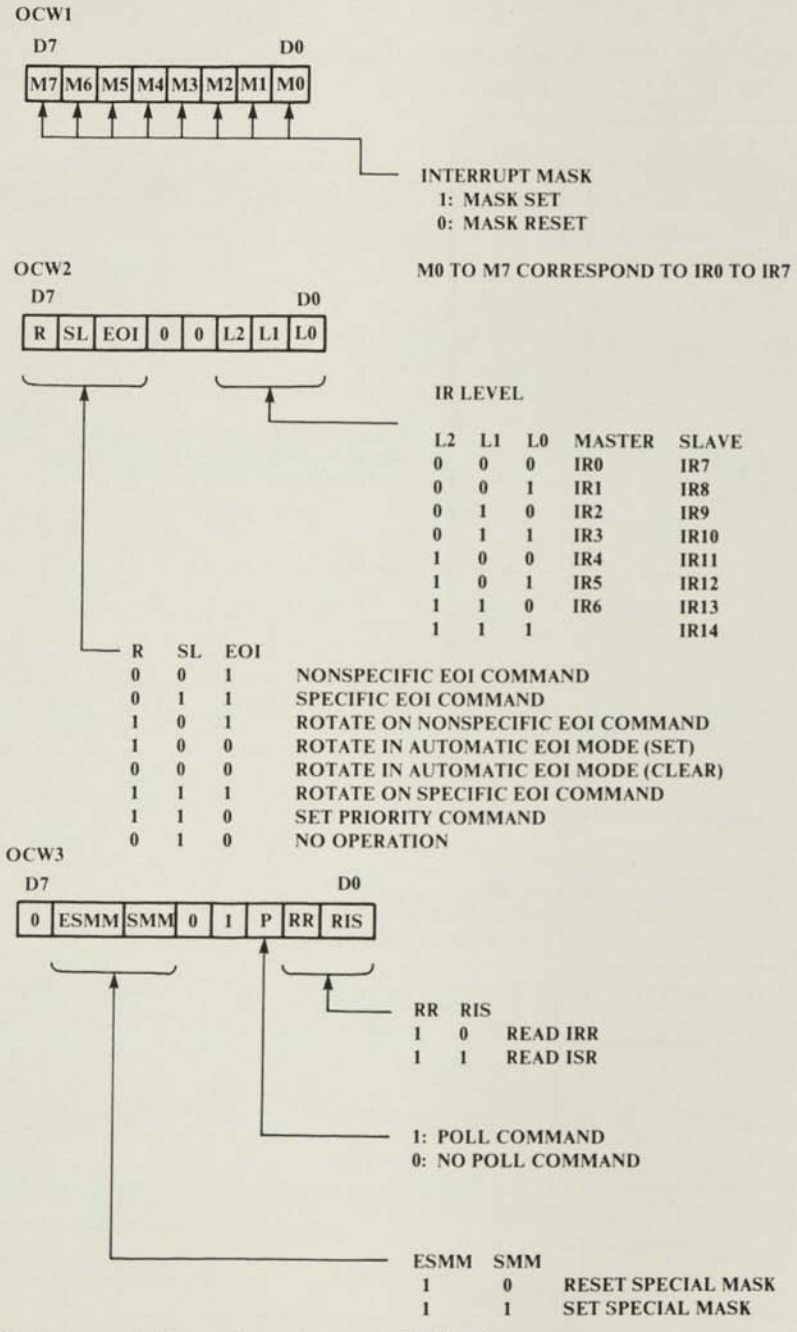


Figure 2-16 Interrupt Operation Command Words

2.6 MEMORY

Figure 2-17 is the system memory map that shows how the memory space addresses are allocated.

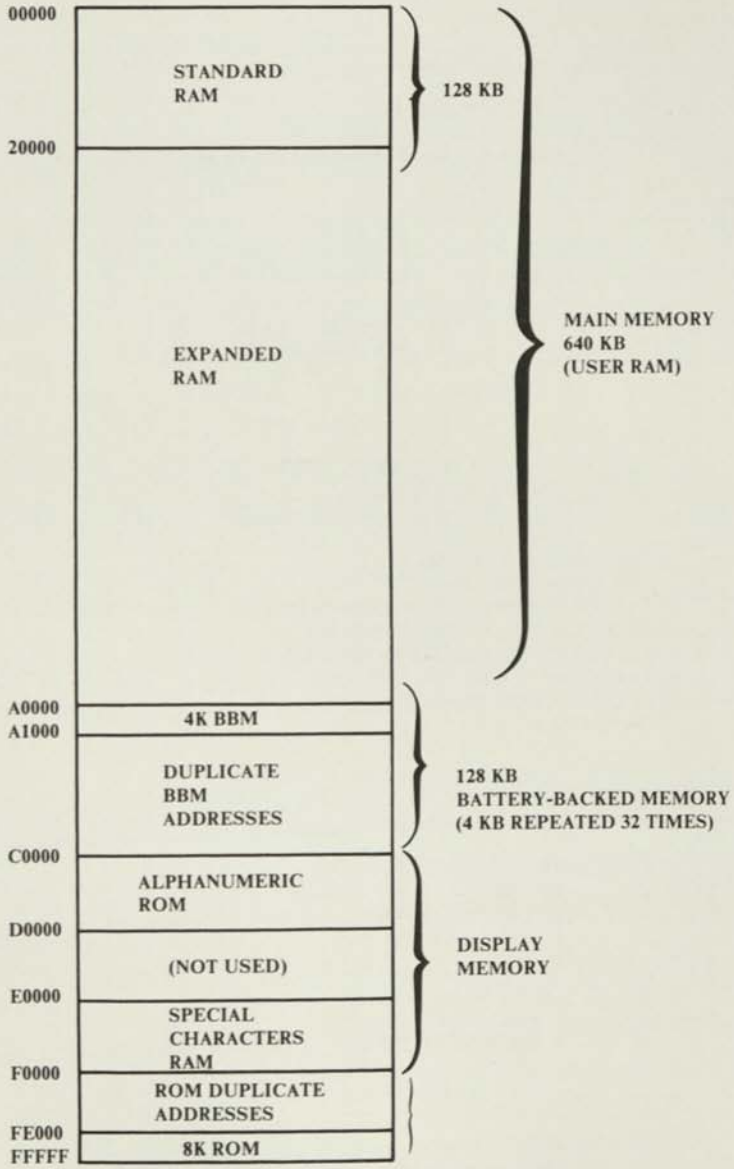


Figure 2-17 System Memory Map

2.6.1 Main Memory

The Processor PCB contains 128 KB (64 Kwords: 16 bits of data, 18 bits wide, with 1 bit parity for each 8 bits) of RAM, organized into eighteen 64K x 1-bit dynamic memory chips. Figure 2-18 is a block diagram of the circuit. The RAM is refreshed during the non-memory-access cycle, and its access time is 200 ns. Parity check is carried out with two additional memory chips. A detected parity error lights the D4 red Light Emitting Diode (LED), located near the top edge of the Processor PCB.

As shown in Figure 2-17, the main memory is expandable to a maximum of 640 KB, of which 256 KB can be supported by the present APC equipment configuration.

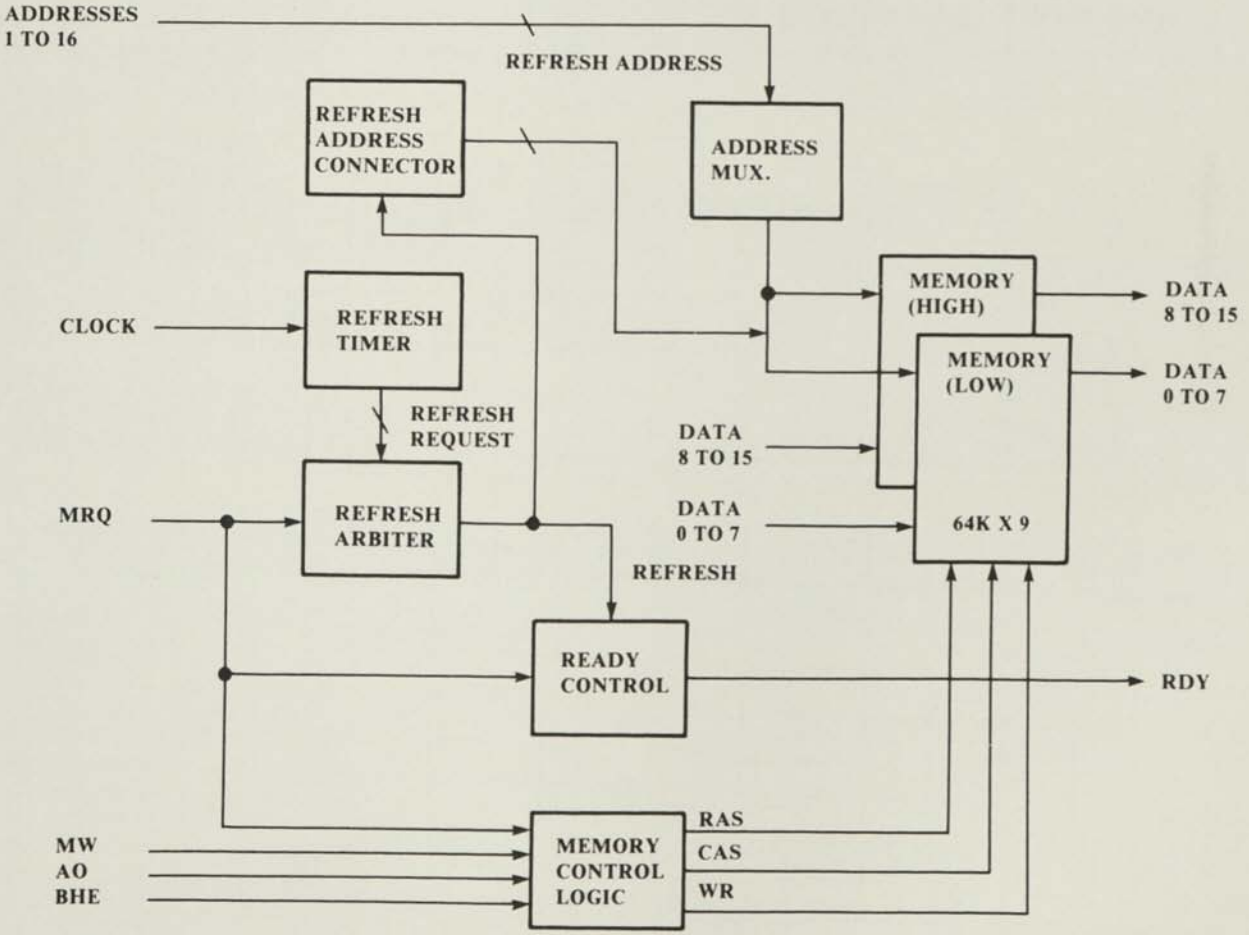


Figure 2-18 Main Memory Block Diagram

2.6.2 Battery-Backed Memory

The BBM is composed of 4K (two 2K X 8-bit chips) of Complementary Metal Oxide Semiconductor (CMOS) static RAM and is addressable from A0000 through C0000 hexadecimal (HEX) in 32 4K visible sections of memory, each section containing the same data. The APC uses partial address decoding of this 128 KB of memory, which results in 4 KB of BBM. The BBM contains system information and is protected from loss for at least two years by the battery that plugs into the Processor PCB.

As shown in Figure 2-19, the BBM read/write operation is identical to that of the main memory except for a BBM write protect circuit that safeguards the BBM from unintentional data manipulation.

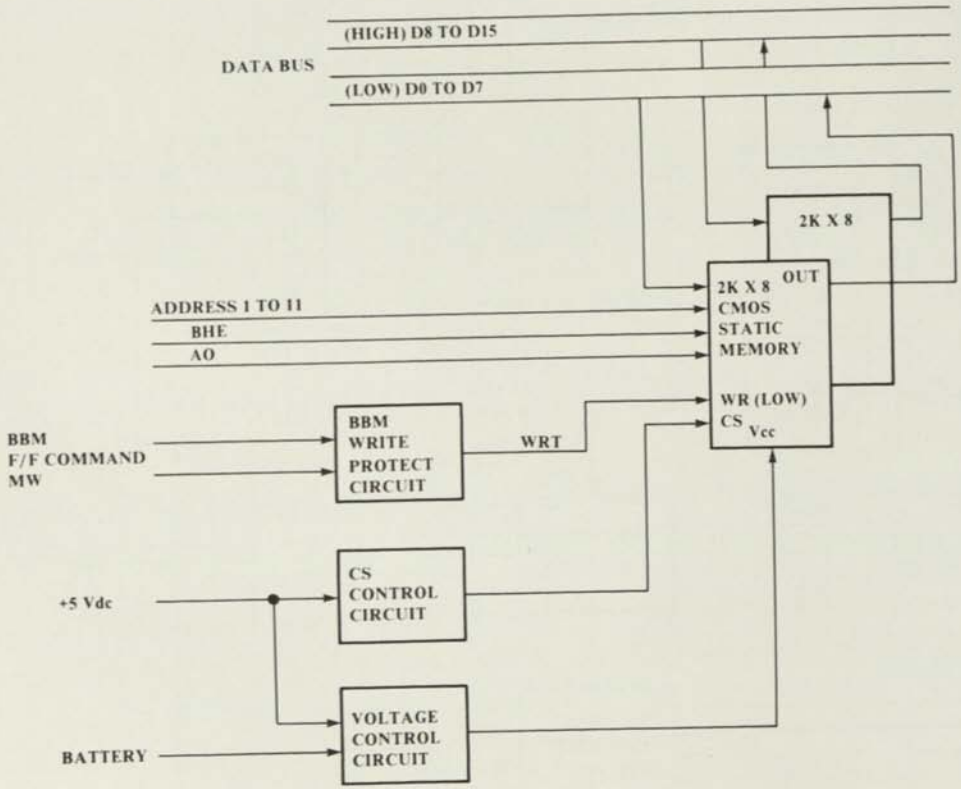


Figure 2-19 Battery-Backed Memory Block Diagram

The BBM write protect command I/O port address is 59(HEX). A logical "1" on the Least Significant Bit (LSB) position on the data bus enables writing to the BBM; a "0" sets the BBM for write protection.

2.6.3 Read Only Memory

The Processor PCB contains 8K of ROM in two 4K x 8-bit Erasable Programmable Read-Only Memory (EPROM) chips. The ROM has two functions: flexible disk self-testing and bootstrap loading. As shown in Figure 2-17, the ROM occupies the 8K addresses from FE000 through FFFFF and is visible in eight duplicate 8K sections from F0000 through FFFFF. At APC power-on, the 8086 code segment and instruction-pointer registers are set to FFFF(HEX) and 0000(HEX) addresses respectively for loading and auto self-test, instructions for which are resident in the ROM.

2.7 PARALLEL PRINTER CONTROL

This portion of the logic provides an I/O TTL interface with an external parallel-data-bus printer.

As shown in Figures 2-20 and 2-21, the parallel printer control consists of an NEC μPD8255A Programmable Peripheral Controller that interfaces with connector CN2 through LS244 drivers. A flat-type 26-conductor cable connects the CN2 board connector to a connector at the rear of the main unit that, in turn, goes to the printer. The pin connections are listed in Table 2-6. The interface is adaptable to either an Output Device Adapter (ODA) or Centronics-type printer by setting appropriate jumpers on TM2, TM3, and TM4 on the Processor PCB (see Figure 2-29).

2.7.1 Interface

Table 2-7 lists the interface lines.

2.7.2 Programming Considerations

The 8255A device is operated in the APC as Mode 0 (basic I/O) in the Group A ports (Port A and upper 4 lines of Port C), and Mode 1 (strobed) in the Group B ports (Port B and lower 4 lines of Port C). The eight lines of Port B (PB0 through PB7) carry the strobed data to the printer; I/O control line levels are from Ports A and C.

Programming and execution of the 8255 is accomplished using the instructions described in Tables 2-8 and 2-9. Figures 2-22 and 2-23 show interline timing under various operating conditions.

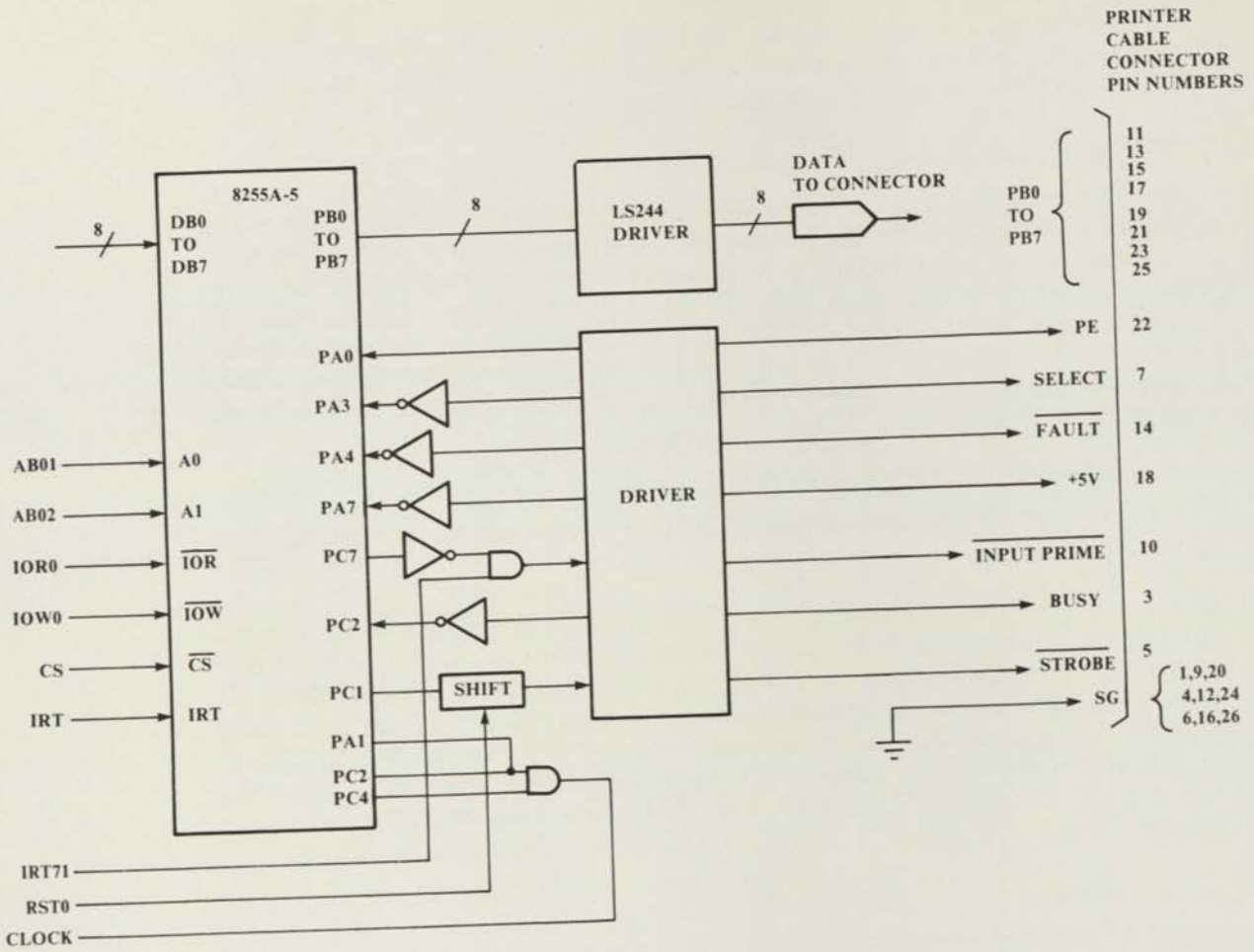
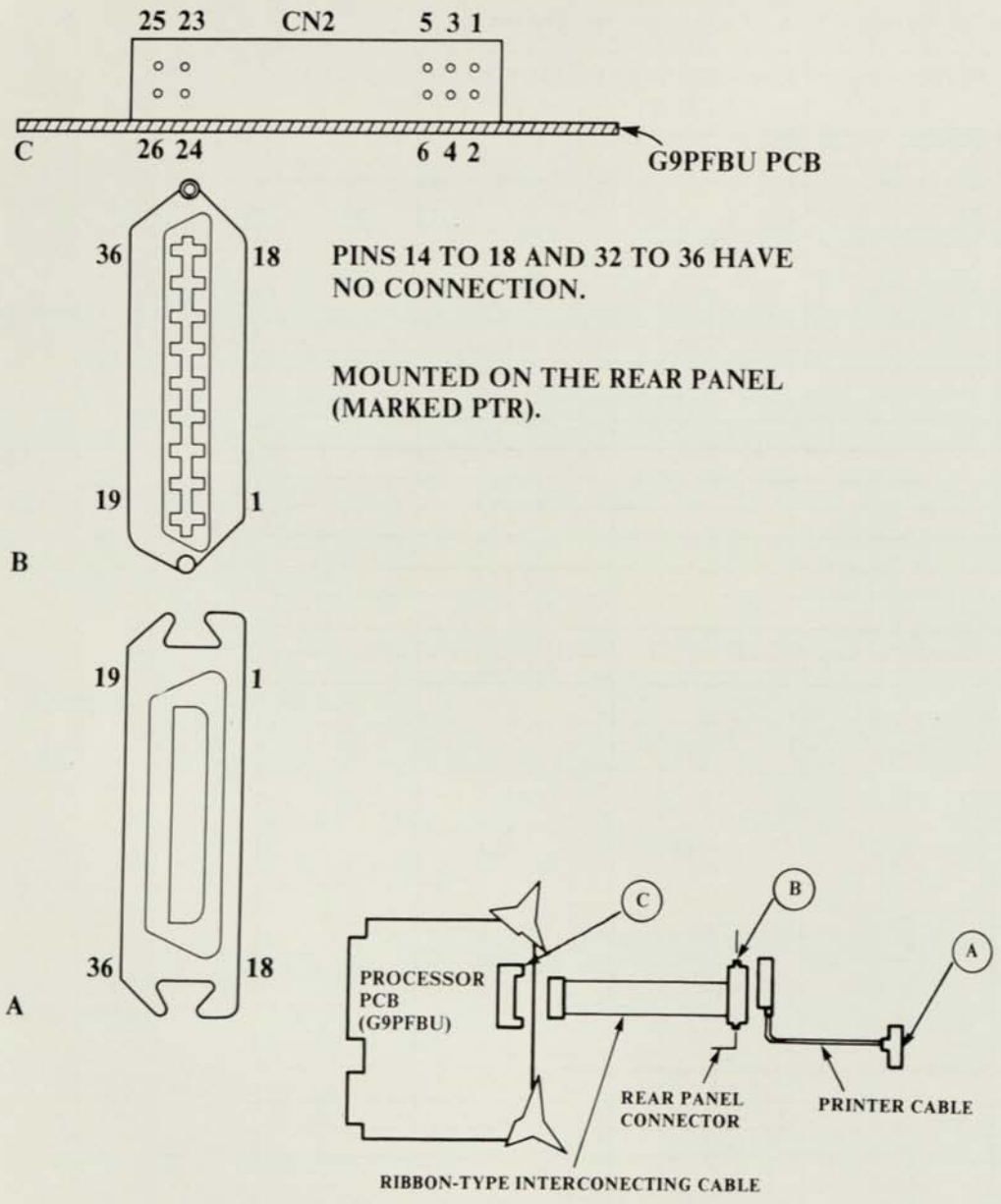


Figure 2-20 Parallel Printer Control Block Diagram

Table 2-6 Parallel Printer Connectors Pin Assignments

SIGNAL	PIN NUMBER AT A	PIN NUMBER AT B	PIN NUMBER AT C	REMARKS
$\overline{\text{DATA STB}}$	1	3	2	
DATA 1	2	6	16	
DATA 2	3	7	4	
DATA 3	4	8	17	
DATA 4	5	9	5	
DATA 5	6	10	18	
DATA 6	7	11	6	
DATA 7	8	12	19	
DATA 8	9	13	7	
$\overline{\text{ACK}}$	10	2	14	
Input Busy	11	22	9	
PE	12	29	25	
SELECT	13	4	15	
Signal Ground	14	NC	NC	
NC	15	NC	NC	
Signal Ground	16	NC	NC	
Chassis Ground	17	NC	NC	
+5 Vdc	18	27	NC 24	
Twisted Pair -				
Ground (Pin 1)	19	NC	NC	
Ground (Pin 2)	20	20	8	
Ground (Pin 3)	21	21	21	
Ground (Pin 4)	22	5	3	
Ground (Pin 5)	23	24	10	
Ground (Pin 6)	24	26	11	
Ground (Pin 7)	25	28	12	
Ground (Pin 8)	26	30	13	
Ground (Pin 9)	27	31	26	
Ground (Pin 10)	28	NC		
Ground (Pin 11)	29	NC		
Ground (Pin 31)	30	NC		
$\overline{\text{Input Prime}}$	31	23	22	
$\overline{\text{Fault}}$	32	25	23	
Signal Ground	33	NC	NC	
NC	34	NC	NC	
NC	35	18		
Input Busy	36	NC	NC	
		19	20	No signal
		1	1	No signal

NOTE: NC means No Connection.



NOTE: SEE TABLE 2-6 FOR PIN NUMBERS AT LOCATIONS A, B, AND C.

Figure 2-21 Parallel Printer Cable Connect

Table 2-7 Parallel Printer Interface Signals

SIGNAL	SOURCE	DESCRIPTION
RMS	APC	*Receive Machine Set.* This signal is used with the ODA printer interface only.
BUSY	Printer	Goes high to indicate that the printer cannot receive data: 1. During data entry 2. During printing operation 3. In offline state 4. During printer error status.
$\overline{\text{STROBE}}$	APC	Strobe pulse to read data in. The signal level is normally High. Read-in of data is performed at the Low level of this signal.
SG		Twisted-pair return signal ground level.
SELECT	Printer	Goes high to indicate that the printer is in selected state.
$\overline{\text{ACKNLG}}$	Printer	Acknowledge goes Low to indicate that data has been received and that the printer is ready to accept other data.

Table 2-7 Parallel Printer Interface Signals (cont'd)

SIGNAL	SOURCE	DESCRIPTION
$\overline{\text{INPUT PRIME}}$	APC	Goes Low to initialize the printer.
DATA 1	APC	Data lines from 8255A, PB0 through PB7. High is logic 1; Low is logic 0.
DATA 2	APC	
DATA 3	APC	
DATA 4	APC	
DATA 5	APC	
DATA 6	APC	
DATA 7	APC	
DATA 8	APC	
$\overline{\text{FAULT}}$	Printer	Goes Low when the printer is in 1. Paper End state 2. Offline state 3. Error state.
+5 V	Printer	Device Control (DCN)
PE	Printer	Goes high to indicate that printer is out of paper.

Table 2-8 Parallel Printer Controller Instruction

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
			7	6	5	4	3	2	1	0
Write Signal 0	W	6E	1	0	0	1	0	1	0	0
Write Signal 1	W	6E	0	0	0	0	0	1	0	INTE
Write Signal 2	W	6E	0	0	0	0	0	1	1	RMS
Write Signal 3	W	6E	0	0	0	0	1	0	0	MASK
Write Signal 4	W	6E	0	0	0	0	1	1	1	IRT
Write Signal 5	W	6C	—IP	X	X	MASK	X	X	X	X
Read Signal	R	68	+5V	0	0	—FAULT	SELECT	0	RDRQ	PE
Write Data	W	6A	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1

Table 2-9 Parallel Printer Controller Instruction Sequence

INSTRUCTION	DESCRIPTION
Write Signal 0	Set the 8255 Mode
Write Signal 1	Interrupt Enable Flag (INTE) 1: Flag On 0: Flag Off
Write Signal 2 (Not used for Centronics I/F)	Receive Machine Set (RMS) 1: RMS On 0: RMS Off
Write Signal 3	Mask Set or Reset 1: Reset 0: Set
Write Signal 4	Input Prime (IP) Set or Reset 1: Reset 0: Set
Write Signal 5	IP and Mask Set or Reset
Read Signal	Read the status of the printer
Write Data	Write data to be printed

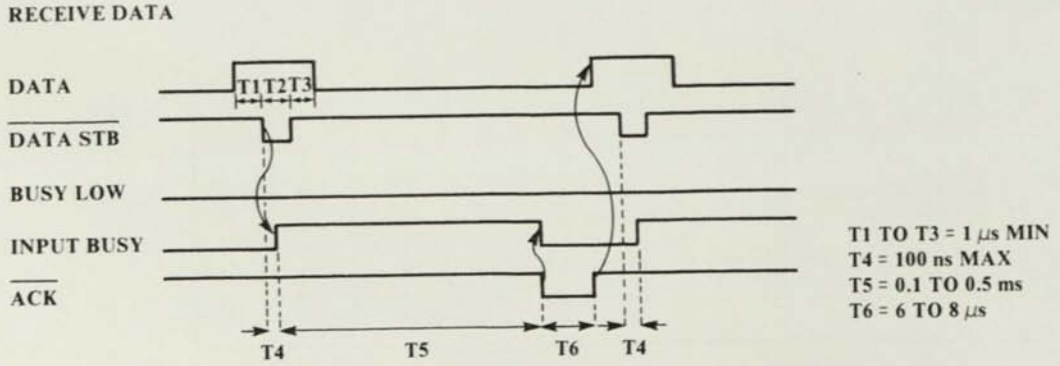


Figure 2-22 Parallel Printer Controller Interface Timing

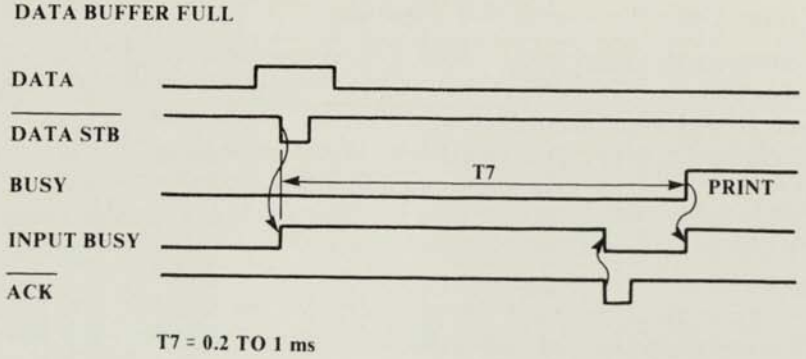


Figure 2-22 Parallel Printer Controller Interface Timing (cont'd)

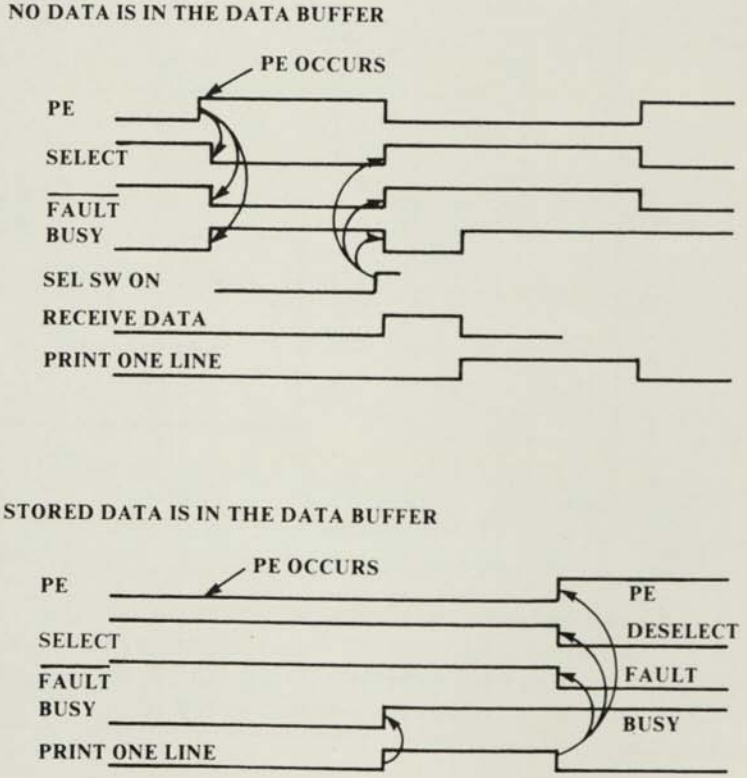


Figure 2-23 Parallel Printer Controller Interface at Paper Out Status

2.8 KEYBOARD

The Keyboard employs capacitance technology and an 8048, 8-bit microprocessor that performs keyboard scanning and coding functions. It contains 109 keys in three major groupings. The central area is a standard typewriter layout. Above the central area are 22 user-definable function keys in a single row. To the right of the central area are 25 keys that consist of a numeric entry pad and a set of cursor/control keys.

As shown in Figure 2-24, the Keyboard is arranged as a matrix (8 x 16), with 128 possible X/Y coordinate output combinations (only 109 of which are represented by key positions). The 8048 microprocessor, in combination with an LS74159 decoder chip, produces a scan code output function peculiar to each key position and shift/control status. These scan codes are sent to the Processor PCB on an eight-bit scan data bus designated SD1 through SD8.

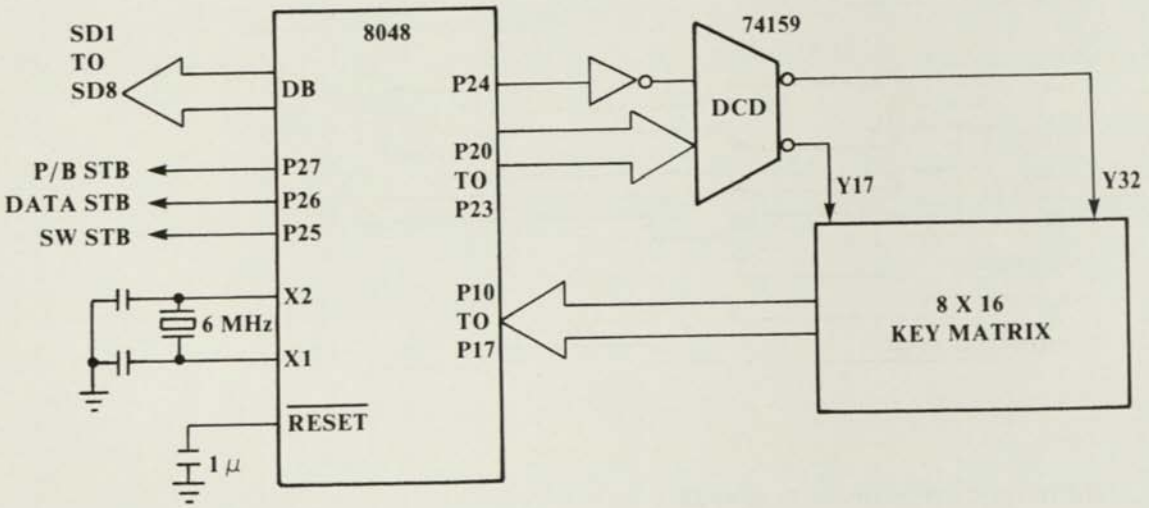


Figure 2-24 Keyboard Block Diagram

Pressing a key produces a strobe that latches the corresponding scan code into a key data register or switch (SW) register located on the Processor PCB and generates an interrupt request. Pressing a switch key (such as FNC or SHIFT) is recorded in an SW register on the Processor PCB, the output of which is combined with the key data register to produce the code output.

The CPU I/O address is hexadecimal 48 for the key data register and 4C for the SW register. The CPU can also read the keyboard status at address 4A.

2.8.1 Keyboard Layout and Scan Codes

The Keyboard layout and designated key position numbers are shown in Figure 2-25. The corresponding scan codes are listed in Table 2-10. The scan codes are usually different than the hex codes for the keys. For hex code information, see Appendix D.

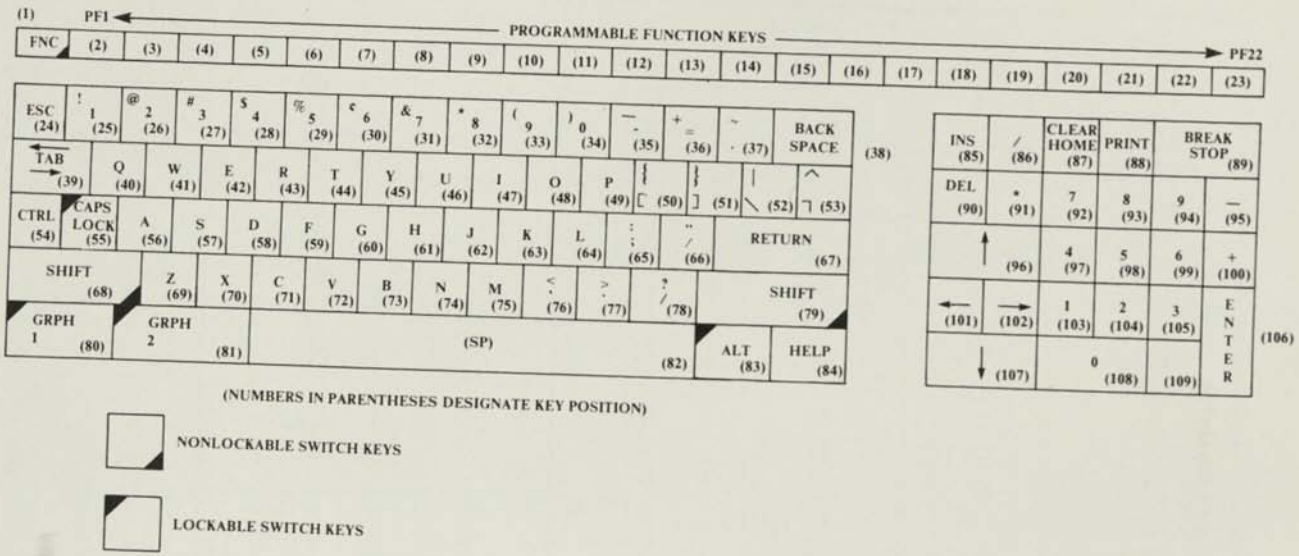


Figure 2-25 Keyboard Layout

Table 2-10 Keyboard Scan Codes

KEY POSITION	SCAN CODE	KEY POSITION	SCAN CODE	KEY POSITION	SCAN CODE
1*	—	38	9C	75	4D
2	80	39	98	76	2C
3	81	40	51	77	2E
4	82	41	57	78	2F
5	83	42	45	79*	—
6	84	43	52	80*	—
7	85	44	54	81*	—
8	86	45	59	82	20

*Positions 1 (FNC), 54 (CTRL), 55 (CAPS LOCK), 68 and 79 (SHIFT), 80 (GRPH 1), 81 (GRPH 2), and 83 (ALT) must be used with another key to generate a scan code.

Table 2-10 Keyboard Scan Codes (cont'd)

KEY POSITION	SCAN CODE	KEY POSITION	SCAN CODE	KEY POSITION	SCAN CODE
9	87	46	55	83*	—
10	88	47	49	84	9E
11	89	48	4F	85	FB
12	8A	49	50	86	6F
13	8B	50	5B	87	9A
14	8C	51	5D	88	FF
15	8D	52	5C	89	96
16	8E	53	5E	90	FC
17	8F	54*	—	91	6A
18	90	55*	—	92	77
19	91	56	41	93	78
20	92	57	53	94	79
21	93	58	44	95	6D
22	94	59	46	96	F7
23	95	60	47	97	74
24	1B	61	48	98	75
25	31	62	4A	99	76
26	32	63	4B	100	6B
27	33	64	4C	101	FA
28	34	65	3A	102	F9
29	35	66	3B	103	71
30	36	67	97	104	72
31	37	68*	—	105	73
32	38	69	5A	106	FD
33	39	70	58	107	F8
34	30	71	43	108	70
35	50	72	56	109	6E
36	2D	73	42		
37	40	74	4E		

*Positions 1 (FNC), 54 (CTRL), 55 (CAPS LOCK), 68 and 79 (SHIFT), 80 (GRPH 1), 81 (GRPH 2), and 83 (ALT) must be used with another key to generate a scan code.

2.8.2 Interface

The Keyboard connects with a coiled multiconductor cable to the rear of the Main Unit (see Figure 2-26 and Table 2-11). The cable is a shielded 19-wire design that includes power (+5 Vdc), grounds, and twelve signal lines. The cable is permanently attached to the Keyboard.

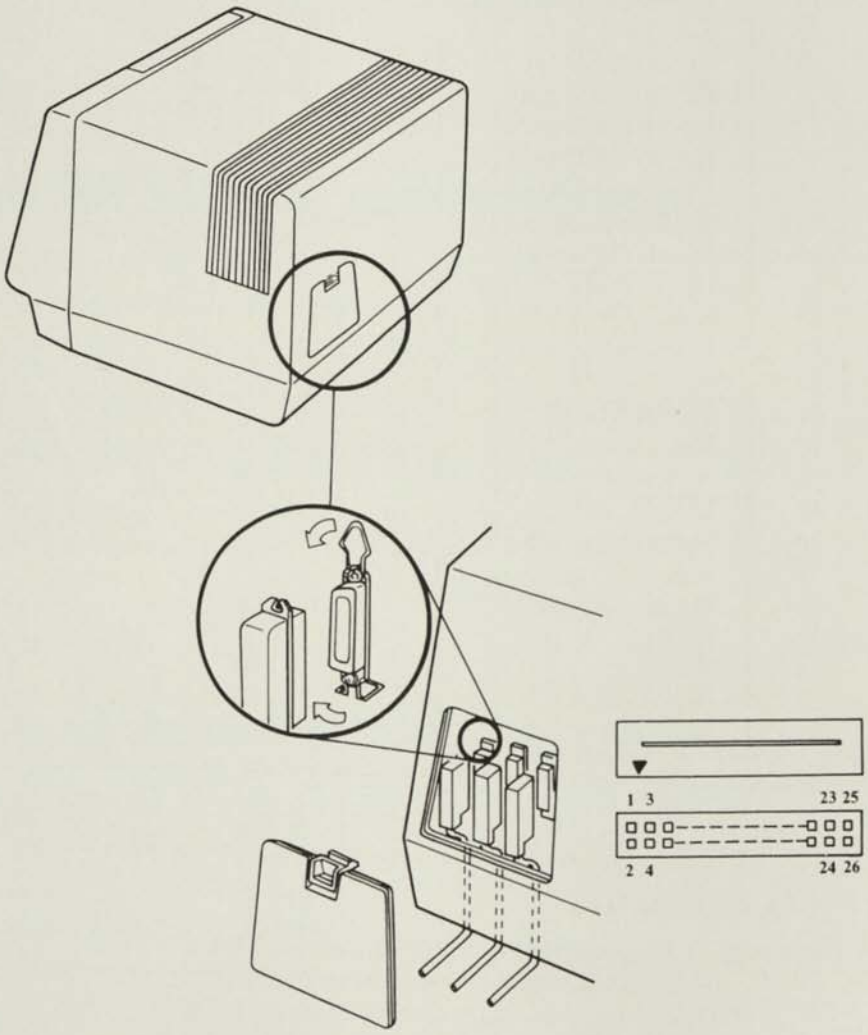


Figure 2-26 Keyboard Interface

Table 2-11 Keyboard Interface Lines

PIN	SIGNAL
1	Not used
2	Not used
3	Keyboard Data 1
4	Keyboard Data 2
5	Keyboard Data 3
6	Keyboard Data 4
7	Keyboard Data 5
8	Keyboard Data 6
9	Keyboard Data 7
10	Keyboard Data 8
11	Signal Ground
12	$\overline{\text{Data Strobe}}$
13	Signal Ground
14	Not used
15	Not used
16	$\overline{\text{Switch Strobe}}$
17	Not used
18	Not used
19	$\overline{\text{Debug}}$
20	Signal Ground
21	Signal Ground
22	Signal Ground
23	+5 Vdc
24	+5 Vdc
25	Not used
26	Not used

2.9 CALENDAR AND CLOCK GENERATOR

The Calendar and Clock Generator is supported by a CMOS Integrated Circuit (IC) (NEC μPD1990AC). This IC independently registers the month, day of the month, day of the week, hour, minute, and second, and it can receive or send this information from or to the microprocessor. Because this IC carries out all clock functions, it frees the microprocessor from these duties, increasing the capabilities of the microprocessor in other areas.

2.9.1 Circuit Description

As shown in Figure 2-27, the clock generator is driven by a 32.768 kHz crystal oscillator. Should a power break occur, system battery power prevents calendar-and-clock data loss. A 14-pin IC encloses all functions.

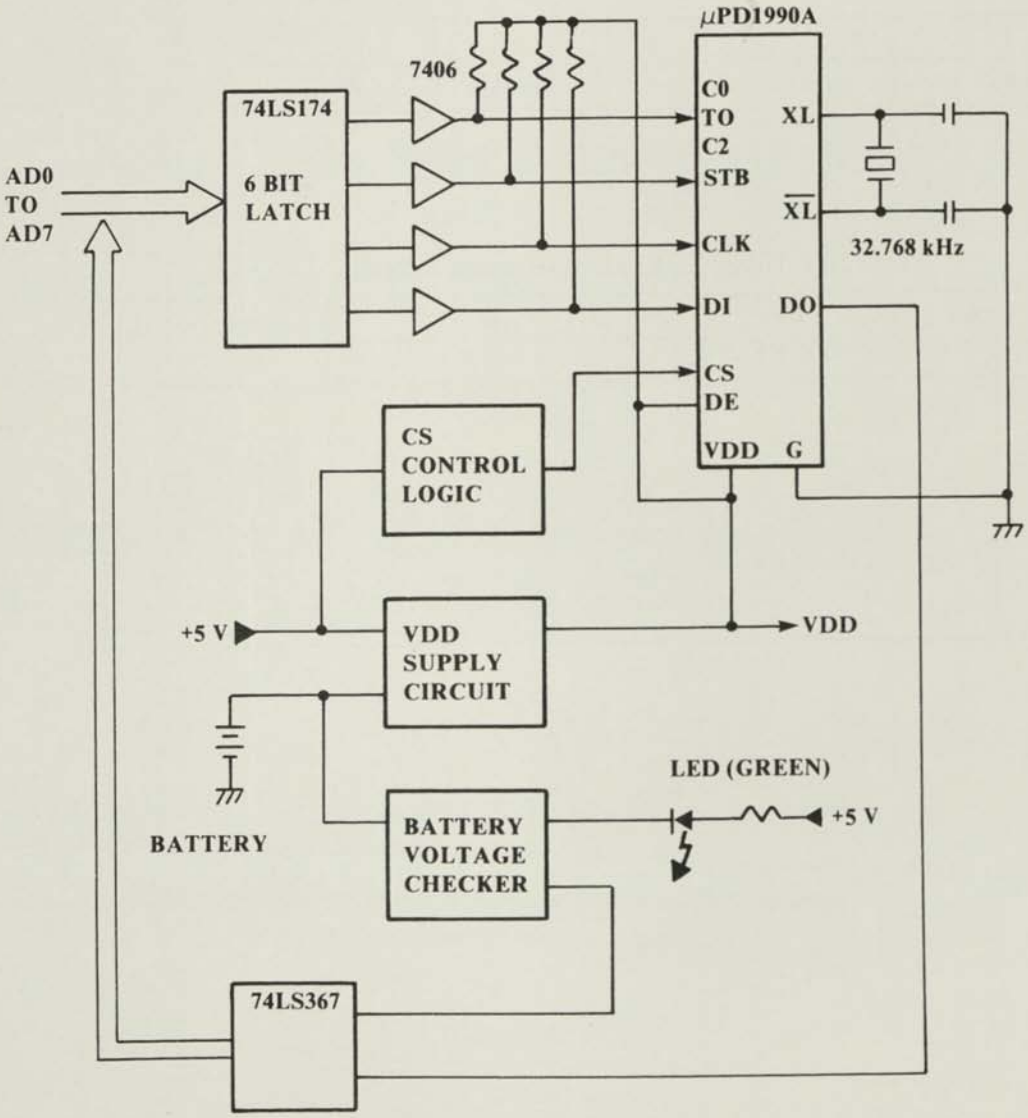


Figure 2-27 Clock/Calendar Block Diagram

2.9.2 Programming Considerations

Input and output of clock/calendar data is available on command as a 40-bit serial word having the following format.

MSB					LSB
4 bits	4 bits	8 bits	8 bits	8 bits	8 bits
month	day of wk.	date	hour	minute	second

The write/read instruction format is shown in Table 2-12 and Figure 2-28.

Table 2-12 Clock/Calendar Instruction Format

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS 7	6	5	4	3	2	1	0	DESCRIPTION
Set Register	W	58	0	0	DI	CLK	STB	C2	C1	C0	See Figure 2-28 (1)
Read Data	R	58	—	—	—	—	—	—	BATT	DO	See Figure 2-28 (2)

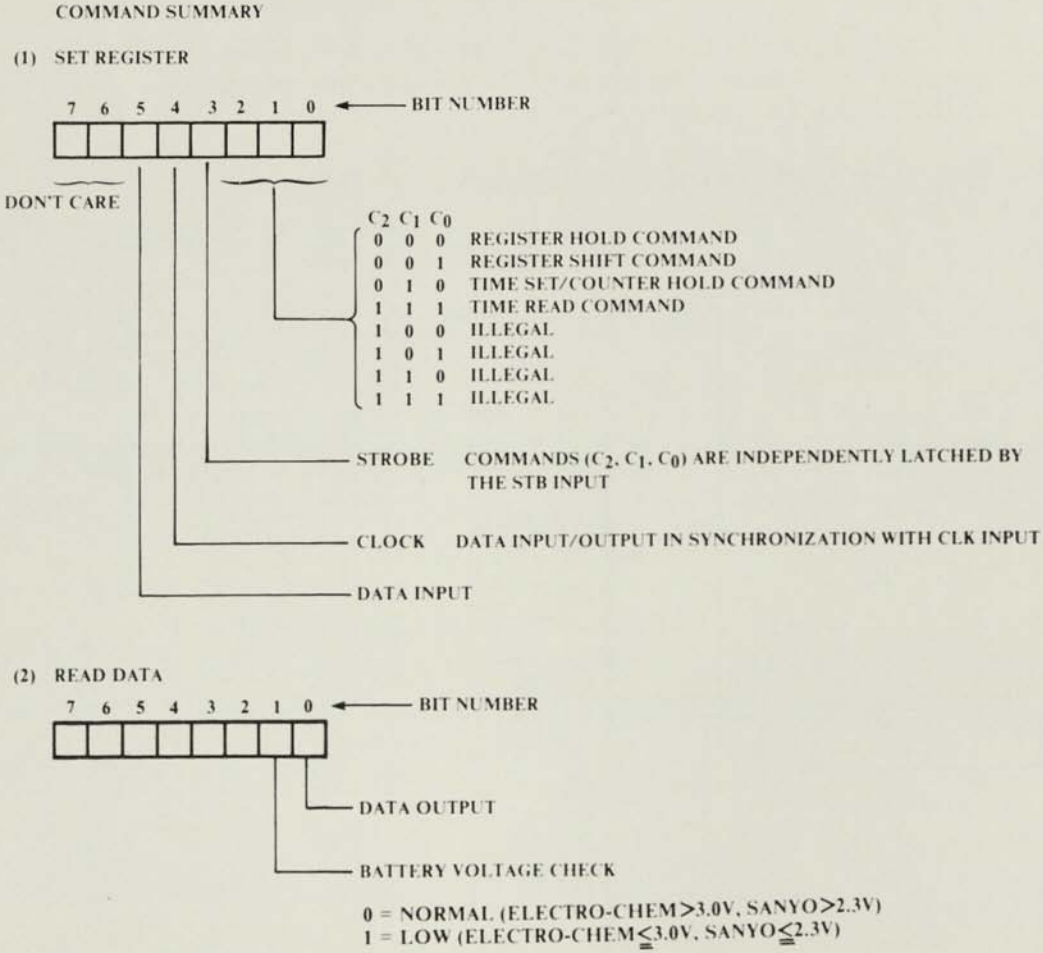


Figure 2-28 Clock/Calendar Format

2.10 JUMPER SETTINGS

The Processor PCB has four jumpers (TM1, TM2, TM3, and TM4). TM1 is not related to system functions, but to battery replacement. To prevent harm to the diode when replacing the battery, TM1 must be removed.

To adapt the APC interface for a Centronics-type or ODA printer, set TM2, TM3, and TM4 as instructed in Figure 2-29.

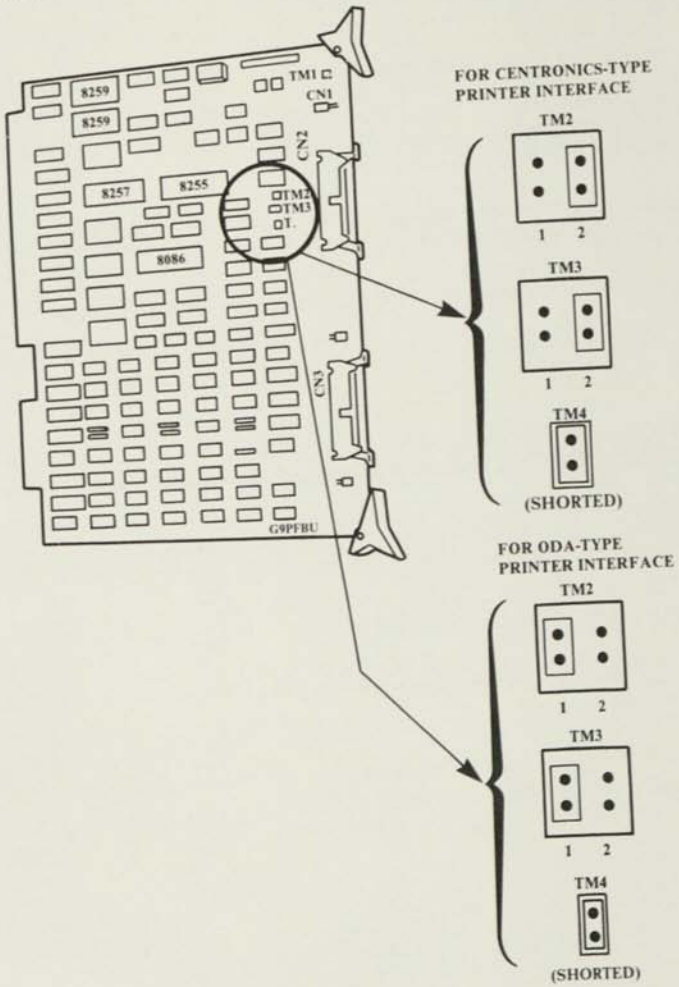
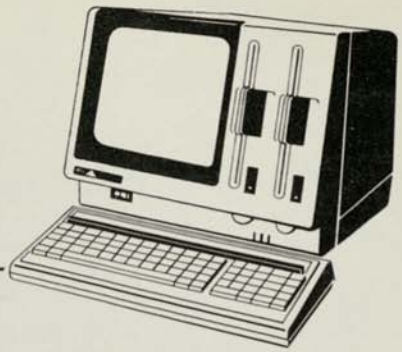


Figure 2-29 Processor PCB Jumper Settings

CONTROLLER PCB



Chapter 3

Controller PCB

The Controller PCB (G9PFCU) is the same size and has the same general physical arrangement as the Processor PCB. Like the Processor PCB, it fits into the Mother Board with a 100-pin card-edge socket. It is normally located in the first slot position (closest to the CRT).

Installed on the Controller PCB are five cable connectors: a communications interface connector, a CRT interface connector, an FDD interface connector, a speaker interface connector, and a volume interface connector (see Figure 3-1).

Figure 3-2 shows the functional relationships between the five principal components that occupy the Controller PCB.

- CRT Display control for the 12-inch monochrome or color display -- designed around the μPD7220 graphic display controller
- An 8-inch FDD control, that can read from and drive double-sided double-density flexible disks or single-sided single-density disks
- Serial I/O device control, supported by the NEC 8251A controller, converts serial data to parallel data and parallel data to serial data -- it can do so synchronously or asynchronously, using half- or full-duplex at various baud rates
- Sound control is supported by Large-Scale Integration (LSI) NEC μPD1771-006 and generates signal beeps and programmed melodies
- Arithmetic processing unit, an optional device, that provides high performance fixed-and-floating-point arithmetic operations and floating-point trigonometric operations.

3.1 MOTHER BOARD/CARD CAGE INTERFACE

For a description of this interface, see Section 2.1.

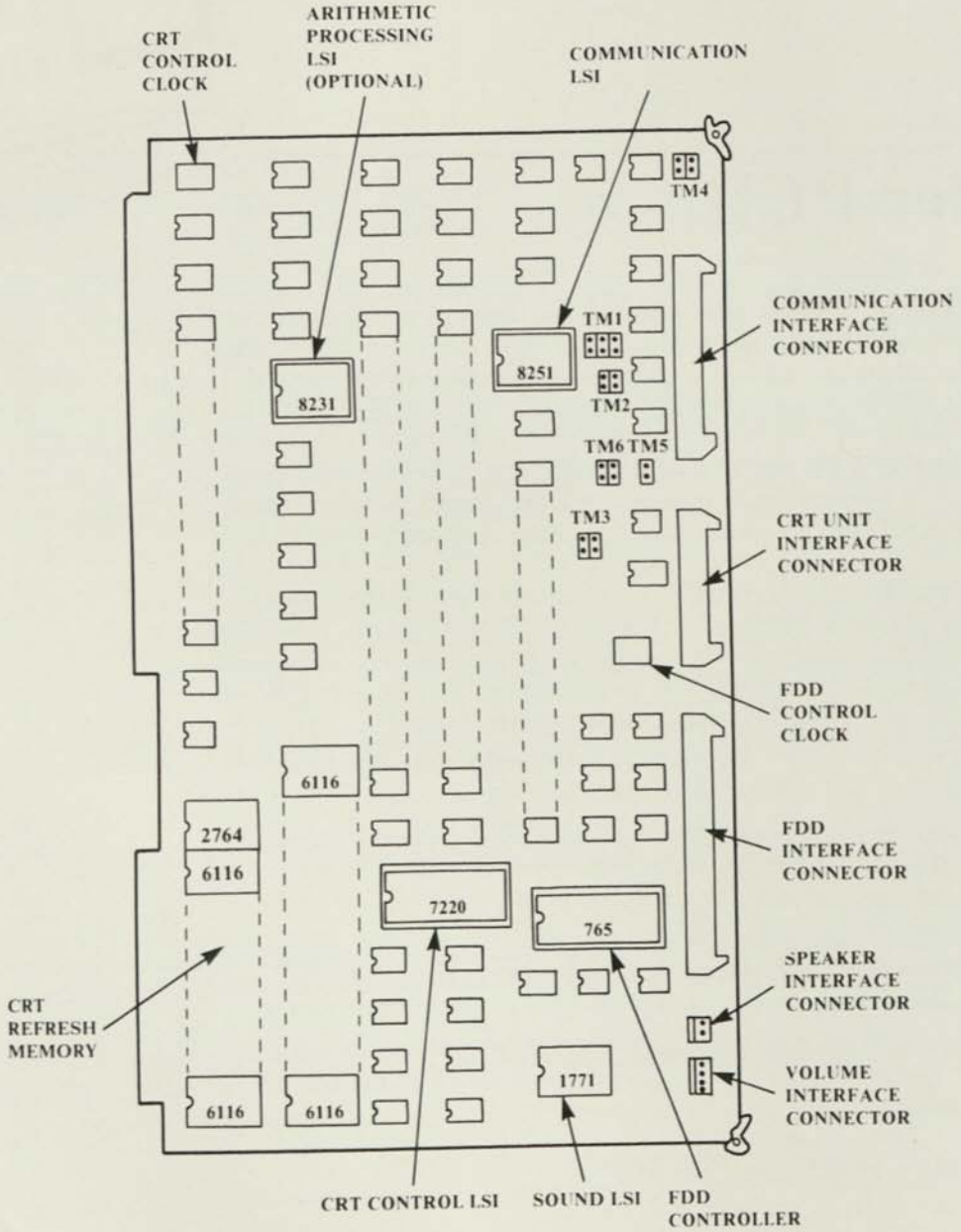


Figure 3-1 Controller PCB

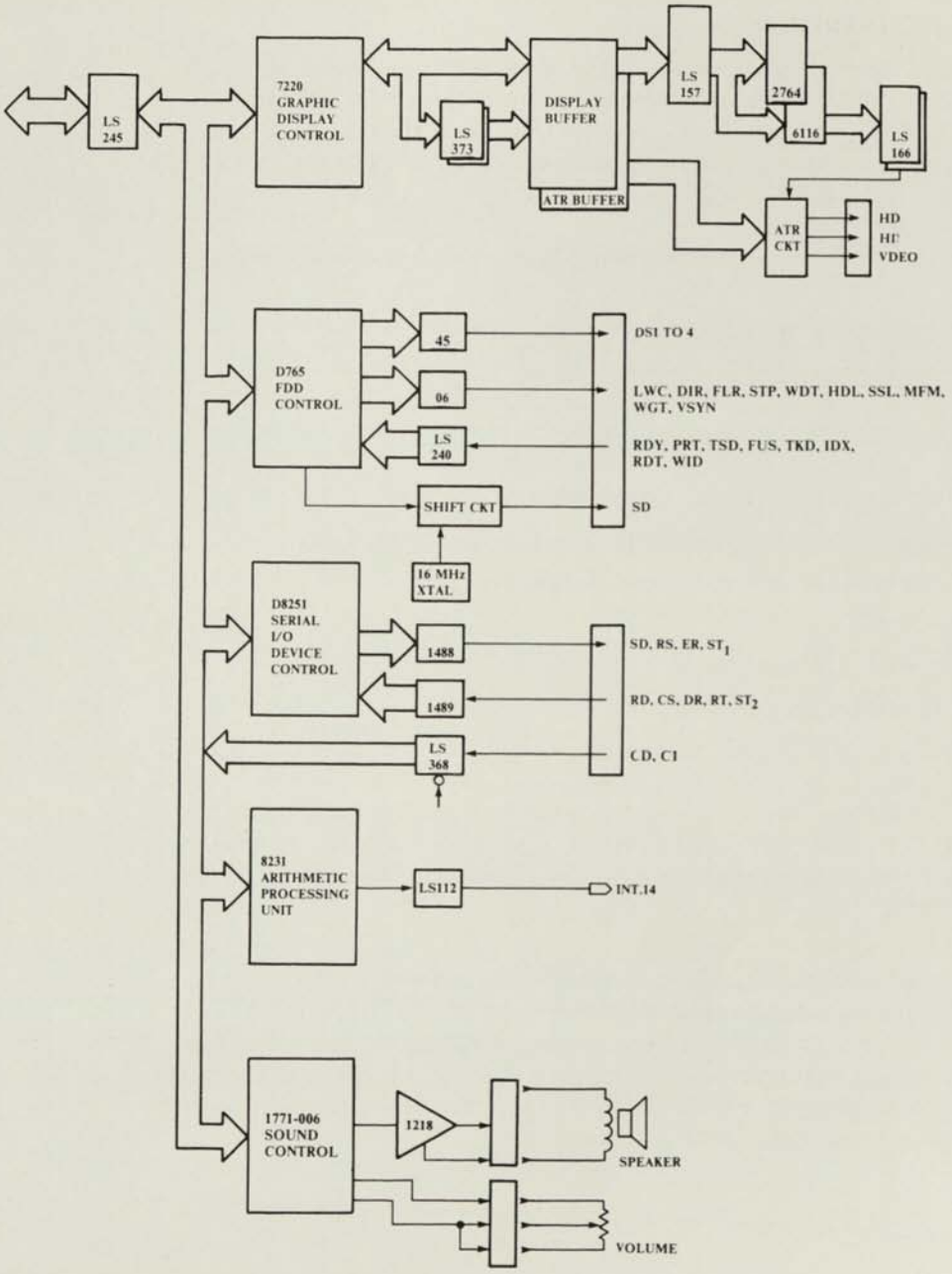


Figure 3-2 Controller PCB Block Diagram

3.2 CRT DISPLAY CONTROL

This adapter connects the microprocessor with a 12-inch monochrome or color display. At the heart of this computer-graphics system is the μPD7220 Graphic Display Controller (GDC), an intelligent LSI microprocessor that carries out the high-speed and repetitive duties required to generate the raster display and manage the display memory. The GDC duties include

- Generating the basic video raster timing (including sync and blanking signals)
- Video-display-memory modification and data moves
- Calculating display-memory addresses.

Some characteristics of the CRT-control design are

- Display buffer is independent of system memory
- An 80-character by 25-line screen (2000 characters)
- A 26th line reserved for system status information
- Direct drive output
- An 8-dot by 19-dot character box
- A 7-dot by 11-dot character
- 8-dot by 16-dot special programmable characters.

A character generator supplies the video process logic with the information necessary for displaying the characters. Additionally, a special-character generator contains the fonts for user-programmable characters; these are 8 by 16 characters in 8 by 19 character boxes.

In the display-control adapter is a character-code buffer memory that stores character codes or special-character codes (each character has 1 of 256 codes in RAM or 250 codes in ROM, of which 6 in ROM are not assigned) and an attribute-code buffer memory that stores character attributes (each character is associated with one or more of eight attributes). Figure 3-3 shows the functional relationships between the principal components of CRT control.

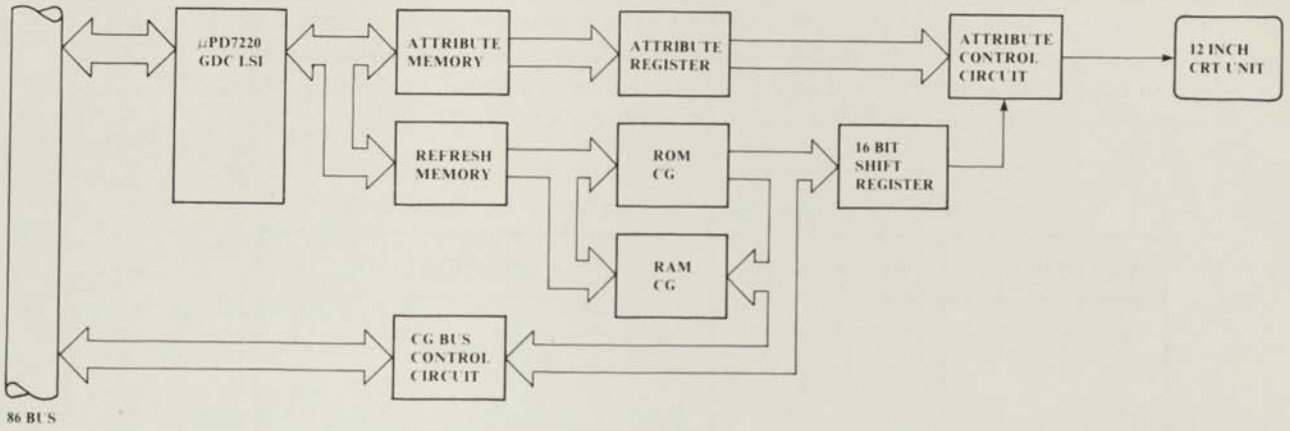


Figure 3-3 CRT Display Control Block Diagram

3.2.1 Display Buffer Memory

There are 2000 positions on the display screen, and each position is associated with 3 bytes (24 bits) of display buffer memory. Two of the three bytes of data indicate the character code or special-character code for an individual display position. A '1' in the character-set bit (Bit 7) indicates that the character comes from the special (or user programmed) character set (see Figure 3-4).

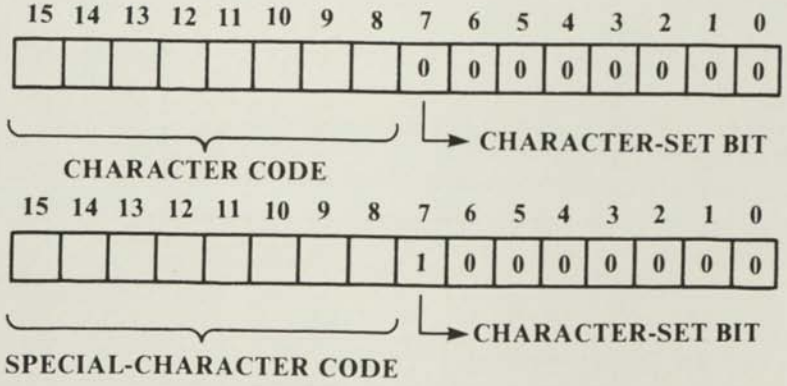


Figure 3-4 Character-Code Representation in the Character Code Buffer Memory

The character code (or special-character code) indicates to the character generator which of the 256 possible characters to display in a given display position. Also associated with each display position is an attribute code, which requires the third byte of data. The attribute code specifies the absence or presence of eight possible character supplements, which are shown in Table 3-1 and Figure 3-5.

Table 3-1 Attribute Description for Character Attribute Code

ATTRIBUTE	FUNCTION	COMMENT
GR	Green	Must always equal '1' with monochrome display.
BU	Blue	Character is blue.
R/H	Red/ highlight	Red color (color display)/high-lighted character (monochrome).
RV	Reverse video	Character and Field Video transposed.
BL	Blinking	
VB	Vertical bar	
OB	Over-bar	
UB	Under-bar	
GR, R/H, and BU all equal '0'	Nullify (secret)	No character displayed.

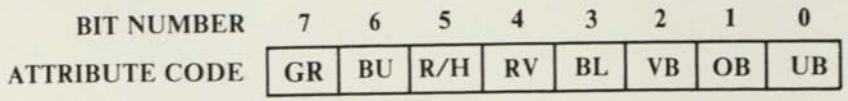


Figure 3-5 Bit Map for Character Attribute Code

Therefore, associated with each display position are a character code (or special-character code) and an attribute code. Both codes are stored in different physical areas of the display buffer memory, which is separate from main memory and accessible to only the GDC. This buffer has four 2K x 8-bit CMOS static RAMs for the character-code memory and two 2K x 8-bit CMOS static RAMs for the attribute-code memory.

The logical arrangement of this buffer is seen as a single 4K x 24-bit storage area, with associated character codes and attribute codes logically concatenated into single 24-bit words. Specifically, for any given display unit, the bit address of its character code is identical to that of its attribute code except for Bit 12. Bit 12 is '0' for the character-code address and '1' for the attribute-code address. For example, character-code address '0000' is associated with attribute-code address '1000' because their addresses are identical except for Bit 12. Figure 3-6 is a memory map that shows the organization of the display buffer memory. Notice that Bit 12 determines whether an address accesses a character code (Bit 12 = 0) or a character attribute code (Bit 12 = 1).

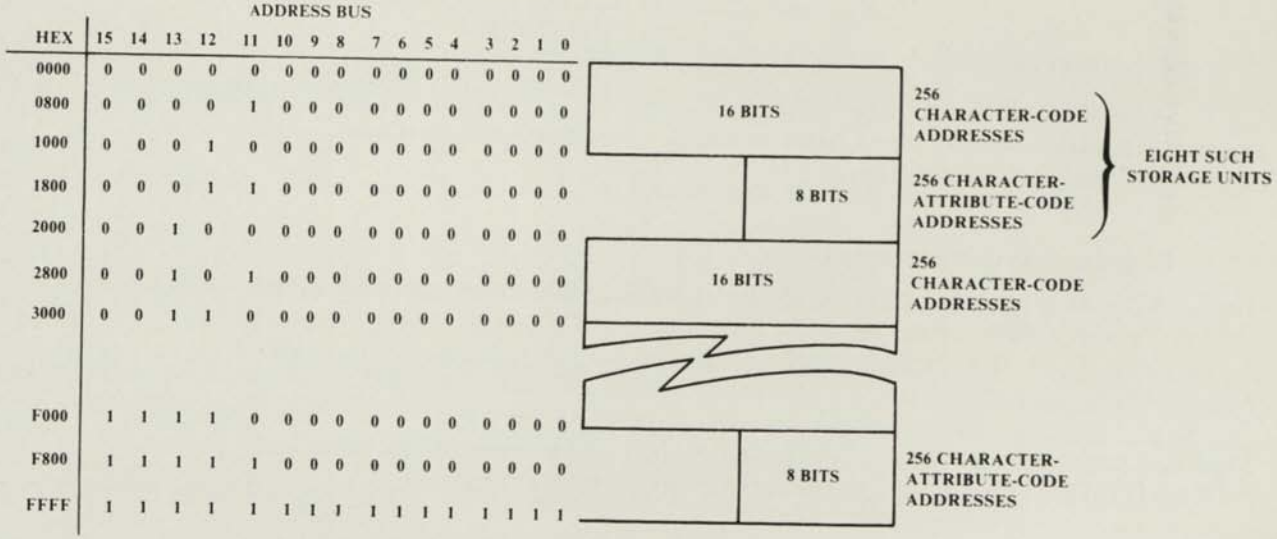


Figure 3-6 Display Buffer Memory Map

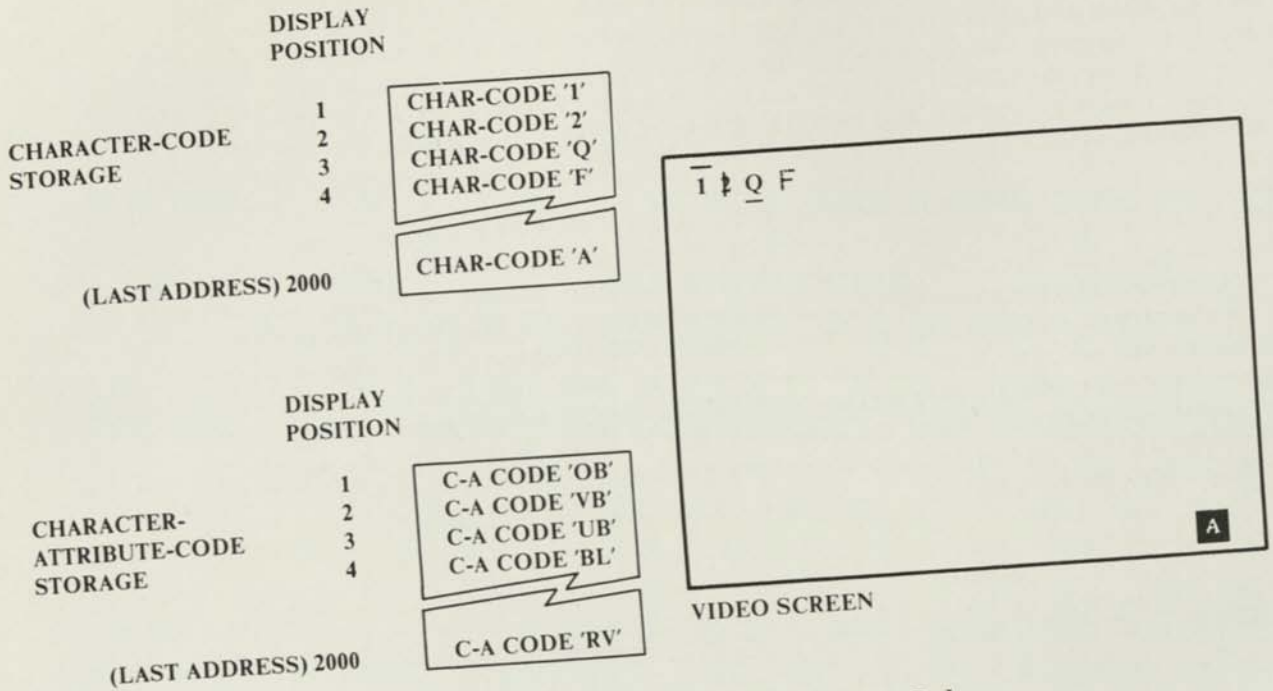


Figure 3-7 Relationship Between Character Code, Character-Attribute Code, Display Position, and Video Screen

3.2.2 Programming Considerations

The GDC has four registers, all of which can be accessed directly or indirectly by the 8086 processor: status register, First-In First-Out (FIFO), command register, and data register. The I/O addresses, functions, and bit maps are summarized in Table 3-2.

The status register is an 8-bit read-only register. Its I/O address is 80 (HEX). Using the 8086 I/O In command, the status register can be read at any time.

Figure 3-8 is a bit map of the GDC status register. Table 3-3 describes the contents of the status register.

Table 3-2 GDC I/O-Address and Bit Map

I/O ADDRESS	READ/ WRITE	BIT MAP 7	6	5	4	3	2	1	0	INSTRUCTION
40	Read	LP	HB	VS	DMA	DW	FE	FF	DR	Read Status Register
40	Write	P7	P6	P5	P4	P3	P2	P1	P0	Write Parameter Register
42	Read	D7	D6	D5	D4	D3	D2	D1	D0	Read Data Register
42	Write	C7	C6	C5	C4	C3	C2	C1	C0	Write Command Register
46	Write								CRT	Reset Interrupt Request

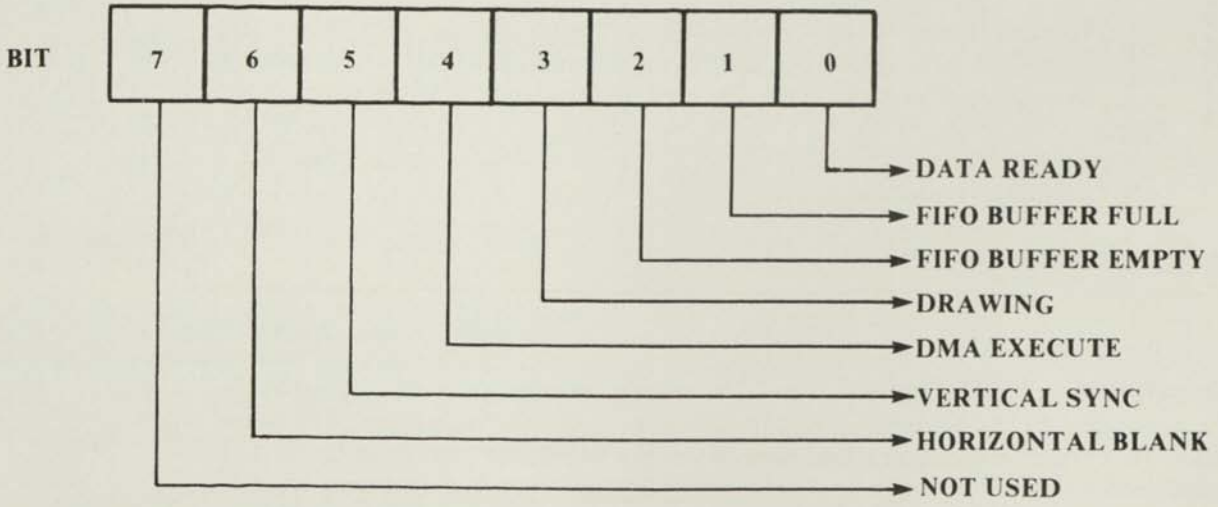


Figure 3-8 GDC Status Register Bit Map

Table 3-3 Contents of the GDC Status Register

BIT	DESCRIPTION
0	When this flag is a '1', it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a '0' while the data is transferred from the FIFO into the microprocessor interface data register.
1	A '1' at this flag indicates a full FIFO in the GDC. A '0' ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.
2	This bit and the FIFO-Full flag coordinate system microprocessor accesses with the GDC FIFO. When the bit is '1', the Empty flag ensures that the commands and parameters previously sent to the GDC have been processed.
3	While the GDC is drawing a graphics figure, this status bit is a '1'.
4	This bit is a '1' during DMA data transfers.
5	Vertical retrace sync occurs while this flag is a '1'. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.
6	A '1' value for this flag signifies that horizontal retrace blanking is currently underway.
7	Not used.

The FIFO is an internal buffer of the GDC that stores microprocessor commands. Access to the FIFO is coordinated through flags in the status register. The command processor fetches command bytes from the FIFO and interprets them. The command bytes are decoded and succeeding parameters are distributed to their proper destinations within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

The Parameter RAM stores parameters that are used repetitively during the display and drawing processes.

Table 3-4 defines the GDC abbreviations and symbols. Table 3-5 lists and describes the GDC commands. Table 3-6 lists the command constants. The APC uses the GDC in Character Mode only.

Table 3-4 GDC Symbols

SYMBOL	NAME	DESCRIPTION
A0 TO A15	Address 0 to Address 15	Controls display position of cursor.
BLD	Blinking Disable	Cursor blinks (BLD = 0) or does not blink (BLD = 1).
BL	Blinking Rate	Controls frequency of blinking.
CF1	Cursor Finish	Controls at which line the cursor finishes.
CHR	Character Mode	Character Mode (CHR) and Graphic Mode (G) define the display modes as follows: CHR G Mode 0 0 Character Mode 0 1 0 Character Mode 1 0 1 Not Used
CIR	Circle	Indicates that a circle is being drawn if CIR = 1.
CSR	Display Cursor	Controls presence (CSR = 1) or absence (CSR = 0) of the cursor.
CST	Cursor Start	Controls at which line the cursor starts.
C/R	Character Per Row	Defines horizontal display period.

Table 3-4 GDC Symbols (cont'd)

SYMBOL	NAME	DESCRIPTION
DE	Display Enable	Controls display start (DE = 1) or display stop (DE = 0).
DIR	Direction	Controls drawing direction.
D	Dynamic RAM	D = 1 implies display buffer consists of dynamic RAM; otherwise (D = 0) consists of static RAM.
F	Flashless Mode	Controls for flashless drawing (F = 1) or flashing drawing (F = 0).
G	Graphic Mode	Not used; see CHR.
HBP	Horizontal Back Porch	Defines the amount of left horizontal blanking time.
HFP	Horizontal Front Porch	Defines the amount of right horizontal blanking time.
HOS	Horizontal Sync	Horizontal sync occurs when HOS = 1.
I	Interlace	Display is interlaced (I = 1) or not interlaced (I = 0).
LIN	Line	LIN = 1 indicates that line is being drawn.
L/F	Lines Per Frame	Defines the number of lines in the vertical display period.
L/R	Lines Per Row	L/R defines the number of lines in each row.
M	Master	M = 0 indicates GDC is in multi (slave)-mode; M = 1 indicates single (master)-mode. The APC only uses master mode.

Table 3-4 GDC Symbols (cont'd)

SYMBOL	NAME	DESCRIPTION
MOD	Modify	Controls data that is accessed by CODEW command or CODER command.
RAD	RAM Address	RAD defines the RAM address that stores the scroll address.
REC	Rectangle	REC = 1 indicates that a rectangle is being drawn.
S	Shrink	Affects line center (S = 1).
SL0 to SL9	Scroll Line	Controls scroll-line count.
SLA	Slant	Controls slant of text or drawing.
VBP	Vertical Back Porch	Defines the amount of upper vertical blanking time.
VES	Vertical Sync	Vertical sync occurs when VES = 1.
VFP	Vertical Front Porch	Defines the amount of lower vertical blanking time.

Table 3-5 GDC Commands

COMMAND/ PARAMETER	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	SYNC SET								Sets parameters for synchronization of signals.
C	0	0	0	0	1	1	1	DE	
P1	0	0	CHR	F	I	D	G	S	
P2	← C/R →								
P3	← VSL →		← HS →						
P4	← HFP →						VSH →		
P5	0	0 ← HBP →							
P6	0	0 ← VFP →							
P7	← L/F →								
P8	← VBP →						L/F →		
	MASTER/SLAVE								Selects master or slave video synchronization mode.
C	0	1	1	0	1	1	1	M	
	RESET								Resets the GDC to its idle state and specifies video-display format.
C	0	0	0	0	0	0	0	0	
	DISP START								Starts the display scanning process.
C	0	1	1	0	1	0	1	1	
	DISP START								
C	0	0	0	0	1	1	0	1	
	DISP STOP								Stops the display scanning process.
C	0	0	0	0	1	1	0	0	
	ZOOM W								Specifies zoom coefficients for the display and graphics-character writing.
C	0	1	0	0	0	1	1	0	
P	← ZR →				← ZW →				
	CSR W								Sets the position of the cursor in display memory.
C	0	1	0	0	1	0	0	1	
P1	A7	A6	A5	A4	A3	A2	A1	A0	
P2	A15	A14	A13	A12	A11	A10	A9	A8	

Table 3-5 GDC Commands (cont'd)

COMMAND/ PARAMETER	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	CSR DISP								Specifies the height of the cursor and the character row.
C	0	1	0	0	1	0	1	1	
P1	CSR	0	0	←	L/R			→	
P2	←	BL	→	BD	←		CST	→	
P3	←		CFI		→	←	BL	→	
	SCROLL W								Specifies parameters for scroll: defines the starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
C	0	1	1	1	←	RA		→	
P1	A7	A6	A5	A4	A3	A2	A1	A0	
P2	A15	A14	A13	A12	A11	A10	A9	A8	
P3	SL3	SL2	SL1	SL0	0	0	0	0	
P4	0	IM	SL9	SL8	SL7	SL6	SL5	SL4	
P5	A7	A6	A5	A4	A3	A2	A1	A0	
P6	A15	A14	A13	A12	A11	A10	A9	A8	
P7	SL3	SL2	SL1	SL0	0	0	0	0	
P8	0	IM	SL9	SL8	SL7	SL6	SL5	SL4	
	CODEW								Writes the character-code data into the display memory.
C	0	0	1	0	0	0	←	MOD →	
P1	C7	C6	C5	C4	C3	C2	C1	C0	
P2	C15	C14	C13	C12	C11	C10	C9	C8	
	LOW BYTE CODEW								Writes the low-order byte of the character-code data into the display memory.
C	0	0	1	1	0	0	←	MOD →	
P1	C7	C6	C5	C4	C3	C2	C1	C0	
	HIGH BYTE CODEW								Writes the high-order byte of the character code data into the display memory.
C	0	0	1	1	1	0	←	MOD →	
P1	C15	C14	C13	C12	C11	C10	C9	C8	

Table 3-5 GDC Commands (cont'd)

COMMAND/ PARAMETER	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	PITCH W								Specifies the width of the X dimension of the display memory.
C	0	1	0	0	0	1	1	1	
P1	P7	P6	P5	P4	P3	P2	P1	P0	
	MASK W								Sets the mask register contents.
C	0	1	0	0	1	0	1	0	
P1	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
P2	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	
	VECT W								Vector parameters set: specifies the parameters for the drawing processor.
C	0	1	0	0	1	1	0	0	
P1	SL	R	C	T	L	←DIR→			
P2	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0	
P3		DGD	DC13	DC12	DC11	DC10	DC9	DC8	
P4	D7	D6	D5	D4	D3	D2	D1	D0	
P5			D13	D12	D11	D10	D9	D8	
P6	D27	D26	D25	D24	D23	D22	D21	D20	
P7			D213	D212	D211	D210	D29	D28	
P8	D17	D16	D15	D14	D13	D12	D11	D10	
P9			D113	D112	D111	D110	D19	D18	
P10	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	
P11			DM13	DM12	DM11	DM10	DM9	DM8	
	WORD CODER								Reads the character-code data from the display memory.
C	1	0	1	0	0	0	←MOD→		
	LOW BYTE CODER								Reads the low-order byte of the character-code data from the display memory.
C	1	0	1	1	0	0	←MOD→		

Table 3-5 GDC Commands (cont'd)

COMMAND/ PARAMETER	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
			HIGH BYTE CODER						
C	1	0	1	1	1	0	←MOD→		Reads the high-order byte of the character-code data from the display memory.
			CSR R						
C	1	1	1	0	0	0	0	0	Reads the display position of the cursor.
			WORD DREQW						
C	0	0	1	0	0	1	←MOD→		Requests a DMA write transfer for the entire word.
			LOW BYTE DREQW						
C	0	0	1	1	0	1	←MOD→		Requests a DMA write transfer for the low-order byte only.
			HIGH BYTE DREQW						
C	0	0	1	1	1	1	←MOD→		Requests a DMA write transfer for the high-order byte only.
			WORD DREQR						
C	1	0	1	0	0	1	←MOD→		Requests a DMA read transfer for the entire word.
			LOW BYTE DREQR						
C	1	0	1	1	0	1	←MOD→		Requests a DMA read transfer for the low-order byte only.
			HIGH BYTE DREQR						
C	1	0	1	1	1	1	←MOD→		Requests a DMA read transfer for the high-order byte only.

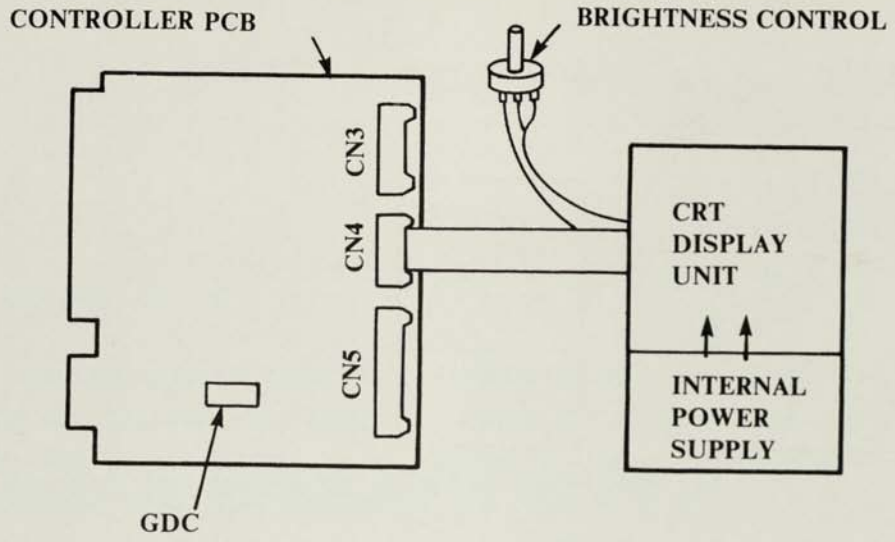
Table 3-6 GDC Command Constants

COMMAND/ PARAMETER	SETTING VALUE (HEX)	REMARKS
C	SYNCSET	Character display mode '0': no interlace, flashless drawing, static RAM, 80 characters per row
P1	10	
P2	4E	
P3	52	
P4	0E	
P5	06	
P6	13	
P7	EE	
P8	45	
C	Master/slave	Master versus slave video synchronization
C	ZOOM W	Zooming disabled
P1	00	
C	CSR DISP	Blinking block cursor
P1	12	
P2	C1	
P3	8B	
C	PITCH W	80 characters per row
P1	50	
C	MASK W	
P1	FF	
P2	FF	

3.3 CRT DISPLAY UNIT

The CRT Display unit consists of a chassis-mounted circuit, a 12-inch monochrome or color CRT Display, Controller PCB, and internal power unit.

The monochrome or color display units connect to the Controller PCB (see Figures 3-9 and 3-10).



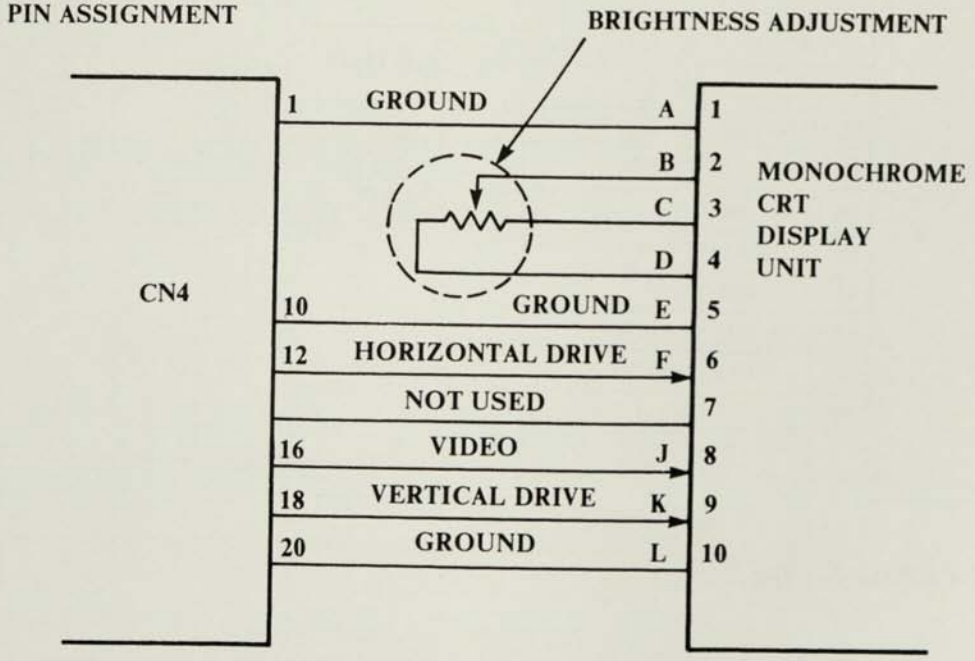
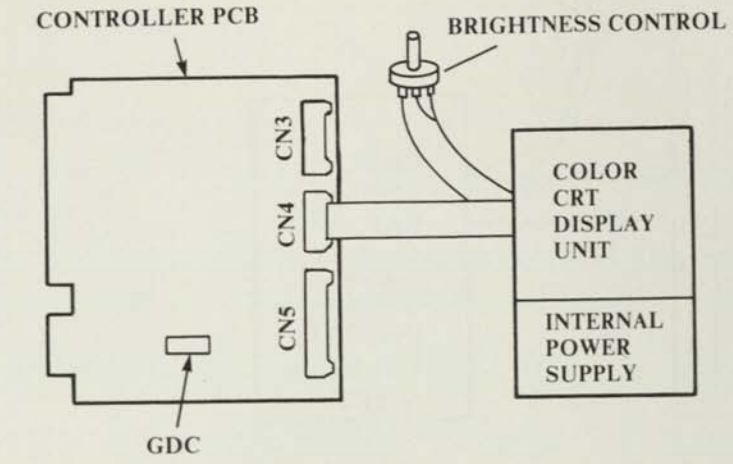


Figure 3-9 Monochrome-CRT Display Interface



PIN ASSIGNMENT

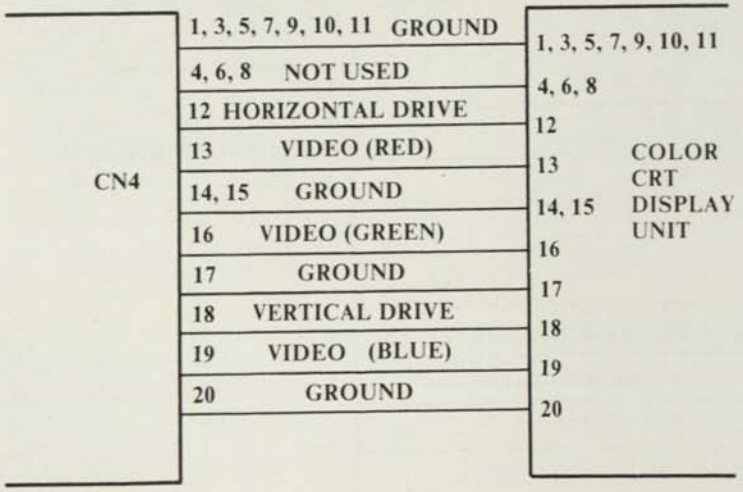


Figure 3-10 Color-CRT Display Interface

Another internal cable, the power supply cable, carries 115 Vac power from the system power supply to the internal power supply of the CRT Display. This internal power unit provides the CRT Display with +12 Vdc.

The following items are the principal operating characteristics of the monochrome CRT Display.

- *Display control*. A brightness control knob is available to the operator on the front of the unit.
- *Monochrome Display screen*. The Monochrome CRT Display employs a yellow-green, long-persistence phosphor (P39) and has a reduced-glare surface. The display format is 80 characters wide by 25 lines high plus one status line. Each standard character consists of a 7 (width)-by-11 (height) dot matrix. Special characters can be as large as 8-by-16 dots. The screen is composed of 475 lines of vertical resolution.
- *Color Display screen*. The Color Display has an 8-color, high-resolution, reduced-glare screen.
- *Horizontal drive*. This positive level, TTL compatible frequency is 22.727 kHz. The minimum pulse width is 3 μs.
- *Vertical drive*. This frequency is 41.5 Hz and is negative level/TTL compatible.
- *Video signal*. The video signal is positive level with a 50-ns minimum pulse width.
- *CRT Display interface*.

3.4 FLEXIBLE DISK DRIVE CONTROLLER

The APC has space and power for two 8-inch FDDs. The drives are soft-sectored and two-sided, with 77 cylinders (0 to 76). They use Modified Frequency Modulation (MFM) coded in 256 byte sectors (except index track), giving an unformatted capacity of about 1.2 MB per drive. They have a track access time of 5 ms.

The 8-inch Flexible Disk Drive Controller (FDC) on the Controller PCB attaches to the FDD with an internal flat cable, which is daisy-chained if there are two FDDs.

The FDC is designed for double-density MFM-coded drives, uses write precompensation, and employs the NEC μPD765. The FDC uses DMA for record-data transfers. An interrupt level indicates completed operation or a status condition that requires processor attention.

Figure 3-11 is a functional block diagram of the FDC. This controller contains two registers that can be accessed by the main processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC and can be accessed at any time. This register facilitates the transfer of data between the processor and FDC. It can be read only. Table 3-7 summarizes the bit functions of the main status register.

The 8-bit data register (which actually consists of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are written into the data register to program the FDC and are read out of it to obtain results after a command.

The FDC can perform 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command can also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the FDC and the processor, each command can be considered in three phases.

- *Command Phase* — The FDC receives all information required to perform a particular operation from the processor.
- *Execution Phase* — The FDC performs the operation.
- *Result Phase* — Status and other housekeeping information are made available to the processor.

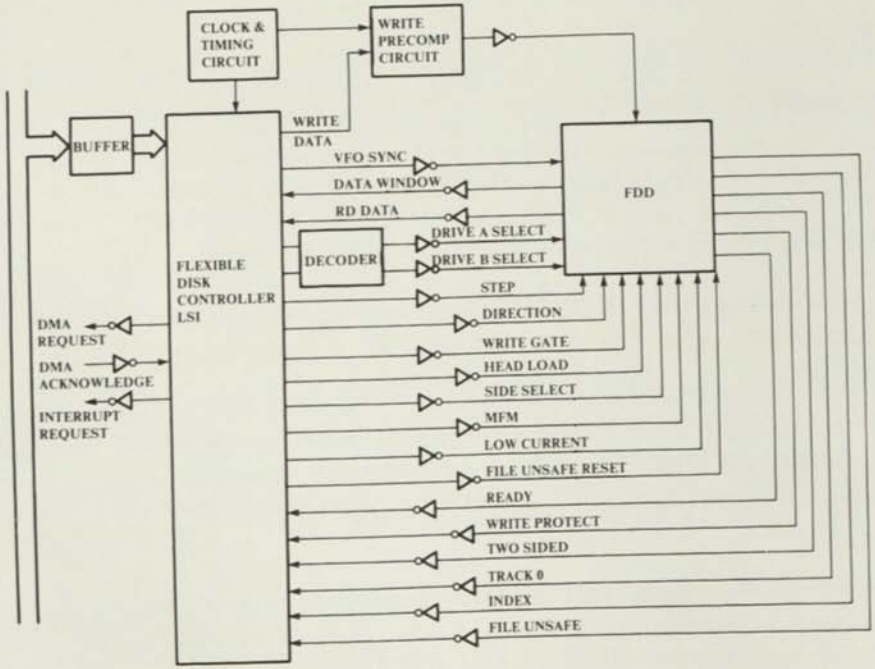


Figure 3-11 FDC Block Diagram

Table 3-7 Bit Description of the FDC Main Status Register

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB0	FDD A Busy	DAB	FDD A is in the Seek Mode.
DB1	FDD B Busy	DBB	FDD B is in the Seek Mode.
DB2	FDD C Busy	DCB	Not used.
DB3	FDD D Busy	DDB	Not used.
DB4	FDC Busy	CB	A read or write command is in process.
DB5	Non-DMA Mode	NDM	The FDC is in the Non-DMA Mode.
DB6	Data Input/ Output	DIO	Indicates direction of data transfer between the FDC and the processor. DIO = '1' indicates transfer is from FDC data register to the processor; DIO = '0' indicates transfer is from processor to FDC data register.
DB7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

Figure 3-12 is a timing diagram that defines the timing of this three-phase command process.

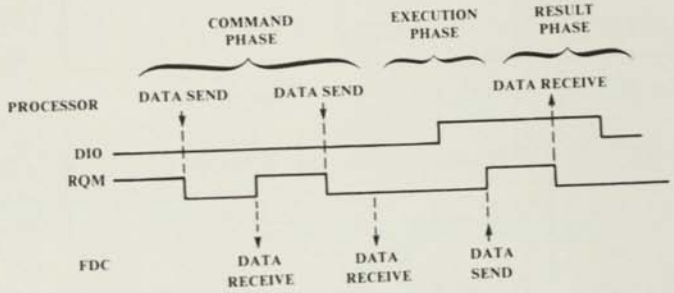


Figure 3-12 FDC Timing Diagram

3.4.1 Programming Considerations

Table 3-8 defines the symbols used in the FDC command summary given in Table 3-9. Tables 3-10, 3-11, 3-12 and 3-13 define the bit functions of the command status registers. Table 3-14 lists the I/O addresses and functions of the FDC registers.

Table 3-8 FDC Symbols

SYMBOL	NAME	DESCRIPTION
A0	Address Line 0	Controls the selection of the Main Status Register (A0=0) or Data Register (A0=1).
C	Cylinder Number	Specifies the selected cylinder number.
D	Data	Specifies the data pattern that is going to be written into a sector.
D7 to D0	Data Bus	8-bit Data Bus, where D7 is the most significant bit, and D0 is the least significant bit.
DTL	Data Length	When N is defined as 00, DTL is the data length that users are going to read out or write into the sector.
EOT	End of Track	Indicates the final sector number on a cylinder.

Table 3-8 FDC Symbols (cont'd)

SYMBOL	NAME	DESCRIPTION
GPL	Gap Length	Specifies length of Gap 3 (spacing between sectors excluding VCO Sync. Field).
H	Head Address	Specifies the head number 0 or 1, as specified in the ID field.
HD	Head	Specifies the selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	Indicates the head load time in the FDD (2 to 256 ms in 2-ms increments).
HUT	Head Unload Time	Indicates the head unload time after a read or write operation has occurred (0 to 240 ms in 16-ms increments).
MF	FM or MFM Mode	If MF is Low, FM Mode is selected; if High, MFM Mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is High, a multitrack operation is to be performed. (A cylinder under both HD0 and HD1 is read or written.)
N	Number	Specifies the number of data bytes written in a sector.
NCN	New Cylinder Number	New cylinder number, which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	Signals that operation is Non-DMA Mode.
PCN	Present Cylinder Number	Designates cylinder number at the completion of Sense Interrupt Status Command, indicating the position of the head at present time.

Table 3-8 FDC Symbols (cont'd)

SYMBOL	NAME	DESCRIPTION
R	Record	Specifies the sector number, which is read or written.
R/W	Read/Write	Specifies the Read (R) or Write (W) signal.
SC	Sector	Indicates the number of sectors per cylinder.
SK	Skip	Specifies the Skip Deleted Data Address Mark.
SRT	Step Rate Time	Specifies the Stepping Rate for the FDD (1 to 16 ms in 1-ms increments).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	Specifies which of four registers will store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A0 = 0). ST 0 to 3 can be read only after a command has been executed. They contain information relevant to that particular command.
STP	Scan Test	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA). If STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	Specifies the selected drive number.

Table 3-9 FDC Commands

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		READ DATA								
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system
Result	R					ST0				Status information after Command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information after Command execution
	R					H				
	R					R				
	R					N				
		READ DELETED DATA								
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				

X = Don't care.

Table 3-9 FDC Commands (cont'd)

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					WRITE DATA					
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information to command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the main system and FDD
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				
					WRITE DELETED DATA					
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between FDD and main system
Result	R					ST0				Status ID information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				

X = Don't care.

Table 3-9 FDC Commands (cont'd)

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
					READ A TRACK					
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system. FDD reads all of cylinders contents from index hole to EOT.
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				
					READ ID					
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the cylinder is stored in data register
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information during execution phase
	R					H				
	R					R				
	R					N				

X = Don't care.

Table 3-9 FDC Commands (cont'd)

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		FORMAT TRACK								
Command	W	0	MF	0	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					N				Bytes/Sector
	W					SC				Sector/Track
	W					GPL				Gap 3
	W					D				filler byte
Execution										FDC formats an entire cylinder
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				In this case, the ID information has no meaning
	R					H				
	R					R				
	R					N				
		SCAN EQUAL								
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to command execution
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					STP				
Execution										Data compared between the FDD and main system
Result	R					ST0				Status information after command execution
	R					ST1				
	R					ST2				
	R					C				Sector ID information
	R					H				
	R					R				
	R					N				

X = Don't care.

Table 3-9 FDC Commands (cont'd)

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		SCAN LOW OR EQUAL								
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Section ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
		SCAN HIGH OR EQUAL								
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

X = Don't care.

Table 3-9 FDC Commands (cont'd)

PHASE	READ/ WRITE	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
		RECALIBRATE								
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution No Result Phase										Head retracted to track 0
		SENSE INTERRUPT STATUS								
Command	W	0	0	0	0	1	0	0	0	Command Code
Result	R	ST0								Status information about the FDD at the end of seek operation
	R	PCN								
		SPECIFY								
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	← SRT →						← HUT →		
	W	← HLT →							ND	
No Result Phase										
		SENSE DRIVE STATUS								
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST3								Status information about FDD
		SEEK								
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	← NCN →								
Execution										Head is positioned over proper cylinder on diskette
No Result Phase										
		INVALID								
Command	W	Invalid Codes								Invalid command codes (NoOp - FDC goes into standby state)
Result	R	ST0								ST0 = 80

X = Don't care.

Table 3-10 FDC Status Register 0

NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7 D6	Interrupt Code	IC	D7 = 0 and D6 = 0 Normal termination (NT) of command. Command was completed and properly executed. D7 = 0 and D6 = 1 Abnormal termination (AT) of command. Execution of command was started, but not successfully completed. D7 = 1 and D6 = 0 Invalid command issue (IC). Command which was issued was never started. D7 = 1 and D6 = 1 Abnormal termination because during command execution the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the Seek command, this flag is set to 1 (High).
D4	Equipment Check	EC	If a fault signal is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command), then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at interrupt
D1 D0	Unit Select 1 Unit Select 0	US 1 US 0	These flags are used to indicate a Drive Unit number at interrupt.

Table 3-11 FDC Status Register 1

NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	—	—	Not used. This bit is always 0 (Low).
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D4	Over Run	OR	If the FDC is not serviced by the main systems during data transfers within a certain time interval, this flag is set.
D3	—	—	Not used. This bit is always 0 (Low).
D2	No Data	ND	During execution of a Read Data, Write Deleted Data, or Scan command, if the FDC cannot find the sector specified in the ID register, this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During the execution of the Read-a-Cylinder command, if the starting sector cannot be found, then this flag is set.
D1	Not Writable	NW	During Execution of a Write Data, Write Deleted Data, or Format a Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark, this flag is set. Also at the same time, the MD Flag of Status Register 2 is set.

Table 3-12 FDC Status Register 2

NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7	—	—	Not Used. This bit is always 0 (Low).
D6	Control Mark	CM	During execution of the Read Data or Scan command, if the FDC encounters a sector that contains a Deleted Data Address Mark, this flag is set.
D5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data, then this flag is set.
D4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium are different from that stored in the ID Register, this flag is set.
D3	Scan Equal Hit	SH	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During execution of the Scan command, if the FDC cannot find a sector on the cylinder that meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related with the ND bit, and when the contents of C on the medium are different from that stored in the ID Register and the content of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

Table 3-13 FDC Status Register 3

NUMBER	BIT NAME	SYMBOL	DESCRIPTION
D7	Fault	FT	Indicates the status of the Fault signal from the FDD.
D6	Write Protected	WP	Indicates the status of the Write Protected signal from the FDD.
D5	Ready	RY	Indicates the status of the Ready signal from the FDD.
D4	Track 0	T0	Indicates the status of the Track 0 signal from the FDD.
D3	Two Side	TS	Indicates the status of the Two Side signal from the FDD.
D2	Head Address	HD	Indicates the status of Side Select signal to the FDD.
D1	Unit Select 1	US 1	Indicates the status of the Unit Select 1 signal to the FDD.
D0	Unit Select 0	US 0	Indicates the status of the Unit Select 0 signal to the FDD.

Table 3-14 FDC Register I/O Addresses and Functions

I/O ADDRESS	READ/ WRITE	FUNCTION
50	Read	Read-Status Register
52	Read	Read-Data Register
52	Write	Write-Data Register

3.4.2 Drive A and B Interface

All signals are TTL compatible, and all outputs are driven by open-collector gates. The drives provide termination networks; each input is terminated with a 150-ohm resistor. The output signals are described in Table 3-15, the input signals are described in Table 3-16.

Table 3-15 Output Signals

SIGNAL	DRIVER	DESCRIPTION
Drive Select A and B	7445	When the line associated with a drive is not active, these two lines are used by Drives A and B to degate all drivers to the adapter and all receivers from the attachment.
Step	7406	The selected drive moves the read/write head one cylinder in or out (according to the direction-line signal) for each pulse present on this line.
Direction	7406	For each recognized pulse of the step line, the read/write head moves one cylinder toward the spindle if this line is active, and away from the spindle if this line is inactive.
Write Data	7406	For each inactive-to-active transition of this line (while Write Enable is active), the selected drive causes a flux change to be stored on the disk.
Write Gate	7406	Unless this line is active, the drive disables the write current for the head.
Head Load	7406	While this line is active, the drive loads the read/write head.
Side Select	7406	The read/write head selects which side of the flexible disk to read/write. 0 = head 0 1 = head 1
M/FM	7406	This signal selects the Code-Reading Mode, FM or MFM. 0 = FM Mode 1 = MFM Mode

Table 3-15 Output Signals (cont'd)

SIGNAL	DRIVER	DESCRIPTION
VFO Sync	7406	This signal enables or disables the VFO Circuit Mode. 0 = enable 1 = disable
Low Current	7406	This line relays head-position information to the drive.
File-Unsafe Reset	7406	This line resets a drive if it is in fault status.

Table 3-16 Input Signals

SIGNAL	DESCRIPTION
Index	The selected drive supplies one pulse per disk revolution on this line.
Write Protect	The selected drive activates this line when a write protected diskette is mounted in the drive.
Track 0	The selected drive activates this line when the read/write head is over Track 0.
Read Data	The selected drive supplies a pulse on this line for each flux change encountered on the disk; it relays data from the flexible disk.
Ready	This line becomes active when the selected drive is ready.
Dual Side	When a dual-sided disk is mounted on the drive, this line becomes active.
File Unsafe	If the drive is in a fault state, the selected drive activates this line.
Data Window	The selected drive combines read data with clock data, which allows the FDC to discriminate data from read data.

3.5 FDD UNIT

The 8-inch FDD is a two-sided, double-density unit that can read from and write to one-sided and single-density flexible disks as well. The FDD can read and record digital data using either FM or MFM. Signal transfer is in the VFO Mode.

The FDD unit attaches to the FDC with the signal cable and the flexible disk interface connector, which is located on the Controller PCB (see Figure 3-1). A power cable connects each FDD unit to the APC power supply.

To enable disk reading, insert a disk, and close the front latch; this causes the drive hub to clamp the disk and turn it at 360 rpm. When an index sensor detects the index hole, it activates a signal. The stepper motor positions the read/write heads over the desired tracks for reading.

3.5.1 Specifications

The FDD specifications are listed in Table 3-17.

Table 3-17 FDD Specifications

CHARACTERISTIC	SPECIFICATION
Transfer Rate	
FM	31.25 KB/sec
MFM	62.5 KB/sec
Disk Speed	360 rpm
Seek Time	5 ms track to track
Seek Settling Time	15 ms
Head-Load Time	50 ms
Tracks Per Inch	48
Maximum Bits Per Inch	
FM	3.408
MFM	6.816
Recording Mode	FM or MFM

Table 3-17 FDD Specifications (cont'd)

CHARACTERISTIC	SPECIFICATION
Dimensions Height Width Depth Weight	 8.55 in. (217.2 mm) 2.28 in. (58.0 mm) 12.73 in. (323.0 mm) 7.7 lb (3.5 lb)
Operating Temperature Range	50 to 113° F (10 to 45° C)
Relative Humidity Tolerance Range	20 to 80%
Power	+24 Vdc ±10% 0.75 A (starting) 0.90 A (average) +5 Vdc ±5% 0.8 A -5 Vdc ±5% 0.07A
Power Consumption	28 W (maximum)
Error Rate Recoverable Non-Recoverable Seeks	 1 per 10^9 1 per 10^{12} 1 per 10^6

3.5.2 Interface

Figure 3-13 shows the signal connector interface and pin assignments; Figure 3-14 illustrates the power connector interface and pin assignments.

3.5.3 Terminations and Jumper Settings

The location and installation of the termination resistor modules are shown in Figure 3-15, and the jumper location and jumper setting are shown in Figure 3-16.

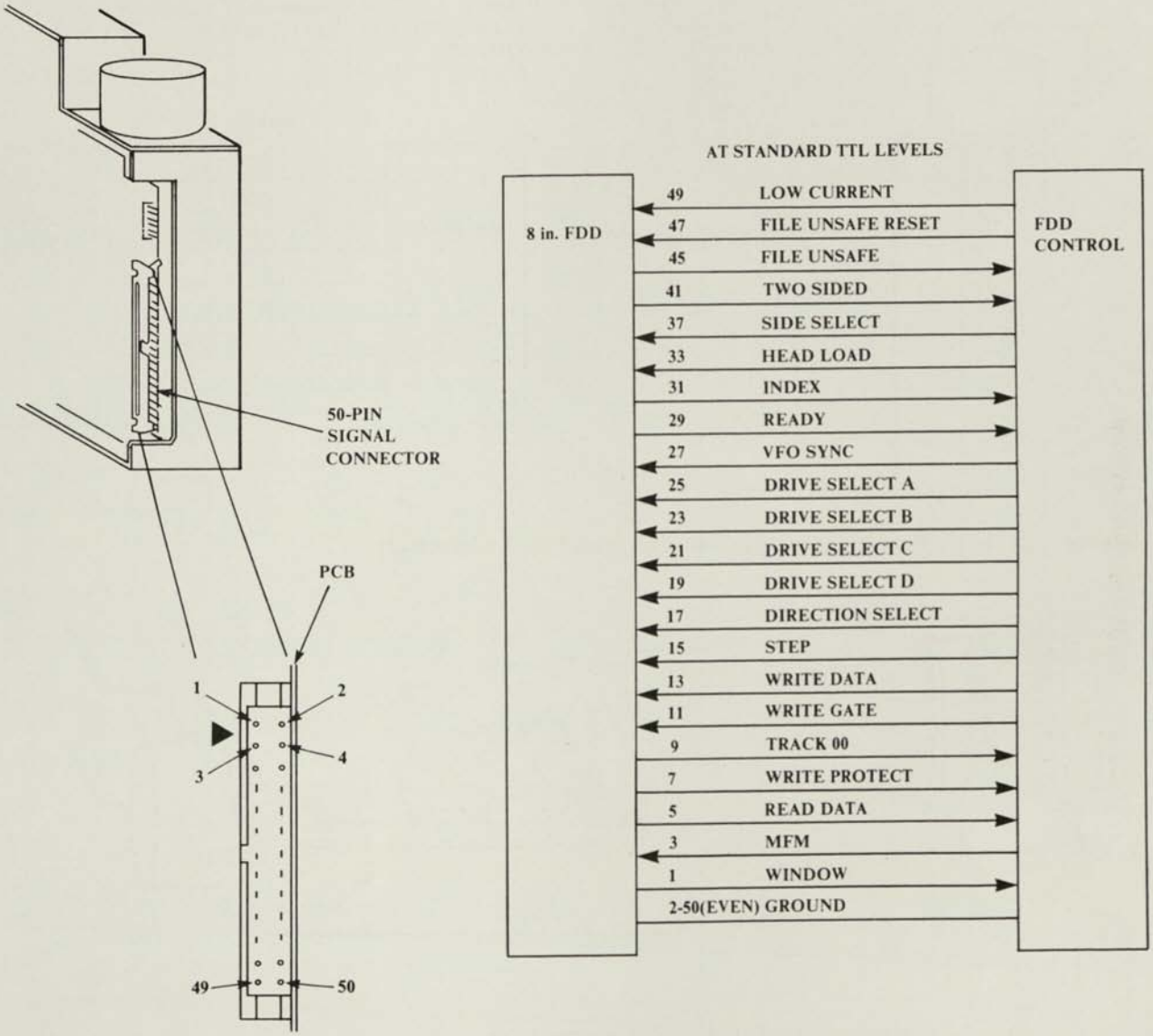


Figure 3-13 FDD Signal Connector Interface and Pin Assignments

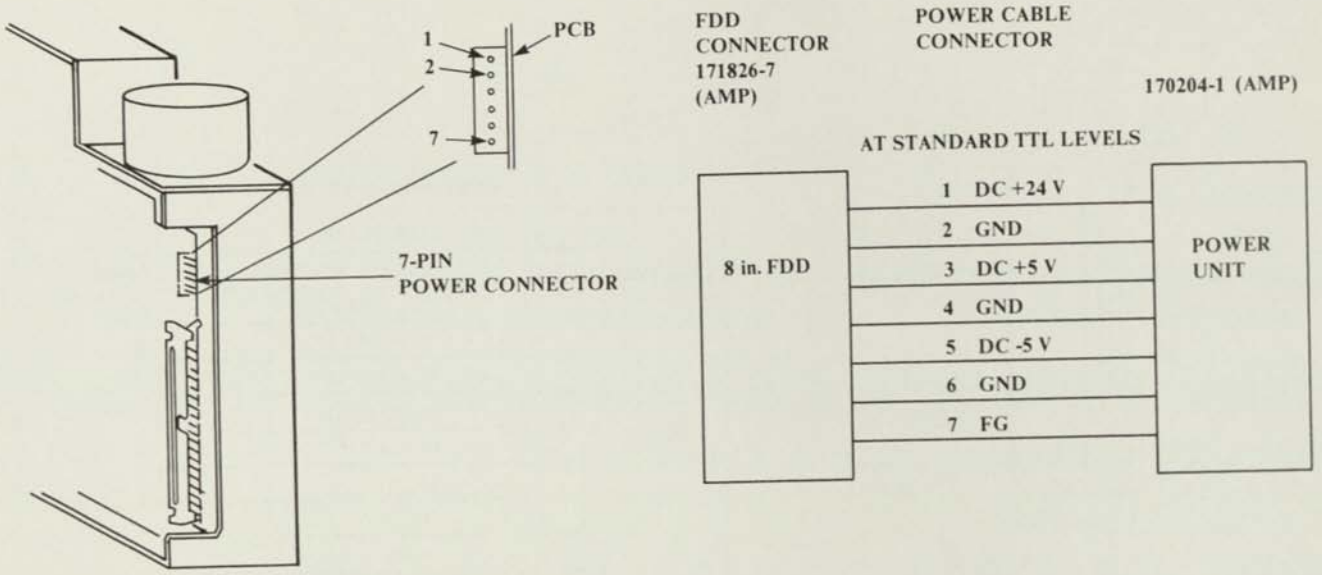


Figure 3-14 FDD Power Connector Interface and Pin Assignments

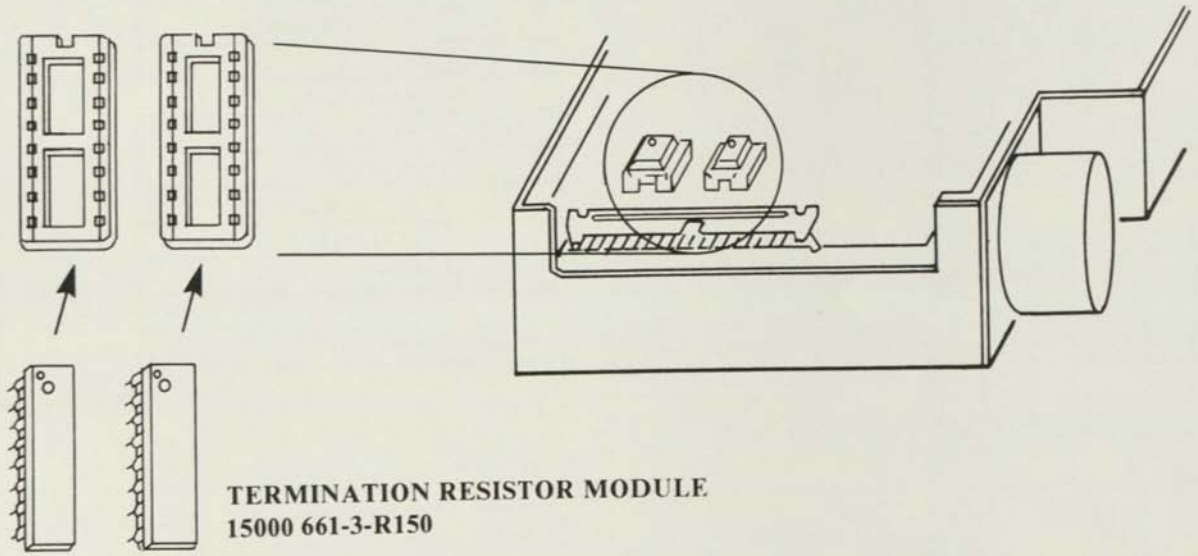


Figure 3-15 FDD Termination Resistor Modules, Location and Installation

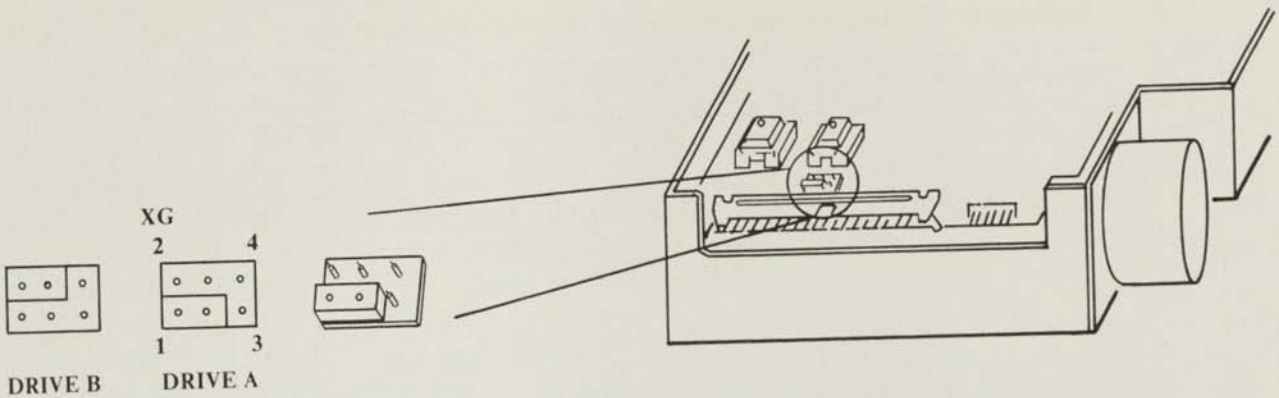


Figure 3-16 FDD Jumper, Location and Proper Setting

3.6 SERIAL I/O COMMUNICATIONS CONTROLLER

Supported by the 8251A USART controller, this communications interface circuit is programmed by the CPU to operate using synchronous, asynchronous, or business-machine serial-data-transmission techniques. Basically, the serial I/O device converts parallel data of the microprocessor into serial data and vice versa and generates appropriate supervisory lines to interface with a modem or other external peripheral devices.

3.6.1 Specifications

Table 3-18 lists the specifications for the Serial I/O Communications Controller.

3.6.2 Circuit Description

A functional block diagram of the serial I/O device is shown in Figure 3-17. Table 3-19 lists the serial I/O commands.

3.6.3 Interface

The serial I/O connects to the APC rear panel with a 26-pin cable connector, designated CN3 on the Controller PCB. The other end of the 26-pin cable connects to a 36-pin D-type connector similar to the printer connector. Table 3-20 lists and Figure 3-18 shows the pin assignments of all the cables. Table 3-21 explains the interface signals.

3.6.4 Programming Considerations

Operation of the 8251A processor is programmed by two 8-bit control words:

- A mode instruction word, which is the first word written into the 8251A after reset
- A command instruction word, which defines the operation to be performed.

Table 3-18 Serial I/O Communications Controller Specifications

Characteristics	Specifications
Processor	NEC 8251A
Channel	1
Transmission Mode	Half-Duplex or Full-Duplex
Synchronization	Synchronous or Asynchronous
Interface	EIA RS-232C
Line Speed	
Asynchronous Mode	50 to 19.2K Baud
Synchronous Mode	50 to 19.2K Baud
Business Machine	1200 Baud

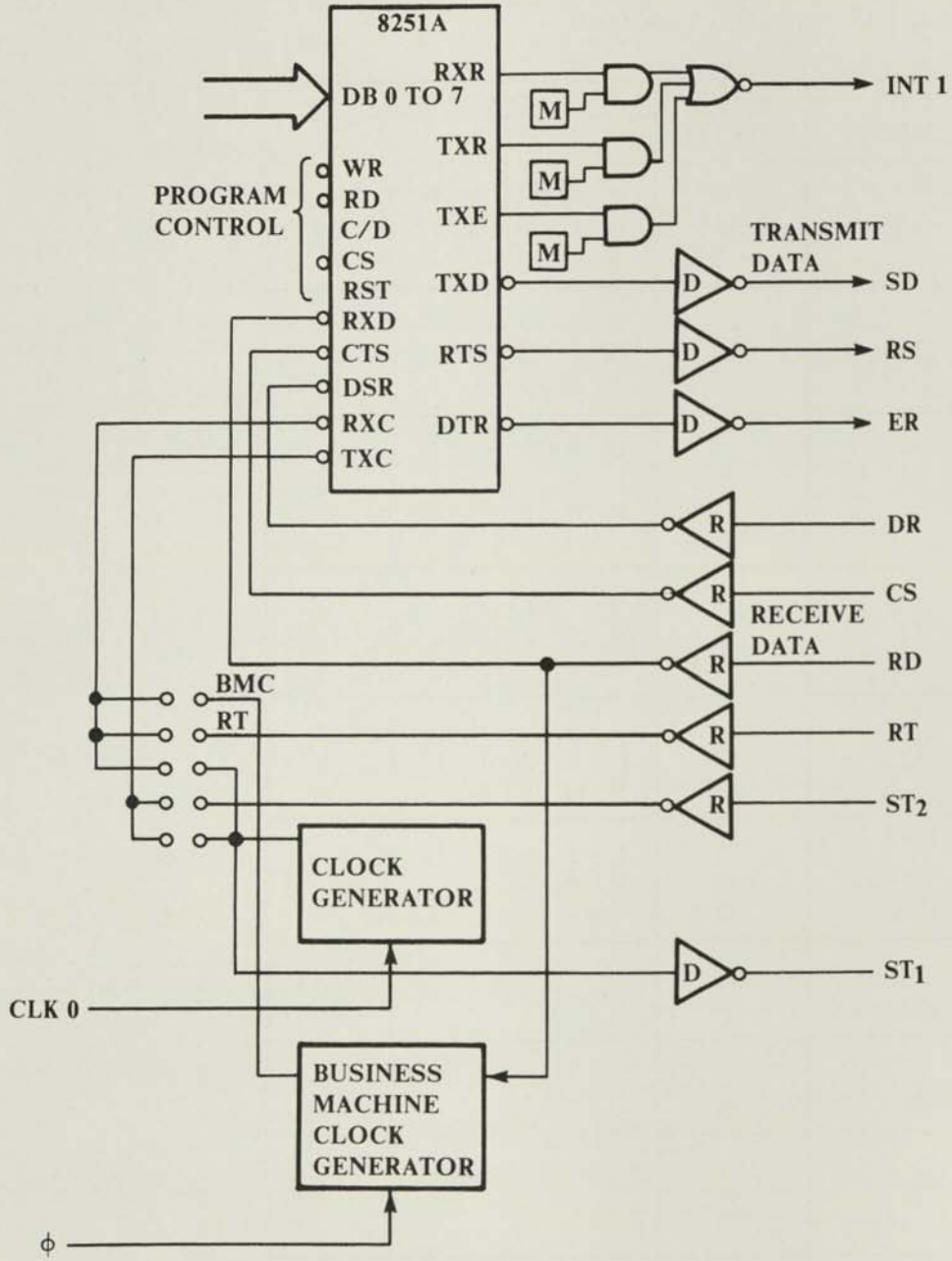


Figure 3-17 Serial I/O Communications Controller Block Diagram

Table 3-19 Serial I/O Commands

COMMAND	I/O ADDRESS	READ/ WRITE	DATA BUS							
			7	6	5	4	3	2	1	0
Read Data	30	R	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Write Data	30	W	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Read Status	32	R	DR	SYN	FE	OE	PE	TE	RRDY	TRDY
Write Mode (A)	32	W	S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1
Write Mode (S)	32	W	SCS	ESD	EP	PEN	L_2	L_1	0	0
Write Command	32	W	EH	IR	RS	RST	SBR	REN	ER	TEN
Write Mask	34	W							T_XE	R_XR T_XR
Read Signal	34	R							CS	CI CD
Write Signal	36	W								TDC

Table 3-20 Serial I/O Connectors Pin Assignments

SIGNAL	PIN NUMBER AT A	PIN NUMBER AT B	PIN NUMBER AT C	REMARKS
Frame Ground	1	1	1	
SD	2	2	3	
RD	3	3	5	
RS	4	4	7	
CS	5	5	9	
DR	6	6	11	
Signal Ground	7	7	13	
CD	8	8	15	
	9	9	17	No signal
	10	10	19	
	11	11	21	
	12	12	23	
	13	13	25	
	14	19	2	
ST2	15	20	4	
	16	21	6	No signal
RT	17	22	8	
	18	23	10	
	19	24	12	No signal
ER	20	25	14	
	21	26	16	
	22	27	18	No signal
	23	28	20	
ST1	24	29	22	
	25	30	24	No signal

Table 3-21 Serial I/O Device Interface Connector Pin Descriptions

SIGNAL	SOURCE	DESCRIPTION
SG	—	Signal ground
SD	Controller	Send data
RD	Modem	Receive data
RS	Controller	Request to send
CS	Modem	Clear to send
DR	Modem	Data set ready
SG		
ST2(TxC)	Modem	Transmit Clock
RT	Modem	Receive Clock
ER	Controller	Data Terminal Ready
ST1(RxC)	Controller	Transmit Clock

The processor can also read a status word from the 8251A, or write sync characters (in the Synchronous Mode), or specify that the data bus is to be read from or written to and transmitted to or received from (respectively) the modem. Instruction to the 8251A is determined by the levels on IC Pins 10, 11, 12, 13 and 21 (see Table 3-22).

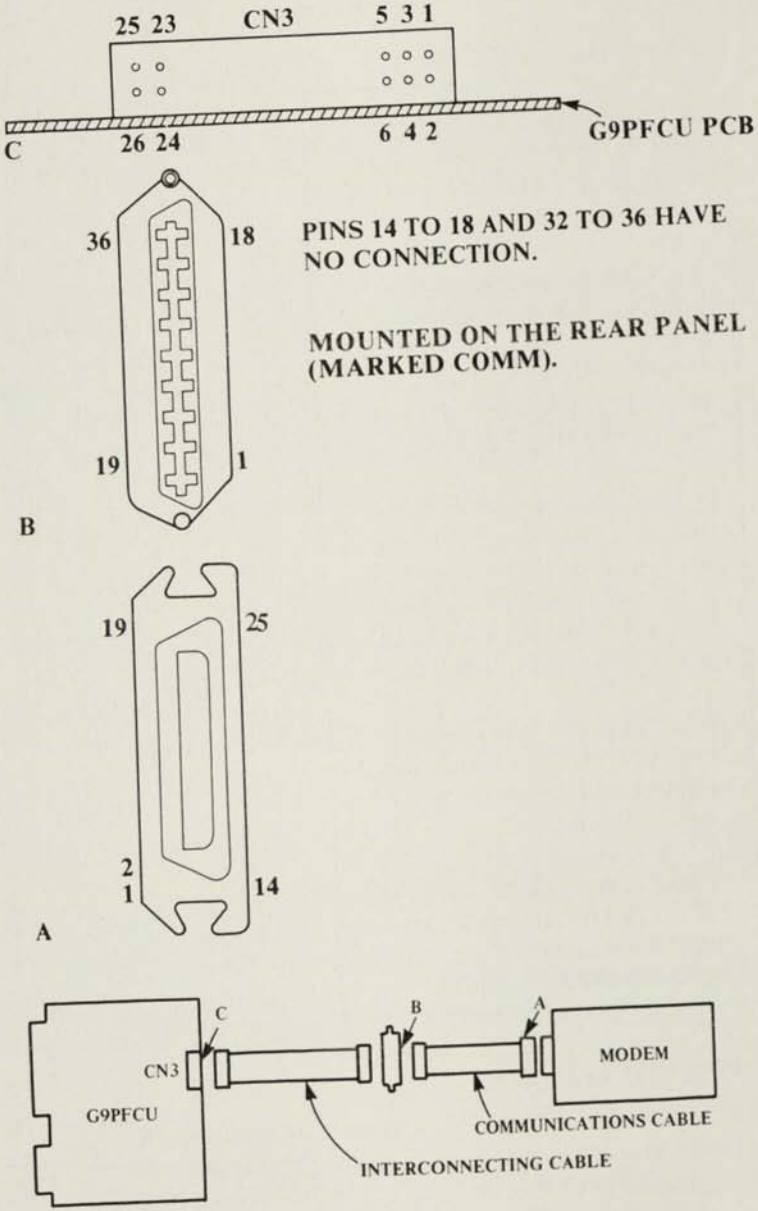


Figure 3-18 Communications Controller Cable Connections

Table 3-22 8251A Instructions

SYMBOL	NAME	DESCRIPTION
$\overline{WR}$	$\overline{WRITE}$	A Low on this line indicates that data on the bus is to be written into the 8251A (APC IOW line).
$\overline{CS}$	$\overline{CHIP\ SELECT}$	A Low on this line selects the 8251A, enabling read or write operations. This line must be Low for the 8251A to respond to or affect the data bus (APC S10 line).
C/$\overline{D}$	CONTROL/$\overline{DATA}$	A High on this line specifies that a control word is being written in or that a status word read out. A Low means that data is being written in or read out (APC AB line).
$\overline{RD}$	$\overline{READ}$	A Low on this line indicates that the data or a status word is being read from the 8251A (APC IOR line).
RST	RESET	A High on this line places the 8251A in an idle mode, waiting for a new set of control words (APC RST line).

3.6.4.1 ASYNCHRONOUS OPERATING MODE

The mode instruction word for asynchronous operation is shown in Figure 3-19. The format of the command instructions word is shown in Figure 3-20. Figure 3-21 shows the setup of jumper settings and the resulting circuit. Table 3-23 shows how the Baud rate is set.

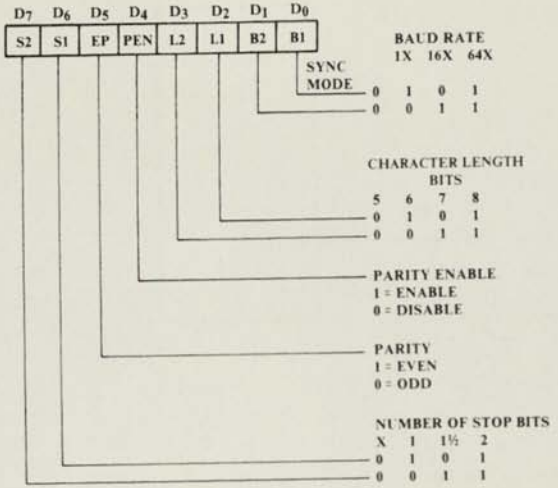


Figure 3-19 Asynchronous Mode Instruction Word

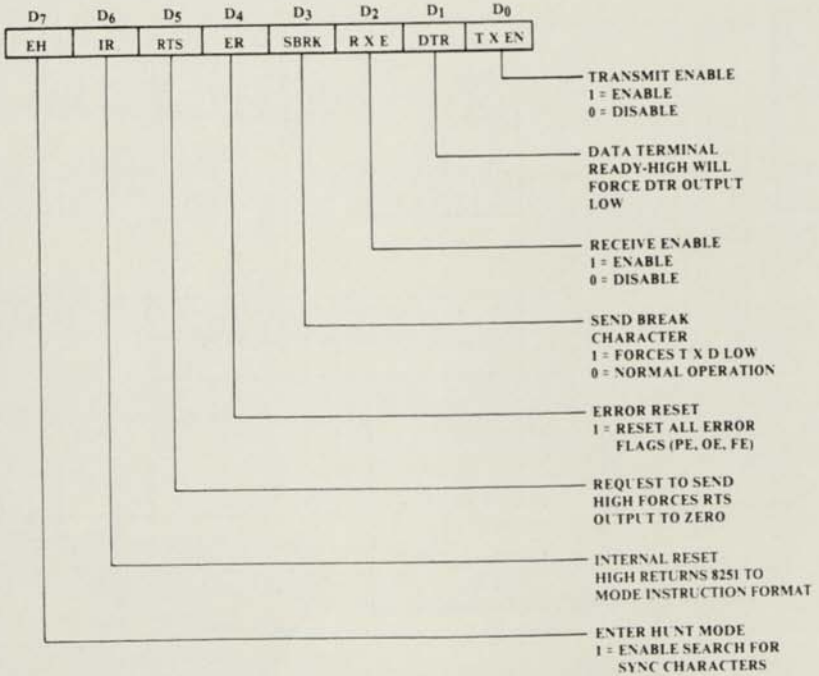


Figure 3-20 Command Instruction Word Format

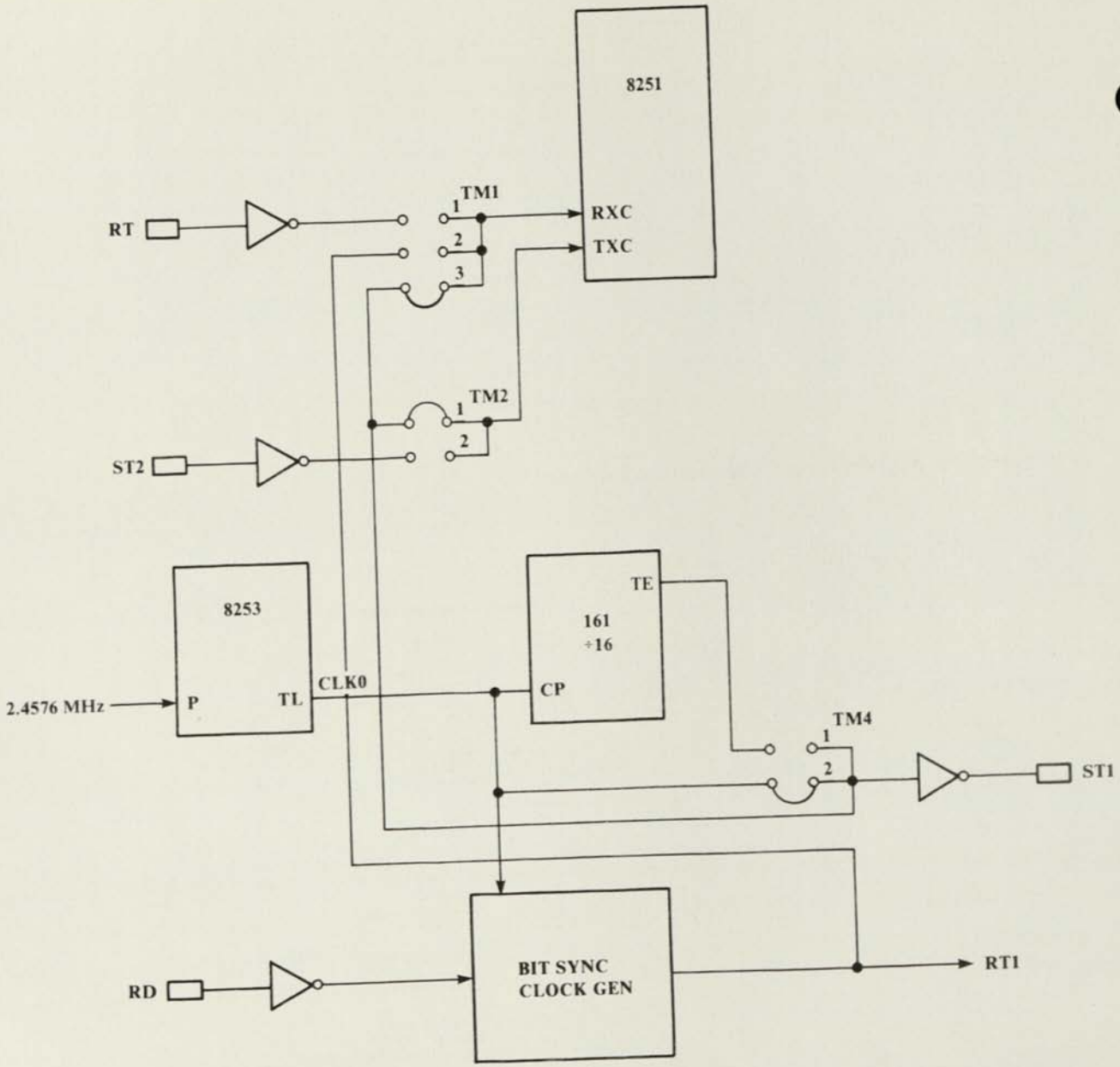


Figure 3-21 Communications Controller, Circuit for Asynchronous Operation

Table 3-23 Communications Controller, Baud Rate Coding During Asynchronous Operation

BAUD RATE	COUNT RATE*	COUNT REGISTER HIGH								COUNT REGISTER LOW							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19.2K	8	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9600	16	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
4800	32	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
2400	64	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1200	128	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
600	256	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
300	512	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
200	768	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
135																	
100	1536	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
75	2048	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
50	3072	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

*Count Rate = 2457600/(RxC or TxC) x 16 (Hz)

3.6.4.2 SYNCHRONOUS OPERATING MODE

The mode instruction word for synchronous operation is shown by Figure 3-22. Figures 3-23 and 3-24 show the circuits for synchronous operation using external (Modem) and interval clocks, respectively. Table 3-24 lists the Baud rate setting codes in synchronous operation.

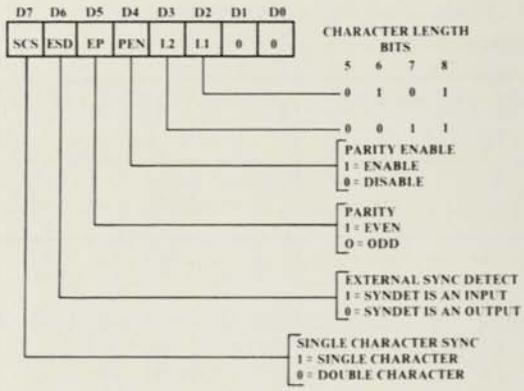


Figure 3-22 Synchronous Mode Instruction Word

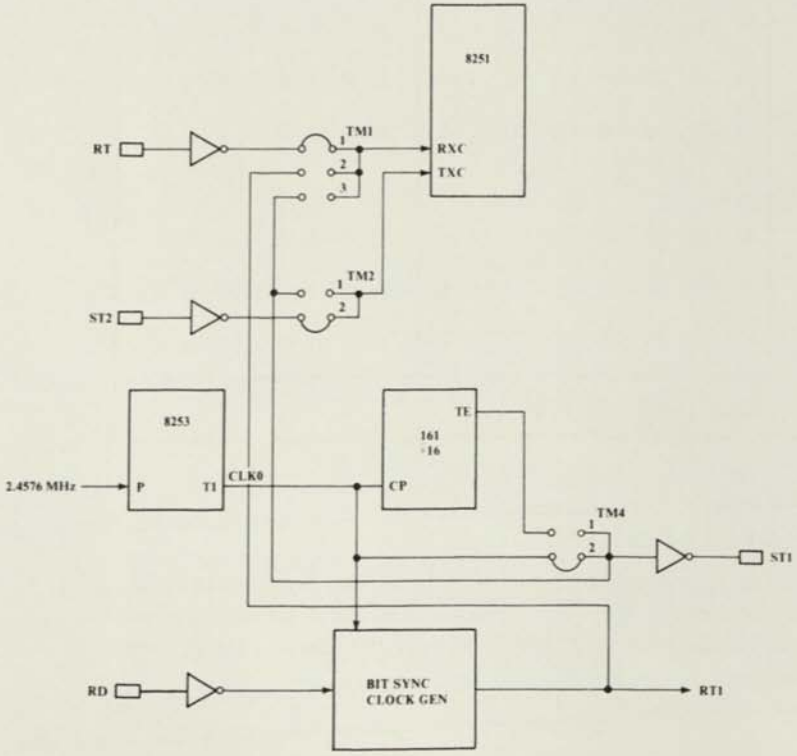


Figure 3-23 Communications Controller, Circuit for Synchronous Operation Using External Clock

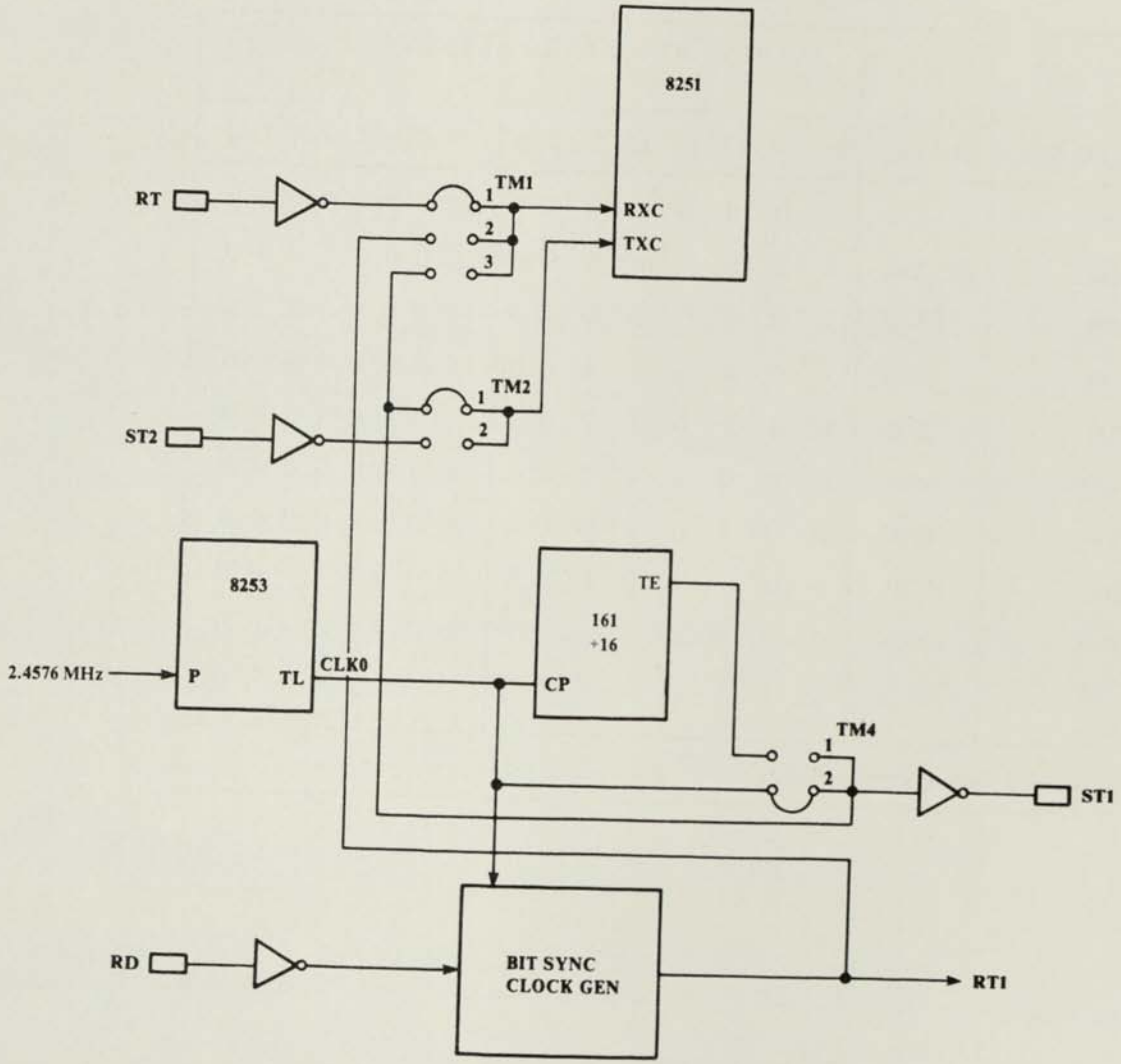


Figure 3-24 Communications Controller, Circuit for Synchronous Operation Using Internal Clock

Table 3-24 Communications Controller, Baud Rate Coding During Synchronous Operation

BAUD RATE	COUNT RATE*	COUNT REGISTER HIGH								COUNT REGISTER LOW							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19.2K	128	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
9600	256	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
4800	512	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
2400	1024	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1200	2048	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
600	4096	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
300	8192	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
200	12288	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
100	18204	0	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0
75	24756	0	1	1	0	0	0	0	0	1	0	1	1	0	1	0	0

*Count Rate = 2457600/Baud (Hz)

3.6.4.3 BUSINESS MACHINE OPERATING MODE

Figure 3-25 shows the circuit and Table 3-25 lists the Baud rate setting codes when operation with business-machine timing.

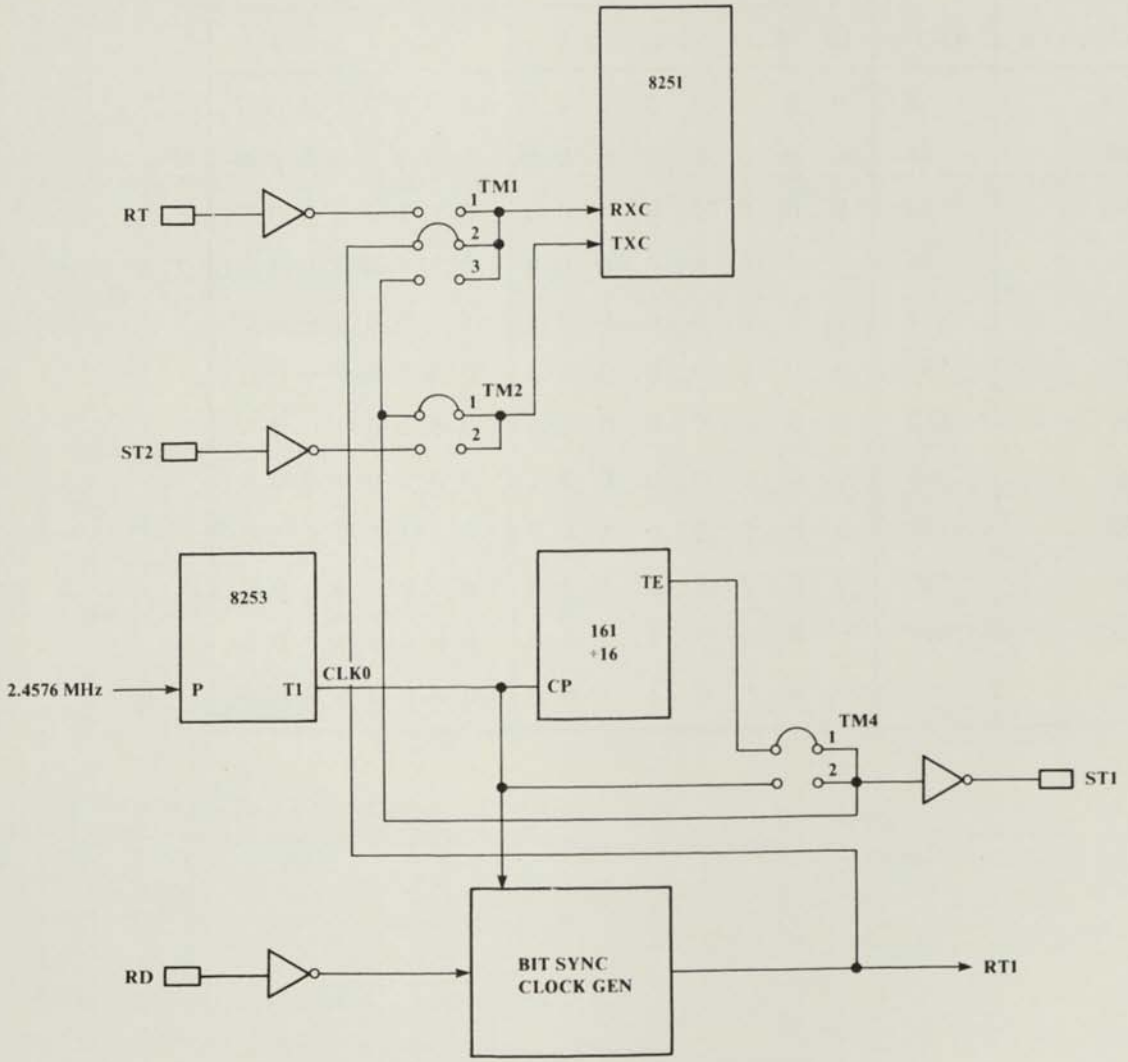


Figure 3-25 Communications Controller, Circuit for Business Machine Clock

Table 3-25 Communications Controller, Baud Rate Coding During Operations with Business Machine Clocking

BAUD RATE	RATE	COUNT REGISTER HIGH								COUNT REGISTER LOW							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
19.2K	8	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9600	16	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
4800	32	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
2400	64	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1200	128	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
600	256	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
300	512	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
200	768	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
135	1138	0	0	0	0	0	1	0	0	0	1	1	1	0	0	1	0
100	1536	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
75	2048	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
50	3072	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

3.6.5 Status Word Format

The status word format is shown by Figure 3-26.

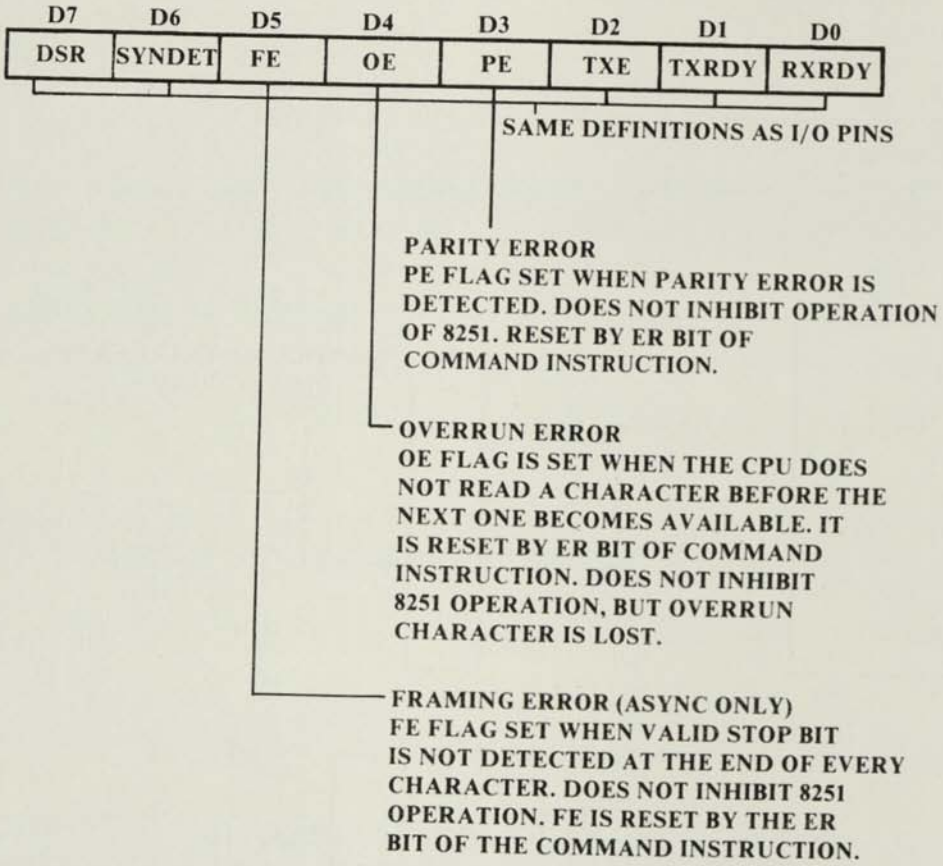


Figure 3-26 Communications Controller, Status Word Format

3.7 SOUND CONTROL

The sound control system is supported by the NEC μPD1771C-006, which drives a loudspeaker through a ¼-Watt audio amplifier. This LSI generates audio signals and programmable music. Through music programming, the sound control system can generate tones ranging over two octaves in frequency, at specified note lengths, intensities, and tempos.

A functional block diagram of the sound control system is shown in Figure 3-27. The sound system speaker is mounted near the front of the main unit. An operator's volume control is also provided.

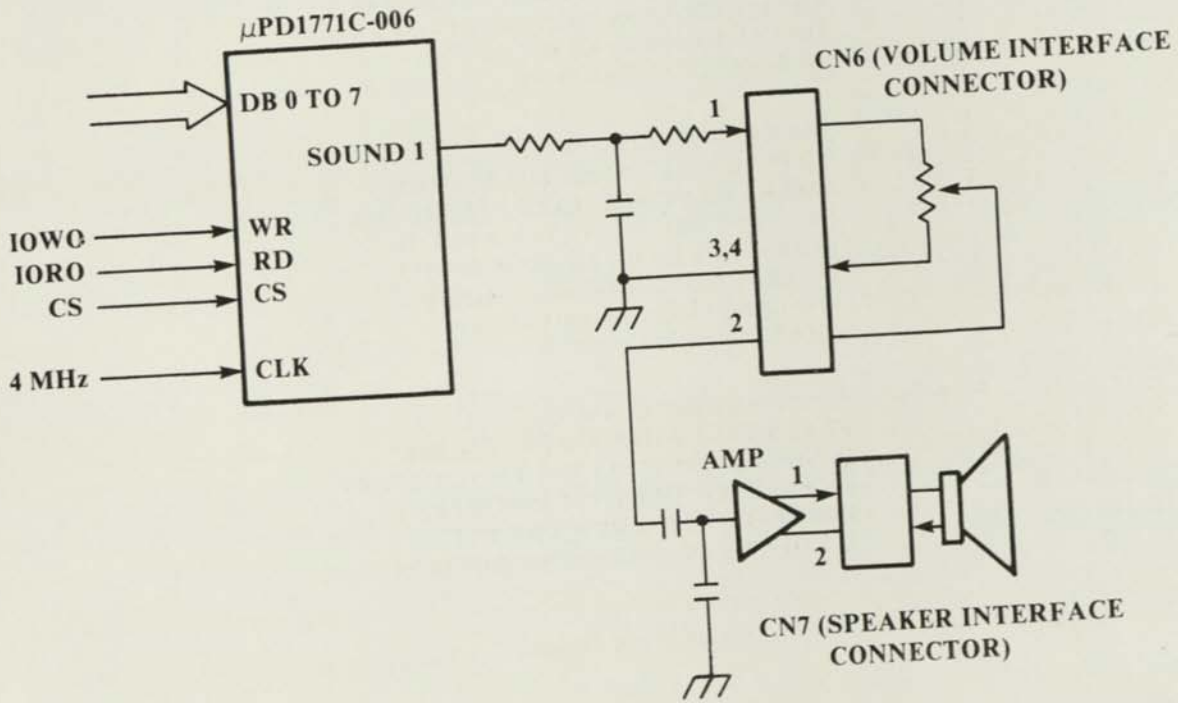


Figure 3-27 Sound Control Block Diagram

3.7.1 Interface

Figure 3-28 shows the sound control interface with the Controller PCB, and Table 3-26 describes the pin assignments.

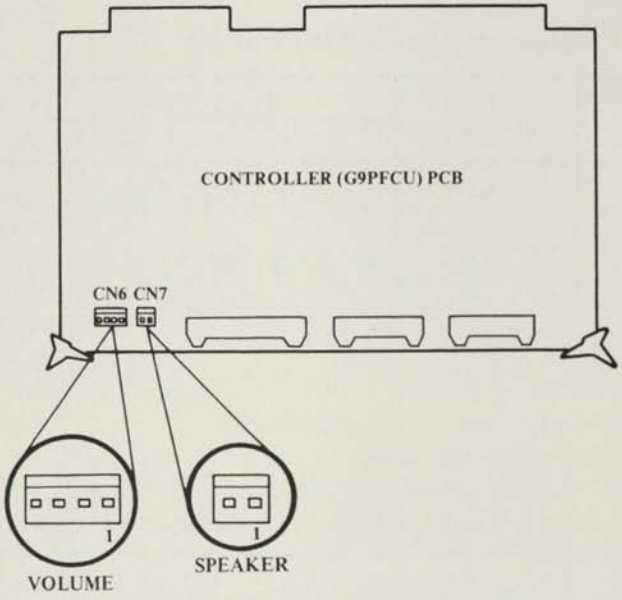


Figure 3-28 Location of Sound Interface Connectors

Table 3-26 Sound Interface Pin Assignments

CONNECTOR	PIN	SIGNAL
CN6 (Volume Interface)	1	Volume In
	2	Volume Out
	3	Ground
	4	Ground
CN7 (Speaker Interface)	1	SP+
	2	SP-

3.7.2 Programming Considerations

Tables 3-27, 3-28 and 3-29 give format and command information for sound-programming users.

Table 3-27 Sound Programming Read/Write Format

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS 7 6 5 4 3 2 1 0
Write Command	W	60	0 FS C5 C4 C3 C2 C1 C0
Read Status	R	60	S7 S6 S5 S4 S3 S2 S1 S0

Legend:

FS = First (0) or Second (1) command identification
C0 to C5 = Sound Control and Scale commands
S0 to S7 = Status information: if HEX value is 80, all the write commands are accepted; if HEX value is 00, only the Beep command is accepted.

Table 3-28 Sound Control Commands

FIRST COMMAND		SECOND COMMAND		
COMMAND	DATA BUS 7 6 5 4 3 2 1 0	MUSIC EXPRESSION		DATA BUS 7 6 5 4 3 2 1 0
Music Notes	0 0 1 1 0 0 0 1	Volume	Illegal	0 1 0 0 0 0 0 0
Beep Notes			Piano	0 1 0 0 0 0 0 1
20 ms	0 0 1 1 1 0 X X		Medium	0 1 0 0 0 0 1 0
6 minutes	0 0 1 1 1 1 X X		Forte	0 1 0 0 0 0 1 1
710 Hz	0 0 1 1 1 X 0 0	Tempo	Slow (1.0 sec)	0 1 0 1 0 0 0 0
1202 Hz	0 0 1 1 1 X 0 1		Moderately Slow (0.87 sec)	0 1 0 1 0 0 0 1
2038 Hz	0 0 1 1 1 X 1 0			

Table 3-28 Sound Control Commands (cont'd)

FIRST COMMAND		SECOND COMMAND	
	DATA BUS		DATA BUS
COMMAND	7 6 5 4 3 2 1 0	MUSIC EXPRESSION	7 6 5 4 3 2 1 0
3906 Hz	0 0 1 1 1 X 1 1	Moderately Fast (0.56 sec)	0 1 0 1 0 0 1 0
		Fast (0.38 sec)	0 1 0 1 0 0 1 1
		Sharp Attack (Bell-like)	
		Illegal	0 1 1 0 0 0 0 0
		Piano	0 1 1 0 0 0 0 1
		Medium	0 1 1 0 0 0 1 0
		Forte	0 1 1 0 0 0 1 1
		Soft Attack (Piano-like)	
		Illegal	0 1 1 1 0 0 0 0
		Piano	0 1 1 1 0 0 0 1
		Medium	0 1 1 1 0 0 1 0
		Forte	0 1 1 1 0 0 1 1

Table 3-29 Sound Scale Commands

FIRST COMMAND (NOTE TONE)		SECOND COMMAND (NOTE DURATION)	
	DATA BUS		DATA BUS
COMMAND	7 6 5 4 3 2 1 0	COMMAND	7 6 5 4 3 2 1 0
Illegal	0 0 0 0 0 0 0 0	Moderately emphatic rhythm	0 1 0 0 X X X X
C	0 0 0 0 0 0 0 1	Emphatic rhythm	0 1 0 1 X X X X
C#	0 0 0 0 0 0 1 0	Note without point	0 1 0 X 0 X X X
D	0 0 0 0 0 0 1 1	Note with point	0 1 0 X 1 X X X
D#	0 0 0 0 0 1 0 0	(Except thirty-second note)	
E	0 0 0 0 0 1 0 1	Whole note (o)	0 1 0 X X 0 0 0
F	0 0 0 0 0 1 1 0	Half note (o)	0 1 0 X X 0 0 1
F#	0 0 0 0 0 1 1 1	Quarter note (♩)	0 1 0 X X 0 1 0
G	0 0 0 0 1 0 0 0	Eighth note (♪)	0 1 0 X X 0 1 1
G#	0 0 0 0 1 0 0 1		

Table 3-29 Sound Scale Commands (cont'd)

FIRST COMMAND (NOTE TONE)									SECOND COMMAND (NOTE DURATION)								
COMMAND	DATA BUS 7	6	5	4	3	2	1	0	COMMAND	DATA BUS 7	6	5	4	3	2	1	0
A	0	0	0	0	1	0	1	0	Sixteenth note (♬)	0	1	0	X	X	1	0	0
A#	0	0	0	0	1	0	1	1	Thirty-second note (♬)	0	1	0	X	X	1	0	1
B	0	0	0	0	1	1	0	0	Illegal	0	1	0	X	X	1	1	0
C	0	0	0	0	1	1	0	1	Illegal	0	1	0	X	X	1	1	1
C#	0	0	0	0	1	1	1	0									
D	0	0	0	0	1	1	1	1									
D#	0	0	0	1	0	0	0	0									
E	0	0	0	1	0	0	0	1									
F	0	0	0	1	0	0	1	0									
F#	0	0	0	1	0	0	1	1									
G	0	0	0	1	0	1	0	0									
G#	0	0	0	1	0	1	0	1									
A	0	0	0	1	0	1	1	0									
A#	0	0	0	1	0	1	1	1									
B	0	0	0	1	1	0	0	0									
C	0	0	0	1	1	0	0	1									
C#	0	0	0	1	1	0	1	0									
D	0	0	0	1	1	0	1	1									
D#	0	0	0	1	1	1	0	0									
E	0	0	0	1	1	1	0	1									
	0	0	0	1	1	1	1	0									
Illegal	Through																
	0	0	1	0	1	1	1	1									
Rest	0	0	1	1	0	0	0	0									
	0	0	1	1	0	0	0	1									
Illegal	Through																
	0	0	1	1	1	1	1	1									

3.8 JUMPER SETTINGS

Figure 3-29 shows the Controller PCB jumper settings, which adapt the system to various communications situations and to either monochrome or color display.

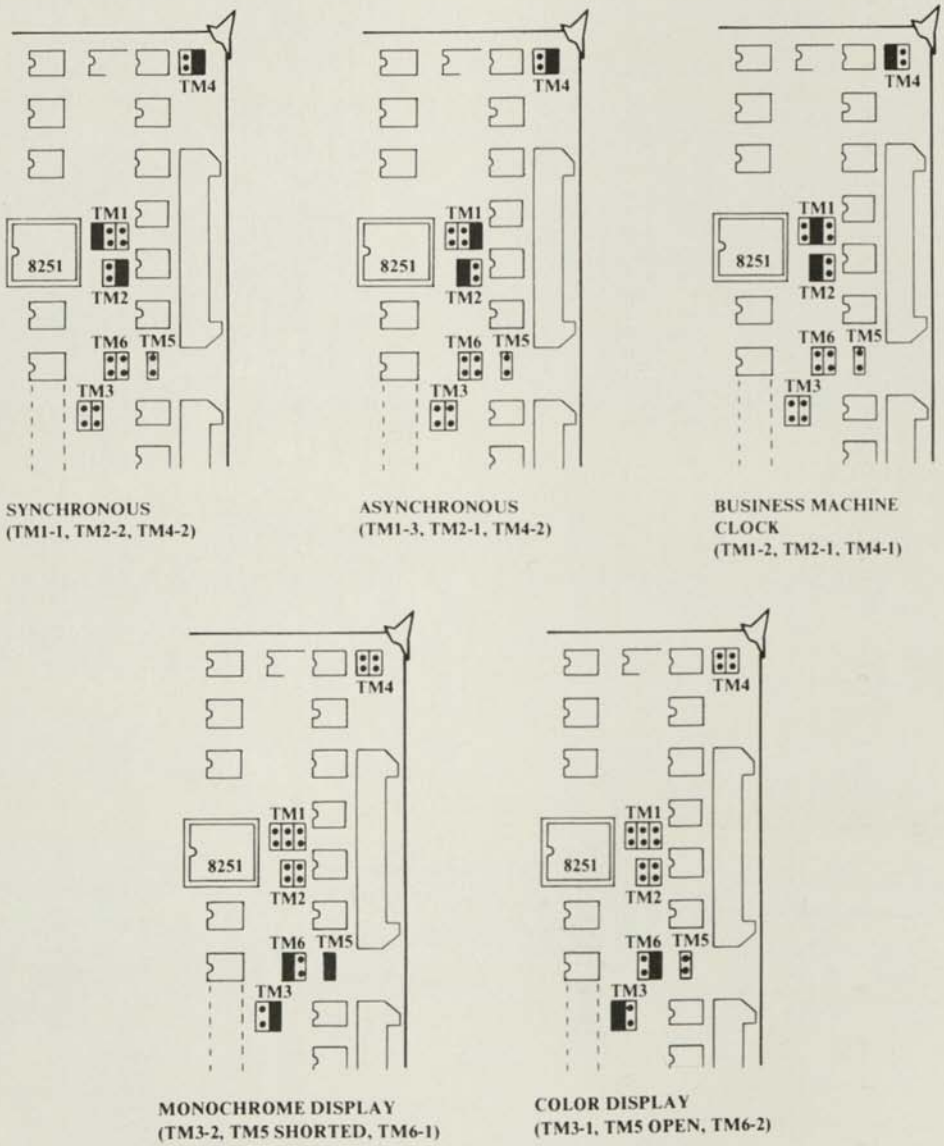
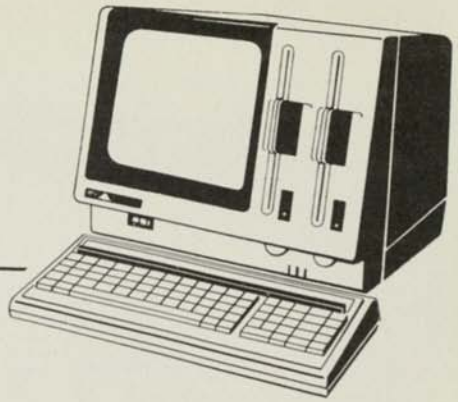


Figure 3-29 Controller PCB Jumper Settings

POWER SUPPLY



Chapter 4

Power Supply

The dc power supply is a 100 W, 5-voltage level, switching regulator providing the following dc outputs. The power supply also provides a noise-filtered switched 115 V, 60 Hz output at 1.2 A, and a single-pole, single-throw power control switch output for external power On/Off control.

- +5 Vdc ± 5% @ 9 A
- -5 Vdc ± 5% @ 0.3 A
- +12 Vdc ± 5% @ 0.3 A
- -12 Vdc ± 5% @ 0.25 A
- +24 Vdc ± 10% @ 1.8 A

The power supply furnishes all required power to APC components in the Keyboard and terminal cabinet and is located in a removable chassis module under the CRT Display. The power On/Off Switch is an integral part of the power supply.

All dc outputs are regulated and have overcurrent and overvoltage protection. Ripple voltage does not exceed 50 mV at any dc output except the 24 V output, where the ripple voltage does not exceed 100 mV. Spike noise voltage is less than 250 mV on any output. If an overload or overvoltage condition exists on any of the dc outputs, the unit automatically shuts down until the condition is corrected and the power is recycled off and on. The power supply is designed for continuous operation at 100 W of dc output and 130 W of ac output. The ac output is 2.5 A maximum at 104 to 132 V, 60 ± 0.5 Hz and is fused for 5.0 A.

The APC power supply incorporates a POF circuit that enables remote On/Off switching of both ac and dc outputs. The POF character is 5B and its address is AD08.

A functional block diagram of the power supply is shown by Figure 4-1, which also shows additional specifications of the POF feature.

The input and output cable connections to and from the power supply are shown in Figure 4-2 and listed in Table 4-1.

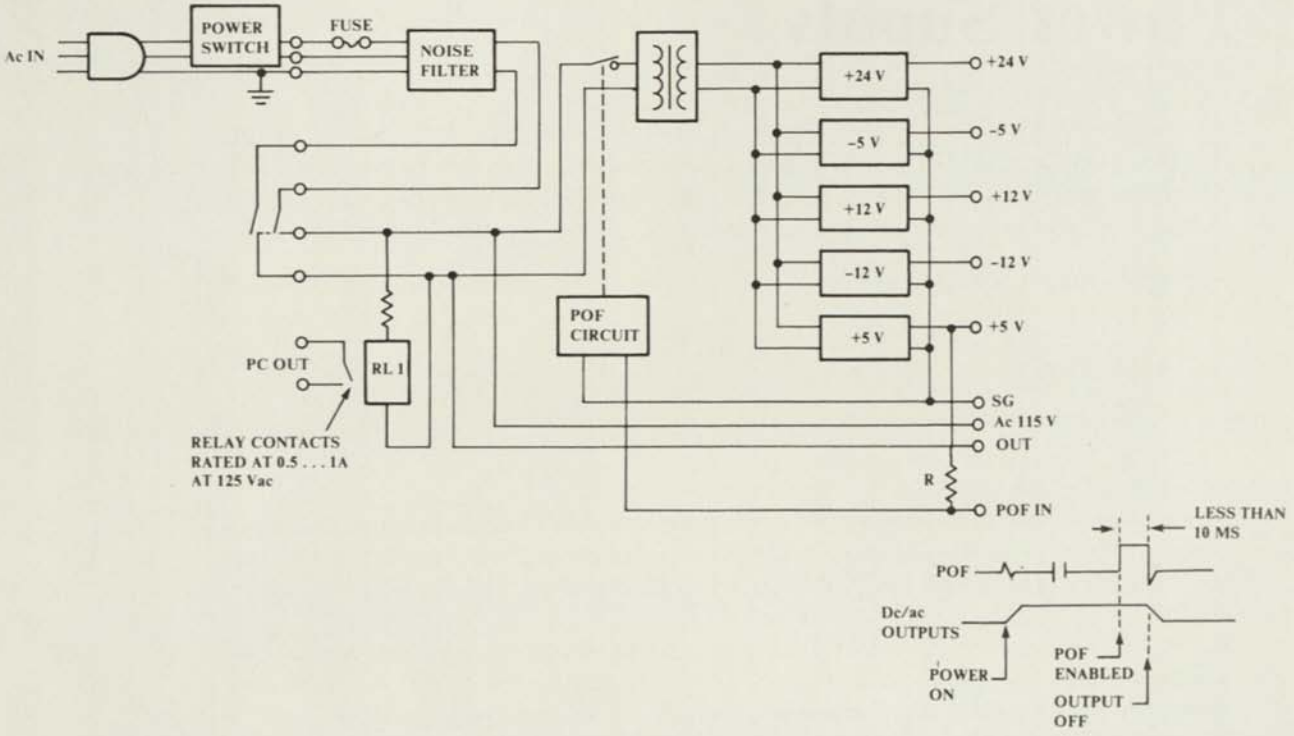


Figure 4-1 System Power Supply Block Diagram

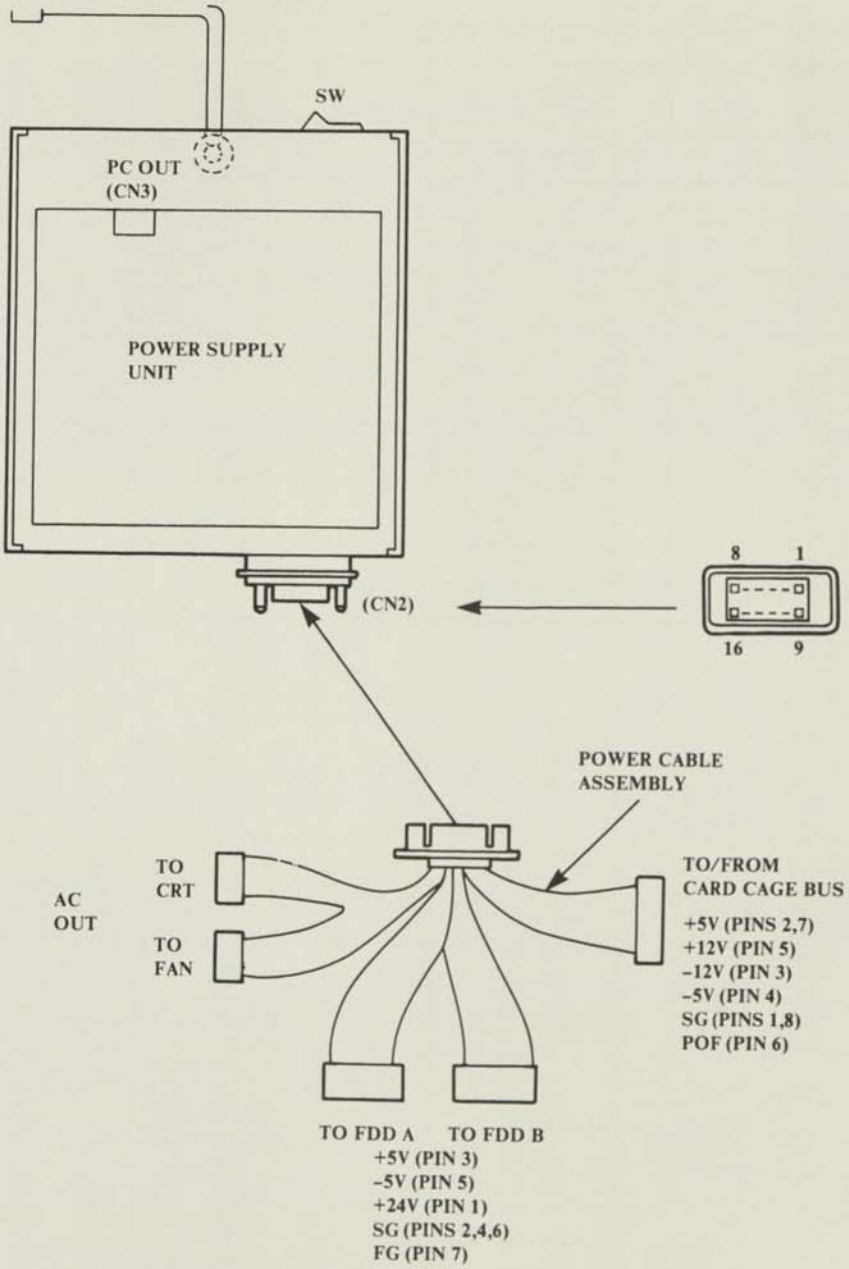


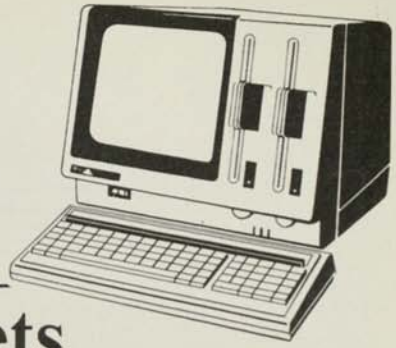
Figure 4-2 Power Supply Interconnection Diagram

Table 4-1 Power Supply Pin Command Assignments

CN2 PIN NUMBER	DESCRIPTION	CN2 PIN NUMBER	DESCRIPTION
1	115 Vac	9	115 Vac
2	Ground	10	Ground
3	+12 Vdc	11	-12 Vdc
4	-5 Vdc	12	-5 Vdc
5	P0F	13	+24 Vdc
6	+5 Vdc	14	Ground
7	+5 Vdc	15	+5 Vdc
8	Ground	16	Ground

IC DATA SHEETS

IC DATA SHEETS



Appendix A

Integrated Circuit Data Sheets

16-BIT MICROPROCESSOR*

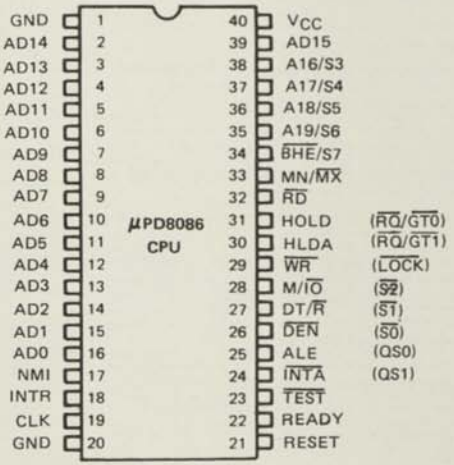
DESCRIPTION

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

FEATURES

- Can Directly Address 1 Megabyte of Memory
- Fourteen 16-Bit Registers with Symmetrical Operations
- Bit, Byte, Word, and Block Operations
- 8- and 16-Bit Signed and Unsigned Arithmetic Operations in Binary or Decimal
- Multiply and Divide Instructions
- 24 Operand Addressing Modes
- Assembly Language Compatible with the μPD8080/8085
- Complete Family of Components for Design Flexibility

PIN CONFIGURATION



*Preliminary

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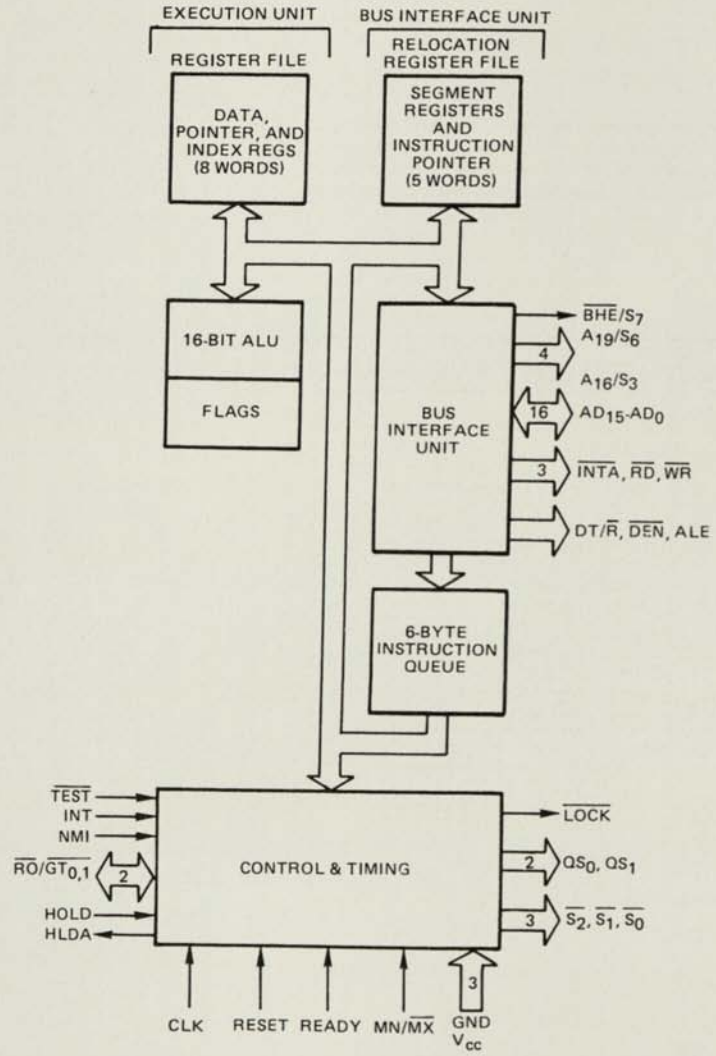
NOTE: These manufacturer's specifications are provided for reference. The APC may not use some of the functions described here.

PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
2-16, 39	AD0-AD15	Address/Data Bus	Multiplexed address (T_1) and data (T_2, T_3, T_W, T_4) bus. 8-bit peripherals tied to the lower 8 bits, use A0 to condition chip select functions. These lines are tri-state during interrupt acknowledge and hold states.
17	NMI	Non-Maskable Interrupt	This is an edge triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.
18	INTR	Interrupt Request	A level triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.
19	CLK	Clock	The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	ALE	Address Latch Enable	This is used in conjunction with the μPD8282/8283 latches to latch the address, during T_1 of any bus cycle.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/Receive	Used to control the direction of data flow through the transceivers.
28	M/$\overline{IO}$	Memory/IO Status	This is used to separate memory access from I/O access.
29	$\overline{WR}$	Write	Depending on the state of the M/$\overline{IO}$ line, the processor is either writing to I/O or memory.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus return active one cycle after HOLD goes back low.
31	HOLD	Hold	When another device requests the local bus, driving HOLD high, will cause the μPD8086 to issue a HLDA.
32	$\overline{RD}$	Read	Depending on the state of the M/$\overline{IO}$ line, the processor is reading from either memory or I/O.
33	MN/$\overline{MX}$	Minimum/Maximum	This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.
34	$\overline{BHE}$/S_7	Bus/High Enable	This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.
35-38	A16-A19	Most Significant Address Bits	The four most significant address bits for memory operations. Low during I/O operations.
26, 27, 28 34-38	S_0-S_7	Status Outputs	These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.
24, 25	QS_1, QS_0	Que Status	Used to track the internal μPD8086 instruction que.
29	$\overline{LOCK}$	Lock	This output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.
30, 31	$\overline{RQ}$/$\overline{GT_0}$ $\overline{RQ}$/$\overline{GT_1}$	Request/Grant	Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−1.0 to +7V
Power Dissipation	2.5W

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	+0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.5 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Power Supply Current μPD8086/ μPD8086-2	I_{CC}		 340 350	 mA mA	$T_a = 25°C$
Input Leakage Current	I_{LI}		±10	μA	$0V < V_{IN} < V_{CC}$
Output Leakage Current	I_{LO}		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Clock Input Low Voltage	V_{CL}	−0.5	+0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IN}		15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IO}		15	pF	fc = 1 MHz

AC CHARACTERISTICS

μPD8086: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

MINIMUM COMPLEXITY SYSTEM

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data In Setup Time	TDVCL	30		20		ns	
Data In Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ①②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ①②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY Inactive to CLK ③	TRYLCL	–8		–8		ns	
HOLD Setup Time	THVCH	35		20		ns	
INTR, NMI, $\overline{TEST}$ Setup Time ②	TINVCH	30		15		ns	
Input Rise Time	TILIH		20			ns	From 0.8V to 2.0V
Input Fall Time	TIHIL		12			ns	From 2.0V to 0.8V

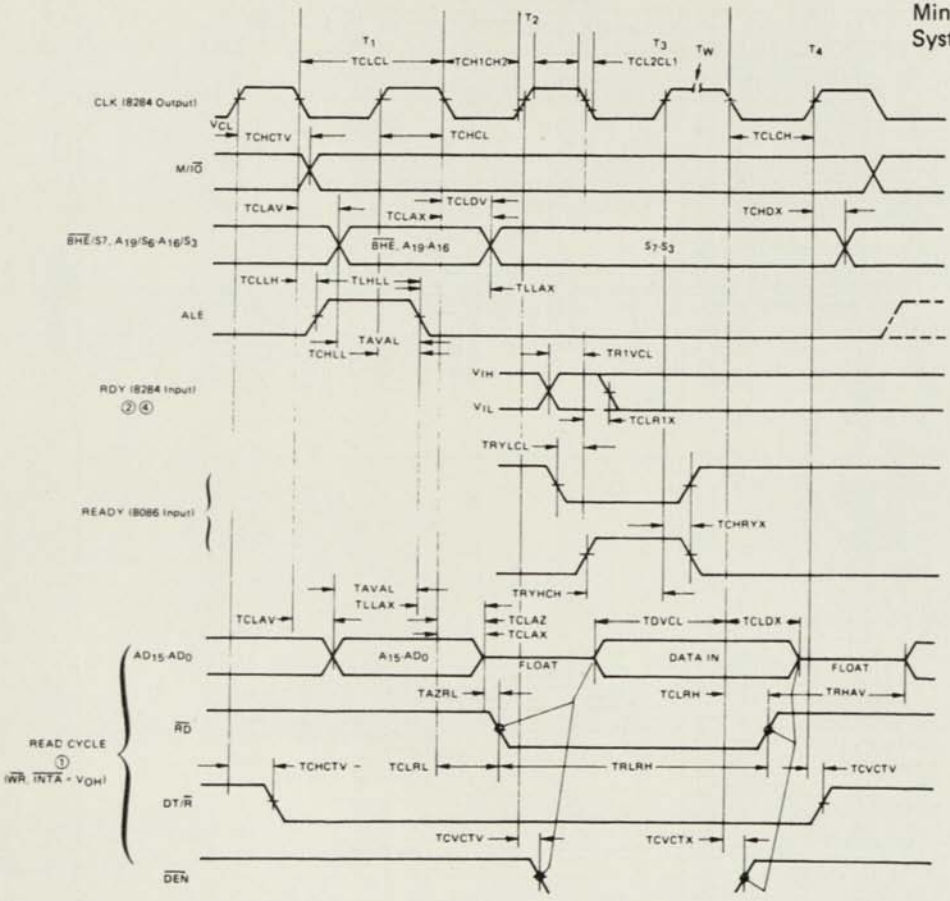
TIMING RESPONSES

TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Valid Delay	TCLAV	10	110	10	60		
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
ALE Width	TLHLL	TCLCH–20		TCLCH–10		ns	
ALE Active Delay	TCLLH		80		50	ns	
ALE Inactive Delay	TCHLL		85		55	ns	
Address Hold Time to ALE Inactive	TLLAX	TCHCL–10		TCHCL–10		ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
Data Hold Time	TCHDX	10		10		ns	
Data Hold Time After WR	TWHDX	TCLCH–30		TCLCH–30		ns	
Control Active Delay 1	TCVCTV	10	110	10	70	ns	
Control Active Delay 2	TCHCTV	10	110	10	60	ns	
Control Active Delay	TCVCTX	10	110	10	70	ns	
Address Float to READ Active	TAZRL	0		0		ns	
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL–45		TCLCL–40		ns	
HLDA Valid Delay	TCLHAV	10	160	10	100	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL–75		2TCLCL–50		ns	
$\overline{WR}$ Width	TWLWH	2TCLCL–60		2TCLCL–40		ns	
Address Valid to ALE Low	TAVAL	TCLCH–60		TCLCH–40		ns	
Output Rise Time	TOLOH		20			ns	From 0.8V to 2.0V
Output Fall Time	TOHOL		12			ns	From 2.0V to 0.8V

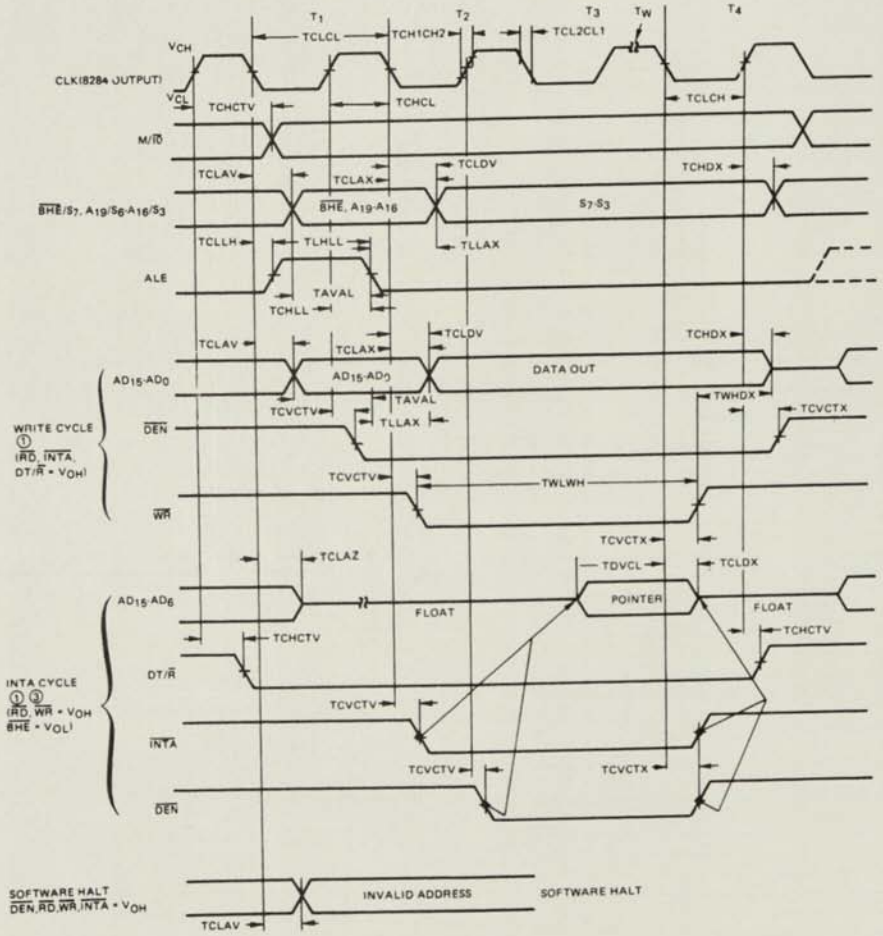
NOTES: ① Signal at μPD8284 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T2 state. (8 ns into T3)

Minimum Complexity Systems ⑤



TIMING WAVEFORMS

Minimum Complexity Systems (Con't.) ⑤



NOTES:

① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.

③ Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

④ Signals at μPD8284 are shown for reference only.

⑤ All timing measurements are made at 1.5V unless otherwise noted.

MAXIMUM MODE SYSTEM
With μPB8288
Bus Controller

TIMING WITH μPB8288 BUS CONTROLLER

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data in Setup Time	TDVCL	30		20		ns	
Data in Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ①②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ①, ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY inactive to CLK ④	TRYLCL	-8		-8		ns	
Setup Time for Recognition (INTR, NMI, TEST) ②	TINVCH	30		15		ns	
RQ/GT Setup Time	TGVCH	30		15		ns	
RQ/GT Hold Time into μPD8086	TCHGX	40		30		ns	
Input Rise Time	TILIH		20			ns	From 0.8V to 2.0V
Input Fall Time	TIHIL		12			ns	From 2.0V to 0.8V

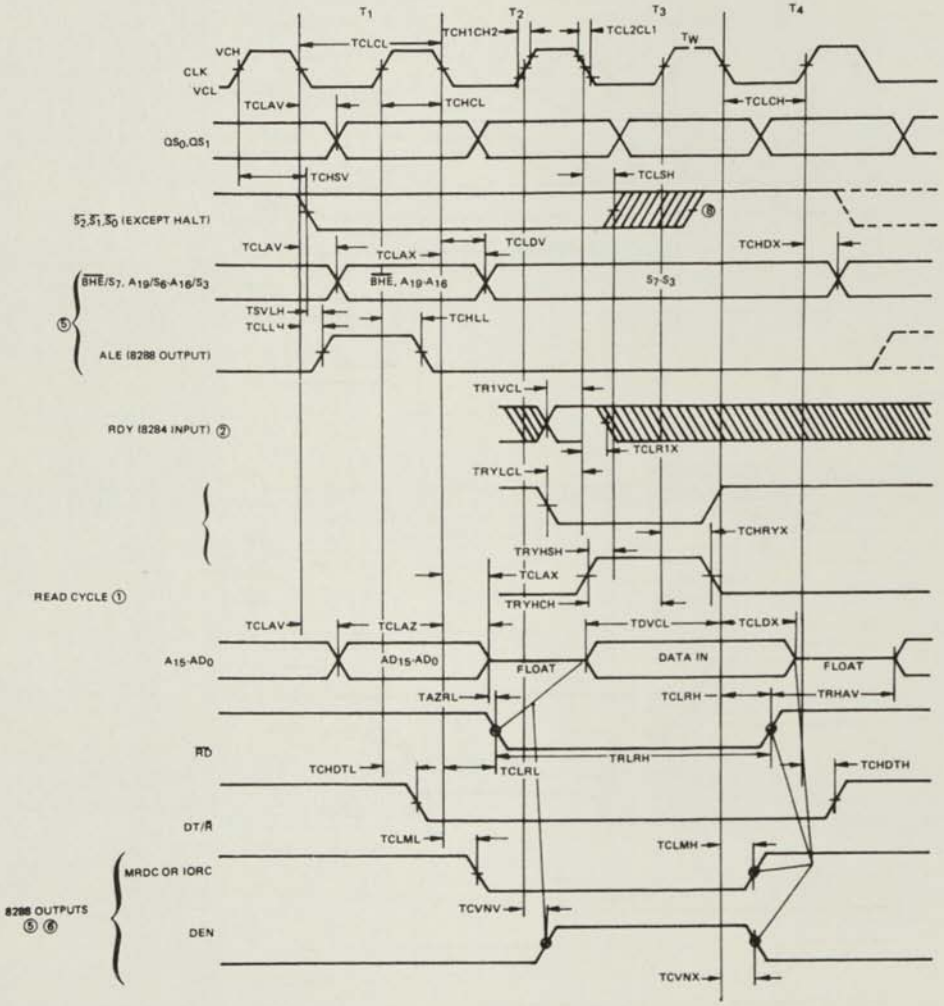
TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Command Active Delay (See Note 1)	TCLML	10	35	10	35	ns	
Command Inactive Delay (See Note 1)	TCLMH	10	35	10	35	ns	
READY Active to Status Passive (See Note 3)	TRYHSH		110		65	ns	
Status Active Delay	TCHSV	10	110	10	60	ns	
Status Inactive Delay	TCLSH	10	130	10	70	ns	
Address Valid Delay	TCLAV	10	110	10	60	ns	
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
Status Valid to ALE High (See Note 1)	TSVLH		15		15	ns	
Status Valid to MCE High (See Note 1)	TSVMCH		15		15	ns	
CLK Low to ALE Valid (See Note 1)	TCLLH		15		15	ns	
CLK Low to MCE High (See Note 1)	TCLMCH		15		15	ns	
ALE Inactive Delay (See Note 1)	TCHLL		15		15	ns	C_L = 20-100 pF for all μPD8086 Outputs (in addition to μPD8086 self-load)
MCE Inactive Delay (See Note 1)	TCLMCL		15		15	ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns	
Control Inactive Delay (See Note 1)	TCVNX	10	45	10	45	ns	
Address Float to Read Active	TAZRL	0		0		ns	
RD Active Delay	TCLRL	10	165	10	100	ns	
RD Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns	
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns	
Direction Control Inactive Delay (See Note 1)	TCHDTH		30		30	ns	
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns	
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL-50		2TCLCL-50		ns	
Output Rise Time	TOLOH		20			ns	From 0.8V to 2.0V
Output Fall Time	TOHOL		12			ns	From 2.0V to 0.8V

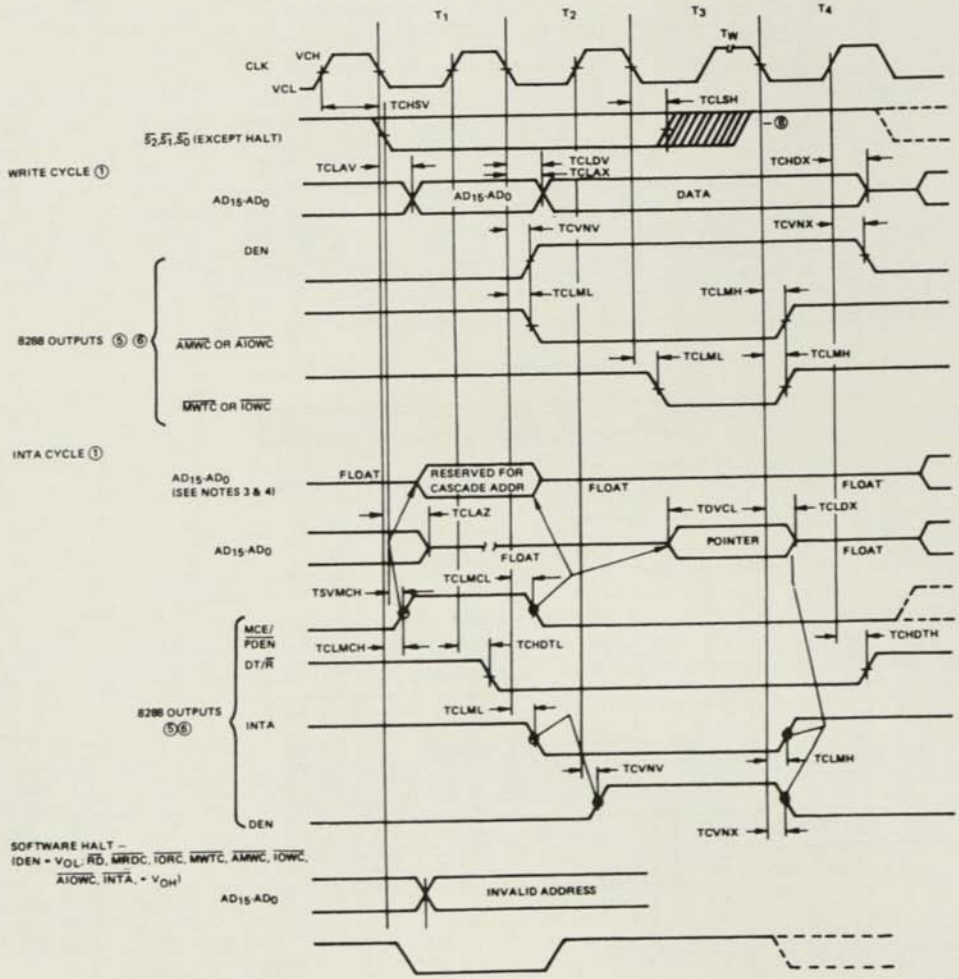
NOTES: ① Signal at μPB8284 or μPB8288 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T3 and wait states.
④ Applies only to T2 state (8 ns into T3).

TIMING WAVEFORMS

Maximum Mode System Using μPB8288 Controller ⑦

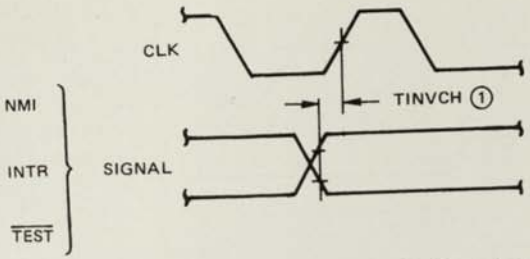


TIMING WAVEFORMS
Maximum Mode
System Using
μPB8288 Controller
(Con't.) ⑦



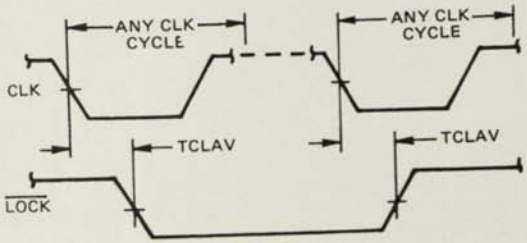
NOTES:
① All signals switch between V_{OH} and V_{OL} unless otherwise specified.
② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
③ Cascade address is valid between first and second INTA cycle.
④ Two INTA cycles run back-to-back. The 8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
⑤ Signals at 8284 or 8288 are shown for reference only.
⑥ The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
⑦ All timing measurements are made at 1.5V unless otherwise noted.
⑧ Status inactive in state just prior to T_4.

ASYNCHRONOUS SIGNAL RECOGNITION

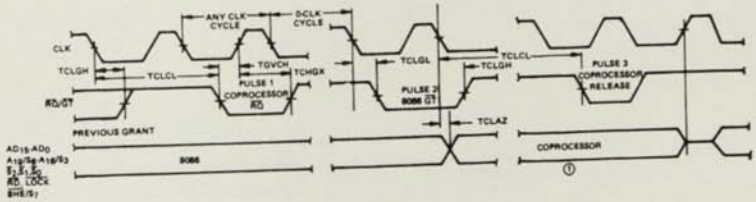


NOTE: ① Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING



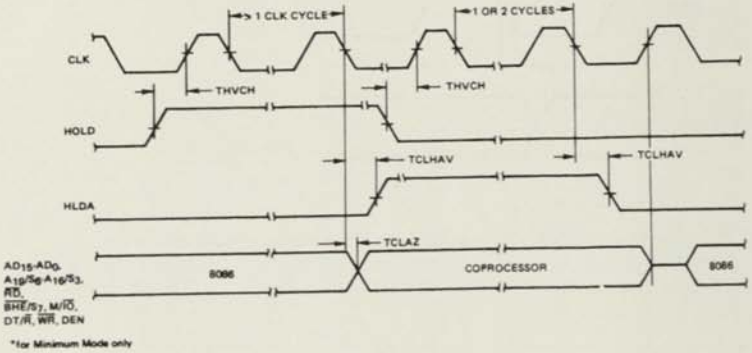
REQUEST/GRANT SEQUENCE TIMING*



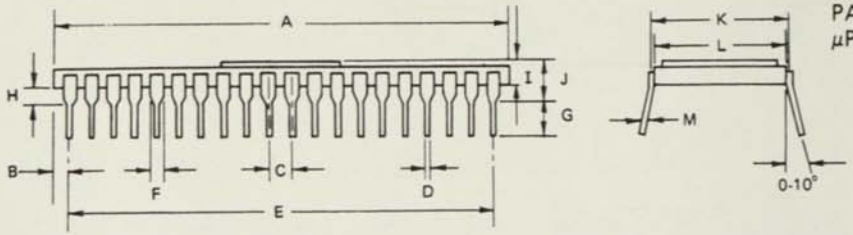
NOTE: ① The coprocessor may not drive the buses outside the region shown without risking contention.

*for Maximum Mode only

HOLD/HOLD ACKNOWLEDGE TIMING*



PACKAGE OUTLINE μPD8086D



Cerdip

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

PROGRAMMABLE COMMUNICATION INTERFACES

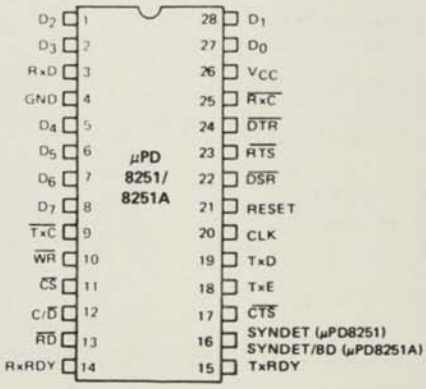
DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the 8080A or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - Five 8-Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - Five 8-Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate (1X Mode) – DC to 56K Baud (μPD8251)
  – DC to 64K Baud (μPD8251A)
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080A/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply, ± 10% (8251A) ± 5% (8251)
- Separate Device Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/$\overline{D}$	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock (TTL)
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

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NOTE: These manufacturer's specifications are provided for reference. The APC may not use some of the functions described here.

FUNCTIONAL DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operation of the μPD8251 and μPD8251A, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251 or μPD8251A converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

μPD8251A FEATURES AND ENHANCEMENTS

The μPD8251A is an advanced design of the industry standard 8251 USART. It operates with a wide range of microprocessors, including the 8080, 8085, and μPD780 (Z80™). The additional features and enhancements of the μPD8251A over the μPD8251 are listed below.

1. The data paths are double-buffered with separate I/O registers for control, status, Data In and Data Out. This feature simplifies control programming and minimizes processor overhead.
2. The Receiver detects and handles "break" automatically in asynchronous operations, which relieves the processor of this task.
3. The Receiver is prevented from starting when in "break" state by a refined Rx initialization. This also prevents a disconnected USART from causing unwanted interrupts.
4. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
5. The Tx Disable command is prevented from halting transmission by the Tx Enable Logic enhancement, until all data previously written has been transmitted. The same logic also prevents the transmitter from turning off in the middle of a word.
6. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through a flip-flop which clears itself upon a status read.
7. The possibility of a false sync detect is minimized by
   - ensuring that if a double sync character is programmed, the characters be contiguously detected.
   - clearing the Rx register to all Logic 1s (V_{OH}) whenever the Enter Hunt command is issued in Sync mode.
8. The $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device as long as the μPD8251A is not selected.
9. The μPD8251A Status can be read at any time, however, the status update will be inhibited during status read.
10. The μPD8251A has enhanced AC and DC characteristics and is free from extraneous glitches, providing higher speed and improved operating margins.
11. Baud rate from DC to 64K.

BASIC OPERATION

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	μPD8251/μPD8251A → Data Bus
0	1	0	0	Data Bus → μPD8251/μPD8251A
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

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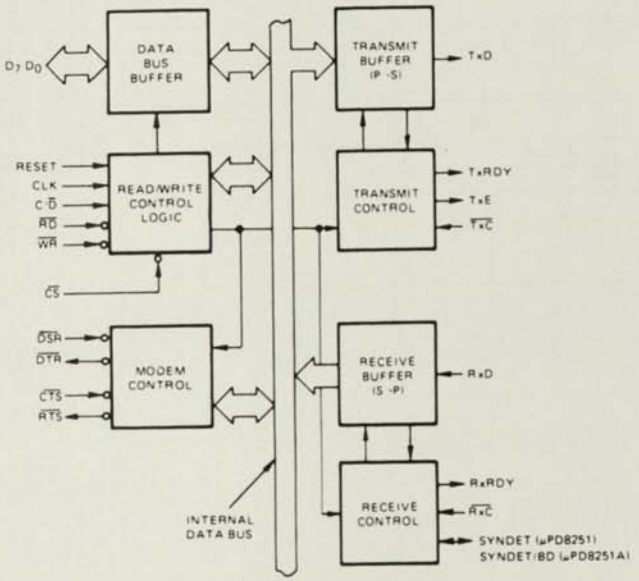
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10% for 8251A and ± 5% for 8251; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	TYP	MAX	LIMITS μPD8251A MIN	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	0.5	0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	2.2	V_{CC}	V	
Output Low Voltage	V_{OL}			0.45		0.45	V	μPD8251: I_{OL} = 1.7 mA μPD8251A: I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			2.4		V	μPD8251: I_{OH} = -100 μA μPD8251A: I_{OH} = -400 μA
Data Bus Leakage	I_{DL}			-50		-10	μA	V_{OUT} = 0.45V
				10		10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10		10	μA	At 5.5V
Power Supply Current	I_{CC}		45	80		100	mA	μPD8251A: All Outputs = Logic 1

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5.0V ± 10% for 8251A; GND = 0V, V_{CC} = 5.0V ± 5% for 8251

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	LIMITS μPD8251 MAX	LIMITS μPD8251A MIN	LIMITS μPD8251A MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before READ (CS, C/D)	t_{AR}	50		50		ns	
Address Hold Time for READ (CS, C/D)	t_{RA}	5		50		ns	
READ Pulse Width	t_{RR}	430		250		ns	
Data Delay from READ	t_{RD}		350		250	ns	μPD8251 C_L = 100 pF μPD8251A C_L = 150 pF
READ to Data Floating	t_{DF}	25	200	10	100	ns	μPD8251 C_L = 100 pF C_L = 15 pF
WRITE							
Address Stable before WRITE	t_{AW}	20		50		ns	
Address Hold Time for WRITE	t_{WA}	20		50		ns	
WRITE Pulse Width	t_{WW}	400		250		ns	
Data Set Up Time for WRITE	t_{DW}	200		150		ns	
Data Hold Time for WRITE	t_{WD}	40		30		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0.420	1.35	0.32	1.35	μs	
Clock Pulse Width High	t_{pW}	220	0.7 t_{CY}	140	t_{CY} 90	ns	
Clock Pulse Width Low	t_{pW}			90		ns	
Clock Rise and Fall Time	$t_{R,F}$	0	50	5	20	ns	
TxD Delay from Falling Edge of TxC	t_{DT_x}		1		1	μs	
Rx Data Set Up Time to Sampling Pulse	t_{SR_x}	2		2		μs	μPD8251 C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HR_x}	2		2		μs	
Transmitter Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	t_{T_x}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	12 1		12 1		t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	15 3		15 3		t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	t_{R_x}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	12 1		12 1		t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	15 3		15 3		t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{T_x}		16		8	t_{CY}	μPD8251 C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{R_x}		20		24	t_{CY}	
Internal SYNDET Delay from Center of Data Bit	t_{IS}		25		24	t_{CY}	
External SYNDET Set Up Time before Falling Edge of RxC	t_{ES}	16		16		t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}		16		20	t_{CY}	μPD8251 C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, DTR, RTS)	t_{WC}		16		8	t_{CY}	
Control to READ Set Up Time (DSR, CTS)	t_{CR}	16		20		t_{CY}	

Notes ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8 and with load circuit of Figure 1

② This recovery time is for initialization only; when MODE, SYNC1, SYNC2 COMMAND and first DATA BYTE are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1

③ The TxC and RxC frequencies have the following limitations with respect to CLK
For 1X Baud Rate, t_{T_x} or $t_{R_x} \leq 1/30\ t_{CY}$
For 16X and 64X Baud Rate t_{TX} or $t_{R_x} \leq 1/4.5\ t_{CY}$

④ Reset Pulse Width = 6 t_{CY} minimum

⑤ $T_{TxRDYCLR} = 2T_{CY} + T_D + T_R + 200ns$

⑥ $T_{RxRDYCLR} = 2T_{CY} + T_D + T_R + 170ns$

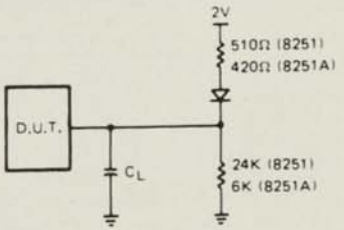
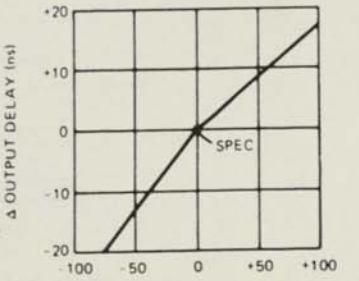
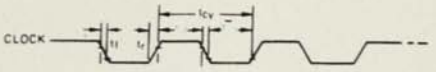


Figure 1.

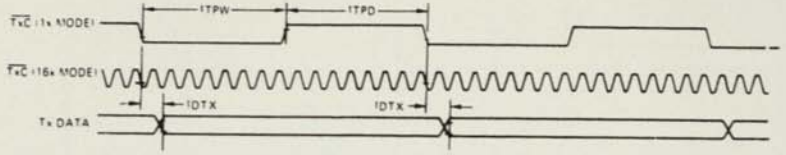
TEST LOAD CIRCUIT



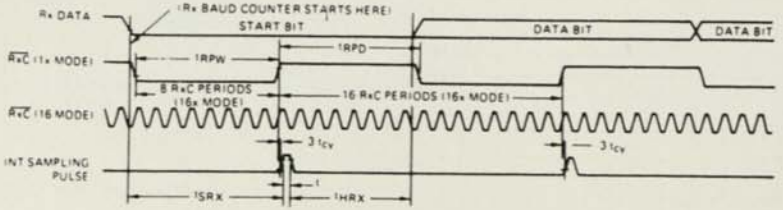
Typical Δ Output
Delay Versus Δ Capacitance (pF)



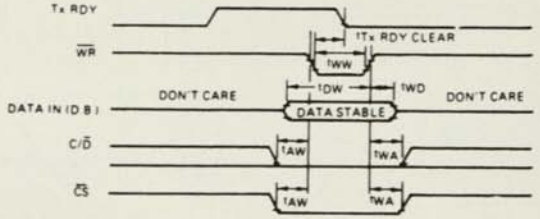
SYSTEM CLOCK INPUT



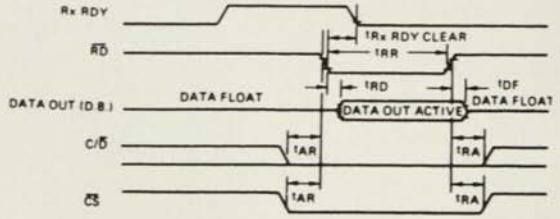
TRANSMITTER CLOCK AND DATA



RECEIVER CLOCK AND DATA

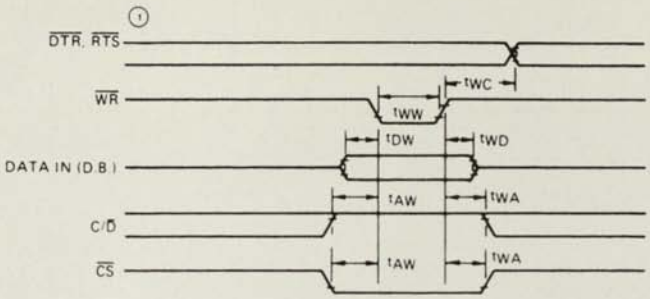


WRITE DATA CYCLE (PROCESSOR → USART)

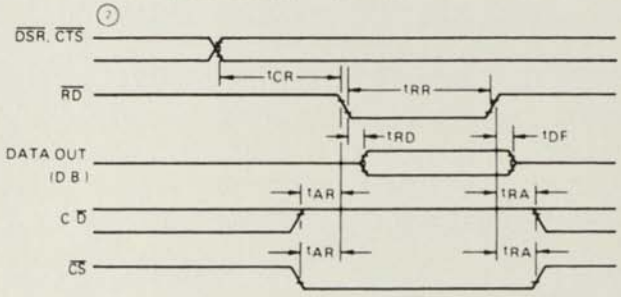


READ DATA CYCLE (PROCESSOR ← USART)

TIMING WAVEFORMS
(CONT.)



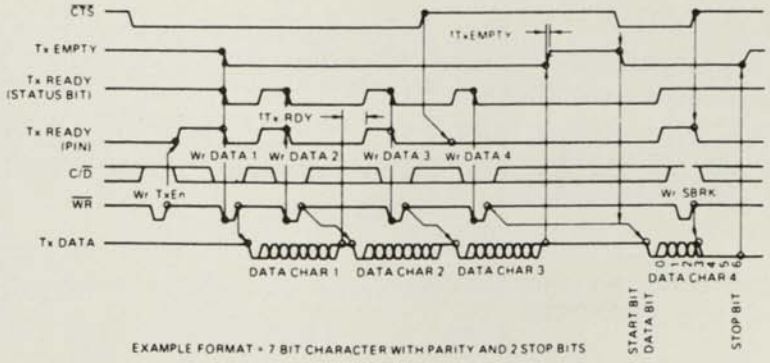
WRITE CONTROL OR OUTPUT PORT CYCLE
(PROCESSOR → USART)



READ CONTROL OR INPUT PORT CYCLE
(PROCESSOR ← USART)

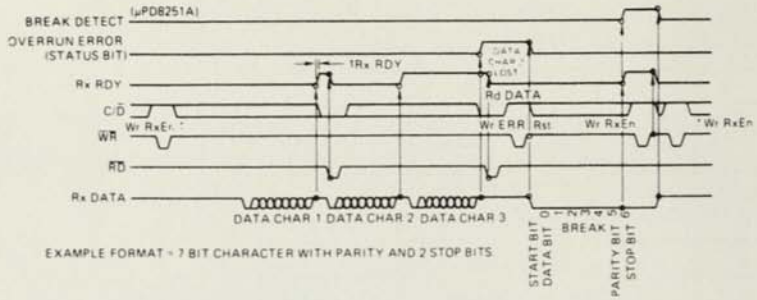
NOTES: ① T_{WC} includes the response timing of a control byte

② T_{CR} includes the effect of CTS on the TxENBL circuitry



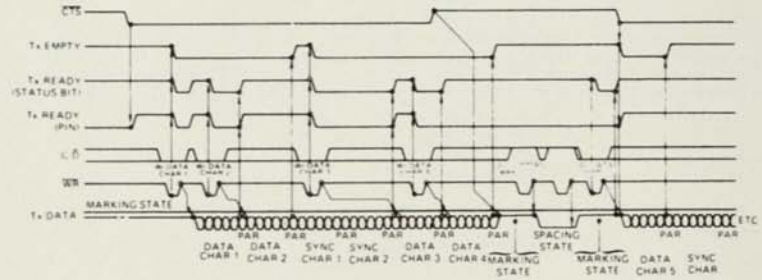
TRANSMITTER CONTROL AND FLAG TIMING
(ASYNC MODE)

TIMING WAVEFORMS (CONT.)



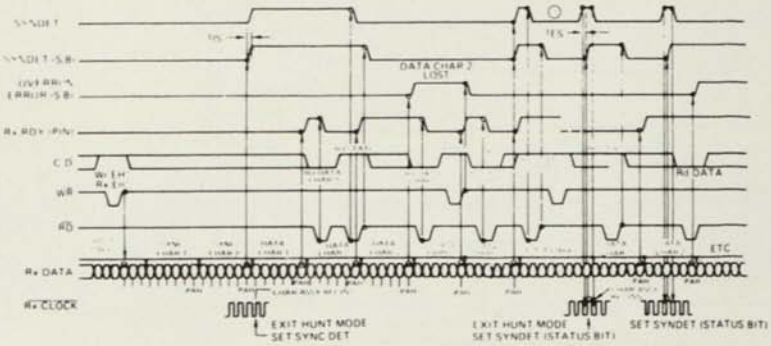
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS

RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY AND 2 SYNC CHARACTERS

TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)

Notes: ① Internal sync, 2 sync characters, 5 bits, with parity.
② External sync, 5 bits, with parity.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is 6 t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the USART to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data, 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART to read from or write to the processor.
Modem Control			The μPD8251 and μPD8251A have a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

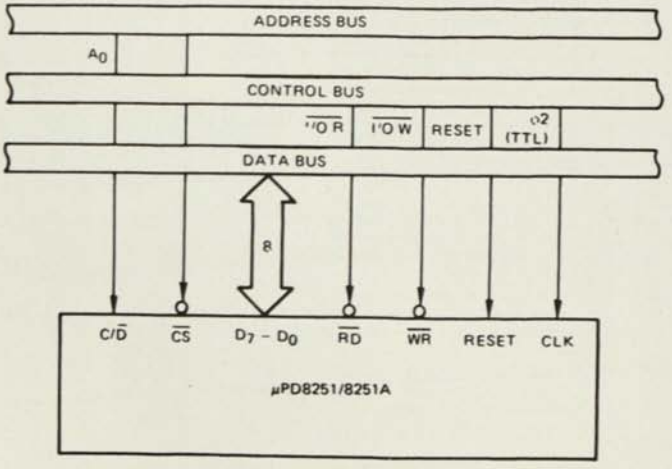
TRANSMIT BUFFER

The Transmit Buffer receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251 AND μPD8251A INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVE BUFFER

The Receive Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 and μPD8251A set the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
	Receiver Control Logic		This block manages all activities related to incoming data
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock determines the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 and μPD8251A on the rising edge of $\overline{RxC}$ ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.
16	SYNDET BD (μPD8251A)	Sync Detect Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high which all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note ① Since the μPD8251 and μPD8251A will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples

If the Baud Rate equals 110 (Async)
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300
$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 and μPD8251A to define the desired mode and communications format. The control words will specify the BAUD rate factor (1x, 16x, 64x), character length (5 to 8), number of STOP bits (1, 1-1/2, 2) Asynchronous or Synchronous mode, SYNDET (IN or OUT), parity, etc.

After receiving the control words, the μPD8251 and μPD8251A are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 and μPD8251A may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 and μPD8251A may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 and μPD8251A cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new control words.

USART PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A RESET (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251 and μPD8251A.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

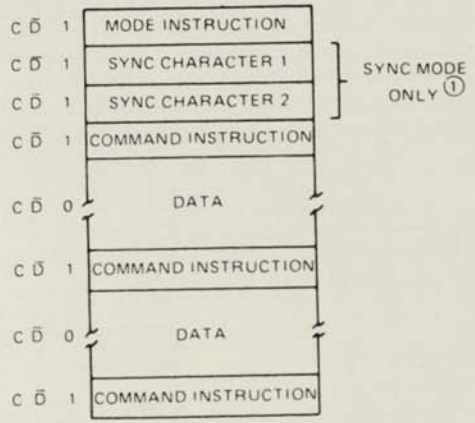
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the Synchronous or Asynchronous mode, BAUD rate factor, character length, parity, and number of stop bits. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the μPD8251 and μPD8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251 and μPD8251A to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 and μPD8251A can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components (one asynchronous and the other synchronous) which share the same support circuits and package. Although the format definition can be changed at will or "on the fly," the two modes will be explained separately for clarity.

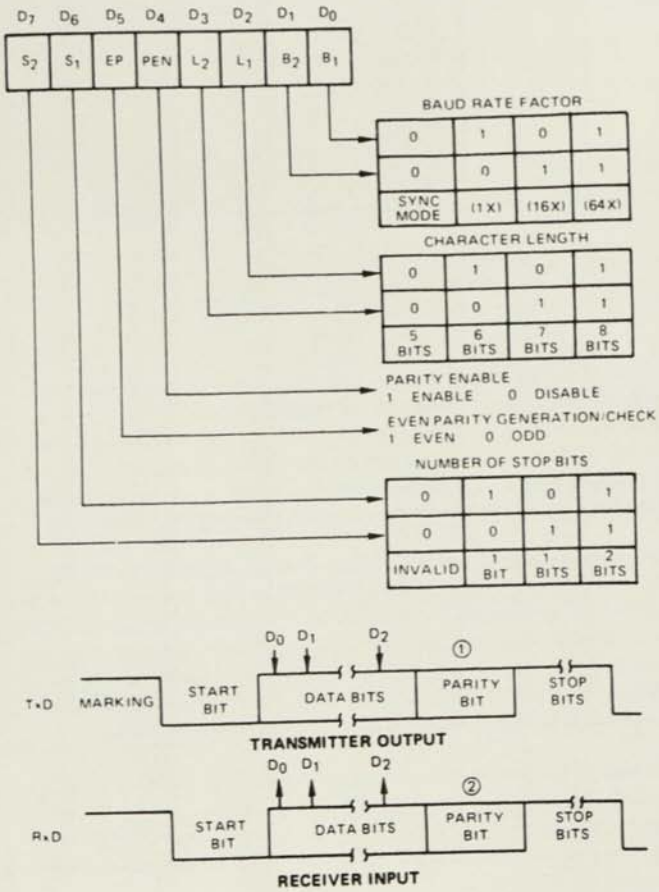
ASYNCHRONOUS TRANSMISSION

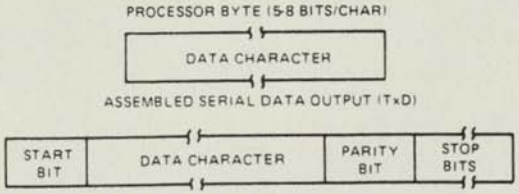
When a data character is written into the μPD8251 and μPD8251A, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of TxC at TxC, TxC/16 or TxC/64, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251 and μPD8251A, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

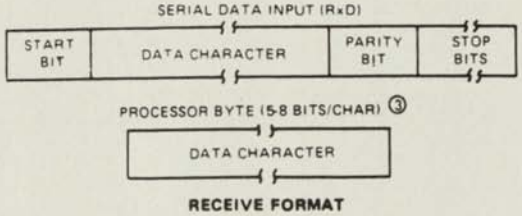
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and μPD8251A and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.





TRANSMISSION FORMAT



RECEIVE FORMAT

Notes ① Generated by μPD8251/8251A
② Does not appear on the Data Bus.
③ If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero."

SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 and μPD8251A receive the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 and μPD8251A Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 and μPD8251A become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

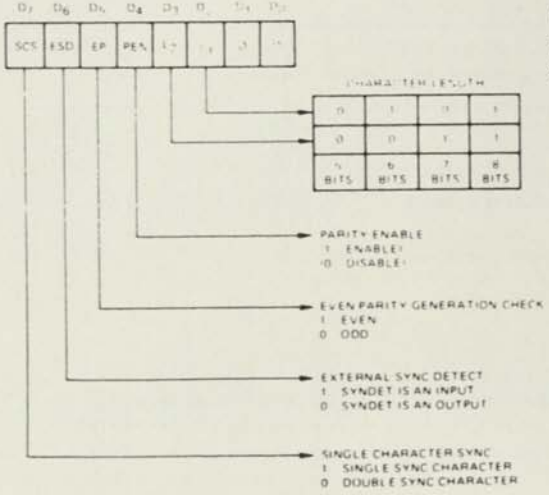
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receive Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 and μPD8251A leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

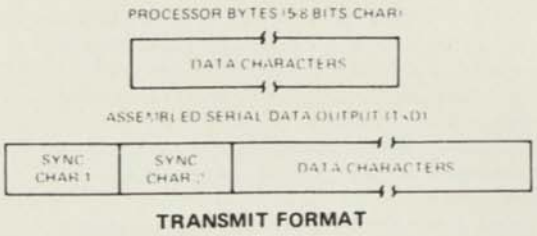
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

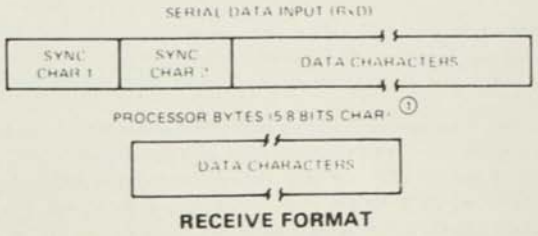
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Note: ① If character length is defined as 5, 6 or 7 bits, the unused bits are set to "zero."

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 and μPD8251A has been specified by the Mode Instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 and μPD8251A to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251 and μPD8251A have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 and μPD8251A to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of 16 clock periods in the μPD8251 and 28 clock periods in the μPD8251A.

PARITY ERROR

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

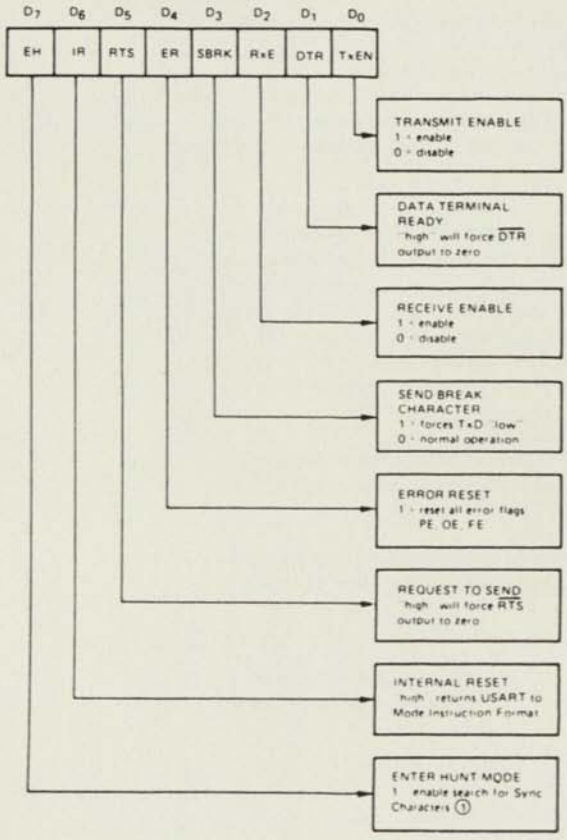
If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

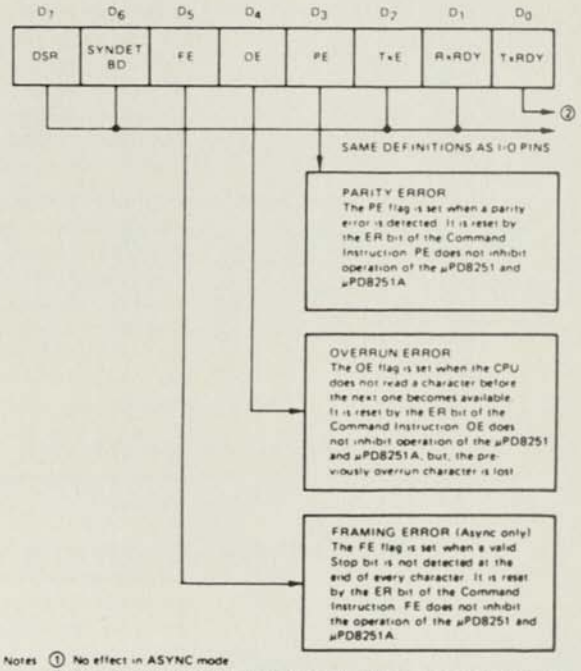
If a valid STOP bit is not detected at the end of a character, the FE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



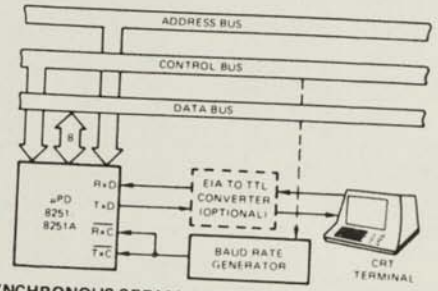
Notes (1) No effect in ASYNC mode.

(2) TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

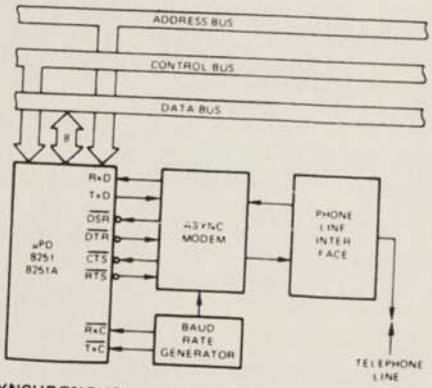
TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • $\overline{CTS}$ • TxEn

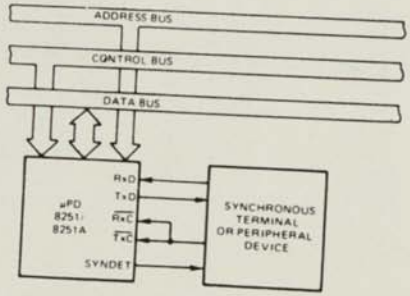
APPLICATION OF THE μPD8251 AND μPD8251A



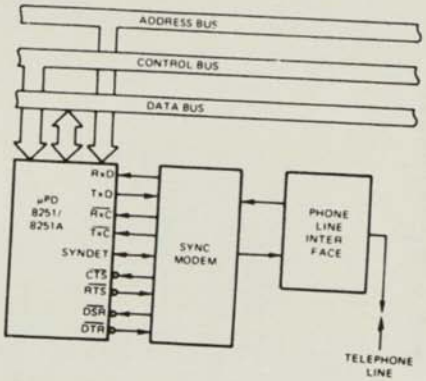
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

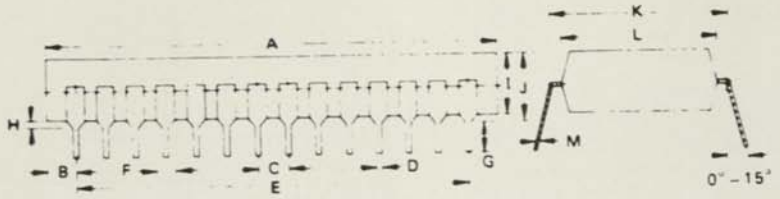


SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

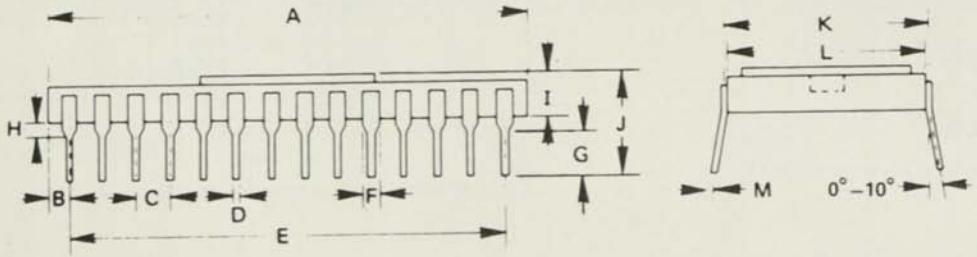
PACKAGE OUTLINES
μPD8251C
μPD8251AC



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

μPD8251D
μPD8251AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002

SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

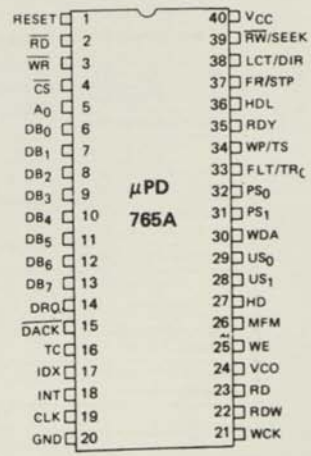
Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability – Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

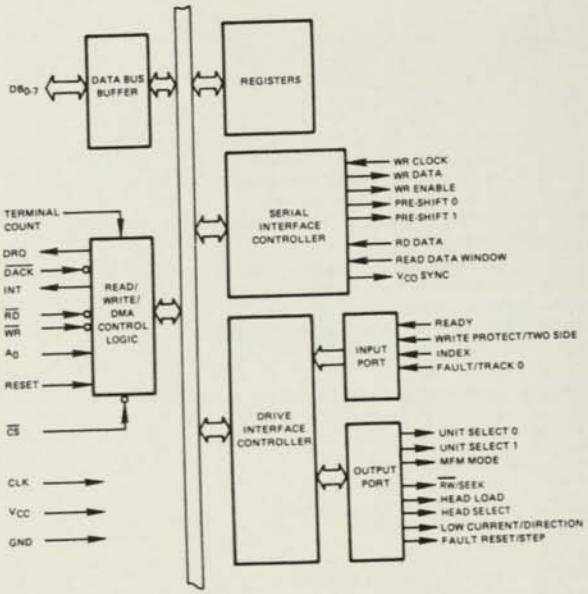
PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

NOTE: These manufacturer's specifications are provided for reference. The APC may not use some of the functions described here.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-55°C to +150°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Power Dissipation	1 Watt

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -200 µA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	µA	V_{IN} = V_{CC}
				-10	µA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	µA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	µA	V_{OUT} = +0.45V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input (1)	Processor	Control signal for transfer of data from FDC to Data Bus; when "0" (low).
3	$\overline{WR}$	Write	Input (1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and WR to be enabled.
5	A_0	Data/Status Reg Select	Input (1)	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/ Output (1)	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1."
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high). Head 0 selected when "0" (low).
28,29	US_1,US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1,PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when CS = 1.

AC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Clock Period	Φ_{CY}	120	125	500	ns	
Clock Active (High, Low)	Φ_0	40			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pf
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			µs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	1			ΦCY	
Reset Width	T_{RST}	14			ΦCY	
WCK Cycle Time	T_{CY}		2 or 4② 1 or 2		µs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	80	250	350	ns	
WCK Rise Time	T_r			20	ns	
WCK Fall Time	T_f			20	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		100	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		100	ns	
RDD Active Time (High)	T_{RDD}	40			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		µs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	15			ns	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			µs	8 MHz Clock Period
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			µs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			µs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	5.0			µs	
STEP Active Time (High)	T_{STP}	6.0	7.0		µs	
STEP Cycle Time	T_{SC}	33	③	③	µs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	µs	
Write Data Width	T_{WDD}	T_0-50			ns	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			µs	8 MHz Clock Period
Seek Hold Time from DIR	T_{DS}	30			µs	
DIR Hold Time after STEP	T_{STD}	24			µs	
Index Pulse Width	T_{IDX}	10			ΦCY	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	8 MHz Clock Period
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	µs	

Notes: ① Typical values for T_a = 25°C and nominal supply voltage.
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.
③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.
④ For mini-floppy applications, Φ_{CY} must be 4 mHz.

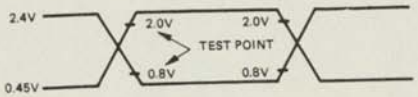
CAPACITANCE

$T_a = 25°C$; $f_c = 1$ MHz; $V_{CC} = 0V$

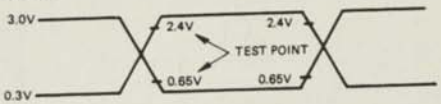
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Input Capacitance	$C_{IN(\Phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC TEST CONDITION

INPUT/OUTPUT



CLOCK



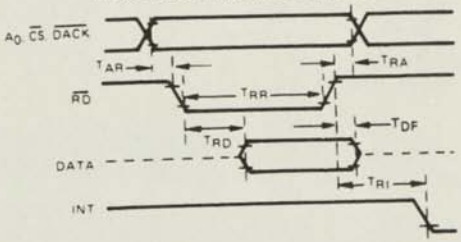
AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

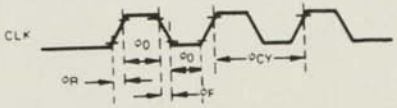
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

TIMING WAVEFORMS

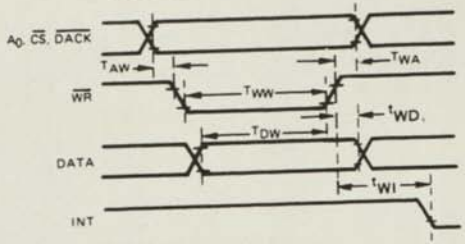
PROCESSOR READ OPERATION



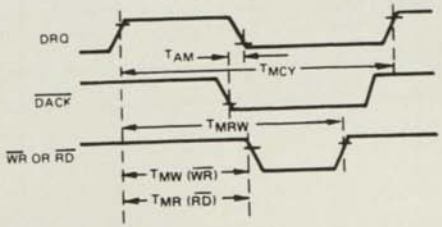
CLOCK



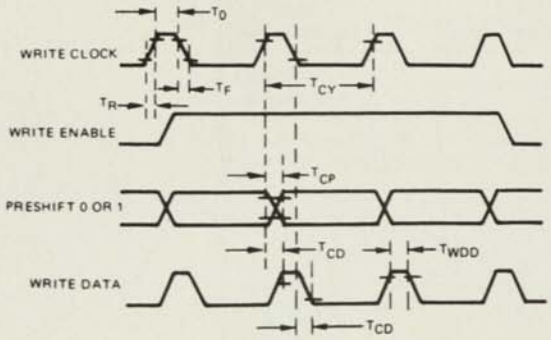
PROCESSOR WRITE OPERATION



DMA OPERATION

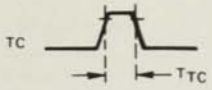


FDD WRITE OPERATION

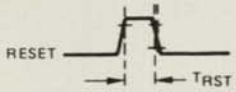


	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

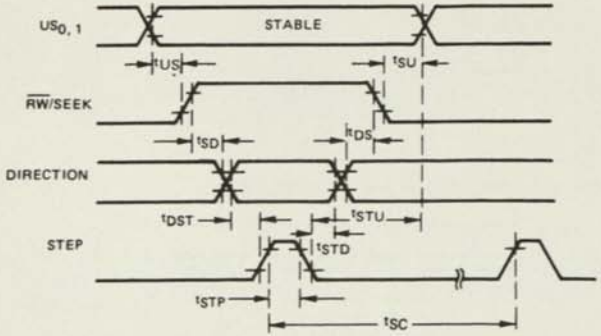
TERMINAL COUNT



RESET

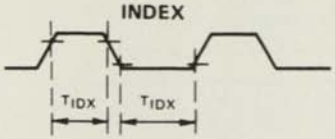


SEEK OPERATION

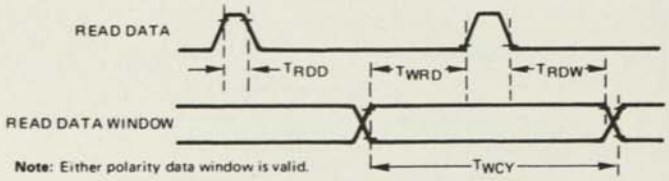


FLT RESET

INDEX



FDD READ OPERATION



Note: Either polarity data window is valid.

INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

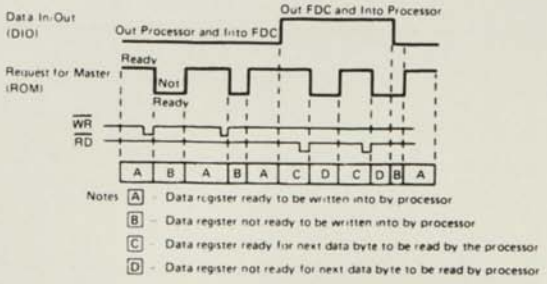
A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



Notes
- A – Data register ready to be written into by processor
- B – Data register not ready to be written into by processor
- C – Data register ready for next data byte to be read by the processor
- D – Data register not ready for next data byte to be read by processor

COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

- Command Phase: The FDC receives all information required to perform a particular operation from the processor.
- Execution Phase: The FDC performs the operation it was instructed to do.
- Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

INSTRUCTION SET

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior Command execution
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior Command execution
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———			STO				———	Status information at the end of seek-operation about the FDC
	R	———			PCN				———	
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	———	SRT		◄				HUT ———	
	W	———	HLT					►	ND	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	———			ST 3				———	Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			NCN				———	
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	———			Invalid Codes				———	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	———			ST 0				———	ST 0 = 80 (16)

INSTRUCTION SET ① ② (CONT.)

READ DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data-transfer between the FDD and main system
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data-transfer between the FDD and main system
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data-transfer between the main-system and FDD
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DELETED DATA

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data-transfer between the FDD and main system
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data-transfer between the FDD and main system. FDC reads all data fields from index hole to EOT
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ ID

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information read during Execution Phase from Floppy Disk
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

FORMAT A TRACK

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— N ———								Bytes/Sector
	W	——— SC ———								Sectors/Track
	W	——— GPL ———								Gap 3
	W	——— D ———								Filler Byte
Execution										FDC formats an entire track
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								In this case, the ID information has no meaning
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

SCAN EQUAL

PHASE	R/W	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— STP ———								
Execution										Data compared between the FDD and main system
Result	R	——— ST 0 ———								Status information after Command execution
	R	——— ST 1 ———								
	R	——— ST 2 ———								
	R	——— C ———								Sector ID information after Command execution
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

Note: ① Symbols used in this table are described at the end of this section.

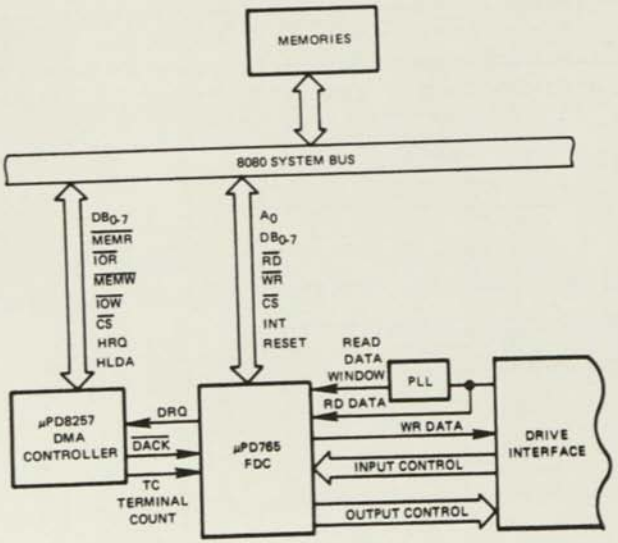
② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.

SYSTEM CONFIGURATION



COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

POLLING FEATURE OF THE μPD765

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.

After the Specify command has been sent to the μPD765, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the μPD765 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the μPD765 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

FUNCTIONAL DESCRIPTION OF COMMANDS

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.
The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM Mode, and every 13 µs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes.

	8" STANDARD FLOPPY					5¼" MINI FLOPPY				
FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	SECTOR SIZE	N	SC	GPL ①	GPL ②
FM Mode	128 bytes/Sector	00	1A	07	1B	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A	128	00	10	10	19
	512	02	08	1B	3A	256	01	08	18	30
	1024 bytes/Sector	03	04	47	8A	512	02	04	46	87
	2048	04	02	C8	FF	1024	03	02	C8	FF
	4096	05	01	C8	FF	2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	256	01	12	0A	0C
	512	02	0F	1B	54	256	01	10	20	32
	1024	03	08	35	74	512	02	08	2A	50
	2048	04	04	99	FF	1024	03	04	80	F0
	4096	05	02	C8	FF	2048	04	02	C8	FF
	8192	06	01	C8	FF	4096	05	01	C8	FF

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

③ In MFM mode FDC can not perform a read/write/format operation with 128 bytes/sector. (N = 00)

④ All the values are hexidecimal.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} < D_{Processor}$, or $D_{FDD} > D_{Processor}$. The hexidicemial byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regarus the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head

position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the μPD765 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find a 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (CONT.)

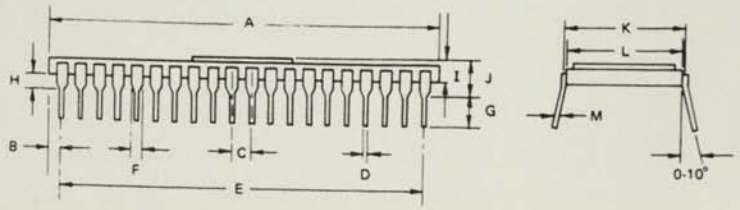
BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

It is suggested that you utilize the following applications notes:

① #8 – for an example of an actual interface, as well as a "theoretical" data separator.

② #10 – for a well documented example of a working phase lock loop.

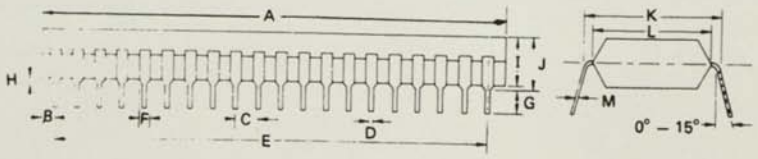
PACKAGE OUTLINE μPD765AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

PACKAGE OUTLINE μPD765AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 · 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

PRELIMINARY

GRAPHICS DISPLAY CONTROLLER

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

Features

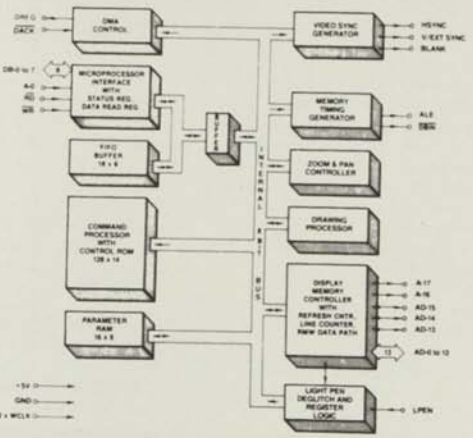
- ☐ Microprocessor Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM reresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode:
  - Four megabit, bit-mapped display memory
- ☐ Character Mode:
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Characters Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities:
  - Figure drawing of lines, arc/circles, rectangles, and graphics character in 800ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale.
  - Two independently scrollable areas
- ☐ Character Capabilities:
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5 volt, NMOS, 40-pin DIP
- ☐ DMA Capability:
  - Bytes or word transfers
  - 4 clock periods per byte transferred

System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

GDC Components

The GDC block diagram illustrates how these tasks are accomplished.



Microprocessor Bus Interface

Control of the GDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destina-

NOTE: These manufacturer's specifications are provided for reference. The APC may not use some of the functions described here.

tions within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control
The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM
The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator
Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator
The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's ALE and $\overline{\text{DBIN}}$ outputs.

Zoom & Pan Controller
Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independent of the other display areas.

Drawing Processor
The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing processor needs no further assistance to complete the figure drawing.

Display Memory Controller
The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher
Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC
The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	STATUS REGISTER	PARAMETER INTO FIFO
1	FIFO READ	COMMAND INTO FIFO

GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacts the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

GDC Command Summary

Video Control Commands
1. RESET: Resets the GDC to its idle state.
2. SYNC: Specifies the video display format.
3. VSYNC: Selects master or slave video synchronization mode.
4. CCHAR: Specifies the cursor and character row heights.

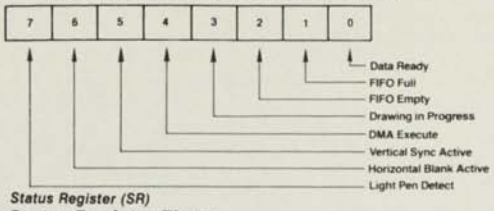
Display Control Commands
1. START: Ends Idle mode and unblanks the display.
2. BCTRL: Controls the blanking and unblanking of the display.
3. ZOOM: Specifies zoom factors for the display and graphics characters writing.
4. CURS: Sets the position of the cursor in display memory.
5. PRAM: Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
6. PITCH: Specifies the width of the X dimension of display memory.

Drawing Control Commands
1. WDAT: Writes data words or bytes into display memory.
2. MASK: Sets the mask register contents.
3. FIGS: Specifies the parameters for the drawing processor.
4. FIGD: Draws the figure as specified above.
5. GCHRD: Draws the graphics character into display memory.

Data Read Commands
1. RDAT: Reads data words or bytes from display memory.
2. CURD: Reads the cursor position.
3. LPRD: Reads the light pen address.

DMA Control Commands

1. DMAR: Requests a DMA read transfer.
2. DMAW: Requests a DMA write transfer.



Status Register (SR)

Status Register Flags

SR-7: Light Pen Detect
When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active
A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync
Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute
This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress
While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty
This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

SR-1: FIFO Full
A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready
When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires the differentiation of the first byte of a command sequence from the succeeding bytes. This first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT command or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

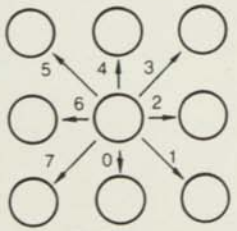
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the modify data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHz, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

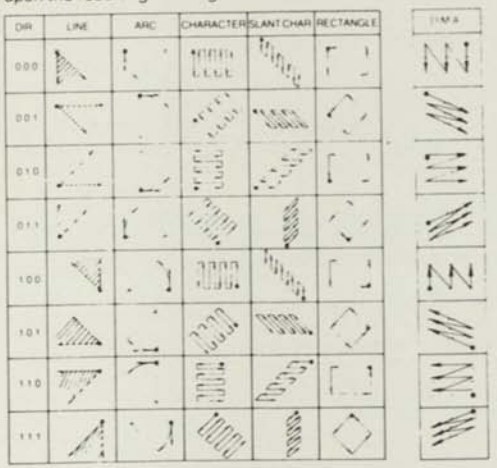
The table below summarizes these operations for each direction.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the

DIR	OPERATIONS TO ADDRESS THE NEXT PIXEL
000	EAD - P → EAD
001	EAD - P → EAD dAD (MSB) 1 EAD - 1 → EAD dAD → LR
010	dAD (MSB) 1 EAD - 1 → EAD dAD → LR
011	EAD P → EAD dAD (MSB) 1 EAD - 1 → EAD dAD → LR
100	EAD P → EAD
101	EAD P → EAD dAD (LSB) 1 EAD 1 → EAD dAD → RR
110	dAD (LSB) 1 EAD - 1 → EAD dAD → RR
111	EAD - P → EAD dAD (LSB) 1 EAD - 1 → EAD dAD → RR

dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the GDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Processor coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

DRAWING TYPE	DC	D	D2	D1	DM
Initial Value*	0	B	B	−1	−1
Line	|Δl|	2(|ΔD| − |Δl|)	2(|ΔD| − |Δl|)	2|ΔD|	—
Arc**	r sin 0°	r−1	2(r−1)	−1	rsin θ
Rectangle	3	A−1	B−1	−1	A−1
Area Fill	B−1	A	A	—	—
Graphic Character***	B−1	A	A	—	—
Read & Write Data	W−1	—	—	—	—
DMAW	D−1	C−1	—	—	—
DMAR	D−1	C−1	(C−1)/2+	—	—

* Initial values for the various parameters are loaded during the handling of the FIGS op code byte.

** Circles are drawn with 8 arcs, each of which span 45°, so that sin 0 = 1/√2 and sin θ = 0.

*** Graphic characters are a special case of bit-map area filling in which B and A ≤ 8. If A = 8 there is no need to load D and D2.

Where:

−1 = all ONES value.

All numbers are shown in base 10 for convenience. The GDC accepts base 2 numbers (2s complement notation where appropriate).

– = No parameter bytes sent to GDC for this parameter.

Δl = The larger at Δx or Δy.

ΔD = The smaller at Δx or Δy.

r = Radius at curvature, in pixels.

ϕ = Angle from major axis to end at the arc. ϕ ≤ 45°.

θ = Angle from major axis to start at the arc. θ ≤ 45°.

↑ = Round up to the next higher integer.

↓ = Round down to the next lower integer.

A = Number of pixels in the initially specified direction.

B = Number of pixels in the direction at right angles to the initially specified direction.

W = Number of words to be accessed.

C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected).

D = Number of words to be accessed in the direction at right angles to the initially specified direction.

DC = Drawing count parameter which is one less than the number of RMW cycles to be executed.

DM = Dots masked from drawing during arc drawing.

\+ = Needed only for word reads.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The GDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the GDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA 0 to 15

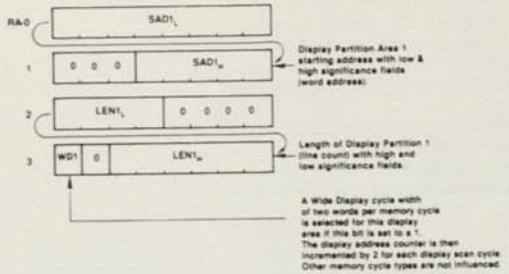
The parameters stored in the parameter RAM, PRAM, are available for the GDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the GDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

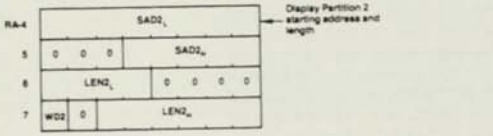
The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

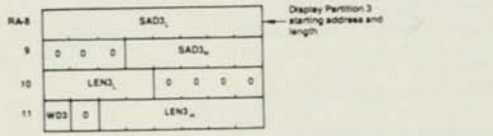
The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the GDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

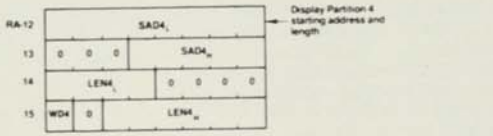
Details of the bit assignments are shown on the following pages for the various modes of operation.

Character Mode

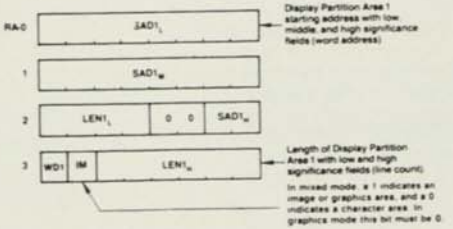


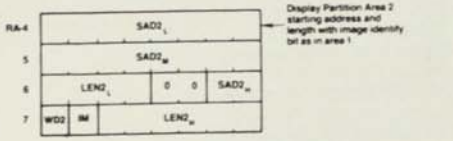


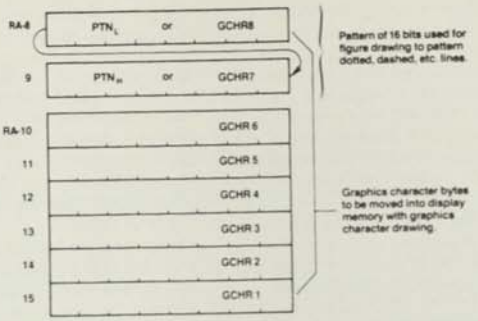




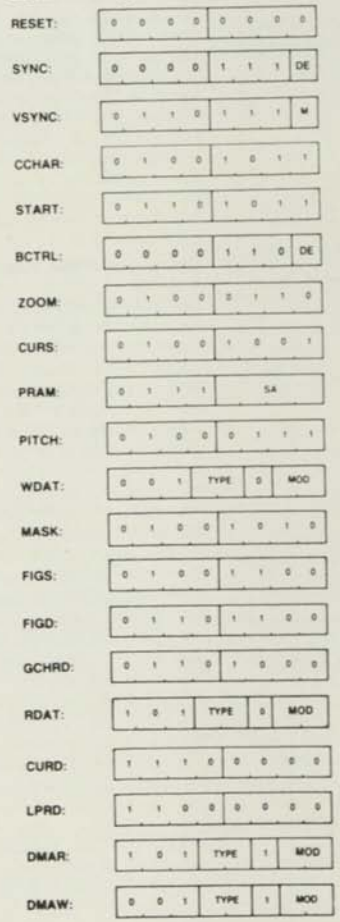
Graphics and Mixed Graphics and Character Modes





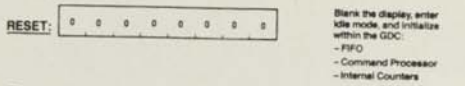


Command Bytes Summary



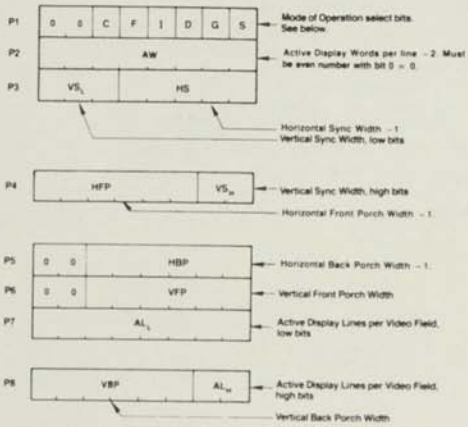
Video Control Commands

Reset



This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below.
Idle mode is exited with the START command.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any.
The number of active words per line must be an even number from 2 to 256.
An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters.
All horizontal widths are counted in display words.
All vertical intervals are counted in lines.

SYNC Generator Period Constraints

Horizontal Back Porch Constraints

1. In general:
   HBP ≥ 3 Display Word Cycles (6 clock cycles).
2. If the IMAGE or WD modes change within one video field:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. If the display ZOOM function is used at other than 1X:
   HFP ≥ 2 Display Word Cycles (4 clock cycles).
2. If the GDC is used in the video sync Slave mode:
   HFP ≥ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ≥ 6 Display Word Cycles (12 clock cycles).

Horizontal SYNC Constraints

1. If Interlaced display mode is used:
   HS ≥ 3 Display Word Cycles (6 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Noninterlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.
Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.
Noninterlaced Framing: 1 field brings all of the information to the screen.

Total scanned lines in interlace mode is odd. The sum of VFP + VS + VBP + AL should equal one less than the desired odd number of lines.

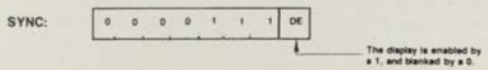
D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

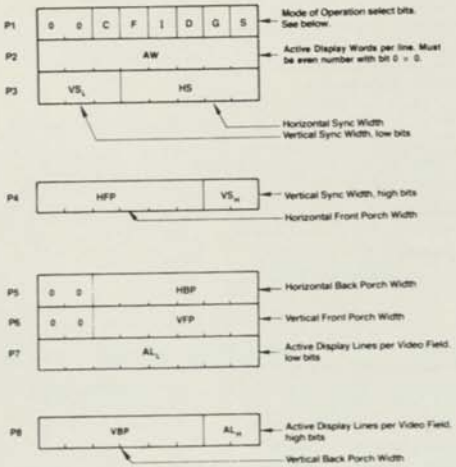
Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

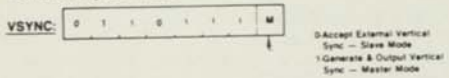
SYNC Format Specify





This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The GDC is not reset nor does it enter idle mode.

Vertical Sync Mode



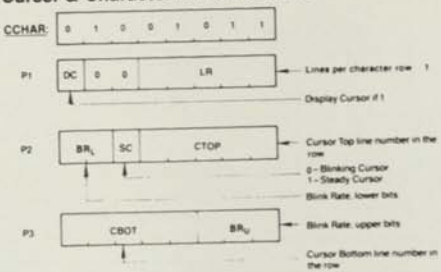
When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

Slave Mode Operation

A few considerations should be observed when synchronizing two or more GDCs to generate overlayed video via the VSYNC INPUT/OUTPUT pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave GDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave GDC to complete the operation before the start of the HSYNC interval.

Once the GDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master GDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

Cursor & Character Characteristics

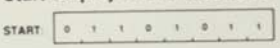


In graphics mode, LR should be set to 0.

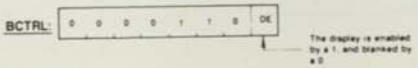
The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle.

Display Control Commands

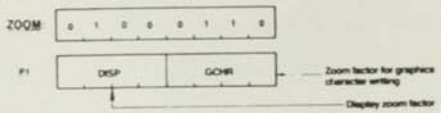
Start Display & End Idle Mode



Display Blanking Control

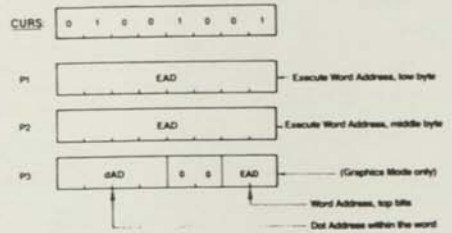


Zoom Factors Specify



Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

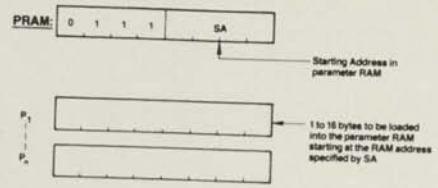
Cursor Position Specify



In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address.

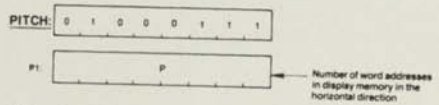
In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load



From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

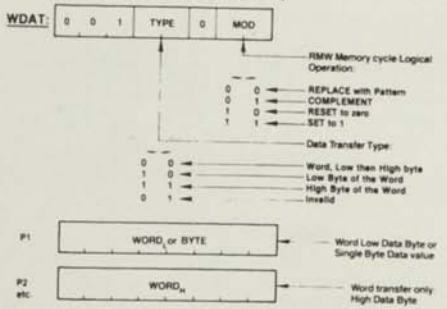


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. In situations in which these two values are equal there is no need to execute a PITCH command.

Drawing Control Commands

Write Data into Display Memory



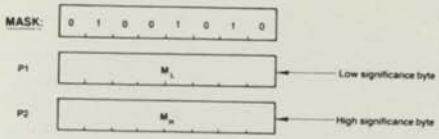
Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceeded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter + 1 will be the number of RMW cycles done by the GDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed.

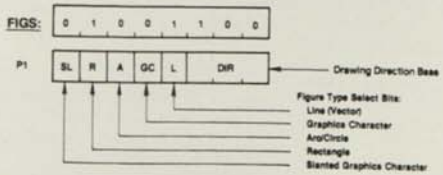
Mask Register Load

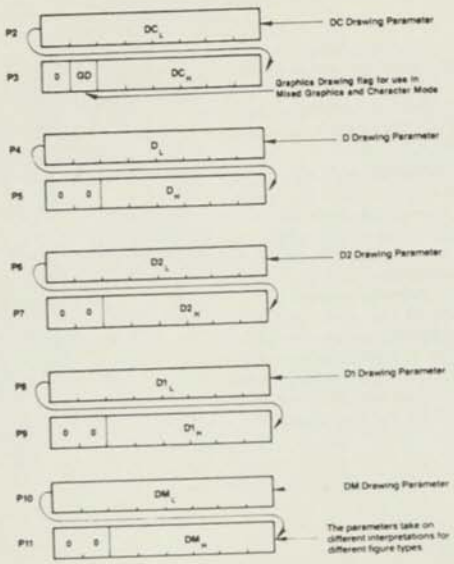


This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 of 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing opertions using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output.

Figure Drawing Parameters Specify



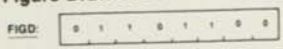


Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted graphics character drawing and slanted area filling

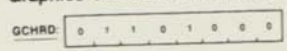
Only these bit combinations assure correct drawing operation.

Figure Draw Start



On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

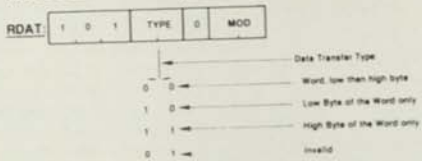
Graphics Character Draw and Area Filling Start



Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

Data Read Commands

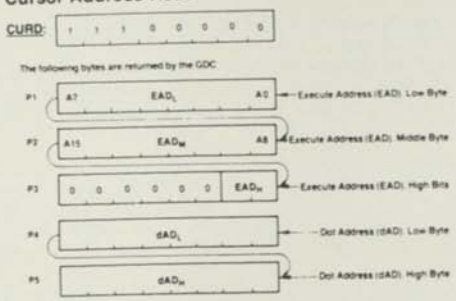
Read Data from Display Memory



Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

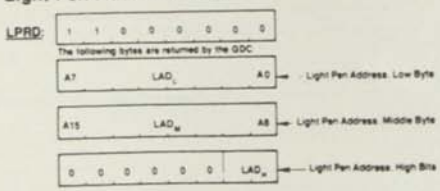
Cursor Address Read



The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

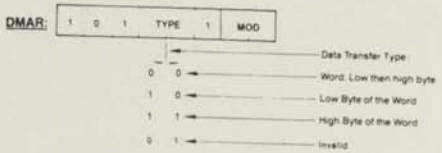
Light Pen Address Read



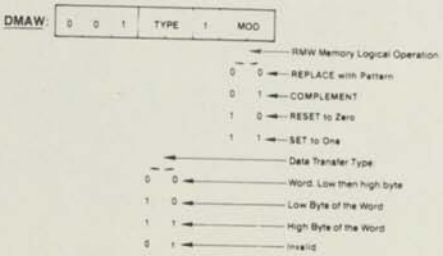
The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request



DMA Write Request



Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0 °C to 70 °C
Storage Temperature	−65 °C to 150 °C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

t_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Input Low Leak Current	I_{IL}		−10	μA	V_I = 0V
Input High Leak Current	I_{IH}		+10	μA	V_I = V_{CC}
Output Low Leak Current	I_{OL}		−10	μA	V_O = 0V
Output High Leak Current	I_{OH}		+10	μA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5	0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
V_{CC} Supply Current	I_{CC}		270		

Capacitance

t_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input Capacitance I/O Capacitance	C_{IN} C_{VO}		10 20	pF pF	fc = 1 MHz V_I (unmeasured) = 0V
Output Capacitance Clock Input Capacitance	C_{OUT} C_ϕ		20 20	pF pF	

AC Characteristics

t_A = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Read Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AR}	Address Setup to $\overline{RD}$↓	0		ns	
t_{RA}	Address Hold from $\overline{RD}$↑	0		ns	
t_{RR1}	$\overline{PD}$ Pulse Width	t_{RD1} + 20	80	ns	
t_{RD1}	Data Delay from $\overline{RD}$↓		80	ns	C_L = 50 pF
t_{DF}	Data Floating from $\overline{RD}$↑	0	100	ns	
t_{RCY}	$\overline{RD}$ Pulse Cycle	4 t_{CLK}		ns	

Write Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AW}	Address Setup to $\overline{WR}$↓	0		ns	
t_{WA}	Address Hold from $\overline{WR}$↑	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup to $\overline{WR}$↑	80		ns	
t_{WD}	Data Hold from $\overline{WR}$↑	0		ns	
t_{WCY}	$\overline{WR}$ Pulse Cycle	4 t_{CLK}		ns	

DMA Read Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{KR}	$\overline{DACK}$ Setup to $\overline{RD}$↓	0		ns	
t_{RK}	$\overline{DACK}$ Hold from $\overline{RD}$↑	0		ns	
t_{RR2}	$\overline{RD}$ Pulse Width	t_{RD2} + 20		ns	
t_{RD2}	Data Delay from $\overline{RD}$↓		1.5 t_{CLK} + 80	ns	C_L = 50 pF
t_{REQ}	DREQ Delay from 2XCCLK↑		120	ns	C_L = 50 pF
t_{QK}	DREQ Setup to $\overline{DACK}$↓	0		ns	
t_{DK}	$\overline{DACK}$ High Level Width	t_{CLK}		ns	
t_E	$\overline{DACK}$ Pulse Cycle	4 t_{CLK}		ns	
$t_{KQ(R)}$	DREQ ↓ Delay from $\overline{DACK}$↓		2 t_{CLK} + 120	ns	C_L = 50 pF

DMA Write Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{KW}	$\overline{DACK}$ Setup to $\overline{WR}$↓	0		ns	
t_{WK}	$\overline{DACK}$ Hold from $\overline{WR}$↑	0		ns	
$t_{KQ(R)}$	DREQ ↓ Delay from $\overline{DACK}$↓		t_{CLK} + 120	ns	C_L = 50 pF

R/M/W Cycle (GDC ↔ Display Memory)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AD}	Address/Data Delay from 2XCCLK↑		130	ns	C_L = 50 pF
t_{OFF}	Address/Data Floating from 2XCCLK↑	10	130	ns	C_L = 50 pF
t_{DIS}	Input Data Setup to 2XCCLK↓	40		ns	
t_{DIH}	Input Data Hold from 2XCCLK↓	0		ns	
t_{DBI}	DBIN Delay from 2XCCLK↓		90	ns	C_L = 50 pF
t_{RR}	ALE↑ Delay from 2XCCLK↑	30	110	ns	C_L = 50pF
t_{RF}	ALE↓ Delay from 2XCCLK↓	20	90	ns	C_L = 50 pF
t_{RW}	ALE Width	1/3 t_{CLK}		ns	C_L = 50 pF

Display Cycle (GDC ↔ Display Memory)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{VD}	Video Signal Delay from 2XCCLK↑		120	ns	C_L = 50 pF

Input Cycle (GDC ↔ Display Memory)

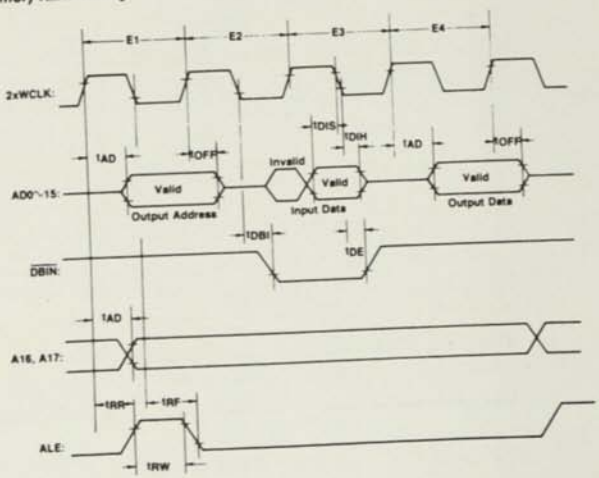
Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{PS}	Input Signal Setup to 2XCCLK↑	20		ns	
t_{PW}	Input Signal Width	t_{CLK}		ns	

Clock

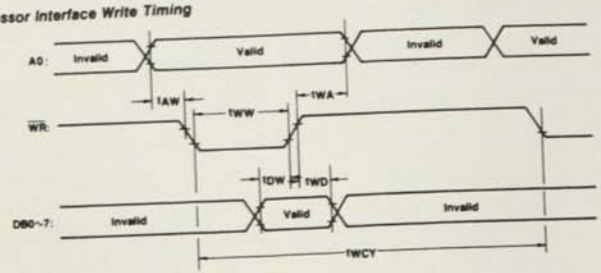
Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{CR}	Clock Rise Time		10	ns	
t_{CF}	Clock Fall Time		10	ns	
t_{CH}	Clock High Pulse Width	95		ns	
t_{CL}	Clock Low Pulse Width	95		ns	
t_{CLK}	Clock Cycle	200	2000	ns	

Timing Waveforms

Display Memory RMW Timing

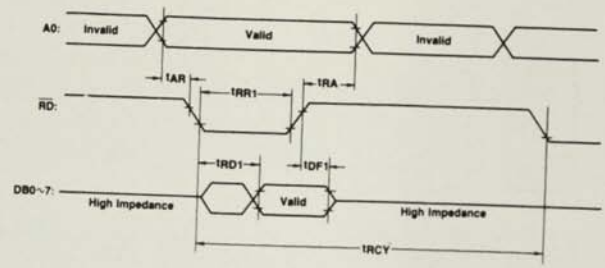


Microprocessor Interface Write Timing

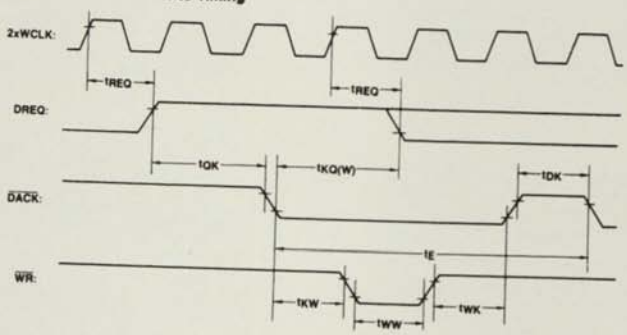


Timing Waveforms (Cont.)

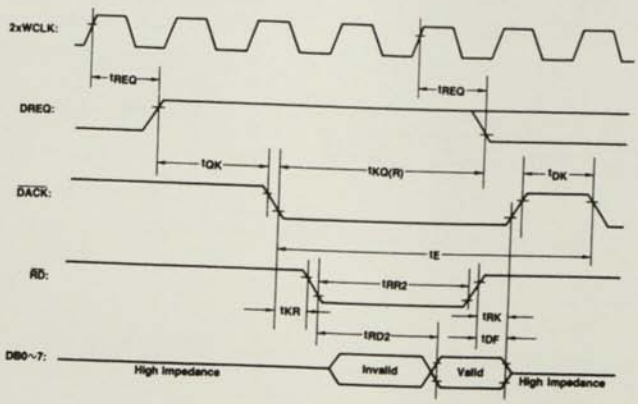
Microprocessor Interface Read Timing



Microprocessor Interface DMA Write Timing

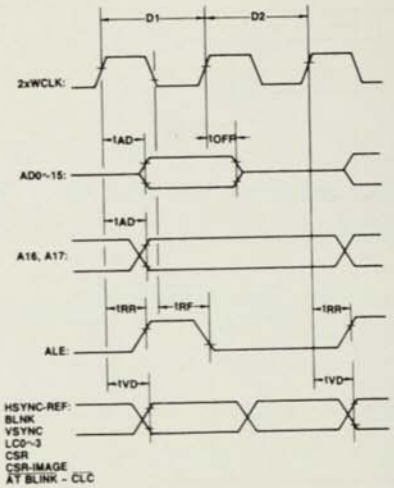


Microprocessor Interface DMA Read Timing

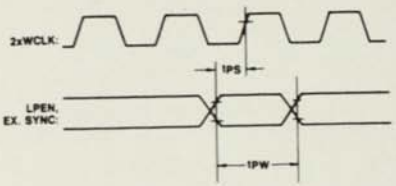


Timing Waveforms (Cont.)

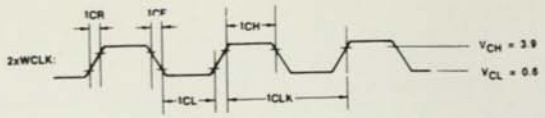
Display Memory Display Cycle Timing



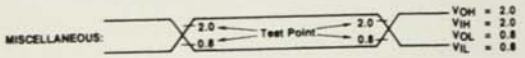
Light Pen and External Sync Input Timing



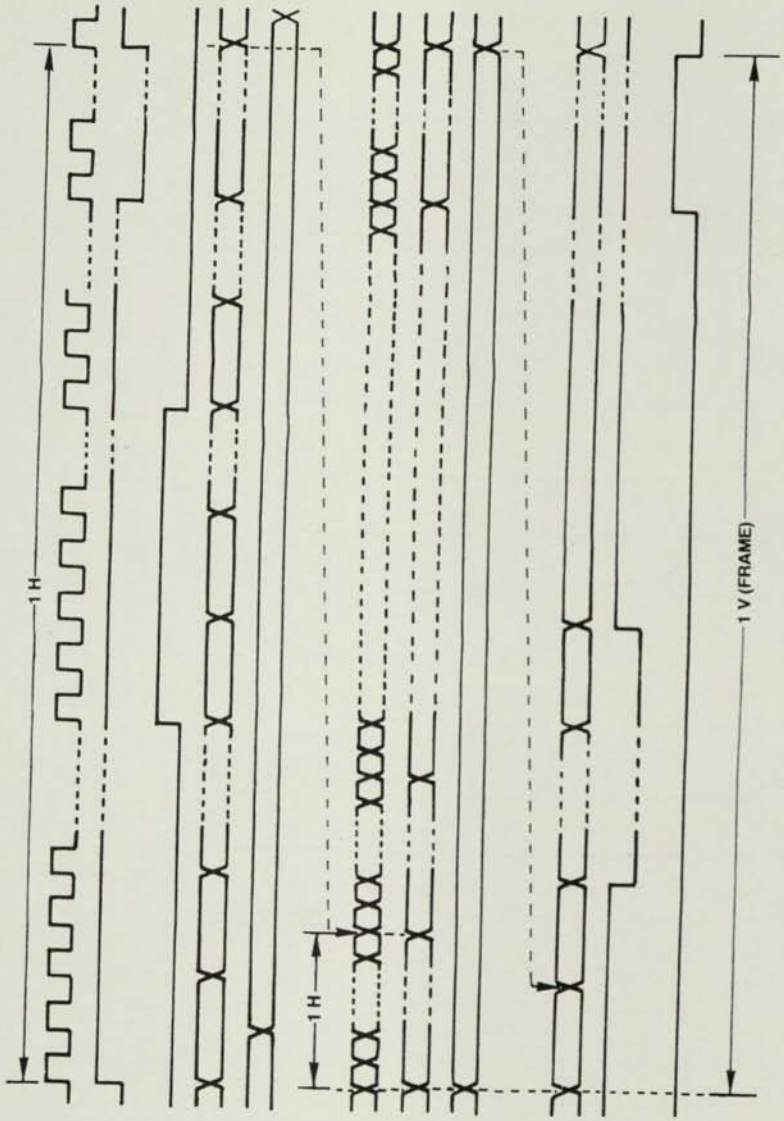
Clock Timing



Test Level (for AC Tests)



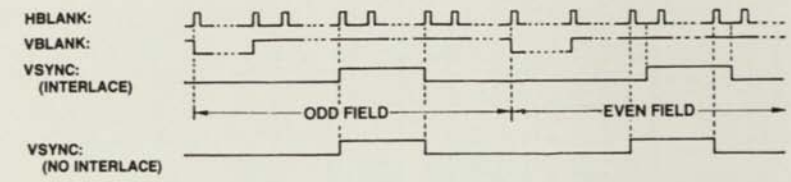
Timing Waveforms (Cont.)



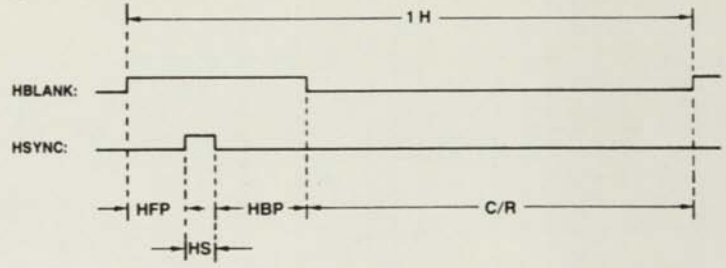
Video Sync Signals Timing

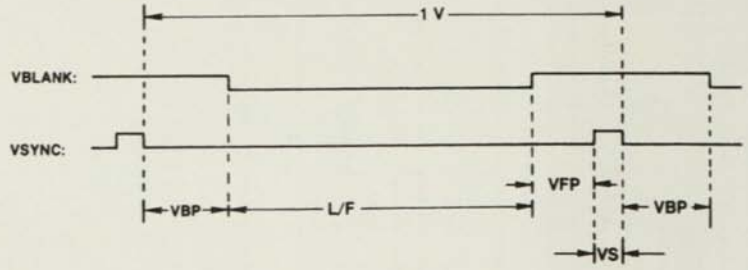
Timing Waveforms (Cont.)

Interlaced Video Timing



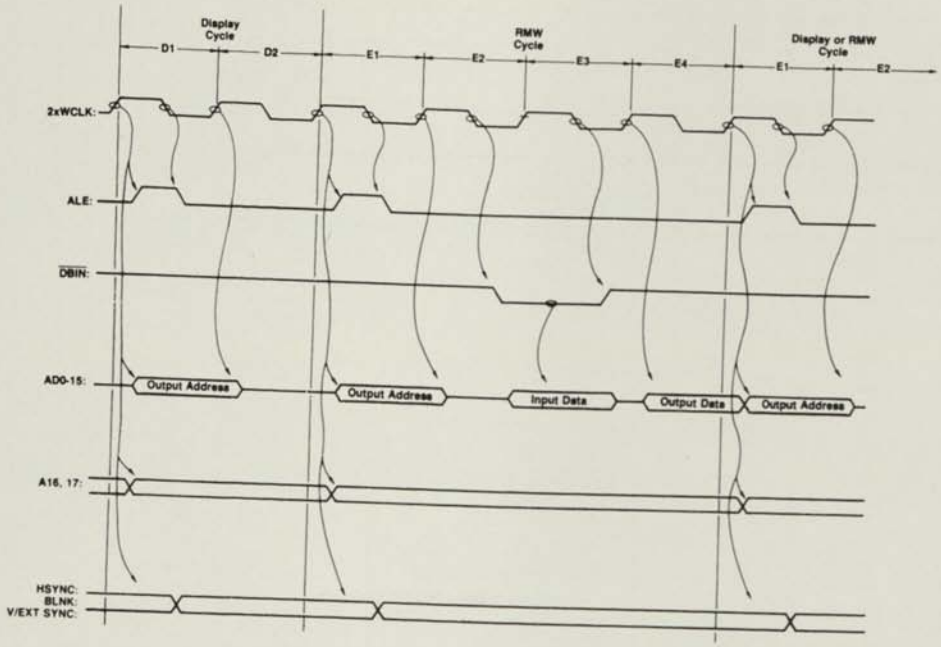
Video Sync Generator Parameters



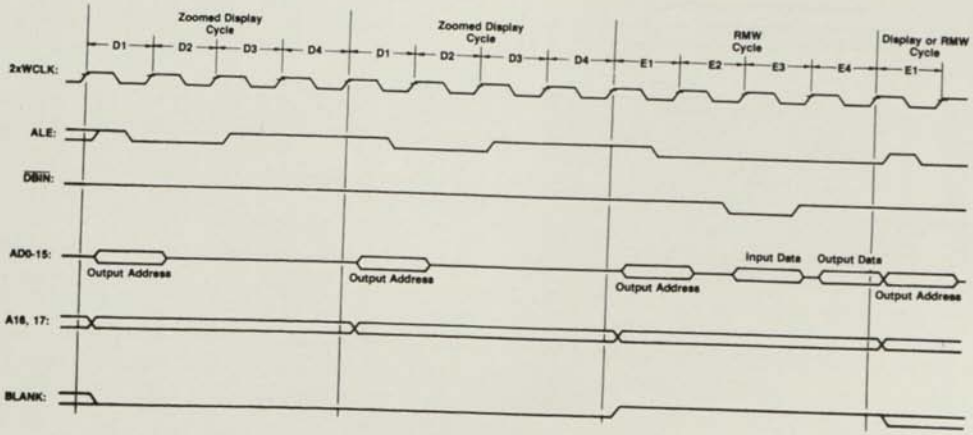


Timing Waveforms (Cont.)

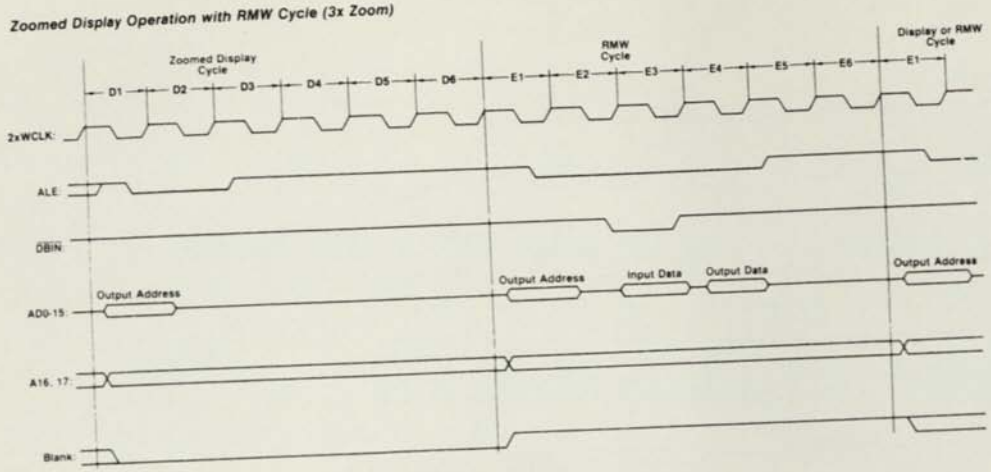
Display and RMW Cycles (1x Zoom)



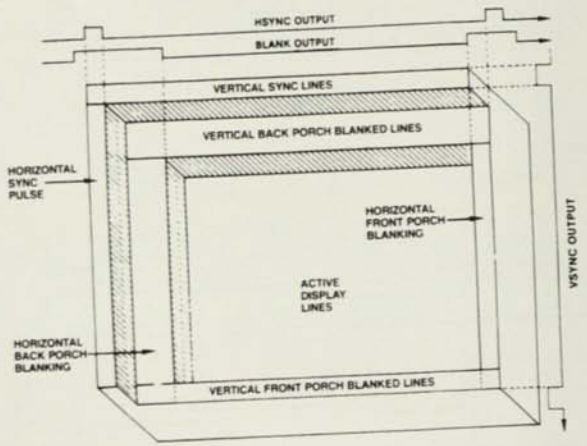
Display and RMW Cycles (2x Zoom)



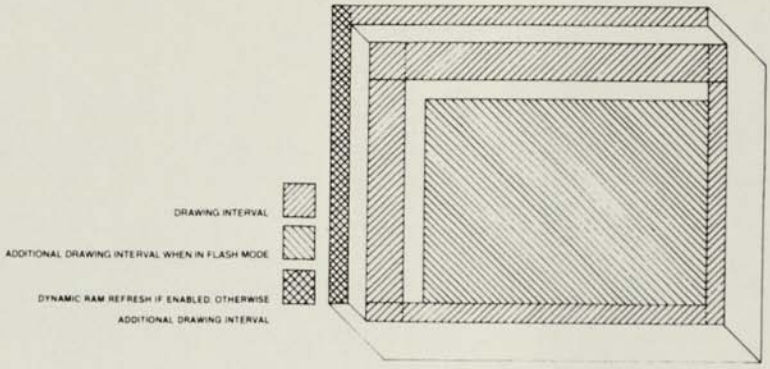
Zoomed Display Operation with RMW Cycle (3x Zoom)



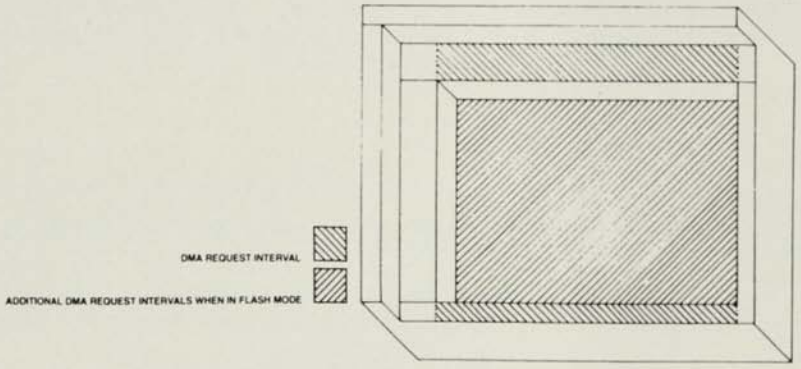
Video Field Timing



Drawing Intervals



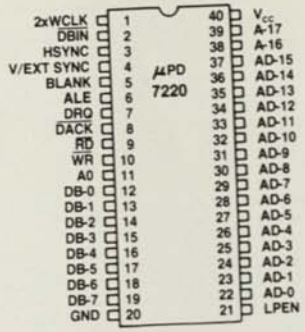
DMA Request Intervals



Pin Identification

Pin No.	Symbol	Direction	Function
1	2xWCLK	IN	Clock Input
2	$\overline{DBIN}$	OUT	Display Memory Read Input Flag
3	HSYNC	OUT	Horizontal Video Sync Output
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External VSYNC Input
5	BLANK	OUT	CRT Blanking Output
6	ALE ($\overline{RAS}$)	OUT	Address Latch Enable Output
7	DRQ	OUT	DMA Request Output
8	$\overline{DACK}$	IN	DMA Acknowledge Input
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface
10	$\overline{WR}$	IN	Write Strobe Input for Microprocessor Interface
11	A0	IN	Address Select Input for Microprocessor Interface
12–19	DB0 to 7	IN/OUT	Bidirectional Data Bus to Host Microprocessor
20	GND	—	Ground
21	LPEN	IN	Light Pen Detect Input
22–34	AD0 to 12	IN/OUT	Address and Data Lines to Display Memory
35–37	AD13 to 15	IN/OUT	Utilization Varies with Mode of Operation
38	A16	OUT	Utilization Varies with Mode of Operation
39	A17	OUT	Utilization Varies with Mode of Operation
40	V_{CC}	—	+5V ± 10%

Pin Configuration



Character Mode Pin Utilization

Pin No.	Name	Direction	Function
35–37	AD13 to 15	OUT	Line Counter Bits 0 to 2 Outputs
38	A16	OUT	Line Counter Bit 3 Output
39	A17	OUT	Cursor Output

Mixed Mode Pin Utilization

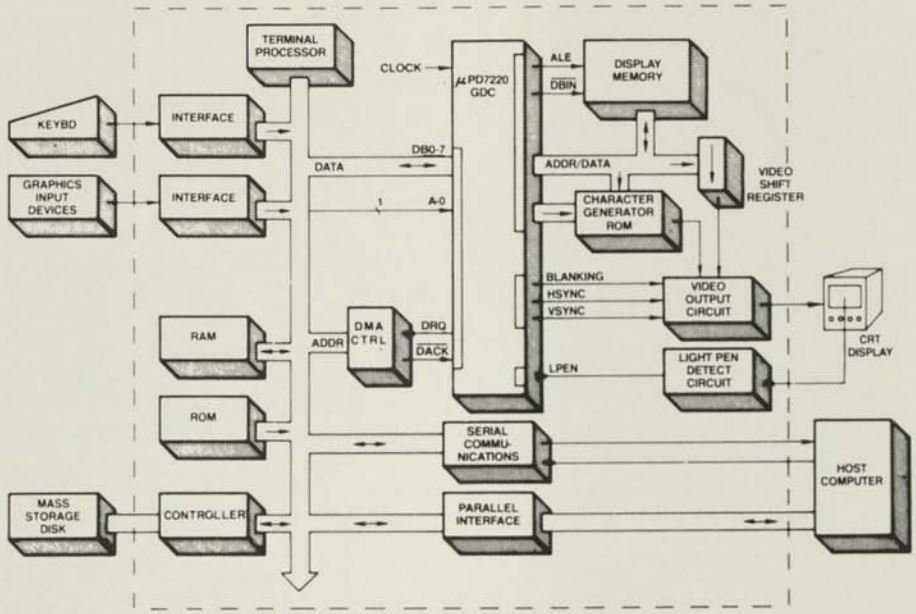
Pin No.	Name	Direction	Function
35–37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Attribute Blink and Clear Line Counter* Output
39	A17	OUT	Cursor and Bit-Map Area* Flag Output

* = Output during the HSYNC interval. Use the trailing edge at HSYNC to clock this value into a flop for reference during the rest of the video line.

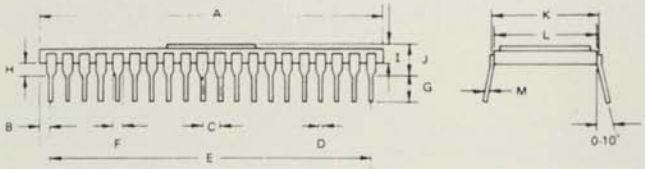
Graphics Mode Pin Utilization

Pin No.	Name	Direction	Function
35–37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Address Bit 16 Output
39	A17	OUT	Address Bit 17 Output

Block Diagram of a Graphics Terminal



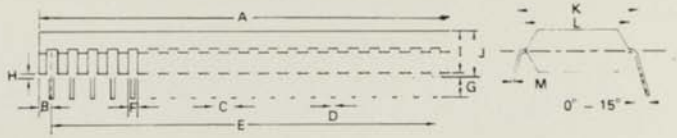
Package Outlines
μPD7220D



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

μPD7220C



Plastic

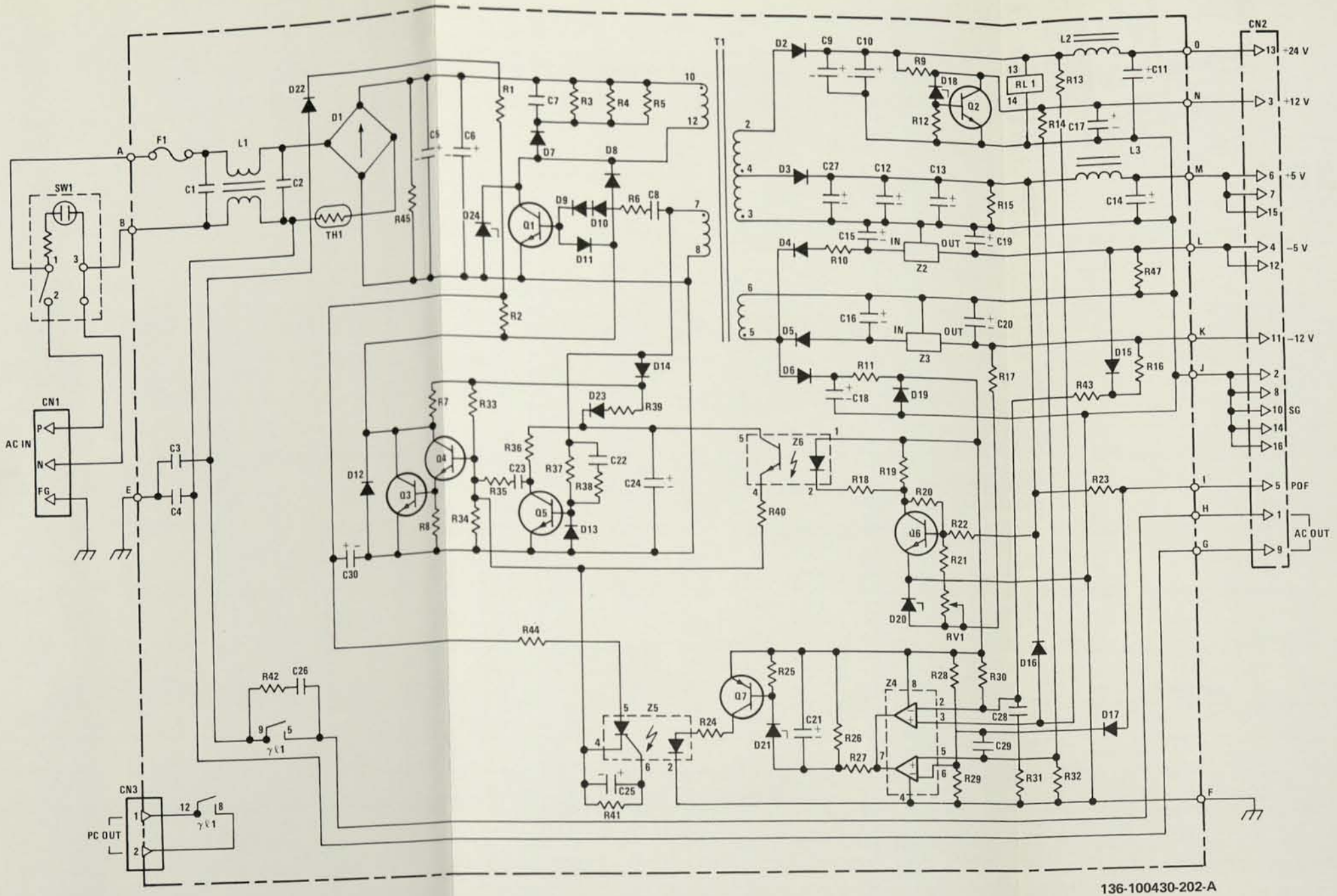
ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

SCHEMATIC
DIAGRAMS

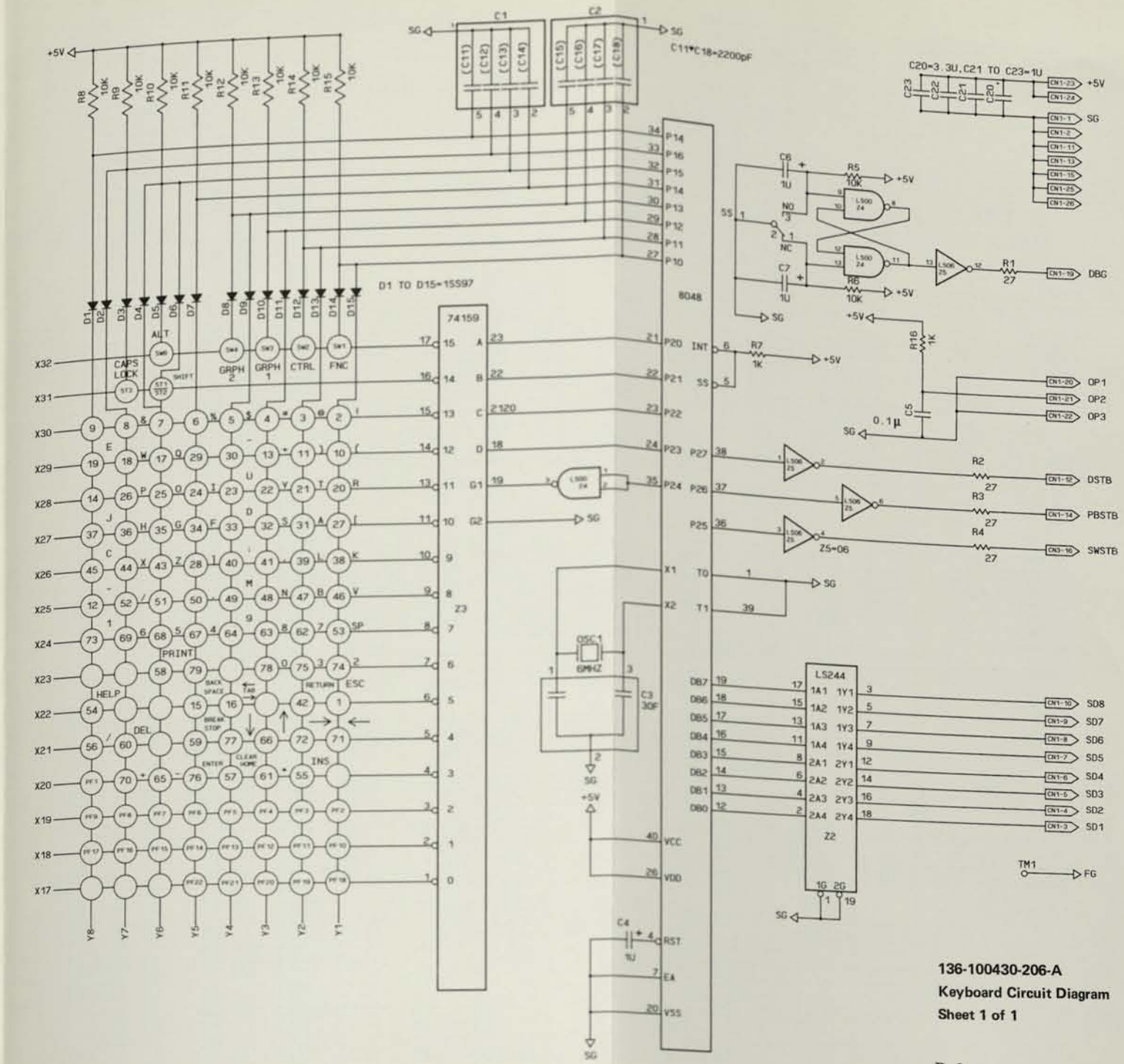
Appendix B

Logic and Schematic Diagrams

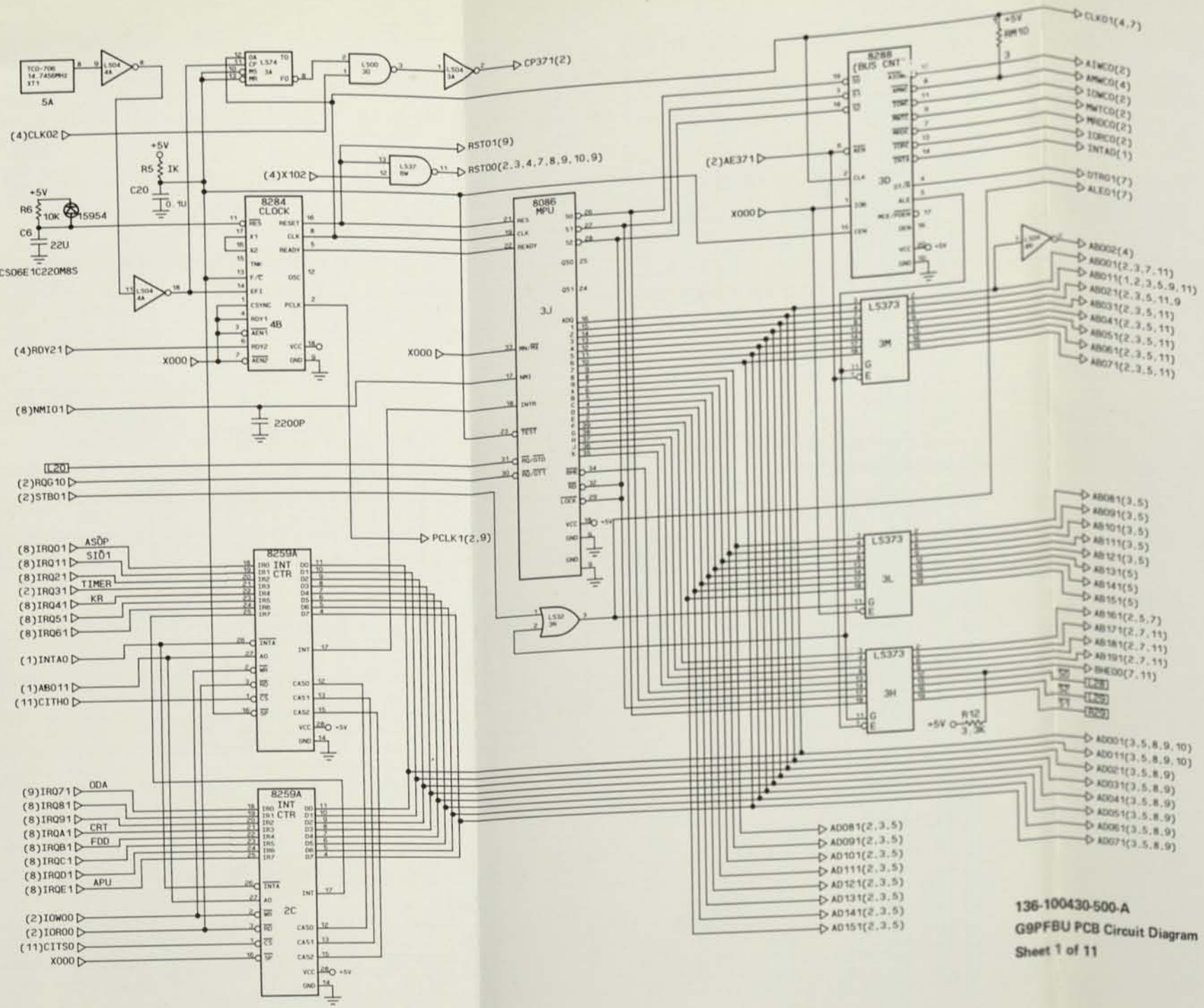
The APC logic and schematic diagrams are arranged in drawing number sequence.



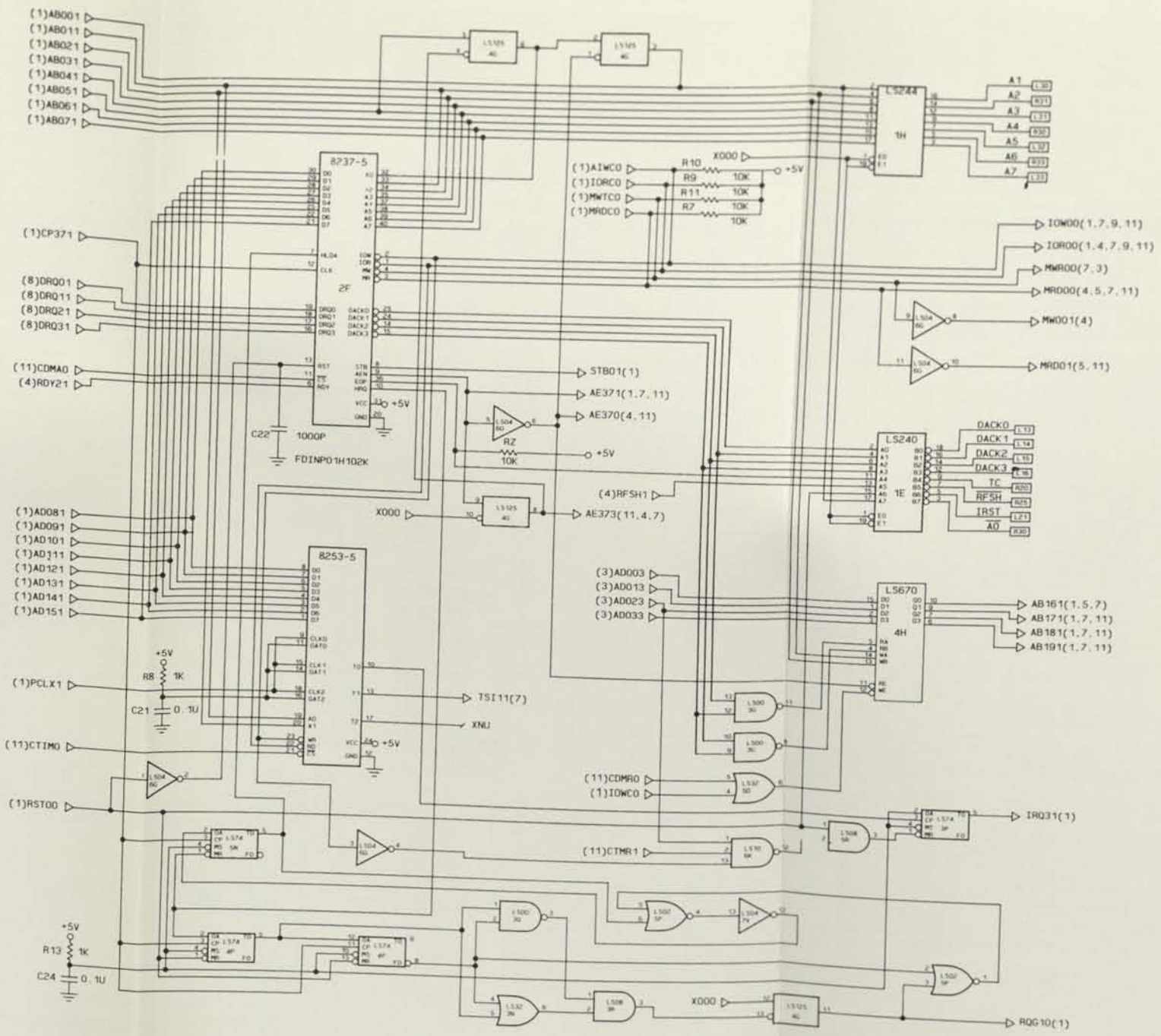
136-100430-202-A
H Type Power Supply Circuit Diagram
Sheet 1 of 1



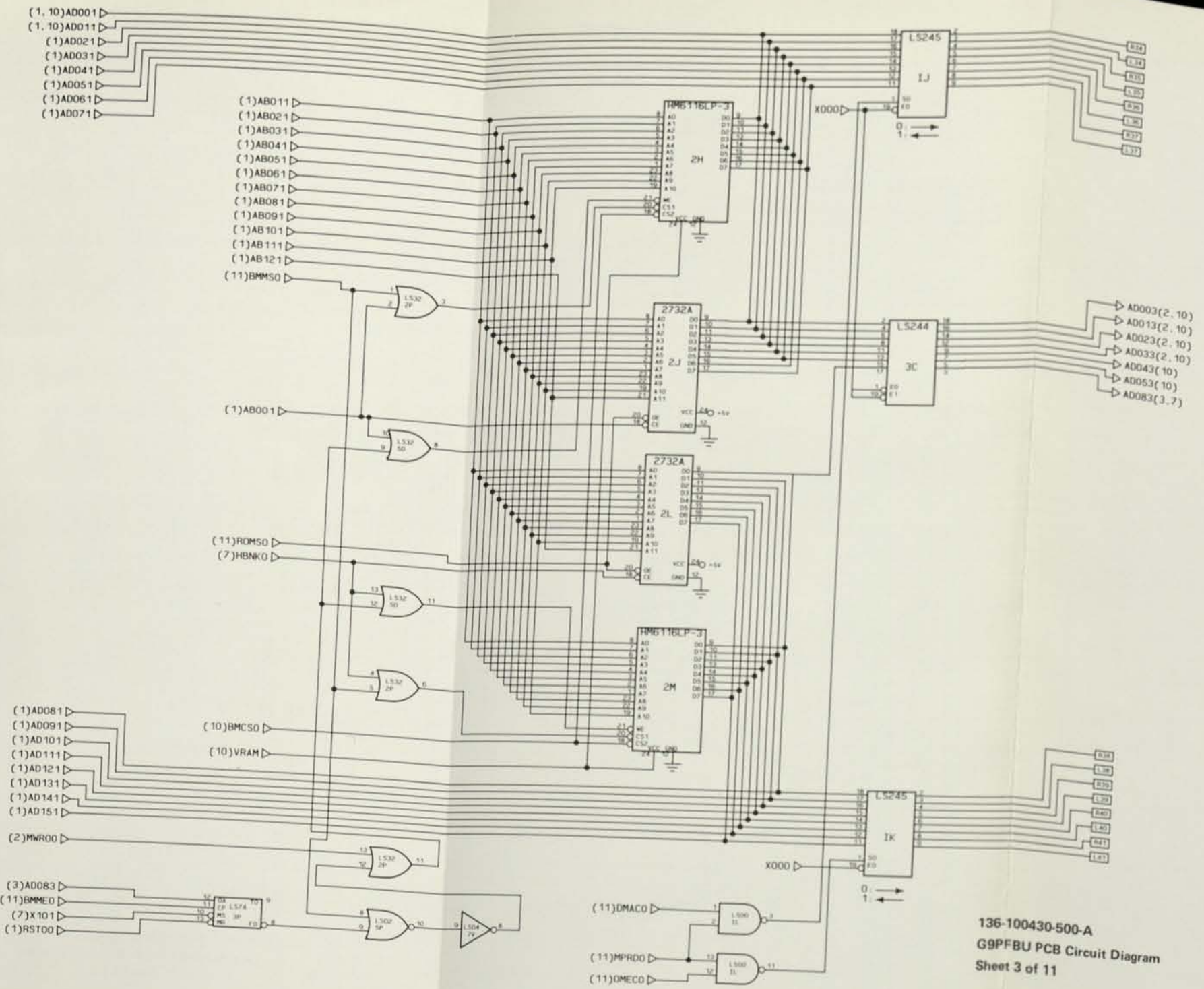
136-100430-206-A
Keyboard Circuit Diagram
Sheet 1 of 1



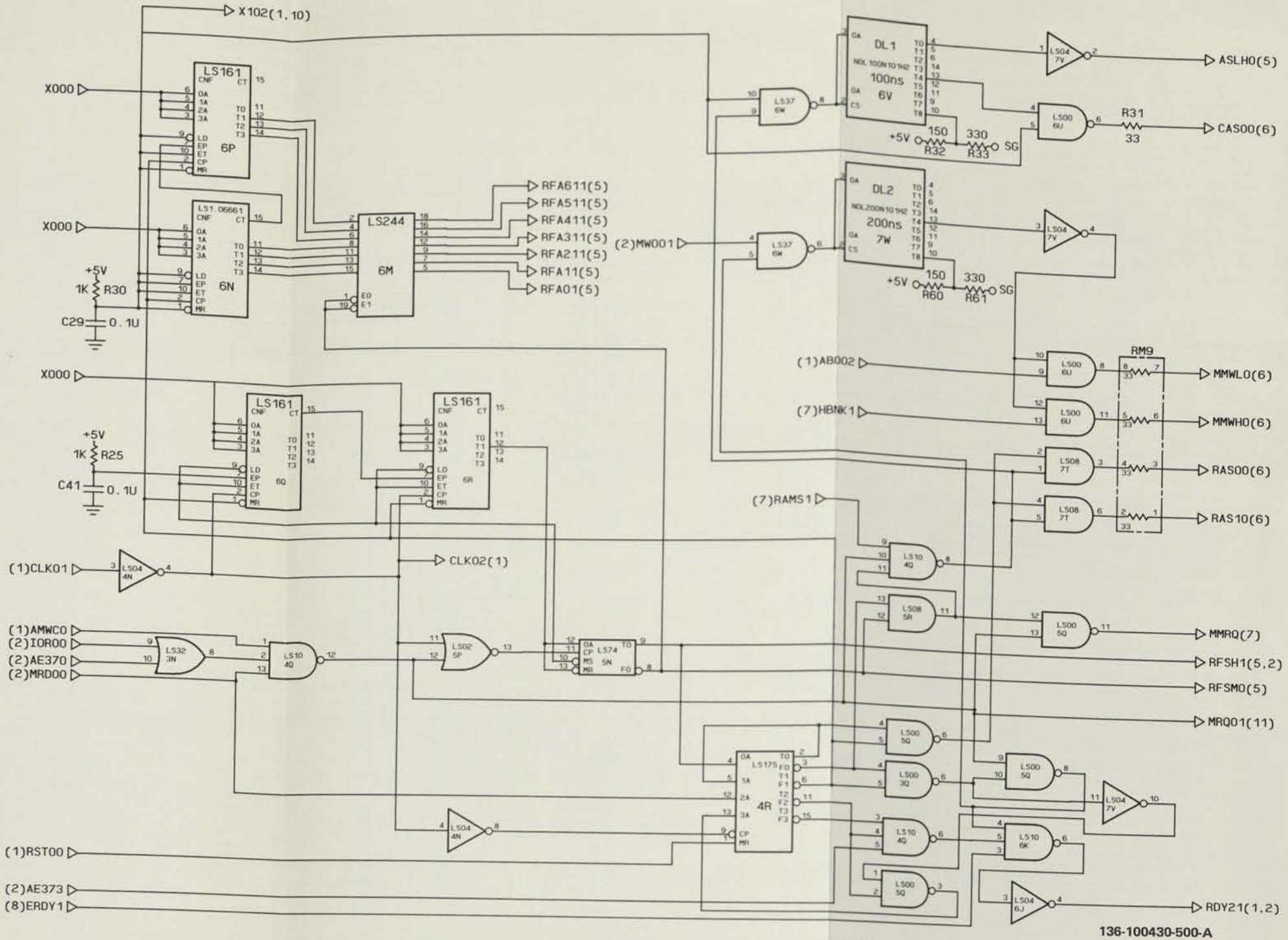
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 1 of 11



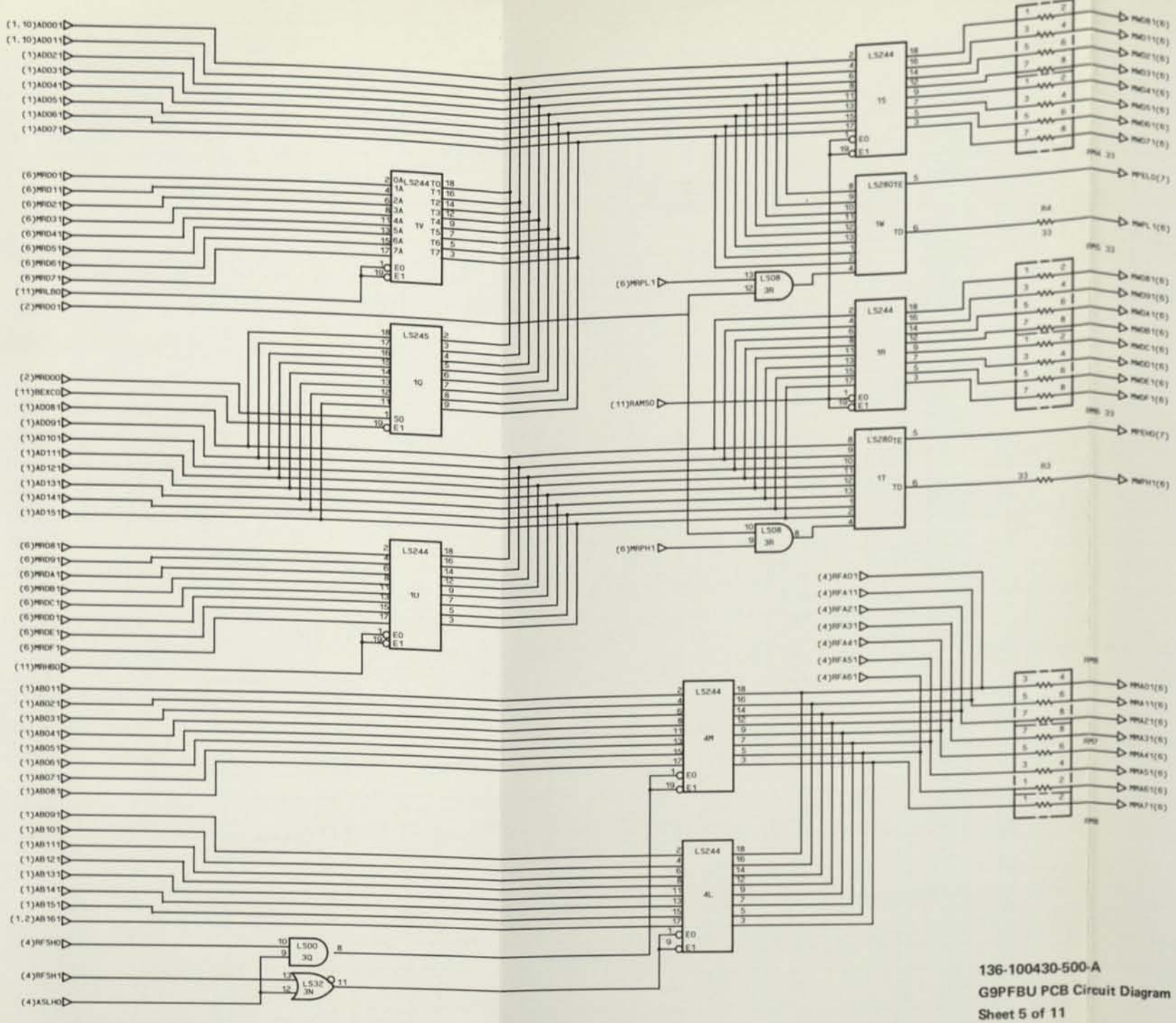
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 2 of 11



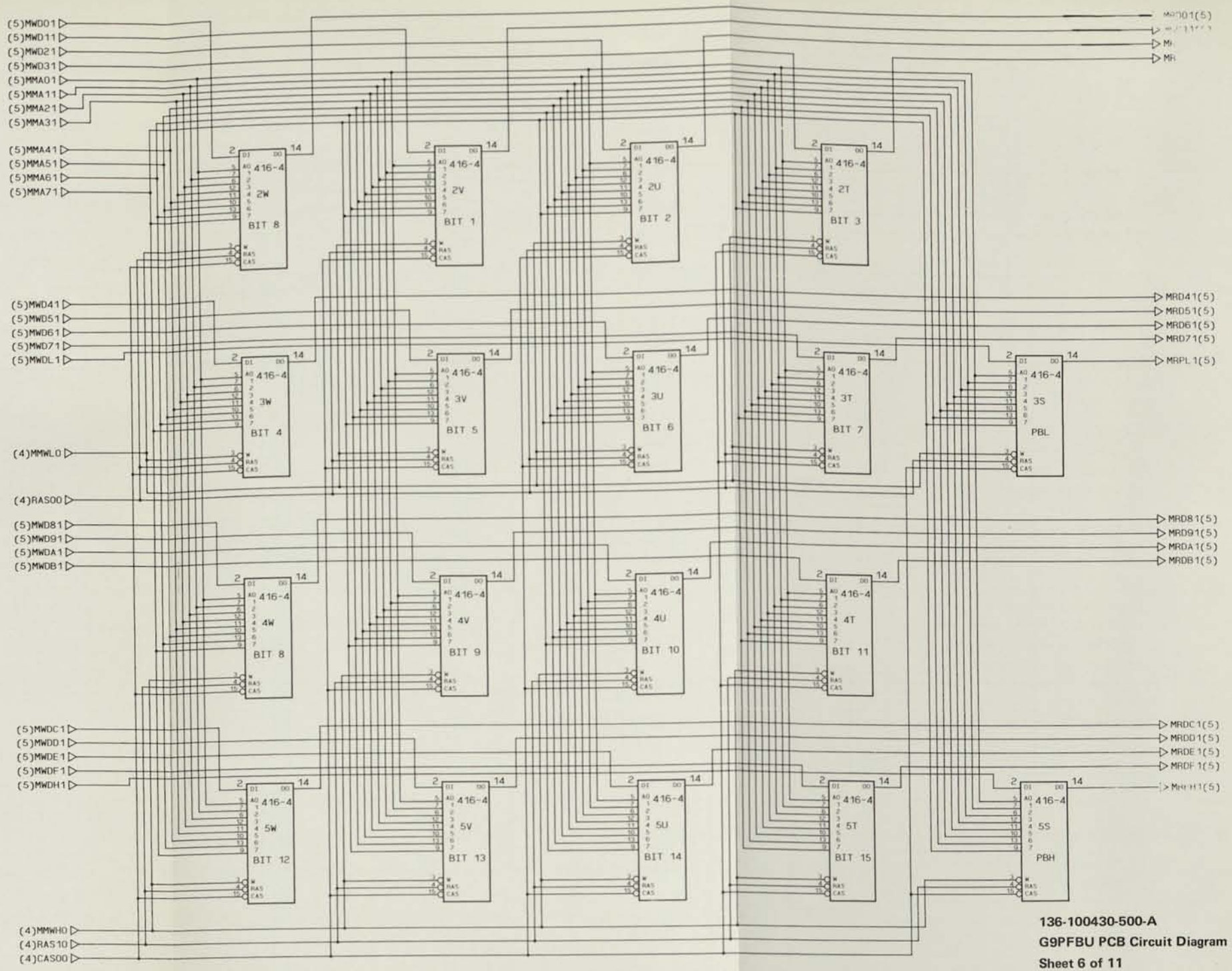
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 3 of 11



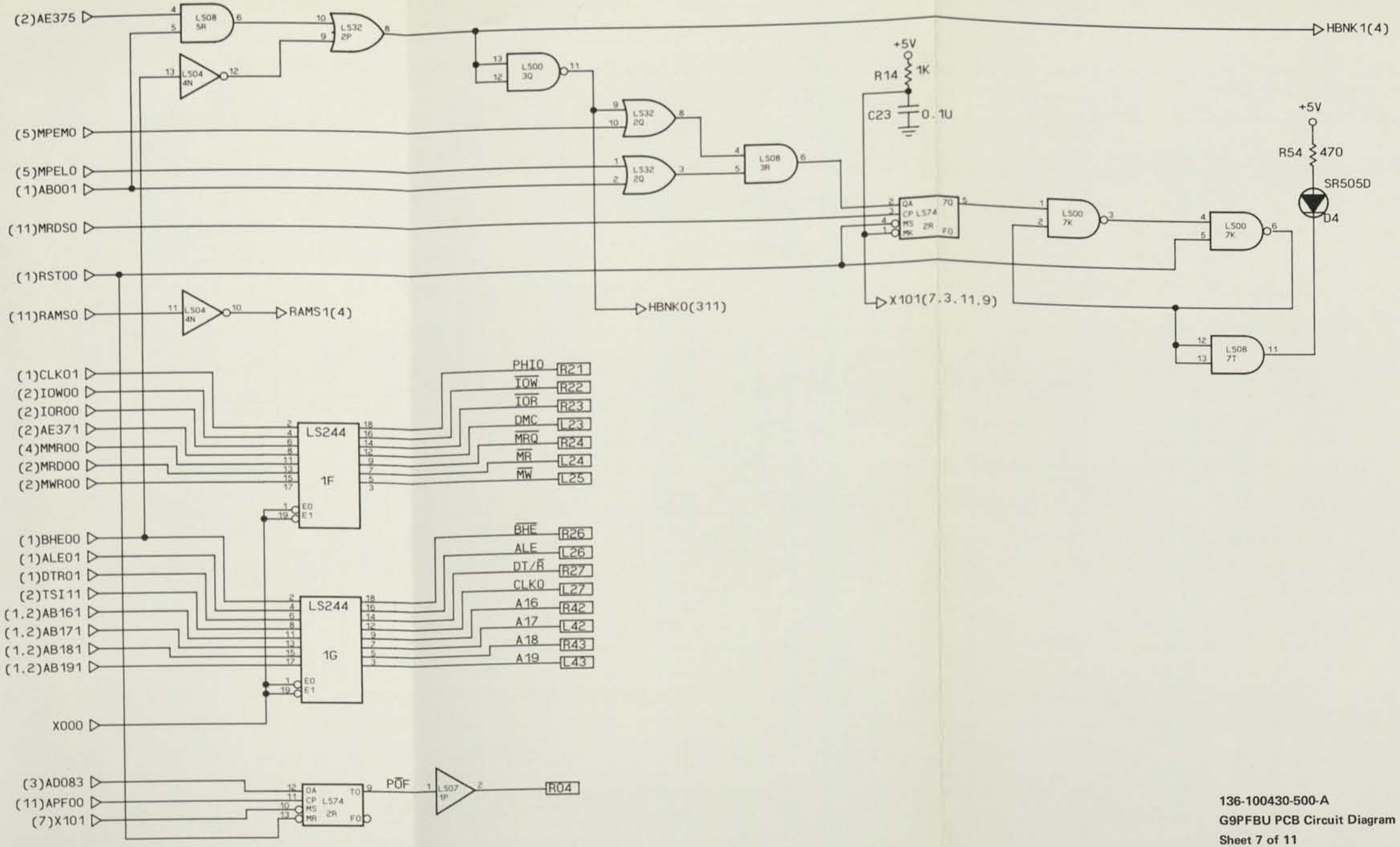
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 4 of 11



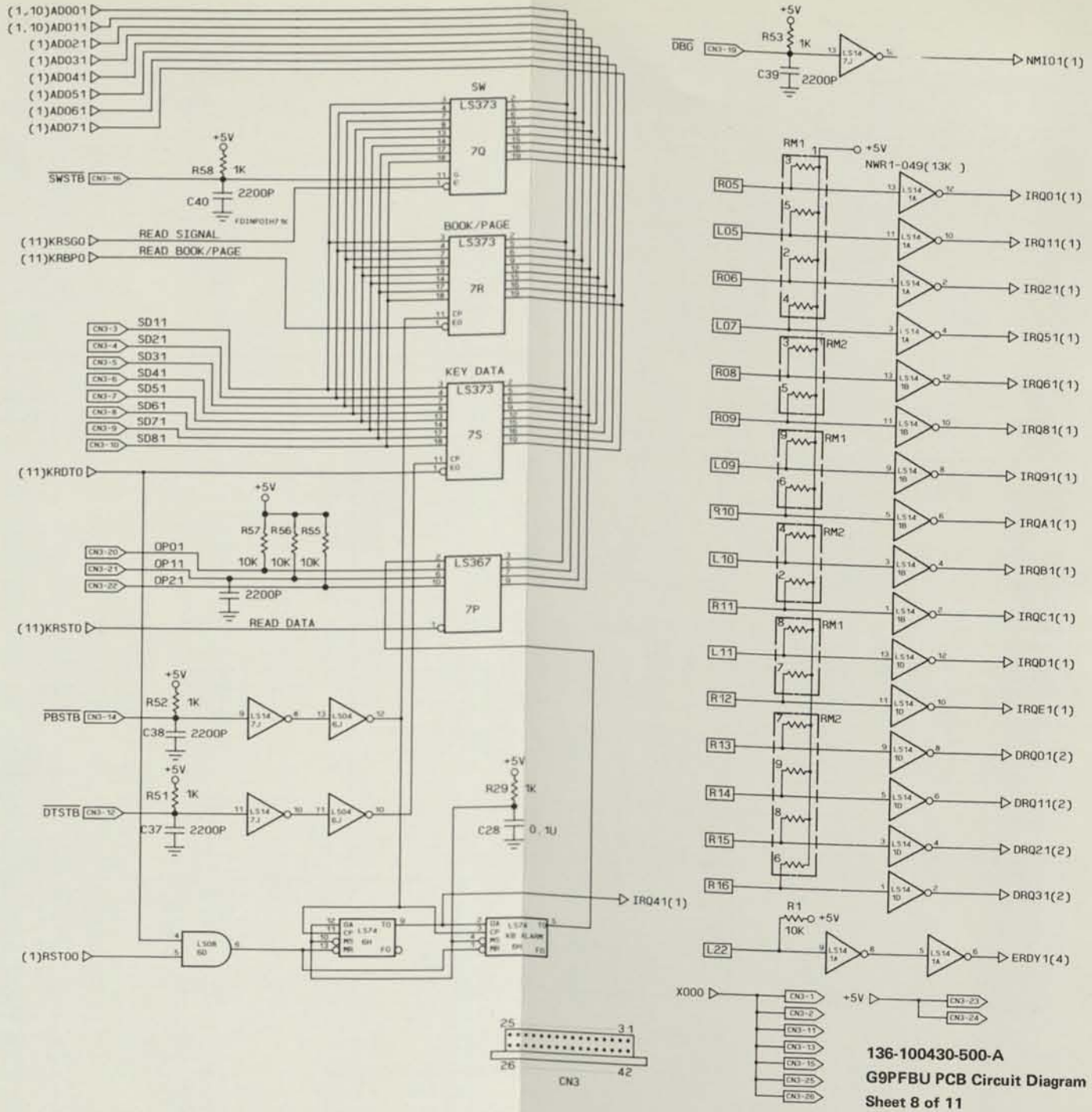
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 5 of 11



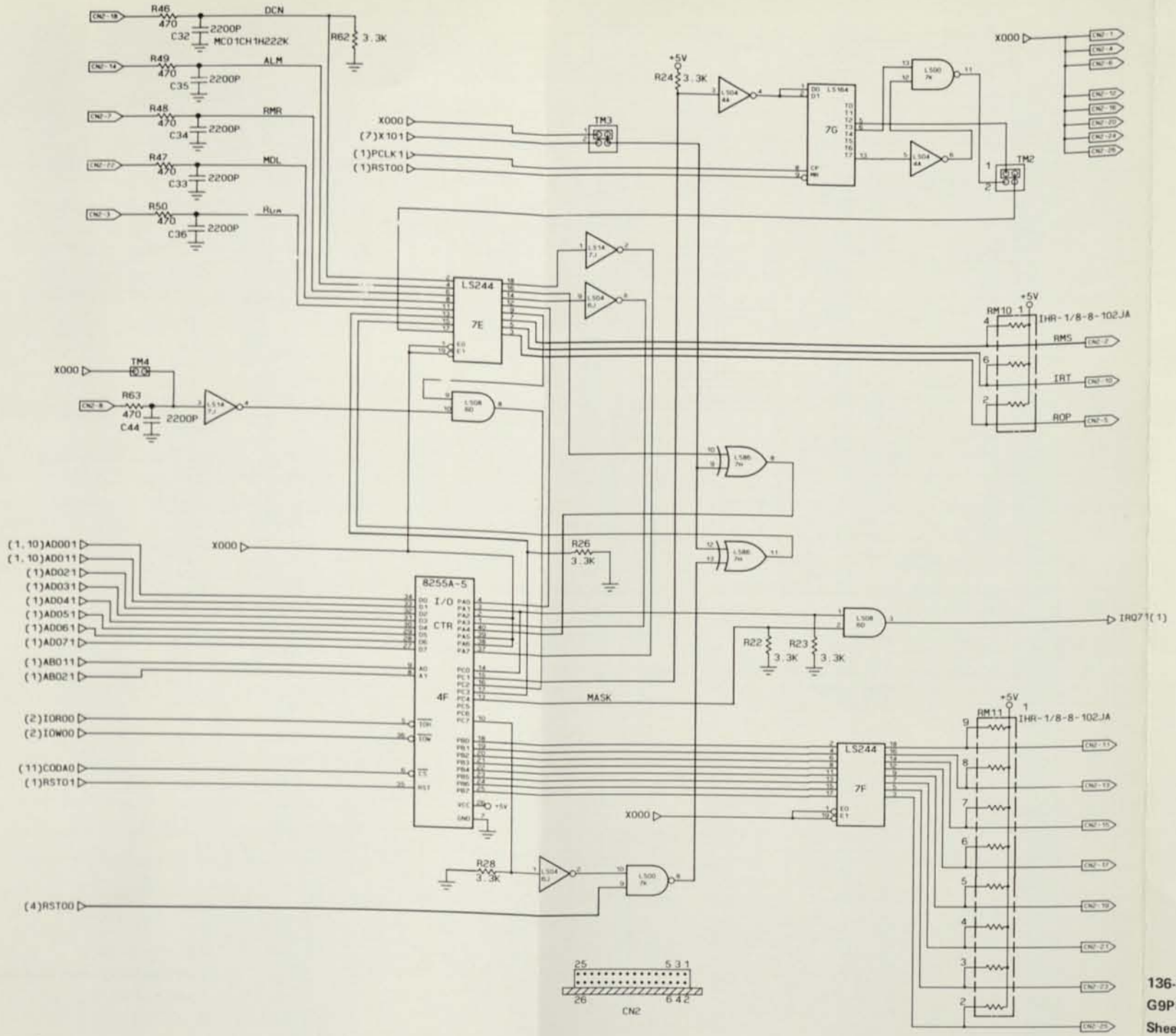
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 6 of 11



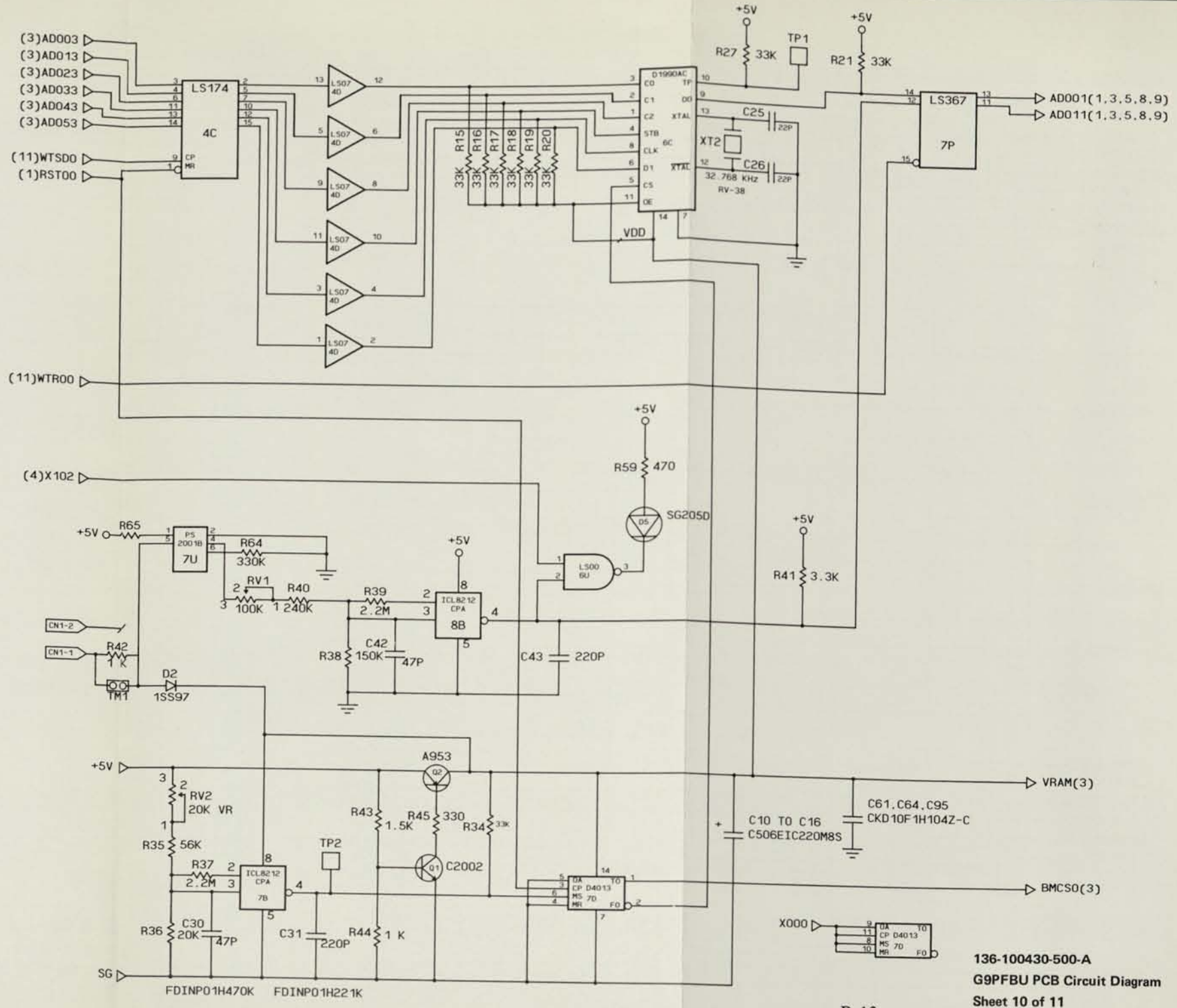
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 7 of 11



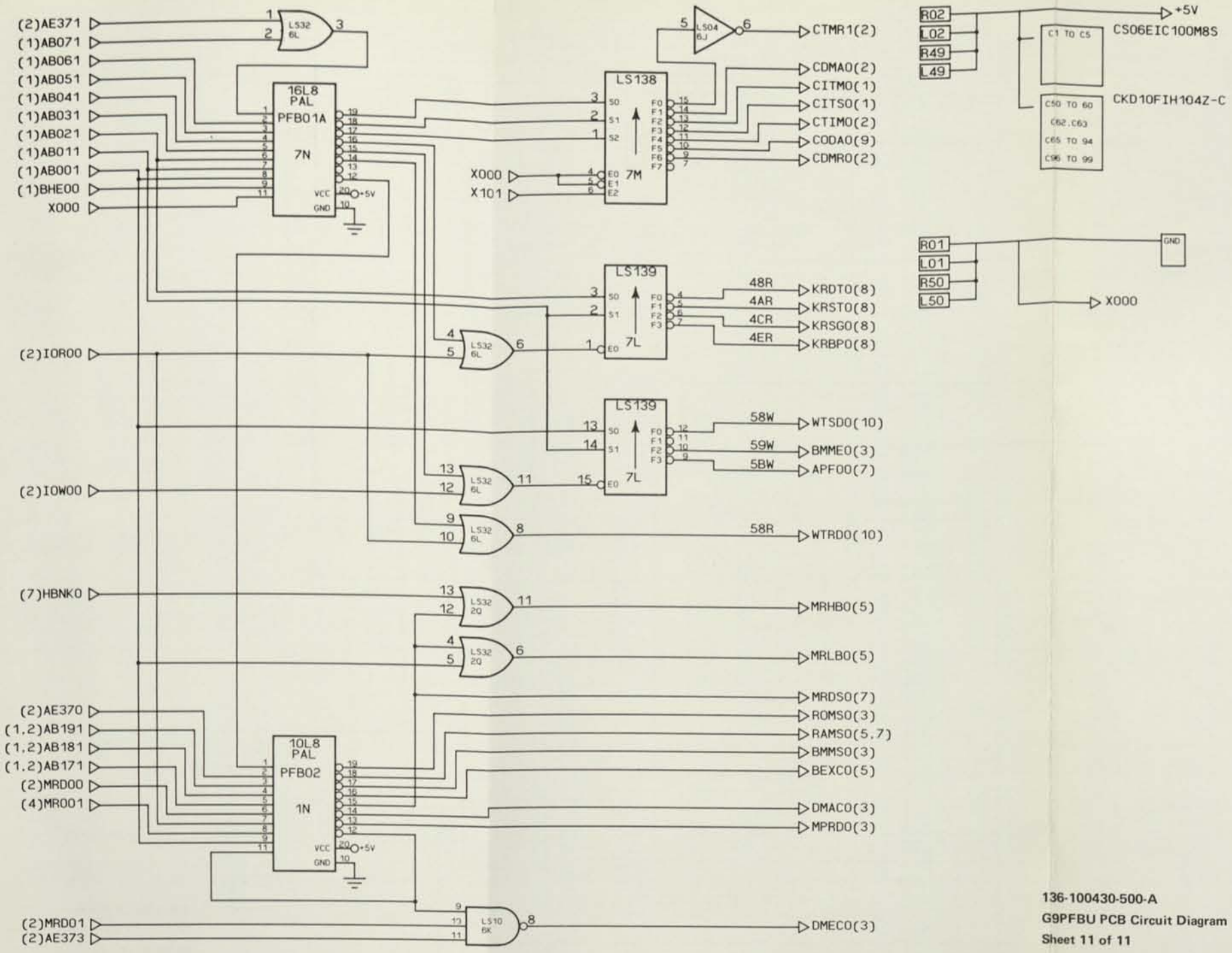
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 8 of 11



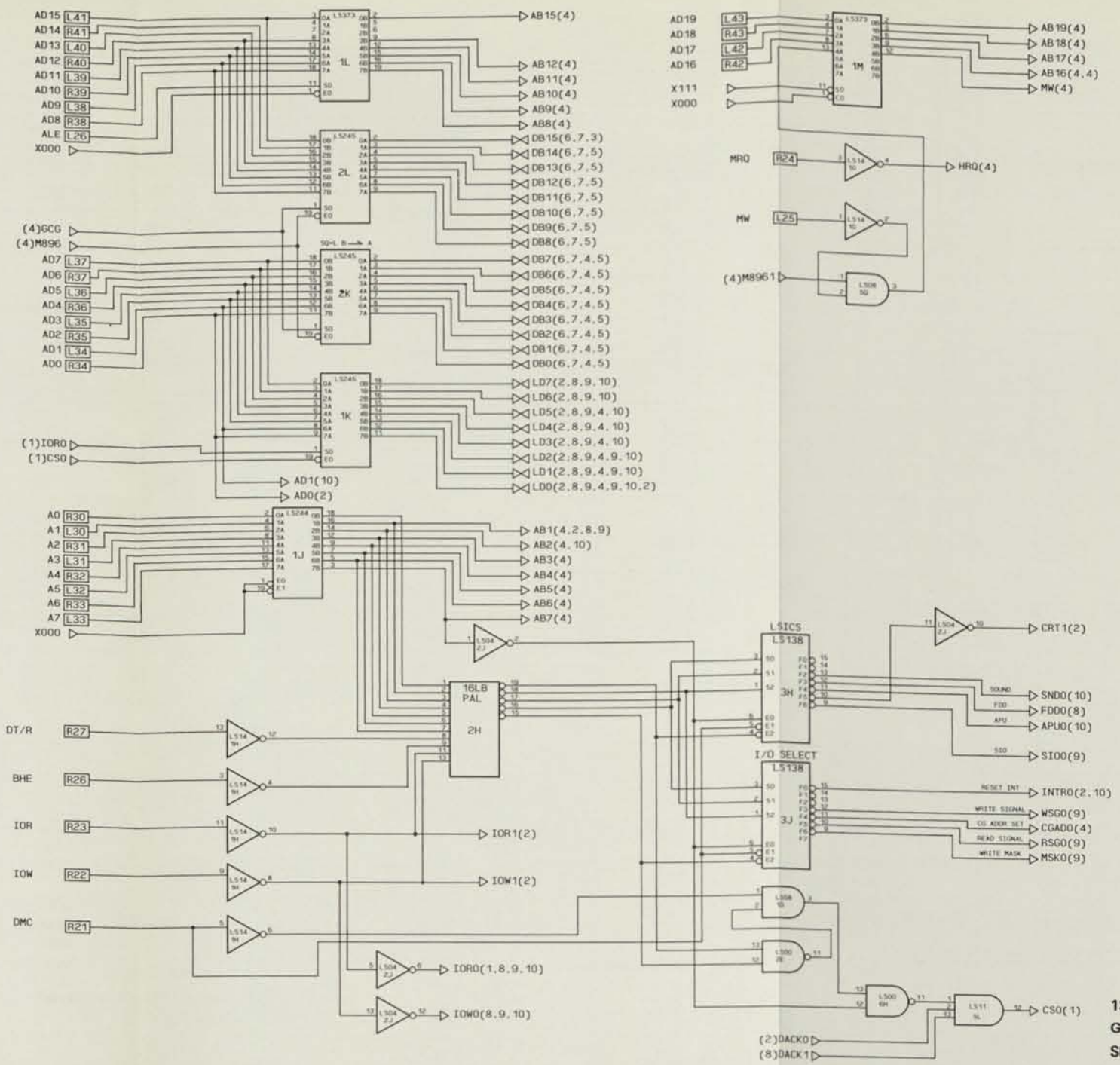
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 9 of 11



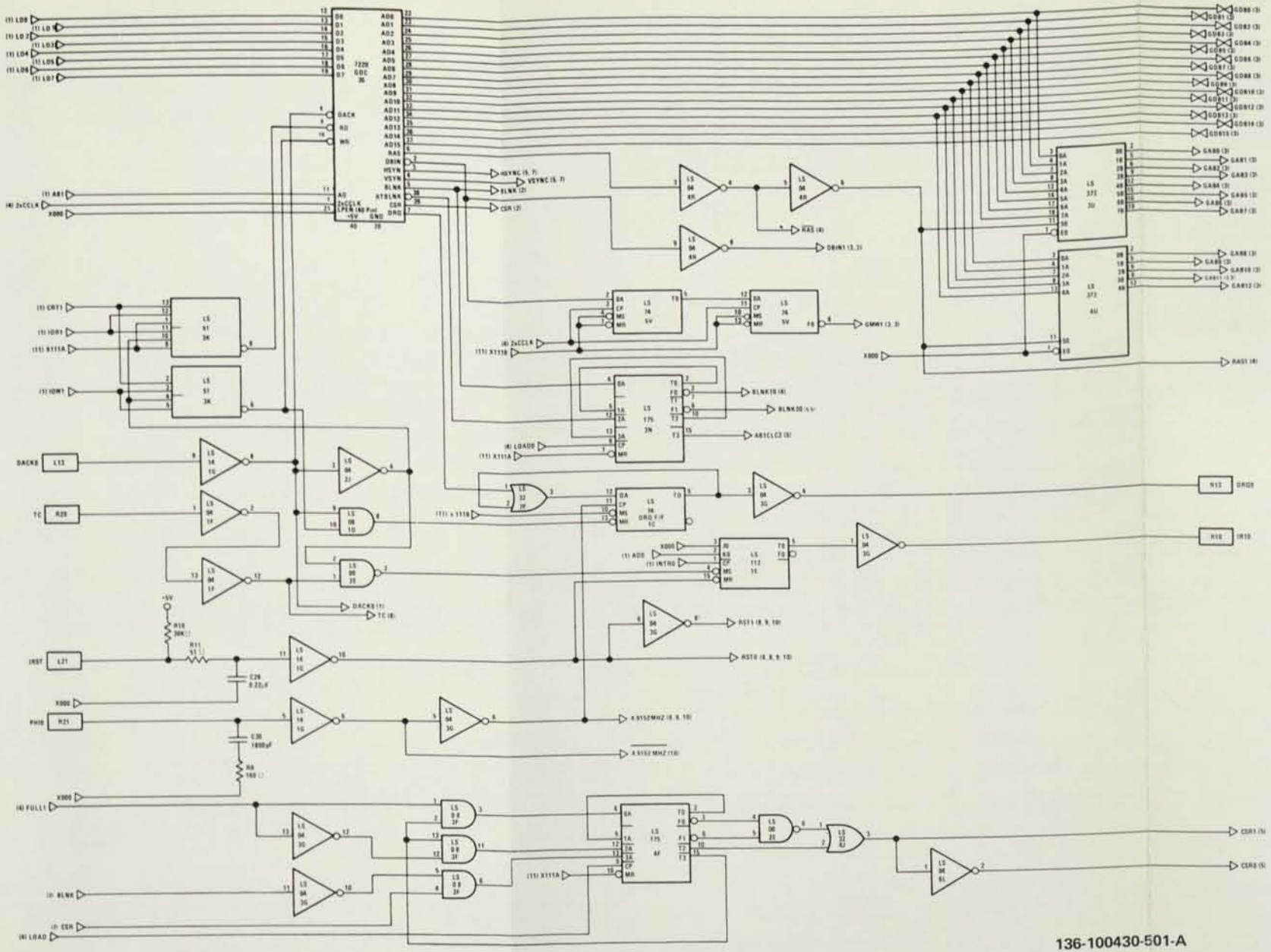
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 10 of 11



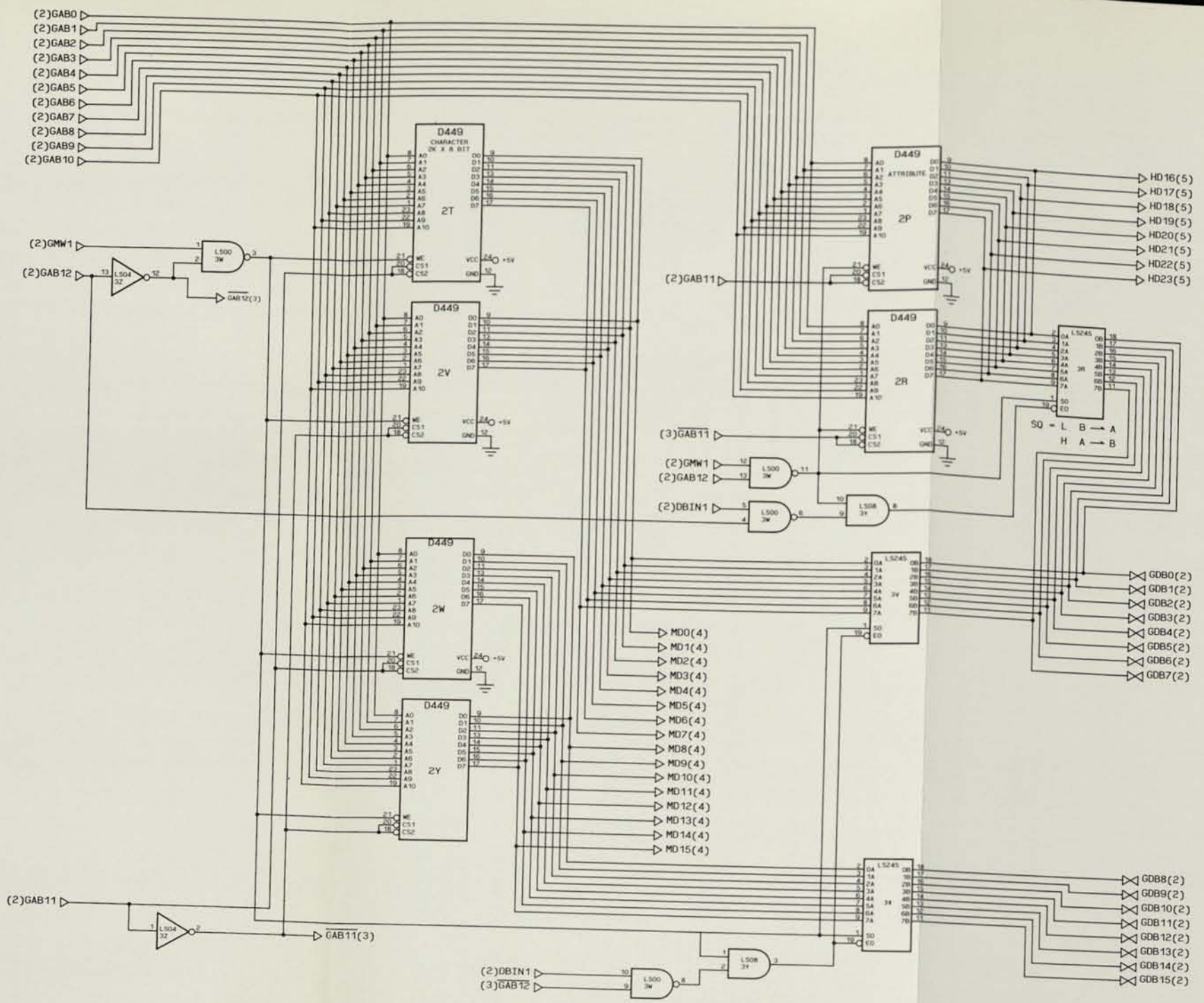
136-100430-500-A
G9PFBU PCB Circuit Diagram
Sheet 11 of 11



136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 1 of 11



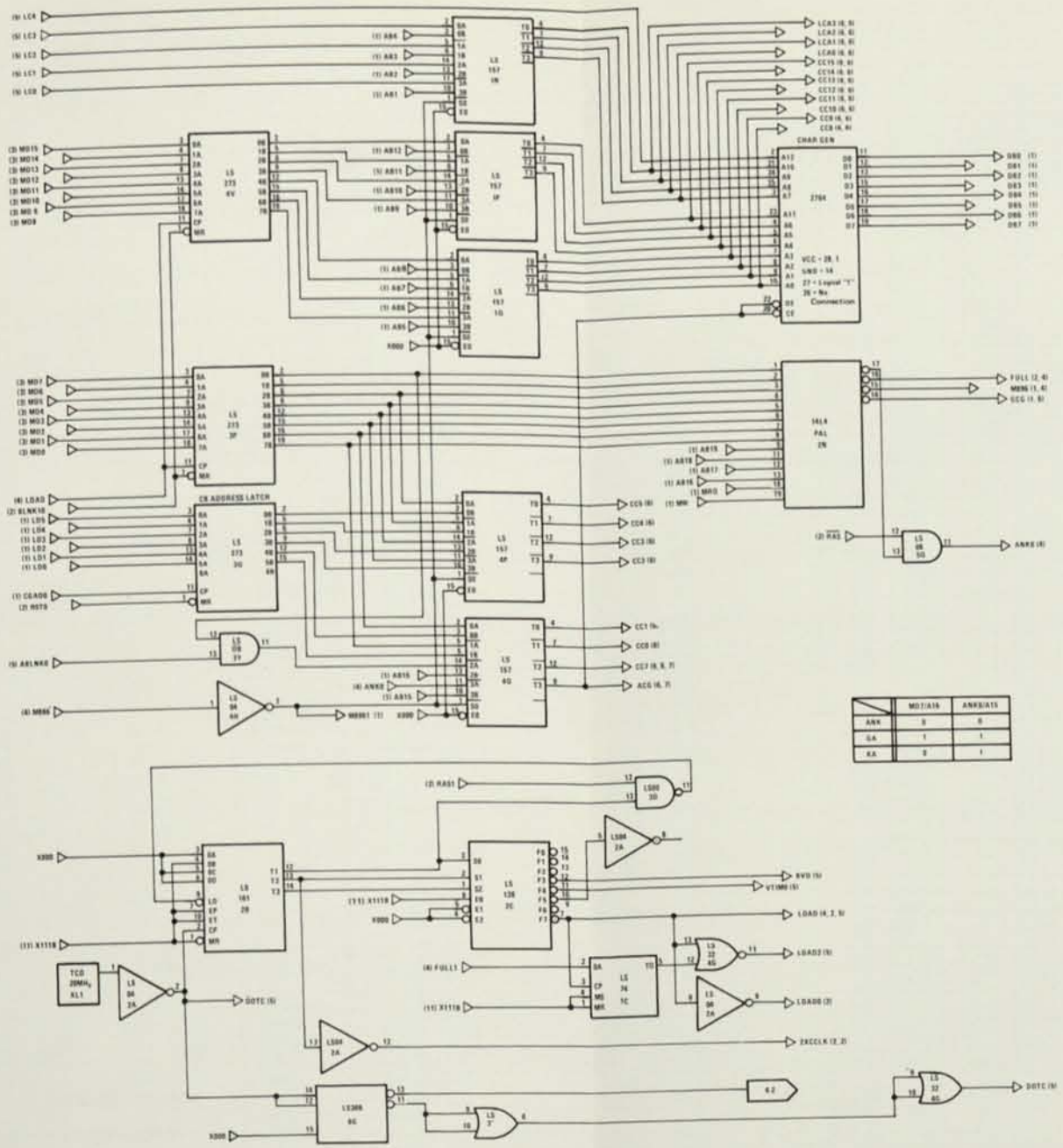
136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 2 of 11



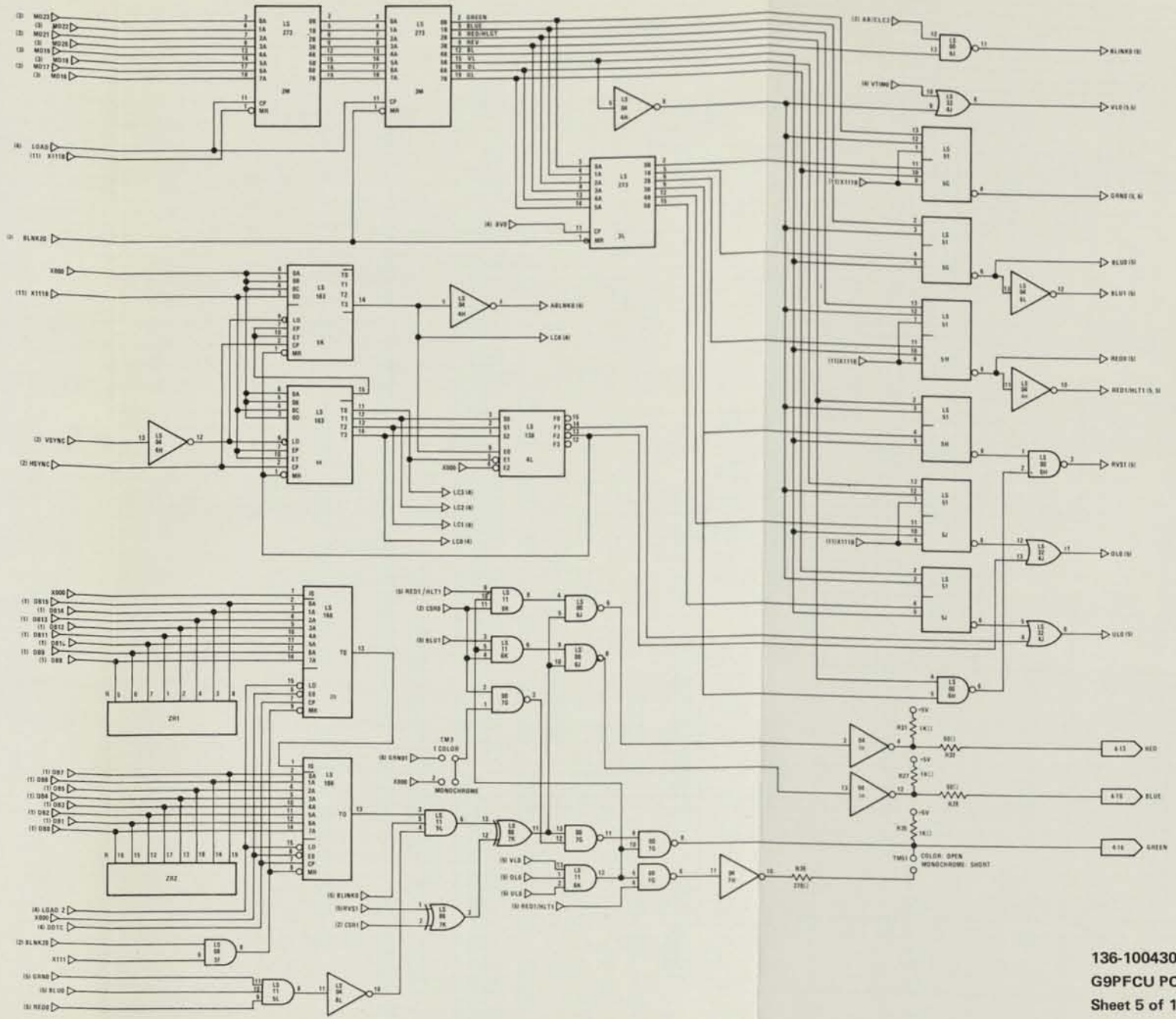
136-100430-501-A

G9PFCU PCB Circuit Diagram

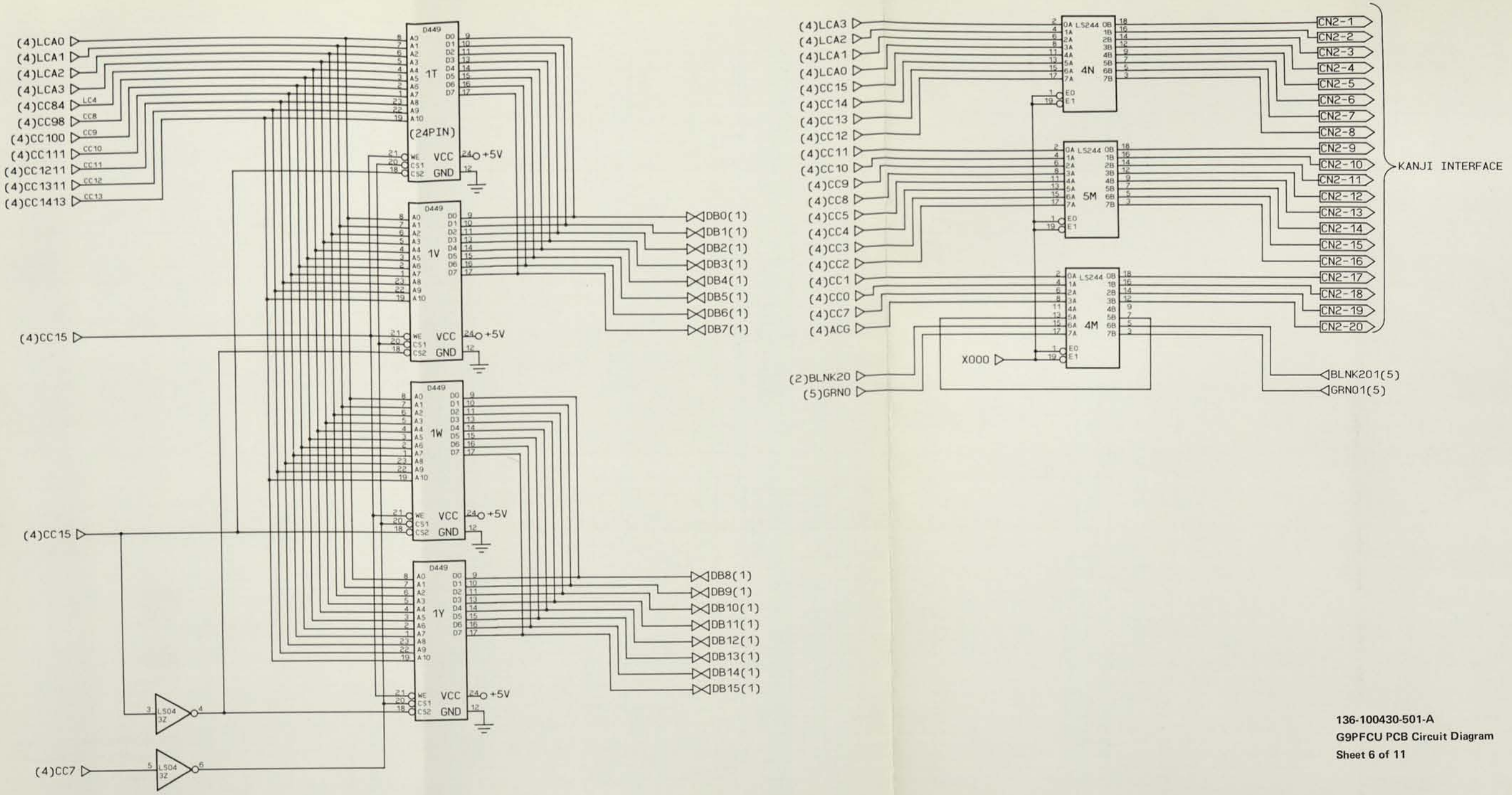
Sheet 3 of 11



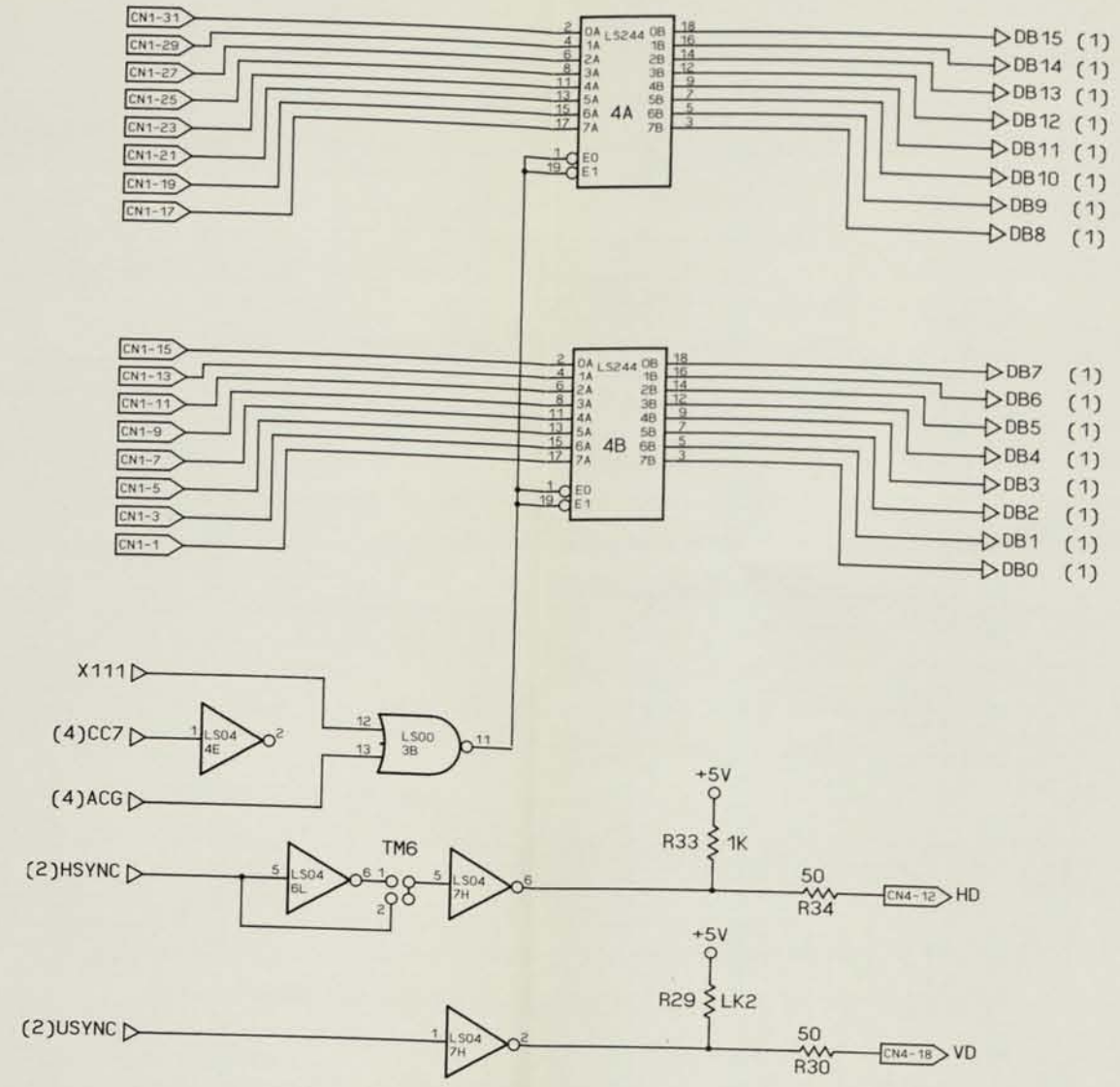
136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 4 of 11

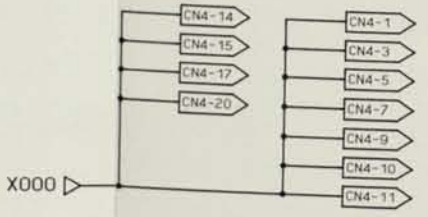


136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 5 of 11

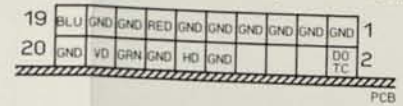


136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 6 of 11

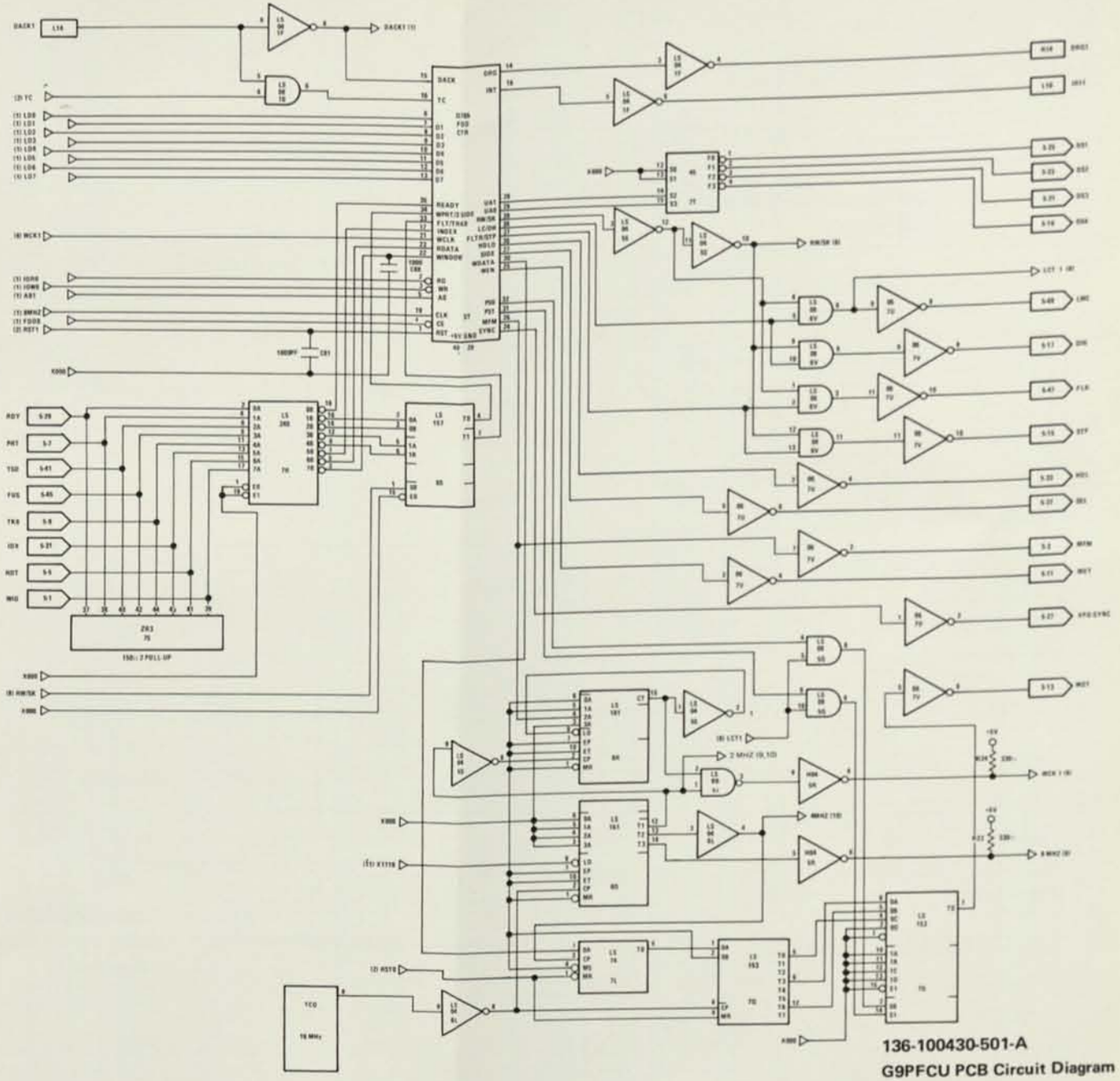




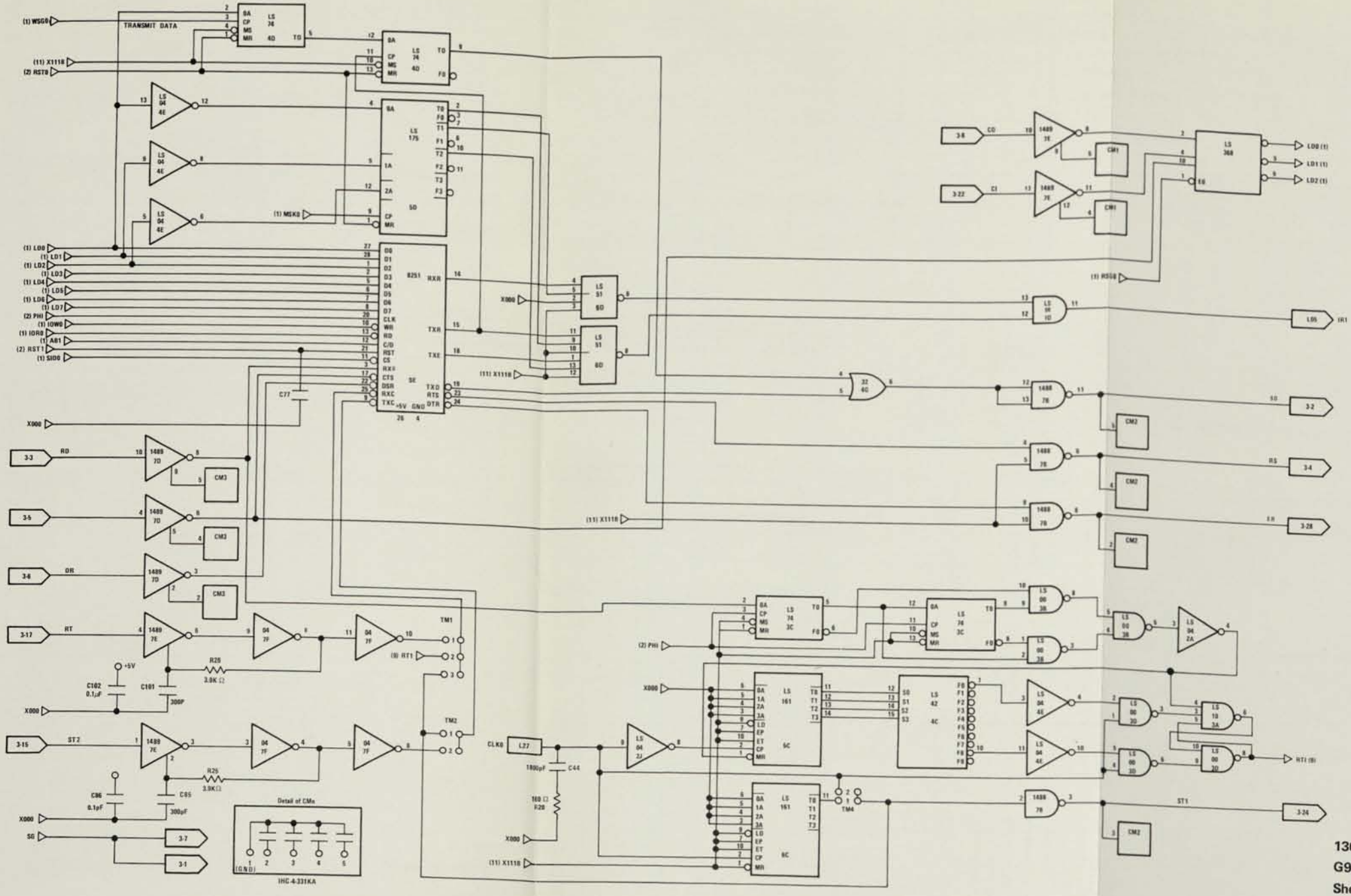
Pin assignment of CRT display unit connector



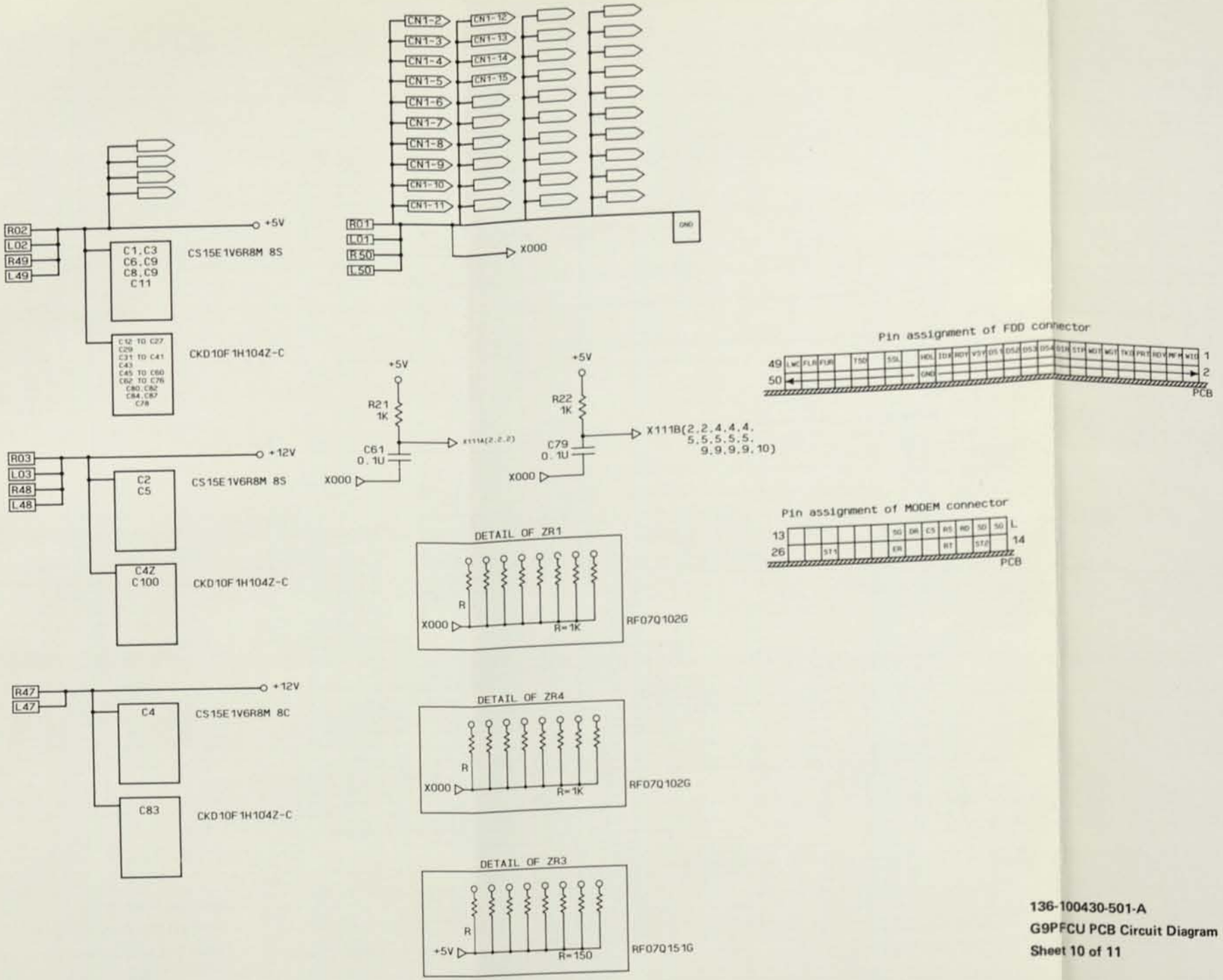
136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 7 of 11



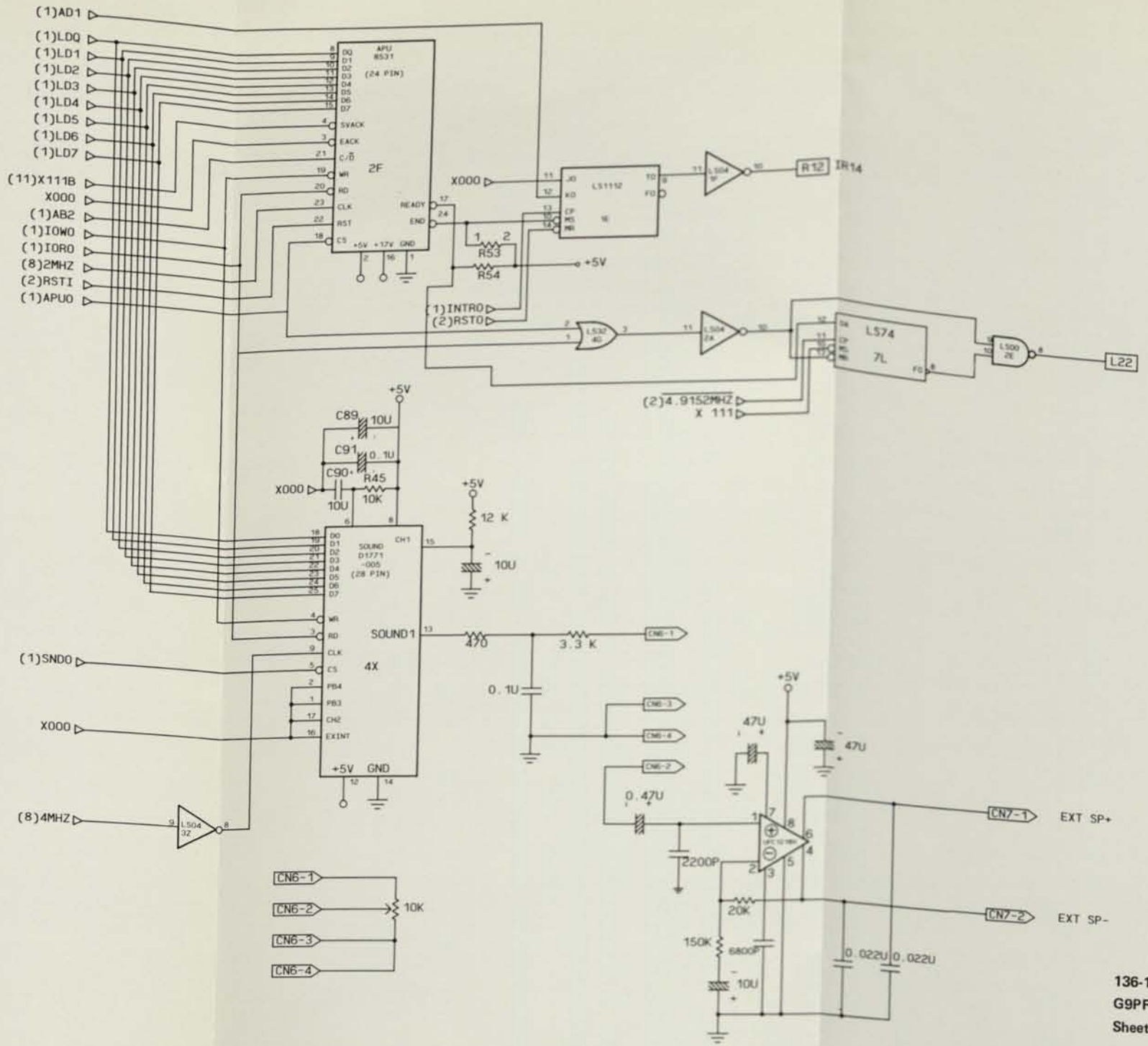
136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 8 of 11



136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 9 of 11

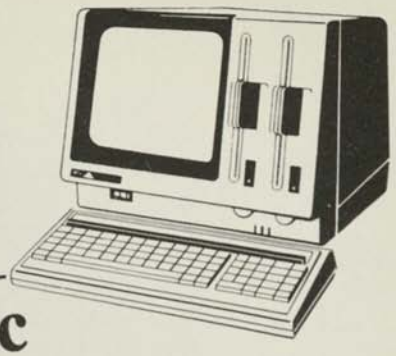


136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 10 of 11



136-100430-501-A
G9PFCU PCB Circuit Diagram
Sheet 11 of 11

PAL DECODING
SPECIFICATIONS



Appendix C

Programmable Array Logic Decoding Specifications

There are four Programmable Array Logic (PAL) devices in the APC, two on the Processor PCB and two on the Controller PCB. These devices are identified and listed in Table C-1. Tables C-2 to C-5 describes each PAL device in terms of its inputs and outputs.

Table C-1 Identification and Location of PAL Devices

STAMPED IDENTIFICATION	MANUFACTURER DATA	PCB LOCATION
PFB01C	MMI PAL 16L8 or Signetics N 82S153F	G9PFBU (Processor PCB) Location 7N
PFB02	MMI PAL 10L8	G9PFBU (Processor PCB) Location 1N
PFC01	MMI PAL 14L4 or Signetics N 82S153F	G9PFCU (Controller PCB) Location 2H
NMS02	MMI PAL 14L4	G9PFCU (Controller PCB) Location 2N

Table C-2 PFB01C Inputs/Outputs

INPUT		OUTPUT	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	A7	19	B0
2	A6	18	B1
3	A5	17	B2
4	A4	16	KB
5	A3	15	C0
6	A2	14	WAT
7	A1	13	CDMA0
8	A0	12	MBC
9	BHE0		
11	AE371		

$\overline{B0} = (\overline{A7}\cdot\overline{A6}\cdot\overline{A5}\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot\overline{A2}\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot\overline{A0}\cdot\overline{AE371})$

$\overline{B1} = (\overline{A7}\cdot\overline{A6}\cdot\overline{A5}\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot A3\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot A5\cdot\overline{A4}\cdot A3\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot\overline{A0}\cdot\overline{AE371})$

$\overline{B2} = (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot A3\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot A4\cdot A3\cdot\overline{A0}\cdot\overline{AE371}) + (A7\cdot A6\cdot A5\cdot A4\cdot A3\cdot A2\cdot A1\cdot A0\cdot AE371)$

$\overline{KB} = (\overline{A7}\cdot A6\cdot\overline{A5}\cdot\overline{A4}\cdot A3\cdot\overline{A0}\cdot\overline{AE371})$

$\overline{C0} = (\overline{A7}\cdot A6\cdot\overline{A5}\cdot A4\cdot A3\cdot\overline{A2}\cdot\overline{A1}\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A5}\cdot A4\cdot A3\cdot\overline{A2}\cdot\overline{BHE0}\cdot\overline{AE371})$

$\overline{WAT} = (\overline{A7}\cdot A6\cdot\overline{A5}\cdot A4\cdot A3\cdot\overline{A2}\cdot\overline{A1}\cdot\overline{A0}\cdot\overline{AE371})$

$\overline{MBC} = (\overline{A7}\cdot\overline{A6}\cdot\overline{A5}\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot\overline{A4}\cdot A3\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A4}\cdot A3\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot\overline{A6}\cdot A5\cdot A4\cdot A3\cdot\overline{A0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A5}\cdot A4\cdot A3\cdot\overline{A2}\cdot\overline{BHE0}\cdot\overline{AE371}) + (\overline{A7}\cdot A6\cdot\overline{A5}\cdot A4\cdot A3\cdot\overline{A2}\cdot\overline{A1}\cdot\overline{A0}\cdot\overline{AE371})$

$\overline{CDMA0} = (\overline{A7}\cdot\overline{A6}\cdot\overline{A5}\cdot\overline{BHE0}\cdot\overline{AE371})$

Table C-3 PFB02 Inputs/Outputs

INPUT		OUTPUT	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	MBCS	19	ROMS
2	DMC	18	RAMS
3	AB19	17	BMMS
4	AB18	16	BEXC
5	AB17	15	MRBS
6	MRD	14	DMA
7	IOR	13	MPR
8	MRQ	12	ITMM
9	AB0		
11	IMM		

$\overline{ROMS} = (AB19 \cdot AB18 \cdot AB17 \cdot \overline{MRD})$

$\overline{RAMS} = (\overline{AB19} \cdot \overline{AB18} \cdot \overline{AB17})$

$\overline{BMMS} = (AB19 \cdot \overline{AB18} \cdot AB17 \cdot MRQ)$

$\overline{BEXC} = (\overline{DMC} \cdot MRQ \cdot AB0)$

$\overline{MRBS} = (\overline{AB19} \cdot \overline{AB18} \cdot \overline{AB17} \cdot \overline{MRD})$

$\overline{DMA} = (\overline{DMC} \cdot \overline{IOR}) + (\overline{DMC} \cdot \overline{MRD} \cdot \overline{AB0} \cdot IMM)$

$\overline{MPR} = (DMC \cdot MBCS \cdot \overline{IOR}) + (DMC \cdot \overline{MRD} \cdot IMM)$

$\overline{ITMM} = (\overline{AB19} \cdot \overline{AB18} \cdot \overline{AB17}) + (AB19 \cdot AB17)$

Table C-4 PFC01 Inputs/Outputs

INPUT		OUTPUT	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	A0	19	LSI
2	A1	18	B0
3	A2	17	B1
4	A3	16	B2
5	A4	15	IO
6	A5	14	CS0
7	A6	12	CS1
8	DT/R		
9	BHE		
11	IOR		
13	IOW		

$$\overline{LSI} = (\overline{A6}\cdot A5\cdot A4\cdot\overline{A3}\cdot\overline{A2}\cdot A0) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A0) + (\underline{A6}\cdot\overline{A5}\cdot A4\cdot\underline{A3}\cdot\overline{A2}\cdot A0) + (A6\cdot\overline{A5}\cdot A4\cdot A3\cdot A1\cdot A0) + (\overline{A6}\cdot\underline{A5}\cdot\underline{A4}\cdot\underline{A3}\cdot\underline{A2}\cdot BHE) + (A6\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot\overline{A1}\cdot A0) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot BHE)$$

$$\overline{B0} = (\overline{A6}\cdot A5\cdot\underline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A0) + (A6\cdot\overline{A5}\cdot\underline{A4}\cdot\underline{A3}\cdot\underline{A1}\cdot\underline{A0}) + (\underline{A6}\cdot A5\cdot\overline{A4}\cdot\underline{A3}\cdot\underline{A2}\cdot\overline{A1}\cdot A0) + (A6\cdot\overline{A5}\cdot A4\cdot\overline{A3}\cdot\underline{A2}\cdot\underline{BHE}) + (\overline{A6}\cdot A5\cdot A4\cdot\overline{A3}\cdot A2\cdot\overline{A1}\cdot A0\cdot\overline{DT/R}) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot A3\cdot A2\cdot\overline{A1}\cdot A0\cdot\overline{DT/R}) + (A6\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A1\cdot A0)$$

$$\overline{B1} = (\underline{A6}\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A0) + (A6\cdot\overline{A5}\cdot\underline{A4}\cdot A3\cdot A1\cdot A0) + (\overline{A6}\cdot A5\cdot A4\cdot\underline{A3}\cdot\overline{A2}\cdot\underline{BHE}) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot BHE) + (\overline{A6}\cdot A5\cdot A4\cdot\overline{A3}\cdot A2\cdot\overline{A1}\cdot A0\cdot DT/R) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot\overline{A1}\cdot A0\cdot\overline{DT/R}) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot A0\cdot\overline{DT/R})$$

$$\overline{B2} = (A6\cdot\overline{A5}\cdot\underline{A4}\cdot\underline{A3}\cdot\overline{A2}\cdot\underline{A0}) + (\overline{A6}\cdot A5\cdot\underline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot BHE) + (\underline{A6}\cdot A5\cdot\overline{A4}\cdot\underline{A3}\cdot\overline{A2}\cdot A1\cdot A0) + (A6\cdot\overline{A5}\cdot A4\cdot\underline{A3}\cdot\underline{A2}\cdot\underline{BHE}) + (\overline{A6}\cdot A5\cdot A4\cdot\overline{A3}\cdot A2\cdot A1\cdot A0\cdot\overline{DT/R}) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot A0\cdot\overline{DT/R}) + (A6\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A1\cdot A0)$$

$$\overline{IO} = (\overline{A6}\cdot A5\cdot A4\cdot\overline{A3}\cdot A2\cdot\overline{A1}\cdot A0\cdot IOW) + (\overline{A6}\cdot\underline{A5}\cdot\underline{A4}\cdot\overline{A3}\cdot A2\cdot\overline{A1}\cdot A0\cdot IOR) + (\overline{A6}\cdot\underline{A5}\cdot\underline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot A0\cdot IOW) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\underline{A3}\cdot\underline{A2}\cdot\overline{A1}\cdot A0\cdot IOW) + (A6\cdot\overline{A5}\cdot\overline{A4}\cdot\overline{A3}\cdot A2\cdot A1\cdot A0\cdot IOW) + (A6\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A1\cdot A0\cdot IOW) + (A6\cdot A5\cdot\overline{A4}\cdot\overline{A3}\cdot\overline{A2}\cdot A1\cdot A0\cdot IOR)$$

$$\overline{CS0} = (A6\cdot A5\cdot A4)$$

$$\overline{CS1} = (\overline{A6}\cdot\overline{A5}\cdot A4)$$

Table C-5 NMS02 Inputs/Outputs

INPUT		OUTPUT	
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	CC7	17	ANK0
2	CC6	16	FULL1
3	CC5	15	BE0
4	CC4	14	BS0
5	CC3		
6	CC2		
7	CC1		
8	CC0		
9	M8960		
11	MRQ0		
12	MW0		
13	XNU		
18	XNU		
19	XNU		

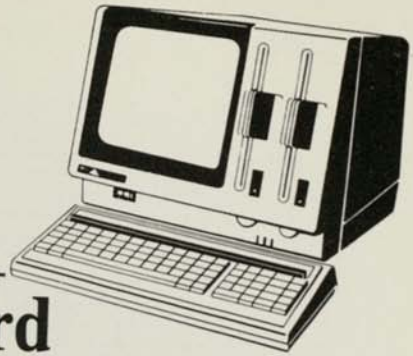
$\overline{ANK0} = (\overline{CC7} \cdot \overline{CC6} \cdot \overline{CC5} \cdot \overline{CC4} \cdot \overline{CC3} \cdot \overline{CC2} \cdot \overline{CC1} \cdot \overline{CC0})$

$$\overline{FULL1} = (\overline{CC6} \cdot \overline{CC5} \cdot \overline{CC4} \cdot CC3 \cdot \overline{CC2} \cdot \overline{CC1} \cdot \overline{CC0}) + (\overline{CC6} \cdot \overline{CC5} \cdot \overline{CC4} \cdot CC3 \cdot \overline{CC2} \cdot CC1 \cdot \overline{CC0}) + (\overline{CC6} \cdot \overline{CC5} \cdot \overline{CC4} \cdot CC3 \cdot \overline{CC2} \cdot \overline{CC1} \cdot CC0) + (\overline{CC6} \cdot \overline{CC5} \cdot \overline{CC4} \cdot CC3 \cdot CC2 \cdot \overline{CC1} \cdot \overline{CC0})$$

$\overline{BE0} = (\overline{M8960} \cdot \overline{MRQ0})$

$BS0 = (\overline{M8960} \cdot \overline{MRQ0} \cdot \overline{MW0})$

CHARACTER CODE
AND KEYBOARD



Appendix D

Character Code and Keyboard Information

This appendix gives important character code and keyboard information for the APC. The characters that can be generated and their associated codes are shown in Table D-1. The meanings of the ASCII special characters are given in Table D-2. Table D-3 lists the APC special characters that differ in representation from the ASCII standard, but the generated code is the same. A quick reference quide for easy association of the ASCII special characters and APC special characters is provided in Table D-4. The APC GRPH1 characters are shown in Figure D-1, the GRPH2 characters in Figure D-2.

Table D-1 Code Table

SECOND HEX DIGIT	FIRST HEX DIGIT															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUL 00	DLE 16	SP 32	0 48	@ 64	P 80	96	p 112	128	144	160	∞ 176	α 192	¢ 208	224	240
1	SOH 01	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113	129	145	≥ 161	3 177	ν 193	ω 209	225	241
2	STX 02	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114	130	146	• 162	τ 178	Δ 194	≈ 210	226	242
3	ETX 03	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115	131	147	* 163	4 179	β 195	√ 211	227	243
4	EOT 04	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116	132	148	≤ 164	5 180	ξ 196	7 212	228	244
5	ENQ 05	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117	133	149	/ 165	6 181	η 197	8 213	229	245
6	ACK 06	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118	134	150	• 166	∈ 182	θ 198	9 214	230	246
7	BEL 07	ETB 23	39	7 55	G 71	W 87	g 103	w 119	135	151	↑ 167	ρ 183	1 199	ι 215	231	247
8	BS 08	CAN 24	(40	8 56	H 72	X 88	h 104	x 120	136	152	½ 168	σ 184	± 200	ϕ 216	♠ 232	248
9	HT 09	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121	137	153	↓ 169	ψ 185	υ 201	≠ 217	♥ 233	249
A	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122	138	154	← 170	Ω 186	π 202	χ 218	♦ 234	250
B	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123	139	155	→ 171	Γ 187	∧ 203	° 219	♣ 235	251
C	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| 124	140	156	+ 172	0 188	2 204	0 220	● 236	252
D	CR 13	GS 29	— 45	= 61	M 77	] 93	m 109	} 125	141	157	(173	δ 189	⊕ 205	ζ 221	○ 237	253
E	SO 14	RS 30	. 46	> 62	N 78	∧ 94	n 110	~ 126	142	158	) 174	κ 190	¯ 206	λ 222	238	254
F	SI 15	US 31	/ 47	? 63	O 79	— 95	o 111	DEL 127	143	159	¼ 175	Σ 191	τ 207	μ 223	239	255

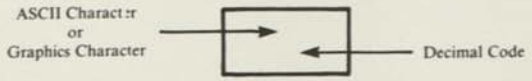


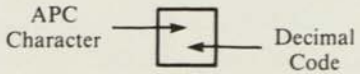
Table D-2 ASCII Special Characters

CODE	MEANING
NUL	Null
SOH	Start of Heading
STX	Start Text
ETX	End Text
EOT	End of Transmission
ENQ	Enquiry
ACK	Acknowledge
BEL	Bell
BS	Backspace
HT	Horizontal Tab
LF	Line Feed
VT	Vertical Tab
FF	Form Feed
CR	Carriage Return
SO	Shift Out
SI	Shift In
DLE	Data Link Escape
DC1	Device Control 1
DC2	Device Control 2
DC3	Device Control 3
DC4	Device Control 4
NAK	Negative Acknowledge
SYN	Synchronous Idle
ETB	End Transmission Block
CAN	Cancel
EM	End of Medium
SUB	Substitute
ESC	Escape
FS	Form Separator
GS	Group Separator
RS	Record Separator
US	Unit Separator
SP	Space
DEL	Delete

NOTE: These codes are not displayed on the APC as shown. Some of these codes are not used by the APC, but the unused codes can still be transmitted for use by other devices.

Table D-3 APC Special Characters

SECOND HEX DIGIT	FIRST HEX DIGIT	
	0	1
0	00	16
1	01	17
2	02	18
3	03	19
4	04	20
5	05	21
6	06	22
7	07	23
8	08	24
9	09	25
A	10	26
B	11	27
C	12	28
D	13	29
E	14	30
F	15	31

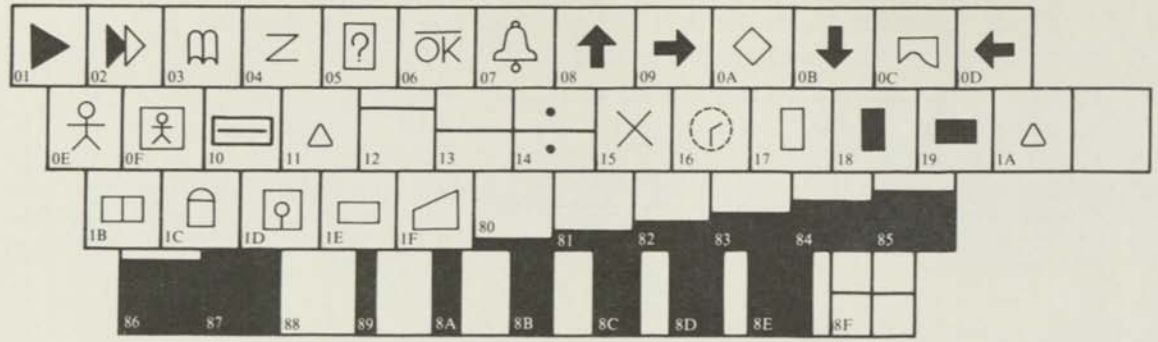


NOTE: Only characters that are not associated with a specific APC function are displayed on the screen.

Table D-4 Quick Reference Guide for ASCII Special Character/APC Special Character Association

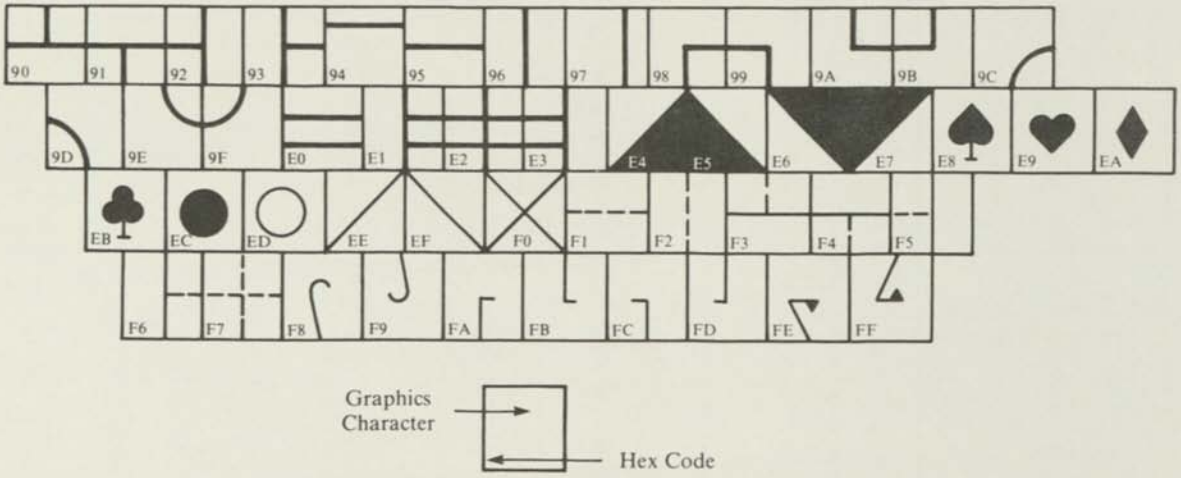
ASCII SPECIAL CHARACTER	APC SPECIAL CHARACTER
NUL	
SOH	
STX	
ETX	
EOT	
ENQ	
ACK	
BEL	
BS	
HT	
LF	
VT	
FF	
CR	
SO	
SI	
DLE	
DC1	
DC2	
DC3	
DC4	
NAK	
SYN	
ETB	
CAN	
EM	
SUB	
ESC	
FS	
GS	
RS	
US	
SP	
DEL	

NOTE: Characters associated with a specific APC function are not displayed.



NOTE: Characters associated with a specific APC function are not displayed.

A. UNSHIFTED (SHIFT KEY UP)



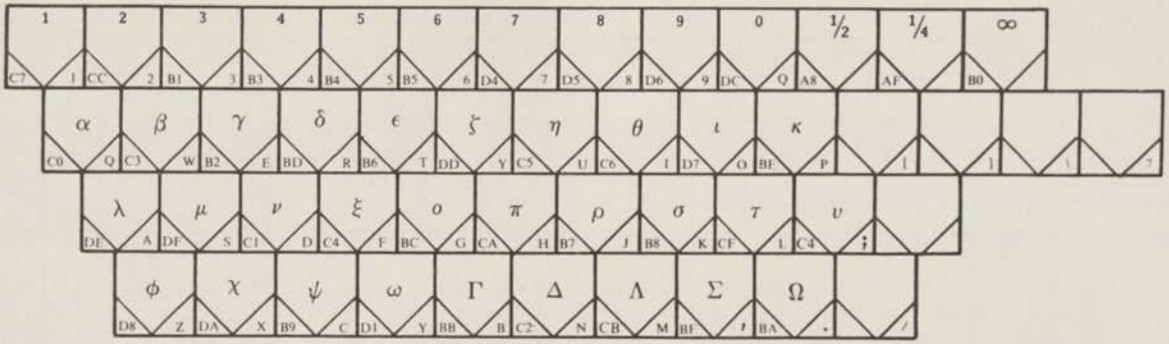
B. SHIFTED (SHIFT KEY DOWN)

NOTES: 1 GRPH1 CHARACTERS ARE PRODUCED WHEN THE GRPH1 KEY IS PRESSED.

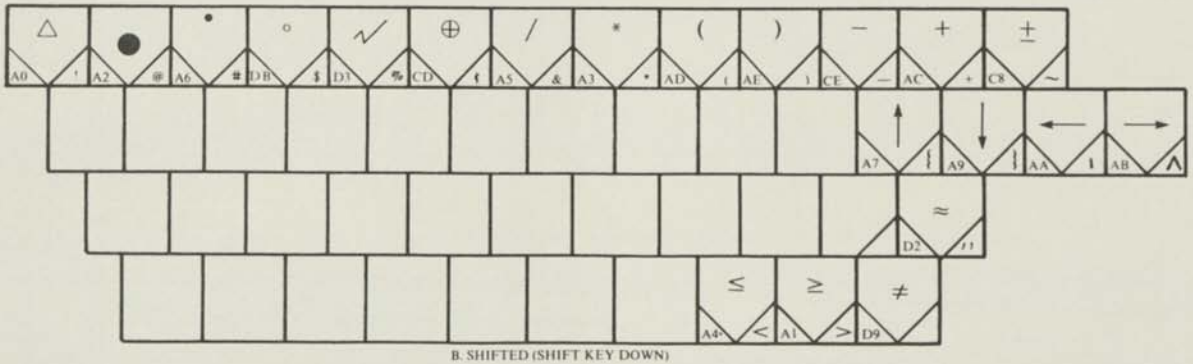
2 GRAPHICS SYMBOLS ASSOCIATED WITH A SPECIFIC APC FUNCTION ARE NOT DISPLAYED ON THE SCREEN. INSTEAD, THE FUNCTION IS PERFORMED.

3 THE ALPHANUMERIC SYMBOLS ASSOCIATED WITH THE GRAPHIC SYMBOLS ARE THE HEXADECIMAL (HEX) CODES GENERATED BY PRESSING THE KEYS.

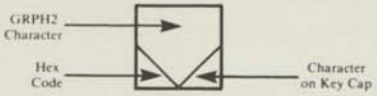
Figure D-1 APC GRPH1 Characters



A. UNSHIFTED (SHIFT KEY UP)

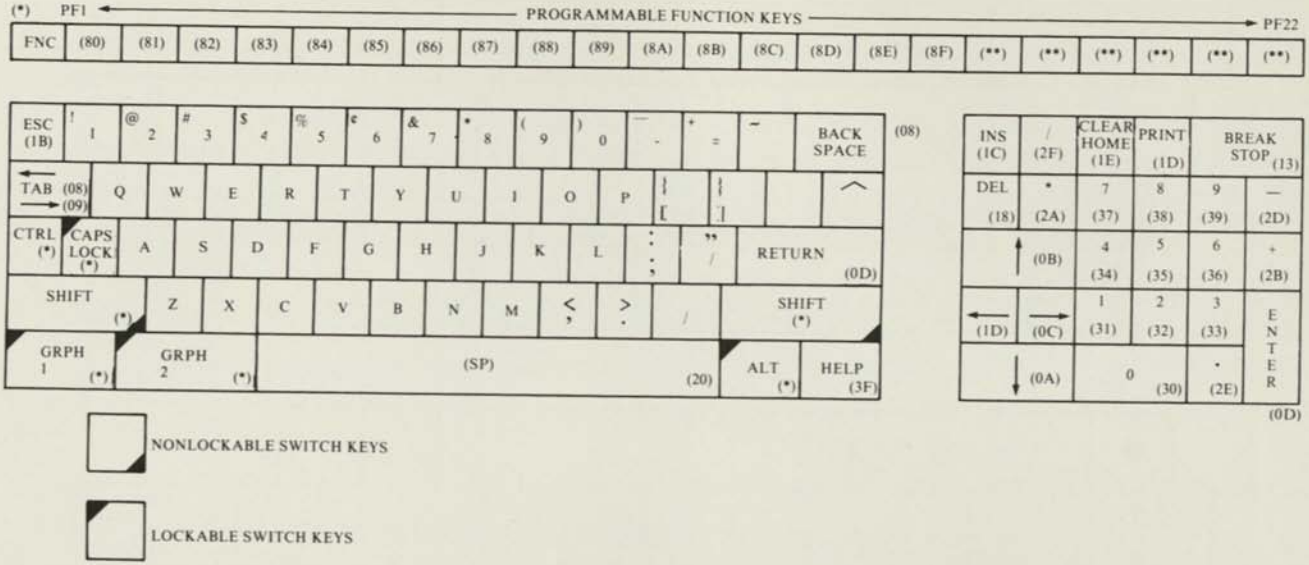


B. SHIFTED (SHIFT KEY DOWN)



NOTE: GRPH2 CHARACTERS ARE PRODUCED WHEN THE GRPH2 KEY IS PRESSED

Figure D-2 APC GRPH2 Characters



NOTES: 1. HEX NUMBERS IN PARENTHESES DESIGNATE HEX CODES.

2. FOR HEX CODES OF STANDARD ALPHANUMERIC CHARACTERS, SEE TABLE D-1.

3. KEYS WITH (*) MUST BE USED WITH ANOTHER KEY TO GENERATE A CODE.

4. "SHIFT" OR "CTRL" PLUS "BREAK STOP" GENERATES HEX CODE 03.

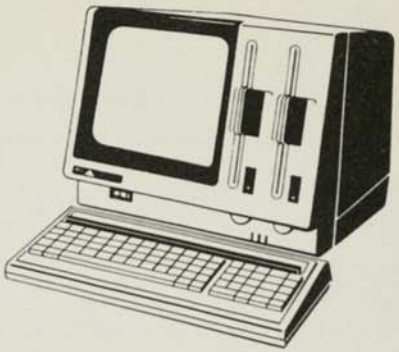
5. KEYS WITH (**) (PF17 TO PF22) GENERATE THE SPECIAL CODES SHOWN BELOW.

	PF17	ESC O O
	PF18	ESC O P
	PF19	ESC O Q
	PF20	ESC O R
	PF21	ESC O S
	PF22	ESC O T
FNC	PF17	ESC O U
FNC	PF18	ESC O V
FNC	PF19	ESC O W
FNC	PF20	ESC O X
FNC	PF21	ESC O Y
FNC	PF22	ESC O Z

Figure D-3 Keyboard Layout Showing Hex Codes For Special Keys

I/O ADDRESSES
AND INSTRUCTIONS

I/O ADDRESSES
AND INSTRUCTIONS



Appendix E

I/O Port Addresses and Instructions

The I/O port addresses and instructions for all devices are listed in Tables E-1 to E-21.

Data bus bit descriptions are listed left to right as Bits 7 through 0 for low order bytes and Bits 15 through 8 for high order bytes.

Table E-1 I/O Port Address and Instructions for the DMA Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS
CH0 Address Read	R	01	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH0 Address Write	W	01	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH0 Word Count R.	R	11	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH0 Word Count W.	W	11	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH1 Address Read	R	03	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH1 Address Write	W	03	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH1 Word Count R.	R	13	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH1 Word Count W.	W	13	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH2 Address Read	R	05	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH2 Address Write	W	05	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH2 Word Count R.	R	15	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH2 Word Count W.	W	15	W7 W6 W5 W4 W3 W2 W1 W0 W15 W14 W13 W12 W11 W10 W9 W8
CH3 Address Read	R	07	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8
CH3 Address Write	W	07	A7 A6 A5 A4 A3 A2 A1 A0 A15 A14 A13 A12 A11 A10 A9 A8

Table E-1 I/O Port Address and Instructions for the DMA Controller (cont'd)

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
CH3 Word Count	R	17	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8
CH3 Word Count	W	17	W7 W15	W6 W14	W5 W13	W4 W12	W3 W11	W2 W10	W1 W9	W0 W8
DMA Status Read	R	09	RQ3	RQ2	RQ1	RQ0	TC3	TC2	TC1	TC0
DMA Command Write	W	09	KS	DS	WS	PR	TM	CE	AH	MM
Illegal	R	19	—	—	—	—	—	—	—	—
Write Request Register	W	19	—	—	—	—	—	RB	CS1	CS0
Illegal	R	0B	—	—	—	—	—	—	—	—
Write Single Mask	W	0B	—	—	—	—	—	MK	CS1	CS0
Illegal	R	1B	—	—	—	—	—	—	—	—
Write Mode	W	1B	MS1	MS0	ID	AT	TR1	TR0	CS1	CS0
Illegal	R	0D	—	—	—	—	—	—	—	—
Clear F/F	W	0D	—	—	—	—	—	—	—	—
Read Temporary Register	R	1D	D7	D6	D5	D4	D3	D2	D1	D0
Master Clear	W	1D	—	—	—	—	—	—	—	—
Illegal	R	0F	—	—	—	—	—	—	—	—
Illegal	W	0F	—	—	—	—	—	—	—	—
Illegal	R	1F	—	—	—	—	—	—	—	—
Write All Mask	W	1F	—	—	—	—	MB3	MB2	MB1	MB0

Table E-2 I/O Port Addresses and Instructions for the Interrupt Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read IRR/ISR/IRL	R	20	D7	D6	D5	D4	D3	D2	D1	D0
OCW2	W	20	R	SL	EOI	0	0	L2	L1	L0
OCW3	W	20	0	ESM	SMM	0	1	P	PR	RIS
ICW1	W	20	0	0	0	1	0	0	0	1
Read Mask R.	R	22	—	M6	M5	M4	M3	M2	M1	M0
OCW1	W	22	—	M6	M5	M4	M3	M2	M1	M0
ICW2	W	22	T7	T6	T5	T4	T3	0	0	0
ICW3	W	22	1	0	0	0	0	0	0	0
ICW4	W	22	0	0	0	0	0	0	0	1
	R	24								
	W	24								
	R	26								
	W	26								
Read IRR/ISR/IRL	R	28	D7	D6	D5	D4	D3	D2	D1	D0
OCW2	W	28	R	SL	EOI	0	0	L2	L1	L0
OCW3	W	28	0	ESM	SMM	0	1	P	PR	RIS
ICW1	W	28	0	0	0	1	0	0	0	1
Read Mask R.	R	2A	M14	M13	M12	M11	M10	M9	M8	M7
OCW1	W	2A	M14	M13	M12	M11	M10	M9	M8	M7
ICW2	W	2A	T7	T6	T5	T4	T3	0	0	0
ICW3	W	2A	0	0	0	0	0	1	1	1
ICW4	W	2A	0	0	0	0	0	0	0	1

Table E-3 I/O Port Addresses and Instructions for the Interval Timer

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Counter 0	R	29	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Load Counter 0	W	29	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Read Counter 1	R	2B	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Load Counter 1	W	2B	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Read Counter 2	R	2D	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
Load Counter 2	W	2D	C7 C15	C6 C14	C5 C13	C4 C12	C3 C11	C2 C10	C1 C9	C0 C8
No Operation	R	2F	—	—	—	—	—	—	—	—
Write Mode	W	2F	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Table E-4 I/O Port Addresses and Instructions for the Serial I/O Communications Controller Number 1

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Data	R	30	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Write Data	W	30	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Read Status	R	32	DR	SYN	FE	OE	PE	TE	RR	TR
Write Mode (A)	W	32	S2	S1	EP	PEN	L2	L1	B2	B1
Write Mode (S)	W	32	SCS	ESD	EP	PEN	L2	L1	0	0
Write Command	W	32	EH	IR	RS	RST	SBR	REN	ER	TEN
Write Mask	W	34	0	0	0	0	0	TXE	RXR	TXR
Read Signal	R	34	—	—	—	—	—	CS	CI	CD
Write Signal	W	36	0	0	0	0	0	0	0	TDC
	R	36								

Table E-5 I/O Port Addresses and Instructions for the Serial I/O Communications Controller Number 2

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Data	R	31	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1
Write Data	W	31	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Read Status	R	33	DR	SYN	FE	OE	PE	TE	RRDY	TRDY
Write Mode (A)	W	33	S2	S1	EP	PEN	L2	L1	B2	B1
Write Mode (S)	W	33	SCS	ESD	EP	PEN	L2	L1	B2	B1
Write Command	W	33	EH	IR	RS	RST	SBR	REN	ER	TEN
Write Mask	W	35	0	0	0	0	0	TXE	RXR	TXR
Read Signal	R	35	—	—	—	—	SCA	CS	CI	CD
Write Signal	W	37	0	0	0	0	0	0	0	TDC

Table E-6 I/O Port Addresses and Instructions for the DMA Address Registers

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS
CH0 Read Address R.	R	38	
CH0 Write Address R.	W	38	0 0 0 0 A19 A18 A17 A16
CH1 Read Address	R	3A	
CH1 Write Address R.	W	3A	0 0 0 0 A19 A18 A17 A16
CH2 Read Address	R	3C	
CH2 Write Address R.	W	3C	0 0 0 0 A19 A18 A17 A16
CH3 Read Address	R	3E	
CH3 Write Address R.	W	3E	0 0 0 0 A19 A18 A17 A16

Table E-7 I/O Port Addresses and Instructions for the CRT Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS
Read Status	R	40	LP HP VS DMA DW FE FF DR
Write Parameter	W	40	P7 P6 P5 P4 P3 P2 P1 P0
Read Data	R	42	D7 D6 D5 D4 D3 D2 D1 D0
Write Command	W	42	C7 C6 C5 C4 C3 C2 C1 C0
Reset Intr.	W	46	GDC TM APU CRT

Table E-8 I/O Port Addresses and Instructions for the Graphics Display Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Status	R	70	LP	HB	VS	DMA	DW	FE	FF	DR
Write Parameter	W	70	P7	P6	P5	P4	P3	P2	P1	P0
Read Data	R	72	D7	D6	D5	D4	D3	D2	D1	D0
Write Command	W	72	C7	C6	C5	C4	C3	C2	C1	C0
Graph Enable	W	76	—	—	—	—	—	—	—	1/0

NOTE: For Graph Enable, 1 = Release From Blanking Status; 0 = Blanking Always. At power on, Blanking Always is selected.

Table E-9 I/O Port Addresses and Instructions for the Keyboard Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Data	R	48	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Buzzer Set	W	48	—	—	—	—	—	—	—	—
Read Status	R	4A					TP2	TP1	TP0	ALM
Buzzer Reset	W	4A	—	—	—	—	—	—	—	—
Read Signal	R	4C	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
Read Book/Page	R	4E	B4	B3	B2	B1	P4	P3	P2	P1
Read Shift	R	4E	0	0	0	0	SF4	SF3	SF2	SF1

Table E-10 I/O Port Addresses and Instructions for the FDD Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Status	R	50	RQM	DIO	NDM	FCB	F3B	F2B	F1B	F0B
Read Data	R	52	D7	D6	D5	D4	D3	D2	D1	D0
Write Command	W	52	C7	C6	C5	C4	C3	C2	C1	C0

Table E-11 I/O Port Addresses and Instructions for the Clock and Calendar

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Data	R	58	—	—	—	—	—	—	BATTDO	
Set Register	W	58	0	0	DI	CLK	STB	C2	C1	C0

Table E-12 I/O Port Address and Instruction for the BBM Enable

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS
BBM Enable	W	59	ENB

Table E-13 I/O Port Addresses and Instructions for the APU

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Data	R	5A	D7	D6	D5	D4	D3	D2	D1	D0
Write Data	W	5A	D7	D6	D5	D4	D3	D2	D1	D0
Read Status	R	5E	B	S	Z	E3	E2	E1	E0	CRY
Write Command	W	5E	C7	C6	C5	C4	C3	C2	C1	C0

Table E-14 I/O Port Address and Instruction for the Power Off Control

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS
Power Off	W	5B	OFF

Table E-15 I/O Port Addresses and Instructions for the Sound Control

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Write Command	W	60	0	FS	C5	C4	C3	C2	C1	C0
Read Status	R	60	S7	S6	S5	S4	S3	S2	S1	S0

Table E-16 I/O Port Addresses and Instructions for the Timer

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Counter 0	R	61	C7	C6	C5	C4	C3	C2	C1	C0
			C15	C14	C13	C12	C11	C10	C9	C8
Load Counter 0	W	61	C7	C6	C5	C4	C3	C2	C1	C0
			C15	C14	C13	C12	C11	C10	C9	C8
		63								
		63								
		65								
		65								
		67								
Write Mode	W	67	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Table E-17 I/O Port Addresses and Instructions for the ODA Controller Number 1

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Signal	R	68	$\overline{DCN}$	0	0	ALM	$\overline{RMR}$	0	DPQ	MDL
Write Data	W	6A	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1
Write Signal 2	W	6C	IRT			MASK				
Write Signal 0	W	6E	1	0	0	1	0	1	0	0
Write Signal 1	W	6E	0	0	0	0	0	1	0	INTE
Write Signal 1	W	6E	0	0	0	0	0	1	1	RMS
Write Signal 1	W	6E	0	0	0	0	1	0	0	MASK
Write Signal 1	W	6E	0	0	0	0	1	1	1	IRT

Table E-18 I/O Port Addresses and Instructions for the IDA Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Read Signal	R	71	$\overline{DCN}$	IP3	IP2	PSM	$\overline{SMR}$	IP1	SDRQ	STT
Read Data	R	73	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Write Signal 2	W	75	IRT	SDR	SMS	MASK				
Write Signal 0	W	77	1	0	0	1	0	1	1	0
Write Signal 1	W	77	0	0	0	0	0	1	0	INTE
Write Signal 1	W	77	0	0	0	0	1	0	0	MASK
Write Signal 1	W	77	0	0	0	0	1	0	1	SMS
Write Signal 1	W	77	0	0	0	0	1	1	0	SDR
Write Signal 1	W	77	0	0	0	0	1	1	1	IRT
Write Signal 3	W	79								SDA

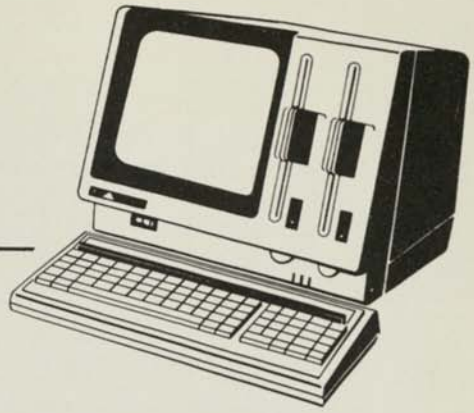
Table E-19 I/O Port Addresses and Instructions for the Communications Adapter

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Write BUF1	W	80	D7	D6	D5	D4	D3	D2	D1	D0
Read BUF4	R	80	D7	D6	D5	D4	D3	D2	D1	D0
Write BUF2	W	82	D7	D6	D5	D4	D3	D2	D1	D0
Read BUF5	R	82	D7	D6	D5	D4	D3	D2	D1	D0
Write BUF3	W	84	D7	D6	D5	D4	D3	D2	D1	D0
Read BUF6	R	84	D7	D6	D5	D4	D3	D2	D1	D0
Start DMA	W	86	—	—	—	—	—	—	—	—
Set INT1	W	88	—	—	—	—	—	—	—	—
Reset INT2	W	8A	—	—	—	—	—	—	—	—
Reset SDMA INT	W	8C	—	—	—	—	—	—	—	—
Reset RDMA INT	W	8E	—	—	—	—	—	—	—	—
Read INT	R	90	—	—	—	—	INT1	INT2	MSDE	MRDE

Table E-20 I/O Port Addresses and Instructions for the ASOP Controller

INSTRUCTION	READ/ WRITE	I/O ADDRESS	DATA BUS							
Low Address Set	W	F0	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Mid Address Set	W	F2	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
High Address Set	W	F4					SA19	SA18	SA17	SA16
Mask Set	W	F6								MASK
Read Signal	R	F6							R/W	INT

HARDWARE
SPECIFICATIONS



Appendix F

Hardware Specifications

FEATURE	SPECIFICATION
CPU*	NEC μPD 8086
Word Length	16 bits
Clock Rate	5 MHz
ROM*	8K (bootstrap and self-test)
RAM	64K chips, 200 ns Access Time
Standard Size*	128 KB
Maximum Size	256 KB
Memory with Battery Backup*	4 K (CMOS) Two-year life Can be protected against accidental writing
I/O Facilities	
Standard*	
Printer	Parallel
RS-232C	Asynchronous and Synchronous at speeds up to 19,200 bps
Optional	Software Emulators for all important IBM Workstations and Communications subsystems Second RS-232C Port
Other Standard Features*	
Music	Pitch Range: 2 + Octaves Number of Tempos: 4 Note Duration: thirty-second to whole Dynamics: piano, medium, forte accent

*Standard Feature, included with Basic Unit

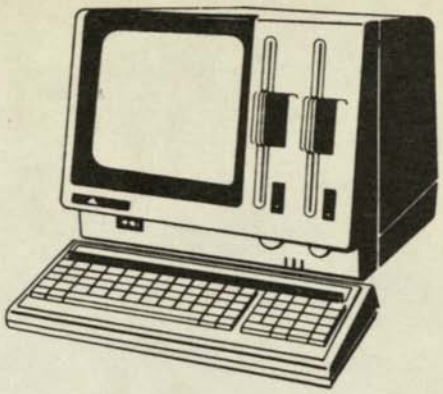
FEATURE	SPECIFICATION
Other Standard Features* (cont.)	
Alarm	Pitch: 4 selectable frequencies Length: 20 ms or continuous Loudness: 3 levels
Clock/Calendar	Hardware (with battery backup)
Automatic Power Off	Can be initiated locally or remotely
Lithium Battery	Backs up CMOS RAM and Clock/Calendar Two-year life
Flexible Disk Drives*	
Packaging	Integrated (one* or two)
Size	8 in.
Formatted Capacity (each)	
Single-Sided, Single-Density	243 KB } Both supported
Double-Sided, Double-Density	1 MB } Both supported
Standard Number of Drives	monochrome model - one color model - two
Maximum Number of Drives	two
Maximum Disk Capacity	2 MB
Disk Performance Characteristics	
Rotation Rate	360 rpm
Head Settle Time	50 ms
Track-track Time	5 ms
Transfer Rate	62.5 KB/sec
Display Screen*	
Size (Diagonal)	12 in.
Lines x Columns	25 x 80 plus status line
Character Set	
Predefined*	250 Symbols (8 x 19 matrix)
User-Definable*	256 Symbols (all displayable and printable)
Monochrome* Phosphor Type	Green Black
Video Interface	Integrated CRT Display
Color	8-color (high res. 640 x 475 pixels)
Virtual Graphic Area Size	1,024 x 1,024 pixels
Real Graphic Window Size	640 x 475 pixels — 8-color

*Standard Feature, included with Basic Unit

FEATURE	SPECIFICATION
Display Screen* (cont.)	
Character Graphics*	Overline, underline, vertical line, highlight, inverse video, blinking, secret
Line Drawing	Line segment, rectangle, arc, circle
Keyboard*	
Number of Keys (excluded in Programmable Function Keys)	86
Number of Programmable Function Keys	22, Dual Mode (effectively, 44)
Numeric Pad	Standard
Standard Printer	
Type	Dot Matrix
Speed	100 Characters per second
Controller*	Standard
Dimensions	
Main Enclosure	19.7 in. (50 cm) wide x 13.8 in. (35 cm) high x monochrome: 18.1 in. (46 cm) deep color: 19.9 in. (50.5 cm) deep.
Keyboard	19.7 in. (50 cm) wide x 2.4 in. (6 cm) high x 9.1 in. (23 cm) deep

*Standard Feature, included with Basic Unit

Advanced
Personal Computer



APC-H31/H32 Memory Expansion Unit Installation Guide

NEC
NEC Information Systems, Inc.
819-000104-9001 Rev. 01
4-84

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AND
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NEC Information Systems, Inc. (NECIS) products are warranted in accordance with the terms of the applicable NEC Information Systems, Inc. product specification. Product performance is affected by system configuration, software, the application, customer data, and operator control of the system among other factors. While NECIS products are considered to be compatible with most systems, the specific functional implementation by customers of the product may vary.

Therefore, the suitability of a product for a specific application must be determined by the customer and is not warranted by NECIS.

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Contents

Illustrations

Tables

This guide shows you how to install your new APC-H31 Memory Expansion Unit, and also how to set switches, if necessary, to make the unit compatible with your particular APC system.

To increase your APC's system's memory capacity above 128K bytes to 256K bytes, you can install the standard APC-H31 Memory Expansion Unit. If you wish to further increase the memory capacity of the standard APC-H31, you can install an additional memory kit, the APC-H32, on the APC-H31 board.

APC-H31 MEMORY EXPANSION UNIT

The APC-H31 Memory Expansion Unit is a printed circuit board (PCB), G9SNB, containing 18 dynamic random-access memory (RAM) integrated circuits (ICs) soldered on the board (see Figure 1).

The combined amount of memory provided by these ICs is 128K bytes. Additional memory ICs can be added to the APC-H31 in increments of 128K by installing APC-H32 Memory Kits.

APC-H32 128K MEMORY KIT

Each APC-H32 Memory Kit contains 18 dynamic RAM ICs. Each kit expands the memory capacity of the APC-H31 board by 128K bytes. It is possible to install up to two APC-H32 kits on the APC-H31 board. The ICs in the kit are easily inserted into socket sets 1 and 2 (see Figure 1).

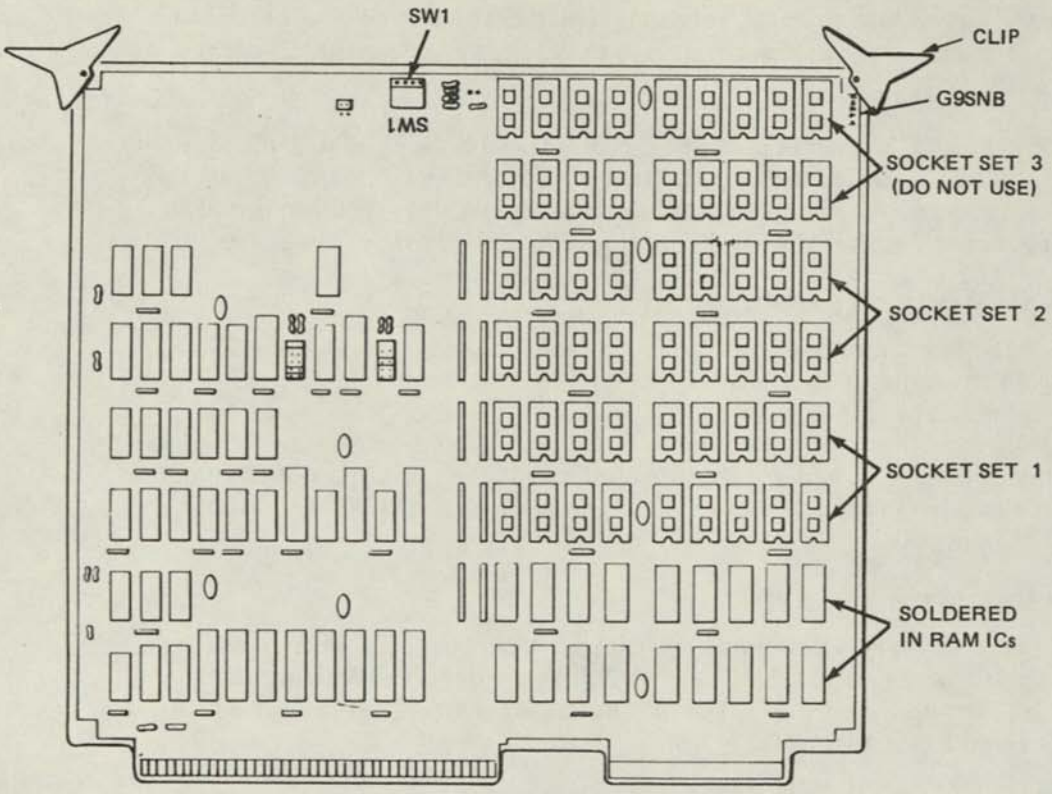


Figure 1. The APC-H31 Memory Expansion Unit PCB (G9SNB)

WHERE TO START

Before you can install the APC-H31/H32 Memory Expansion Unit, you must do the following:

- unpack it
- determine which revision you own
- calculate existing system memory
- add the APC-H32 kit (if you have one)
- check the total system memory
- and set switches, if necessary.

These procedures are described in the following paragraphs. To avoid a system failure, perform the six easy preparation procedures in the order given.

UNPACKING

Carefully remove the APC-H31 Memory Expansion Unit PCB from the packing materials.

DETERMINING WHICH REVISION YOU HAVE

To determine whether you own Revision (Rev.) 1 or 2, use the following procedure.

1. Locate the red slider switch SW1 on the APC-H31 PCB (see Figure 1).
   Rev. 1 has four slider switches (see Figure 2).
   Rev. 2 has eight slider switches (see Figure 3).
2. Check the revision you own based on the number of slider switches in SW1.

CHECK HERE	YOU OWN
The board has four slider switches.	Rev. 1
The board has eight slider switches.	Rev. 2.

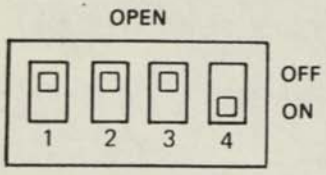


Figure 2 Revision 1 SW1

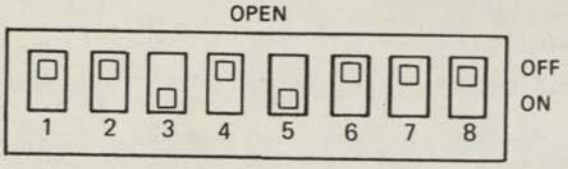


Figure 3 Revision 2 SW1

CALCULATING EXISTING SYSTEM MEMORY

There are two reasons why you must determine your "Existing System Memory" before adding the APC-H31 unit: First, knowing your system's existing memory lets you set the switches properly; second, you will be able to determine the number of memory expansion APC-H32 kits you can install on the APC-H31 PCB without exceeding the 512K system limit.

To calculate the "Existing System Memory" proceed as follows:

1. Check off the memory options your system now supports (see Table 1).
2. Calculate the "Existing System Memory" by multiplying the number of checks by 128K (see Table 1). This total represents the "Existing System Memory" before adding the APC-H31 unit. Notice that the APC base is checked off for you. Include this check in your total.

Table 1 Calculating Existing System Memory

MEMORY UNIT	MEMORY AMOUNT	CHECK HERE
APC BASE	128K	√
APC H08	128K	
APC H11/12	128K	

TOTAL CHECKS (including APC base)	

X 128K

EXISTING SYSTEM MEMORY = ____

NOTE

If you are not adding APC-H32 ICs to the APC-H31 PCB, skip to CHECKING THE TOTAL SYSTEM MEMORY.

ADDING ADDITIONAL MEMORY ICs (APC-H32)

If you wish to install the APC-H32 Memory Kit or kits, check Table 2 to determine the amount of memory you can add to the board.

The total APC system memory must not exceed 512K bytes. Exceeding the 512K limit will cause a system failure. Follow the suggested memory expansion possibilities in Table 2.

Table 2 Possible Memory Expansion

EXISTING SYSTEM MEMORY (From Table 1)	POSSIBLE EXPANSION
128K	Can fill socket sets 1 & 2 (Two APC-H32 128K memory kits)
256K	Can fill socket set 1 (One APC-H32 128K memory kit)
384K	Cannot add APC-H32 ICs to the APC-H31 board

Installing the APC-H32 128K Memory Kit

To install the APC-H32 Memory Kit, do the following procedure.

1. Carefully remove the APC-H32 kit from the packing materials. Each kit contains 18 ICs.
2. Lay the APC-H31 PCB down with the chip side up and the blue clips on top (see Figure 4).

   Notice that there are six rows of blue sockets (nine to a row, 18 to a set).

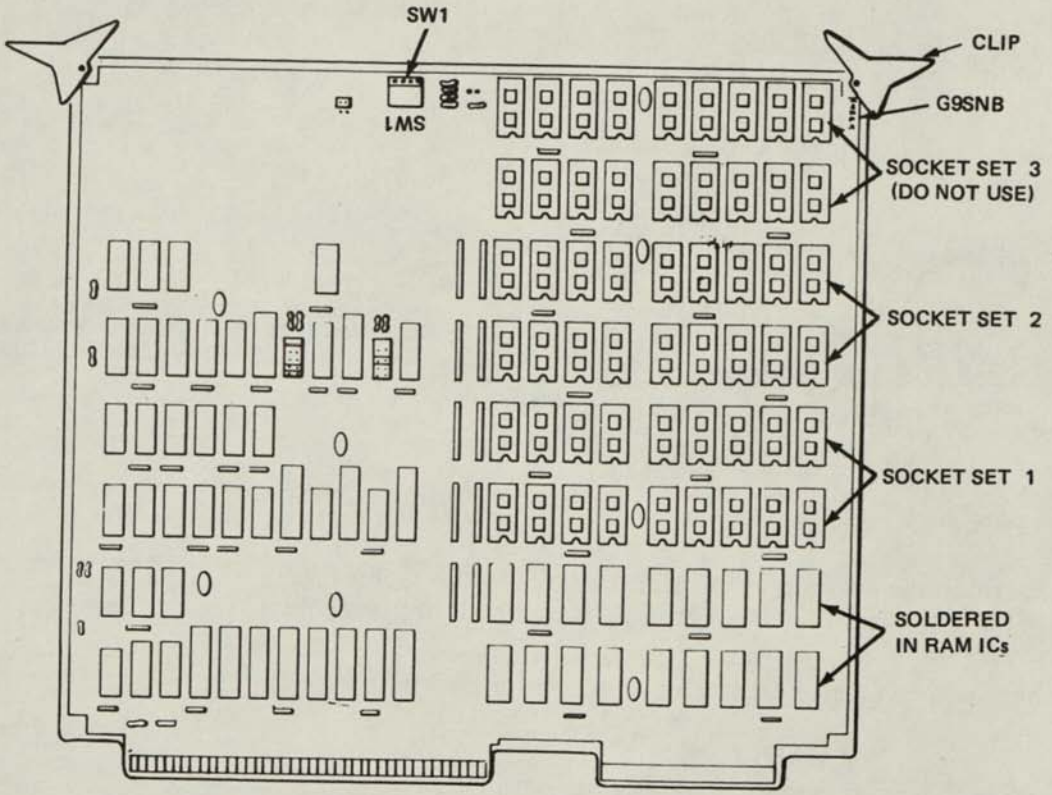


Figure 4 The APC-H31 Memory Expansion Unit PCB (G9SNB)

CAUTION

Static electricity can damage ICs. Avoid static electricity while handling ICs.

3. Gently remove the ICs from the package. Do not bend the pins on the ICs during installation.
4. Align the notch in the IC over the notch in the socket (see Figure 5).

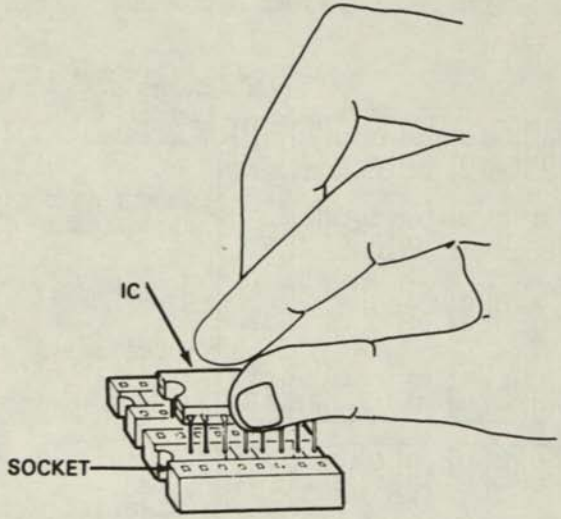


Figure 5 Inserting the IC into the Socket

5. Carefully position the pins on the IC over the holes in the socket before pressing the IC into the position (see Figure 5). Press firmly until the chip is seated in the socket fully.

   Fill rows one and two (socket set 1) with the 18 ICs in the kit.

CAUTION

FILL ONLY AS MANY SOCKET SETS AS INDICATED IN TABLE 2.

Do not fill rows five and six (socket set 3). This can cause a system failure).

6. If you are installing two APC-H32 kits, fill the next two rows (socket set 2) with 18 ICs.

CHECKING THE TOTAL SYSTEM MEMORY

The maximum amount of memory allowed in the APC system is 512K bytes. Use table 3 to determine your total system memory.

Find your "Existing System Memory" (as determined in Table 1). Then check off the line that represents what you are adding. Your answer is figured for you under "Your Total System Memory Is".

CAUTION

The total system memory must not exceed 512K bytes or a system failure will occur.

Table 3 Total System Memory

LINE #	EXISTING MEMORY (From Table 1)	ADDING H31	ADDING H32	CHECK OFF LINE THAT APPLIES	YOUR TOTAL SYSTEM MEMORY IS
1	128K	YES	NO		256K
2	265K	YES	NO		384K
3	384K	YES	NO		512K
4	128K	YES	ONE		384K
5	128K	YES	TWO		512K
6	256K	YES	ONE		512K
7	384K	YES	NO		512K

NOTE

This section applies to Revision 1 only. Skip to "Revision 2 Switch Settings," if you have Revision 2.

REVISION 1 SWITCH SETTINGS

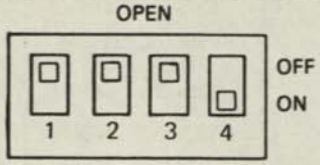
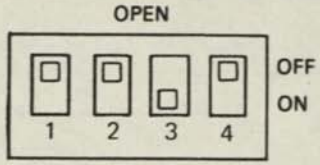
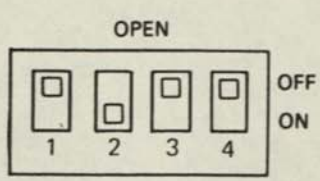
Before installing the APC-H31 Rev. 1 board, you must set slider switches SW1 and move jumper TM3.

Setting Revision 1 Slider Switches

To set the four slider switches SW1, perform the following procedure.

1. Look up your "Existing System Memory" from Table 1.
2. Match your total from Table 1 with the "Existing System Memory" in Table 4.
3. Set switches or verify switch settings that apply to your "Existing System Memory" (see Table 4).

Table 4 Revision 1 Slider Switch SW1 Positions

EXISTING SYSTEM MEMORY	SET SWITCHES
128K	
256	
384	

Moving Jumper TM3

To move jumper TM3, perform the following procedure.

1. Locate jumper TM3 on the APC-H31 PCB Rev. 1 (see Figure 6).

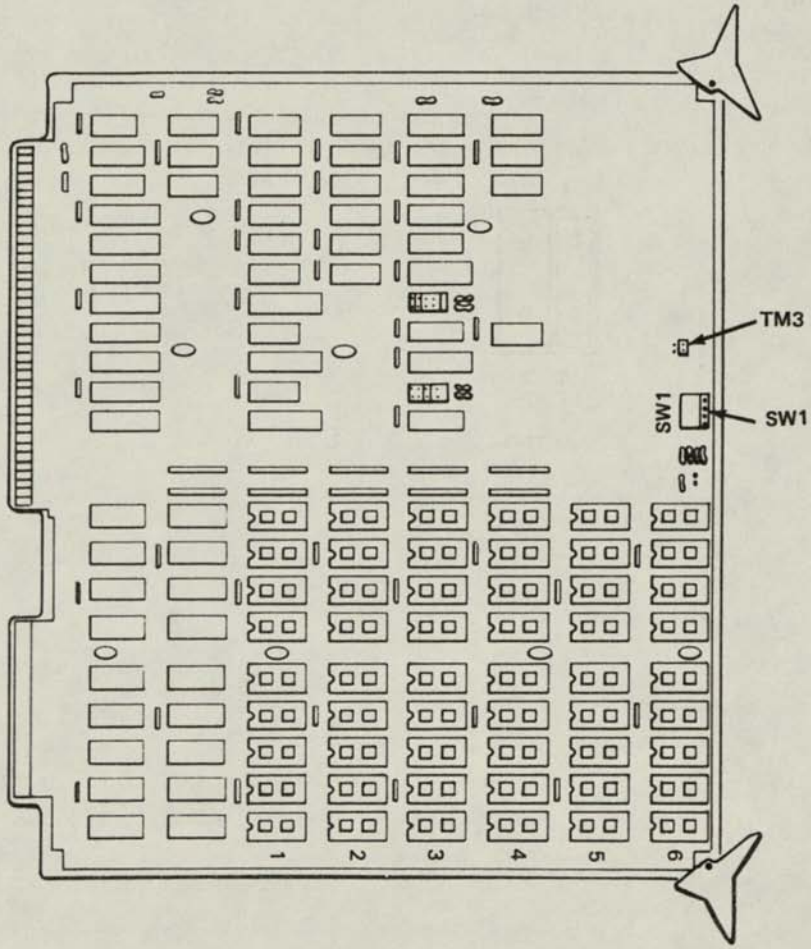


Figure 6 TM3 Jumper Location on the APC-H31 PCB Revision 1

2. Move the plastic cap (jumper) from pins numbered 2-3 to pins 1-4 (see Figure 7).

CAUTION

A system failure may occur if jumper TM3 is not set from pin 1 to pin 4.

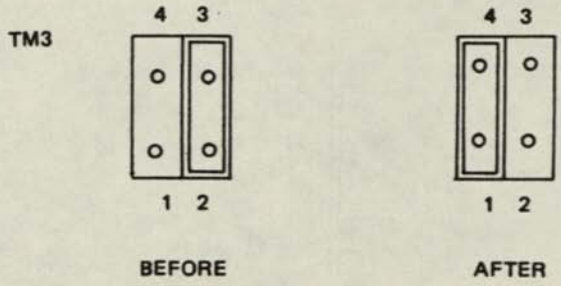


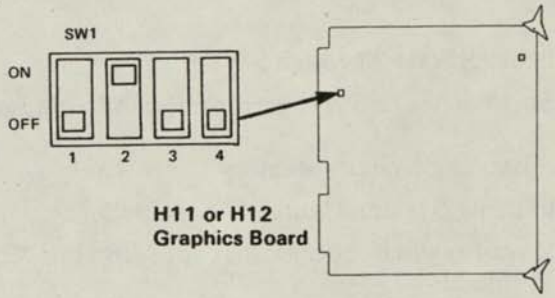
Figure 7 TM3 Jumper Position

Setting Additional Switches

NOTE

If your APC contains either a monochrome (APC-H11) or color (APC-H12) Graphics Subsystem Board with memory, you must verify the settings of slider switch SW1 on the H11/H12 PCB (see Figure 8).

SWITCH SETTINGS FOR THE APC-H11 OR APC-H12 WHEN THE APC CONTAINS AN H-08 EXPANSION MEMORY BOARD (G9PTV).



SWITCH SETTINGS FOR THE APC-H11 OR H-12 WHEN THE APC DOES NOT CONTAIN AN H-08 EXPANSION MEMORY BOARD (G9PTV).

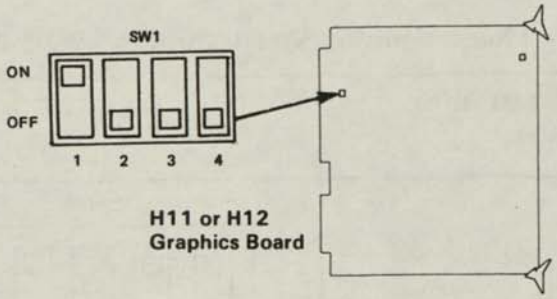


Figure 8 Switch Positions for the APC-H11/H12

Revision 1 Switch Setting Checklist

Did you set SW1?

Move TM3?

Check your Graphics Subsystem Switch Settings?

When you have answered yes to the above three questions, you can install your APC-H31 Memory Expansion Unit (see INSTALLING THE APC-H31 MEMORY EXPANSION UNIT PCB).

REVISION 2 SWITCH SETTINGS

NOTE

This section applies to Revision 2 only. Refer to "Revision 1 Switch Settings," if you have Revision 1.

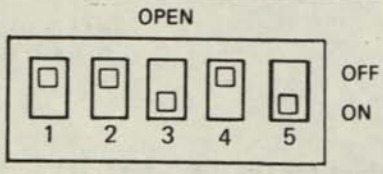
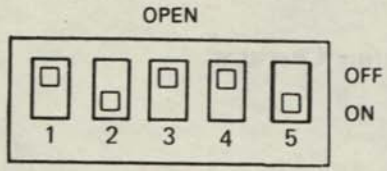
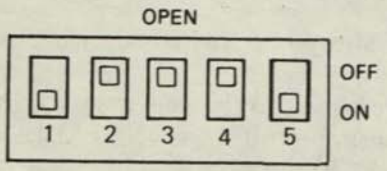
Before installing the APC-H31 Rev. 2 board, you must set the eight slider switches in SW1.

Setting Revision 2 Switches SW1-1 Through SW1-5

To set the first five slider switches in SW1, perform the following procedure.

1. Look up your "Existing System Memory" from Table 1.
2. Match your "Existing System Memory" in Table 5.
3. Set switches, or verify switch settings, that apply to your "Existing System Memory" (see Table 5).

Table 5 Revision 2 Slider Switches SW1-1 Through SW1-5 Positions

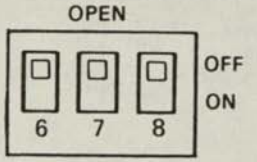
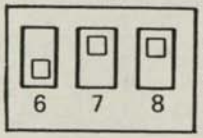
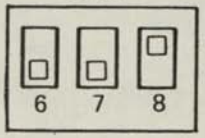
EXISTING SYSTEM MEMORY (From Table 1)	SET SWITCHES
128K	
256K	
384K	

Setting Switches SW1-6 Through SW1-8

Slider switches SW1-6 through SW1-8 are set according to the amount of memory installed on the APC-H31 PCB.

To set these slider switches, refer to Table 6.

Table 6 Revision 2 Slider Switches SW1-6 through SW1-8 Positions

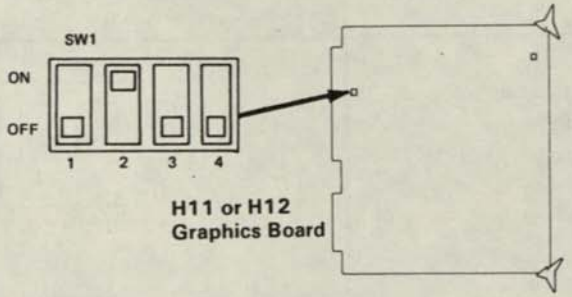
MEMORY ON APC-H31 PCB (Refer to Table 3)	SET SWITCHES
Standard APC-H31 PCB (soldered ICs only) APC-H31 board memory is 128K Lines 1, 2, 3, or 7 from Table 3	 (VERIFY FACTORY SETTING)
APC-H31 with one APC-H32 kit (socket set 1 filled) APC-H31 Board Memory is 256K Line 4 or 6 from Table 3	
APC-H31 with two APC-H32 Kits (socket sets 1 & 2 filled) APC-H31 board memory is 384K Line 5 from Table 3	

Setting Additional Switches

NOTE

If your APC contains either a monochrome (APC-H11) or color (APC-H11) or color (APC-H12) Graphics Subsystem Board with memory, you must verify the settings of slider switch SW1 on the H11/H12 PCB (see Figure 9).

SWITCH SETTINGS FOR THE APC-H11 OR APC-H12 WHEN THE APC CONTAINS AN H-08 EXPANSION MEMORY BOARD (G9PTV).



SWITCH SETTINGS FOR THE APC-H11 OR H-12 WHEN THE APC DOES NOT CONTAIN AN H-08 EXPANSION MEMORY BOARD (G9PTV).

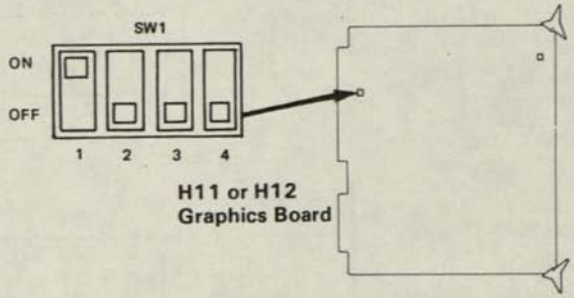


Figure 9 Switch Positions for the APC-H11/H12

Revision 2 Switch Setting Checklist

Did you set switches SW1-1 through SW1-5?

Did you set switches SW1-6 through SW1-8?

Check your Graphics Subsystem Switch Settings?

When you have answered yes to the above three questions, you can install your APC-H31 Memory Expansion Unit (see INSTALLING THE APC-H31 MEMORY EXPANSION UNIT PCB).

INSTALLING THE APC-H31 MEMORY EXPANSION UNIT PCB

Before installing the APC-H31 PCB, make sure that you have followed all the preparation procedures.

To install the APC-H31 PCB, first do the following procedure.

1. Turn off and unplug the APC.
2. Loosen the screws that hold the latch locks in place (see Figure 10). Make sure that the locks hang straight down from the screws.

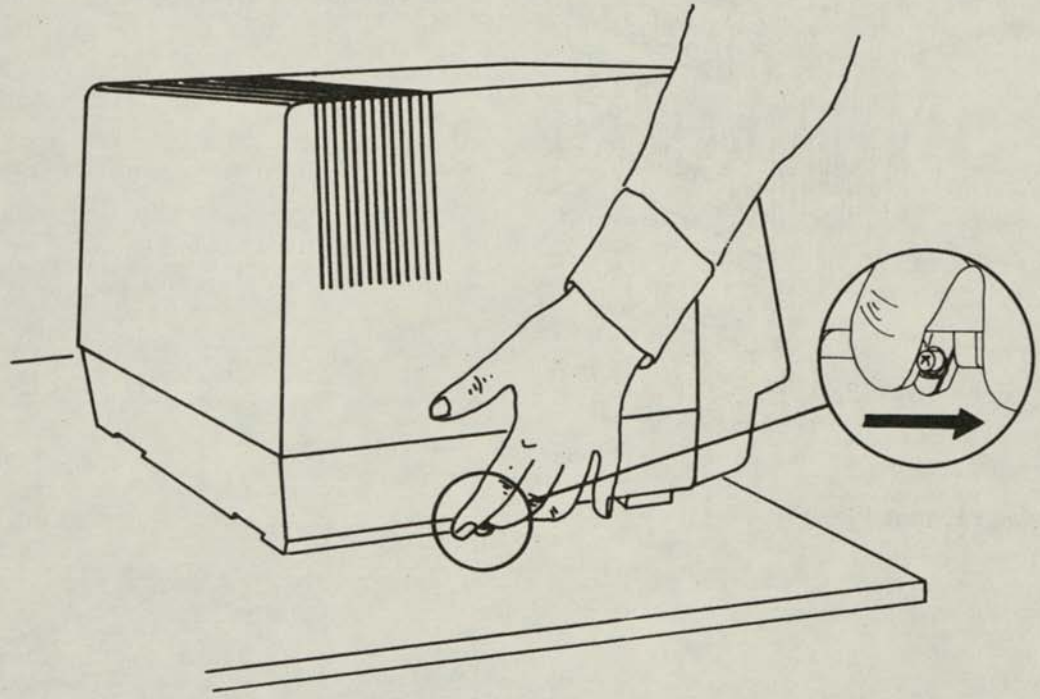


Figure 10 Removing the APC Top Cover

3. Pull the latch levers forward and lift the top cover up and off the computer.
4. Choose an empty slot in the card cage (see Figure 11) for the APC-H31 PCB.

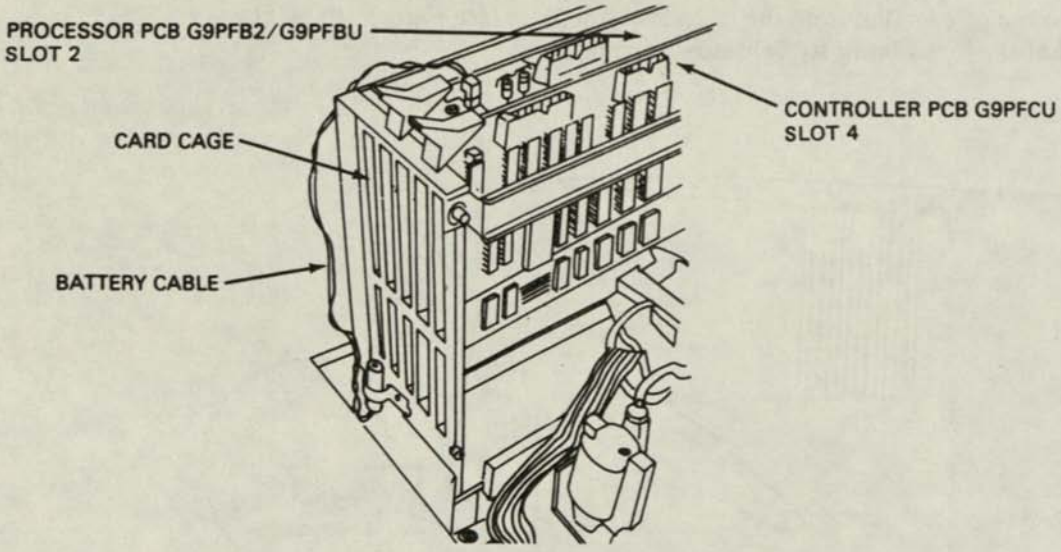


Figure 11 Card Cage (Front View)

CAUTION

The processor PCB (G9PFB2/G9PFBU) has a small battery cable attached to the left side. DO NOT DISCONNECT THE BATTERY CABLE.

5. Disconnect any cables (other than the battery cable) in the way of the available slot.

   To disconnect a cable, press down on the small clips and lift the cables up (see Figure 12).

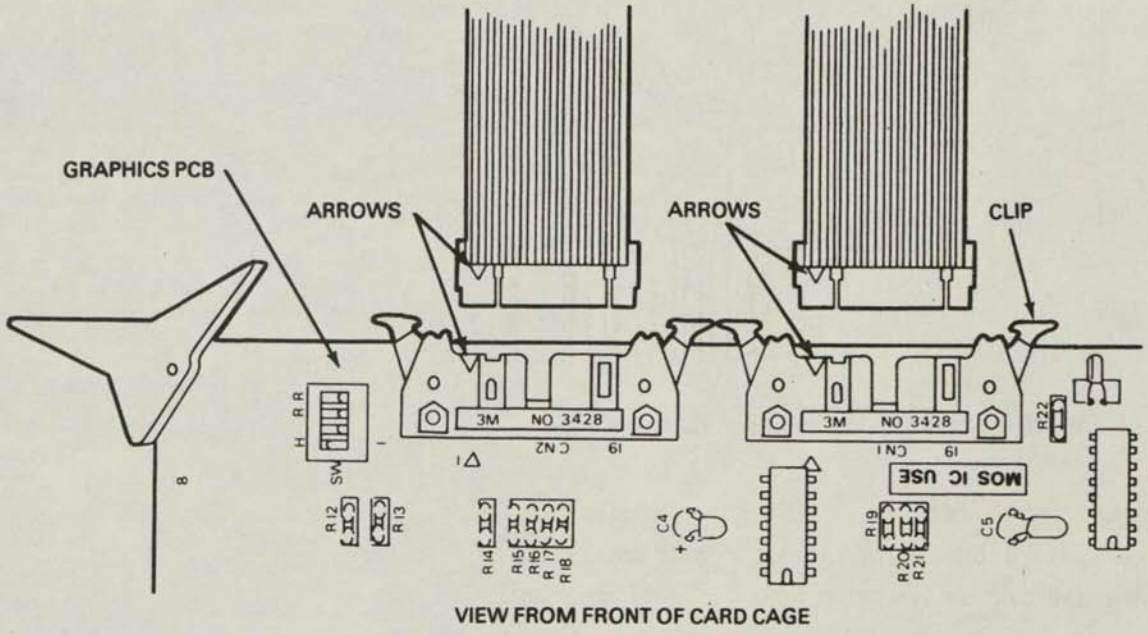


Figure 12 Disconnected Cables

6. Hold the board with the IC side facing the front of the card cage (see Figure 13).
7. Firmly press the PCB into place.

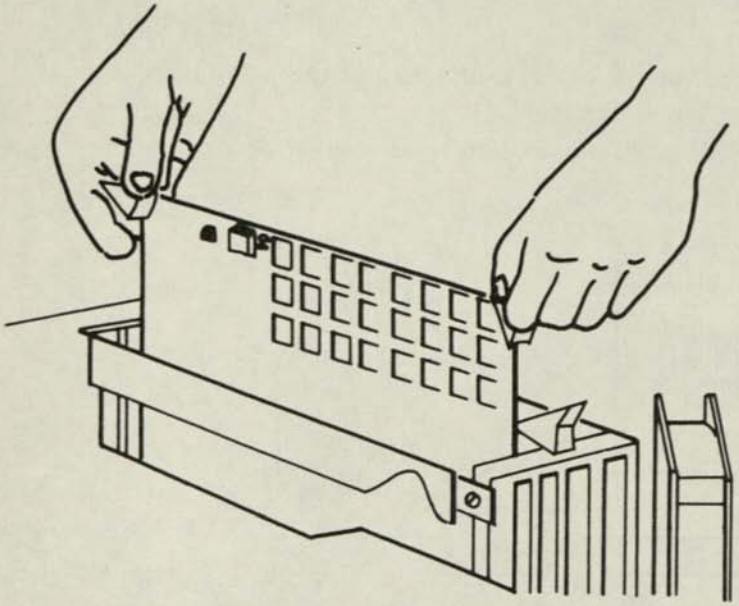


Figure 13 Inserting the APC-H31 PCB in the card cage

8. Reconnect any cables that you disconnected in step 5.
9. Align, lower, and latch the computer cover into place.
10. Lastly, tighten the screws that hold the latches in place.

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USER'S COMMENTS FORM

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Document No.: 819-000104-9001 Rev. 01

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Glossary

A Abbreviation for Ampere.

AD0 to AD15 Address and Data lines 0 to 15; bus interface channels. See Chapter 2 for information.

Address Bus A set of parallel conductors that carry address codes from the microprocessor to memory and I/O devices.

ALE Address Latch Enable.

AND A logic operator having the property that if P is a statement, Q is a statement, R is a statement..., then the AND of P,Q,R...is true if and only if all statements are true, false if any statement is false.

ANSI American National Standards Institute; an organization that develops and publishes industry standards, including terminology and standard codes.

APC Advanced Personal Computer.

ASCII American Standard Code for Information Interchange; this standard defines character set codes that are used for data interchange between equipment of different manufacturers. This code defines 96 displayed characters (64 without lowercase) and 32 non-displayed controls in terms of 7 bits (plus an eighth bit for parity check).

Assembler A computer program that prepares a machine-language program from a symbolic language program.

Asynchronous Without relation to a regular time period.

Asynchronous Communications A method of transmitting data in which the timing of character placement on connecting transmitting lines is not critical. The transmitted characters are preceded by a start bit and followed by one or more stop bits; this designates individual characters and allows the interval between characters to vary.

Attribute, Character In the APC, one of eight supplements that can accompany a character on the display screen.

A16 to A19 Address bits 16 to 19; bus interface channels.

BASIC Beginner's All-purpose Symbolic Instruction Code; a common, high-level, numerical-application-oriented, computer program language that is easily learned.

Baud (1) A unit of signaling speed equal to the number of discrete conditions or signal events per second. For example, one baud equals one-half dot cycle per second in Morse code, one bit per second in a train of binary signals, and one 3-bit value per second in a train of signals each of which can assume one of eight different states. (2) In asynchronous transmission, the baud is a unit of modulation rate that equals the unit intervals.

BBM Battery-Backed Memory.

BHE Bus High Enable; a bus-interface channel. See Chapter 2.

Binary (1) A condition that can have exactly two values; for example, ON and OFF, 1 and 0. (2) A numbering system that includes the digits zero and one and uses two as its base; that is, the base-2 numbering system.

Binary-Coded Decimal (BCD) Positional notation in which the individual decimal digits are represented by a set of four binary numerals; for example, the number twenty-three is represented by 0010 0011 in binary-coded decimal notation, and by 10111 in binary notation.

Bootstrap A technique or device designed to bring itself into a desired state by means of its own action; for example, a machine routine whose first few instructions are sufficient to bring the rest of itself into the computer from an input device.

Buffer A temporary storage area between devices used to compensate for differences in data flow rates or in the occurrence of events; a storage area that temporarily holds input or output data.

Bus A number of parallel conductors (usually 8 or 16, sometimes 20) used for transmitting data signals or power; for example, address bus, data bus.

Byte A sequence of adjacent binary digits (eight digits in most machines including the APC) operated upon as a unit and usually shorter than a computer word (a word is composed of two bytes in the APC).

C/$\overline{D}$ (CONTROL/$\overline{DATA}$) An input signal of the NEC 8251A Communications Controller. See Chapter 3.

Central Processing Unit (CPU) (1) A unit of a computer that includes the circuits controlling the interpretation and execution of instructions. (2) In the APC, the NEC μPD8086 microprocessor.

Chip A tiny piece of semiconductor material on which microscopic electronic components are photoetched to form one or more circuits. After connector leads and a case are added, it is called an integrated circuit.

CLKO Communications Clock; a bus-interface channel. See Chapter 2.

COBOL Common Business Oriented Language; a business data processing language.

Clock (1) The basic source of synchronizing signals in the microcomputer; PHI0 in the APC. (2) In data communications, the clock — CLK0 in the APC — that controls the timing of signal sending and receiving.

CMOS Complementary Metal Oxide Semiconductor

Code (1) A system for representing data according to unambiguous rules; e.g. a binary decimal code. (2) Within a given machine or storage location, a system of binary digits given certain arbitrary meanings, used for transmitting information; for example, in the APC, character code, character-attribute code, command code. (3) To change the symbolic representation of data or commands in order to make them conform to such a system.

Communications Refers to communication between computers or between computers and terminals. Information is transmitted with synchronous or asynchronous timing, and in serial-data or parallel-data form.

Computer A data processor capable of high-speed mathematical or logical calculations, able to assemble, store, and otherwise process information derived from coded data in accordance with a predetermined program.

CP/M Control Program For Microprocessors; a registered trademark of Digital Research, an operating system that comprises four subsystems: basic input-output system (BIOS), basic disk-operating system (BDOS), console command processor (CCP), and transient program area (TPA). Programs that are created, edited, debugged, assembled, and executed on one CP/M-based configuration run on all CP/M-based configurations. CP/M is thus a standard interface between user programs and system hardware. Among the high-level languages that currently run with CP/M are BASIC, COBOL, FORTRAN, Pascal, APL, and PL/1.

CRT Cathode Ray Tube; a vacuum tube in which electrons are accelerated to and focused upon a fluorescent screen.

CRT Display Unit In the APC, the equipment that receives data and transforms it into visible images on the CRT display screen. Specifically, the unit includes a cathode ray tube, display control, display screen, horizontal driver, and vertical driver.

CS Code Segment

$\overline{\text{CS}}$ (Chip Select) An input signal of the Intel 8251A Communications Controller. See Chapter 3.

DACK0 to DACK3 DMA-request Acknowledgement 0 through 3; bus-interface channels. See Chapter 2.

Data (1) A representation of facts, concepts, or instructions in a formalized manner suitable for communication, interpretation, or processing by humans or automatic means. (2) Any representations such as characters or analog quantities to which meaning is or might be assigned.

DIP Dual In-Line Package; a popular IC packaging container that has two parallel rows (hence dual) of leads, which connect the unit to a circuit board. They are available in a variety of configurations, from 14-pin to 40-pin assemblies.

Disk, Flexible A type of magnetic disk, so named because it is soft and bends easily; also called floppy disk.

Disk, Hard Conventional magnetic disk that is stiffer than a flexible disk, contains more concentrated data, and can be read faster.

Disk, Magnetic A flat circular plate with a magnetic surface on which data can be stored by selective magnetization of portions of the flat surface.

Display Position A unit on the video display screen capable of containing one character; that is, each display unit holds one character box. The APC video display has 25 lines of 80 display positions; and each display position is composed of an 8 x 19 dot matrix.

DMA Direct Memory Access; high-speed data transfer operation in which an I/O channel transfers information directly to or from the memory. Transfers take place with no microprocessor intervention using a "cycle-stealing" method. Also called "data break."

DMC DMA Cycle; a bus-interface channel. See Chapter 2.

Double Density Refers to a type of magnetic disk storage organization in which 256 characters of information are stored on each sector of a track. Compare with single density.

DRQ0 to DRQ3 DMA Request 0 to 3, bus interface channels. See Chapter 2.

DS Data Segment

DT/R Data Transmit or Receive; a bus-interface channel. See Chapter 2.

EIA Electronics Industries Association; an electronics trade association that formulates and establishes industry standards.

EPROM Erasable Programmable Read-Only Memory. Like a PROM, it is a programmable read-only memory, but unlike an ordinary PROM its contents can be erased and rewritten more than once. Like any ROM device, an EPROM retains its contents indefinitely.

FDC Flexible Disk Controller.

FDD Flexible Disk Drive.

FIFO First-In First-Out.

Firmware Refers to microprocessors and other software that have been permanently written into ROM chips; for example, the bootstrap loader is a firmware program.

Fixed-Point Arithmetic Computer calculations in which the computer does not consider the radix point. Compare floating-point arithmetic.

Flag An indicator used to specify the status of a designated condition. A flag is usually one or two bits and can be hardware- or software-implemented.

Floating-Point Arithmetic Arithmetic procedures in which the computer keeps track of the radix point. Compare fixed-point arithmetic.

FM Frequency Modulation.

Full Duplex In communications, pertains to simultaneous two-way independent transmission in both directions; also called duplex. Compare with half duplex.

GDC Graphic Display Controller.

Half Duplex In communications, pertains to an alternate, one-way-at-a-time independent transmission. Compare with full duplex.

Hexadecimal (HEX) Refers to the number system with 16 as its base. The hexadecimal system uses 16 symbols: 0 to 9, and A to F for the base-10 numbers 10 to 15. One hexadecimal digit can be represented by four bits.

Hertz (Hz) A unit of frequency equal to one cycle per second.

Highlighting A method used to distinguish or emphasize data on a CRT Display. There are a number of methods: reversing the field, blinking, underlining, changing color, changing light intensity, or some combination of these. The APC features all of these highlighting methods.

High-Order Position In this manual (and in general), the left-most position in a string of digits, characters, or bytes. A high-order position is more significant than a low-order position.

ICW Initialization Command Word.

Impact Printer A printer that forms characters by physically striking the paper through a ribbon; for example, conventional typewriters print this way.

Input/Output (I/O) Pertaining to a hardware device that can transmit data into or receive data from a computer.

Integrated Circuit (IC) A microunit consisting of interconnected elements, inseparably associated and formed on or within a single substrate to function as an electronic circuit.

Intel A large semiconductor designer, manufacturer, and distributor.

Interlace To assign successive storage location numbers to physically separate storage locations; this reduces access time.

Interrupt (1) A suspension of the normal flow of a process in such a way that the flow can be resumed. (2) A special control signal from an I/O device that diverts the attention of the CPU from the program to a specific address.

IOR I/O Read; a bus-interface channel. See Chapter 2.

IOW I/O Write; a bus-interface channel. See Chapter 2.

IP Instruction Pointer.

IR0 to IR14 Interrupt Request 0 to 14; bus-interface channels. See Chapter 2.

IRR Read Interrupt Register.

IRST Initial Reset; a bus-interface channel. See Chapter 2.

ISR Read Inservice Register.

K Abbreviation for kilo. (1) Prefix meaning 1000. (2) With regard to memory space and addressing, kilo means 1024 (2 to the 10th power); for example 2K equals 2048.

KB Abbreviation for kilobyte; 1024 bytes.

kHz Abbreviation for kilohertz; a unit of frequency equal to 1000 hertz.

LAD Light Pen Address.

Low-Order Position The left-most position in a string of digits, characters, or bytes. A low-order position is less significant than a high-order position.

LSB Least Significant Bit.

LSI Large Scale Integration; (1) Refers to a component density of 100 or more per chip. (2) A chip with more than 100 components.

M Abbreviation for mega. (1) Prefix meaning 1,000,000. (2) With regard to memory space and addressing, mega means 1,048,576 (2 to the 20th power); for example, one MB equals one megabyte, 1,048,576 bytes.

Machine Language Binary-coded language; the only type of language that can be directly used by the machine.

Main Unit In the APC, the Main Unit houses all the microcomputer devices except the Keyboard and Printer. In addition, all interfaces are in or on this unit.

Matrix Printer A printer that forms characters by printing a pattern of dots.

MB Megabyte; 1,048,576 bytes. The addressing power of the APC.

Memory Address (1) The unique location of a word in memory. (2) In the APC, a 20-bit value that identifies a specific portion of memory.

Memory Map A symbolic representation of memory locations that defines the boundaries of various memory segments.

MFM Modified Frequency Modulation; a magnetic-disk coding system that uses double-density encoding of information.

MHz Megahertz; a unit of frequency equal to one million hertz.

Microprocessor (1) The principal component of a microcomputer, it is a semiconductor central processing unit. Usually contained on a single chip, which is mounted on a DIP, it includes an arithmetic logic unit, control logic, and control-memory unit. (2) In the APC, the microprocessor is the NEC μPD8086, which is mounted on a 40-pin DIP.

Mnemonic An abbreviation of two or three letters (abbreviated in a way to aid human memory) that is used instead of terminology.

Mode Refers to various methods of operation; for example, the synchronous versus the asynchronous mode.

Modem MOdulator-DEModulator; a device that modulates signals transmitted over communication facilities. This device enables computers and terminals to communicate over telephone circuits.

Monitor (1) A device that observes and verifies the operation of a data processing system and indicates any significant departure from the norm. (2) Software or hardware that observes, supervises, controls, or verifies the operation of a system. (3) A video display.

MOS Metal Oxide Semiconductor.

Mother Board A circuit board into which various printed circuit boards (PCB) are plugged. In the APC, the Mother Board is inside the card cage and has five PCB slots.

MR Memory Read; a bus-interface channel. See Chapter 2.

MRQ Memory ReQuest, a bus-interface channel. See Chapter 2.

ms millisecond; one-thousandth of one second, 0.001 second.

MSB Most Significant Bit.

Multiplexer A device capable of combining several low-speed inputs into one high-speed data stream transmitted on a single channel. A demultiplexer subsequently reconverts the single data stream into low-speed inputs for the host computer. Two kinds of multiplexers are time-division multiplexers in which the channel is divided into time slots and frequency-division multiplexers in which the channel is divided into frequency bands.

MW Memory Write; a bus-interface channel. See Chapter 2.

NAND A logical operator that is the negation of AND.

NEC Nippon Electric Company; a large manufacturer of electronics equipment, including semiconductors and microcomputers.

NOR A logical operator that is the negation of OR.

ns nanosecond; one billionth of a second, 0.000000001 second.

NT Normal Termination.

OCW Operational Command Word.

ODA Output Device Adapter.

OR A logic operator having the property that if P is a statement, Q is a statement, R is a statement..., then the OR of P,Q,R...is true if at least one statement is true, false only if all statements are false. Often represented by +, as in P + Q.

Output Pertaining to a device, process, or channel involved in an output process, or to the data or states involved in an output process.

Overflow That portion of the result of an operation that exceeds the capacity of the intended unit of storage.

Parallel Data Method for representing data in which characters are transmitted and received over separate lines, usually simultaneously. Compare serial data.

Parameter In general, a quantity used to specify I/O devices or to designate desired routines.

PCB Printed Circuit Board.

Personal Computer A relatively low-cost computer that is based on tiny microcomputer chips and is therefore portable and personally controllable. Personal computers are often classified as home, hobbyist, professional, business, small business, appliance, and others.

PHIO System Clock; a bus-interface channel. See Chapter 2.

POF Power-Off Control; (1) A bus-interface channel. See Chapter 2. (2) In the APC, a control circuit that shuts off the system power supply by a microprocessor command.

Printed Circuit Board Also called pc board, plate, card, chassis, and — in this manual — PCB; an insulating board with metallic wiring paths for point-to-point connections, but it can also include metallized connecting surfaces and heat sinks or heat radiators. Printed circuit boards are single-sided, double-sided, or multilayer; all pc boards in the APC are multilayer.

Program A series of instructions or statements, in a form acceptable to a computer, prepared in order to achieve a certain result.

Programmable Array Logic (PAL) TTL Schottky bipolar devices designed to replace standard TTL logic. They are fully programmable to provide a high degree of design flexibility and efficiency. The basic logic implementation is the AND-OR array, where the AND is programmable and the OR fixed. PALs are used to make logic modification quicker and easier than with standard devices.

PROM Programmable Read Only Memory; unprogrammed upon manufacture, can be programmed once and only once. After programming, like ROMs, they retain their contents indefinitely.

Protocol In data communications, a specific set of rules defining the format and content of messages between communicating devices.

P39 Phosphor Used in both the monochrome and color displays of the APC, it is a yellow-green, long-persistence phosphor that provides good luminescence, small dot size, and good focus.

RAM Random Access Memory. See Read/Write Memory.

Raster Scan A technique of graphics CRT displays; it operates by varying the intensity of a beam that periodically scans left-to-right and top-to-bottom. This CRT graphics method is the type used in the APC and conventional home TV; it is the only method that makes full color display possible.

$\overline{RD}$ $\overline{READ}$; an input signal of the NEC 8251A Communications Controller. See Chapter 3.

RDY Ready; a bus-interface channel. See Chapter 2.

Read/Write Memory Also called random access memory or RAM. A type of memory in which each cell can be both sensed at appropriate output terminals and changed in response to electrical input signals.

Refreshing A process of periodically reactivating or restoring information that decays when left idle; for example, the phosphor on a CRT must be refreshed in order to maintain the image, and dynamic memory cells need constant refreshing to maintain their contents.

RFSH Refresh; a bus-interface channel. See Chapter 2.

Register A device capable of storing a specified amount of data such as one word.

rpm Revolutions Per Minute.

ROM Read-Only Memory; memory that can be read but not altered.

RS-232C Interface An interface between a modem and the associated data terminal equipment that is standardized by EIA Standard 232C.

RST RESET; an input signal of the NEC 8251A Communications Controller. See Chapter 3.

Serial Data Method for representing data in which the data stream is transmitted and received as a single signal by a single transmission path. Compare parallel data.

Single Density Refers to a magnetic disk storage technique in which 128 characters of information are stored on each sector of a track. Compare double density.

Software A set of programs, procedures, and possibly associated documentation concerned with the operation of a data processing system.

Sound Generator In general, a computer device that includes a tone-generator and speaker for outputting tones. In the APC, the sound generator is fully programmable and capable of generating user-programmed melodies and various beep signals.

Special Character In the APC, a character that the user can create through the ACGGEN utility program; the programmed character is stored in display RAM (and on disk if desired) and is accesible on command. There is storage allocation for 256 special characters, though an indefinite number can be stored on disk.

SS Stack Segment.

Status Register A register that provides storage for arithmetic and control status flags.

SW Switch.

Synchronous Having a constant time interval between successive bits, characters, or events.

Synchronous Communications A method of transmitting information in which the timing of character placement signifies the division between characters. A data stream of an indefinite number of characters is preceded by one or two sync bits, which indicate where the data stream begins.

TC Terminal Count; a bus-interface channel. See Chapter 2.

TTL Transistor/Transistor Logic.

USART Universal Synchronous/Asynchronous Receiver/Transmitter

V Abbreviation for Volt.

VFO Variable Frequency Oscillator.

W Abbreviation for Watt.

Word A group of characters that occupy one storage location and are treated as a single entity, instruction, or quantity. In the APC, two bytes (16 bits) make up a word.

$\overline{\text{WR}}$ ($\overline{\text{WRITE}}$) An input signal of the NEC 8251A Communications Controller. See Chapter 3.

Advanced Personal Computer

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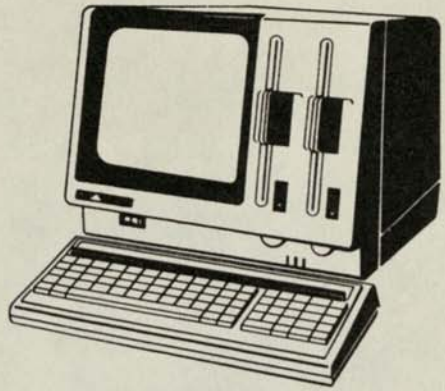

APC Hard Disk Subsystem Reference Guide

NEC
NEC Information Systems, Inc.
819-000102-6002 Rev. 00
4-83

APC-HARD DISK SUBSYSTEM REFERENCE GUIDE
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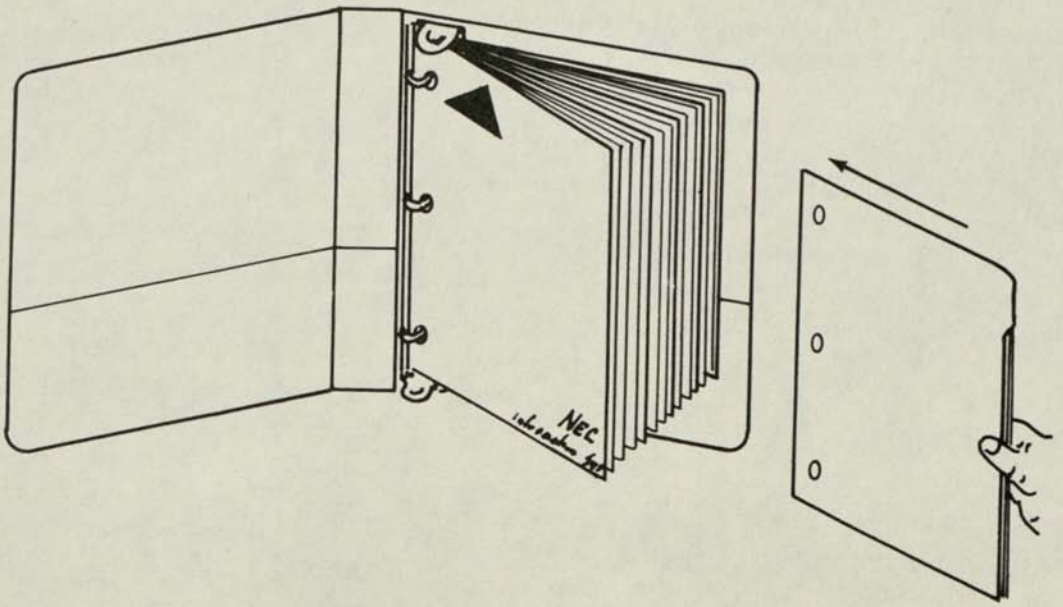

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FEDERAL COMMUNICATIONS COMMISSION RADIO FREQUENCY INTERFERENCE STATEMENT

"WARNING: This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A Computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide protection against such interference. Operation of the equipment in a residential area is likely to cause interference in which case, the user will be required to take whatever measures may be required to correct the interference."

Manufacturer's Instructions and User's Responsibilities to Prevent Radio Frequency Interference

Manufacturer's Instructions

The user must observe the following precautions in installing and operating this device:

1. Operate the equipment in strict accordance with the manufacturer's instructions for the model.
2. Ensure that the unit is plugged into a properly grounded wall outlet and that the power cord supplied with the unit is used and not modified.
3. Ensure that the unit is always operated with the factory-installed cover set on the unit.
4. Make no modification to the equipment which would affect its meeting the specified limits of the Rules.
5. Properly maintain the equipment in a satisfactory state of repair.

User's Responsibility

The user has the ultimate responsibility to correct problems arising from harmful radio-frequency emissions from equipment under his control. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures. All of these responsibilities and any others not mentioned are exclusively at the expense of the user.

1. Change in orientation of the receiving device antenna.
2. Change in orientation of the equipment.
3. Change in location of equipment.
4. Change in equipment power source.

If these attempts are unsuccessful, install one or all of the following devices:

1. Line isolation transformers
2. Line filters
3. Electro-magnetic shielding

If necessary, the user should consult the dealer, NEC, or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission to be helpful: "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

"Note: The operator of a computing device may be required to stop operating his device upon finding that the device is causing harmful interference and it is in the public interest to stop operation until the interference problem has been corrected."

Contents

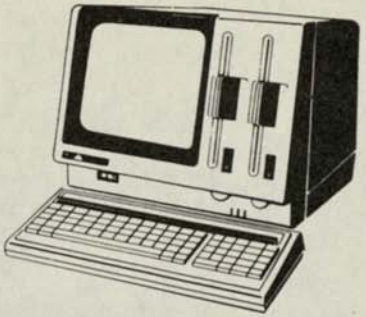
Contents (cont'd)

List of Illustrations

List of Tables

Preface

This manual is written for those who desire an understanding of the Disk Unit (DKU) operations; not only as an external storage device in an APC system configuration, but also its operations within an APC control unit. This information includes the functional capabilities of the DKU, as well as, the status information sent to the APC control unit for interrogation and processing of data and I/O commands. The manual also describes the principal features of the DKU, the applicable environmental considerations, the physical and functional capabilities of the major Printed Circuit Boards (PCB), and the disk drive assembly itself. Maintenance and installation information are mentioned on an as needed basis, only. This type of information is provided in the APC Maintenance Guide and the Hard Disk Subsystem Installation Guide.



Chapter 1

General Description

The APC disk subsystem is used as an external storage device in an APC system (see Figure 1-1). It comes as a stand-alone Disk Unit (DKU), model APC-H26, and an expansion DKU, model APC-H27. The stand-alone DKU is also referred to as the master and the expansion unit as the slave. Each model provides a disk storage capacity of approximately 10 Megabytes (MB) of formatted data. When installed together they provide an overall storage capacity of approximately 20 MBs. Included in each model is a sealed multidisk module designed to improve the operational reliability by minimizing contaminents on the recording surface (see Figure 1-2). Operational reliability is further improved with the use of magnetic heads with NEC Large Scale Integration (LSI) circuits designed to enhance the weakest signals.

The model APC—H26 contains the interface and control logic for the stand-alone and the expansion DKUs on a single Printed Circuit Board (PCB), called the 3302 Format (FMT) control PCB. Both the stand-alone and expansion DKUs contain their respective disk drive electronics.

The APC control unit houses a disk controller, called, the Disk Adapter PCB. This adapter connnects directly with the 3302 FMT PCB in the stand-alone DKU (see Figure 1-3), and contains the interface logic to support the appropriate APC system configuration.

1.1 PRINCIPAL FEATURES

The APC Disk Units (DKU) are compact, fast-access data storage devices designed for use with an APC system. Data is stored on 5.25 inch metal-oxide-coated disks that are mounted on a common rotating spindle and, along with the Read/Write (R/W) heads, are housed in an air-tight, sealed module. This arrangement assures maintenance-free operation, negating maintenance checks. The metal oxide coated disks are also known as platters.

Both models contain four 2-sided disks; each disk surface is equipped with a pair of Winchester type magnetic R/W heads. The R/W heads are supplied as standard equipment and are structured on a swing out mechanism driven by a stepping motor assembly. All heads incorporate a preamplifier to improve read data signal-to-noise ratio.

Depending on the disk configuration, that is, a stand-alone only or a stand-alone and an expansion disk unit, the disk system is capable of storing approximately 10 or 20 MBs of formatted data at a maximum recording density of 7480 bits per inch. The recording method used is the Modified Frequency Modulation (MFM) technique, and the data transfer rate is 500 KBytes per second.

1.2 MODELS

The model disk units currently available for the APC are listed below and are briefly described in the preceding text. A more detailed description is provided in subsequent chapters.

Model APC-H26 Stand-alone DKU (Master Unit).

Model APC-H27 Expansion DKU (Slave Unit).

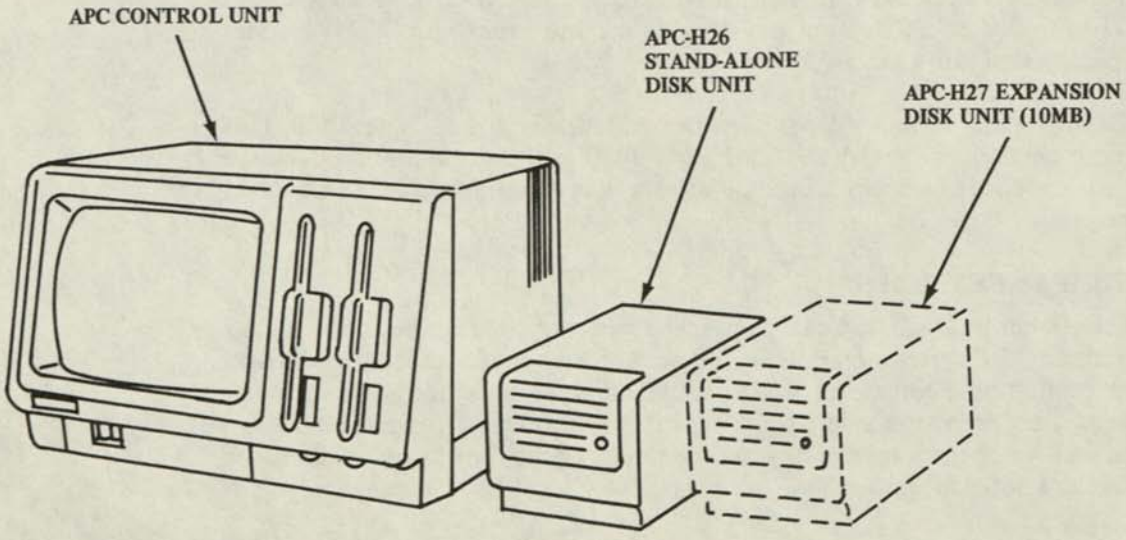


Figure 1-1 Typical APC System Configuration

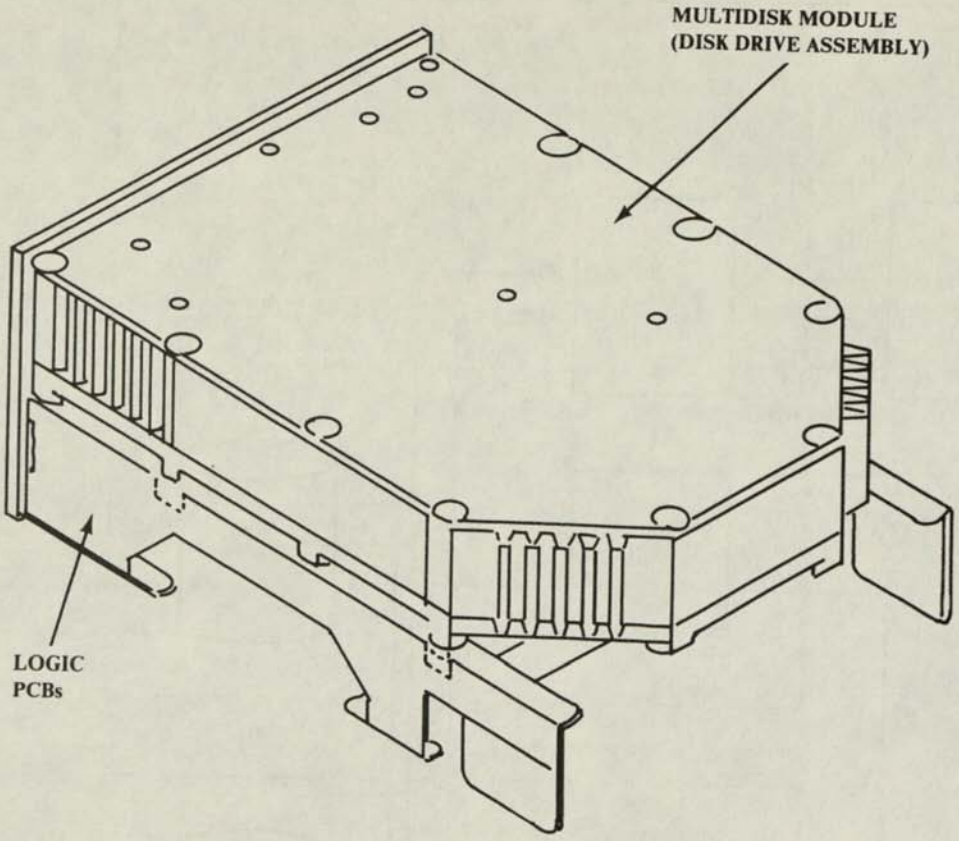


Figure 1-2 Multidisk Module (Disk Drive Assembly)

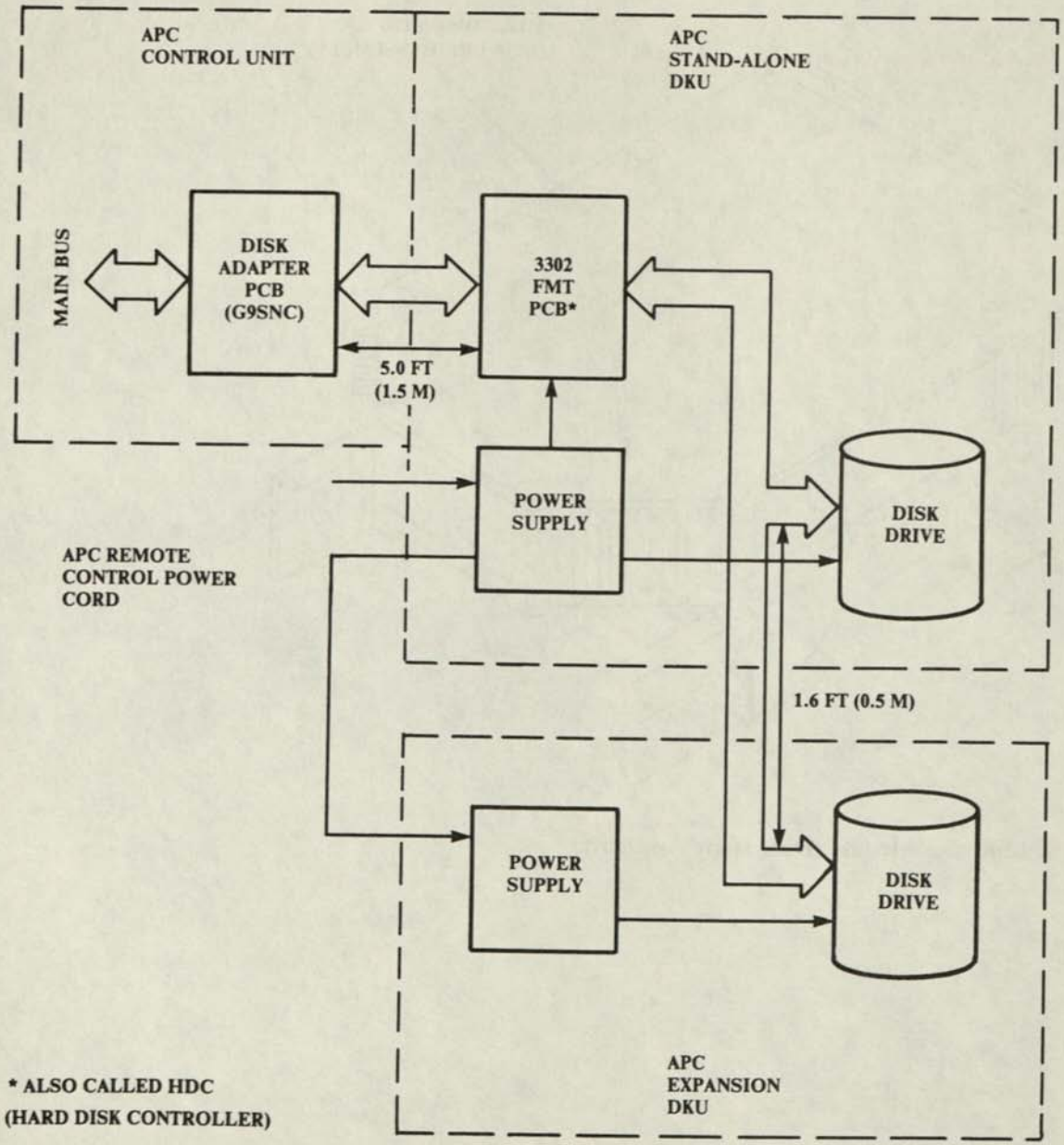


Figure 1-3 APC Stand-Alone/Expansion DKU Functional Block Diagram

1.3 DISK UNIT/MODULE ORGANIZATION

Figure 1-4 shows the physical layout of the major disk drive components contained in the sealed module within the APC Disk Unit (DKU). They are briefly described below. The associated DKU cabinetry and related components are described in subsequent chapters.

1.3.1 Sealed Module

The sealed module contains a sealing type metal cover, spindle, four 5.25 inch platters, eight Winchester type R/W heads, interface and control logic PCB, and other related components shown in the illustration and described in subsequent sections.

The metal cover seals the module against contaminents from the surrounding environment, and maintains constant filtered air flow through the module. Because the interior is sealed from the environment and kept clean by a circulatory air flow, the APC DKU is assured of stable operation under ordinary office conditions.

CAUTION

The cover is normally installed at the factory and should never be removed in the field. When the DKU is defective, return it to the local branch office for service.

The spindle supports and drives the four platters and is driven by a 115 Vac constant drive motor.

The 5.25 inch platters are two-sided magnetic disks that permit the use of Winchester type read and write heads over each surface, resulting in the high storage capabilities in each DKU. That is, each 5.25 inch disk surface has a track density of 220 tracks per inch, resulting in a maximum recording density of 7480 bits per inch. The number of sectors per track is 26 assuming formatted data. When storage is unformatted, the storage capacity and number of sectors are variable up to a maximum storage capacity of approximately 12 MBs. Additional information is provided in subsequent sections.

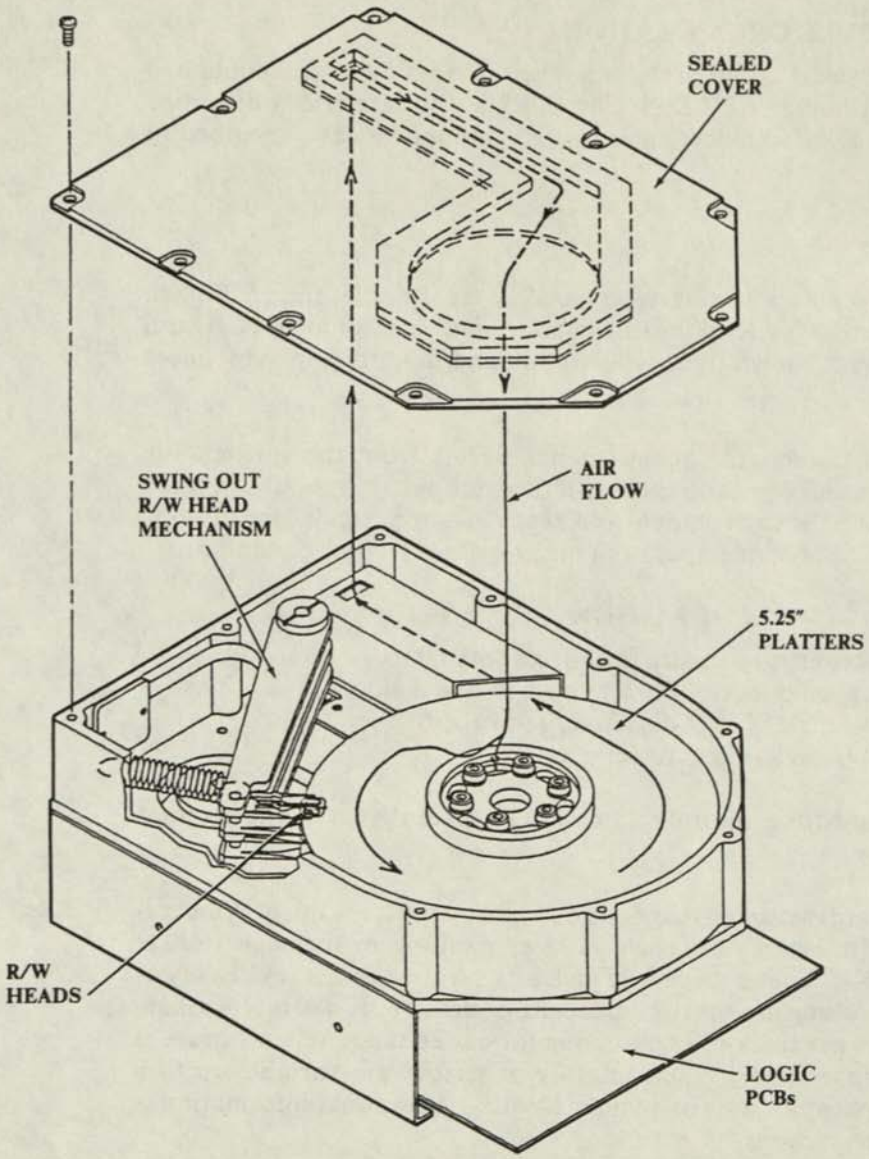


Figure 1-4 APC Disk Module (Major Components)

Winchester type R/W heads are supported by a swing-arm mechanism which is driven by a 5-phase stepping motor. This arrangement reduces the seek time to less than 2 ms.

1.3.2 Printed Circuit Boards (PCBs)

The following printed circuit boards are used in the respective APC control unit or DKU as indicated. Functional and cabling information for each PCB is provided in subsequent chapters.

1. APC Control Unit — G9SNC Disk Adapter (136-432222-B).
2. Stand-alone DKU — 3302 FMT PCB (808-863492-201-A).
   — G9NXT Disk Drive Package (134-835090).
   — G9QKR VFO PCB (134-835122-0).
   — Power Supply (808-863492-201-A).
3. Expansion DKU — G9NXT Disk Drive Package (134-835090).
   — G9QKR VFO PCB (134-835122-0).
   — Power Supply (808-863492-201-A).

1.4 POWER SUPPLY

The 115 Vac, 50/60 Hz input power to the power supply simultaneously starts the power supply and fan. The power supply converts the ac input into regulated dc outputs of +5 and +24 Vdc and distributes the dc voltage throughout the DKU.

Ac input power to the DKU(s) is interlocked with the ac input power in the APC control unit. This makes the APC on/off switch the common power on/off element to all the DKU attachments, as well as, the APC control unit. Hence, the DKU attachments are turned on when the APC control unit is turned on, and are turned off when the APC control unit is turned off.

1.5 ENVIRONMENTAL/FUNCTIONAL CHARACTERISTICS

This section provides the environmental and functional characteristics for the Hard Disk Unit (DKU). This includes the environmental considerations, dimensions, weight, cabling, and an overview of the DKU functional characteristics.

1.5.1 Environmental Considerations

The environmental considerations are as follows:

1. Humidity (Noncondensing)	10% to 80%
2. Operating Temperature	50° to 90° F
3. Vibration (Operating)	Less than 0.5 G

1.5.2 Dimension/Weight

The dimensions and weight for the APC DKU are as follows.

1.	Depth	15.20 inches (380 mm)
2.	Height	7.00 inches (175 mm)
3.	Width	10.00 inches (250 mm)
4.	Weight	25.30 lbs (11.5 Kg)

1.5.3 Interface/Interlock Cabling

Two interface cables and an ac interlock cable, described below, are required to connect the stand-alone DKU to the APC control unit and, when used, the expansion unit to the stand-alone unit. Further cabling information is provided in the APC-H26/-H27 Hard Disk Subsystem Installation Guide.

1. Interface Cables
   a. Model APC-H26 Stand-alone DKU—The interface cable comes attached to the stand-alone DKU, is approximately 4.96 feet in length, and connects to the APC control unit.
   b. Model APC-H27 expansion DKU—The interface cable comes attached to the expansion DKU, is approximately 1.65 feet in length, and connects to the stand-alone DKU.
2. Ac Interlock Cable
   a. Length—between the APC control unit and stand-alone DKU. 4.96 feet
      —between the stand-alone DKU and the expansion DKU 1.65 feet
   b. Part Numbers

Ac interlock cables	
APC-H26	808-863492-207-A
APC-H27	808-863492-208-A
Ac power supply cables	
APC-H26	808-863492-209-A
APC-H27	808-863492-210-A

1.5.4 DKU Functional Characteristics

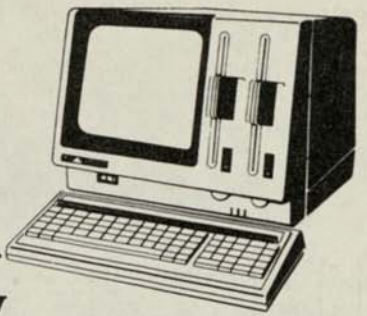
The DKU functional characteristics, summarized in Table 1-1, are estimated at 256 bytes/sector times 26 sectors/track.

Table 1-1 Functional Characteristics

FUNCTION	SPECIFICATION
1. Access Time	
a. Average seek time	120 msec
b. Maximum seek time	360 msec
c. Minimum seek time	2 msec
d. Settling time	15 msec
2. Data Transfer Rate	500 Kbytes
3. Disk (Platter) Configuration	
a. Cylinders	181 Total 174 Data CYL 6 Spare CYL 1 DIAG. CYL
b. Heads (Read/Write)	8
c. Platters	4 (2 sides each)
4. Power—115 Vac input, 50/60 Hz	±10%, 1.0A
a. +5 Vdc (output)	±5%, 1.8A (with VFO)
b. +24 Vdc (output)	±10%, 1.2A (average 2.2A (starting)
5. Recording Density	
a. Bit density	7480 BPI
b. Track density	220 TPI
6. Recording Format	MFM
7. Reliability	
a. MTBF	10,000 Power on Hours
b. Error Rate	
• Non-Recoverable	1 per 10^{12}
• Recoverable	1 per 10^{10}
• Seek errors	1 per 10^{6}
8. Rotational Speed	3600 RPM
9. Start/Stop Time	Less than 10 sec
10. Storage Capacity	
a. Formatted	9.27 MB
• Bytes/Cylinder	53,248
• Bytes/Track	6,656
b. Unformatted	12.0 MB

1.6 TYPICAL DISK DRIVE READ/WRITE OPERATION

To write data on a disk (platter) the FMT controller, described in Chapter 2, converts 8-bit parallel data characters from the APC control unit (see Figure 1-3) into bit-by-bit serial data characters. The disk drive electronics (see Chapter 3) accepts the serial data from the FMT controller and gates it to the disk drive assembly where it is written, bit-by-bit, into the designated sector (or sectors) on the selected platter. A read operation fetches bit-by-bit serial data from the designated sector (or sectors) on the selected platter, and sends this serial data to the FMT controller where it is converted back to 8 bit parallel data characters for transmission to the APC control unit.



Chapter 2

PCB Structure/Functionality

This chapter provides the structural characteristics for the two major DKU PCBs used in an APC system configuration (see Figures 1-1 and 1-3), and includes a brief description of their functional capabilities. The two major PCBs are as follows.

- G9SNC Disk Adapter (Disk Controller) PCB
- 3302 Format (FMT) Control PCB

2.1 DISK ADAPTER PCB

The disk adapter provides the interface and control logic between the APC control unit and the associated DKU attachments (see Figure 1-3). It contains the FMT interface logic and connector, resides in the APC control unit, and consists of the following logic components (see Figure 2-1).

- 8237 DMAC
- 8K Byte Static RAM
- RS422 Formatter Interface

The disk adapter fits into any blank slot in the card cage (mother board) within the APC control unit, and provides the following logic circuits.

- DMA Control Logic
- Error Detect Logic
- FMT Interface Logic
- Interrupt Logic
- I/O Decoder
- Main Bus Control
- Memory Buffer

2.1.1 Disk Adapter Operational Modes

Functionally the disk operates in two modes.

a. Internal Bus Mode
b. Main Bus Mode

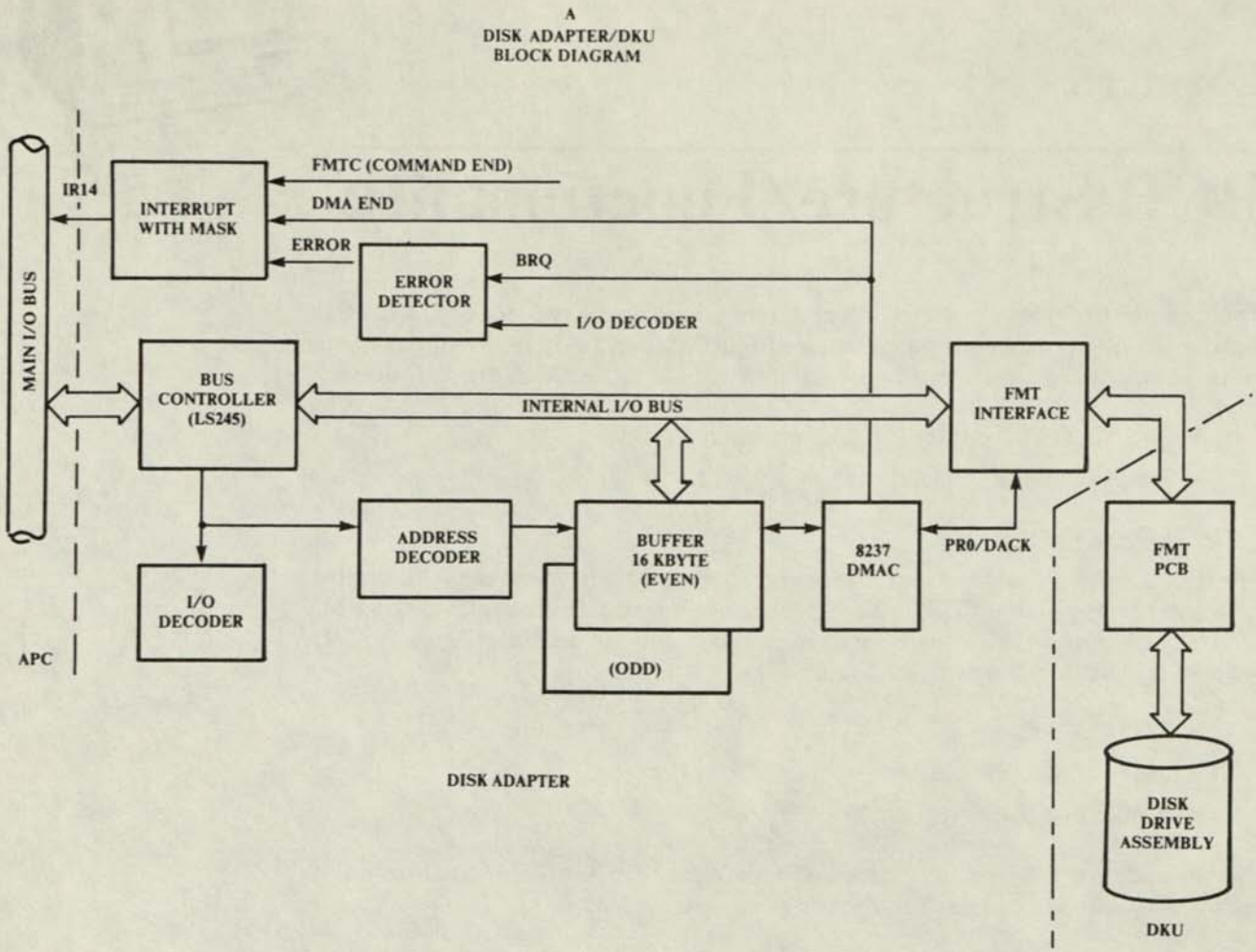


Figure 2-1 Disk Adapter Functional Block Diagram

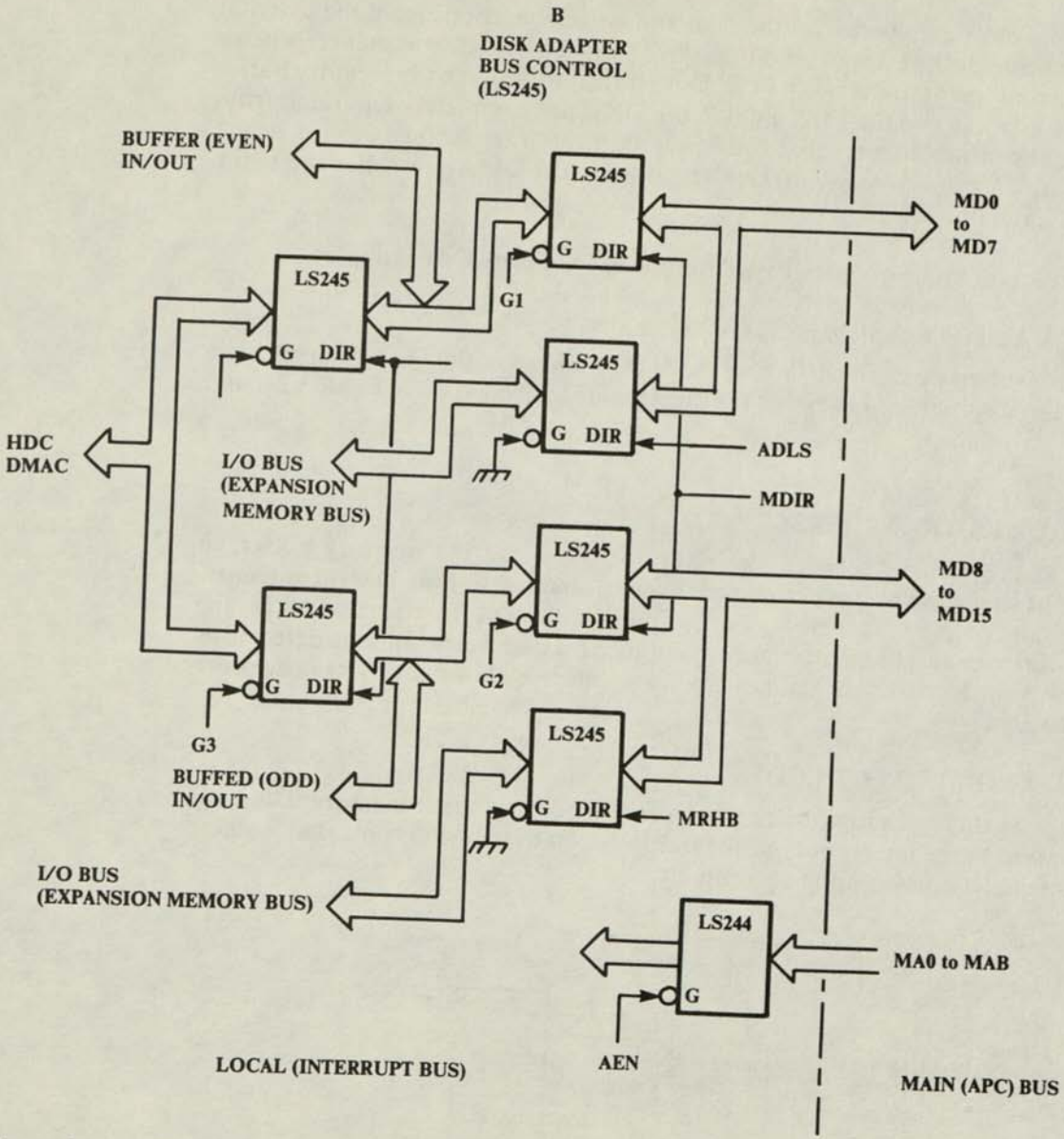


Figure 2-1 (cont'd)

The internal bus mode performs the read and write operations from the external disk drive through the Format (FMT) control PCB. This mode commences when a disk command is sent to the FMT PCB. Data transfers between the memory buffer in the disk adapter and the FMT PCB in the DKU are completely separated from the main bus in the adapter and operate within the internal bus. Access to the memory buffer, transmission of I/O instructions to the DMA controller and to the FMT PCB are inhibited.

The main access mode accesses data from the RAM in the Disk Adapter.

2.1.2 Disk Adapter Functional Capabilities

This section briefly describes the functional capabilities of the Disk Adapter logic circuits, listed earlier, and shown in the functional block diagram in Figures 2-1 and 2-2.

2.1.2.1 DIRECT MEMORY ACCESS CONTROLLER (DMAC DATA TRANSFERS)

DMAC data transfers between the FMT interface and the memory buffer, in demand or single mode, are performed through channel 1 of the DMA controller. In addition, access to the memory buffer and execution of I/O instructions for the DMA controller and FMT interface are inhibited. These operations are detected as errors. All other channels are not used and memory to memory transfers are disallowed.

2.1.2.2 ERROR DETECT LOGIC

The error detect logic monitors the DMAC logic for any possible errors. The error status is sent to the interrupt logic for transmission to the APC control unit where the error status is acted upon accordingly.

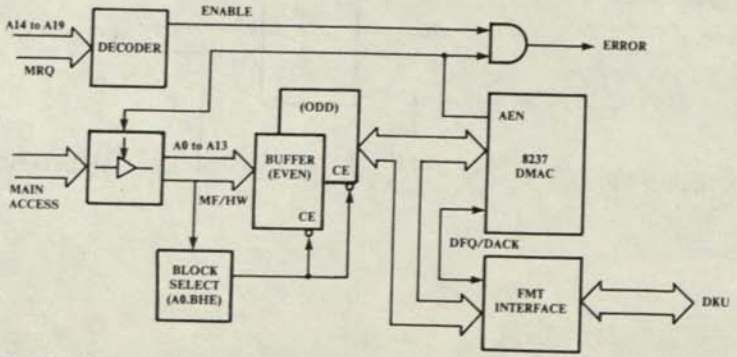


Figure 2-2 Buffer Control Block

2.1.2.3 DISK ADAPTER FMT INTERFACE LOGIC

The FMT Interface logic within the disk adapter provides the communication link between the disk adapter, specifically the DMA controller, and the FMT PCB. It is connected directly to the format control PCB (3302 FMT) in the DKU (Model APC H-26), and controls the data format to the disk drive.

Figures 2-3 and 2-4 show the electrical circuit for the RS422 interface, and Table 2-1 lists the the signal-to-pin assignment for the interface connector. In addition, Figures 2-5 and 2-6 show the timing diagrams for the FMT interface and a DMA access operation.

The FMT PCB is seen as an I/O port to the main processor in the APC control unit. This I/O port has three registers, IR0, IR2, and IR3 that are selected by the FMT control lines, and the appropriate register function is also enabled as shown in Table 2-2.

The IR0 register controls the information for an FMT operation.

The IR2 and IR3 registers correspond to the command/status register and parameter/result registers, respectively. For further details refer to FMT in Section 2.2.

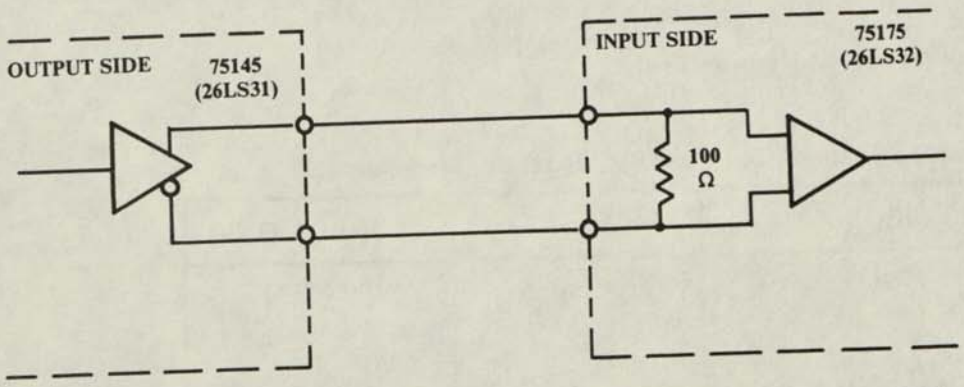


Figure 2-3 Typical Driver/Receiver Circuit

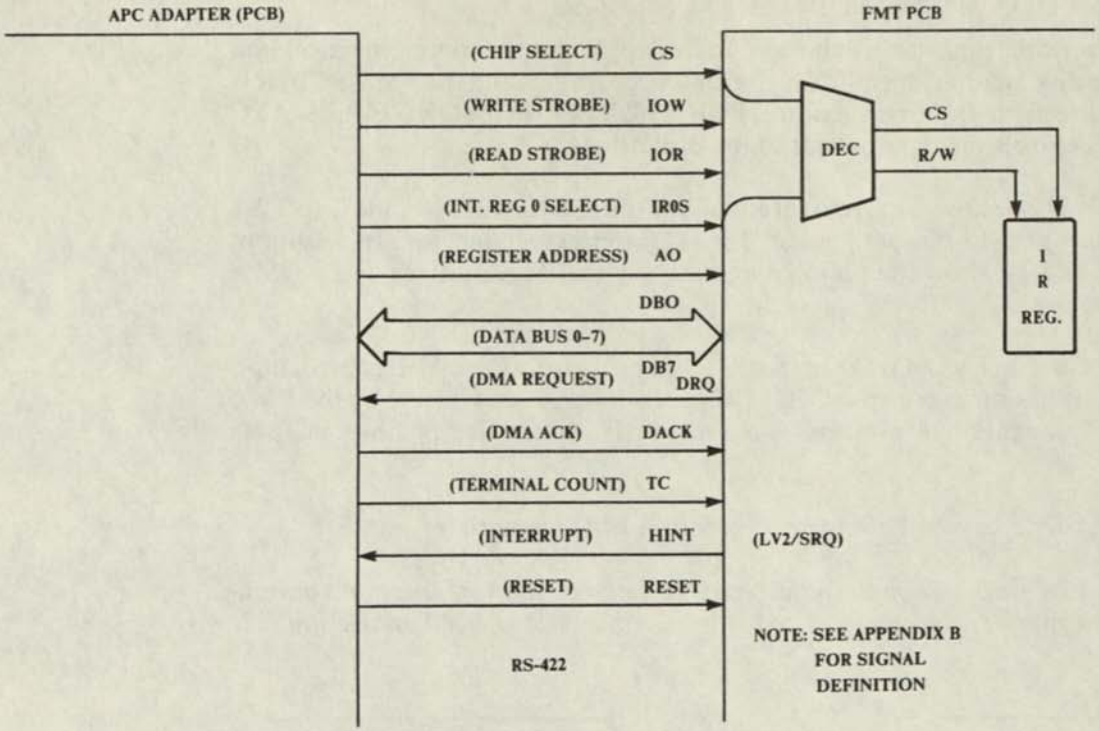


Figure 2-4 Interface Signals (Adapter to FMI)

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
1 26	GND		
2 27	IOW-H IOW-L	-	→
3 28	IOR-H IOR-L	-	→
4 29	HDCS-H HDCS-L	-	→

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
5 30	TC-H TC-L	–	→
6 31	IROS-H (*1) IROS-L	–	→
7 32	GND		
8 33	AO-H AO-L	–	→
9 34	RESET-H RESET-L	–	 →
10 35	DACK-H (*2) DACK-L	–	→
11 36			
12 37	GND		
13 38	DB7-H DB7-L	+	→ ←
14 39	DB6-H DB6-L	+	→ ←
15 40	DB5-H DB5-L	+	→ ←
16 41	DB4-H DB4-L	+	→ ←
17 42	DB3-H DB3-L	+	→ ←

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
18	DB2-H	+	→
43	DB2-L		←
19	DB1-H	+	→
44	DB1-L		←
20	DB0-H	+	→
45	DB0-L		←
21			
46			
22			
47			
23	DRQ-H	+	←
48	DRQ-L		
24	HINT-H	-	←
49	HINT-L		
25			
50			

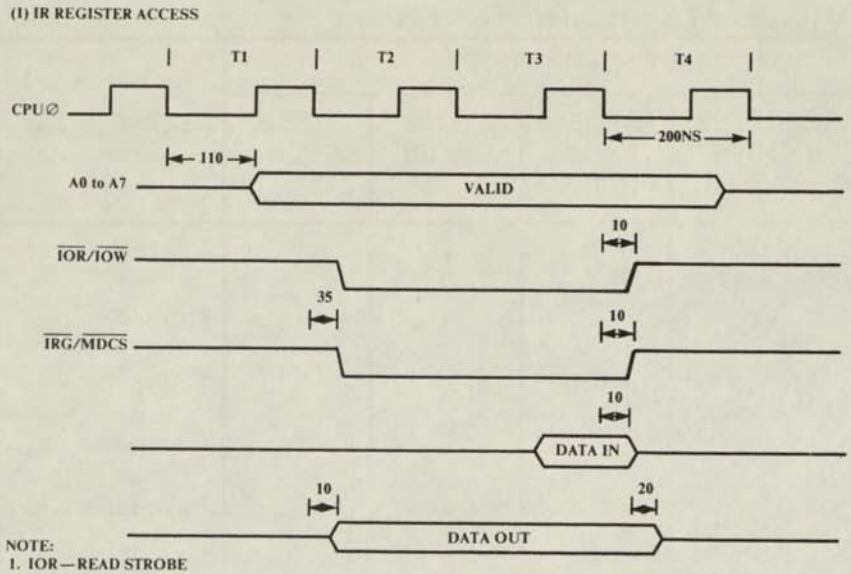


Figure 2-5 FMT Interface Timing

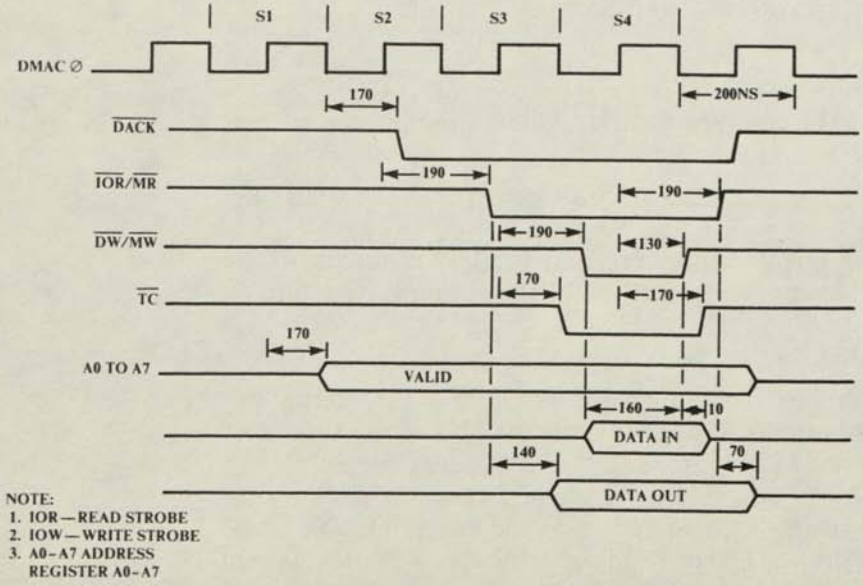


Figure 2-6 DMA Access Timing

Table 2-2 FMT Control Line Register Select/Function

REGISTER SELECT	FMT CONTROL LINES					FUNCTION
	HARD DISK CONTROLLER (HDC)	REGISTER ADDRESS (AD)	READ STROBE (IOR)	WRITE STROBE (IOW)	IR0 SELECT (IROS)	
IR3 READ	0	1	0	1	1	Result Status
IR3 WRITE	0	1	1	0	1	Parameter
IR2 READ	0	0	0	1	1	Status Reg.
IR2 WRITE	0	0	1	0	1	Command Reg.
IR2 READ	0	1	0	1	0	Info. Line
IR0 WRITE	0	1	1	0	0	Info. Line

0 — Designates active state of selected signal or register. For example, HDC = 0 and IOR (Read Strobe) = 0, HDC (FMTC) selected and Interrupt Register 3 (IR3 Read) addressed to read the result status.

2.1.2.4 INTERRUPT LOGIC

The interrupt logic processes FMT commands, DMA operations and the current error status for transmission to the APC control unit.

2.1.2.5 I/O DECODER

The I/O decoder monitors the bus controller (LS245) for I/O commands. The resulting command is returned to the bus controller for the appropriate action.

2.1.2.6 MAIN BUS CONTROLLER

The main bus controller (LS245) processes information from or to the internal bus (see Figure 2-1), the main bus in the APC control unit, the I/O decoder, address decoder, memory buffer and the FMT interface.

Two Programmable Array Logic (PAL), also known as the Programmable Logic Array (PLA), chips are used to decode I/O instructions from the main processor in the APC control unit and to control the bus interface.

2.1.2.7 MAIN PROCESSOR INTERRUPTS (INT) FROM THE APC

Interrupts to the main processor in the APC control unit are ORed with a mask designator through channel 14 in the disk adapter. Individual masking is possible with each interrupt. I/O instructions for read interrupt commands are incorporated prior to masking.

Interrupts

- DMIN —This interrupt occurs when a DMA data transfer between the FMT and the memory buffer is finished in a specified number of counts.
- HDIN —This interrupt designates the completion of a command to the FMT (HDIN = LV2 = CE + SRQ).
- MDER—Denotes error, signifying a memory access operation to the memory buffer from the APC control unit during a DMA operation.
- HDER —Denotes an error when a command is issued to HDC during an FMT command (The HDC is called the Hard Disk controller which is another name for the FMT controller described in Section 2.2).

2.1.2.8 MEMORY BUFFER

Memory is an 8K buffer that consists of four NEC 4016-3 2K × 8 bit static RAMs. In the main access mode the buffer is composed of odd and even numbered blocks and is common to the APC control unit. Address assignment is fixed at AC002 to AFFFF.

Under internal mode, the memory address is continuously assigned.

Data transfer between the buffer and FMT interface is controlled by the DMA controller. Access from the APC control unit is prohibited. If accessed by the APC control unit an error is flagged.

2.1.3 Programming Considerations

The programming considerations consist of a working knowledge of the main (APC) processors ability to access the DMA controller, memory buffer, interrupt registers and other related logic circuits in the disk adapter and HDC (or FMT controller).

Included in the programming considerations are the I/O address functions and bit maps, summarized in Section 2.1.3.2, all I/O byte operations to the main processor, and the word or byte formats to access the memory buffer. The following sections briefly describe the above operations and include additional operations, the knowledge of which, is recommended for successful programming of the HDC.

2.1.3.1 FMT I/O AND PROCESSOR MEMORY ACCESSIBILITY

In an HDC R/W data operation, during a DMA data transfer cycle, I/O and memory access operations from the main processor are not allowed. This action is because the disk adapter and main processor are not in sync with each other. Error detection logic is included to flag the respective HDC operation as an I/O access error (HDER) to the HDC, or a DMA memory access error (MAER) within the adapter. The following briefly describes the above error conditions and provides additional FMT/DMA operations.

1. FMT Complete Confirmation (Read Status)

   A read status register operation during an HDC operation generates an HDER error. To avoid this, completion of an FMT operation must be verified as follows.

   - With a read interrupt from the FMT.
   - Confirmation of an on-going HDC operation with a HDEX flag. This flag is set with a write command to FMT and is cleared by a seek Command End (CEL or CEH) or a Sense Interrupt Status Request (SRQ) command from the FMT.

2. FMT Operation Without a DMA Operation (for example, Seek Command).
   - Memory buffer accessability and I/O command operation to the DMAC allowed.
   - FMT I/O command allowed.
   - HDER generated with an I/O write command.

3. HDER Generation
   - Issuance of a DMAC/FMT I/O command during a DMA data transfer.
   - A command sent to the HDC before the HDC completes an operation.

4. MAER Generation—Access to memory buffer during a DMA data transfer operation.

2.1.3.2 I/O COMMANDS

This section categorizes the I/O commands and provides the appropriate commands, codes and other related information in Tables 2-3 through 2-7. Included are notes that briefly describe the operation and purpose of each command and related function.

Table 2-3 I/O Commands (DMA)*

CATE-GORY	I/O COMMAND		DATA FIELD (HIGH BYTE)								FUNCTION
	NAME	ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	
DMA Note 1	CHANNEL 1										
	DMA ADR. L	A3	A7	A6	A5	A4	A3	A2	A1	A0	
	DMA ADR. H	A3	A15	A14	A13	A12	A11	A10	A9	A8	Read/Write
	DMA Count. L	93	C7	C6	C5	C4	C3	C2	C1	C0	(Note 3)
	DMA Count. H	93	C15	C14	C13	C12	C11	C10	C9	C8	
	Status	A9	R03	R02	R01	R00	TC3	TC2	TC1	TC0	Read
	Write CMD	A9	KS	DS	WS	PR	TM	LE	AH	MM	(Note 2)
	Register Request	99	—	—	—	—	—	RE	CSI	CS0	Write
	Single Mask	AB						MSK	CSI	CS0	Write
	Mode Register	9B	MS1	MS0	ID	AT	TR1	TR0	CS1	CS0	Write
	Clear F/F	AD									Write
	TEMP. Register	9D	D7	D6	D5	D4	D3	D2	D1	D0	Read
	Master Clear	9D									Write
	All Make	9F					MB3	MB2	MB1	MB0	Write

* See (8237) DMA LSI Functional Specifications for details.

NOTES:
1. All unused channels (CH) except CH1 must be masked.
2. Data for command register is set to all zeroes.
3. DMA address bits, A15 and A14, are ignored if memory buffer is 16 KB or less.

Table 2-4 I/O Command (HDC/FMT)

CATE-GORY	I/O COMMAND		DATA FIELD (LOW BYTE)								
	NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HDC (3302 FMT)	Result Status	A0	D7	D6	D5	D4	D3	D2	D1	D0	Read (R)
	Parameter	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write (W)
	Status	92	CB	CEH	CEL	SRQ	RBQ	IER	NCI	DBQ	Read (R)
	Write CMD	92	CC4	CC3	CC2	CC1	CC0	UA2	UA1	UA0	Write (W)
3302 FMT (Notes)	Interface Register (IR)0	A2	—	CB	DACK	—	—	CE	LV2	SRQ	Read (R)
	IR0	A2	INTI	CLDB	RSTR	CLCE	0	EOP	0	HSR0	Write (W)

NOTES:
1. See 3302 FMT firmware functional specifications for detail. The FMT has the equivalent HDC I/O commands installed.
2. During a DMA operation an HDER is generated when the 3302 FMT is accessed with the execution of a format control operation.
3. LV2 interrupt bit for an IR0 read is the same as the HDIN interrupt bit for a read INT. command.

Table 2-5 I/O Command (RESET/INT)

CATE-GORY			DATA FIELD (LOW BYTE)								
	NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Reset (Note 1)	H/W Reset (RST)	94									RST Write (W)
INT Note 2	INT Reset	96					HDER	MAER	DMIN		RST Read (R)
	INI/HDEX	96			HDEX	HDER	MAER	DMIN	HDIN		Read (R)
	INI Mask Set	98					IDER	DMIN	HDIN		Set INT MSK

NOTES:
1. H/W RESET command resets the hardware.
2. Interrupt RESET command data bus bit assignment.

DATA BUS BIT	DATA BUS STATUS	DESCRIPTION
D0	DMIN	Interrupt reset by TC during DMA.
D1	MAER	Reset memory access error.
D2	HDER	Reset I/O command timing error.

Table 2-6 Read INT/HDEX Command*

DATA BUS		DESCRIPTION
BIT	STATUS	
D0	X	Don't care
D1	HDIN	HDC Interrupt
D2	DMIN	TC Interrupt in DMA
D3	MAER	Memory Access Error
D4	HDER	I/O Timing Error
D5	HDEX	HDC In Operation (Note)

* The read INT/HDEX I/O command is used to sense an interrupt and an HDC execution.

NOTE:
The HDEX flag is set when an FMT command write is issued, and reset by an HDC interrupt command complete (CEL, CEH, or SRQ) signal.

Table 2-7 INT Mask Set I/O Commands

DATA BUS		DESCRIPTION
BIT	STATUS	
D1	HDIN	HDC Interrupt Mask
D2	DMIN	DMA TC Interrupt Mask
D3	IOER	MAER and HDER Mask

NOTES:
1. Set mask logic "0" (logic "1" nonmask).
2. All mask set at initial reset time.

2.2 3302 FMT DISK DRIVE CONTROLLER

The 3302 FMT disk drive controller, also called the Hard Disk Controller (HDC) or FMT PCB, resides in the model APC-H26 stand-alone DKU and provides the interface and control signals to the disk drive assembly within the stand-alone DKU and the disk adapter in the APC control unit (see Figure 2-7). Also, the FMT PCB provides the interface to the disk drive in the expansion DKU when included in the system. The physical dimensions and attached interface and power connector placements for the FMT PCB are shown in Figure 2-8. The 3302 FMT controller is composed of four sandwiched layers, including the signal ground and dc power plains. The major logic elements are as follows.

- Z80 compatible microprocessor (μPD780).
- 8K RAM of local memory.
- 2K ROM for disk drive firmware.
- D8237 DMA controller that interfaces with the disk adapter, local memory and the disk drive.
- D8255AC Programmable I/O device designed to control the transmission of the disk drive status, the device address/head address, and the step pulse for a seek operation.
- μPD3302 disk control LSI which is controlled by a subcommand sequencer. It (LSI) is intended to perform a serialize/deserialize operation on data to or from the disk drive and to modulate/demoduolate the MFM recorded data.
- 8065 BEP LSI intended to perform polynomial functions and to generate correctable 1 bit burst type errors.

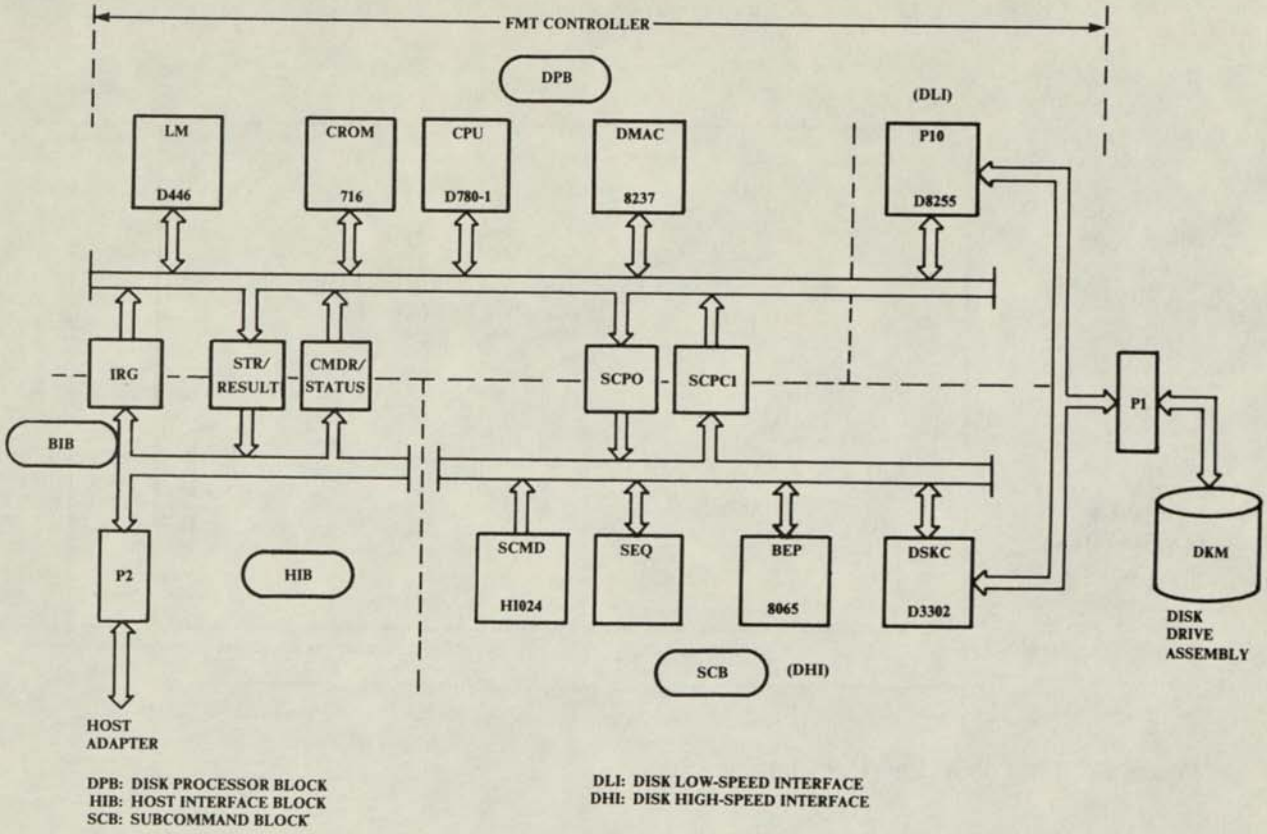


Figure 2-7 FMT Block Diagram

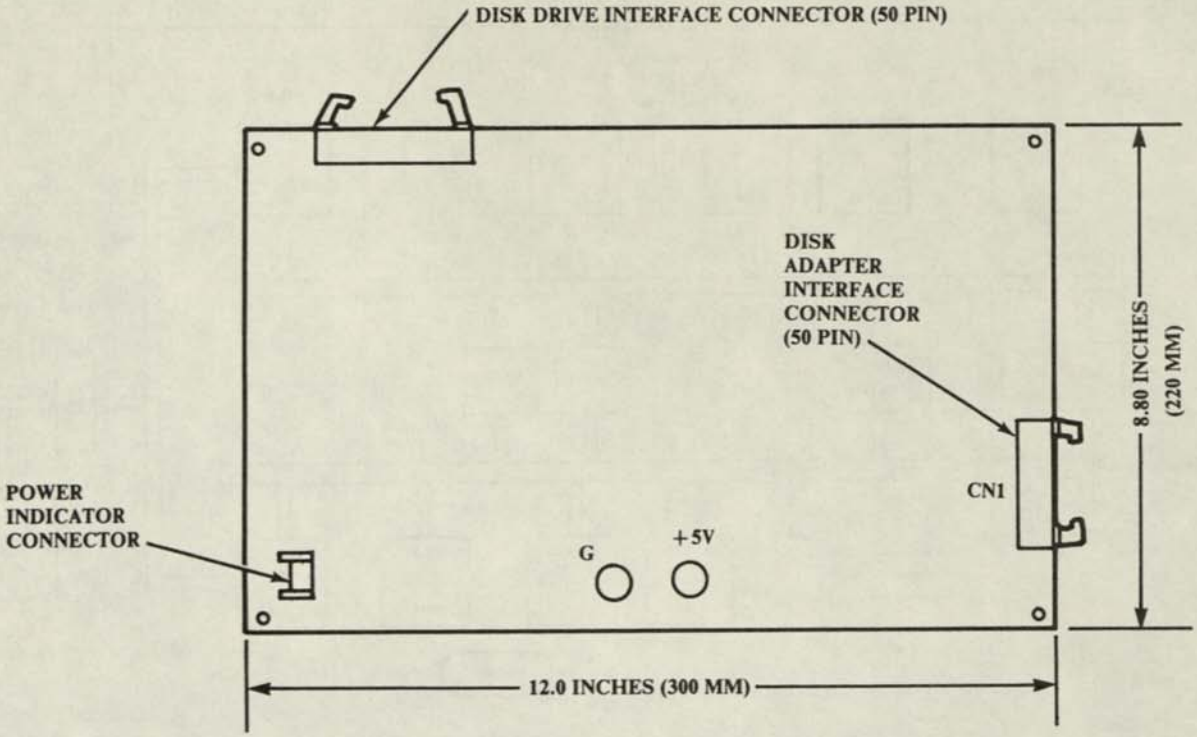


Figure 2-8 FMT PCB Physical Configuration

2.1.1 FMT Disk Operations

This section summarizes the functional capabilities of the FMT PCB operations. A more detailed description of each operation is provided in subsequent sections.

1. Performs seek operations to read or write data on a disk by moving the arm assembly (Read/Write heads) to the specified disk address.
2. Recalibrates the disk at head zero, cylinder zero.
3. Performs a read address seek operation to the specified disk address for transmission of the address to main memory.
4. Reads up to one cylinder of data from the DKU for transmission to main memory.
5. Writes up to one cylinder of main memory data into the DKU.
6. Verifies the transmission of up to a cylinder of data by checking the CHECK BYTE.

2.2.2 Firmware Overview

This section briefly describes the firmware characteristics and summarizes the firmware operation.

2.2.2.1 FIRMWARE CHARACTERISTICS

Firmware for the FMT PCB resides in the Z80 microprocessor, also called the Central Processing Unit (CPU), and provides the control procedures for all read/write and seek operations to the disk drive. It performs these procedures by decoding the main processor I/O instructions from the APC disk adapter. Firmware visibility with the adapter is provided by three registers; IR0, IR2, and IR3, all of which, reside on the FMT PCB (see Figure 2-9 and Table 2-2).

The transfer of data to form the command status and parameter/result status between the adapter and FMT is performed in the IR2 and IR3 registers (see Table 2-8). That is, initially, a disk command and its parameters are set in the IR2 and IR3 registers with an I/O command. The FMT firmware is then started and the data is stored in local memory. The Z80 CPU accepts and executes the I/O command. On completion the status is set in the IR2 and IR3 registers where they are sent to the main memory processor through the disk adapter. The IR0 register is used with firmware to set the command and receive the status (see Tables 2-9 through 2-11). The quantity of data transferred from or to the disk adapter corresponds to the number of sectors specified in the parameter.

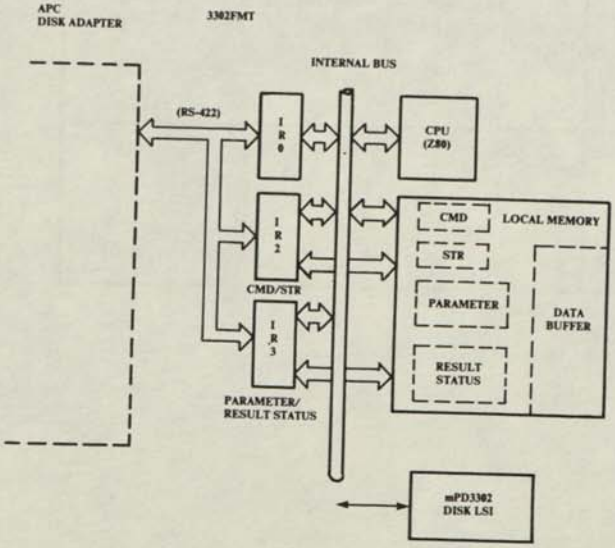


Figure 2-9 Firmware Hardware Interface

Table 2-8 FMT I/O Read/Write (Status) Commands

FMT COMMAND	R/W	I/O ADDRESS	3302 FMT
Result Status Read	R	AO	IR3 Read
Parameter Write	W	AO	IR3 Write
Status Read	R	92	IR2 Read
Command Write	W	92	IR2 Write

Table 2-9 FMT I/O Commands (RD/WR)

COMMAND	R/W	I/O ADDRESS	DATA BUS (LOW PART)							
			D7	D6	D5	D4	D3	D2	D1	D0
IR0 Read	R	A2	—	CB	DACKH	—	—	CE	LV2	SRQ
IR0 Write	W	A2	INTI	CLDB	RSTR	CLCE	0	E0P	0	HSRQ

Table 2-10 IR0 Write

DATA	NAME	DESCRIPTION	REMARKS
D0	HSRQ	SRQ interrupt mask	
D1	0	Must be zero	
D2	EOP	Notifies completion of the access to IR2/IR3 in the command set or status receive procedure...	After setting this bit, procedure completes 2 more accesses to IR2/IR3.
D3	0	Must be zero	
D4	CLCE	Interrupt LV2 reset	
D5	RSTR	Request start of the result status receiving procedure.	
D6	CLDB	Request start of disk command set procedure.	
D7	Initialize	Reset for 3302 FMT. Set 'ON', next 'OFF'. This signal must be more than 2μsec.	AUX command corresponds to RST.

Table 2-11 IR0 Read

DATA	NAME	DESCRIPTION	REMARKS
D0	SRQ	Seek end, equipment check, ready change: '1' Issue of sense interrupt request command requested. HSRQ masking constitutes a factor in the generation of LV2.	The same as bit 4 of STR (IR2, read)
D1	LV2	Interrupt signal	LV2 = HDIN = CE + SRQ·$\overline{\text{HSRQ}}$
D2	CE	End of disk command: '1' Next command setting or CLCE setting: '0' LV2 interrupt factor.	CE = CEL + CEH corresponds to bit 6 (CEH) and bit 5 (CEL) of STR.
D3	—	Don't care	
D4	—	Don't care	
D5	DACKH	'1': CLDB disk command setting mode and RSTR result status receiving mode are started and internal DMA is started for data transfer via IR3 register.	'1' is given on the command run of read/write data also.
D6	CB	Formatter busy.	The same as bit 8 of STR.
D7	—	Don't care	

2.2.2.2 FIRMWARE OPERATIONAL OVERVIEW

There are six operational phases performed by internal firmware. They consist of a Seek Command phase, an Idle phase, a Clear Data Buffer (CLDB) phase, a Run phase, a Control End (CE) phase, and a Result Status Read (RSTR) phase. Each is briefly described below.

1. Seek Command —Denotes a seek operation occurred in the idle state and sets LV2 (SRQ) interrupt (usually at end of seek).
2. Idle phase —Waits for, accepts, and processes seek commands and associated command parameters.
3. CLDB phase —Stores the command and command parameters and sequence steps for the next phase.
4. Run phase —Executes the command, processes the applicable data, and sets the LV2 (CE) interrupt at the end of the command cycle.
5. Control End (CE) phase —Status read into IR0/IR2.
6. Result Status Read (RSTR) —Result status read into IR3.

2.2.2.3 FIRMWARE START UP

The FMT firmware start up procedure is the same as that for the Hard Disk Controller (HDC) LSI. However, the start up I/O instruction to set the command and receive the status differ somewhat, and must be performed as shown in Figures 2-10 and 2-11 and described below.

1. Command Set
   a. Check Status Register for Controller Busy (CB).
      - If busy, wait.
      - If not busy continue with step b.
   b. Initiate Clear Data Buffer (CLDB) command through the auxiliary command register.
   c. Check status register for DACKH signal being on.
      - If on, continue with step d.
      - If off, wait.
   d. Send first parameter to Data Buffer Register.
   e. Send each additional parameter, one after the other to the data buffer register. There is a minimum of 2 between transfers.

f. Before sending the last parameter, initiate an End of Process (EOP) command through the auxiliary command register.

g. After last parameter is sent, send command to the command register.

h. Check Status Register for DACKH to be off.

i. When DACKH is off, The Central Processing Unit (CPU) can perform other operations, because HDC will signal when it is completed by sending an interrupt.

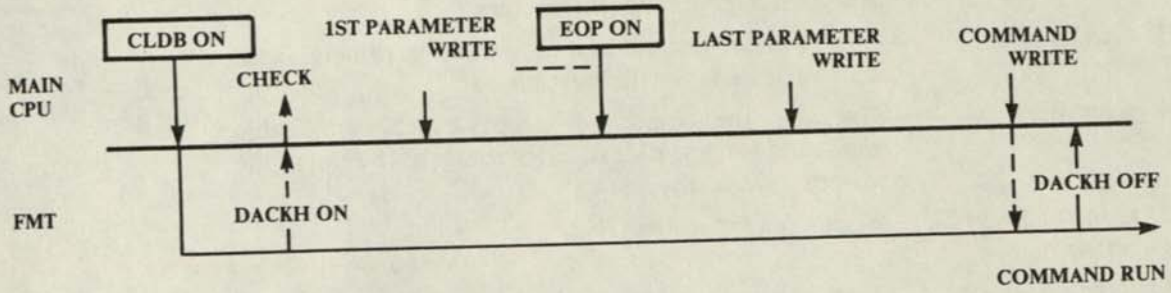
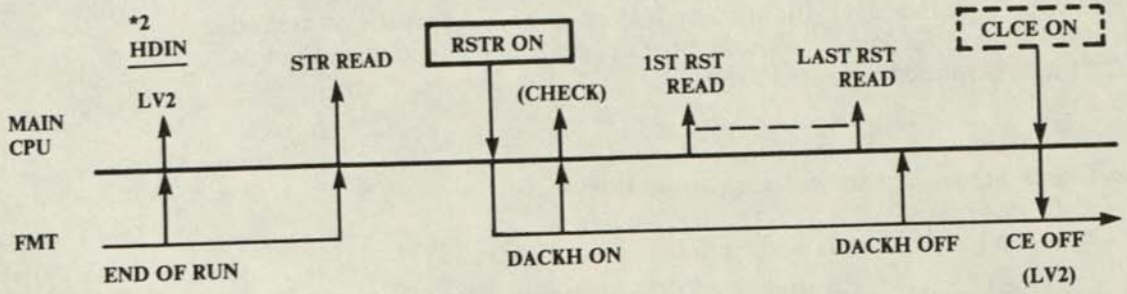


Figure 2-10 Command Set



*2 HDIN = LV2 = CE + SRQ*HSRQ

Figure 2-11 Receive Result Status

2. Receive Result Status
   a. Wait for interrupt to occur.
   b. Read interrupt register to determine what type of interrupt occurred.
   c. If an HDC interrupt has occurred, read the status register.
   d. If status/command indicates that it is necessary to read the request Result Status Read (RSTR) command through the auxiliary command register.
   e. Check status to see if DACKH is on.
      - If on, continue with step b.
      - If off, wait.
   f. Continue to read additional status, one after the other, as the command requires. A minimum of 2 is required between transfers.
   g. After last parameter is read, check status register for DACKH signal to be off. Indicates that the procedure is completed.
   h. Proceed to next command.

2.2.2.4 FIRMWARE FUNCTIONAL NOTATIONS

This section highlights the major DKU operations that a user should be aware of to understand the operation of the hard disk. The user should reference Figure 2-12 through 2-17 and Tables 2-12 through 2-18. The figures provide a flowchart of the Firmware operations, the sector format, and the appropriate timing diagrams. The tables provide the command code (Bits D7 through D4) for each command, the command name and resultant parameters, the appropriate parameters for each command, and tabulates the status in the respective status registers. Additional information is provided in Section 2.2.3.

1. A cylinder seek occurs with a Power On Reset operation or with a reset I/O command from the disk adapter (see Figure 2-12).

   A recalibrate operation is performed after every reset command.

2. After IRQ CLDB is set in a command set operation, the command operation requires a maximum delay of 50 secs for DACKH to turn on, after which, the command set operation continues. After EOP sets, the command set operation ends with two access operations (last parameter and command) and DACKH turns off.

3. The receive status operation also requires a maximum delay of 50 secs for DACKH to turn on. After RSTR sets, the operation is the same as described in step 2 above. With the number of status results determined by an execute I/O command, DACKH turns off after the final status result is read. When the number of read status is smaller than the number of result status, stalls occur causing a wait state.
4. In some cases DACKH turns on during the execution of a read/write data command.
5. The command set and receive status operations cannot be reset once they are in operation.
6. In seek and recalibrate command operations an SRQ interrupt occurs after Control End (CE) is on resulting in a new time difference between the interrupt and CE. A new command can be executed with CE on during any SRQ occurence.
7. In systems equipped with two or more DKUs a new command to the second DKU is permissible as the first DKU is performing a seek operation. An SRQ interrupt is sent when the new command ends, but the SRQ status is held until this time. However, the SRQ status is reset if the DKU that ended a seek command commences another command before accepting the SRQ status. Accordingly, a seek command can be sent to the same DKU after the SRQ status is received.

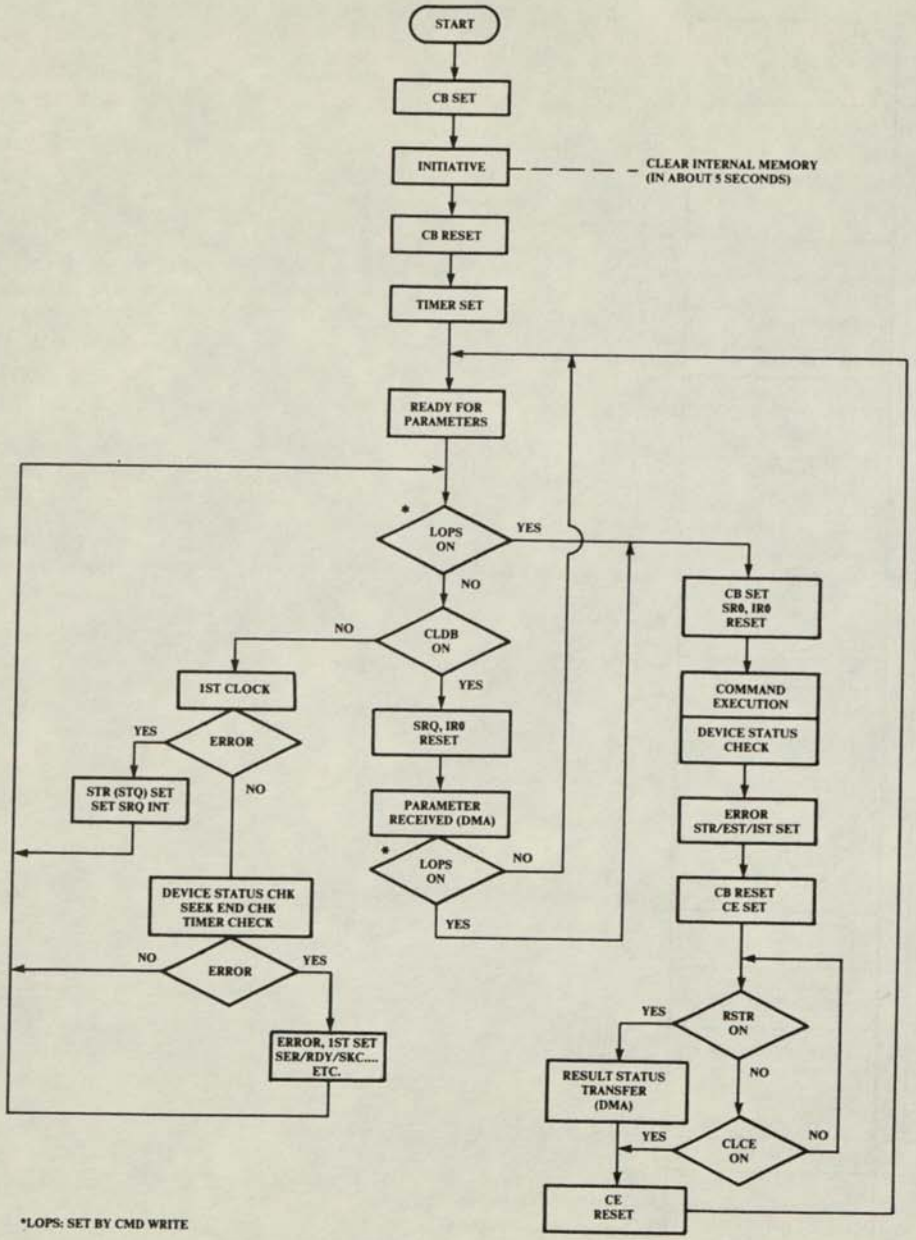


Figure 2-12 FMT Firmware Flowchart

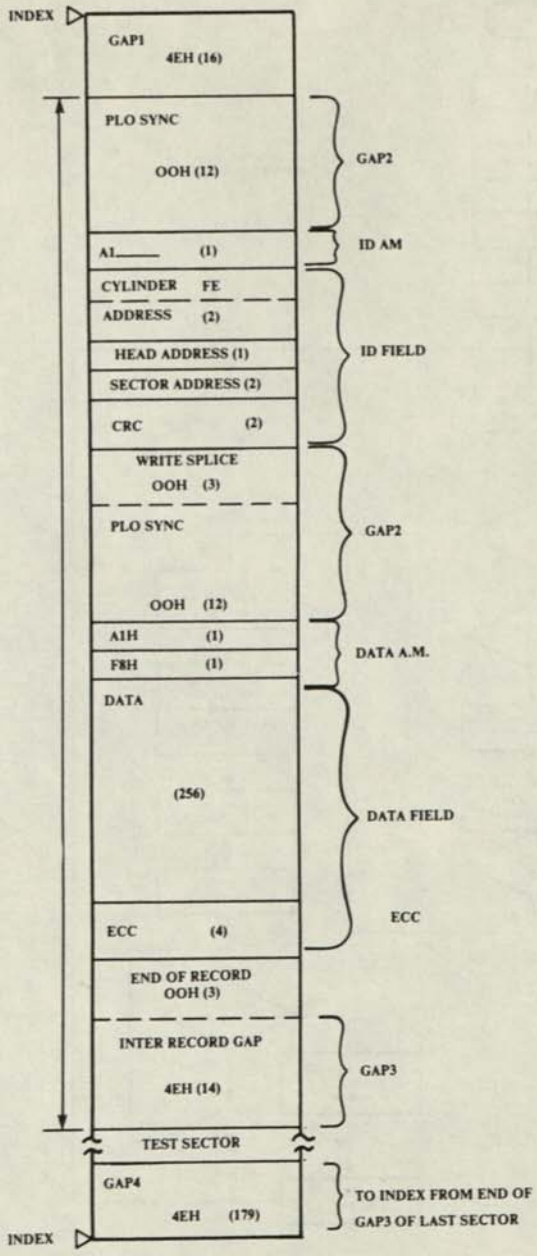


Figure 2-13 Sector Map (Disk)

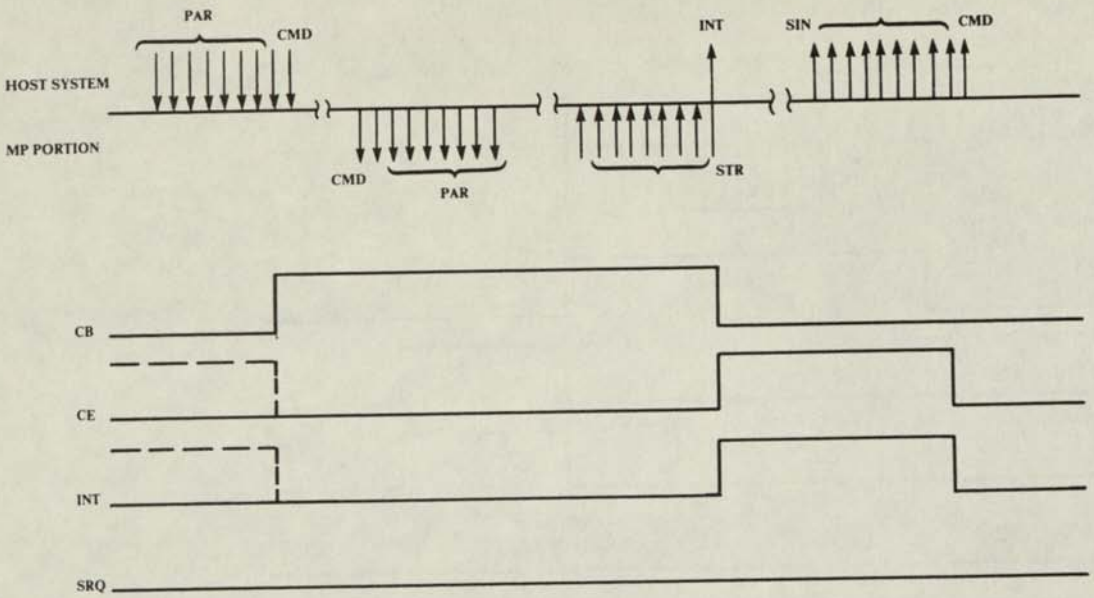


Figure 2-14 Read/Write Command Timing

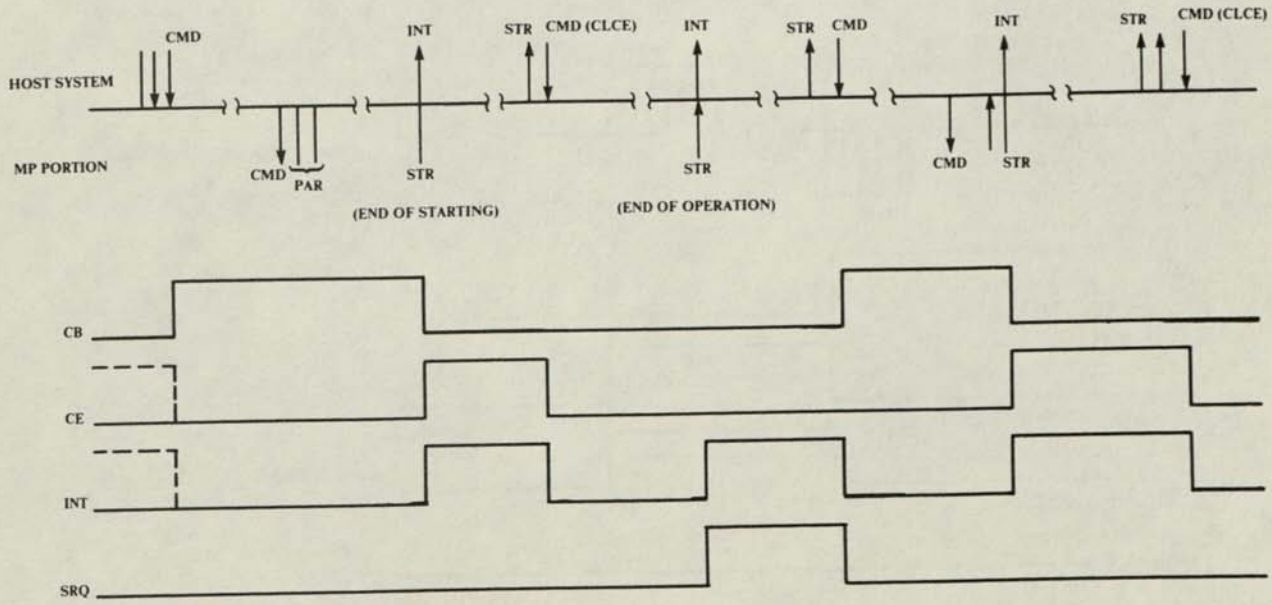


Figure 2-15 Seek/Recalibrate Timing

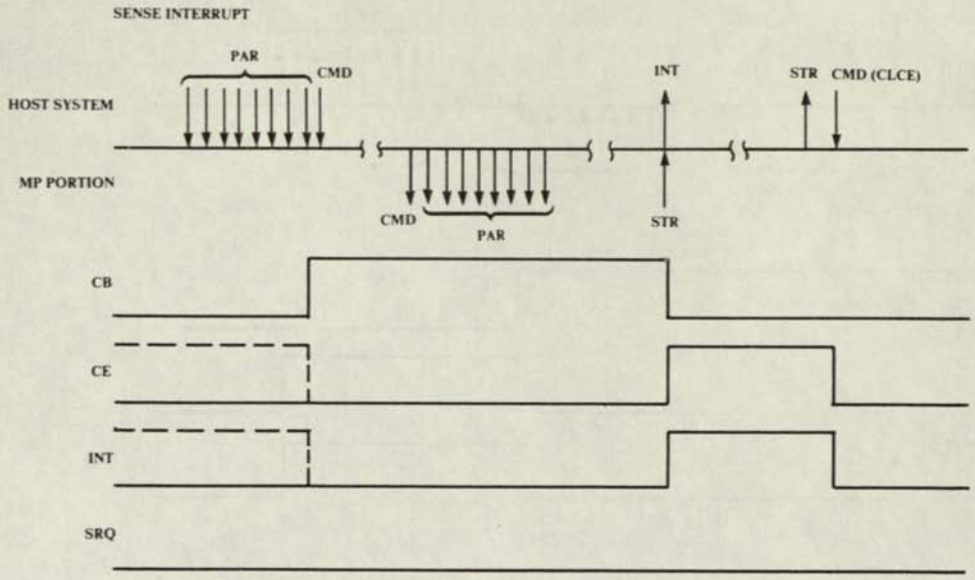


Figure 2-16 Sense Interrupt Timing

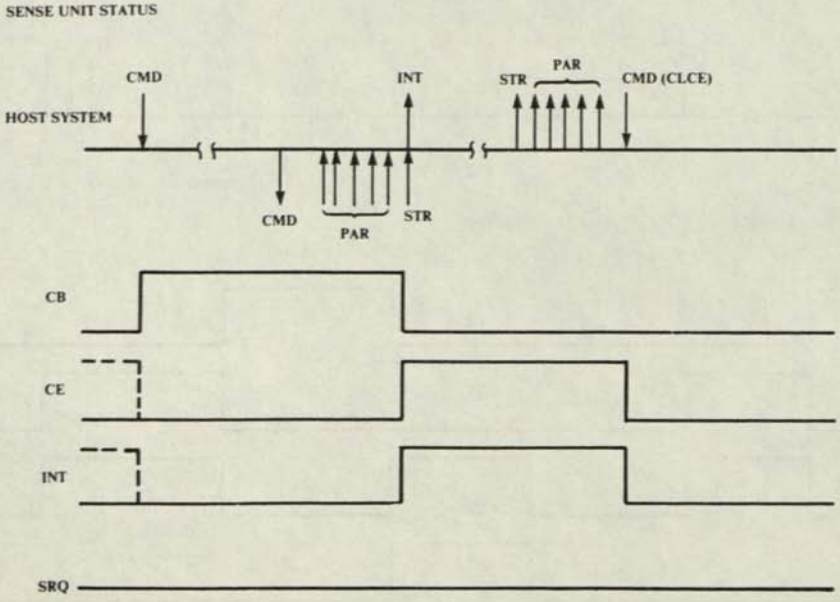


Figure 2-17 Sense Unit Status

Table 2-12 Commands/Status Results

COMMAND	OPERATIONAL PHASE	COMMAND BIT A0 = X*	Data Register (Low Byte)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Recali-brate	Command	0	0 1 0 1 0 UA	Command and unit address (UA)
	Result	0	Status Register	Status Register (STR)
Seek	Command	0	0 1 1 0 1 UA	Command and unit address
		1	Physical Cylinder Number	High Byte (PCNH)
		1	Physical Cylinder Number	Low Byte (PCNL)
	Result	0	Status Register	STR
Write ID	Command	0	0 1 1 1 0 UA	Command and unit address
		1	Physical Head Number	PHN
		1	Sector Count	SCNT
		1	Data Pattern	DPAT
		1	Gap Length 1	GPL1
		1	Gap Length 3	GPL3
	Result	0	Status Register	STR
		1	End Status	EST
			Sector Count	SCNT
Read ID	Command	0	1 0 0 1 0 UA	Command and unit address
		1	Physical Head Number	PHN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Sector Count	SCNT

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Read Data	Command	0	1 0 1 1 X UA	Command and unit address (UA)
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Sector Count	SCNT
	Result	1	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
Check	Command	0	1 1 0 0 X UA	Command and UA for CMD set.
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Write Data	Command	0	1 1 1 1 X UA	Command and unit address (UA)
		1	Physical Head Number	PHN
		1	Logical Cylinder Number 1	LCN 1
		1	Logical Cylinder Number 2	LCN 2
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number 1	High Byte (PCNH)
		1	Logical Cylinder Number 2	Low Byte (PCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
Sense Interrupt Status	Command	0	0 0 0 1 X X X X	For CMD set
	Result	0	Status Register	STR
		1	Interrupt Status	IST
Sense Unit Status	Command	0	0 0 1 1 X UA	Command and unit address (UA)
		1	Status Number n	STN n
		1	Status Number n	STN n N=1: Summary Status =2: Detailed Status (HDC Detail 6) Set: Status number only
	Result	0	Status Register	STR
		1	Unit Status n	USTn n=same as
		1	Unit Status n	USTn above

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Invalid	Command	0	All Zeroes	Command
	Result	0	Status Register	STR (60)
Detect Error	Command	0	0 1 0 0 X X X X	For CMD set
	Result	0	Status Register	STR
		1	Error Address	High Byte (ADRH)
		1	Error Address	Low Byte (ADRL)
		1	Error Pattern 1	EPAT 1
		1	Error Pattern 2	EPAT 2
		1	Error Pattern 3	EPAT 3

* A_0 = 0—Command Register or status register access.
A_0 = 1—Parameter or result status access.
** Data register bits D7 through D4—command code.

Table 2-13 Parameters

COMMAND	PARAMETERS	
	NAME	HEX VALUE
SEEK	Present Cylinder Number High (PCNH) Byte	0
	Present Cylinder Number Low (PCNL) Byte	00 to B4
Write ID Write Data Read ID Read Data Check	Present Head Number (PHN)	00 to 07
	Sector Count (SCNT)	00 to FF
Write ID	Data Pattern (DPAT)	Any
	Gap Length 1 (GPLI)	10
	Gap Length 3 (GP3)	0E
Check Read Data Write Data	Logical Cylinder Number High (LCNH) Byte	FE
	Logical Cylinder Number Low (LCNL) Byte	00 to B4
	Logical Head Number (LHN)	00 to 07
Sense Unit Status	Logical Sector Number (LSN)	00 to 19
	Status Number 1 (STN 1)	Any

Table 2-14 (STR) Status Register

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	Controller	CB	1: a command is sent to HDC from the host system. 0: Controller busy (D7) reset when the host system is interrupted by HDC.
D6 D5	Command End	CEH	D6 | D5 0 | 0 Command in progress or no command sent after last reset signal or CLCE. 0 | 1 : Abnormal End 1 | 0 : Normal End 1 | 1 : Invalid Ending
D4	Sense Interrupt Status Request	SRQ	With SEN, EQC, or a change in RDY detected this bit (D4) sets initiating a SRQ from HDC.
D3	0	—	
D2	0	—	
D1	0	—	
D0	X	—	

Table 2-15 (EST) Error Status

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	End of Cylinder	ENC	Set when access is continued beyond the maximum sector number of one cylinder.
D6	0	—	
D5	Data Error	DER	Set when the data on a disk is read and an error is detected.
D4	Equipment Check	EQC	Set when a 'fault' signal is reported by the device.
D3	Not Ready	NR	Set when the device cannot perform both read and write.
D2	No Data	ND	Set when a designated sector is not detected on the track.
D1	0	—	
D0	Missing Data Mark	MDM	Set when a disk is read and the address mark of the data portion is not detected.

Table 2-16 (IST) Interrupt Status

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	Seek End	SEN	End of seek operation
D6	Ready Change	RC	The status of the device has changed.
D5	Seek Error	SER	A seek error has occurred.
D4	Equipment Check	EC	Set when a 'fault' signal is reported by the device or track '0', seek complete signal is not detected within a fixed time on 'seek' or 'recalibrate' command run.
D3	Not Ready	NR	Set then the device cannot perform both read and write.
D2	Unit Address	UA2	The device number on interruption.
D1		UA1	
D0		UA0	

Table 2-17 (US1) Unit Status 1

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7			
D6			
D5			
D4	1 (Must Be One)		1
D3	Seek Complete	SC	End of seek operation
D2	Track 00	T0	Positioner is positioned at cylinder '0'.
D1	Ready	RDY	The spindle makes enough revolutions and the data area is normally loaded with a R/W head.
D0	Write Fault	WF	Turns on in any of the following cases. • Loss of Voltage • Clock Fault • Positioner of Track • Write Fault • Head Fault • Head Select Fault

Table 2-18 (US2) Unit Status 2

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7			
D6			
D5			
D4			
D3			
D2	Device Type	DT	Always a 1-10 MB DKU
D1	Detailed Status 1	ST1	The code—ST0 or 1—of the detailed status information held by the device.
D0	Detailed Status 0	ST0	ST0 ST1 0 0 Spindle Speed Loss 0 1 Not Track 000 1 0 Read/Write Fault 1 1 -------

2.2.3 Command Functional Overview

This section provides a brief functional description of the following disk commands.

- Check
- Read Data
- Read ID
- Recalibrate
- Write Data
- Write ID
- Seek
- Sense Interrupt Status
- Sense Unit Status

2.2.3.1 CHECK COMMAND

The data from the data sector, selected by the Logical Cylinder Number High Byte (LCNH), Logical Cylinder Number Low Byte (LCNL), Logical Head Number (LHN), and the Logical Sector Number (LSN) during the command phase, is read but is not sent to the host system. It is treated in the same manner as a read data command described in steps 2 through 9 of the next section.

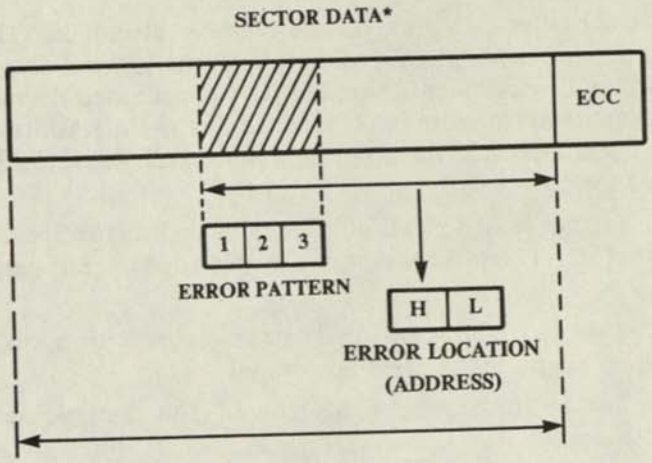
2.2.3.2 READ DATA COMMAND

1. The sectors designated by the Logical Cylinder Number High (LCNH) byte, the Logical Cylinder Number Low (LCNL) byte, the Logical Head Number (LHN), and the Logical Sector Number (LSN), activated during the command phase, are read from the DKU selected by the Unit Address (UA). This address is contained in the command word (see Table 2-12) from the host disk adapter.
2. Upon completion of a sector read operation in a multi-read sector operation, the Sector Count (SCNT) and LSN signals are upgraded to read data from the next sector.

   When the SCNT reaches zero the result (end) status is set with a stop instruction and the host adapter is notified accordingly.

   If the LSN equals the End Sector Number (ESN), the LHN is changed and the read process continues.
3. If the SCNT does not equal zero upon completion of read from the last sector, that is, the Last Sector Number (LSN) = the End Sector Number (ESN) or the Logical Head Number (LHN) = the End Track Number (ETN), the command run sequence is terminated with the End of Cylinder (ENC) bit on in the Error Status (EST) byte (see Table 2-15). The Status Register (STR) shows an abnormal ending (see Table 2-14).
4. When a fault signal is read from the device, command run is terminated with the Equipment Check (EQC) bit on in the EST byte. The STR shows an abnormal ending.
5. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.

6. If a read error is detected in the Error Correct Code (ECC), the error is checked to determine if it is a recoverable or unrecoverable error. If recoverable, the error location and data pattern are stored and command run is terminated with the Data Error (DER) bit on in the EST byte (see Table 2-15). The host fetches this information with the detect error command to make the necessary corrections.



* SEE FIGURE 2-13

If an unrecoverable error was detected the detect error command is terminated with the DER bit on in the EST byte. The Status Register (STR) shows an abnormal ending (see Table 2-14).

7. If a designated sector is not found after a second index mark is detected, command run is terminated with the No Data (ND) bit on in the EST byte. The STR shows an abnormal ending.

8. When the Terminal Count (TC) signal turns on, data transfers to the host stops. However, a sector read operation continues until the sector designated by the Sector Count (SCNT) is found, or until another abnormal operation occurs.

9. The resulting status for a normal termination of a command are shown below.

Normal End Status

LAST SECTOR TRANSFERRED			RESULT STATUS			
LCNL	LHN	LSN	LCNH	LCNL	LHN	LSN
		0 ESN–1	No change	No change	No change	LSN+1
	0 ETN–1	ESN	No change	No change	LHN + 1	00
LCVL≠256	ETN	ESN	No change	LCNL+1	00	00
LCNL≠256	ETN	ESN	LCNH+1	00	00	00

NOTE: LHN (PHN) shows the head number for the last sector data transfer.

With an abnormal command termination the error position is set as the result status.

10. If a data address is not present after the VFO SYNC for data, command run is terminated with the Missing Data (MDM) bit on in the EST byte.

2.2.3.3 READ ID

1. A read ID operation reads the cylinder, head and sector address and the Cyclic Redundancy Character (CRC) from the ID field starting with the first sector on a track designated by the Physical Head Number (PHN) signal (see Figure 2-14). If the CRC is normal (no errors) and the address data is sent, the process stops after sending one ID data field, and command run is terminated. If abnormal, the ID data field is not sent and the process continues.
2. When a sector read operation is incomplete before SCNT equals zero, the result status contains a No Data (ND) status and the host is notified accordingly.

3. If a fault signal is received from the device the commmand run terminates with the Equipment Check (EQC) bit on in the EST byte (see Table 2-15).
4. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.
5. If a designated sector is not found after a second index mark is detected, command run is terminated with the ND bit on in the EST byte.

2.2.3.4 RECALIBRATE

1. Seek to cylinder zero.
2. Recalibrate End of Start—Command run is normally ended after a step pulse signal is sent 256 times.
3. Recalibrate End of Operation—Track zero (T0) signal is checked at the above fixed pulse rate. When set, the recalibrate operation is normally terminated with Seek End (SEN) bit on in the IST (see Table 2-16) and the Sense Interrupt Status Request (SRQ) set.

   If the T0 (00) signal is not on after the above rate is exceeded, the recalibrate operation is terminated with the Seek Error (SER) BIT on in IST.

   If the device is Not Ready (NRY) or a fault is detected the recalibrate operation is terminated with the NRY or EQC bit on.
4. The Interrupt Status (IST) is set and the host system obtains the result of the recalibrate operation with the Sense Interrupt Status command (see Section 2.2.3.8).

2.2.3.5 WRITE DATA

1. Data from the host system is written to the sector designated by the Logical Cylinder Number High (LCNH) byte, the Logical Cylinder Number Low (LCNL) byte, the Logical Head Number (LHN), and the Logical Sector Number (LSN) in the DKU selected by the Unit Address (UA) field in the command byte (see Table 2-12).
2. Upon completion of a sector write operation, in a multi-write disk operation, the sector counter (SCNT) and the LSN signals are upgraded to write data in the next sector.

   When the SCNT reaches zero the result (end) status is set with the stop instruction and the host system is notified accordingly.

   If the LSN equals the End Sector Number (ESN), the LHN is changed to LHN + 1, the head assignment is changed, and the write process continues.

3. If the SCNT does not equal zero upon completion of a write in the last sector, the command run sequence is terminated with the End of Cylinder (ENC) bit on in the Error Status (EST) byte (see Table 2-15).
4. When a fault signal is received from the device, command run is terminated with the Equipment Check (EQC) bit on in the EST byte.
5. If the device is Not Ready (NRY), command run terminates with the NRY bit on in the EST byte.
6. If a designated sector is not found after a second index mark is detected, command run is terminated with the No Data (ND) bit on in the EST byte.
7. The resulting normal ending status is shown in the chart in step 9, Section 2.2.3.2.
8. When the Terminal Count (TC) signal turns on, all zeroes are written on the remaining sector area. However, the sector write operation continues until the sector count in the SCNT is reached, or until an abnormal operation occurs.

2.2.3.6 WRITE ID

1. A write ID operation writes the cylinder, head and sector address, and causes the generation of the Cyclic Redundancy Character (CRC) in the ID field starting with the first sector following the index mark on a track designated by the Physical Head Number (PHN).
2. Upon the completion of a write sector operation and the Sector Counter (SCNT) equals zero, the result (end) status is set with a stop instruction and the host system is notified accordingly.
3. If a fault signal is detected from the device the command run terminates with the Equipment Check (EQC) bit on in the Error Status (EST) byte (see Table 2-15).
4. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.

2.2.3.7 SEEK OPERATION

1. Causes arm/head assembly to seek (search) the disk (platters) for the Object Cylinder Number (OCN) designated by the Physical Cylinder Number (PCNH/PCNL) during the command pause.

2. End of Seek Start Operation

   With the Present Cylinder Number (PCN) less than the OCN, repeat PCN+1 and command run (Step in Pulse) until PCN equals OCN.

   With the PCN greater than OCN, repeat PCN–1 and command run (Step Out Pulse) until PCN equals OCN.

   In either case, with PCN equal to OCN, indicates that the command and parameter are received and command run terminates normally.

3. End of Seek Operation (Seek Complete)

   A Seek Complete (SC or SKC) signal is checked at a designated pulse rate. If this signal is on, the seek operation is terminated normally and the Sense Interrupt Status Request (SRQ) signal is on with Seek End (SEN).

   If the seek complete signal is not on after a fixed time interval (the difference between OCN and PCN), the seek operation terminates with the SER flag on.

   If the device is Not Ready (NRY) or a fault signal occurs, the seek operation is terminated and the NRY or EQC bit is on.

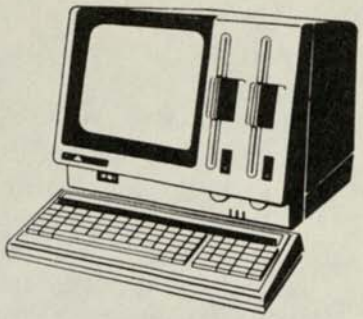
4. When the Sense Interrupt Status command is sent from the host the Interrupt Status (IST) flag is examined and the host is notified accordingly.

2.2.3.8 SENSE INTERRUPT STATUS

1. This command notifies the host of the following device status.
   - End of a seek operation (Seek or Recalibrate Operation).
   - Device ready or not ready.
2. If this command is sent without the Sense Interrupt Status Request (SRQ) signal on, an abnormal termination occurs.

2.2.3.9 SENSE UNIT STATUS

Notifies the host of a Unit Status 1 (US1) or Unit Status 2 (US2) device status (see Tables 2-17 and 2-18).



Chapter 3

Disk Drive Assembly

This chapter describes the physical characteristics and functional capabilities of the disk drive assembly used in the Model APC-H26 and Model APC-H27 Disk Units (DKUs). Both DKUs are briefly described in Chapter 1. DKU installation information is highlighted in subsequent sections with more detailed information provided in the Hard Disk Subsystem Installation Guide (Document No. 819-000102-9001).

The disk drive assembly is of modular construction designed to conserve space, enhance overall performance, and to eliminate periodic maintenance. The drive assembly uses 5.25 inch metal oxide platters, also called, disks or plates, and Winchester-type technology that provides the most modern method of storing information for high-speed computer operations and accessability. Many other features are available, several of which, are as follows.

1. Horizontal or vertical mounting.
2. 5-phase stepping motor (reduces track-to-track seek time to less than 2 ms).
3. Buffered operation (enhances random access seek operations).
4. Cam-operated swing arm mechanism (designed to support and drive the read/write heads).
5. Variable Frequency Oscillator (VFO—designed to process Return-to-Zero (RZ) data).
6. Winchester-type read/write heads (provides the latest recording method).

3.1 PHYSICAL/FUNCTIONAL ORGANIZATION

Figure 3-1 illustrates the modular construction and compactness of the disk drive assembly, and Figure 3-2 provides a functional block diagram of the disk drive logic. The disk drive assembly, also called the Disk Enclosure (DE), consists of a base plate, a swing out read/write head mechanism, magnetic read/write heads, a top sealing cover, and many other subassemblies shown in Figure 3-1. Note the "Air-Flow" path through the module when the sealing cover is in place. Included are the G9QKQ or G9NXT logic PCB and the G9QKR VFO PCB (the latter is not shown in the illustration).

The G9NXT PCB, and when installed, the G9QKR PCB, are referred to as a "Package Assembly" and provides the following disk drive logic functions (see Figure 3-2).

1. G9NXT Interface/Control Logic
   a. Interface Logic
      The interface logic consists of a microprocessor, LSIs, and other logic elements, designed to route data, addresses, device status and control signals between the disk drive and the FMT controller.
   b. Motor Logic (DC Motor AMP)
      The motor logic provides the dc power to drive the spindle motor and to control its rotational speed, and also to drive the stepping motor for seek operations.
   c. Read/Write Logic
      The read/write logic writes MFM-encoded data from the interface onto a disk (platter) and reads the MFM data from the selected disk and sends it to the interface logic for processing (also see VFO logic).
2. G9QKR VFO Logic
   The VFO logic separates clocks from MFM recorded data during a read data operation, synchronizes the clocks with the data, and sends the clocked data to the FMT as Read Clocks (RCK). The VFO performs no other operation and is required in both the stand-alone DKU and the expansion DKU.

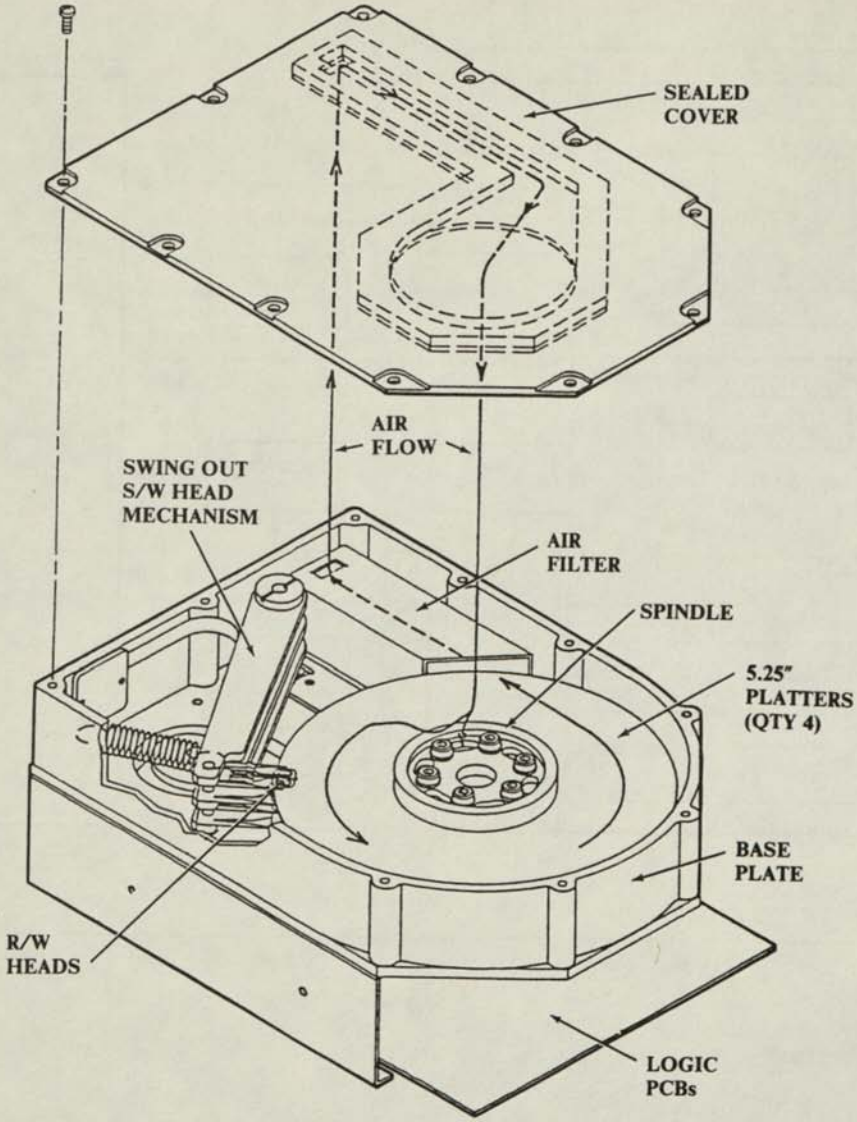


Figure 3-1 APC Disk Module (Exploded View)

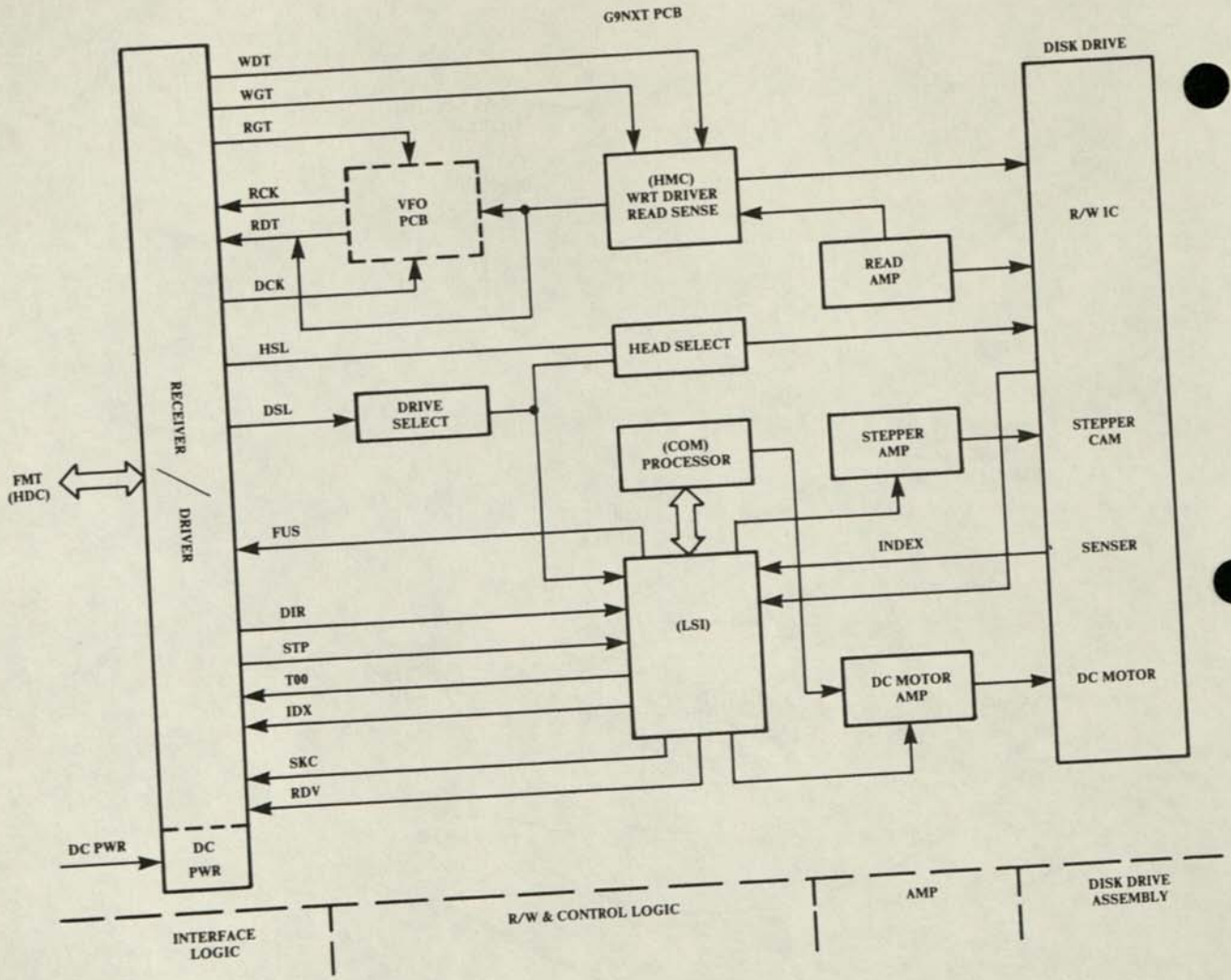


Figure 3-2 Functional Block Diagram

3.2 ENVIRONMENTAL CONSIDERATIONS AND FUNCTIONAL SPECIFICATIONS

The environmental considerations and functional specifications for the disk drive are the same as those for the DKU as described in chapter 1, Section 1.5. This is because the DKU houses the disk drive assembly and associated logic, power supply, and so forth. The only difference is the overall dimension and weight of the disk drive assembly when removed from the DKU, and are as follows.

	Disk Drive Assembly
1. Depth	8.12 inches (203 mm)
2. Height	4.06 inches (101.6 mm)
3. Width	5.84 inches (146 mm)
4. Weight	7.7 lbs (3.5 Kg)

3.3 ADDRESS/POWER/TERMINATOR CONNECTOR CONSIDERATIONS

The disk assembly contains the address, power, and terminator plugs and connectors as shown in Figure 3-3. The address and terminators are normally set at the factory. If changes are desired refer to the Hard Disk Subsystem Installation Guide for details. Additional connector information is provided in subsequent sections.

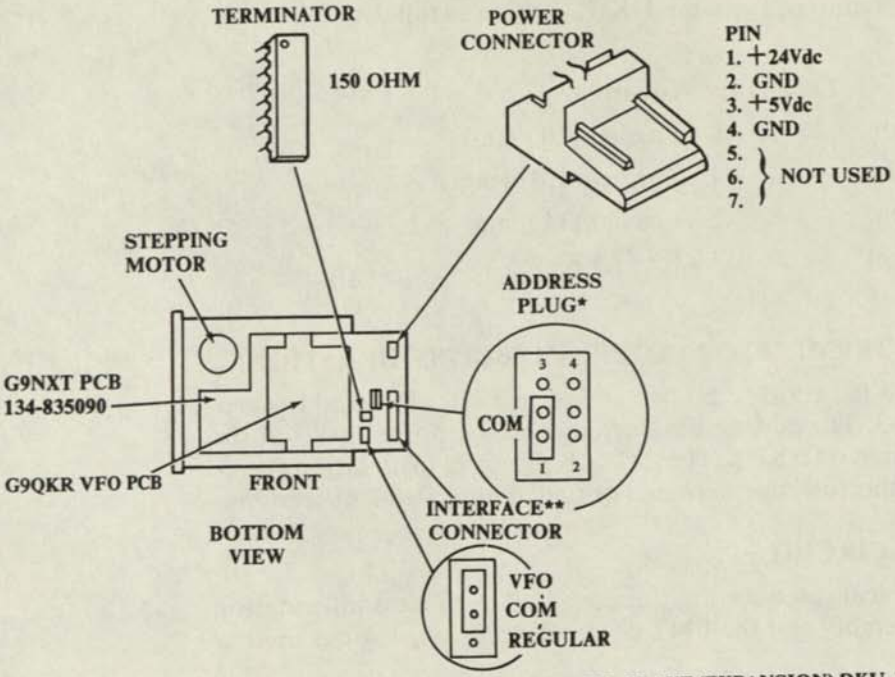
3.4 INTERFACE LOGIC CIRCUITS

Figure 3-4 illustrates a typical interface logic circuit used to process information between the disk drive assembly and the FMT controller. Positive logic is used as shown below.

Logic "0" = 0.00 Vdc to 0.40 Vdc
Logic "1" = 4.75 Vdc to 5.25 Vdc

3.5 INTERFACE CABLING CONSIDERATIONS

Figure 3-5 illustrates the type interface connector used on the disk drive assembly and provides the pin to pin assignment in each connector. Included are the signal names assigned to each pin.



* ADDRESS PLUG SET FOR MASTER (STAND-ALONE) DKU. SLAVE (EXPANSION) DKU-JUMPER PIN 2 TO COM (COMMON).
** CONNECTOR ON G9NXT PCB.

Figure 3-3 Terminator/Address Plug Layout

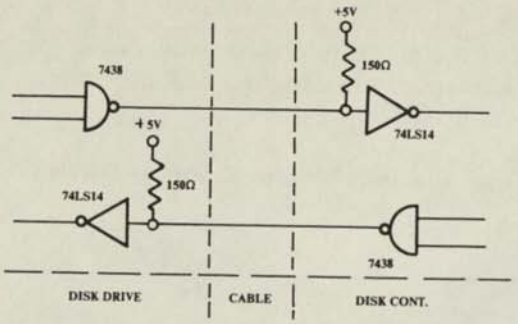
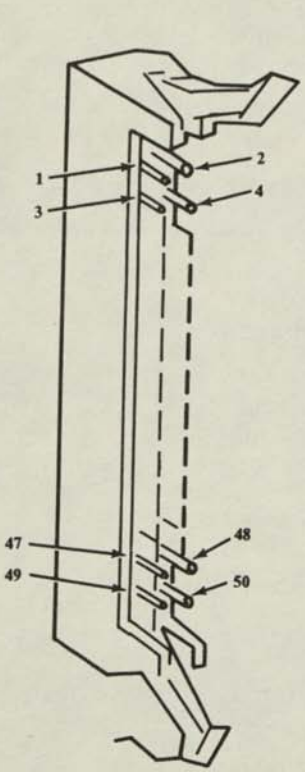
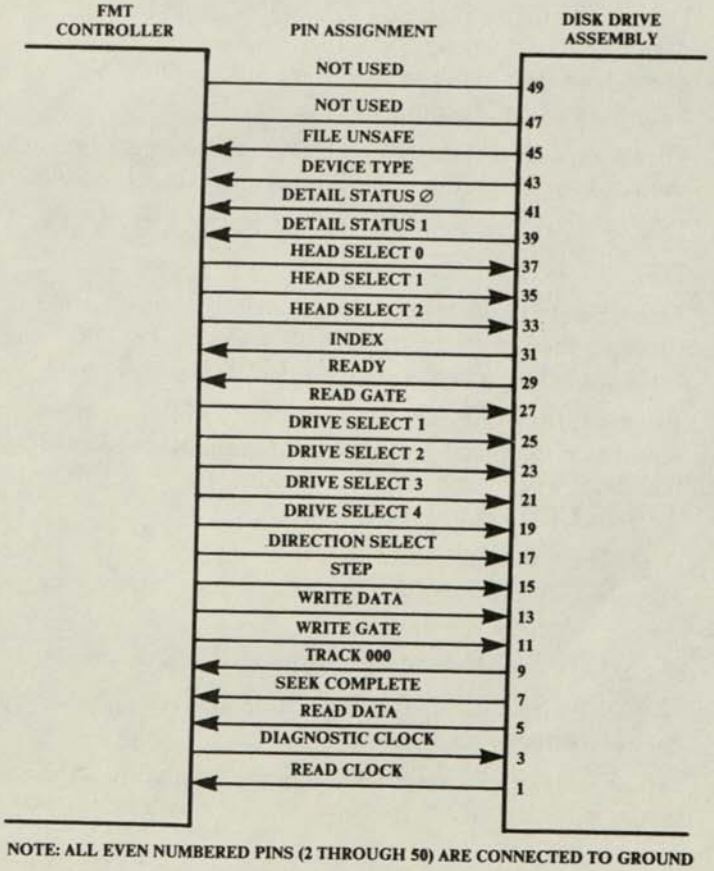


Figure 3-4 Typical Interface Logic Circuit





NOTE: ALL EVEN NUMBERED PINS (2 THROUGH 50) ARE CONNECTED TO GROUND

Figure 3-5 Interface Cable Connector/Pin Assignment

3.6 INTERFACE SIGNAL FUNCTIONS

This section briefly describes the function of the major interface signals used to control the flow of information through the interface logic to the FMT controller and to the disk drive assembly.

a. Detailed Status (ST0/ST1)—Defines the File Unsafe Status (FUS) as follows.

ST0	ST1	
0	1	see FUS step f1
1	0	see FUS step f2

b. Device Type (DTP)—Always a One (1) denoting a 10 MB disk drive.

c. Diagnostic Clock (DCK)—The DCK signal is used to substitute the read data signal in selected operations and is required for VFO synchronization in modes other than the read data mode. The clock period is 250 ns with a 50% duty cycle (nominal value).

d. Direction Select (DSL)—The DSL signal specifies the direction in which the read/write head assembly moves as shown below.

DSL = 0—Head assembly moves towards cylinder zero.

DSL = 1—Head assembly moves away from cylinder zero.

e. Drive Select 1 and 2 (DS1 and DS2)—The DS1 and DS2 lines enable a disk drive in the selected DKU. A disk drive is enabled and its input/output lines are active when its drive select line is low.

f. File Unsafe (FUS)—A FUS condition of Zero, indicates that a write alarm condition occurred, or that the spindle speed is out of tolerance. The following specifies the actual conditions.

1. When FUS equals zero and;

WGT = 0—Indicates that the write current is not on, there is no write current inversion 3 μsec after WGT becomes active or when,

WGT = 1—Indicates that the write drive current is activated.

2. An FUS value of zero only, indicates the spindle spped exceed its rated tolerance of +1.5%.

The FUS signal is reset to a logic "1" when the Drive Select (DS) signal is set at a logic "1".

g. Head Select 0 through 2 (HS0 through HS2)—The head select logic selects one of eight heads as shown below.

HEAD ADDRESS	HEAD SELECT CODE 0	1	2
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

h. Index (IDX) Mark signal—A negative change (logic "1" to logic "0") of the IDX mark indicates the starting point on a track.

i. Ready (RDY) signal—With the RDY and SKC signals at a logic "0" signifies that the disk drive assembly is ready to perform a read, write, or seek operation.

The disk assembly is also ready for a disk operation after the recalibrate procedure, following a power on sequence, is completed.

j. Read Clock (RCK) signal—The RCK signal is sent to the FMT controller as RZ encoded (clocked) data (see Section 3.1, item 2).

k. Read Data (RDT) signal—The RDT signal is used with the VFO option to denote the transmission of RZ data to the FMT controller.

l. Read Gate (RGT) signal—The RGT signal enables data to be read. This signal must be zero in the data access to read data in VFO operation.

m. Seek Complete (SKC) signal—The SKC signal indicates the completion of a seek operation when zero. The SKC signal changes to zero 400 ns after the Step (STP) signal goes to zero.

n. Step (STP) signal—The STP signal moves the read/write head assembly in the direction specified in the Direction Select (DSL) signal. A STP signal change from logic zero to logic one moves the head one cylinder position. The DSL signal must be stabilized at least 40 ns before the STP signal changes. The step operation can be performed in the normal or buffered mode. The minimum STP signal interval and pulse width are 400 ns each.

o. Track 00 (T00) signal—The T00 signal, when at zero, indicates that the read/write head is at track zero (out-most data track).

p. Write Data (WDT) signal—The WDT signal implements a write operation to write data on the disk. The WDT signal must be zero when WGT is high (logic "1").

q. Write Gate (WGT) signal—When WGT signal is a low level (logic "0") data is written on the disk. If RDY or DKC signals are at a high level (logic "1") a write operation is inhibited.

3.7 DATA RECORD FORMAT

The following is a recommended example of a data record on the disk.

1	2	3	4	5	6	7	8	9	10	11	12	13
12 bytes	AM	CYL	HD	SEC	CRC	3 bytes	12 bytes	AM	256 bytes	ECC	3 bytes	14 bytes
00	A1FE					00	00	A1FE	Data		00	4E

1. 12 bytes —VFO SYNC area
2. (ALFE) —ID address mark (including missing bits)
3. —Cylinder address
4. —Head address
5. —Sector address
6. 2 byte CRC —$G(X) = X^{16} - 1$
7. 3 bytes, (00) —WRT switching gap
8. 12 bytes, (00) —VFO SYNC area
9. (A1F8) —Data address mark (including missing bits)
10. 256 data bytes —Data area
11. 4 bytes ECC —$G(X) = (X^{21} + 1)(X^{11} + X^2 + 1)$
12. 3 bytes, (00) —WRT switching gap
13. 14 bytes, (4E) —Sector separating gap

One sector is made up of items c through e, g through i, and l through q in Section 3.6 above.

- Index gap = 16 bytes, (4E)
- Rotational deviation gap = 179 bytes, (4E)—typical value.

3.8 PCB REMOVAL/REPLACEMENT AND ELECTRICAL ADJUSTMENTS

This section portrays, in picture form, the PCB removal/replacement techniques for the G9QKR (VFO) and G9QKQ/G9NXT (logic) PCBs. Included is the appropriate electrical adjustments for each PCB.

3.8.1 PCB Removal/Replacement

Figure 3-6 illustrates the recommended disassembly/assembly steps to remove or replace the VFO and/or logic PCB; either independently, or as a package. It assumes that ac power is disconnected, and that the disk drive assembly is removed from the DKU.

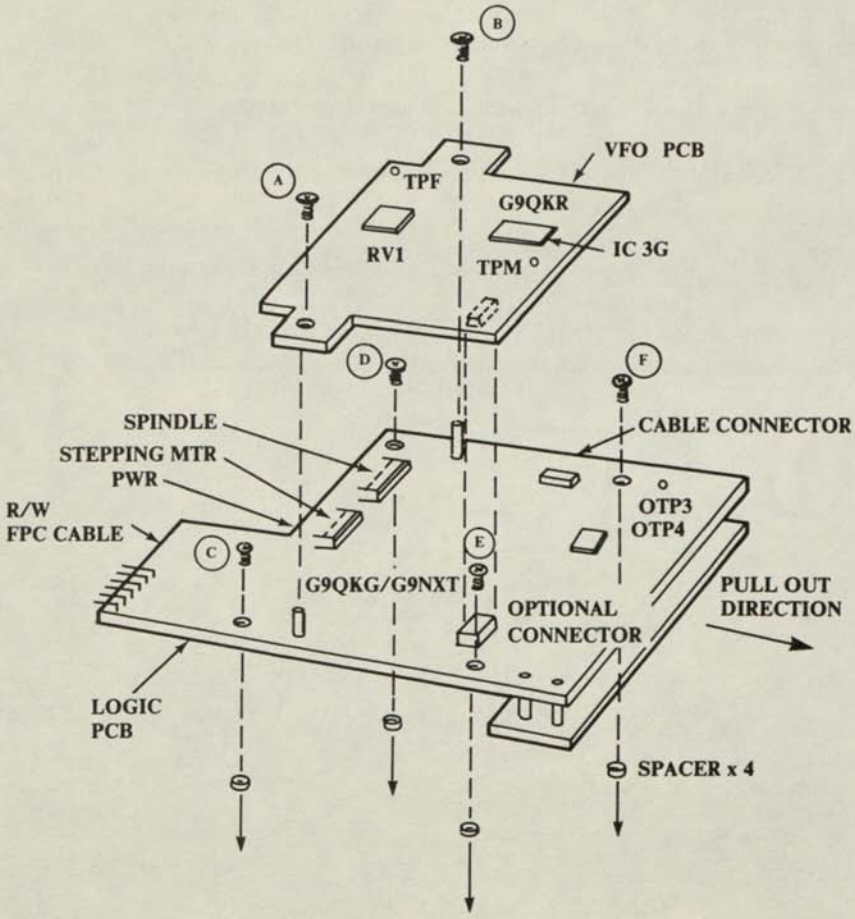


Figure 3-6 PCB Diassembly/Assembly (Disk Drive)

3.8.2 Electrical Adjustments

This section is in two parts; 1. G9QKQ/G9NXT logic PCB balance (speed) adjustment, and 2. Optional VFO PCB adjustment. Part 1 sets the spindle motor speed and part 2 balances the VFO control signal with the logic PCB.

NOTE

When the VFO and logic PCB are received and installed as a matched set, the VFO adjustments are not required. Only the logic PCB adjustment is required.

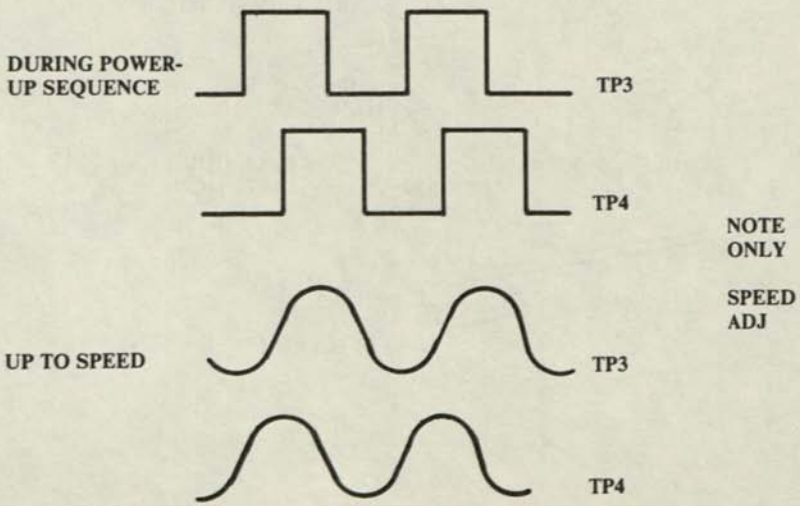
These adjustments assume that the disk assembly is installed in the DKU.

A dual channel oscilloscope, with a 10 MHz band-width, is recommended.

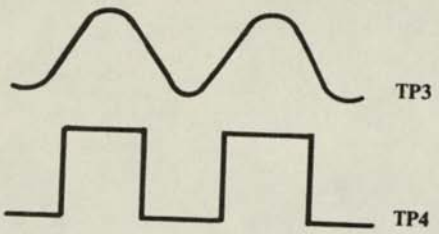
1. G9QKQ/G9NXT PCB Balance (speed) adjustment (see Figure 3-6).
   a. Attach oscilloscope as follows.

      Channel 1 to TP3
      Channel 2 to TP4

   b. Turn on the ac power and verify the phase differential shown below as the disk drive assembly comes up to, and attains its designed speed.



c. With the disk drive at a constant speed adjust RV1 until both waveforms are in phase as shown below. This adjustment sets the spindle motor at its designed speed.



2. G9QKR VFO PCB Adjustment (see Figure 3-6).

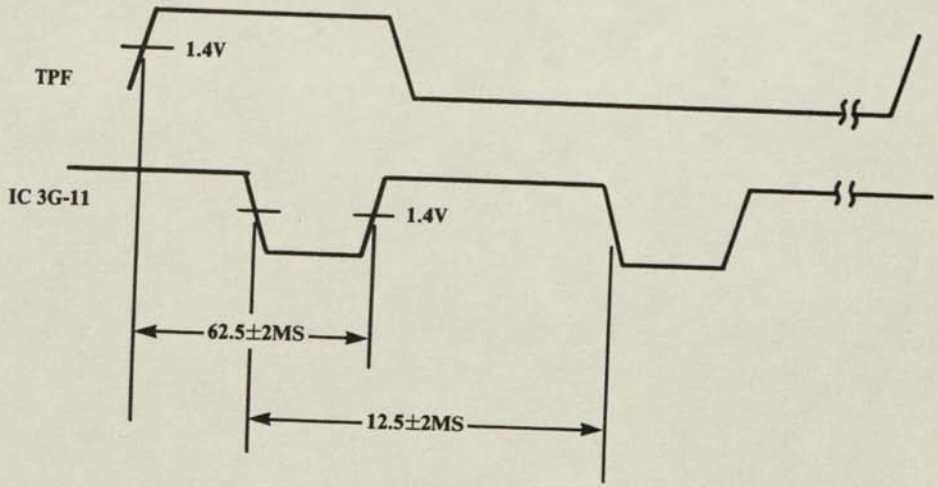
NOTE

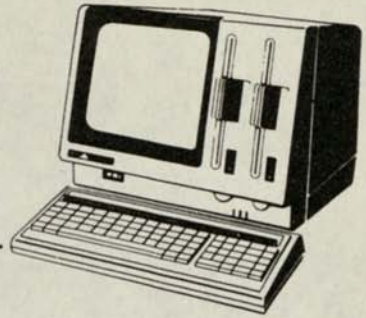
Make sure the disk drive is not being addressed.

a. Attach oscilloscope as follows.

Channel 1 to TPF
Channel 2 to IC 3G pin 11 (or TPH).

b. Adjust RV1 to produce the following waveforms.





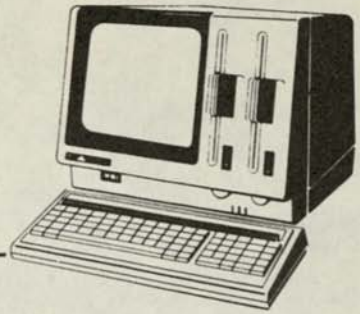
Appendix A

List of Abbreviations

ADR	Address
ADRH	Error Address High Byte
ADRL	Error Address Low Byte
A0	Address Bit 0
CB	Controller Busy
CE	Command End
CEH	Command End High Bit
CEL	Command End Low Bit
CH	Channel
CLCE	Clear Command End
CLDB	Clear Data Buffer
CMD	Command
CRC	Cyclic Redundancy Character
CS	Chip Select
CYL	Cylinder
DACK	DMA Acknowledge
DB	Data Bus
DCK	Diagnostic Clock
DER	Data Error
DIAG	Diagnostic
DMAC	Direct Memory Access Cont.
DMIN	DMA Interrupt
DPAT	Data Pattern
DRO	Data Request
DRQ	DMA Request
DS1 to DS4	Drive Select 1 to 4
DSKC	Disk Controller
DSL	Direction Select
DT or DTP	Device Type
DTLH	Data Length (High Byte)
DTLL	Data Length (Low Byte)

ECC	Error Correct Logic
ENC	End of Cylinder
EOP	End of Process
EPAT 1 through 3	Error Pattern 1 through 3
EQC	Equipment Check
ESN	End Sector Number
EST	End Status/Error Status Byte
ETN	End Track Number
FUS	File Unsafe
FM	Frequency Modulation
FMT	Format
GPL 1 through 3	Gap Length 1 through 3
HDC	Hard Disk Controller
HDER	Hard Disk (I/O Timing) Error
HDEX	Hard Disk Executing
HSL	Head Select
HSRQ	Status Request
IDX	Index Mark
IER	ID Error
I/O	Input/Output
IOER	I/O Error denoting simultaneous HDER and MAER Mask
IST	Interrupt Status
LCNH	Logical Cylinder Number (High Byte)
LCNL	Logical Cylinder Number (Low Byte)
LHN	Logical Head Number
LSN	Logical Sector Number
MA	Missing Address Mark
MAER	DMA Error
MDA	Missing A.M. in data field
MDM	Missing Data
MFM	Modified Frequency Modulation
MTFB	Mean Time Between Failures
NCN	Present Cylinder Number (NCN should read PCN).
ND	No Data
NR (NRY)	Not Ready
OCN	Object Cylinder Number
OVR	Overrun
PCB	Printed Circuit Board
PCNH	Physical Cylinder Number High
PCNL	Physical Cylinder Number Low
PHN	Physical Head Number

PLA	Programmable Logic Array
PLO	Phase Lock Oscillator
POH	Power on Hours
RC	Ready Change
RCK	Read Clock
RDT	Read Data
RDY	Ready
RGT	Read Gate
RSTR	Reset Status Register
SCMD	Seek command
SCNT	Sector Count(er)
SEN	Seek End
SER	Seek Error
SEQ	Sequence
SK or SKC	Seek Command
SEQ	Sense Interrupt Status Request
STN	Status Number
STP	Step
STR	Status Register
ST0/ST1	Status 0/Status 1
TC	Terminal Count
T0 or T00	Track 00
UA	Unit Address
UST	Unit Status
VFO	Variable Frequency Osc.
WDT	Write Data
WF	Write Fault
WGT	Write Gate



Appendix B

FMT Interface Signal Definitions

A0	Register select input. When high, the command/status register is selected. When low, the data buffer is selected.
CS	Chip Select. When low, enables reading from or writing into the register selected by A0.
DB	Data Bus. Data bus bits 0 through 7
DRQ	DMA Request. Normally low, set high to request a transfer of data between the disk controller and memory.
IOR	Write Strobe. When low, data is written into the selected register.
IOW	Read Strobe. When low, contents of selected register are read.
HINT	Interrupt request to the system, set high to make request.
RESET	Reset input. When high, sets the idle state in the DKU. The DKU remains in this state until a command is received.
TC	Terminal Count. Terminal counter input during DMA.

Note: See Section 2.1.2.3 and Figure 2-4 for additional information.

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USER'S COMMENTS FORM

Document: APC Hard Disk Subsystem Reference Guide

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