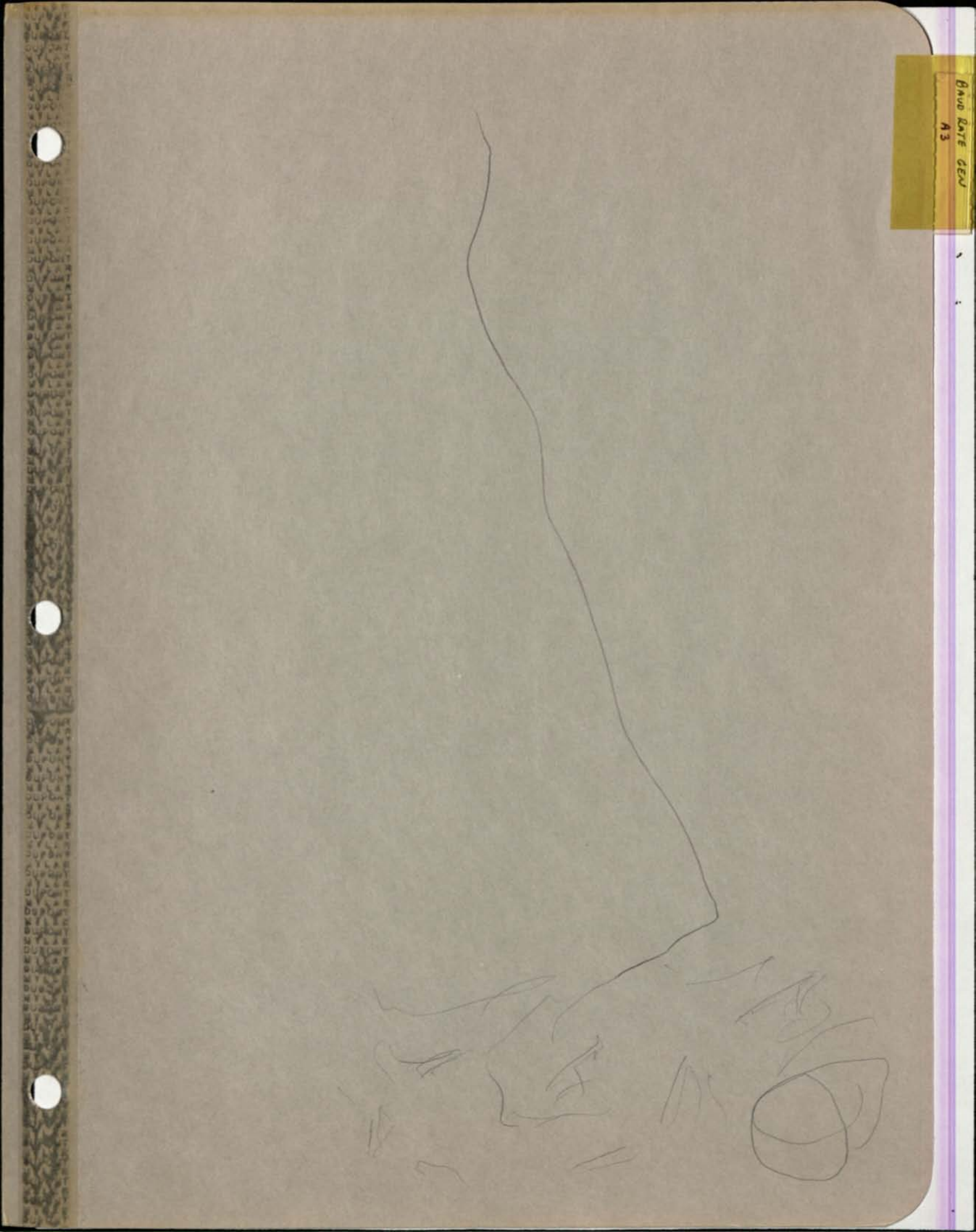

BAUD RATE GEN
A3

A 6502 Op Code Table

Lemuel A Fugitt
11316 Linares St
San Diego CA 92129

Table 1: An explanation of the abbreviations used in the 6502 reference chart.

abs:	absolute.
abx:	indexed absolute using x register.
acc:	accumulator.
aby:	indexed absolute using y register.
i,x:	indexed indirect using x register.
i,y:	indexed indirect using y register.
imm:	immediate.
imp:	implied.
ind:	absolute indirect.
rel:	relative.
zer:	zero page.
zpx:	indexed zero page using x register.
zpy:	indexed zero page using y register.
*:	not implemented.

Here's a nice compact reference chart to help you debug those hexadecimal dumps from your 6502 microprocessor. To use the table, find the most significant digit along the top of the chart and follow the column down until you reach the value of the least significant bit of the hexadecimal code on the horizontal row. You now have not only the mnemonic but also the addressing mode being used. Table 1 is an explanation of the abbreviations used in the chart. ■

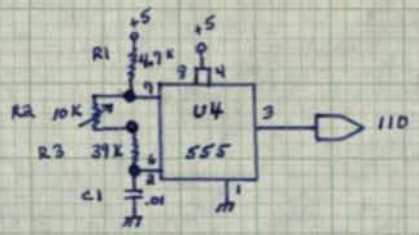
LEAST SIGNIFICANT 4 BITS

MOST SIGNIFICANT 4 BITS

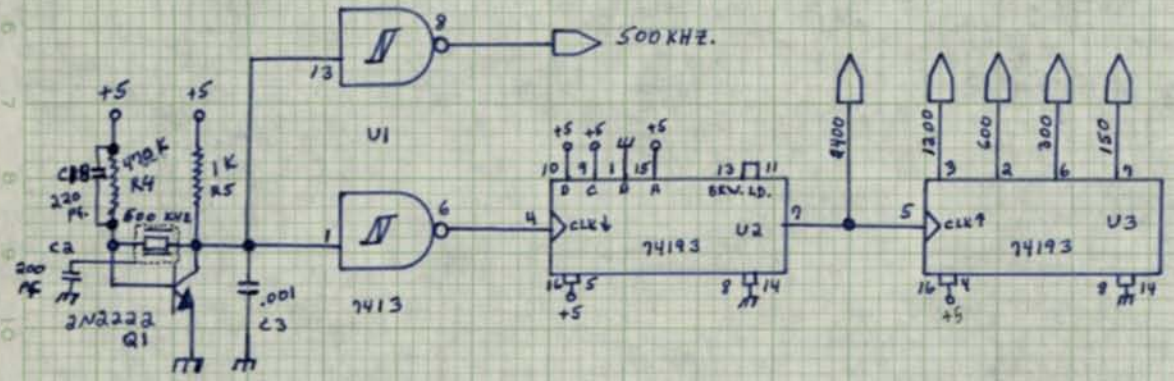
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK imp	BPL rel	JSR abs	BMI rel	RTI imp	BVC rel	RTS imp	BVS rel	*	BCC rel	LDY imm	BCS rel	CPY imm	BNE rel	CPX imm	BEQ rel
1	ORA i,x	ORA i,y	AND i,x	AND i,y	EOR i,x	EOR i,y	ADC i,x	ADC i,y	STA i,x	STA i,y	LDA i,x	LDA i,y	CMP i,x	CMP i,y	SBC i,x	SBC i,y
2	*	*	*	*	*	*	*	*	*	*	LDX imm	*	*	*	*	*
3	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
4	*	*	BIT zer	*	*	*	*	*	STY zer	STY zpx	LDY zer	LDY zpx	CPY zer	*	CPX zer	*
5	ORA zer	ORA zpx	AND zer	AND zpx	EOR zer	EOR zpx	ADC zer	ADC zpx	STA zer	STA zpx	LDA zer	LDA zpx	CMP zer	CMP zpx	SBC zer	SBC zpx
6	ASL zer	ASL zpx	ROL zer	ROL zpx	LSR zer	LSR zpx	*	*	STX zer	STX zpy	LDX zer	LDX zpy	DEC zer	DEC zpx	INC zer	INC zpx
7	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
8	PHP imp	CLC imp	PLP imp	SEC imp	PHA imp	CLI imp	PLA imp	SEI imp	DEY imp	TYA imp	TAY imp	CLV imp	INY imp	CLD imp	INX imp	SED imp
9	ORA imm	ORA aby	AND imm	AND aby	EOR imm	EOR aby	ADC imm	ADC aby	*	STA aby	LDA imm	LDA aby	CMP imm	CMP aby	SBC imm	SBC aby
A	ASL acc	*	ROL acc	*	LSR acc	*	*	*	TXA imp	TXS imp	TAX imp	TSX imp	DEX imp	*	NOP imp	*
B	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
C	*	*	BIT abs	*	JMP abs	*	JMP ind	*	STY abs	*	LDY abs	LDY abx	CPY abs	*	CPX abs	*
D	ORA abs	ORA abx	AND abs	AND abx	EOR abs	EOR abx	ADC abs	ADC abx	STA abs	STA abx	LDA abs	LDA abx	CMP abs	CMP abx	SBC abs	SBC abx
E	ASL abs	ASL abx	ROL abs	ROL abx	LSR abs	LSR abx	*	*	STX abs	*	LDX abs	LDX aby	DEC abs	DEC abx	INC abs	INC abx
F	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

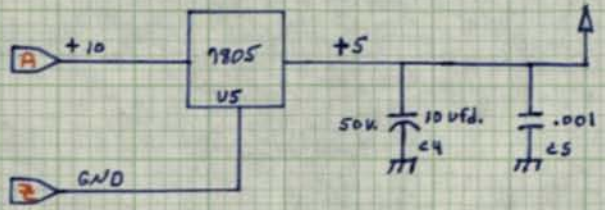
145 ma. 10 v. line

Ref	TYPE	Vcc	GND
U1	7413	14	7
U2,3	74193	16	8
U4	555	8	1



wh/yellow/BLK → Pin 3 - U4
Remove U4

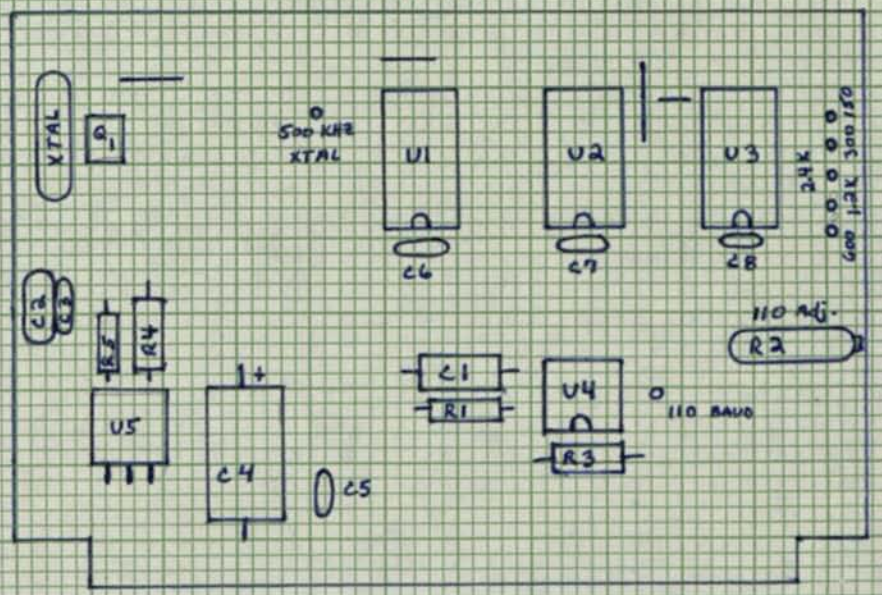




Baud Rate Generator - A3

.001 ByPass Cap at Vcc Pin of U1, U2, U3

C6, C7, C8



BAUD RATE GEN. - A3

Parts List

C1	.01 ufd. 100 v.	Poly.
C2	200 Pf.	mica
C3,5,6,7	.001	50 v. Ceram.
C4	10 ufd.	50v. Elect.
C8	220 Pf.	500v. mica
R1	4.7 K	½ w.
R2	10 K	TRIMPOT
R3	39 K	½ w.
R4	470 K	½ w.
R5	1 K	¼ w.
U1	7413	
U2,U3	74193	
U4	555	
U5	7805	
Q1	2N2222	
XTAL	500 KHz.	

VIDEO DISPLAY
ASSEMBLY-A1

ELECTRONIC SYSTEMS

(415) 573-7788

TVT

* 32 Char/Line
* Parallel Input
* 1K on board memory
* Output for computer controlled curser

P. O. BOX 212, BURLINGAME, CA

TVT

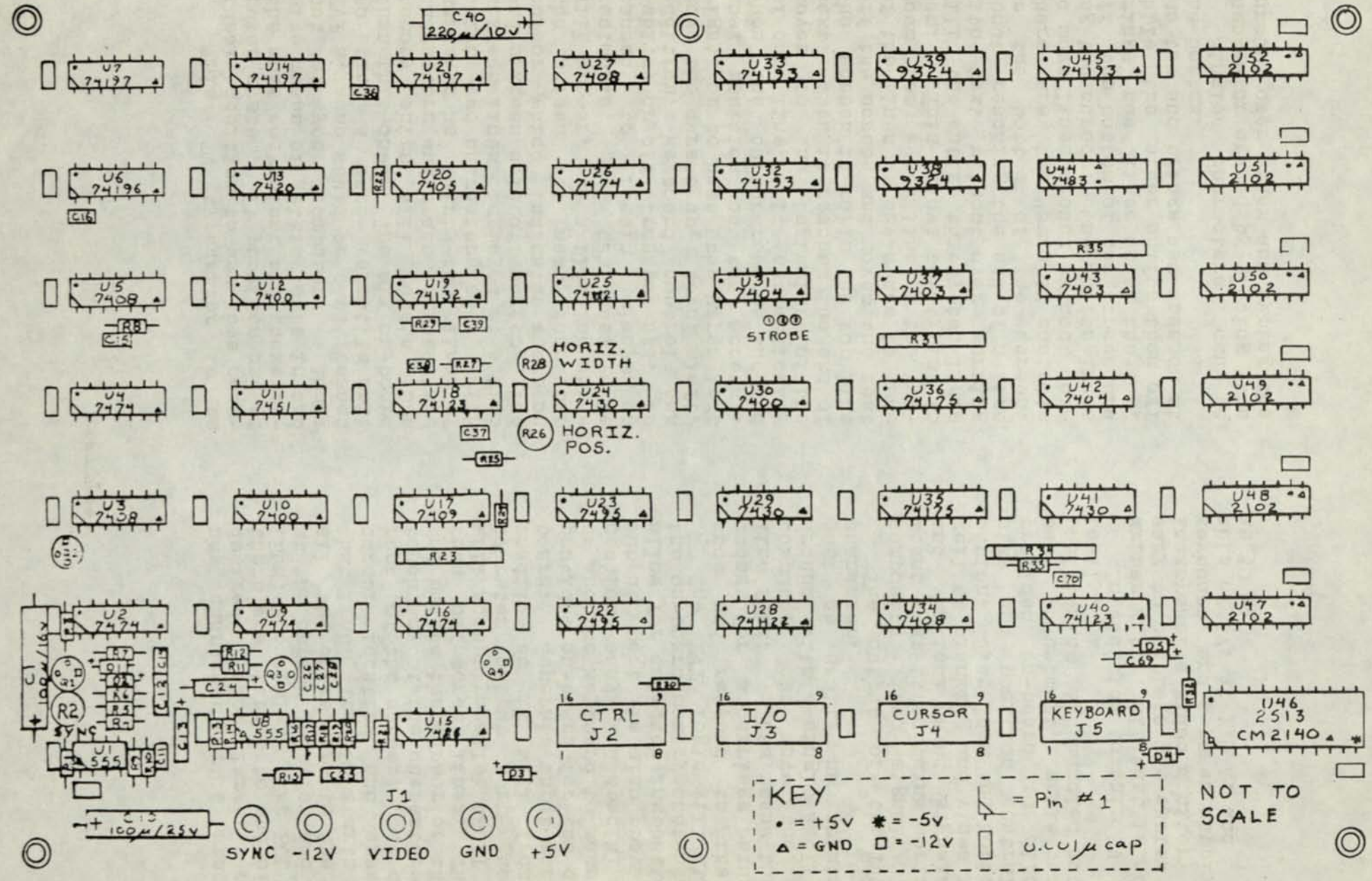
This TV typewriter is an ideal addition to any home computer system. It provides one of the most convenient and inexspensive means of getting data in and out of your computer. Among TVT's, one would be hard pressed to find a more versatile unit than this one. The six on-board memory chips will retain 1024 characters and spaces. These are arranged as thirty-two lines of thirty-two characters each, with sixteen lines displayed at a time and sixteen held off screen. The cursor which indicates where on the screen the next character will appear, as a flashing white rectangle; but can easily be caused to remain always on (white) or off (transparent). In addition, keyboard controls can move the cursor up, down, left, right, or to home (the upper left most position on the screen). When the cursor reaches the end of one line, it automatically moves to the beginning of the next. When it reaches the end of the screen it rolls the top line off the screen and moves the rest of the lines up one space to make room for a new line at the bottom. This allows the typist to fill the entire thirty-two lines with text without ever worring about reaching the end of a line or the bottom of the screen. There are two "scroll" controls to move lines around without moving the cursor. One shifts lines off the bottom of the screen and brings new lines on at the top, while the other shifts them off the top and brings new ones on at the bottom.

Single characters can be changed or erased by placing the cursor over them and typing the new character or a space as desired. For larger changes there are "erase to end of line" (EOS) controls. The EOL starts at the cursor location and erases all the characters to the end of that line. The EOS starts at the cursor location and erases the rest of the screen, but doesn't touch any of the characters above and before the cursor or the sixteen off-screen lines. The TVT will accept parallel ASCII from a computer output port just as readily as it will from a key board. Seperate input ports are provided on-board for the computer and the keyboard to make connection easy. A special memory output port is also provided to allow for computer inspection of the on-board memory contents.

The TVT logic will also decode and respond to the ASCII codes for a carriage return and line feed. This means that the computer can move the cursor around with a single ASCII word, just as easily as printing a character.

The output of the TVT is a composite video signal. This means that it contains horizontal and vertical sync signals, as well as blanking and video information. Sync lock and horizontal size and position controls are provided on-board to allow for easy adjustment, while vertical positioning is handled automatically.

In addition to this TV typewriter kit, all that is nessessary to complete the system is an inexspensive video monitor, a keyboard, and a power supply capable of 5V. at 1,5 A. and -12V. at 30 mA.


C40 220µ/10V
U7 74197
U14 74197
U21 74197
U27 7408
U33 74193
U39 9324
U45 74193
U52 2102
C38
U6 74196
U13 7420
U20 7405
U26 7474
U32 74193
U38 9324
U44 7483
U51 2102
C16
R22
R35
U5 7408
U12 7400
U19 74132
U25 74121
U31 7404
U37 7403
U43 7403
U50 2102
R8
C15
R29
C39
STROBE
R31
HORIZ. WIDTH
R28
C36
R27
U4 7474
U11 7451
U18 74123
U24 7430
U30 7400
U36 74175
U42 7404
U49 2102
C37
R26
HORIZ. POS.
R25
U3 7408
U10 7400
U17 7409
U23 7495
U29 7430
U35 74175
U41 7430
U48 2102
R24
R23
R34
R33
C70
U2 7474
U9 7474
U16 7474
U22 7495
U28 74123
U34 7408
U40 74123
U47 2102
D5
C69
C1 100µ/16V
R7
Q1
R6
R5
R4
R2
SYNC
U1 555
C5
C4
C11
C13
C14
R12
R11
C24
Q3
C26
C27
C28
U8 555
R13
R14
R15
R16
R17
R18
C22
C23
R21
U15 74123
R19
C25
D3
R30
CTRL J2
I/O J3
CURSOR J4
KEYBOARD J5
D4
R32
1146 2513 CM2140
C12 100µ/25V
J1
SYNC
-12V
VIDEO
GND
+5V
KEY
• = +5V
✱ = -5V
△ = GND
□ = -12V
= Pin #1
0.001µ cap
NOT TO SCALE

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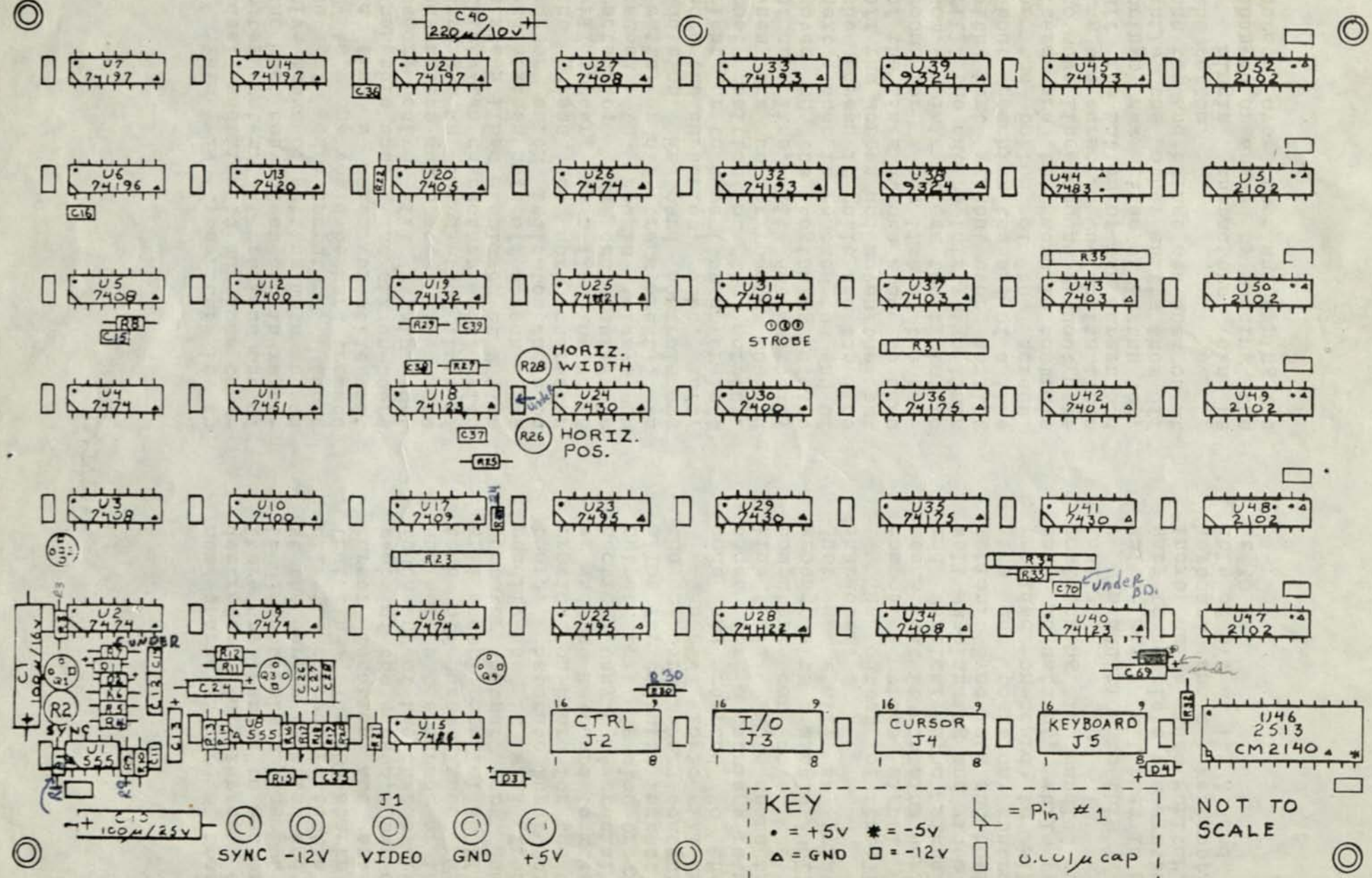
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U42 7404
U49 2102
U3 7408
U10 7400
U17 7409
R23
U23 7495
U29 7430
U35 74175
R34
R33
C70
under BD.
U41 7430
U48 2102
U2 7474
U9 7474
U16 7474
U22 7495
U28 74H22
U34 7408
U40 74123
U47 2102
C69
under
C1 100μ/16V
under
C24
U8 555
U1 555
SYNC
U15 7486
R30
CTRL J2
I/O J3
CURSOR J4
KEYBOARD J5
D4
1146 2513 CM2140
C15 100μ/25V
J1
SYNC
-12V
VIDEO
GND
+5V
KEY
• = +5V
✱ = -5V
△ = GND
□ = -12V
= Pin # 1
0.001μ cap
NOT TO SCALE

TV TYPEWRITER

Theory of Operation

INPUT:

The TV Typewriter will accept inputs coded in ASCII (American Standard Code for Information Interchange) from either a keyboard or directly from a computer output port. The seven ASCII bits coming directly from the keyboard are passed directly into a latch consisting of U35 and U36; except for bit six, which is inverted first, for reasons which will be explained later. A pulse on the input strobe line clocks the input word into the latch and passes the six least significant bits on to the 1K by 6 bit memory made up of U47 through U52. Bit 6 is taken from the inverted output of the latch to restore it to its original logic state. The six least significant bits from the computer input connector are combined with the six least significant bits from the latch at the memory inputs. All seven bits from both the keyboard latch and the computer input connector are presented to a control instruction recognizer for decoding of carriage return and line feed instructions.

CHARACTER GENERATION:

As each memory location is addressed, its contents appear at the memory output. This is fed both to a memory output connector, and to the most significant six of the nine address lines on the character generator, U46. These six bits select a unique character out of the sixty-four character patterns stored in the generator. Each character is made up of seven rows of five bits each, with an eighth row which is always blank. The other three address lines select which of the eight five bit rows is to be placed on the character generator's five output lines. These three address lines are driven by the three least significant bits of the dot counter, U6, which counts from zero to nine. The dot counter is incremented once for each horizontal scan of the television raster by the horizontal sync pulse. On count zero the blank line is output. For counts one through seven, the bits making up the character pattern are output. With counts eight and nine the three address lines are held low by control logic which causes the blank line to be output two more times. This results in three blank scan lines separating each set of seven scan lines which make up a row of characters. The five output lines of the character generator are clocked into a shift register, U22 and U23, by the system timing after they have had time to stabilize. They are in turn clocked out of the register, one at a time, into the video mixer. The rate at which they are clocked out determines the width of the displayed character and hence the entire display. This rate is controlled by trimmer pot R28 and multivibrator U18.

CURSOR OPERATION:

The cursor uses the count and compare technique of memory update wherein a semi-static cursor address; held by the cursor character and line counters, U26, U32, and U33; is compared to the ever-changing addresses of the display character and line counters, U7, U14, and U21. When the comparator, U38 and U39, senses a match between the instantaneous memory address and the cursor location, and the strobe line is pulsed, the memory write line is momentarily brought low and the new character waiting in the keyboard latch or on the bus input is loaded into the memory. If a character was already present in that location, i.e. the cursor was superimposed on a character, the new character will replace the old one. The cursor must always remain within the visible page, unlike individual characters, which can go off of the screen. To accomplish this, the output of the display line counter, U7, is added to the output of the roll counter, U45, for memory addressing. The value in the roll counter represents the number of lines between the cursor and the end of the page. When the cursor would otherwise go off the screen, the roll counter

is either incremented or decremented as necessary to keep it on screen. This has the effect of rolling one line of text off one end of the screen while replacing it with another from the other end. The keyboard scroll controls, or "roll up" and "roll down" increment and decrement the roll counter directly to accomplish their function, while "cursor up" and "cursor down" increment and decrement the cursor line counter, U32. Similarly, "cursor left" and "cursor right" cause the cursor character counter, U26 and U33, to count up or down. Pulling low on the "home" control line clears both the cursor character and line counters.

ERASING:

The cursor symbol is an all white square which blinks off and on with the oscillations of U8. The flashing can be made to stop by pulling the "solid cursor" pin low, or to disappear entirely (become transparent), by pulling the "cursor off" pin low.

The keyboard latch is cleared after each entry. This clear causes all of the outputs to go low except for bit 6. As was mentioned earlier, bit 6 is taken from the inverted output. This means that the seven bit ASCII word normally at the latch output is 0100000, which is the code for a blank space. When the "EOL" pin is pulled low the memory write line is enabled and the latch contents (0100000) are clocked into consecutive memory locations until the end of the line is reached. In this way the portion of the line after the cursor position is rewritten with blank spaces, effectively erasing the line. "EOS" works in exactly the same way except that it doesn't stop until the cursor reaches the end of the page.

SYNC GENERATION AND VIDEO OUTPUT:

The horizontal oscillator is built around U1 and can be synchronized with the 60 Hz. power line by adjusting trimmer pot R2. Horizontal position is determined by R26 which sets the delay time between the horizontal sync pulse and the start of video from the sync generator. Vertical sync is derived by dividing down the output of the horizontal oscillator through the display line counter, U7 and U4. The horizontal pulse itself is shaped by a Schmitt trigger and is combined with the vertical sync pulse in U17. Composite sync from U17 is then joined with the video pulses from the shift register in video mixer, 04, resulting in a full composite video output.

TV TYPEWRITER

Assembly and Trouble Shooting

CAUTION: The six memory I.C.'s, U47 through U52; the character generator, U46; and the two field effect transistors, Q1 and Q3, are all static sensitive devices. To avoid static damage, they should be left in the conductive foil until they are inserted in the board. When out of the foil, avoid finger contact with the leads.

ASSEMBLY:

1.) Examine the parts package carefully to see that all parts are present. Since the parts are inserted directly into the layout diagram, it should be immediately obvious from the diagram if any are missing. The printed circuit board should be positioned so that it matches the layout of the parts package for easiest assembly.

2.) Begin by inserting the fixed value resistors. The direction of insertion is not important with resistors. Solder the resistor leads, then clip off the excess wire next to the joint.

3.) Insert the four resistor networks R23, R31, R34, and R35; being careful to insert pin 1 in the hole with the square pad. Pin 1 is usually indicated by an indentation or a mark on the package. Solder the leads and clip off any excess wire.

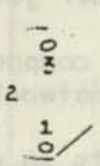
4.) When inserting capacitors, careful attention must be paid to the polarity of C1, C10, C13, C24, C40, and C69. These six caps should be inserted with the positive terminal in the hole with the square pad. Their proper orientation is also indicated on the layout diagram. The rest of the capacitors can be inserted in either direction. As always, clip off any excess wire after soldering.

5.) Insert diodes D1 through D5 with their negative terminal in the hole with the square pad. The negative end is the end with a stripe around it. When soldering diodes, use as little heat as possible and allow the diode to cool after soldering the first lead before soldering the second.

6.) Compare transistors Q1 through Q4 to the basing diagram below and note the location of pin 1. Insert the transistors in their respective locations with pin 1 going in the hole with the square pad. Solder the leads one at a time, allowing the transistor to cool between one lead and the next.

Q1 and Q3
Pin 4 not
used.

Q2 and Q4



Bottom View

7.) Insert the variable resistors R2, R26, and R28 next. In each case there are three holes, two of which are connected together. One of the end leads and the center lead should go in these holes, the other end lead should go in the third hole. Solder the leads and clip off the excess wire.

8.) Sockets have been supplied for I.C.'s U46 through U52. Solder the sockets into these locations, being careful to put pin 1 in the hole with the square pad. Do not insert the I.C.'s in the sockets yet.

9.) Insert the rest of the I.C.'s, U1 through U45, in their respective locations.

being very careful to insert pin 1 in the hole with the square pad. Pin 1 is usually identifiable by a dot or indentation next to the pin or on its end of the package. When soldering the I.C.'s, be very careful not to overheat them, and also not to bridge solder between adjacent leads. Allow the package to cool between the soldering of one lead and the next.

10.) Next to U31 are three holes labeled 1, 2, and 3 on the layout diagram. If the strobe output from your keyboard is a positive pulse, connect pin 1 to pin 2; if it is a negative pulse, connect pin 3 to pin 2 instead.

11.) Insert U46 through U52 in their sockets, being careful to get pin 1 in the correct place.

12.) Connect the computer and the keyboard to J2 through J5 using the guide on the schematic.

13.) Before going any further, look the board over carefully. Make sure all of the I.C.'s are in the right places and oriented properly. Make sure the other polarized components like diodes, transistors, and electrolytic and tantalum capacitors are not reversed. Check the back of the board for cold solder joints and solder bridges.

14.) Connect the power supply to the Gnd., +5 V., and -12 V. inputs. Connect the video monitor to J1 (OUT) and Gnd. A 60 Hz. sine wave of up to 12.6 Vrms. can be applied to the sync input, but is usually not required since the circuit is sensitive enough to sync with 60 Hz. radiated from house wiring.

15.) The +5 V. input should draw about 1.5 A., while the -12 V. should only be in the 15 mA. range. If the currents are much greater than this, shut off the circuit immediately and go back to step 13.

16.) Adjust R2 for a stable display on the video monitor. The screen will be filled with random characters from memory power-up. There should also be a flashing rectangle, which is the cursor. Adjust R26 and R28 for the size and position of the display.

TROUBLE SHOOTING:

Listed below are some of the things to check if there are any problems.

1.) Cold solder joints or solder bridges.

2.) Reversed components like diodes, transistors, polarized capacitors, I.C.'s, or resistor networks.

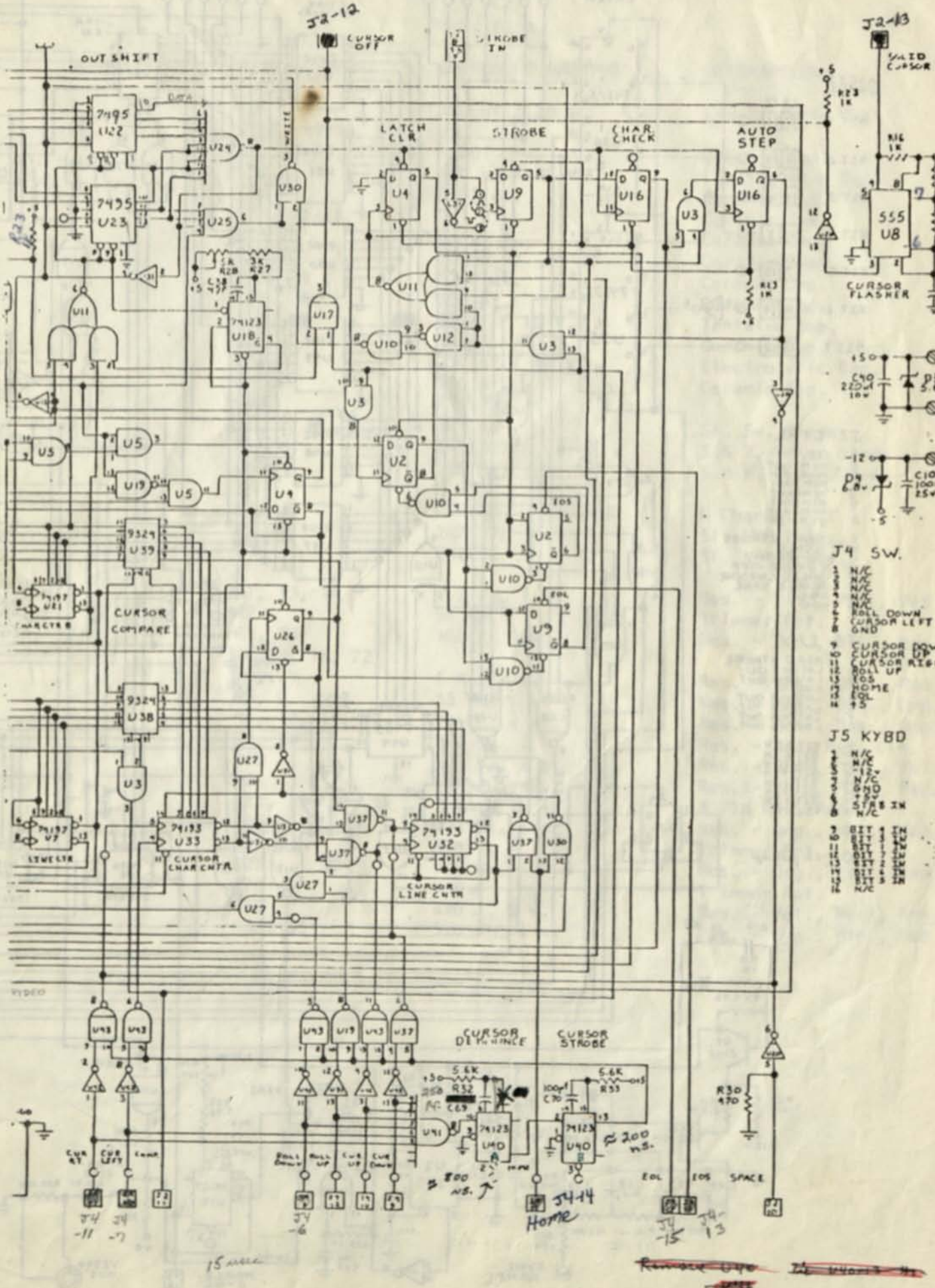
3.) Components in wrong places. Check color codes and device markings with layout and parts list.

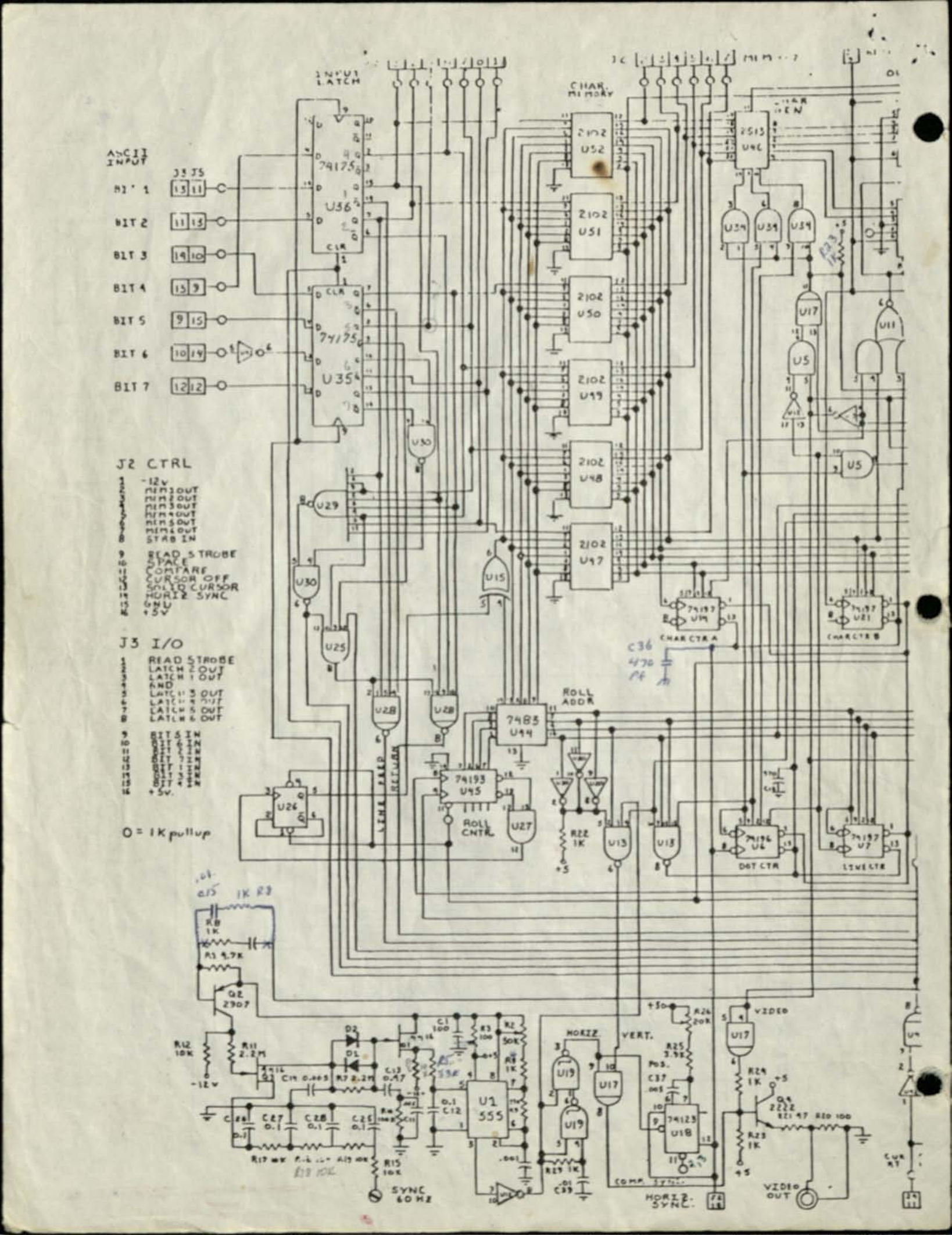
4.) Components damaged by heat while soldering.

5.) Variable resistors R2, R26, and R28 adjusted improperly.

6.) Input strobe not connected, see instruction #10.

7.) Keyboard or video monitor malfunction.


J2-12
CURSOR OFF
STROBE IN
J2-13
VALID CURSOR
OUT SHIFT
LATCH CLR
STROBE
CHAR CHECK
AUTO STEP
74195 U22
7495 U23
555 U8
CURSOR FLASHER
9324 U39
9324 U38
CURSOR COMPARE
74193 U33
CURSOR CHAR CNTR
74193 U32
CURSOR LINE CNTR
CURSOR DELAY
CURSOR STROBE
74123 U40
74123 U41
≈ 800 ms.
≈ 200 ms.
J4 SW.
N/C
N/C
N/C
N/C
N/C
ROLL DOWN
CURSOR LEFT
GND
CURSOR DOWN
CURSOR UP
CURSOR RIGHT
ROLL UP
EOS
HOME
EOL
+5
J5 KYBD
N/C
N/C
-12v
N/C
GND
+5v
STB IN
N/C
J4-14 Home
J4-15 EOL
J4-13 EOS
SPACE


INPUT LATCH
CHAR. MEMORY
ASCII INPUT
J3 J5
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
74175
U36
U35
2102 U52
2102 U51
2102 U50
2102 U49
2102 U48
2102 U47
2513 U46
J2 CTRL
-12v
MEM3 OUT
MEM2 OUT
MEM1 OUT
MEM4 OUT
MEM5 OUT
MEM6 OUT
STRB IN
READ STROBE
SPACE
COMPARE
CURSOR OFF
SOLID CURSOR
HORIZ SYNC
GND
+5V
J3 I/O
READ STROBE
LATCH 2 OUT
LATCH 1 OUT
AND
LATCH 3 OUT
LATCH 4 OUT
LATCH 5 OUT
LATCH 6 OUT
BIT 5 IN
BIT 6 IN
BIT 7 IN
BIT 1 IN
BIT 2 IN
BIT 3 IN
BIT 4 IN
+5V.
0 = 1K pullup
74193 U95
ROLL CNTRL
7485 U44
ROLL ADDR
CHAR CTR A
CHAR CTR B
DOT CTR
LINE CTR
U1 555
SYNC 60 HZ
HORIZ.
VERT.
HORIZ. SYNC
VIDEO
VIDEO OUT
Q1 2907
Q2 2907
Q3 2222

TV TYPEWRITER

Parts List

QUANTITY	PART NUMBER	COMPONENT MARKING	DESCRIPTION
1	C1	100 uf./ 16 V.	Electrolytic Cap.
64	C2-9, 17-23, 29-35, 41-68, 71-84	0.001 uf.	Ceramic Cap.
1	C10	100 uf./ 25 V.	Electrolytic Cap.
1	C11	0.02 uf.	Ceramic Cap.
5	C12, 25-28	0.1 uf.	Ceramic Cap.
1	C13	0.47 uf.	Ceramic Cap.
2	C14, 37	0.005 uf.	Ceramic Cap.
2	C15, 39	0.01 uf.	Ceramic Cap.
2	C16, 36	500 pf.	Ceramic Cap.
2	C24, [redacted]	[redacted]22[redacted] uf./ 10 V.	Tantalum Cap.
1	C38	47 pf.	Ceramic Cap.
1	C40	220 uf./ 10 V.	Electrolytic Cap.
1	C70	100 pf.	Ceramic Cap.
	C69	250 pf.	
3	D1, 2, [redacted] DO REMOVED	1N4148	Si. Sw. Diode
1	D3	1N5232B	5.6 V. Zener Diode
1	D4	1N5235B	6.8 V. Zener Diode
2	Q1, 3	2N4416 MPF 102	N Channel FET
1	Q2	2N2907	Si. PNP Trans.
1	Q4	2N2222	Si. NPN Trans.
3	R1, 13, 14	4.7 Kn, ¼ w.	Res. - Yel., Pur., Red
1	R2	50 Kn	Trimmer Pot.
2	R3, 20	100 n, ¼ w.	Res. - Brn., Blk., Brn.
6	R4, 8, 16, 22, 24, 29	1 Kn, ¼ w.	Res. - Brn., Blk., Red
2	R5, 9	33 Kn, ¼ w.	Res. - Org., Org., Org.
6	R6, 12, 15, 17-19	10 Kn, ¼ w.	Res. - Brn., Blk., Org.
2	R7, 11	2.2 Mn, ¼ w.	Res. - Red, Red, Grn.
1	R10	100 Kn, ¼ w.	Res. - Brn., Blk., Yel.
1	R21	47 n, ¼ w.	Res. - Yel., Pur., Blk.,
4	R23, 31, 34, 35	1 Knx 7	8 Pin Res. Pack
1	R25	3.9 Kn, ¼ w.	Res. - Org., Wht., Red
1	R26	10 Kn	Trimmer Pot.
1	R27	3.0 Kn, ¼ w.	Res. - Org., Blk., Red
1	R28	5 Kn	Trimmer Pot.
1	R30	470 n, ¼ w.	Res. - Yel., Pur., Brn.
2	R32, 33	5.6 Kn, ¼ w.	Res. - Grn., Blu., Red

QUANTITY	PART NUMBER	COMPONENT MARKING	DESCRIPTION
2	U1, 8	555	Timer IC
5	U2, 4, 9, 16, 26	7474	Dual D Flip Flop IC
4	U3, 5, 27, 34	7408	Quad 2-Input AND Gate IC
1	U6	74196	40 MHz. Presettable Decade Counter / Latch IC
3	U7, 14, 21	74197	40 MHz. Presettable Binary Counter / Latch IC
3	U10, 12, 30	7400	Quad 2-Input NAND Gate IC
1	U11	7451	Dual 2-Wide 2-Input AND-OR-INVERT Gate IC
1	U13	7420	Dual 4-Input NAND Gate IC
1	U15	7486	Quad EXCLUSIVE-OR Gate IC
1	U17	7409	Quad 2-Input AND Gate (Open Collector) IC
2	U18, 40	74123	TTL / Monostable Multivibrator IC
1	U19	74132	Quad 2-Input NAND Schmitt Trigger IC
1	U20	7405	Hex Inverter (Open Collector) IC
2	U22, 23	7495	4-Bit Right-Shift / Left-Shift Register IC
3	U24, 29, 41	7430	8-Input NAND Gate IC
1	U25	7421	Dual 4-Input AND Gate IC
1	U28	74H22	Dual 4-Input NAND Gate (Open Collector) IC
2	U31, 42	7404	Hex Inverter IC
3	U32, 33, 45	74193	Synchronous 4-Bit Up / Down Counters (Dual Clock With Clear) IC
2	U35, 36	74175	Quad D Flip Flop With Clear IC
2	U37, 43	7403	Quad 2-Input NAND Gate
2	U38, 39	9324	5-Input Comparator IC
1	U44	7483	4-Bit Binary Full Adder and Dual Single-Bit Binary Full Adder IC
1	U46	2513	5 x 7 CM2140 Chr. Gen. IC
6	U47-52	2102	1K x 1 RAM IC

Where substitutions have been made or where actual component markings differ substantially from the printed parts list, new part numbers have been shown for your convenience.

If an (RO-3-2513) is used instead of the 2513 then the -12 volt supply is not needed.

Active Elect. Sales

IC's $ 29.63

Bd. $ 39.00

Passive $ 4.00

Sockets $ 10.00

TVT MODIFICATION
64 Char per line

MODIFICATION INSTRUCTIONS

1. DO NOT attempt this modification unless your TVT is completely functional.

2. Refer to the attached drawings and make the circuit TRACE cuts exactly as shown. (The 2 cuts in the circle at U-17 are only for the cursor Underscore change. Do not cut them unless you are going to install that change concurrent with the 64 Char change.)

3. Remove the IC (7486) at location U-15. This is no longer needed.

4. Using small (30 AWG) wire connect the following points.

   ( ) Connect U14-5 to U12-5
   ( ) Connect U14-12 to U14-8
   ( ) Connect U14-8 to U15-6 (U15 is empty socket)
   ( ) Connect U27-9 to U31-11
   ( ) Connect U27-10 to U31-9

5. REMOVE C38 (47pf) capacitor located next to U18-15 and REPLACE with a 18pf capacitor

6. Carefully Drill holes to mount 2 14-pin and 2 16-pin sockets along the edge of the board adjacent to U39, U45 and U52. (you may wish to mount these sockets on a small PC board.)

7. Using your favorite wiring technique (ie, wire wrap, point to point, or etched circuit) wire the 4 sockets as shown on the schematic and connect to the locations indicated on the TVT.

8. Install the 4 IC's

9. DOUBLE-CHECK all wiring and Trace Cuts.

10. Apply power and readjust the 3 POTS for a stable display.

11. If you do not have a stable 64x16 display RE-CHECK all wiring again.

12. If you do have a good display, enter all 64 ASCII Characters and verify they display correctly.

13. Turn off the power and then turn it back on to get a full screen of mixed characters.

14. Adjust the DOT RATE POT over its full range while watching the screen and see if any characters change their dot pattern. If they do, the most probable cause is SLOW MEMORIES. This problem has also been traced to a SLOW CHARACTER GENERATOR. It is possible, by observation to figure out which Memory is causing the problem. (If your memories are rated for 500ns or faster) You should have no problem, unless it is the 2513 Character Gen.

15. In some cases, it might not be possible to cover the entire range of the DOT RATE POT without some of the characters changing their pattern. This is OK as long as we can get a full 64 Char. line on the screen without errors.

    Since many MONITORS overscan the screen, you should try adjusting your Horiz Width to JUST BARELY fill the screen. This will in effect, give the slowest DOT RATE requirement and the best operating point for the TVT.

    NOTE- SOME MONITORS use the overscan, to cover up Horizontal Linearity problems, so your width adjustment might have to be a Compromise between Linearity and DOT RATE.

COMMENTS

I hope anyone installing this change will enjoy it as much as I do. It makes the BAY AREA TVT a very pleasant looking display and leaves little to be desired. If you add the Underscore Cursor and 1200 BAUD changes its even better yet!

With the addition of some more memory and some additional changes I see no reason the Second Page could not be implimented as in the orginal TVT. (I have not attempted this yet!)

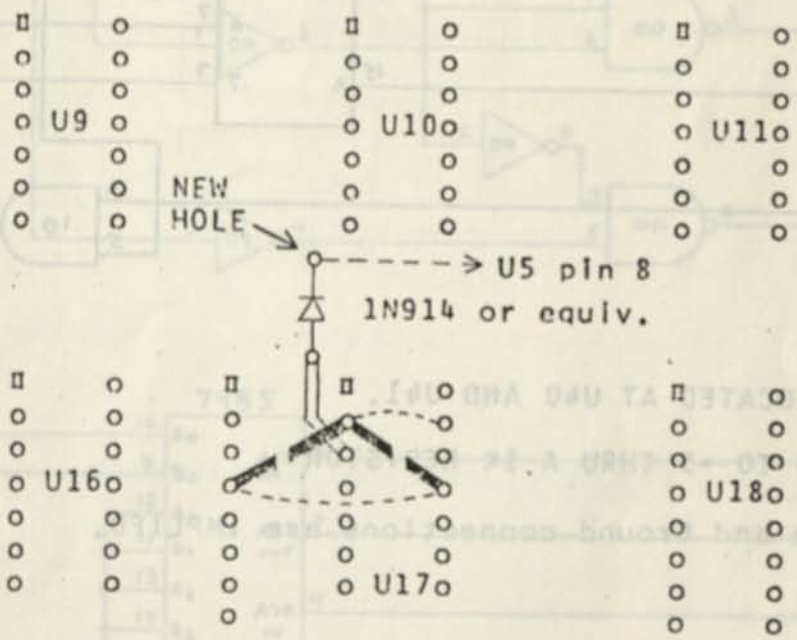
BAY-AREA TVT CURSOR MODIFICATION

PURPOSE: This modification changes the function of the CURSOR from a BIG flashing square to a flashing UNDERSCORE which will not obscure the character being marked!

COMMENTS: This modification is very simple and only requires the cutting of 2 PC Traces and the addition of a single diode and 3 JUMPERS.

NOTE: The IC and/or Socket located at U17 MUST be removed since one of the traces which must be cut is located on the component side under it! Install U17 when modification is completed.

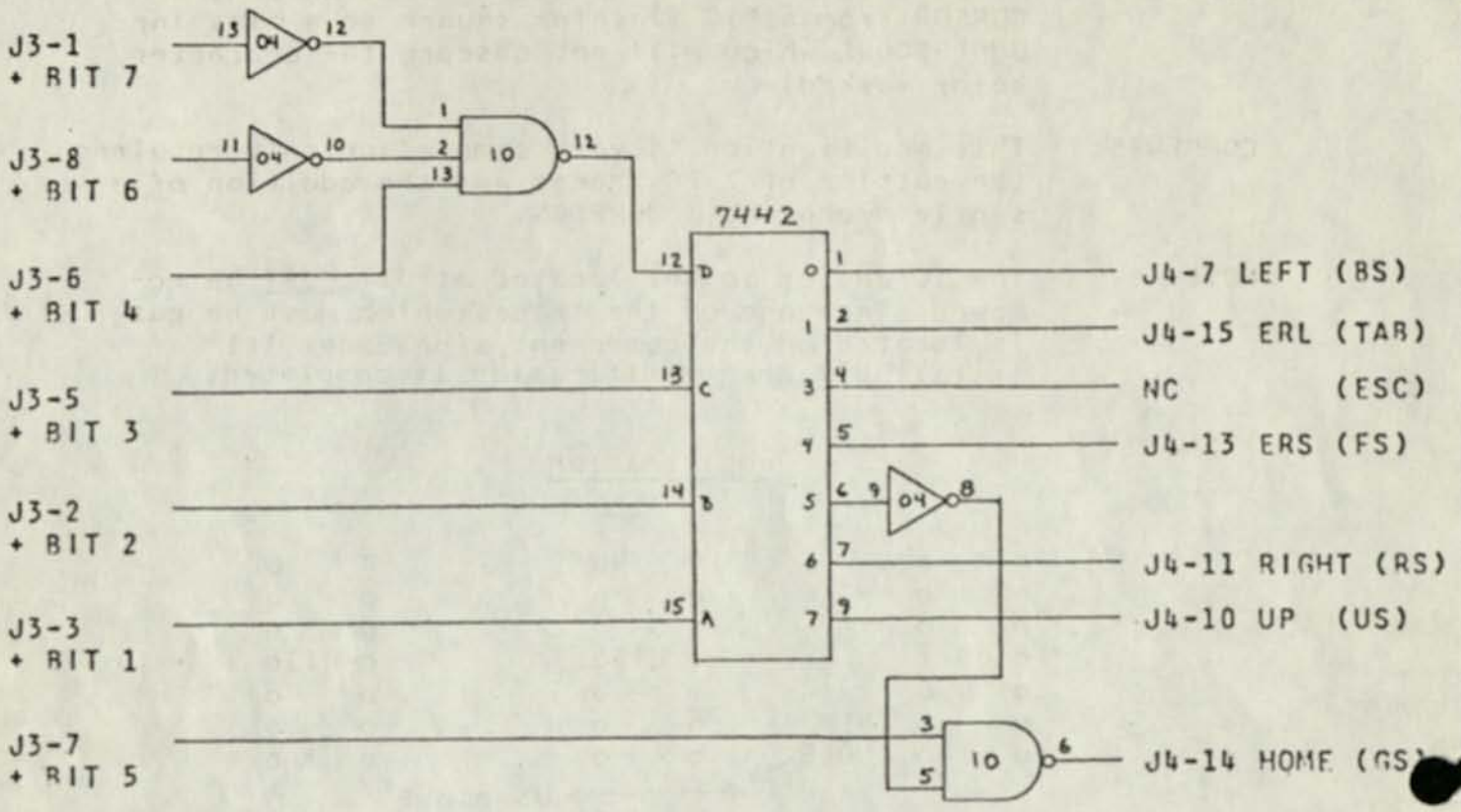
MODIFICATION



COMPONENT SIDE

------ JUMPER
LAND (COMPONENT SIDE)
LAND (CIRCUIT SIDE)
CUT LAND

BAY AREA TVT
CURSOR CONTROL



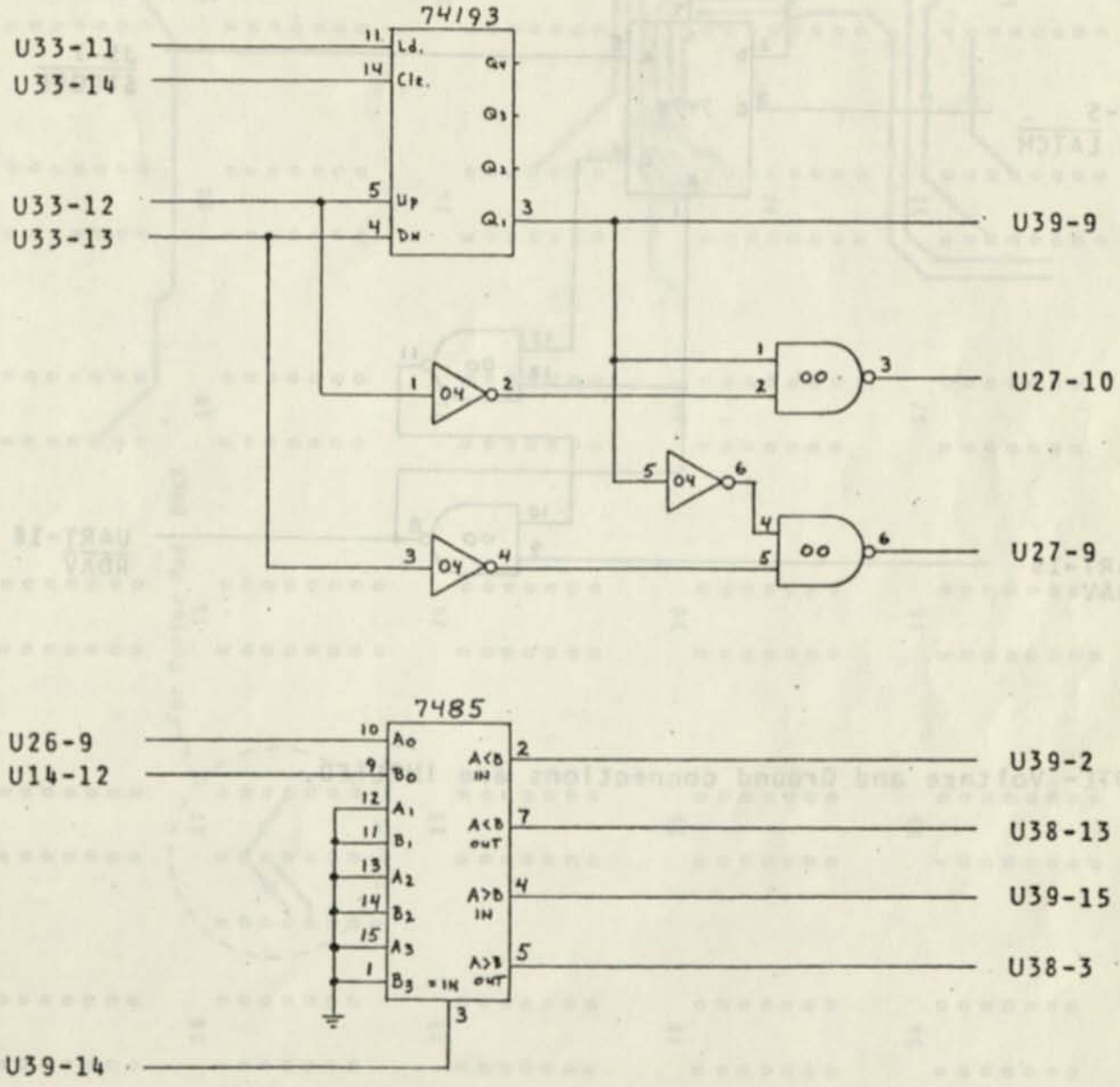
REMOVE IC's LOCATED AT U40 AND U41.

TIE UP U40-13 TO +5 THRU A 1K RESISTOR

NOTE- Voltage and Ground connections are IMPLIED.

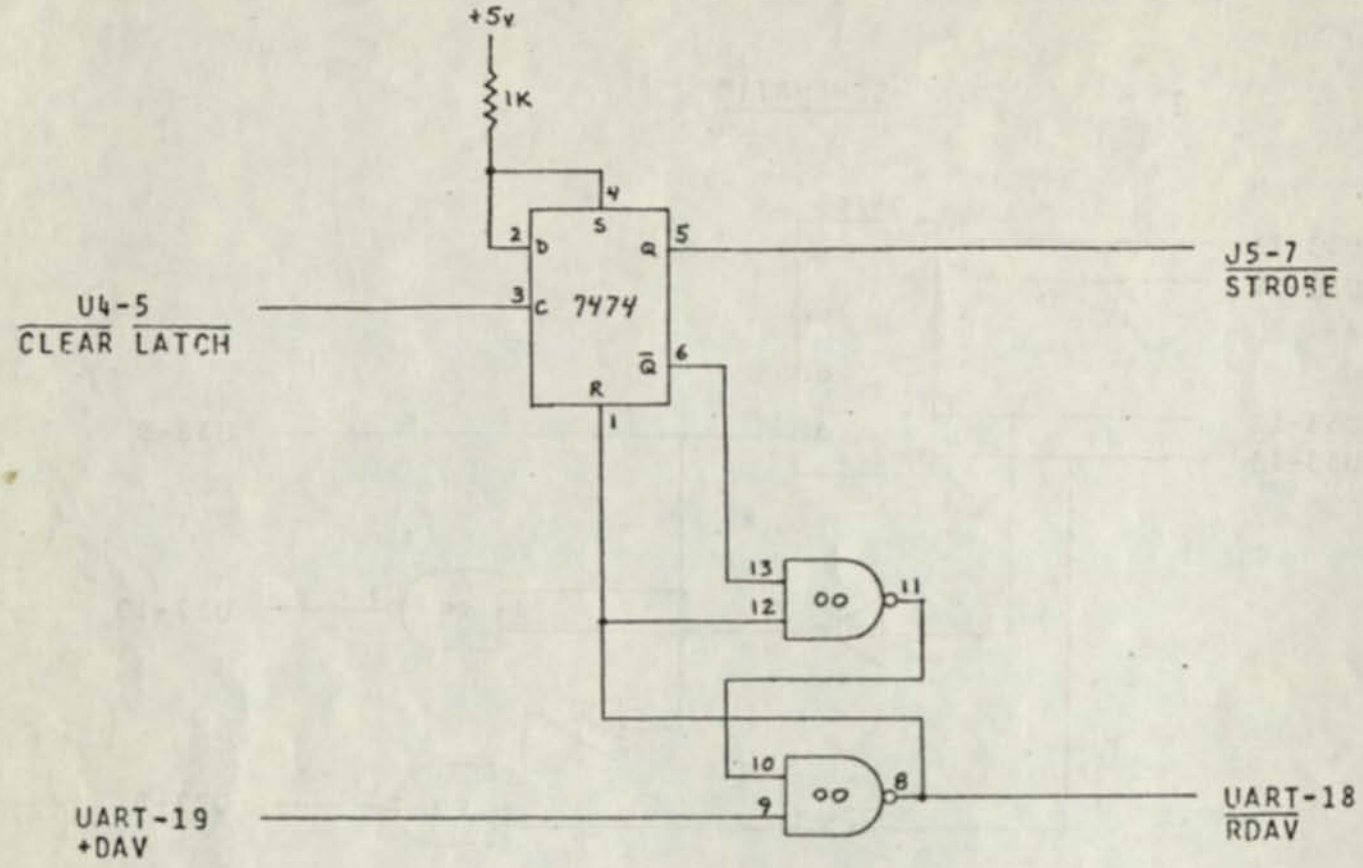
BAY AREA TVT MOD.
64 Char per Line

SCHEMATIC



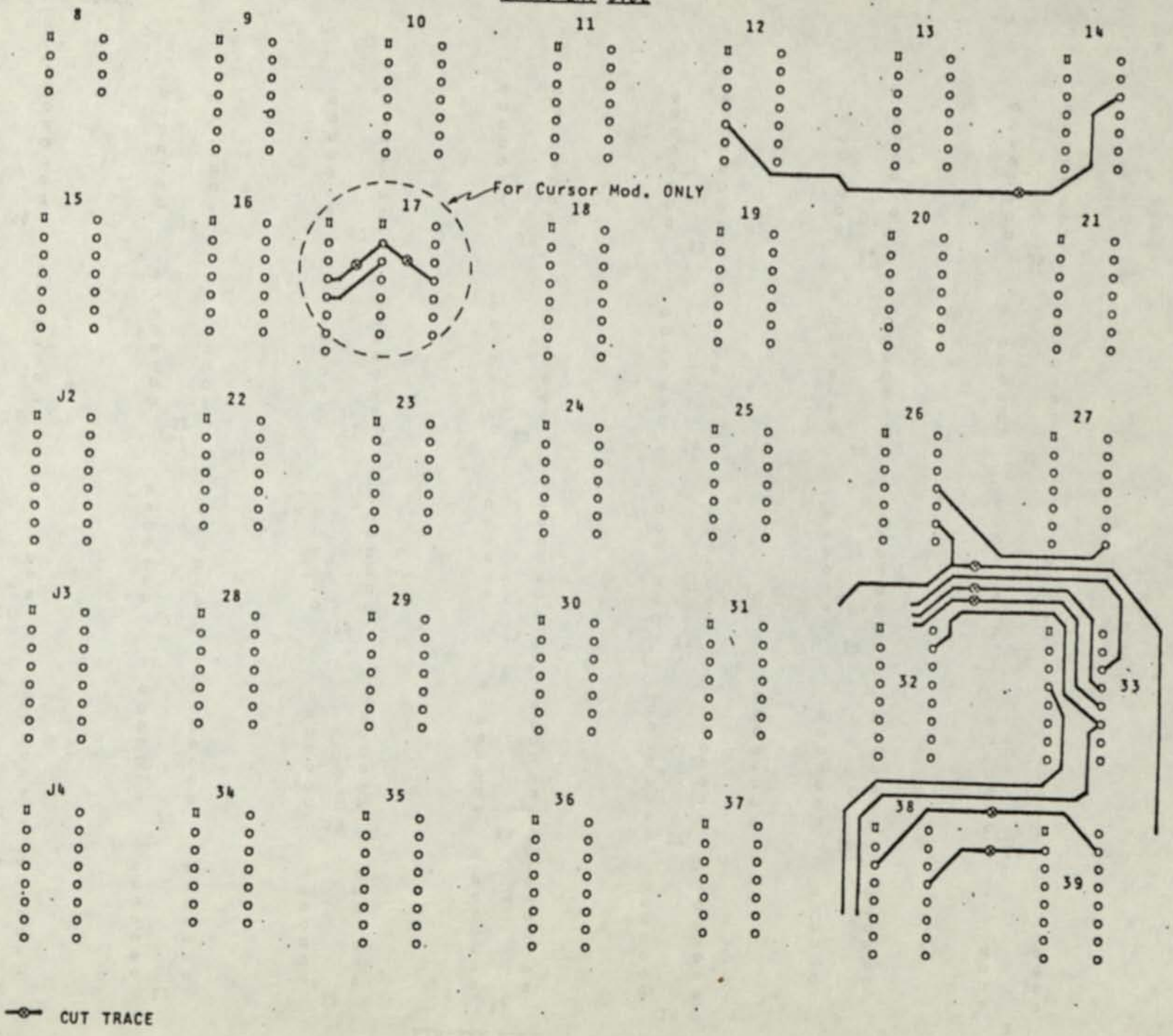
NOTE - Voltage and Ground connections are IMPLIED.

1200 BAUD TVT MOD.



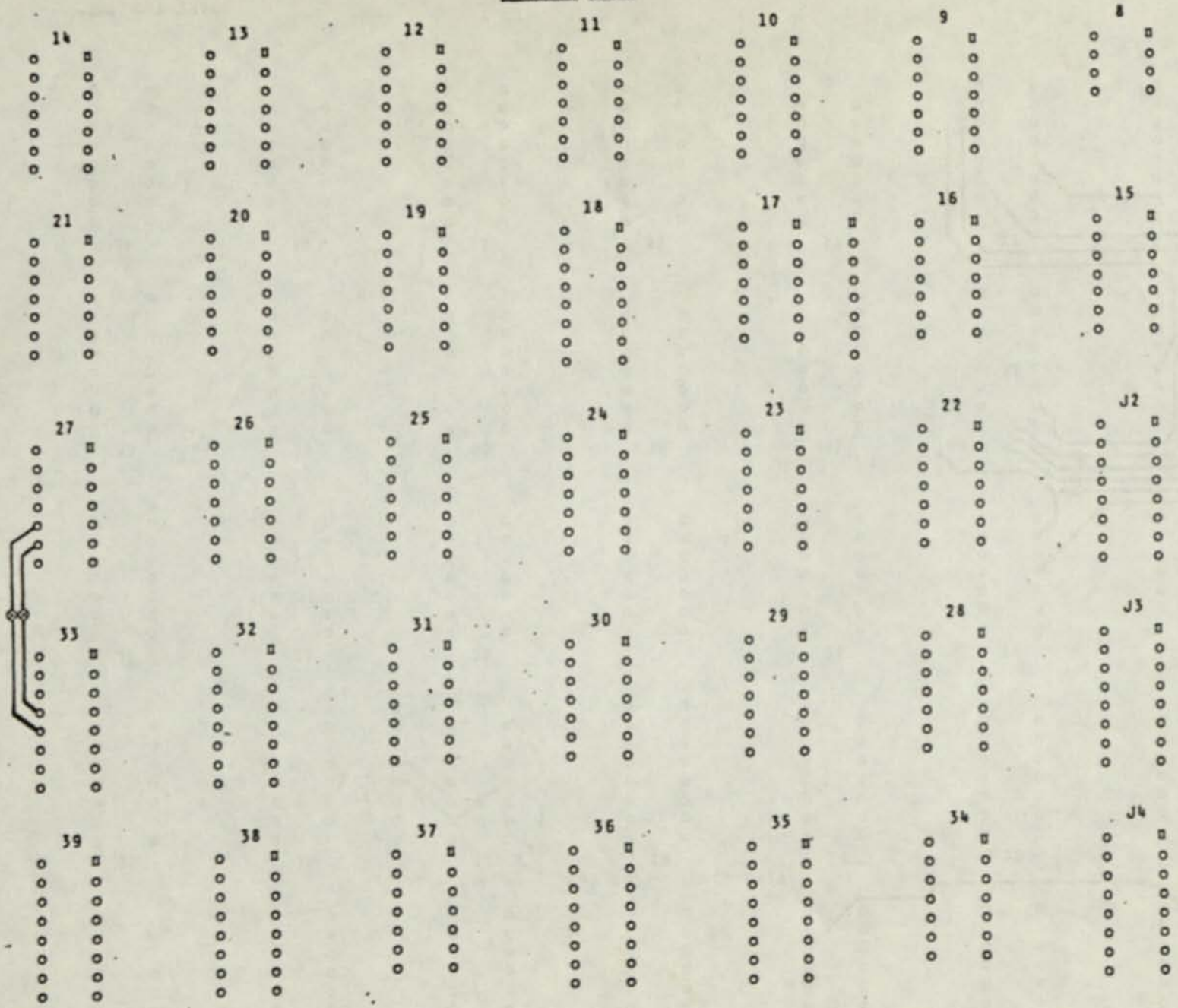
NOTE- Voltage and Ground connections are IMPLIED.

COMPONENT SIDE



CUT TRACE

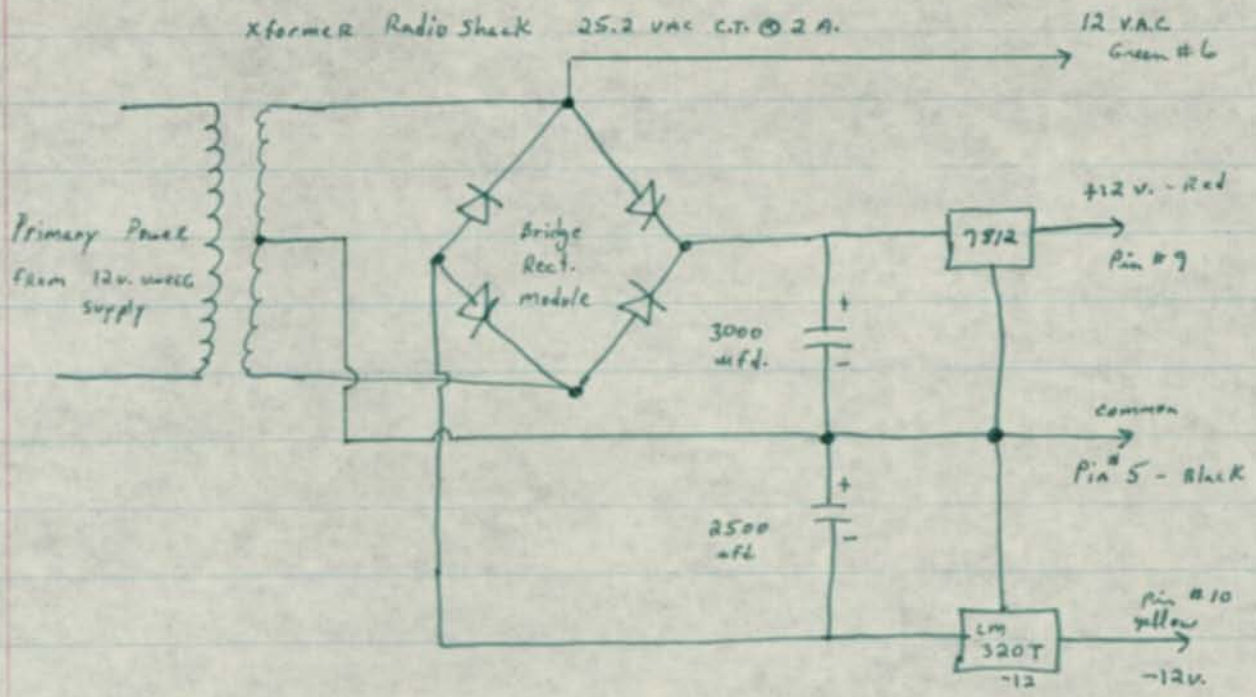
CIRCUIT SIDE



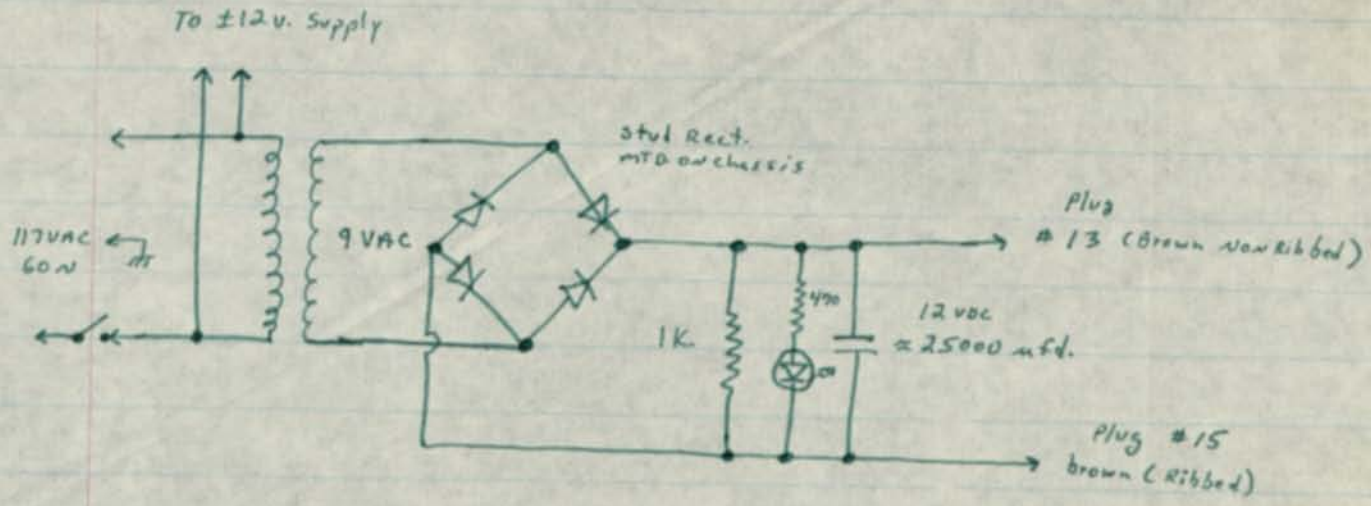
CUT TRACE

Power Supply

± 12 v. at 1 A.

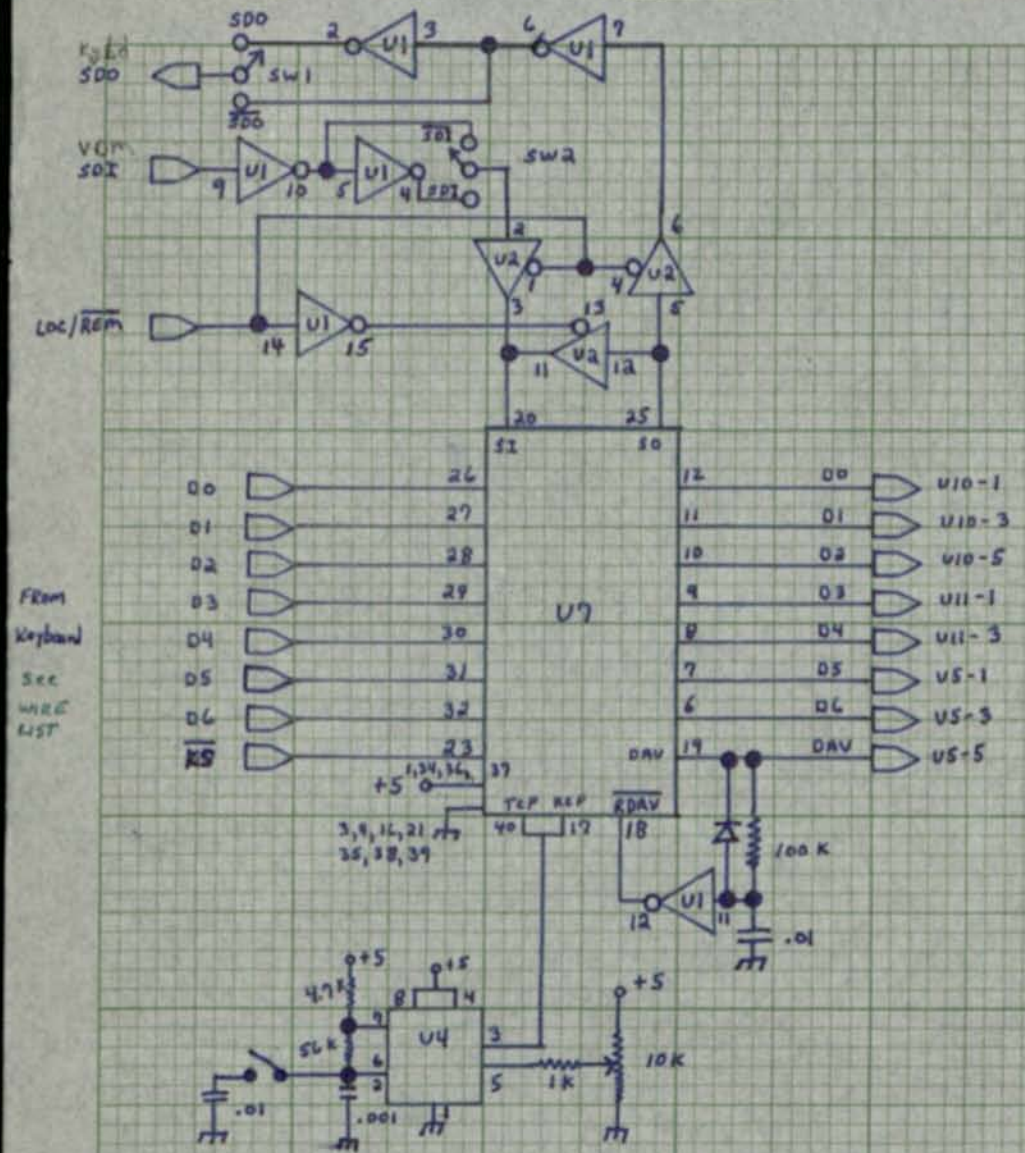

Xformer Radio Shack 25.2 VAC C.T. @ 2 A.
12 V.A.C
Green #6
Primary Power
from 12v. unreg
supply
Bridge
Rect.
module
7812
+12 v. - Red
Pin #9
3000
mfd.
+
-
common
Pin #5 - Black
2500
mfd
+
-
Pin #10
yellow
LM
320T
-12
-12v.

+12 UNREG


To ±12v. Supply
117VAC
60~
9 VAC
Stnl Rect.
mtd on chassis
Plug
13 (Brown Non Ribbed)
1K.
470
12 VDC
≈ 25000 mfd.
Plug #15
brown (Ribbed)

UART & CONTROL -A2
DECODE ASSY

UART/SERIAL P/O A2



Ref	TYPE	Vcc	GND	V_{BB}
U1	CD4049	1	8	
U2	74125	14	7	
U4	555	8	1	
U7	AY5-1013A	1	3	2

UART

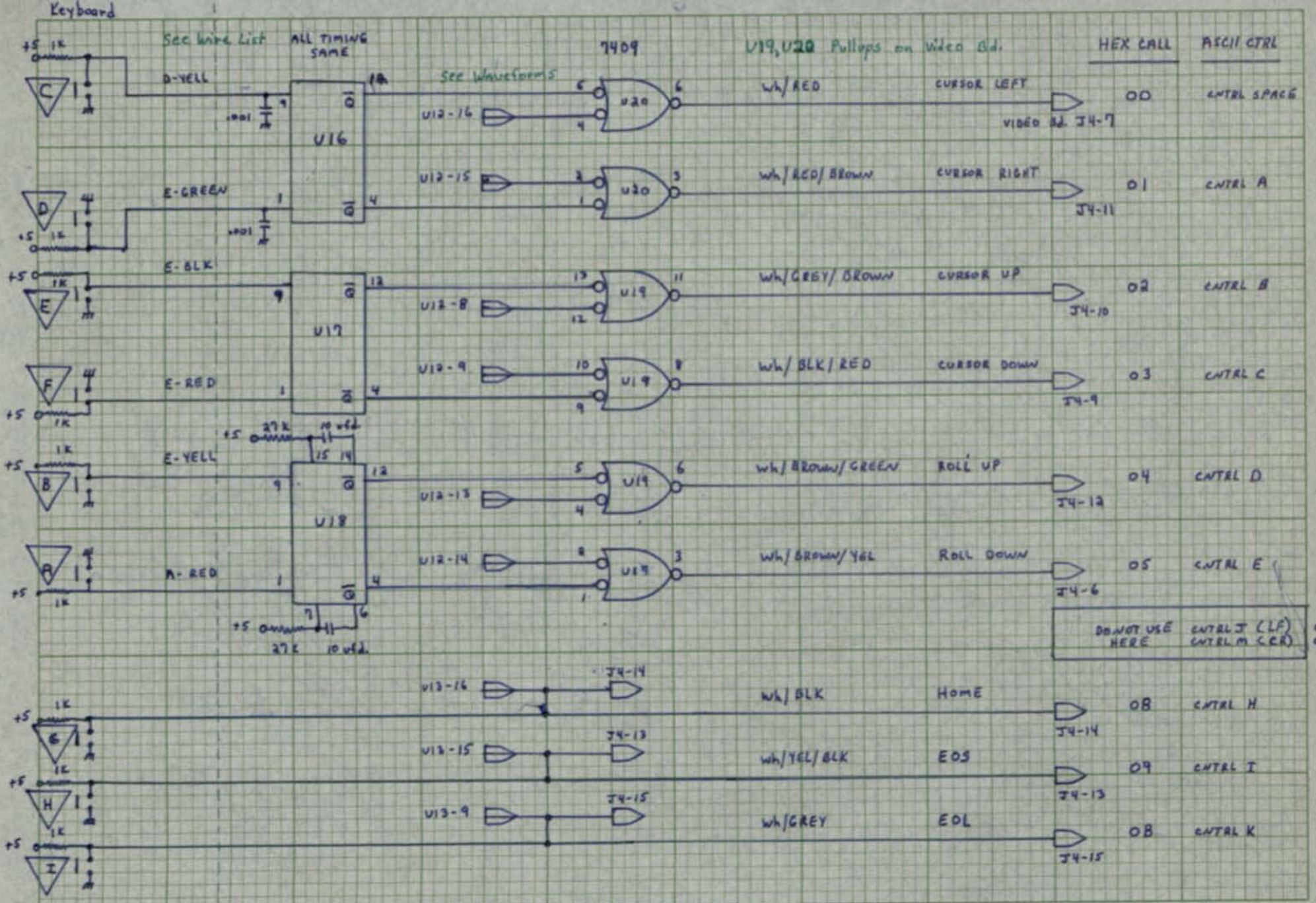
7 BITS/char
1 Parity Bit
1 START BIT
2 STOP BITS

GRAPHIC CONTROLS CORPORATION BUFFALO, NEW YORK — SQUARE 10 X 10 TO THE INCH AS-0007-47

Debounce P/O A2

Ref	TYPE	Vcc	GND
U16, 17, 18	74123	16	8
U19, 20	7409	14	7

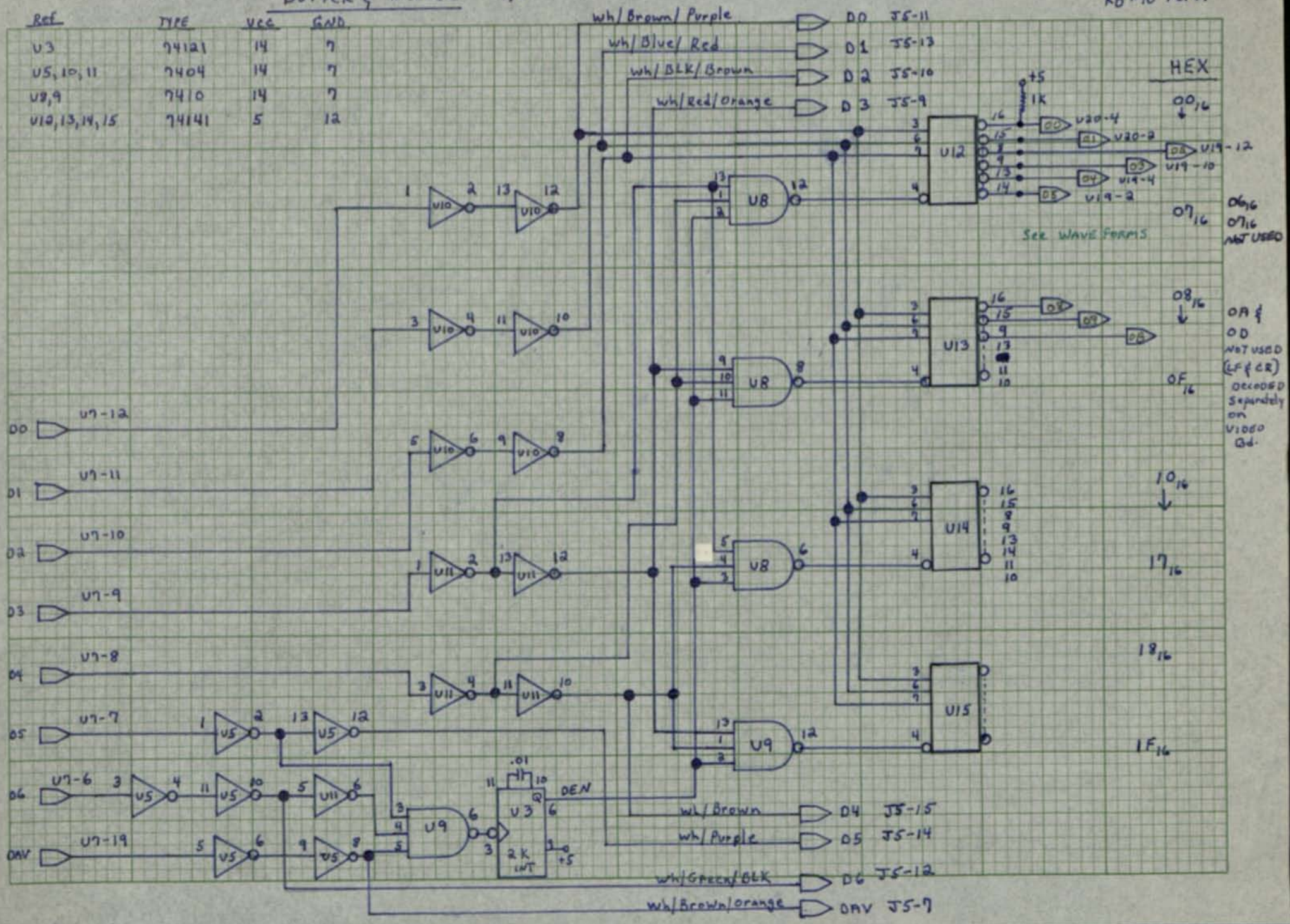
Keyboard

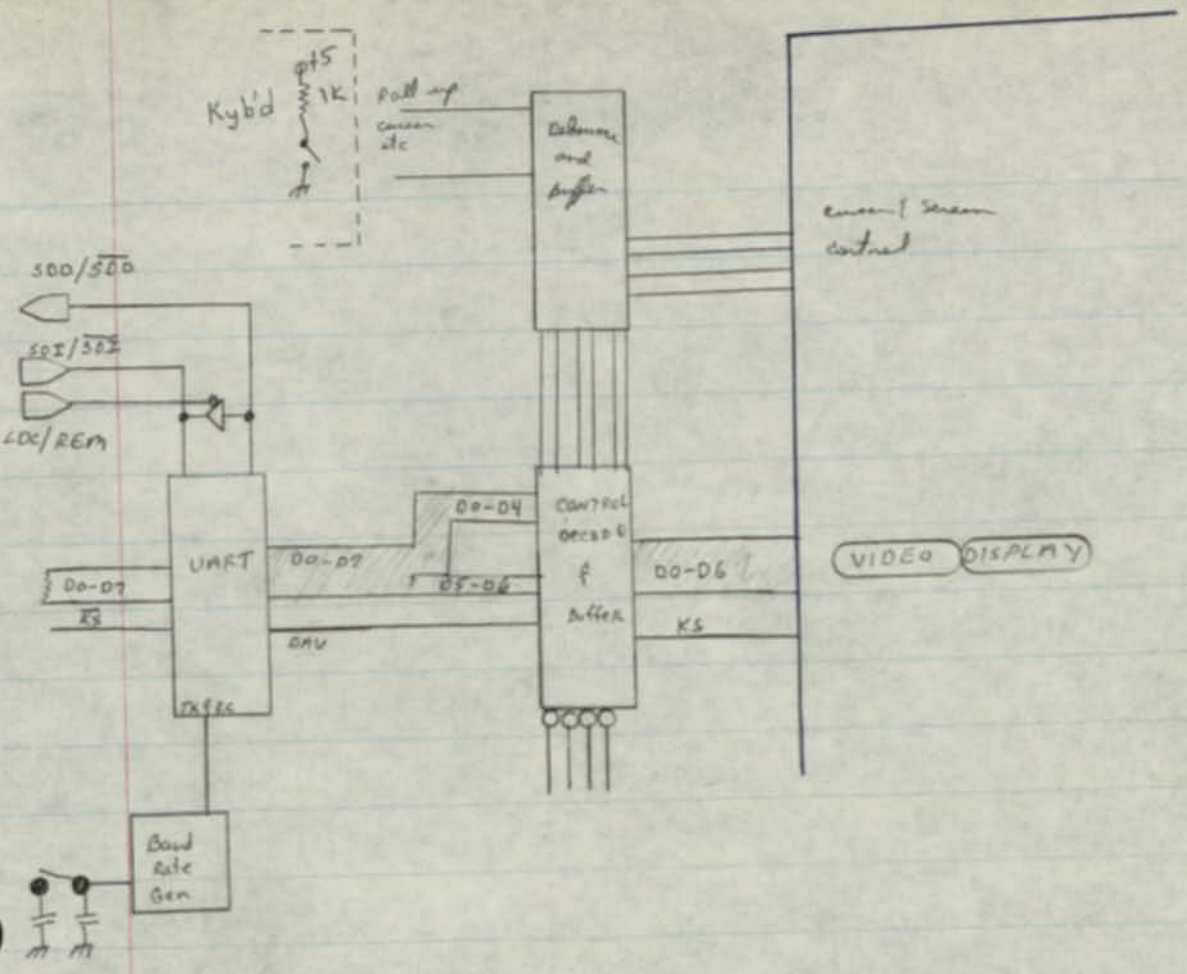


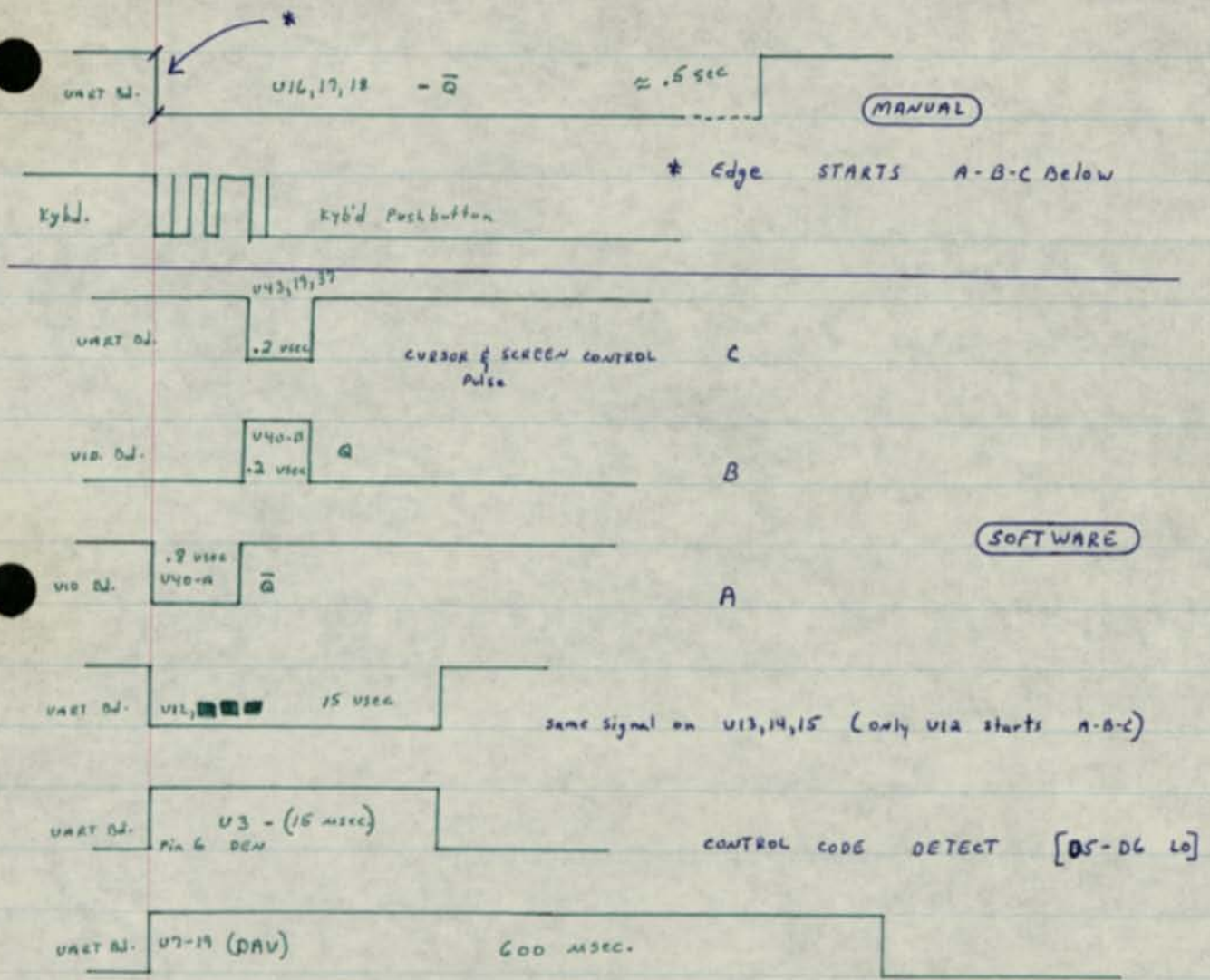
Buffer & Decode P/O A2

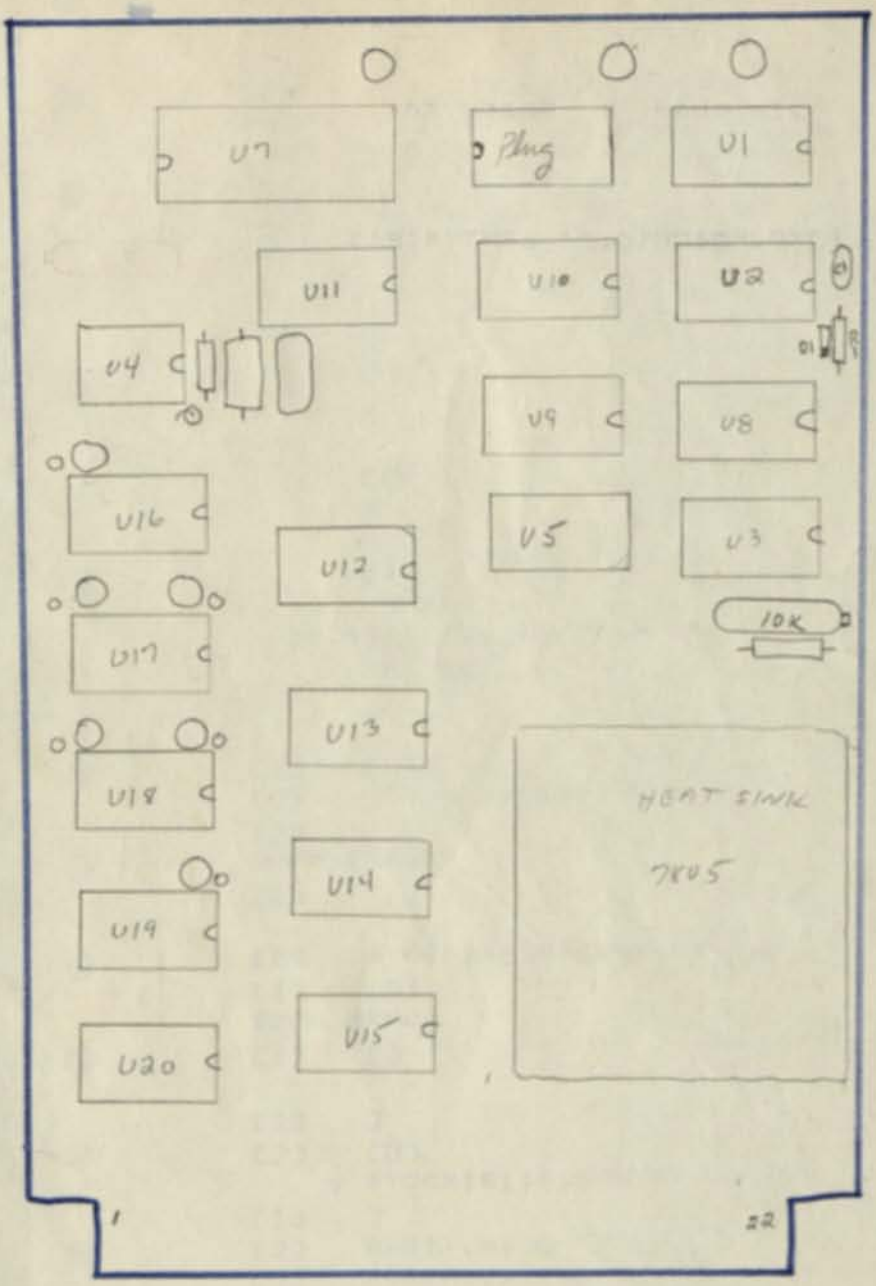
KB #10 Pc. 81

Ref	TYPE	VCC	GND
U3	74121	14	7
U5, 10, 11	7404	14	7
U8, 9	7410	14	7
U12, 13, 14, 15	74141	5	12



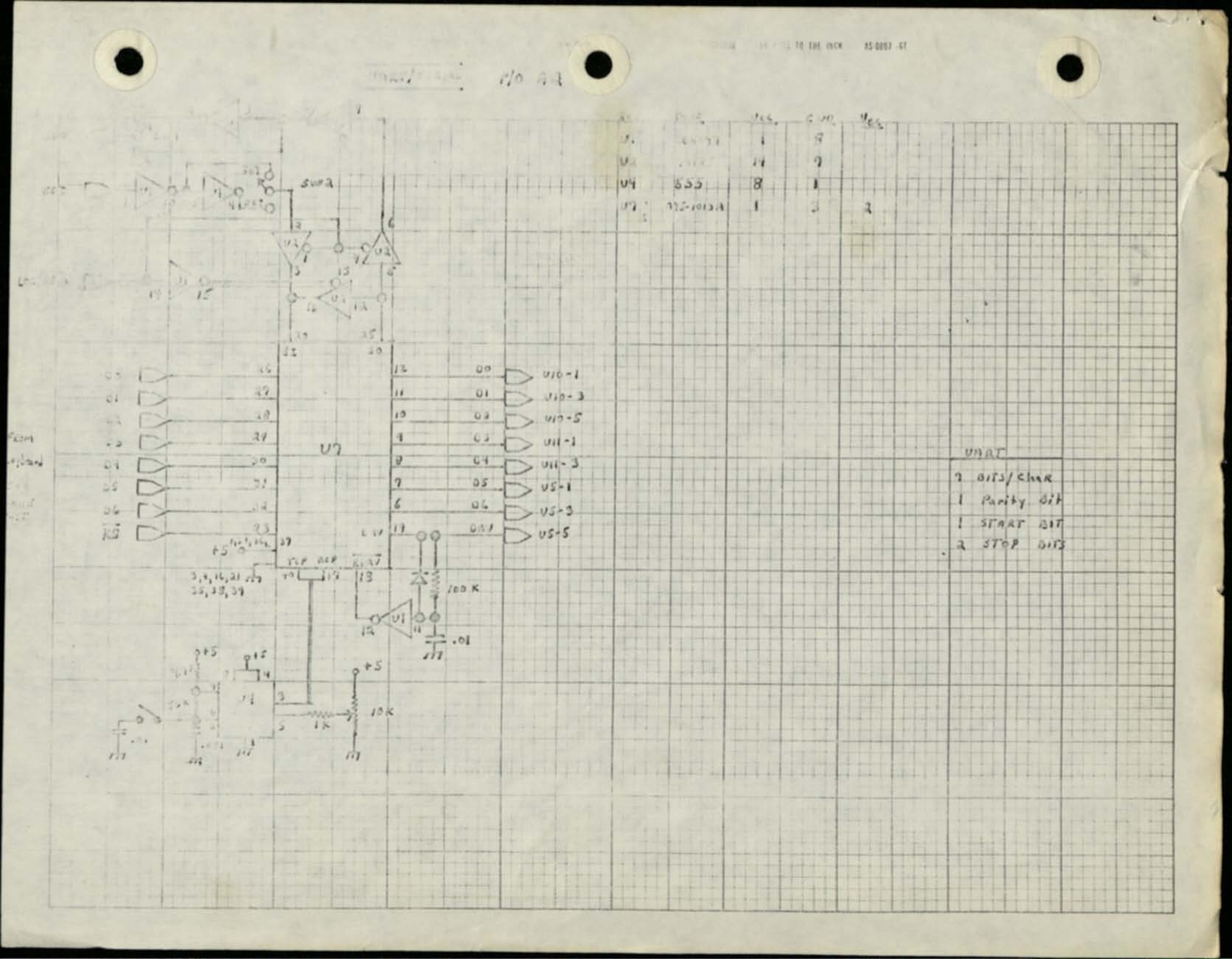

Kyb'd
pt5
1K
Pull up
SDO/SDO
SDI/SDI
LOC/REM
UART
D0-D7
RS
DAV
D0-D4
D5-D6
CONTROL
DECODE
&
BUFFER
D0-D6
RS
VIDEO
DISPLAY
Baud
Rate
Gen


UART BJ.
U16, 17, 18 - $\overline{Q}$
≈ .5 sec
MANUAL
* Edge STARTS A-B-C Below
Kybd.
kyb'd Pushbutton
U43, 19, 37
UART BJ.
.2 msec
CURSOR & SCREEN CONTROL Pulse
C
VID. BJ.
U40-B
.2 msec
Q
B
SOFTWARE
VID BJ.
.8 msec
U40-A
$\overline{Q}$
A
UART BJ.
U12,
15 msec
same signal on U13, 14, 15 (only U12 starts A-B-C)
UART BJ.
U3 - (16 msec)
Pin 6 DEN
CONTROL CODE DETECT [D5-D6 LO]
UART BJ.
U7-19 (DAV)
600 msec.

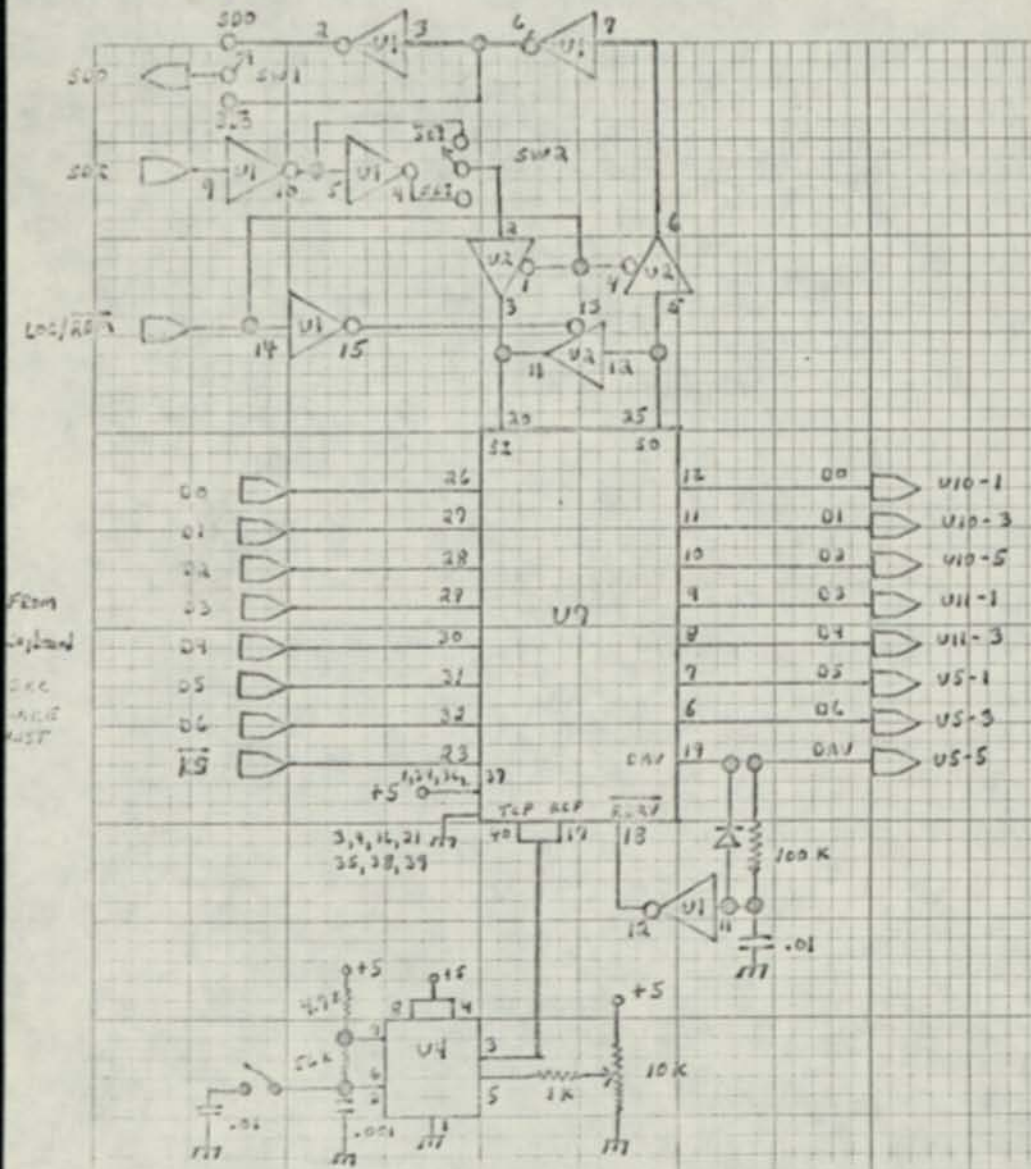


UART

CONTROL DECODE


SW2
U7
U10-1
U10-3
U10-5
U11-1
U11-3
U5-1
U5-3
U5-5
100 K
.01
10K
1K
+5
VART
7 BITS/CHAR
1 Parity BIT
1 START BIT
2 STOP BITS

UART/SERIAL P/O A2



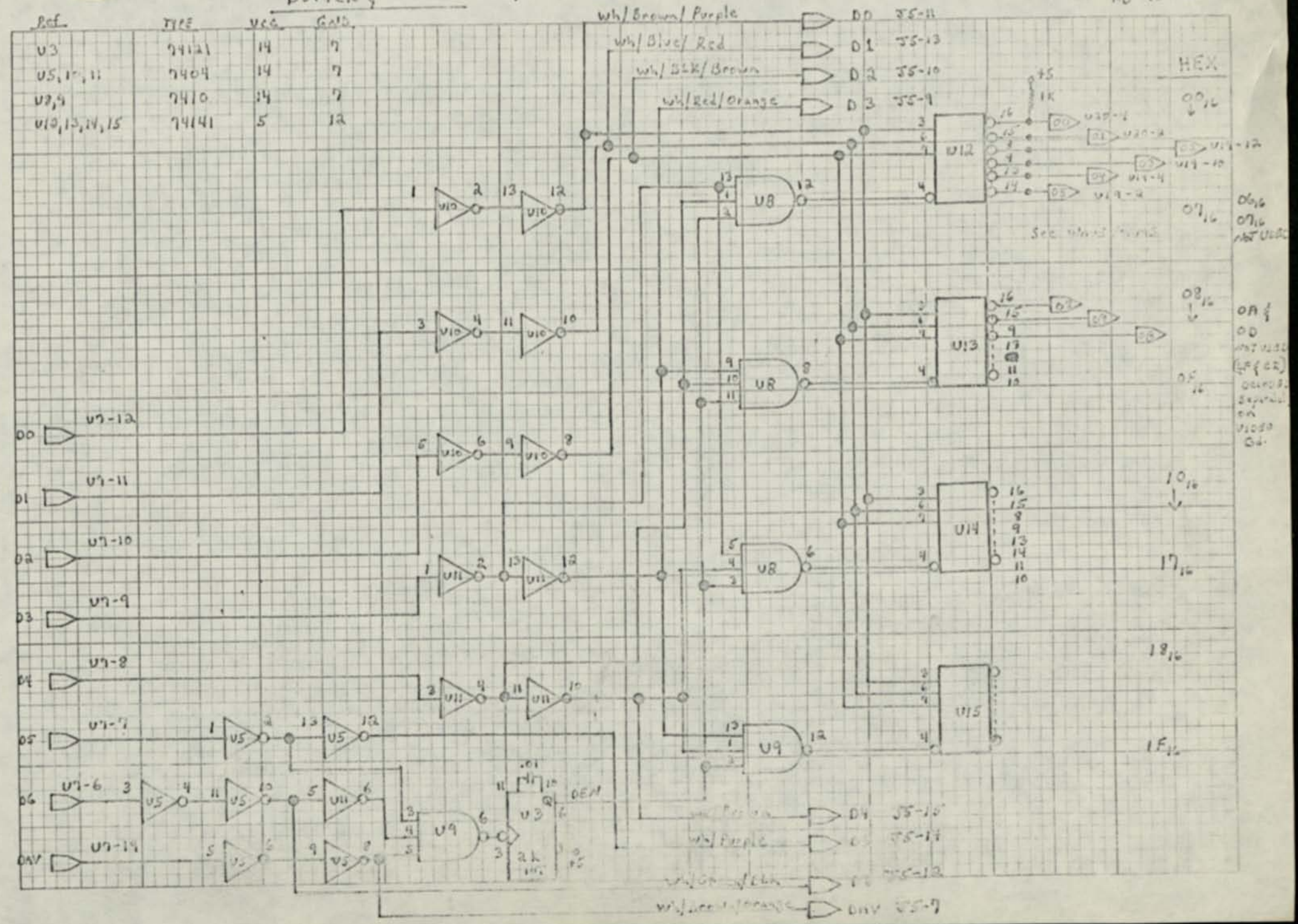
Ref.	Type	Vcc	GND	V_{BB}
U1	2049A9	1	8	
U2	74125	14	7	
U4	555	8	1	
U7	AYS-1013A	1	3	2

UART
7 BITS/CHAR
1 Parity Bit
1 START BIT
2 STOP BITS

Buffer & Decode P/O A2

KB #10 Pg. 91

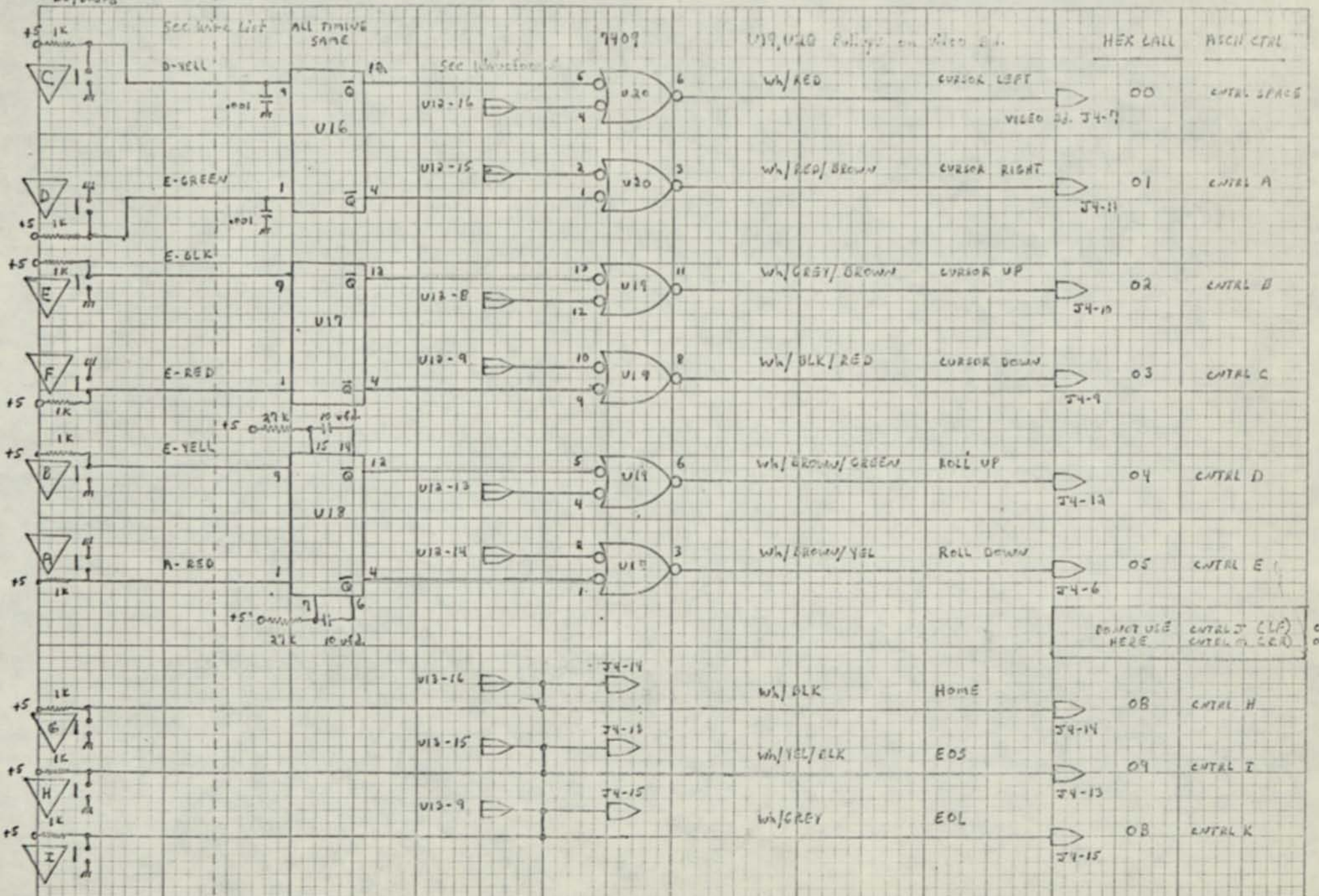
Ref.	Type	Vcc	Gnd
U3	74121	14	7
U5, 7, 11	7404	14	7
U8, 9	7410	14	7
U12, 13, 14, 15	74141	5	12



Debounce P/O A2

Ref	TYPE	Vcc	GND
U16,17,18	74123	16	8
U19,20	7409	14	7

Keyboard



MARCH 1974

UAR/T UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

AY-5-1013/AY-5-1013A

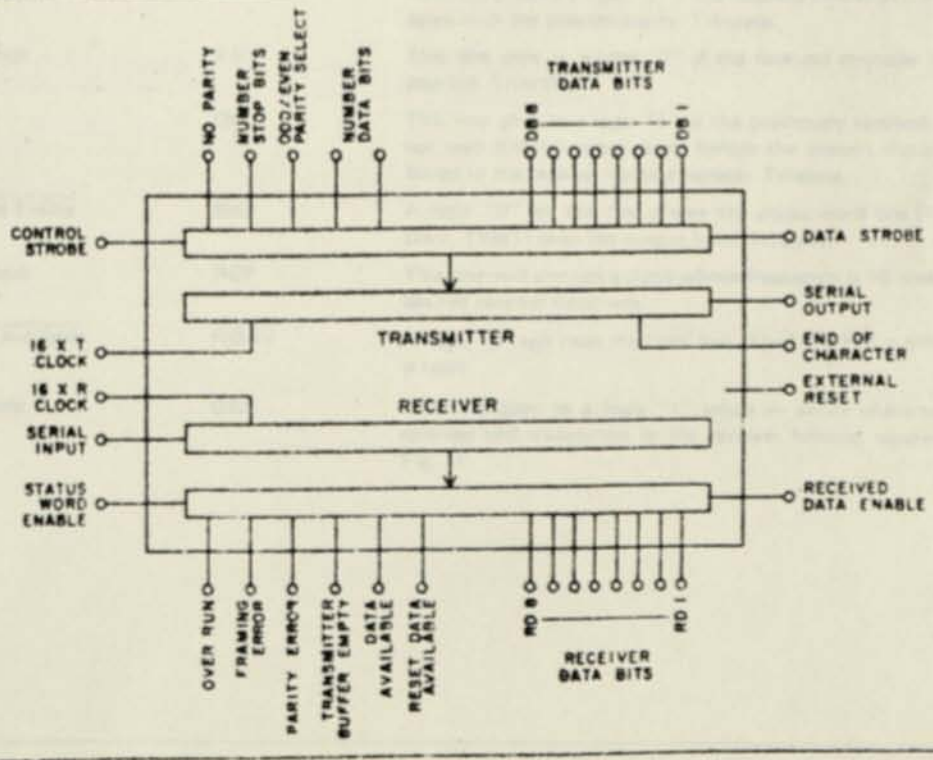
FEATURES

- DTL and TTL Compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- External reset of error flags.
- High Speed Operation—greatest through-put: 30k baud (AY-5-1013), 40k baud (AY-5-1013A).
- Tri-State Outputs—bus structure capability.
- Low Power—minimum power requirements.
- Input Protected—eliminates handling problems.
- Hermetic DIP Package—easy board insertion and mechanical handling.

GENERAL DESCRIPTION

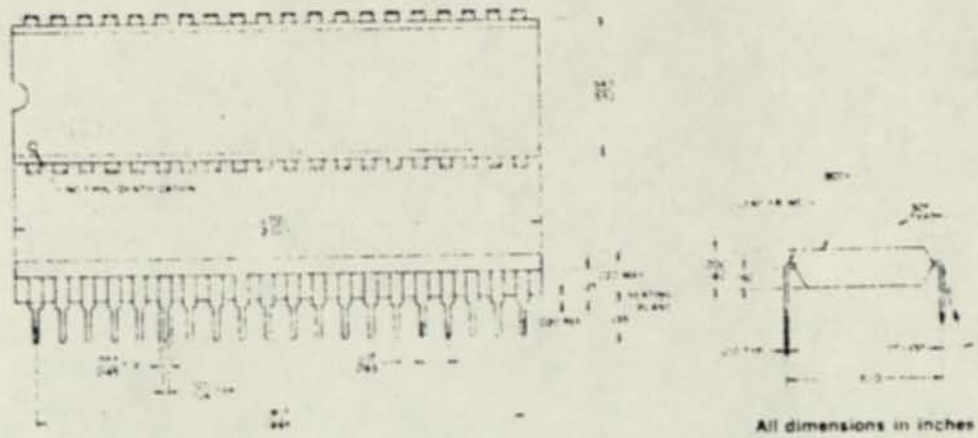
The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud rate, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL logic without the need for interfacing components and with all strobed outputs having tri-state logic.

FIGURE 1
BLOCK DIAGRAM



PIN CONFIGURATION

PACKAGE: 40 LEAD PLASTIC DUAL IN-LINE



All dimensions in inches

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	−12V Supply
3	Ground	V_{GI}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run	OR	This line goes to a logic "1" is the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDAV}$	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available	DAV	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 13

Pin No.	Name	Symbol	Function
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 12, 13.
21	External Reset	XR	Resets shift registers. Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 29, 21.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 18, 20.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 17.
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits/Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

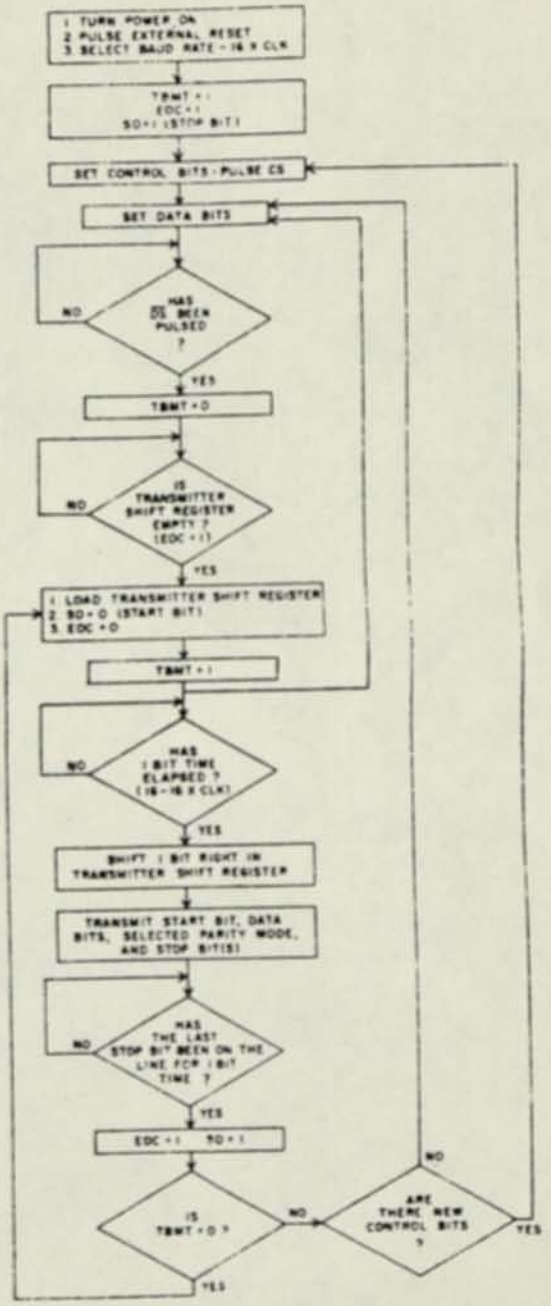
TRANSMITTER OPERATION
FIGURE 2

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occuring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1", When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.



RECEIVER OPERATION
FIGURE 3

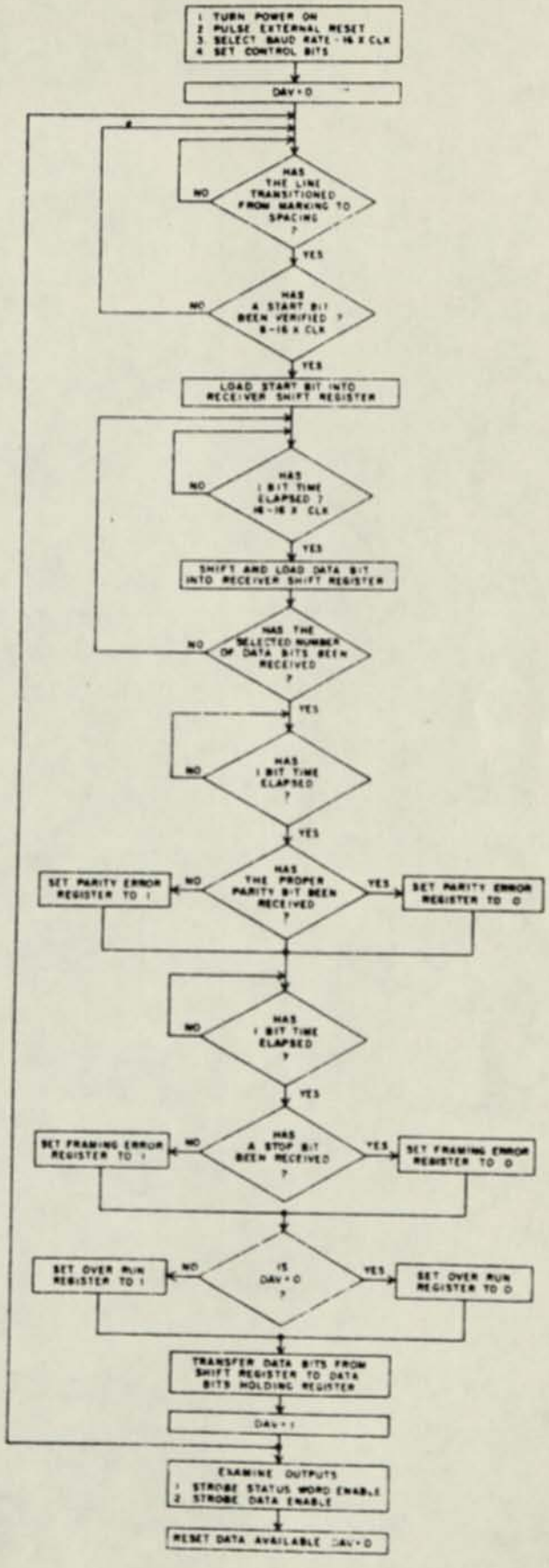
Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DAV) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{GG} (with respect to V_{CC})	−20 to +0.3V
Clock and logic input voltages (with respect to V_{CC})	−20 to +0.3V
Storage Temperature	−65°C to 150°C
Operation Temperature	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	330°

STANDARD TEST CONDITIONS

The following characteristics apply for any combination of the following test conditions, unless otherwise noted. All voltages are measured with respect to ground. Positive current is defined as flowing into the referenced pin.

$V_{GG} = -12V \pm 5\%$ $V_{CC} = 5V \pm 5\%$ $0°C < T_A < 70°C$

ELECTRICAL CHARACTERISTICS (see standard conditions)

PARAMETER	CONDITIONS AND COMMENTS	MIN.	TYP.	MAX.	UNITS
Input Logic Levels					
Logic 0	V_{IL} (I_{IL} = −1.6mA max.)	0	–	0.8	volts
Logic 1	V_{IH} Unit has internal pullup resistors	V_{CC}−1.5	–	V_{CC}+0.3	volts
Input Capacitance					
All Inputs	0 volts bias, f = 1MHz	–	–	20	pF
Leakage Currents					
Tri-State Outputs	0 volts	–		1.0	µA
Data Output Levels					
Logic 0	I_{OL} = 1.6mA (sink)	–	–	+0.4	volts
Logic 1	I_{OH} = −.3mA (source)	V_{CC}−1.0			volts
Output Capacitance		–	10	15	pF
Short Ckt. Current	See Fig. 24	–	–	–	–
Power Supply Current					
I_{GG} 25°C, all inputs +5V	See Fig. 26a	–	14	16	mA
I_{CC}	See Fig. 26b	–	18	20	mA
A.C. CHARACTERISTICS	T_A = 25°C, Output load capacitance 50pF max.				
Clock Frequency	AY-5-1013	DC	–	480	kHz
	AY-5-1013A	DC	–	640	kHz
Baud Rate	AY-5-1013	0	–	30	k baud
	AY-5-1013A	0	–	40	k baud
Pulse Width					
Clock Pulse	AY-5-1013 See Fig. 10	1.0	–		µs
	AY-5-1013A	750	–	–	ns
Control Strobe	See Fig. 16	300	–	–	ns
Data Strobe	See Fig. 15	190	–	–	ns
External Reset	See Fig. 14	500	–	–	ns
Status Word Enable	See Fig. 22	500	–	–	ns
Reset Data Available	See Fig. 23	250	–	–	ns
Received Data Enable	See Fig. 22	500	–	–	ns
Set Up & Hold Time					
Input Data Bits	See Fig. 15	>0	–	–	ns
Input Control Bits	See Fig. 16	>0	–	–	ns
Output Propagation Delay					
TPD0	See Fig. 22 & 25		–	500	ns
TPD1	See Fig. 22 & 25		–	500	ns

FIGURE 4 TRANSMITTER–BLOCK DIAGRAM

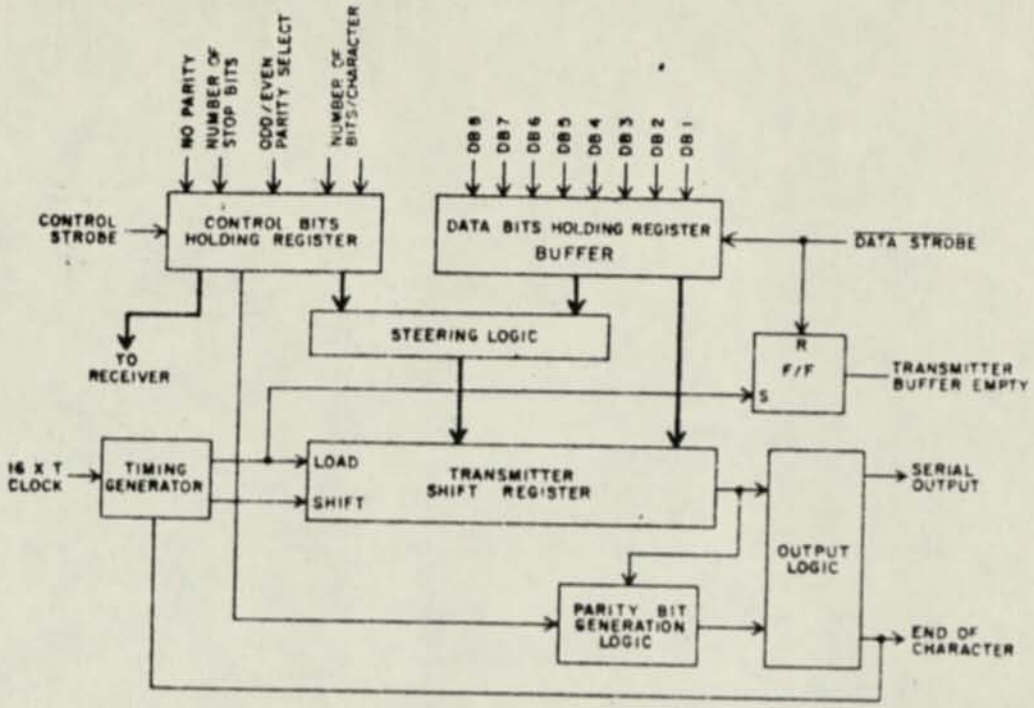


FIGURE 5 RECEIVER–BLOCK DIAGRAM

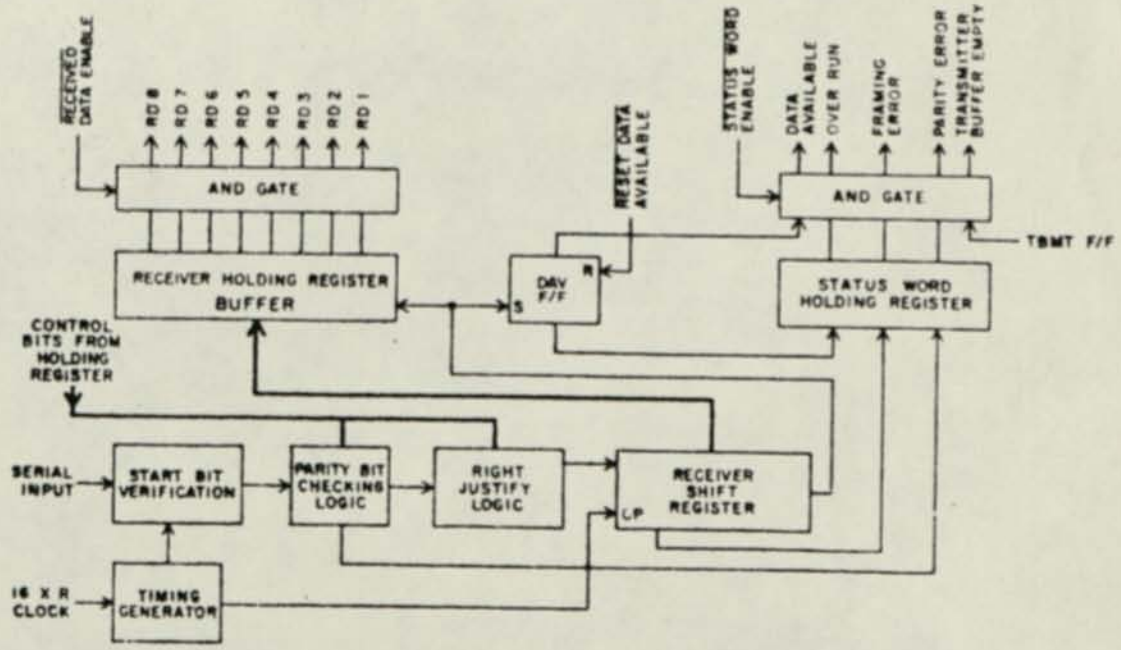
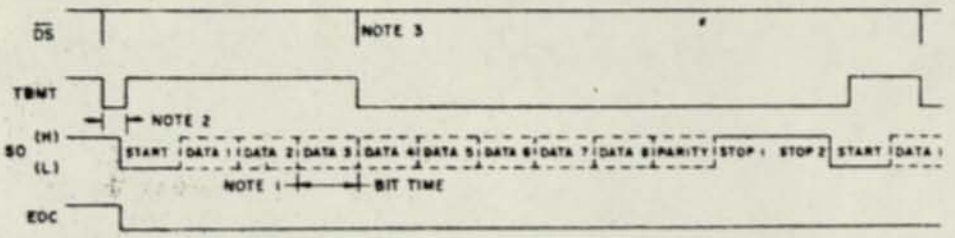


FIGURE 6 UAR/T–TRANSMITTER TIMING



NOTE SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

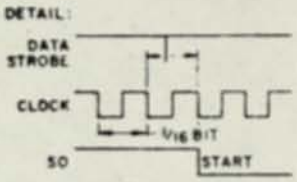


FIGURE 7 TRANSMITTER AT START BIT

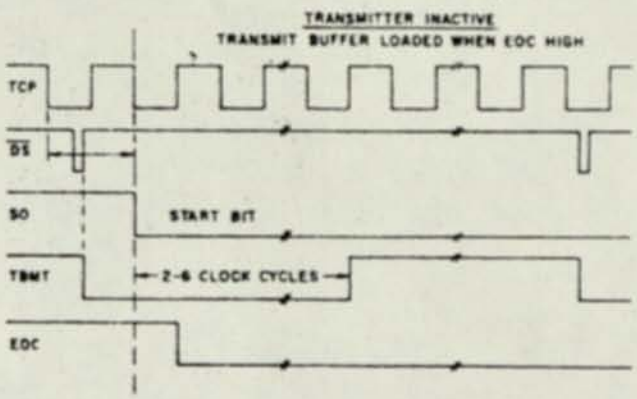


FIGURE 8 TRANSMITTER AT START BIT

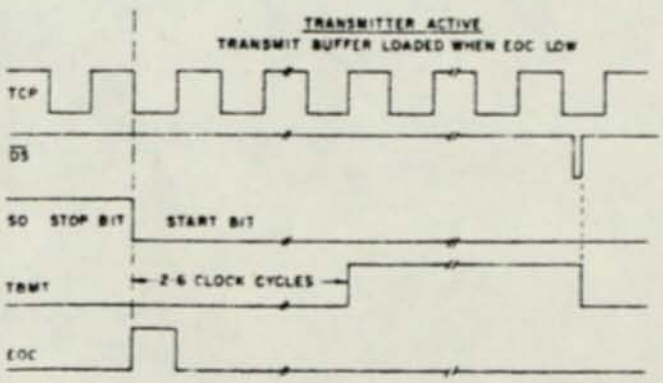


FIGURE 9 ALLOWABLE POINTS TO USE CONTROL STROBE

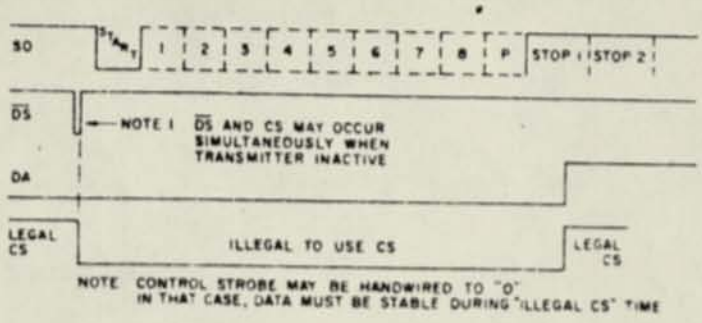


FIGURE 10 ALLOWABLE TCP, RCP

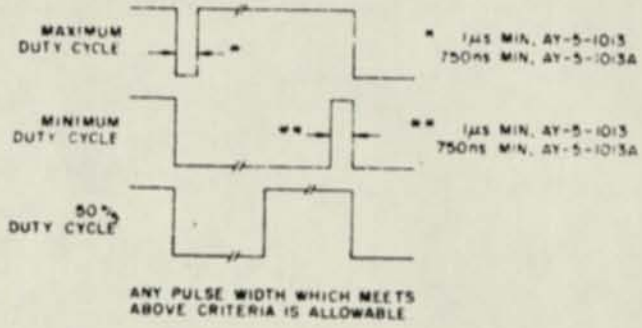
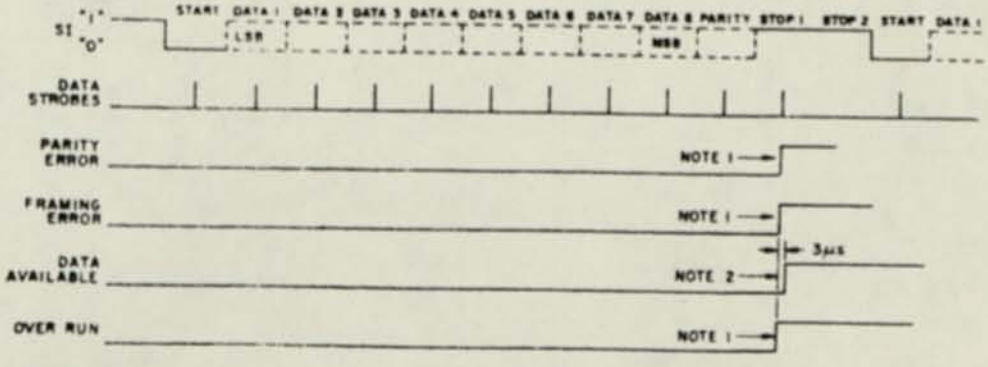


FIGURE 11 UAR/T–RECEIVER TIMING



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE OUTPARTED, IF ERROR OCCURS
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP FOR NO PARITY, STOP BITS FOLLOW DATA
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*, THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

FIGURE 12

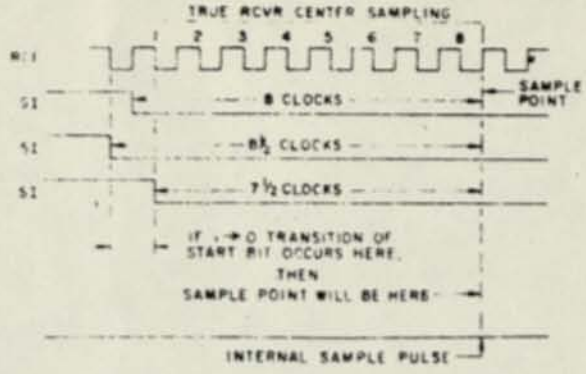


FIGURE 13 RECEIVER DURING 1st STOP BIT

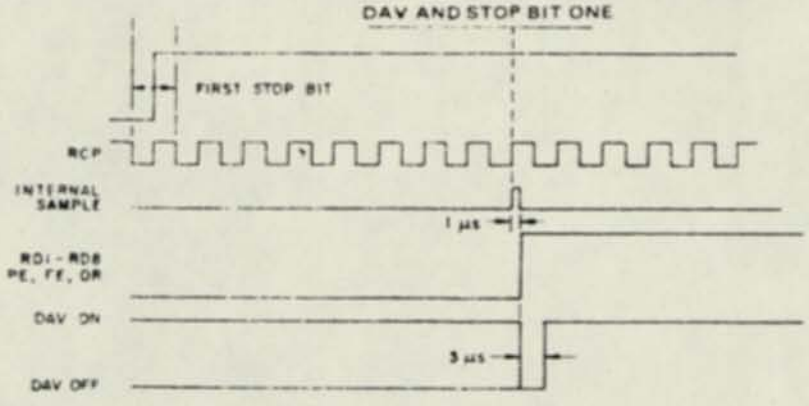
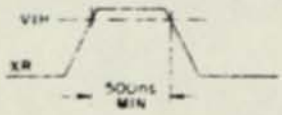


FIGURE 14 XR PULSE



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER RECEIVED DATA SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V.

FIGURE 15 $\overline{DS}$

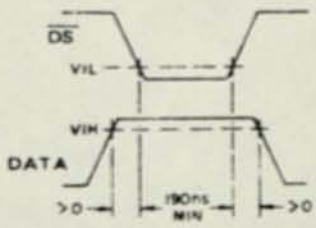
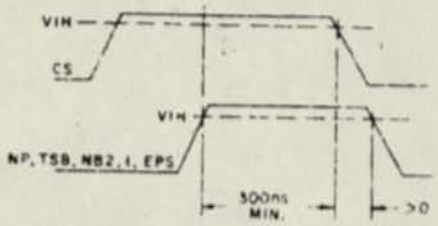
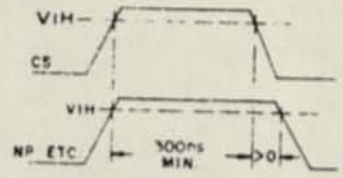


FIGURE 16a CS



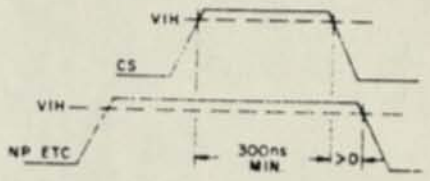
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

FIGURE 16b



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM

FIGURE 16c



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

FIGURE 17 SEROUT

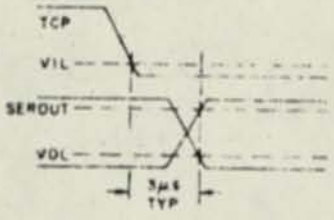


FIGURE 18 EOC TURN-ON

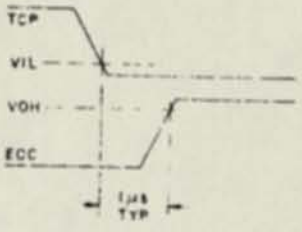


FIGURE 19 TBMT TURN-OFF

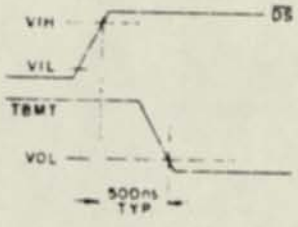


FIGURE 20 EOC TURN-OFF

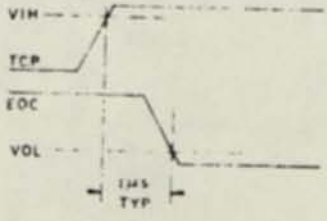


FIGURE 21 TBMT TURN-ON

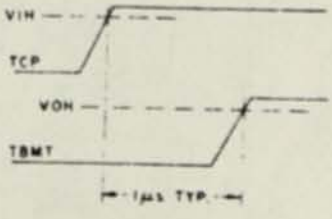


FIGURE 22 $\overline{RDE}$, $\overline{SWE}$

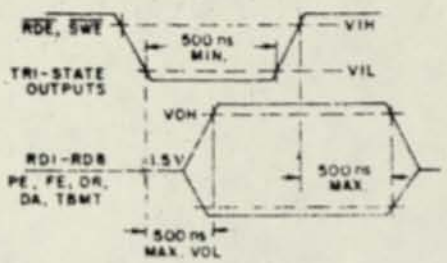


FIGURE 23 $\overline{RDAV}$

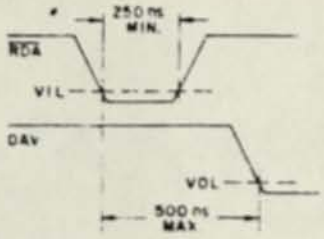


FIGURE 24 SHORT CIRCUIT OUTPUT CURRENT

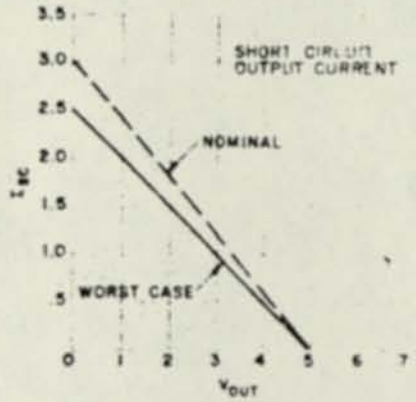


FIGURE 25 RD1–RD8, PE, FE, OR, TBMT, DAV

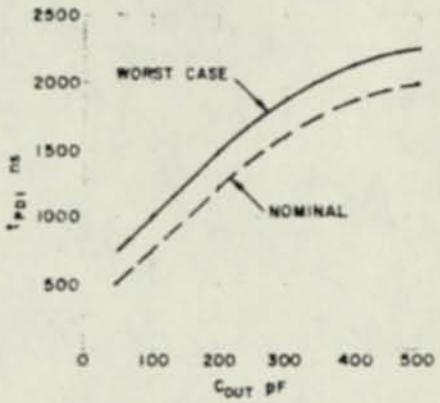


FIGURE 26a –12 VOLT SUPPLY CURRENT

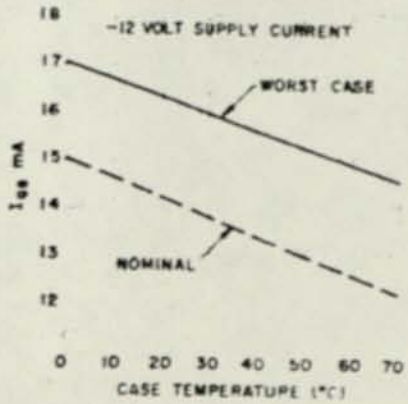
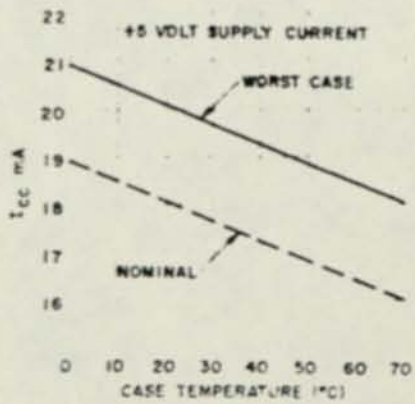


FIGURE 26b +5 VOLT SUPPLY CURRENT



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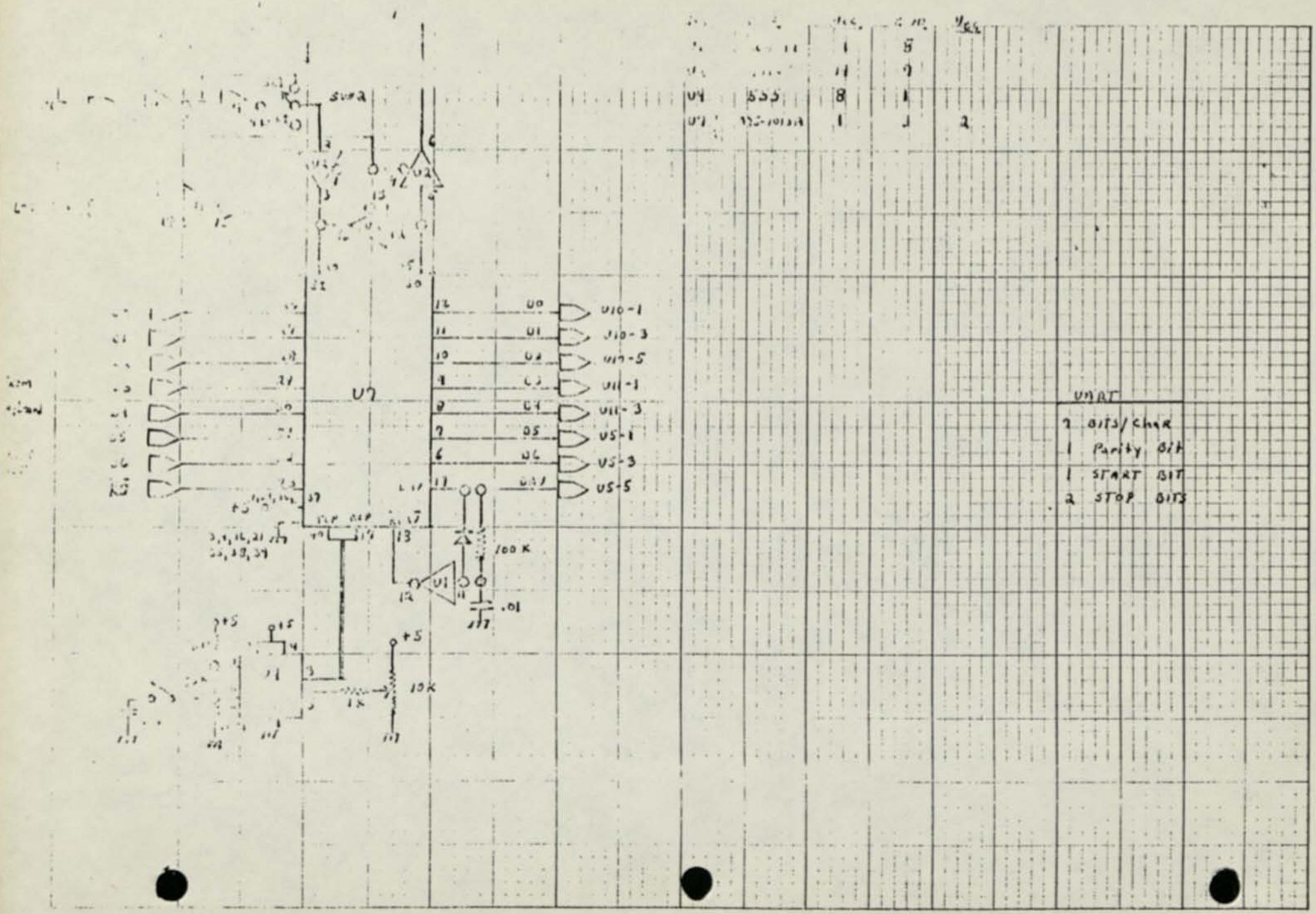

SW#2
U2
U7
U0
U1
U2
U3
U4
U5
U6
U7
U10-1
U10-3
U10-5
U11-1
U11-3
U5-1
U5-3
U5-5
100 K
.01
+5
10K
UART
7 BITS/CHAR
1 Parity BIT
1 START BIT
2 STOP BITS

AY-5-1013/AY-5-1013A

UAR/T UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

GIANT

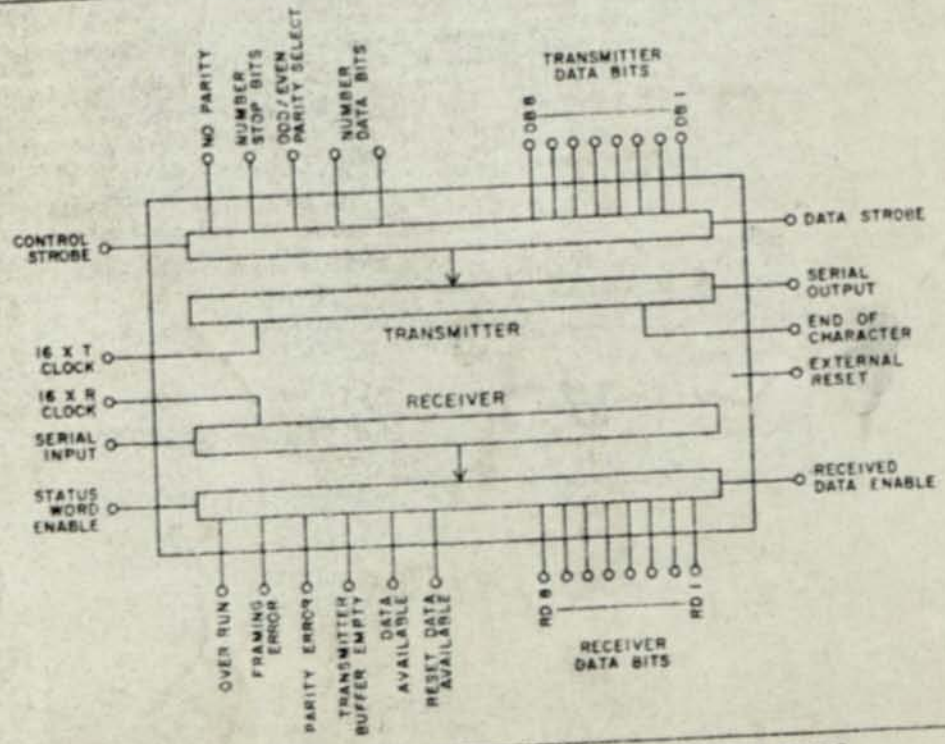
FEATURES

- DTL and TTL Compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple baud rates (receiving-transmitting) simultaneously.
- Start Bit Verification—decreases error rate with center sampling.
- Receiver center sampling of serial input; 46% distortion immunity.
- External reset of error flags.
- High Speed Operation—greatest through-put: 30k baud (AY-5-1013), 40k baud (AY-5-1013A).
- Tri-State Outputs—bus structure capability.
- Low Power—minimum power requirements.
- Input Protected—eliminates handling problems.
- Hermatic DIP Package—easy board insertion and mechanical handling.

GENERAL DESCRIPTION

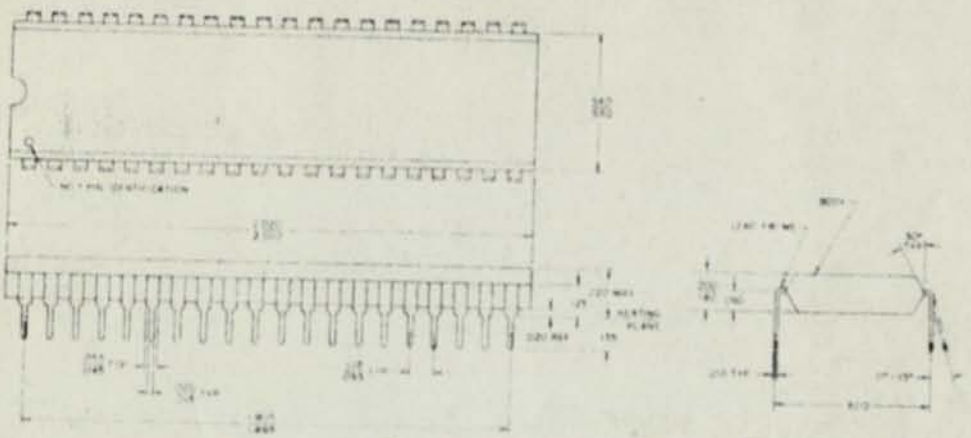
The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud rate, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL logic without the need for interfacing components and with all strobed outputs having tri-state logic.

FIGURE 1
BLOCK DIAGRAM



PIN CONFIGURATION

PACKAGE: 40 LEAD PLASTIC DUAL IN-LINE



All dimensions in inches

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	V_{CC} Power Supply	V_{CC}	+5V Supply
2	V_{GG} Power Supply	V_{GG}	−12V Supply
3	Ground	V_{GI}	Ground
4	Received Data Enable	$\overline{RDE}$	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits	RD8-RD1	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error	PE	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error	FE	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run	OR	This line goes to a logic "1" is the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable	$\overline{SWE}$	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	Reset Data Available	$\overline{RDAV}$	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available	DAV	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 13.

Pin No.	Name	Symbol	Function
20	Serial Input	SI	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 12, 13.
21	External Reset	XR	Resets shift registers. Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty	TBMT	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 29, 21.
23	Data Strobe	$\overline{DS}$	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of $\overline{DS}$. Data must be stable during entire strobe.
24	End of Character	EOC	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 18, 20.
25	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 17.
26-33	Data Bit Inputs	DB1-DB8	There are up to 8 data bit input lines available.
34	Control Strobe	CS	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity	NP	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits	TSB	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.
37-38	Number of Bits/Character	NB2, NB1	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select	EPS	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

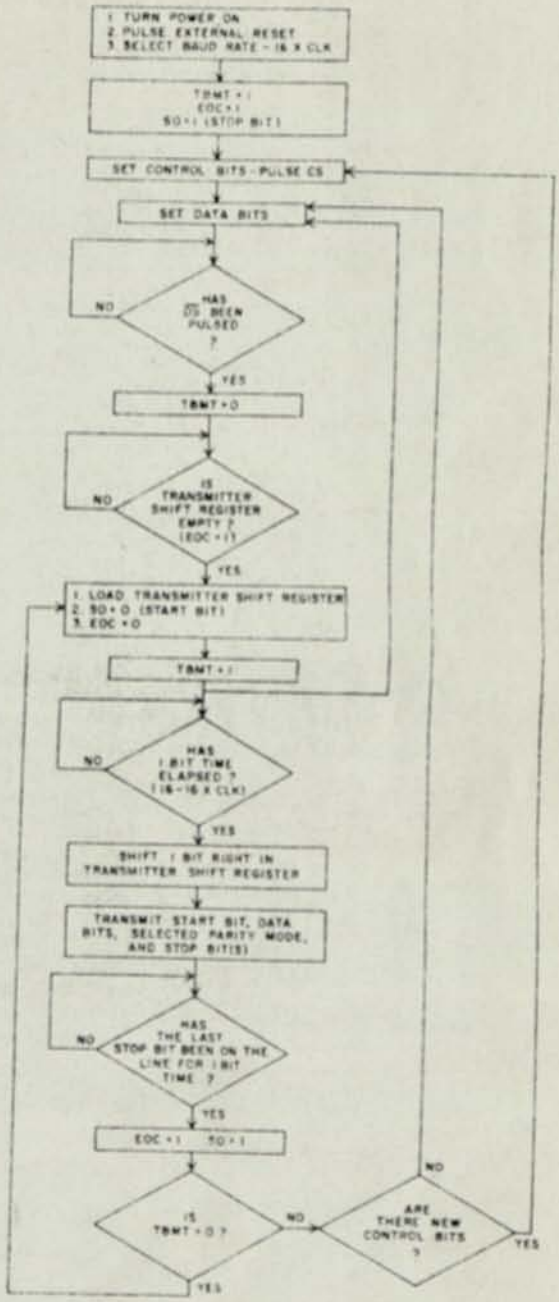
TRANSMITTER OPERATION
FIGURE 2

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occuring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.



RECEIVER OPERATION
FIGURE 3

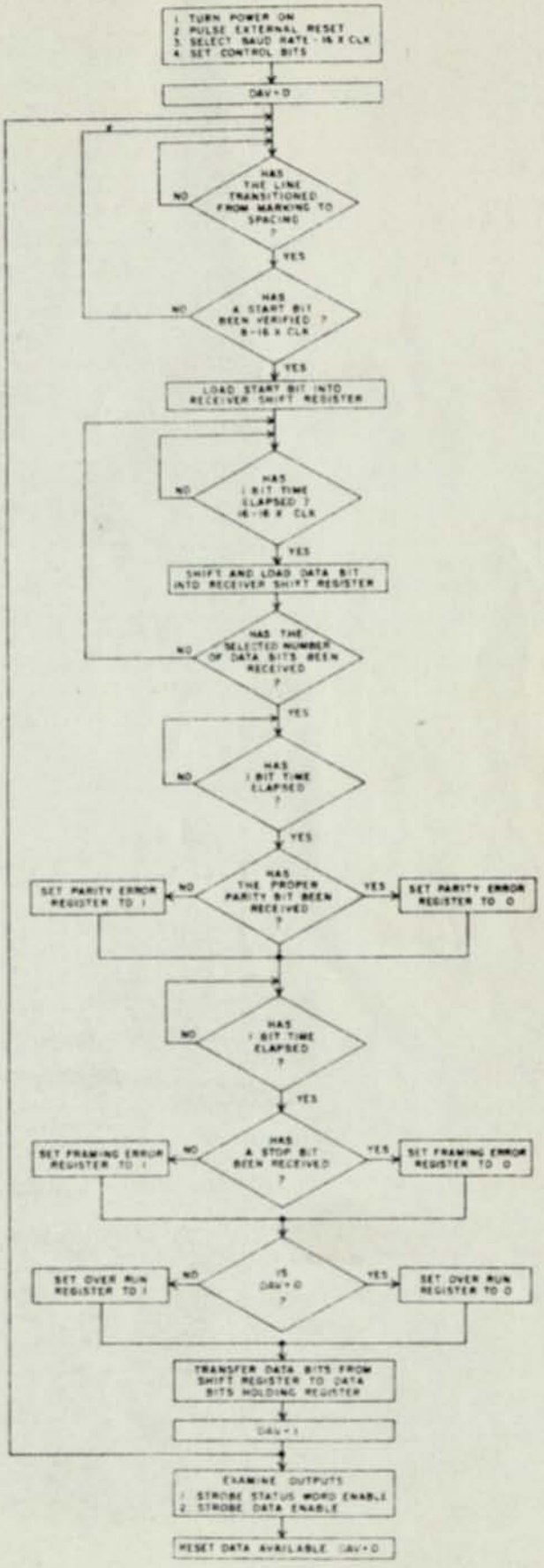
Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DAV) to a logic "0".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{GG} (with respect to V_{CC})	−20 to +0.3V
Clock and logic input voltages (with respect to V_{CC})	−20 to +0.3V
Storage Temperature	−65°C to 150°C
Operation Temperature	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	330°

STANDARD TEST CONDITIONS

The following characteristics apply for any combination of the following test conditions, unless otherwise noted. All voltages are measured with respect to ground. Positive current is defined as flowing into the referenced pin.

$V_{GG} = -12V \pm 5\%$ $V_{CC} = 5V \pm 5\%$ $0°C < T_A < 70°C$

ELECTRICAL CHARACTERISTICS (see standard conditions)

PARAMETER	CONDITIONS AND COMMENTS	MIN.	TYP.	MAX.	UNITS
Input Logic Levels					
Logic 0	V_{IL} (I_{IL} = −1.6mA max.)	0	–	0.8	volts
Logic 1	V_{IH} Unit has internal pullup resistors	V_{CC}−1.5	–	V_{CC}+0.3	volts
Input Capacitance					
All Inputs	0 volts bias, f = 1MHz	–	–	20	pF
Leakage Currents					
Tri-State Outputs	0 volts	–		1.0	μA
Data Output Levels					
Logic 0	I_{OL} = 1.6mA (sink)	–	–	+0.4	volts
Logic 1	I_{OH} = −.3mA (source)	V_{CC}−1.0			volts
Output Capacitance		–	10	15	pF
Short Ckt. Current	See Fig. 24	–	–	–	–
Power Supply Current					
I_{GG} 25°C, all inputs +5V	See Fig. 26a	–	14	16	mA
I_{CC}	See Fig. 26b	–	18	20	mA
A.C. CHARACTERISTICS	T_A = 25°C, Output load capacitance 50pF max.				
Clock Frequency					
AY-5-1013		DC	–	480	kHz
AY-5-1013A		DC	–	640	kHz
Baud Rate					
AY-5-1013		0	–	30	k baud
AY-5-1013A		0	–	40	k baud
Pulse Width					
Clock Pulse	AY-5-1013 See Fig. 10	1.0	–	–	μs
	AY-5-1013A See Fig. 10	750	–	–	ns
Control Strobe	See Fig. 16	300	–	–	ns
Data Strobe	See Fig. 15	190	–	–	ns
External Reset	See Fig. 14	500	–	–	ns
Status Word Enable	See Fig. 22	500	–	–	ns
Reset Data Available	See Fig. 23	250	–	–	ns
Received Data Enable	See Fig. 22	500	–	–	ns
Set Up & Hold Time					
Input Data Bits	See Fig. 15	>0	–	–	ns
Input Control Bits	See Fig. 16	>0	–	–	ns
Output Propagation Delay					
TPD0	See Fig. 22 & 25		–	500	ns
TPD1	See Fig. 22 & 25		–	500	ns

FIGURE 4 TRANSMITTER–BLOCK DIAGRAM

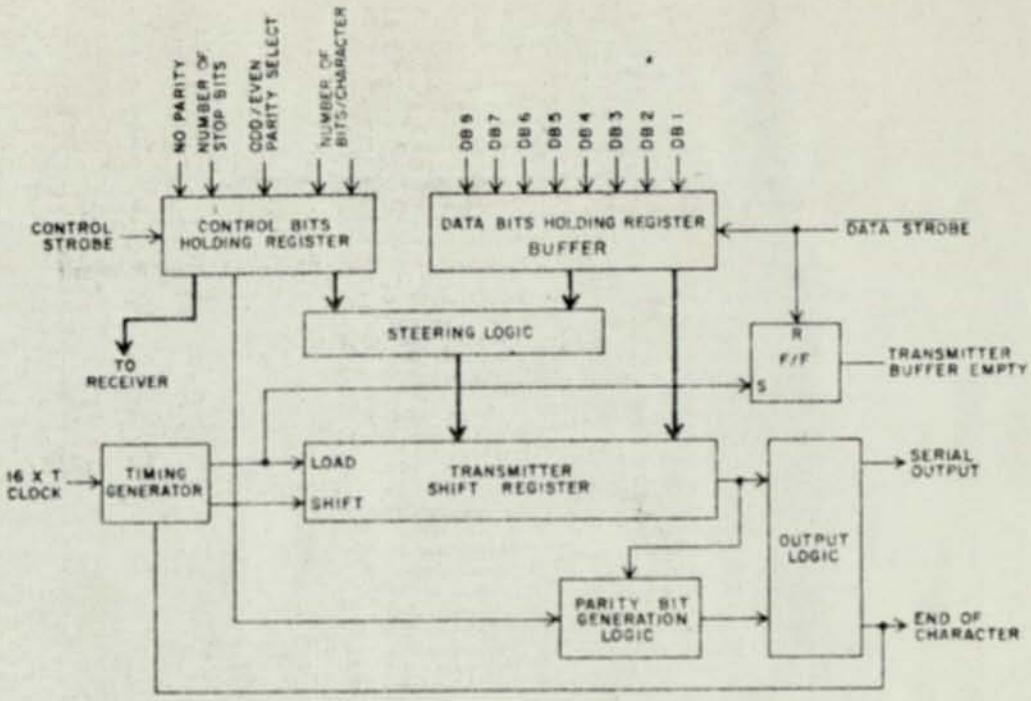


FIGURE 5 RECEIVER–BLOCK DIAGRAM

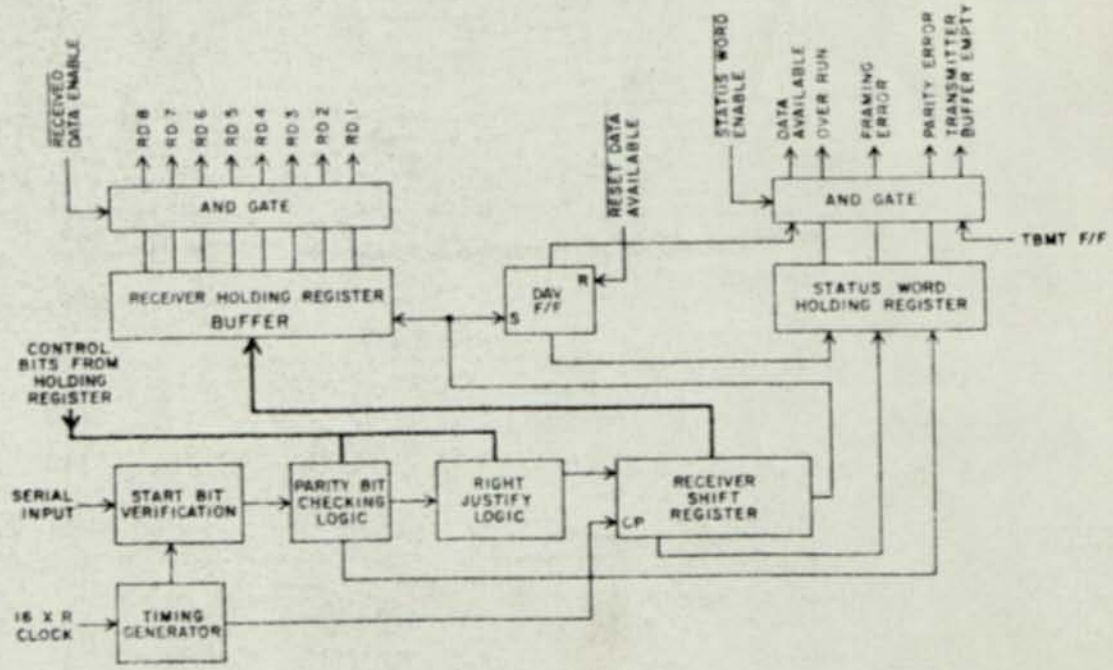
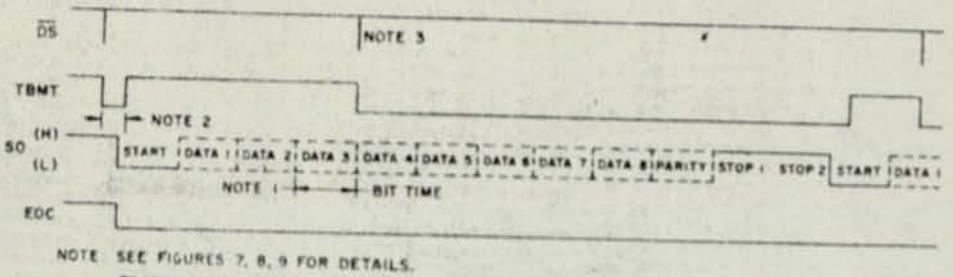


FIGURE 6 UAR/T–TRANSMITTER TIMING



NOTE SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

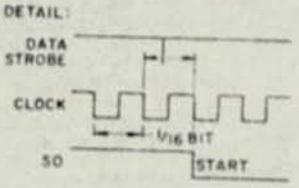


FIGURE 7 TRANSMITTER AT START BIT

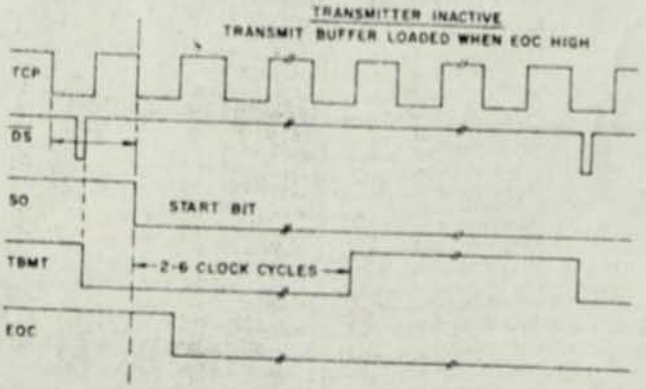


FIGURE 8 TRANSMITTER AT START BIT

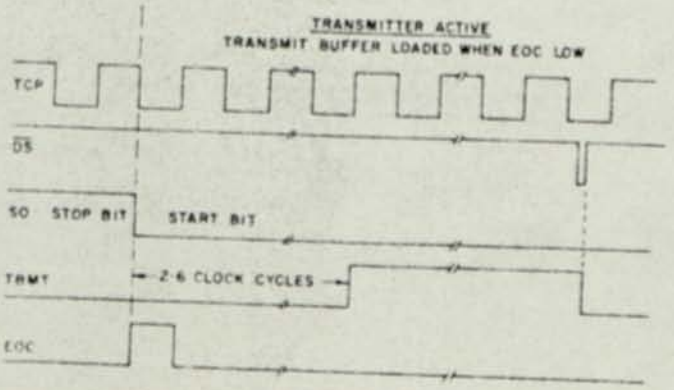


FIGURE 9 ALLOWABLE POINTS TO USE CONTROL STROBE

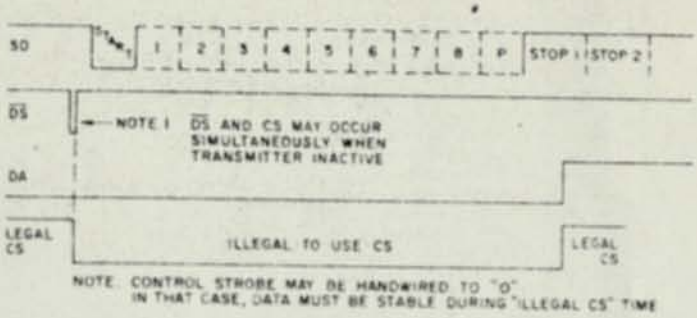


FIGURE 10 ALLOWABLE TCP, RCP

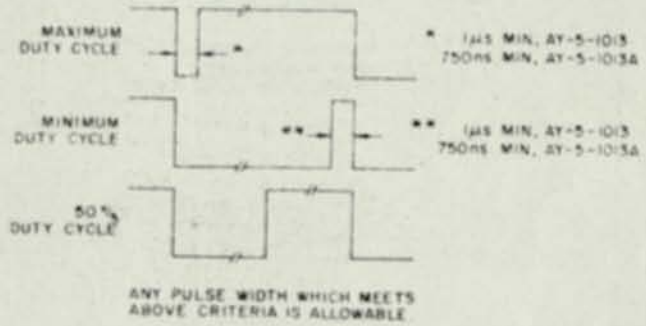
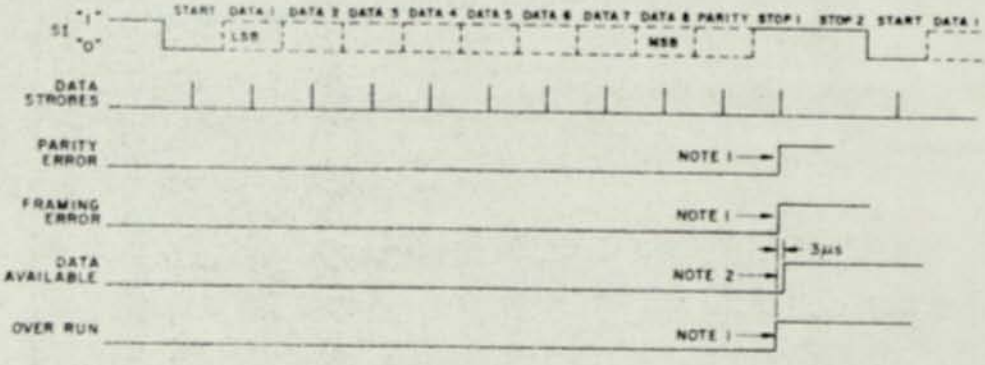


FIGURE 11 UAR/T–RECEIVER TIMING



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE OUTPARTED, IF ERROR OCCURS
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*, THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

FIGURE 12

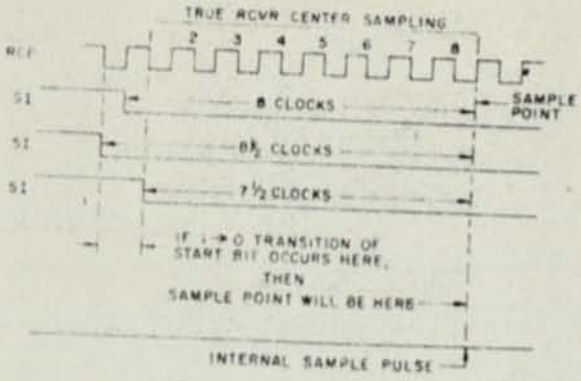


FIGURE 13 RECEIVER DURING 1st STOP BIT

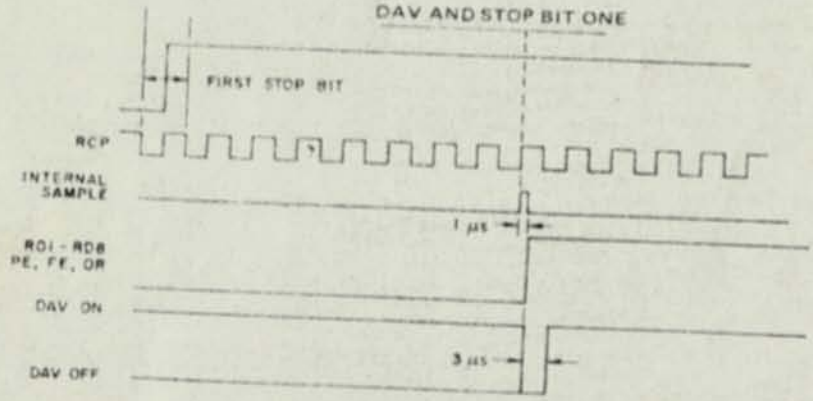
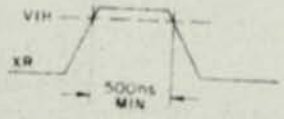


FIGURE 14 XR PULSE



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER. RECEIVED DATA SO, TBMT, EOC ARE RESET TO 5V. ALL OTHER OUTPUTS RESET TO 0V.

FIGURE 15 $\overline{DS}$

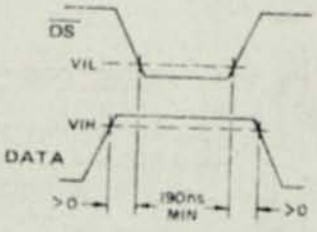
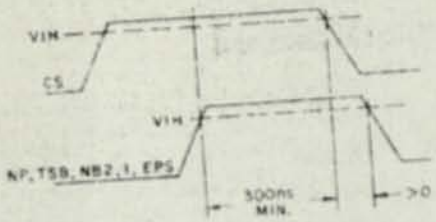
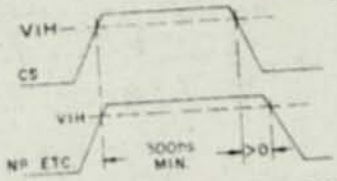


FIGURE 16a CS



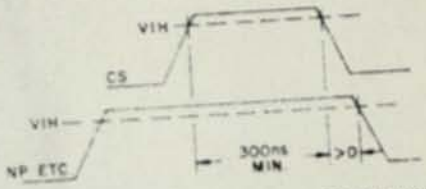
CONTROL BITS MUST BE STABLE FOR LAST 500ns OF CS.

FIGURE 16b



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM.

FIGURE 16c



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

FIGURE 17 SEROUT

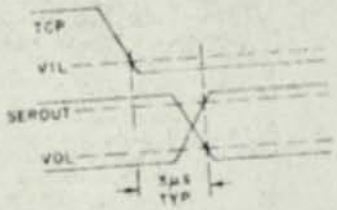


FIGURE 18 EOC TURN-ON

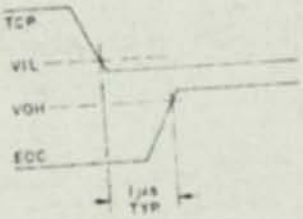


FIGURE 19 TBMT TURN-OFF

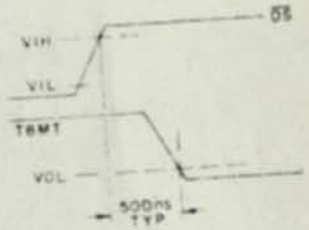


FIGURE 20 EOC TURN-OFF

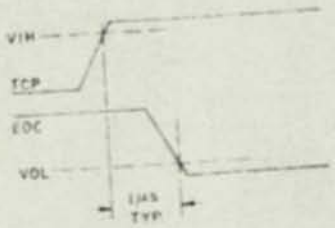


FIGURE 21 TBMT TURN-ON

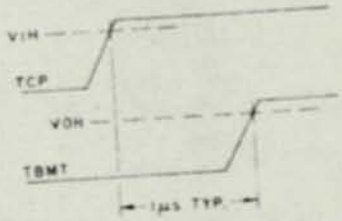


FIGURE 22 $\overline{RDE}$, $\overline{SWE}$

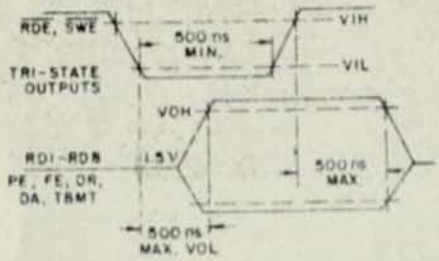


FIGURE 23 $\overline{RDAV}$

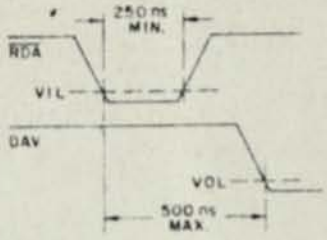


FIGURE 24 SHORT CIRCUIT OUTPUT CURRENT

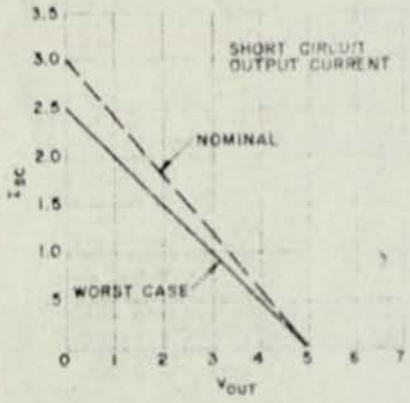


FIGURE 25 RD1–RD8, PE, FE, OR, TBMT, DAV

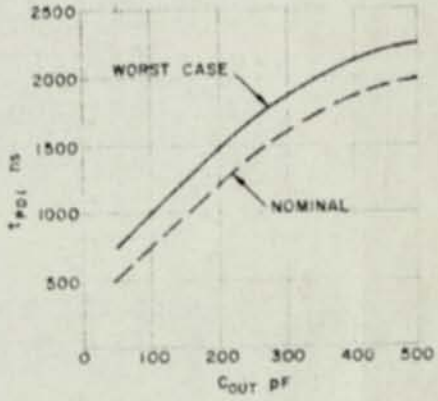


FIGURE 26a –12 VOLT SUPPLY CURRENT

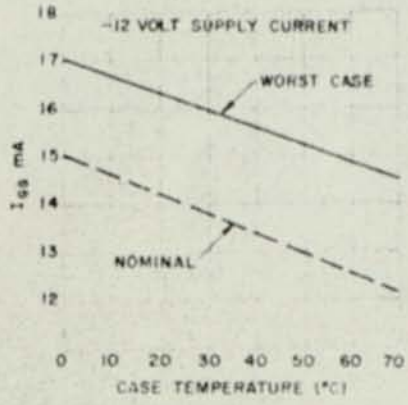
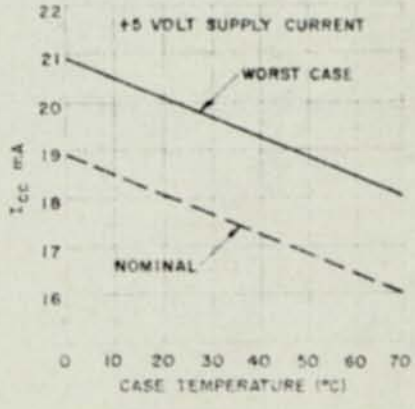


FIGURE 26b +5 VOLT SUPPLY CURRENT



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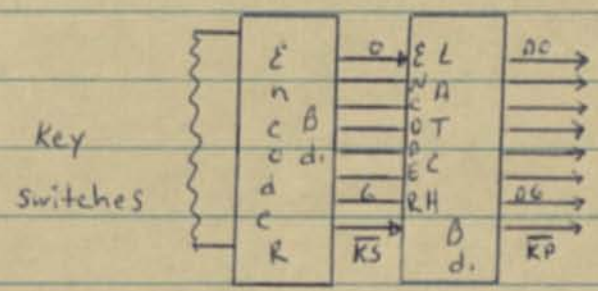
NERAL INSTRUMENT FRANCE SA, 11-13 Rue Gordon, 75-Paris 13eme, France, Tel: 588 74 31
NERAL INSTRUMENT DEUTSCHLAND GMBH, Hauptmarkten Strasse 61, 8 Munich 80, West Germany, Tel: 452238/450181
NERAL INSTRUMENT INTERNATIONAL CORP., Fukuda Building No. 17, Shiba Fukudacho, Minato-ku, Tokyo 105, Japan, Tel: (03) 437-0761
NERAL INSTRUMENT OF TAIWAN LTD., P.O. Box 23226, Taipei, Taiwan, Tel: 833861-3

Keyboard

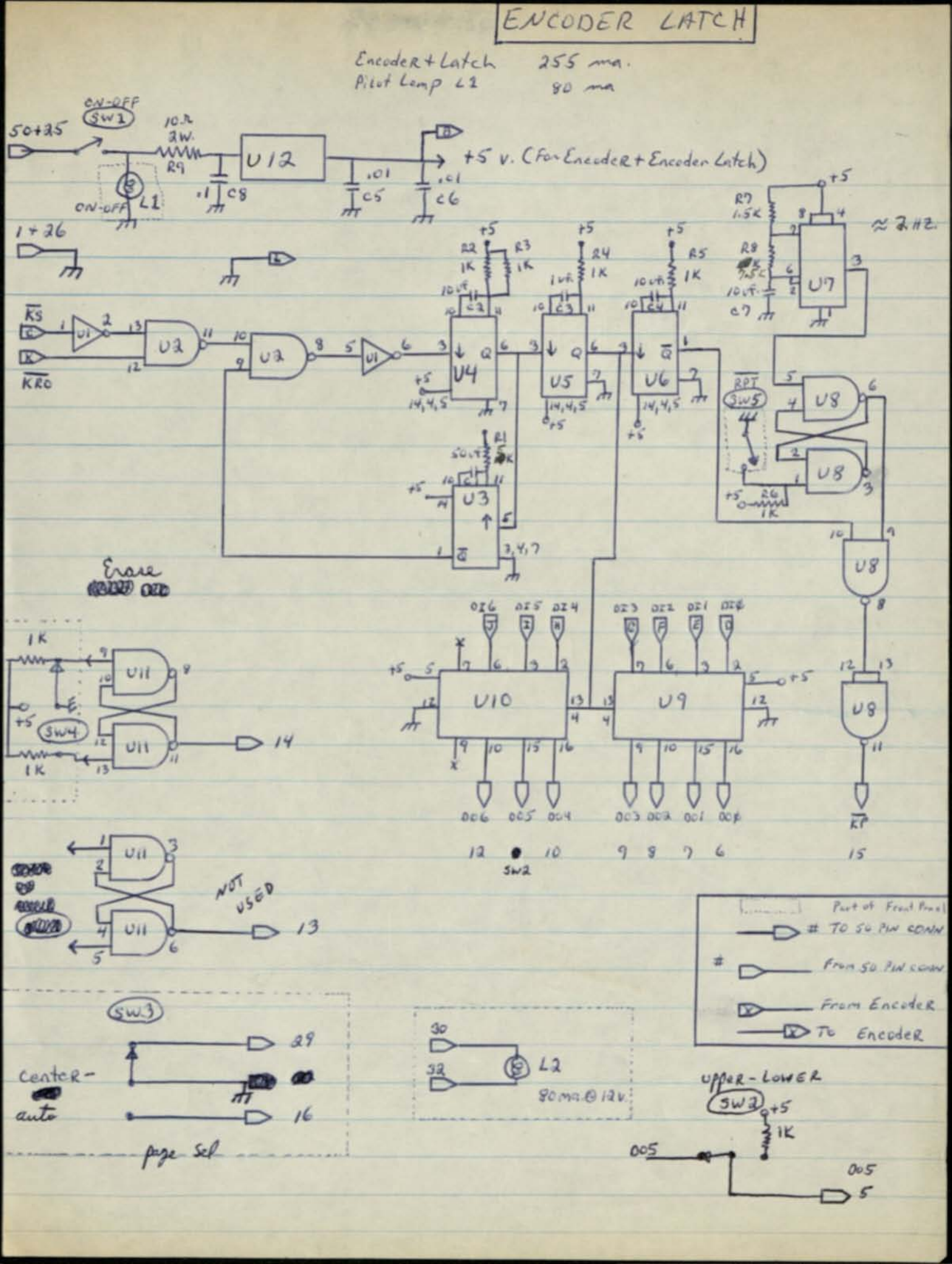
and

Encoder (w/ Latch)

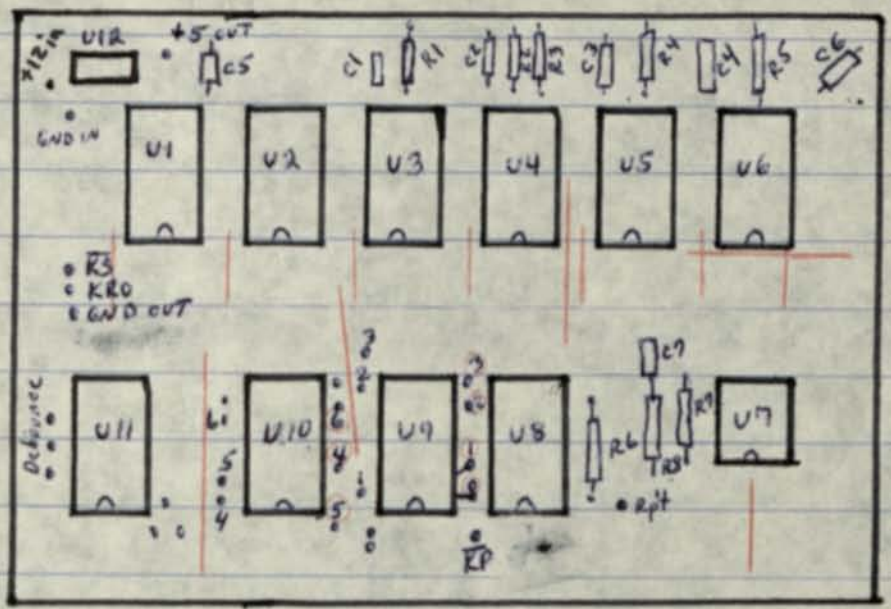


ENCODER LATCH

Encoder + Latch 255 ma.
Pilot Lamp L2 80 ma



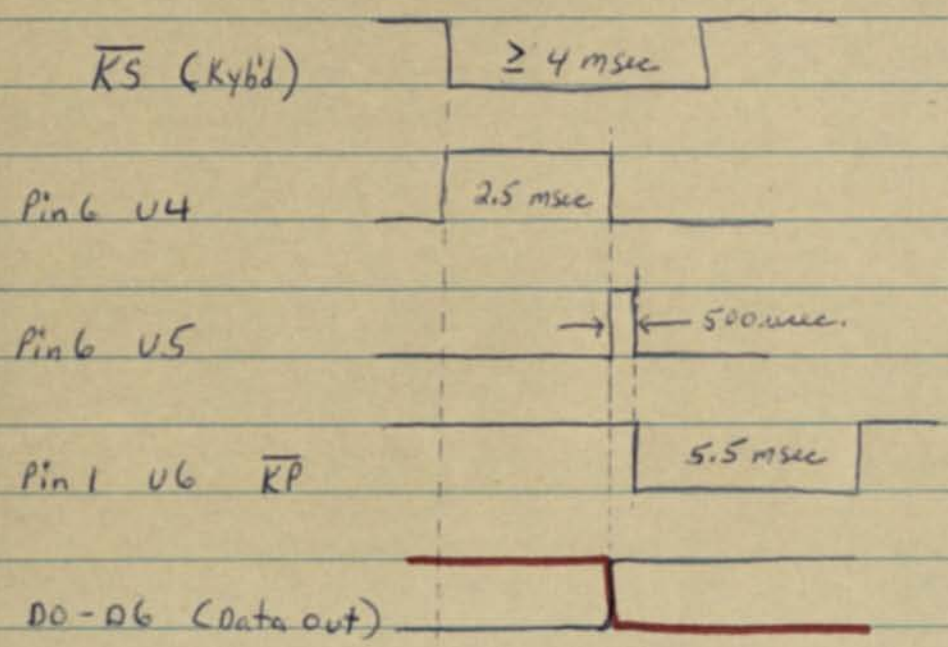
ENCODER LATCH



1-6 D0-D6 IN

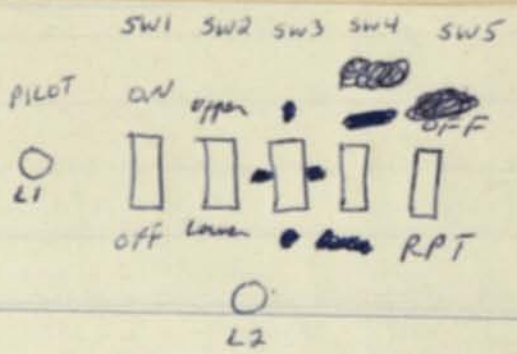
1-6 D0-D6 OUT

ENCODER LATCH

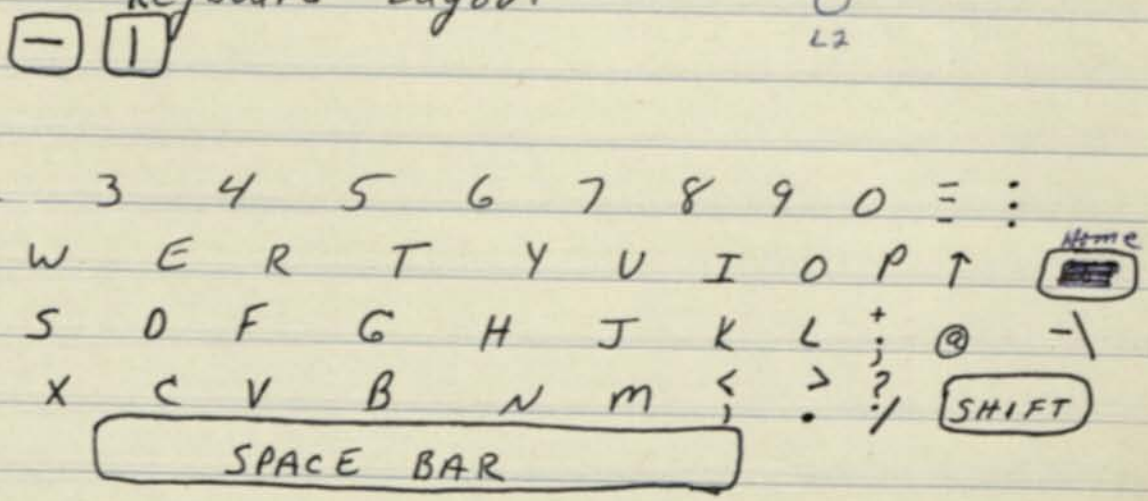


pins 14, 15, 10, 9 U9

Pins 14, 15, 10 U10



Keyboard Layout

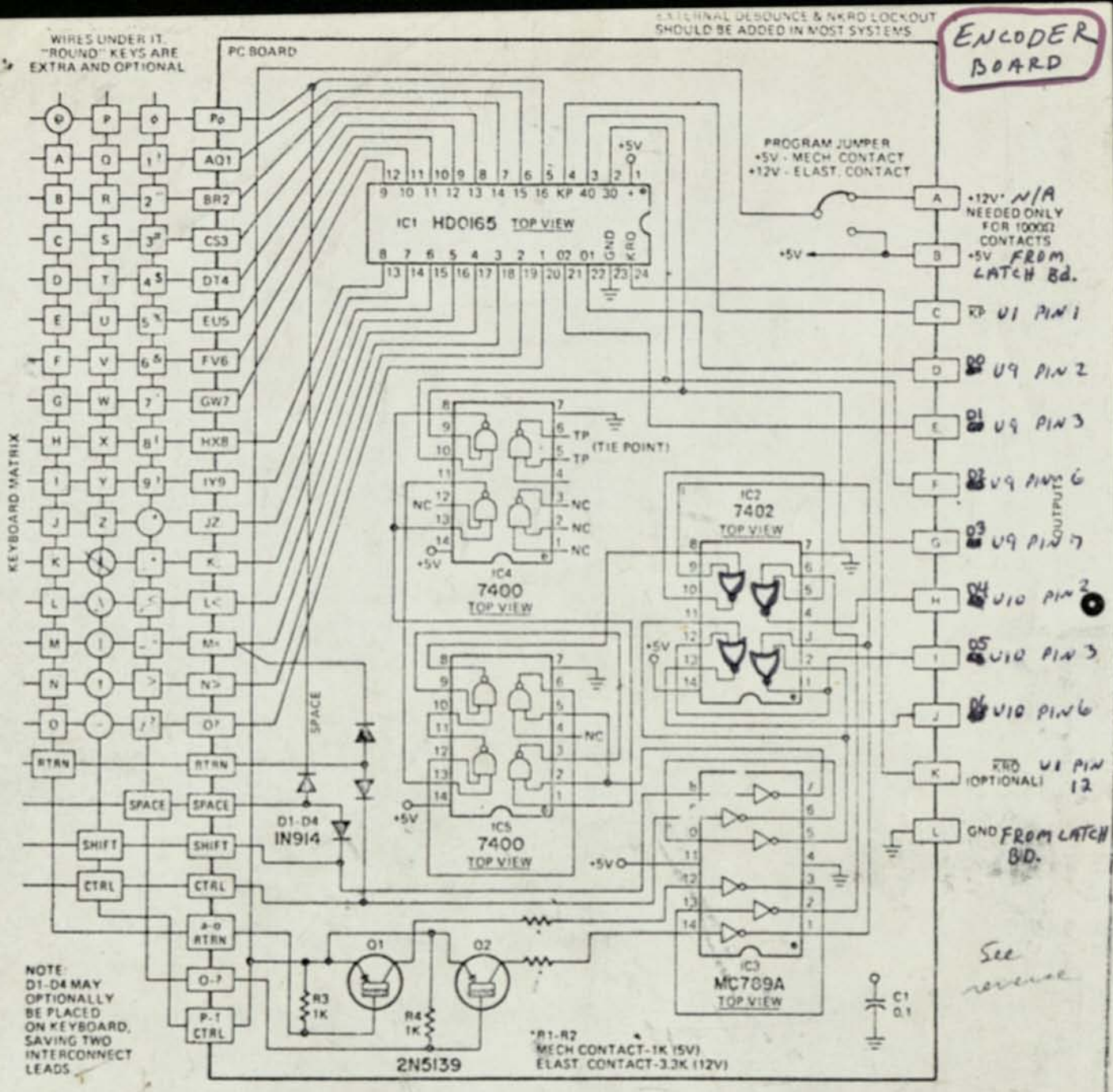


Parts LIST FOR ENCODER LATCH

U1	7404
U2,8,11	7400
U3,4,5,6	74121
U7	555
U9,10	7475
U12	7805

R1	10K||10K ¼w
R2	1K ¼w
R3	1K ¼w
R4	1K ¼w
R5	1K ¼w
R6	1K ¼w
R7	1.5K ¼w
R8	15K||15K ¼w
R9	10Ω 2w

C1	50 ufd. 10v.
C2	10 ufd. 10v.
C3	1 ufd.
C4	10 ufd. 10v.
C5	.01 50v.
C6	.01 50v.
C7	10 ufd. 10v.
C8	.1 ufd. 100v.



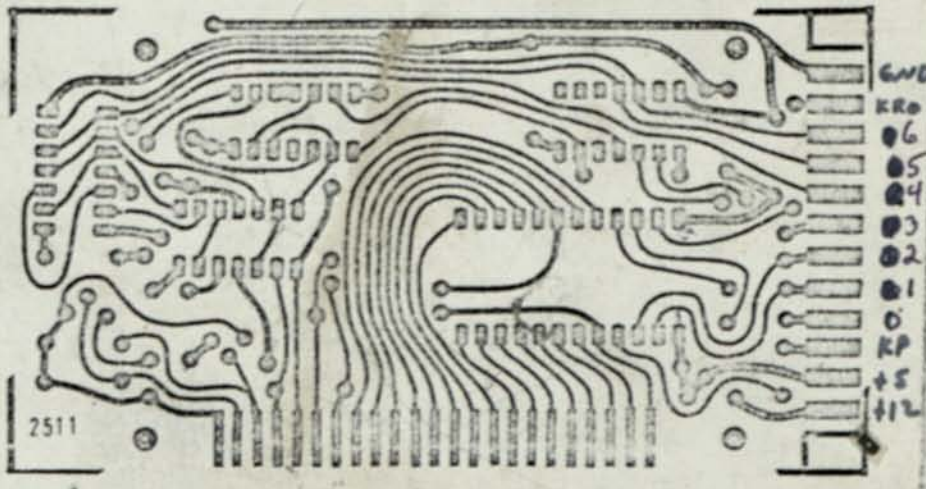


FIG. 1—ASCII ENCODER CIRCUIT (top) is easy to build. FULL SIZE FOIL PATTERN (above) is for the circuit board. PARTS LAYOUT (right) shows where to mount the components on the circuit board.

1PARTS LIST

C1—0.1-μF disc ceramic, Mount *flat*.
D1, D2, D3, D4—1N914 or equivalent silicon computer diode
IC1—HD0165 Encoder (Harris)
IC2—7402 TTL Quad NOR gate
IC3—MC789AP Hex Inverter, RTL, do not substitute
IC4, IC5—7400 TTL Quad NAND gate
Q1, Q2—2N5139, silicon pnp
R1, R2—Varies with keyboard, 1000 ohms for mechanical contacts and +5 supply; 3300 ohms for elastomeric high resistance contacts and +12 supply.
R3, R4—1000 ohms, ¼-watt carbon

MISC: PC Board, Solder; No.24 Solidereeze wire, 20 feet for keyboard wiring, sleeving, No.24 solid wire jumpers.

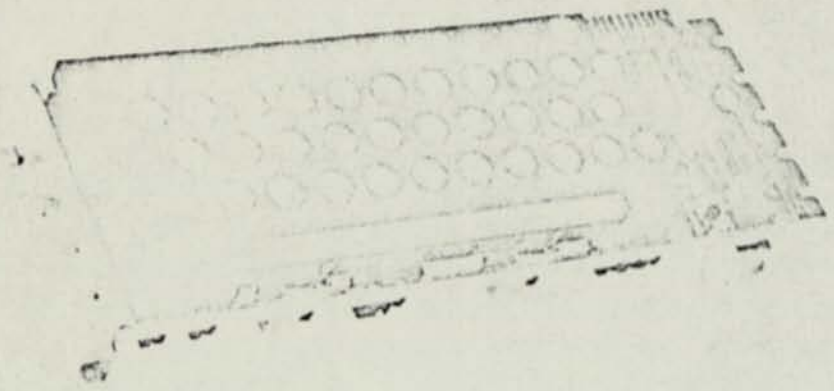
NOTE: The following is available from Southwest Technical Products, 219 West Rhapsody, San Antonio, Texas, 78216

PC Board, etched and drilled: $5.75.

need no new keys for the control commands, unless we are really going to use that command often. CARRIAGE RETURN is often used, so, it's handy to have a special key that *simultaneously* gives us a CONTROL and a M command. Similarly, we can get a spacebar by simultaneously giving a SHIFT and a 0 command. Other special functions (DELETE, ESCAPE, ALT MODE, etc. . . .) are easily added in the same way.

To decide when a code is sent, a keypressed command is given when a key is *deliver* a keypressed command for the shift or control key, for they are always used in conjunction with another key. And, in our circuit, we get a free "there's two keys pressed!" output that can be used to tell whatever is on the other end that the typist is running too fast or just made a mistake and please ignore what just arrived. One final, and slightly messy detail involves the > = < and ? keys. Normally, we like to type commas, dashes, periods, and slashes *without* shifting, and save the question, *shifted* commands. This is clearly backwards from the standard code. So if we are going to go along with the standard code (often we are forced to because of the keytops on the keyboard we're going to use), we have to arrange the shift key so that it operates *backwards* on these four keys. All this takes are two 2½ IC's, but this is a complex and painful little detail to resolve.

The output of the code consists of seven bits in *parallel*, or all-at-once form. An eighth *parity* bit can optionally be added for error detection, or the seventh bit can optionally be dropped to get the 10-bit code that has only alphanumerics to run a character generator. Should we want to talk to a computer or a phone line, we have to convert this code to a *serial* form, easily done with either the circuit shown in the original article or with a new MOS terminal transmitter/receiver chip. Depending on the type of keyboard and the debouncing in the rest of the system, we may have to add a contact conditioning and debouncing system as well.



TYPICAL KEYBOARD WITH ENCODER. The small encoder board is mounted at the right end of the keyboard.

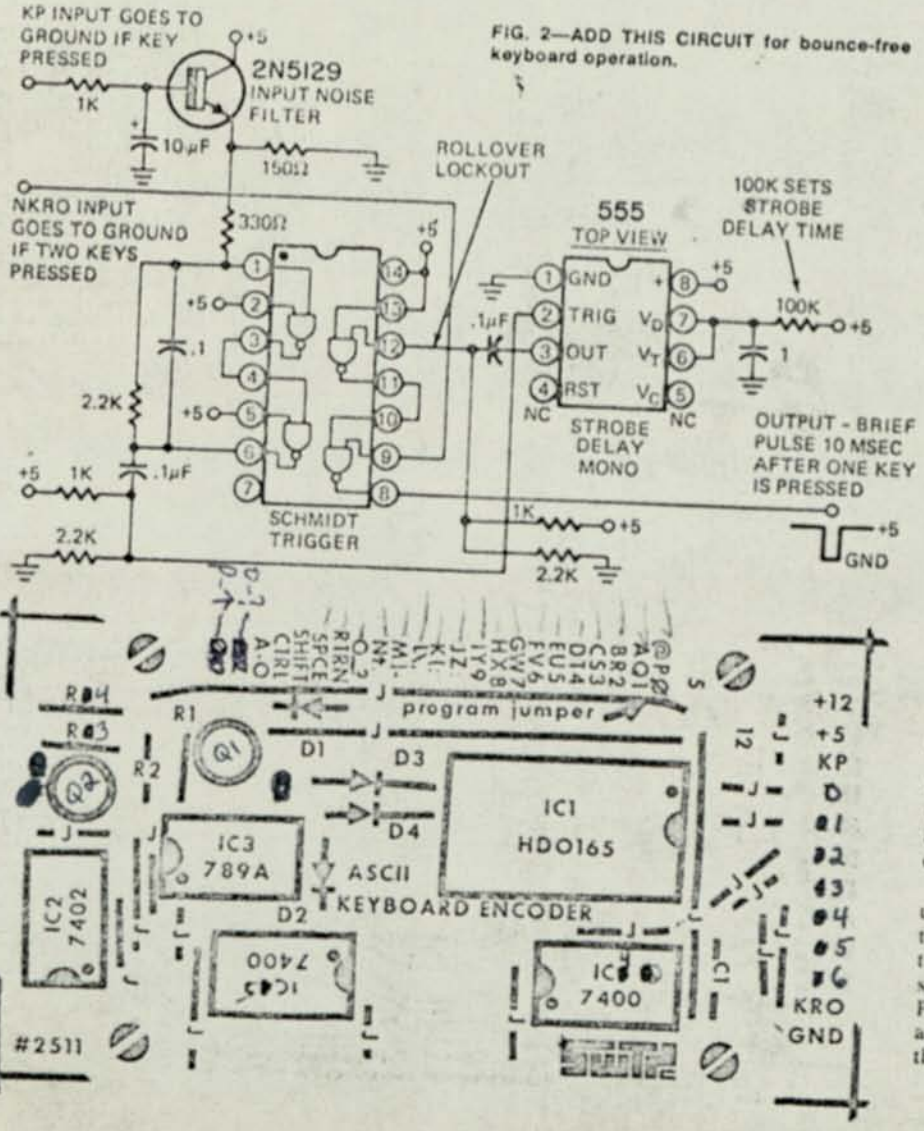


FIG. 2—ADD THIS CIRCUIT for bounce-free keyboard operation.

About the new circuit

The new circuit is shown in Fig. 1. Except for IC1 (presently around $7.50), all the remaining parts are nickel and dime stuff, and there are only 19 components in all. Just like the code of Table 1, we can split the problem into two parts, for the lower four bits couldn't care less what the upper three are doing, so long as everything ends up right. Thus a lower four bits 1101 code could be a carriage return, a group seperator (a very rare machine command), a dash or minus, an equals, a M, or a large unbracket. IC1 singlehandedly takes care of the lower four bits for us. It has sixteen input lines and four output lines. If you make any *one* (only one!) input line positive, it gives the binary equivalent to that code. Thus the third line generates a 0011, the eighth line a 1000, and so on.

The inputs are RTL style and simply need an impedance path to +5 or +12 to serve as an input command. Whatever *else* the input current flows through on the way to set up the upper three bits is of no concern to IC1, so long as the current gets there when it is needed. IC1 also generates a keypressed output that's high if all the inputs are low and goes low if any key is pressed. It also produces an optional output that goes low if two keys or more are simultaneously pressed. This is called a NKRO output, short for N-key-rollover.

It only takes about +3.5 volts to turn on an IC1 input. Since the input is current operated, we can either get our current from a low impedance (mechanical or reed) contact and a +5 supply, or from a higher impedance (elastomeric or foam) contact and a +12 supply. Around two milliamperes are needed, but it can handle much more than that safely. Thus, we can use virtually any kind of keyboard contact simply by picking one optional low current supply voltage.

So much for the lower four bits. The upper three bits are generated by responding to *what* the IC1 input current is routed through on the way down from the positive supply. If it goes through nothing, we set up P-Z. If it goes through Q1, we set up A-O, and if it goes through Q2, we set up zero through 9 and the related punctuation. The

(continued on page 92)

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS-INTERTYPE CORPORATION

HD-0165

Keyboard Encoder

ORIGINAL

DIGITAL DATA

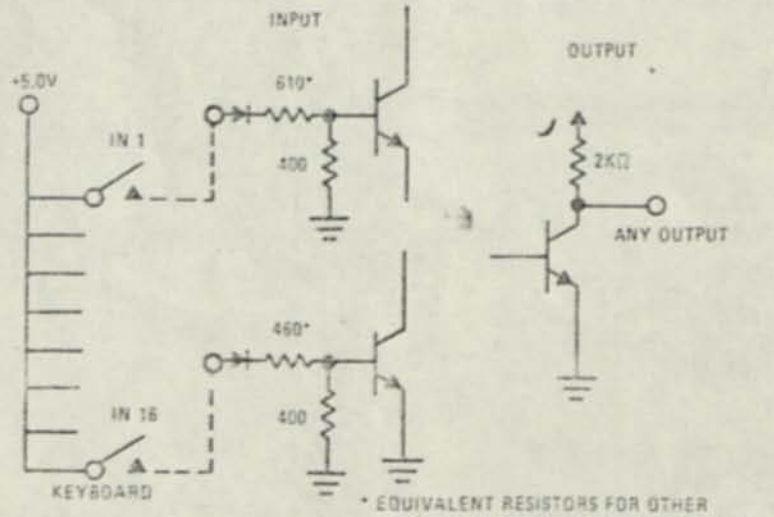
FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED, DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual in-line package and operates over the temperature range of 0°C to +75°C.

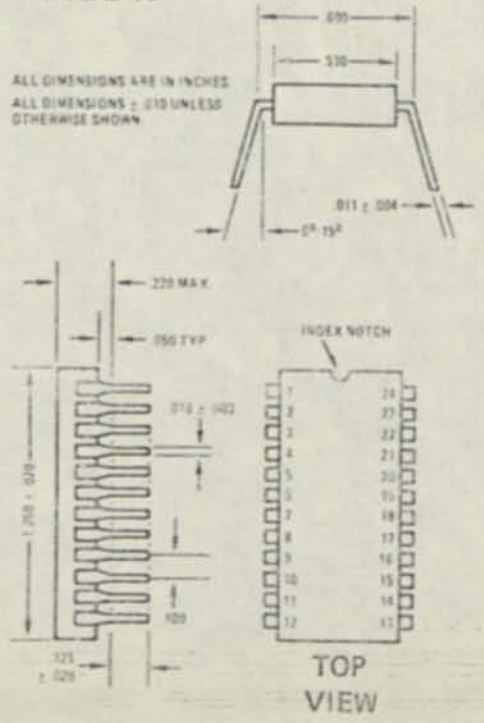
EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

PACKAGE

CODE 1J



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^0 to $+150^0$C
Output Voltage	+5.5V	Operating Temperature (Case)	0^0C to $+75^0$C

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^0C$ to $+75^0C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
					+0.4		$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
	Output Voltage "1"	V_{OH}	+2.4	+4.0			V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^0C$ $V_{CC} = V_{IN} = +5.0V$ $C_L < 50pF$

NOTE (1) Skew time is the maximum time differential between propagation delay times of any outputs including strobe and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS L = Open Circuit or < +1.0V H = > +4.3V Current Source
OUTPUTS L = < +0.4V H = > +2.4V X = Erroneous Data

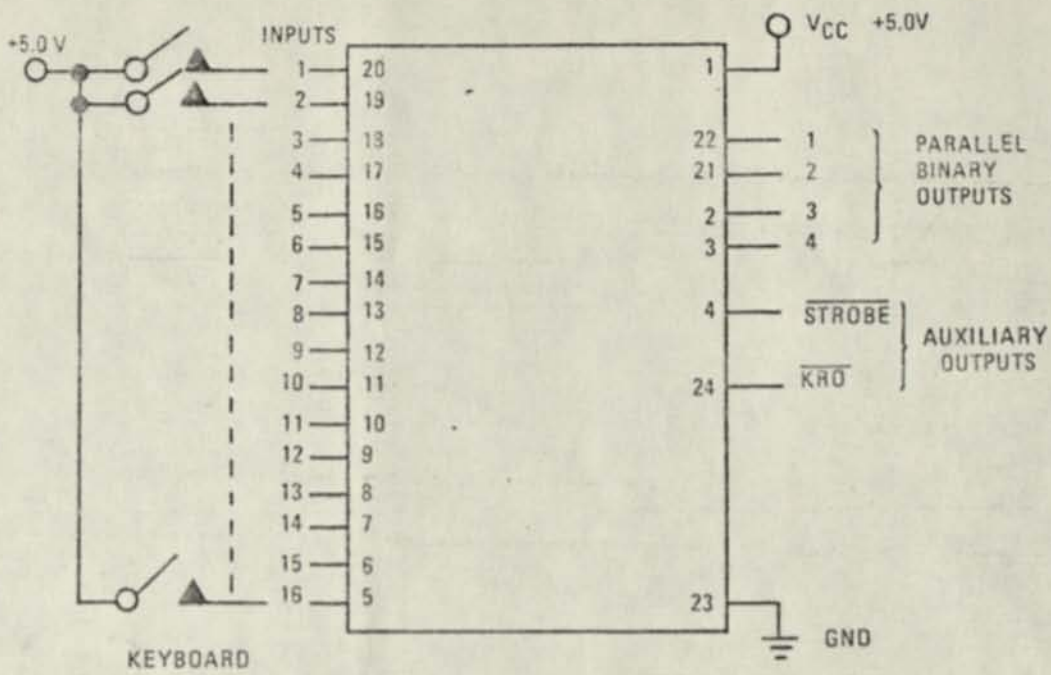


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

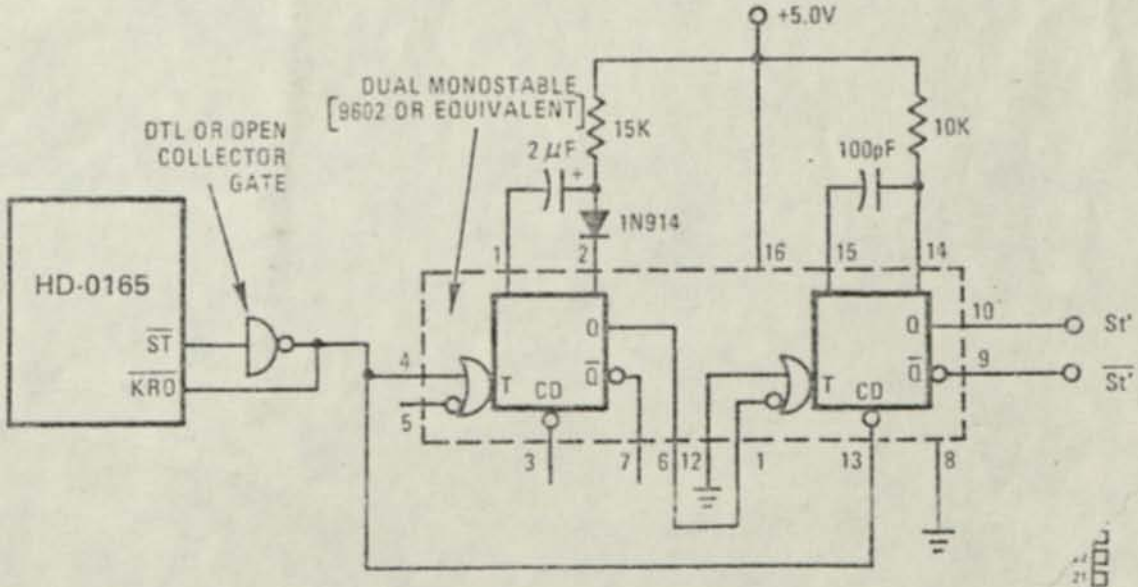
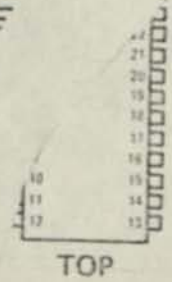


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.



TOP VIEW

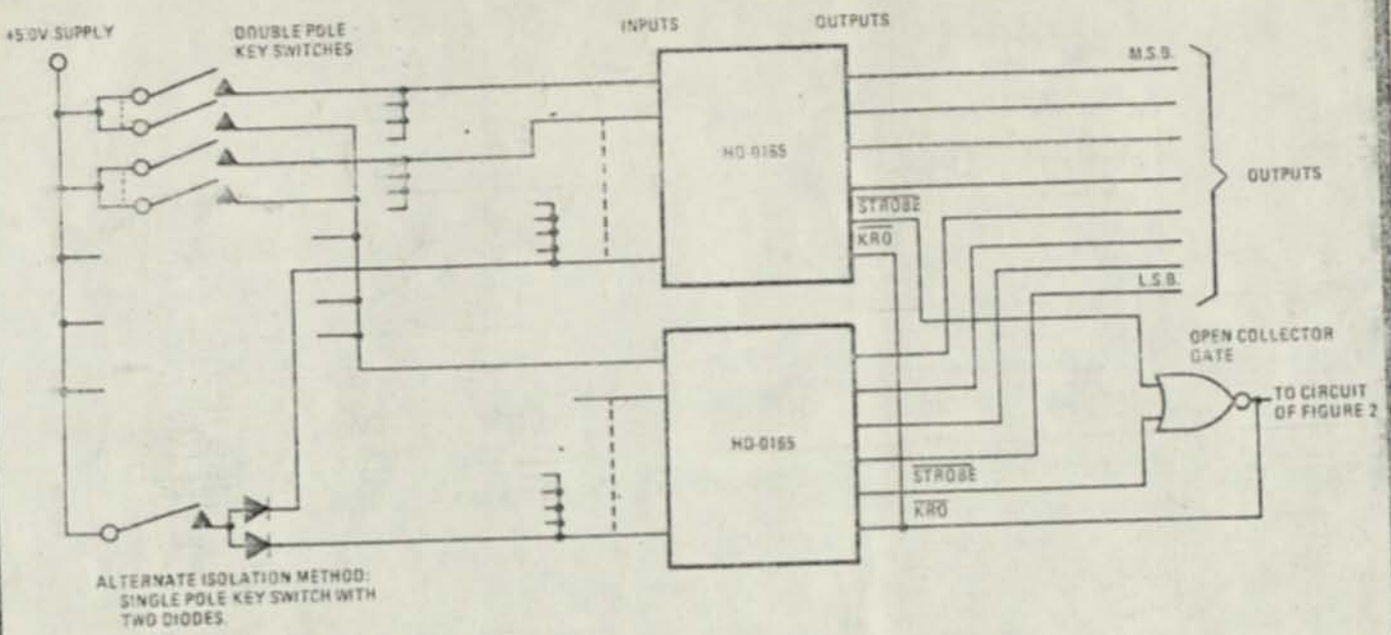


Figure 3. ENCODING UP TO 256 KEYS

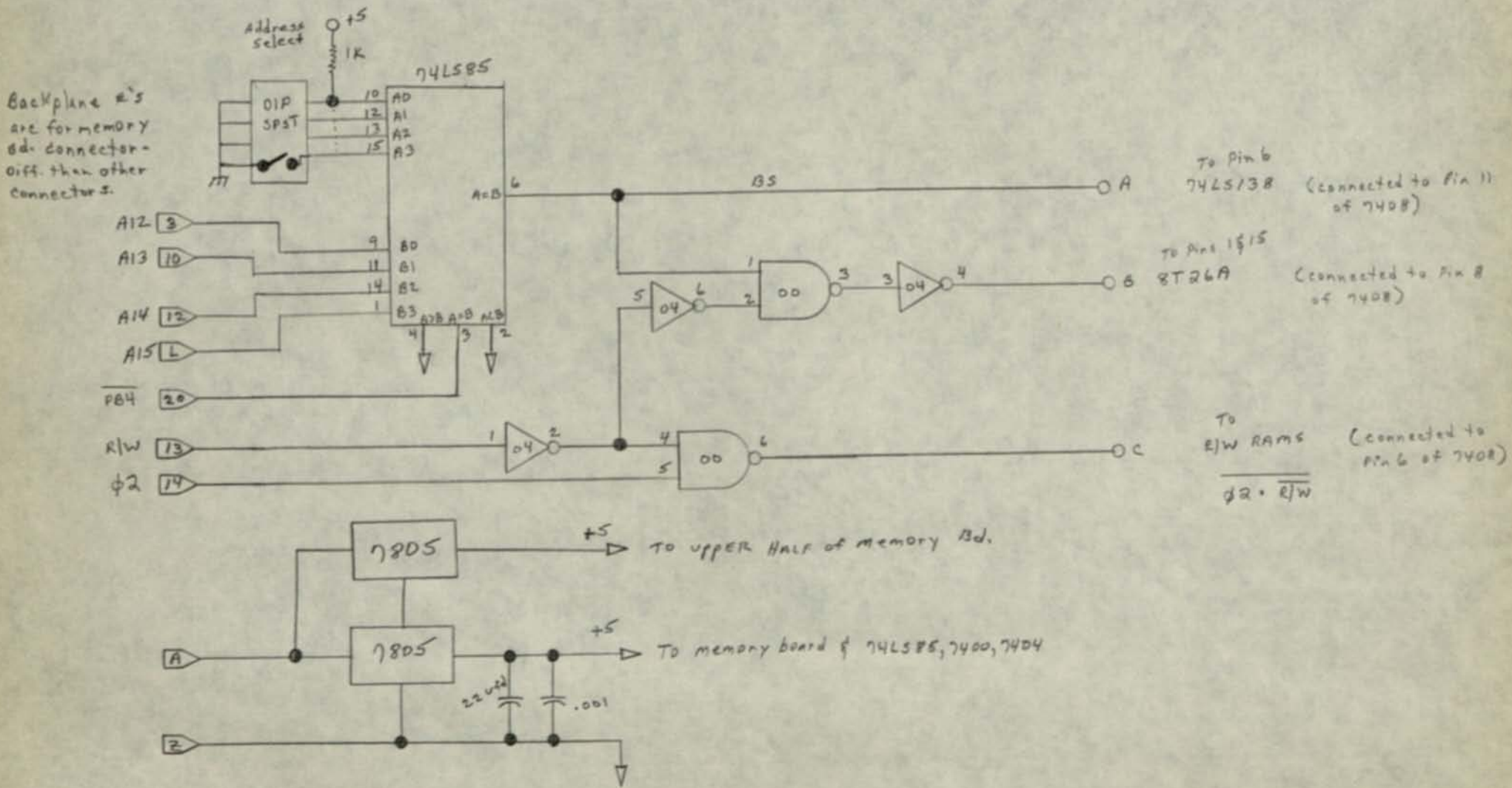
Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

L
L
L L
L L
L L
L L L
ANY TWO O

INPUTS L
OUTPUTS L

Memory



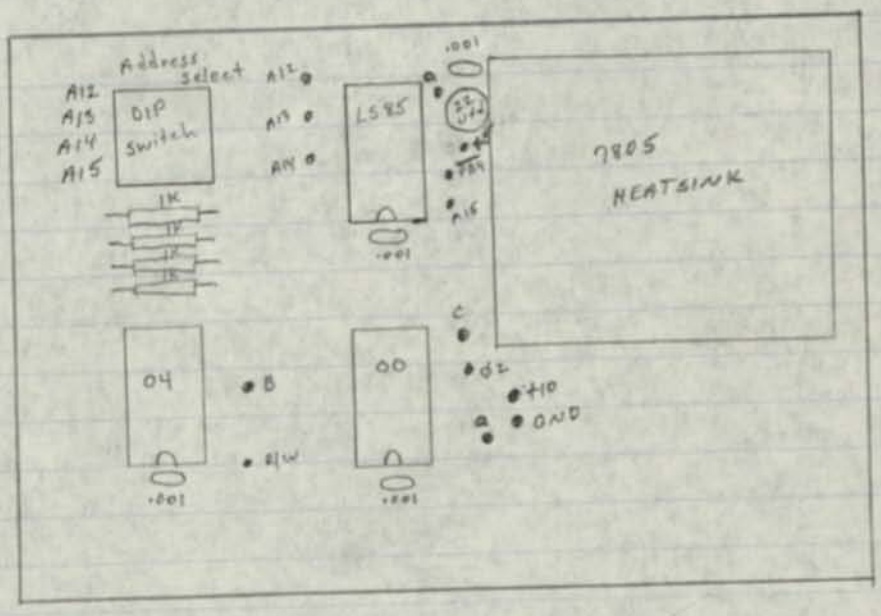
Backplane #'s are for memory Bd. connector - diff. than other connectors.

To Pin 6 74LS138 (connected to Pin 11 of 7408)

To Pins 1 & 15 8T26A (Connected to Pin 8 of 7408)

To R/W RAMS $\overline{\Phi 2 \cdot R/W}$ (connected to Pin 6 of 7408)

Memory Select Board



CCS

4K RAM BOARD

INTERCONNECTION DIAGRAM

44 PIN
EDGE CONNECTOR

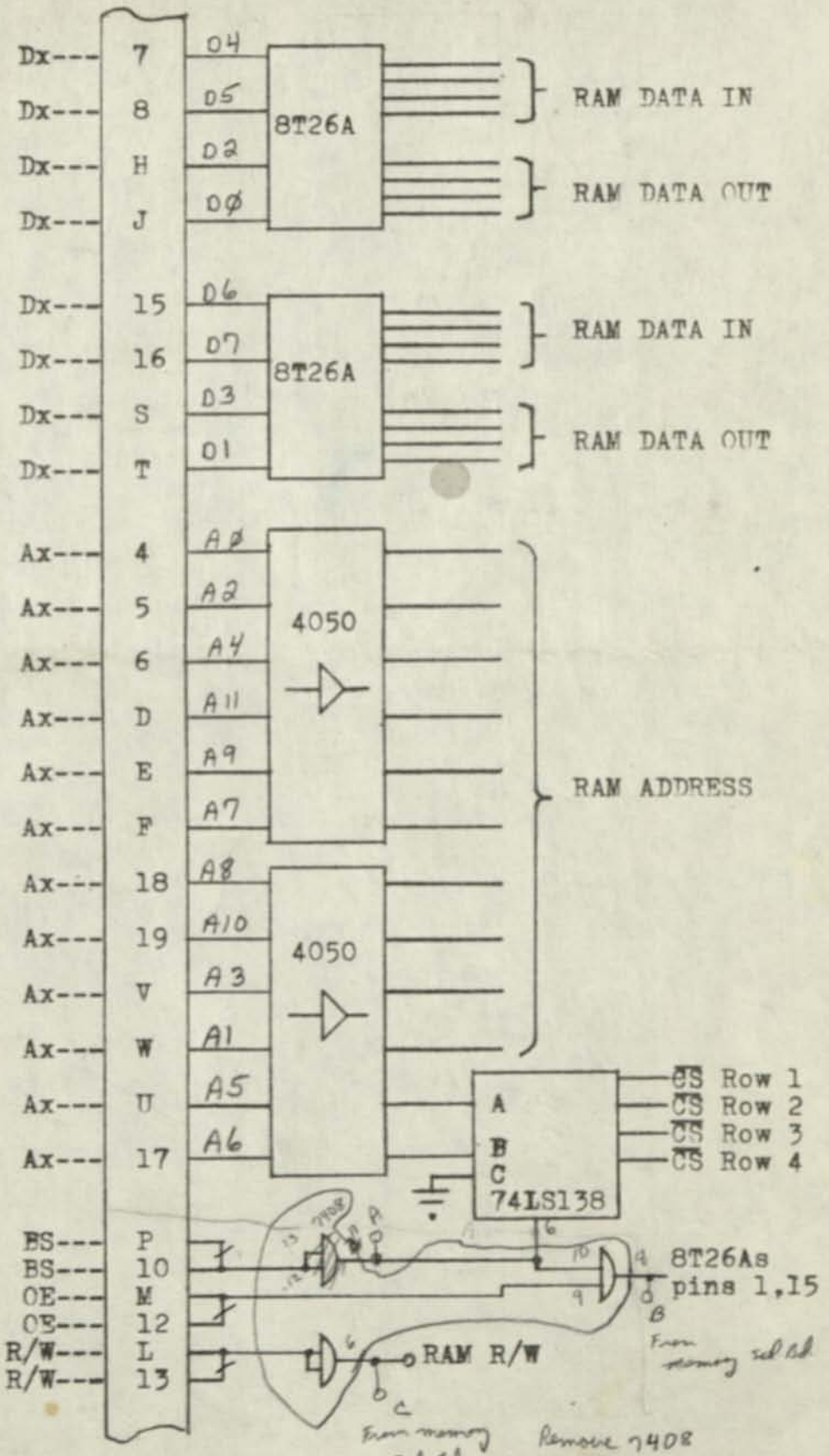
1	GND	GND	A
2	GND	GND	B
3	VCC	VCC	C
4	Ax	Ax	D
5	Ax	Ax	E
6	Ax	Ax	F
7	Dx	Dx	H
8	Dx	Dx	J
9	-	-	K
10	BS	R/W	L
11	-	OE	M
12	OE	-	N
13	R/W	BS	P
14	-	-	R
15	Dx	Dx	S
16	Dx	Dx	T
17	Ax	Ax	U
18	Ax	Ax	V
19	Ax	Ax	W
20	VCC	VCC	X
21	GND	GND	Y
22	GND	GND	Z

See Bus listing for complete Memory Board bus pinout

NOTE

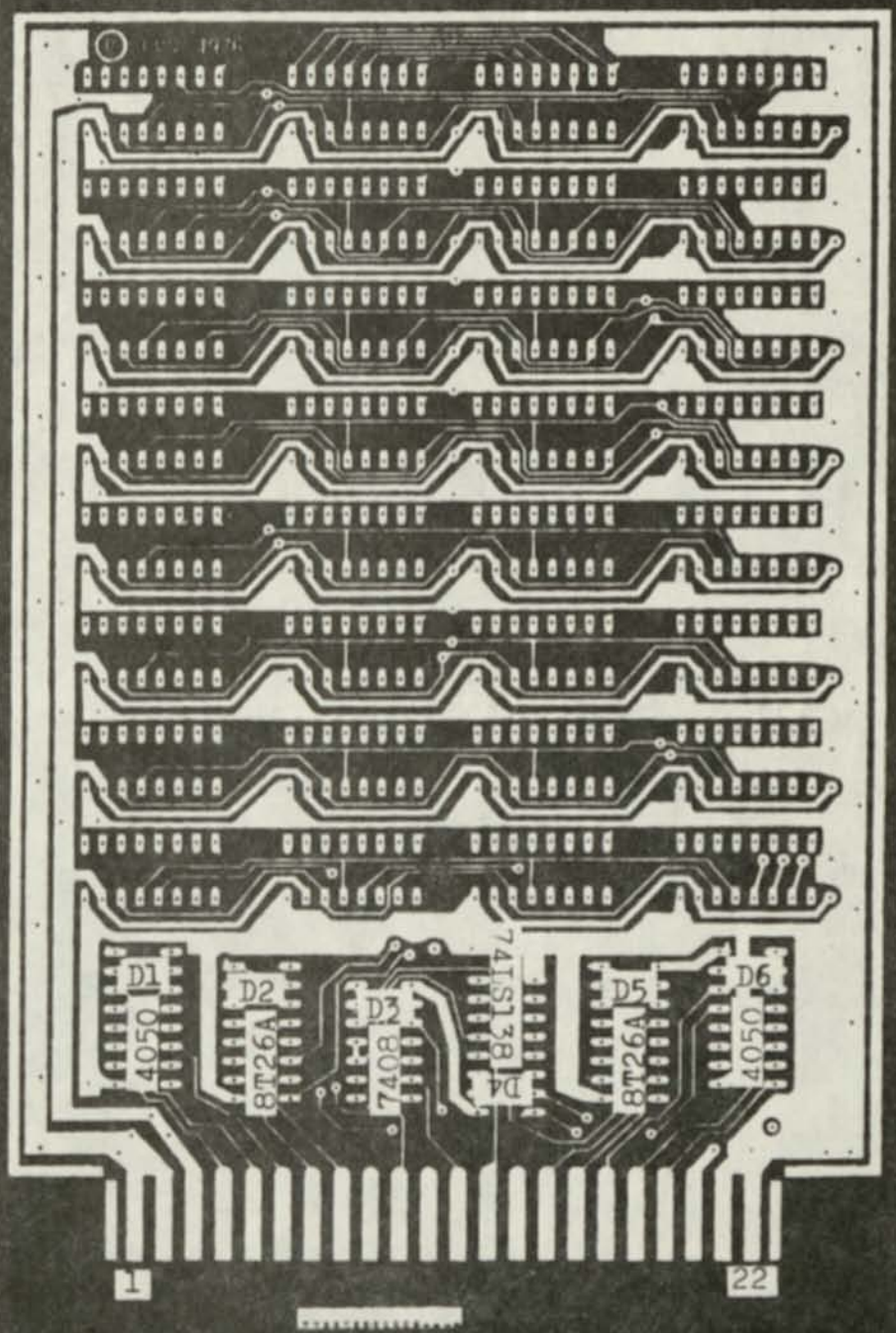
There are 12 Address (Ax) lines and 8 Data (Dx) lines. They are not assigned numbers by their significance. These lines are mutually exclusive, enabling the connector to be wired in any desired combination of the 12 LEAST significant address or 8 data lines. Note also the functional symmetry of the connector, allowing the board to be inserted in either direction.

FUNCTIONAL SCHEMATIC



CCS 12-76

SUPPORT CHIP LOCATION



CCS

4K RAM BOARD

APPLICATIONS NOTES

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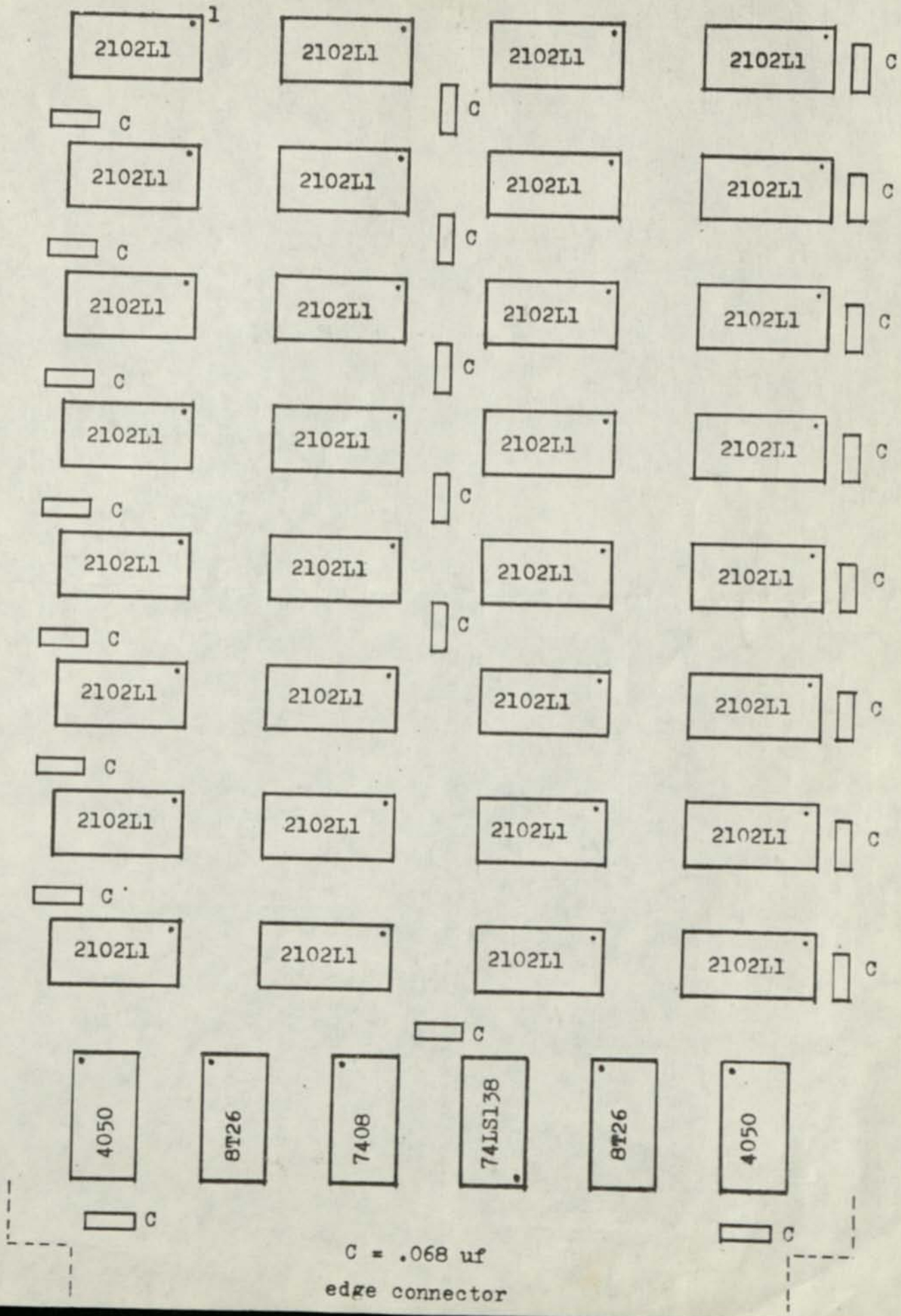
1. Prior to assembly of the kit, note that the orientation of the 74LS138 (D4 on the 'support chip location' figure) is opposite that of the other support chips.

2. MOS Handling Procedures
   a. The MOS ICs in the kit are packaged in an anti-static jacket. Do not remove them until assembly.
   b. The kit components, handling tools, work area, and the assembler should be at ground potential.
   c. Do not wear nylon clothing while handling MOS circuits.
   d. Following assembly, insure that system power is OFF before the 4K RAM BOARD is inserted or removed from a connector.

3. There are 3 lines not buffered through the 4050s or 8T26s. These lines (BS, OE, and R/W) are defined as follows:
   a. BOARD SELECT (BS)
      The BOARD SELECT signal is a board enable, and should be generated by a 4 to 16 decoder on the 4 MOST significant address lines. This line is active high,i.e., enabled by a logic 1.
   b. OUTPUT ENABLE (OE)
      The OUTPUT ENABLE line controls the data direction of the system RAM. When high, this line changes the data direction from input to output, driving the data bus from decoded RAM outputs. For example, in a typical 6800 system, this signal may be implemented with the CPU R/W.
   c. READ/WRITE (R/W)
      The READ/WRITE control line signals the memory whether the CPU is in a Read(high) or Write(low) state. During a write cycle, this line should remain high until the address has been present at the RAMs for a minimum of 170 nanoseconds and should return high 40 nanoseconds before the data becomes invalid.

IC LOCATION DRAWING



MEM-2

16 KByte 2114 Static RAM Memory Board

Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface (see figure 1).

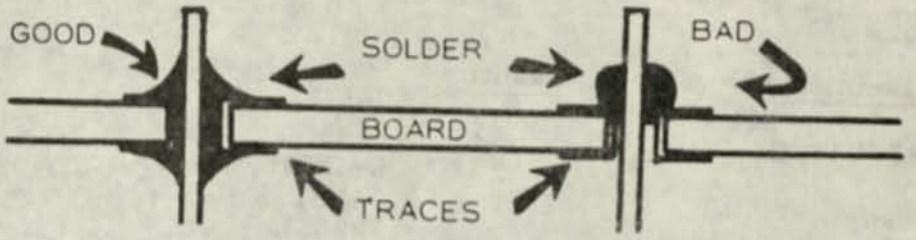


Figure 1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty) it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking, don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without over heating.

Please note: The notation on the solder mask for the polarity of the 22uf capacitors is backwards. Install the capacitors opposite to the way indicated on the solder mask.

C47 is correct

The MEM-2 is a memory board designed to interface 2114's to the S-100 (WAMECO$_{TM}$) bus (see Tables I and II). Provisions have been made for multiple wait states, memory addressing options, Phantom Disable, and Bank Addressing. Any multiple of two memory chips can be used in the board start and stop address can be effectively set in 4 K boundries anywhere in the 65 K Byte memory of your computer. If 4 K Bytes or less, the board can be configured to occupy only the amount of 4 K Bytes in the memory map of your computer. This selection can be increased by 4 K Byte increments until the full 16 K Bytes is selected.

PARTS LIST

Schematic Identifier	Quantity	Part
U1-U5	5	7805
U6-U21, U37-U44, U47-U54	32	2114
U22, U23	2	DM8098, 8T98, or 74368
U24, U27	2	74LS138
U25, U26	2	7485
U28	1	74LS02
U29	1	7404
U30, U31	2	74LS74
U32	1	74122
U33, U35	2	74LS20
U34	1	74LS32
U36, U45, U46	3	DM8097, 8T97, 74367
C1, C4, C14, C19, C25, C36, C37, C46, C50, C52	10	0.1μF disc ceramic capacitor
C2, C3, C13, C24, C47, C49	6	22μF 16V(or higher) Tantalum Capacitor
C5-C12, C15-C18, C20-C23, C26, C29-C32, C34, C35, C38-C45, C48, C51	33	0.01μF disc ceramic capacitor
C28	1	39pF disc ceramic capacitor
C33	1	680pF disc ceramic capacitor
R1	1	330Ω 1/4 W carbon film resistor
R2	1	100Ω 1/4W carbon film resistor
R3-R20	18	2.7KΩ 1/4W carbon film resistor
S1, S2	2	8 position dip switch
	5	#361 AHAM (or equivalent) heat sinks
	8	14 pin low profile sockets
	9	16 pin low profile sockets
	32	18 pin low profile sockets

TOOLS OR SUPPLIES NEEDED TO ASSEMBLE AND TEST MEM-2

1 Q Tip cotton swab
1 pair needle nose pliers
1 pair diagonal cutting pliers
1 bottle rosin flux
1 tube silicone thermal compound
1 jar solder cleaner
1 roll solder wick
1 Phillips screwdriver
1 small adjustable wrench or socket to fit regulator nut
1 roll (.031" or .040") SN60/40 rosin core solder
1 25 to 40 W soldering iron with small spade tip
1 Strong light
1 magnifying glass
1 XACTO knife with number 16 blade
1 multimeter with leads
1 power supply with variable outputs

S-100 (WAMECO) BUS DESCRIPTION

PIN	MNEMONIC	TERM.
1	+5V	
2	+15V	
3	XRDY	X
4	$\overline{VI0}$	X
5	$\overline{VI1}$	X
6	$\overline{VI2}$	X
7	$\overline{VI3}$	X
8	$\overline{VI4}$	X
9	$\overline{VI5}$	X
10	$\overline{VI6}$	X
11	$\overline{VI7}$	X
12		
13		
14		
15		
16		
17		
18	STAT DISABLE	X
19	CIC DISABLE	X
20	UNPROTECT	X
21	SS	X
22	ADDR DSBL	X
23	DO DSBL	X
24	Ø2	X
25	Ø1	X
26	PHLDA	X
27	PWAIT	
28	PINTE	
29	A5	
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	DO1	X
36	DOØ	X
37	A10	
38	DO4	X
39	DO5	X
40	DO6	X
41	DI2	X
42	DI3	X
43	DI7	X
44	SMI	
45	SOUT	
46	SINP	
47	SMEMR	
48	SHLTA	
49	CLOCK (2MHz)	
50	GND	

PIN	MNEMONIC	ALTER. PIN DESIG.	TERM.
51	+5V	A	
52	-15V	B	
53	SSW DSB	C	
54	EXT CLR	D	X
55		E	
56		F	
57		H	
58		J	
59		K	
60		L	
61		M	
62		N	
63		P	
64		R	
65		S	
66		T	
67	PHANTOM	U	
68	MWRITE	V	X
69	PS	W	
70	PROTECT	X	X
71	RUN	Y	X
72	PRDY	Z	X
73	PINT	a	X
74	PHOLD	b	X
75	PRESET	c	X
76	PSYNC	d	X
77	PWR	e	X
78	PDBIN	f	X
79	AØ	h	
80	A1	j	
81	A2	k	
82	A6	l	
83	A7	m	
84	A8	n	
85	A13	p	
86	A14	r	
87	A11	s	
88	DO2	t	X
89	DO3	u	X
90	DO7	v	X
91	DI4	w	X
92	DI5	x	X
93	DI6	y	X
94	DI1	z	X
95	DIØ	AA	X
96	SINTA	AB	
97	SWO	AC	
98	SSTACK	AD	
99	POC	AE	
100	GND	AF	

Table I

Pin #	Mnemonic	Enabled State	Description
1	+8 Volts	NA	Unregulated +8 Volts DC. This voltage should not be less than +8 or greater than +11 volts.
2	+16 Volts	NA	Unregulated +16 Volts DC. This voltage should not be less than +16 or greater than +20 Volts.
3	XRDY	Low	Causes CPU to enter WAIT state when enabled.
4	$\overline{VI0}$	Low	Vectored Interrupt priority 0
5	$\overline{VI1}$	Low	Vectored Interrupt priority 1
6	$\overline{VI2}$	Low	Vectored Interrupt priority 2
7	$\overline{VI3}$	Low	Vectored Interrupt priority 3
8	$\overline{VI4}$	Low	Vectored Interrupt priority 4
9	$\overline{VI5}$	Low	Vectored Interrupt priority 5
10	$\overline{VI6}$	Low	Vectored Interrupt priority 6
11	VI7	Low	Vectored Interrupt priority 7
12	---	NA	Not used
13	---	NA	Not used
14	---	NA	Not used
15	---	NA	Not used
16	---	NA	Not used
17	---	NA	Not used
18	STAT DISABLE	Low	The eight status line buffers on the CPU board enter the high impedance state when enabled.
19	C/C DISABLE	Low	The six command/control line buffers on the CPU board enter the high impedance state when enabled.
20	UNPROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be cleared.
21	SS	High	Indicates the CPU is single stepping.
22	$\overline{ADDR\ DSBL}$	Low	The 16 address line buffers on the CPU board enter the high impedance state when enabled.
23	$\overline{DO\ DSBL}$	Low	The eight data-out lines on the CPU board enter the high impedance state when enabled.
24	Ø2	High	Buffered TTL CPU phase 2 clock.
25	Ø1	High	Buffered TTL CPU phase 1 clock.
26	PHLDA	High	CPU board "Hold Acknowledge" to HOLD-H input.
27	PWAIT	High	CPU output showing a WAIT state is occuring.

Table II

Pin #	Mnemonic	Enabled State	Description
28	PINTE	High	CPU output showing that Interrupts are enabled.
29	A5	High	Address Bit 5
30	A4	High	Address Bit 4
31	A3	High	Address Bit 3
32	A15	High	Address Bit 15
33	A12	High	Address Bit 12
34	A9	High	Address Bit 9
35	DO1	High	CPU Data Out Bit 1
36	DO0	High	CPU Data Out Bit 0
37	A10	High	Address Bit 10
38	DO4	High	CPU Data Out Bit 4
39	DO5	High	CPU Data Out Bit 5
40	DO6	High	CPU Data Out Bit 6
41	D12	High	Data In Bit 2 to CPU
42	D13	High	Data In Bit 3 to CPU
43	D17	High	Data In Bit 7 to CPU
44	SM1	High	CPU output indicating it is performing Fetch Instruction.
45	SOUT	High	CPU output showing it is in an output cycle.
46	SINP	High	CPU output showing it is in an input cycle.
47	SMEMR	High	CPU status signal indicating the current cycle is a Memory Read cycle.
48	SHLTA	High	CPU status signal indicating the CPU is halted.
49	CLOCK(2MHz)	Low	A buffered 2 MHz clock for general use.
50	GND	NA	Ground (common)
51	+8 Volts	NA	(Same as pin 1)
52	-16 Volts	NA	Unregulated-16 Volts DC. This voltage should not be greater than -16 or less than -20 Volts.
53	$\overline{\text{SSW DSB}}$	Low	Sense Switch Disable disables CPU board data input buffers so that CPU can read sense switches.
54	$\overline{\text{EXT CLR}}$	Low	Front panel generated I/O clear signal.
55	---	NA	Not used
56	---	NA	Not used
57	---	NA	Not used
58	---	NA	Not used
59	---	NA	Not used
60	---	NA	Not used
61	---	NA	Not used
62	---	NA	Not used
63	---	NA	Not used
64	---	NA	Not used
65	---	NA	Not used
66	---	NA	Not used
67	PHANTOM	NA	Used for Memory Bank Selection (or for SOL© Systems)

Table II

Pin #	Mnemonic	Enabled State	Description
68	MWRITE	High	CPU output showing Data Out Bus data is to be written into the memory selected by the address lines.
69	$\overline{PS}$	Low	Shows Protect Status of selected memory.
70	PROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be set.
71	RUN	High	Front panel indication that CPU run instruction has been input.
72	PRDY	Low	Causes the CPU to enter the WAIT state when enabled.
73	$\overline{PINT}$	Low	If interrupts have been enabled causes the CPU to enter the Interrupt Acknowledge condition at the conclusion of the current instruction.
74	$\overline{PHOLD}$	Low	CPU input which causes a HOLD status to occur. DMA transfer request signal is $\overline{PHOLD}$.
75	$\overline{PRESET}$	Low	CPU board system reset signal.
76	PSYNC	High	CPU output showing the start of a new machine cycle. This signal is used on the CPU board to enable the loading of the System Status Latch.
77	$\overline{PWR}$	Low	Indication that data on the Data Out Bus is to be written either to a memory or an I/O device.
78	PDBIN	Low	Indication to the selected memory or I/O device that the CPU expects data on the Data In Bus.
79	A0	High	Address Bit 0
80	A1	High	Address Bit 1
81	A2	High	Address Bit 2
82	A6	High	Address Bit 6
83	A7	High	Address Bit 7
84	A8	High	Address Bit 8
85	A13	High	Address Bit 13
86	A14	High	Address Bit 14
87	A11	High	Address Bit 11
88	DO2	High	CPU Data Out Bit 2
89	DO3	High	CPU Data Out Bit 3
90	DO7	High	CPU Data Out Bit 7
91	DI4	High	Data In Bit 4 to CPU
92	DI5	High	Data In Bit 5 to CPU
93	DI6	High	Data In Bit 6 to CPU

Table II

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
94	DI1	High	Data In Bit 1 to CPU
95	DI0	High	Data In Bit 0 to CPU
96	SINTA	High	CPU Interrupt Acknowledge Signal
97	SWO	Low	CPU output indicating the current cycle involves writing to a memory or I/O device.
98	SSTACK	High	CPU output indicating the address bus contains the stack address and the current cycle will have a stack operation.
99	$\overline{\text{POC}}$	Low	Power On Clear reset signal
100	GND	NA	Ground (common)

Table II

I. Assembly of MEM-2

I-1. Before placing any parts on the board, check the board for any hairline shorts (slivers). All boards have been inspected at least three times before shipping. Still, a good hobbyist checks any board he buys.

I-2. Using a strong light and a magnifying glass, very carefully check all leads on the top of the board (this is the side marked COMPONENT SIDE). If any slivers are found, carefully cut and scrape them with an XACTO knife. The underside of the board will be checked after assembly.

I-3. Place all the 14, 16, and 18 pin sockets in their positions on the top side of the board.

I-4. After positioning all the sockets in place, check to ensure that a socket is not in the position S1 or S2. Dip switches will not stay in place in a socket. Place a book on top of the sockets, hold the book tight against the board and turn them over so that the underside of the board is up. Press down on the board and solder one pin on each end of each socket. This will ensure the sockets are flat against the board. When the tacking of all sockets is completed, finish soldering all the other pins of the sockets.

NOTE

DO NOT PUT IC'S IN SOCKETS AT THIS TIME. THEY WILL BE INSTALLED LATER.

I-5. Bend the leads on R3-R20 (2.7KΩ RED, VIOLET, RED) and place in board. Check parts placement drawing (figure 3) for correct locations. Bend the leads of the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

I-6. Bend the leads on R1 (330Ω ORANGE, ORANGE, BROWN) and place in board. Check parts placement drawing (figure 3) for correct location. Bend the leads of the resistor on the underside of the board to retain it in place until it is soldered. Turn the board over and solder the resistor. Clip the leads of the resistor flush with the underside of the board with the diagonal pliers.

I-7. Bend the leads on R2 (100Ω BROWN, BLACK, BROWN) and place in board. Check parts placement drawing (figure 3) for correct location. Bend the leads on the resistor on the underside of the board to retain it in place until it is soldered. Turn the board over and solder the resistor. Clip the leads of the resistor flush with the underside of the board with the diagonal pliers.

CAUTION

CHECK DISC CAPACITORS FOR PROPER VALUE BEFORE INSERTING IN BOARD. ENSURE .01 μF AND .1 μF DISC CAPACITORS ARE NOT INTERCHANGED.

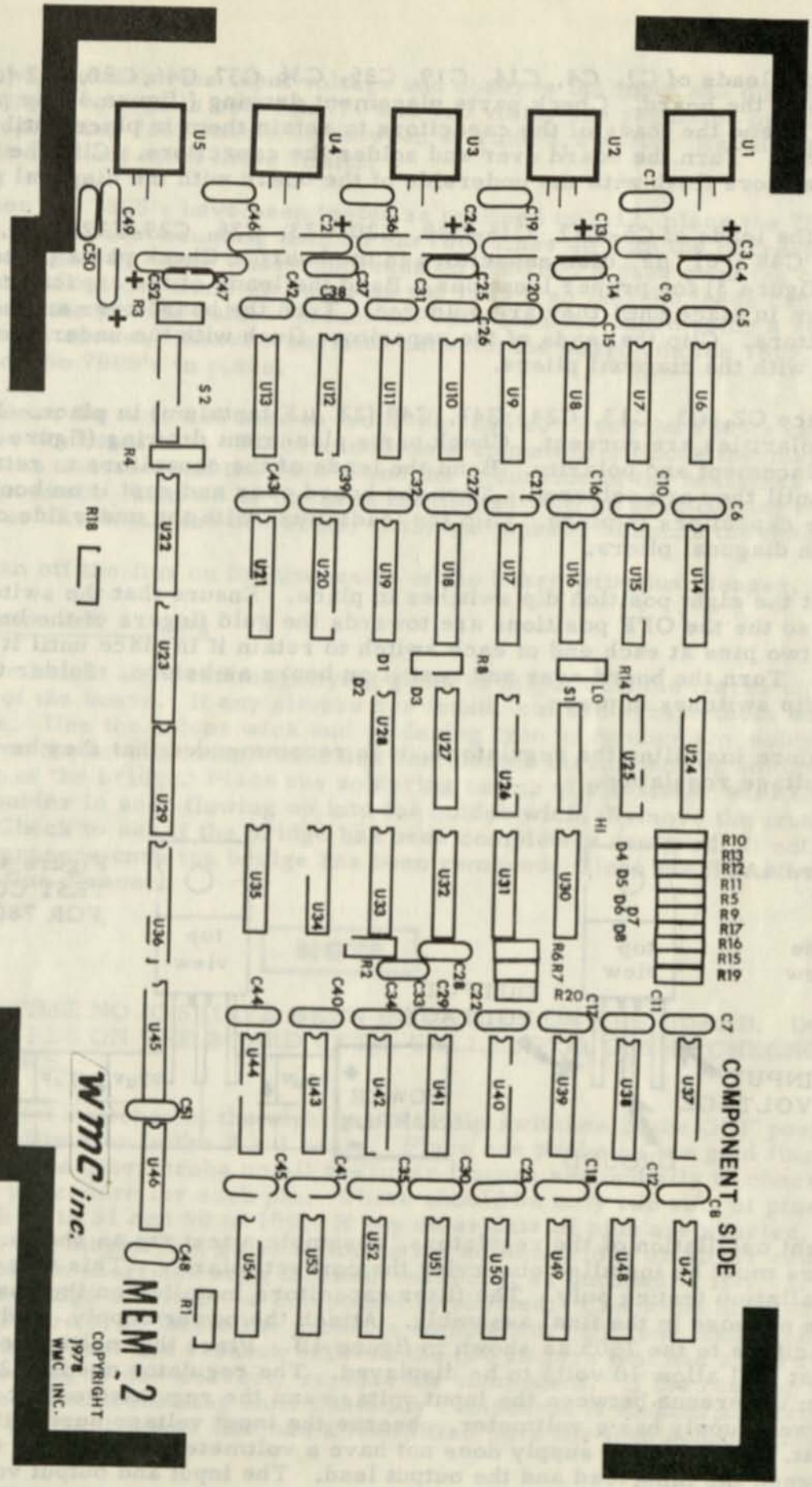


Figure 3. MEM-2 Parts Placement Diagram

I-8. Put the leads of C1, C4, C14, C19, C25, C36, C37, C46, C50, C52 (.1 F) disc capacitors in the board. Check parts placement drawing (figure 3) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and solder the capacitors. Clip the leads of the capacitors flush with the underside of the board with the diagonal pliers.

I-9. Put the leads of C5-C12, C15-C18, C20-C23, C26, C29-C32, C34, C35,C51 C38-C45, C48 (.01 μF) disc capacitors in the board. Check parts placement drawing (figure 3) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and solder the capacitors. Clip the leads of the capacitors flush with the underside of the board with the diagonal pliers.

I-10. Place C2, C3, C13, C24, C47, C49 (22 μF tantalum) in place. Ensure that the polarities are correct. Check parts placement drawing (figure 3) for correct placement and polarity. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books. Solder the capacitors in place. Clip the leads flush with the underside of the board with diagonal pliers.

I-11. Put the eight position dip switches in place. Ensure that the switches are installed so the the OFF positions are towards the gold fingers of the board. Bend the two pins at each end of each switch to retain it in place until it is soldered. Turn the board over and rest it on books as before. Solder the eight position dip switches in place.

I-12. Before installing the regulators, it is recommended that they be tested for proper voltage regulation.

Figure 4A.
7805

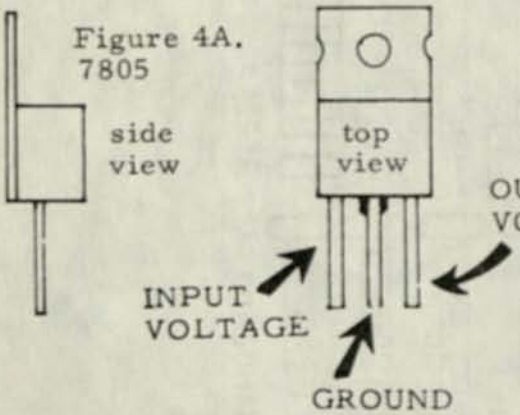
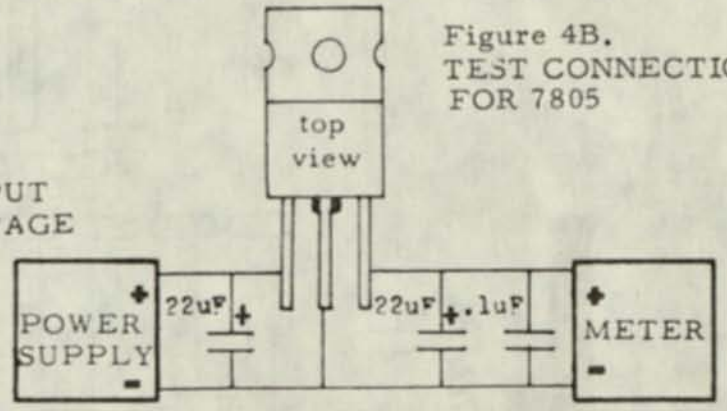


Figure 4B.
TEST CONNECTIONS
FOR 7805



To prevent oscillation of the regulators, assemble a test rig as shown. The capacitors must be installed observing the correct polarity. This test rig is for pre-installation testing only. The filter capacitors installed on the board serve the same purpose in the final assembly. Attach the power supply, multimeter, and capacitors to the 7805 as shown in figure 4B. Place the multimeter in a DC range that will allow 10 volts to be displayed. The regulator needs a 2.0 volt minimum difference between the input voltage and the regulated output voltage. If the power supply has a voltmeter, observe the input voltage during the test using that. If the power supply does not have a voltmeter, switch the + meter lead between the input lead and the output lead. The input and output voltages can thus be observed.

I-13. Slowly increase the input voltage and observe the input and output voltages. When the input voltage is between 7.0 and 7.5 volts, the regulated output of a properly operating 7805 should be between 4.8 and 5.2 volts. Replace the regulator if it does not meet these limits.

I-14. When the 7805's have been tested as outlined in I-12, place the 7805's on the board so that the mounting hole on the 7805 lines up with the corresponding hole on the MEM-2. Note where the leads on the 7805's pass over the connection holes on the MEM-2. Bend the leads on the 7805's so that the leads can be inserted into the proper holes. Mount the 7805's on the board using a #6 nut and 5/8" 6-30 screw. Insert a heatsink between the board and the 7805. Solder the leads of the 7805's in place.

I-15. Remove the nuts and screws from the 7805's. Bend the 7805's upward and remove the heatsinks. Place a moderate amount of silicone thermal heat grease on the underside of the 7805's and the underside of the heatsinks with a Q tip cotton swab. Coat all of the area mentioned with an even coating of the heat grease. Reinstall the heatsinks, nuts, and screw. Ensure the nuts are tight.

I-16. Clean off the flux on the underside of the board with flux cleaner.

II. Inspection and Testing

II-1. Use a bright light and magnifying glass to inspect all the traces on the underside of the board. If any slivers are found, cut and scrape them with an Xacto knife. Use the solder wick and soldering iron to remove any solder bridges found. Cover the solder bridge with flux and place a clean piece of solder wick on top of the bridge. Place the soldering on top of the solder wick and hold until solder is seen flowing up into the solder wick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

NOTE

AT THIS TIME NO IC'S HAVE BEEN INSTALLED ON THE BOARD. DO NOT INSTALL IC'S ON THE BOARD UNTIL CALLED FOR IN THE CHECKOUT PROCEDURE.

II-2. Place all switches of the eight position dip switches in the OFF position. Place the multimeter in the R x 1 scale. Place one probe on the gold finger for pin 1. Place the other probe on all the other fingers sequentially to check for shorts. Repeat this procedure for each pin. There should be only two sets of pins that are shorted; 1 to 51 and 50 to 100. If any other pair of pins are shorted, use a strong light and magnifying glass to locate the solder bridge or sliver causing the short. When the short has been located, correct it as outlined in II-1. If there is no solder bridge or sliver, a component is shorted. Check the MEM-2 schematic (figure 5) to locate the probable component. Lift one lead of the suspected component and recheck between the two fingers that had a bad reading. If the bad reading is now correct, replace the component. If the reading is still bad, continue troubleshooting until the faulty component is located and replaced. Ensure that all components that had a lead lifted have the lead reconnected.

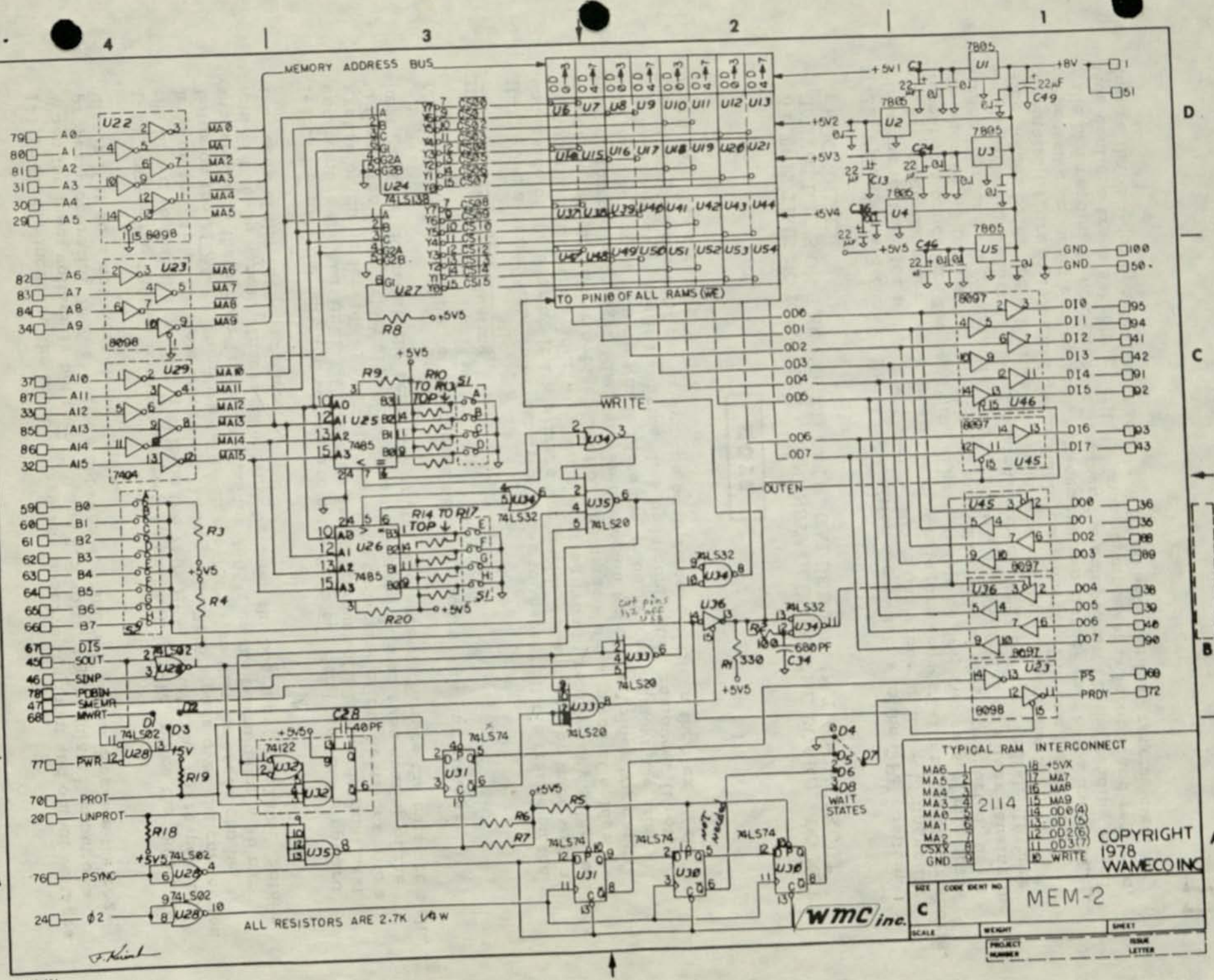


Figure 5. MEM-2 Schematic

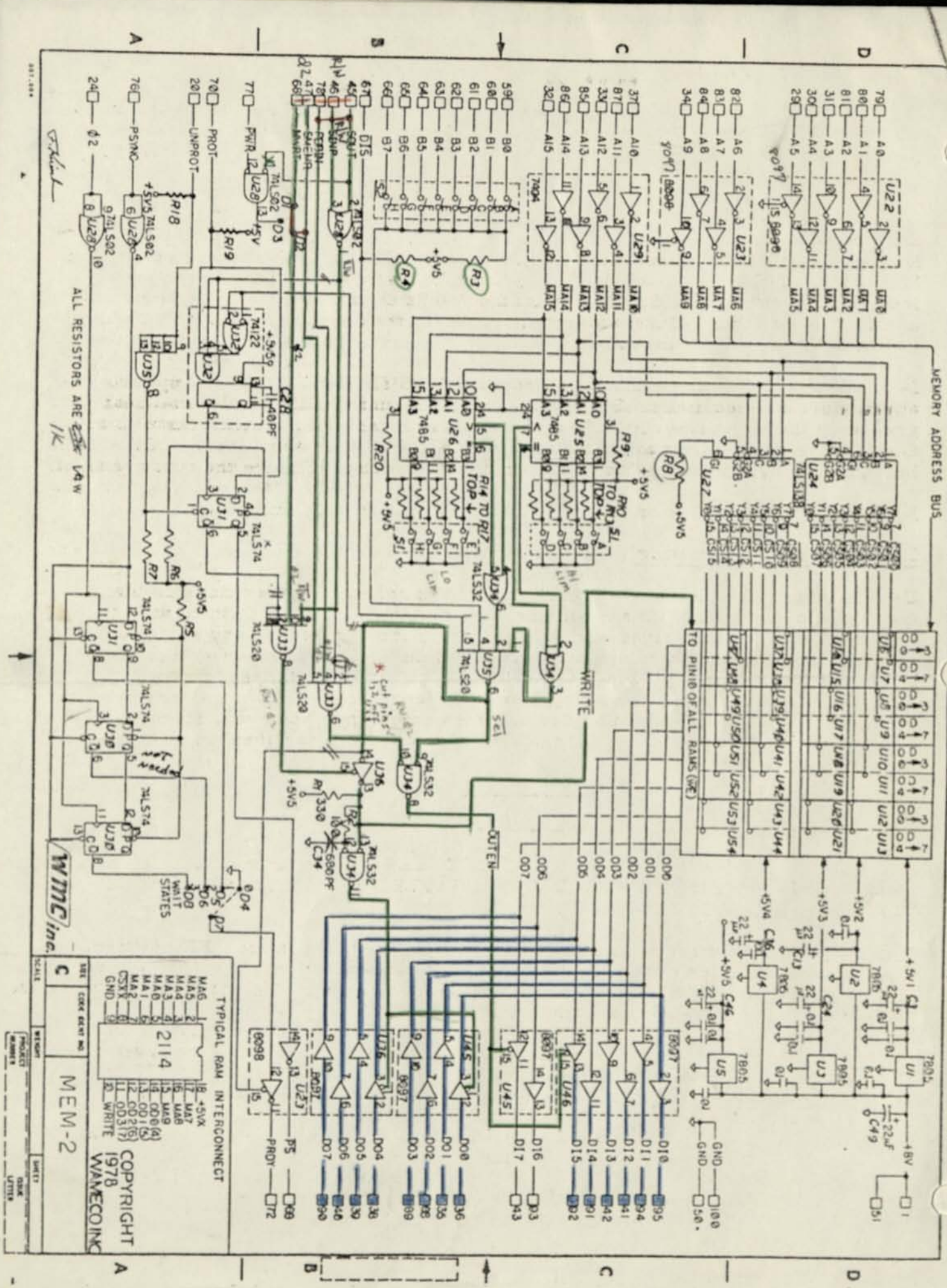


Figure 5. MEM-2 Schematic

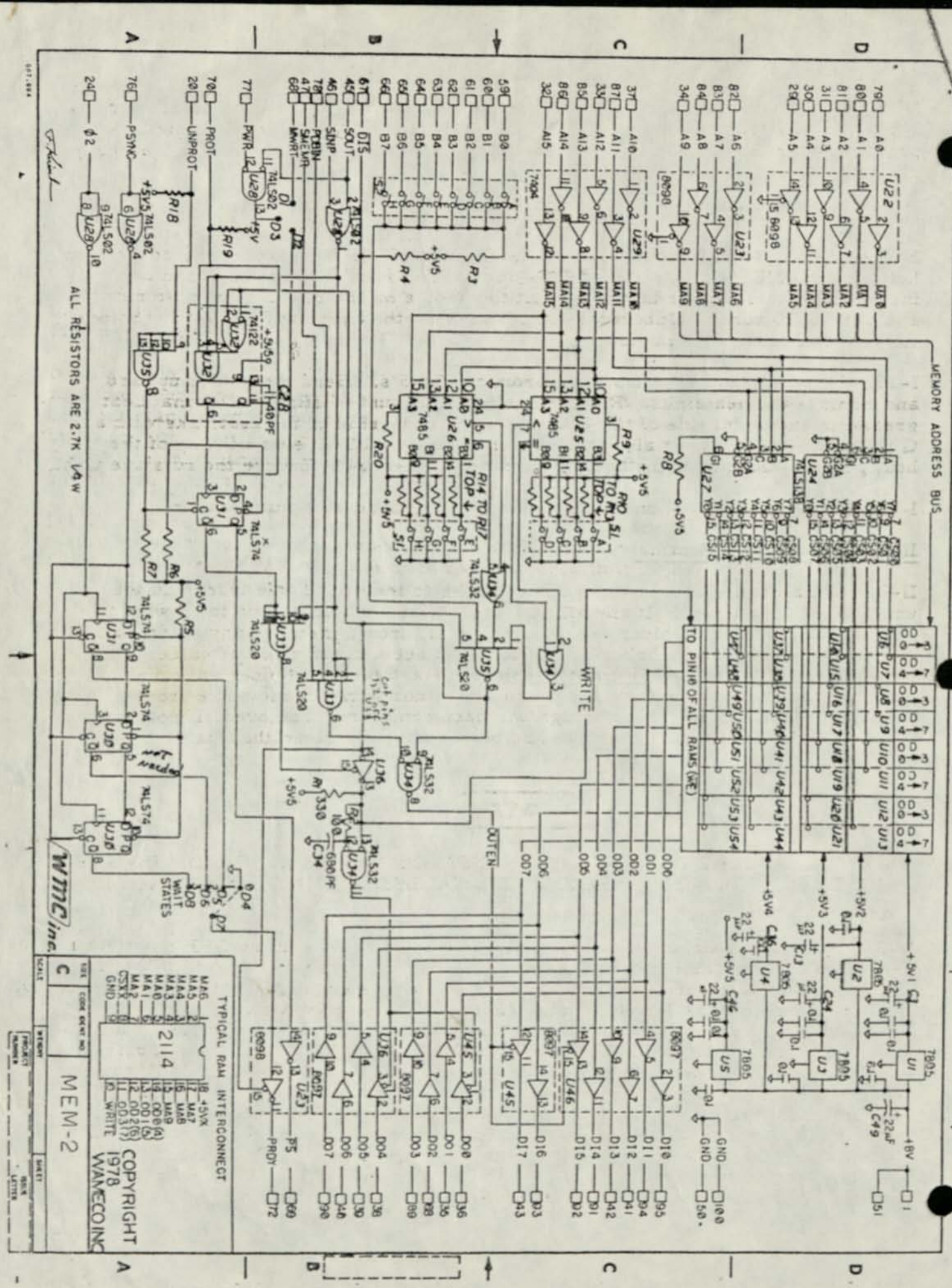


Figure 5. MEM-2 Schematic

U25 7485 —
U26 7485 —
U22 8098
U23 8098
U29 7404 —
U24 74LS138 —
U27 74LS08 —
U28 74LS02 —
U33 74LS28
U34 74LS32 —
U35 74LS20
U45 8097 —
U46 8097 —
U36 8097

WARNING

DO NOT INSTALL OR REMOVE ANY BOARD IN COMPUTER WITH POWER ON. DAMAGE TO BOARDS AND COMPUTER MAY RESULT.

II-3. Ensure computer is OFF. Plug MEM-2 into the motherboard. Check that the MEM-2 is correctly plugged in and that the board is fully seated in the connector. Turn the computer power ON and check the outputs of each regulator on the MEM-2. If the regulators do not have outputs as stated in I-13, turn the computer power OFF and replace the defective regulator. Repeat I-13 to check out the new regulator before installing. If the voltage on the regulator is not now correct, check the voltages on the motherboard. If the voltages on the motherboard are incorrect, repair the power supply as needed. If and when the voltage check good, turn the computer power OFF and remove the MEM-2 from the motherboard.

II-4. Select the proper wait state and MWRITE selection for the board by installing the jumpers on the MEM-2 as shown in Figure 6.

II-5. Clean off the flux on the underside of the board with flux cleaner.

II-6. Install all the IC's on the MEM-2. Check parts placement drawing (Figure 3) for proper location and correct polarity of IC's.

CAUTION

ENSURE ALL IC'S ARE INSTALLED CORRECTLY. INCORRECT POLARIZATION OF IC WILL RESULT IN DAMAGE TO IC AND CAUSE SUBSEQUENT TROUBLES TO APPEAR ON THE BOARD.

II-7. The memory of the MEM-2 is addressed in 4KByte segments. The minimum segment that can be selected is 4K. The board can be populated in 1KByte increments (2 memory chips) at a time. The memory is divided into four separate sections which will be referred to as A through D (see Figure 7). A will always have memory starting at 0000H, 4000H, 8000H, or C000H. B will always have memory starting at 1000H, 5000H, 9000H, or D000H. C will always have memory starting at 2000H, 6000H, A000H, or E000H. D will always have memory starting at 3000H, 7000H, B000H, or F000H.

II-8. Since the memory starting point of the board dictates which section has the starting (lowest) address, it is important that you consider the addressing examples given below.

EXAMPLE A. 5 KBytes of memory to be put on board, starting at 3000H. 8 KBytes of memory space will be used. Section D will be completely filled and U6 and U14 of section A will be filled. Memory addressing increases from top to bottom of each section. Low limit address switches of S1 (A-D) will be OFF, OFF, ON, ON. High limit (E-H) will be OFF, ON, OFF, OFF.

MWRITE SELECTION

No front panel or no MWRITE - Jumper D2 to D3
Front panel with MWRITE - Jumper D1 to D2

WAIT STATE JUMPER SELECTION

WAIT STATE	JUMPER D7 TO
0	D4
1	D5
2	D6
3	D8

NOTE

U30 DOES NOT HAVE TO BE INSTALLED IF 0 OR 1 WAIT STATE IS SELECTED.

MEMORY ADDRESS RANGE SELECT (S1)

LOW LIMIT				HIGH LIMIT					
A	B	C	D	E	F	G	H	ADDRESS RANGE	SECTION
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0000-0FFF	A
OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	1000-1FFF	B
OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	2000-2FFF	C
OFF	OFF	ON	ON	OFF	OFF	ON	ON	3000-3FFF	D
OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	4000-4FFF	A
OFF	ON	OFF	ON	OFF	ON	OFF	ON	5000-5FFF	B
OFF	ON	ON	OFF	OFF	ON	ON	OFF	6000-6FFF	C
OFF	ON	ON	ON	OFF	ON	ON	ON	7000-7FFF	D
ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	8000-8FFF	A
ON	OFF	OFF	ON	ON	OFF	OFF	ON	9000-9FFF	B
ON	OFF	ON	OFF	ON	OFF	ON	OFF	A000-AFFF	C
ON	OFF	ON	ON	ON	OFF	ON	ON	B000-BFFF	D
ON	ON	OFF	OFF	ON	ON	OFF	OFF	C000-CFFF	A
ON	ON	OFF	ON	ON	ON	OFF	ON	D000-DFFF	B
ON	ON	ON	OFF	ON	ON	ON	OFF	E000-EFFF	C
ON	ON	ON	ON	ON	ON	ON	ON	F000-FFFF	D

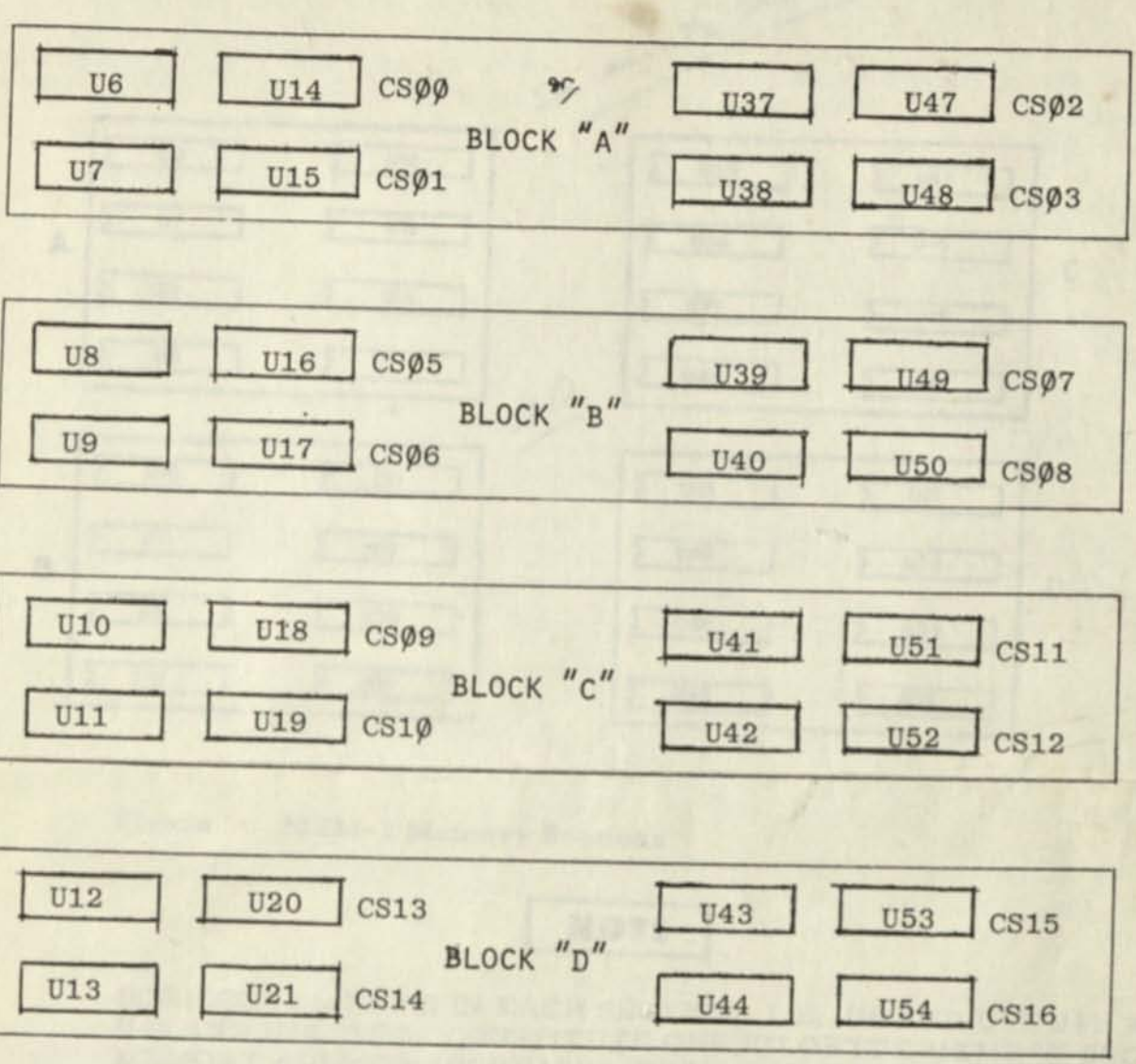
ADDRESS SELECT REQUIREMENT

LOW LIMIT SETTING DESIRED ADDRESS RANGE HIGH LIMIT SETTING

Figure 6. MEM-2 Board Configuration

ERRATA FOR WAMECO MEM-2

1. Fig. 7, page 15 should be:



Schematic should be amended to reflect correct "U" numbers for each chip select.

EXAMPLE B. 12 KBytes of memory to be put on board, starting at 9000H. 12 KBytes of memory space will be used. Section B will be the lowest address block. Sections B, C, and D will be completely filled. Low limit switches of S1 (A-D) will be ON, OFF, OFF, ON. High limit (E-H) will be ON, OFF, ON, ON.

II-9. Select the address range desired on S1. Insert the memory chips as dictated by the selected memory address. Insure that the polarity of the memory chips are correct (see Figure 3).

II-10. The two horizontially adjacent memory chips in each section are the chip pairs that form a one KByte block. Memory increases in address from top to bottom of each section.

II-11. Ensure computer is OFF. Plug the MEM-2 into the motherboard. Check that MEM-2 is correctly plugged in and that the board is fully seated in the connector.

NOTE

WHEN POWER IS APPLIED TO AN 8080 SYSTEM, THE MICROPROCESSOR DOES NOT COME UP IN ANY DETERMINABLE STATE. TO CORRECTLY INITIALIZE THE COMPUTER, HOLD THE STOP SWITCH IN STOP AND PUSH THE RESET TO RESET.

II-12. There are three different programs given to check out the memory of your board. They are:

1. Memory Address/Checkerboard Test (RTEST)
2. Walking One (WLKON)
3. Walking Zero (WLKZR)

II-13. All three tests require that your board be configured for address 0000H. If your computer will not allow this address to be used, you will have to modify the programs to use an allowable address range.

II-14. After configuring your board as above, turn your computer ON and input your choice of the memory tests given. RTEST will only take about a second to run once it has been inputted, WLKON and WLKZR take an expodential time to run as more and more memory is tested. It is therefore recommended that you not run more than 2 KBytes at a time on these two tests.

II-15. These programs are very basic and are given to help you debug your board. They will stop upon completion or when an error is found. It may therefore be needed to run them a series of times until all errors have been found and corrected. It is possible to modify the programs so that they will execute until completion and give an output of all errors found. We leave this modification up to you as an exercise in assembly language programming. The programs are written to be input from your front panel. If you don't have a front panel or if you wish to use another input device, you will have to modify the programs to meet your system requirements.

III. BANK ADDRESSING

III-1. Switch S2 controls the bank addressing capabilities of MEM-2. If S2 is not installed, the board will respond if the address presented to it falls within the limits selected by switch S1.

III-2. If S2 is installed, MEM-2 will respond if and only if the address is within the limits selected by S1 and the CPU has selected a memory bank corresponding to the setting of S2.

III-3. If MEM-2 is to be used in an application using bank addressing, use Figure 8 to select the correct bank.

BANK ADDRESSING SELECTION (S2)

A	B	C	D	E	F	G	H	BANK
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	1
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	2
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	3
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	4
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	5
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	6
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	7
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	8

Figure 8. MEM-2 Bank Addressing Selection

CAUTION

ENSURE ONLY ONE SWITCH IS ON AT ANY TIME. MULTIPLE ON SETTINGS WILL CONFUSE THE BOARD.

NOTE

ALL SWITCHES OFF DISABLE THE BANK SELECT OPTION.

IV. GENERAL

IV-1. The WAMECO INCORPORATED product you have purchased has an unlimited guarantee good for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by WAMECO INCORPORATED, pre-paid freight or mailing, the board will be replaced and your shipping charges cheerfully refunded. The guaranty is limited to replacement of the board with an equivalent board even though the board may be defective through negligence in manufacturing or through other fault.

IV-2. For future reference, a print of the front and back traces of the MEM-2 is shown (see Figure 9A and B).

IV-3. We sincerely hope that the MEM-2 will give you long and satisfactory service. If you have any problems with the MEM-2, or if you just want to comment on the board, please write to me personally.

Norm Walters
President
WAMECO INCORPORATED
3107 Laneview Drive
San Jose, Ca. 95132

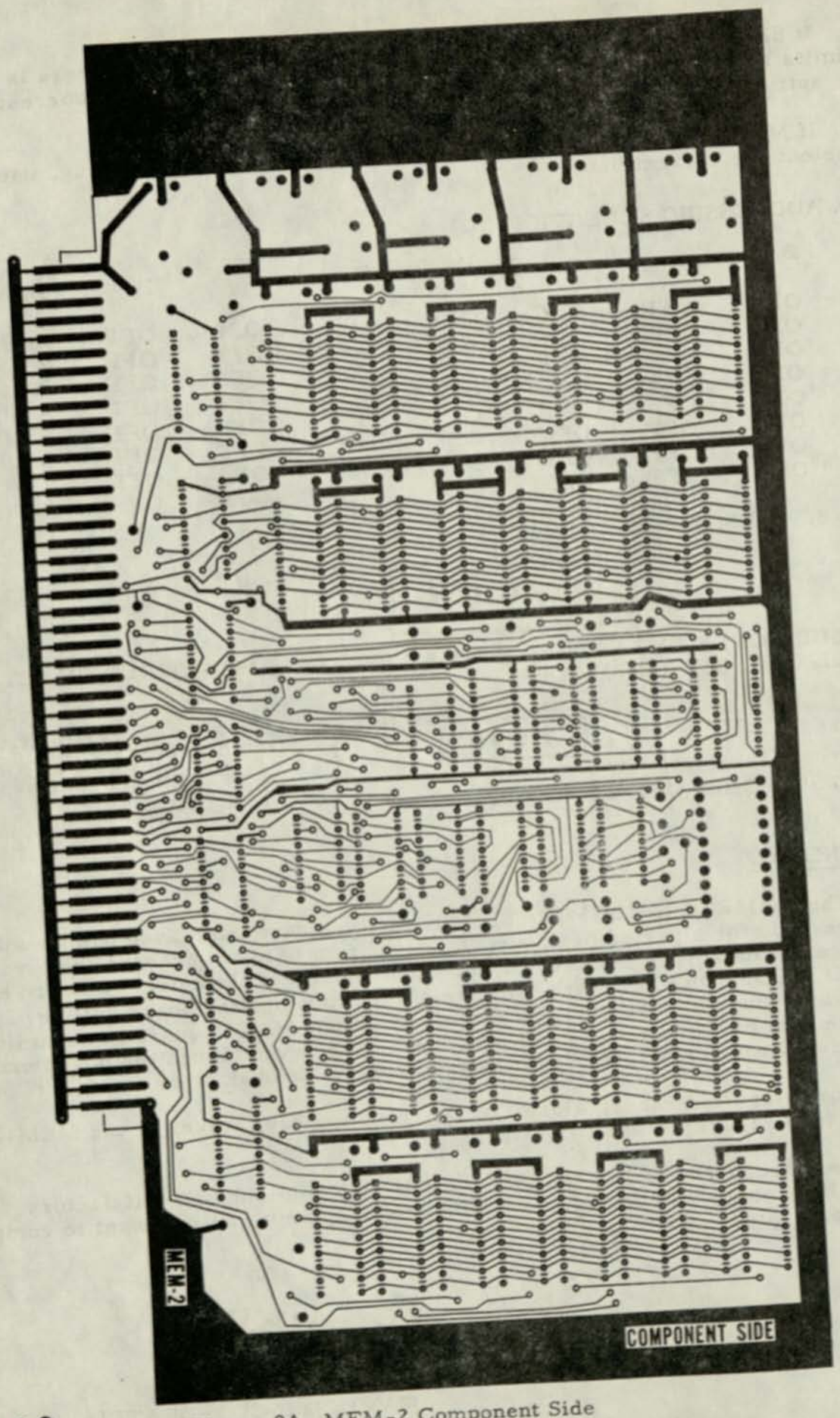


Figure 9A. MEM-2 Component Side

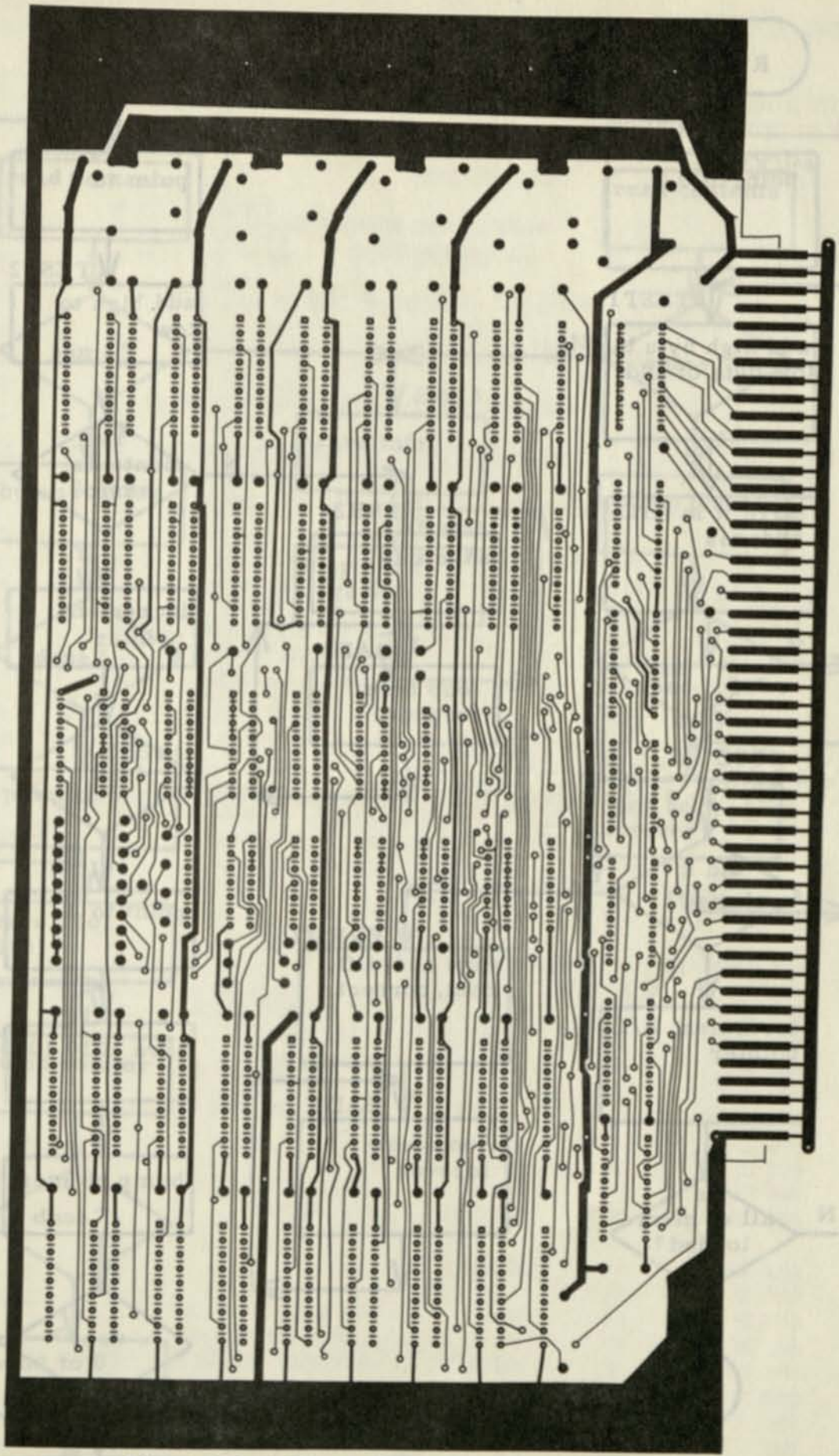
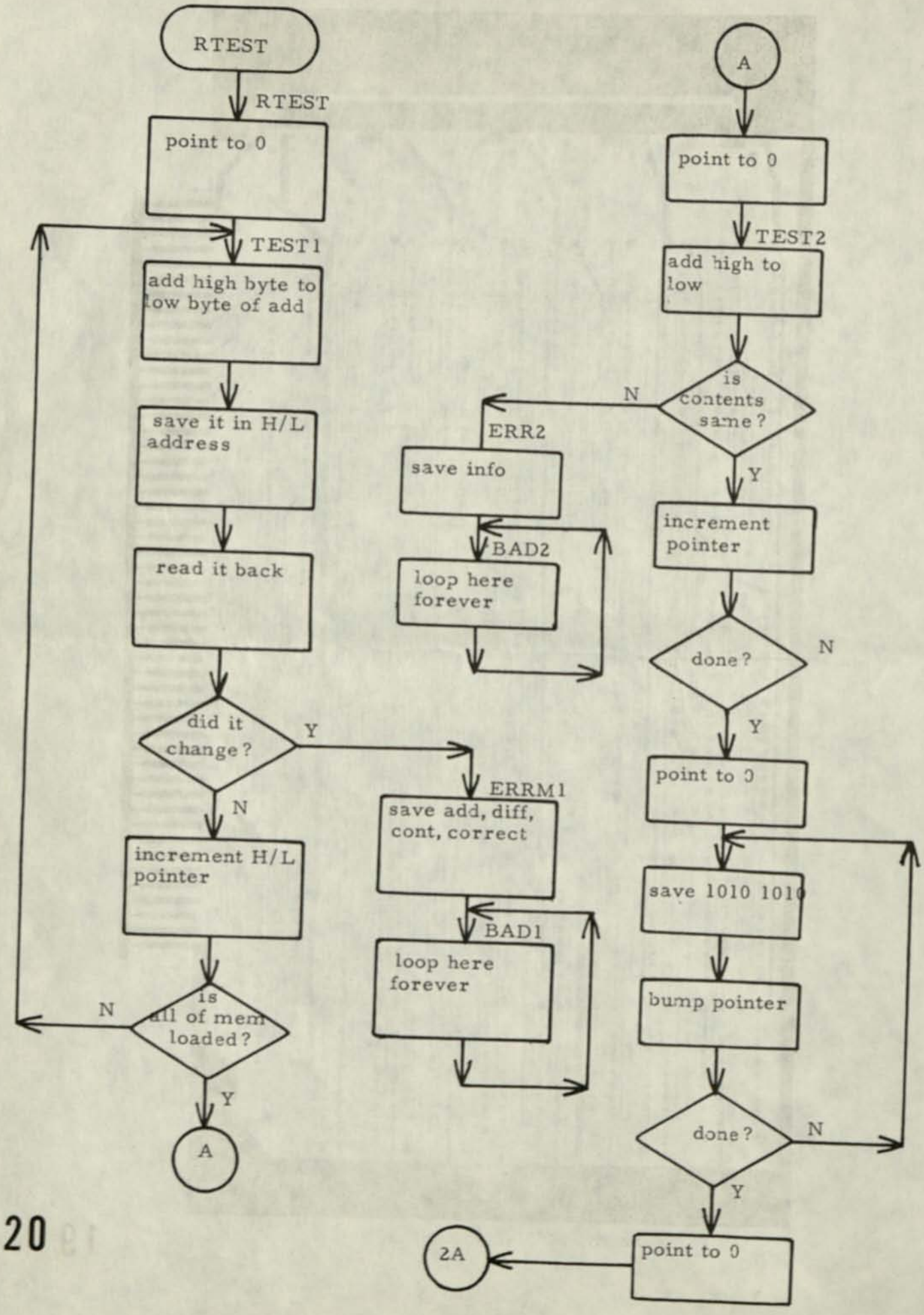
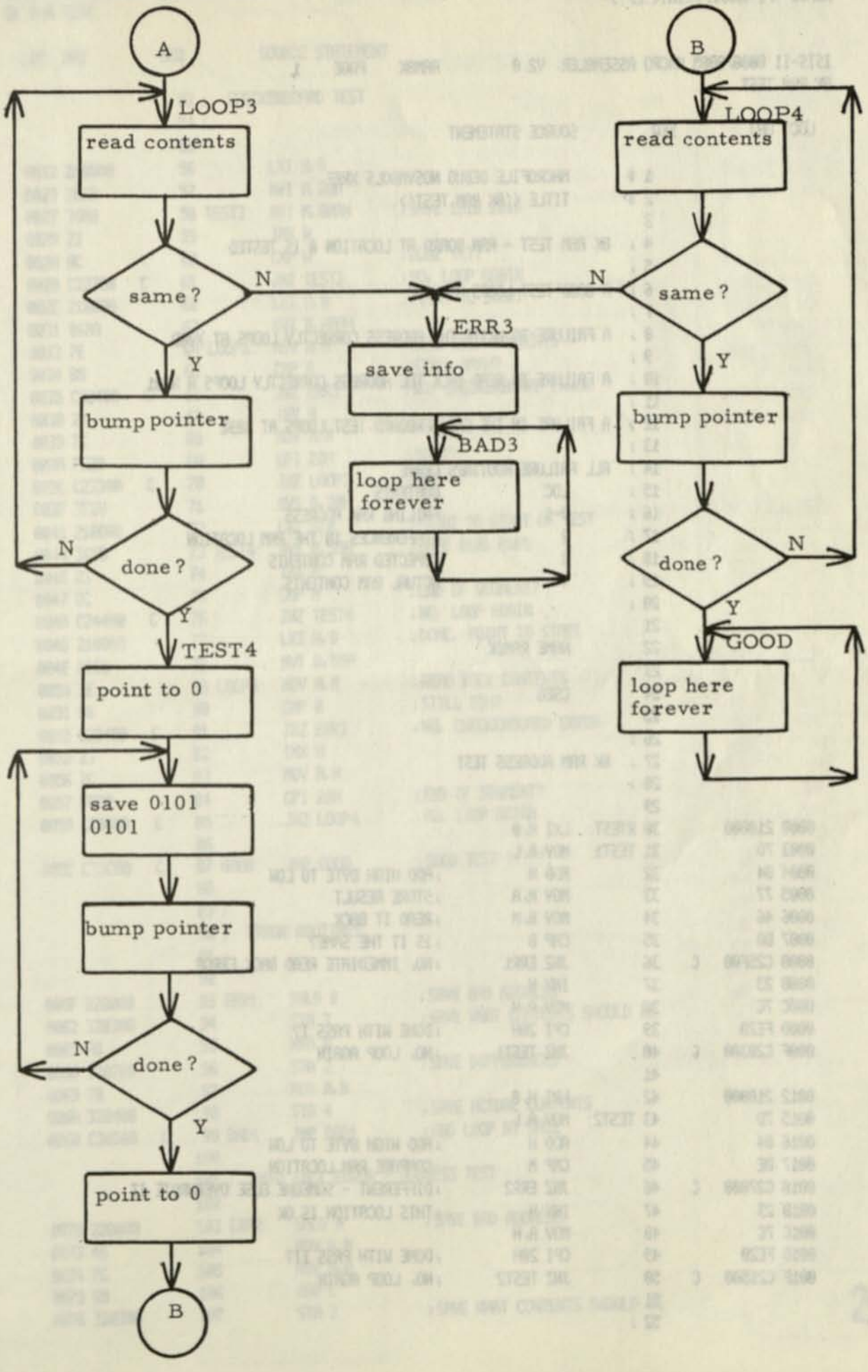


Figure 9B. MEM-2 Trace Side


RTEST
RTEST
point to 0
TEST1
add high byte to low byte of add
save it in H/L address
read it back
did it change?
Y
N
ERRM1
save add, diff, cont, correct
BAD1
loop here forever
increment H/L pointer
is all of mem loaded?
N
Y
A
A
point to 0
TEST2
add high to low
is contents same?
N
ERR2
save info
BAD2
loop here forever
Y
increment pointer
done?
N
Y
point to 0
save 1010 1010
bump pointer
done?
N
Y
point to 0
2A


A
LOOP3
read contents
same?
N
Y
bump pointer
done?
N
Y
TEST4
point to 0
save 0101
0101
bump pointer
done?
N
Y
point to 0
B
ERR3
save info
BAD3
loop here
forever
B
LOOP4
read contents
same?
N
Y
bump pointer
done?
N
Y
GOOD
loop here
forever

```
RSM80 :F1:8KRAM PRINT(:LP:)


ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        RAM8K    PAGE   1
8K RAM TEST

 LOC  OBJ        SEQ        SOURCE STATEMENT

                    1 $       MACROFILE DEBUG NOSYMBOLS XREF
                    2 $       TITLE ('8K RAM TEST')
                    3
                    4 ;  8K RAM TEST - RAM BOARD AT LOCATION 0 IS TESTED
                    5 ;
                    6 ;  A GOOD TEST LOOPS AT X05C
                    7 ;
                    8 ;  A FAILURE TO WRITE THE ADDRESS CORRECTLY LOOPS AT X06D
                    9 ;
                   10 ;  A FAILURE TO READ BACK THE ADDRESS CORRECTLY LOOPS A X081
                   11 ;
                   12 ;  A FAILURE IN THE CHECKERBOARD TEST LOOPS AT X092
                   13 ;
                   14 ;  ALL FAILURE ROUTINES LEAVE
                   15 ;       LOC             CONTENTS
                   16 ;       0-1             FAILING RAM ADDRESS
                   17 ;       2               DIFFERENCES IN THE RAM LOCATION
                   18 ;       3               EXPECTED RAM CONTENTS
                   19 ;       4               ACTUAL RAM CONTENTS
                   20 ;
                   21
                   22         NAME RAM8K
                   23
                   24         CSEG
                   25
                   26 ;
                   27 ;  8K RAM ADDRESS TEST
                   28 ;
                   29
0000 210000        30 RTEST:  LXI H,0
0003 7D            31 TEST1:  MOV A,L
0004 84            32         ADD H          ;ADD HIGH BYTE TO LOW
0005 77            33         MOV M,A        ;STORE RESULT
0006 46            34         MOV B,M        ;READ IT BACK
0007 B8            35         CMP B          ;IS IT THE SAME?
0008 C25F00   C    36         JNZ ERR1       ;NO, IMMEDIATE READ BACK ERROR
000B 23            37         INX H
000C 7C            38         MOV A,H
000D FE20          39         CPI 20H        ;DONE WITH PASS I?
000F C20300   C    40         JNZ TEST1      ;NO, LOOP AGAIN
                   41
0012 210000        42         LXI H,0
0015 7D            43 TEST2:  MOV A,L
0016 84            44         ADD H          ;ADD HIGH BYTE TO LOW
0017 BE            45         CMP M          ;COMPARE RAM LOCATION
0018 C27000   C    46         JNZ ERR2       ;DIFFERENT - SOMEONE ELSE OVERWROTE IT
001B 23            47         INX H          ;THIS LOCATION IS OK
001C 7C            48         MOV A,H
001D FE20          49         CPI 20H        ;DONE WITH PASS II?
001F C21500   C    50         JNZ TEST2      ;NO, LOOP AGAIN
                   51
                   52 ;
```

```
LOC  OBJ          SEQ        SOURCE STATEMENT

                    53 ;  CHECKERBOARD TEST
                    54 ;
                    55
0022 210000         56         LXI H,0
0025 3E20           57         MVI A,20H
0027 36AA           58 TEST3:  MVI M,0AAH     ;SAVE 1010 1010
0029 23             59         INX H
002A BC             60         CMP H          ;DONE YET?
002B C22700    C    61         JNZ TEST3      ;NO, LOOP AGAIN
002E 210000         62         LXI H,0        ;POINT TO START
0031 06AA           63         MVI B,0AAH
0033 7E             64 LOOP3:  MOV A,M        ;READ BACK CONTENTS
0034 B8             65         CMP B          ;STILL 0AAH?
0035 C23400    C    66         JNZ ERR3       ;NO, CHECKERBOARD ERROR
0038 23             67         INX H
0039 7C             68         MOV A,H
003A FE20           69         CPI 20H        ;DONE?
003C C23300    C    70         JNZ LOOP3      ;NO
003F 3E20           71         MVI A,20H
0041 210000         72         LXI H,0        ;POINT TO START OF TEST
0044 3655           73 TEST4:  MVI M,55H      ;SAVE 0101 0101
0046 23             74         INX H
0047 BC             75         CMP H          ;END OF SEGMENT?
0048 C24400    C    76         JNZ TEST4      ;NO, LOOP AGAIN
004B 210000         77         LXI H,0        ;DONE, POINT TO START
004E 0655           78         MVI B,55H
0050 7E             79 LOOP4:  MOV A,M        ;READ BACK CONTENTS
0051 B8             80         CMP B          ;STILL 55H?
0052 C23400    C    81         JNZ ERR3       ;NO, CHECKERBOARD ERROR
0055 23             82         INX H
0056 7C             83         MOV A,H
0057 FE20           84         CPI 20H        ;END OF SEGMENT?
0059 C25000    C    85         JNZ LOOP4      ;NO, LOOP AGIAN
                    86
005C C35C00    C    87 GOOD:   JMP GOOD       ;GOOD TEST !!!!!!
                    88
                    89 ;
                    90 ;  ERROR ROUTINES
                    91 ;
                    92
005F 220000         93 ERR1:   SHLD 0         ;SAVE BAD ADDRESS
0062 320300         94         STA 3          ;SAVE WHAT CONTENTS SHOULD BE
0065 A8             95         XRA B
0066 320200         96         STA 2          ;SAVE DIFFERENCES
0069 78             97         MOV A,B
006A 320400         98         STA 4          ;SAVE ACTUAL CONTENTS
006D C36D00    C    99 BAD1:   JMP BAD1       ;AND LOOP AT BAD1
                   100
                   101 ;  READ BACK ERROR - ADDRESS TEST
                   102
0070 220000        103 ERR2:   SHLD 0         ;SAVE BAD ADDRESS
0073 46            104         MOV B,M
0074 7C            105         MOV A,H
0075 85            106         ADD L
0076 320300        107         STA 3          ;SAVE WHAT CONTENTS SHOULD BE
```

8K RAM TEST

```
LOC  OBJ        SEQ        SOURCE STATEMENT

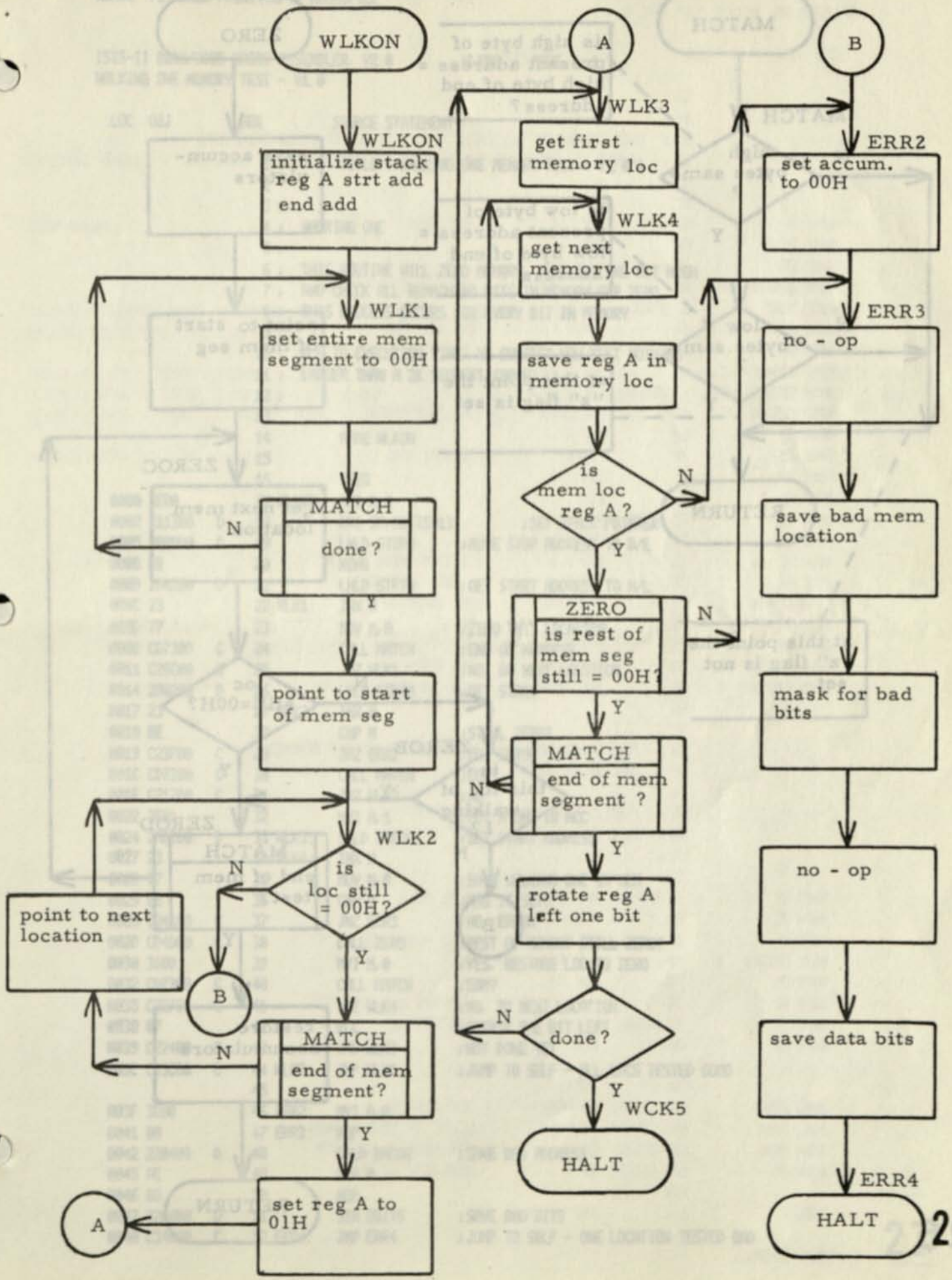
0079 A8          108        XRA B
007A 320200      109        STA 2          ;SAVE DIFFERENCES
007D 78          110        MOV A,B
007E 320400      111        STA 4          ;SAVE ACTUAL CONTENTS
0081 C38100   C  112 BAD2:   JMP BAD2       ;AND LOOP AT BAD2
                 113
                 114 ; CHECKERBOARD ERROR
                 115
0084 220000      116 ERR3:   SHLD 0         ;SAVE BAD ADDRESS
0087 320400      117        STA 4          ;SAVE ACTUAL CONTENTS
008A A8          118        XRA B
008B 320200      119        STA 2          ;SAVE DIFFERENCES
008E 78          120        MOV A,B
008F 320300      121        STA 3          ;SAVE WHAT CONTENTS SHOULD BE
0092 C39200   C  122 BAD3:   JMP BAD3       ;AND LOOP AT BAD3
                 123
                 124        END

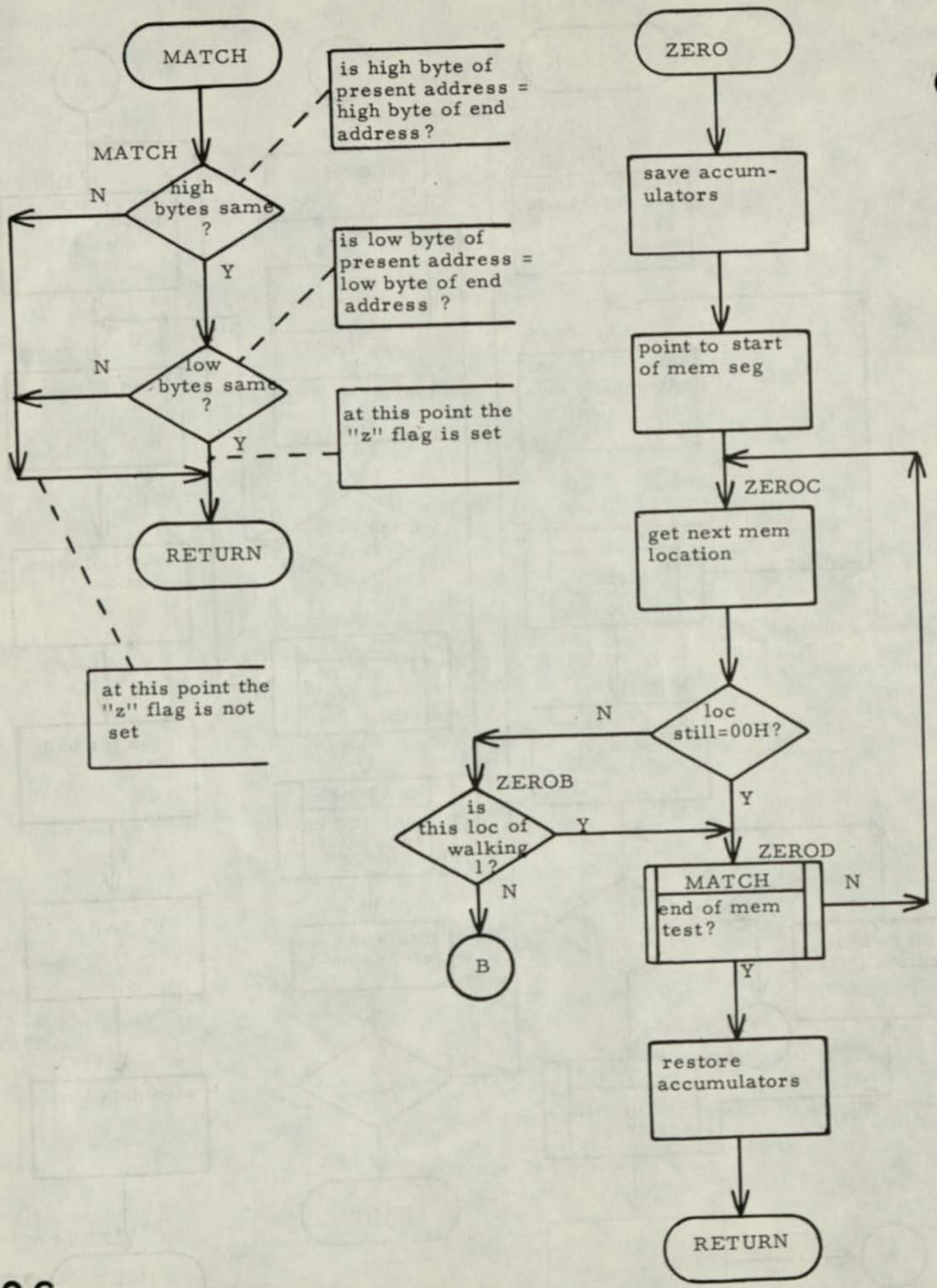
ASSEMBLY COMPLETE,  NO ERRORS
```

ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V2.0

```
BAD1     99#   99
BAD2    112#  112
BAD3    122#  122
ERR1     36    93#
ERR2     46   103#
ERR3     66    81   116#
GOOD     87#   87
LOOP3    64#   78
LOOP4    79#   85
RAM8K    22
RTEST    30#
TEST1    31#   40
TEST2    43#   50
TEST3    58#   61
TEST4    73#   76
```

CROSS REFERENCE COMPLETE


WLKON
WLKON
initialize stack reg A strt add end add
WLK1
set entire mem segment to 00H
MATCH
done?
N
Y
point to start of mem seg
WLK2
is loc still = 00H?
N
Y
point to next location
B
MATCH
end of mem segment?
N
Y
set reg A to 01H
A
A
WLK3
get first memory loc
WLK4
get next memory loc
save reg A in memory loc
is mem loc reg A?
N
Y
ZERO
is rest of mem seg still = 00H?
N
Y
MATCH
end of mem segment ?
N
Y
rotate reg A left one bit
done?
N
Y
WCK5
HALT
B
ERR2
set accum. to 00H
ERR3
no - op
save bad mem location
mask for bad bits
no - op
save data bits
ERR4
HALT


MATCH
is high byte of present address = high byte of end address ?
MATCH
high bytes same ?
N
Y
is low byte of present address = low byte of end address ?
low bytes same ?
N
Y
at this point the "z" flag is set
RETURN
at this point the "z" flag is not set
ZERO
save accumulators
point to start of mem seg
ZEROC
get next mem location
loc still=00H?
N
Y
ZEROB
is this loc of walking 1?
Y
N
B
ZEROD
MATCH
end of mem test?
N
Y
restore accumulators
RETURN

```
ASM80 :F1:WLKON PRINT(:LP:) MACROFILE


ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        WLKON    PAGE    1
WALKING ONE MEMORY TEST - V1.0

 LOC  OBJ          SEQ         SOURCE STATEMENT
                     1 $        TITLE ('WALKING ONE MEMORY TEST - V1.0')
                     2
                     3 ;
                     4 ;  WALKING ONE
                     5 ;
                     6 ;  THIS ROUTINE WILL ZERO MEMORY, THEN SET ONE BIT HIGH
                     7 ;  AND CHECK ALL REMAINING BITS IN MEMORY FOR ZERO.
                     8 ;  THIS PROCESS OCCURS FOR EVERY BIT IN MEMORY.
                     9 ;
                    10 ;  DUE TO EXECUTION TIME, WE SUGGEST YOU TEST NOTHING
                    11 ;  LARGER THAN A 2K SEGMENT (800H)
                    12 ;
                    13
                    14          NAME WLKON
                    15
                    16          CSEG
0000 3E00           17 WLKON:   MVI A,0
0002 311300    D    18          LXI SP,BBITS+13         ;SET STACK POINTER
0005 2A0000    D    19          LHLD STOPA      ;MOVE STOP ADDRESS TO D/E
0008 EB             20          XCHG
0009 2A0200    D    21          LHLD STRTA      ;GET START ADDRESS TO H/L
000C 23             22 WLK1:    INX H
000D 77             23          MOV M,A         ;ZERO THIS LOCATION
000E CD7300    C    24          CALL MATCH      ;END OF MEMORY?
0011 C20C00    C    25          JNZ WLK1        ;NO, DO NEXT LOCATION
0014 2A0200    D    26          LHLD STRTA      ;GET START
0017 23             27 WLK2:    INX H
0018 BE             28          CMP M           ;STILL ZERO?
0019 C23F00    C    29          JNZ ERR2        ;NO, ERROR
001C CD7300    C    30          CALL MATCH      ;EOM?
001F C21700    C    31          JNZ WLK2        ;NO
0022 3E01           32          MVI A,1         ;PUT A ONE IN ACC
0024 2A0200    D    33 WLK3:    LHLD STRTA      ;GET START ADDRESS
0027 23             34 WLK4:    INX H
0028 77             35          MOV M,A         ;SAVE WALKING ONE IN MEM
0029 BE             36          CMP M           ;WAS IT SET?
002A C24100    C    37          JNZ ERR3        ;NO, ERROR
002D CD4D00    C    38          CALL ZERO       ;REST OF MEMORY STILL ZERO?
0030 3600           39          MVI M,0         ;YES, RESTORE LOC TO ZERO
0032 CD7300    C    40          CALL MATCH      ;EOM?
0035 C22700    C    41          JNZ WLK4        ;NO, TO NEXT LOCATION
0038 07             42          RLC             ;ROTATE ONE BIT LEFT
0039 D22400    C    43          JNC WLK3        ;NOT DONE YET
003C C33C00    C    44 WLK5:    JMP WLK5        ;JUMP TO SELF - ALL LOCS TESTED GOOD
                    45
003F 3E00           46 ERR2:    MVI A,0
0041 00             47 ERR3:    NOP
0042 220400    D    48          SHLD BADDR      ;SAVE BAD ADDRESS
0045 AE             49          XRA M
0046 00             50          NOP
0047 320600    D    51          STA BBITS       ;SAVE BAD BITS
004A C34A00    C    52 ERR4:    JMP ERR4        ;JUMP TO SELF - ONE LOCATION TESTED BAD
```

```
LOC  OBJ          SEQ        SOURCE STATEMENT

                    53
                    54 ;
                    55 ;  THIS SUBROUTINE WLL CHECK MEMORY TO SEE IF IT IS STILL ZERO.
                    56 ;  IF NOT, IT CHECKS TO SEE IF THIS IS OUR WALKING ONE LOCATION.
                    57 ;
                    58
004D 4F             59 ZERO:   MOV C,A          ;SAVE REGS
004E C5             60         PUSH B
004F E5             61         PUSH H
0050 2A0200   D     62         LHLD STRTA       ;POINT TO START OF MEM
0053 3E00           63 ZEROC:  MVI A,0
0055 23             64         INX H            ;GET NEXT LOC
0056 BE             65         CMP M            ;ZERO?
0057 C26400   C     66         JNZ ZEROB        ;NO
005A CD7300   C     67 ZEROD:  CALL MATCH        ;EOM?
005D C25300   C     68         JNZ ZEROC        ;NO, DO SOMEMORE
0060 E1             69         POP H
0061 C1             70         POP B            ;RESTORE REGS
0062 79             71         MOV A,C
0063 C9             72         RET
0064 C1             73 ZEROB:  POP B
0065 C5             74         PUSH B
0066 7C             75         MOV A,H          ;IS THIS WHERE WALKING
0067 B8             76         CMP B            ;  ONE IS STORED?
0068 C23F00   C     77         JNZ ERR2         ;NO, ERROR #2
006B 7D             78         MOV A,L          ;MAYBE
006C B9             79         CMP C
006D C23F00   C     80         JNZ ERR2         ;NO, ERROR #2
0070 C35A00   C     81         JMP ZEROD        ;YES, DO NEXT LOCATION
                    82
                    83 ;
                    84 ;  THIS SUBROUTINE WILL DETERMINE IF WE HAVE REACHED
                    85 ;  THE END OF MEMORY
                    86 ;
                    87 ;  FLAG Z=0 IF NOT END OF MEMORY
                    88 ;  FLAG Z=1 IF END OF MEMORY
                    89 ;
                    90
0073 47             91 MATCH:  MOV B,A          ;SAVE ACC
0074 7C             92         MOV A,H
0075 BA             93         CMP D            ;DOES HIGH BYTE MATCH?
0076 C27B00   C     94         JNZ MTCHA        ;NO
0079 7D             95         MOV A,L
007A B8             96         CMP E            ;COMPARE WITH LOW BYTE
007B 78             97 MTCHA:  MOV A,B          ;RESTORE ACC
007C C9             98         RET
                    99
                   100         DSEG
0000 FF07          101 STOPA:  DW 7FFH          ;END ADDRESS
0002 9600          102 STRTA:  DW 96H           ;START OF TEST SEGMENT - 1
0004 0000          103 BADDR:  DW 0             ;BAD ADDRESS LOCATION
0006 00            104 BBITS:  DB 0             ;BAD BITS LOCATION
                   105
0000          C    106         END WLKON

PUBLIC SYMBOLS
```

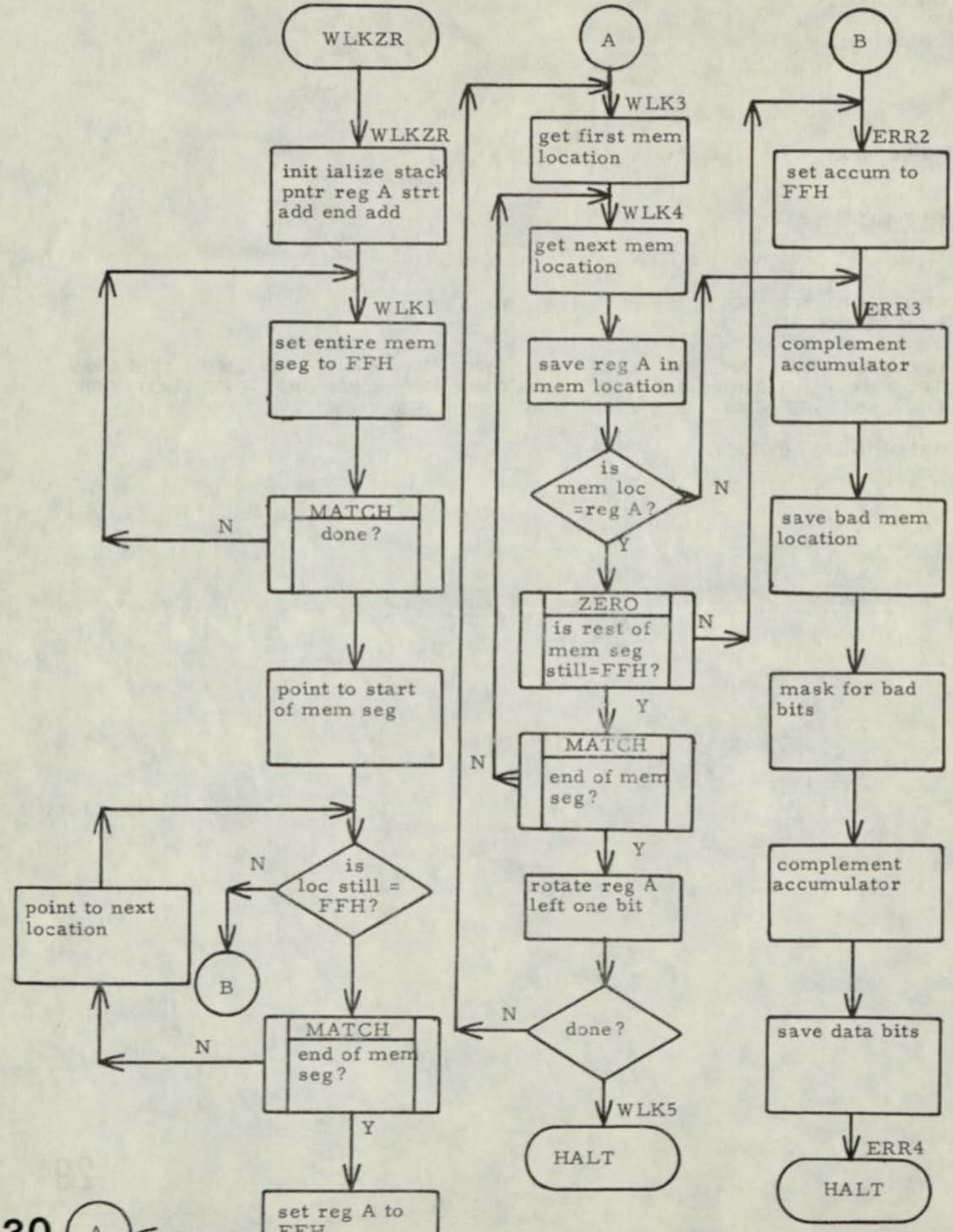
EXTERNAL SYMBOLS

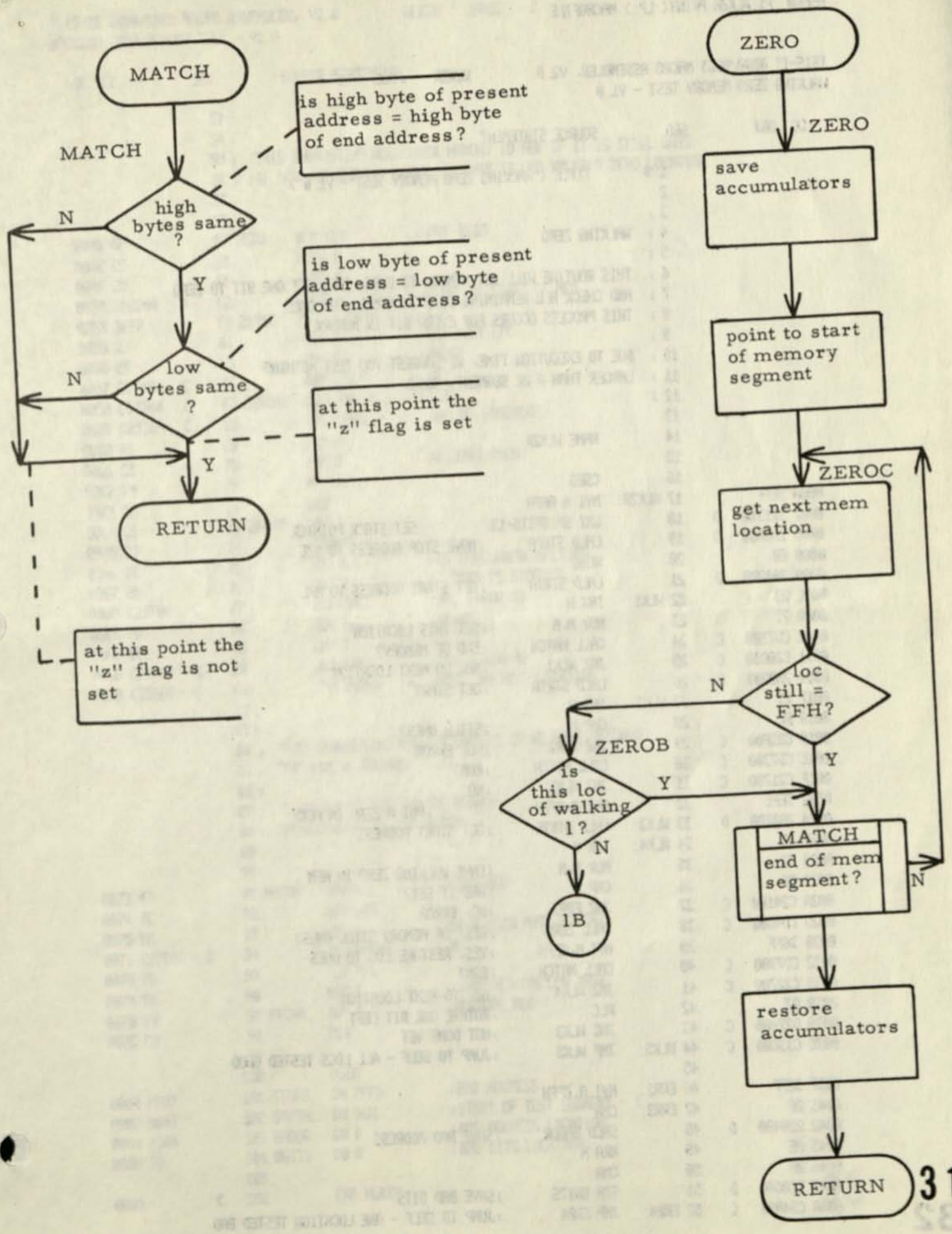
USER SYMBOLS

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        WLKON    PAGE    3
WALKING ONE MEMORY TEST - V1.0

BADDR  D 0004   BBITS  D 0006   ERR2   C 003F   ERR3   C 0041   ERR4   C 004A   MATCH  C 0073   MTCHA  C 007B
STOPA  D 0000   STRTA  D 0002   WLK1   C 000C   WLK2   C 0017   WLK3   C 0024   WLK4   C 0027   WLK5   C 003C
WLKON  C 0000   ZERO   C 004D   ZEROB  C 0064   ZEROC  C 0053   ZEROD  C 005A

ASSEMBLY COMPLETE,  NO ERRORS
```


WLKZR
WLKZR
init ialize stack pntr reg A strt add end add
WLK1
set entire mem seg to FFH
MATCH
done?
N
point to start of mem seg
point to next location
N
is loc still = FFH?
B
MATCH
end of mem seg?
N
Y
set reg A to FEH
A
A
WLK3
get first mem location
WLK4
get next mem location
save reg A in mem location
is mem loc =reg A?
N
Y
ZERO
is rest of mem seg still=FFH?
N
Y
MATCH
end of mem seg?
N
Y
rotate reg A left one bit
done?
N
WLK5
HALT
B
ERR2
set accum to FFH
ERR3
complement accumulator
save bad mem location
mask for bad bits
complement accumulator
save data bits
ERR4
HALT


MATCH
MATCH
high bytes same ?
N
Y
is high byte of present address = high byte of end address?
low bytes same ?
N
Y
is low byte of present address = low byte of end address?
at this point the "z" flag is set
RETURN
at this point the "z" flag is not set
ZERO
ZERO
save accumulators
point to start of memory segment
ZEROC
get next mem location
loc still = FFH?
N
Y
ZEROB
is this loc of walking 1?
Y
N
1B
MATCH
end of mem segment?
N
restore accumulators
RETURN

```
ASM80 :F1:WLKZR PRINT(:LP:) MACROFILE


ISIS-II 8080/8085 MACRO ASSEMBLER, V2.0        WLKZR   PAGE   1
WALKING ZERO MEMORY TEST - V1.0

 LOC  OBJ          SEQ        SOURCE STATEMENT

                     1 $       TITLE ('WALKING ZERO MEMORY TEST - V1.0')
                     2
                     3 ;
                     4 ;  WALKING ZERO
                     5 ;
                     6 ;  THIS ROUTINE WILL SET MEMORY TO ONES, THEN SET ONE BIT TO ZERO
                     7 ;  AND CHECK ALL REMAINING BITS IN MEMORY FOR ONES.
                     8 ;  THIS PROCESS OCCURS FOR EVERY BIT IN MEMORY.
                     9 ;
                    10 ;  DUE TO EXECUTION TIME, WE SUGGEST YOU TEST NOTHING
                    11 ;  LARGER THAN A 2K SEGMENT (800H)
                    12 ;
                    13
                    14         NAME WLKZR
                    15
                    16         CSEG
0000 3EFF           17 WLKZR:  MVI A,0FFH
0002 311300    D    18         LXI SP,BBITS+13          ;SET STACK POINTER
0005 2A0000    D    19         LHLD STOPA       ;MOVE STOP ADDRESS TO D/E
0008 EB             20         XCHG
0009 2A0200    D    21         LHLD STRTA       ;GET START ADDRESS TO H/L
000C 23             22 WLK1:   INX H
000D 77             23         MOV M,A          ;SET THIS LOCATION
000E CD7300    C    24         CALL MATCH       ;END OF MEMORY?
0011 C20C00    C    25         JNZ WLK1         ;NO, DO NEXT LOCATION
0014 2A0200    D    26         LHLD STRTA       ;GET START
0017 23             27 WLK2:   INX H
0018 BE             28         CMP M            ;STILL ONES?
0019 C23F00    C    29         JNZ ERR2         ;NO, ERROR
001C CD7300    C    30         CALL MATCH       ;EOM?
001F C21700    C    31         JNZ WLK2         ;NO
0022 3EFE           32         MVI A,0FEH               ;PUT A ZERO IN ACC
0024 2A0200    D    33 WLK3:   LHLD STRTA       ;GET START ADDRESS
0027 23             34 WLK4:   INX H
0028 77             35         MOV M,A          ;SAVE WALKING ZERO IN MEM
0029 BE             36         CMP M            ;WAS IT SET?
002A C24100    C    37         JNZ ERR3         ;NO, ERROR
002D CD4D00    C    38         CALL ZERO        ;REST OF MEMORY STILL ONES?
0030 36FF           39         MVI M,0FFH       ;YES, RESTORE LOC TO ONES
0032 CD7300    C    40         CALL MATCH       ;EOM?
0035 C22700    C    41         JNZ WLK4         ;NO, TO NEXT LOCATION
0038 07             42         RLC              ;ROTATE ONE BIT LEFT
0039 D22400    C    43         JNC WLK3         ;NOT DONE YET
003C C33C00    C    44 WLK5:   JMP WLK5         ;JUMP TO SELF - ALL LOCS TESTED GOOD
                    45
003F 3EFF           46 ERR2:   MVI A,0FFH
0041 2F             47 ERR3:   CMA
0042 220400    D    48         SHLD BADDR       ;SAVE BAD ADDRESS
0045 AE             49         XRA M
0046 2F             50         CMA
0047 320600    D    51         STA BBITS        ;SAVE BAD BITS
004A C34A00    C    52 ERR4:   JMP ERR4         ;JUMP TO SELF - ONE LOCATION TESTED BAD
```

```
LOC  OBJ              SEQ     SOURCE STATEMENT

                       53
                       54 ;
                       55 ;  THIS SUBROUTINE WLL CHECK MEMORY TO SEE IF IT IS STILL ONES.
                       56 ;  IF NOT, IT CHECKS TO SEE IF THIS IS OUR WALKING ZERO LOCATION.
                       57 ;
                       58
004D 4F                59 ZERO:   MOV C,A          ;SAVE REGS
004E C5                60         PUSH B
004F E5                61         PUSH H
0050 2A0200    D       62         LHLD STRTA       ;POINT TO START OF MEM
0053 3EFF              63 ZEROC:  MVI A,0FFH
0055 23                64         INX H            ;GET NEXT LOC
0056 BE                65         CMP M            ;ONES?
0057 C26400    C       66         JNZ ZEROB        ;NO
005A CD7300    C       67 ZEROD:  CALL MATCH       ;EOM?
005D C25300    C       68         JNZ ZEROC        ;NO, DO SOMEMORE
0060 E1                69         POP H
0061 C1                70         POP B            ;RESTORE REGS
0062 79                71         MOV A,C
0063 C9                72         RET
0064 C1                73 ZEROB:  POP B
0065 C5                74         PUSH B
0066 7C                75         MOV A,H          ;IS THIS WHERE WALKING
0067 B8                76         CMP B            ;  ZERO IS STORED?
0068 C23F00    C       77         JNZ ERR2         ;NO, ERROR #2
006B 7D                78         MOV A,L          ;MAYBE
006C B9                79         CMP C
006D C23F00    C       80         JNZ ERR2         ;NO, ERROR #2
0070 C35A00    C       81         JMP ZEROD        ;YES, DO NEXT LOCATION
                       82
                       83 ;
                       84 ;  THIS SUBROUTINE WILL DETERMINE IF WE HAVE REACHED
                       85 ;  THE END OF MEMORY
                       86 ;
                       87 ;  FLAG Z=0 IF NOT END OF MEMORY
                       88 ;  FLAG Z=1 IF END OF MEMORY
                       89 ;
                       90
0073 47                91 MATCH:  MOV B,A          ;SAVE ACC
0074 7C                92         MOV A,H
0075 BA                93         CMP D            ;DOES HIGH BYTE MATCH?
0076 C27B00    C       94         JNZ MTCHA        ;NO
0079 7D                95         MOV A,L
007A BB                96         CMP E            ;COMPARE WITH LOW BYTE
007B 78                97 MTCHA:  MOV A,B          ;RESTORE ACC
007C C9                98         RET
                       99
                      100         DSEG
0000 FF07             101 STOPA:  DW 7FFH          ;END ADDRESS
0002 9600             102 STRTA:  DW 96H           ;START OF TEST SEGMENT - 1
0004 0000             103 BADDR:  DW 0             ;BAD ADDRESS LOCATION
0006 00               104 BBITS:  DB 0             ;BAD BITS LOCATION
                      105
0000           C      106         END WLKZR

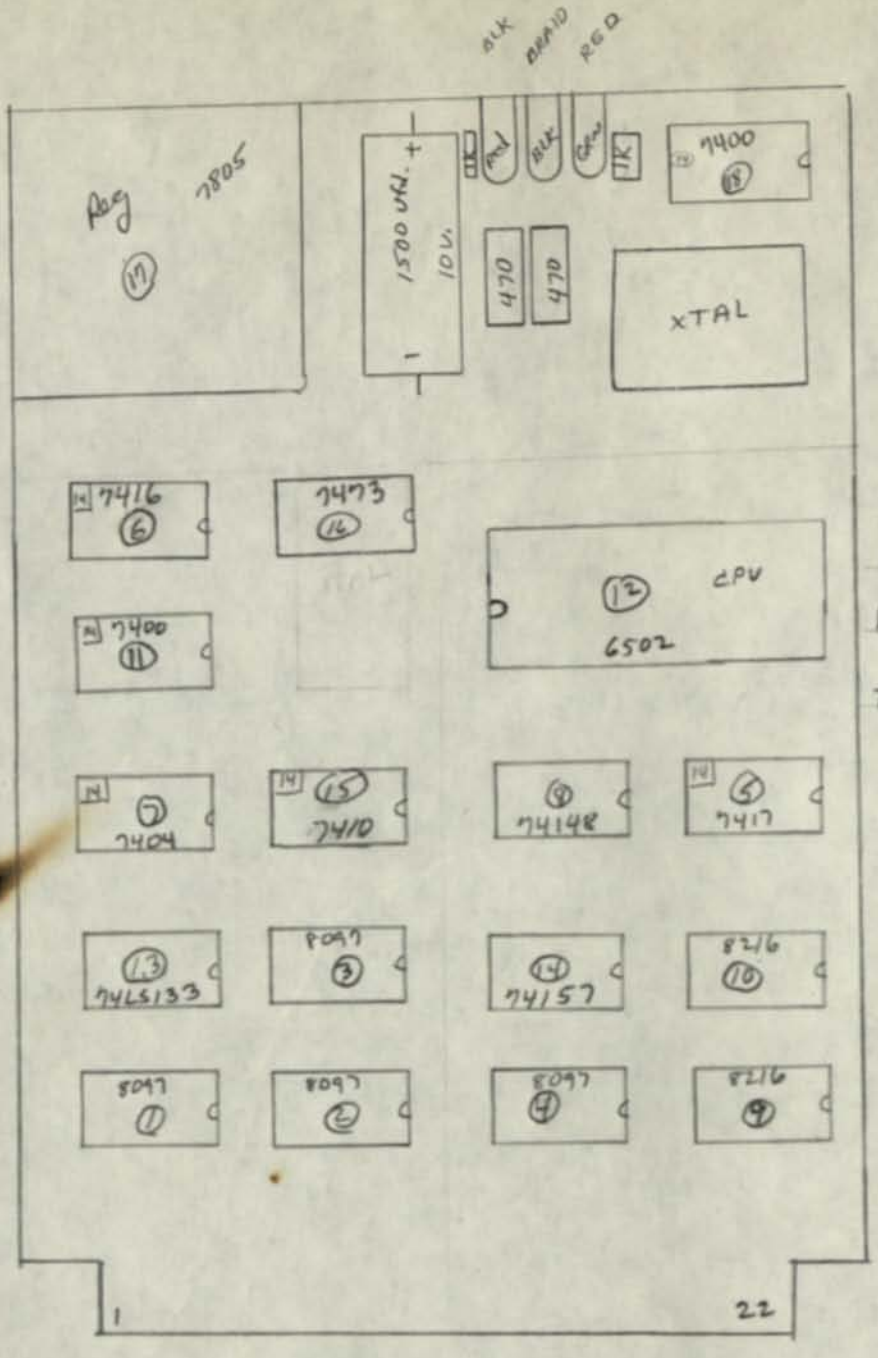
PUBLIC SYMBOLS
```

EXTERNAL SYMBOLS

USER SYMBOLS

BADDR	D	0004	BBITS	D	0006	ERR2	C	003F	ERR3	C	0041	ERR4	C	004A	MATCH	C	0073	MTCHA	C	007B
STOPA	D	0000	STRTA	D	0002	WLK1	C	000C	WLK2	C	0017	WLK3	C	0024	WLK4	C	0027	WLK5	C	003C
WLKZR	C	0000	ZERO	C	004D	ZEROB	C	0064	ZEROC	C	0053	ZEROD	C	005A						

ASSEMBLY COMPLETE, NO ERRORS


BLK
BRN
RED
Reg
7805
1500 uf.
10v.
+
-
BRN
BLK
ORN
1K
7400
470
470
XTAL
7416
7473
CPU
6502
NOTE: 6502 is
Reversed w/respect
TO others
7400
7404
7410
74148
7417
74LS133
8097
74157
8216
1
22

2.094 mHz.

XTAL

Reset

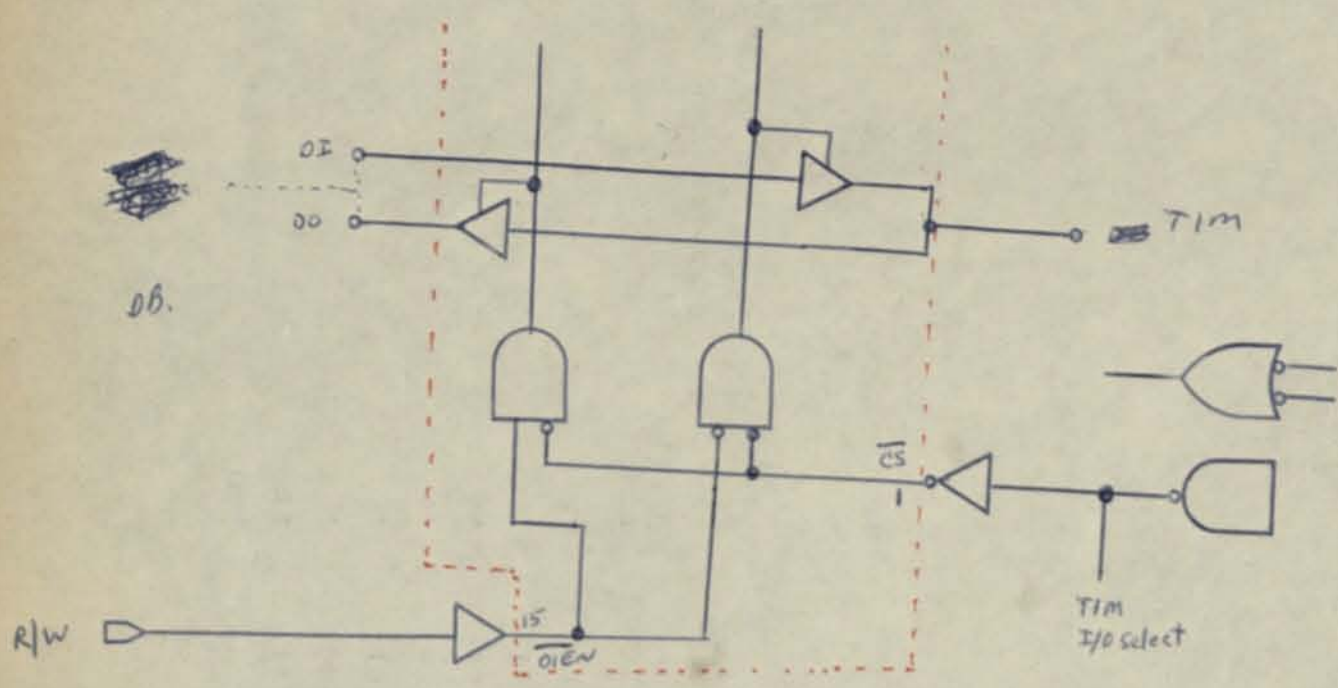
IRQ	Vector Thru:
6	FFE0 - FFE1
5	FFE2 - FFE3
4	FFE4 - FFE5
3	FFE6 - FFE7
2	FFE8 - FFE9
1	FFEA - FFEB

FFFE/FFFF decode

1500 uFd. 10V.

.1 on each IC

8216 P. 8-96 INTEL Manual



2 used

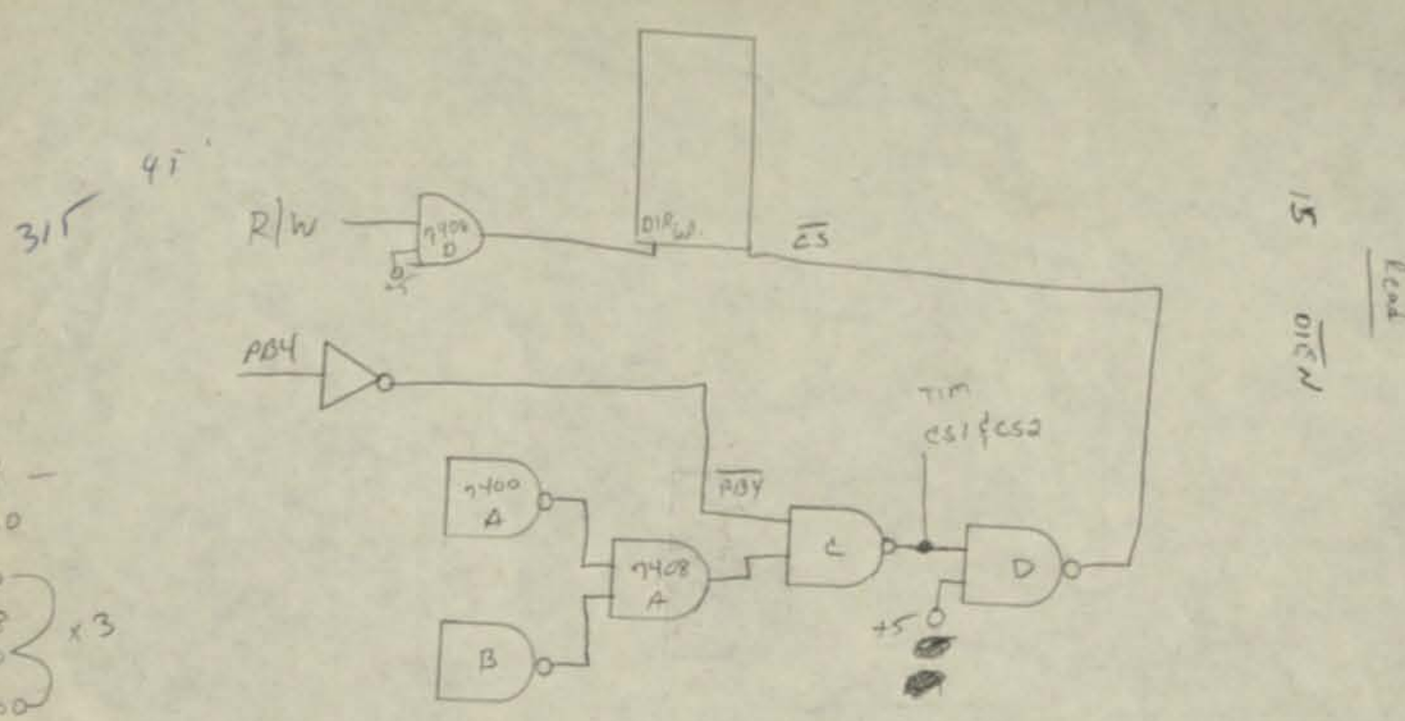
P. 65 data Sales

AM8216 # 2.20

P. 65

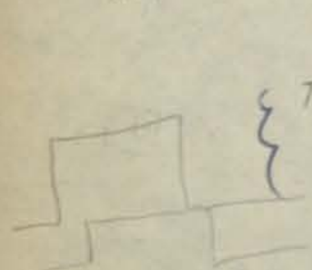
4 qty

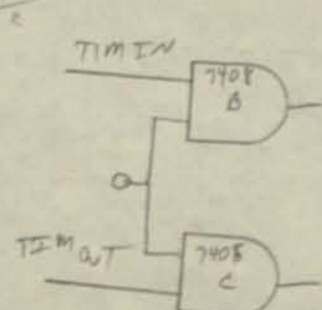
AMD



7404 —
74260
7400
7408 } x3
7400
7400

7400 22 66 ma 36
7404 22 15
27 15
5
120 nsec

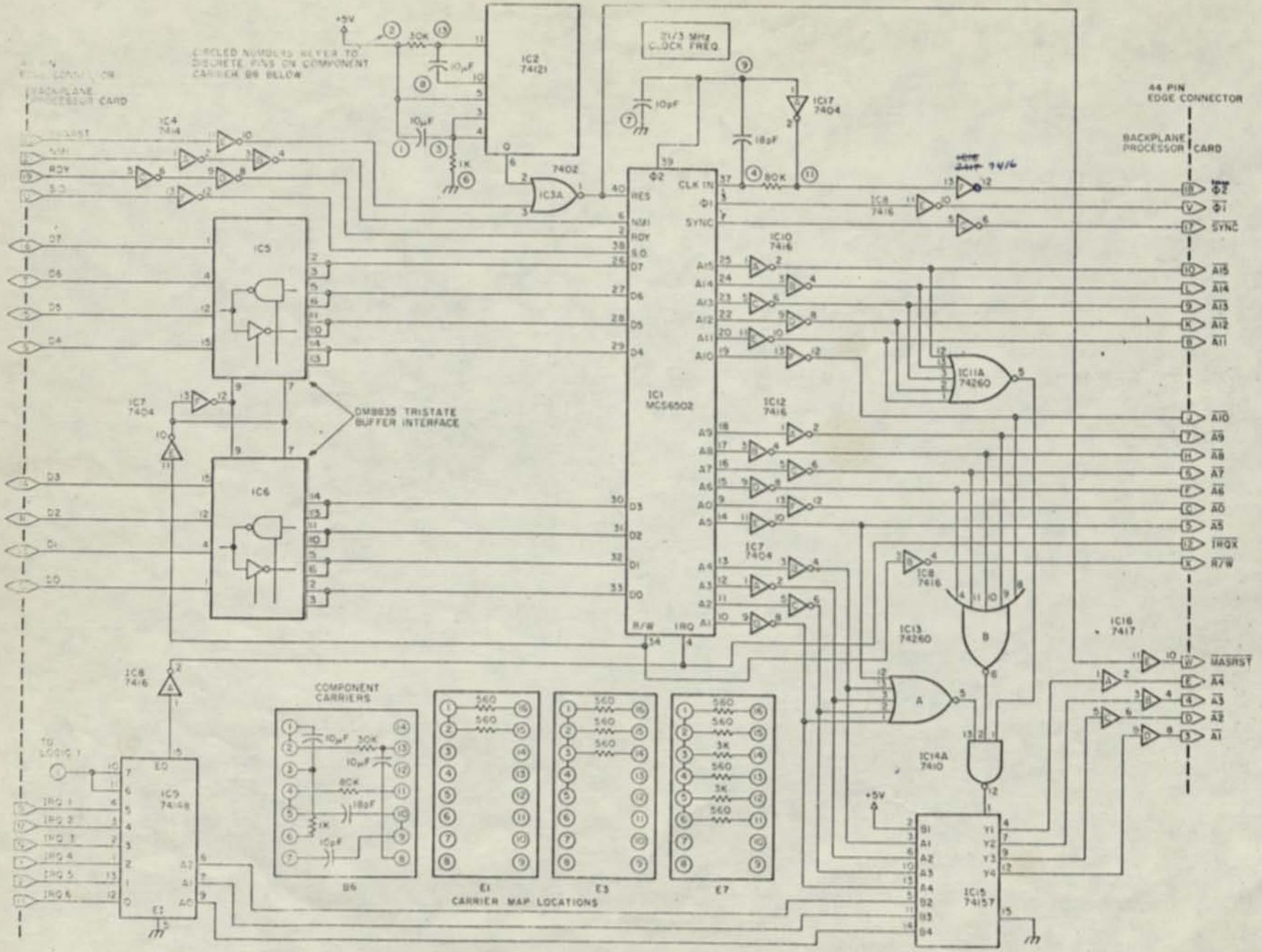




Parts List - IC's CPU Board

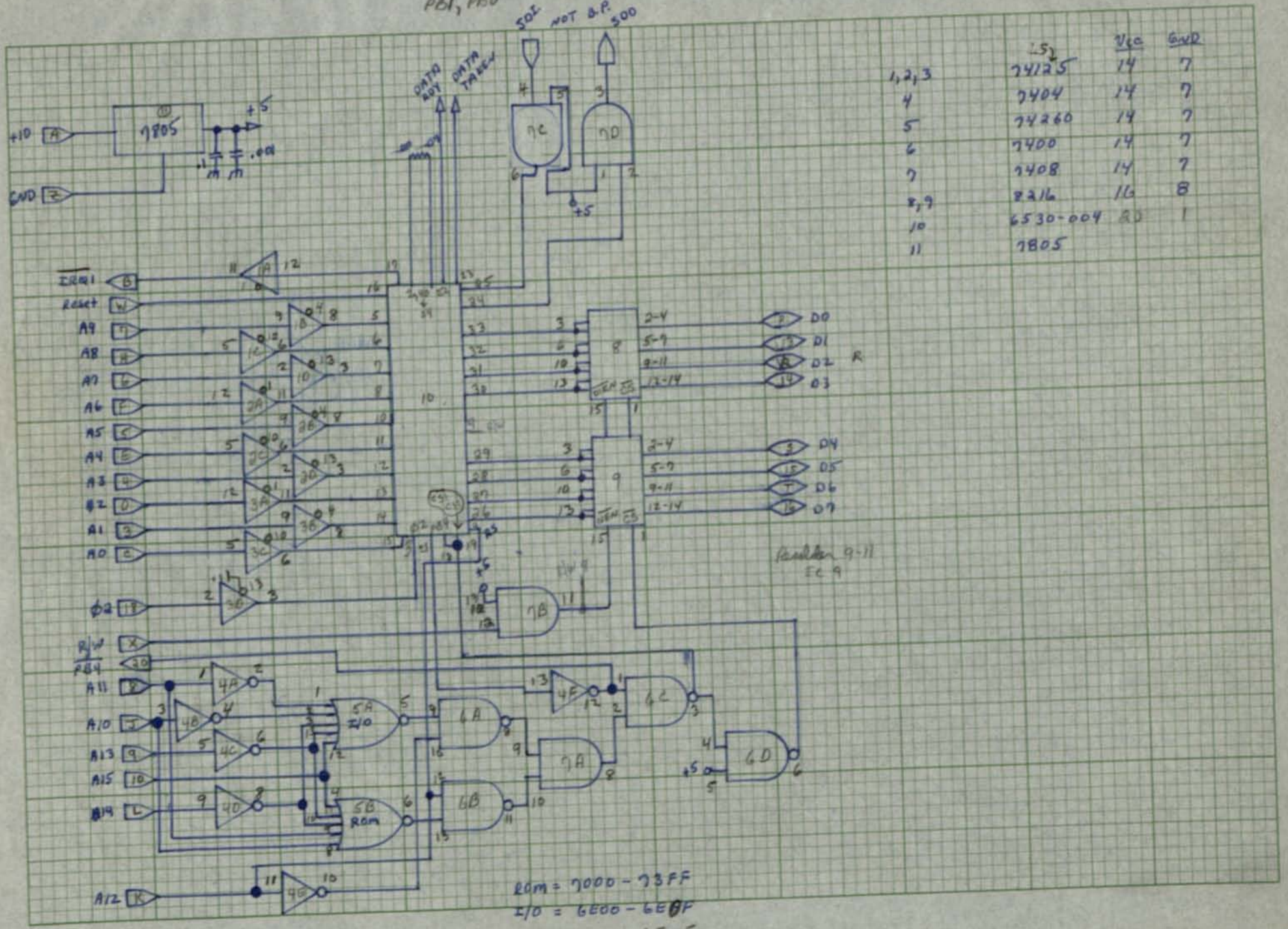
Ref. #	IC	Vcc	Gnd
1,2,3,4	8097	16	8
5	7417	14	7
6	7416	14	7
7	74L04	14	7
8	74148	16	8
9,10	8216	16	8
11	74LS00	14	7
12	6502	8	1,21
13	74LS133	16	8
14	74157	16	8
15	74LS10	14	7
16	7473	4	11
17	7805		
18	7400	14	7

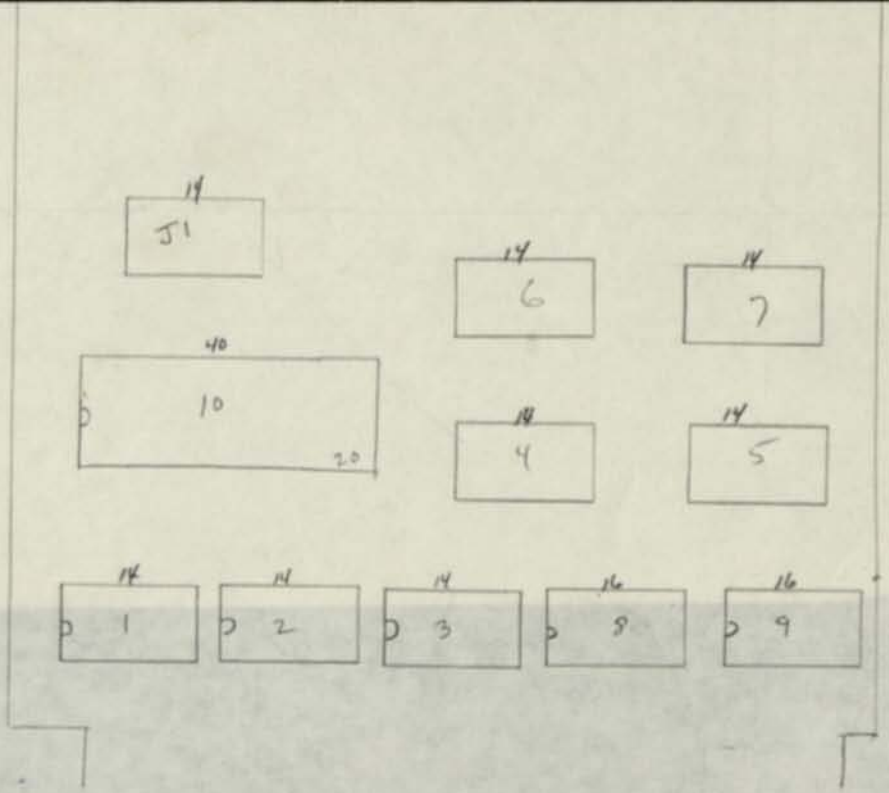
	IRQ	Vector Thru:
Lowest Priority	1	FFEA - FFEB
	2	FFE8 - FFE9
	3	FFE6 - FFE7
	4	FFE4 - FFE5
	5	FFE2 - FFE3
Highest Priority	6	FFE0 - FFE1


CIRCLED NUMBERS REFER TO DISCRETE PINS ON COMPONENT CARRIERS B6 BELOW
BACKPLANE PROCESSOR CARD
+5V
IC2 74121
IC4 7414
IC3A 7402
IC7 7404
IC1 MCS6502
IC5
IC6
OM8835 TRISTATE BUFFER INTERFACE
IC10 7416
IC12 7416
IC11A 74260
IC13 74260
IC8 7416
IC14A 7410
IC16 7417
IC15 74157
IC9 74148
44 PIN EDGE CONNECTOR
BACKPLANE PROCESSOR CARD
COMPONENT CARRIERS
B6
E1
E3
E7
CARRIER MAP LOCATIONS
MASRST
SYNC
R/W
IRQX

TIM - A4

Pin 24 & 25
PB1, PB0




14
J1
14
6
14
7
40
10
20
14
4
14
5
14
1
14
2
14
3
16
8
16
9

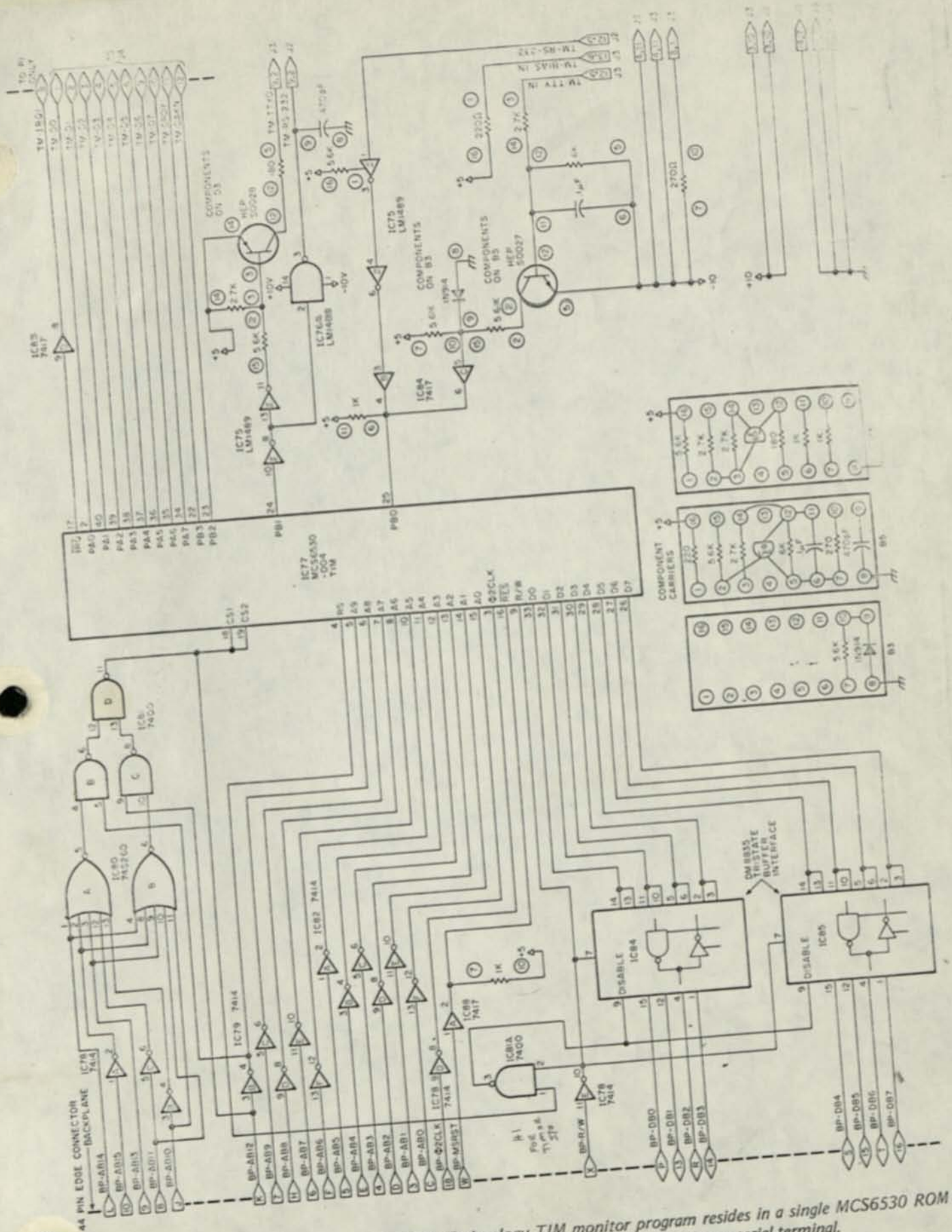


Figure 4.1: TIM interface module details. The MOS Technology TIM monitor program resides in a single MCS6530 ROM and peripheral interface circuit. The TIM interface module allows Kompuutar to be used with any serial terminal.

Wiring & Bus List

CPU & TIM board

PUTAR's BUS

NOT memory Bds

A	+10 UNREG	1	+12 Reg
B	IRQ 1	2	IRQ 5
C	A0	3	A1
D	A2	4	A3
E	A4	5	A5
F	A6	6	A7
H	A8	7	A9
J	A10	8	A11
K	A12	9	A13
L	A14	10	A15
M	IRQ 2	11	IRQ 6
N	IRQ 3	12	INTA (INT Pending)
P	D0	13	D1
R	D2	14	D3
S	D4	15	D5
T	D6	16	D7
U	500 KHZ	17	SYNC
V	ϕ1CLK	18	ϕ2 CLK
W	MASRST	19	RDY
X	R/W	20	$\overline{\text{PB4}}$
Y	IRQ 4	21	NMI
Z	GND	22	-12 REG

WASATCH

SEMICONDUCTOR PRODUCTS

FOR PRODUCT INFORMATION OR TELEPHONE ORDERS CALL (714) 752-1374

Memory Bd

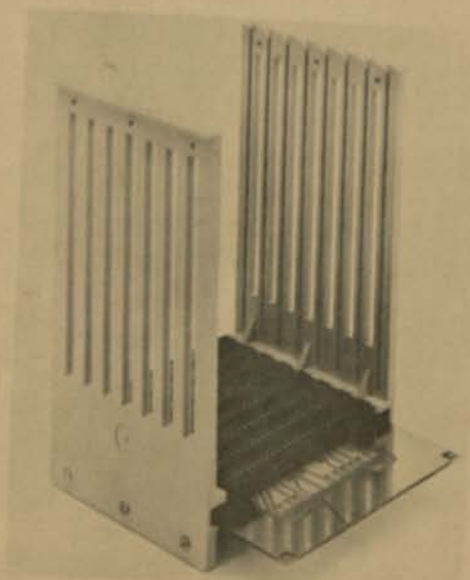
ABOUT OUR 44 PIN CCS BUS

44 PIN CCS BUS

REG +12	1	GND	GND	A	+10 UNREG
IRQ5	2	GND	GND	B	IRQ1
A12	3	VCC	VCC	C	IRQ6
A0	4	Ax	Ax	D	A11
A2	5	Ax	Ax	E	A9
A4	6	Ax	Ax	F	A7
D4	7	Dx	Dx	H	D2
D5	8	Dx	Dx	J	D0
IRQ2	9	-	-	K	IRQ3
A13	10	GND	GND	L	A15
XTX	11	-	OE	M	Ø1
A14	12	VCC	-	N	MASRST
R/W	13	R/W	BS	P	SYST EX.
Ø2	14	-	-	R	SYNC
D6	15	Dx	Dx	S	D3
D7	16	Dx	Dx	T	D1
A6	17	Ax	Ax	U	A5
A8	18	Ax	Ax	V	A3
A10	19	Ax	Ax	W	A1
R64	20	VCC	VCC	X	ROY
NMI	21	GND	GND	Y	-12 REG
IRQ4	22	GND	GND	Z	GND

The CCS BUS was developed for an OEM medical application with an over-riding concern for adequate power and ground connections. The CCS BUS provides 8 ground and 4 power connections to assure such adequacy. In addition, the CCS BUS carries 12 address lines, 8 data lines, board select, ram r/w, output enable (data direction), and 6 spares for system expansion.

WASATCH SEMICONDUCTOR PRODUCTS fully supports the 44 pin CCS BUS with an expanding family of quality products. Our products are readily interfaced to most popular microprocessors. Look for our ad in Kilobaud Magazine.



MOTHER BOARD SET

* 8 SLOTS ON 0.5" CENTERS
* 44 PIN CCS BUS
* 50 PIN I/O CONNECTOR
* 44 PIN CARD CONNECTORS

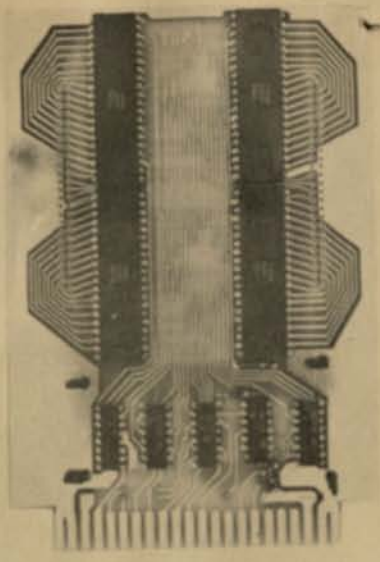
PRICE

• MOTHER BOARD ONLY	$20.00
• 44 PIN CARD CONNECTORS, EA.	$ 2.50
• CARD GUIDE SET	$10.00

80 LINE DIGITAL I/O BOARD

* 44 PIN CCS BUS
* FULLY BUFFERED, 5 VOLT ONLY
* 64 BIDIRECTIONAL DATA LINES
* 16 INTERRUPT LINES
* 2 50 PIN I/O CONNECTORS

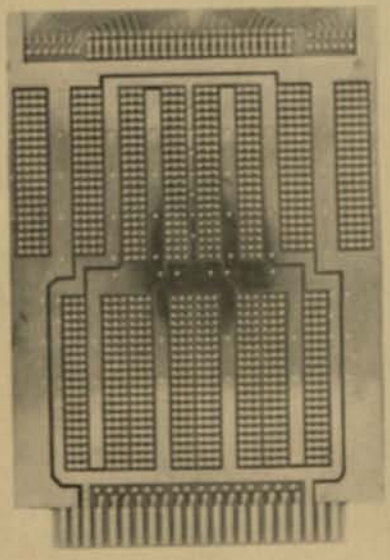
4 6820 PIA's



PRICE

- DIGITAL I/O BOARD ONLY $22.50
- KIT WITH ALL COMPONENTS $59.95

WIRE-WRAP BOARD



* 44 PIN CCS BUS
* ACCOMMODATES 14, 16, 20, 22, 24, 40 PIN IC's
* ACCOMMODATES VARIOUS HYBRID PACKAGES
* SUBSTANTIAL BUSSED GROUND & POWER PLANES
* ACCOMMODATES 50 PIN I/O CONNECTOR

PRICE

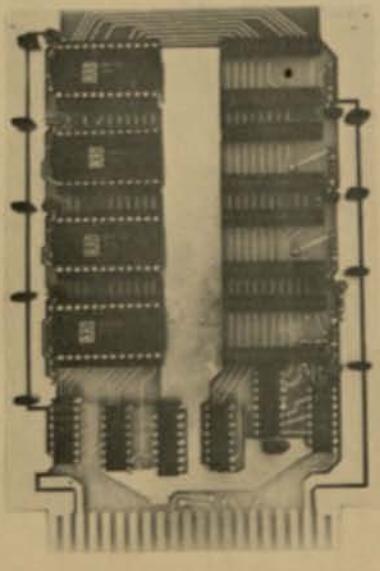
- WIRE-WRAP BOARD ONLY $15.00
- ACCESSORY KIT $ 5.00
  1 50 pin I/O connector
  17 bypass capacitors

4K PROM BOARD

* 44 PIN CCS BUS
* FULLY BUFFERED, 5 VOLT ONLY
* LOW POWER (CLOCKED VCC)
* POPULAR 512x8 BIPOLAR PROMS

PRICE

- PROM BOARD ONLY $ 22.50
- KIT WITH 2K PROM $ 79.95
- KIT WITH 4K PROM $129.95



price includes programming
to your binary tape

Video Board

+5 reg (yel) 580 ma
+5 reg (red) 480 ma.
-12 reg ≈ 18 ma.

UART Board

+5 reg 300 ma.
-12 reg.

Baud Gen.

+5 reg 145 ma.

TIM Bd.

Logic Analyzer Bd.

+5 reg 150 ma (all LED's on)

Memory Bd (2102L)

+5 reg 700 ma.

CPU Board

I/O Board

+5 reg ≈ 200 ma. w/ 4 6821's

Cassette Interface Bd.

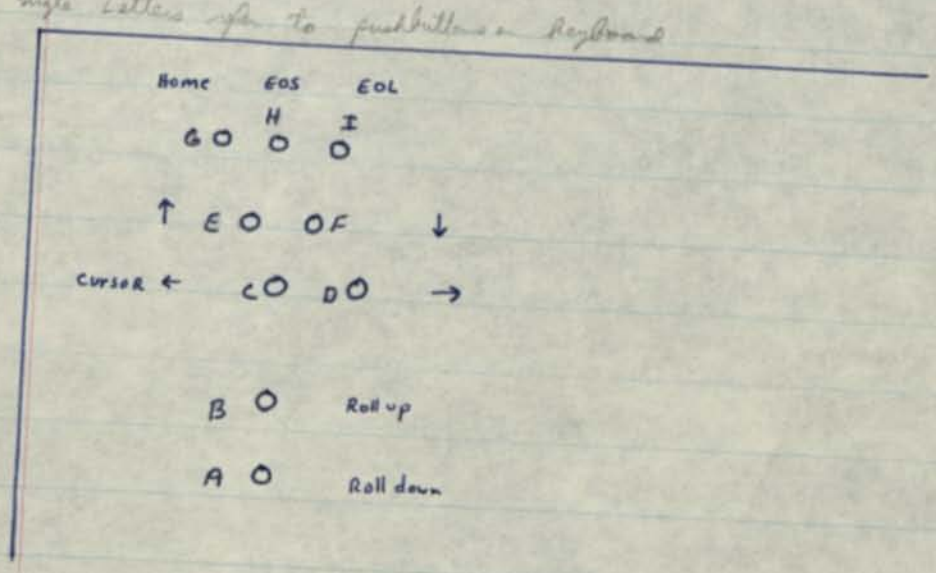
J1 Cable from Keyboard

(6-4 viewed)

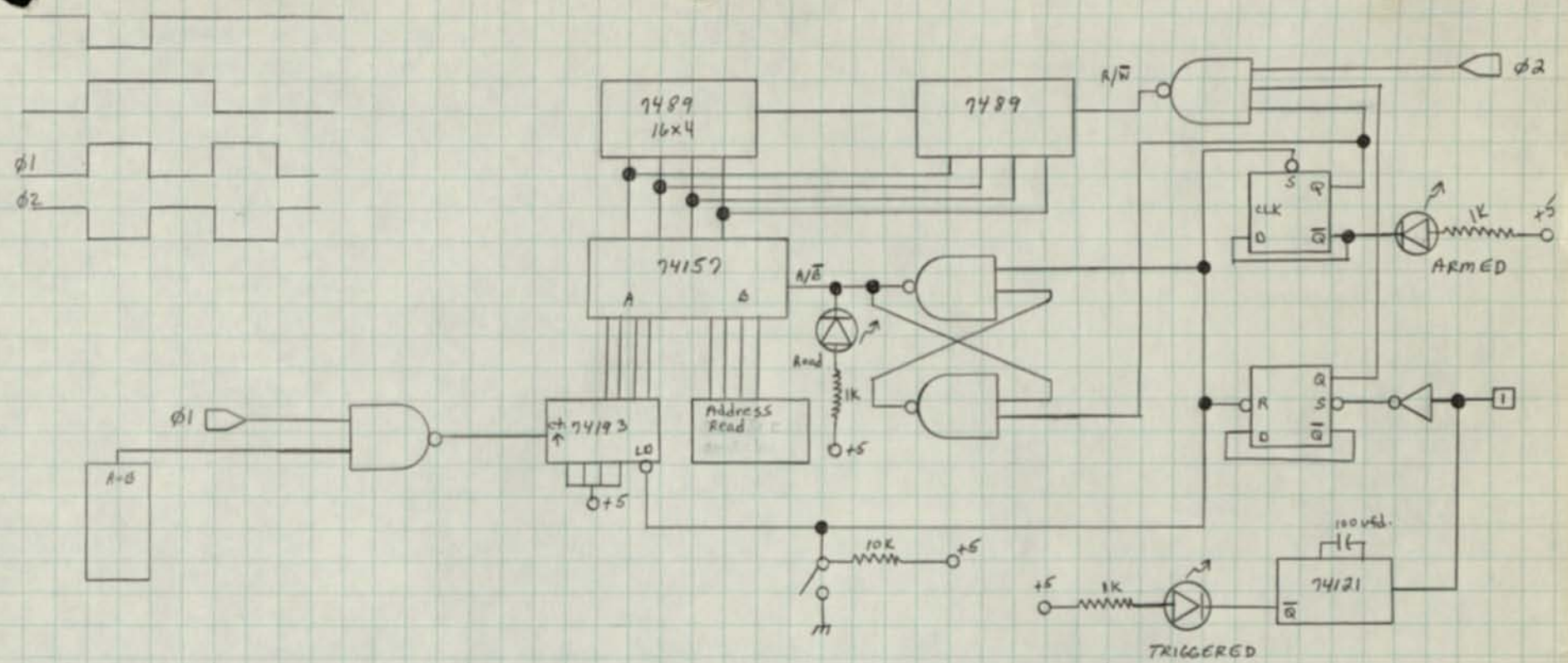
J1 #	50 cond. Cable	Function	To	J1 cable
1 & 26	Blk-Gray Gray-Blk	GND		
4	Green Blk *	(D) CURSOR DOWN	VIDEO-J4-9	E-red
5	Brown Blk	D5-B6	U7-31 (VIA PA5)	C-BLK
6	yellow Blue	D0-B1	U7-26 "	C-GRN
7	Orange Blk	D1-B2	U7-27 "	C-Yel
8	Orange Red	D2-B3	U7-28 "	C-Red
9	Red-Grey	D3-B4	U7-29 "	B-BLK
10	Brown-Red	D4-B5	U7-30 "	B-Grn
11	Red-Brown *	(A) ROW DOWN	VIDEO-J4-6	A-Red
12	Blue-Brown (Blk?)	D6-B7	U7-32 "	B-Yel
13	Green Brown *	(G) HOME	Video-J4-14	A-Yel
14	Purple-Brown	SW4		
15	Purple-Orange	$\overline{KP}$	U7-23	B-Red
16	Red Green	(SW2) CURSOR	Video J2-12	D-Green
17	Grey-White *	(B) EOS	Video-J4-13	A-Green
18	White Brown *	(C) CURSOR LEFT	Video-J4-7	D-Yel
19	Orange Purple *	(E) EOL	Video-J4-15	A-Blk
20	White grey			
21	Brown			
22	Brown White			
25	(See #50)			
26	(See #1)			
29	Blue-yellow	(SW3) CURSOR	Video J2-13	F-Green
30	Yel-Grey			

J1 #	50 cond. Cable	Function	To	J1 Cable
31	Black Brown *	ⓑ ROLL-UP	Video - J4 - 12	E - yel
32	Grey - Yellow	L2		
34	Black - Blue *	ⓑ CURSOR Right	Video - J4 - 11	E - Green
35	Orange - White *	ⓑ CURSOR UP	Video - J4 - 9	E - Blk
37	White - green			
25 & 50	Purple - Green Purple Grey	+12 UNREG		

Single Letters refer to push buttons on Keyboard



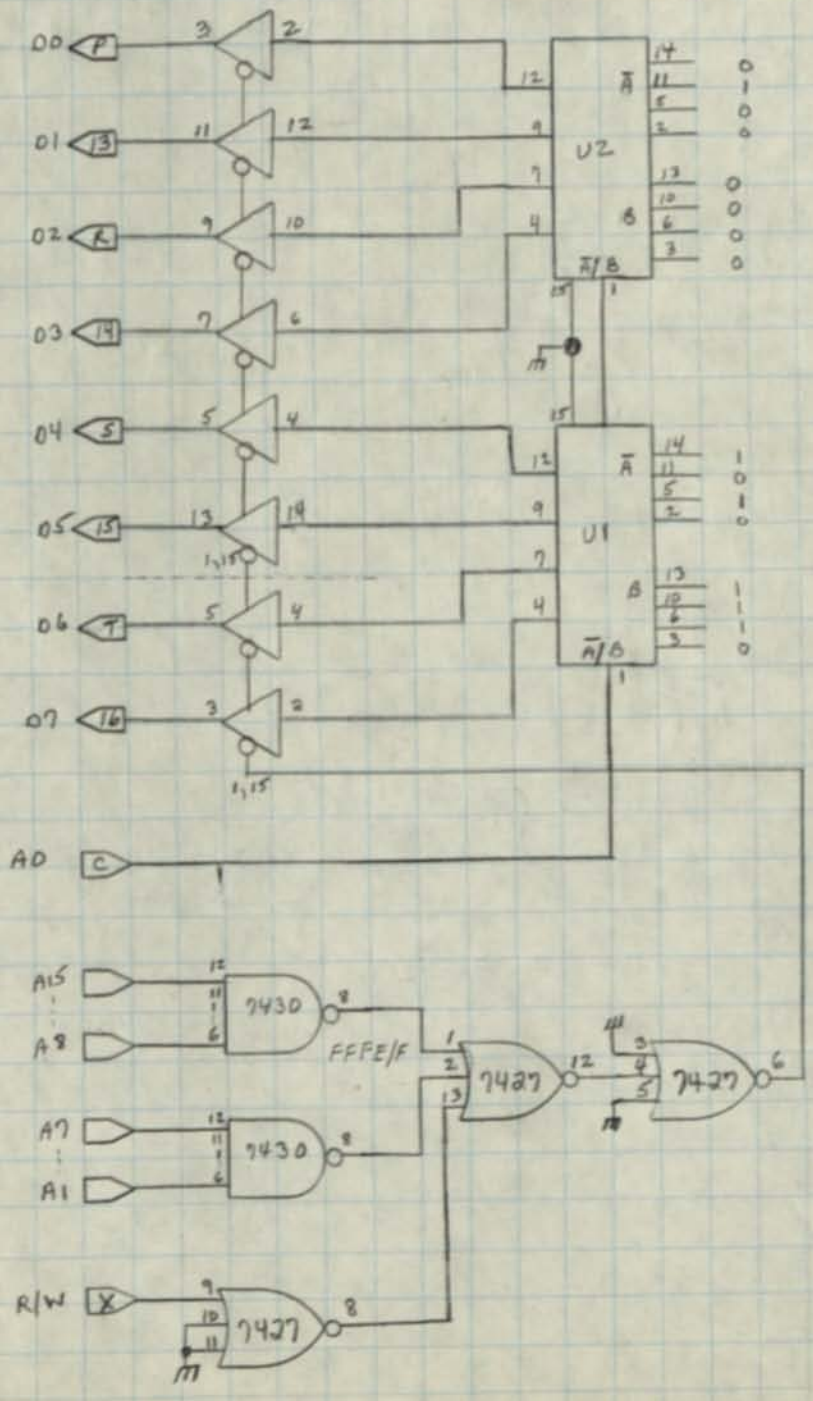
MISC. & TIM Listing


Φ1
Φ2
7489
16x4
7489
R/W
Φ2
74157
A
B
R/W
Read
1K
+5
Address
Read
Φ1
74193
LD
+5
A+B
10K
+5
CLK
S
R
Q
D
Q
1K
+5
ARMED
R
S
Q
D
Q
1
100 Vfd.
74121
Q
+5
1K
TRIGGERED

ARK Vector Generator

	Vcc	Gnd
8097	16	8
74157	16	8
7427	14	7
7430	14	7

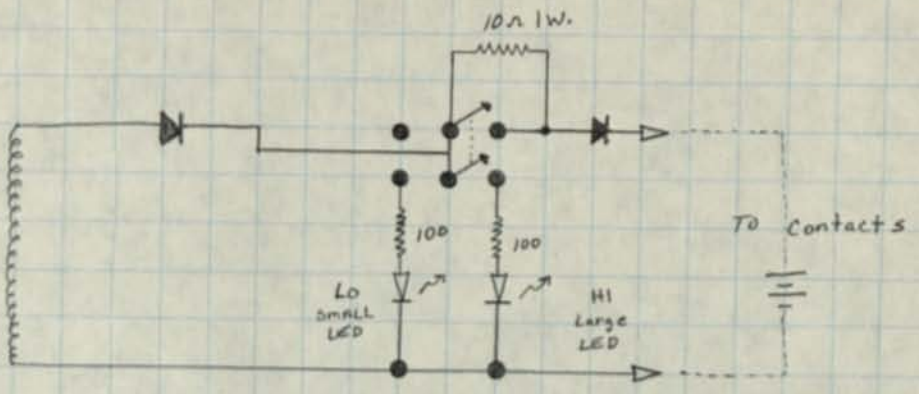
8097



A15 - 10
A14 - L
A13 - 9
A12 - K
A11 - 8
A10 - J
A9 - 7
A8 - H

A7 - 6
A6 - F
A5 - 5
A4 - E
A3 - 4
A2 - D
A1 - 3

Soldering Iron



MOS

MICROCOMPUTERS

TIM
TERMINAL INTERFACE MONITOR
MANUAL

Publication Number 6500-20

MCS6500

MICROCOMPUTER FAMILY

TIM MANUAL

MARCH, 1976

Second Edition

MOS TECHNOLOGY, INC.
950 Rittenhouse Road
Norristown, PA. 19401

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I. INTRODUCTION

TIM is the Terminal Interface Monitor program for MOS Technology's 65XX microprocessors. It is supplied in read-only memory (ROM) as part of the MCS6530-004 multi-function chip. Because the TIM code is nonvolatile, it is available at system power-on and cannot be destroyed inadvertently by user programs. Furthermore, the user is free to use only those TIM capabilities which he needs for a particular program. Both interrupt types, interrupt request (IRQ) and nonmaskable interrupt (NMI) may be set to transfer control to TIM or directly to the user's program.

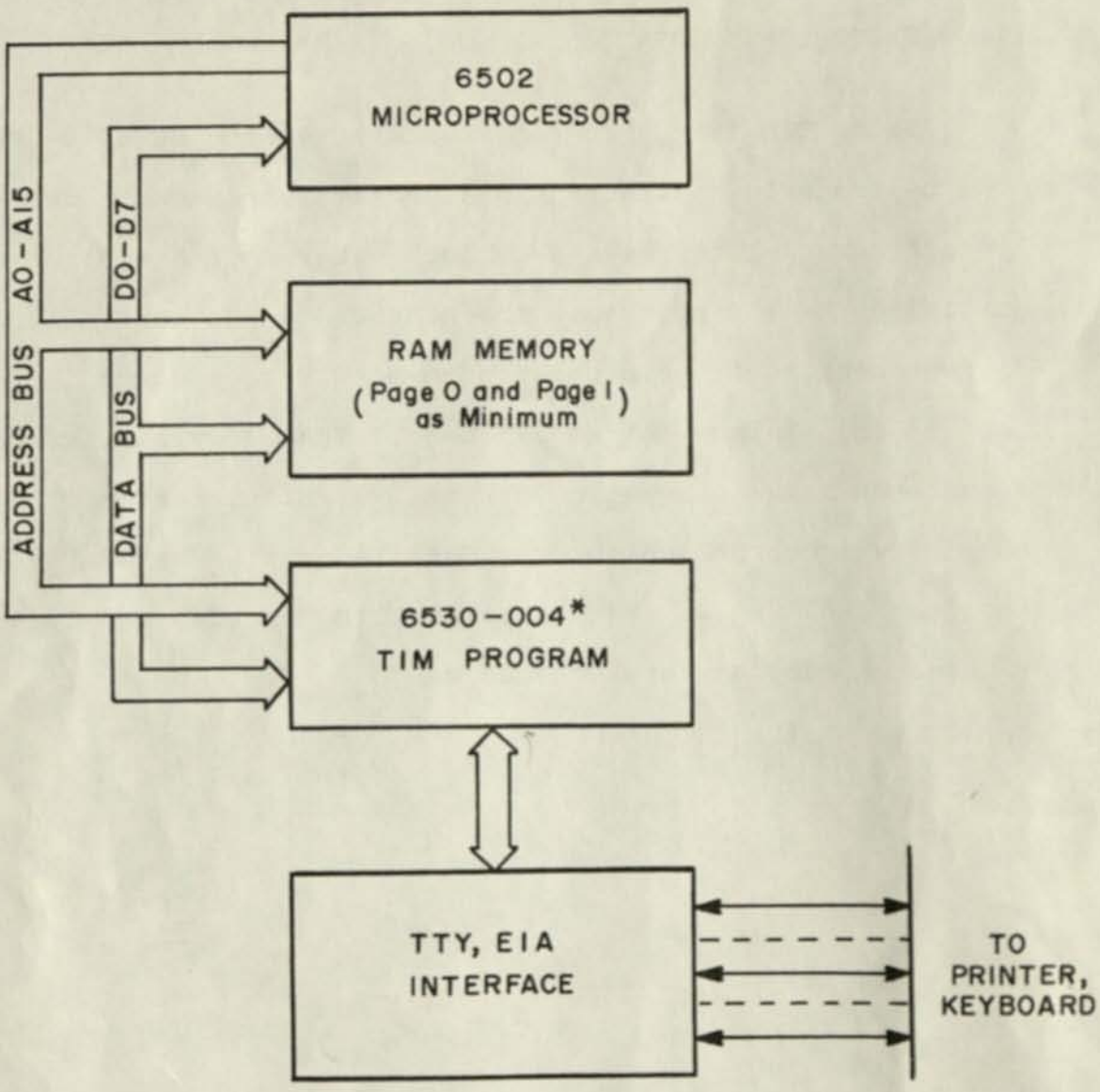
TIM communicates with the user via a serial full-duplex port (using ASCII codes) and automatically adjusts to the speed of the user's terminal. Any speed--even nonstandard ones--can be accommodated. If the user's terminal has a long carriage return time, TIM can be set to perform the proper delay. Commands typed at the terminal can direct TIM to start a program, display or alter registers and memory locations, set breakpoints, and load or punch programs. If available in the system configuration, a high-speed paper tape reader may be used to load programs through a parallel port on the MCS6530-004 chip. Programs may be punched in either of two formats--hexadecimal (assembler output) or BNPF (which is used for programming read-only memories). On loading or modifying memory, TIM performs automatic read-after-write verification to insure that addresses memory exists, is read/write type, and is responding correctly. Operator errors and certain hardware failures may thus be detected using TIM.

TIM also provides several subroutines which may be called by user programs. These include reading and writing characters on the terminal, typing a byte in hexadecimal, reading from high-speed paper tape, and typeing a carriage-return, line-feed sequence with proper delay for the carriage of the terminal being used. Program tapes loaded by TIM may also specify a start address so that programs may be started with a minimum of operator action.

II. SYSTEM CONFIGURATION

Since TIM is a "program" resident in the MCS6530-004 it must be properly configured in a proper system environment.

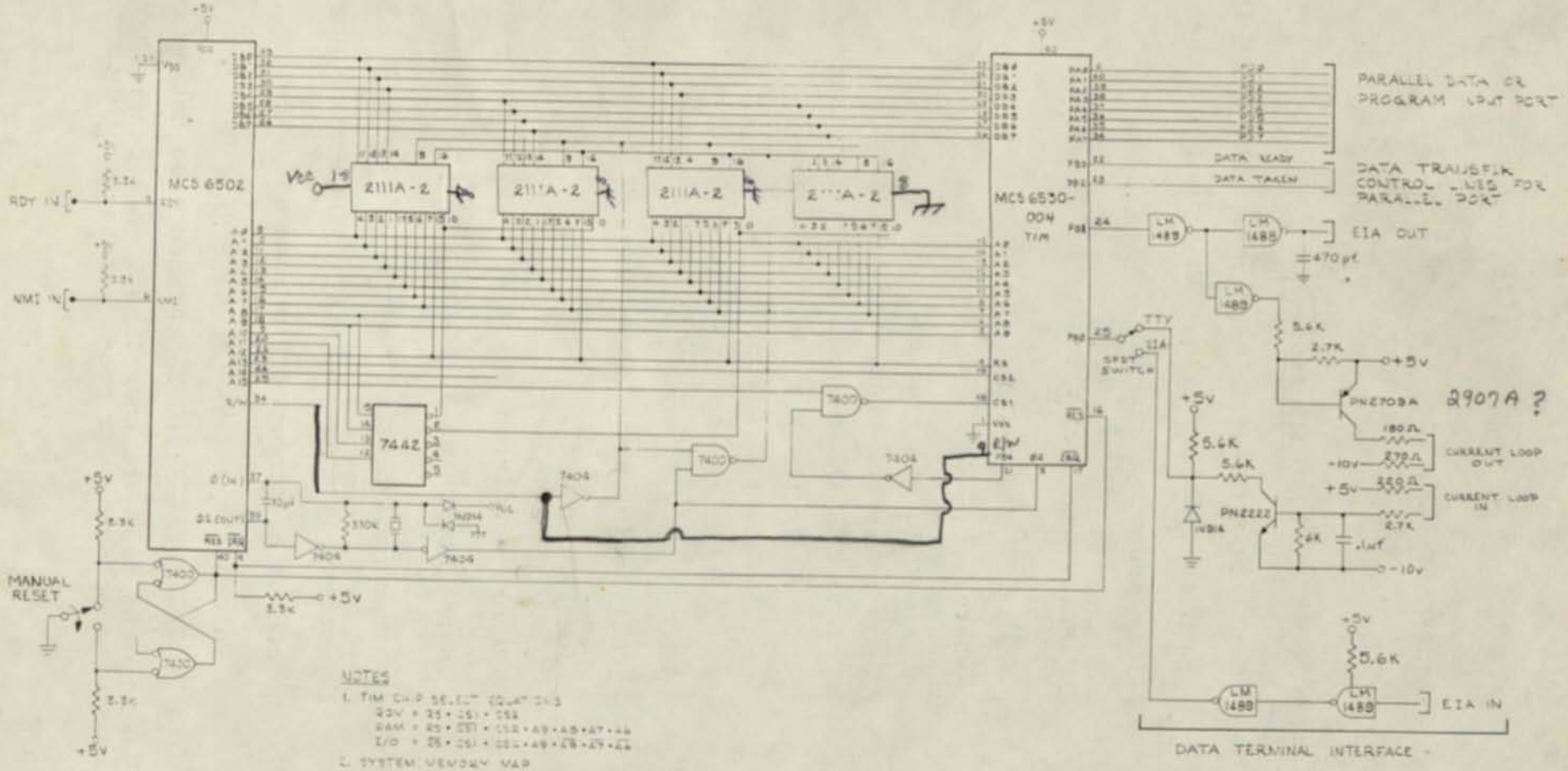
Figure 2-1 represents a block diagram of a minimum system utilizing the TIM program. The MCS6502 is the controlling microprocessor with two pages of memory (pages 0 and 1) representing the minimum RAM requirement. These devices, as well as a representative schematic for the TTY, EIA interfaces, are shown in Figure 2-2 which is a detailed system schematic utilizing the MCS6530-004. Note that the TIM function select equations are found on this schematic.



* Note that the TIM as sold consists only of the MCS6530-004 component accompanied by supporting information to build this system

TYPICAL MINIMUM CONFIGURATION
FOR "TIM" SYSTEM

FIGURE 2-1



NOTES

1. TIM CHIP SELECT EQUATIONS
   ROM = Φ2 • CS1 • CS2
   RAM = Φ2 • CS1 • CS2 • A9 • A8 • A7 • A6
   I/O = Φ2 • CS1 • CS2 • A9 • A8 • A7 • A6
2. SYSTEM MEMORY MAP
   0000 - 01FF = RAM
   ~~6500 - 65FF~~ = TIM I/O 6E00 - 6E0F = TIM I/O
   7000 - 73FF = TIM ROM
   ~~FF00~~ FFC0 - FFFF = TIM RAM
3. THE SYSTEM SHOWN CAN BE EXPANDED WITH ADDITIONAL I/O AND MEMORY USING THE ADDRESS BUS, DATA BUS, R/W LINE ETC.
4. INITIALIZATION OF PB4 AS SHOWN ALLOWS THE RESET VECTOR TO BE FETCHED FROM THE TIM ROM (7BFC AND 7BFD).

System Memory MAP

0000 - 01FF	RAM
6E00 - 6E0F	TIM I/O
7000 - 73FF	TIM Rom
FFC0 - FFFF	TIM RAM

"TIM" SYSTEM SCHEMATIC

FIGURE 2-2

III. OPERATIONAL FEATURES OF TIM

A. TIM Commands*

Command	Description
↴	Set line speed. After RESET, a carriage return is typed to allow TIM to measure the line speed.
.R	Display user registers. The format is: PC P A X Y S where: PC is the program counter P is the processor status A is the A (accumulator) register X is the X (index) register Y is the Y (index) register S is the stack pointer low byte (high byte is always 01)
.G	Go. Begin execution at user PC location (see R command).
.M addr	Memory examine. TIM will display the eight bytes beginning at address addr.
.: ADDR data	Alter registers or memory. TIM allows the user to alter registers (if R command precedes) or memory (if M command precedes). Values for registers or memory locations which are not to be changed need not be typed

* Characters typed by the user are underlined. All other characters are typed by the computer. ↴ means carriage-return.

—these fields may be skipped by typing spaces instead of data. The remainder of the fields in a line may be left unchanged by typing carriage return. The : command may be repeated to alter subsequent memory locations without the necessity of typing intervening M commands. Note that TIM automatically types spaces to separate data fields.

.LH Load Hexadecimal. TIM responds with carriage return, line-feed and loads data in assembler output format from the terminal or high-speed paper tape reader. The format is:

Zero or more leading characters except ";" (usually blank leader)

Any number of records of the form:

;ccaaaadddd....ddssss

where:

cc is the number of bytes in the record in hex

aaaa is the hex address to store the first byte of data

dddd....dd is the data (two hex digits per byte)

ssss is the check-sum, which is the arithmetic sum, to 16 bits, of all the count, address and data bytes represented by the record

A terminating record of zero length, either: ;00 or ;↓

Note that read-after-write and check-sum tests are performed. An error will result in a "?" being typed at the point the error occurred. Data from records with bad check-sums is deposited in memory as received, prior to the error stop.

.H — High-speed/low-speed reader switch. This command switches the load device from the user's terminal to the high-speed reader or vice versa.

.WH addl addh↵ — Write Hexadecimal. An assembler-format tape is generated at the user's terminal. Format is as described above in the LH command description. Note that the address range must be specified with the lower address first. As in the Alter command, TIM types the space between the address fields.

.WB addl addh↵ — Write BNPF. A BNPF format tape is generated at the user's terminal. Format is one or more records as follows:

aaaa BddddddddF BddddddddF BddddddddF BddddddddF

where:

aaaa is the address of the first of the four bytes specified in the record. (Note: BNPF conventions require that the letter "B" never occur in the address field. Blanks are substituted by TIM.)

B is the letter "B", meaning begin data.

dddddddd is eight data bits—P for logical true, N for logical false.

F is the letter "F", meaning finish.

Note that the BNPF format is output as multiples of four bytes. Thus, a multiple of four bytes will always be punched even if a non-multiple of four bytes is specified.

Cancel Command. While typing any command, its further effect may normally be terminated by typing one or two carriage returns, as required. During alter (:), carriage return means that no further bytes (or registers) are to be altered.

B. TIM Interrupt and Breakpoint Action

BRK

The BRK instruction causes the CPU to interrupt execution, save PC and P registers on the stack. and branch through a vector at locations FFFE and FFFF. TIM initializes this vector to point to itself on RESET. Unless the user modifies this vector, TIM will gain control when a BRK instruction is executed, print an asterisk "*" and the registers (as in R command), and wait for user commands. Note that after a BRK which vectors to TIM, the user's PC points to the byte following the BRK; however, users who choose to handle BRK instructions themselves

should note that BRK acts as a two-byte instruction, leaving the PC (on return via RTI) two bytes past the BRK instruction.

IRQ

Interrupt Request is also vectored through location FFFE. The CPU traps (as with BRK) through this vector when IRQ goes low, provided interrupts are not inhibited. Since this vector is the same as for BRK, TIM examines the BRK bit in the P register after this type of interrupt. If a BRK did not cause the interrupt, then TIM will pass control through the UINT vector. Users should normally put the address of their interrupt service routine in the UINT vector location. If an IRQ occurs and UINT has not been set by the user, TIM reports the unexpected interrupt in the same way as an NMI (see below).

NMI

Non-Maskable Interrupts vector through location FFFA. TIM initializes this vector at RESET to point to itself. If an NMI occurs, a pound-sign character (#) precedes the asterisk and CPU registers printout. This action is the same for IRQ's if the user has not set this vector to point to his own routine.

RESET or POWER-UP

On RESET or POWER-UP, TIM takes control, initializes itself and the system, sets defaults for interrupt vectors and waits for a carriage-return input from the user to determine terminal line speed. After carriage-return is typed, control is passed to the user as in BRK.

C. TIM Monitor Calls and Special Locations

Call	Address	Action	Arg.	Result	Notes
JSR WRT	72C6	Type a character	A	None	A,X cleared Y preserved
JSR RDT	72E9	Read a character	None	A	X cleared Y not preserved
JSR CRLF	728A	Type CR-LF and delay	None	None	A,X cleared Y preserved
JSR SPACE	7377	Type a space character	None	None	A,X,Y preserved
JSR WROB	72B1	Type a byte in hex	A	None	A,X cleared Y preserved
JSR RDHSR	733D	Read a character from high-speed paper tape reader	None	X—char read A—char trimmed to 7 bits	Y preserved

Function	Locations	Notes
Start Address	00F6,00F7	Set with hex tape on load
CR-LF Delay	00E3	Set on load or with user program (in bit times, minimum of 1. Zero means 256 bits-time delay).
UINT	FFF8	User IRQ vector
NMI Vector	FFFA	Hardware NMI vector
RESET Vector	FFFC	Hardware RESET vector
IRQ Vector	FFFE	Hardware IRQ vector

D. TIM Memory Usage

TIM uses the top 29_{10} bytes of page zero (locations 00E3 through 00FF). The user is advised to avoid these locations, except as noted above, if return to TIM or use of TIM subroutines is required before RESETing the processor. TIM also uses the hardware stack when it is in control. Provided the user does not alter the stack pointer during a break, and provided the stack does not overflow, TIM will restore the stack to its original status before returning to the user's program. The user is advised to use page 1 (the stack page) cautiously, leaving at least 20_{10} bytes for TIM use during a break or when using other TIM functions.

IV. TIM CHECKOUT PROCEDURE

The following step-by-step procedure assumes the user has built the TIM hardware system and is now ready to verify its functionality.

( ) 1. Turn power on, or if the power is on, perform a RESET operation. Type a carriage-return on the terminal. TIM should respond with:

```
* 7052 30 18 FF 01 FF
```

(Exact values may vary, although the first and last values should be as shown). If no response or a garbled response occurs, RESET and try again. In case of continued trouble, refer to the diagnostic section of the MOS Hardware Manual.

The "* 7052 30 18 FF 01 FF" printout is TIM's standard breakpoint message format. It consists of an asterisk "*" to identify the breakpoint printout, followed by the CPU register contents in this order: PC, P, A, X, Y, and S, i.e., Program Counter, Processor Status, Accumulator, X index, Y index and Stack Pointer. Note that all TIM inputs and outputs are in base 16 which is referred to as hexadecimal, or just hex. In hexadecimal, the "digits" are 0, 1, 2,..., A, B, C, D, E. F. After printing the CPU registers, TIM is ready to receive commands from you, the operator. TIM indicates this "ready" status by typing the prompting character "." on a new line.

( ) 2. TIM's response to RESET is to wait for a carriage-return and then print the user's registers. TIM uses this carriage-return character to measure the terminal line speed. If you have a settable-rate terminal, change the

rate (any speed between 10 and 30 cps will work) and repeat Step 1. TIM should respond at the new terminal speed.

( ) 3. The user's CPU registers may also be displayed with the R command. Type an R. The monitor should respond as above, but without the asterisk. Presence of the asterisk indicates that an interrupt or break instruction caused the printout.

```
.R  7052  30  18  FF  01  FF
```

( ) 4. Displayed values may be modified using the Alter (:) command. To modify register contents, type a colon (:) followed by the new values. For example:

```
.R  7052  30  18  FF  01  FF
.:  0100  00  00  00  00  FF
.R  0100  00  00  00  00  FF
```

Notice that TIM automatically types spaces to separate data fields. (Note: Characters typed by you, the user, are underlined in this document for clarity. Everything else is typed by the computer.) Examine your registers (R command) to verify the changes.

Memory may be examined and modified, as above, using the M and : commands. Try this:

```
.M  0100  00  66  23  EE  01  A2  41  6E
```

The memory command (M) causes TIM to type the contents of the first eight bytes of memory. (Memory data will be random on startup). Alter and verify these bytes using the Alter command, as above:

```
.M   0100  00  66  23  EE  01  A2  41  6E
.:   0100  00  01  02  03  04  05  06  07
```

If only part of a line is to be altered, items to be left unchanged can be skipped over by typing blanks, and carriage-return (↓). Try this:

```
.M   0100  00  01  02  03  04  05  06  07
.:   0100  FF  __  FF  FF  ↓
.M   0100  FF  01  FF  FF  04  05  06  07
```

( ) 5. Try to alter a location in TIM ROM:

```
.M   7000  85  F9  A9  23  D0  58  A9  16
.:   7000  00?
```

TIM verifies all changes to memory. Since locations 7000 through 7007 are in read-only memory, alteration is not possible. TIM signals write failure with a question mark. Similarly, the monitor will notify you of an attempt to alter a non-existant location:

```
.M   9000  90  90  90  90  90  90  90  90
.:   9000  00?
```

Note that attempts to read non-existant memory will normally yield the high-order byte of the address read.

( ) 6. There are three hardware facilities which may be used to stop a running (or run-away) program without the program itself calling TIM . These are the hardware inputs RESET,

IRQ, and NMI. To test this feature enter the following program at location 0000:

location	contents	instruction
0000	4C	LOOP JMP LOOP
0001	00	
0002	00	

(Use the M and : commands.)

Now, set the program counter (PC) to this location using the R and : commands. Finally, tell TIM to start executing your program using the Go (G) command:

```
.M 0000 FF 11 11 11 91 91 71 91
.: 0000 4C 00 00 ↓
.M 0000 4C 00 00 11 91 91 71 91
.R 0000 30 00 00 00 FF
.: 0000 ↓
.G
```

The computer should now be executing the program. It will continue to run until interrupted. Using the interrupt request line (IRQ), interrupt the processor. It should respond with:

```
*  0000 30 00 00 00 FF
```

Try the same experiment with non-maskable interrupt (NMI). The result should be the same except for a "#" character preceeding, which identifies the NMI printout. Finally, try it with RESET. RESET, however, forces a CPU branch to TIM, losing the old PC and other register contents. Thus NMI is the preferred means for manually interrupting program execution. IRQ may also be

used unless it is required for other functions such as peripheral interrupts.

( ) 7. Use M and : to enter the following test program called CHSET because it prints the character-set on the terminal. Note that Alter (:) commands may be repeated without intervening M commands to set sequential locations:

```
                        ;CHECKOUT PROGRAM -- PRINT THE CHARACTER SET ON USER TERMINAL
                        CRLF    =$728A          ;ADDRESS OF TIM CRLF ROUTINE
                        WRT     =$72C6          ;ADDRESS OF TIM WRITE ROUTINE
                        ;
CCCC                            *=0             ;VARIABLE STORAGE IN PAGE ZERO
0000                    CHAR    *=*+1           ;STORAGE FOR CHARACTER
                        ;
0001                            *=$01C0         ;PROGRAM STARTS ON PAGE ONE
                        ;
0100  20 8A 72          CHSET   JSR CRLF        ;DO CARRIAGE RETURN & LINE FEED
0103  A9 20                     LDA #$20        ;FIRST CHAR IS A SPACE
0105  85 00                     STA CHAR        ;INITIALIZE
                        ;
0107  A5 00             LOOP    LDA CHAR        ;GET CHARACTER
0109  C9 6C                     CMP #$6C        ;CHECK FOR LIMIT
010B  F0 08                     BEQ DONE        ;DONE IF 60
                        ;
010D  20 C6 72                  JSR WRT         ;PRINT CHAR
0110  E6 00                     INC CHAR        ;NEXT CHAR CODE
0112  4C 07 01                  JMP LOOP        ;CONTINUE
                        ;
0115  00                DONE    BRK             ;STOP & RETURN TO TIM MONITOR
                        ;
0116  4C 00 01                  JMP CHSET       ;DO IT AGAIN
```

```
.M  0100  20  8D  72  20  EC  72  8D  26
.:  0100  20  8A  72  A9  20  85  00  A5
.:  0108  00  C9  60  F0  08  20  C6  72
.:  0110  E6  00  4C  07  01  00  4C  00
.:  0118  01  ↓
```

Now run the program. Do this by setting the PC to 0100 and using the G command. The listing should look like this:

```
.R  0000 30 00 00 00 FF
.:  0100 ↓
.G
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←
 *  0116 33 60 00 00 FF
```

The program may be continued, causing it to execute again, by typing G:

```
.G
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←
 *  0116 33 60 00 00 FF
.G
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←
 *  0116 33 60 00 00 FF
.G
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←
 *  0116 33 60 00 00 FF
```

The CHSET program uses two TIM monitor functions: CRLF is the TIM function which causes a carriage-return and line-feed to be typed on the terminal. WRT is the routine which prints the character whose code is in the A register at the time of the call.

( ) 8. Save the CHSET program on paper tape (if your

terminal has a punch) as follows: First, punch some leader tape with the terminal in local mode. Then return to line mode and enter:

.WH 0100 0118 ↓

Turn the punch on after typing the second address, but before typing carriage-return. Then type carriage-return to punch the tape. When punching stops, turn the terminal back to local and type:

;00

and some blank trailer. This is a zero-length record which terminates your tape. See Appendix II for more information on tape formats.

( ) 9. Try re-loading your program using the LH command:

.LH

Now start the reader to load the program. The tape will be read and printed simultaneously. Stop the tape when the end is reached. (Before loading, you may wish to destroy the program in memory to verify that loading from tape actually works.)

( ) 10. Use the M and : commands to load the following program:

```
                        ;CHECKOUT PROGRAM -- PRINT BINARY OF TYPED CHARACTER
                        ;
                        ;
CCCC                    .       *=0             ;VARIABLE STORAGE IN PAGE ZERO
0000                    BINARY  *=*+1           ;STORAGE FOR CHAR DURING DISSECTION
0001                    COUNT   *=*+1           ;COUNT OF BITS REMAINING TO PRINT
                        ;
0002                            *=$0100         ;PROGRAM BEGINS ON PAGE ONE
                        ;
                        CRLF    =$728A           ;TIM  CRLF ROUTINE
                        WRT     =$72C6           ;TIM  WRITE ROUTINE
                        RDT     =$72E9           ;TIM  READ ROUTINE
                        SPACE   =$7377           ;TIM  SPACE ROUTINE
                        ;
0100  20 8A 72          PBIN    JSR CRLF        ;PRINT CARRIAGE RETURN & LINE FEED
 0103  20 E9 72                 JSR RDT         ;GET A CHARACTER
 0106  85 CC                    STA BINARY      ;SAVE FOR DISSECTION
 0108  20 77 73                 JSR SPACE       ;PRINT A SPACE
                        ;
0108  A9 08                     LDA #8          ;INITIALIZE BIT COUNT
010D  85 01                     STA COUNT
                        ;
010F  A9 30             PBLOOP  LDA #'0         ;ASSUME ZERO: LOAD ASCII "0"
0111  06 00                     ASL BINARY      ;C=NEXT BIT
0113  BC 02                     BCS PRINT       ;PRINT ZERO
                        ;.
0115  A9 31                     LDA #'1         ;LOAD ASCII "1"
                        ;
0117  20 C6 72          PRINT   JSR WRT         ;PRINT BINARY DIGIT
011A  C6 01                     DEC COUNT       ;COUNT BIT PRINTED
011C  10 F1                     BPL PBLOOP      ;DO NEXT BIT
                        ;
011E  4C 00 01                  JMP PBIN        ;DO IT ALL AGAIN
```

```
.M  0100  20  8D  72  A9  20  85  00  A5
.:  0100  20  8A  72  20  E9  72  85  00
.:  0108  20  77  73  A9  08  85  01  A9
.:  0110  30  06  00  B0  02  A9  31  20
.:  0118  C6  72  C6  01  10  F1  4C  00
.:  0120  01  ↓
```

The purpose of this program is to print the binary representation of an ASCII input character on the terminal. Run the program by starting it at location 0100. Try typing some characters:

```
.R  0116  33  60  00  00  FF
.:  0100  ↓
.G
U  101010101
B  101111011
1  110011101
```

There is obviously something wrong with the program. Bits which should be printed as 1's are 0's and vice versa. (Refer to your 6500 reference card for character codes.) Looking at the program, the problem is that the branch after PBLOOP goes the wrong way! It should be BCC, Branch if Carry Clear (or alternatively, the 1 and 0 loads could be interchanged). Thus, when a one-bit is shifted out of the character, a one should be printed.

Patch the program and try again (the code for BCC is 90).

```
.M   0113  B0  02  A9  31  20  C9  72  C6
.:   0113  90  ↓
.R   7052  31  FC  FF  01  FF
.:   0100  ↓
.G
U  010101010
B  010000100
1  001100010
```

There is, alas, still an error--one too many bits is being printed. The cause of this is a little less obvious. (Do you see it?) To investigate the problem, set a breakpoint at location 011E. Do this by replacing the instruction there with a BRK (code of 00). Then run the program:

```
.M   011E  4C  00  01  EF  4C  00  01  00
.:   011E  00  ↓
.R   7052  31  FC  FF  01  FF
.:   0100  ↓
.G
U  010101010
 *   011F  B0  00  00  AA  FF
```

Once the break has occurred, you are free to investigate the state of the program using TIM. In particular, check the value in location COUNT:

```
.M   0000  00  FF  1B  2E  31  EA  F0  FA
```

Aha! Although COUNT starts out with a value of 8, it is going one step too far (FF is minus 1). This is because the test instruction, BPL PBLOOP is testing to see whether the count is

greater than or equal to zero. Replace it with BNE (code D0), replace your breakpoint with the original contents at that location, and try the program again.

```
.M 011C 10 F1 00 00 01 EF 4C
.: 011C D0 __ 4C ↓
.R 011F B0 00 00 AA FF
.: 0100 ↓
.G
U 01010101
B 01000010
1 00110001
I 01001001
W 01010111
O 01001111
R 01010010
K 01001011
S 01010011
```

```
                        ;CHECKOUT PROGRAM -- PRINT BINARY OF TYPED CHARACTER
                        ;

                        ;
0000                    *=0                     ;VARIABLE STORAGE IN PAGE ZERO
0000                BINARY *=*+1                ;STORAGE FOR CHAR DURING DISSECTION
0001                CCUNT  *=*+1                ;COUNT OF BITS REMAINING TO PRINT
                        ;
0002                    *=$01C0                 ;PROGRAM BEGINS ON PAGE ONE
                        ;
                    CRLF   =$728A                ;TIM  CRLF ROUTINE
                    WRT    =$72C6                ;TIM  WRITE ROUTINE
                    RDT    =$72E9                ;TIM  READ ROUTINE
                    SPACE  =$7377                ;TIM  SPACE ROUTINE
                        ;
01C0  20 8A 72      PBIN   JSR CRLF             ;PRINT CARRIAGE RETURN & LINE FEE
01C3  20 E9 72             JSR RDT              ;GET A CHARACTER
01C6  85 00                STA BINARY           ;SAVE FOR DISSECTION
01C8  20 77 73             JSR SPACE            ;PRINT A SPACE
                        ;
01CB  A9 08                LDA #8               ;INITIALIZE BIT COUNT
01CD  85 01                STA CCUNT
                        ;
01CF  A9 30        PBLOOP  LDA #'0              ;ASSUME ZERO: LOAD ASCII "0"
0111  06 00                ASL BINARY           ;C=NEXT BIT
0113  90 02                BCC PRINT            ;PRINT ZERO
                        ;
0115  A9 31                LDA #'1              ;LOAD ASCII "1"
                        ;
0117  20 C6 72     PRINT   JSR WRT              ;PRINT BINARY DIGIT
011A  C6 01                DEC CCUNT            ;COUNT BIT PRINTED
011C  D0 F1                BNE PBLOOP           ;DO NEXT BIT
                        ;
011E  4C C0 01             JMP PBIN             ;DO IT ALL AGAIN
```

CORRECTED PBIN PROGRAM

( ) 11. Save the corrected program using the WH command. Before punching the terminating record (as above in step 8), turn off the punch and set the PC to the start address of the program (0100). Then punch locations 00F6 and 00F7 on the tape, then the terminator (;00), and finally, some trailer:

```
.R   7052  30  37  FF  01  FF
.:   0100  ↓
.WH  00F6  00F7  ↓
;0200F6000101A2
.;00
```

The resulting tape can be loaded and then started as follows:

```
.LH
  :  (program loads in)
.G
```

Locations 00F6 and 00F7 contain the starting address for programs. You may assemble and load your starting address into these locations to make tapes which can be started with a minimum of operator action. The carriage-return delay time may also be set in this manner. See Appendix II.

( ) 12. It is also possible to punch BNPF-format tapes using TIM. BNPF is the format used by some ROM programmers. The command is similar to that for writing hex tapes:

```
.WB  0100  0127  ↓
```

This command would punch the corrected PBIN program in BNPF

format. Try punching a BNPF tape. (Note that TIM will not load tapes in this format--use hex format (WH) for saving programs for later loading into your 65XX.)

( ) 13. If you have a high-speed paper tape reader attached to your 65XX system, you can use it to load programs in hex format. The H command switches the load device to and from the high speed reader. If you have a high speed reader, try loading a tape as follows:

.H
.LH

Note that control will not return to the user terminal until a terminator record (;00) is read.

APPENDIX A

MEMORY ADDRESS TEST

```
CARD # LOC    CODE        CARD
     1                   ;MEMORY ADDRESS TEST
     2                   ;FOR EACH LOC IN TEST RANGE
     3                         ;CLEAR WHOLE RANGE
     4                   ;     SET LOC TO $FF
     5                   ;     VERIFY WHOLE RAGE $00 EXCEPT (LOC)
     6                   ;     VERIFY (LOC) TO BE $FF
     7                   ;BREAK TO MONITOR ON ERROR WITH LOC IN (C,1)
     8                   ;PRINT "*" ON COMPLETION OF PASS & REPEAT
     9                   ;
    10  0000                   *=$0000           ;PAGE 0
    11                   ;
    12                   WRT    =$72C2
    13  0000             LOC    *=*+2             ;TEST CELL ADDR
    14  0002             LOW    *=*+2              ;LOWER LIMIT OF TEST
    15  0004             HIGH   *=*+2             ;UPPER LIMIT OF TEST+1
    16  0006             PTR    *=*+2             ;POINTER TO CELL UNDER TEST
    17                   ;
    18  0008                   *=$0C1C           ;START ADDR
    19                   ;
    20  0010  A9 0D       MAD    LDA #$0D          ;TYPE CR
    21  0012  20 C6 72           JSR WRT
    22  0015  A9 0A              LDA #$0A          ;& LF
    23  0017  20 C6 72           JSR WRT
    24                   ;
    25  001A  20 E8 00           JSR RSTLOC        ;LOC=LOW

    26  001D  20 71 00           JSR RSTPTR        ;PTR=LOW

    27  0020  A2 00              LDX #0
    28                   ;
    29                   ;CLEAR MEMORY AREA UNDER TEST
    30  0022  A9 00       ML1    LDA #0
    31  0024  81 06              STA (PTR,X)       ;STORE ZERO
    32  0026  20 7A 00           JSR INCPTR        ;INCREMENT & TEST

    33  0029  D0 F7              BNE ML1           ;NEXT LOC
    34                   ;
    35                   ;PUT $FF IN SELEXTED CELL
    36  002B  A9 FF       TEST   LDA #$FF
    37  002D  81 00              STA (LOC,X)
    38                   ;VERIFY ALL CELLS ZERO EXCEPT (LOC)
    39  002F  20 71 00           JSR RSTPTR        ;PTR=LOW

    40                   ;
    41  0032  A1 06       VLOOP  LDA (PTR,X)       ;GET CELL
    42  0034  F0 17              BEQ NEXTC         ;OK IF ZERO
    43  0036  A4 06              LDY PTR           ;NOT ZERO--IS THIS (LOC)?
    44  0038  C4 00              CPY LOC
    45  003A  F0 01              BEQ OK1
    46  003C  00                 BRK               ;NOT (LOC)
    47                   ;
    48  003D  A4 07       OK1    LDY PTR+1
```

```
CARD # LOC    CODE        CARD
  49  003F  C4 01          CPY LOC+1
  50  0041  F0 01          BEQ CK2
  51  0043  00             BRK                 ;ACT (LOC)
  52                    ;
  53  0044  C9 FF       CK2 CMP #$FF            ;IS (LOC)--IS DATA OK?
  54  0046  F0 01          BEQ OK3
  55  0048  00             BRK                 ;WRONG DATA
  56                    ;
  57  0049  A9 00       OK3 LDA #0              ;RESET (LOC)
  58  004B  81 00          STA (LOC,X)
  59                    ;
  60  004D  20 7A 00    NEXTC JSR INCPTR        ;NEXT CELL

  61  0050  D0 EC          BNE VLOOP           ;IF NOT AT LIMIT
  62                    ;
  63  0052  A5 00          LDA LOC             ;PRINT STAR EVERY PAGE ECUNDAI
  64  0054  D0 07          BNE NOSTAR
  65  0056  A9 2A          LDA #'*
  66  0058  20 C6 72       JSR WRT
  67  005B  A2 00          LDX #0              ;FIX X AFTER MON CALL
  68                    ;
  69  005D  20 8B 00    NOSTAR JSR INCLOC       ;NEXT LOC

  70  0060  D0 C9          BNE TEST
  71                    ;
  72  0062  20 68 00       JSR RSTLOC          ;PASS COMPLETE

  73  0065  4C 10 00       JMP MAD             ;NEXT PASS
  74                    ;
  75                    ;RESET LOC TO LOW
  76  0068  A5 02       RSTLOC LDA LOW
  77  006A  85 00          STA LOC
  78  006C  A5 03          LDA LOW+1
  79  006E  85 01          STA LOC+1
  80  0070  60             RTS
  81                    ;
  82                    ;RESET PTR TO LOW
  83  0071  A5 02       RSTPTR LDA LOW
  84  0073  85 06          STA PTR
  85  0075  A5 03          LDA LOW+1
  86  0077  85 07          STA PTR+1
  87  0079  60             RTS
  88                    ;
  89                    ;INCREMENT PTR & CHECK FOR LIMIT
  90  007A  E6 06       INCPTR INC PTR          ;INCREMENT
  91  007C  D0 02          BNE INC1
  92                    ;
  93  007E  E6 07          INC PTR+1
  94                    ;
  95  0080  A5 04       INC1   LDA HIGH         ;CHECK
  96  0082  C5 06          CMP PTR
  97  0084  D0 04          BNE IPRET           ;NOT AT LIMIT
```

```
CARD # LOC     CODE        CARD
   94
   95  0086  A5 05          LDA HIGH+1
  100  0088  C5 07          CMP PTR+1          ;Z=1 IF AT LIMIT
  101
  102  008A  60        IPRET  RTS
  103
  104                  ;INCREMENT LOC & CHECK FOR LIMIT
  105  008B  E6 00     INCLOC INC LOC            ;INCR
  106  008D  D0 02          BNE INC2
  107
  108  008F  E6 01          INC LOC+1
  109
  110  0091  A5 04     INC2   LDA HIGH           ;CHECK
  111  0093  C5 00          CMP LOC
  112  0095  D0 04          BNE ILRET
  113  0097  A5 05          LDA HIGH+1
  114  0099  C5 01          CMP LOC+1          ;Z=1 IF AT LIMIT
  115
  116  009B  60        ILRET  RTS

END OF MOS/TECHNOLOGY 6501 ASSEMBLY VERSION 3
NUMBER OF ERRORS =   0,  NUMBER OF WARNINGS =   0
```

SYMBOL TABLE

SYMBOL	VALUE	LINE DEFINED	CROSS-REFERENCES
HIGH	0004	15	95 95 110 113
ILRET	009B	116	112
INCLOC	008B	105	69
INCPTR	0079	90	32 60
INC1	008C	95	91
INC2	0091	110	106
IPRET	008A	102	97
LOC	0000	13	37 44 49 58 63 77 79 105 108 111 114
LOW	0002	14	76 78 83 85
MAC	001C	20	73
ML1	0022	30	33
NEXTC	004C	60	42
NOSTAR	005C	69	64
OK1	003C	48	45
OK2	0044	53	50
OK3	0049	57	54
PTR	0006	16	31 41 43 48 84 88 90 93 96 100
RSTLOC	006E	76	25 72
RSTPTR	0071	83	26 39
TEST	002B	36	70
VLOOP	0032	41	61
WRT	72C2	12	21 23 66

APPENDIX B

TIM PROGRAM LISTINGS

```
    TIM VERSION 1.0 - MEM PAGE 0
CARD # LOC     CODE        CARD
     2                     ;
     3                     ;       MOS TECHNOLOGY 650X TERMINAL INTERFACE MONITOR (TIM)
     4                     ;              VERSION 1.0  AUGUST 31, 1975
     5                     ;              COPYRIGHT 1975 MOS TECHNOLOGY
     6                     ;              ALL RIGHTS RESERVED.  UNAUTHORIZED USE
     7                     ;              OF ALL OR PART STRICTLY PROHIBITED.
     8                     ; - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     9                     ;
    10                     ;  PROMPTING CHARACTER IS A PERIOD (.)
    11                     ;  ----------------------------------
    12                     ;
    13                     ;
    14                     ;  DISPLAY COMMANDS
    15                     ;  ----------------
    16                     ;
    17                     ;  .R           DISPLAY REGISTERS (PC,F,A,X,Y,SP)
    18                     ;  .M  ADDR     DISPLAY MEMORY ( 8 BYTES BEGINNING AT ADDR )
    19                     ;
    20                     ;
    21                     ;  ALTER COMMAND (:)
    22                     ;  -----------------
    23                     ;  .:  DATA       ALTERS PREVIOUSLY DISPLAYED ITEM OR NEXT ITEM
    24                     ;
    25                     ;
    26                     ;  PAPER TAPE I/O COMMANDS
    27                     ;  ----------------------
    28                     ;
    29                     ;  .LH                      LOAD HEX TAPE
    30                     ;  .WB ADDR1 ADDR2          WRITE BNPF TAPE (FROM LOW ADDR1 TO HIGH ADDR2
    31                     ;  .WH ADDR1 ADDR2          WRITE HEX TAPE (FROM LOW ADDR1 TO HIGH ADDR2
    32                     ;
    33                     ;  CONTROL COMMANDS
    34                     ;  ----------------
    35                     ;
    36                     ;  .G                       GO, CONTINUE EXECUTION FROM CURRENT PC ADDRESS
    37                     ;
    38                     ;  .H                       TOGGLES HIGH-SPEED-READER OPTION
    39                     ;                             (IF ITS ON, TURNS IT OFF; IF OFF, TURNS ON
    40                     ;
    41                     ;  BRK AND NMI ENTRY POINTS TO TIM
    42                     ;  ------------------------------
    43                     ;
    44                     ;      TIM IS NORMALLY ENTERED WHEN A 'BRK' INSTRUCTION IS
    45                     ;          ENCOUNTERED DURING PROGRAM EXECUTION.  AT THAT
    46                     ;          TIME CPU REGISTERS ARE OUTPUT:  # PC F A X Y SP
    47                     ;          AND CONTROL IS GIVEN TO THE KEYBOARD.
    48                     ;      USER MAY ENTER TIM BY PROGRAMMED BRK OR INDUCED NMI.  NMI
    49                     ;          ENTRIES CAUSE A '#' TO PRECEDE THE '#' IN THE CPU REGISTER
    50                     ;          PRINTOUT FORMAT
    51                     ;
    52                     ;  NON-BRK INTRQ (EXTERNAL DEVICE) INTERRUPT HANDLING
    53                     ;  --------------------------------------------------
```

```
CARD #  LOC     CODE        CARD
    54                      ;
    55                      ;       A NON-BRK INTRQ INTERRUPT CAUSES AN INDIRECT JUMP TO THE ADDRESS
    56                      ;           LOCATED AT 'UINT' (HEX FFF8).  THIS LOCATION CAN BE SET
    57                      ;           USING THE ALTER CMD, OR LOADED AUTOMATICALLY IN PAPER TAPE
    58                      ;           FORM WITH THE LH CMD IF THE USER ASSIGNS HIS INTRQ INTERRUPT
    59                      ;           VECTOR TO $FFF8 IN THE SOURCE ASSEMBLY PROGRAM.
    60                      ;       IF NOT RESET BY THE USER, UINT IS SET TO CAUSE EXTERNAL
    61                      ;           DEVICE INTERRUPTS TO ENTER TIM AS NMI'S.  I.E.,
    62                      ;           IF A NMI OCCURS WITHOUT AN INDUCED NMI SIGNAL, IT IS
    63                      ;           AN EXTERNAL DEVICE INTERRUPT.
    64                      ;
    65                      ;   SETTING AND RESETTING PROGRAM BREAKPOINTS
    66                      ;   ----------------------------------------
    67                      ;
    68                      ;       BREAKPOINTS ARE SET AND RESET USING THE MEMORY DISPLAY
    69                      ;           AND ALTER COMMANDS.  BRK HAS A '00' OPERATION CODE.
    70                      ;       TO SET A BREAKPOINT SIMPLY DISPLAY THE MEMORY LOCATION
    71                      ;           (FIRST INSTRUCTION BYTE) AT WHICH THE BREAKPOINT IS
    72                      ;           TO BE PLACED THEN ALTER THE LOCATION TO '00'.  THERE IS
    73                      ;           NO LIMIT TO THE NUMBER OF BREAKPOINTS THAT CAN BE
    74                      ;           ACTIVE AT ONE TIME.
    75                      ;       TO RESET A BREAKPOINT, RESTORE THE ALTERED MEMORY LOCATION
    76                      ;           TO ITS ORIGINAL VALUE.
    77                      ;       WHEN AND IF A BREAKPOINT IS ENCOUNTERED DURING EXECTUION,
    78                      ;           THE BREAKPOINT DATA PRECEDED BY AN '*' IS DISPLAYED.
    79                      ;           THE PROGRAM COUNTER VALUE DISPLAYED IS THE BRK
    80                      ;           INSTRUCTION LOCATION + 1.
    81                      ;
    82                      ;   ---------------------------------------------------------------
    83                      ;                                   P07 6 5 4
    84                      MDBK    =%CCC1011C          ; X,X,X,POR,DATA-AVAIL,GOT-DATA,SERIAL-OUT,IN
    85                      DAVAIL  =$08
    86                      GOTDAT  =$C4
    87                      IOBASE  =$6F00
    88                      MPA     =IOBASE+0
    89                      MDA     =IOBASE+1
    90                      MPB     =IOBASE+2
    91                      MDB     =IOBASE+3
    92                      MCLKIT  =IOBASE+4
    93                      MCLKRD  =IOBASE+4
    94                      MCLKIF  =IOBASE+5
    95                      UINT    =$FFF8
    96                      NCMDS   =7
    97                      MPC     =$7000
    98                      MP1     =$7100
    99                      MP2     =$7200
   100                      MP3     =$7300
   101                      ;
   102                      ;  ZERO PAGE MONITOR RESERVE AREA
   103                      ;
   104                      CRDLY   =227                ;DELAY FOR CR IN BIT-TIMES
   105                      WRAP    =228                ;ADDRESS WRAP-AROUND FLAG
```

```
CARD # LOC  CODE      CARD
   106                DIFF    =229
   107                HSPTR   =231
   108                HSPCP   =232
   109                PREVC   =233
   110                MAJORT  =234
   111                MINORT  =235
   112                ACMD    =236
   113                TMPC    =238
   114                TMP2    =240
   115                TMP4    =242
   116                TMP6    =244
   117                PCL     =246
   118                PCH     =247
   119                FLGS    =248
   120                ACC     =249
   121                XR      =250
   122                YR      =251
   123                SP      =252
   124                SAVX    =253
   125                TMPC    =254
   126                TMPC2   =255
   127                RCNT    =TMPC
   128                LCNT    =TMPC2
   129                ;
   130                ;  64 BYTE RAM MONITER RESERVE AREA
   131                ;
   132                RAM64   =$FFCC
   133  0000                  *=RAM64
```

FFFF 70
FFFE 52
FFFD 70
FFFC 06
FFFB 70
FFFA 00
FFF9 70
FFF8 00

MPO TIM PAGE 0

```
CARD #  LOC   CODE        CARD
  135                     ;
  136                     ;
  137                     ;  TIM PAGE 0 (RELATIVE)
  138   FFC0              *=MPO
  139                     ;
  140   7000  85 F9       NMINT  STA ACC            ; SAVE A (0 page)
  141   7002  A9 23              LDA #'#            ; SET A=# TO INDICATE NMINT ENTRY
  142   7004  DC 55              BNE B3             ; JMP B3
  143                     ;
  144   7006  A9 16       RESET  LDA #MDBK  [16H]; INIT DIR REG, PCR TC 1 RELOCATES
  145                     ;                        00010110
  146   7008  8D 03 6E           STA MDB      0DRB     0 IN
  147                     ;                           1 OUT
  148   700B  A2 08              LDX #8             ; X=0
  149   700D  BD F7 73    R1     LDA INTVEC-1,X     ; INITIALIZE INT VECTORS
  150   7010  9D F7 FF           STA UINT-1,X
  151   7013  CA                 DEX
  152   7014  D0 F7              BNE R1
  153                     ;
  154   7016  86 EA (0page)      STX MAJORT         ; INIT MAJOR T COUNT TO ZERO
  155   7018  86 E7              STX HSPTR          ; CLEAR HSPTR FLAGS
  156   701A  86 E8              STX HSRCP
  157   701C  CA                 DEX                ; X=FF
  158   701D  9A                 TXS                ; SP=FF        SP is 8 bit Reg.
  159                     ;
  160                     ;                        ; COMPUTE BIT-TIME CONSTANT, X=FF
  161                     ;
  162   701E  AC 01              LDY #1             ; SET TO MEASURE 2 BITS
  163   7020  84 E3 (0page)      STY CRDLY          ;INIT CR DELAY TIME PARAMETER
  164   7022  AD 02 6E    R0     LDA MPB            ; WAIT FOR START   INVERTED DATA
  165   7025  4A                 LSR A
  166   7026  9C FA              BCC R0
  167                     ;
  168   7028  8E 04 6E    R2     STX MCLKIT         ; START CLOCK INITIALLY WITH FF
  169   702B  AD 05 6E    R3     LDA MCLKIF           Read INT FLAG (1st int)
  170   702E  10 04              BPL R4               FLAG IS SIGN BIT
  171   7030  E6 EA              INC MAJORT         ; COUNT MAJOR T
  172   7032  DC F4              BNE R2             ; GO RESTART CLOCK WITH X = FF
  173                     ;
  174   7034  98          R4     TYA
  175   7035  4D C2 6E           EOR MPB
  176   7038  29 01              AND #1                  REG.
  177   703A  FC FF              BEQ R3             ; WAIT FOR Y BIT 0 AND SERIAL-IN NOT EQU
  178   703C  88                 DEY
  179   703D  10 EC              BPL R3             ; LOOP UNTIL START OF BIT 2
  180                     ;
  181   703F  AD 04 6E           LDA MCLKRD           Read Timer INT FLAG
  182   7042  49 FF              EOR #$FF           ; COMPLEMENT RESIDUE
  183   7044  4A          R5     LSR A              ; HALF IT
  184   7045  46 EA              LSR MAJORT         ; HALF MAJOR
  185   7047  90 02              BCC R6
  186   7049  09 80              ORA #$80           ; PROPAGATE HC TO LC
```

```
MPO TIM PAGE 0

CARD #  LOC   CODE        CARD
  187   7048  C8          R6      INY
  188   704C  FC F6               BEQ R5
  189   704E  85 EB               STA MINGRT
  190                     ;
  191   7050  58                  CLI                 ; ENABLE INTS
  192   7051  00                  BRK                 ; ENTER TIM BY BRK
  193                     ;
  194   7052  85 F9       INTRQ   STA ACC             ; SAVE ACC
  195   7054  68                  PLA                 ; FLAGS TO A
  196   7055  48                  PHA                 ; RESTORE STACK STATUS
  197   7056  29 10               AND #$10            ; TEST BRK FLAG
  198   7058  F0 27               BEQ BX              ; USER INTERRUPT
  199                     ;
  200   705A  0A                  ASL A               ; SET A=SPACE (10 X 2 = 20)
  201   705B  85 FE       B3      STA TMPC            ; SAVE INT TYPE FLAG
  202   705D  D8                  CLD                 ; CLEAR DECIMAL MODE
  203   705E  4A                  LSR A               ; # IS 000, SPACE IS EVEN
  204                                                 ; SET CY FOR PC BRK CORRECTION
  205                     ;
  206   705F  86 FA               STX XR              ; SAVE X
  207   7061  84 FB               STY YR              ; Y
  208   7063  68                  PLA
  209   7064  85 F8               STA FLGS            ; FLAGS
  210   7066  68                  PLA
  211   7067  69 FF               ADC #$FF            ; CY SET TO PC-1 FOR BRK
  212   7069  85 F6               STA PCL
  213   706B  68                  PLA
  214   706C  69 FF               ADC #$FF
  215   706E  85 F7               STA PCH
  216   7070  BA                  TSX
  217   7071  86 FC               STX SP              ; SAVE ORIG SP
  218                     ;
  219   7073  20 BA 72    B5      JSR CRLF  →①
  220   7076  A6 FE               LDX TMPC
  221                     ;
  222   7078  A9 2A               LDA #'*
  223   707A  20 CC 72            JSR WRTWO
  224   707D  A9 52               LDA #'R             ; SET FOR R DISPLAY TO PERMIT
  225   707F  D0 16               BNE S0              ;   IMMEDIATE ALTER FOLLOWING BREAKPOINT.
  226                     ;
  227   7081  A5 F9       BX      LDA ACC
  228   7083  6C FB FF            JMP (UINT)          ; CONTROL TO USER INTRQ SERVICE ROUTINE
  229                     ;
  230   7086  A9 00       START   LDA #0              ;NEXT COMMAND FROM USER
  231   7088  85 E7               STA HSPTR           ;CLEAR H. S. PAPER TAPE FLAG
  232   708A  85 F4               STA WRAP            ;CLEAR ADDRESS WRAP-AROUND FLAG
  233   708C  20 BA 72            JSR CRLF
  234   708F  A9 2E               LDA #'.             ; TYPE PROMPTING '.'
  235   7091  20 C6 72            JSR WRCC
  236   7094  20 E9 72            JSR RDCC            ; READ CMD, CHAR RETURNED IN A
  237                     ;
  238   7097  A2 06       S0      LDX #NCMDS-1        ; LOOK-UP CMD
```

```
CARD # LOC    CODE        CARD
  239  7099  DD 06 71  S1      CMP CMDS,X
  240  709C  D0 19             BNE S2
  241                  ;
  242  709E  A5 FC             LDA SAVX          ; SAVE PREVIOUS CMD
  243  70A0  85 F9             STA PREVC
  244  70A2  86 FC             STX SAVX          ; SAVE CURRENT CMD INDEX
  245  70A4  A9 71             LDA #MP1/256      ; JMP INDIRECT TO CMD CODE
  246  70A6  85 ED             STA ACMD+1        ;   ALL CMD CODE BEGINS ON MP1
  247  70A8  BD 0D 71          LDA ADRS,X
  248  70AB  85 EC             STA ACMD
  249  70AD  E0 03             CPX #3            ; IF :, R CR M (0, 1, CR 2)  SPACE 2
  250  70AF  B0 03             BCS IJMP
  251  70B1  20 74 73          JSR SPAC2
  252                  ;
  253  70B4  6C EC 00  IJMP    JMP (ACMD)
  254                  ;
  255  70B7  CA        S2      DEX
  256  70B8  10 DF             BPL S1            ; LOOP FOR ALL CMDS
  257                  ;
  258  70BA  A9 3F     ERROPR  LDA #'?           ; OPERATOR ERR, TYPE '?', RESTART
  259  70BC  20 C6 72          JSR WRCC
  260  70BF  90 C5             BCC START         ; JMP START (WRCC RETURNS CY=0)
  261                  ;
  262  70C1  38        DCMP    SEC               ; TMP2-TMP0 DOUBLE SUBTRACT
  263  70C2  A5 F0             LDA TMP2
  264  70C4  E5 EE             SBC TMP0
  265  70C6  85 E5             STA DIFF
  266  70C8  A5 F1             LDA TMP2+1
  267  70CA  E5 EF             SBC TMP0+1
  268  70CC  A8                TAY               ;RETURN HIGH ORDER PART IN Y
  269  70CD  C5 E5             CMP DIFF          ; OR LO FOR EQU TEST
  270  70CF  60                RTS
  271                  ;
  272  70D0  A5 EE     PUTP    LDA TMP0          ; MOVE TMP0 TO PCH,PCL
  273  70D2  85 F6             STA PCL
  274  70D4  A5 EF             LDA TMP0+1
  275  70D6  85 F7             STA PCH
  276  70D8  6C                RTS
  277                  ;
  278  70D9  A9 00     ZTMP    LDA #0            ; CLEAR REGS
  279  70DB  95 EE             STA TMP0,X
  280  70DD  95 EF             STA TMP0+1,X
  281  70DF  60                RTS
  282                  ;
  283                  ;  READ AND STORE BYTE.  NO STORE IF SPACE OR RCNT=0.
  284                  ;
  285  70E0  20 B3 73  BYTE    JSR RCOB          ; CHAR IN A, CY=0 IF SP
  286  70E3  90 10             BCC BY3           ; SPACE
  287                  ;
  288  70E5  A2 00             LDX #0            ; STORE BYTE
  289  70E7  81 EE             STA (TMP0,X)
  290                  ;
```

```
CARD # LOC   CODE        CARD
  291  7CE5  C1 FE           CMP (TMPO,X)       ; TEST FOR VALID WRITE (RAM)
  292  7CE8  F0 05           BEQ BY2
  293  7CEC  68              PLA                ; ERR, CLEAR JSR ADR IN STACK
  294  7CED  68              PLA
  295  7CEE  4C BA 7C        JMP ERROPR
  296                 ;
  297  7CF2  20 7C 72  BY2    JSR DADD           ; INCR CKSUM
  298  7CF5  20 97 73  BY3    JSR INCTMP         ; GO INCR TMPC ADR
  299  7CF8  C6 FE            DEC RCNT
  300  7CFA  60               RTS
  301                 ;
  302  7CFB  A5 F8    SETR    LDA #FLGS          ; SET TC ACCESS REGS
  303  7CFD  85 FE            STA TMPC
  304  7CFF  A9 00            LDA #0
  305  71C1  85 FF            STA TMPC+1
  306  7103  A9 05            LDA #5
  307  71C5  6C               RTS
  308                 ;
  309  71C6  3A      CMDS     .BYTE ':'
  310  71C7  52               .BYTE 'R'
  311  71C8  4D               .BYTE 'M'
  312  71C9  47               .BYTE 'G'
  313  71CA  48               .BYTE 'H'
  314  71CB  4C               .BYTE 'L'
  315  71CC  57               .BYTE 'W'          ; W MUST BE LAST CMD IN CHAIN
  316  71CD  3A      ADRS     .BYTE ALTER-MP1
  317  71CE  14               .BYTE DSPLYR-MP1
  318  71CF  1C               .BYTE DSPLYM-MP1
  319  71C0  5C               .BYTE GO-MP1
  320  7111  6F               .BYTE HSP-MP1
  321  7112  74               .BYTE LH-MP1
  322  7113  C2               .BYTE WO-MP1
```

TIM I/O
6EØØ-6EØF

MP1 TIM PAGE 1

```
CARD # LOC      CODE        CARD
  324                       ;
  325                       ;
  326                       ;  NOTE -- ALL CMD CODE MUST BEGIN ON MP1
  327                       ;
  328                       ;  DISPLAY REG CMD - A,F,X,Y, AND SP
  329                       ;
  330   7114  20 A6 72      DSPLYR JSR WRPC          ; WRITE PC
  331   7117  20 FB 70             JSR SETR
  332   711A  D0 07                BNE MC           ; USE DSPLYM
  333                       ;
  334   711C  20 A4 73      DSPLYM JSR RDDA          ; READ MEM ADR INTO TMPC
  335   711F  90 16                BCC ERRS1        ; ERR IF NO ADDR
  336   7121  A9 08                LDA #8
  337   7123  85 FE          MC    STA TMPC
  338   7125  A0 00                LDY #0
  339   7127  20 77 73       M1    JSR SPACE        ; TYPE 8 BYTES OF MEM
  340   712A  B1 FE                LDA (TMPC),Y     ; (TMPC) PRESERVED FOR POSS ALTER
  341   712C  20 B1 72             JSR WRDB
  342   712F  C8                   INY              ; INCR INDEX
  343   7130  C6 FE                DEC TMPC
  344   7132  D0 F3                BNE M1
  345   7134  4C E6 70      BEGS1 JMP START
  346                       ;
  347   7137  4C BA 70      ERRS1 JMP ERRCPR
  348                       ;
  349                       ;  ALTER LAST DISPLAYED ITEM (ADR IN TMPC)
  350                       ;
  351   713A  C6 E9         ALTER  DEC PREVC         ; R INDEX = 1
  352   713C  D0 0D                BNE A3
  353                       ;
  354   713E  20 A4 73             JSR RDDA         ; CY=0 IF SP
  355   7141  90 03                BCC A2           ; SPACE
  356   7143  20 DC 70             JSR PUTP         ; ALTER PC
  357   7146  20 FB 70       A2    JSR SETR         ; ALTER R'S
  358   7149  D0 C5                BNE A4           ; JMP A4 (SETR RETURNS ACC = 5)
  359   714B  20 9A 72       A3    JSR WRDA         ; ALTER M, TYPE ADR
  360   714E  A9 08                LDA #8           ; SET CNT=8
  361                       ;
  362   7150  85 FE          A4    STA RCNT
  363   7152  20 77 73       A5    JSR SPACE        ; PRESERVES Y
  364   7155  20 EC 70             JSR BYTE
  365   7158  D0 F8                BNE A5
  366   715A  FC D8          A9    BEQ BEGS1
  367                       ;
  368   715C  A6 FC          GO    LDX SP
  369   715E  9A                   TXS              ; GRAB ON NEW SP VALUE TO SP
  370   715F  A5 F7                LDA PCH
  371   7161  48                  PHA
  372   7162  A5 F6                LDA PCL
  373   7164  48                  PHA
  374   7165  A5 F8                LDA FLGS
  375   7167  48                  PHA
```

```
MP1 TIM PAGE 1

CARD # LOC    CODE        CARD
  376  716B  A5 F9          LDA ACC
  377  716A  A6 FA          LDX XR
  378  716C  A4 FB          LDY YR
  379  716F  4C             RTI
  380                ;
  381  716F  E6 E8    HSP   INC HSROP        ; TOGGLE BIT 0
  382  7171  4C 86 7C       JMP START
  383                ;
  384  7174  20 E9 72  LH    JSR RDCC         ; READ SECOND CMD CHAR
  385  7177  2C 8A 72        JSR CRLF
  386  717A  A6 E8           LDX HSROP        ; ENABLE PTR OPTION IF SET
  387  717C  86 E7           STX HSPTR
  388  717E  2C E9 72  LH1   JSR RDCC
  389  7181  C9 3B          CMP #';          ; FIND NEXT RCD MARK (;)
  390  7183  DO F5           BNE LH1
  391                ;
  392  7185  A2 04           LDX #4
  393  7187  2C D9 7C        JSR ZTMP         ; CLEAR CKSUM REGS TMP4
  394  718A  2C B3 73        JSR RDOB
  395  718D  DO 06           BNE LH2
  396                ;
  397  718F  A2 00           LDX #0           ; CLEAR HS RCR FLAG
  398  7191  86 E7           STX HSPTR
  399  7193  F0 9F           BEQ BEGS1        ; FINISHED
  400                ;
  401  7195  85 FE    LH2    STA RCNT         ; RCNT
  402  7197  2C 7C 72        JSR DADD         ; RCD LNGH TO CKSUM
  403  719A  2C B3 73        JSR RDOB         ; SA HO TO TMPC+1
  404  719D  85 EF           STA TMPC+1
  405  719F  2C 7C 72        JSR DADD         ; ADD TO CKSUM
  406  71A2  2C B3 73        JSR RDOB         ; SA LO TO TMPC
  407  71A5  85 EE           STA TMPC
  408  71A7  2C 7C 72        JSR DADD         ; ADD TO CKSUM
  409                ;
  410  71AA  2C EC 7C  LH3   JSR BYTE         ; BYTE SUB/R DECRS RCNT ON EXIT
  411  71AC  D0 F8           BNE LH3
  412  71AF  2C A4 73        JSR RDCA         ; CKSUM FROM HEX RCD TO TMPC
  413  71B2  A5 F2           LDA TMP4         ; TMP4 TO TMP2 FOR DCMP
  414  71B4  85 F0           STA TMP2
  415  71B6  A5 F3           LDA TMP4+1
  416  71B8  85 F1           STA TMP2+1
  417  71BA  2C C1 7C        JSR DCMP
  418  71BD  F0 BF           BEQ LH1
  419  71BF  4C BA 70  ERRP1 JMP ERROPR
  420                ;
  421  71C2  20 E9 72  WC    JSR RDOC         ; RD 2ND CMD CHAR
  422  71C5  85 FE           STA TMPC
  423  71C7  2C 77 73        JSR SPACE
  424  71CA  2C A4 73        JSR RDOA
  425  71CD  2C B7 73        JSR T2T2         ; SA TO TMP2
  426  71DC  2C 77 73        JSR SPACE        ; SPACE BEFORE NEXT ADDRESS
  427  71D3  20 A4 73        JSR RDOA
```

```
CARD #  LOC    CODE        CARD
  428   71D6  20 87 73          JSR T2T2          ; SA TO TMP0, EA TO TMP2
  429   71D9  20 E9 72          JSR RDOC          ; DELAY FOR FINAL CR
  430   71DC  A5 FE             LDA TMPC
  431                     ;
  432   71DE  C9 48             CMP #'H
  433   71E0  D0 59             BNE WB
  434                     ;
  435   71E2  A6 E4       WH0   LDX WRAP          ;IF ADDR HAS WRAPPED AROUND
  436   71E4  D0 52             BNE BCCST         ;THEN TERMINATE WRITE OPERATION
  437                     ;
  438   71E6  20 8A 72          JSR CRLF
  439   71E9  A2 18             LDX #24
  440   71EB  86 FE             STX RCNT          ; RCNT=24
  441   71ED  A2 04             LDX #4            ; CLEAR CKSUM
  442   71EF  20 D9 7C          JSR ZTMP
  443                     ;
  444   71F2  A9 3B             LDA #';
  445   71F4  20 C6 72          JSR WRDC          ; WR RCD MARK
  446                     ;
  447   71F7  20 C1 7C          JSR DCMP          ; EA-SA (TMP0+2-TMP0) DIFF IN LOC DIFF,+1
  448   71FA  98                TYA               ; MS BYTE OF DIFF
  449   71FB  D0 CA             BNE WH1
  450   71FD  A5 E5             LDA DIFF
  451   71FF  C9 17             CMP #23
  452   7201  B0 C4             BCS WH1           ; DIFF GT 24
  453   7203  85 FE             STA RCNT          ; INCR LAST RCNT
  454   7205  E6 FE             INC RCNT
  455   7207  A5 FE       WH1   LDA RCNT
  456   7209  20 7C 72          JSR DADD          ; ADD TO CKSUM
  457   720C  20 B1 72          JSR WRCB          ; RCD CNT IN A
  458   720F  A5 EF             LDA TMPC+1        ; SA HC
  459   7211  20 7C 72          JSR DADD
  460   7214  20 B1 72          JSR WRCB
  461   7217  A5 EE             LDA TMPC          ; SA LC
  462   7219  20 7C 72          JSR DADD
  463   721C  20 B1 72          JSR WRCB
  464                     ;
  465   721F  AC CC       WH2   LDY #0
  466   7221  B1 EE             LDA (TMP0),Y
  467                     ;
  468   7223  20 7C 72          JSR DADD          ; INC CKSUM, PRESERVES A
  469   7226  20 B1 72          JSR WRDB
  470   7229  20 57 73          JSR INCTMP        ; INC SA
  471   722C  C6 FE             DEC RCNT
  472   722E  D0 EF             BNE WH2           ; LOOP FOR UP TO 24 BYTES
  473                     ;
  474   7230  20 9E 72          JSR WRDA4         ; WRITE CKSUM
  475                     ;
  476   7233  20 C1 7C          JSR DCMP
  477   7236  B0 AA             BCS WH0           ; LOOP WHILE EA GT CR = SA
  478   7238  4C 86 7C   BCCST  JMP START
  479                     ;
```

```
MPL TIM PAGE 1

CARD #  LOC    CODE        CARD
  480                      ;
  481  7238  E6 FD         WB      INC SAVX          ; SAVX TO = NCMDS FOR ASCII SUB/R
  482  723C  A5 E4         WB1     LDA WRAP          ;IF ADDR HAS WRAPPED AROUND
  483  723F  D0 F7                 BNE BCCST         ;THEN TERMINATE WRITE OPERATION
  484                      ;
  485  7241  A9 04                 LDA #4
  486  7243  85 EC                 STA ACMD
  487  7245  20 8A 72              JSR CRLF
  488  7248  20 9A 72              JSR WRDA          ; OUTPUT HEX ADR
  489                      ;
  490  724B  20 77 73      WBNPF   JSR SPACE
  491  724E  A2 09                 LDX #9
  492  7250  86 FE                 STX TMPC          ; LOOP CNT =9
  493  7252  A1 E5                 LDA (TMPC-9,X)
  494  7254  85 FF                 STA TMPC2         ; BYTE TO TMPC2
  495  7256  A9 42                 LDA #'B
  496  7258  D0 08                 BNE WBF2          ; WRITE B
  497                      ;
  498  725A  A9 50         WBF1    LDA #'P
  499  725C  06 FF                 ASL TMPC2
  500  725E  BC C2                 BCS WBF2
  501  7260  A9 4E                 LDA #'N
  502                      ;
  503  7262  20 C6 72      WBF2    JSR WRCC          ; WRITE N OR P
  504  7265  C6 FE                 DEC TMPC
  505  7267  DC F1                 BNE WBF1          ; LOOP
  506  7269  A9 46                 LDA #'F
  507  726B  20 C6 72              JSR WRDC          ; WRITE F
  508                      ;
  509  726E  20 97 73              JSR INCTMF
  510                      ;
  511  7271  C6 EC                 DEC ACMD          ; TEST FOR MULTIPLE OF FOUR
  512  7273  DC D6                 BNE WBNPF
  513                      ;
  514  7275  20 C1 7C              JSR DCMP
  515  7278  BC C3                 BCS WB1           ; LOOP WHILE EA GT CR = SA
  516  727A  9C BC                 BCC BCCST
  517                      ;
  518  727C  4B            DADD    PHA               ; SAVE A
  519  727D  18                    CLC
  520  727E  65 F2                 ADC TMP4
  521  7280  85 F2                 STA TMP4
  522  7282  A5 F3                 LDA TMP4+1
  523  7284  69 00                 ADC #0
  524  7286  85 F3                 STA TMP4+1
  525  7288  68                    PLA               ; RESTORE A
  526  7289  60                    RTS
  527                      ;
  528  728A  A2 0D  ① → CRLF   LDX #$0D   CR
  529  728C  A9 0A               LDA #$0A   LF
  530  728E  20 C0 72            JSR WRTWO → ①
  531  7291  AE E3  (2 page)     LDX CRDLY         ;BIT-TIME COUNT FOR DELAY
```

```
CARD #  LOC   CODE        CARD
  532   7293  20 1D 73  CR1     JSR DLY2          ;DELAY OF ONE BIT-TIME
  533   7296  CA              DEX
  534   7297  D0 FA           BNE CR1
  535   7299  6C              RTS
  536                   ;
  537                   ;  WRITE ADR FROM TMPC STORES
  538                   ;
  539   729A  A2 01     WRDA    LDX #1
  540   729C  D0 0A             BNE WRDA1
  541   729E  A2 05     WRCA4   LDX #5
  542   72A0  D0 06             BNE WRDA1
  543   72A2  A2 07     WRCA6   LDX #7
  544   72A4  D0 02             BNE WRDA1
  545   72A6  A2 09     WRPC    LDX #9
  546   72A8  B5 ED     WRDA1   LDA TMPD-1,X
  547   72AA  48                PHA
  548   72AB  B5 EE             LDA TMPC,X
  549   72AD  20 B1 72          JSR WRDB
  550   72B0  68                PLA
  551                   ;
  552                   ;  WRITE BYTE - A = BYTE
  553                   ;  UNPACK BYTE DATA INTO TWO ASCII CHARS. A=BYTE; X,A=CHARS
  554                   ;
  555   72B1  48        WRDB    PHA
  556   72B2  4A                LSR A
  557   72B3  4A                LSR A
  558   72B4  4A                LSR A
  559   72B5  4A                LSR A
  560   72B6  20 58 73          JSR ASCII         ; CONVERT TO ASCII
  561   72B9  AA                TAX
  562   72BA  68                PLA
  563   72BB  29 0F             AND #$0F
  564   72BD  20 58 73          JSR ASCII
  565                   ;
  566                   ;  WRITE 2 CHARS - X,A = CHARS
  567                   ;
  568   72C0  48    (2) → WRTWO   PHA
  569   72C1  8A                TXA
  570   72C2  20 C6 72          JSR WRT → (3)
  571   72C5  68                PLA
  572                   ;
  573                   ;  WRITE SERIAL OUTPUT
  574                   ;  A = CHAR TO BE OUTPUT
  575                   ;
  576   72C6  20 1D 73 (3)→WRT    JSR DLY2 → (4)
  577   72C9  A2 09             LDX #9
  578                   WRDC    =WRT
  579   72CB  49 FF             EOR #$FF          ; COMPLEMENT A
  580   72CD  38                SEC
  581                   ;
  582   72CE  20 DA 72  WRT1    JSR CLT
  583   72D1  20 1D 73          JSR DLY2
```

```
CARD #  LOC   CODE        CARD
  584   72D4  4A              LSR A
  585   72D5  CA              DEX
  586   72D6  DC F6           BNE WRT1
  587   72D8  FC 3F           BEQ RDT5
                                        ; *USE BNE?
  588
  589                   ;
  590   72DA  48        OUT   PHA       ; SAVE A
  591   72DB  AD 02 6E        LDA MPB   ; OUTPUT BIT FROM CY
  592   72DE  29 FD           AND #%11111101
  593   72EC  90 02           BCC OUT1
  594   72E2  09 02           ORA #%00000010
  595   72E4  8D C2 6E  OUT1  STA MPB
  596   72E7  68              PLA       ; RESTORE A
  597   72E8  60              RTS
  598                   ;
  599                   ;  OUTPUT  RETURNS CHAR IN A
  600                   ;
  601   72E9  A5 E7     RDT   LDA HSPTR ; TEST HS PTR OPTION
  602   72EB  4A              LSR A
  603   72EC  BC 4F           BCS RDHSR
                        RDOC  =RDT
  604                         LDX #8                INVERTED DATA IN
  605   72EE  A2 08
  606                   ;
  607   72FC  AC C2 6E  RDT1  LDA MPB   ; WAIT FOR START BIT
  608   72F3  4A              LSR A
  609   72F4  9C FA           BCC RDT1
  610                   ;
  611   72F6  2C 2C 73        JSR DLY1
  612   72F9  2C DA 72        JSR CLT   ; ECHO START BIT
  613                   ;
  614   72FC  2C 1D 73  RDT2  JSR DLY2
  615   72FF  AC C2 6E        LDA MPB   ; CY = NEXT BIT
  616   73C2  4A              LSR A
  617   73C3  2C DA 72        JSR CLT   ; ECHO
  618                   ;
  619   73C6  08              PHP       ; SAVE BIT
  620   73C7  98              TYA       ; Y CONTAINS CHAR BEING FORMED
  621   73C8  4A              LSR A
  622   73C9  28              PLP       ; RECALL BIT
  623   73CA  9C C2           BCC RDT4
  624   73CC  09 80           ORA #$80  ; ADD IN NEXT BIT
  625   73CE  A8        RDT4  TAY
  626   73CF  CA              DEX
  627   731C  DC EA           BNE RDT2  ; LOOP FOR 8 BITS
  628   7312  49 FF           EOR #$FF  ; COMPLEMENT DATA
  629   7314  29 7F           AND #$7F  ; CLEAR PARITY
  630                   ;
  631   7316  20 1D 73        JSR DLY2
  632   7319  18        RDT5  CLC
  633   731A  20 DA 72        JSR CLT   ;AND DELAY 2 HALF-BIT-TIMES
  634                   ;
  635   731D  20 20 73  DLY2  JSR DLY1
```

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MPI TIM PAGE 1

CARD # LOC    CODE      CARD
  636  7320  48       → DLY1   PHA              ; SAVE FLAGS AND A
  637  7321  08                PHP
  638  7322  8A                TXA              ; SAVE X
  639  7323  48                PHA
  640  7324  AE EA             LDX MAJCRT
  641  7326  A5 EB             LDA MINORT
  642                     ;
  643  7328  8D C4 6E    DL2    STA MCLK1T
  644                     ;
  645  732B  AD C5 6E    DL3    LDA MCLK1F
  646  732E  10 FB             BPL DL3
  647  7330  CA                DEX
  648  7331  08                PHP
  649  7332  AD C4 6E          LDA MCLKRD       ; RESET TIMER INT FLAG
  650  7335  28                PLP
  651  7336  10 F3             BPL DL3
  652                     ;
  653  7338  68                PLA              ; RESTORE REGS
  654  7339  AA                TAX
  655  733A  28                PLP
  656  733B  68                PLA
  657  733C  60          DLX    RTS →@
  658                     ;
  659  733D  AD C2 6E    RDHSR  LDA MPB          ; LOOP ON DATA AVAIL
  660  7340  29 08             AND #DAVAIL
  661  7342  F0 F9             BEQ RDHSR
  662                     ;
  663  7344  AE 00 6E          LDX MPA          ; READ DATA
  664  7347  AD C2 6E          LDA MPB          ; SEND DCT-DATA PULSE
  665  734A  09 04             ORA #GOTDAT
  666  734C  8D C2 6E          STA MPB
  667  734F  29 FB             AND #%11111011
  668  7351  8D C2 6E          STA MPB
  669  7354  8A                TXA
  670  7355  29 7F             AND #$7F
  671  7357  60                RTS
  672                     ;
  673  7358  18          ASCII  CLC
  674  7359  69 06             ADC #6
  675  735B  69 F0             ADC #$F0
  676  735D  90 02             BCC ASC1
  677  735F  69 06             ADC #$06
  678                     ;
  679  7361  69 3A       ASC1   ADC #$3A
  680  7363  48                PHA              ; TEST FOR LETTER B IN ADR DURING WBNPF
  681  7364  C9 42             CMP #'B
  682  7366  D0 0A             BNE ASCX
  683  7368  A5 FD             LDA SAVX
  684  736A  C9 07             CMP #NCMDS
  685  736C  D0 04             BNE ASCX         ; NOT WB CMD
  686  736E  68                PLA
  687  736F  A9 20             LDA #'           ; FOR WB, BLANK B'S IN ADR
```

```
CARD #  LOC   CODE      CARD
  688   7371  48        ASCX  PHA
  689   7372  68              PLA
  690   7373  60              RTS
  691                   ;
  692   7374  20 77 73  SPAC2 JSR SPACE
  693   7377  48        SPACE PHA                 ; SAVE A,X,Y
  694   7378  8A              TXA
  695   7379  48              PHA
  696   737A  98              TYA
  697   737B  48              PHA
  698   737C  A9 20           LDA #' '
  699   737E  20 C6 72        JSR WRT             ; TYPE SP
  700   7381  68              PLA                 ; RESTORE A,X,Y
  701   7382  A8              TAY
  702   7383  68              PLA
  703   7384  AA              TAX
  704   7385  68              PLA
  705   7386  60              RTS
  706                   ;
  707   7387  A2 02      T2T2  LDX #2
  708   7389  B5 ED      T2T21 LDA TMPC-1,X
  709   738B  48              PHA
  710   738C  B5 EF           LDA TMP2-1,X
  711   738E  95 ED           STA TMPC-1,X
  712   7390  68              PLA
  713   7391  95 EF           STA TMP2-1,X
  714   7393  CA              DEX
  715   7394  D0 F3           BNE T2T21
  716   7396  60              RTS
  717                   ;
  718                   ;INCREMENT (TMPC,TMPC+1) BY 1
  719   7397  E6 EE      INCTMP INC TMPC           ;LOW BYTE
  720   7399  F0 01           BEQ INCT1
  721   739B  60              RTS
  722                   ;
  723   739C  E6 EF      INCT1  INC TMPC+1         ;HIGH BYTE
  724   739E  F0 01           BEQ SETWRP
  725   73A0  60              RTS
  726                   ;
  727   73A1  E6 E4      SETWRP INC WRAP           ;POINTER HAS WRAPPED AROUND - SET FLAG
  728   73A3  60              RTS
  729                   ;
  730                   ; READ HEX ADR, RETURN HO IN TMPC, LO IN TMPC+1 AND CY=1
  731                   ;    IF SP CY=0
  732                   ;
  733   73A4  20 B3 73  RDOA  JSR RDOB           ; READ 2 CHAR BYTE
  734   73A7  90 02           BCC RDOA2           ; SPACE
  735                   ;
  736   73A9  85 EF           STA TMPC+1
  737   73AB  20 B3 73  RDOA2 JSR RDOB
  738   73AE  90 02           BCC RDEXIT          ; SP
  739   73B0  85 EE           STA TMPC
```

```
CARD #  LOC   CODE        CARD
  740   73B2  6C          RDEXIT RTS
  741                     ;
  742                     ;  READ HEX BYTE AND RETURN IN A, AND CY=1
  743                     ;    IF SF CY=0
  744                     ;    Y REG IS PRESERVED
  745                     ;
  746   73B3  98          RDDB    TYA                 ; SAVE Y
  747   73B4  48                  PHA
  748   73B5  A9 00               LDA #C              ; SET DATA = C
  749   73B7  85 EC               STA ACMD
  750   73B9  20 E9 72            JSR RDDC
  751   73BC  C9 CD               CMP #$0D            ; CR?
  752   73BE  D0 C6               BNE RDDB1
  753   73C0  68                  PLA                 ;YES - GO TO START
  754   73C1  68                  PLA                 ;CLEANING STACK UP FIRST
  755   73C2  68                  PLA
  756   73C3  4C B6 7C            JMP START
  757                     ;
  758   73C6  C9 20       RDDB1   CMP #'              ; SPACE
  759   73C8  D0 CA               BNE RDDB2
  760   73CA  20 E9 72            JSR RDDC            ; READ NEXT CHAR
  761   73CD  C9 20               CMP #'
  762   73CF  D0 CF               BNE RDDB3
  763   73D1  18                  CLC                 ; CY=0
  764   73D2  90 12               BCC RDDB4
  765                     ;
  766   73D4  20 EB 73    RDDB2   JSR HEXIT           ; TO HEX
  767   73D7  0A                  ASL A
  768   73D8  0A                  ASL A
  769   73D9  0A                  ASL A
  770   73DA  0A                  ASL A
  771   73DB  85 EC               STA ACMD
  772   73DD  20 E9 72            JSR RDDC            ; 2ND CHAR ASSUMED HEX
  773   73EC  20 EB 73    RDDB3   JSR HEXIT
  774   73E3  05 EC               ORA ACMD
  775   73E5  38                  SEC                 ; CY=1
  776   73E6  AA          RDDB4   TAX
  777   73E7  68                  PLA                 ; RESTORE Y
  778   73E8  A8                  TAY
  779   73E9  8A                  TXA                 ;SET Z & N FLAGS FOR RETURN
  780   73EA  60                  RTS
  781                     ;
  782   73EB  C9 3A       HEXIT   CMP #$3A
  783   73ED  08                  PHP                 ; SAVE FLAGS
  784   73EE  29 0F               AND #$0F
  785   73F0  28                  PLP
  786   73F1  90 02               BCC HEX09           ; 0-9
  787   73F3  69 08               ADC #8              ; ALPHA ADD 8+CY=9
  788   73F5  60          HEX09   RTS
  789                     ;
  790   73F6                      *=MP3+$F8
  791                     ;
```

```
MPI TIM PAGE 1

CARD # LOC    CODE      CARD
  792  73F8  CC 70  INTVEC .WORD NMINT        ; DEFAULT USER INTRQ TO NMINT
  793  73FA  00 70        .WORD NMINT
  794  73FC  06 70        .BYTE RESET
  795  73FE  52 70        .WORD INTRQ
  796                ;

END OF MOS/TECHNOLOGY 6501 ASSEMBLY VERSION 3
NUMBER OF ERRORS =    0,  NUMBER OF WARNINGS =    0
```

SYMBOL	VALUE	LINE DEFINED	CROSS-REFERENCES
R6	704B	187	185
SAVX	00FC	124	242 244 481 683
SETR	7CFB	302	331 357
SETWRP	73A1	727	724
SP	COFC	123	217 368
SPACE	7377	693	339 363 423 426 490 692
SPAC2	7374	692	251
START	7086	230	260 345 382 478 756
SC	7097	238	225
S1	7099	239	256
S2	7CB7	255	240
TMPC	00FE	125	127 201 220 337 343 422 430 492 504
TMPC2	COFF	126	128 494 499
TMPO	COFE	113	264 267 272 274 279 280 289 291 303 305 340 404 407 458 461 466 493 546 548 708 711 719 723 736 739
TMP2	COFC	114	263 266 414 416 710 713
TMP4	COF2	115	413 415 520 521 522 524
TMP6	COF4	116	
T2T2	73B7	7C7	425 428
T2T21	73B9	7C8	715
UINT	FFF8	95	150 228
WB	723B	481	433
WBF1	725A	498	505
WBF2	7262	5C3	496 500
WBNPF	724B	490	512
WB1	723C	482	515
WFC	71E2	435	477
WH1	72C7	455	449 452
WH2	721F	465	472
WC	71C2	421	322
WRAP	00E4	105	232 435 482 727
WROA	729A	539	355 488
WRCA1	72AB	546	540 542 544
WRCA4	729E	541	474
WROA6	72A2	543	
WRCB	72B1	555	341 457 460 463 469 545
WROC	72C6	578	235 259 445 503 507
WRPC	72AE	545	330
WRT	72C6	576	570 578 699
WRTWO	72CC	568	223 530
WRT1	72CE	582	586
XR	COFA	121	206 377
YR	COFB	122	207 378
ZTMP	70C9	278	393 442

INSTRUCTION	COUNT
ADC	9
AND	9
ASL	6
BCC	15
BCS	6
BEQ	11
BIT	0
BMI	0
BNE	33
BPL	5
BRK	1
BVC	0
BVS	0
CLC	4
CLD	1
CLI	1
CLV	0
CMP	11
CPX	1
CPY	0
DEC	6
DEX	8
DEY	1
EOR	4
INC	7
INX	0
INY	2
JMP	9
JSR	89
LDA	65
LDX	24
LDY	4
LSR	13
NOP	0
ORA	6
PHA	18
PHP	4
PLA	23
PLP	4
ROL	0
RTI	1
RTS	19
SBC	2
SEC	3
SED	0
SEI	0
STA	45
STX	11
STY	2
TAX	4
TAY	4
TSX	1
TXA	5
TXS	2
TYA	5

SYMBOL TABLE

SYMBOL	VALUE	LINE DEFINED	CROSS-REFERENCES
ACC	00F9	120	140 194 227 376
ACMD	00EC	112	246 248 253 486 511 749 [illegible] 774
ADRS	71CC	316	247
ALTER	713A	351	316
ASCII	735E	673	560 564
ASCX	7372	689	682 685
ASC1	7361	679	676
A2	714E	357	355
A3	714B	359	352
A4	715C	362	358
A5	7152	363	365
A9	715A	366	
BCCST	7238	478	436 483 516
BEQS1	7134	345	366 369
BX	7081	227	198
BYTE	70E0	285	364 410
BY2	70F2	297	292
BY3	70F5	298	286
B3	7058	201	142
B5	7073	219	
CMDS	71C6	309	239
CRDLY	00E3	104	163 531
CRLF	728A	528	219 233 385 438 487
CR1	7293	532	534
CADD	727C	518	297 402 405 408 456 459 462 468
CAVAIL	0008	85	660
CCMP	70C1	262	417 447 476 514
CIFF	00E5	106	265 269 450
CLX	733C	657	
CLY1	732C	636	611 635
CLY2	731C	635	532 576 583 614 631
CL2	7328	643	
CL3	7328	645	646 651
CSPLYM	711C	334	318
CSPLYR	7114	330	317
ERROPR	70BA	258	295 347 419
ERRP1	71BF	419	
ERRS1	7137	347	335
FLGS	00F8	119	209 302 374
GC	715C	368	319
GOTDAT	CCC4	66	665
HEXIT	73EB	782	766 773
HEXC9	73F5	788	786
HSP	716F	381	320
HSPTR	00E7	107	155 231 387 398 601
HSROP	CCF8	108	156 381 386
IJMP	70B4	253	250
INCTMP	7397	719	298 470 509
INCT1	739C	723	720
INTRQ	7052	154	795
INTVEC	73F8	792	149

SYMBOL	VALUE	LINE DEFINED	CROSS-REFERENCES
IOBASE	6ECC	87	88 89 90 91 92 93 94
LCNT	COFF	128	
LH	7174	384	321
LH1	717E	388	390 418
LH2	7195	401	395
LH3	71AA	410	411
MAJORT	00EA	110	154 171 184 640
MCLKIF	6E05	94	165 645
MCLKRD	6EC4	93	181 649
MCLKIT	6EC4	92	168 643
MDA	6EC1	89	
MDB	6E03	91	146
MDBK	0016	84	144
MINORT	00EB	111	189 641
MPA	6EC0	88	663
MPB	6E02	90	164 175 591 595 607 615 659 664 66E 668
MPC	70CC	97	138
MP1	71CC	98	245 316 317 318 319 320 321 322
MP2	72CC	99	
MP3	73CC	100	79C
MO	7123	337	332
M1	7127	339	344
NCMDS	0007	96	238 6E4
NMINT	70CC	140	792 793
OUT	72DA	550	582 612 617 633
OUT1	72E4	555	593
PCH	00F7	118	215 275 370
PCL	00F6	117	212 273 372
PREVC	00E9	109	243 351
PUTP	70DC	272	356
RAM64	FFC0	132	133
RCNT	00FE	127	295 362 401 440 453 454 455 471
RDEXIT	73B2	74C	738
RDFSR	733C	659	603 6E1
RDOA	73A4	733	334 354 412 424 427
RDOA2	73AB	737	734
RDOB	73B3	746	285 394 403 406 733 737
RDOB1	73C6	758	752
RDOB2	73D4	76E	755
RDOB3	73EC	773	762
RDOB4	73E6	77E	764
RDOC	72E5	6C4	23E 384 388 421 429 75C 76C 772
RDT	72E9	6D1	604
RDT1	72FC	6D7	6C5
RDT2	72FC	614	627
RDT4	73CE	625	623
RDT5	7319	632	587
RESET	7006	144	794
R0	7022	164	166
R1	70CC	149	152
R2	7028	168	172
R3	702A	169	177 179
R4	7034	174	17C
R5	7044	183	188

Cassette Interface

July 76
Byte

DIGITAL GROUP 1024 CHARACTER TV READOUT/CASSETTE INTERFACE CARD

General Design

This PC Board combines two functions needed by microprocessors, the ability to output data and messages on a low-cost TV set, and the ability to reliably store, retrieve, and exchange programs or data at low cost. The TV Readout will display 1024 characters, 16 lines of 64 characters per line, with upper and lower case alpha characters, Greek alphabet, math symbols, and special characters. The characters are formed from a 7 x 13 matrix of dots, producing easy to read characters with a normal height to width aspect ratio.

The cassette section provided circuits for recording data as well as receiving data previously recorded. Frequency Shift Keying is utilized, 2125 Hz being the Mark of "1" frequency, and 2975 Hz used as the Space or "0" frequency. The frequency shift keying system gives a better signal/noise ratio and the wide spacing of the harmonically unrelated frequencies permit the use of low cost home cassette recorders in spite of their generally poor "wow" and "flutter".

Software parallel to serial conversion systems are used for record, and software serial to parallel conversion systems for data playback. These software conversion systems permit complete flexibility in Data rate (from near Ø to 1000 bits per second), Codes utilized (ASCII, Baudot, etc.), and Error checking (Parity, CRC, etc.) inclusion.

TV Readout Description

The TV Readout consists of five interacting sections. They are Memory, Character Generation, Composite Video Output, Read Clock, and Write Clock. The memory section consists of seven 2102A or faster 1K memories, giving a possible storage of 1024 seven bit ASCII characters. The microprocessor, keyboard, or some attached circuit writes the characters one by one into the 2102's, and then the TV Readout continuously displays these characters until either more characters are entered, or the circuit is turned off.

The character generation circuit consists of two IC's, the MCM6571L character generator, and 74165 parallel to serial converting shift register. the 6571 takes the seven bit ASCII character coming from the memories and outputs 7 dots making up a character row for each of 13 potential rows making up each character. The 74165 loads these 7 dots coming out at a time into its internal memory, and then outputs these one at a time for serial transmission to a TV set. For more information on TV character generators, I would suggest reading an excellent article by Don Lancaster in June, 1974 Radio-Electronics (p. 48-52).

The video output section uses a 74151 data selector, a 7401 open collector NAND gate and a driver transistor to produce a low impedence composite video signal. The 74151 permits selecting either white characters on a black background, or black characters on a white background. In addition extermal binary level video (such as TV graphics) may be selected/inverted. The TV output is around 2 volts peak to peak with about a ½volt horizontal and vertical sync and blanking pedestal.

The Read Clock is the master control of the various sections. Starting from an initial frequency of 11.980 MHz, a countdown chain of three 74193's (IC's 26, 25, and 37) produce and 8µs horizontal sync when gated by 1/6 IC2, 1/2 IC27, 2/3 IC29, and 1/4 IC28. A 20 µs horizontal blanking circuit prevents loss of characters at the edges of the screen and is produced by the gating action of 3/4 IC17, 1/6 IC2, and 1/3 IC29. The resultant horizontal frequency is 15,598 Hz, somewhat lower than the standard 15,750 Hz, but usually only requires trimming horizontal hold slightly if at all.

The vertical countdown chain uses three more 74193's (IC's 1,15, and 5) to obtain a final vertical frequency of 60 Hz, syncronous with the AC line to avoid hum roll and wobble problems on low cost TV's. 3/6 IC7 and IC8 produce an 820µs Vertical sync pulse, 2/3 IC6 gives a ÷ 22 gating to IC's 15 and 5, and the 1/6 IC7 produces a 3.5ms Vertical blanking pulse.

A special feature of this TV Readout board is its ability to be externally syncronized to an external video timed base. This permits syncronizing the microprocessor's video countdown chain to an external video source such as a TV camera or a commercial TV program for titling, "Frame Grab", etc. operations. The horizontal countdown chain is syncronized by a short negative going pulse applied to connector pin U which will reset the horizontal counters and the horizontal sync pulse. The Vertical chain is reset by applying a short negative pulse to connector pin V.

The various Read Clock timings are brought out to the connector so that external video based systems (such as graphics) may be easily coupled with this TV system. As if these operations weren't enough, various timings from the Read Clock also tell which of the 13 rows, which make up each character, is being currently accessed, and loads the 74165 when the row of 7 dots is available from the 6571. The 11.980 MHz signal then shifts out 8 dot peroids (the 8th one is a horizontal space between characters) before the next dot load command occurs. All of these timings are very critical during the design phase, but the builder should have no problems, since no adjustments are needed. The Read Clock also controls which of 1024 characters is currently being inputed to the 6571 for dot encoding, except during Write Clock times.

I thought you'd never ask about the Write Clock. Well, it controls the entry of the characters from whatever external source into the 2102 memory bank. Several alternatives in character entry are possible. However, this design tries to be as simple as possible, yet give the user a very capable unit, particularly when using a microprocessor, or even mini, midi, or maxi processors.

A sequential entry system is utilized. A Home Reset control signal is developed by IC22 when it detects the 7 character defining input lines high ("1"). IC's 23, 13, and 3 are then preset so that the next character to be entered will result in its being displayed as the top leftmost character on the screen. The 2nd character will be viewed to the right of the first,....until on the 65th character a new line appears, displaying the 65th character. Up to 1024 characters are thus sequentially entered and displayed. If a 1025th and following characters are entered, an overwrite condition results, with the new page load displayed from the top

leftmost, the former character overwritten "gone forever". The display may be reset at any time. Screen erase consists of either 1024 or more ASCII "spaces" (Octal 240) and an ASCII ∎ (all bits on (either a 177 or a 377)), or an ASCII ∎ and exactly 512 ASCII spaces, the latter being preferable.

Memory writing occurs when the MSB goes high. The 74157's then allow the 74193's IC23, 13 and 3 in the Write Clock to control the memory address lines on a priority interrupt basis. 600 ns later, a 600 ns strobe pulse writes the new character into memory.

There is a parallel logic path to step the Write Clock address forward or backward without writing a character. This produces a "Pseudo Cursor" effect without the usual expense of a number of comparators, etc. A software "blink" may be easily implemented with a final result indistinguishable from a hardware cursor. The "Pseudo Cursor" logic consists of 1/4 IC16 and IC38 which detect the presence of an LSB, toggling the Write Clock 74193's up in count without firing the 74L123 (IC20) Write Strobe if not simultaneously brought high (indicating character entry then, of course). LSB + 1 high without the MSB toggles the Write Clock 74193's down in count, which backs up the cursor.

A 74122 (IC39) produces a short pulse each time the MSB is brought high, thereby blanking the screen while the memory updating process is taking place. This reduces the glitches appearing on the screen when high rate updating occurs. The only way to completely eliminate the glitches would be to only update during the Vertical blanking pulse, but this would seriously downgrade performance in some critical operations.

Cassette Interface Circuit Description

The previous 512 character Digital Group TVC used a tunable oscillator which required careful alignment. This requirement has been eliminated by using a digital frequency synthesizer countdown chain. The TV master oscillator is divided by either 5650 or 4030 to get the 2125 or 2975 cassette frequencies. The actual frequencies are a few Hertz low, but well within tolerances. The main cassette countdown chain consists of IC's 45, 46, and 43. IC49 is used to gate an early reset to achieve the 2125 tone, and IC48 gates an early reset for 2975. The actual output of this chain is 10 times too high, and the 7490 (IC42) provides a ÷ 10 smoothing and squaring function. A logic level input at pin 18 on the connector controls the resultant audio frequency at output pin 10. A high input ("1") produces a 2125 Hz output, and a low output ("Ø") results in 2975 Hz. The output wave shape is a symetrical square wave. The 47K (R13) resistor in series with the output is a typical value to be used when coupling to the low level, low impedence external microphone inputs of most cassette recorders.

The cassette receive circuitry detects the prerecorded frequency shift keying and produces a "1" or a "Ø" output as a result of a detected 2125 Hz or 2975 Hz tone at the input. IC40 is a clamped limiter which prevents variations in amplitude from affecting the resultant detection process. The output of IC40 should be about 1.2 volts p-p, roughly a square wave of the incoming frequency, constant in amplitude regardless of tape volume setting or minor tape "dropout" problems.

Two bandpass active filters then amplify a tone 5 times when actually tuned to their respective frequencies of 2975 Hz for the top filter and 2125 Hz for the lower filter. The further off the tuned frequency the tone is, the less amplification the filter will produce. The actual resonance points of the filters may be easily adjusted by merely trimming the multiturn potentiometers in each filter.

Full wave active detectors produce rectified full wave pulses at the summing junction, pin 5 of IC47. The 2975 Hz tones are rectified +, and the 2125 Hz tones are rectified -. As tones depart from either exact frequency, a value less + or - is produced until approximately midway a summed voltage of Ø results.

A 3-pole lowpass active filter then removes the remaining traces of pulsating DC from the summed signal with almost no effect on the data pulses up to a speed of 1000 bits per second. If lower data rates were to be utilized, an improved signal to noise ratio could be obtained by multiplying the values of C35, C37, and C38 by the reciprocal of the data rate difference. I doubt you would notice any operational difference, however.

The final section is a slicer connected 741 (IC51). This op amp detects whether the voltage at its pin 2 is + or - with respect to the constant voltage at its pin 3. The output voltage will then swing either to nearly +5 or to nearly -12. A forward biased germanium diode prevents the actual output voltage from going less than ≈ -.2 volts, so that valid TTL levels are not exceeded. An offset adjusting pot allows the output to be placed in a "Mark Hold" condition when no tone input is being detected. 2/4 7400 (IC50) provides output TTL level buffering, and allows data inversion by tapping the output to the pin 11 section if a customized circuit required this modification.

Construction

Tools: Fine tipped, low wattage soldering iron, "wire solder" (around 20 gauge resin solder), small diagonal cutters.

Test Equipment: Ohmeter
Audio Generator helpful
10 MHz or better triggered sweep oscilloscope
Frequency Counter
Microprocessor, Mini, etc.

Estimated Construction Time: 3-6 hours

1. Insert the 24-pin socket, 5 8-pin sockets, 28 16-pin sockets, and 17 14-pin sockets into the PC board. If the sockets have a keyway indication, orient this away from the connector. Note: the top side of the board is indicated by The Digital Group label.

2. Invert the board and carefully solder in the sockets. A special plating process is used by The Digital Group to minimize solder joint troubles. We would suggest a "warmup area" by starting with the cassette interface sections of the card.

3. Insert and solder the 17 resistors in the TV Readout section enclosed by the +12 bus line. Insert and solder the 22 resistors in the cassette section.

4. Insert and solder the zener diode, the germanium diode, and the 8 silicon diodes. Note: all of the diodes are oriented with their cathode or "bar" end oriented towards the right.

5. Insert and solder the output transistor in the TV Readout section.

6. Insert and solder the two 220 pfd and the 330 pfd and the 100 pfd condensers in the TV Readout section.

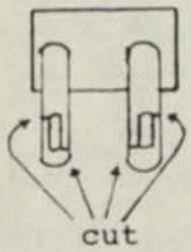
7. Insert and solder the fourteen condensers in the Cassette Interface section.

8. Insert and solder the three potentiometers in the Cassette section. Note that the potentiometer is a 50K, the other two are long multi-turn 500 ohm units.

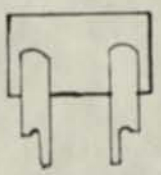
9. Insert and solder the various bypass condensers in the TV Readout section. Note: the positive (+) end of the dipped tantalum condensers is indicated by the vertical marking (paint strip) along one side. Additional holes have been provided between IC's 9 and 30 for additional input bypassing with 50-200 pfd condensers if your installation so requires.

10. Trim the crystal socket's pins as shown to fit into the crystal holes.

Pin view:



Result:



Press the rear tab into the board hole provided for it. Solder the pins and the rear tab.

The socket provides a space-saving flat mount as well as avoids soldering to the heat-sensitive crystal.

11. At this point, measure the resistance between ground (pin 20) and the other voltage supply pins (19, 21, & 22). A very low resistance indicates a bad bypass or a solder bridge short somewhere.

12. Insert the IC's in the TV Readout section except for the memories (2102's) and the MCM6571L character generator. The notch or pin 1 end of each IC should be oriented away from the connector end of the board. Measure the resistance between pins 19 & 20, noting the value. Reverse the ohmeter leads and remeasure. A shorted reading indicates a bad IC, and near equal readings indicates a reversed IC.

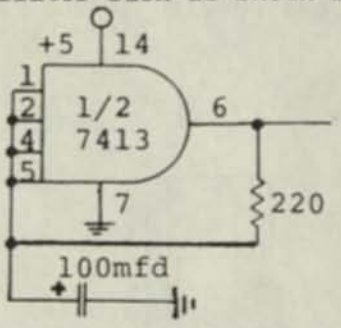
13. Temporarily groung pin 1 of the TV readout and connect a TV set modified for direct video, or a commercial TV monitor, between pins 16 (video) and 20 (ground).

14. Putting a +5 voltage between pins 19 (+) and 20 (Ground) should result in 64 vertical white columns on the screen. Refer to "Troubles" section if this does not happen.

15. Connect the other ±12 supplies, and turn on power again. Measure the voltages on pins 1, 2, and 3 of the MCM6571L socket. They should measure -5, +5, and +12 respectively.

16. Plug in the 2102's and the 6571. The temporary grounding jumper to pin 1 should still be connected as well as the TV monitor. Turning on power this time should result in a random display of 1024 characters on the screen. The actual character at each location is determined by the chance bit structure at the memory locations. Remove the temporary grounding jumper from pin 1 when done with this test.

17. Complete testing of the TV Readout is best performed under microprocessor control, and sample diagnostic programs are included with The Digital Group Systems. "Breadboard diagnostic testing" may be accomplished by temporarily tieing each of pins 2 - 8 to +5 through a 1K resistor. Tie pin 1 to the output of a simple oscillator such as shown below:



Grounding pins 2 - 8 to ground should produce:

pin to ground	Character
8	∿
7	}
6	{
5	w
4	o
3	
2	$\overline{?}$

18. Plug in the twelve IC's in the Cassette section.

19. Connect a calibrated frequency counter between pin 10 and ground.

20. Apply +5 and ±12 voltages to the board. With the Cassette Write input pin 18 open or tied to +5, the frequency counter should read approximately 2120 Hz.

21. With voltages still applied, ground input pin 18. The frequency counter should now read approximately 2970 Hz. This completes cassette write turn up. Easy, isn't it.

22. Jumper pins 10 and 9 together. This permits using the Write Cassette section as a master oscillator to align the Read Cassette section.

23. Measure the output at pin 6 of the 741 limiter (IC40) with an oscilloscope. The waveshape should be an approximate square wave of about .6 volts p-p.

24. Keeping the jumper from ground to connector pin 18, (the frequency counter should read about 2970 yet) measure the output at pin 7 of the 5558 active bandpass filter (IC41). Turn the 2975 trimmer pot (R30-the pot in the right corner) until the signal exactly peaks, and leave at this point.

25. Move the jumper on connector pin 18 from gorund over to +5. The frequency counter should now read about 2120. Measure the output at pin 1 of IC41. Turn the 2125 pot (R29-the middle pot) until the signal exactly peaks, and leave at this point.

26. Measure the detected voltages at pin 5 of IC47. When the input frequency approaches 2125, the output should go -. When approaching 2975, the output should go +. Trouble in this area would most likely be caused by reversed or defective diodes, or adjacent line shorts.

27. Measure the voltage at the cathode (bar) end of the output clamping germanium diode (G1). If desired, remove the jumpers and attach an audio oscillator. Sweeping the frequency between 2125 and 2975 Hz should result in a clean voltage jump somewhere between 2125 and 2975. Be sure that the negativemost voltage at this point is about -.2 volts.

28. Remove the jumper between pins 9 and 10 and short input pin 9 temporarily to ground. Measure the output at pin 6 of IC40 again. A stable condition (no oscillation) should be seen. Connect the oscilloscope to the cathode of G1 again. Adjust the balance potentiometer (R18 - the small leftmost pot) clockwise so that the voltage is at a - level. Slowly turn the potentiometer counterclockwise until the voltage jumps + and leave setting at this point.

29. Disconnect the temporary jumper from connector pin 9 and reconnect the audio oscillator. Perform step 24 again. If all proceeds well at this point, the cassette interface is ready to receive data.

Troubles - General

1. One of the more difficult troubles to find is an IC pin which was bent under the IC when it was inserted. Any unusual pressure when inserting an IC should be investigated.

2. Every pin should be soldered. The most frequent cause of trouble is an unsoldered pin, generally an end IC pin. Carefully sighting down parallel rows of pins usually finds any that are not soldered.

3. When troubleshooting with a 'scope probe, measure from the top side of the IC, not the bottom, to eliminate a bent under pin problem or defective socket from misleading.

4. Before ever plugging in any IC's, always measure the voltages at the PC board and at the pins of the more expensive IC's, like the 6571.

5. When handling IC's, avoid static charges. Run your house humidity high, and ground yourself ty touching a grounded chassis before touching IC's.

6. Beware of solder splashes and drilling errors. Please inform The Digital Group of board manufacturing errors that you detect. A flashover or splash on the topside would be very difficult to find after soldering the sockets. The black socket body of the sockets used in The Digital Group kits may be pried off after removing the IC should a hidden splash be suspected.

7. Beware of shorts in the cassette area between component leads and underlying circuitry.

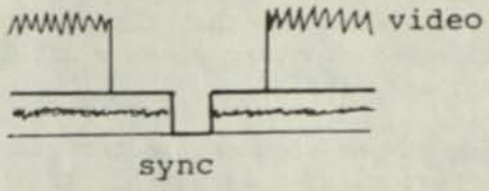
Specific Troubles

No white colums on the screen at step 14.

1. Bad connection between connector pin 16 and TV.
2. Temporary jumper from connector pin 1 to ground not connected.
3. Crystal not oscillating. Check for pulses at pin 1 of IC16.
4. Horizontal Countdown chain defective. Successively measure output at pin 3 of IC's 26, 25, and 37. Each should be progressively lower in frequency.
5. Vertical Countdown chain defective. As above #4, but measure IC's 1, 15, and 5.
6. Defective video mixer. Look for pulses at pins 1 and 13 of IC19.

Poor or lacking syncronization at step 14.

1. TV is overloaded by the ≈ 3 volts of video. Swamp the video with a 10 ohm resistor to see of sync & video stabilizes.
2. Check for Horizontal and Vertical sync and blanking pulses at connector pin 16. A 75 ohm load should be attached. The pattern should look like:



   a. If Horizontal Sync is defective, check IC's 2, 27, 28, and 29.
   b. If Vertical Sync is defective, check IC's 7 and 8.
   c. If Horizontal Blank, check IC's 2, 17, and 29.
   d. If Vertical Blank, IC7.

No characters at Step 16.

1. Missing voltages at the MCM6571 (IC11).
2. Defective Character generator.
3. Defective 74165 (IC10) or 74157 (IC18).
4. Defective logic signals to and from IC11 and IC10. All inputs and outputs should be pulsing at valid TTL levels (Ø to .8 volts = low/ 2 to 5 volts = high).
5. Pins 11 and 10 of 74151 (IC18) not at +5.

Wrong character(s) in display

1. Miswired or misjumpered input.
2. Defective Memory IC. Note: the bit difference between the intended character. IC30 is the memory for the Least Significant Bit (LSB) of the character... and IC36 is the Most Significant Bit's (MSB) memory.
3. Defective 74157(s) - IC's 24, 14, and 4.
4. Shorted lines in the memory and write clock area.

"Twinkling" character on TV

1. Slow memories. 500 nanoseconds or faster 2102's must be used.
2. Overheated memories. Access times increase with heat.
3. Slow 6571L - none seen so far, but possible.

Uneven lighting of leading and trailing edges of characters, esp. "H".

1. Monitor bandwidth too low produces a dim left side of H, bright on the horizontal bar part.
2. Incorrectly high peaked monitors give an excessively bright left edge to characters such as "H".
3. Dim right side of "H" and other characters may be monitor or may require increasing the clock lag condenser (IC43) in value. Too high of a value will reduce the left side of characters such as "H".

Won't write characters

1. Missing Storbe pulse, or continuous level on MSB input (connector pin 1).
2. No Write pulse from 74L123 (IC20). Measure at pin 12 of IC20, looking for an ≃ 600 ns negative going pulse. Connecting the MSB (connector pin 1) to a ≃50KHz TTL clock will permit viewing on lower cost oscilloscopes.
3. Write Clock not toggling. With above temporary oscillator inputting to MSB, look for pulses at pin 3 of IC's 23, 13, and 3.
4. Defective Read/Write Multiplexers (IC's 24, 14, and 4.

Extraneous Characters

1. Noise on the input lines to the memory, particularly on the MSB (connector pin 1). Pads for C1, C2, and C3 - small pfd condensers used on the input line to suppress most noise sources. This trouble generally shows up as an α appearing on the screen when another port is addressed.
2. Data sent to the TV character generator faster than it can handle. Data must be valid for 1.5 microseconds following the rise of MSB strobe. Faster data rates can be handled by reducing the value of the condensers in the 74L123 (IC20) Write strobe singleshot. Alternatively, a data hold loop consisting of NOP's can slow the data output to the readout.
3. Defective or slow memories. Look at the bit pattern of the extraneous character to determine if a single memory is bad.
4. More bypassing required. A number of unused voltage bypassing pads at the top of the TV Readout section have been included should your particular system require them.

Defective level output from Cassette Input Limiter

1. None at all: Check for ±12 to IC40.
2. Too high output level. Diodes (S3 and S4) open or one is reversed.

Bandpass Active Filter Problems

1. Check by sweeping with audio oscillator for proper range.
2. Swap 5558 (IC41) with IC's 44 and 47.
3. Check for shorts or out of tolerance (5%) condensers C30, C31, C32, or C33. Disc ceramics are a no-no in tuned circuits!

Full Wave Detector

1. Diodes open, reversed or shorted.
2. Defective 5558 (IC44).

Low Pass Active Filter

1. Shorted or out of tolerance condensers.
2. Defective IC47.

Output Slicer (IC38)

1. Reversed, open, or not Germanium diode at G1.
2. Defective or missoldered resistors in pin 3 circuitry of 741 (IC51).
3. Defective 741 (IC51).

1024 CHARACTER READOUT & CASSETTE INTERFACE - PARTS LIST

IC's	
IC30,36	7 - 2102-1 or better
IC11	1 - MCM6571L
IC9, 17, 28, 50	4 - 7400
IC19	1 - 7401
IC16	1 - 7402
IC2, 7	2 - 7404
IC6, 29	2 - 7410
IC27	1 - 7420
IC8, 22, 48, 49	4 - 7430
IC42	1 - 7490

IC's	
IC39	1 - 74122
IC20, 38	2 - 74L123
IC18	1 - 74151
IC4, 14, 24	3 - 74157
IC10	1 - 74165
IC1, 3, 5, 12, 13, 15, 21, 23, 25, 26, 37, 43, 45 46	14 - 74193
IC40, 51	2 - 741
IC41, 44, 47	3 - 5558 or LM1458

Capacitors	
C2	1 - 100 pfd mica
C4, 5	2 - 220 pfd mica
C43	1 - 330 pfd mica
C24	1 - 1000 pfd mica
C35	1 - .0047 mylar
C30 - C33	4 - .01 polystyrene (may be marked 10000)
C37	1 - .01 mylar
C38	1 - .015 mylar

Diodes	
S1 - S8	8 - 1N914 or 1N4148
G1	1 - 1N48 or eq. Germanium
Z1	1 - 5V 1 watt zener (1N4733 or eq.)
T1	1 - 2N5129/2N2369

Bypass Capacitors
24 - .01 mfd disc
4 - 1 mfd tantalums

Crystal
1 - 11.980 MHz

Misc
5 - 8 pin sockets
17 - 14 pin sockets
28 - 16 pin sockets
1 - 24 pin sockets
1 - crystal holder
1 - documentation

Resistors - all ¼ watt 5% unless noted	
R11	1 - 22 ohm
R12	1 - 220 ohm
R31	1 - 390 ohm
R1, 2, 10	3 - 470 ohm
R28	1 - 470 ohm ½ watt
R32	1 - 620 ohm
R5, 42	2 - 1K
R6, 7, 8, 9, 14	5 - 2.2K
R22	1 - 4.7K
R3, 4, 22	3 - 6.8K

Resistors	
R16, 17, 19, 20, 21, 26, 27, 35, 36, 37, 38	11 - 10K
R15	1 - 33K
R13, 24, 25, 33	4 - 47K
R34	1 - 68K
R39, 40, 41	3 - 100K
R29, 30	2 - 500Ω trimpot
R18	1 - 50K pot

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po box 6528 denver, colorado 80206 (303) 777-7133

1024 Character TVC

Front of Board

Pin	Function	
1	MSB	Strobe
2	MSB	
3	MSB	
4	MSB	Data to TV
5	MSB	
6	MSB	
7	MSB	
8	LSB	
9	Data from Cassette	
10	Data to Cassette	
11	Clock	
12	H sync	
13	V sync	
14	H Blank	
15	V Blank	
16	Video	
17	Data to CPU	
18	Data from CPU	
19	+5	
20	Ground	
21	+12	
22	-12	

Pin Side of Board

Pin	Function	
A	P	
B	A	
C	B	
D	C	Horz
E	D	
F	E	
H	N	
J	F	
K	G	
L	H	
M	I	Vert
N	J	
P	K	
R	L	
S	M	
T	Data Inv	
U	H Preset	
V	V Preset	
W	Graphic Input	
X	Graphic Select	
Y	not used	
Z		

512 TO 1024 UPGRADE SPECIAL DIRECTIONS

This 512 to 1024 character upgrade kit permits using most of the 512 character IC's in addition to a new board, sockets, resistors, condensers and miscellaneous parts to achieve a 1024 character TV readout.

Steps:

1. Remove all IC's from your 512 board except IC27 (74L00), IC23 (74123), and IC33 (566).

2. Add the 34 IC's just removed to the IC's supplied with the 1024 character upgrade kit.

3. Continue with regular 1024 character readout directions.

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1024 CHARACTER READOUT & CASSETTE INTERFACE UPGRADE - PARTS LIST

IC's	
(IC30, 36)	7 - 2102-1 or better
(IC11)	1 - MCM6571L
IC9, 17 (28, 50)	4 - 7400
(IC19)	1 - 7401
IC16	1 - 7402
(IC2, 7)	2 - 7404
IC6, (29)	2 - 7410
(IC27)	1 - 7420
IC8, 22, (48, 49)	4 - 7430
IC42	1 - 7490

IC's	
IC39	1 - 74122
IC20, 38	2 - 74L123
IC18	1 - 74151
(IC4, 14, 24)	3 - 74157
(IC10)	1 - 74165
IC1, 3, 5, 12, 13, 15, 21, 23, 25 (26, 37, 43, 45, 46)	14 - 74193
(IC40, 51)	2 - 741
(IC41, 44, 47)	3 - 5558 or LM1458

Capacitors	
C2	1 - 100 pfd mica
C4, 5	2 - 220 pfd mica
C43	1 - 330 pfd mica
C24	1 - 1000 pfd mica
C35	1 - .0047 mylar
C30 - C33	4 - .01 polystyrene (may be marked 10000)
C37	1 - .01 mylar
C38	1 - .015 mylar

Diodes	
S1 - S8	8 - 1N914 or 1N4148
G1	1 - 1N48 or eq. Germanium
Z1	1 - 5V 1 watt zener (1N4733 or eq.)
T1	1 - 2N5129/2N2369

Bypass Capacitors	Misc
24 - .01 mfd disc	5 - 8 pin sockets
4 - 1 mfd tantalums	17 - 14 pin sockets
	28 - 16 pin sockets
Crystal	1 - 24 pin sockets
1 - 11.980 MHz	1 - crystal holder
	1 - documentation

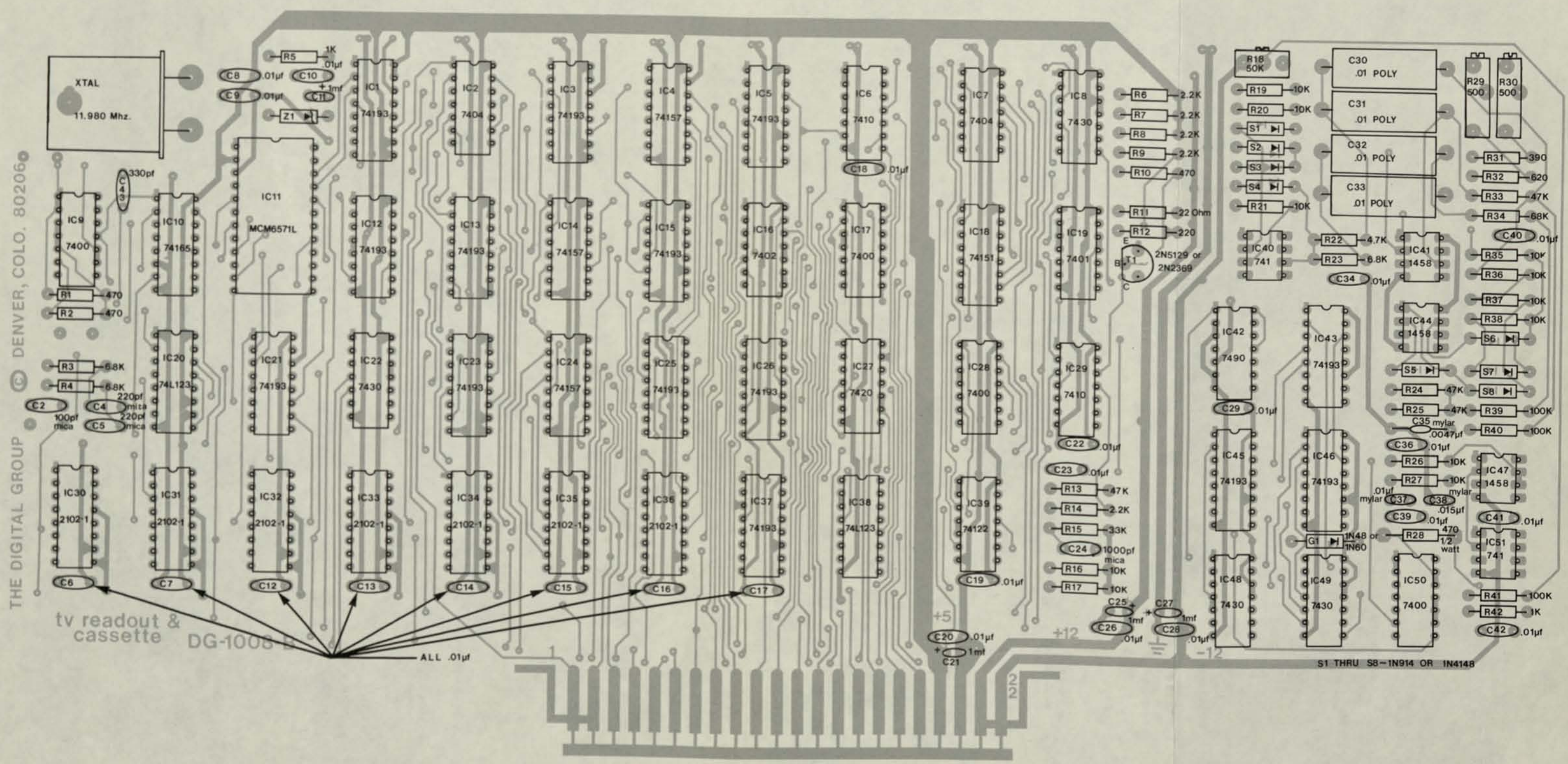
Resistors - all ¼ watt 5% unless noted

R11	1 - 22 ohm
R12	1 - 220 ohm
R31	1 - 390 ohm
R1, 2, 10	3 - 470 ohm
R28	1 - 470 ohm ½ watt
R32	1 - 620 ohm
R5, 42	2 - 1K
R6, 7, 8, 9, 14	5 - 2.2K
R22	1 - 4.7K
R3, 4, 22	3 - 6.8K

Resistors	
R16, 17, 19, 20, 21, 26, 27, 35, 36, 37, 38	11 - 10K
R15	1 - 33K
R13, 24, 25, 33	4 - 47K
R34	1 - 68K
R39, 40, 41	3 - 100K
R29, 30	2 - 500Ω trimpot
R18	1 - 50K pot

( ) indicates IC's removed from 512 Character Readout and Cassette Interface

1024 CHARACTER TV READOUT & CASSETTE INTERFACE



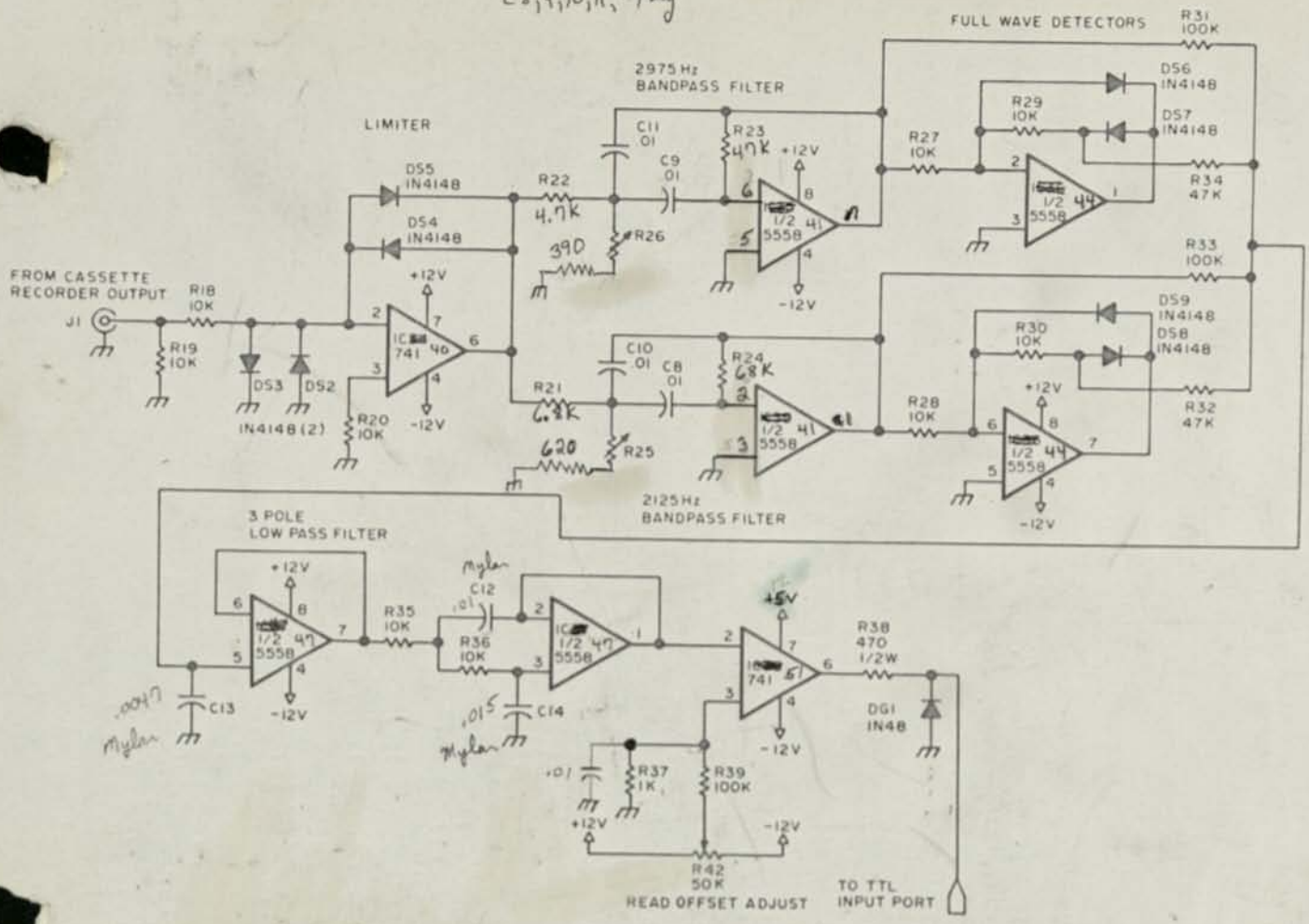
THE DIGITAL GROUP

1024 CHARACTER TV READOUT

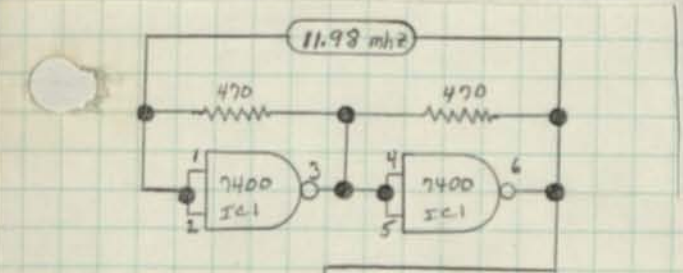
CASSETTE INTERFACE

3	77193	
1	7790	
1	7900	
2	7930	
2	7941	
3	5558	

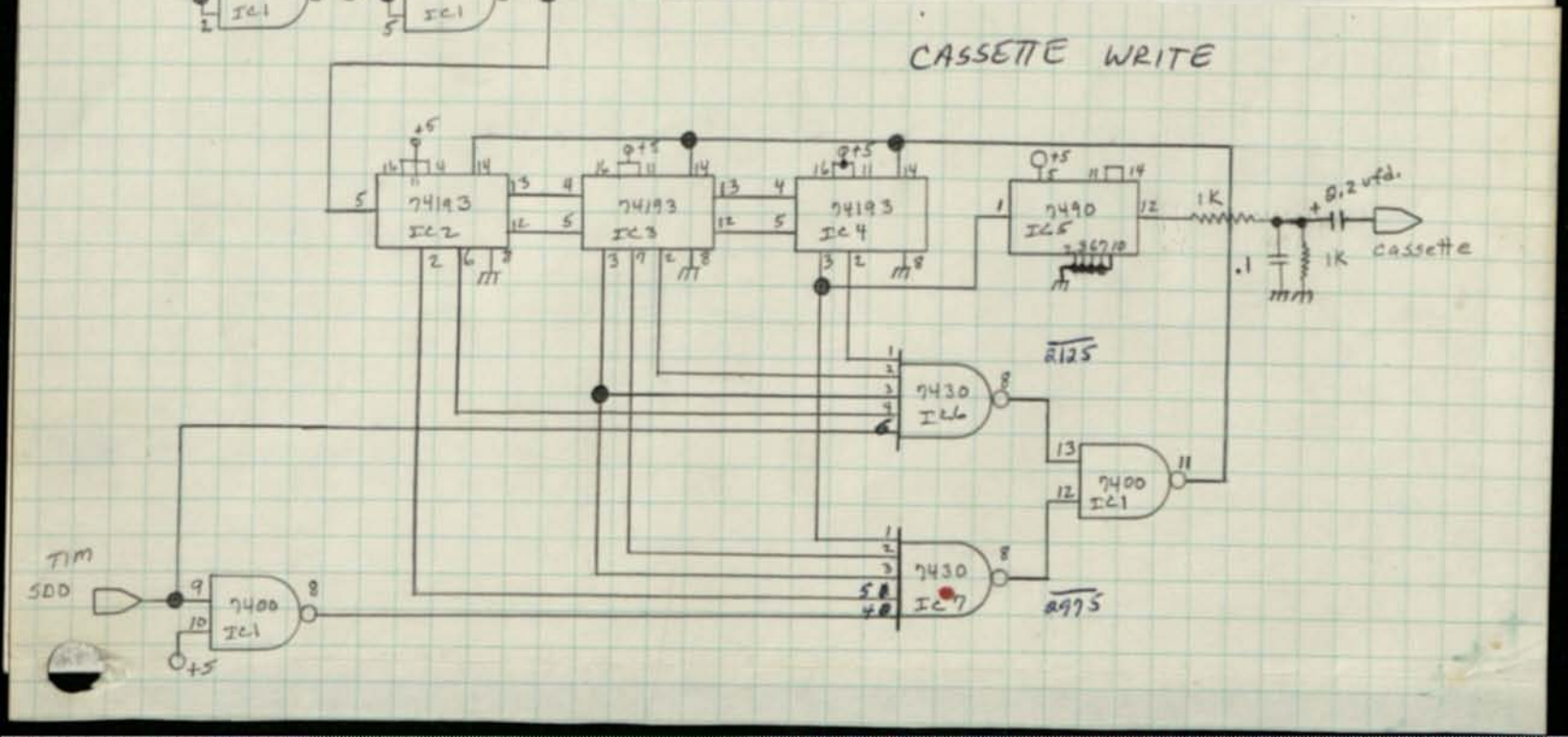
C8, 9, 10, 11, - Poly



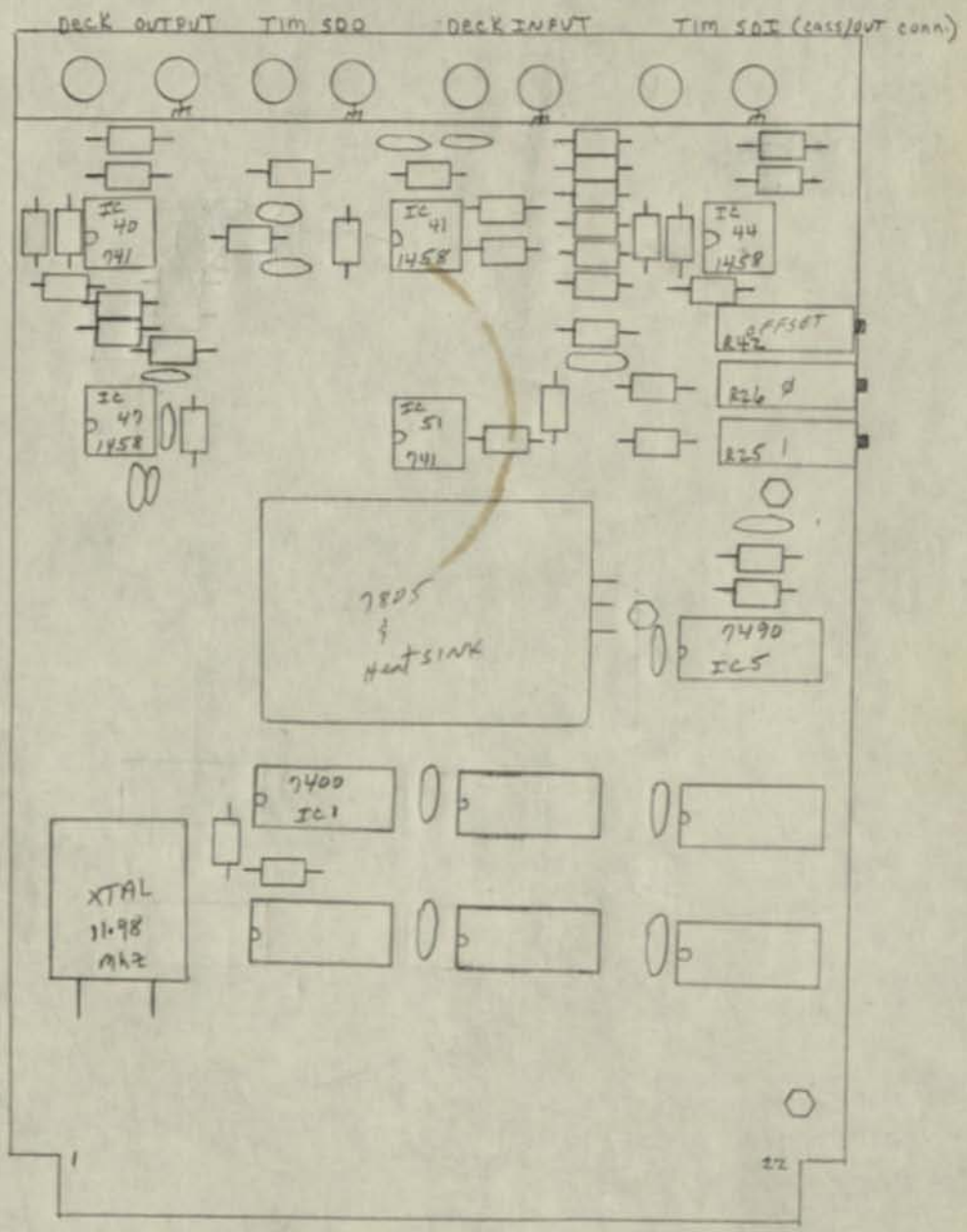
CASSETTE READ



CASSETTE WRITE

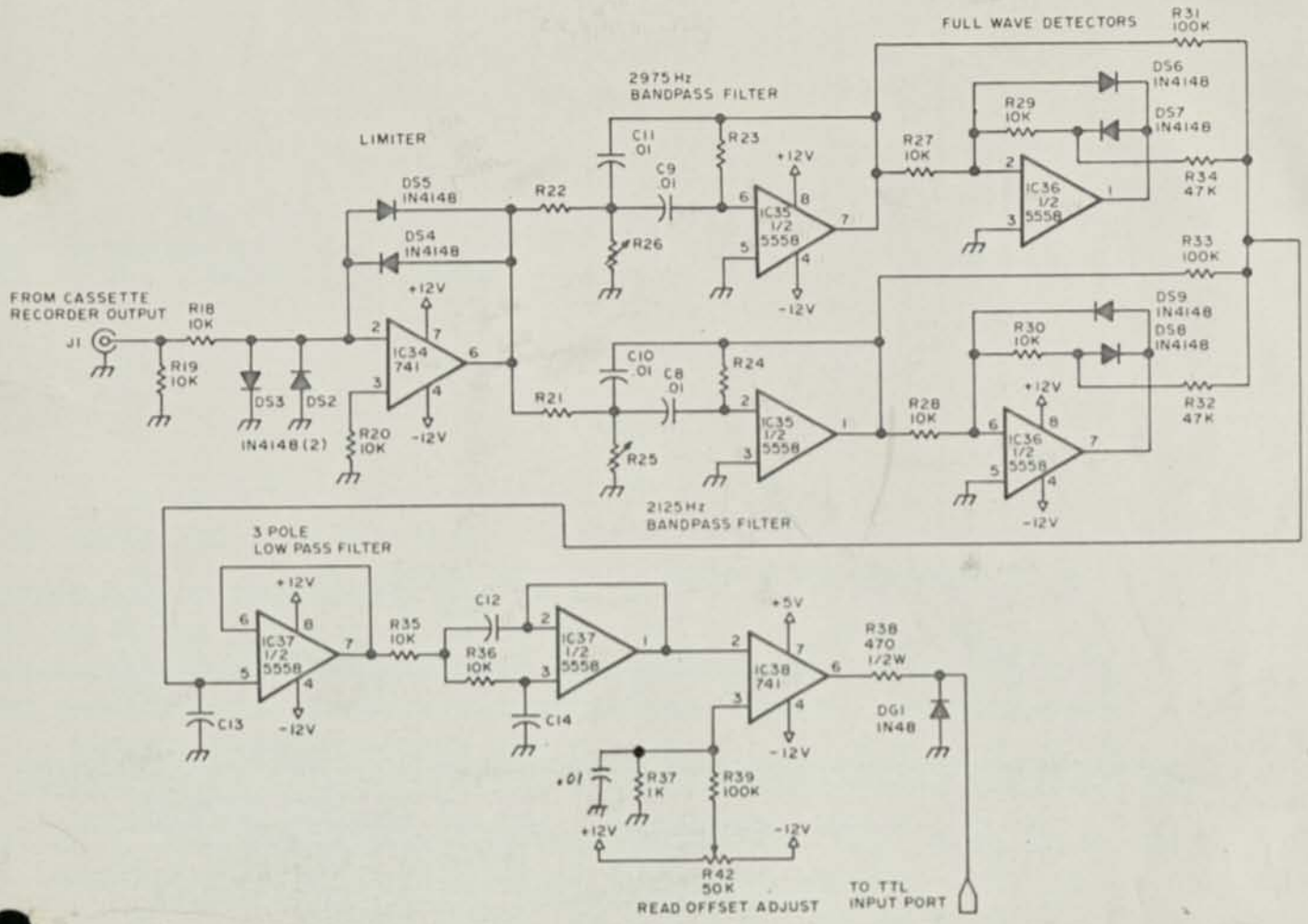


CASSETTE INTERFACE Bd.



Read Section

Write Section


FULL WAVE DETECTORS
R31 100K
DS6 IN4148
DS7 IN4148
R29 10K
R27 10K
R34 47K
IC36 1/2 5558
2975 Hz BANDPASS FILTER
LIMITER
C11 .01
C9 .01
R23
+12V
DS5 IN4148
DS4 IN4148
R22
R26
IC35 1/2 5558
-12V
R33 100K
FROM CASSETTE RECORDER OUTPUT
J1
R18 10K
R19 10K
DS3
DS2
IN4148 (2)
+12V
IC34 741
R20 10K
-12V
DS9 IN4148
DS8 IN4148
R30 10K
R32 47K
C10 .01
C8 .01
R24
R21
R25
R28 10K
2125 Hz BANDPASS FILTER
3 POLE LOW PASS FILTER
C12
R35 10K
R36 10K
C13
C14
IC37 1/2 5558
+5V
IC38 741
R38 470 1/2W
DG1 IN48
.01
R37 1K
R39 100K
R42 50K
READ OFFSET ADJUST
TO TTL INPUT PORT

	Low Filter			High Filter			Low Pass Filter			VCO	
	R21	R24	R25 *	R22	R23	R26 *	C13	C12	C14	R12	R15
2125-2975 Hz 1100 Baud	6.8 k	68 k	938	4.7 k	47 k	697	.0056 μF	.01	.015	2.7 k	1.3 k
1200-2400 Hz 300 Baud (Simple)	6.8 k	68 k	4173	4.7 k	47 k	1162	.0056 μF	.01	.015	470 k	2.7 k
1200-2400 Hz 300 Baud (Correct)	12 k	120 k	1668	5.6 k	56 k	906	.015 μF	.033	.047	470 k	2.7 k
2125-2295 100 Baud (Simple)	6.8 k	68 k	938	4.7 k	47 k	1301	.0056 μF	.01	.015	47 k	2.7 k
2125-2295 100 Baud (Correct)	36 k	360 k	156	27 k	270 k	179	.056 μF	.1	.15	47 k	2.7 k

*** means that the value so indicated is the typical calculated value. The precise value is dependent on component tolerance.**

Table 1: Theoretical values of components for alternate frequencies. This table gives values of components to be used with the circuits of figures 1 and 2 in order to make this cassette interface work with several alternate specifications. See the text for a definition of the various comments at the left of the table.

Potential Troubles

Knowing about potential problem areas is a first step to minimization of their effects. Troubles seem to break down into *six* classes.

- Cassette recorders and the cassettes used: A marriage between your $1000 microprocessor and junior's $20 cassette recorder, which has been using 30¢ cassettes for the last five years, will not produce happy offspring! I have been using a Superscope C-104 for the past year, and can report no failures except for defective cassette tapes. The C-104 has several attractive features. Besides the usual conveniences such as index counter, cuing, etc, it has a variable readback speed control, dandy for out of spec cassettes from friends. Inside, another special motor speed control potentiometer is located near the speaker which allows precisely setting the record/write speed. Quality control seems good overall, and the list price of $120 (cheaper at discount stores) is worth the investment. Don't waste your money on cheap cassettes. Sony Low Noise C-45s have been generally good. Some $2 – $4 Data Certified Cassettes are superior, but not needed.
- Microprocessor caused problems: Some microprocessor designs will not work directly with this interface system. This interface was designed to be connected directly to a single bit IO port, with the processor handling all of the bit timings through timing loops. If your processor must periodically catch its breath for such things as dynamic memory refreshing, you may be unable to directly use the "Software UART" system. What a shame! However, a hardware UART will permit using the system even with a system of this nature.
- Cabling problems: It is possible to connect your cassette recorders with the read and write cables reversed. Enough crosstalk from the write line to the read limiter existed to give the appearance of data being read, but so many errors resulted that the programming would not run.
- Tuning problems: Circuit tuning is the most common problem. *Carefully* tune the active filters!
- Cassette Crashes: Cassette damage is frequent on tapes which have always worked before, but now mysteriously fail. The most common cause of this is removing a cassette from the recorder without completely rewinding. The exposed oxide then gets damaged, and is no longer usable.
- Miscellaneous circuit problems:

Defective level output from cassette read limiter.
1. None at all: Check for ±12 V to IC34, and IC34.
2. Too high output level: Diodes (DS4 and DS5) open, or one is reversed.

Bandpass active filters don't filter.
1. Off frequency
2. Bad 5558
3. Check for shorts or out of tolerance condensers C8, C9, C10, or C11. Disk ceramics are a "no-no" in tuned circuits.
4. Resistors improperly wired or inserted.

Full wave detector does not work as described:
1. Diodes open, reversed or shorted.
2. Defective IC36.

Low pass active filter fails to work:
1. Shorted or out of tolerance condensers.
2. Defective IC37.

Output slicer (IG38) fails to produce TTL levels:
1. Reversed, open or not Germanium diode at DG1.
2. Too heavily loaded output. This circuit should drive no more than one TTL load (standard for most IO ports).

VCO won't oscillate.
1. Defective 566 (IC33).
2. Shorted condenser C6.

VCO has parasitic oscillation (high frequency):
1. C7 not connected.
2. Defective 566.
3. C6 is open, producing a very high frequency.

VCO won't tune to frequency or stay there:
1. Out of tolerance or defective C6. You really didn't use a disk ceramic here, did you?
2. Defective 566.
3. Non-TTL levels used to drive VCO.
4. Defective potentiometers R40 or R41.
5. DS1 or DZ2 reversed or defective.

Listing 1: Stand Alone Suding Cassette Input Program. This program is a self contained data transfer routine which will transfer a block of data from cassette to split octal memory locations xxx/xxx through yyy/000. This program assumes that MEMTOCAS (see listing 2) was used to create the tape being read. A more generally useful input facility would be modelled on this program and linked to a system monitor as a subroutine.

Split Octal Address	Octal Code	Label	Op.	Operand	Commentary
<0>/100	041 xxx xxx	CASTOMEM	LXI	H,xxx/xxx	Load starting address in HL pair;
<0>/103	021 010 000	STARTBYT	LXI	D,000/000	Load E, clear D;
<0>/106	333 001	SYNCHLOO	IN	1	Port 1 bit 0 read for input;
<0>/110	346 001		ANI	1	Mask all but bit 0;
<0>/112	302 106 <0>		JNZ	SYNCHLOO	If not start bit then reiterate loop;
*<0>/115	006 300		MVI	B,300	Time delay to middle of first data bit*;
<0>/117	005	WSYNCH	DCR	B	Decrement synch wait count;
<0>/120	302 117 <0>		JNZ	WSYNCH	If not done then keep waiting;
<0>/123	333 001	GETDATA	IN	1	Read port 1 bit 0 again;
<0>/125	346 001		ANI	1	Mask all but bit 0 again;
<0>/127	202		ADD	D	Sum old bits with new bit;
<0>/130	017		RRC		Rotate new and old into next position;
<0>/131	127		MOV	D,A	Save result back in D;
*<0>/132	006 200		MVI	B,200	Time delay between bits;
<0>/134	005	WDATA	DCR	B	Decrement data wait count;
<0>/135	302 134 <0>		JNZ	WDATA	If not done then keep waiting;
<0>/140	035		DCR	E	Decrement data count loaded at 0/103;
<0>/141	302 123 <0>		JNZ	GETDATA	If not done then repeat for next bit;
<0>/144	162		MOV	M,D	Save received data in memory;
<0>/145	043		INX	H	Point to next available location;
<0>/146	174		MOV	A,H	Move high order address to A for end check;
✓<0>/147	376 yyy		CPI	yyy	Has high order address reached end?
<0>/151	302 103 <0>		JNZ	STARTBYT	If not then reiterate for next byte;
<0>/154	166		HLT		End input;

Notes:

- Input is assumed to be wired to bit 0 of port 1, from output of IC38 pin 6 via resistor R38 and shunted by diode DG1.
- Loading proceeds from split octal address xxx/xxx to address yyy/000. Enter this program by jumping to location <0>/100 after setting up constants of address.
- "*" indicates a timing constant for the "software UART" inputs.
- "✓" indicates the end of transfer comparison mentioned in text.
- <0> indicates an arbitrary page location for this program, to be replaced by a real memory page number when actually loading the program at byte 100 of some page.

Listing 2: Stand Alone Suding Cassette Output Program. This program is a self contained data transfer routine which will transfer a block of data from split octal memory locations xxx/xxx through yyy/000 onto cassette tape after a five second leader output delay. This program assumes that CASTOMEM (see listing 1) will be used to read the tape being created. A more generally useful output facility would be modelled on this program and linked to a system monitor as a subroutine.

Split Octal Address	Octal Code	Label	Op.	Operand	Commentary
<0>/200	041 xxx xxx	MEMTOCAS	LXI	H,xxx/xxx	Load starting address in HL pair;
<0>/203	076 001		MVI	A,1	Start port output in high state;
<0>/205	323 001		OUT	1	Send initial state out;
<0>/207	026 012		MVI	D,012	Outer leader delay count;
<0>/211	006 377	LEADER5S	MVI	B,377	Outer leader delay loop return;
<0>/213	016 377	LEADER5X	MVI	C,377	Middle leader delay loop return;
<0>/215	015	LEADER5Y	DCR	C	Inner leader delay loop return;
<0>/216	302 215 <0>		JNZ	LEADER5Y	If inner loop not done then reiterate;
<0>/221	005		DCR	B	Middle leader delay count;
<0>/222	302 213 <0>		JNZ	LEADER5X	If middle loop not done then reiterate;
<0>/225	025		DCR	D	Outer leader delay count;
<0>/226	302 211 <0>		JNZ	LEADER5S	If outer loop not done then reiterate;
		*			
		* Upon reaching this point, 5 seconds of mark (high) state have			
		* been output to the cassette interface.			
<0>/231	016 011	BYTEOUT	MVI	C,011	Define output bit count (decimal 9);
<0>/233	257		XRA	A	Clear carry (start bit level is 0);
<0>/234	176		MOV	A,M	Move current byte to A;
<0>/235	027		RAL		Rotate bit into position (carry=0 first);
<0>/236	323 001	WNEXBIT	OUT	1	Send current LSB to output port;
*<0>/240	006 200		MVI	B,200	Time delay between bits;
<0>/242	005	WOUTLOOP	DCR	B	Decrement delay count;
<0>/243	302 242 <0>		JNZ	WOUTLOOP	If time left then reiterate;
<0>/246	037		RAR		Rotate new bit into position;
<0>/247	015		DCR	C	Decrement output bit count;
<0>/250	302 236 <0>		JNZ	WNEXBIT	If data left then reiterate;
<0>/253	076 001		MVI	A,001	Stop bit state defined
<0>/255	323 001		OUT	1	then sent out to port;
*<0>/257	006 377		MVI	B,377	Stop bit value set;
<0>/261	005	WIBDELAY	DCR	B	Decrement stop bit counter;
<0>/262	302 261 <0>		JNZ	WIBDELAY	If time left then reiterate;
<0>/265	043		INX	H	Increment memory address;
<0>/266	174		MOV	A,H	Move high order address to A for end check;
✓<0>/267	376 yyy		CPI	yyy	Has high order address reached end?
<0>/271	302 231 <0>		JNZ	BYTEOUT	If not then continue output process;
<0>/274	166		HLT		End output;

Note:

- Output is assumed to be wired from bit 0 of port 1 to DS1 in figure 2.
- See notes to listing 1 for listing conventions.

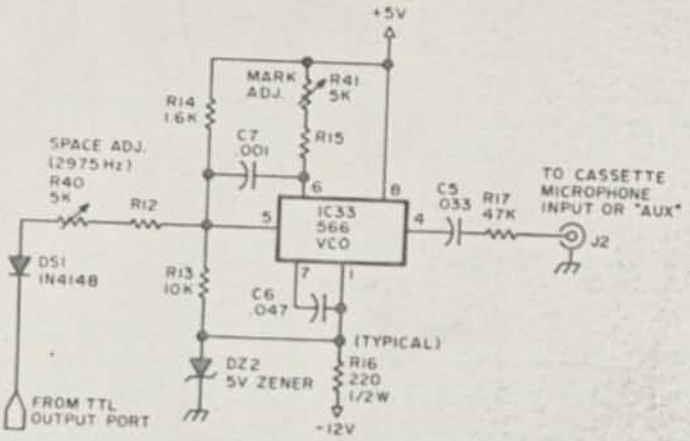


Figure 2: The schematic of the Suding cassette output interface as found in the Digital Group systems. The output interface is a simple audio frequency shift keyer made up of a 566 voltage controlled oscillator with two frequency states controlled by a single TTL data line. The TTL level which drives the output modulator is a single bit derived from an output port. The software (see listing 2) to drive this output interface is shown as a programmed simulation of a UART output algorithm; an actual UART or ACIA device could be substituted if desired.

negative is produced until approximately midway (2550 Hz) a summed voltage of 0 results.

A three pole lowpass active filter then removes the remaining traces of pulsating DC from the summed signal with almost no effect on the data pulses up to a speed of 1000 bits per second. If lower data rates were to be utilized, an improved signal to noise ratio could be obtained by multiplying the values of C12, C13, and C11 by the reciprocal of the data rate ratio. Table 1 shows some component values for alternative frequency designs.

The final receiver section is a 741 operational amplifier, IC38, connected as a slicer. This operational amplifier detects whether the voltage at its pin 2 is positive or negative with respect to the constant voltage at its pin 3. The output voltage will then swing either to nearly −12 V or to nearly +5 V. Notice that this operational amplifier has +5 as its positive supply voltage, pin 7. A forward biased germanium diode prevents the actual output voltage from going less

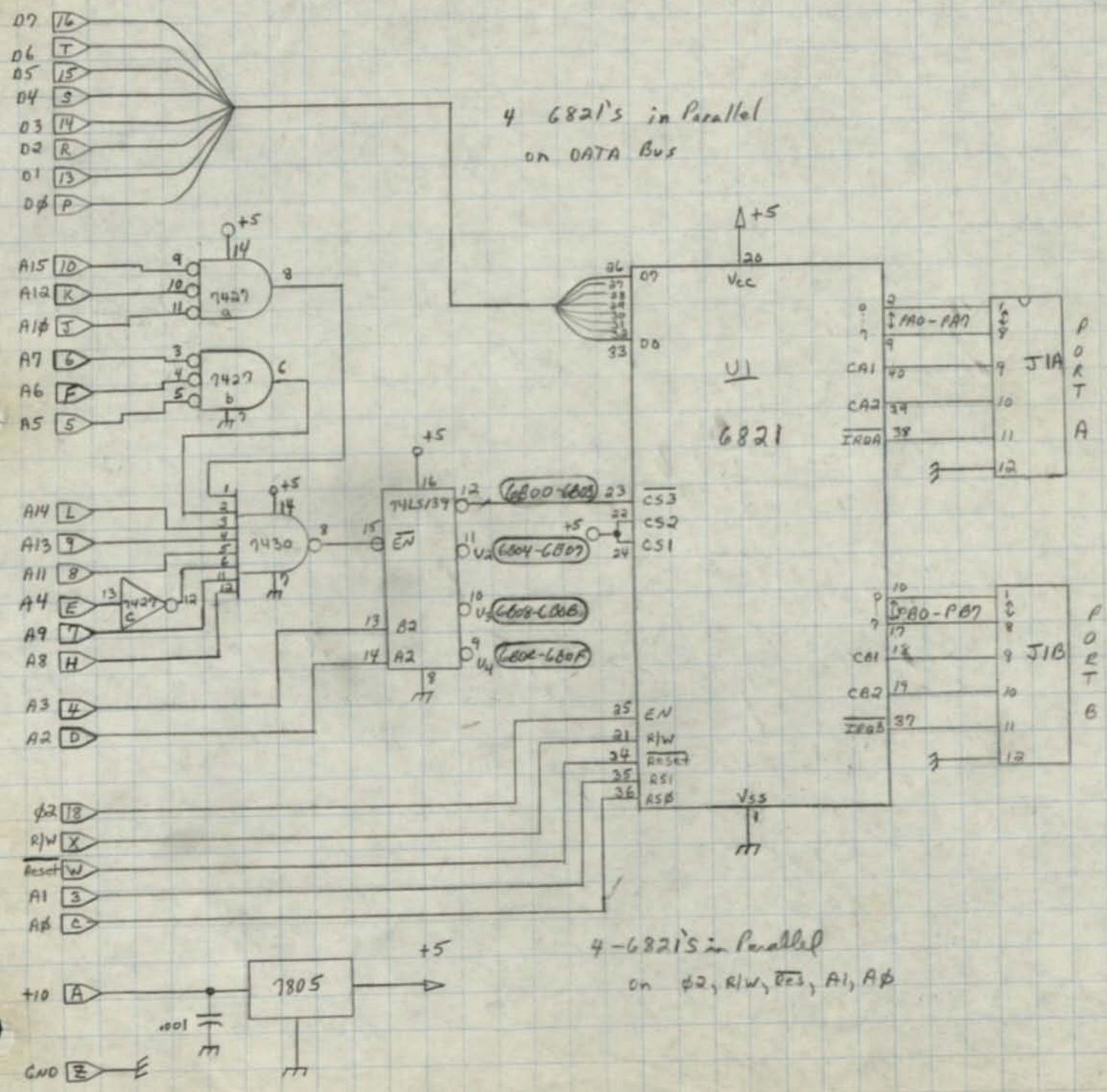
Tune Up Notes

The cassette interface must be carefully tuned to achieve proper performance. Careless tuning has been the most frequent cause of cassette system failure.

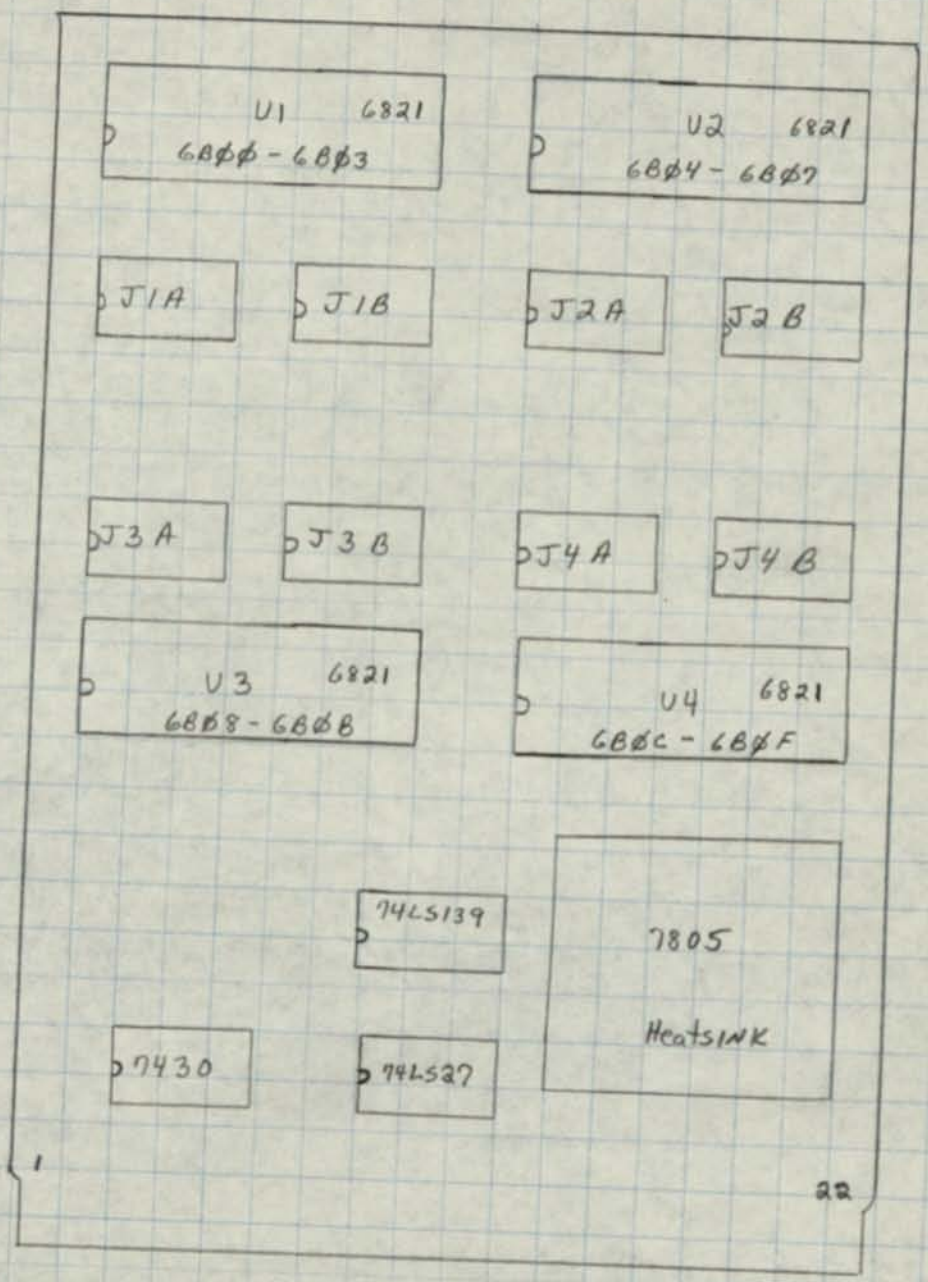
1. Plug in the six integrated circuits of the cassette interface.
2. Connect a calibrated audio oscillator between the limiter input and ground. A digital frequency counter driven by the audio oscillator is highly recommended. The oscillator should cover the desired range of 2 – 3 kHz, with a sine wave output of .5 or so, although the precise level is not at all critical.
3. Apply +5 and ±12 voltages to the circuit. Measure the output at pin 6 of the 741 limiter (IC34) with an oscilloscope. The wave shape should be a rounded square wave of about .6 V peak to peak.
4. Set the audio oscillator to 2125 Hz. Measure the output at pin 1 of the 5558 active bandpass filter. Slowly turn R25 until the signal peaks. Be sure that you are peaking at 2125 Hz, not a harmonic. Vary the oscillator frequency a few decades to insure 2125 Hz is the tuned frequency.
5. Similarly, set the oscillator to 2975 Hz and measure the output at pin 7 of the 5558 (IC35). Slowly turn R26 until the signal peaks. Vary the oscillator to insure a 2975 Hz peak.
6. Measure the detected voltages at pin 5 of IC37. When the oscillator approaches 2125, the voltage should go negative. When approaching 2975, the voltage should go positive. Trouble in this area would most likely be caused by reversed or defective diodes, or shorts between adjacent lines.
7. Measure the voltage at the cathode (bar) end of the output clamping germanium diode (G1). Sweeping the frequency between 2125 and 2975 Hz should result in a clean voltage jump somewhere between 2125 and 2975 Hz. Measure the output swing to insure that it does not exceed +5, −.3 V.
8. Remove the audio oscillator and short input connector J1 temporarily to ground. Measure the output at pin 6 of IC34. A stable condition (no oscillation) should be seen. Connect the oscilloscope to the cathode of G1 again. Adjust the balance potentiometer (R42) so that the output voltage is a negative level. Slowly turn the potentiometer until the output voltage jumps to a positive level and leave the setting at this point.
9. Disconnect the temporary jumper from the input connector and reconnect the audio oscillator. Perform step 7 again. The crossover threshold should be close to 2550 now. If all proceeds well at this point, the cassette interface is ready to receive data.
10. Connect the oscilloscope to pin 4 of the 566 voltage controlled oscillator (IC33). A triangular wave output should be seen.
11. Connect a temporary jumper between the TTL input going to DS1 and +5 V. Connect a frequency counter to pin 3 of the VCO (IC33). Adjust potentiometer R41 for a resultant output frequency of 2125 Hz.
12. Remove the jumper from +5 V and connect the jumper from DS1's input to ground. This time adjust R40 for 2975 Hz output.
13. Remove the jumpers, and you are ready for final tune in the driving circuit. Connect the cassette interface to the driving output port, and program the driving processor to send a TTL high level ("1") output to the cassette interface. Adjust R41 to 2125 Hz. Then have the processor send a "0" level. This time adjust R40 for 2975 Hz output. The cassette interface is now ready for use.

I/O Bd.

I/O BOARD


D7 16
D6 T
D5 15
D4 S
D3 14
D2 R
D1 13
D0 P
4 6821's in Parallel
on DATA Bus
+5
A15 10
A12 K
A10 J
7427 a
A7 6
A6 F
A5 5
7427 b
7427 c
A14 L
A13 9
A11 8
7430
A4 E
A9 T
A8 H
A3 4
A2 D
74LS139
EN
A2
A1
A0
6800-6803
6804-6807
6808-680B
680C-680F
U1
6821
D7
D0
Vcc
Vss
CS3
CS2
CS1
EN
R/W
RESET
RS1
RS0
PA0-PA7
CA1
CA2
IRQA
JIA
PORT A
PB0-PB7
CB1
CB2
IRQB
JIB
PORT B
Φ2 18
R/W X
Reset W
A1 3
A0 C
4-6821's in Parallel
on Φ2, R/W, RES, A1, A0
+10 A
.001
7805
+5
GND E

I/O Board


U1 6821
6800 - 6803
U2 6821
6804 - 6807
J1A
J1B
J2A
J2B
J3A
J3B
J4A
J4B
U3 6821
6808 - 680B
U4 6821
680C - 680F
74LS139
7805
Heatsink
7430
74LS27
1
22

Board Address Range ⇒ 6B00 - 6B0F

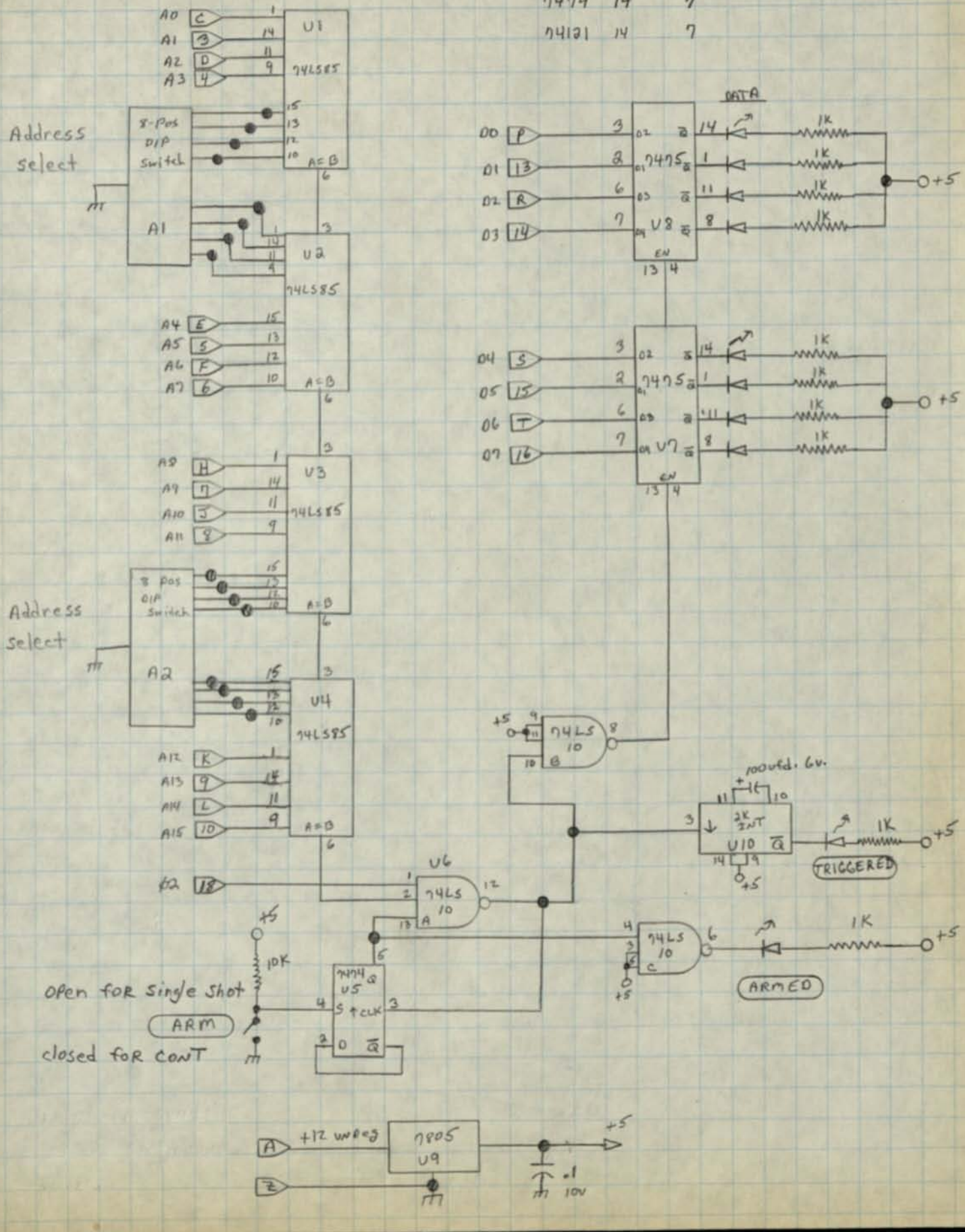
I/O PORT	1A	6B00 - 6B01
	1B	6B02 - 6B03
I/O PORT	2A	6B04 - 6B05
	2B	6B06 - 6B07
I/O PORT	3A	6B08 - 6B09
	3B	6B0A - 6B0B
I/O PORT	4A	6B0C - 6B0D
	4B	6B0E - 6B0F

I/O Connector Pin #	Function
1 - 8	PA0-PA7 or PB0-PB7
9	CA1 or CB1
10	CA2 or CB2
11	$\overline{IRQA}$ or $\overline{IRQB}$
12	GND or GND

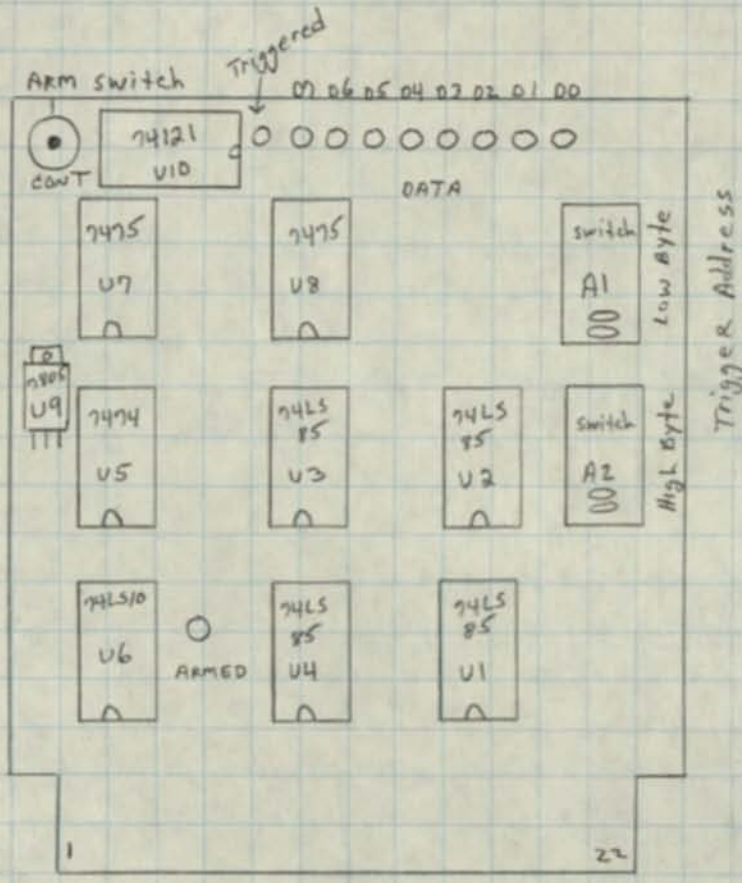
Logic Analyzer

	Vcc	Gnd
74LS85	16	8
7475	5	12
74LS10	14	7
7474	14	7
74121	14	7

● = 10K +5

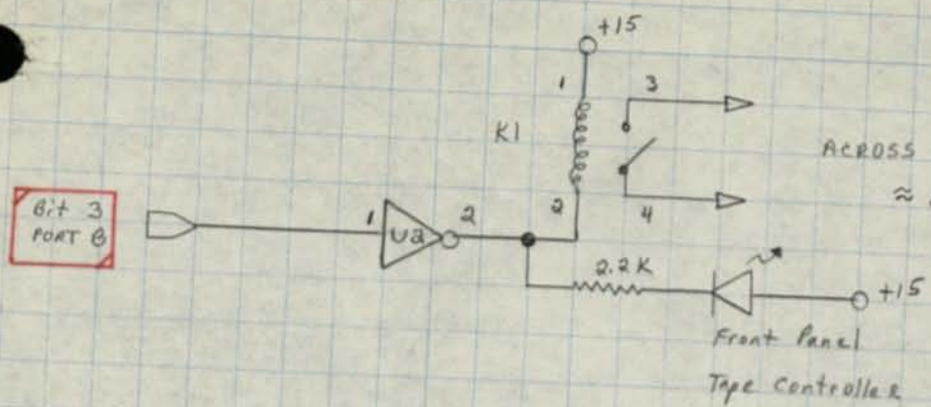


Logic Analyzer



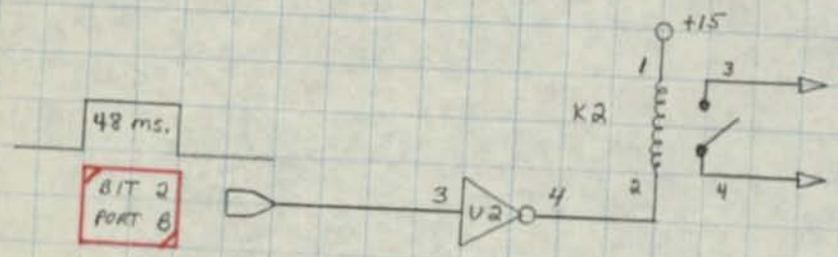
Ref #	IC	Vcc	Gnd
1,2,3,4	74LS85	16	8
5	7474	14	7
6	74LS10	14	7
7,8	7475	5	12
9	7805	—	—
10	74121	14	7

F. FWD



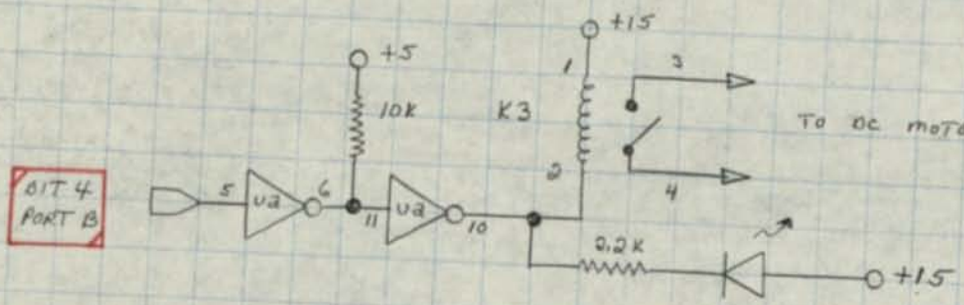
ACROSS F. FWD SWITCH ON Front Panel
≈ 270 ma avg.

TRK CHANGE



ACROSS TRK change switch That MONITORS Tape
≈ 1.2 A

MOTOR CONTROL

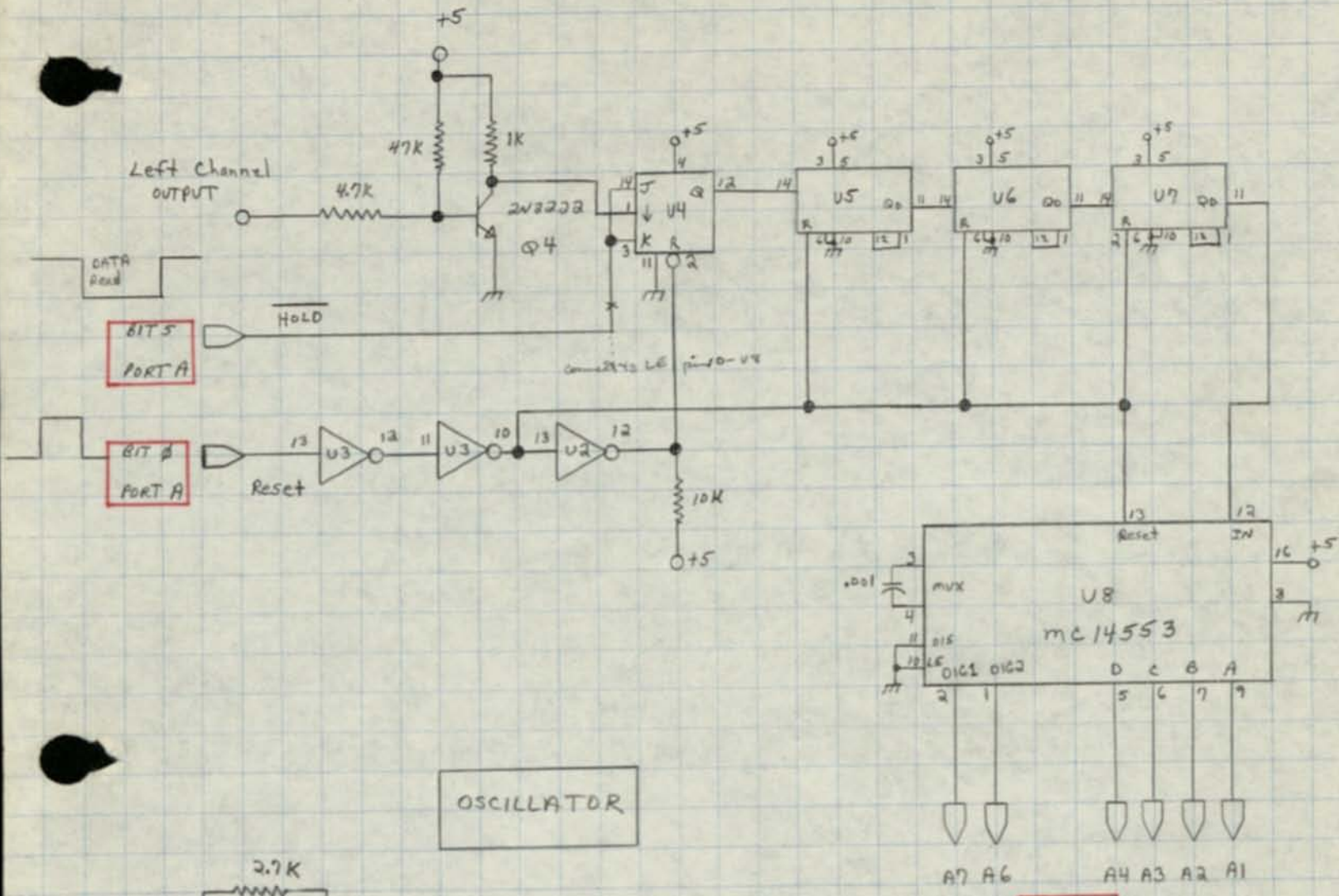


To DC MOTOR "+" Lead

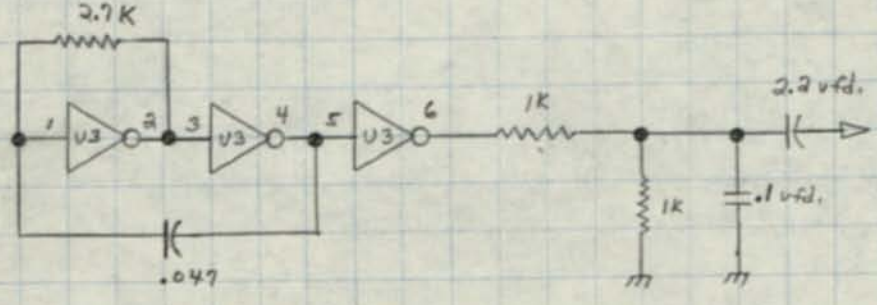
ALL Relays

Electrol Relay
R1554-3
coil 1-2
switch 3-4
≈ 5 ma

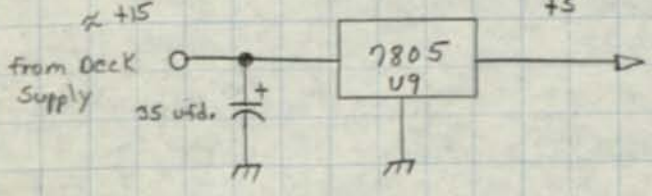
TAPE POSITION counter



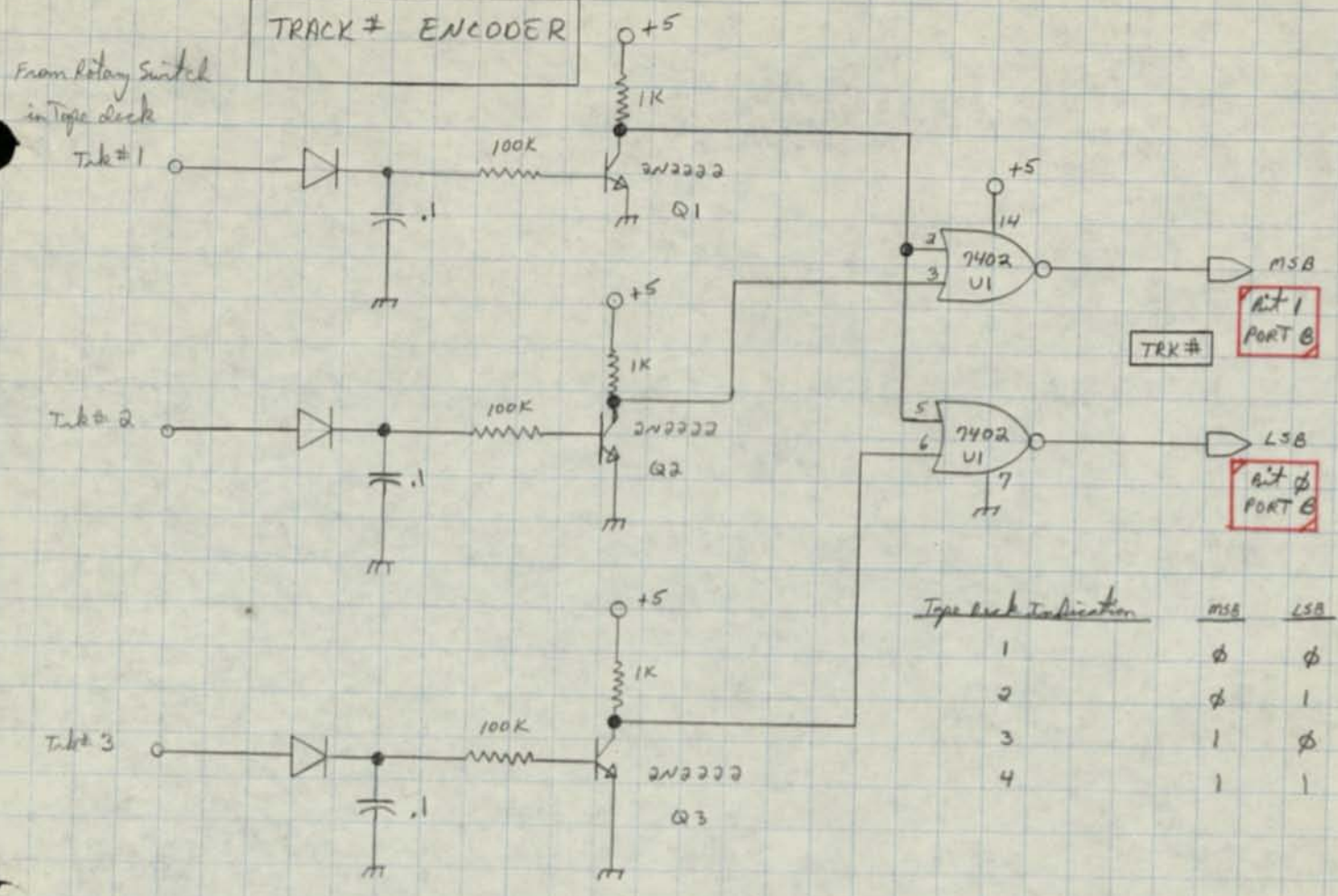
OSCILLATOR



Regulated Supply



TRACK # ENCODER



Tape Deck Indication	MSB	LSB
1	Ø	Ø
2	Ø	1
3	1	Ø
4	1	1

I/O PORT CONFIGURATION

	A7	A6	A5	A4	A3	A2	A1	AØ
	DIG1	DIG2	HOLD ↓	BCD 8	BCD 4	BCD 2	BCD 1	↑ Reset
21_{16}	Ø	Ø	1	Ø	Ø	Ø	Ø	1

	B7	B6	B5	B4	B3	B2	B1	BØ
				MOTOR	F. FWD	TRK CHNG	TRK # MSB	TRK # LSB
$1C_{16}$				1	1	1	Ø	Ø

PORT A 6BØØ CRA-2 = 1
CRA = 6BØ1
DDRA 6BØØ CRA 2 = Ø

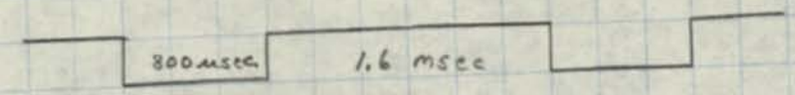
PORT B 6BØ2 CRB-2 = 1
CRB = 6BØ3
DDRB 6BØ2 CRB-2 = Ø

PORT A INITIALIZED W/ 2Ø H (HOLD DISABLED, Reset DISABLED)
PORT B INITIALIZED W/ 1Ø H (MOTOR OFF, FFWD OFF, TRK CHNG OFF)

BIT 7 PORT A

DIG 1

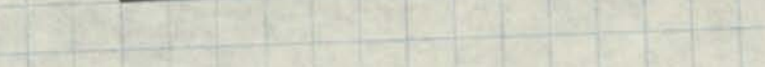
(U8-2)

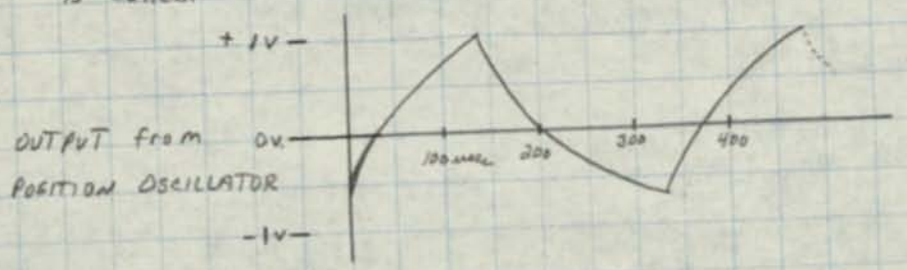


BIT 2 PORT B

(U2-3) TRK CHNG

when subroutine is called.





Ref #	Type	
U1	7402	QUAD 2-INPUT NOR
U2	7416	Hex INVERTOR Open collector
U3	74LS04	Hex INVERTOR
U4	7473	Dual JK Flip Flop
U5,6,7	7490	Decade Counter
U8	mc14553	3 Digit Decade Counter (cmos) RS# 276-2498
U9	7805	+5 volt Regulator
Q1,2,3,4	2N2222	Gen Purpose NPN
K1,2,3	x12V. 5ma coil current	Electrol # R1554-3 coil 1-2 swivel 3-4

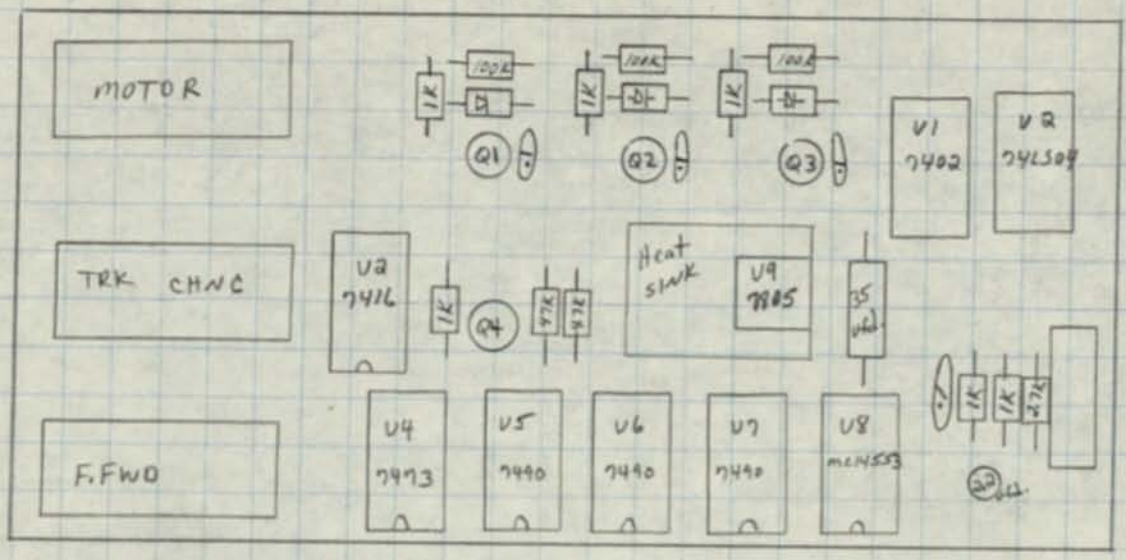
Tape DATA

Speed- Play 3.75 IPS
- F.F. ≈ 11 IPS

TRACK Length - 45 min 2531 in. - 211 ft.
- 30 min 1688 in - 141 ft.

Track count - 45 min ≈ 950 avg.
- 30 min

1 count = 2.63 inches of Tape



yell	A0	Green	B0	
OR	A1	yell	B1	
Red	A2	Or	B2	
Brwn	A3	Red	B3	
Blk	A4	Brown	B4	
white	A5	Blk	B5	not used
Grey	A6	white	B6	not used
Pur	A7			
Blue	GND			

yell	+15
Orange	GND

8-Track Recorder/Player Deck

TR-882

OWNER'S MANUAL

PLEASE READ BEFORE USING THIS EQUIPMENT

REALISTIC®

Cat. No. 14-944

CUSTOM MANUFACTURED FOR RADIO SHACK A TANDY CORPORATION COMPANY

REALISTIC®

THE BRAND WITH OVER 1,000,000 CUSTOMERS

Your REALISTIC TR-882 is a component-styled Stereo Tape Recorder/Player for 8-track cartridges. It operates from 120 Volt, AC power (220/240 volts, 50 Hz AC power where the sets are so marked on the rear for European and Australian models).

SPECIFICATIONS

POWER REQUIREMENTS	: 120 volts, 60 Hz, AC 35 watts (220/240 volts, 50 Hz, 35 watts)
RECORDING SYSTEM	: AC Bias, 50 kHz
ERASE SYSTEM	: AC Erase
TAPE SYSTEM	: 8-track, 2-channel stereo
TAPE SPEED	: 3-3/4 ips.
FREQUENCY RESPONSE	: 50–10,000 Hz
INPUTS	
MIC	: 0.25 mV input sensitivity (–70 dB)
AUX IN	: 0.080 volt input sensitivity (–20 dB)
OUTPUT	: PREAMP OUTPUT, adjustable from 0.05 to 0.75 volts output
DIMENSIONS	: 3-7/8" × 13-1/4" × 8-3/5"
WEIGHT	: 8.3 lbs.

GUARANTEE: The Realistic guarantee is stated on the Guarantee Card packed with the equipment. It is in effect from coast to coast. At any time, Realistic equipment may be restored to new condition with original parts with MINIMUM delay anywhere in the U.S.A., usually in your own neighborhood. In 98% of the cases; it is NOT necessary to return Realistic equipment to our Laboratories.

FEATURES

- Push-button PAUSE control for cuing and editing.
- AUTO-STOP button allows automatic stop after last program.
- When AUTO-STOP is not in use, program automatically changes after last program to go back and repeat tape over and over as long as cartridge is in place.
- PROGRAM select button permits you to advance to the desired program.
- FAST-Forward button advances the tape rapidly for fast selection of programs.
- Dual meters for precise stereo recording levels.
- Dual level controls for recording levels.
- Dual Auxiliary input jacks for stereo recordings from external sources.
- Rear panel Output Level Control for setting suitable output level from deck (to match input level requirements of your amplifier or receiver.)

INSTALLATION AND CONNECTION

Your TR-882 can be installed in any convenient position for operation with your stereo system. It must be connected to an amplifier or receiver for operation; it does not include a power amplifier, thus must use the power amplifier of your existing stereo system.

CONNECTING TO YOUR AMPLIFIER/RECEIVER

For Playing back tapes:

Connect a pair of cables between the LINE OUTPUT jacks of the TR-882 to the auxiliary input (Aux In or Aux Input) jacks of your Amplifier/Receiver. Connect Right jacks (labeled R) together and Left jacks (labeled L) together. The output level from these LINE OUTPUT jacks can be adjusted using the "Output Level Control" mounted next to the LINE OUTPUT jacks on the rear of the unit.

For Recording:

Connect a pair of cables between LINE INPUT jacks on the back of the TR-882 to the Tape Output jacks on your Amplifier/Receiver. Connect Right to Right and Left to Left. This will permit you to record signals being played through your Amplifier/Receiver.

To record directly from microphones, plug microphones into L and R MIC jacks on the front of your TR-882. Use high-quality microphones with an output rating of −50 to −70 dB.

For Recording from Other Sources:

You can record from other signal sources when proper connections are made.

Recording from an FM Tuner:

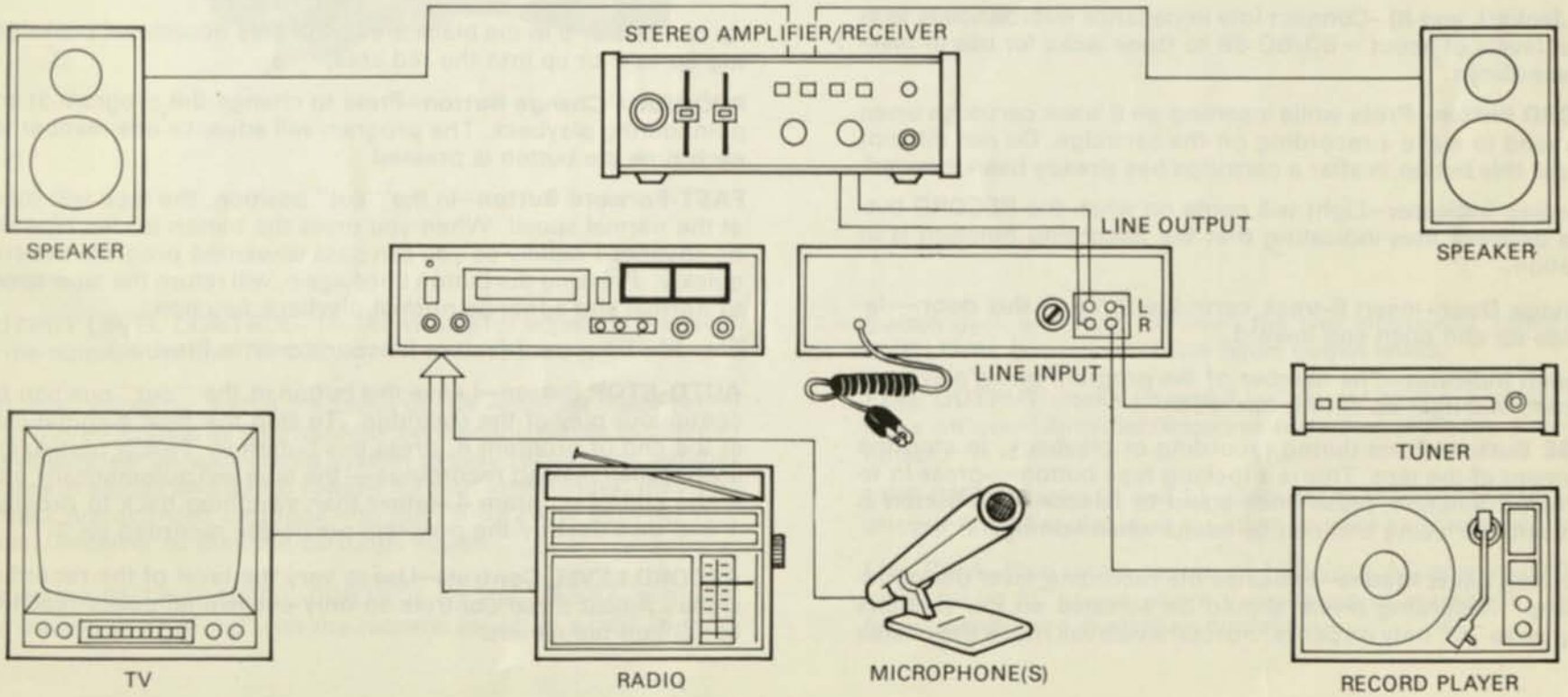
Connect the Output jacks on the Tuner to the LINE INPUT jacks on the back of the TR-882.

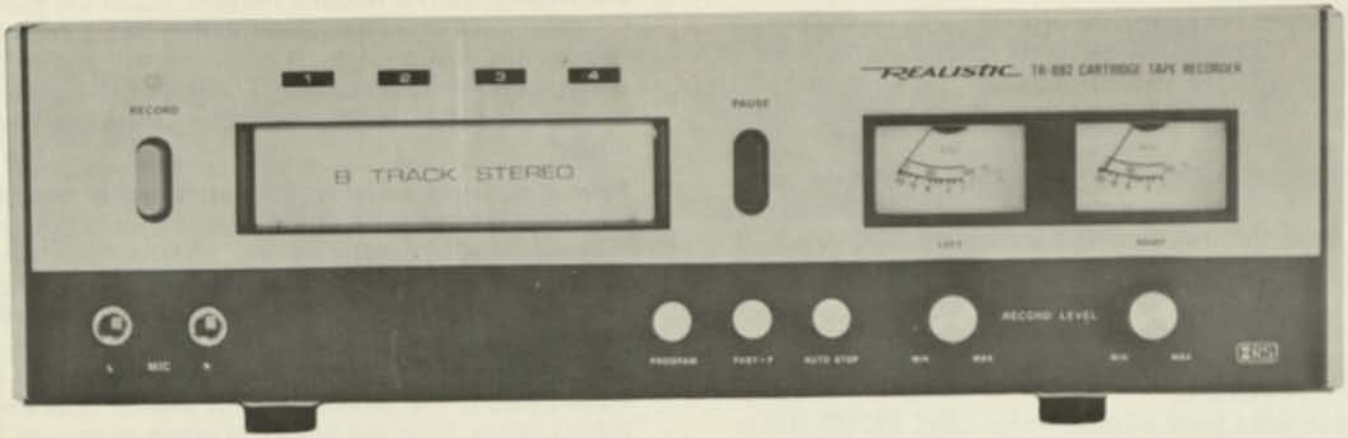
Recording from a Record Player:

If you have a record player which has a ceramic cartridge, you can record directly from it. Connect the output cable from the record player to the LINE INPUT jacks on the back of the TR-882. If the record player uses a magnetic cartridge, you can not record directly.

Recording from a Radio, TV Set or Other Source:

For other types of signal sources, connect cables from jacks labeled "Ear", "Earphone" or "External Speaker" to the MIC input jacks on the front of the TR-882. If the jacks on the signal sources are labeled "Aux", "Auxiliary", "Output" or "High Level Output", connect cables from them to the LINE INPUT jacks on the rear of the TR-882. A signal source should provide approximately 100 mV of peak signal for proper operation with the LINE INPUT jacks. Plug the line cord into a source of 120 Volts, 60 Hz AC Power (220/240 volts 50 Hz AC power where the sets are so marked on the rear for European and Australian models).





MIC Jacks (L and R)—Connect low impedance microphones with output levels of about −50/60 dB to these jacks for use in making recordings.

RECORD Button—Press while inserting an 8-track cartridge when you intend to make a recording on the cartridge. Do not attempt to press this button in after a cartridge has already been inserted.

Recording Indicator—Light will come on when the RECORD button is pressed, thus indicating that the Recording function is in operation.

Cartridge Door—Insert 8-track cartridge through this door—label side up and open end inward.

Program Indicator—The number of the program being played or recorded will light up during operation.

PAUSE Button—Press during recording or playback, to stop the movement of the tape. This is a locking type button—press in to set PAUSE function, press once again to release. This button is very useful for cuing and can be useful when editing.

Recording Level Meters—Indicates the recording level during recording. Recording levels should be adjusted so the pointers swing up to "0" only on peaks; normal levels will move the needle up to 10, 6 or 3 in the black area (with only occasional peaks going up to 0 or up into the red area).

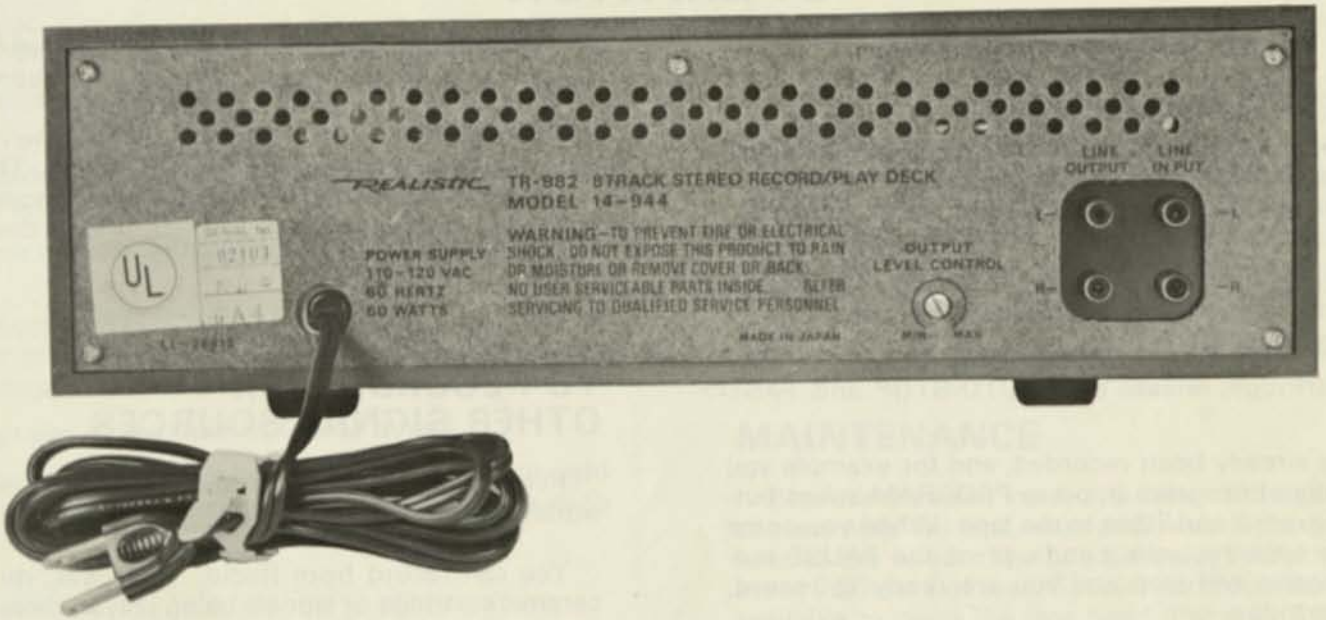
PROGRAM Change Button—Press to change the program at any point during playback. The program will advance one number for each time the button is pressed.

FAST-Forward Button—In the "out" position, the tape will move at the normal speed. When you press the button in, the tape will be advanced rapidly so you can pass unwanted program material quickly. Pressing the button once again, will return the tape speed to normal and continue normal playback function.

This FAST-Forward feature functions only in Playback.

AUTO-STOP Button—Leave this button in the "out" position for continuous play of the cartridge. To stop the tape automatically at the end of program 4, press this button in. This is particularly useful when making recordings—the tape will automatically stop at the end of program 4, rather than switching back to program 1 and thus destroy the program previously recorded on 1.

RECORD LEVEL Controls—Use to vary the level of the recording signal. Adjust these controls so only occasional peaks reach up to "0" on the meters.



OUTPUT LEVEL CONTROL—This control is for adjusting the level of the output from the TR-882.

Set this control to match the input of the Amplifier/Receiver in your Stereo System as follows: After connecting cables as outlined previously, set up your stereo system to play records (or another source of signal) and adjust volume for normal listening; insert an 8-track prerecorded cartridge into the TR-882 and set your Amplifier/Receiver to play the cartridge sound.

Adjust the OUTPUT LEVEL CONTROL on the TR-882 to match the volume as obtained with the records (or other signal source). Switch back and forth between the two inputs and adjust OUTPUT LEVEL control to obtain equal output levels.

LINE OUTPUT Jacks (R and L)—Connect to the auxiliary input jacks on your Amplifier/Receiver (or other jacks as previously noted).

LINE INPUT Jacks (R and L)—Connect to the Tape Output Jacks on your Amplifier/Receiver (or other sources as previously noted).

Line Cord—Plug into a source of 120 volts AC power (220/240 volts, 50 Hz AC power where the sets are so marked on the rear for European and Australian models).

OPERATION

TO RECORD WITH MICROPHONES

1. Make all connections as previously instructed.
2. Select the point on the tape at which the recording is to begin, if it is not already in the correct position. Insert the cartridge into the cartridge door and press PROGRAM select button until program 4 is indicated. Press in AUTO-STOP button.

   Press in FAST-Forward. When the tape reaches the end of program 4 it will stop automatically and you will be ready to start at the beginning of program 1.

   Withdraw the cartridge, release both AUTO-STOP and FAST-Forward.
3. If program 1 has already been recorded, and for example you are into the middle of program 3, press PROGRAM select button to obtain program 3 and listen to the tape. When you come to the point where the recording ends, press the PAUSE button; the tape motion will stop and you are ready to record. Withdraw the cartridge.
4. With PAUSE button still pressed in, press and hold in RECORD button while inserting the cartridge into the cartridge door opening. The Record light will come on, indicating that the Record function is ready.

CAUTION: Do not attempt to press the RECORD button when a cartridge is already seated in place (the switch mechanism can be damaged).

5. Adjust RECORD LEVEL controls as required to keep Meter readings within the black scale area, with only the highest peaks moving the pointer up to the "0" or touching up into the red area. Excessive recording levels (meter readings constantly going up to "0" and into the red area) will result in distortion.

NOTE: To keep the tape from moving, while setting levels and preparing for actual recording, keep PAUSE button " in ". This will keep the tape stopped, but permit you to set recording levels. When you are ready for recording, press the PAUSE button to release the Pause function.

6. The program or track number will light up showing you what track you are on in your recording function.
7. To automatically stop tape movement when you reach the end of track 4, press in AUTO-STOP button. Thus, when the tape has been completely recorded, it will automatically stop (rather than switching back to track 1 and thus destroy material previously recorded on track 1).

TO RECORD FROM OTHER SIGNAL SOURCES

Recording operation is exactly the same when using any other signal source.

You can record from Radio, TV, Tuner, record changer with ceramic cartridge or signals being played through your Amplifier/Receiver by making the proper connections as noted previously.

NOTES

1. To stop a recording, press the PAUSE button. PAUSE is useful for setting the tape at a particular position and then cuing up for the start of a new recording.
   Thus, you can play a tape through to the desired position, press PAUSE, pull out the cartridge, press in RECORD while inserting the cartridge once again and be ready to start with your recording at that exact point on the tape. To start the tape moving, press PAUSE.
2. The FAST-Forward function does not operate in the Record mode.
3. Store cartridges (both blank as well as recorded) in a place free from excessive temperatures and humidity and not in direct sunlight. Do not place recorded cartridges near magnetic fields (radio, TV, transformers, etc.).

TO PLAY BACK TAPES

1. Make all connections as previously instructed. Turn on your stereo system.
2. Insert a pre-recorded 8-track stereo cartridge into the cartridge door (label side up and open end in).
3. Adjust volume on your Amplifier/Receiver for desired level of sound.
4. If necessary, adjust OUTPUT LEVEL CONTROL on the rear of the TR-882 for proper matching of the input jacks on your Amplifier/Receiver.
5. To change programs, press the PROGRAM button.
6. To move the tape forward rapidly, press the FAST-Forward button; to return to normal playing speed, release by pressing the button again.

NOTES

1. To stop playing instantly, press PAUSE button.
2. If you want the tape to play through just once (programs 1 through 4) and then stop, press in AUTO-STOP. With AUTO-STOP in, the tape will stop playing when it comes to the end of program 4.
3. The Level Meters do not function during playback.
4. NEVER LEAVE A CARTRIDGE INSERTED ALL THE WAY IN WHEN YOU ARE NOT USING THE TR-882. REMOVE THE CARTRIDGE AT LEAST HALF-WAY OUT (OR REMOVE ENTIRELY)
5. If you press the RECORD button while you are inserting a pre-recorded cartridge, any previously recorded material will be erased. Thus, be careful that you do not press the RECORD button by accident.

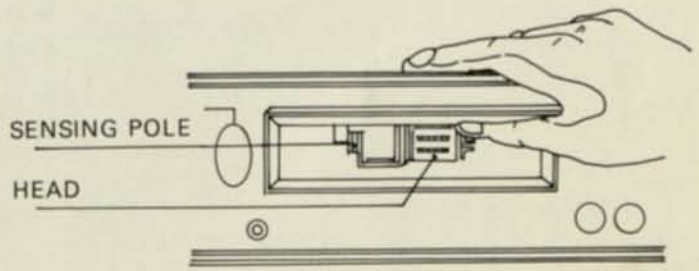
ERASING

When you make a recording, any previous recording made on the tape is automatically erased before the new recording is placed on the tape. Thus, only the new recording remains. To erase recordings, without making a new recording, set RECORD LEVEL controls maximum counterclockwise (MIN position) and disconnect cables to MIC and LINE INPUT jacks. Operate the TR-882 in a normal manner for recording; this will erase all previous recordings and leave you with a blank tape for brand new recordings.

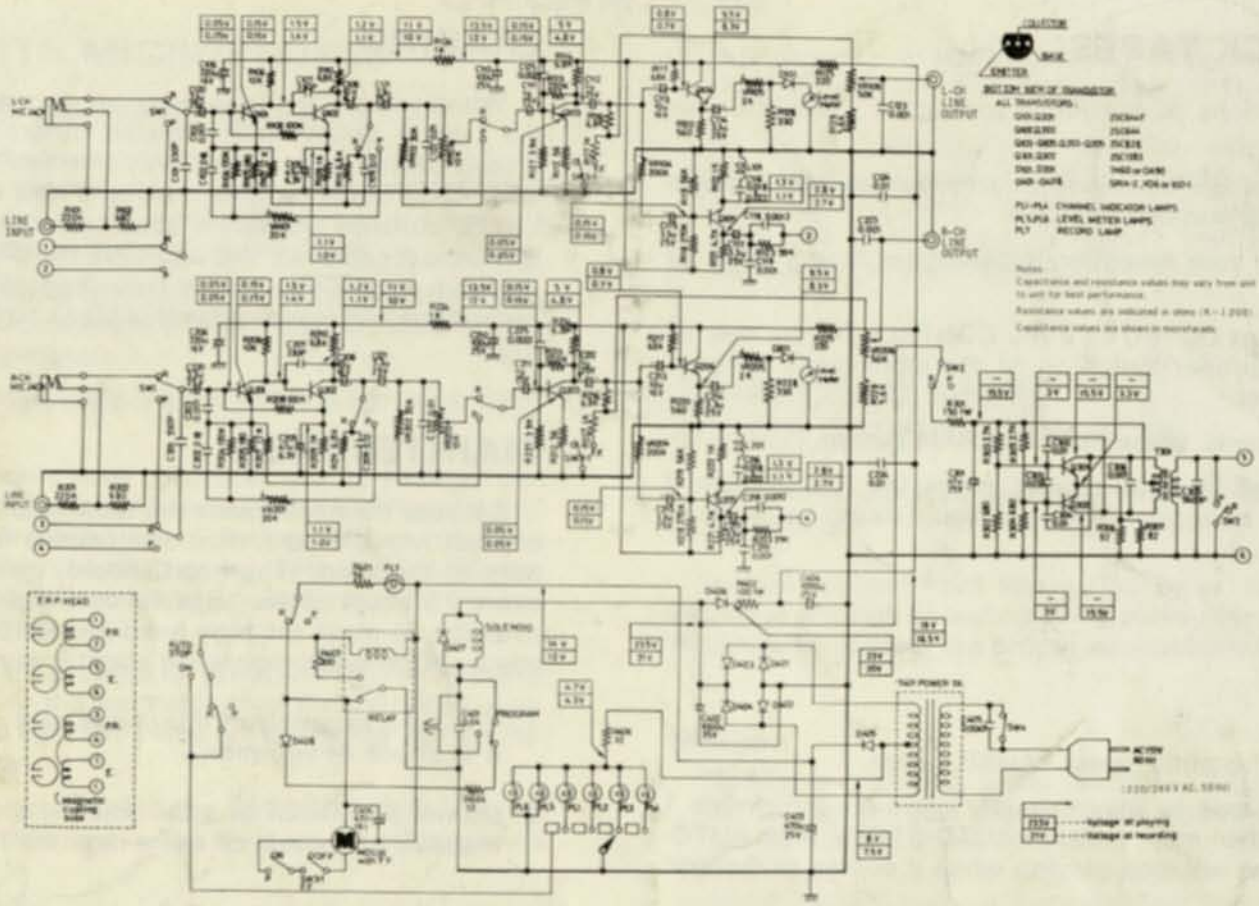
MAINTENANCE

Because the head inside the tape cartridge door is in constant contact with the tape, dust and residue from the tape easily adhere to the head. The head should, therefore, be cleaned after every 25 hours of use. Special cartridge-tape head cleaners are available to clean the tape head (Realistic Cat. No. 44-1161). Or use a cotton swab moistened slightly with alcohol.

1. The head assembly of this unit is very delicate. Do not subject it to shock or vibration.
2. Do not allow iron or steel objects, such as s screw-driver or magnet, to contact or come near the head.



SCHEMATIC DIAGRAM



RADIO SHACK A TANDY CORPORATION COMPANY

FORT WORTH, TEXAS 76107

TANDY ELECTRONICS

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