OPERATIONS COMMITTEE MEETING

January 27, 1969

AGENDA

1. Additions and Corrections to Minutes of the January 20th Meeting
2. Marketing Review Committee Summary - (Ted Johnson)
   (See attached minutes of the January 21st meeting)
3. Function of the Marketing Review Committee - (Ted Johnson)
4. Discussion of Trade Shows - Number, Etc. - (Ted Johnson)
5. SJCC Trade Show Booth - (Bob McInnes)
6. Review of the KV Graphic System - (Bob Collings)
   (See attached report)
7. Proposed Corporate Press Conference - (Mark Nigberg)
   (See attached report)
8. Financial and Consultant Relations Proposal - (Mark Nigberg)
   (See attached report)
9. PDP-11 Announcement - (Nick Mazzarese)
10. Discussion of the Disposal of Company Reports - (Stan Olsen)
11. Procedure for Setting Date for Taking Orders of New Products and Peripherals

COMPANY CONFIDENTIAL

MINUTES OF THE OPERATIONS COMMITTEE

January 27, 1969

Present: Ken Olsen, Stan Olsen, Nick Mazzarese, Ted Johnson, Win Hindle
Pete Kaufmann, Secretary

1. The minutes of the January 20th meeting were approved.

2. PDP-11 Announcement

Immediate leaks were proposed by Nick Mazzarese. John Cohen's kit will go to all Regional and District Sales Managers. No price and no delivery dates will be quoted. Internally, we will plan to make a production lot of 50 pieces, not for sale, to work out engineering problems. The risk is that all these pieces may be scrapped. This strategy was approved.

Nick and Ted will investigate the hiring of a consultant to evaluate the PDP-11 and the PDP-15.

3. Marketing Review Committee

Gabe D'Annunzio will be encouraged by Ken Olsen to make a proposal to take over the management of Trade Shows.

4. Function of the Marketing Review Committee

Ted suggested that the function of the Marketing Committee should be as follows:

1. Review marketing plans similar to a design review.

2. Offer constructive criticism and help to the Marketing and Product Line people for making marketing plans.

3. Offer horizontal communication path.

4. Set guidelines and standards for company marketing plans.

Ted feels that the Marketing and the Product Line Managers have the responsibility and that the Marketing Review Committee has no authority to stop a marketing plan but can act only as a review to the plan. Ken expressed concern that we put more stress on written paper in marketing and engineering than on results and on fits of inspiration.

John Jones' opinion of the Marketing Committee was submitted to the Operations Committee as follows:

It takes as much effort to review a marketing plan as it does to do one. The present Marketing Committee, as constructed, cannot perform this function. John suggested that a separate qualified committee should be established to review marketing plans. The committee should be made

irrespective of present titles.

Ken suggested that the Operations Committee should assign, from a recommended list, a review committee for each engineering and marketing plan. These reviews should be reported back to the Operations Committee.

Nick suggested that the Engineering and Marketing Committees can take responsibility for the functional problems that exist in their respective areas.

5. SJCC Trade Booth

Jim Jordan proposed a new booth system, using 4' x 8' panels and modular construction without a false floor. Ken suggested that the damageability of the new system does not compare with the old carpeted system. The proposal was rejected.

A number of booth suggestions were made. Ken proposed that we redo our present system so that the carpeted back panels can be utilized with a false floor carpeted or without a false floor. Ken also suggested that we bring too much equipment to the Trade Shows and that, maybe, we should take one computer to each show. Stan suggested only a carpet and equipment, no booth. John Jones suggested that island booths tend to make it possible to get people into the booth and out of the aisle.

The theme for the SJCC seems to be "New Products" and/or DEC's "Broad Capabilities".

6. Number of Trade Shows - Ted Johnson

Ted broke down the number of shows, by product line, region, market, show size and show cost. Ted wants to look at educational and bio-medical shows, as well as March, April and May, which are the heavy show months. Nick and Win will assist. Pressure for show participation comes primarily from the Maynard Product Line Managers and the Marketing Managers. Also, Ted will look at the Return/Marketing Dollar versus hiring additional marketing people or promotional literature.

7. Corporate Press Conference - (Middle of April between IEEE and SJCC Shows)

This proposal does not commit us to quote delivery and price; but, as part of a public and financial relation's program, this conference was approved. Mark Nigberg is responsible and will submit a final plan, including the integrated advertising and promotion program.

8. Financial and Consultant Relations Proposal

This program is designed towards integrating our external communication's program. The Financial Relations Program was approved with the following exceptions:

(1) The Operations Committee will not talk individually in front of the Financial Analysts. This will be taken care of by biannual plant visits.

(2) Individual stock analyst's meetings will be the complete responsibility of the Vice President of Finance.

The Consultant Relations Proposal requires an additional person and will be discussed next week. It was suggested that we walk into this program step by step and, when successful, move on to a new group.

9. Stock Options

Win suggested that we think about additional stock options to personnel.

10. Next week's agenda should include the following items:

(a) TU-79 review - Bob Savell
(b) Review of Bob Collings' Proposal KV Graphic System - Nick Mazzarese
(c) Consultants Relations Proposal - Mark Nigberg
(d) Discussion of the Disposal of Company Reports - Stan Olsen
(e) Procedure for Setting Dates for Taking Orders of New Products and Peripherals.

jb

digital INTEROFFICE MEMORANDUM

DATE: 17 January 1969

SUBJECT: Pre-Announcement of PDP-11

TO: Operations Committee FROM: John Cohen

PDP-11 Marketing has prepared a "first package" of technical information on the the new computer. To accomplish the "pre-announcement" quickly and efficiently, I propose that the attached information be sent to the district managers immediately.

INTEROFFICE MEMORANDUM

DATE: 17 January 1969

SUBJECT: Pre-Announcement of PDP-11

TO: District Managers FROM: John Cohen

I. Introduction

We will soon have a major new computer product. The PDP-11 will be announced and demonstrated in New York on April 14. Before that time, we want to break the news to OEM's and selected customers (at the discretion of the district managers). Don't lose to competitive 8 or 16 bit machines because the customer doesn't know about the impending PDP-11. The three attached memos may be discussed with and "leaked to" customers (however, don't give them this memo).

II. What Is the PDP-11?

The PDP-11 is Digital Equipment Corporation's new small computer family. There are three basic configurations. The PDP-11C is the smallest member consisting only of a processor, a 1K read-only memory and a 64 byte read/restore memory.

Next, the PDP-11B contains a processor, a 4K byte read/restore memory, a teletype and a console. Unlike the 11C, it is a full-scale general purpose computer.

Finally, the PDP-11A consists of a fast processor, 8K bytes of fast memory (1 microsecond), teletype and console.

Be sure to tell your customers:

--the PDP-11 will be delivered this year
--the price will be less than the price of the PDP-8/L
--the performance/price of the PDP-11 is significantly greater than that of any other small computer in the industry.

III. Why Are We Building It?

PDP-11 is intended to affirm Digital Equipment Corporation's small

computer leadership. We anticipate competition from various other manufacturers and intend PDP-11 to stifle all of this. We want to be in the position to produce the "cheapest computer to do the job". In its basic configurations, the PDP-11 will be the most inexpensive computer on the market. But beyond this, its modular building block organization will allow us to configure an endless variety of special systems. No one will have to buy more than he needs in one capability in order to get just what he needs in an other.

The PDP-11 handles both bytes (8 bits) and words (16 bits) with equal ease. This has been accomplished without degrading its performance on one for the other.

Because of the extremely low price of the PDP-11 and because of its startling performance, DEC will be able to forge into new application areas where computers are considered too expensive at this time.

IV. Who Will Buy The PDP-11?

PDP-11 is applicable to much of the existing PDP-8 market. This includes OEM's, general computing and communications. The interrupt capability and the byte handling of PDP-11 will put us in an extremely strong position for communication products. It is hoped that one new market will be commercial applications such as payroll, labor distribution, inventory control, accounts payable, accounts receivable and sales analysis.

V. Who Won't Buy The PDP-11?

Quite likely, some Computerpacs will not be converted to the PDP-11 (for example, type setting and GASCHROM-8). The PDP-11 and the PDP-8 are not program compatible. Thus the expense of re-writing the software for some of the systems might offset the gains to be achieved by the lower hardware cost.

The PDP-11 will initially have no multiply, divide or floating point arithmetic. It has been intended that the machine primarily serve data handling, bit-shuffling applications. The system has been designed such that EAE's are very easy to design and interface -- however, we do not plan to build any extended arithmetic this year.

PDP-11 is not intended for the general time-sharing market. It has no memory protect feature and its interrupt structure, while extensive, has not been designed to compete with the PDP-10.

VI. Instruction Set

PDP-11 has 10 basic memory reference instructions. These are:

load byte
load word
store byte
store word
add byte
add word
compare byte
compare word
and
increment
jump
jump to subroutine

It has an operate group similar to the PDP-8 and PDP-9 for accumulator manipulations and shifting. It has a group of "push/pop" instructions which provide re-entrant interrupts and the "best" subroutine linkage capability. It has a group of conditional jump instructions which test the results of previous arithmetic operations.

The PDP-11 has been exhaustively compared with many other small computers to determine the merit of its instruction set. Frankly, we have been startled by the results. Running speed will be approximately 5 times that of the PDP-8, although the memory speed of the PDP-11A is simply 1 microsecond.

VII. Bit Economy

The PDP-11 has a number of features which allow programs to be encoded in many fewer instruction bits than other small computers. The first of these is "mini addressing" which allows certain memory words to be referred to in a single 8-bit memory reference instruction. These three words are intended to be used for frequently referenced data. Our coding examples show that 65 to 75% of memory reference instructions can be made to refer to these words.

The operate group consists of 8-bit instructions. Thus when a programmer wants to increment the accumulator, he does so by single 8-bit command. On the PDP-8, this takes 12 bits; and 18 bits on the PDP-9.

Subroutine communication is handled with a hardware push down list. Thus return addresses are placed automatically in a stack. It is not necessary to save and restore the return address - nor is it necessary to reserve a word in each subroutine for this purpose.

Arguments are picked up and restored using an indexed, deferred addressing mode. This feature has, up to now, only been found in higher priced computers (for example, the PDP-10).

In small computer applications it is frequently desired to compare byte and word data (in an accumulator) with the contents of a memory location. This comparison is used typically in conjunction with a branch or skip on condition. The PDP-11 has compare byte and compare word instructions which allow the accumulator to be easily compared with any memory word. The instruction results in certain control bits being set in the processor. Neither the accumulator nor the memory word is effected. These instructions are normally followed by a conditional jump instruction which is controlled by the setting of the result condition codes. This feature dramatically cuts down on the number of instructions needed to perform complex comparisons.

VIII. Interfacing

The PDP-11 has a single 27 wire bus which is used to connect both memory and input/ouput devices. All subassemblies communicate with each other using a simple, asynchronous dialogue. We will provide standard interface modules to make it extremely easy to perform the normal functions of connecting a user device to a PDP-11. The modules will

- --allow the user to select a memory or processor register address
- --transfer data to the selected register or memory word
- --transfer data from the selected register or memory word
- --perform a direct memory access operation (data channel) easily
- --cause the processor to transfer control to an interrupt handling routine

IX. Configurations

PDP-11 allows a greater range of configurations than any other small computer. It is possible to inter-mix memory types - there may be up to 56K bytes of memory with any combination of read only and read/restore. Memories may also be of different speeds - for example, it is possible to have a system with 1K fast (1 microsecond) memory and 16K slow (3 microsecond) memory. Memory and devices are connected to a similar bus and have similar address types. Thus there is no reasonable limit on the number of input/ouput devices which can be connected to a PDP-11.

A PDP-11 may be sold with or without a console. It is even possible to put more than one console on a system with a single processor. Next year it is anticipated that the PDP-11 line will be extended to

include the facility for multiple processors - allowing us to configure very low price systems with an extraordinary range of capability.

X. Impact On DEC

As Gabe D'Annunzio phrases it, Digital Equipment Corporation has "reinvented" the small computer with the PDP-11. Its effect on our competitors should be fairly obvious. The low price coupled with the extremely high performance will unquestionably open many new application areas. We feel that without question, the PDP-11 is a hot product and greatly appreciate the efforts of all of the groups in the company helping to produce it.

Preliminary Specification

PDP-11 Instruction Set

January 14, 1969

CONFIDENTIAL

DIGITAL EQUIPMENT CORPORATION

PM 21-18

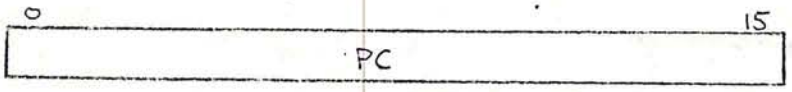
I. Introduction

The PDP-11 is a 16-bit small computer. It operates on bytes (8 bits) or words (16 bits). The memory is byte addressable, to a maximum of 65536 bytes. Instructions are 1, 2, or 3 bytes (8, 16, 24 bits). This memo describes the processor registers, the memory reference instruction addressing and the four groups of machine instructions - memory reference, operate, conditional jump and add to register.

II. Processor Registers

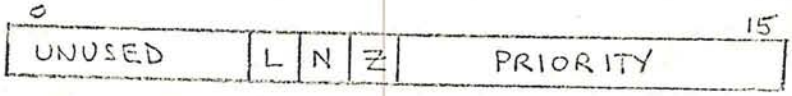
The PDP-11 has 8 16-bit hardware registers.

A. Program Counter



Prior to each instruction, the program counter contains a number which is 1 less than the address of the next instruction to be executed. The program itself is addressable at (177760)8.

B. Status Register



The status register is divided into 2 bytes - the high order contains condition codes and the low order the current priority of the processor The register is addressable at (177762)8.

1. Condition Codes

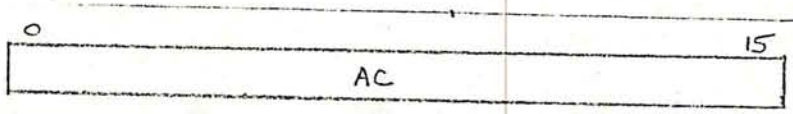
Bit 5 through 7 of the status register are called the condition codes. They are set according to the results of most instructions. L (bit 5) is complemented as a result of carry out from the adder. N (bit 6) is set (reset) if the result of an arithmetic instruction is negative (non-negative). Z (bit 7) is set (reset) if the result of an arithmetic operation is Ø (non-Ø). Bit Ø through 4 of the status register are not used by the processor and, as such, may be used by the program as temporary storage.

2. Priority

Bit 8 through 15 of the status register determine the priority of the currently running program. The permissable contents are:

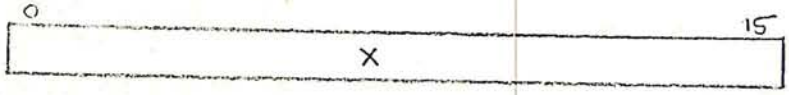
8							15	
0	0	0	0	0	0	0	0	LOWEST PRIORITY
0	0	0	0	0	0	0	1	
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	1	1	
0	0	0	0	1	1	1	1	
0	0	0	1	1	1	1	1	
0	0	1	1	1	1	1	1	
0	1	1	1	1	1	1	1	
1	1	1	1	1	1	1	1	HIGHEST PRIORITY

C. Accumulator



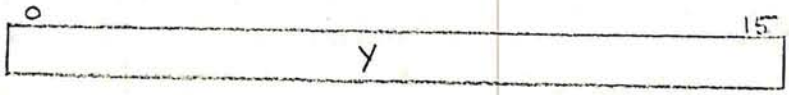
This register is used both as an operand and as the result register for most arithmetic instructions. In addition to being implicitly addressed by these instructions, it also may be explicitly addressed at location (177764)8.

D. X-Register



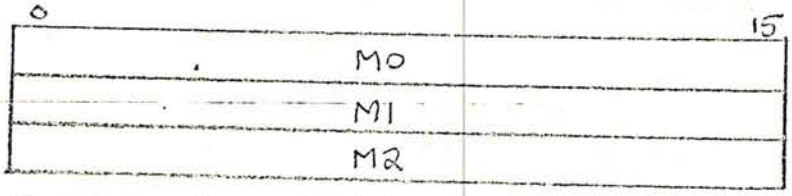
The X-Register is used to provide a hardware push down list facility. It may also be employed as a general index register. It is incremented by 2 during the subroutine call instruction and decremented by 2 during the subroutine return. It is also incremented and decremented by the ATX instruction to provide reentrant subroutines. It may be explicitly addressed at (177766)8.

E. Y-Register



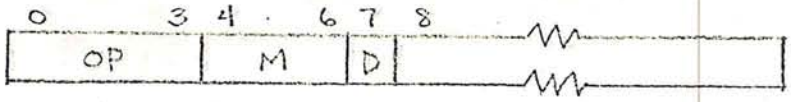
This register is used for subroutine argument communication and as a general index register. For subroutine communication, it is set to the return address by the subroutine calling instruction. The Y-register may also be explicitly addressed at (177770)8.

F. "Mini" Registers



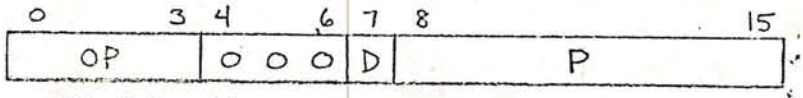
The "mini" registers are three hardware 16-bit registers used by the program as temporary storage. They are normally addressed in the "mini" mode described below in Section III. In addition, MØ, M1, M2 may be explicitly addressed at (177772)8, (177774)8, (177776)8, respectively.

III. Memory Reference Instruction Addressing



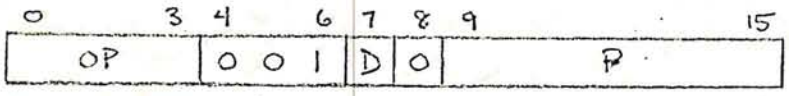
Each memory reference instruction consists of 1, 2 or 3 bytes. The first byte is called the instruction byte. Successive bytes, if any, contain either address information or data. The operation code (OP) is in the range of Ø through (14)8. The mode bits (M) determine the address computation. The deferred bit (D) specifies whether the address is to be deferred 1 level indirectly.

A. Relative Addressing



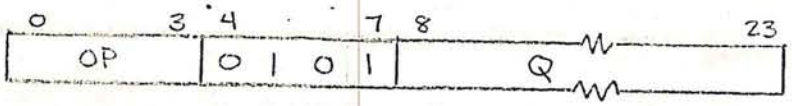
The 2's complement offset P is added to the program counter to form an effective address which is in the range (-200, +177) relative to the program counter.

B. Page Ø Addressing



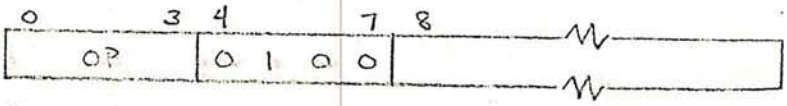
P is used to form an address in the range (0, 177).

C. Full Addressing



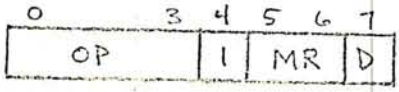
Q is taken as a full 16-bit address. This address mode cannot be deferred.

D. Immediate Addressing



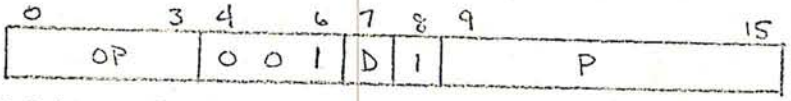
The operand is taken directly from the byte or word following the instruction byte. The operand is a byte or a word depending on the operation code (see section IV). This addressing mode may not be deferred.

E. "Mini" Addressing



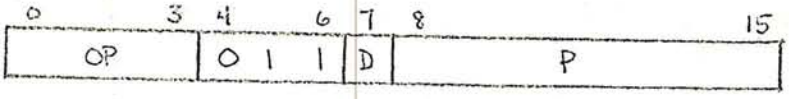
The effective address before deferral is MØ, M1, M2 depending on whether MR is Ø, 1, 2, respectively. If D is set, an "autoincrement" is added to the mini register to determine the effective address. This new effective address also replaces the contents of the mini register. The autoincrement is Ø, 1 or 2 depending on the instruction (see section IV).

F. External Addressing



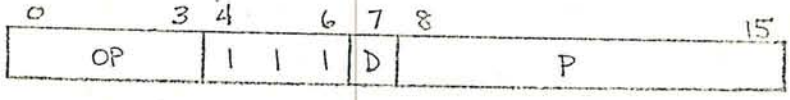
In this mode, the high order 9 bits of the effective address before deferral are all ones. The low order 7 bits are the 2's complement of P. Thus the address range before deferral is (177600-177777). Input/output and external devices are typically assigned in this area - thus the external addressing mode allows input/output or external references in a 2 byte instruction.

G. X-Indexed Addressing



The effective address before deferral is the sum of the 2's complement number P and the contents of the X-register. This provides a range of (-200, +177) relative to the contents of X.

H. Y-Indexed Addressing

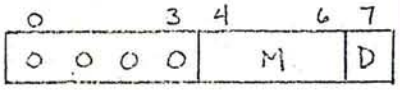


The effective address, before deferral, is the sum of the 2's complement

number P and the contents of the Y-register. This provides a range of (-200, +177) relative to the contents of Y.

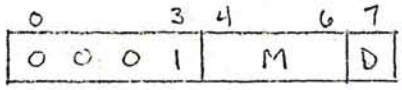
IV. Memory Reference Instruction Group

A. Load Byte (LDB)



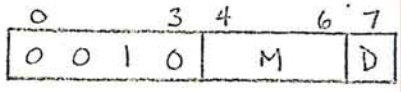
The effective byte is loaded into bits 8 through 15 of the accumulator. The left of the accumulator (bit Ø through 7) are cleared. L is not effected. N is set to bit Ø of the effective byte. Z is set to 1 (Ø) if the effective byte is Ø (non-Ø). The autoincrement is 1.

B. Load Word (LDW)



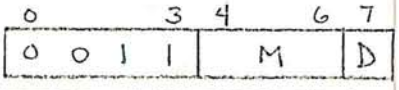
The effective word is loaded into the accumulator. L is not changed. N is set to bit Ø of the effective word. Z is set to 1 (Ø) if the effective word is Ø (non-zero). The autoincrement is 2.

C. Store Byte (STB)



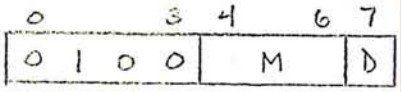
The contents of accumulator bits 8 through 15 are stored in the effective byte. The condition codes are not effected. The autoincrement is 1.

D. Store Word (STW)



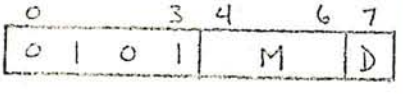
The contents of the accumulator are stored in the effective word. The condition codes are not effected. The autoincrement is 2.

E. Add Byte (ADB)



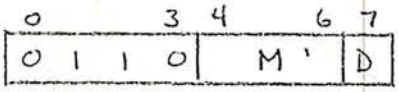
The effective byte is treated as a positive 8-bit quantity and added to the contents of the accumulator. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero). The autoincrement is 1.

F. Add Word (ADW)



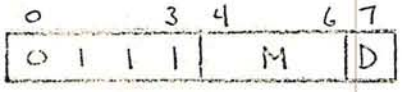
The effective word is added to the contents of the accumulator. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero). The autoincrement is 2.

G. Compare Byte (CPB)



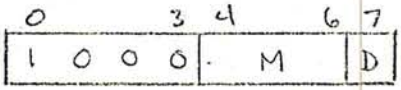
The 2's complement of the accumulator and the effective byte are added together. The effective byte is treated as a positive 8-bit quantity. The result is not stored in any register, but is used to set the condition codes. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero). The autoincrement is 1.

H. Compare Word (CPW)



The 2's complement of the accumulator and the effective word are added together. The result is not stored in any register, but is used to set the condition codes. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero). The autoincrement is 2.

I. And Byte (ANB)

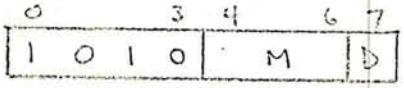


The effective byte is anded to the contents of the accumulator bits 8 through 15. Bit Ø through 7 of the accumulator are not effected. L is not changed. N is set to Ø. Z is set to one (zero) if the accumulator is zero (non-zero) after the operation. The autoincrement is 1.

J. Increment (INC)

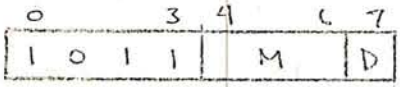
The effective word is incremented by one. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero). The autoincrement is two.

K. Jump (JMP)



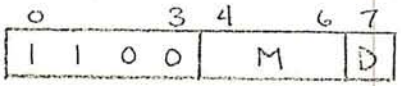
The effective address replaces the contents of the program counter. The condition codes are not effected. The autoincrement is zero.

L. Jump to Subroutine (JSR)



The program counter is stored in the word which has the address one greater than the contents of the X-register. The X register is then incremented by two. The old program counter is also stored in the Y-register. The effective address then replaces the contents of the program counter. The condition codes are not effected. The autoincrement is zero.

M. Interrupt (INT)



The INT instruction functions one of three ways, depending on the

high order 8 bits of the effective address.'

1. Interrupt of Processor

This instruction causes the processor to "interrupt itself" -- that is, respond as if the interrupt had occurred from an external device. It occurs if the high order 8 bits of the effective address are zero. The effective address bits 8 through 15 are stored in the location which is 1 greater than the contents of the X-register. The program counter is stored in the location which is 2 greater than the contents of the X-register. The status register is stored in the location which is 4 greater than the contents of the X-register. The X-register itself is incremented by 5.

The contents of the effective address replace the contents of the program counter. The contents of the word with the address 2 greater than the effective address replace the status register. The autoincrement is zero.

2. Trap

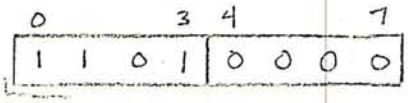
If bits Ø through 7 of the effective address are not all zeros nor or ones, the effect is the same as an interrupt instruction with aneffective address of zero. This is used to simulate unimplemented operation codes by software or firmware programs. The contents of the word at location zero must thus be the starting address of a software trap handler.

3. Stop

If bit zero through 7 of the effective address are all ones, the system stops. The condition codes are not effected. The autoincrement is zero.

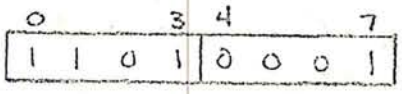
V. Operate Instruction Group

A. No Operation (NOP)



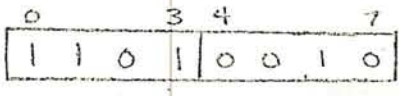
The program counter is advanced one byte. The condition codes are not changed.

B. Increment Accumulator (IAC)



The accumulator is incremented by one. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

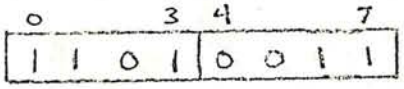
C. Complement Accumulator (CMA)



The contents of the accumulator are replaced by the ones complement of the original contents. The L bit is not effected. N is set to

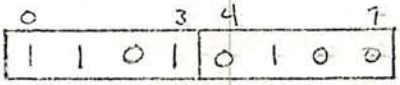
the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

D. Negate (NEG)



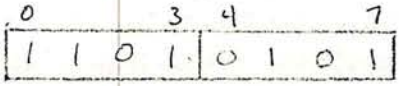
The two's complement of the accumulator replaces the original accumulator contents. L is not changed. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

E. Clear Accumulator (CLA)



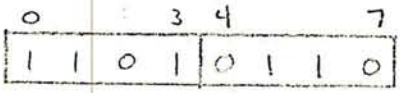
The contents of the accumulator areset to zero. L is not effected. N is set to zero and Z is set to one.

F. Plus One to Accumulator (POA)



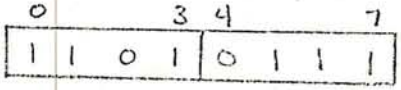
The accumulator is set to plus one. L is not effected. Both N and Z are set to zero.

G. Minus One to Accumulator (MOA)



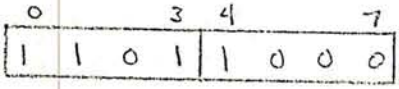
The accumulator is set to minus one. L is not effected. N is set to one and Z is set to zero.

H. Clear Accumulator and Link (CAL)



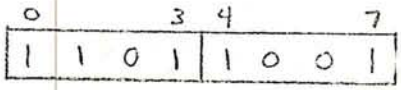
The accumulator and the L bit are both set to zero. N and Z are not changed.

I. Rotate Accumulator Right (RAR)



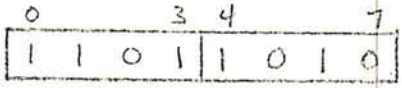
The L bit and the accumulator are treated as a single 17 bit circular register. The combination is rotated right one bit position (L goes into accumulator bit zero and accumulator bit 15 goes into L). N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

J. Rotate Accumulator Left (RAL)



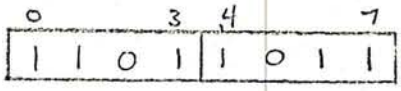
The L bit and the accumulator are treated as a single 17 bit register. The combination is rotated left one bit position (L goes to accumulator bit 15 and accumulator bit zero goes to L). N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

K. Clear Link (CLL)



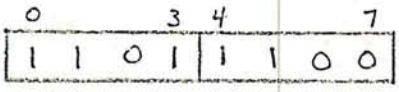
L is set to zero. N and Z are not effected.

L. Complement Link (CML)



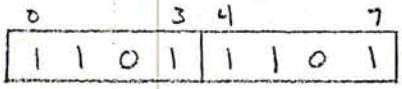
The L bit is complemented. N and Z are not effected.

M. Return (RTN)



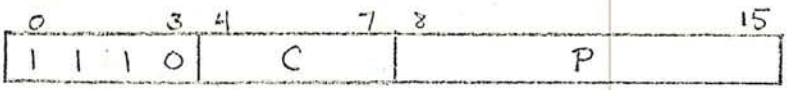
The word at the address which is one less than the contents of X replaces the program counter. The contents of the X-register are then decremented by two. This instruction is the return for JSR.

N. Return from Interrupt (RTI)



The program counter is replaced by the word in the address three less than the contents of X. The status register is replaced by the word at the address one less than the contents of X. The X-register is then decremented by five. This instruction is the return for INT and also is the last instruction in each interrupt handling routine.

VI. Conditional Jump Instruction Group



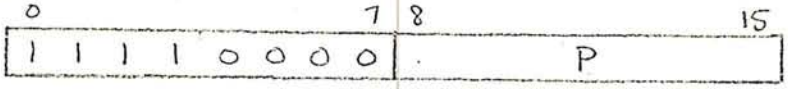
The C field is associated with the possible conditions of the L, N and Z codes. If the specified condition is met, the offset P is added as a two's complement number to the program counter. This provides a range of (-200, +177) relative to the current program counter. If the condition is not met, the next instruction is executed. The condition codes themselves are not effected.

The mnemonics, C field and the conditions tested are:

C	mnemonic	meaning	condition
01	JEQ	jump on equal	Z
11	JNE	jump on not equal	not Z
02	JLT	jump on less than	N
13	JGT	jump on greater than	not N and not Z
03	JLE	jump on less than or equal	N or Z
12	JGE	jump on greater or equal	not N
04	JLS	jump on link set	L
14	JLR	jump on link reset	not L

VII. Add to Register Group

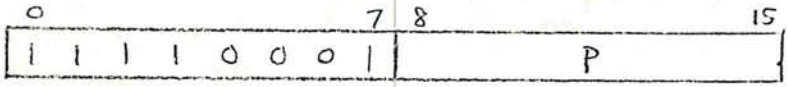
A. Add to MØ (AMØ)



P is treated as an 8-bit two's complement number and added to the contents of MØ. L is complemented if the operation causes a carry

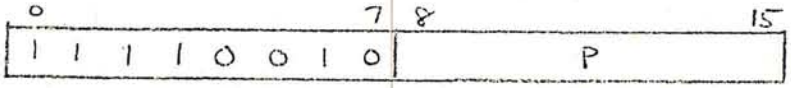
out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

B. Add to M1 (AM1)



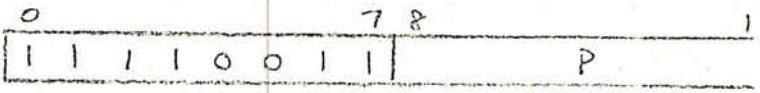
P is treated as an 8-bit two's complement number and added to M1. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

C. Add to M2 (AM2)



P is treates as an 8-bit two's complement number and added to M2. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

D. Add to X-Register (ATX)



P is treated as an 8-bit two's complement number and added to X. L is complemented if the operation causes a carry out of bit zero of the adder. N is set to the high order bit of the result. Z is set to one (zero) if the result is zero (non-zero).

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digital INTEROFFICE MEMORANDUM

PM 35-2

DATE: 11 January 1969

SUBJECT: How Good is the PDP-11?

TO: Ted Johnson
Nick Mazzarese

FROM: John Cohen

As you know, we have devoted much time and effort programming comparison examples of the PDP-11 and other machines. The results have been quite significant - the PDP-11 turns out to be significantly ahead of all other small computers in both speed and memory economy.

Some of the most startling statistics are:

--the PDP-11A runs programs 5 times faster than any other small computer
--programs can be coded on the PDP-11 using 50% fewer bits than an equivalent program on any other computer

We are naturally quite excited about these statistics. In addition, the feed-back we get from the groups producing the software indicates that the machine is very easy to program. It almost seems too good to be true, but I have checked through the technical material myself and find that it is accurate.

The detailed programming comparison examples appear in Project Memoranda PM 18-3 and PM 35-1. I shall summarize the results here.

We used five test problems. Two are principally character oriented and two arithmetic. Two of the routines will require to be "subroutinized", in that they picked up arguments from calling routine or restored values. The problems were:

1. Move characters in edit
2. Multiply subroutine
3. Tolerance check
4. Histogram compellation
5. Decimal to binary conversion

Machines in the comparison were:

PDP-11A (fast PDP-11)
PDP-11B (slow PDP-11)
PDP-8
Data General NOVA
Varian 520I
Varian 620I

Hewlett-Packard 2114A
Interdata I3 (internal instruction set)
Interdata I3 (external instruction set)
PDP-X (a machine we never built)
SPC-12
PDC-808

The following table shows the number of bits need to encode each of the five problems on the 12 instruction sets:

	1	2	3	4	5
PDP-11A	280	280	240	320	200
PDP-11B	280	280	240	320	200
PDP-8	468	432	420	376	256
NOVA	640	272	320	400	368
520I	752	488	632	496	320
620I	1130	496	780	896	440
2114A	1040	384	576	656	340
I3 (INT)	864	1100	1200	784	512
I3 (EXT)	784	640	688	640	384
PDP-X	576	368	432	448	304
SPC-12	824	1030	1420	752	344
PDC-808	664	1080	1320	728	632

Normalizing this to 100 for the PDP-11, we get:

	1	2	3	4	5	ave
PDP-11A	100	100	100	100	100	100
PDP-11B	100	100	100	100	100	100
PDP-8	167	160	175	118	128	150
NOVA	229	97	133	125	184	154
520I	269	171	264	155	160	203
620I	404	177	326	280	220	281
2114A	372	137	240	206	170	225
I3 (INT)	309	393	500	245	256	340
I3 (EXT)	280	229	287	200	192	237
PDP-X	206	131	180	140	152	161
SPC-12	295	368	592	235	172	332
PDC-808	237	386	550	228	316	343

The average over the five problems for each machine appears in the right hand column. It is very significant to notice the differences between machines. Some machines (Interdata Internal, SPC-12, PDC-808) actually use more than three times as many bits

to encode a problem than the best machine in this category.

The number of machine cycles to execute each problem was also tallied. These results were:

	1	2	3	4	5
PDP-11A	4260	149	1210	12400	49
PDP-11B	8210	297	2220	20600	98
PDP-8	50500	313	2640	21600	198
NOVA	31200	135	1530	16600	190
520I	35200	260	4880	40000	218
620I	43100	451	2260	51800	190
2114A	17400	149	1750	33800	133
I3 (INT)	18200	294	4080	32700	125
I3 (EXT)	21000	500	2560	40500	102
PDP-X	11400	188	1320	16500	85
SPC-12	32200	843	10500	57400	196
PDC-808	27000	979	12000	63700	529

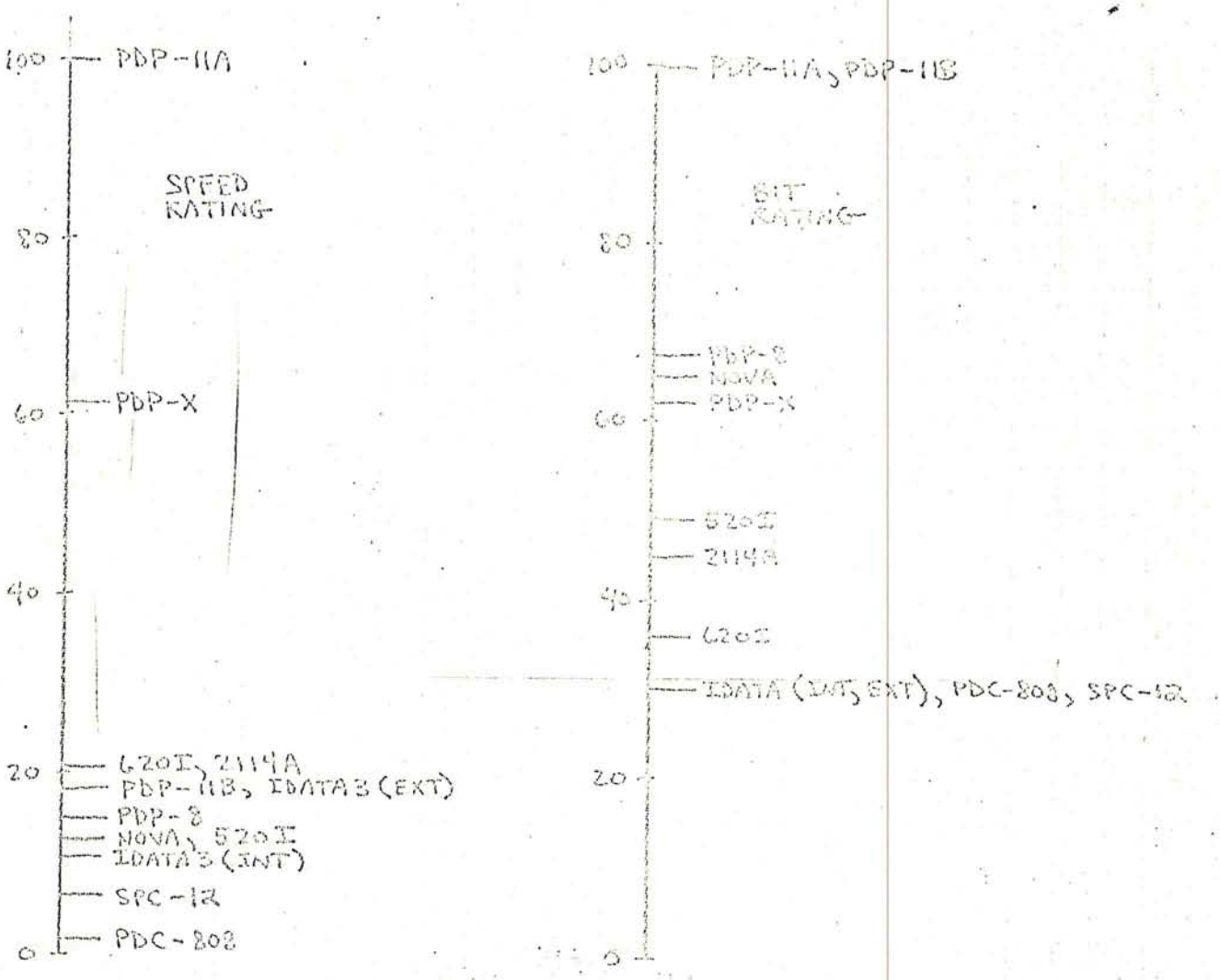
Again normalizing to a 100 for the PDP-11A, we get:

	1	2	3	4	5	ave	cyc	spd
PDP-11A	100	100	100	100	100	100	1.0	100
PDP-11B	193	199	182	166	200	188	3.0	564
PDP-8	1190	210	218	174	404	439	1.5	658
NOVA	734	91	127	134	388	294	2.6	764
520I	1210	175	404	322	446	511	1.5	767
620I	1010	303	187	418	388	461	1.0	461
2114A	409	100	145	272	272	239	2.0	478
I3 (INT)	428	195	337	264	256	296	3.0	887
I3 (EXT)	494	336	212	326	208	315	1.8	567
PDP-X	268	126	109	133	173	161	1.0	161
SPC-12	760	567	869	462	400	611	2.4	1460
PDC-808	635	656	992	514	1080	775	8.0	6190

The number of cycles for each machine was averaged in the column headed "ave". The next column (cyc) contains the cycle time for the machine. Finally, the right hand column gives the normalized averaged speed for the five problems on each machine. Again there is a tremendous spread. The fact that the PDP-11 wins so strongly in both speed and memory economy, couple with its low price, clearly indicates that the product has unlimited potential.

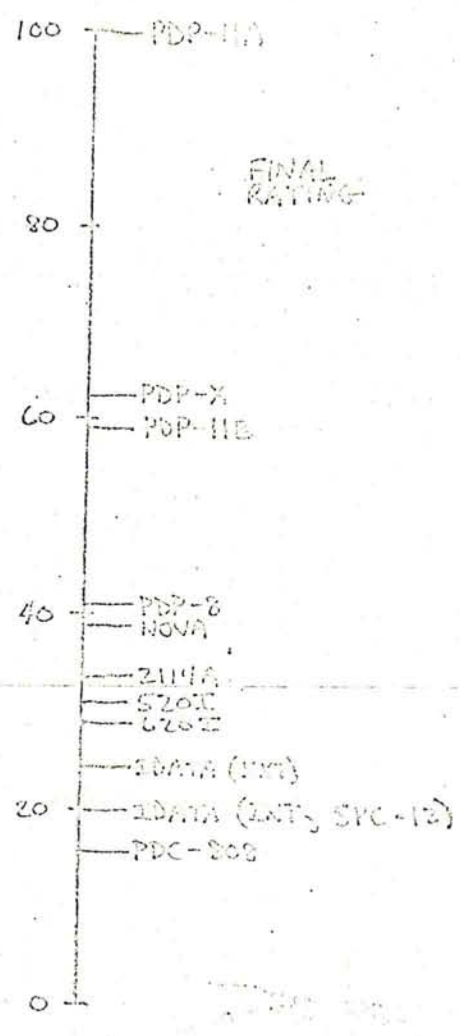
We have compiled ratings by taking the inverse of the bit and speed normalized averages for each machine. The plots for both speed and

memory economy are:



This graphically indicates how the PDP-11A simply runs away from all the other machines in processing speed and how the entire PDP-11 family handily defeats all other computers in bit efficiency.

As a final rating, we averaged the speed with the bit efficiency, counting each equally, The results speak for themselves:



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INTEROFFICE MEMORANDUM

PM 35-1

DATE: 11 January 1969

SUBJECT: Comparison of PDP-11, PDP-8 and the NOVA

TO: Distribution List FROM: John Cohen

I. Introduction

When the PDP-11 instruction set design was completed, a number of people asked how it compared with other computers. To get the answer, it was decided to compare typical small computer problems on the PDP-11, PDP-8 and the NOVA. Five examples were chosen - some character oriented and some arithmetic. Each problem was coded for the three computers. Instruction bits and execution cycles were counted. The results of these counts were used to evaluate the performance of the various instruction sets.

The PDP-11 turned out to be best both in speed and memory economy. Specifically:

--the PDP-8 used 50% more instruction bits than the PDP-11
--the NOVA used 54% more instruction bits that the PDP-11
--the PDP-11A runs the example problems 6 times faster than the PDP-8
--the PDP-11A runs the problems 7 times faster than the NOVA
--the PDP-11B is 20% faster than the PDP-8
--the PDP-8 is 15% faster than the NOVA

The study procedure which we followed is defined in Section II. The results of the study are given in Section III. Appendix A contains the actual code which we generated for the test problems.

II. Data Gathering

This section discusses the test applications in the study and describes the evaluation procedure.

A. Applications

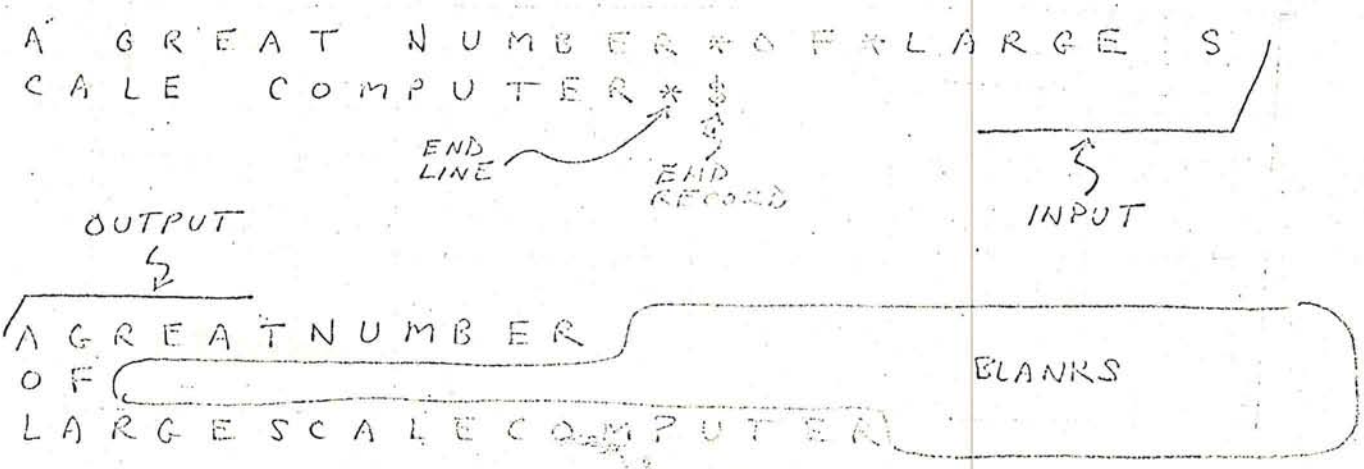
We used five test problems. Two were principally character oriented and two arithmetic. Another operated on both 8-bit and 16-bit data. Two of the routines were required to be "subroutinized", in that they picked up arguments from a calling routine and restored values.

1. Move Characters and Edit

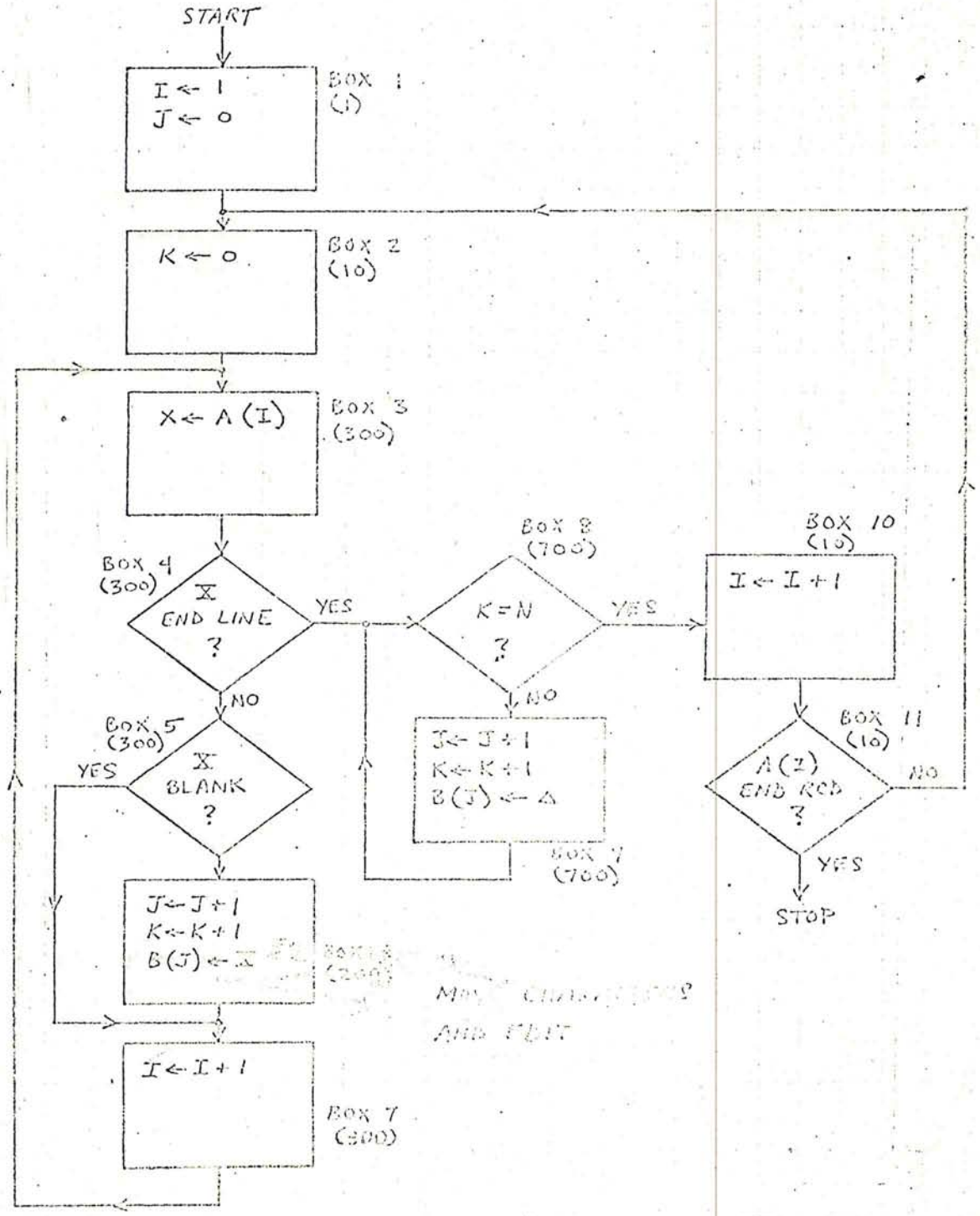
This problem tested the ability of the machine to move characters (8-bits) from one memory block to another. It also made use of array indices - which had ranges of less than 256 and also which had ranges greater than 256. The ability of the machine to branch on character matches was also important.

The input characters were broken down into a variable number of lines, and terminated with a special end of record character. Each line was of variable length, terminated by a special end of line character. The output character array was the same as the input, except that the lines were edited to a fixed length. The end of line, end of record characters were removed, as well as all embedded blanks. The individual lines were blank filled on the right to make them all the same leng (the output line length was greater than the number of nonblank characters in each input line).

An example of the operation of this routine is:



The flow chart is:



where A is the input array
B is the output character array
I is an index to the input
J is an index to the output
K counts the number of characters in an output line
X holds the current input character
N is the (variable) number of characters in an output line

Notice that the boxes in the flow chart are numbered. The number of times each box is executed is given by the assoicated number in parenthesis.

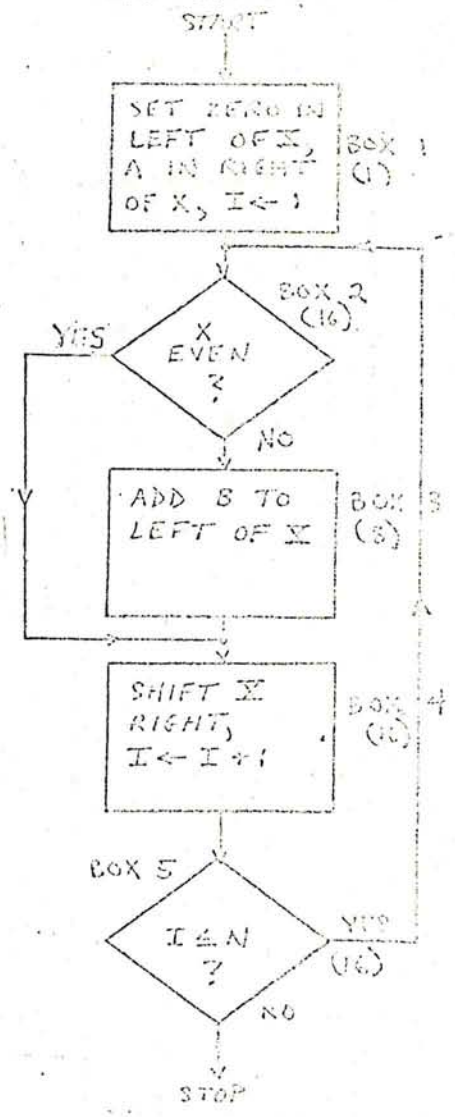
We assumed that there were 10 input lines of 30 characters each, 20 of which were nonblank. The output line length was 100. Box 1 is executed once for initialization. Boxes 2, 10 and 11 are entered 10 times - once for each line. Boxes 3, 4, 5 and 7 are executed for each input character - in our example 300 or 30 per line. Box 6 is executed for only the nonblank characters - thus 200 times or 20 times per line. Boxes 8 and 9 are used to fill the input lines with blanks. This occurs 70 times per line for a total of 700 in the problem.

2. Multiply Subroutine

This problem had a number of objectives - testing the ability of the machine to set up subroutine linkage, to sense bit configurations and branch conditionally and to easily shift double words. The test is also important because the multiply operation is commonly used.

The program first picked up two 16-bit operands from the calling program. These were multiplied together by the usual shifting and adding method. The 32-bit result was returned to the calling program. The routine operated only on unsigned integers.

The flow chart is:



where X is a double word to hold one of the operands and the result
A is one of the operands
B is the other operand
I is an index to the number of bits in each operand
N is the number of bits in each operand

We assumed 16-bit operands in all cases. On the PDP-8, the program was written for 12-bit words, but the cycle count was later adjusted as if the main loop was executed 16 times. We assumed that the first input argument contains exactly 8 one's.

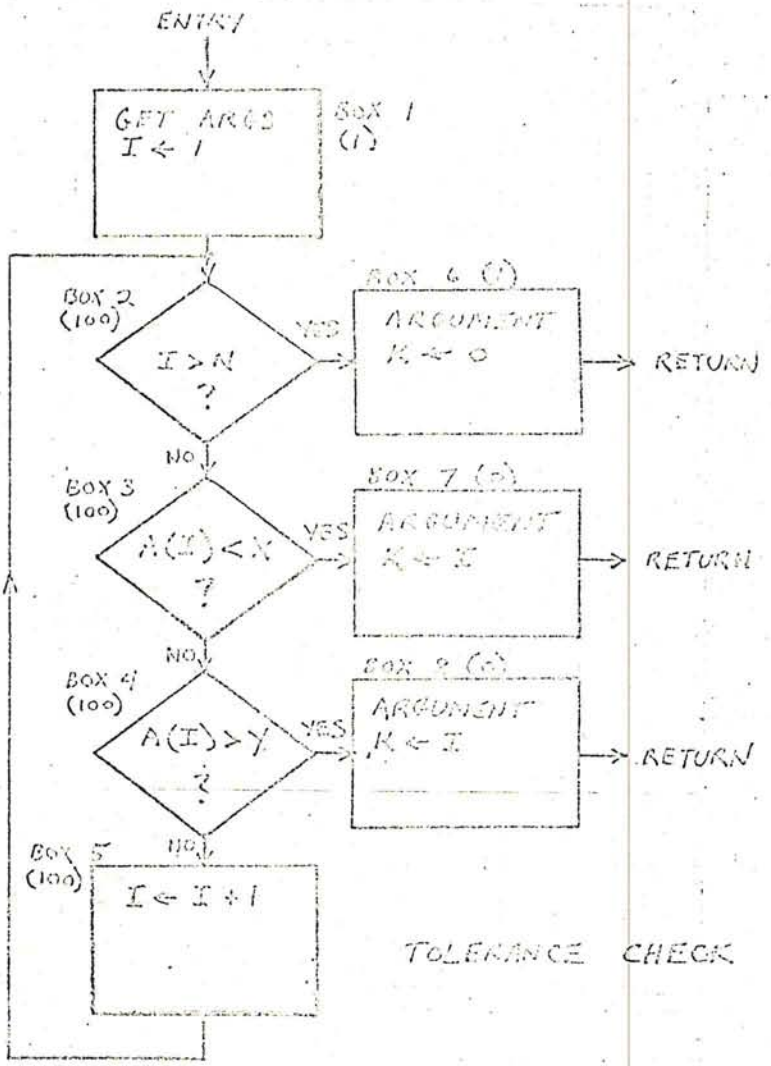
Box 1 is initialization and hence executed once. Boxes 2, 3 and 5 are entered for each bit - 16 times. Box 4 is executed only for 1 bits in the first operand - 8 times according to our assumptions.

3. Tolerance Check

The objective of this problem is to test arithmetic comparison capabilities and the ease in which the machine can index through an array of 16-bit quantities. Subroutine linkage was also considered in that the calling sequence to this problem was more complicated than that to the multiply subroutine.

The program picked up an array address, the count of the number of elements in the array and two tolerance limits from the calling program. It indexed through the array, checking each element against the low and high limits. If all elements were within tolerance, the program returned an output value of zero to the caller. If any were out of tolerance, the index in the array of the offender was returned.

The flow chart is:



where I is an index to the number of elements in the array
N is the number of elements in the array
A is the array of numbers
X is the low limit
Y is the high limit
K is the return argument

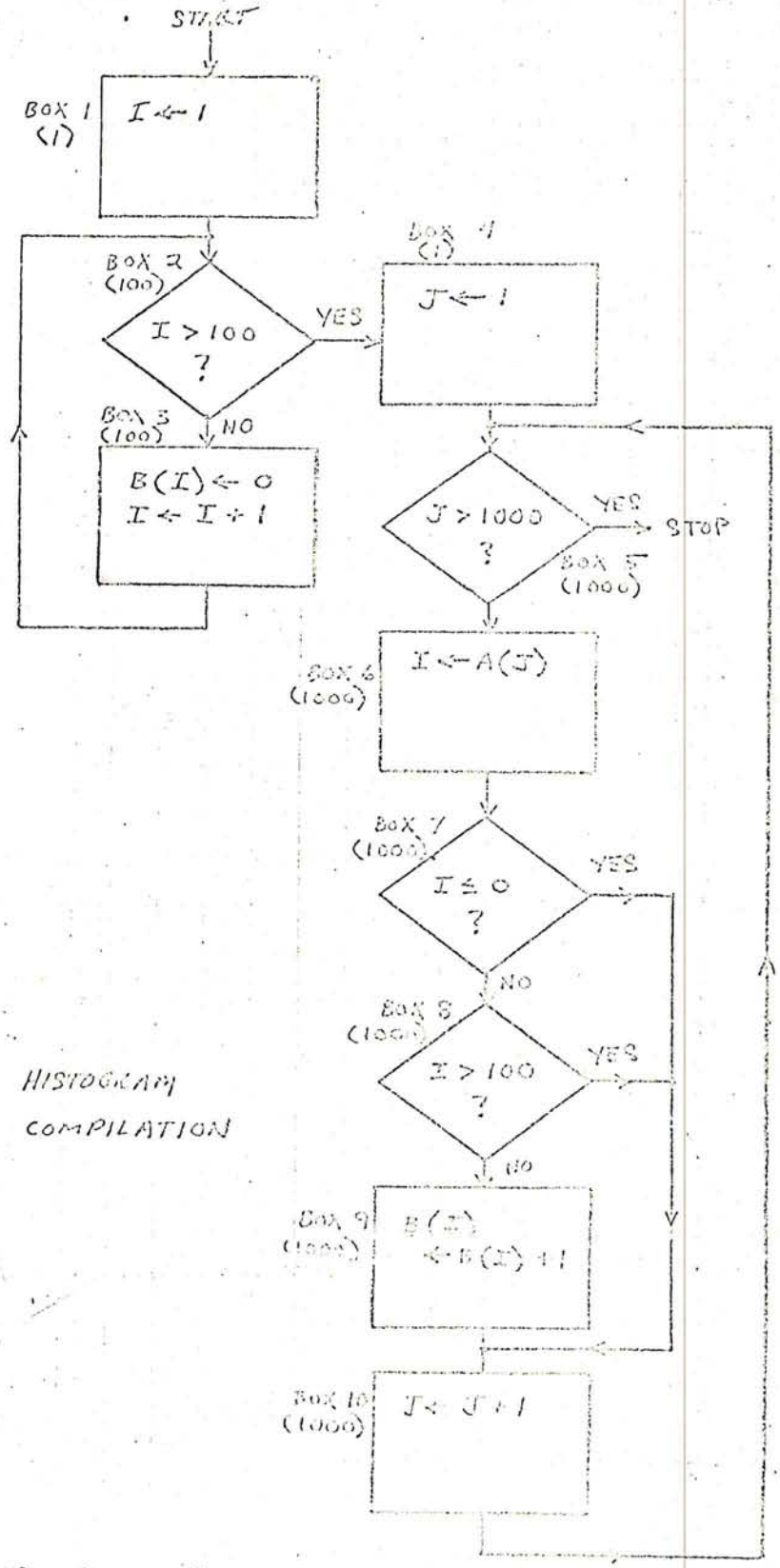
For timing considerations, we assumed that there were 100 entries in the array and that they were all in tolerance. Boxes 1 and 6 are executed once, as they involve initialization and termination, respectively. Boxes 2,3,4 and 5 are executed 100 times - once per array entry. Boxes 7 and 8 are not executed because of our assumption that all entries are in tolerance.

4. Histogram Compilation

It tests the ability of the machine to randomly index to memory arrays and to increment 16-bit memory integers.

The input is an array of 1,000 16-bit numbers, with values normally in the range of 1 through 100. The program must contain code to ignore other values - 0 or 101 through 256. The output is a memory array of 100 16-bit numbers. These contain the counts of occurences of the 100 possible input values. For example, if the 16-bit number 20 occurs exactly 15 times in the input array, the contents of the 20th element of the output array must be 15.

The flow chart for this problem is:



where A is the input data array
B is the output histogram array
I is an index through the output array
J is an index through the input array

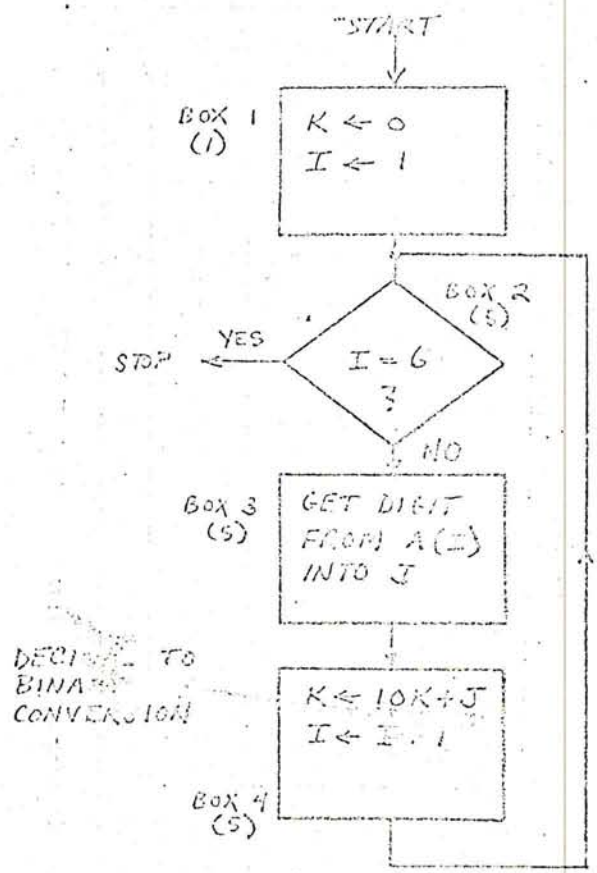
Boxes 1 and 4 are for initialization and hence, executed once. Boxes 2 and 3 are used to zero the output array and are executed once per output entry of 100 times. Boxes 5 through 10 are entered once per input entry, 1,000 times total.

5. Decimal to Binary Conversion

The objective of this test was to determine how the machines performed in this rather common application. The problem also tests character manipulation and the ability to do specialized multiplication using shifts and adds.

The input is a five character array and the output is an unsigned integer less than 32768. On the PDP-8, the routine was written for a 12-bit operation, but the cycle counts were multiplied by 16.

The flow chart is:



where A is the input character array
I is an index to the input characters
J is a temporary storage location for each binary digit
K is the binary result

B. Procedure

After the problems had been coded, we counted the number of bits and cycles used. The bit count involved a tally of the instruction words and storage for constant data. Temporary storage was not tallied, as it could be shared among routines or was contained in general registers. The word count was simply multiplied by the word length to get the program bit count.

Each program was partitioned as specified by the boxes in the flow charts. The number of machine cycles corresponding to each box was counted. This number was then multiplied by the corresponding box frequency, which appears with the box number on the flow charts. These products were then added together for each program, giving the cycle total for the problem.

Time figures for each computer were computed by multiplying the average cycle counts by the cycle time. This is assumed to be 1.5 microseconds for the PDP-8, 3.0 for the PDP-11B, 1.0 for the PDP-11A and 2.6 for the NOVA. The times for the latter were computed by assuming that every instruction took 2 cycles except for JMP and JSR which took 1.

III. Results

The following table summarizes the number of bits used for each problem:

prob	PDP-11A	PDP-11B	PDP-8	NOVA
1	280	280	468	640
2	280	280	432	272
3	240	240	420	320
4	320	320	376	400
5	200	200	256	368

Normalizing this to 100 for the PDP-11, this becomes:

prob	PDP-11A	PDP-11B	PDP-8	NOVA
1	100	100	167	229
2	100	100	160	97
3	100	100	175	133
4	100	100	118	125
5	100	100	128	184
average	100	100	150	154

The PDP-8 and the NOVA both have the liability of no byte handling instructions. Subroutines to load and store bytes were coded and called when relevant, but the bit count for these is not included (assuming that the routines are shared over a large number of programs).

The number of bits used by the PDP-8 varied from 18% more than the PDP-11 for the histogram example to 75% more in the tolerance check. The NOVA performed fairly well in this area for 16 bit arithmetic, but very poorly for character manipulations - even though a subroutine call was used.

B. Speed

Appendix B contains a detailed listing of the cycle counts for each problem on the three computers. The table for each problem has one row for each box on the flow chart. The number of times that box is executed is given in the frequency column. Then for each computer, the number of cycles to execute the box and the cycle total is given. The cycle totals are added together to form a grand total of memory cycles for each computer. A summary of these is:

prob	PDP-11A	PDP-11B	PDP-8	NOVA
1	4260	8210	50500	31200
2	149	297	313	135
3	1210	2220	2640	1530
4	12400	20600	21600	16600
5	49	98	198	190

Normalized to the PDP-11A, this becomes:

prob	PDP-11A	PDP-11B	PDP-8	NOVA
1	100	193	1186	734
2	100	199	210	91
3	100	182	218	127
4	100	166	174	134
5	100	200	248	258
average	100	188	408	269
time	100	564	610	700

The time row above was computed by multiplying the average cycles by the memory cycle time. As was mentioned before, the NOVA times were simplified by assuming all instructions took 2 memory cycles except JMP and JSR which took 1. The NOVA cycle is assumed to be 2.6 microseconds. The superiority of the PDP-11A is quite startling and it is significant that the PDP-11B edges out both the PDP-8 and the NOVA.

Appendix A. Coding For Example Problems

```
*       EXAMPLE 1A,B
*       MOVE CHARACTERS AND EDIT
*       PDP-11
START   LDW,I   A               1
        STW,M   MØ              1
        LDW,I   B-1             1
        STW,M   M1              1
Q2      LDW,I   -N              2
        STW,M   M2              2
Q3      LDB,LD  MØ              3
        CPB,I   1               4
        JEQ     Q8              4
        JLT     Q7              5
        INC,M   M2              6
        STB,MD  M1              6
Q7      INC,M   MØ              7
        JMP     Q3              7
Q8      CLA                     8
Q9      STB,MD  M1              9
        INC,M   M2              9
        JNE     Q9              9
        LDB,MD  MØ              1Ø
        CPB,I   2               11
        JNE     Q2              11
```

```
*       EXAMPLE 1C
*       MOVE CHARACTERS AND EDIT
*       PDP-8
START   CLA                     1
        DCA     I               1
        DCA     J               1
Q2      TAD     MN              2
        DCA     K               2
Q3      TAD     I               3
        JMS     LDC             3
                A               3
        DCA     X               3
        TAD     X               4
        TAD     MENDL           4
        SNA CLA                 4
        JMP     Q8              4
        TAD     X               5
        SNA                     5
        JMP     Q7              5
        ISZ     J               6
        ISZ     K               6
        JMS     STC             6
                J               6
                B               6
Q7      ISZ     I               7
        JMP     Q3              7
Q8      ISZ     J               9
        JMS     STC             9
                J               9
                B               9
        ISZ     K               9
        JMP     Q8              9
        ISZ     I               1Ø
        TAD     I               11
        JMS     LDC             11
                A               11
        TAD     MENDR           11
        SZA CLA                 11
        JMP     Q2              11


MN              -N
MENDL           -1
MENDR           -2
LDC     Ø
        CLL RAR
        TADI    LDC
        SNL
        JMP     P1
        RTR
        RTR
        RTR
```

```
P1      AND     MR
        ISZ     LDC
        JMPI    LDC
STC     Ø
        DCA     T1
        TADI    STC
        DCA     T2
        TADI    T2
        CLL RAR
        ISZ     STC
        TADI    STC
        DCA     T2
        SNL
        JMP     P2
        CLL
        TAD     T1
        RTL
        RTL
        RTL
        DCA     T1
        TADI    T2
        AND     MR
P3      TAD     T1
        DCAI    T2
        ISZ     STC
        JMPI    STC
P2      TADI    T2
        AND     ML
        JMP     P3

ML              77ØØ
MR              ØØ77
```

```
*       EXAMPLE 1D
*       MOVE CHARACTERS AND EDIT
*       NOVA
START   SUB     Ø,Ø             1
        STA     J               1
        INC     Ø,Ø             1
        STA     I               1
Q2      LDA     KP              2
        STA     K               2
Q3      LDA     1,AADR          3
        LDA     2,I             3
        JSR     LDC             3
        LDA     3,ENDL          4
        SUBN    Ø,3,SNR         4
        JMP     Q8              4
        MOVN    0,0,SNR         5
        JMP     Q7              5
        ISZ     J               6
        DSZ     K               6
        LDA     1,BADR          6
        LDA     2,J             6
        JSR     STC             6
Q7      ISZ     I               7
        JMP     Q3              7
Q8      SUB     Ø,Ø             8
Q9      ISZ     J               9
        LDA     1,BADR          9
        LDA     2,J             9
        JSR     STC             9
        DSZ     K               9
        JMP     Q9              9
        ISZ     I               1Ø
        LDA     1,AADR          11
        LDA     2,I             11
        JSR     LDC             11
        LDA     3,ENDR          11
        SUBN    Ø,3,SZR         11
        JMP     Q2              11
AADR            A
BADR            B
ENDL            1
ENDR            2


KP              N
LDC     MOVZR   2,2
        ADD     1,2
        LDA     Ø,(2)
        MOV     Ø,Ø,SZC
        MOVS    Ø,Ø
        LDA     1,MR
        AND     1,Ø
        JMP     Ø,3
```

```
STC     STA     3,RTN
        MOVZR   2,2
        ADD     1,2
        LDA     1,(2)
        MOV     Ø,Ø,SZC
        JMP     P1
        LDA     3,ML
P2      AND     3,1
        ADD     Ø,1
        STA     1,(2)
        JMPI    RTN
P1      MOVS    Ø,Ø
        LDA     3,MR
        JMP     P2
ML              1774ØØ
MR              377
```

```
*       EXAMPLE 2A,B
*       MULTIPLY
*       PDP-11
MPY     CLA                     1
        STW,M   MØ              1
        LDW,XD  (1)             1
        STW,M   M1              1
        LDB,I   2Ø              1
        STW,M   M2              1
Q2      LDW,M   M1              2
        RAR                     2
        JLR     Q4+1            2
        LDW,M   MØ              3
        ADW,X   2(1)            3
        STW,M   MØ              3
Q4      CLL                     4
        LDW,M   MØ              4
        RAR                     4
        STW,M   MØ              4
        LDW,M   M1              4
        RAR                     4
        STW,M   M1              4
        DEC,M   M2              4
        JNE     Q2              4
        LDW,X   4(1)            Ø
        STW,M   M2              Ø
        LDW,M   MØ              Ø
        STW,MD  M2              Ø
        LDW,M   M1              Ø
        STW,MD  M2              Ø
        JMP     6(1)            Ø
```

```
*       EXAMPLE 2C
*       MULTIPLY
*       PDP-8
MPY     Ø                       1
        DCA     XL              1
        TADI    MPY             1
        DCA     T1              1
        TADI    T1              1
        DCA     XR              1
        ISZ     MPY             1
        TADI    MPY             1

        DCA     BADR            1
        TAD     M16             1
        DCA     T1              1
Q2      TAD     XR              2
        RAR                     2
        SNL CLA                 2
        JMP     Q4+1            2
        TADI    BADR            3
        TAD     XL              3
        DCA     XL              3

Q4      TAD     XL              4
        CLL RAR                 4
        DCA     XL              4
        TAD     XR              4
        RAR                     4
        DCA     XR              4
        ISZ     T1              4
        JMP     Q2              5
        ISZ     MPY             Ø
        TADI    MPY             Ø
        DCA     AUTØ/           Ø
        TAD     XL              Ø
        DCAI    AUTØ            Ø
        TAD     XR              Ø
        DCAI    AUTØ            Ø
        ISZ     MPY             Ø
        JMPI    MPY             Ø
M16             -2Ø
```

```
*       EXAMPLE 2D
*       MULTIPLY
*       NOVA
MPY     LDA     Ø,M16           1
        STA     Ø,I             1
        LDAI    1,(3)           1
        LDAI    2,1(3)          1
        SUB     Ø,Ø             1
Q2      MOVRM   1,Ø,SZC         2
        ADD     B,Ø             3
        MOVZR   Ø,Ø             4
        MOVR    1,1             4
        ISZ     I               5
        IMP     Q2              5
        LDA     2,2(3)          Ø
        STA     2,AUTØ          Ø
        STAI    Ø,AUTØ          Ø
        STAI    1,AUTØ          Ø
        JMP     3,(3)           Ø
M16             -2Ø
```

```
*       EXAMPLE 3A,B
*       TOLERANCE CHECK
*       PDP-11
TOL     LDW,XD  (1)             1
        NEG                     1
        STW,M   MØ              1
        LDW,X   2(1)            1
        STW,M   M1              1
Q2      LDW,MD  M1              3
        CPW,XD  4(1)            3
        JLT     Q7              3
        CPW,XD  6(1)            4
        JGT     Q7              4
        INC,M   MØ              5
        JNE     Q2              5
        CLA                     6
Z1      STW,XD  1Ø(1)           6
        JMP     12(1)           6
Q7      LDW,M   MØ              7
        ADW,X   (1)             7
        INA                     7
        JMP     Z1              7
```

```
*       EXAMPLE 3C
*       TOLERANCE CHECK
*       PDP-8
TOL     Ø
        CMA                     1
        TAD     TOL             1
        DCA     AUTØ            1
        TADI    AUTØ            1
        DCA     IP              1
        TADI    IP              1
        CIA                     1
        DCA     IP              1
        TADI    AUTØ            1
        DCA     AADR            1
        TADI    AUTØ            1
        DCA     XADR            1
        TADI    AUTØ            1
        DCA     YADR            1
        TADI    AUTØ            1
        DCA     KADR            1
        INA                     1
        DCAI    KADR            1
Q2      TADI    XADR            3
        CIA                     3
        TADI    AADR            3
        SPA CLA                 3
        JMP     Q7              3
        TADI    AADR            4
        CIA                     4
        TADI    YADR            4
        SPA CLA                 4
        JMP     Q7              4
        ISZ     AADR            5
        ISZI    KADR            5
        ISZ     IP              5
        JMP     Q2              5
        DCAI    KADR            6
Q7      JMPI    AUTØ            6
```

```
*       EXAMPLE 3D
*       TOLERANCE CHECK
*       NOVA
TOL     LDAI    Ø,(3)           1
        STA     I               1
        LDA     Ø,1(3)          1
        STA     Ø,AUTØ          1
        LDAI    1,2(3)          1
        LDAI    2,3(3)          1
        LDA     Ø,K1            1
        STA     Ø,4(3)          1
Q2      LDAI    AUTØ            3
        SUBNZ   1,Ø,SZC         3
        JMP     Q7              3
        SUBNZ   Ø,2,SZC         4
        JMP     Q7              4
        ISZI    4(3)            5
        DSZ     I               5
        JMP     Q2              5
        SUB     Ø,Ø             6
        STAI    Ø,4(3)          6
Q7      JMP     5(3)            6
K1              1
```

```
*       EXAMPLE4A,B
*       HISTOGRAM
*       PDP-11
START   LDW,I   B               1
        STW,M   MØ              1
        LDB,I   1ØØ             1
        STW,M   M1              1
        CLA                     1
Q2      STW,MD  MØ              3
        DEC,M   M1              3
        JNE     Q2              3
        LDW,I   A               4
        STW,M   MØ              4
        LDW,I   1ØØØ            4
        STW,M   M1              4
        LDW,I   B-1             4
        STW,L   XØ              4
Q5      LDW,MD  MØ              6
        JLE     Q1Ø             7
        CPW,I   1ØØ             8
        JGT     Q1Ø             8
        STB,R   .+2             9
        INC,X   Ø(Ø)            9
        DEC,M   M1              1Ø
        JNE     Q5              1Ø
```

```
*       EXAMPLE4C
*       HISTOGRAM
*       PDP-8
START   CLA                     1
        TAD     BADR            1
        DCA     AUTØ            1
        TAD     M1ØØ            1
        DCA     I               1
Q2      DCAI    AUTØ            3
        ISZ     I               3
        JMP     Q2              3
        TAD     M1ØØØ           4
        DCA     J               4
        TAD     AADR            4
        DCA     AUTØ            4
Q5      TADI    AUTØ            6
        CIA                     7
        SNA                     7
        JMP     Q1Ø             7
        CIA                     8
        TAD     M1Ø1            8
        SMA                     8
        JMP     Q1Ø             8
        TAD     BP              9
        DCA     T1              9
        ISZI    T1              9
Q1Ø     ISZ     J               1Ø
        JMP     Q5              1Ø
AADR            A
BADR            B
BP              B+144
M1ØØ            -144
M1Ø1            -145
M1ØØØ           -175Ø
```

```
*       EXAMPLE 4D
*       HISTOGRAM
*       NOVA
START   LDA     Ø,AADR          1
        STW     Ø,AUTØ          1
        LDA     Ø,M1ØØ          1
        SUB     1,1             1
Q2      STAI    1,AUTØ          3
        INC     Ø,Ø,SZR         3
        JMP     Q2              3
        LDA     Ø,AADR          4
        STA     Ø,AUTØ          4
        LDA     1,P1ØØ          4
        LDA     Ø,BADR          4
        LDA     3,M1ØØØ         4
Q5      LDAI    2,AUTØ          6
        NEGZN   2,2,SNC         7
        JMP     Q1Ø             7
        NEGZN   2,1,SZC         8
        JMP     Q1Ø             8
        ADD     Ø,2             9
        ISZ     (2)             9
Q1Ø     INC     3,3,SZR         1Ø
        JMP     Q5              1Ø
AADR            A
BADR            B-1
P1ØØ            144
M1ØØØ           -175Ø
```

```
*       EXAMPLE 5A,B
*       DECIMAL TO BINARY
*       PDP-11
START   LDW,I   A               1
        STW,M   MØ              1
        LDB,I   6               1
        STW,M   M1              1
        CLA                     1
        STW,M   M2              1
Q2      LDW,M   M2              4
        CLL                     4
        RAL                     4
        RAL                     4
        RAL                     4
        ADW,M   M2              4
        ADW,M   M2              4
        STW,M   M2              4
        LDW,MD  MØ              3
        ANB,I   17              3
        ADW,M   M2              4
        STW,M   M2              4
        DEC,M   M1              4
        JNE     Q2              4
```

```
*       EXAMPLE 5C
*       DECIMAL TO BINARY
*       PDP-8
START   TAD     M6              1
        DCA     IP              1
        DCA     I               1
        DCA     K               1
Q2      TAD     K               4
        CLL RTL                 4
        RAL                     4
        TAD     K               4
        TAD     K               4
        DCA     K               4
        TAD     I               3
        JMS     LDC             3
                A               3
        AND     MSK             3
        TAD     K               4
        DCA     K               4
        ISZ     I               4
        ISZ     IP              4
        JMP     Q2              4
M6              -6
MSK             17
```

```
*       EXAMPLE 5D
*       DECIMAL TO BINARY
*       NOVA
START   SUB     Ø,Ø             1
        STA     Ø,K             1
        STA     Ø,I             1
        LDA     Ø,P6            1
        STA     Ø,IP            1
Q2      LDA     1,AADR          3
        LDA     2,I             3
        JSR     LDC             3
        LDA     1,MSK           3
        AND     1,0             3
        LDA     1,K             4
        MOVZL   1,1             4
        MOVZL   1,2             4
        MOVZL   2,2             4
        ADD     1,2             4
        ADD     Ø,2             4
        STA     2,K             4
        ISZ     I               4
        DSZ     IP              4
        JMP     Q2              4
AADR            A
P6              6
MSK             17
```

Comparison of PDP-11, PDP-8 and the NOVA
Appendix B. Detailed Cycle Counts

Example 1

	PDP-11A		PDP-11B		PDP-8		NOVA	
box	freq	ct	tot	ct	tot	ct	ct	tot
0	1	0	0	0	0	0	0	0
1	1	4	4	8	8	5	8	8
2	10	2	20	4	40	4	4	40
3	300	1	300	2	600	23	13	3900
4	300	2	600	4	1200	6	5	1500
5	300	1	300	2	600	4	3	900
6	200	2	400	3	600	43	24	4800
7	300	2	600	3	900	3	3	900
8	700	0	0	1	700	0	2	1400
9	700	3	2100	5	3500	44	25	17500
10	10	1	10	2	20	2	2	20
11	10	3	30	4	40	21	19	190
			4264		8208			31158

Example 2

	PDP-11A		PDP-11B		PDP-8		NOVA	
box	freq	ct	tot	ct	tot	ct	ct	tot
0	1	8	8	15	15	21	11	11
1	1	5	5	10	15	23	12	12
2	16	2	32	4	64	5	2	32
3	8	3	24	6	48	7	2	16
4	16	5	80	10	160	12	4	64
			149		297			135

Example 3

box	freq	PDP-11A ct	PDP-11A tot	PDP-11B ct	PDP-11B tot	PDP-8 ct	PDP-8 tot	NOVA ct	NOVA tot
0	1	0	0	0	0	0	0	0	0
1	1	7	7	13	13	39	39	19	19
2	100	0	0	0	0	0	0	0	0
3	100	6	600	11	1100	9	900	6	600
4	100	4	400	8	800	9	900	3	300
5	100	2	200	3	300	8	800	6	600
6	1	5	5	9	9	5	5	6	6
7	0	5	0	8	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0
			1212		2222		2644		1525

Example 4

box	freq	PDP-11A ct	PDP-11A tot	PDP-11B ct	PDP-11B tot	PDP-8 ct	PDP-8 tot	NOVA ct	NOVA tot
0	1	0	0	0	0	0	0	0	0
1	1	5	5	9	9	9	9	8	8
2	100	0	0	0	0	0	0	0	0
3	100	4	400	6	600	6	600	6	600
4	1	7	7	13	13	8	8	10	10
5	1000	0	0	0	0	0	0	0	0
6	1000	2	2000	3	3000	3	3000	3	3000
7	1000	2	2000	2	2000	3	3000	3	3000
8	1000	2	2000	5	5000	5	5000	3	3000
9	1000	4	4000	7	7000	7	7000	4	4000
10	1000	2	2000	3	3000	3	3000	3	3000
			12412		20622		21617		16618

Example 5

box	freq	PDP-11A ct	PDP-11A tot	PDP-11B ct	PDP-11B tot	PDP-8 ct	PDP-8 tot	NOVA ct	NOVA tot
0	0	0	0	0	0	0	0	0	0
1	1	4	4	8	8	8	8	10	10
2	5	0	0	0	0	0	0	0	0
3	5	3	15	5	25	19	95	17	85
4	5	6	30	13	65	19	95	19	95
			49		98		198		190

(Includes Participation Either Wholly or Partial)

	US	Europe	Other②	Total
Modules	25	8	8	41
8 Family①	54	13	5	72
9	8	7	—	15
10	3	2	2	7
12	18	3	—	21
TPL	2	—	—	2

8 Family includes Numerical Control, Typesetting, Education

Other = Canada & Asia

CHART #2 = NUMBER OF SHOWS EACH MONTH by CLASS OF SHOWS (...①)

MONTH	A	B	C	D	TOTAL	U.S.	EUROPE	OTH
JAN	+	1	4	1	6	3	1	2
FEB	—	2	3	1	6	4	1	1
MAR	2	4	2	5	13	9	4	—
APRIL	1	3	4	3	11	9	1	1
MAY	1	3	6	2	12	9	1	2
JUNE	—	2	2	1	5	3	1	1
July	=	—	=	=	=	=	=	=
AUGUST	2	—	1	2	5	4	1	+
SEPT	2	3	+	—	6	3	3	=
OCT	—	4	2	1	7	4	2	1
NOV	1	2	1	2	6	6	—	—
DEC	—	—	—	2	2	2	—	
TOTAL	9	25	26	20	79	56	15	8

①

A=. MAJOR Show, Cross product with Equip Displayed > 20' OF SPACE > 20,000 ATTEN. > $15,0

B= MAJOR Show, Cross product, with Equipn Displayed < 20' OF Space 10-25,000 ATTENDANCE $5-$15,00
(Might Be VERTICAL MARKET)

C = Small Regional Shows - 10' OF SPACE, Computer displayed < 5,000 ATTENDANCE. COST $5,000

D = SAME AS "C" BUT NO Equip.—

Chart #3 = Number & Classification of Shows
By Region

Region	A	B	C	D	Total
N.E.R	1	1	—	2	4
M.A.R.	1	4	6	7	18
C.R.O	1	6	3	9	19
W.R.O.	2		8	3	15.
Canada			8		8
Europe	3	12			15
Total	8	23	25	21	77

Does not include 2 shows in Japan

Chart #4 = This Shows Product Line Participation in Trade Shows in our Various Markets -

Note - Total Column Shows Number of Shows we Partic in That Market.

Market	M	8	9	10	12	To
Biomedical	5	16	4	—	11	16
Physics	—	2	2	—	—	2
Typsetting	—	4	—	—	—	4
Numerical Control	2	2	—	—	—	2
Analy Chemistry	2	8	1	1	2	10
Education	21	21	—	—	—	21
Elec & Inst	16	16	1	—	—	16
Communications	—	1	—	—	—	1
Computer	—	2	2	2	2	2
Oceanological	—	1	—	—	—	1
Total	45	73	10	3	14	75

Chi, J S — This Chart Shows [illegible] Estimated Participation From Cost
out of CC 153 And Break down by Product Line. See Note 1 B
1 Also Does NOT include European Shows which are Budgeted By Eu

PL

MARKET	m	8	9	10	12	TOTAL
Bio Med		13.5 K	4.2 K		16.5 K	34.2
Physics		2.8 K	4.8 K			7.6 K
Typesetting		9.4 K				9.4 K
Numerical Control	1.2 K	3.3 K				4.5 K
Analy. Chemistry	1.8 K	14.5 K	3.8 K		2.5 K	22.6 K
Education	6.0 K	9.0 K				15.0 K
Elec. & Inst.	28.0 K	10.5 K	5.0 K		.5 K	44.0 K
Communications		1.5 K				1.5 K
Computer		10.3 K	13.0 K	13.0 K		36.3 K
Oceanological						
TOTAL	37.0 K	74.8 K	30.8	13.0	19.5	175.1 K

Note ① CC 153 Expenses include only Cost for Booth Space, Shipping, Service Charges @ Show. And any Expenses incurred by members of CC 153. Does NOT include individual

INTEROFFICE MEMORANDUM

DATE: January 22, 1969

SUBJECT: CORPORATE PRESS CONFERENCE

TO: Ken Olsen

FROM: Mark Nigberg

cc: Operations Committee
Gabe d'Annunzio

If we may paraphrase our previous memo on the Corporate Press Conference:

Because the PDP-11 announcement will have such a major impact in the industry, we believe it is essential that a clear, uncluttered impression of what we are doing is presented to the public.

We understand DEC will introduce a number of new products, in addition to the PDP-11, during the next few months--PDP-14, the PDP-15, Indac-8, NMR-8, and a new graphics system.

As a leading force in the computer industry, all of our product introductions are of major importance to the public. However, we can easily confuse our customers and potential customers if these announcements are made haphazardly to a press that does not understand what DEC is doing nor why. Unless these announcements are closely coordinated, we believe DEC will not emerge with a clear, understandable message in the marketplace, nor will our new products appear to be part of a comprehensive and well-defined computer line.

Therefore, we recommend that, instead of announcing the PDP-11, PDP-14, PDP-15, Indac-8, and other products separately, we hold a single news conference to announce these products, putting them into the context of DEC's total product spectrum, and explaining why we offer them.

The Pitch

Ever since we suggested this approach to announcing our products, there has been a basic question in the minds of those to whom we've talked. Is there really a way to tie all of DEC's products together? We believe there is, and the following is the way we propose we do it:

DEC offers the most comprehensive line of computing equipment available today. From its building block logic modules to its large time sharing systems, the DEC product line is designed to provide a spectrum of alternatives from which a customer can chose to solve his particular computer-oriented problem.

The DEC product line did not emerge overnight. It has gone through more than a decade of careful planning and development. A decade in which DEC has learned that no single size computer, no single word length can offer a universal solution. A decade in which DEC has learned that a computer manufacturer must provide a customer with more than a basic computer mainframe; it must offer a range of interfacing and peripheral equipment, easy-to-use and efficient software packages, and reliable, worldwide service and support.

DEC has also learned to view computer markets in two ways. It has learned that one segment of its markets is concerned with the specific computer specifications of its comprehensive line of equipment. Another segment seeks packaged solutions. They do not ask about mainframe price/performance, memory size, bytes, or bits. They ask about the price/performance of their particular problem/solution and they want the answers in a language they understand.

The DEC product line reflects this two-pronged approach. We have built a variety of basic mainframes, the 8, 9, and 10, and two new mainframes, the 11 and 15, which will be introduced today. We have also introduced computer-based systems designed for specific markets: The PDP-12, our general-purpose laboratory computer; Time Share-8, our small time sharing computer; the 680/A, our message switching and concentration system. During the past six months alone, we have introduced special systems for clinical, chemical, and physics laboratories, the metalworking industry, typesetting, education, engineering, and satellite navigation. Today, we will be introducing more market-oriented systems: The PDP-14, a new, special purpose computer that fills the gap between modules and general purpose computers in the machine control market; Indac-8, a new system designed for industrial process control; a graphics system which opens up a wide new market for computer-based displays, and NMR-8, a data acquisition and analysis system for nuclear magnetic resonance spectrometry. In addition, we have worked closely with system houses and manufacturers of all types of business, industrial, and scientific equipment so that today we can safely say that a DEC computer is at work in almost every conceivable computer application.

Conference Agenda

We would like to hold a two-session conference. During the first session, the president would provide the overview. He would describe who we are, where we are, and where we are going. This would be followed by the pitch--how we intend to get there, and what services we offer. We strongly recommend stressing the service aspects of our company's approach to its markets.

After Ken has concluded his remarks, we will have a brief question and answer period followed by lunch.

After lunch, the press will be escorted to another location where all of our new products will be on display. Ken will again provide the overview for the new product introductions.

Each product will be manned by an appropriate product representative, and the second part of the press conference will turn into an "Un-joint Computer Conference."*

Members of the PR staff will be available to discuss future articles with the editors. A complete press kit including a summary of Ken's remarks, plus product info will be given out at the beginning of the conference.

Timing and Location

We propose having the press conference at a centrally located New York City hotel on April 14 beginning at 10 a.m. and concluding at approximately 3 p.m. Ken has suggested the possibility

of locating an appropriate conference and display room in the Coliseum. This would certainly add some impact to the event. He has also suggested that this might be an appropriate time and place to display our entire array of products. This also would provide a much more impressive view of DEC.

We propose inviting approximately 100 members of the general, financial, and trade press. We would like you to present an overview of the company and our product lines, putting our new products into the correct frames of reference. We would also like to have representatives of our new product lines available to answer questions.

Because of the importance of this conference and the time factors involved, I would appreciate the opportunity of discussing this plan with you in greater detail as soon as possible.

MN/sf

*An expression borrowed from Ken Olsen

digital INTEROFFICE MEMORANDUM

DATE: January 20, 1969

SUBJECT: FINANCIAL AND CONSULTANT RELATIONS PROPOSAL

TO: Ken Olsen

FROM: Mark Nigberg

cc: Operations Committee
Gabe d'Annunzio

In most companies, the Public Relations function takes on new dimensions as the company grows and prospers. For example, when DEC entered the computer market, it was concerned with building a broad publicity cover for the company's products. As DEC developed a reputation in its specific vertical markets, PR began to broaden the range of its publicity cover to defining the company's position in these markets. In the main, during this entire period, the primary audience which PR attempted to reach was our customers and prospects.

However, as the company continues to grow, new publics are added. Increased employment produced employees with which the company must communicate; as the company became a greater economic and social influence, the community became a public. When we began offering our stock on the American Exchange, the financial community became a public; as DEC takes its place as a major industrial influence, business management and industrial consultants will become important publics.

We have developed what we believe is the multi-faceted role of PR in this proposal for consultant and financial relations activities, because we believe that the most effective approach DEC could take in terms of PR is to build an integrated, well-executed program in which all PR activities are joined together. This is a subject which we believe the Operations Committee should consider in evaluating how this proposal might be implemented.

Financial Relations Proposal

In defining financial relations, we first established that there were essentially three financial publics with which the company is now concerned:

1. Financial Analysts
2. Financial Press
3. Stockholders

Security analysts are vitally interested in DEC and where we are going. The analysts we have talked to want to know and understand our management approach; they want to see our facilities; they want to know all about our products, our markets, our financial condition, and our research and development programs. Of course, they do not want a "snow job." Overpromoting is quickly spotted by a good analyst. As far as an analyst is concerned, this sin is as bad as the other extreme--underpromoting the DEC story.

-more-

Here are some of the things my group would like to implement with the approval of the Operations Committee:

1. We would like to set up a regular program to invite analysts to visit our plant.

2. Wall Street is interested not only in financial figures, but also in basic company news, such as expansion of facilities, new products, and top management changes. Releases of this type will be sent to selected security analysts. We will also send them our monthly DIGITAL NEWSLETTER. Quarterly Earnings Statements, and our Annual Report. 1/2 year

3. In many major cities, security analysts have an association which meets regularly. These groups usually invite top management people from publicly held companies to make presentations. We would like to be able to call on members of the Operations Committee to speak at these gatherings on occasion. Copies of the talk could then be sent to other security analysts. Keep down

4. Many securities analysts like to meet occasionally with company officials on an informal, off-the-record basis. Off-the-record, in the case of a security analyst, means that he will not quote the individual from whom he obtained information. It does not mean--and securities analysts are usually honest about this--that he will not use the information in evaluating stocks either in written reports or verbally.

5. Security analysts, of course, want information about bad news. If problems are explained to them with honesty and forthrightness, they usually understand the situation. Often, security analysts can be of help in cushioning the financial community against the shock of bad news. For example, if some untoward event occurs in a company that will have a temporary negative effect on sales or profits, but not a permanent one, security analysts can help prevent unnecessary activity in sale and purchase of the stock.

6. The same laws and rules covering publicity activities on stock issues are particularly applicable to security analysts. It is just as wrong to push an upcoming stock in private meetings with security analysts as it is to promote the stock with premature publicity. Also, we do not intend to give security analysts advance information about company news. Wall Street is like a party line as far as "inside" information is concerned. Rumors and "reports" based on prematurely disclosed information crackle over the "grapevine" almost unimaginably fast. This is the reason, of course, that the SEC and the stock exchanges insist on immediate disclosure of information that will affect the stock market.

We propose taking a similar approach with the financial press. In addition, we would also like to include in our Financial Relations Program the following:

1. Greetings to new shareholders. We would like to make DEC shareholders feel they are part of the corporate family. We would send letters of welcome to new shareholders, along with product brochures, the latest annual and quarterly reports, and other information

2. We would propose going beyond financial figures in preparing quarterly reports. We propose sending a quarterly newsletter giving all important news that has occurred during the previous three months.

3. Our annual meeting is attracting stockholders in increasing numbers; of course, not nearly all of the shareholders are able to attend most meetings. This is due, of course, to the geographical spread of our shareholders. To meet this need, we propose preparing a post-meeting report. This report will relate the official business which was transacted at the annual meeting.

We believe a comprehensive, well-directed Financial Relations Program will produce immeasurably important results in good will and understanding for the Company. We believe this program should be administered within the Public Relations Group under the guidance of the President and Vice President for Finance, with the counselling of the rest of the Operations Committee. We anticipate no immediate manpower increase required for this program. It is probable, however, that one man may be required in FY 1970.

Consultant Relations Proposal

In determining what approach we should recommend for DEC's consultant relations activity, it soon became apparent that a great deal of what we would propose would really apply to several important publics. These include:

1. Consultants
2. System Houses
3. Service Bureaus
4. OEMs

The common denominators for all of these groups is that they all have a major influence on the buying decision for our products; they are all indirect DEC salesmen, and therefore should be aware of our development programs and marketing plans as are our salesmen: and they are all concerned with specific technical details as well as general corporate information.

Here are some of the things my group would like to implement with the approval of the Operations Committee:

1. We would like to set up a regular program to invite consultants to visit our plant.

2. All of these groups are concerned with facts--not fancy. We would therefore propose providing them with well-written technical documentation on our products, including summary specifications, benchmarks, and application notes. A series of option bulletins and technical flyers for all product lines is presently under development by the Sales Promotion Group. These could be given to consultants with little or no modification.

-more-

3. These groups are also interested in general company news. We would send them our monthly DIGITAL NEWSLETTER and Annual Report. In addition, we propose sending information on new developments with the specific approval of the appropriate Group Vice President

4. We would like to work closely with DECUS in developing seminars of interest to these groups.

5. We would like to work closely with product lines in developing workshops.

We believe a program of the type recommended will produce tangible results, changing brand recognition into brand preference.

The major cost of this program for the first six months will be manpower. We would need a fulltime man, plus support from other groups in the Advertising and Sales Promotion Department, to implement this program. For FY 1970, we would require an additional man to develop consultant documentation.

A direct benefit of this program is that a great deal of information developed through this program could easily be used by the sales forces.

MNsf

Start slow doing things

OPERATIONS COMMITTEE MEETING

January 20, 1969

AGENDA

1. Additions and Corrections to Minutes of the January 13th and 14th Meetings.
2. Marketing Review Committee Summary - (Ted Johnson)
   (See attached minutes of the January 14th meeting)
3. Salary Reviews - (Ted Johnson)
   (Sales people not reviewed at the SRC meeting on Wednesday)
4. Relocation Expenses for Gerry Moore - (Ted Johnson)
   (See attached report from Graydon Thayer)
5. Discussion of FJCC, SJCC and IEEE - (Roy Gould/Dave Cotton/Bob McInnes)
6. Trade Show Schedule for 1969 - (Roy Gould)
   (See attached report)
7. Plans for the Security Analysts Meeting on January 29th - (Phil Markell)
   (See attached report)
8. Cross-Product Line Marketing Reporting System - (Ed Savage/Mike Dowling)
   (See attached report)
9. Press Conference for New Product Announcements
   (See attached report from Mark Nigberg)
10. Corporate Communications Program
    (See attached report from Mark Nigberg)
11. Proposed Relocation of the Print Shop - (Nick LoRusso)
    (See attached report)

THE NEXT "WOODS" MEETING IS SCHEDULED FOR THE AFTERNOON OF FEBRUARY 12TH AND ALL DAY THE 13TH

MINUTES OF OPERATIONS COMMITTEE

January 20, 1969

Present: K. Olsen, P. Kaufmann - Secretary, S. Olsen, W. Hindle, T. Johnson

Absent: N. Mazzarese

1. The minutes of January 13 and January 14 meetings were approved.

2. Marketing Review Committee

Ken suggested that the Marketing Review Committee must take responsibility and a stronger managerial approach to decision making. They seem to only discuss and criticize issues and take no executive action in areas where they should like Trade Shows. The Marketing Committee will review their charter and recommend through Ted at next week's Operation Committee what their function should be, where it is executive function and where it is a review function.

3. Trade Shows

Roy Gould, Dave Cotton, Bob McInnes

Trade shows should be reviewed prior to January 1. There are 96 shows requested by Marketing Managers and Product Line Managers. The list should be collated by the Marketing group and costs of the shows should be estimated. The local sales office should be involved in the planning of the show and work with the one Marketing man who is responsible for that particular show. The number of shows we attend must be reduced, as must the dollars we spend. Our booth needs should be simple. The SJCC could be either an island or a linear booth. A decision must be made this week. We constantly change our minds regarding what we want and it is necessary to standardize our desires. The Marketing Committee will review the number of shows, the dollar cost and assign a man to be responsible for each one.

Bob McInnes suggested that we can split Trade Shows by having some of them local shows, completely supported by the district field sales office.

4. Relocation Expenses - Gerry Moore

The interest on Gerry's loan for purchase of a house in Chicago was approved. Also, the relocation policy will apply one year later in this case.

5. Security Analyst Meeting

Ken Olsen and Pete Kaufmann will take responsibility for the tour route. Pete Kaufmann will take a dry run with tour guides selected and talk about what to say. Win Hindle and Ken Olsen will give talks to the

Security Analysts. Ken will decide where lunch will be served. Each Vice President will assure his areas are clean, orderly and neat.

6. Cross Product Line Marketing Report System

A question in this reporting system is sub-product reporting vs cross-product marketing. The general feeling is that we should collect information on both sub-products and cross-product marketing.

7. Press Conference - New Product Announcements

Mark Nigberg will present consistent pitch on new product announcements to the Operations Committee next week.

8. Corporate Communications Program

This communication between financial analysts, computer consultants, system houses time-share utilities and top management of our important customers seems like a good idea. Mark Nigberg will submit a plan and budget for this program next week. Ted Johnson suggested that we make a list of consultants and each Vice President assume a piece of this marketing responsibility.

9. Relocation of the Print Shop

The proposal was approved in principal.

10. PDP-11 Announcement

Ken would like the announcement of the PDP-11 to leak out and not be formally announced like this. No delivery commitments, no price commitment and no orders will be taken. The effect this has on the PDP-8 and 9 must be a positive one, not a negative force in the market. The purpose should be to stimulate the PDP-8 and 9 sales and give the impression that we are developing new equipment, which is faster and better than any of our competition.

11. Shipments

Third quarter shipments were estimated to be 5.634 under the present budget by Pete Kaufmann.

12. Salary Reviews - T. Johnson

jb

digital INTEROFFICE MEMORANDUM

DATE: January 15, 1969

SUBJECT: Trade Shows 1969

TO: Ted Johnson
Win Hindle
Stan Olsen
Ken Olsen ✓

FROM: Roy Gould

cc: Ron Smart

Attached is the proposed Trade Show Schedule for calendar 1969. The person requesting each show appears under the show. The European list shows Steve Bower's name and these shows were approved at a recent European Regional Meeting.

This list does not include ~~ten more~~ additional education shows (National Council Teachers of Math and American Math Society Meetings) which was just given to me by Bob Allison, PDP-8 Educational Marketing. Also, I am quite sure that there will be another fifteen shows requested by various people that we attend throughout the year.

This list is incredible. In March and April alone there are eighteen shows in the United States. I know that I cannot support this many shows throughout the year, and I am quite sure that the product lines cannot support this number of shows with equipment.

I feel, with the exception of small educational shows, that we should always have a piece of working equipment at a Trade Show.

By the way that people are requesting Trade Shows shows to me that they are not taking serious thought into what they are committing the Company to in terms of dollars and image in the industry. Even the smallest of shows requires a good deal of work from my area, Field Sales, and Field Service.

Let us take a far more serious approach to our Trade Show effort for this year and the future.

This schedule is in the hands of your Product Line Managers, and is scheduled to be discussed at the next Marketing Review Committee Meeting, January 21.

jac
Attachments

SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIELD
BRITISH MED COMP SOCIETY Steve Bowers	BIRMINGHAM, ENGLAND	JAN 6-10					
GR LAKES NEWSP MECHANICAL Marv Cothran	TORONTO, CANADA	JAN 11-14		800	20'		
BRAIN DOCTORS' CONFERENCE Harold Leaman	ASPEN, COLORADO	JAN 12-17		300	10'		
FIFTH INT'L SYMPOSIUM Brad Dewey	LAS VEGAS, NEVADA	JAN 20-23		1,000	20'		
CANADIAN EDUCATION SHOW John Hughes	TORONTO, CANADA	JAN 23-25		16,000	10'		
NCTM Bob Allison	NEW ORLEANS	JAN 24-26		5,000			
PHYSICS	NEW YORK	FEB 3-6		10,000	30'		
ONTARIO PSYCHOLOGICAL Frank Ollie	TORONTO, CANADA	FEB 6-7		1,000			
~~AM ASSO OF SCH ADMINISTRATORS Bob Allison~~	~~ATLANTIC CITY, N.J.~~	~~FEB 15-19~~		~~33,000~~			

	SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIELI
))	GRAPHIC ARTS Steve Bowers	FRANKFORT, GERMANY	FEB 17-21					
.)	OCEANOLOGY INTERNATIONAL Steve Bowers	BRIGHTON, ENGLAND	FEB 18-21					
!)	NCTM Bob Allison	L. ANGELES, CALIFORNIA	FEB 21-23		5,000			
1)	NEUROELECTRIC CONFERENCE Mort Ruderman	SAN FRAN., CALIFORNIA	FEB 26-28		1,000	20'		
4)	AM COL OF CARDIOLOGY Mort Ruderman	NEW YORK	FEB 27-MAR 1		3,000			
5)	NAT'L ASSO SECONDARY SCHOOL PRINCIPALS Bob Allison	SAN FRAN., CALIFORNIA	MAR 1-5		15,000	20'		
6)	AM RESEARCH & DEVELOPMENT	BOSTON, MASS.	MAR 5			30'		
7)	NAT'L ASSO INDEPENDENT SCHOOLS Bob Allison	NEW YORK	MAR 2-4		1,000	10'		
8)	PITTSBURGH CONFERENCE Brad Dewey	CLEVELAND, OHIO	MAR 3-7		7,500	60'		

SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIEL
INT'L EXH OF INDUSTRIAL ELECTRONICS Steve Bowers	BASEL, SWITZERLAND	MAR 4-8					
INT'L MEDICAL ENGINEERING & AUTOMATION Steve Bowers	LONDON, ENGLAND	MAR 10-14					
ASSO FOR SUPERVISION & CURRICULUM DEVELOPMENT Bob Pouliot	CHICAGO, ILLINOIS	MAR 16-20		5,200	10'		
NSTA Bob Allison	DALLAS, TEXAS	MAR 21-25		5,000	10'		
ST MORITZ CONFERENCE Mort Ruderman	SWITZERLAND	MAR 24-26			Loan of machine by Mort Ruderman		
IEEE	NEW YORK	MAR 24-27		50,000	80'		
LABEX Steve Bowers	LONDON, ENGLAND	MAR 25-29					
MID-ATLANTIC NEWSPAPER MECHANICAL CONFERENCE Marv Cothran	PITTSBURGH, PENN.	MAR 27-29		1,000	20'		
FIFTH FLINTRIDGE CONF. John Leng	PASADENA, CALIFORNIA	MAR 28-29					

SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FI
28) INT'L EXHIBITION OF ELECTRONIC COMPUTERS Steve Bowers	PARIS, FRANCE	MAR 28-APR 2					
29) ~~ANPA~~ ~~Marv Cothran~~	~~NEW YORK~~	~~APR~~					
30) NAT'L CATHOLIC EDUCATION ASSOCIATION Bob Allison	DETROIT, MICHIGAN	APR 7-10		15,000	10'		
31) CECON Bob Hughes	CLEVELAND, OHIO	APR 8-10		1,000	20'		
32) EASTERN PSYCHOLOGICAL ASSOCIATION Mort Ruderman	PHILADELPHIA PENN.	APR 10-12		3,500			
33) NATIONAL SCHOOL BOARDS Bob Allison	MIAMI, FLORIDA	APR 12-15		10,000	10'		
34) QUEBEC EDUCATION Frank Ollie	MONTREAL, CANADA	APR 10-12					
35) AUTOMATED MANUFACTURING PROCESSING PRODUCTION Stan Olsen	CINCINNATI, OHIO	APR 14-17		10,000	20' x 15'		
36) FASEB MORT RUDERMAN	ATLANTIC CITY, N.J.	APR 14-18		23,000	40'		

	SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIEI
7)	~~INSTRUMENTS EXHIBITION~~ ~~Steve Bowers~~	~~BRUSSELS, ENGLAND~~	~~APR 14-23~~					
8)	COLLEGE OF ENGINEERING EXPOSITION Mort Ruderman	MADISON, WISCONSIN	APR 18-20		1,000	20'		
9)	AM COL OF PHYSICIANS Mort Ruderman	CHICAGO, ILLINOIS	APR 20-24		3,500	20'		
0)	~~INT'L PETROLEUM ENGR EXPOSITION~~ ~~Steve Bowers~~	~~LONDON, ENGLAND~~	~~APR 22-30~~					
1)	~~SWIEEECO~~ ~~Tony Liveris~~	~~SAN ANTONIO, TEXAS~~	~~APR 23-25~~		~~1,000~~	~~20~~'		
2)	NCTM Bob Allison	MINNEAPOLIS, MINNESOTA	APR 23-26		5,000	30'		
3)	HANNOVER FAIR Steve Bowers	HANNOVER, GERMANY	APR 26-MAY 4					
4)	AM SOCIETY FOR CLINICAL INVESTIGATION Mort Ruderman	ATLANTIC CITY, N.J.	MAY 4-6					
5)	TELECOMMUNICATIONS EXPOSITION Don Murphy	L. ANGELES CALIFORNIA	MAY 4-8		500	20'		

SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIE
46) EEMTIC & IM Denny Doyle	OTTOWA, CANADA	MAY 5-7		2,000	20'		
47) DESIGN ENGINEERING STAN Olsen	NEW YORK	MAY 5-8		20,000	20'		
48) AEROSPACE MEDICAL ASSO Mort Ruderman	SAN FRAN., CALIFORNIA	MAY 5-8		3,000			
49) ASTME George Rice	CHICAGO, ILLINOIS	MAY 5-9		35,000	20'		
50) ASSO FOR EDUCATIONAL DATA SYSTEMS Bob Allison	PORTLAND, OREGON	MAY 6-9		1,000	20'		
51) NAT'L ASSO EDUCATIONAL BUYERS Bob Allison	WASHINGTON	MAY 8-10		500			
52) MIDWESTERN PSYCHOLOGICAL ASSOCIATION Mort Ruderman	CHICAGO, ILLINOIS	MAY 8-10		3,500			
53) ADV ANALYTICAL CLINICAL LAB EQUIPMENT Howie Painter	TOKYO, JAPAN	MAY 12-17					
54) SJCC	BOSTON, MASS.	MAY 14-16		20,000	30' x 40'		

	SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIEI
5)	INT'L LONDON ELECTRONIC COMPONENT Steve Bowers	LONDON, ENGLAND	MAY 20-23					
6)	~~INT'L ELECTRONIC COMP.~~ ~~Steve Bowers~~	~~OLYMPIA~~	~~MAY 20-23~~					
7)	~~AM SOCIETY FOR ENGINEERING EDUCATION~~ ~~Bob Allison~~	~~PHILA., PENN.~~	~~MAY 22-28~~		~~2,000~~	~~10~~'		
3)	ANPA Marv Cothran	CHICAGO, ILLINOIS	JUN 8-12		2,000	32'		
9)	WESTERN PSYCHOLOGICAL ASSOCIATION Mort Ruderman	VANCOUVER, CANADA	JUN 18-21		1,000			
0)	INT'L HOSPITAL EXHIBITION Steve Bowers	GERMANY	JUN 19-25					
1)	ASEE Bob Allison & Bob Pouliot	PENNSYLVANIA	JUN 23-26		1,500	10'		
2)	INT'L CONGRESS OF CLINICAL PATHOLOGY Ray Lindsay	MONTREAL, CANADA	JUL 13-19		1,000	20'		
3)	AM ASSO OF CLINICAL CHEMISTS Mort Ruderman	DENVER, COLORADO	AUG 17-22		1,000			

	SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIE
54)	WESCON	SAN FRAN., CALIFORNIA	AUG 19-21		40,000			
55)	DATA FAIR Steve Bowers	ENGLAND	AUG 25-29					
56)	~~NORBEX Steve Bowers~~	~~SCOTLAND~~	~~SEP 3-11~~					
57)	AMERICAN CHEMICAL SOC Brad Dewey	ATLANTIC CITY, N.J.	SEP 9-11		7,000	30'		
58)	~~INT'L EXHIBITION HOSP & MEDICAL EQUIPMENT Steve Bowers~~	~~BELGIUM~~	~~SEP~~					
59)	ELECTRONICS INSTRUM & CONTROL Steve Bowers	ENGLAND	SEP 25-OCT 3					
60)	CANADIAN MATERIALS & PROCESSING John Holser	TORONTO, CANADA	SEP 30-OCT 2		8,000	20'		
61)	INSTRUMENT EXHIBITION Steve Bowers	HOLLAND	SEP 30-OCT 3					
62)	STOCKHOLM TECHNICAL FAIR Steve Bowers	SWEDEN	OCT 1-7					

	SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIE
73)	~~INTERNATIONAL PRINTING~~ ~~Steve Bowers~~	~~ITALY~~	~~OCT 4-11~~					
74)	INT'L ELECTRONICS CONF Frank Ollie	TORONTO, CANADA	OCT 6-8		1,000			
75)	NUCLEX Steve Bowers	SWITZERLAND	OCT 6-11					
76)	~~ILMAC~~ ~~Steve Bowers~~	~~SWITZERLAND~~	~~OCT~~ 6-11					
77)	~~INT'L MEDICAL EQUIPMENT~~ ~~Steve Bowers~~	~~HOLLAND~~	~~OCT 7-16~~					
78)	ISA	HOUSTON, TEXAS	OCT 27-30		25,000	30'		
79)	IEEE NUCLEAR SCIENCE SYMPOSIUM Rudy Penzer	SAN FRAN., CALIFORNIA	OCT 29-31		750			
80)	~~SALON DES COMPOSANTS~~ ~~Steve Bowers~~	~~PARIS, FRANCE~~	~~OCT~~					
81)	SICOB Steve Bowers	PARIS, FRANCE	OCT					

SHOW & PERSON REQUESTING	LOCATION	DATE	REASON FOR ATTENDING	APPROXIMATE ATTENDANCE	PRODUCT SPACE	MARKETING MANAGER	STAFFING PLANT/FIEI
2) NEC	CHICAGO, ILLINOIS	OCT		15,000			
3) DEC ANNUAL MEETING	BOSTON, MASS	OCT					
4) FJCC	LAS VEGAS, NEVADA	NOV 18-20		20,000			
5) EASTERN ANALYTICAL SYMPOSIUM Brad Dewey	NEW YORK	NOV 19-21		3,500			
6) NEREM	BOSTON, MASS.	NOV		20,000	32'		
7) American Heart Assc. Bob McInnis	Florida	NOV					

digital INTEROFFICE MEMORANDUM

DATE: January 9, 1969

SUBJECT: Gerry Moore's Relocation Expenses

TO: T. Johnson

FROM: G. Thayer

CC: W. Farnham

In reviewing the attached material on Gerry Moore's relocation, I wanted to point out the following:

The expenditures for the lease forfeiture in Germany and the shipment of the car from Germany to the United States will necessitate securing a receipt of these payments from Gerry before the expense voucher should be approved.

As regards to the interest on his loan, I agree that this will require Operations Committee approval; however, I should like to point out that if you feel that this is a reasonable request, some stipulation, I think, should be agreed to by Gerry; namely, that he would not be eligible for the loss on sale of his home in Bedford once he sells it. Also, you might want to consider as part of your argument that in lieu of the Company paying interest and taxes on his home in Bedford for ninety days as is currently provided in the policy, the payments of the interest of the loan may, in effect, amount to the same outlay for the Company, or less, depending on the mortgage and the interest levy in Bedford.

Of the twelve items listed by Gerry, these would be the only departures from our relocation policy for transferred employees with the exception that there is no provision in the policy for the Company's paying for the rental of a leased car for which, in Gerry's case, Digital has already assumed a $300 charge. I would like to point out to you that we have declined this type of payment to other employees because it is not specifically covered in the policy. However, I recognize that in certain instances, like Gerry's, it is reasonable and proper to do. We may want to consider modifying our relocation policy to provide some reasonable period wherein automobiles may be rented at Company expense on such overseas relocations.

GT /lw

digital INTEROFFICE MEMORANDUM

DATE: December 10, 1968

SUBJECT: Gerry Moore's Relocation.

TO: Graydon Thayer FROM: Bill Farnham

The attached letter from Gerry explains his relocation in some depth.

In addition, I have asked Gerry to make out an expense voucher for:

1. Lease forfeiture in Germany. $225 - Receipt
2. Shipment of car from Germany to U.S. Nov.-Dec., 1967 no receipt. $250 - Receipt
3. Interest on loan $16,000 at 7% of $1120 Payment to be made quarterly. $280

I see no problem with items one and two. Item 3 will have to take special approval, but shouldn't be a problem. In addition, I am going to advise Gerry of his eligibility to receive up to $200 of legal fees on the new home. After the sale of his Bedford, Mass. home, the real estate commission will be reimbursable.

I will forward his expense voucher for the above as soon as I receive it.

Bill

Bill

Gail Dictation - ASAP TODAY

PERSONNEL
DEC 11 1968
G. A. THAYER

Please discuss this with Thorpe.
Ted

Memo

To: Ted Johnson

From: Gerry Moore

Subject: Relocation Costs from Germany

When I stopped in Maynard on my return from Germany, I discussed briefly with you my request to have the company pay the interest on my loan of $16,000 which I needed as a down payment on my Glenview house. Harry Mann suggested that this be taken up in Committee, but not without having an overall picture of all the other relocation expenses. As I've been up to my neck in work, I havn't had a chance to pull the information together until now.

Estimation of relocation expenses

	ITEM	AMOUNT	STATUS
1.	Rental of vehicle in Germany last week (after selling my own car)	approx. $100.	Already paid by GMBH
2.	One way tickets to U.S. for 8 persons	Approx. $1900.	Already paid by GMBH
3.	Tickets to Chicago for 8 persons (from East Coast	Approx. $300.	Already paid by DEC
4.	Shipping of car to U.S.	$250.	Paid by me - to be reimbursed
5.	One months rental termination in Germany	$225.	to be reimbursed Paid by me
6.	Surface freight of household goods from Germany (about 2 sealifts)	Approx. $1200.	Already paid by GMBH
7.	Airfreight of a small shipment from Germany	$300 (a wild guess)	Already paid by GMBH
8.	Rental of car for 2 weeks in Chicago	Approx. $200.	Already paid by DEC

In summary, the interest expense is certainly occasioned by the short notice for the move. I don't think one can say, in view of the plans made (in April and May) to keep me in Germany until the summer of 69, that I could have arranged my personal affairs in a better way and avoided the need for borrowing this money. So, I propose that I pay the quarterly interest bills as they come due and be reimbursed for them by the company for a period of up to one year of loan maturity, but not beyond the date of sale of my Bedford house. I propose that the company reimburse me the realtor's fee at the time of sale (which is in line with company policy).=

Two other items, above, should be explained:

1. Two hundred and fifty dollars for shipping a car to the U.S. - this is in line with current company policy. you will recall that I had to ship my Mercedes to the U.S. because I could not register it in Germany for another year. I don't know if the car shipment policy was in effect at the time I shipped it, however, I believe others may have received this reimbursement prior to this time. The actual cost of shipping the car was over $250, but I don't believe I could now find the papers.

2. $225 for Sept. rent in Germany. The terms of my lease in Germany required that I give three months notice. As I was only able to give notice in late July, I could have been required to pay rent until the end of October. My landlord settled for Sept.'s rent(I departed on 13 August).

So, I propose that the company reimburse me $475 for these two items.

Regards

Sam

9.	Interest on $16000 loan for one year at 7%	$1120	Due quarterly to bank
10.	Transport of furniture from Boston area (approx. 7500 lbs)	$600 (a wild guess)	Billed directly to DEC (Ray Michel should know exact amount)
11.	Realtor's fee on sale of house in Bedford	Approx. $2250	To be reimbursed to me at time of sale of house - approx. one year after moving from Germany.
12.	Thirty days living expenses in Chicago area for fam. of 8	$1850	Expense vouchers have just been submitted under separate cover.
	Total estimated cost of relocation	$10,300	

I confess that the total shocks me.

I believe that the only item which is not covered by policy is the interest on the loan. My argument in favor of this item being approved is as follows:

a. Shortly before you asked me to relocate to the U.S., you and John Leng had asked me to remain in Germany for one more year.

b. I agreed and arranged my personal affairs to suit the situation. Specifically, I asked the real estate agent who keeps my house in Bedford rented for me to re-rent the house for another year.

c. He did so, arranging a one year lease with a new tenant, to start in July.

d. In July you offered me the Chicago regional managership. I accepted and moved my family to the U.S. about 3 weeks after the final decision was made.

e. Upon arriving in Chicago, I found house rentals as scarse as hens teeth and extremely expensive. I came prepared to make a long temm commitment to this job and decided that it would be necessary to buy a house in order to properly settle my family.

f. My tenant in Bedford is not interested in either moving from the house there or buying it. Therefore it is not saleable until the lease terminates and my equity in it is not available to me.

g, So, I had to borrow $16000 in order to make a down payment on a house in Illinois.

digital INTEROFFICE MEMORANDUM

DATE: January 15, 1969

SUBJECT: Cross Product Line Marketing

TO: Operations Committee

FROM: Ed Savage / Mike Dowling

Attached is an updated version of the basic plan for accounting for Cross Product Line Marketing. An earlier version of this memo was sent to the Members of the Operations Committee.

The following is a summary of the progress to date on implementing these plans, along with highlights of the problems to be resolved:

Too much?

1.0 Bookings

1.1 Bookings are now being coded by the salesmen as to Market Application area. In December, however, only about 50% of the total dollar volume of bookings were coded. A data processing report of bookings by market area was produced for December data.

1.2 The present policy is that lack of an application code will not be allowed to hold up a booking. However, Ted Graff has accepted the responsibility for communicating with the sales offices when no code is given to insure that all computer bookings over $1000 have an application code.

Since for practical reasons this communication must take place via letter when codes are omitted there may be some lapse of time between the original booking of an order and the amending of that order to reflect the application code. We can help insure that the monthly bookings report by application area is as complete as possible by

(a) Constantly reminding salesmen of the importance of the codes and encouraging them to forward paperwork supporting the orders promptly.

(b) Running the bookings report by application areas about one week after the normal bookings report by product lines. This will allow additional time for amendments to be made to that month's bookings.

2.0 Expenses

2.1 A system has been developed whereby expenses incurred in market applications areas can be collected using the discrete project reporting system. Marketing expenses common to more than one product line can be split according to pre-determined percentages unique to each market area. The accounting department will make these allocations monthly so the cross-product line marketing manager will know his expenses by product line for each major item of marketing expense (Advertising, Promotional Literature, etc.).

2.2 A meeting was held in late December to instruct the managers of the cost centers which normally perform marketing services of the new expense reporting system. Sufficient time has not elapsed to judge whether the new reporting is properly understood and being used, but the probability is that more instruction and emphasis in this area will be needed in order to obtain

meaningful data.

3.0 Budgeting

3.1 Formal budgets by market area were not derived during the recent budgeting cycle. That is, within the product line budgets there were no official detailed breakdowns by market areas, so that the funds to be spent for advertising, sales promotion, trade shows, etc. are still under the ultimate control of the product lines.

3.2 During the budgeting cycle there were, however, many conversations among the various product lines and cross product marketing people, so that in most cases informal working budgets were determined. Bookings and expenses for each market area during the next six months can be measured against these guidelines. The Financial Analyst for each area will produce these reports of expenses and bookings vs. these budgets.

4.0 Cross-Product Marketing vs. Sub-Products.

4.1 It is often convenient for management control purposes for a product line manager to create what has been termed sub-products. Often these sub-products overlap one or more market application areas and the question as to how the two relate is a complicated one. The issues are discussed below in some detail because :

(a) They greatly affect the path of cross-product marketing reporting and

(b) They are controversial so that the Operations Committee should probably voice its preferences.

4.2 Primary question is whether or not to report the same expenses twice if they relate both to a market area and a sub-product.

If the expenses common to both a sub-product and a market area are not classified both ways, (double-counted) some people point out that the expense of doing business in a certain market area will be understated. The argument is further made that the bookings for a market area relative to the expenses for that area can be distorted if expenses are not classified both ways. A specific example will help illustrate the problem:

The Lab-8 is a sub-product which primarily serves the biomedical market but can also be used in analytical instrumentation. Therefore, the majority of the bookings it generates will be credited to the biomedical area, but unless a portion of the expenses of the Lab-8 are reported as biomedical expenses, biomedical bookings relative to biomedical expenses will look artifically high compared with some other application area which might have no overlapping sub-product to take away part of its expenses.

One solution might be to identify Lab-8 bookings and exclude them from the biomedical bookings so a better matching of bookings and expenses occurs. Indeed, this solution is probably desirable and present plans are to work toward a system of coding sub-product bookings. However, there is no coding of bookings by sub-product at this time and there will in all probability always be some sub-products for which we can not identify bookings to match them with expenses so these bookings would not be excluded from those of the related market areas.

The persons arguing in favor of mutually exclusive reporting of sub-product and market area expenses (no double-counting) acknowledge the above arguments but make the following points:

1. To ask service groups to code expenses as related to sub-product, market area, or both complicates the reporting system and enhances the chances of confusion.

2. Many expenses of a sub-product will not relate to one market area any more than another, so the service cost center would report them only as sub-product expenses. So even under the double-counting system we would expect a significant amount of expenses which would not be allocated to market areas but would surely influence the bookings in those areas.

3. The most important argument made against double-counting of expenses centers around budgeting and control of these expenses by the managers. If expenditures by sub-products are also charged against market areas, the cross-product marketing manager will probably

(a) Feel that he has no control over his expenses

(b) Have to budget for his own expenses plus the expenses he thinks he will incur from the overlapping sub-products, which could get confusing.

MJD/ba
Attachment

digital INTEROFFICE MEMORANDUM

DATE: December 16, 1968

SUBJECT: Cross-Product Marketing Reporting (Updated version of November 20 memo)

TO: Marketing Review Committee
Dave Packer
Ted Graff
G. D'Annunzio

FROM: Ed Savage/Mike Dowling

A great deal of interest has been generated in recent months concerning the development of information related to the marketing activities within our organization. The purpose for recasting existing data into market applications is to establish a meaningful report which would show the marketing specialists how the volume of business, from their particular areas, is stepping up and also the costs that are directly related to that marketing activity.

A second benefit to be derived from such a report is the significant role it would play in future budgeting efforts of the company.

Attached is an outline of the reporting system for cross-product marketing and sub-products. The plan is to have the Cross-Product Marketing reporting in operation by the start of the 3Q, Fy 1969. The initial goal will be to issue to market managers a monthly report by product line for each market area with the following format:

		TOTAL	8 FAMILY	9 FAMILY	ETC
BOOKINGS	$				
Special Engineering Expenses					
Marketing Expense					
Space Advertising					
Promotional Literature					
Direct Mail and Trade Shows					
Total Expense	$				

The first goal will be to make this report accurate and timely on a corporate-wide basis. After this goal is achieved and depending upon the experience gained and the desires of operating management, our next objective will be to add billings and cost of sales information to these reports.

The addition of billings and cost of sales information would produce a report having the following format:

Bookings	$
Billings	$
Job and Standard Costs	
Gross Margin	$
Special Engineering Expense	
Marketing Expense	
Spare Advertising	
Promotional Literature	
Direct Mail and Trade Shows	
Profit Contribution	$

Each booking or expense item will be reported only once. When the information is reported as a sub-product, it will not be included again in the report for the market containing that sub-product.

The coding of bookings by sub-product (e.g., LAB-8, INDAC-8, etc.) is more complicated than coding by market areas because of the problem of identification. This will have to be worked out over the next few weeks, but expenses by sub-product can be collected and reported immediately using the discrete project reporting system.

By the time we are ready to begin our budgeting cycle for fiscal 1970, these reports should have been in use long enough to allow meaningful budgeting for market areas and sub-products.

cd

Mike Dowling
November 20, 1968

I. Cross-Product Marketing

A. Bookings:

1. Salesmen world wide to note application on the Master Order Cover Sheet for all orders when submitted.

2. Central order desk to monitor incoming orders and insure that applications areas are marked. If not, COD has responsibility for contacting the sales office and code all bookings for amounts over $1,000.

3. A monthly report of bookings by product line for each application area will be generated by Data Processing and distributed to the marketing managers responsible for that application area. (Exhibit I) Since all bookings are coded in the application area, this report will show bookings by application for both products and sub-products. Accounting will be able to idenify and exclude sub-products in arriving at the booking figures for general application areas. (Discussion of sub-product coding in Section II.)

4. Lack of codes will not be allowed to hold up booking of orders. Central order desk will file an amendment to the DEC order when the code is determined

5. Foreign bookings defined as Master Order Forms sent to Maynard Computer Administration by the subsidiaries. Orders placed by TWX are not considered official because they can not show the market code which must be marked on the cover sheet of the Master Order Form.

B. Expense:

A variation of the normal discrete project reporting system will be used to collect cross-product marketing expenses.

You will recall that the project number used in reporting expenses has 7 digits, 2 for the product line and 5 for the discrete project number. For cross-product marketing, the product line code will still be used. But only the first digit of the discrete project code section will be filled with an alphabetic character (see next page). When no one product line can be identified, the code "93" should be used to denote an expense to be shared by all product lines.

Cost centers working for one of these market areas should fill in the alphabetic code for that area and the product line code. The cost centers charging will normally be marketing centers, advertising and promotion, printing, art, documentation, trade shows, direct mail, and occasionally some engineering centers.

Mike Dowling
November 20, 1968

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(SAMPLE)

APPLICATION Physics

MONTHLY SUMMARY BOOKINGS BY APPLICATION CODE

Appl Code	PL	MFG.	DEC #	CUST #	CUSTOMER	GROSS	NET
P	08	00	53740	00270	ACE IND	10,000	9,800
P	09	00	53780	00610	NUC Physics	22,000	19,500
P	10	00	53600	00310	DEC UK	10,000	7,000

Domestic Gross	32,000	29,300 Domestic Net
Foreign Gross	10,000	7,000 Foreign Net

Total: Domestic Net + Foreign Gross 39,300 *

EXHIBIT I

Mike Dowling
November 20, 1968

Project Number Reporting at Cross-Product Marketing Expenses

Product Line Code	
08	8 Family
09	PDP-9
10	PDP-10
36	LINC
50	Modules
93	"Shared" Marketing Expense
99	Traditional Products

Marketing Application Code		
Code	Market	Specialist
B	Biomedical	Mort Ruderman
P	Physics	Ken Larsen
A	Andytical Chemistry	Brad Dewey
G	Geophysics/Marine	Bob O'Hagen
E	Educational	Norm Doelling
S	Other Applied Science	
T	Typesetting	Marv Cothran
N	Numerical Control	
I	Industrial Control	Ron Noonan
K	Other Industrial	
F	Computation Facility	
H	Hybrid Simulation	
D	Display Research	
C	Communications	Don Murphy
M	Miscellaneous	

Each month a report similar to the present discrete project report will be issued by Data Processing which will show the expenses for that market area by product line and cost center (Exhibit II).

Just as with discrete project reporting, the cross-product marketing manager can go to the various cost center managers charging him and ask for a detailed breakdown of the expenses for a particular period. The new "Project charges by Cost Centers" report which is distributed with each cost center report should be of particular value (Exhibit III).

In order for the reporting system to be effective, it is very important that the cost centers making charges use the codes! Marketing managers should insure that the service centers are aware of the appropriate codes and use them.

Sub-Product Lines

Bookings Code *	Sub-Product	Specialist
80	Lab-8	Mort Ruderman
81	Indac-8	Ron Noonan
82	Gas Chrom-8	Brad Dewey
83	Communic-8	Don Murphy
84	Time Share-8	Norm Doelling
85	Typeset-8	Marv Cothran
86	PHA-8	Ken Larsen
87	Quickpoint-8	
88	Navig-8	Bob O'Hagen
70	Clinical Lab	Mort Ruderman
71	A Series Modules	Al Devault
72	M.Series Modules	Al Devault
73	K Series Modules	Al Devault

* To be used only by Computer Administration.

(SA PLE)

GENERAL MARKET EXPENSES

Market Area Biomedical Code B Date

PL		Cost Center	Month Actual
08	255	Biomed. Mktg.	$2,000
	287	Prom. Lit.	1,000
		PL Total	3,000 *
09	255	Biomed. Mktg	4,000
	360	Programming	1,500
		PL Total	5,500 *
93	255	Biomed Marketing	200
	152	Direct Mail	300
		PL Total	500 *
		Market Total	$9,000 *

EXHIBIT II

(SAMPLE)

Period Ending 11-23-68

PROJECT CHARGES BY COST CENTER

Cost Center 287

Overhead Rate is 50%

Acitivity	Prod-Line	Project	Labor	Overhead	Material	Vouchers	Total
A	08	B	200.00	100.00			300.00
A	08	07006	400.00	200.00	500.00		1100.00
A	09	B	600.00	300.00	100.00		1000.00
A	93	P	100.00	50.00		50.00	200.00
	Cost Center		1300.00	650.00	600.00	50.00	2600.00 ***

NOTE: In the above example it can be seen that this is a marketing cost center (287) and the legal activity code is "A". Project "B" is work for general Biomedical Marketing. Project 07006 is a discrete project for a sub-product within the "8" Family. Product Line "93" and Project "P" denote Physics marketing expense which cannot be identified with a particular product line and will be allocated to product lines on a pre-determined basis.

EXHIBIT III

Mike Dowling
November 20, 1968

II. Sub-Product Lines

Sub-product lines, although they often may relate closely to a cross-product market, can usually best be thought of as separate entities. For example, for budgeting and reporting purposes it is more clear-cut to think of the Lab-8 as a sub-product distinct from general biomedical marketing, even though most Lab-8 installations are in the biomedical area and both the Lab-8 and general biomedical marketing are the responsibility of Mort Ruderman.

A. Bookings

1. The Central Order Desk will code bookings as to a sub-product, if applicable. They will determine codes based on examination of the orders submitted, so field salesmen will be asked to code only market areas.
2. The codes to be used are shown on the following page. They are to be used in addition to the major product line code.
3. Data processing will furnish monthly booking reports by sub-product. The reports of bookings by market areas will include some bookings of sub-products, but the latter will be easily distinguishable by the unique codes and can be pulled out so that sub-product and general market area bookings can be reported separately to their respective managers.

The major difficulty in this area will be the ability of Computer Administration to identify sub-products so that they can code the bookings. Most sub-products are nothing more than certain combinations of peripherals and processors. The practicality of reporting bookings by sub-product depends upon the ability to specify clear-cut guidelines for identification.

B. Expenses

The normal discrete project reporting system will be used to collect expenses for sub-products. The first two digits of the project number relate to the major product line and the next five digits establish a unique sub-product. One project number can be used to collect expenses from all types of cost centers likely to serve the sub-product.

A sample of the normal discrete project report is attached (EXHIBIT IV).

EXAMPLE OF EXPENSE CODING:

	Product Line Code	Project Code
General Cross-Product Line Marketing		
Biomedical for PDP-8 Family	08	B _ _ _ _
Biomedical - Shared	93	B _ _ _ _
Sub-Product		
Lab 8	08	0 7 1 1 4

cd

DISCRETE PROJECT REPORT — Period Ending 8/30/68

36 07166 — LABCOM — M.Ruderman/W.Hindle

Current Month						Year-to-Date			Project to Date
;ual	Budget	Better Worse		Cost Center		Actual	Budget	Better Worse	
57		57*	153	Trade Show	R.Smart	368		368*	593
.30	3,200	70	258	Biomedical/ Marketing	M.Ruderman	6,970	6,400	570*	8,216
	250	250	287	Promotional Literature	G.D'Annunzio		500	500	
.25	2,100	25*	360	Programming	L.Portner	4,560	4,200	360*	8,323
300		300*	380	LINC Engr.	R.Clayton	632		632*	809
512	5,500	62*		TOTAL		12,530	11,100	1,430	17,941

EXHIBIT IV

digital INTEROFFICE MEMORANDUM

DATE: January 10, 1969

SUBJECT: Press Conference for New Product Announcements

TO: Ken Olsen FROM: Mark Nigberg

Because the PDP-11 announcement will have such a major impact in the industry, we believe it is essential that a clear, uncluttered impression of what we are doing is presented to the public.

We understand DEC will introduce a number of new products, in addition to the PDP-11, during the next few months - the PDP-14, the PDP-15, Indac-8, NMR-8, and a new graphics system.

As a leading force in the computer industry, all of our product introductions are of major importance to the public. However, we can easily confuse our customers and potential customers if these announcements are made haphazardly to a press that does not understand what DEC is doing nor why. Unless these announcements are closely coordinated, we believe DEC will not emerge with a clear, understandable message in the marketplace, nor will our new products appear to be part of a comprehensive and well-defined computer line.

Therefore, we recommend that, instead of announcing the PDP-11, PDP-14, PDP-15, Indac-8, and other products separately, we hold a single news conference to announce these products, putting them into the context of DEC's total product spectrum, and explaining why we offer them.

We propose this conference take place in New York either in early March or April. We favor early April because it gives us greater leverage in developing special features to appear in the press before SJCC. The early March announcement, although favored by some, creates serious problems for at least one of the product lines.

We propose inviting approximately 100 members of the general, financial, and trade press. We would like you to present an overview of the company and our product lines, putting our new products into the correct frames of reference. We would also like to have representatives of our new product lines available to answer questions.

Because of the importance of this conference and the time factors involved, I would appreciate the opportunity of discussing this plan with you in greater detail as soon as possible.

MN/tkw

digital INTEROFFICE MEMORANDUM

DATE: January 13, 1969

SUBJECT: Relocation of Print Shop

TO: Operations Committee FROM: Nick LoRusso

Just prior to Harry's accident, he discussed with me and certain members of the Operations Committee the possibility of moving the Print Shop to Building 8. He also thought it would be a good idea to organize materials and records in Buildings 8 and 11. Since organizing the materials in those buildings does not have any bearing on whether or not the Print Shop is relocated, I would like to present the recommendation to the committee in two parts.

Print Shop

At the present time approximately one hundred tons of paper and supplies are moved from our Receiving Department to the Print Shop annually. The distance between the two areas is about 1000 feet. Since Building 8 is served by its own elevator and dock, it may be more desireable to relocate the Print Shop to this area, thus cutting down on movement of material. We have since discovered that there are inadequate power and water facilities in Building 8. We would therefore like to relocate to Building 6B, Floor 3 as an alternative. The vacated area in Building 3 can then be utilized by the growing Programming Department.

Materials in Buildings 8 and 11

Materials in these buildings are of the following types:

1. Advertising Brochures
2. File Records
3. Payroll Records
4. Packaging Material
5. Desks
6. Paper
7. Manuals

The above material is in fenced off areas and assigned to certain cost centers. The materials seem to be of a type that are not

commonly used or are of a surplus nature. The materials stored in the individual areas are not well organized which creates a waste of space and possible damage to materials. The intent is to cut down on wasted space and damage to materials by staffing the area with one man.

This man's responsibilities will be to receive materials of the type stored in these areas at the receiving dock in the Building 8 Annex. He will organize the area so that he can fill requisitions for the material in those areas. He will also create an orderly records center for DEC.

The benefits of accomplishing the above are:

1. Better utilization of space. We can turn over approximately 3600 square feet to the programming group.

2. Cut down on the movement of materials from Receiving to this area.

3. Utilize existing space and records in that area so that we can establish a Records Retention Center and implement a Master Letter File plan.

Moving the Print Shop to that area would not be a short term project, it would take some time. However, if you agree, we should organize the materials in that area. We can begin this work immediately.

Consideration of the above would be greatly appreciated.

digital INTEROFFICE MEMORANDUM

DATE: January 15, 1969

SUBJECT: NOTES ON FIVE-YEAR PLANS

TO: Operations Committee

FROM: Pete Kaufmann, Secretary

These are notes taken from the blackboard at our meeting on Tuesday, the 14th.

	1969	1970	1971	1972	1973
Sales (11/68) $/Product	95	135	180	225	270
Number of people, managers, etc.	2,500	3,400	4,500	5,600	6,750
Number of sq. ft. 10,000/sq.ft./$	950	1,350	1,800	225,000	270,000

ecc

COMPANY CONFIDENTIAL

OPERATIONS COMMITTEE MEETING

January 13, 1969

AGENDA

1. Additions and Corrections to Minutes of the January 6th Meeting
2. Marketing Review Committee Summary - (Ted Johnson)
   (See attached minutes of the January 7th meeting)
3. 1969 - 1970 Northeastern Management Course - (Win Hindle)
   (Report was distributed for last week's meeting)
4. Relocation Policy Change/Special Payment for Miscellaneous Expenses - (Win Hindle)
   (See attached report from Graydon Thayer)
5. Proposed Budget for the KV Graphic System - (Bob Collings)
   (See attached report)
6. Proposed Renovation of the Drafting Department - (Roger Melanson)
   (See attached report)
7. Proposed Acquisition of Building #3 in Puerto Rico - (Cy Kendrick)
   (See attached report)
8. Proposed Purchase of an Environmental Control Chamber - (Al Hanson)
   (See attached report)
9. Catastrophe Plan
   (See attached list of proposed names for this responsibility)

COMPANY CONFIDENTIAL

MINUTES OF OPERATIONS COMMITTEE

January 13, 1969

Present: Nick Mazzarese, Win Hindle, Ken Olsen, Stan Olsen
Pete Kaufmann (Secretary)

Absent: Ted Johnson

1. The minutes of the January 7 meeting were accepted.

2. KV8I Budget

Ken asked if we could have a monthly budget of sales and costs. Marketing costs, Quarter 3-4, 1 and 2, would be 51K. Next week Bob Collings will submit a complete budget including ROI.

3. Marketing Review Committee

Ken would like the "digital" logo to be used, not "DEC". Ken will notify Bellantoni and D'Annunzio of his feelings.

Cross Product Accounting should be discussed with Mike Dowling present.

The new booth for $80,000 seems too expensive.

The committee seems to be critical; but, no one seems to be taking responsibility. Ken suggested that only individuals who will take responsibility should make proposals.

4. Management Northeastern Course

Bill Long and Al Devault (October 1969) and Ed Schwartz (January 1970) will be asked to attend the course if they wish.

5. Relocation Policy Change - Special Payment for Miscellaneous Expenses

Win feels competitively other companies have miscellaneous payments. The revision of the policy was approved as submitted.

In the future all moves of individuals will come to the Operations Committee prior to a commitment to the individual.

6. Drafting

The 20K does not include the auto-shift drawing tables and that portion was not approved. The Computer Room will be in the old Disk area; the partitions will be removed, except around the Reproduction area. The proposal was then approved.

7. Acquisition of Building #3 - San German, Puerto Rico

The proposal was accepted.

8. Environmental Control Chamber

The proposal was not accepted. Some member of the Environmental Control Chamber must come to the Operations Committee with a proposal and take responsibility.

9. Renovation of Lobby

Ken's proposal for Building 12-1 lobby was accepted. He will take responsibility for renovating the lobby.

10. Signs

Al Hanson's signs proposal was accepted.

11. Lunch - Tuesday, January 14 12:00 - 1:00, Ken Olsen's office

Rough pass five year plan for space, shipments and products.

12. VR12

We need an inexpensive light pen; maybe need 18", 21", 27" version and need to exploit in the market. Ken suggested that Stan make a proposal on how to exploit VR12.

jb

digital INTEROFFICE MEMORANDUM

DATE: January 8, 1969

SUBJECT: PROPOSED BUDGET FOR KV GRAPHIC SYSTEM

TO: OPERATIONS COMMITTEE FROM: Bob Collings

The purpose of this memo is to present a proposed budget of $97,000 for the KV Graphic System (Discrete Project #7192). Through December 1968 approximately $42,000 has been spent on this program. The project is expected to be completed in June 1969 with an estimated expenditure of $32,000 in Q_3 and $23,000 in Q_4.

The KV Graphic System is expected to result in the sale of $1,018,000 of options over the next three years and contribute to the sale of an additional $1,125,000 of computer systems. The engineering cost ratio $\frac{97,000}{2,143,000 \text{ (Total Sales)}} = 4.5\%$ or $\frac{97,000}{1,018,000 \text{ (Option Sales)}} = 9.5\%$ is below our traditional ratios. Your approval of this budget is enthusiastically recommended.

Bob Collings

ec

Ken

digital INTEROFFICE MEMORANDUM

DATE: January 2, 1969

SUBJECT: 1969-1970 Northeastern Course

TO: Operations Committee FROM: Win Hindle

The last time we discussed next year's Northeastern Course, we decided that Bill Long, Al Devault, and Ed Schwartz should go. If this still seems reasonable, I suggest that Nick, Stan and Ted respectively talk to these three and that I send their names to Northeastern. We have two spaces in the course starting in October 1969 (I suggest Bill and Al attend) and one space starting in January 1970 (Ed).

bwf

digital INTEROFFICE MEMORANDUM

DATE: January 7, 1969

SUBJECT: Renovation Of Drafting Department

TO: Operations Committee FROM: Roger Melanson

Attached is proposal for renovating Drafting Department Building 4, Floor 4.

ROGER

RM:tl

Atch.

digital INTEROFFICE MEMORANDUM

DATE: January 3, 1969

SUBJECT: Renovation Of Drafting Department

TO: D. Knoll FROM: Roger Melanson

Am proposing that we arrange the drafting facilities to get more efficient and usable space out of our given area and to improve the working environment with a general uplifting of the surroundings.

Estimated cost to renovate the 13,000 square foot area is $20,000.

SPACE

We will gain 2,000 square feet of usable space at a savings of $6,500 per year by:

1. Relocating Photo Resist Department.

2. Remove stairwell between floor 3 and 4.

3. Complete changeover to auto-shift drawing tables.

4. More prudent layout of partitions and furniture.

This additional space will provide 18 more work stations and should take care of our needs for the next 12 - 18 months. At which time, approximately 3- 4,000 square feet of space may be required.

Environment

The importance of good working conditions cannot be underestimated. Good lighting of 150 to 200 candle power in most all areas of the floor is necessary. In order to have minimum distraction the noise level shall be greatly reduced. This will be achieved by isolating reproduction equipment at one end of the floor, by placing the PDP-4 in a closed room, and by routing the traffic from/to Building 6A, 6B, 8 and 11 to the floor below. Climate control will be improved with the addition of 10 ton of air conditioning and installation of heating zone valves to regulate the heat. Walls and ceiling will be painted for a pleasant atmosphere. And the floor will be machined washed and covered with urethane.

WORK SCHEDULE

Since we presently occupy the floor, work will have to be done piecemeal. Distruption of the work force will be minimized with a step by step plan. It is advisable that heavy carpentry work and painting be done during the off-hours. Plant Engineering estimates it will take approximately eight weeks once the work is started.

Attached is a copy of the summary cost estimate and a print of the floor plan.

ROGER

RM:tl
Atch.

CC: A. Hanson
R. Baum

Bldg. #4-3

ESTIMATE SHEET

Description	Quantity	Labor	Material	Total
1. Demolition				$ 1,000
2. Partitions				
7' High	252 Lin. ft.		@$ 8.00	2,016
4' High				
8' Wire				
floor to ceiling	82 Lin. ft.		@ 16.00	1,312
special Wire to Ceil	152 Lin. ft.		@ 8.00	1,216
3. Electrical				
Lighting Additional Lighting				3,000
Power				
Receptacles	115V 15A	60 Cycle		2,000
50 cycle				
4. Compressed Air				
5. Air Conditioning				
10 Ton Additional				4,000
6. Heating				
Zoning Valves				900
7. Ventilation				
8. Plumbing				
9. Painting				1,500
10. Work Tables				
11. Shelves				
12. Floor				
sealing				
tile				
repair				
13. Rigging				500
14. Remove Stairwell				800
				$18,244
			Cont. 10%	1,824
			TOTAL	$20,068

digital INTEROFFICE MEMORANDUM

DATE: January 8, 1969

SUBJECT: Aquisition of Building #3
San German, Puerto Rico

TO: Operations Committee FROM: Cy Kendrick

By the end of January this year D. E. C. de Puerto Rico will have grown beyond the capacity of Building #1.

Plans are underway to sign the lease, add lease hold improvement and take occupancy in building #2 by late February.

Present schedules have us now at approximately 100 direct labor employees and growing to the full capacity of building #1 and #2 (250 D.L. employees) by December of 1969. (See manpower plan attached.)

Therefore it is recommended that we negotiate a 60,000 square foot building with Pridco, sign a lease no later than March 1, 1969 for planned occupancy by January 1, 1970.

Module and cable assembly will vacate buildings #1 and #2 and will occupy about thirty thousand square feet in building #3, leaving thirty thousand feet available for future expansion of modules, new products or to be available in case of an emergency at Maynard.

Estimated Costs of Lease Hold Improvements:

Restoration of buildings #1 and #2	$ 5K
Relocating building #1 and #2 to building #3	30K
Lighting and power building #3	50K
Mechanical work building #3	40K
Air conditioning and installation building #3	30K
Partitions building #3	10K
Exterior building #3	6K
Treat floor building #3	5K
Miscellaneous expenses	26K
Total	$202K

Cy

mo

PUERTO RICO MANPOWER PLAN
1969

Puerto Rico

Planned Work Load	JAN	FEB	MAR	APR	MAY	JUNE	JULY	AUG	SEPT	OCT	NOV	DEC
Modules	12.1K	16K	24K	23.2K	25.6K	33.6K	32K	32K	38.4K	32.8K	32.8K	34.4K
Cables							2.5K	4.3K	1.3K	5.7K	6.5K	3.8K
Total Hrs.	12.1K	16K	24K	23.2K	25.6K	33.6K	34.5K	36.3K	39.7K	38.5K	39.3K	38.2K
Total People	100	120	150	159	165	175	190	200	220	230	240	250

1970

Planned Work Loan	JAN	FEB	MAR	APR	MAY	JUNE	JULY	AUG	SEPT	OCT	NOV	DEC
Modules	35K	35K	37.5K	37.5K	37.5K	40K	40K	43K	43K	43K	43K	43K
Cables	8.1K	8.8K	6.2K	10.2K	10.8K	8.3K	11.1K	11.4K	14.6K	12.1K	12.5K	15.6K
Total Hrs.	43.1K	43.8K	43.7K	47.7K	48.3K	48.3K	51.1K	54.4K	57.6K	55.1K	55.5K	58.6K
Total D.L. employees	263	265	273	297	300	300	319	340	350	355	360	360

digital INTEROFFICE MEMORANDUM

Memo #481

DATE: January 8, 1969

SUBJECT: Environmental Control Chamber

TO: Operations Committee FROM: Al Hanson

The Environmental Control Committee, chairmaned by Joe St. Amour, would like to propose to the Operations Committee the purchase of an environmental control chamber - the specifications are as follows:

Size (inside)	8' x 10' x 7' high
DB	32° F to 140° F
RH	5% to 95%
Load	4,000 Watts

PURCHASE

The necessary funds can be provided from the capital budget of Plant Engineering, Cost Center 648. (There is 15 K earmarked for environmental control chamber - Delete 10 K from Electrical Primary Metering - Total 25 K.)

MAINTENANCE

Plant Engineering will erect and maintain facility.

SCHEDULING

Joe St. Amour will be directly responsible for scheduling the use of the facility.

- use s/w
- room
- cabinet 5-3

AWH/cr

digital INTEROFFICE MEMORANDUM

DATE: January 6, 1969

SUBJECT: MEN RESPONSIBLE FOR DISASTER PLANS

TO: Operations Committee FROM: Ken Olsen

Listed below are the names you suggested for catastrophe plan responsibilities:

Win Hindle

Bob Savell
Dick Clayton
Bob Lassen
Larry Portner
Bob Dill
Dave Packer
Ken Larsen
Mort Ruderman
Ed Savage

Ted Johnson

Jack Shields
Ron Smart
  Pat Greene
  Bill Farnham
  Ted Graaf
  Bob Fronk
John Bellantoni
Ed Schwartz
Individual Office Managers

Pete Kaufmann

Henry Crouse
Roger Melanson
Dave Knoll
Jack Smith
  Bert Couillard
Dan Sullivan
George Wood
Joe St. Amour
Tom Stockebrand
Loren Prentice
Cy Kendrick
  Phil Wood
Ed Simeone
Bill Hansen

Stan Olsen

George Gerelds - Model Shop
Frank Kalwell - Mail, Shipping, Module Stockroom, Module Order Processing
Nick LoRusso - Office Services Telephone, Supplies, Print Shop
Al Hanson
Al Devault
John Jones
Bob Lane

Nick Mazzarese

Ron Noonan - Data Acquisition
Brad Vachon - Special Systems
Bill Long - PDP-8 Product Line
Gabe d'Annunzio - Advertising & Promotional
Roger Cady - DCM
Bob Collings - Display Products

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COMPANY CONFIDENTIAL

OPERATIONS COMMITTEE MEETING

January 6, 1969

AGENDA

1. Additions and Corrections to Minutes of the December 30th Meeting
2. Marketing Review Committee Summary - (Ted Johnson)
   (See attached minutes of the December 31st meeting)
3. Tape Transport Final Approval - (Arnold Sherman)
   (See attached report)
4. DECtape Final Approval - (Ernie Luttig)
   (See attached report)
5. Line Printer Final Approval - (Bill Owens)
   (See attached report)
6. Mail Room Proposal - (Frank Kalwell, Nick LoRusso)
   (See attached report)
7. Manufacturing Production Rates Report - (Pete Kaufmann)
   (See attached report from Dave Kicilinski)
8. Review of Budget Results and Plans for Module Selling - (Ted Johnson, Stan Olsen, Al Devault)
9. Discussion of Plans for SJCC
10. PDP-10 Open Slots
11. 3rd Quarter Billings
12. Insurance and Catastrophe Plan
13. Data on Nova
    (See attached report written by Grant Saviers and submitted by John Jones)
14. Salary Administration Guidelines - (Win Hindle)
    (See attached report from Graydon Thayer)
15. 1969-1970 Northeastern Management Course - (Win Hindle)
    (See attached report)

MINUTES OF OPERATIONS COMMITTEE

January 6, 1969

Present: Ken Olsen, Nick Mazzarese, Pete Kaufmann, Stan Olsen, Ted Johnson, Win Hindle

Secretary: Pete Kaufmann

1. Minutes of the December 30 meeting were approved with the following correction:

   #6D "Ron feels" - delete "doesn't"

2. Financial Analyst - January 29

   1. Enter Building 5-1 (New Parking Lot)
   2. Demonstration area - Talk
   3. Tour
   4. Lunch - Buffet

3. Tape Transport
   Line Printer - Engineering Proposals
   DECtape

   Proposals were accepted with some concern expressed as to the tightness of the schedule.

4. Review of Budget Results and Plans for Module Selling (Al Devault) 272K/man bookings rate so far this year. Target yield of 232K per man is being met. Regions without market specialists seem to be:

Mid Atlantic -	three vacancies out of 8 slots Princeton, Long Island, N.Y.C.
Europe	five vacancies out of 11 slots
Western	two vacancies out of 7 slots
Central	two vacancies out of 7 slots
Northeast	one vacancy out of 4 slots

   Budget 37 men actual 23 63% of budget

   Al Devault seemed concerned about making his 12 million budget without the people. Ted had some questions about the product specialist form of selling vs a customer specialist. Ted suggested that the Product Line is not working hard enough with District and Regional Managers, that it is their program. Ted asked for a simple list of complaints each month. Each month both groups will list plan and results.

5. Mailroom Proposal

Cut down number of 84 stops to optimize delivery. Rest of proposal approved.

6. Proposed Price Reduction PDP-9 and 9L

Prices get approved by the Operations Committee. Ted Johnson would like to check out this proposal with the Regional Managers. Subject to the agreement of the volume to be obtained by the Regional Managers, the Operations Committee approves.

7. Salary Review Guidelines

Talk about it at Salary Review Meeting

jb

gen

INTEROFFICE MEMORANDUM

CONFIDENTIAL

DATE 27 December 1968

SUBJECT Salary Administration Guidelines 1969 (WC-4)

TO Salary Review Committee FROM G. A. Thayer

Recently, a survey was conducted among 21 companies to determine the salary administration guidelines which they have established for 1969 for exempt employees.

Attached is a copy of the survey; however, the more significant findings are listed below:

(a) The growing cost of living (up 4% in 1968) is weighing significantly on the percentage ground rules and is forcing companies to move their percentage increase to payroll closer each year to the 10% figure.

(b) Fewer and fewer companies each year are distinguishing between percentages used for technical and non-technical exempt personnel. Only seven out of the twenty-one companies reported separate figures for these groups.

(c) Over half of the companies have established a specific guideline establishing a fixed percentage of zero increases of those eligible. The percentage of zero increases established runs from 5% to 25% of those eligible.

(d) The majority of companies have some sort of stretch-out schedule governing the time interval between merit increase review dates, usually geared to the salary of the employee. Most common is 18 months interval for personnel over $18K per year.

Guideline Recommendations 1969:

(a) Increases as a percent of payroll - 9%

(b) Minimum increase - 4%

(c) Normal maximum increase - 10% Increase over this must be warranted by special circumstances.

CONFIDENTIAL

(d) Zero increases - 5% of those eligible- I feel we should take a closer look at the people in bottom performance quartile and, unless performance has improved, seriously consider a zero increase. An employee's performance may not be sufficiently below standard to warrant discharge, but it also may not be adequate to support an increase. Also in this group may be employees who have pretty much reached their growth potential and for whom we should consider some form of stretch-out in their review dates.

(e) Review schedule

Under $20K - 12 months, based on anniversary month

Over $20K - 18 months, based on anniversary month

(Increases considered on a "special" basis for shorter time intervals)

Areas Requiring Corrective Action:

The following groups warrant close attention and possible corrective action based on trend of salaries in the market compared with our prevailing rates:

1. Accountants
2. Programming Instructors, Hardware Instructors
3. Sales/Field Service Engineers
4. Key Personnel - Supervisory/Non-Supervisory
5. Engineering Writers

GAT/gp

CONFIDENTIAL

1969 MERIT INCREASE SURVEY

COMPANY	EXEMPT				
	PERCENT INCREASE			% PAYROLL	% ZEROS
	MAX.	AVER.	MIN.		
Sylvania	-	-	3%	Engineer 8.3% Other 7.5%	20%
Analog Devices	12%	10%-S 9%-NS	8%-S	- -	10%
Hewlett Packard	-	6-7%	3%	- -	5-10%
Honeywell 3 C's	-	-	-	Engineer 9.3% Other 7.0%	-
General Electric Medinet 5% General Increase 1 January 1969 Plus →	-	Prog./ Acct. 3-7% Supv. 5-8%	-	- -	
Bell Labs 3.0-3.5% Market ADJ Plus →	-	6-7%	-	6%	
Ford 3½% General Increase September Plus →	12%	7-8%	5%	2½%	over 25%
NCR	15%	6%	4%	- -	-

1969 MERIT INCREASE SURVEY

COMPANY	EXEMPT PERCENT INCREASE MAX.	EXEMPT PERCENT INCREASE AVER.	EXEMPT PERCENT INCREASE MIN.	% PAYROLL	% ZEROS
SDS	-	7%	-	6%	-
Texas Instruments	None	-	2%	7-9%	5-15%
EG&G	-	6-8%	-	- -	-
AVCO: Engineer Non-Engineer	12% 15%	7% 7%	3% 3%	8%	10%
Anelex	10%	6%	3%	- -	-
Adage	12%	4.6%	None	- -	-
Adams-Russell	10%	7.2%	-	7.5%	5%
Philco-Ford	15%	7-7.5% non-supv. 7.0-10% supv.	5%	6%	25%

1969 MERIT INCREASE SURVEY

COMPANY	EXEMPT PERCENT INCREASE MAX.	EXEMPT PERCENT INCREASE AVER.	EXEMPT PERCENT INCREASE MIN.	% PAYROLL	% ZEROS
MITRE Cost-Living 3.2% 1 January '69 Plus	None	9.0%	3%	Technical 7% Support 7.6% Other 5.0%	20%
RCA (Burlington)	-	-	3%	Technical 8.1% Support 7.3% Other 6.0%	23%
Sanders	-	-	3%	Technical 9.0% Support 7.5% Other 7.5%	15%
Nortronics	-	-	3%	Technical 6.7% Admin. 5.8%	None
Raytheon	-	-	3%	Technical 8.5% Other 7.0%	10%

Ken

INTEROFFICE MEMORANDUM

DATE: December 31, 1968

SUBJECT: Attached Data on Nova

TO: Operations Committee

FROM: J. A. Jones

Because of our interest in this machine, Grant took a very close look. You'll find his comments interesting and penetrating.

John

JAJ/njb

DIGITAL INTEROFFICE MEMORANDUM

DATE: December 23, 1968

SUBJECT: The NOVA Computer

TO: John Jones ✓ FROM: Grant Saviers

cc: Roger Cady

This is a summary of the spying efforts on the Data General NOVA computer conducted at the Fall Joint Computer Conference. Mr. Edson DeCastro seemed pleased to talk about his machine and not at all hesitant at pointing out all its design features. Attached is their advertising brochure that they were passing out at the Fall Joint. The claims of a 4K full processor maching in a five and a quarter inch standard 19 inch rack appeared to be justified from what I could see of the interior of one of their models. The machine is built strictly on large printed circuit boards very similar in construction to those used by Digital. They are plated thru hole boards approximately 15 by 15 inches. There is no great difference in the layout techniques or consequently higher printed wire density than we have been using here. The processor appeared to be constructed on two of these boards with approximately 100 (actual count 96) integrated circuits per board. The memory is located on a third board and the memory stack is not a stack memory. It is cleverly hidden behind aluminum shield. The 2 connectors for each card look to be dual 75 pin with bifurcated contacts similar to the proto connector for the PDP-X. Thus approximately 300 pins per circuit board. The printed circuit connectors are mounted on a PC back plane. There are absolutely no wire wraps on this back plane. It is all in printed circuit. The lay-out from the pin side looks very clean in that it is mostly straight bussing signals, with very short leads. The other side, assuming it is a two sided board, is not visible. The power supply is very similar looking to the 8L power supply in size and fits across the cabinet in the rear. The machine that I looked at contained one memory card and two processor cards. There was a spare or possibly two spare card positions, one of which could be used for read-only memory. The read only memory card was a steel frame which supported two cards approximately 6 by 15 inches. The cards were oriented so

that when facing the front of the machine the connectors were on the left. The advertising literature claims that they could fit 2 K read-only memory inside the processor in place of a 4 K core. There was no read-only memory in the machine that I saw.

The front panel was a printed circuit board. The switches looked reliable and there were some integrated circuits mounted right on the panel. There was no cabling in the machine that I saw therefore it's conjecture whether or not it is a single cable front panel. Mr. DeCastro said that quote, "it was full of MSI", "dual sourced", and the machine that was there was full of "Fairchild duds."

I have briefly looked at the programming structure of the Nova. Memory cycle timing is 2.6 micro seconds in the 4 K version. Read-only memory is no substantial advantage in speed (2.4 micro seconds.) Instruction execution time range from 3.9 micro seconds for an add to 2.6 micro seconds for a jump, most of them being 5 to 5.9 micro seconds in length.

The real advantage in the Nova organization is in the addressing structure, with multiple registers. The indexing is really not indexing. It is called base register addressing and 2 registers are provided for this. A total of four hardware registers can be addressed as accumulator registers- two of which are used as base registers. The scheme looks like it could provide very nice operation when you are passing perameters to subroutines and offers more indirect addressing space then the PDP-8. There are auto incrementing and auto decrementing locations in memory, 8 of each. The complication in the arithmetic and logical instructions is probably not necessary and probably of not much use. The ability to be able to shift when adding is of dubious value. In the brochure there is one fault in the addressing structure or one complication possibly that they were aware of. The machine uses true relative addressing. The effective address is added to the present PC count to determine the final effective address. However, the jump to subroutine instruction does not form the right address to make it a true relative addressing machine. This is often a problem since it requires a subtract operation to be carried out to form a correct relative return address. One of the advantages of relative

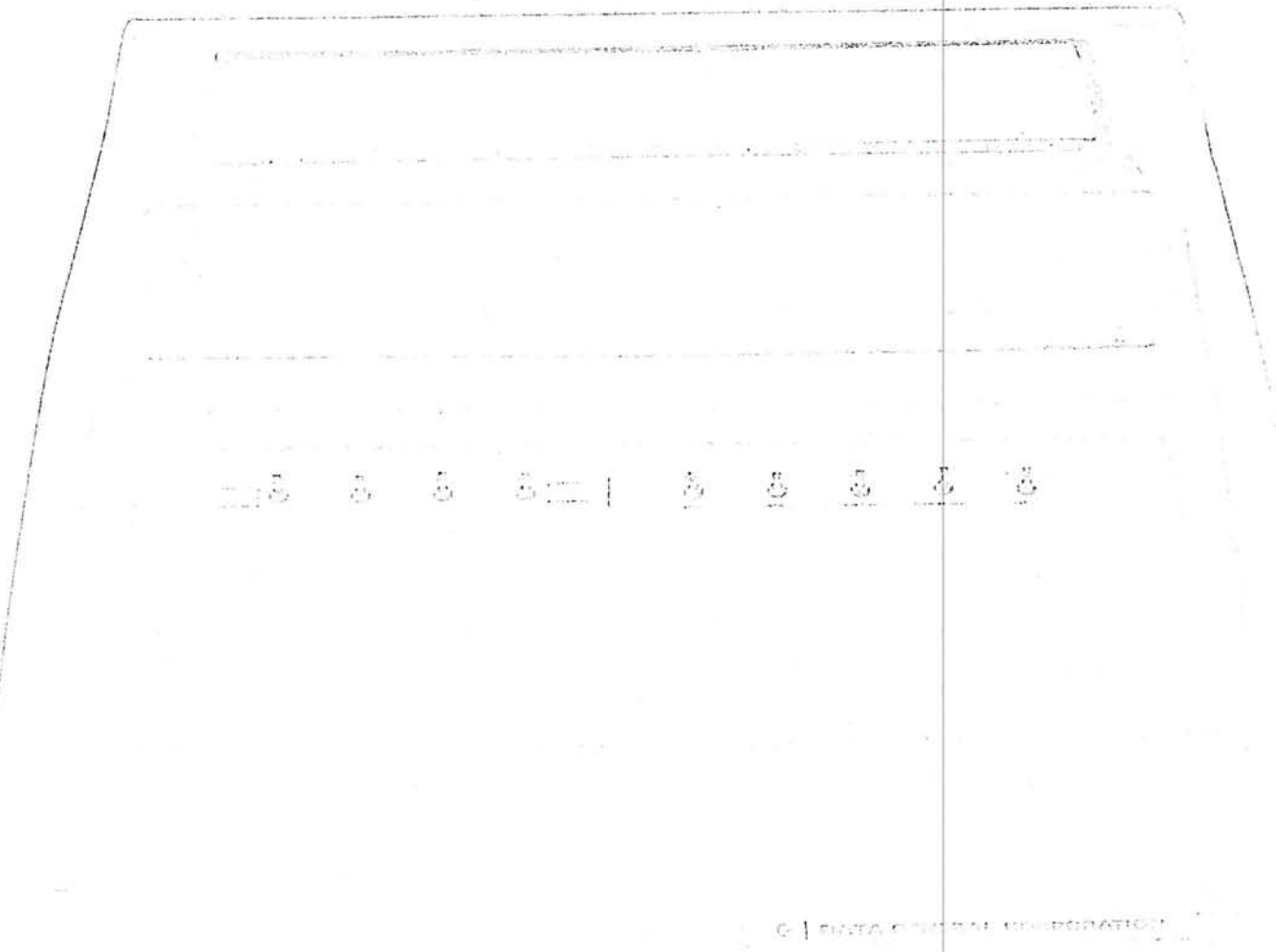
addressing is that programs can be loaded anywhere in core and they will work. If you have some absolute (non-relative) addresses in miscellaneous places in the program, then that program can not be swapped into a different core area. GE found this was a significant problem in the 4020 Process Control machines. This is also going to be a problem in Nova. However, the base register addressing is very nice when looking at tables etc.

There is a glowing omission in terms of input/output capabilities. They refer to high speed input/output but they don't tell you anything about it. I suspect that this is going to be an option in the processor. The brochure implies that program controlled transfers (AC I/O) is the only I/O in the basic machine.

As a brief summary I would say that the Nova instruction set is still a small computer instruction set (there are no compare instructions) essentially identical to the PDP-8. The memory references are slightly more flexible. The machine is considerably slower then a PDP-8. The input/output is considerably less flexible than a PDP-8 since it does not have the high speed data channel built into the basic machine. There is a definite error in the implementation of the relative addressing. There is also no byte addressing, although it is a 16 bit machine.

/bca

The best small computer in the world!



Edson D. de Castro, President, Data General Corporation

A hard look at small computers

Small computers are creating quite a stir.

You hear that they are being purchased faster than any other kind of computer. And that they are creating an applications explosion, expanding even their current rate of sales growth.

It seems manufacturers have not let this action go unnoticed. The expanding marketplace is encouraging a rush of new products. Old designs are being revamped. New designs are being rushed to market. The mini-computer boom is on.

But what is the boom producing? Is a growing market and increasing competition producing better computer value?

Well, the current crop of machines varies considerably. Word lengths vary. Input/output facilities vary. Instruction sets vary. Software varies. Performance varies.

We designed the NOVA believing that new technology and improvements in the art of computer design had offered the opportunity for vast improvements in the price/performance ratio of the minimum configuration of small general purpose digital computers.

But there were some things we had to know before we could take advantage of these opportunities.

We had to know that, mini-computer or not, the power of these machines stems from their performance as general purpose computers. That whatever they are used for, they would have to be programmed first. And that it was possible to so strip a computer of programming power that the machine could become more trouble than it was worth.

At the same time, we had to know that the special domain of these machines is in the on-line, real-time environment. That over half the small computers purchased are built into larger systems as special purpose data reducers and controllers.

I think you will find the NOVA to be a better small computer. We designed the system incorporating an architecture previously found only in medium and large scale third generation computers. This architecture permitted an extremely powerful instruction set. We took full advantage of medium scale integration. We were also able to design the NOVA around the special input/output and packaging requirements of the small computer. We designed a new kind of read-only memory interchangeable with core, for "black box" configurations.

You see, in designing and pricing the NOVA, we were after more than just getting a piece of the small computer action. We were after a machine that would be the basis for starting a major computer company. I think we succeeded. The NOVA is that good.

The hardware

As Ed has mentioned, the architecture of the NOVA had previously never been implemented in a small computer design. The breakthrough that made it possible was medium scale integration.

It now is possible to obtain sixteen flip-flops in a single package for use in regular registers; the cost per function of an MSI component is somewhat lower than the cost of discrete gates and flip-flops. But that is not MSI's major contribution. The big savings with MSI came from the reduction of interconnection and resultant savings in packaging costs. And, of course, the reduction of interconnection also had a very favorable effect on reliability. MSI accounts for over half the gates and flip-flops used in the NOVA.

And there are two kinds of memory available with the NOVA, core and read-only.

A user will create his read-only memory by writing his program using a core memory. He uses the full software of the system to write, edit, and debug his program. After he is satisfied with his program, he dumps it on paper tape and sends the tape to Data General. This tape is used as the basis for manufacturing the memory and verifying its contents. When complete, the read-only memory is simply plugged into the NOVA in place of the core memory. Should changes be required in the read-only memory they can easily be made by a technician.

These two kinds of memory are homogenous; the alterable and read-only storage are treated identically by the program and the processor. The only difference is that different kinds of memory vary in speed. But the two kinds of memory may be mixed. In a system in which only one program is being used, it can be stored along with its constants, in a read-only memory module. The alterable core memory can then be used for the storage of variable data and intermediary results. Or, the system console can be removed and the system operated as a hard wired controller. By changing read-only memories, the functions performed by this controller may be altered. Memories are available in 1K, 2K, or 4K word modules. The maximum memory size is 32K words or 64K bytes.

The read-write cycle times for the several core memory modules and the access time for read-only memory are as follows:

1K	6.5	micro-seconds
2K	3.9	
4K	2.6	
Read-only Memory	2.4	

In and out

Small computers interface with more kinds of devices with greater varying data rates and priority interrupt requirements than any other class of computer. Not only do they interface with the full range of computer peripherals, but they often become part of special or unique systems.

We decided to build a complete input/output facility into the basic NOVA. Included in the system are facilities for program interrupt and high speed data transfers with provision for direct access to memory. Any device can interrupt the normal program flow on a priority basis. A high speed device such as magnetic tape or disk can gain direct access to memory through a data channel without requiring the execution of any instructions. The data channel logic allows the transfer of data to or from memory, incrementing of memory word, and adding external data to a word already in memory. The latter two features facilitate such functions as signal averaging and pulse height analysis.

The NOVA I/O facility consists of 16 bi-directional data lines, 6 lines for device selection, 19 unary control lines from the central processor, and 6 control lines to the central processor. The control lines from the central processor are used to synchronize all data transfers on the data lines, to initiate and stop device functions, and to control the priority interrupt system. The control lines to the processor are used to indicate device status, and to request priority interrupt and data channel service.

The unary control lines from the processor contain two types of information: the specific function to be performed by the device, and timing information. These control lines are arranged in such a way that the device need connect only to those that correspond to the particular I/O functions that the device requires. The timing of the control lines is determined by the processor in such a fashion that the device does not require any time-dependent circuits to connect to the I/O interface.

The input/output system allows the program to address up to 62 external devices.

Instruction power

Most medium and large scale third generation computer systems have central processors organized around multiple general purpose registers or accumulators. The logical and arithmetic instructions of these machines are performed by manipulating the contents of these accumulators. There is less need to address or access memory. Also, the availablility of these multiple registers improves the efficiency of accumulator to memory operations and data flow between the computer and peripheral devices.

Until we designed the NOVA, small computers either had a single accumulator or assigned memory locations to simulate this organization, trading off much of the basic power of the set-up.

In the NOVA we have been able to fully implement a multi-accumulator central processor architecture. It is from this architecture that much of the power of the machine stems.

The NOVA has four full sixteen-bit word accumulators, two of which may be used as index registers. Data can be moved in either direction between any memory location and any NOVA accumulator. Although a word in memory can be incremented or decremented, all other arithmetic and logical operations are performed on operands in the accumulators, with the result appearing in an accumulator. Associated with the accumulators is a single carry flag, which indicates when the magnitude of the result is too large to be accommodated in a single accumulator. The left and right halves of any accumulator can be swapped, the contents of any accumulator can be tested for a skip, and the 17-bit word contained in any accumulator combined with the carry can be rotated right or left. An instruction that references memory can address two of the accumulators as index registers and transfers to and from peripheral devices are also made through the accumulators.

This multi-accumulator organization cuts down on the number of instructions necessary to execute a program. And reduces the amount of data movement in the machine. For example, in as trivial an operation as the exchanging of the contents of two memory locations, the multi-accumulator set-up reduces the number of instructions by one third.

Since an arithmetic or logical instruction does not contain a memory address, there are many bits that can be used for functions other than specifying the basic operation and the operands.

Arithmetic and logical instructions are frequently preceded by instructions which modify an operand and followed by a modification of the result and sometimes by a test. We felt that if these operations could be combined in a single instruction class, a much simpler to use and more powerful instruction structure would be achieved. We designed a class of instructions arranged so that each bit has its own function and thus it is unnecessary to decode most portions of the instruction word. The same instruction that adds or subtracts can also shift the result or swap its halves, test the result and /or carry for a skip, and specify whether or not the result shall actually be retained.

A single input /output instruction can transfer a word between an accumulator and a device and at the same time control the device operation.

The NOVA is much easier to program than single accumulator machines. The results of address calculations are immediately available for index purposes to the memory reference instructions. One accumulator can be used for in-out data transmission without disturbing others being used continually for computations. Complex software routines such as multiplication, division and floating point can be performed without constantly referencing memory.

Henry Burkhardt, III, Vice President, Data General Corporation

Software: first things first

Frankly, the basic NOVA software has been designed for the experienced computer user.

We knew that we would never stop developing new software packages and initially, we decided to concentrate on those things that were most integrally a part of the system.

The initial NOVA software includes a powerful assembler, a context oriented text editor, a multiple breakpoint debugger, complete hardware diagnostics, utility programs, and mathematical routines, including floating point arithmetic.

The NOVA assembler is a two pass system producing absolute binary and an assembly listing. Pseudo commands are provided to alter assembly origin, radix and to define new operation codes. Text may also be processed and packed into binary words. Input/output is fully buffered using the priority interrupt system, a binary search is used for the symbol table, and hence the assembly speed is I/O limited. The assembly language is free-form. The input need not be precisely formatted into columns as is required by many small computer assemblers. Control characters are used to delimit labels, comments and instruction fields. This provides greater freedom in the generation of program text as well as vastly reducing the errors due to missing spaces or blanks. The basic philosophy of the assembler has been to provide as few "default conditions" as possible. If it isn't entirely obvious what the user intended by a given line of code, the assembler will flag the line as questionable.

Since very few small computers are operated in an environment where program tape preparation and assembly services are available, a very high percentage of programming time is consumed in program assembling and editing. But no one is providing a text editing program that is both convenient to use and powerful enough for the experienced user.

Text editors are based upon the simple principle of reading a chunk of text into computer memory, modifying it through keyboard commands, and then outputting a corrected file. Most editors force the user to modify text at the line level — if a line of text has a single character error in it, the user must type the entire line over again. In addition, the actual addressing or locating of the errant text is a difficult process with the text editors available today. To overcome these problems, the NOVA text editor is organized around both line and character operations. Single characters, character strings, whole lines and multiple lines may be inserted, deleted or replaced with single keyboard commands. Text is readily located by means of string searches.

One of the programs that has been most neglected by the manufacturers of small computers is the debugging package. The existing packages are very limited in their permissible use of breakpoints. The user is constrained to use a single breakpoint, if any, and severe restrictions are placed upon the use of the breakpoint — it cannot be used with the machine's program interrupt hardware. The NOVA debugging packages allow the simultaneous operation of four breakpoints with no restrictions upon their placement or usage. The debugger also offers the traditional operations of memory examination and modification, binary punch-out, memory searches and dumps.

The physical construction of the NOVA opens several possibilities for the use of the debugger that have not been available before. Since the NOVA's 5¼" high enclosure can accommodate up to 16K words of core memory in addition to I/O interfaces, the OEM user has the ability to simply plug-in an additional memory module in which the debugging package may reside while checking out his program. The memory module can then be removed before shipment of the machine and applications program. If program bugs are uncovered during field usage of the system, a memory module with the debugger in it can be installed, the source of the bug identified and corrected, and the module removed.

Configuring your system

Small computers should come in any size you wish. The NOVA does.

A general purpose NOVA configuration has a central processor, console, power supply, 4096 sixteen-bit words of core memory and an interface for Teletype. But you can configure your system smaller than this. You can have as little as 1024 words of memory. You can make this memory read-only and remove the display console and have the least expensive computer controller you can buy.

Or you can gracefully expand the basic NOVA. You see, a big part of the total price of a small computer system is in the cost of packaging the system. The NOVA has as much room for expansion in the basic configuration as most customers will need.

The NOVA rack mount version takes up only 5¼ inches of a standard 19 inch rack. The desk top version is slightly larger and handsomer. Both can contain the same amount of hardware.

The NOVA, rack or desk model, contains space for seven printed circuit subassemblies. Each of these subassemblies are 15″ x 15″ with a 200 pin connector on one end and handles for insertion and removal on the other end.

The boards which are inserted in these slots may be any one of several system components. Two slots are used for the central processor. One slot is used for each memory module (4K, 2K, or 1K) added. One slot can contain an I/O option card which contains the control logic for several standard peripheral devices.

Thus, for a 4K system with Teletype, four slots are used and three are available for additional options, memory, and customer designed and built logic. Both the memory bus and the I/O bus are available at these slots so options or memory may be added by simply plugging in the appropriate sub-assembly. No extra wiring is required.

A 5¼″ tall NOVA expansion cabinet can be added to the basic NOVA. It also has the memory bus and I/O bus pre-wired to the slots using printed circuit wiring.

Service, pricing, and delivery

NOVA is backed by a generous guarantee and trained Data General service personnel. These regionally-based service personnel can set up just the kind of service arrangement you need.

They can recommend a back-up of NOVA spare parts and sub-assemblies so that you may never have to call him. You will be able to have your NOVA repaired through the mails at Data General's factory and not lose a minute of computer time.

When you get your NOVA we will teach you how to use it. Comprehensive training classes are available for NOVA programming and maintenance. You will receive complete documentation: User's Handbook, Interface and Installation, Software and Maintenance. You will also receive a documentation up-dating service including an expanding NOVA software library.

We were after a better performing computer and NOVA's performance exceeds that of any machine in its price class in every benchmark we have run. And we deliberately chose benchmarks that competitive manufacturers had been using to demonstrate the superiority of their particular machines.

We were after a lower priced computer and the price for the NOVA is very much lower for comparative configurations of each and every competitive machine — from the most stripped-down controller to general purpose systems with mass storage.

We know that over half the small computers purchased are purchased in quantity by the same customer. And that it costs us less to sell and service one hundred computers to one customer than to one hundred individual customers.

We also know that the way to lower the price of computers is to manufacture in volume.

So we are offering by far the best quantity and OEM discounts ever offered for small computers.

We believe the only way to go in this small computer business is big. So we're starting out to manufacture hundreds of NOVA's our first year. Our rapidly increasing rate of production will equal or exceed the fastest delivery rate of any small computer in the industry.

Soon we will be able to deliver NOVAs as fast as they are ordered. Until then, it's first order, first machine.

NOVA specifications and instructions

SPECIFICATIONS

NOVA is a 16-bit word general purpose computer. It has four accumulators, two of which may be used as index registers. It offers a choice of core or read-only memory of 1K, 2K, 4K, 8K, and up to 32K 16-bit words (or twice that many 8-bit bytes). NOVA comes in desk top console or a 5¼" tall standard rack mount package. Both the desk and rack versions can hold up to 20K 16-bit words of memory or interfaces for a large number of peripheral devices. NOVA has the most flexible I/O facility ever built into a machine of its class. It includes a high-speed Data Channel and automatic interrupt source identification as standard equipment.

Electrical specifications

Power Requirements
90 to 250 volts, 40 to 440 Hz single phase power capable of supplying approximately 5 amperes.

Receptacle required to receive standard three wire plug.

Power Dissipation
400 watts.

I/O Bus Levels
Ground and +5 volts (standard TTL integrated circuit logic levels).

Environmental specifications

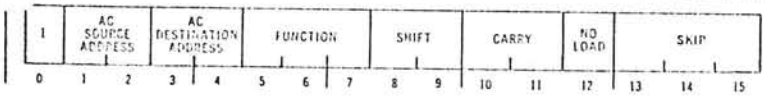
Operating Temperature
0°C to 50°C.

Relative Humidity
To 90%.

INSTRUCTIONS

ARITHMETIC AND LOGICAL INSTRUCTIONS

An instruction that has a 1 in bit 0 performs one of eight arithmetic and logical functions as specified by bits 5--7 of the instruction word. The function, which may be anything from a simple move to a subtraction, always uses the contents of the accumulator specified by bits 1 and 2; and if a second operand is required, it comes from the accumulator addressed by bits 3 and 4.



The instruction also supplies a carry bit to the shifter with the result. Bits 10 and 11 specify a base value to be used in determining the carry bit. The instruction supplies either this value or its complement depending upon both the function being performed and the result it generates. The mnemonics and bit configurations and the base values they select are as follows.

Mnemonic	Bits 10--11	Base valve for carry bit
	00	Current state of carry
Z	01	Zero
C	10	Complement of current state of carry
O	11	One

The three logical functions simply supply the listed value as the carry bit to the shifter. The five arithmetic functions supply the complement of the base value if the operation produces a carry out of bit 0; otherwise they supply the value given. The carry bit can be used in conjunction with the sign of the result to detect overflow in operations on signed numbers. But its primary use is as a carry out of the most significant bit in operations on unsigned numbers, such as the lower order parts in multiple precision arithmetic.

The 17-bit word consisting of the carry bit and the 16-bit result is operated on by the shifter as specified by bits 8 and 9.

Mnemonic	Bits 8--9	Shift operation
	00	None
L	01	Left rotate one place. Bit 0 is rotated into the carry position, the carry bit into bit 15
R	10	Right rotate one place. Bit 15 is rotated into the carry position, the carry bit into bit 0
S	11	Swap the halves of the 16-bit result. The carry bit is not affected

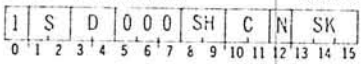
The shifter output is also tested for a skip according to the condition specified by bits 13--15. The processor skips the next instruction if the specified condition is satisfied.

Mnemonic	Bits 13--15	Skip function
	0	Never Skip
SKP	1	Always Skip
SZC	2	Skip on Zero Carry
SNC	3	Skip on Nonzero Carry
SZR	4	Skip on Zero Result
SNR	5	Skip on Nonzero Result
SEZ	6	Skip if Either Carry or Result is Zero
SBN	7	Skip if Both Carry and Result are Nonzero

Arithmetic and Logical Functions

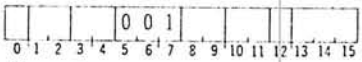
The eight functions are selected by bits 5--7 of the instruction word. For convenience the accumulators addressed by the S and D parts of the instruction are referred to as ACS and ACD.

COM Complement 5.6 μs



Place the (logical) complement of the word from ACS and the carry bit specified by C in the shifter. Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

NEG Negate 5.6 μs



Place the twos complement of the number from ACS into the shifter. Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

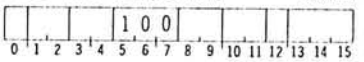
MOV Move 5.6 μs

Place the contents of ACS and the carry bit specified by C in the shifter. Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

INC Increment 5.6 μs

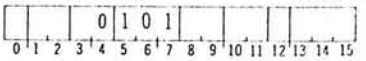
Add 1 to the number from ACS and place the result in the shifter. Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

ADC Add Complement 5.9 μs



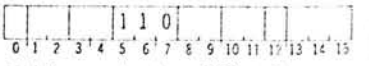
Add the (logical) complement of the number from ACS to the number from ACD, and place the result in the shifter. Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

SUB Subtract 5.9 μs



Subtract by adding the twos complement of the number from ACS to the number from ACD, and place the result in the shifter. If the signs of the operands are the same and ACD ≥ ACS, or the signs differ and ACD is negative, supply the complement of the value specified by C as the carry bit; otherwise supply the specified value. (For unsigned numbers the carry condition is simply that ACD ≥ ACS.) Perform the shift operation specified by SH. Load the shifter output in carry and ACD unless N is 1. Skip the next instruction if the shifter output satisfies the condition specified by SK.

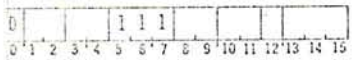
ADD Add 5.9 μs



Add the number from ACS to the number from ACD, and place the result in the shifter. If both summands are negative, or their signs differ and their magnitudes are equal or the positive one is the greater in magnitude, supply the complement of the value specified by C as the carry bit; otherwise

upply the specified value. (For unigned numbers the carry condition s simply that the sum is ≥ 2^{16}.) Perorm the shift operation specified by SH. Load the shifter output in carry nd ACD unless N is 1. Skip the next nstruction if the shifter output satisfies he condition specified by SK.

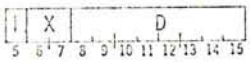
ND And 5.9 μs



Place the logical and function of the wo from ACS and the word from ACD n shifter. Supply the value specified by C as the carry bit. Perform the shift operation specified by SH. Load he shifter output in carry and ACD nless N is 1. Skip the next instruction f the shifter output satisfies the condition specified by SK.

EMORY REFERENCE INSTRUCTIONS

Bits 5–15 have the same format in very memory reference instruction whether the effective address is used for storage or retrieval of an operand or to alter program flow. Bit 5 is the indirect bit, bits 6 and 7 are the index

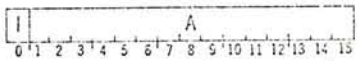


bits, and bits 8–15 are the displacement. The effective address E of the instruction depends on the values of I, X, and D. If X is 00, D addresses one of the first 256 memory locations, i.e., D is a memory address in the range 00000–00377. This group of locations is referred to as page zero.

If X is nonzero, D is a displacement that is used to produce a memory address by adding it to the contents of the register specified by X. The displacement is a signed binary integer in two's complement notation. Bit 8 is the sign (0 positive, 1 negative), and the bits in the octal range —200 to +177 (decimal —128 to +127). If X is 01, the instruction addresses a location relative to its own position, i.e., relative to the address in PC, which is the address of the instruction being executed. This is referred to as relative addressing. If X is 10 or 11 respectively, it selects AC2 or AC3 as a base register to which D is added.

X	Derivation of address
00	Page zero addressing. D is an address in the range 00000–00377.
01	Relative addressing. D is a signed displacement (—200 to +177) that is added to the address in PC.
10	Base register addressing. D is a signed displacement (—200 to +177) that is added to the address in AC2.
11	Base register addressing. D is a signed displacement (—200 to +177) that is added to the address in AC3.

If I is 0, addressing is direct, and the address already determined from X and D is the effective address used in the execution of the instruction. Thus a memory reference instruction can directly address 1024 locations: 256 in page zero, and three sets of 256 in the octal range 200 less than to 177 greater than the addresses in PC, AC2 and AC3. If I is 1, addressing is indirect, and the processor retrieves another address from the location specified by the address already determined. In this new word bit 0 is the indirect bit: bits 1–15 are the effective address if bit 0 is 0; otherwise they specify a location



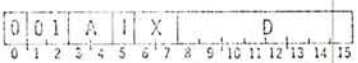
for yet another level of address retrieval. This process continues until some referenced location is found with a 0 in bit 0; bits 1–15 of this location are the effective address E.

If at any level in the effective address calculation an address word is fetched from locations 00020–00037, it is automatically incremented or decremented by one, and the new value is both written back in memory and used either as the effective address or for the next step in the calculation depending on whether bit 0 is 0 or 1. Addresses taken from locations 00020–00027 are incremented, those from locations 00030–00037 are decremented.

Move Data Instructions

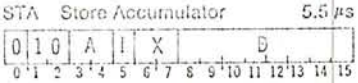
These two instructions move data between memory and the accumulators. In the descriptions of all memory reference instructions, *E* represents the effective address. The time given in the top line is for direct addressing, in page zero or relative to PC. Base register addressing requires an additional .3 μs; indirect addressing requires one extra memory cycle time per level; autoincrementing and autodecrementing require no extra time.

LDA Load Accumulator 5.2 μs



Load the contents of location E into accumulator A. The contents of E are unaffected, the original contents of A are lost.

STA Store Accumulator 5.5 μs

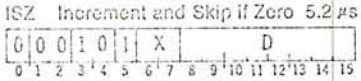


Store the contents of accumulator A in location E. The contents of A are unaffected, the original contents of E are lost.

Modify Memory Instructions

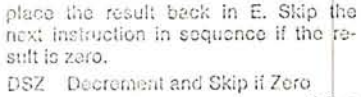
These two instructions alter a memory location and test the result for a skip. They are used to count loop iterations or successively modify a word for a series of operations.

ISZ Increment and Skip if Zero 5.2 μs



Add 1 to the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

DSZ Decrement and Skip if Zero 5.2 μs

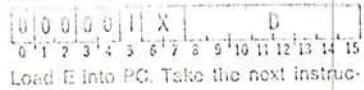


Subtract 1 from the contents of location E and place the result back in E. Skip the next instruction in sequence if the result is zero.

Jump Instructions

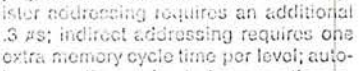
These two instructions allow the programmer to alter the normal program sequence by jumping to an arbitrary location. They are especially useful for calling and returning from subroutines.

JMP Jump 2.6 μs



Load E into PC. Take the next instruction from location E and continue sequential operation from there.

JSR Jump to Subroutine 3.5 μs



Load an address one greater than that in PC into AC3 (hence AC3 receives the address of the location following the JSR instruction). Load E into PC. Take the instruction from location E and continue sequential operation from there. The original contents of AC3 are lost.

INPUT-OUTPUT INSTRUCTIONS

Instructions in the in-out class govern all transfers of data to and from the peripheral equipment, and also perform various operations within the processor. An instruction in this class is designated by 011 in bits 0–2. Bits 10–15 select the device that is to respond to the instruction. The format thus allows for 64 codes of which 62 can be used to address devices (octal 01–76). The code 00 is not used, and 77 is used for a number of special functions including reading the console data switches and controlling the program interrupt.

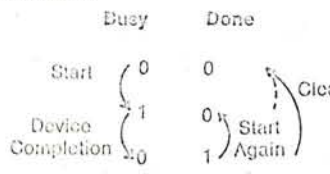
Every device has a 6-bit device selection network, an Interrupt Disable flag, and Busy and Done flags. The selection network decodes bits 10–15 of the instruction so that only the addressed device responds to signals sent by the processor over the in-out bus. The Busy and Done flags together denote the basic state of the device. When both are clear the device is idle. To place the device in operation, the program sets Busy. If the device will be used for output, the program must give a data-out instruction that sends the first unit of data — a word or character depending on how the device handles information. (The word "output" used without qualification always refers to the transfer of data from the processor to the peripheral equipment; "input" refers to the transfer in the opposite direction.) When the device has processed a unit of data, it clears Busy and sets Done to indicate that it is ready to receive new data for output, or that it has data ready for input. In the former case the program would

respond with a data-out instruction to send more data; in the latter with a data-in instruction to bring in the data that is ready. If the Interrupt Disable flag is clear, the setting of Done signals the program by requesting an interrupt; if the program has set Interrupt Disable, then it must keep testing Done or Busy to determine when the device is ready.

In all in-out instructions bits 8 and 9 either control or sense Busy and Done. In those instructions in which bits 8 and 9 specify a control function, the mnemonics and bit configurations and the functions they select are as follows.

Mnemonic	Bits 8–9	Control function
	00	None
S	01	Start the device by clearing Done and setting Busy.
C	10	Clear both Busy and Done, idling the device.
P	11	Pulse the special in-out bus control line — the effect, if any, depends on the device.

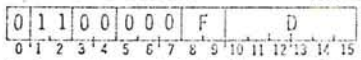
The overall sequence of Busy and Done states is determined by both the program and the internal operation of the device.



The data-in or data-out instruction that the program gives in response to the setting of Done can also restart the device. When all the data has been transferred the program generally clears Done so the device neither requests further interrupts nor appears to be in use, but this is not necessary. Busy and Done both set is a meaningless situation.

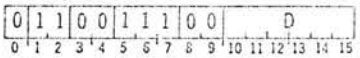
Bits 5–9 specify the complete function to be performed. If there is no transfer (bits 5–7 all alike), bits 3 and 4 are ignored and bits 8 and 9 may specify a control function or a skip condition.

NIO No I/O Transfer 4.4 μs



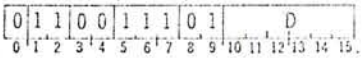
Perform the control function specified by *F* in device *D*.

SKPBN Skip if Busy is Nonzero 4.4 μs



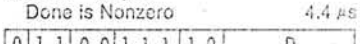
Skip the next instruction in sequence if the Busy flag in device *D* is 1.

SKPBZ Skip if Busy is Zero 4.4 μs



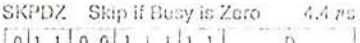
Skip the next instruction in sequence if the Busy flag in device *D* is 0.

SKPDN Skip if Done is Nonzero 4.4 μs



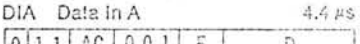
Skip the next instruction in sequence if the Done flag in device *D* is 1.

SKPDZ Skip if Busy is Zero 4.4 μs



Skip the next instruction in sequence if the Done flag in device *D* is 0.

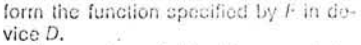
DIA Data In A 4.4 μs



Move the contents of the A buffer in device *D* to accumulator *AC*, and perform the function specified by *F* in device *D*.

The number of data bits moved depends on the size of the device buffer, its mode of operation, etc. Bits in *AC* that do not receive data are cleared.

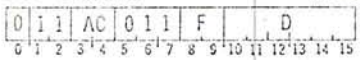
DOA Data Out A 4.7 μs



Send the contents of accumulator *AC* to the A buffer in device *D*, and perform the function specified by *F* in device *D*.

The amount of data actually accepted by the device depends on the size of its buffer, its mode of operation, etc. The original contents of *AC* are unaffected.

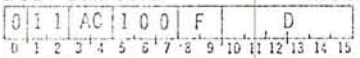
DIB Data In B 4.4 μs



Move the contents of the B buffer in device *D* to accumulator *AC*, and perform the function specified by *F* in device *D*.

The number of data bits moved depends on the size of the device buffer, its mode of operation, etc. Bits in *AC* that do not receive data are cleared.

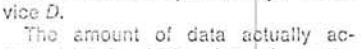
DOB Data Out B 4.7 μs



Send the contents of accumulator *AC* to the B buffer in device *D*, and perform the function specified by *F* in device *D*.

The amount of data actually accepted by the device depends on the size of its buffer, its mode of operation, etc. The original contents of *AC* are unaffected.

DIC Data In C 4.4 μs



Move the contents of the C buffer in device *D* to accumulator *AC*, and perform the function specified by *F* in device *D*.

The number of data bits moved depends on the size of the device buffer, its mode of operation, etc. Bits in *AC* that do not receive data are cleared.

DOC Data Out C 4.7 μs

Send the contents of accumulator *AC* to the C buffer in device *D*, and perform the function specified by *F* in device *D*.

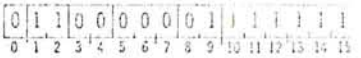
The amount of data actually accepted by the device depends on the size of its buffer, its mode of operation, etc. The original contents of *AC* are unaffected.

Special Code-77 Functions

In-out instructions with the code 77 in bits 10–15 perform a number of special functions rather than controlling a specific device. In all but the skip instructions bits 8 and 9 are used to turn the interrupt on and off. The mnemonics are the same as those for controlling Busy and Done in I/O devices but with code 77 they select the following special functions.

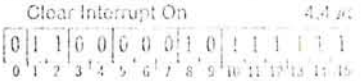
Mnemonic	Function
S	Set the Interrupt On flag to enable the processor to respond to interrupt requests.
C	Clear the Interrupt On flag to prevent the processor from responding to interrupt requests.
P	None.

NIOS CPU Set Interrupt On 4.4 μs



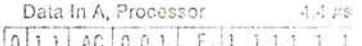
Set the Interrupt On flag to allow the processor to respond to interrupt requests.

NIOC CPU Clear Interrupt On 4.4 μs



Clear the Interrupt On flag to prevent the processor from responding to interrupt requests.

DIA AC,CPU Data In A, Processor 4.4 μs

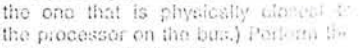


Read the contents of the console data switches into accumulator *AC*, and perform the function specified by *F*.

DIB AC,CPU Data In B, Processor 4.4 μs

Place in accumulator *AC* the device code of the first device on the bus that is requesting an interrupt ("first" means the one that is physically closest to the processor on the bus.) Perform the function specified by *F*.

DOB AC,CPU Data Out B, Processor 4.7 μs

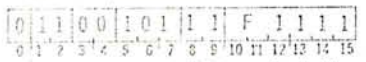


Set up the Interrupt Disable mask in the devices according to the word in accumulator *AC*. For this purpose each device is connected to a given bit

NOVA Options

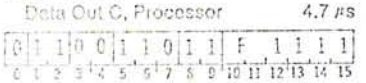
line, and its flag is set or cleared as the corresponding bit in the mask is 1 or 0. Perform the function specified by *F*.

DIC 0,CPU
Data In C, Processor 4.4 μs



Clear the control flipflops, including Busy, Done and Interrupt Disable, in all devices connected to the bus. Perform the function specified by *F*.

DOC 0,CPU
Data Out C, Processor 4.7 μs

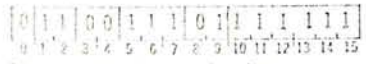


Perform the function specified by *F*, and then halt the processor.

SKPBN CPU Skip If
Busy is Nonzero, Processor 4.4 μs

Skip the next instruction in sequence if the Interrupt On flag is 1.

SKPBZ CPU Skip If
Busy is Zero, Processor 4.4 μs



Skip the next instruction in sequence if Interrupt On is 0.

The assembler recognizes a number of convenient mnemonics for instructions with device code 77.

Mnemonic Meaning	Mnemonic Equivalent		Octal Equivalent
Read Switches	DIA	---,CPU	060477
IO Reset	DICC	0,CPU	062577
Halt	DOC	0,CPU	063077
Interrupt Enable	NIOS	CPU	060177
Interrupt Disable	NIOC	CPU	060277
Interrupt Acknowledge	DIB	---,CPU	061477
Mask Out	DOB	---,CPU	062077

1K Read-Only Memory Module
(1024 words of 16 bits each)
Includes 1K words (2K bytes) of Read-Only Memory which is interchangeable with the alterable core memory with no wiring modifications required. The contents of this module can be either standard programs or special customer specified programs.

NOVA Central Processor — Rack Mountable
Includes central processor, console (with lock), high-speed data channel, power supply, five subassembly slots available in basic frame. This basic frame is rack mountable in a standard 19" rack with slides.

NOVA Central Processor — Table Top Model
Includes central processor, console (with lock), high-speed data channel power supply, five subassembly slots available in basic frame. This basic frame is enclosed in a cabinet designed for table top use.

4K Core Memory
(4096 words of 16-bits each)
Includes 4K words (8K bytes) of memory with all necessary electronics mounted on a single subassembly (15"x15" printed circuit card) which can be plugged directly into one of the slots in the basic frame with no wiring modifications required.

2K Core Memory
(2048 words of 16 bits each)
Includes 2K words (4K bytes) of memory mounted on a single subassembly (15"x15" printed circuit card) which can be plugged directly into one of the slots in the basic frame with no wiring modifications required.

1K Core Memory
(1024 words of 16 bits each)
Includes 1K words (2K bytes) of memory mounted on a single subassembly (15"x15" printed circuit card) which can be plugged directly into one of the slots in the basic frame with no wiring modifications required.

Expansion Enclosure
This item is a basic frame with a power supply and slots to mount seven (7) subassemblies. This unit is typically mounted directly above the central processor frame and is used to mount additional memory (alterable core or Read Only), additional I/O controllers, or special customer designed hardware.

Power Monitor and Auto Restart
Provides power level detection and a flag which is attached to the Program interrupt and can be sensed by the program. Its function is to allow the program to become aware of an imminent power failure so it can provide for an orderly shut down. The program automatically restarts at location 0.

Real-Time Clock
This option provides a flag which can be enabled by the program to provide a program interrupt at a fixed frequency. Either the AC line or a crystal clock may be specified as the time source.

Teletype Input/Output Interface
This option provides an interface to any one of the Teletype models listed below:

Teletype ASR33
Keyboard/printer, 8 channel reader/punch, 10 char./sec.

Teletype KSR33
Keyboard/printer, 10 char./sec.

Teletype KSR35
Keyboard/printer, 10 char./sec.

Teletype KSR37
Keyboard/printer (upper/lower case), 15 char./sec.

High-Speed Perforated Tape Reader and Control
Paper tape reader and control which senses eight channel, fan fold perforated Mylar or paper tape photo-[illegible] at 150 or 300 characters

High-Speed Perforated Tape Punch and Control
BRPE11 Punch and Control which punches eight channel fan fold paper tape at 63.3 characters per second.

Cathode Ray Tube Display and Control
This equipment includes a Tektronix Type 602 5" Rectangular Display and a control interface operating in a point plotting mode (256 points x 256 points) using the Data Channel for display refresh.

Medium-Speed Line Printer and Control
This option includes a Potter Medium-Speed Line Printer Type HSP3502 and control. This is a chain printer with a full ASCII interface including paper advance (LF, FF) characters.

Card Reader and Control
Soroban SCCR card reader and control which operates at 225, 400 or 600 cards per minute.

Incremental Plotter
Plotters and control interfaces to units made by two different manufacturers. 1) The California Computer Products 500 Series units (Drum or Flat Bed Style). 2) The Houston Instruments Complot DP-1 Digital Plotter which uses "Z fold" style paper.

In addition, the following devices will be available: magnetic disk, incremental tape, IBM compatible magnetic tape, and a complete line of A/D and D/A equipment.

digital INTEROFFICE MEMORANDUM

DATE: 12/10/68

SUBJECT: MAIL ROOM PROPOSAL

TO: OPERATIONS COMMITTEE FROM: Nick LoRusso/Frank Kalwell

We have discussed the problem of moving material and mail through Digital and have agreed that, at least for the present, our mail problem should be handled separately. We therefore suggest the following steps be taken to improve our mail service.

RELOCATION:

We feel the mail room should be moved to a more central location, Build. 4, Floor 3. The mail room would be located adjacent to where our office staff is concentrated, Build. 5. Since we are grouping our other services in Build. 4, this location is more desirable because it is close to stationary, forms inventory, publications inventory, and communications. The mail can be a means of moving material and messages to our staff. Amount of square footage required in Bldg. 4, Floor 3, is , 2,000 square ft.

DELIVERIES:

Five deliveries a day is desirable. For many of us, the mail is a source of work. This would even out the flow of mail and insure a quick response for interdepartmental requests.

TYPE OF DELIVERY:

At the present, the mail is delivered directly to the addressee. This makes the job of mail delivery more complex, slows down delivery, and increases the margin of error. It also makes the job of training messengers more difficult. By the very nature of a mail room, it is usually plagued with a high rate of turnover. The job must be kept as simple as possible. We therefore suggest each floor in each building be served by one centrally located incoming mail box. The boxes could be of a rack type or of a lock box type. The reasoning is, since our employees frequently leave their desks, it would not be inconvenient for them to pick up and drop off their mail at one of these boxes. This would greatly simplify the job of delivering the mail. Present amount of mail stops

on a one run basis at DEC is 84 vs. 14 proposed by one central located incoming mail box. If such a proposal is accepted the 80% time savings would enable the mail department to achieve 5 deliveries per day.

MANPOWER:

1 Supervisor
2 Messengers
1 Aid Girl
1 Part time employee

We suggest the mail room manpower be increased by one. Since the group is not heavily staffed and cannot draw on manpower from other areas, we should cover for growth and absenteeism.

At the present time the Mail Services Department can operate under the Traffic Budget, but if and when the Offices Services is settled, perhaps such function can be considered part of this group. Where the main concern was proximity of mail vs. office services, this should be accomplished by the proposed move and are certain such mail area can function economically and effectively.

Ken

digital INTEROFFICE MEMORANDUM

DATE: December 31, 1968

SUBJECT: MONTHLY PLANNING REPORT

TO: Operations Committee FROM: D. Kicilinski

Attached you will find digests of the monthly planning report.

Included are:

Finished Computer & Peripherals Available For Sales As Of 11/22
Summary Backlog As Of 12/6
Summary Backlog As Of 11/15
Revised Eight-Month Manufacturing Forecast
Revised Ship Versus Build Report

/kb
Attachments (2)

Pete Vanlyzz

FINISHED COMPUTER SYSTEMS AND PERIPHERALS AVAILABLE FOR SALE AS OF 11/22/68

Option or Model Number	"Z" 1613 Quantity	"Z" 1616 Quantity	Cust. Cons. 1608 Quantity	Cust. Cons. 1609 Quantity	Demo's 1612 Quantity	1617 Quantity	Sales Value	Total Mfg. Cost Quantity
PDP-8/L	--	6	--	--	1	--	59.5	7
PDP-8	7	3	3	2	35	--	1030.0	50
PDP-8/S	3	2	4	2	19	--	300.0	30
PDP-8/I	2	13	4	--	34	--	678.4	53
(Plus Teletypes)	--	2	--	--	53	--	66.0	55
Linc-8	1	3	2	--	7	--	500.5	13
PDP-9	4	2	1	--	30	--	1295.0	37
PDP-9/L	--	--	1	--	--	--	19.9	1
DM01	3	2	--	1	12	--	48.6	18
TC58	1	1	1	--	4	--	70.0	7
182	1	2	1	1	1	--	21.0	6
183	5	4	3	--	9	--	31.5	21
184	5	6	3	1	10	--	187.5	25
189	5	--	--	--	2	--	10.5	7
804 7 PCO	25/11	5/10	1/3	2/2	27/52	--	241.8	60/78
DF32	2	4	7	--	20	3	216.0	36
DS32	--	1	6	--	11	1	57.0	19
AF0	10	7	1	--	2	2	99.0	22
TC01	--	5	2	--	9	3	140.6	19
TC02	3	2	2	--	12	--	140.6	19
TU20	--	1	1	1	5	--	96.0	8
TU55	6	23	12	5	60	10	278.4	116
OMD8S	1	1	--	--	1	--	4.5	3
ODB8s	2	1	--	--	3	--	6.0	6
OMC8S	1	--	--	--	--	--	3.5	1
MC08I	1	4	1	--	8	5	95.0	19
DM09A	1	--	--	--	6	--	28.0	7
KE09A	5	4	--	--	25	--	136.0	34
KF09A	4	2	--	--	10	--	80.0	16
TC59	--	2	--	--	4	--	60.0	6
RC09	--	1	--	--	--	--	6.0	1
RM09	--	1	--	--	1	--	15.6	2
550	--	1	--	--	--	--	24.6	1
555	--	--	--	1	--	--	7.4	1
AA01A	5	2	--	--	--	--	11.2	7
149B	--	2	--	--	--	--	65.4	2
MM8I	--	--	--	--	2	--	24.0	2
545	--	--	--	--	1	--	12.0	1
LT09A	1	1	--	--	3	--	6.0	5

Option or Model Number	"Z" 1613 Quantity	"Z" 1616 Quantity	Cust. Cons. 1608 Quantity	Cust. Cons. 1609 Quantity	Demo's 1612 Quantity	1617 Quantity	Sales Value	Total Mfg. Cost Quantity
LT08	==	--	--	--	1	--	1.2	1
AX08A	--	--	--	--	1	--	4.1	1
338	--	--	--	--	2	--	78.0	2
685	--	--	--	--	1	--	4.3	1
PT08	--	--	--	--	23	6	23.2	29
							6,283.8	

December 19, 1968
W. Hanson

COMPANY CONFIDENTIAL

BACKLOG W/E 12/6/68

P/L	Total Bklg.	Late Bklg.	In-Def.	3RD QTR. Dec	Jan	Feb	Mar	4TH QTR. Apr	May	Jun	Remaining
PDP-1	36	6	--	19	--	--	12	--	--	--	--
PDP-4	None	--	--	--	--	--	--	--	--	--	--
PDP-5	8	8	--	--	--	--	--	--	--	--	--
PDP-6	87	2	--	--	5	--	30	--	--	50	--
PDP-7	154	78	--	46	15	2	--	12	--	--	--
PDP-8	1,415	399	110	474	265	48	72	--	14	13	--
PDP-9	3,312	286	109	1,247	456	295	335	74	171	--	338
PDP-10	16,454	5,795	681	2,056	1,377	2,090	1,019	1,030	981	2,073	335
26/8I	7,670	1,497	202	1,872	1,660	915	593	349	355	102	128
27/8L	3,279	240	9	764	718	650	308	65	140	147	242
28/8S	330	80	30	112	76	20	4	--	--	--	7
29/9L	81	19	--	62	--	--	--	--	--	--	--
38/Linc	474	44	6	285	1	57	81	--	--	--	--
50/Modules	978	218	487	188	49	2	1	2	1	30	--
Total	34,278	8,672	1,634	7,125	4,622	4,079 11,156	2,455	1,532	1,662 5,609	2,415	1,070
W/E 11/15/68	34,294	7,139	1,568	4,453	3,772	3,684 9,209	1,753	1,376	1,292 4,468	1,800	623

November 20, 1968

SUMMARY BACKLOG W/E 11/15/68

P/L	Total Bklg.	Late Bklg.	Floating	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	1st + Remaining
PDP-1	287	248	9	---	19	---	---	12	---	---	---	---
PDP-5	8	3	---	5	---	---	---	---	---	---	---	---
PDP-6	83	51	---	3	---	---	---	30	---	---	---	---
PDP-7	154	9	---	127	---	5	1	---	12	---	---	---
PDP-8	1,426	413	113	230	379	235	29	---	---	14	13	---
PDP-9	3,617	781	143	1,244	669	318	207	84	59	112	---	---
PDP-10	16,841	3,530	445	2,657	1,290	1,377	2,646	989	1,030	981	1,540	356
26/8I	7,506	1,482	321	1,787	1,245	1,119	451	471	241	145	102	142
27/8L	2,678	178	22	527	536	613	332	160	32	40	114	124
28/8S	376	117	30	70	58	81	16	4	---	---	---	---
29/9L	---	---	---	---	---	---	---	---	---	---	---	---
38/Linc	362	72	3	54	215	18	---	---	---	---	---	---
Modules	956	255	482	132	42	6	2	3	2	---	31	1
Total	34,294	7,139	1,568	6,836	4,453	3,772	3,684	1,753	1,376	1,292	1,800	623
W/E 10/11 Total	30,538	5,165	1,837	5,030	2,971	2,379	1,856	1,082	←	3,234	→	2,028

December 19, 1968

COMPANY CONFIDENTIAL

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EIGHT-MONTH MANUFACTURING FORECAST
$ Value of Planned Production by Quarters

	2nd Qtr. '69	3rd Qtr. '69	4th Qtr. '69
8 Family	10,168.8	14,081.8	12,821.1
9 Family	4,081.7	4,375.2	3,505.4
10	7,198.4	9,969.0	11,190.0
Linc	946.4	1,771.4	3,287.8
'N'	144.8	335.5	204.0
Module Sales	1,935.0	2,844.0	2,962.0
Total	24,475.1	33,376.9	33,970.3

LATEST EIGHT-MONTH PROJECTION

	December	January	February	March	April	May	June	July	Total
8 Family	4,083.6	4,590.8	4,853.2	4,637.8	4,376.7	4,251.7	4,192.7	4,238.0	35,224.5
9 Family	1,353.3	1,340.9	1,474.1	1,560.2	1,424.4	1,091.8	989.2	889.0	10,122.9
10	2,650.0	3,024.0	3,400.0	3,545.0	3,645.0	3,645.0	3,800.0	3,700.0	27,509.0
Linc	449.4	576.6	537.3	657.5	1,083.0	1,127.6	1,077.2	1,044.6	6,553.2
'N'	72.0	111.5	89.5	134.5	70.0	81.6	52.4	100.0	711.5
Modules	580.0	830.0	980.0	1,034.0	894.0	944.0	1,124.0	944.0	7,330.0
Total	9,188.3	10,473.8	11,334.1	11,569.0	11,493.1	11,241.7	11,235.5	10,915.6	87,451.1

SHIP VERSUS BUILD

December 30,1968

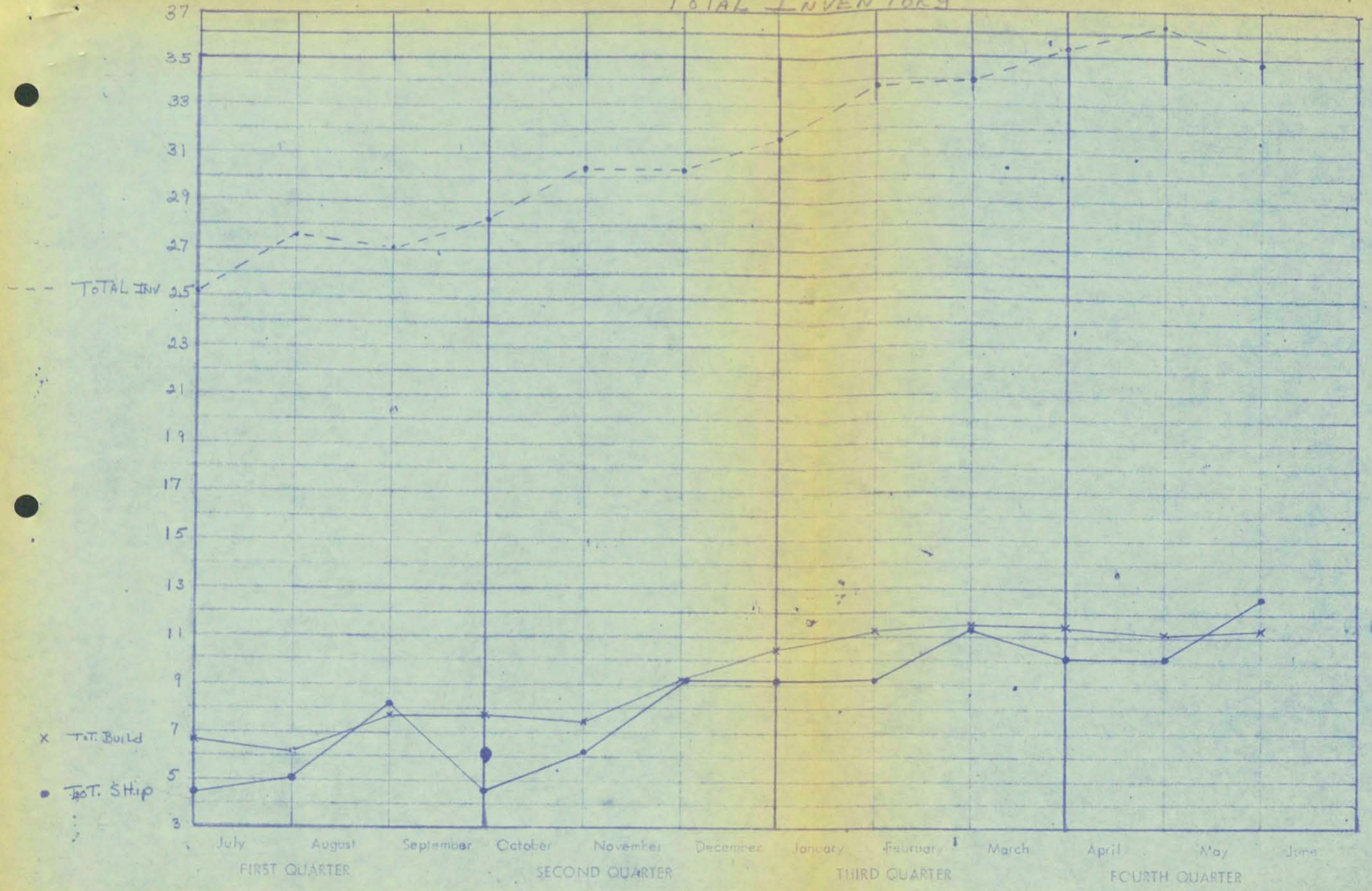
Product Line		Fin. Goods	WIP Inv.	Total Ending Inven.	December Build	December Ship	December End. Inv.	January Build	January Ship	January End. Inv.	February Build	February Ship	February End. Inv.	March Build	March Ship	March End. Inv.
8	**A	3,787	6,265	10,052	4,084	3,620	10,516	4,591	3,540	11,567	4,853	3,540	12,880	4,638	4,420	13,098
	B	2,680	6,100	8,780			8,830									8,830
9	A	1,897	4,713	6,610	1,353	1,400	6,563	1,341	1,320	6,584	1,474	1,320	6,738	1,560	1,660	6,638
	B	1,360	4,600	5,960			6,060									6,100
10	A	0	9,716	9,716	2,650	2,800	9,566	3,024	3,020	9,570	3,400	3,020	9,950	3,545	3,770	9,725
	B	300	6,600	6,900			7,500									8,250
Linc	A	501	353	854	449	200	1,103	577	161	1,519	537	161	1,895	658	203	2,350
	B	500	250	750			625									875
Trad.	A	100	471	571	72	240	403	112	130	385	90	130	345	135	165	315
	B		420	420			500									700
Mod.	A	1,948	611	2,559	580	900	2,239	830	985	2,084	980	985	2,079	1,034	1,230	1,883
	B	1,125	640	1,765			2,015									2,425
Total	A	8,233	22,129	30,362	9,188	9,160	30,390	10,475	9,156	31,709	11,334	9,156	33,887	11,570	11,448	34,009
	B	5,965	18,610	24,575			25,530									27,240

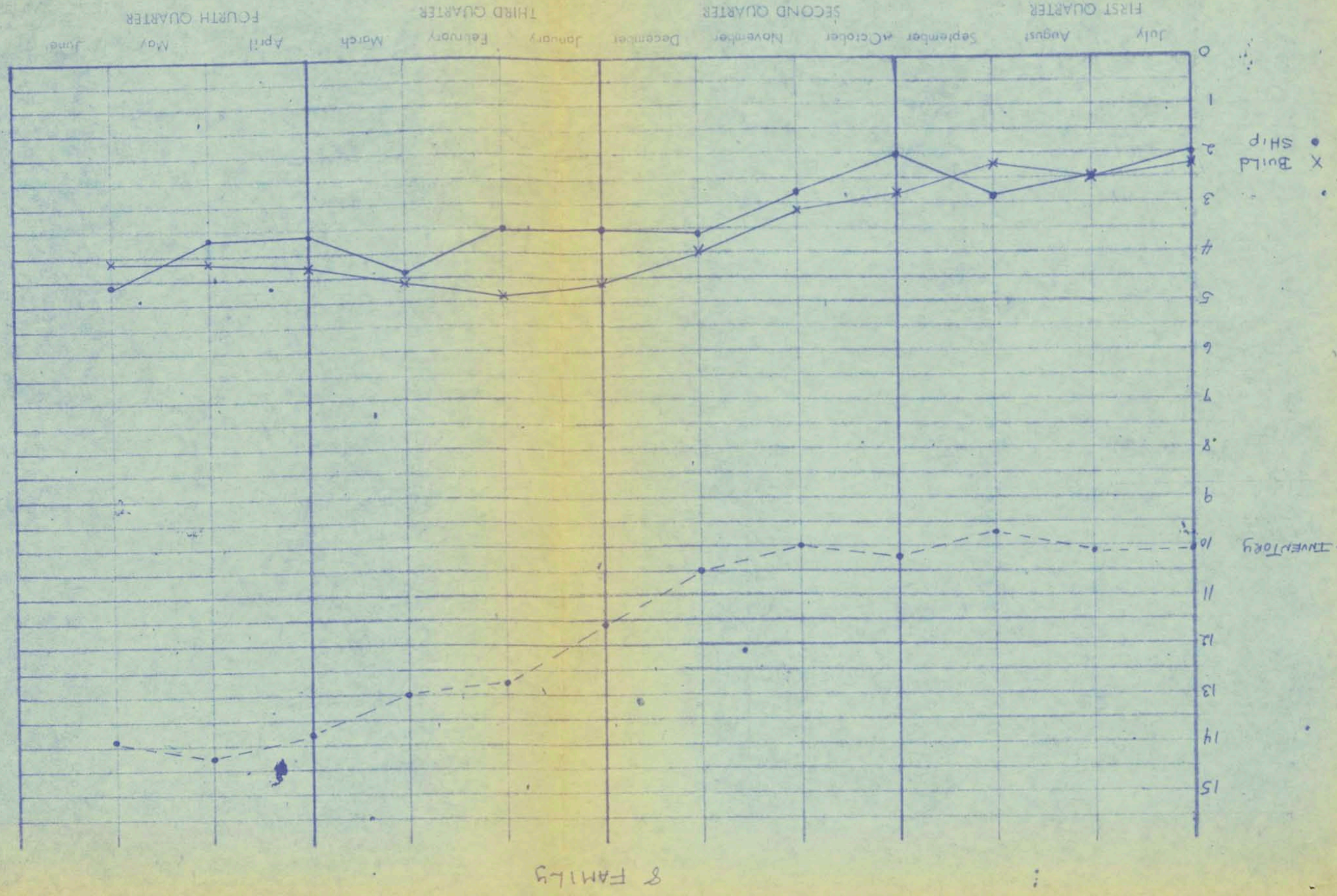
Notes: 1-4 (Same as before)
5 Shipping figures for December are based on latest manufacturing estimate.
6 Shipping figures for January through June were taken from the latest product line budgets.

** A= Actual
B= Budget

Product	Line	April Build	April Ship	April End Inv.	May Build	May Ship	May End Inv.	June Build	June Ship	June End Inv.
8	**A	4,377	3,700	13,775	4,252	3,700	14,327	4,193	4,600	13,920
9	A	1,424	1,415	6,647	1,092	1,415	6,324	989	1,770	5,543
10	A	3,645	3,250	10,120	3,645	3,250	10,515	3,800	4,050	10,265
Linc	A	1,083	576	2,857	1,127	576	3,408	1,077	728	3,757
Trad	A	70	138	247	82	138	191	52	174	69
Mod	A	894	1,078	1,699	944	1,078	1,565	1,124	1,344	1,345
Total	A	11,493	10,157	35,345	11,142	10,157	36,330	11,235	12,666	34,899

TOTAL INVENTORY

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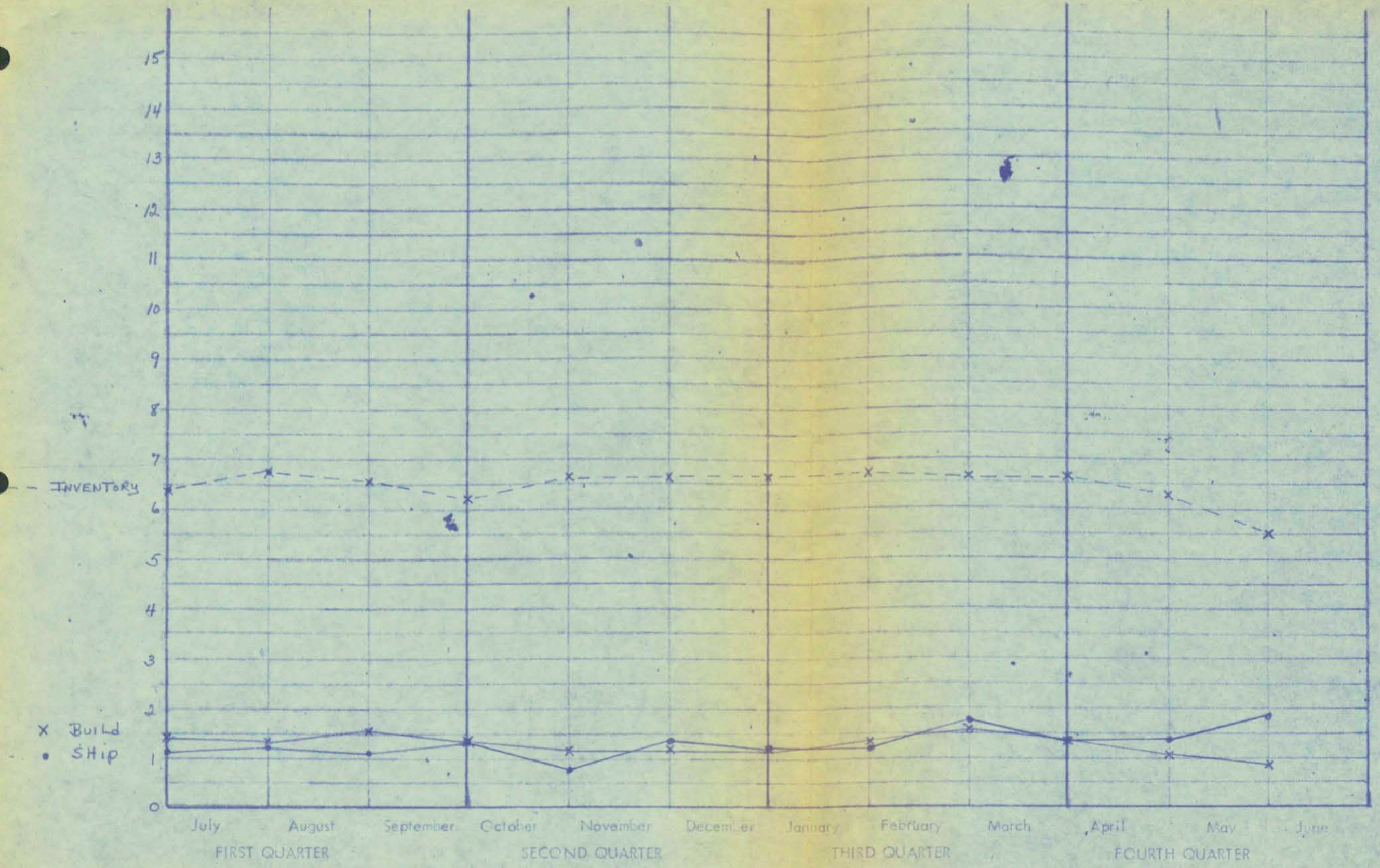
INVENTORY

9 FAMILY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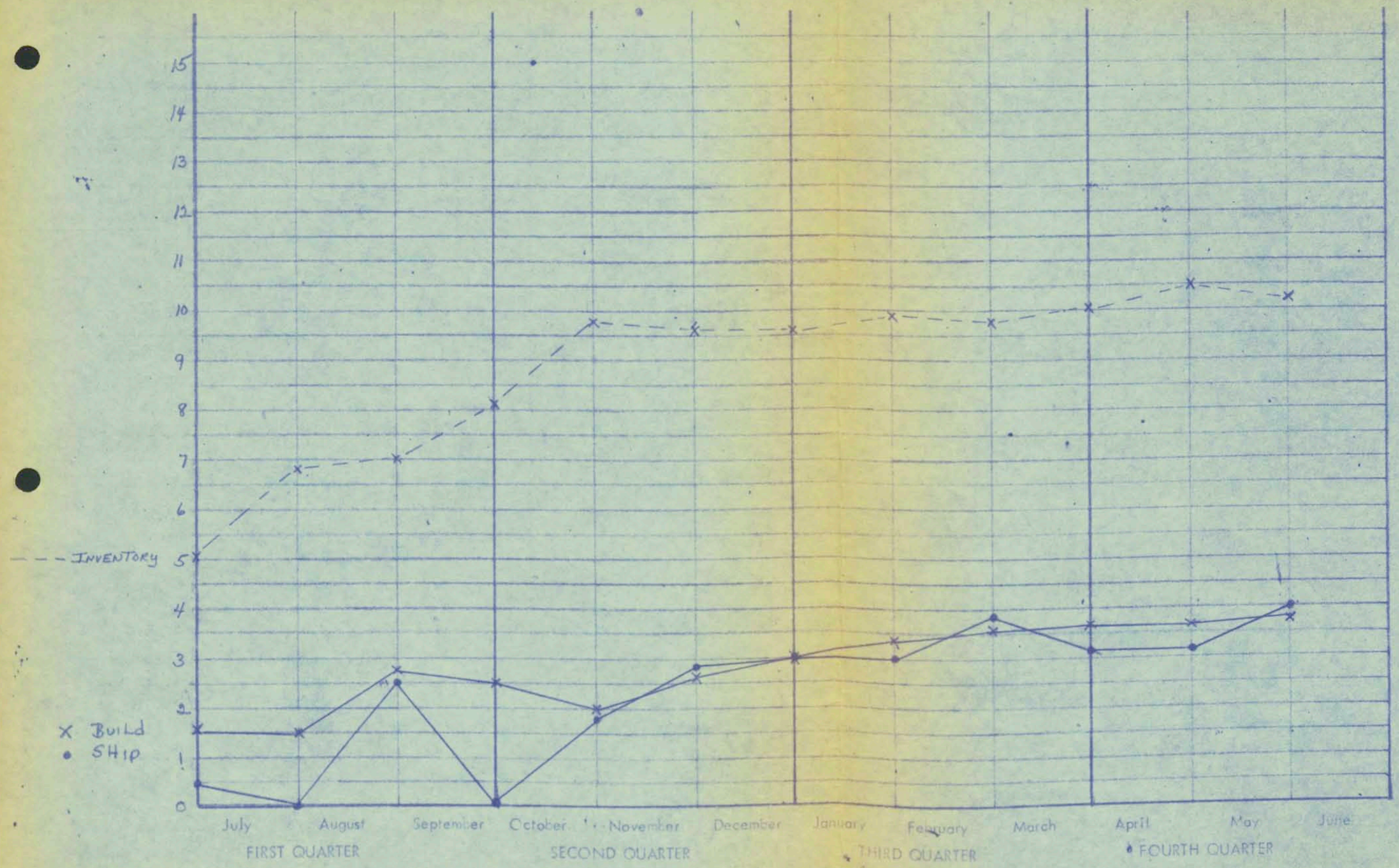
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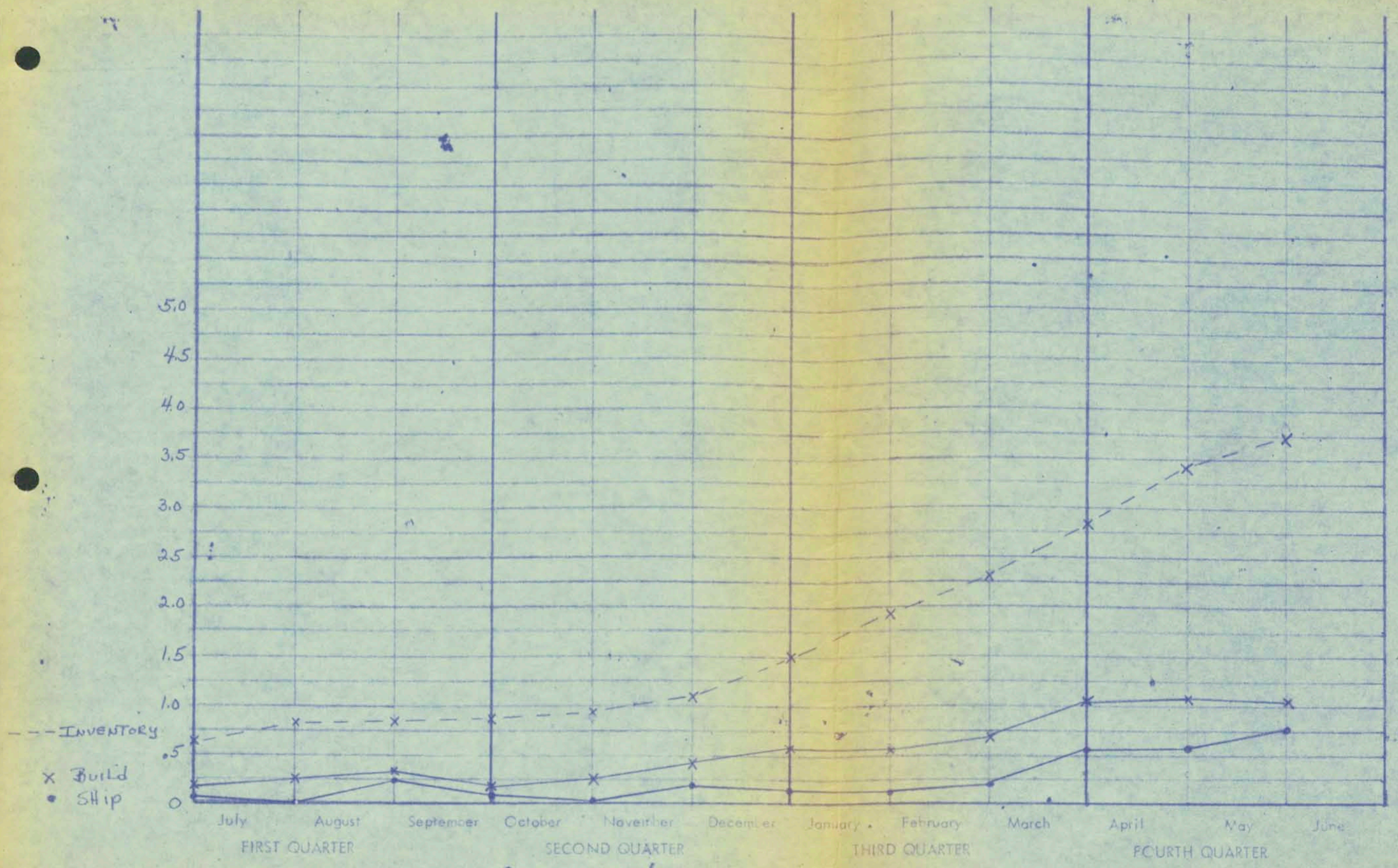
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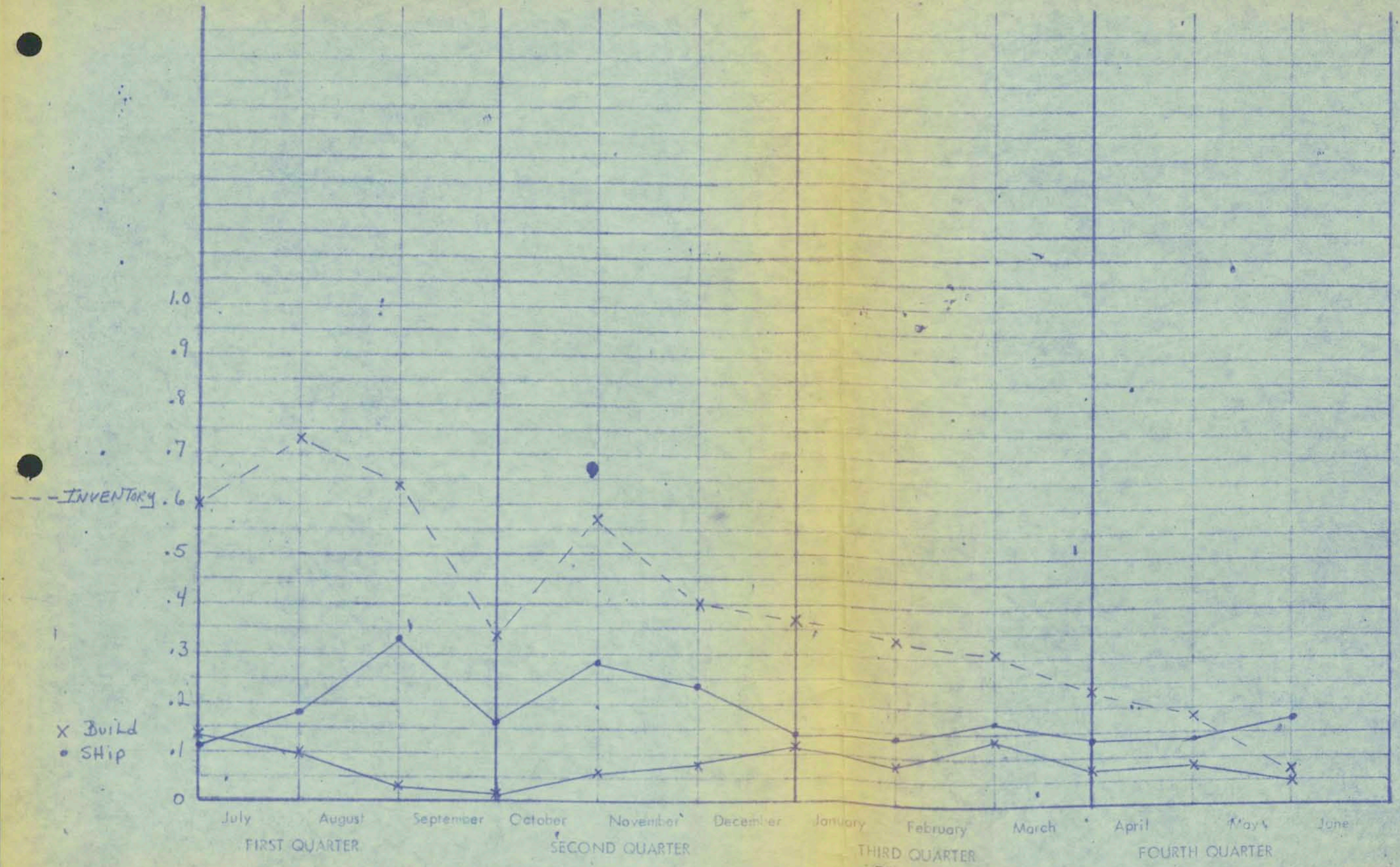

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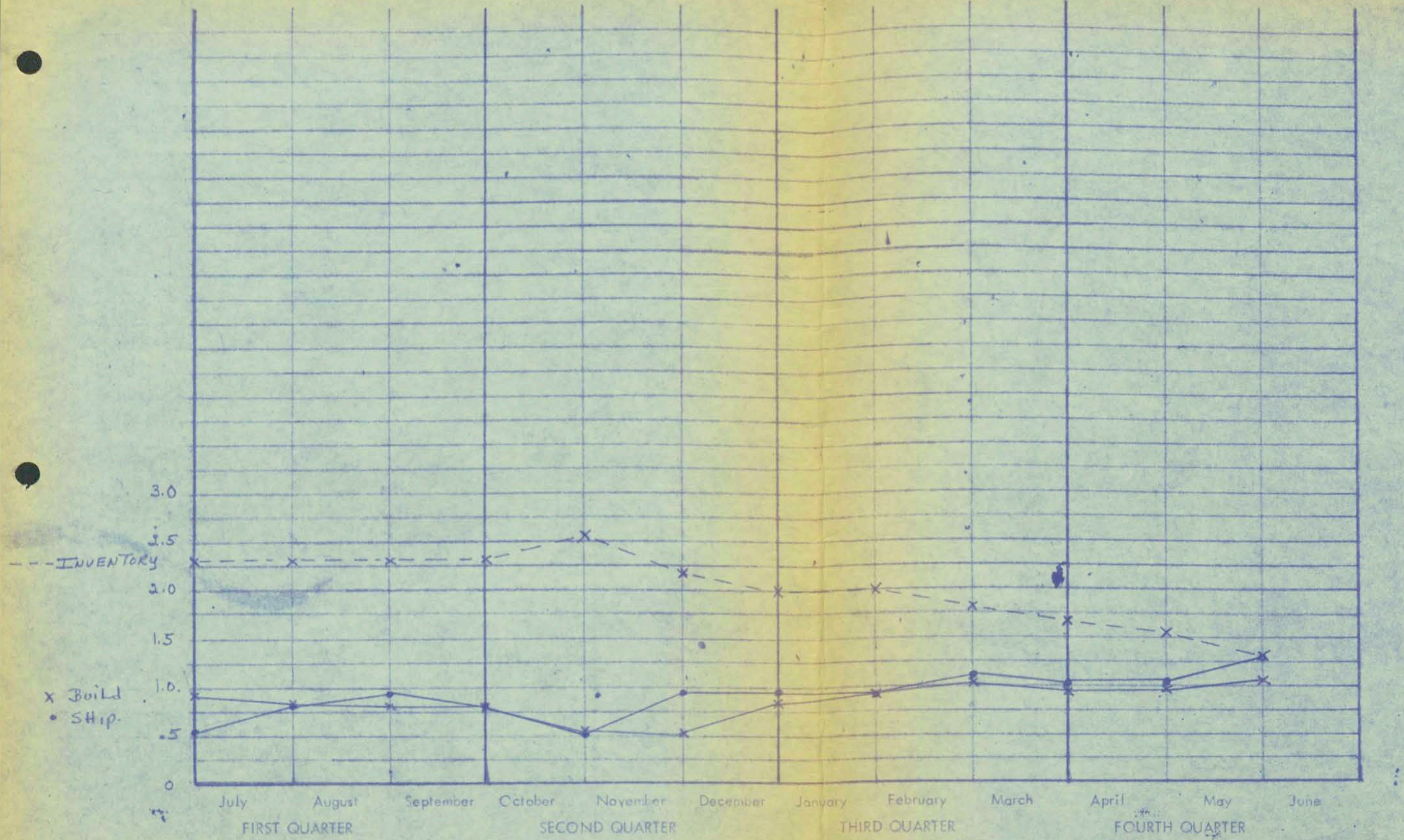
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THIRD QUARTER
FOURTH QUARTER

Ken

CONFIDENTIAL

digital INTEROFFICE MEMORANDUM

DATE: December 31, 1968

SUBJECT: NON-IMPACT PRINTER PRELIMINARY PROPOSAL

TO: Operations Committee FROM: Bill Owens

I propose to build a 96 column, 120 character per second, non-impact printer which will look to the computer like a fast ASR33. Manufacturing cost will be less than $1,000.

Total cost to develop the printer and produce five units using production tooling is $164,000.

Estimated savings compared to 80 column, 30 character per second NCR MINIPRINTER are $750 per unit or about $150,000 per year. Estimated savings compared to 96 column, 300 lpm Anelex unit are $6,500 per unit or about $1,300,000 per year. Truth is somewhere in between. Payback is about one year.

Key dates are: Select design and prove cost in April, prototype printing in May, pre-production run July through September, production in October, 1969. At the April design review, detailed product costs and schedule for project completion, accurate to ± 10%, will be submitted for approval.

Project schedule is attached.

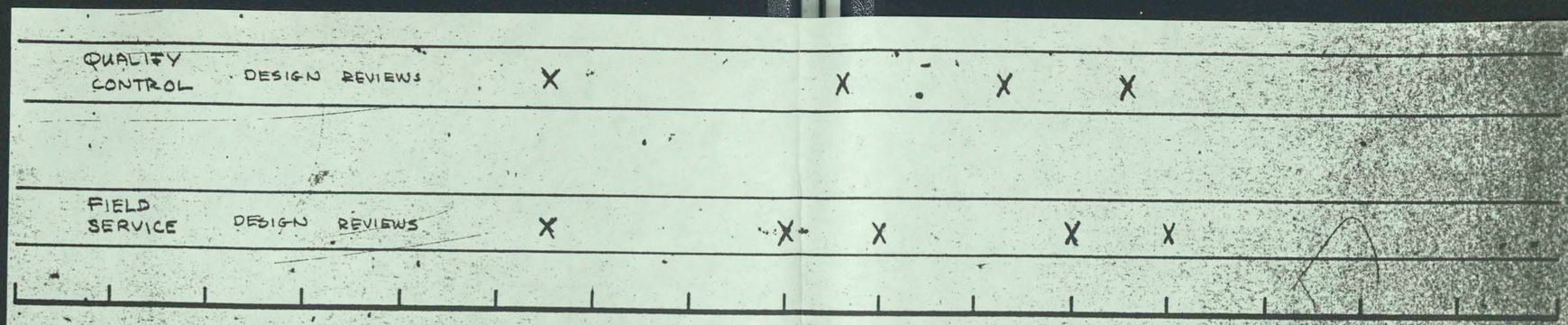
This printer will satisfy 80% of our small and medium size computer printer needs.

Optional versions of the basic printer may be developed as later projects and will greatly increase savings to the company.

Bill

/bn

Line Reference Target LRT-BE4-V2



NON IMPACT PRINTER
Project

By W. OWENS

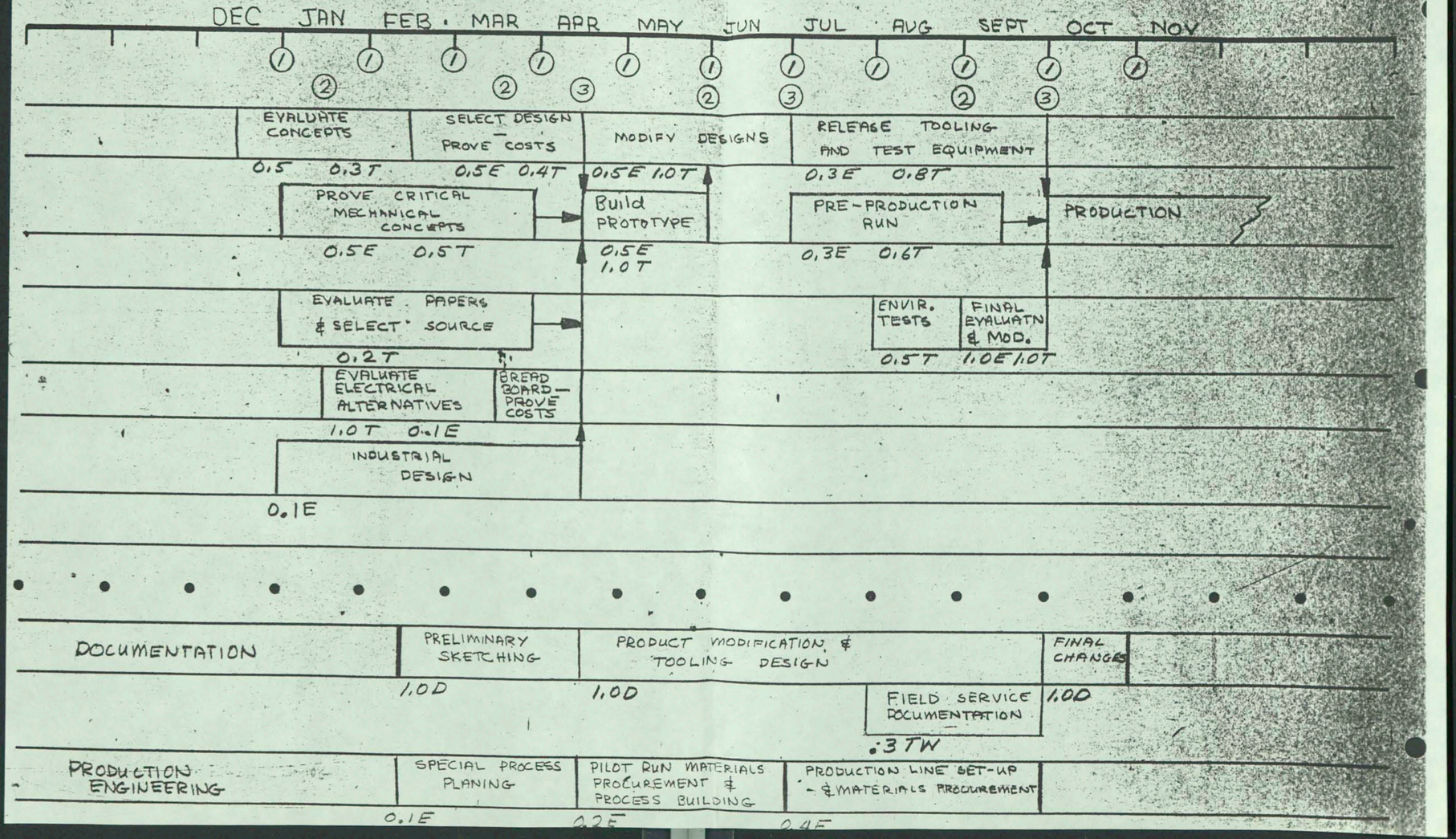
Revision Date

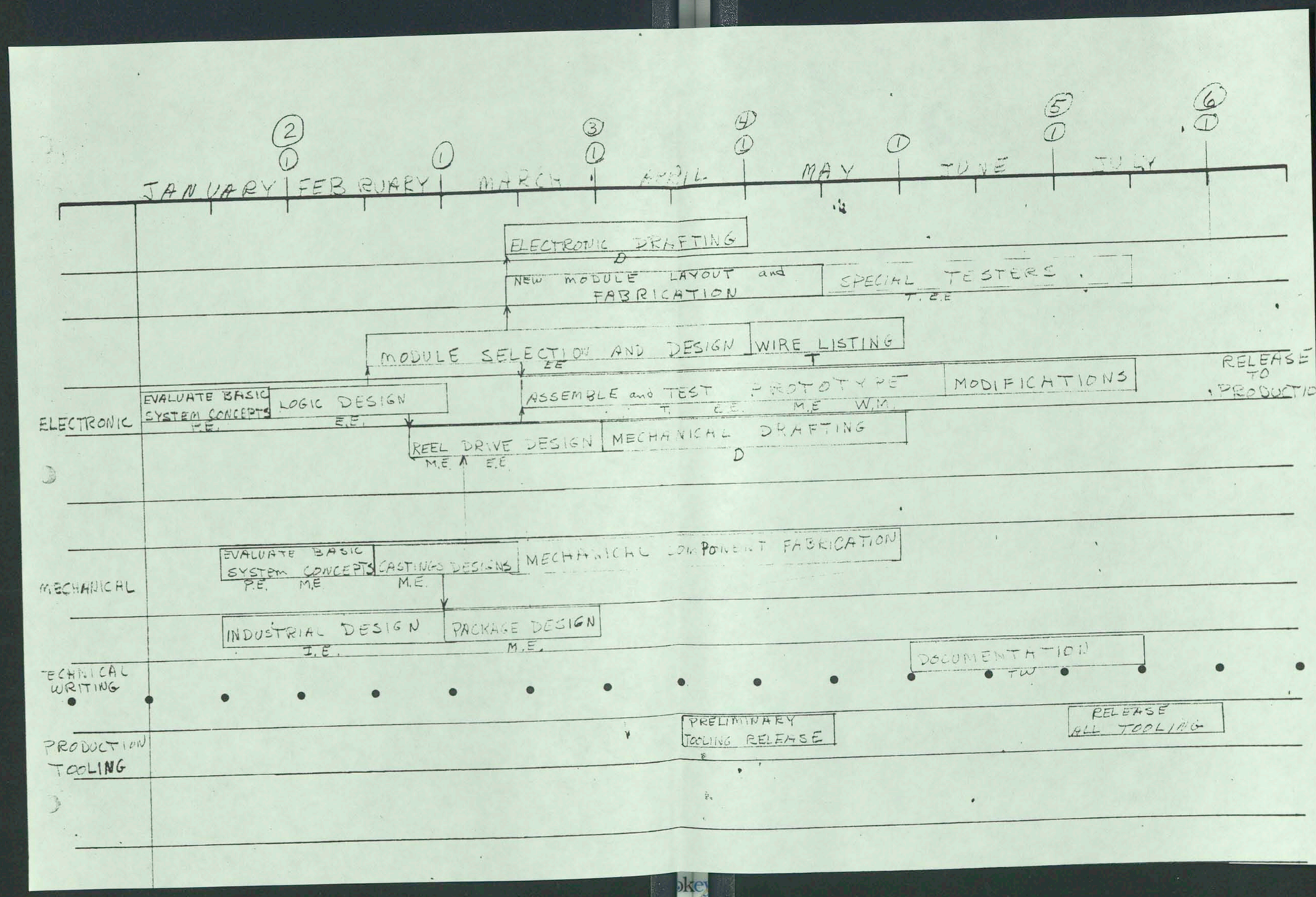
Check Point Table

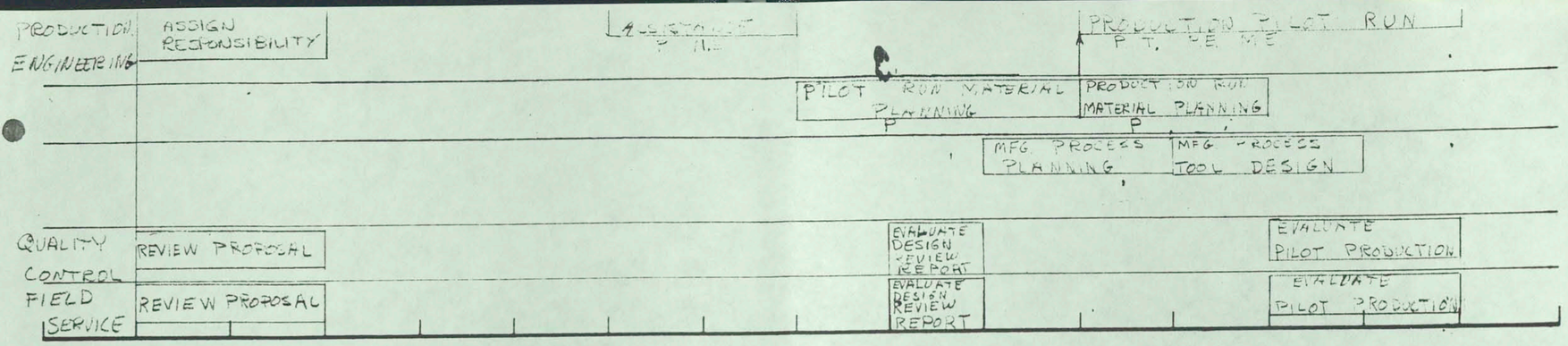
(1)		MONTHLY PROGRESS REPTS									
(2)		INFORMAL DESIGN REVIEW COMMITTEE CONSULTATIONS									
(3)		FORMAL DESIGN REVIEWS									

RB 6/27/66

NON-IMPACT PRINTER







NEXT GENERATION DECTAPE
Project

By ERNEST LUTI

Revision Date _____

Check Point Table

	1	MONTHLY PROGRESS REPORT									
	2	PRELIMINARY DESIGN REVIEW									
	3.	COST REVIEW									
	4	INTERMEDIATE DESIGN REVIEW									
	5	FINAL DESIGN REVIEW									
	6	RELEASE TO PRODUCTION									

RB 6/27/66

CONFIDENTIAL

Ken

digital INTEROFFICE MEMORANDUM

DATE: December 31, 1968

SUBJECT: DEC Tape Redesign

TO: Operations Committee
Marketing Review Committee
Engineering Committee

FROM: Ernest Luttig

New Dual Unit

Proposal

Redesign existing DEC tape transport to eliminate existing problems and reduce manufacturing cost. Performance specifications to remain unchanged.

Basic unit will be a dual (89% of sales are in units of two) although singles can be built on dual casting. Other changes will be use of IC's (probably M series modules), elimination of brakes (dynamic braking), new selector switch, new hubs, new guide manufacturing techniques, and provision to include Read-Write amplifiers in transport as an option to facilitate interface with equipment other than DEC.

Cost saving will be $273.00 per unit. Based on annual volume of 1500 units per year (present projection is 2400 per year) will save $410,000 per year. Estimated development cost including manuals drafting, etc. is $58,000. Payback is less than two months.

Schedule attached shows release to production August 1, 1969.

Your approval is requested so that we may proceed at once with this program to meet the August 1, release date.

Present cost - single tape transport	$845.00
New cost - single tape transport on dual casting (represents 11% of sales)	$640.00
New Cost - single tape transport sold as part of dual unit (represents 89% of sales)	$565.00

/bca

CONFIDENTIAL

Ken

digital INTEROFFICE MEMORANDUM

DATE: December 31, 1968

SUBJECT: Tape Transport Proposal

TO: Operations Committee FROM: A. Sherman

CC: Marketing Review Committee
Engineering Committee

A study has been conducted to determine DEC's present requirements for magnetic tape transports, determine DEC's future requirements for tape transports, and determine the characteristics of tape transports available to the computer market. This study, which has included a make or buy decision, has lead to the following tape transport development recommendations:

1) Develop an inexpensive IBM compatible tape transport. Delivery of units can start during November 1969 at a rate of 6 per month.

2) Upgrade this inexpensive IBM compatible transport to operate at 45 ips and be competitive in performance with the TU20.

3) Modify the TU 79 to develop a 60 kc tape transport having lower production costs and including those modifications necessitated by field use of the unit. Included in this project is a 9 track capability.

4) Investigate the market for and feasibility of a modified TU 79 to permit IBM compatible phase encoded recording at 1600 bits per inch at 75 inches per second, ie 120,000 characters per second.

These four recommendations are four separate projects designed to meet the present and projected requirements for magnetic tape transports for the DEC computer lines. Each of these projects is a separate entity and will be proposed separately. The proposal for item 1 is included in this memo. This transport will be designed in such a manner that implementation of recommendation 2 will utilize the mechanical hardware developed for item 1.

Item 1 will meet the low cost IBM compatible tape transport requirements of the PDP-8 and PDP-9 product lines. This transport will be

capable of writing and reading synchronously with the following specifications:

1) Reel size 10½"
2) Tape capacity 2400 feet of one mil tape
3) IBM compatible at 200, 556, or 800 bits per inch
4) 7 or 9 track capability
5) Synchronous record and play back at speeds of at least 25 inches per second (recommendation 2 will cover the follow on developments for a 45 ips goal).

A tape transport capable of writing 800 bits per inch at 25 inches per second with a 7 track head will have a cost goal of $2,100. Further details concerning cost will be contained in the section on economic analysis. An interface for controlling one transport will have a cost goal of $800 (this controller is scheduled for development for the PEC tape transport). The selling price goal for one transport with a dedicated controller is $7,800.

Anticipated yearly volume for this transport is 150 units for each of the first two years and 200 units in each of the next two years. This represents a conservative projection of the production rates anticipated by the various product lines.

As presently envisioned, the unit will be constructed as follows:

1) Single capstan
2) Vacuum column tape buffers
3) No tachometer in tape path
4) Oxide side of tape contacted only by head assembly
5) Tape transport can be mounted in a standard 19" rack

Various options of the basic tape transport will be available. These options will include a choice of:

1) Recording densities
2) Recording formats, ie 7 or 9 track
3) Magnetic heads (a read after write head will be available)
4) Mounting - ready for rack mounting or rack mounted

A preliminary development schedule and cost for recommendation 3 is also enclosed. This development is considered a continuation of the TU 79 development and is predicated upon completion of the TU 79, its release to production, and its field use by several customers. Use of the TU 79 by our customers is important since this will indicate those areas of design which need to be considered only from a cost reduction standpoint. The schedule indicates that the first few months will be spent in studying and testing design concepts for use in this tape transport. It is envisioned that Jim Young will work on this study part time while completing the TU79 release to production and be available full time by April 1. The overlapping of activity on a "time available" basis will expedite the completion of a final development proposal.

With the above assumptions, the development schedule for item 3 has been prepared. Development of this tape transport will meet present requirements of the PDP-9 and PDP-10 product lines. Since there has been some customer requests for 90 kc data rates, it is anticipated that faster data rates will be required in the future and that the ability to handle 1600 bits per inch will also be required. The need and market for data rates above 60 kc will be thoroughly studied before a proposal concerning this area is prepared.

The 60 kc IBM compatible tape transport will read and write synchronously only. The unit will be capable of meeting the design requirements presently specified for the TU 79. A cost goal for this transport has not yet been established. The following is a summary of the Marketing Committee's anticipated requirements and how this proposal will meet these requirements:

PRODUCT	PRICE	VOLUME (UNITS) FY 69	FY 79	COMMENTS
DECtape	8.0	700	850	The DECtape is currently being investigated and is not included in this report.
Incremental mag. tape	14.0 (with control)	25	35	It appears that a truly incremental tape transport is not a large portion of our market. The development of recommendation 1 will meet the bulk of these requirements.
Low speed cheap IBM tape	12.0 (with control)	90	120	
TU 20	22.0 (with control)			The development of recommendation 2 will compete with the TU 20. (Though the unit will get more expensive, the unit will still be priced well below the TU 20)
TU 79 (60 kc. IBM)	18.0 (prefer 15.0)	90	120	Development of item 3 should permi a selling price of 15K to be achieved.
90 + kc. IBM tape			6 - 12	Though a high volume in units capable of 60+ kc is not presently anticipated, unavailability of suc a unit has affected potential sale of complete computer systems. Development of item 4 would meet the requirements for such a unit without facing the mechanical problems inherent in obtaining 90 or 150 ips operation.

ECONOMIC ANALYSIS

Inexpensive IBM Compatible Transport

Development cost	$251,000	
Income from pre-production	10,000	
Net development cost	241,000	
Anticipated production during four years	700	
Unit amortization	350	
Unit production cost	1,800	
Amortization	350	
Unit cost	2,150	
Total unit cost including G & A (1.7 x unit cost)	3,700	
Suggested selling price	5,400	
Profit (sell price less total cost)	1,700	
Sales during first year	150	units
Profit during first year	255,000	
Payback	12	months
Sales during four years	700	
Profit during four years	1,260,000	
Return on investment	Over 30%	

Peripheral Equipment Corporation tape transports are being used to meet requirements for this type of transport. The PEC unit is being purchased at a cost of $5,500.00 and will be sold at a price of $8,400.00. Our tape transports will have a unit cost of $2,160.00 achieving a cash savings of $3,360.00 per unit to DEC. Our customer will be given a cash savings of $3,000 while receiving a transport having improved capability.

INEXPENSIVE IBM COMPATIBLE

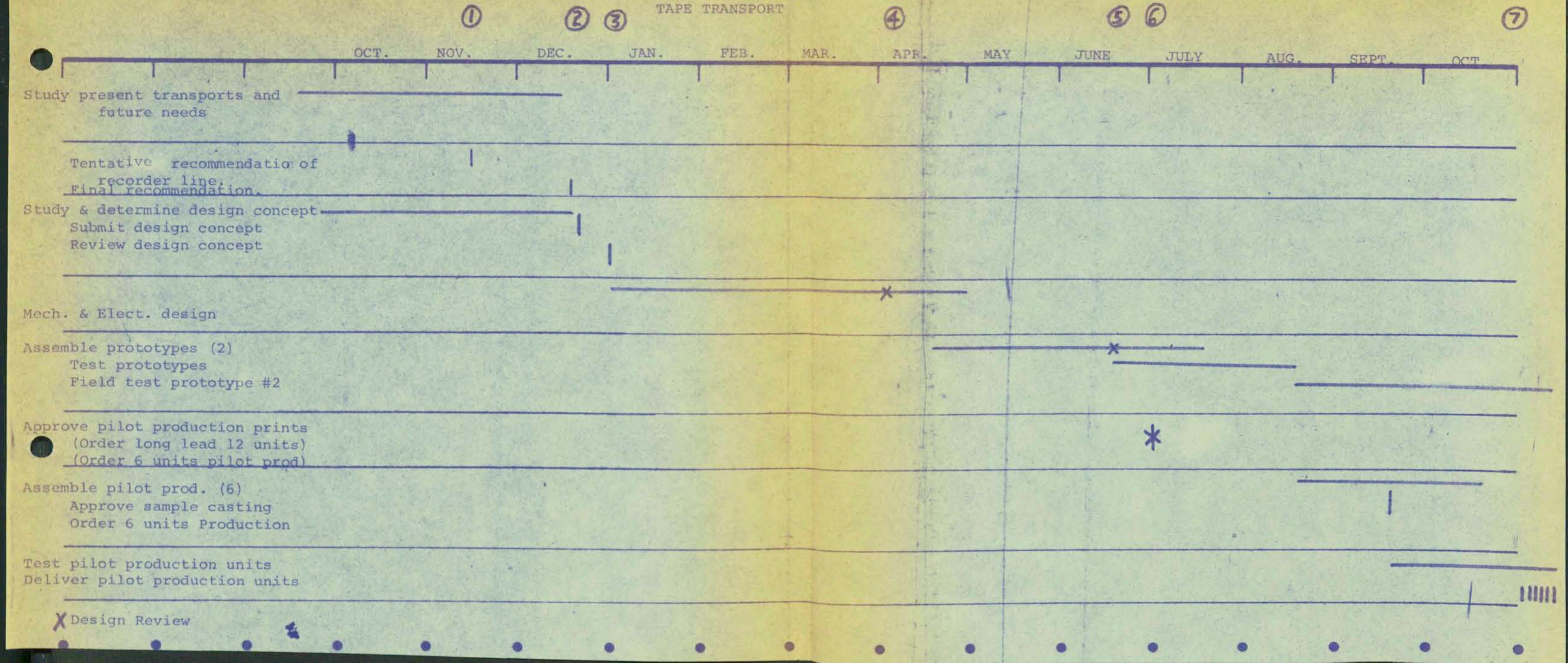
TAPE TRANSPORT

CC 386

Mechanical Engineering	27
Electrical Engineering	22
Technician	25
Mechanical Engineering	10
Industrial Design	5
Model Shop	6
Drafting	12
Process Engineering	5
Production Engineering	15
PDP-8 Engineering	9
Model Shop	6
Programs	5
Diagnostic Programs	5
Manuals	7
Tooling }	
Test Equipment }	27
Facilities	10
Materials	34
Technicians	21
	251

DEVELOPMENT SCHEDULE

LOW COST IBM COMPATIBLE TAPE TRANSPORT



60 KC TAPE TRANSPORT (PRELIMINARY)

CC 386

Mechanical Engineering	21
Electrical Engineering	14
Technician	17
Mechanical Engineering	10
Industrial Design	3
Model Shop	5
Drafting	12
Process Engineering	5
Production Engineering	10
PDP-10 Engineering	5
Model Shop	6
Programs	2
Diagnostic Programs	
Manuals	5
Tooling	
Test Equipment	30
Materials	30
Technicians	8
	183

DEVELOPMENT SCHEDULE (PRELIMINARY)

60 KC TAPE TRANSPORT

FEB. MAR. APR. MAY JUNE JULY AUG. SEPT. OCT. NOV. DEC. JAN. FEB. MAR. APR.

Study Design
(Determine cost goals)
(Determine performance goals)

Propose Design Concept

echanical &
lectrical
Design

Assemble proto-
types (2)

Approve pilot
production
prints

mble pilot
production.
eliver pilot
produc ion.