What significant things remain to be done in S.C.?

1. Packaging
2. Surfaces
3. Complexity

Related areas

1. III-V's
2. Metal-base Xstors
3.

Might as well admit that there is much development yet.

Xstors - some
Diodes - blah
μCkts - yea!

Thesis

1. There are no major problems left in silicon device technology.

2. The promise of active devices of other types is not sufficient to justify large efforts toward achieving them.

3. Large efforts can only be justified in the general direction of large existing markets. ∴ New phenomena & materials are of interest only where the application can be seen.

TABLE OF CONTENTS --- MEETINGS

(Project Reviews & Miscellaneous)

Gordon Moore

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☐	56-803	3 Columns
☐	56-804	4 Columns
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☐	56-810	10 Columns
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INTER-DEPARTMENTAL CORRESPONDENCE

FAIRCHILD
SEMICONDUCTOR CORPORATION

TO: G. E. Moore
CC: Tom Bay
Bob Graham (2)
DATE: 1 August 1962

SUBJECT: MEETING AT AUTONETICS
JULY 31, 1962
FROM: V. H. Grinich

Autonetics personnel present:
Jim Carlyle
Allen Beek
Art Fifer
R. Ramond
Fairchild personnel present:
J. Farley
Vic Grinich
Texas Instruments personnel present:
W. Adcock
J. Lacey
C. Shawn

The purpose of this meeting was to act as a pre-briefing on contract negotiations for parts procurement for Minuteman II. Autonetics has a total of 18 FEB (Functional Electronic Block) which they desire to have in micrologic form. Fourteen of these are from the Computer and Data Systems Department and four are from the Inertial Navigation Department. The last four are linear circuits and, in general, have a much longer time scale than the Computer and Data Systems' circuits.

The first part of the meeting was a discussion on how to test the FEB's which considered the following five points:

1. The use of test points
2. Individual transistors, resistors, and capacitors made by the same process
3. Overstressing
4. Matrix life tests
5. Extrapolation from FSC data.

A discussion was held on what were the new facets to be considered from reliability points of view and were itemized with respect to the present Minuteman planar devices. The difference consists of the following:

1. Geometry (di-attach area)
2. Lead attach
    (a) Lead over oxide
    (b) TCB over oxide
3. UFO's (one-thousandth inch lead spacing)
4. Unimproved packages (new interface problems with assembly)
5. Resistors
6. Capacitors
7. Close coupling through isolation areas
8. Epitaxial.

Processes and things that remain the same are the following:

1. Material
2. Process steps
3. Thermo sensitivity
4. Planar technology
5. Mechanical operations of assembly
6. Surfaces

A discussion of what the objectives are of the RIP program is summarized by the following six items:

1. Discover significant failure modes
2. Discover stresses which may induce modes
3. Set up tests involving these stresses to determine failure rates and parameter drift characteristics
4. Produce screening criterion and reliability predictions
5. Set up tests involving these stresses that evaluate process changes and undertake failure analysis
6. Conduct mass tests to prove failure rate.

A discussion of the approximate program schedule was as follows:

The first year consists of the design and reliability improvement program, while the second half year is primarily a reliability evaluation phase. For a device which will be given the full treatment, the following quantities will probably be used per test: 1. Design sample evaluation - 2000 units, to be followed by phase #2 which consists of two or three matrix tests consisting of the following: (a) static operating life tests that would consume approximately 2000 units and then (b) a dynamic life test (daisy chain ring possibly) - total of 6000 units. 3. Step stress to evaluate design and process changes (task 7) consisting of approximately 5000 units, or approximately 100 units per week. Units that were used in 2(a) or (b) would also have a step stress program. 4. Final proof tests would consist of 20,000 units for 4000 hours.

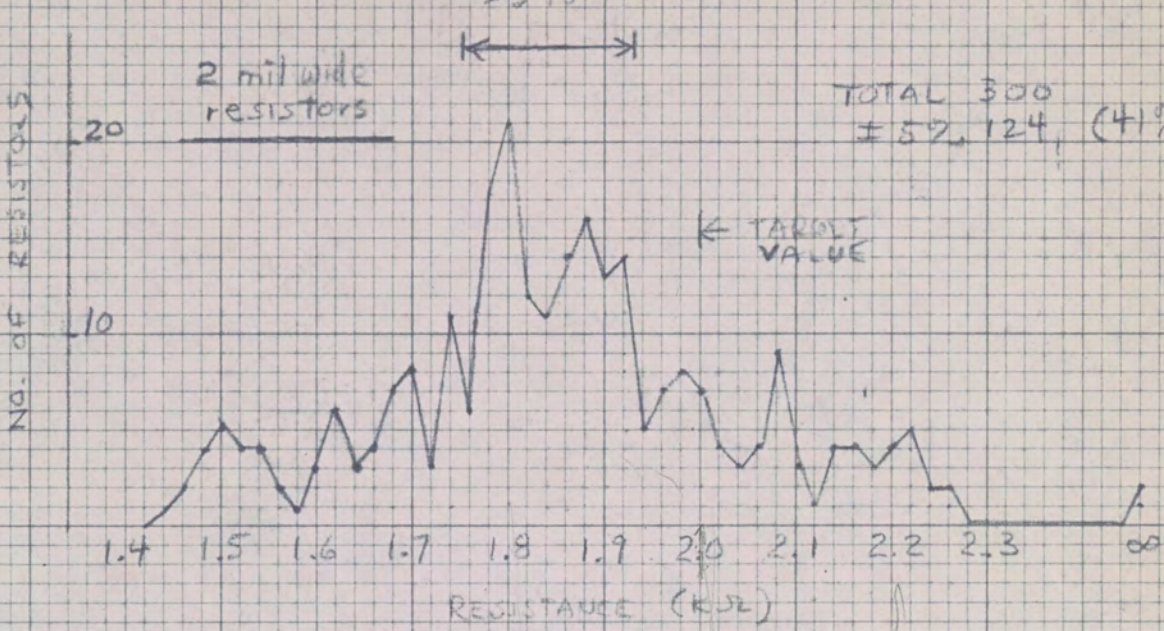
It was assumed by Autonetics that they could evaluate completely one basic circuit as outlined above and then extrapolate results so that only one large scale final proof test would be necessary for about every four circuits. Auto netics originally intended to be able to sign contracts with parts vendors by October, 1962, and receive first design samples by February, 1963. However, it is possible that they will be forced to go into a long and completely open multi-bid proposal negotiation in which case they would not be able to sign a final contract by December, 1962. They will still assume, however, that they will be able to get their parts in the middle of February.

Carlyle wants to get a rough estimate from Fairchild regarding what we think such a development and RIP program would cost for their use in submitting cost estimates to the Air Force. He desires to have this telephoned to him August 2nd. This program cost does not include the cost of the devices to be used in the program.

V. H. Grinich

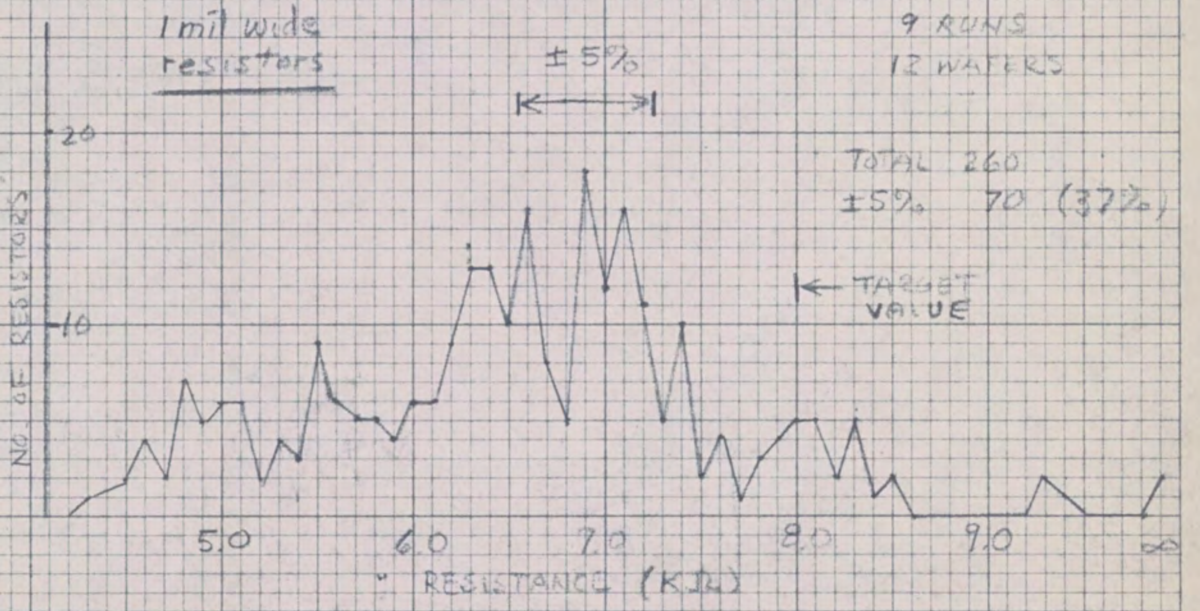
VHG/ea

NICHROME RESISTORS
100 Ω/□ AFTER ALLOY



9 RUNS
12 WAFERS

TOTAL 300
±5% 124 (41%)

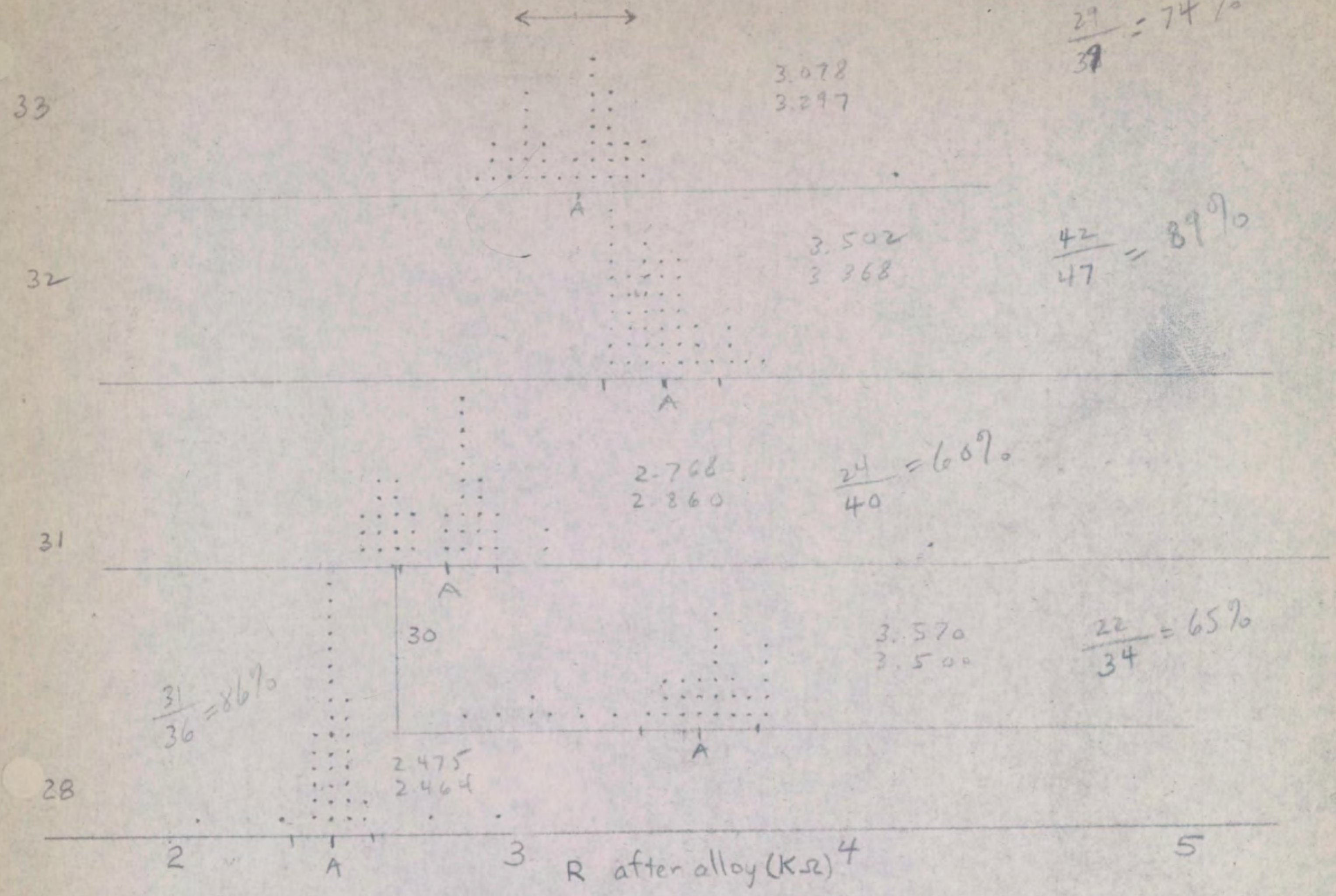


9 RUNS
12 WAFERS

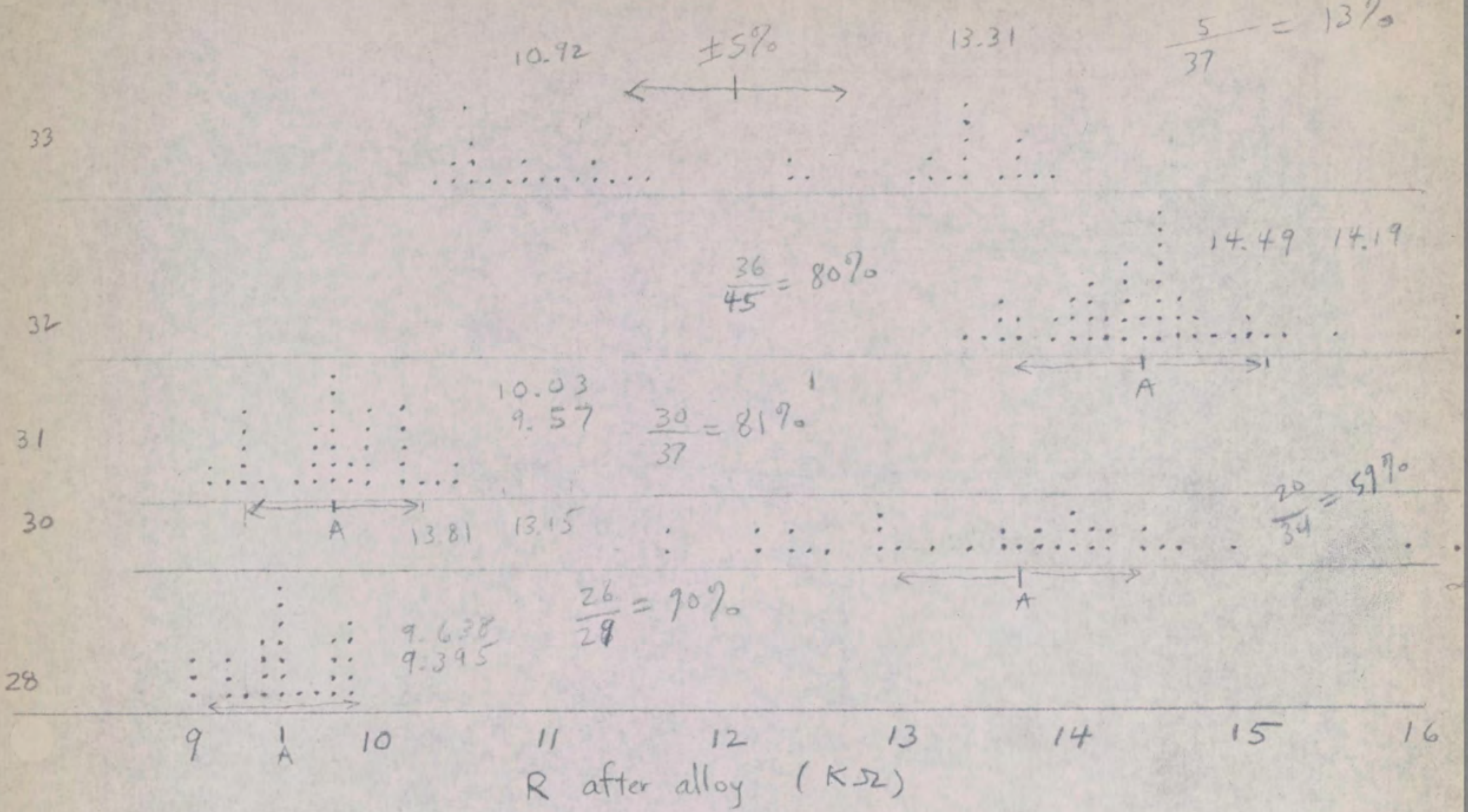
TOTAL 260
±5% 70 (37%)

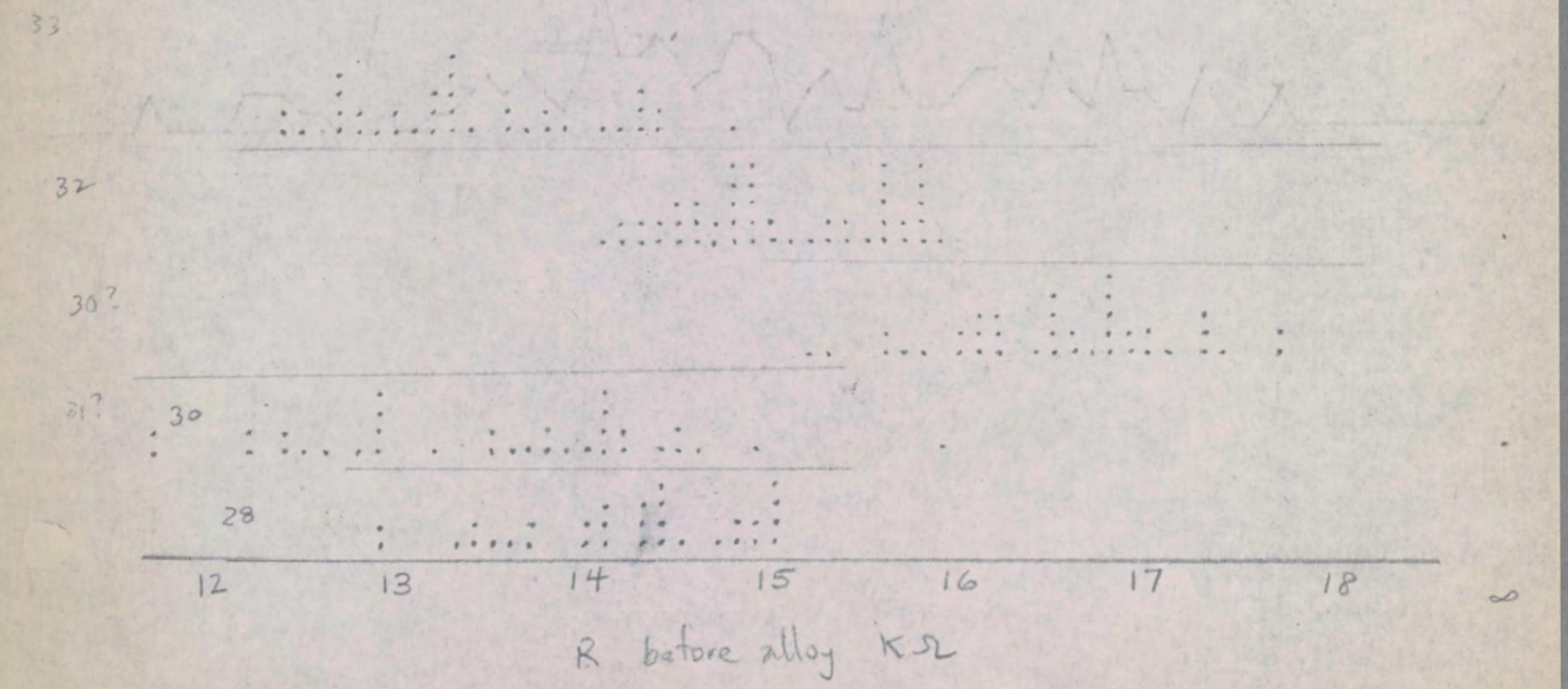
4-12-62
RKW

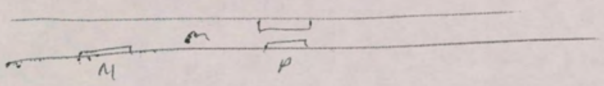
200 Ω/□ 2 mil resistors

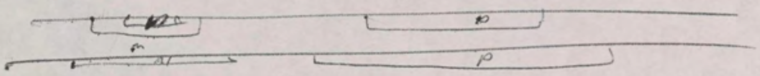


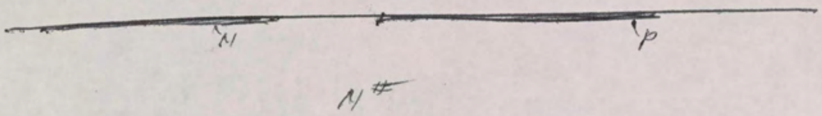
200 Ω/□ 1 mil resistors






m
M
P


P
m
M
P


M
P
M#

Nichrome Thin Film Resistor

ER-Series

Sheet resistance range - 25 Ω/□ - 300 Ω/□
Geometry - 2 mil x 12 mil strip on oxidized Si die. Aluminum contacts Al leads.

Effects of Various Parameters

1. Substrate temperature
   Noting conclusive - most evaporations onto hot substrates resulted in stable units. Similarly for cold substrates.

2. Heat stabilizing of film in N_2 at 575°C after evaporation. No effect. ER-24

3. T.C.R. control
   85 - 330 ppm/°C. No control.
   T.C. not dependent on substrate temperature
   " " " " film resistivity
   " does not change on aging at 300°C for 5000 hours.

4. Al contact "alloy" time
   3-15 min at 575°C - no effect.

5. Al contacts under Nichrome film
   Some instability observed after storage at room temperature for 5000 hours.

6. High temperature storage - 300°C
   5000 hour storage 133 units

Resistance Change	No. Units	%
< 1%	97	73
> 1		
< 2	7	5
> 2		
< 5	20	15
> 5	9	7

Failures (> 10 change) of 345 units (~ 18 runs)

150 hours	5%	16 units (12 failures in three runs of 49 units)
300 hours	2%	6 units

RLM:vt
11-20-61

May 7, 1962 — Meeting on Body English.

Data for next time: — In 2 weeks — 5/21/62

O'Keefe:

1. Pictures in monochromatic light to show the thickness contours from various specimens.

2. Cl_2 etch pit counts in
   a. fresh oxide
   b. after a KPR cycle (no mask)
   c. after P & B predep.

3.

Moore —

1. Aim at permanent masks

For next time
[illegible]
Phil
Marty

May 14 - Diode Array Plans

Get Price to run through a sample of BCD arrays. Consider X-fer to D.D. after feasibility.

May 15 - Discussed c̄ Sam Fok

I. Permanent masks

A. Rh film - Need good, hard, pinhole-free film need from Campbell
B. Cr + Ag
C. Al + evap. SiO_2, Al_2O_3, SiO, MgF_2
D. Cr or other + SiO_2 pyrolytic on quartz

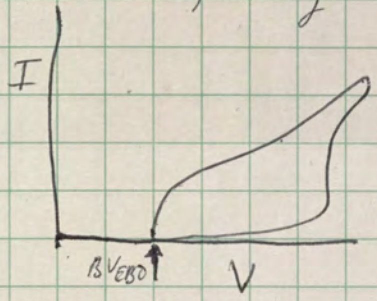
II. Use of phase contrast on film finding

III. Personnel
A. Chet, Gunter
B. Need two girls - one A.W. replacement, one new.
C.

May 15, 1962 - XP-3 Review

Kebell
Smith
Ulmann
Wheeler
Ferguson

Devices cranking through, now showing some of the old, "long channel"-type problem.



8

May 17, 1962 - Section Meeting

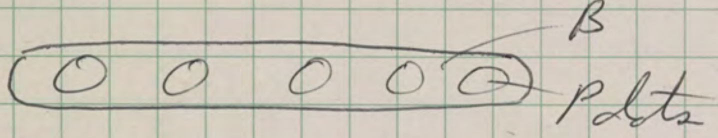
It takes 40 diodes for a BCD array

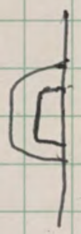
8 4 2 1 code

8 inputs , 10 outputs

Need 40 diodes

John Price was doing



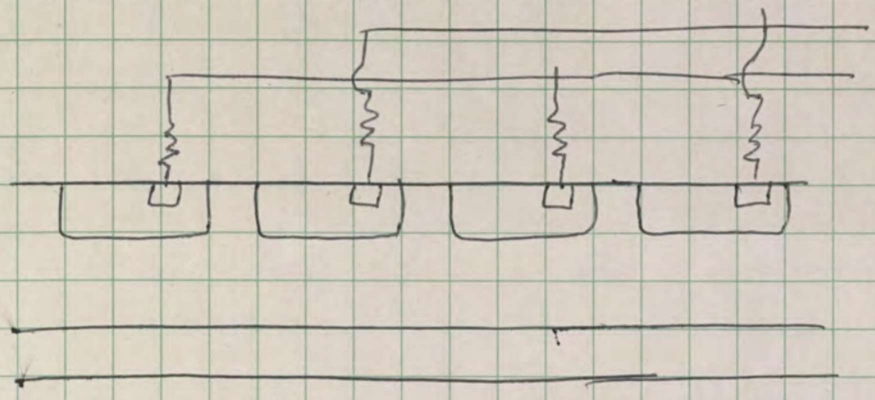


Rundown on Fok's area
Mtn. View is running.
Mesa is going up - S&R tomorrow
Borodale is setting up camera - ready to check out. The bulb came broken. - It is special.
New S&R — final mechanically this week, ready for check out next week.

May 19, 1962 Talbert on the Shift Register

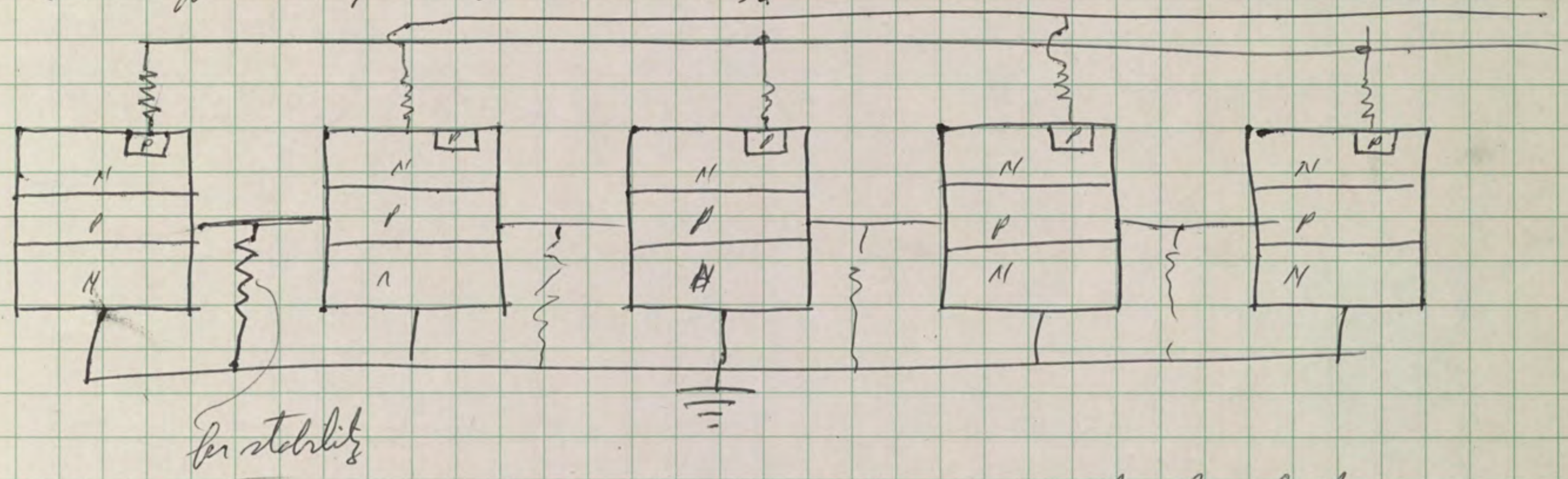
Farina
Ferguson
Grinich
Moore

the Bell (D'Asaro) one was



This one depends upon the interaction of one structure with the next by means of minority carrier diffusion.

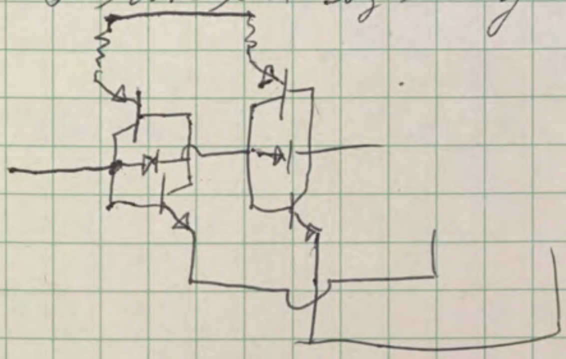
A later version depends upon the resistive drop (it can be connected between different chips and still work).



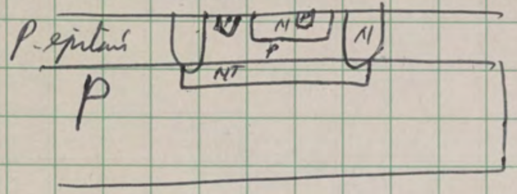
If a given one is conducting, because of the Al and the bottom N is an equipotential plane, there can be a 0.3v drop from one end to the other.

By adding resistors, a big improvement in stability looks like it could be made.

It looks that by using diode coupling and resistors we might do best



This can be integrated as



This sounds exciting!!

Meeting 5/21/62 on Project ROBE

Maury
Rodes
O'Keefe
Gart
Frind
Berliner

Ferguson
Folk
Hill
Engvall
Speck
Bradley

Start

Gordon Davis has shown a plot of viscosity, ∡ acceleration, speed of spinner, and thickness.

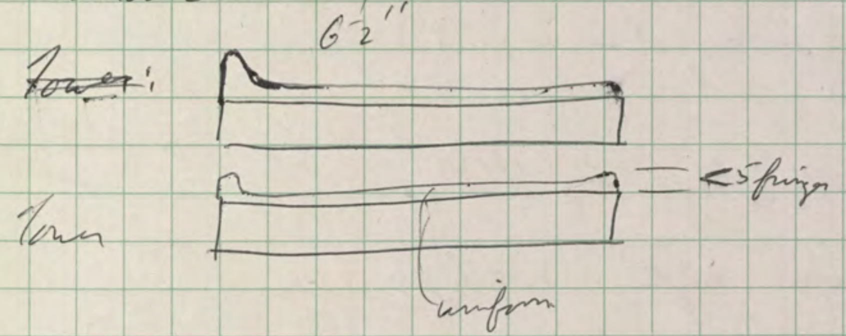
Mtn View now has a std. KPR viscosity to which they adjust all KPR to ~13 ± centistokes.

There are several type spinners:

1. tower in stead of old small ones
2. 8" dish (or 6½)
3. 3' dish
4. Centrifuge type (f ⊥ surface)

Engvall + Maury think that the spinner should be spun until dryness.

Contours:



– only bead is visible in a good monochromatic light.

Paul Hill says that if we have info on what we need, then we can get it with existing knowledge.

Maury says ½ μ (3-4 fringes) is enough for everything we etch. Engvall says this is a thick coating – we use 1-2 fringes.

Hill points out that the whole problem should be looked at.

lets look at whole masking ~~surface~~ system.

Paul Hill on masking ~~surface~~ system

I Surface preparation
  a) std
  b) mech polish
  c) mech - chem polish

II KPR film
  a) what do we get
  b) criteria for a good one
  c) development latitude
  d) thickness
  e) viscosity & filtration

} End up with std KPR
  1. fixed viscosity
  2. fixed spin program
  3. fixed development
  4. fixed film cure
} They have gone thru this already. I will get this.

Present work is on new developing ~~s~~ systems.

~~III~~ Roder ~~[illegible]~~ on Surface prep.

CP-6 works
Mech polish per San Rafael - no data yet - in mill.
Chem - Mech. polish

Plastic lapmaster in HNO_3, HAc, HF, H_2SO_4.

Aim is to get Norm Peterson to prepare surface oxidizing.

Pinholes on initial oxide.

No pinholes except at edge of wafers.
After a 30% etch of oxide etch they got many pinholes.
But thin oxide shows none. - Even oxidizing oxide causes ~~the~~ none.

Now there is an excellent base from which to follow pinholes

By next time:

Developable pinholes in film
Clean mask contribution
a) new
b) at end of life (~)

Correlation

Problem: Making use of what we know about locating pinholes, track down when or where they come in.

On permanent masks by next time we will have tried at least one permanent mask.

May 22, 1962 - μE research section

Points of interest:

1. Pension plan for salaried employees.
2. Phase contrast is on a loan - See Betty Thomas
3. We have ordered an electron microscope

Questions:

1. What people are we looking for?

Sam:

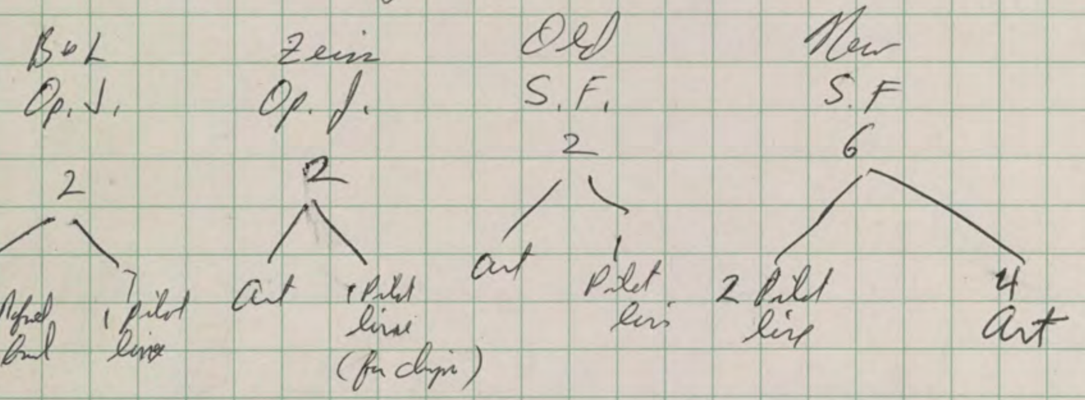
1. Coordinagraph operator (lab tech, draftsman or girl)
2. 1 dark room girl
3. Engr to work in with Art.
4. Technician to work c̄ Van to capable of becoming a foreman

Jim:
Presently nothing, but we should look this over.

Electroforming: We are nowhere now. We will need some 1st class technology here.
We would like to make 2 mil stripes in 6 mo or so.

Equipment: (problem)
1. We are having some trouble in covering the Hg vapor lamps mult

2.



3. Mask frame needed.

4. Step & repeat back for Bonsdale
Like get to 10 positions conveniently,

5.

BCD diode array takes 40 diodes in a 95 X44 pattern.

It should step on 125/75.

Capacitor - giving break-down problems.

We will get tied down on some of the radiation contract.

John Price needs a bridge for capacitor scan.

May 23, 1962 - Discussion with Hamil + Ferguson
concerning Sandia contract proposal.

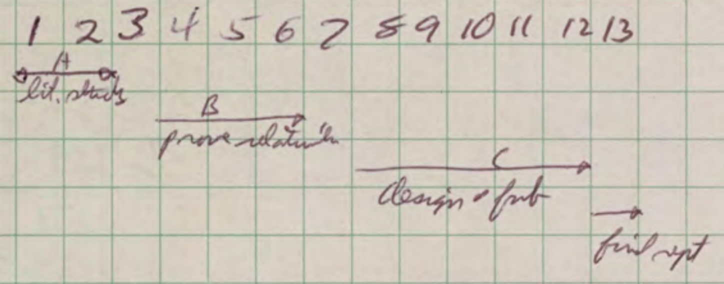
NPM - Proposal due date is 6/1/62 at Sandia

It looks like the 2N917 (1210) is off by a factor of 4 in f_T)

The difficult problem is concerned with the 0.1 ma, −55°C.

What needs to be done?

Phase A - Paper study
Expand VHG relationship.
Measure τ vs T for radiation damage centers
Measure better value of rad. damage const.



Cost estimate basis

	A	B	C
Lauritzen	1/2	1/2	1/2
Gary Parker		1/2	1/2
H. Wolf		1/2	1/2
P. Ferguson	1/8	1/8	1/8
CTS	1/8	1/8	1/8
Brian Jones		1/4	1/4
Tech.	0	1	1
Exp. Assembler.	0	1	2

∴ MTS = 1000 hrs
Tech Sect Head = 500
Asst Engr = 1250
Sr Engr = 420
Technician = 1670
Exp Assembler = 2660

May 24, 1962 PNP PMPM

Ferguson
Shimil

4500, 4700 ok
1740 "
1741 "
1746 50 CEO "
} all in prod.

1731 bunident 5 stripe (all ½ mil)
3501 an obsolete product not going to production
3510 small trident
4510 big trident
~~3510~~
1712 bunident 3 stripe, ¾ mil emitter

Of the pair {1731 {1712 the preferable one looks like the 1712. This is an excellent PNP. It is ready (?) for Xfer — ie, ready to be made in Mtn View.

PUSH {

The 1712 will use an oxide removal step in the emitter.

We will take a piece of paper with the objective spec, comparison c̄ 2N2411,2; and a statement of what's new.

We will offer a die supply starting in 6 weeks: finished units in enough quantity to evaluate, and X-fer memo.

3510 — It is 1741 diffusion, 1746 resistivity, trident masks
Start making in Mtn View
Schedule — Dice (or units on their option) now
Prod. Manl to them July 1

4510 — (Mainly for Autonetics who insist on 0.002 wire) (30 mil center)
There is a thermal resistance increase.
This gets within GTE spec and still has the current handling capability without base ~~[illegible]~~ pretreat.

4700 diffusion to make 4500 replacement.

Mtn View to make split runs.

May 29, 1962 - Section Meeting

We will go ahead and get a tech for mask making.

On new S&R the chuck must be mounted still. We are only a few days of mounting this. Hopefully we'll be checking out next week.

First test on the copy camera are this afternoon.
We hope to use the " " routinely by Monday.

Main complaint - no N_2 yet.

Basic Chem - 1
" electronics 1
" Eng transistors - 1

Jim Campbell would be happy to teach something.

May 29, 1962 — PNP Product Planning — Almost Everybody Attending

Sporck
Yost
Bay
Grinich
(Not Ferguson)

stop 2N996 registration

Device	Status
4500	— Running
~~1740~~	— out
1741	— Running — Registered, but ~~c~~ C_{TE} = 11pf.
1746	— Needs spec -35 v LV_{CEO} spec — same β as 1741 — ~~not~~ sold yet.
4700	
4701	
1731	
1712	
3501	
3510	
4510	

There are two trident I geometries in R&D — 11.5 and 12.5 mil eq. circle diameter.

There is a serious C_{OB} problem here. It looks like even the 11.5 mil one will be too big for the 1741 spec.

We have sold 869 + 995 (Parent 1740). These can be done by 1712.

We have been stalled by the 2411 — It has a 10 ma, 5 v, I_{EBO}, but a 140 Mc f_T

It looks like 3 devices will do the job:

1712

1712 geometry meeting the 2N2412.

3510/1

We may need a low current PNP, but it looks dubious because ~~of~~ stability.

except we still need 4510 for Autonetics

After discussion make

1712
3511, low voltage for new markets, 1740 diffusion, but
4511, high voltage for 4500 replacement.

1740 }
1741 } {2N869, 2N995, 2N996} → 1713 ~~1740 diffusion~~ ft >140, LV$_{CEO}$ > 20, I$_{EBO}$(5v) < 10ma
1746(P) }

2N2411 }
2N2412 } → ~~1712~~

2N501 }
Ge Mesa } → 1712 ft 400, best fast switch LV$_{CEO}$ > 8v
2N996 }

4500 }
4700 ↓ }
4701 ↓ } → 4511 (Need 3000 by Aug) 4700 diffusion
3501 ↓ }
Trident I (4700 diffusion) }

New Markets (1741) } → 3511 1740 diffusion, LV$_{CEO}$ > 25

↓ Means drop

4511 drawings down ~~[illegible]~~ Mtn View, 30 mil masks to be made here and blasted through.

1712 Product manual + 200 chips /week starting July 15 and continuing until Mtn View makes their own dice. Mtn will make new masks (≤20 mil spacing)

3511 Does not have the material in the line yet. Present masks are 30 mil, they are being re-stepped.

1713 Sept 1 for product manual

1746 will continue for now

DEFENSE PRODUCTS DIVISION/PALO ALTO

To: J. Gorry

cc: M. A. Moscarello
R. N. Noyce
H. S. Bobb
G. E. Moore

Subject: Schedule Information
PR 15180

From: R. H. Norman

Date: June 4, 1962

Listed below are the various subtasks which will be performed by Semiconductor as I now see it. Where completion times are noted, they represent desirable dates, except those times associated with July 17, which is a final contractual date. Completion of those tasks up to a week before, or 10 July, would be desirable.

If you would please schedule these subtasks out and let me know time and manpower requirements by Tuesday afternoon, I can then put together a reasonable schedule on time and manpower for the job.

At present it looks like there will be more money in the kitty for R & D than was originally scheduled. I'll know more on that Wednesday morning.

A. Subtask IV - Circuit Development

1. Determine masking and other limitations on die size for a function (R & D) (Comp. 17 July)

2. Recommend final basic gate configuration and physical structure (R & D) (Comp. 17 July)

3. Deliver 30 good units - basic gate structure in multi-lead TO-5 cans. (R & D) (Comp. 17 - 24 July)

4. Determine first preliminary device parameters and rough test specs. (   ) (Comp. 3 August)

B. Subtask V - Basic Circuit Fabrication

1. Deliver 560 good basic 3 input gate structures. (R & D ?) (Comp. 21 August)

2. From test results deliver preliminary d-c test spec. (R & D ?) (Comp. 19 September)

C. Subtask VI - Packaging

1. Starting with a package description of a flat (microbloc) TO type multi-lead package on 17 July, procure and have on hand 1000 good packages - useable for micrologic type production. (Hank Roos)

2. Deliver 100 packages of the type specified in 1. above for use in packaging mockup. (Hank Roos) (Comp. by 24 October)

D. Subtask VII - Phase III - Circuit Development

1. Starting around the 16th of August, upon completion of breadboard evaluation, perform the necessary masking, diffusion assembly and end of line environment steps to produce a minimum of 400 (desirably 450 - 500) good Phase III elements. The Phase III element will be the most complex one in the family. ( )

2. Fabricate die sort probes as will be needed for die sorting these functions. An electrical die sort tester will be available. A simple classification tester will be available by 19 September. ( )

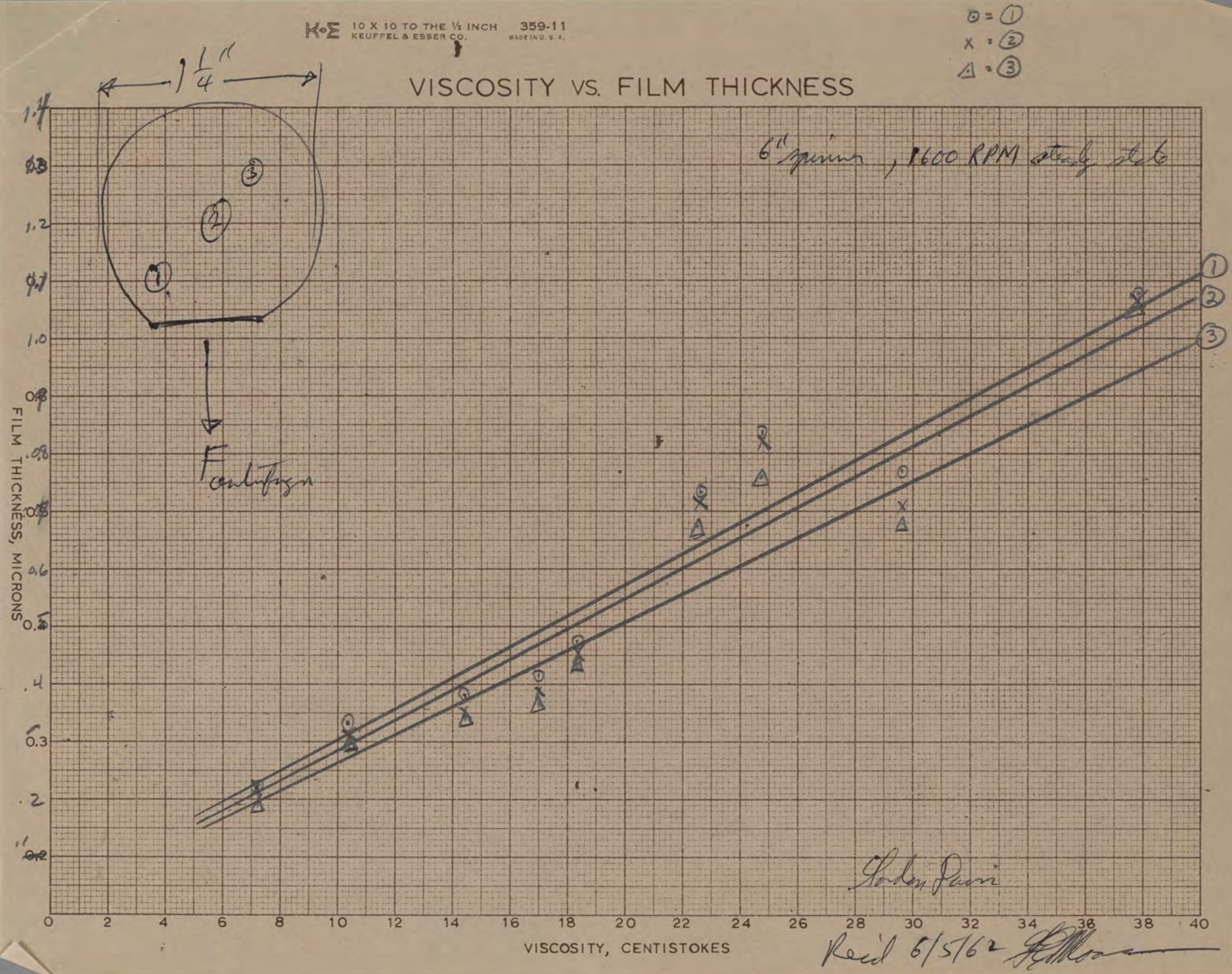
E. Subtask VIII - Reliability Evaluation

Perform reliability evaluation on 350 integrated logic functions as per original proposal from the Reliability Department. Compile and deliver all reliability test results. (J. Farley)

R. H. Norman

RHN:df

VISCOSITY VS. FILM THICKNESS



6" spinner, 1600 RPM steady state

Gordon Davis

Rec'd 6/5/62

June 4, 1962   Meeting on contract.

Norman
Schultz
Sorey
Ferguson
Grinich
Moore

Ground rules:

1. It will use existing technology. This means existing μL technology. Can consider Bunder E resistors as a possibility.

RHN thinks he has money that can be used for extra R&D. This is true, partially because of the lack of need for packaging.

The element that RHN would like to consider as the most complicated is 15 Xstor, 6 node, 6 base resistor shift register stage.

Type of ckts (DCTL, T²L, ?)
Max size, etc.

Anderson will work full time on phase I

A set of bit elements can be given to RHN
RHN will then ask us to ∫, , package, and reliability test.

Discussion c̄ Sah + Hale on evaporation service

Should have:

1. Conventional evap.
2. Sputter
3. Vac brazing
4. Electron beam & resistive heating

Exclude

1. Pilot line
2. Mag. film
3. Thin film tunneling
4. Probably Campbell's system

Available for service:

1. Hales, tank ~~service~~ system
2. UHV
3. Eventually (?) one of Campbell's
4. Sapenar old one
5. Demmil
6. Kobell
7. Seifers

June 5, 1962

Project ROBE meeting

Mtn View
Hill
Yost
Roder
Gordon Davis

San Rafael
Mann

Palo Alto
Moore

Hill:

Recap: Old facts
→ 1. Pinhole free oxide exists after 1st oxide (
2. " " " on seriously contaminated oxide
3. Oxide etch appears to make pin holes
(appears to be selective)

New facts:

Roder:

1. Sandor confirmed Roder no pin-hole
2. None of a group of strong (and weak) acids for leaching made pinholes
3. NaOH did, however, dissolve the pin holes.

→ 4. No pin holes at the step between oxides, both with and without predep.

→ 5. Coat wafer, expose whole surface, oxide etch per usual, clean, O_2. Pinholes on the KPR side, none on black wax side. These were
a) At very high density
b) In a pattern over the surface of the ~~wafer~~
This used std. 4200 KPR.

→ 6. As a side experiment, one wafer dropped on the floor just before exposure. It was carried on. It showed for X 5 - 10 increase.
(Under dark field a large # of white spots appear. These are mostly not pinholes).

7. After 10 min of O_2 etching all the pinholes that are going to develop on longer exposure.

Davis:

→ 1. Taking a constant coating cycle, but with increasing viscosity (ie, increasing thickness) the incidence of pinholes decreased monotonically. ~~and~~

ROBE, cont.

Davi, cont.

2. There is no evidence that the pinholes concentrate at the edge of the device.

Suggested approach:

Roder 1. Study substrate smoothness on pinholes in film.

Davi 2. Isolate those pinholes that are contributed by the mask only.

From this we should go to the heavy APR. In order to do this we info on the relative resolution.

Meet in 2 weeks again @ 2:30. June 19th.

June 11, 1962 Moscarella, Noyce, Grinich

We are committed to deliver 10 ea of the breadboard ckts after environmental test;

We are going to test 300 phase III elements.

The ~3000 bit elements and the integrated ckts will be made in the Mtn View factory. (Cam

Norman	Lee
Grinich	Noyce
Sparck	Gong
Bobb	Campbell
Mgr. Alonzo	Moore
	Grinich
	Farley

General Mtng

Φ-I: Deliver a list of functions and ckt diagrams

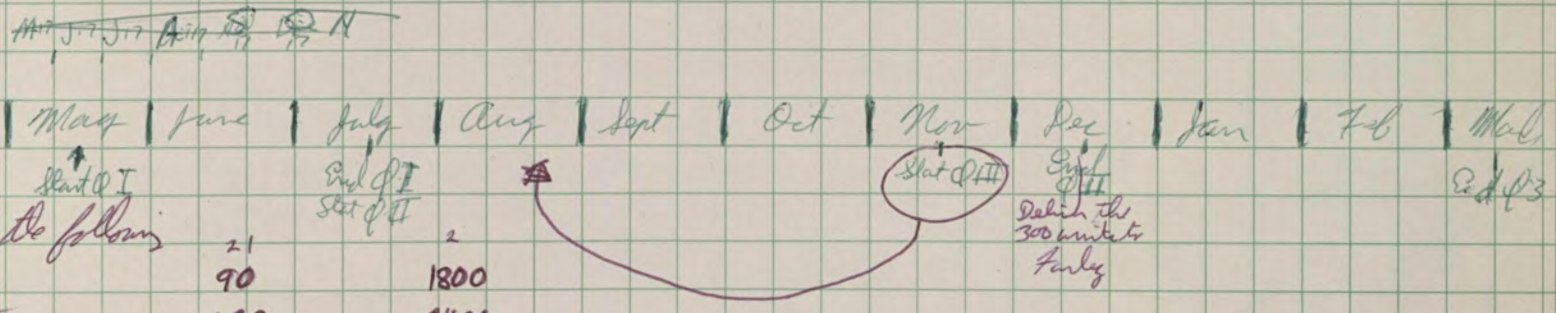
Φ-II: " 10 breadboards of each ckt

Φ-III: " 50 integrated circuits of 1 function. (Customer expects this to have been one of the most complex of the ckts.)

Estimates have been made on 10 ckts needed.
" " " " " ~~making~~ 20 breadboards of each (neglecting bit component cost)

Jay Farley needs many to test. We are contractually committed to ~~make~~ test 300. It is not at all clear that more than 50 good ones need be made.
No need for package other than flat TO- configuration.

Schedule



Norman has asked for the following

	21	2
bit Xstor	90	1800
bit Resistors	120	2400

Rough cost breakdown

	DPD	S/C
Phase I	1600 hrs	100 hrs
Phase II	$6000 material (PC Boards)	
	4500 hrs	4443 ~~3044~~ hrs
Phase III	1742	2000

Section Meeting — 6/12/62

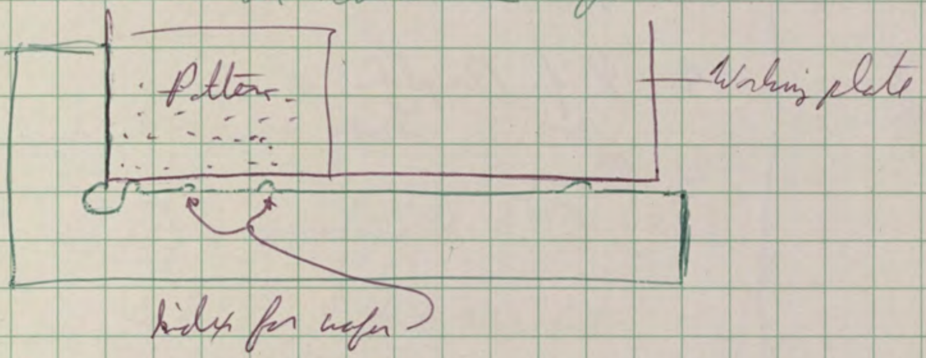
1. Our mask making capability is approaching 2 masks/day. We must change our philosophy concerning the use of masks.

We are short alignment [illegible] marks on masks. Mask making will be responsible for getting these on plates. We will try to work with color transparencies (diazo) for alignment materials

MI asks aligning is a problem

All submasks are on 2x2

Mtn View on their L-frame use



The only advantage is that alignment must be done only once / set of submasters. Disadvantage is that pattern is in very corner.

We are going to put in a 0.1 mil device in the mill.

We have 4 KΩ/□ Nichrome emitters (covered c̄ SiO_x)

We have done KMER pattern covered c̄ Nichrome to make nice, sharp lines, < 0.1 mil.

Microcircuitry Project Review Meeting June 14, 1962

Farina
Grinich
Ferguson
Moore

Proj #172

Jobs in progress:

1. Hi Speed (≤5 ns @ 15 mw) (10 over the temperature range)
    a) Ni-Cr resistor
    b) Diff resistor

2. Low power (75 ns @ 1 mw) (25 @ 3 mw)
    a) Ni-Cr resistor
    b) Diff resistor

3. TTG High Speed

4. Radiation ckty

5. µL-I Redesign / quick µL II

6. Kit device

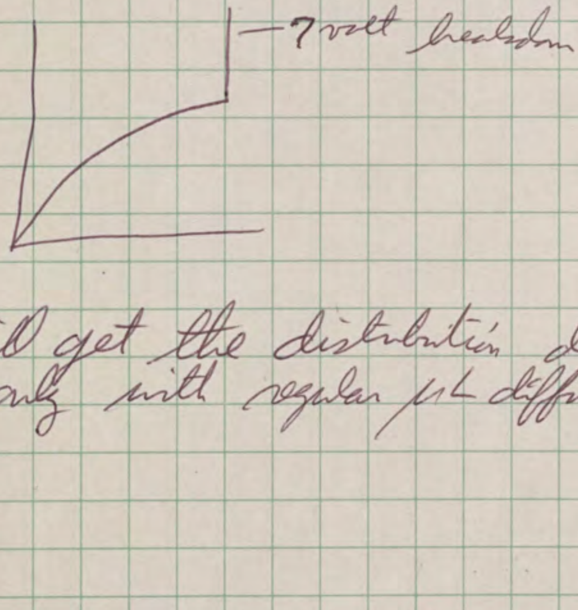
7. PNPN ring counter

8. Dif. Amplifier

9. Memory

We are trying to do 1a and 2a with the same geometry except for the Ni-Cr resistor shape.

On the B under E resistor, we have made a few.



We will get the distribution data on the B under E resistors. These are useful only with regular µL diffusions.

The present μL has a built-in 20% loss from our std tolerances on V/I & h_{FE}.

The big question is - should ~~be~~ we do a re-do on μL now?

The epitaxial is a long way away because the supply of good epitaxial material is not in good shape.

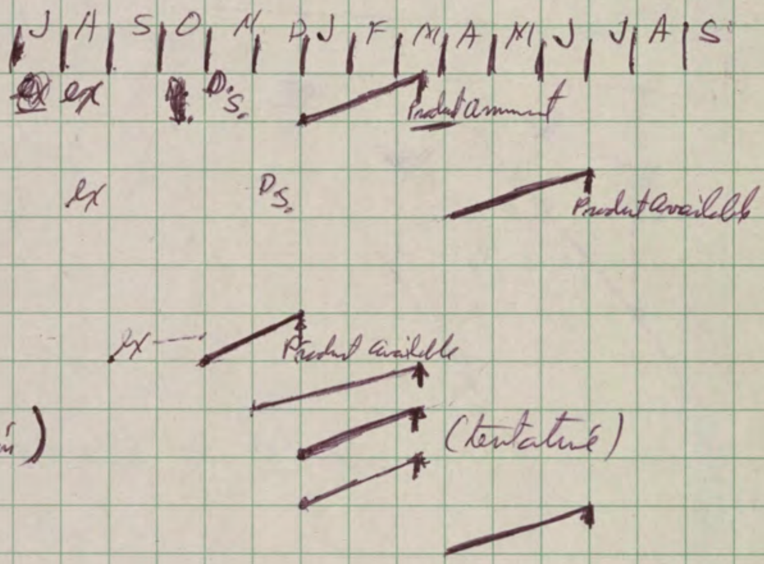
∴ What does our schedule look like?

"Families"

1. Low power gate (1mw)

2. High speed gate (5ns @ R.T.)

3. Additional Ckt components
    a) ~~Base and E resistor~~ resistor E/B
    b) Nichrome resistor (from 1)
    c) MOS capacitor (spin off radiation)
    d) Low power Xstor (from 1)
    e) High speed, epitaxial (from 2)



In order to do this is impt that
the epitaxial growing start being set up by Jan 1
" Nichrome evaporation start " " Jan 1

June 14, 1962 – Magnetic film memories

Perkins
Seely
Hale
Farina
Campbell
Levine
Ferguson
Moore
Grimal

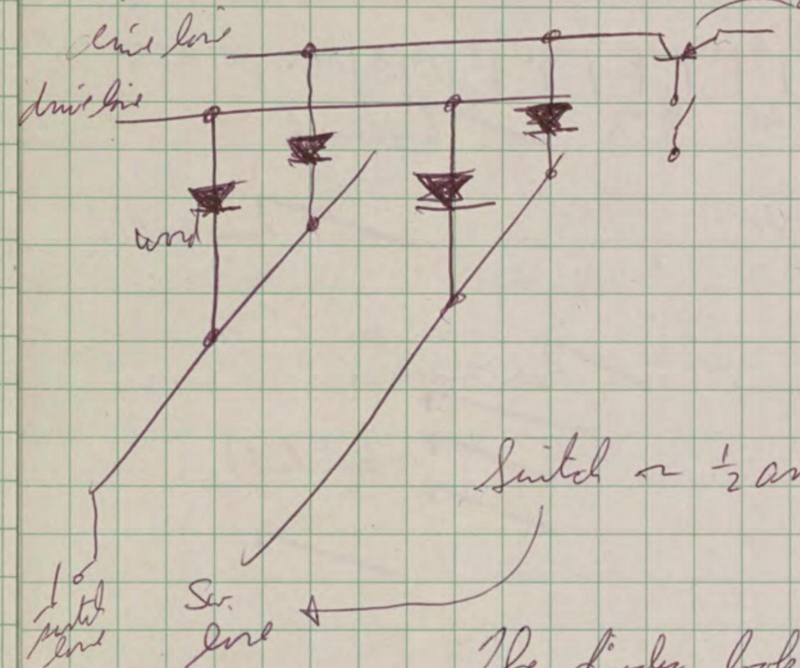
Hanley thinks that the big square one is potentially a very useful one

256 words × 50 bits looks reasonable.

S/A on speed is ~100 ns cycle time

(By comparison the Burroughs one is hoping to push to 5 Mc, IBM is in the 100 ns class)

Hope to use 4 ns rise time



a fast AMP., of the order of 100 ma.

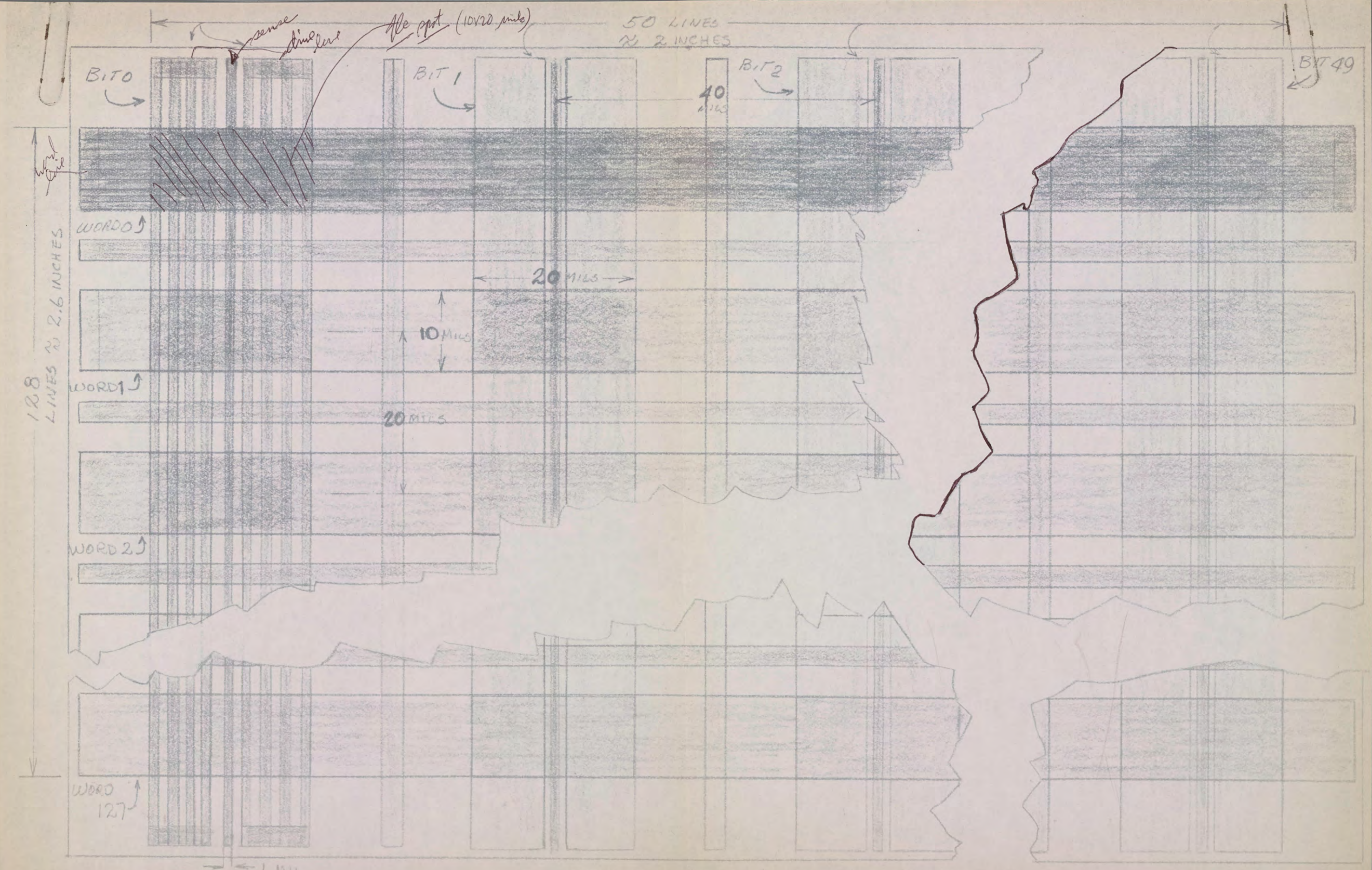
Switch ~ ½ amp, 10 ns rise time

The diodes look like ~ 1 pf.

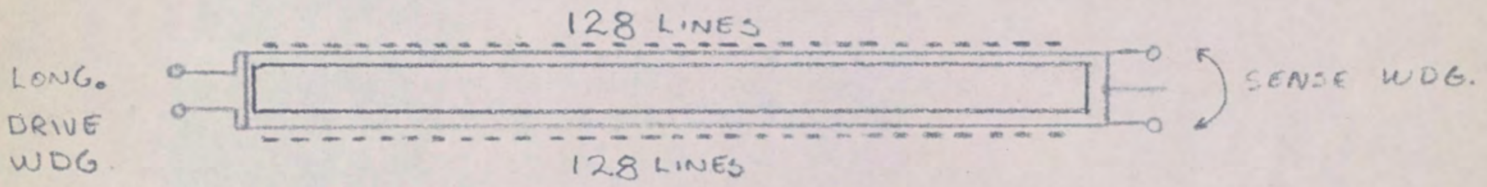
Where do we sit now on technology?

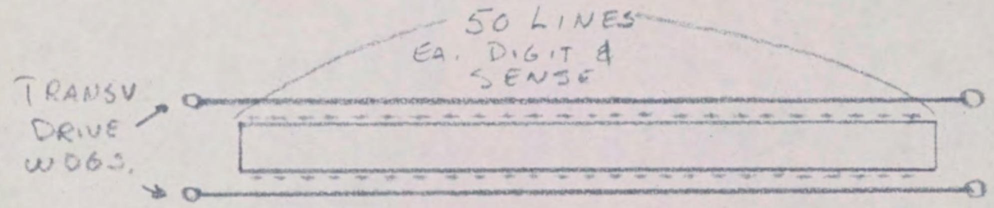
Hane

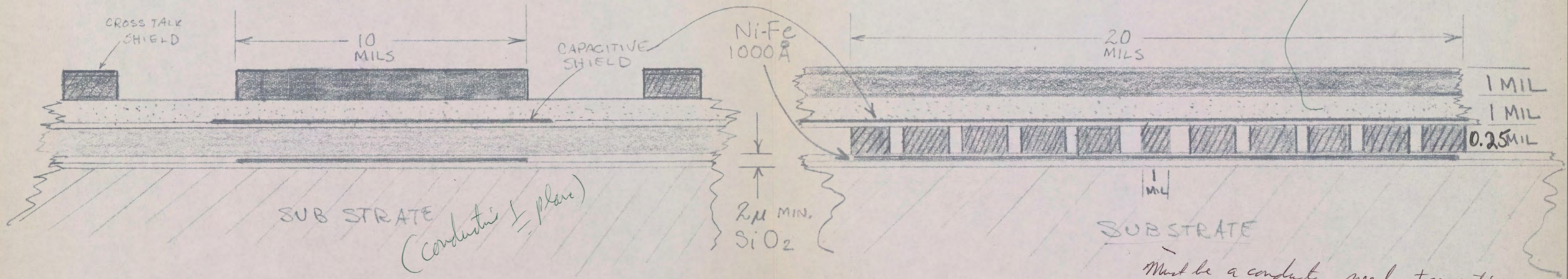
Short



MEMORY SPOT & CONDUCTOR LAYOUT





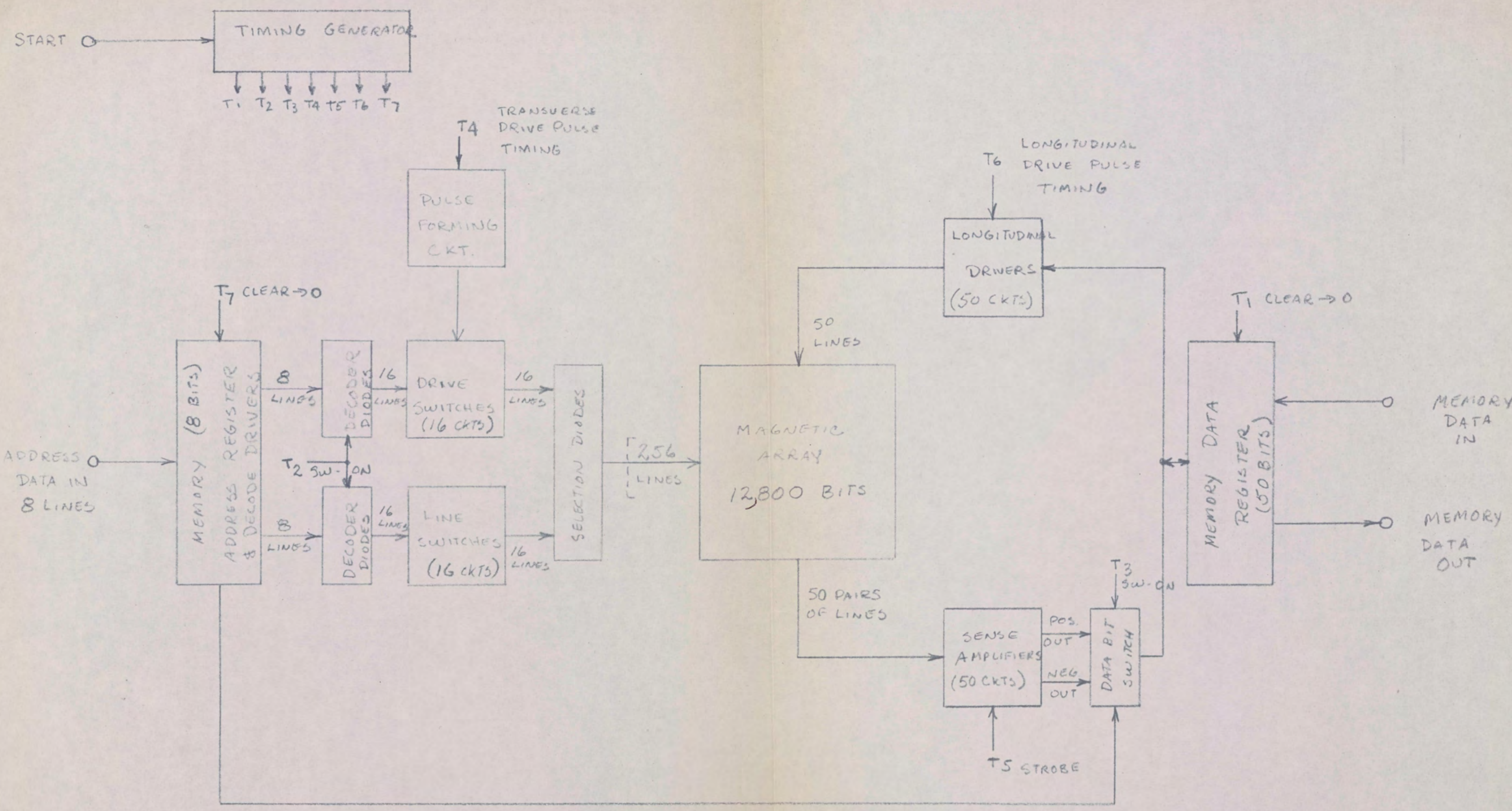


Could be added after. Might be Teflon, for example.

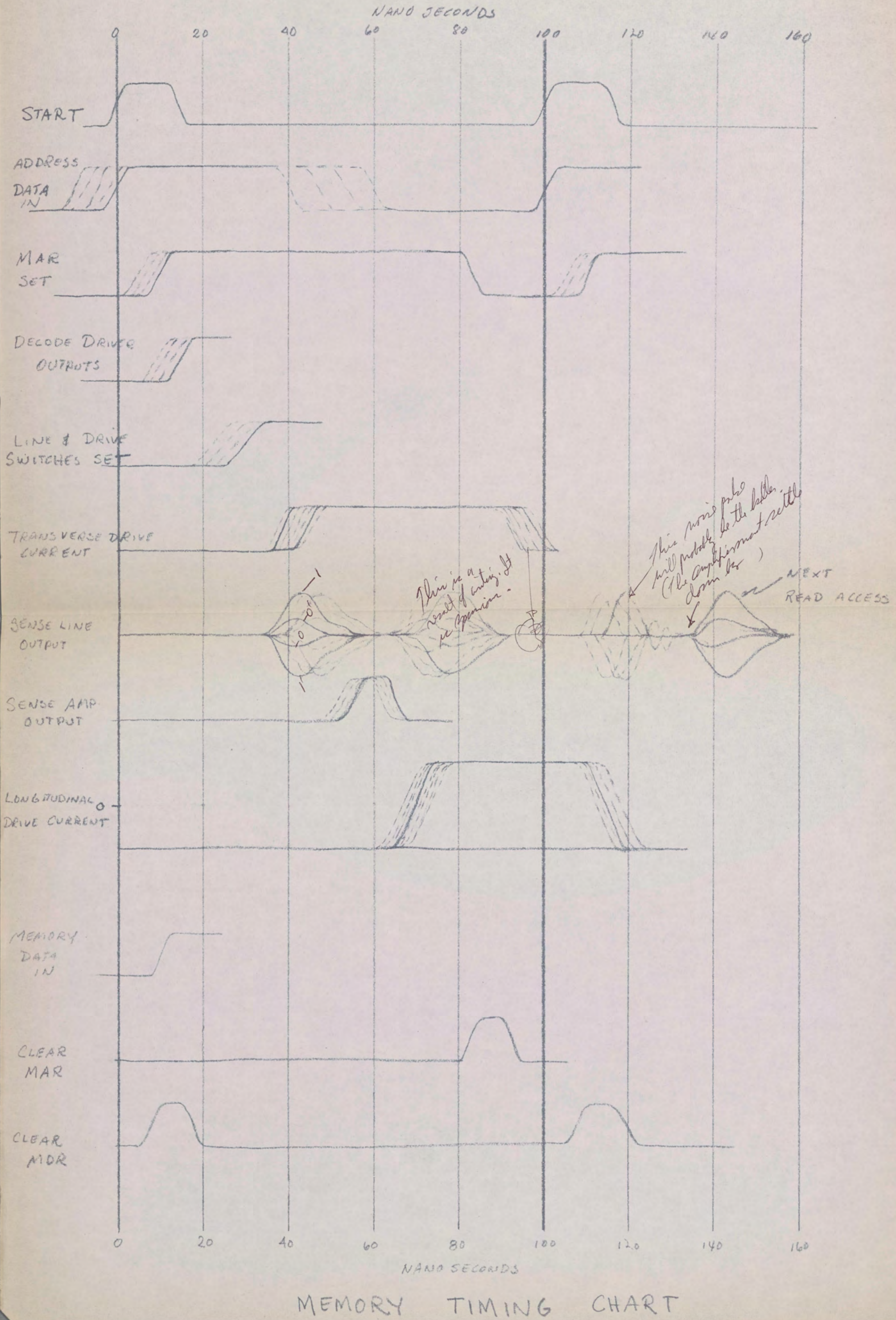
(conductive ⏚ plane)

Must be a conductor, need not magnetic.

MEMORY PLANE SECTION



MEMORY BLOCK DIAGRAM



MEMORY TIMING CHART

June 15, 1962 μL situation review

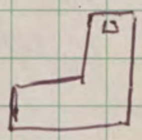
Sporck Ferguson
Noyce Moore
Blough
—
Farina

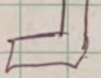
μL problems: (listed order

1. Pinholes — cleaned up by spinning, etc
2. Bonding — eliminate by going to scribing
3. Metalization opening up.
    a) just statistical - Al ~~scratches~~ easily - Optical inspection
    b) Metal was knocked off during the washing operation (Metal near bond)
        - Improved evaporation since ion bombardment & more inspection

4. The S-element
    Pretty good luck on B-stepping (no inverter)
    Bad yields on C- " had several problems including no cut out
    D - " (new pattern, no ears, open b's, 1 mil collector)
        This had low r_b.
        The 1 mil collector was ok.
        The big change was that the 2 mil resistor had too small contacts and this seems to make ~50Ω increase in r_c. ∴ the r_c and r_b went in opposite directions.

D still gave better than C, but just after this the V/I of the base diffusion drifted up.

The E-stepping was  instead of , but with everything the same — ie, wrong collector

The F is like , but with longer wing by ½ mil. Aims at

The Z-stepping uses a complete redo — longer connections to isolation, etc.

The best we can expect to the "A" spec accepting β = 40-150 is

all except G (F/I = 2) = 60%
G F/O = 4, F/I = 3 = 50%
5 = 40%

June 14, 1962

7 hr PPPM/MC - Small Geometry

Ferguson
Grinich
Moore

1250 — They are doing development
1321 ISO —
AGC demo (0001) — (Development compl ~ Sept 1)
1ms (— not in disc. yet
LaFET (FET-2) — Blast on
Small trident (3010) — in Mtn View
1221 (~200 mw @ 500 Mc) — being evaluated by
0002 (1W @ 500 mc) —

? Does the inclusion of an "oxide" over Al stop P.P.? JPF

? Does the $\frac{BVCBO}{LVCEO}$ ratio change with the inclusion of Au. spec and to Mtn View CTS

? Does the use of Sb vAs diffusion in the epi substrate make for lower storage without problem? JPF?

RoD must get ahold of the IBM spec (incl the circuit) and design a specific transistor for the application GM

RoD will develop a no. of device for this family in the 3-4 mo time scale

Small geometry p.p. meeting June 15, 1962

Everybody here
(24 people)

1244 — Use to replace 1240, 1243 as material problem disappear.

1211 — By July 8 get 2-3 stripe ~~diffusion~~ devices and can 1211 ~~be~~ replace 1210?

Header problem is rough! (Single island TO-18 is still in ~~use~~ mill)
We presently use the bridge.

1321 & 1324

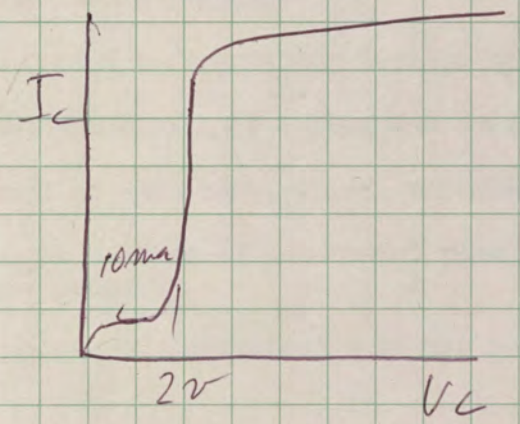
1321 is running — short on volume, majority base is running.

This has developed a yield problem — V_{BE} (problem has occurred)
The 1321 is 13v V_{CEO} max

1324 — 40v V_{CES} needed to make 15v LV_{CEO}

$\frac{40}{15}$ at first $\longrightarrow$ $\frac{40}{12}$

3011 → 5 runs at Mtn View are all dogs!!



Thermal resistance is also a problem

3010	30 mil	C	~~30~~ 47°C/watt
	30 mil	A	77°/watt
	45 mil	A	70°/watt
4200		A	47
		B	72
		C	27

1250 — Real trouble meeting β's. and simultaneously holding punch thru

1221 — We will develop c̄ transfer mono & dice.

U-1, U-2 — We will work on noise and do all fab until the problems are solved.
Wtr. will maintain a regular, limited assembly.

INTER-DEPARTMENTAL CORRESPONDENCE

FAIRCHILD
SEMICONDUCTOR CORPORATION

To: List **CC:** **Date:** June 18, 1962

Subject: Project Review Meeting (#162)
Silicon Epitaxial Service & Research

From: C. T. Sah

A project review is scheduled at 1:00 P. M. Monday (today) in my office.

Verbal project progress report will be given by E. Yim and H. Wigton separately on the works done including:

(1) High resistivity film both n and p type

(2) Film-junction, both n on p a p on n

(3) Control and uniformity of layer thickness and resistivity of the above film.

The discussions should include:

(1) Requirements from Device Development

(2) Brief discussion of method and apparatus of growth and doping

(3) Number of runs made, yield, variation and spread of characteristics of film

(4) No. and percent of successful runs and material delivered to Device Development.

The run data should be summarized from the actual run sheet.

C. T. Sah

CTS:jt

List:

E. Yim
H. Wigton
P. Ferguson
P. Lamond

FORM 5120

June 18, 1962 — Epitaxial problems - Si
Project 162 - Review

Sah
Wigton
Yee
Ferguson
G. Parker
Lamond
Moore —

Ernie Yee on recent dev. dev. requests.

On NN$^+$:

There is still a correlation problem

For example, on high ρ NN$^+$

#	Actual*	Recorded†	Channels?	Problem
3-146	80	180 (160-200)	no	No correlation
2-146 C	50-60	120	no	(mislabeled - slotted base 55v)
3-180	60-80	120	no	
3-126	60-90	240	some	
3-135	60-80	280	some	
2-146 A	100	120	no	

* Just after base diffusion (~2μ deep) c̄ planar diode.

† Just a heavy B predep. and mesa diode.

Gary & Ernie will do a correlation of evaluation results.

In the lower range (~50v) the correlation is very much better.

Gary need 150-200 volts BV_{CBO} junctions in the device, except he really only needs high ρ low.

— In any case, we ~~still~~ get a channel that is different from the std. channel in that the channel does not disappear upon HF treatment.

Split runs with regular material show none on regular material.

These would be good to study with the Field Effect experimental structure!!!

It looks like there is a P layer on the surface.

Gary will try Pierre's etch.

OQO I should issue an instruction that all developmental devices must run through n runs using material from Peterson's area.

Large area, high resistivity material

Problem is basically pyramids.

We do fair on Merck – avg ~3 devices per starting wafer.
On our stuff we run run 100% E-C shorts, even though we have some good CB junctions after base diffusion.

1. Std material

2. Slices at special

3. Technology control
   a) Pyramids
   b) diffused substrates
   c) control of thickness
   d) channels, etc.

FAIRCHILD SEMICONDUCTOR CORPORATION

TO: Martin Oudewall
DATE: June 14, 1962

FROM: Norman Peterson

CC: P. Lammond
P. Gupta
C. Sporck
F. Bourassa
M. Judge
W. Wheeler

SUBJECT: Material Supply for Device #7000
Purchase Order #MV 17258

A meeting was held on June 14, 1962 to evaluate the material supply situation for the 7000 device line. Representatives of both Fairchild and Merck attended and although no decision was reached regarding supplying production quantities for this product, the following program was outlined.

1. Merck presently has no inventory of 7000 type epitaxial material.

2. Merck will produce 50 production wafers and submit for our evaluation.

3. We will photograph each wafer surface and note evaluation rework on back of each photograph.

4. If we feel surfaces are reasonably acceptable we will send 25 wafers each to R&D and Mountain View, and will notify Merck, inorder that they can produce an additional 50 wafers.

5. R&D and Mountain View production lines will retain the identity of each wafer for comparison to Materials Department evaluation.

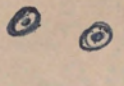
6. If we feel the surfaces are unacceptable we will send 25 wafers each to R&D and Mountain View, and will notify Merck, but Merck will produce no additional material pending the completion of the line evaluation of the first 50 wafers, and as a result thereof, the mutual agreement of wafer specifications for the 7000 product line.

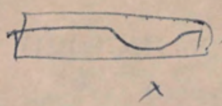
7. Earliest possible delivery date for the first 50 wafers is July 9, 1962 to Fairchild Materials Department.

Norman M. Peterson
Manager, Materials Dept.

NP:sc

FORM 5121



1. Diode breakdown correlation on existing diodes
2. Split wafer evaluation, one whole run
3. Make A&C device material ~~from~~ by putting  " profile
4. Gary will try etching
5. Channel needs probing

~~Probe~~
~~Etch off a~~ little

June 19, 1962 – Project ROBE
(See pp 23, 24)

Hill
Yost
Rodes
Davis
Brown

Ferguson
Moore
Folz
Engval

Old business:

1.

2. What is the mechanism to make pin holes in KPR?
a) In the regular KPR there appear to be a large concentration of bubbles or blow-holes on the junction.
b) In the thicker film (3:1) it seems that there are fewer.

New:

1. Pinholes associated with masks.

2. 1st approximation to std technology.

~~Pinholes~~ Imperfection in masks – pictures taken on shadowgraph (with frosted glass illuminator). of new masks.
Sam points out that the examination under diffuse light is not too critical.

c̄ 49 cs. viscosity 1.3 l.l., 1.2. center 1.1 μ upper right ← Coating thickness

Criteria:
1. "Pinholes" — A subjective count of structural features in oxide.
2. Oxide removal
3. Pattern definition

Compare 4 development systems by 1, 2, 3.

The results are not clear-cut (to say the least).

Exp (sec	Dev.
1. 10	1. Eastman 2 min, xyl - 15 sec
2. 20	2. " 4 ", " - 30 sec
3. 40	3. TCE 2 ", isop - 15 sec
4. 60	4. " 4 ", " - 30 sec

Probably best compromise 20 sec and #2 developer.

ROBE, cont

Roder: Surface effects on pinholes in oxide

The original oxide is always pinhole free.

The KPR coated experiment compared

a) Mech. polished by diode tech

b) CP-6

all cleaned together, oxidized together, etc, together

2.3/ pattern on chem (may run 10-15 compared to >30 before)
0.49/ " " mech polished

Plans: (for next time)

1. Continuing the exposure - development system
   a) Examine more system
   b) Settle on one
   c) Optimize this system

2. Is KMER a necessity? (The factory is floating on to KMER)

3. Implementation
   a) In wafer prep, 1st draft of standardization technique
   b) Pinhole reduction, - data will be in.

Try Au-Al metallization to T.C. bond Au to.

June 21, 1962 - GaAs Project Review

Sanders
Augelin
Schulenburg
Sah
Moore

1. On Steve's work

Aim at study of $TiO_2 - SiO_2$ codeposition for a solution in 3 mo, if possible.

Use other time to tackle making a good GaAs diode and get diffusion data.

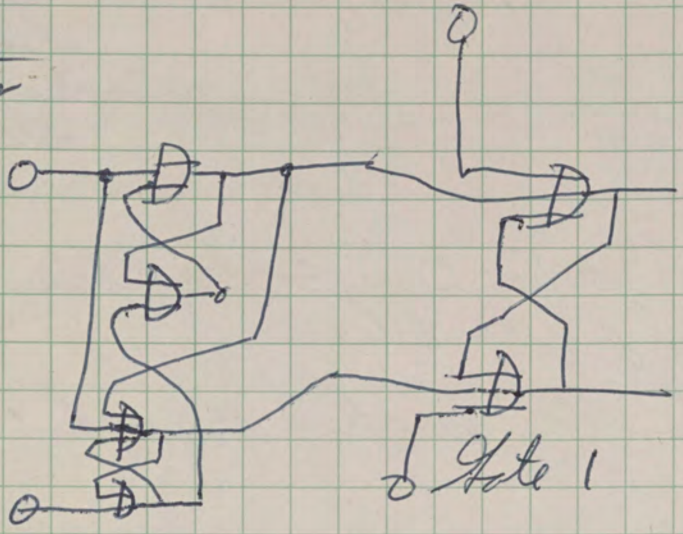
2. On Schulenberg's work

June 21, 1962

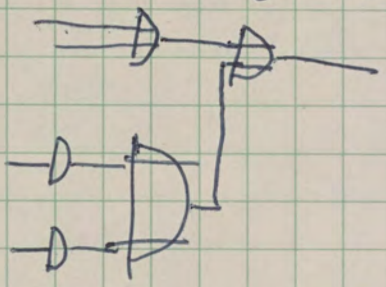
Norman
Sevin
Bogert
Ferguson
Moore

Elements

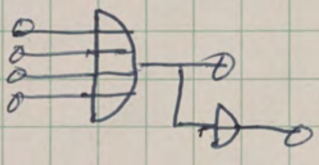
R



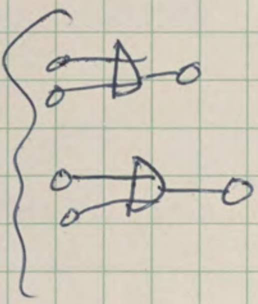
Adder



Gate 1



Gate 2



+ Buffer using all T_1's.

Go go go! on R we will help.

Relative number

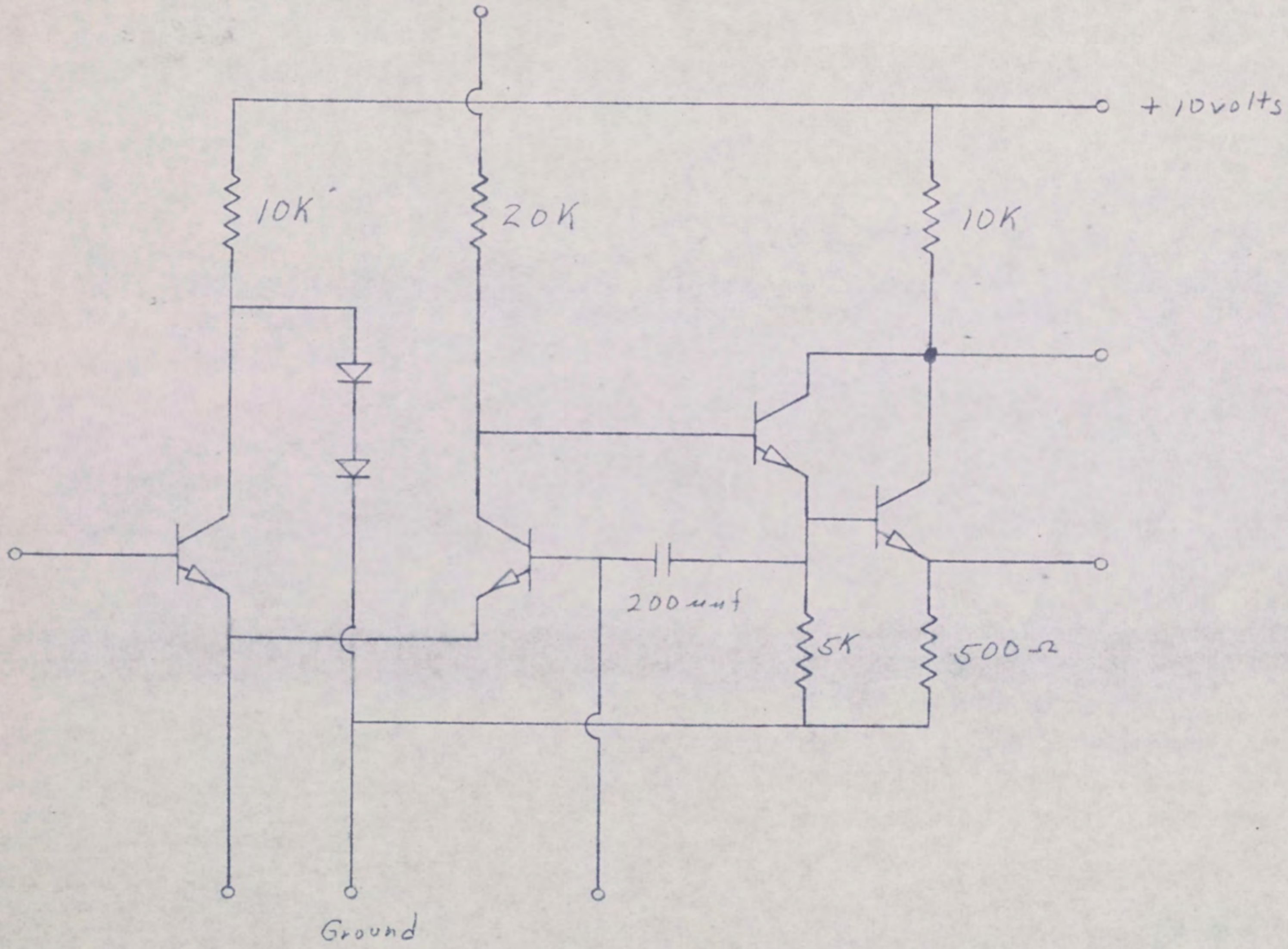
600	R's
200	A's
150	Gates
50	Buffers

INTEGRATED PREAMPLIFIER - DESIGN OBJECTIVES

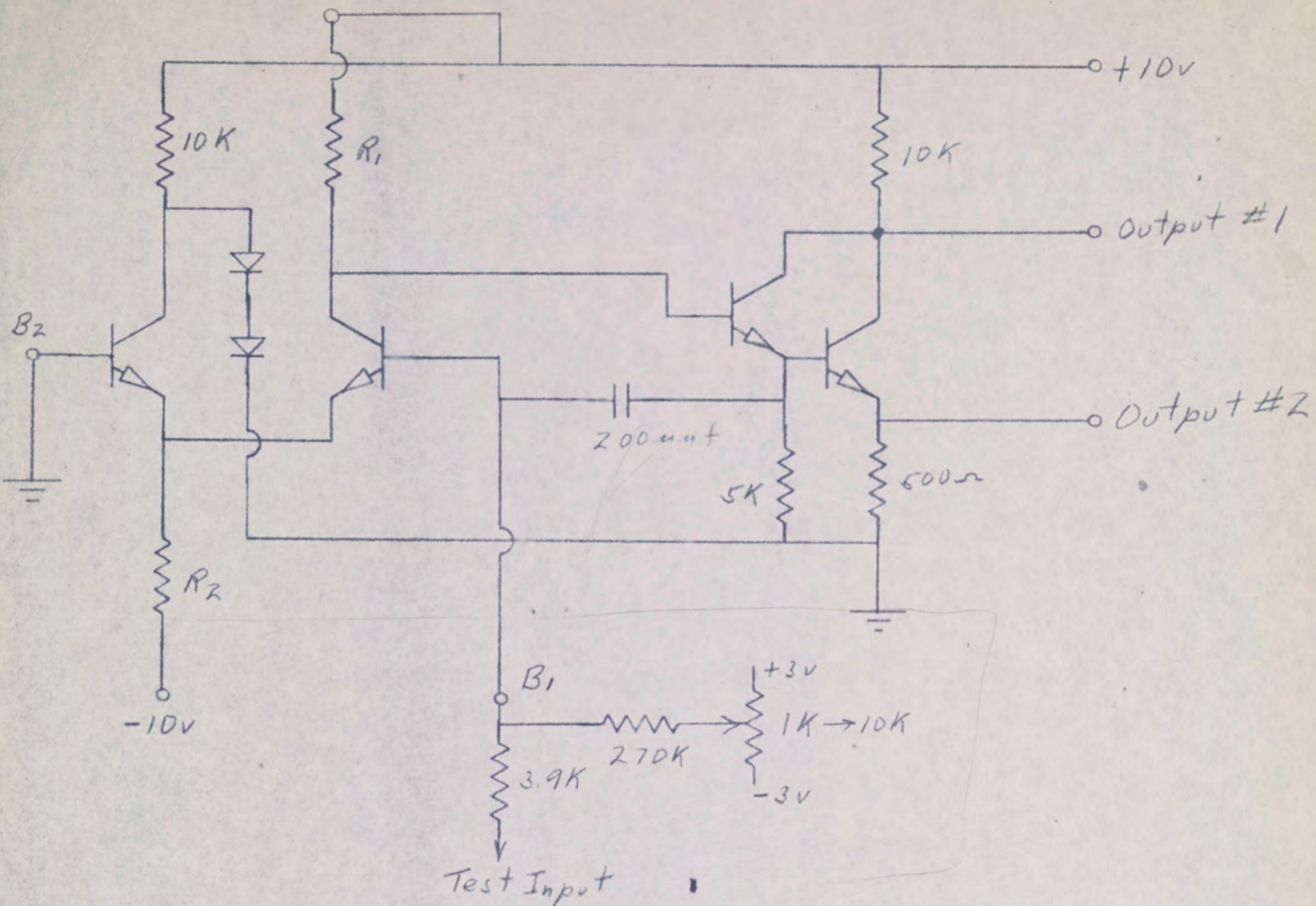
1.	Supply voltage	+ and - 10 volts
2.	Gain	1000 min open loop.
3.	Gain at 20 KC (Figure 1)	160 ± 50% 6 db/octave roll off
4.	Output impedance	less than 10K
5.	Output dynamic range	7 volts peak to peak minimum
6.	Gain polarity	positive or negative depending on external connections.
7.	Input referred voltage drift	Less than 10 mv with 50 K source impedance and from -55 to + 100°C.

VAX = TFX extension Inertial machine for Navy
(They "have" 10 systems, - 15 systems F-110.

Integrated Preamplifier



Integrated Preamplifier Tests.



Condition A: $R_1 = 20K$, $R_2 = 10K$

Condition B: $R_1 = 200K$, $R_2 = 100K$

CONDITION A

BIAS CURRENT
B_1 = 5.6 μa
B_2 = 6.9 μa

for both COND.
Output GAIN
TEST
3 MEG IN R_1
just saturates
output

FREQ	V_{IN} IN MV	V_o #1 PEAK/PEAK	V_o #2 PEAK/PEAK	GAIN $\frac{V_o \#1}{V_{IN}}$	GAIN $\frac{V_o \#2}{V_{IN}}$
500 c/s	2 MV	3.8 V	175 MV	1,900	87.5
1 KC	" "	3.4	155	1,700	77.5
2 "	" "	2.4	110	1,200	55
4 "	" "	1.4	65	700	37.5
10 "	" "	0.60	27	300	13.5
20 "	" "	0.28	15	140	7.5
40 "	" "	0.15	8	75	4
100 "	" "	0.05	3	25	1.5
200 "	" "	0.02	1	10	0.5
400 "	" "	0.005	—	2.5	—

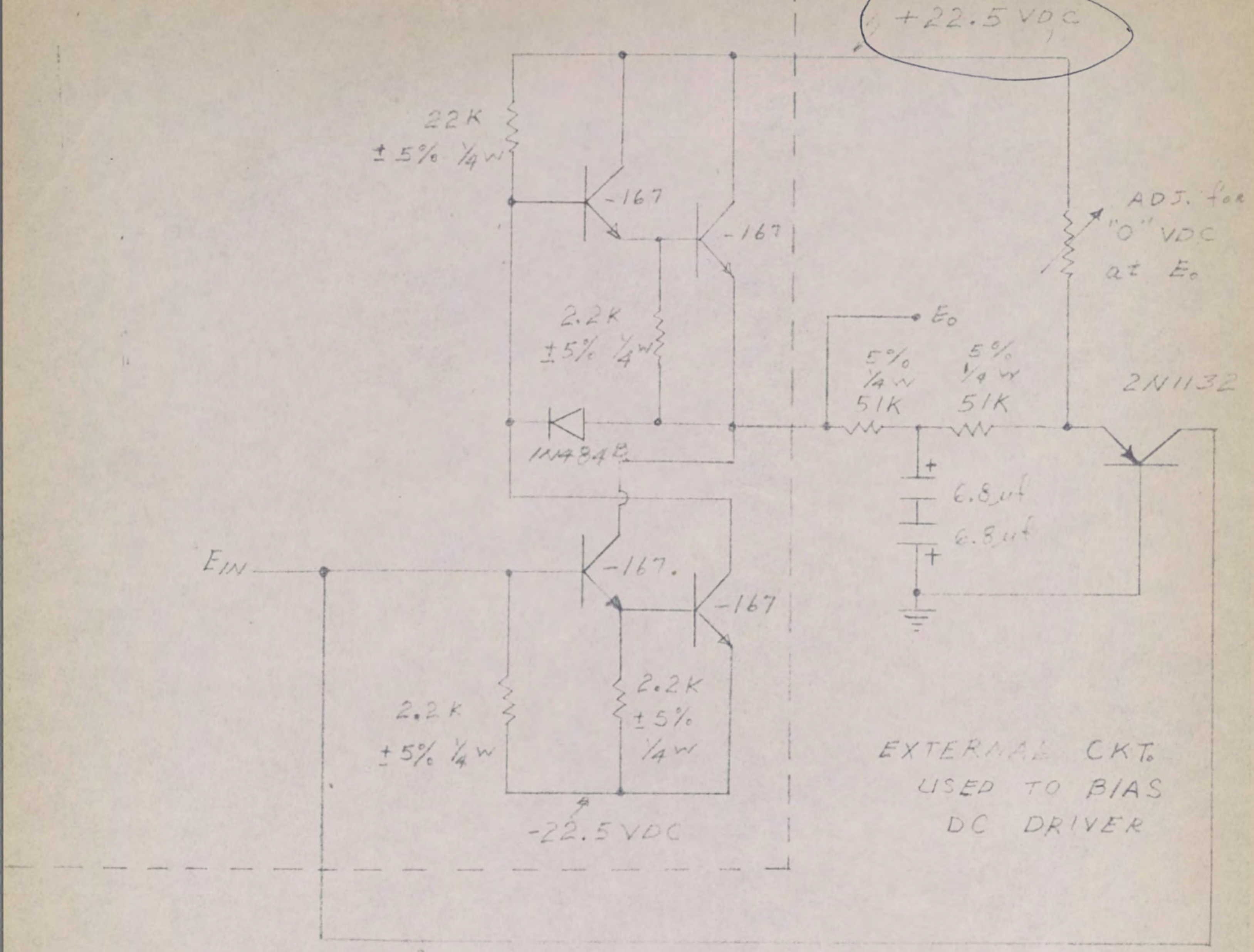
CONDITION B

BIAS CURRENT
B_1 = 0.67 μa
B_2 = 0.9 μa

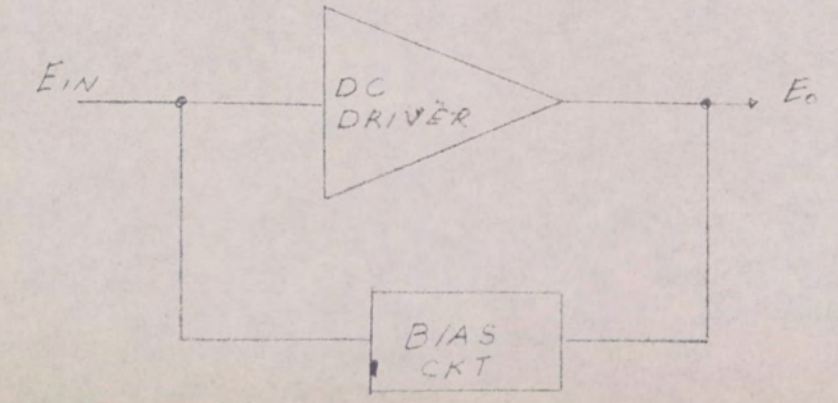
R_1 = 200K
R_2 = 100K

FREQ	V_{IN} IN MV	V_o #1 PEAK/PEAK	V_o #2 PEAK/PEAK	GAIN $\frac{V_o \#1}{V_{IN}}$	GAIN $\frac{V_o \#2}{V_{IN}}$
500 c/s	2 MV	3.25 V	150 MV	1,625	75
1 KC	" "	2.8 "	128 "	1,400	64
2 "	" "	1.8 "	85 "	900	42.5
4 "	" "	1.05 "	47 "	525	23.5
10 "	" "	.44 "	20 "	220	10
20 "	" "	.215 "	10 "	107.5	5
40 "	" "	.105 "	5 "	52.5	2.5
100 "	" "	.040 "	2 "	20	1
200 "	" "	.018 "	—	9	—
400 "	" "	.002 "	—	1	—

DC DRIVER



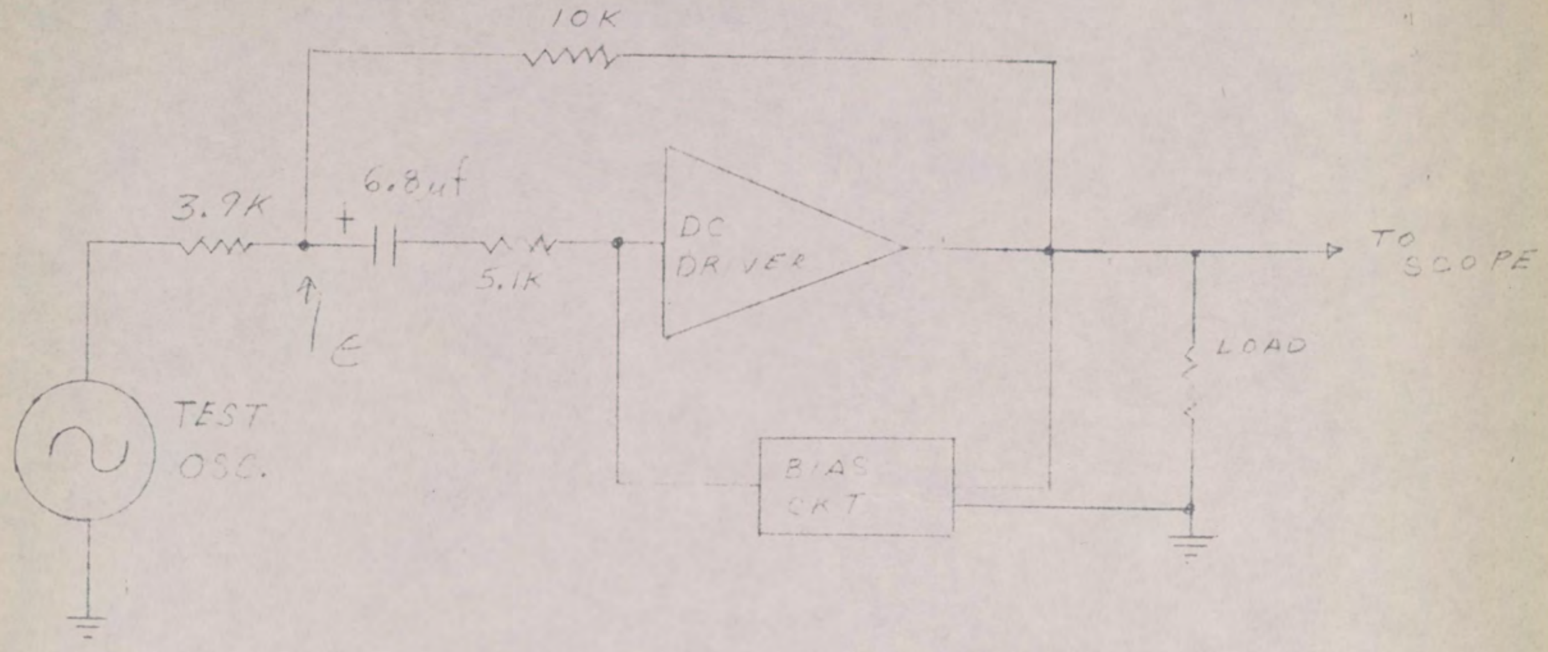
EXTERNAL CKT. USED TO BIAS DC DRIVER



BLOCK DIAG. of CKTS. SHOWN ABOVE

FIG I

I. ARRANGE FIG. I IN A CLOSED LOOP CONFIGURATION WITH VALUES SHOWN BELOW



II THE FOLLOWING ARE TEST DATA COMPILED FOR THE CONFIGURATION SHOWN ABOVE

FREQ.	DEGREES Ø SHIFT	GAIN	MAX Vpp ACROSS LOAD WITHOUT DISTORTION	LOAD
100 c/s	0	2.5	40 Vpp	2K
1 KC	0	2.5	"	"
5 KC	0	2.5	"	"
10 KC	2°	2.5	"	"
15 KC	5°	2.5	"	"
20 KC	7°	2.5	"	"
25 KC	7°	2.5	"	3K
30 KC	7°	2.5	"	4K
40 KC	8°	2.5		7K
50 KC	8°	2.5		10K
100 KC	10°	2.5		50K

III. OPEN LOOP VOLTAGE GAIN; A_{OL}.

$$A_{OL} = \frac{E_o}{e} = 500 \pm 50\%$$ @ 1KC INTO NO LOAD.

IV CLOSED LOOP OUTPUT IMPEDANCE Z_{CL}

$Z_{CL} \leq 200$ OHMS @ 1KC INTO A 10 ma. LOAD.

June 21, 1962 - Litton Custom ccts

Bay
Graham
Shinle
Richward
Farina
Ferguson
Moore

Integrated Preamp and driver for VAX. It looks like Litton will get the machine -
10 machines on dev. contract 250/syst. preamp, 60/syst driv
F-110 program, min 1500 systems (100 per system preamps
60 " " driv)

[The hooker: To get into F-110 board must cost ≤ $250.
4 preamp 2 driv 2 other driv 4 Xstrs 4 rect's
+ 20 other components (R's & C's).]

Time scale VAX program done - 1 year from now
For F-110 program ASAP - 1st prod. in Jan or Feb.

We must propose what we can do.

Let us say we will do the preamp.

5000 units @ $300,000

150,000 " @ 3,000,000

Delivery - Start @1000/MO in 12 MO.
Samples in 9 MO

R&D samples ≤ 100 total shipped.

Unit meeting
Masking meeting June 22, 1962

About up to date on coordinagraph.

Copy camera work is up to date.

S+R should be on air by monday. We are limited by size to ~1.05" center to center.
Mtn View is redesigning to make a chuck with 6 position only.

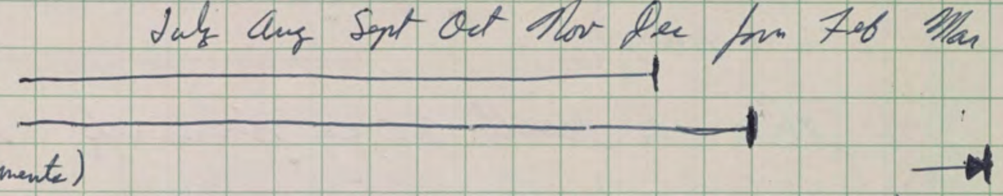
10 position jigging and individual pattern scribing
design about complete
3-4 weeks to get.

July 2, 1962 - Meeting c̄

R. Norman
Bill Scisin
H. Bobb

The schedule was

10 bds each function
R unit dice
R element delivery (50 elements)



Suggested new schedule (on basis of conversation last week c̄ JPF)

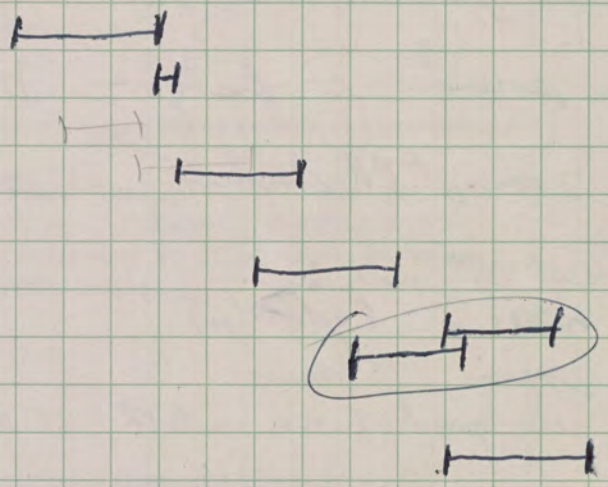
Integrate nors (this would be a new,
eval. nors non-permanent family member)

Integrate 2G2

" G

" R

" A&B



There was a meeting last week including the following to discuss this problem: Noyce, Bay, Graham, Phelps?, Sporck, part incl JPF.

This discussed this problem as a main topic - it was brought about by a ~~discussion~~ request from DPD on 600 R's or eq. by Dec

Questions to get answered:

1. The R - status

2. What is max feasible acceleration?

3. What is quantity vs time possibility?

4. In addition Howard needs quantity prices. These he will get from

Meeting ROBE — Small Meeting 7/3/62

Davis
Hill
Ferguson
Moore

Davis on thickness selection:

0.6 min — (original is ~ 0.3)
1 max

this is with 30 cs viscosity with 6" spinner.

With the thick ~~[illegible]~~ coatings the etch time seems to increase
goes from 15 min to 25 min.

This sounds v. fishy — JPF suggests measure rate vs time meas.

Dev. 2 min KPR developer - still, 15 sec Xylene - agitate looks best for now.

Present 4200 2nd mask:
~33 CS (get ≥ 1μ)
exposure 15 sec
development 2 min in KPR, 30 sec in Xylene → ? TCE degreaser to clean back.

RECEIVED
JUL 19 1962
GORDON E. MOORE

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

July 16, 1962

To: G. Moore D. Yost
P. Ferguson R. Brown
G. Davis D. Kobrin

From: Paul Hill

Subject: Minutes of July 3, 1962 R & D Meeting
on Standardization

The full attendance meeting was rescheduled for July 17, 1962 due to lack of new results since the prior meeting. However, Gordon Moore asked that a short discussion with G. Davis and P. Hill be held anyway to keep him up to date on progress of runs started.

Major Discussion Points

1. Exposure - Development System:

   a. Program has been selected from those previously under consideration.

   b. It is being optimized for specification inclusion.

2. Oxide Etch:

   The use of elevated temperature etch bath is being checked. The advantage to be gained is faster cycling time and less risk of KPR lifting.

3. Criteria for Masking Evaluation:

   The Process Development method of relative pinhole density is acceptable as a count procedure. Electrical counts will be those parameters associated with breakdown and the like, while Beta, softs, punch-through, and the like will not be counted.

General Comments

1. KMER may not necessarily be the answer to metal masking problems (Moore).

2. KMER will be compared, and data from E. Shideler concerning his routine use of it will be reviewed and reported on at the July 17 meeting (Hill).

3. Masking "standardization" may be best handled as one procedure for large geometry best for pinholes, and a second for small geometry resolution (Moore).

4. Resident time or inventory accumulation and effects on pinholes and overall yield reduction was discussed. Current processing times were not known, but 6-7 weeks to die sort were

observed as little as two months ago.

5. Controlled ambient masking (within a drybox system) was discussed. Gordon Moore recommended immediate follow-up on Davis system by purchase of ready built system. This is considered vital engineering follow-up on pinhole yield work done by this group. Process Development is charged with obtaining this type equipment for further development of higher masking yield implementation.

6. Next meeting is scheduled for Tuesday, July 17, 1962 at R & D Plant.

Paul Hill
Process Development

Gordon Davis
Process Development

PH:btc

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR

DIODE PLANT

RECEIVED
JUL 19 1962
GORDON E. MOORE

To R. Brown

From T. Falworth

Subject Test Report on KPR Techniques

Date July 16, 1962

cc J. Berliner
A. Desmond
M. Garfield
✓ G. Moore
P. Hill
L. Punte
T. Roder

Object

To compare turret spinning against flat spinning and etched wafers against polished wafers using:—

[redacted]
1. Normal KPR techniques
2. 2 layers of KPR
3. Enriched KPR (4 to 1)

Procedure

1. Twenty-Four FD-1 wafers were divided into 2 groups of 12 each.

2. Twelve wafers were etched to a thickness of 120 ± 5 µ, and 12 wafers had one side lapped and polished to a thickness of 120 ± 5 µ.

3. Both groups were cleaned and then oxidized in a boron oxidation furnace for one hour @ 1200 °C (4 to 5 hinges of oxide).

4. The wafers were then divided into 3 symmetrical groups of 4 etched and 4 polished wafers.

5. The KPR was applied in the following way.

Group	Method
A	Standard KPR Technique
	2 etched and 2 polished wafers were turret spun " " " " flat spun
B	1 layer of KPR was applied and dried and then another layer of KPR was applied and dried.
	2 etched and 2 polished wafers were turret spun " " " " flat spun
C	One layer of enriched KPR (4 to 1)
	2 etched and 2 polished wafers were turret spun " " " " flat spun

Note: Tests A and B were done using only one KPR bottle.

6. All the wafers were then exposed to light and baked.

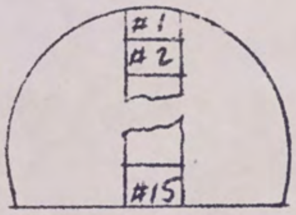
7. All the wafers were then mounted on glass slides using black wax and the fronts etched in oxide etch for 20 minutes.

8. The wafers were then dismounted from the wax, cleaned, rinsed and blown dry.

9. All the wafers were then etched in a chlorine furnace at 900°C.

   Note: The above steps were carried out on the same day using one pair of spinners operated by a production girl. All the remaining steps were carried out by an engineering aide.

10. The wafers were re-examined and the techniques evaluated. The evaluation was carried out as follows:



A central strip in each wafer was divided into 15 1,350μ X 1,350μ squares, and the etched bits in each of these squares were then counted and tabulated.

Results: (Lack of time forbids me to print these results, these may be seen on request.)

Conclusions

1. Irrespective of type of KPR application (3 types tested todate) Mechanically polished wafers have fewer pin holes than etched wafers. In the ratio of 1 to 2 approximately.

2. Irrespective of type of KPR application (3 types tested todate) Turret spun wafers have fewer pin holes than flat spun wafers. In the ratio of 1 to 1.2 approximately.

3. Two KPR layers have less pin holes than the two other KPR techniques which were investigated, that is less pin holes for both etched and polished wafers.

Recommendations

1. With the present evidence at hand, polished wafers should be preferable for KPR work

2. Turret spinners should be further investigated and the spinners mechanically improved.

3. Two layers of KPR techniques should be investigated and various types of KPR tried.

TF: Tw

T. Falworth
Process Engineering

Typical Etch Pits Count.

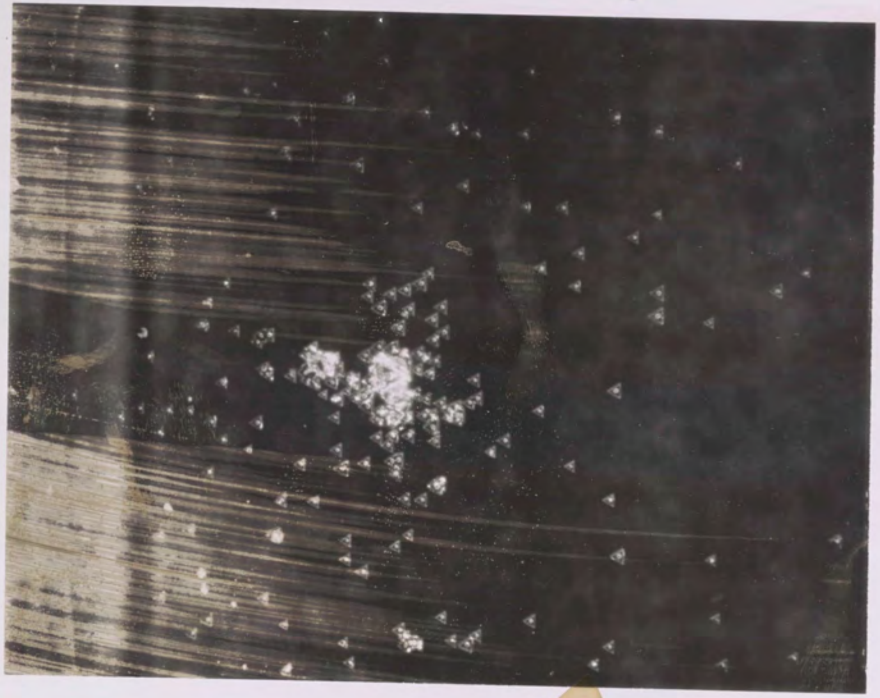
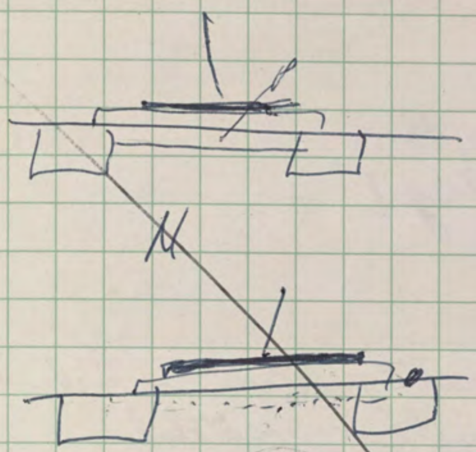
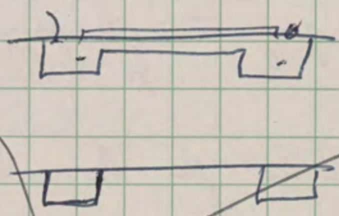


Fig 1

Fig 2

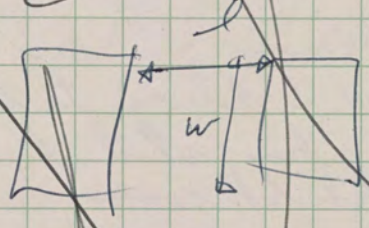
~~PNP~~ -





ρ

100 5 v 1 ma



5000 Ω/□

$R = \rho \frac{l}{w \cdot d}$

5000 Ω = $\rho \cdot$

ρ = 5000 Ω 3×10^{-7}

ρ = 15×10^{-4} 1.5 mΩ-cm

7/5/62 – Sect meeting:

10 position jig – drawings by 14th
Installed by Aug 1

A good 24" lens for Borrodale.

S&R camera – had tape control ~~[illegible]~~ problem – looks ok now.
The Japanese lenses are not adequately matched.

Lenses we have:
20 – Leitz 10x
10 – B&L 10x (delivery to be received)
27 – Japanese from which to select two steps
10 – B&L from old camera.

We need a set of ~0.1 % match.

IBM uses fly's-eye mask.

Permanent masks

Ni-Cr evap. has pinholes – Problem – not under control.

Still trying:

Both Cr & ~~[illegible]~~ Pd have pinholes

7/12/62 Discussion abt. @ Litton

Ferguson
Farina

1. Dif. amp — abt half the usage
uses a 200μf C, ~~looks like the~~
prefer 22.5 v (for standardization)

Must use nichrome resistors.

2. D.C. Driver
Output is 40v peak-to-peak. This is the only having problem.

~~We will try 10v~~

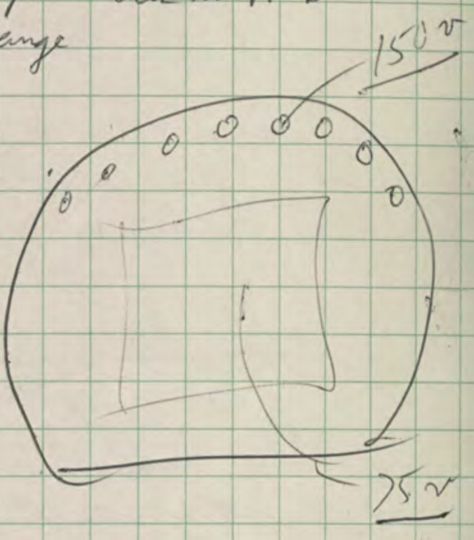
We will take the position that ±10v supplies (20v max swing) is the most we can possibly consider for hardware delivery on their time scale. If they are still interested we will get together with their decision-making technical people to work out details.

July 17, 1962 Small Geometry Product Meeting

Sporck
Grinich
Santos
Shultz
Moore
Sello
Graham
Knudsen

Ferguson
Steidler
Peterson
Noyce
Berg
Bailey
Yost

Start with July 11 memo
Interim decisions
1244 – kill because of material problem – Want remedy for 1210, 1243
1211 – 3 stripes will replace 1210, 1210 out
1321 – ok COC
1324 – out (material) – not even 744 replacement, ~~We could go~~ – Back to R+D
3011 – Make 3010 instead for now. – see anew for change
1250. – Leave device as is, rewrite the spec.
1312 – To R+D – big 3 stripe, 2 emitter structure – To R+D.
1315 – " " " " " " " "
1221 – Yes, but switchback problem.
1224 –
~~U~~ 0001 –
U-1 –
U-2 – > Marketing needs this one.
0002 ?



On 1324 we will select a FT 2368-9 @ LV_{CEO} ~ 10v. We will not make a 2N744 replacement.

We would like to make a 1324 (15v LV_{CEO}), but back to R+D.

Santos says that we have never shot for the 15v LV_{CEO} stuff.

No measurements on NPN concerning the relatively switching performance of the inside-out 3 stripes, 5 stripes, etc.

R+D will take 1324 questions back for answers. What should the geometry be? Is there a material problem? Does the r_b' effect switching times?

If we plugged 50v material in to 1321 Santos thinks that we would make some, but we would loose some on high I sat.

We should do a several month max re-hash of the device in this area. It should meet a 15v LVCEO. The IBM version of the 744 should be considered in the process.

The 3011 was aimed at 35v LV_{CEO} (120-170v diode).

THB suggests run 3010 to get units for 1244. Run epitaxial on top of material available.

The R+D runs ran 0.3v $V_{CE(SAT)}$ @ 500 ma, 30 v LV_{CEO}
Prod " " up to 3v " " 35v LV_{CEO}
(This is a no-gold unit)

We will make 3011, 25v LV_{CEO} min.

[Get the story straight on the following:

1. Sb-doped substrates for epitaxial
2. Program on Sb diffused substrates]

On the 1250 we have 14,000 using no-Ni that have high leakage ready for classification. Several runs using Ni will be thru shortly.

1221 — We made 5000 by mistake (no Au in 1321). ~~The present material used for 1321~~ R+D was going to make dice and supply Kefer now.

We would like to compare TC 1211 & TC 1221.

0001 — TV — Try to make 1210 do the job To early to schedule.

0002 — Spec @ 1 watt @ 500 ma. It is a 1221 (1210) diffusion using 50v BV_{CBO}. Some life-test problems

U-1, U-2: 15 runs in R+D. 10 are U-1. We know ~~that~~ no reason that the U-1's should be low noise.
There are not even 5 db ready.

Perkins
Hale

July 19, 1962 — Project Review — 178 Magnetic films

Review — didn't get as far as we had planned
Have done Ni, Fe; NiFeCo; NiFeCu

Cobalt increases H_k and H_C
Cu " H_C, not H_k

Fe-Ni	min	$H_c \sim 1$,	$H_k \sim 3$
+ Cu		2	7
Co		2	3

We probably want higher, say 7-10 for H_c.
We want higher than other people because we want smaller dots.

My thoughts
We need:
1. Gross cut H_c - H_k flexibility
2. A memory array test vehicle

The present process

1. Clean { MgO rub, $CrO_3 + H_2SO_4$ wash, rinse, acetone
2. Bake in vacuum 30 min (~400°C, c̄ filament heater on, H coils on) and a W-coil to heat to ~40°C to out-gas bell, etc.
3. Cool for 20-30 min
4. Evaporate
    - a) turn on (Substrate @ ~300°, Gun on, H coils on, etc.
    - b) remove shutter
    - c) evap until monitor (resistance) reads properly (2×10^{-5} — 2×10^{-6} mm Hg)
    - d) close shutter
5. Anneal at T of evaporation, variable t & T.
6. Open at 100°C.

The mask making capability is inadequate for the memory planes we need.

This looks like a one-man full load in the shop for 6 Mo.

Chem. expenses out of control
Drafting on the ultrahigh vacuum overboard.

We are short on electronic instrumentation.

COMPANY PRIVATE

July 19, 1962

PROJECT PLAN 178

MAGNETIC FILM STUDIES

A. P. Hale

I. OBJECTIVES:

A. Best practical method and procedure for magnetic film deposition

B. Most efficient geometry for thin magnetic film memory elements

C. Memory elements compatible with microelectronic elements

D. High Speed Memory

E. Understanding ferromagnetic material.

II. PLAN FOR LAST SIX MONTHS OF 1962 TOWARDS OBJECTIVE A

A. Evaporation of films with main emphasis on tighter control of process to maintain uniformity.

1. Annealing
2. Cleaning
3. Masking by mechanical and etching techniques

B. Electrodeposition

C. Vapor Deposition (if time permits)

TOWARDS OBJECTIVES B AND D

A. Memory planes as per Harley Perkins' plan(s).

1. Evaporated ground plane, dielectric, permalloy, dielectric, 1st conductor.
2. Mylar or like and conductor by evaporation or electrodeposition. (Indefinite at this point)

TOWARDS OBJECTIVE C

A. Small array on wafers. Evaluation for uniformity as well as other parameters.

B. Start on integration if time permits

TOWARDS OBJECTIVE E

A. Domain Observation

1. Bitter's technique
2. Kerr magneto-optical method
3. Hall μprobe mapping (maybe, if time permits)

B. Stress and strain measurements

1. Magnetic films
2. Dielectric and metals if time permits

C. Electron microscopy of magnetic films

D. Study of fundamentals (to include magnetometer - do we need it)

III. PERSONNEL

A. Hale		85%	
P. Ferguson		100%	
H. Yee		100%	
			~ 3,000 hrs.
Other	1. Analysis		150
	2. Shop (Mostly for service)		500
	3. Masks, etc.		300
	4. Electron microscopy		300
			1,250 hrs.
		TOTAL	4,250 hrs.

IV. EQUIPMENT

A. Ultra low pressure system in construction	$ 5,300
B. Kerr magneto-optical instruments	2,500
C. Hall μprobe (?)	2,000
D. Vacuum System (Vactite, ordered)	8,000
	$17,800

Both vac. service
already ordered.

APH:jt
7-19-62

July 19, 1962 – Epitaxial layout

Sah
Wrighton
Rodes

I. Evaluation of uniformity of given run of ~ 30 wafers
  a) diode breakdown,
  b) thickness variation
  c) impurity profile – Ga method, capacity
  d) starting ρ of each substrate

II layer: n on n^+, 5μ, 0.5Ω-cm.

III

Cont on July 20, 1962

1. Eqpt: Prober, mask, Ga furnace, etc. — ok

We must check out our tools – but this should be done with good material
  1. Measure profile of one wafer by Ga & C comparison.
    Schedule:
      Run of undoped silane on regular substrates.
      Ga furnace going

July 20, 1962 — μ cktry product planning

Schultz
Grinich
Ferguson
Plough
Phelps
Shands
(Seeds)

Gault
Farina
Graham
Bay
Sporck
Moore

Phelps summary report:

μL-1 — looks like some volume is developing

It looks like appreciable volume is developing. If any of the big stuff we expect comes in, we get swamped.

Looking for 5K sales of μL and
5K " on kit / week in Sept. 20 total sales in Dec.

Yields look like A >50%
B most of rest. at the Dec level.

The die yield on S is ~10%.

The KR + KD elements have as many leads as regular μL elements.

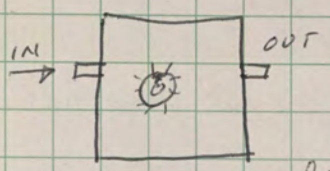
Charlie Plough thinks we will run 75% μL elements to (A+B) Specs

July 23, 1962 μ wave

Guthrie
Solt
Ginzl
Moore

Most promising to date is harmonic generation:

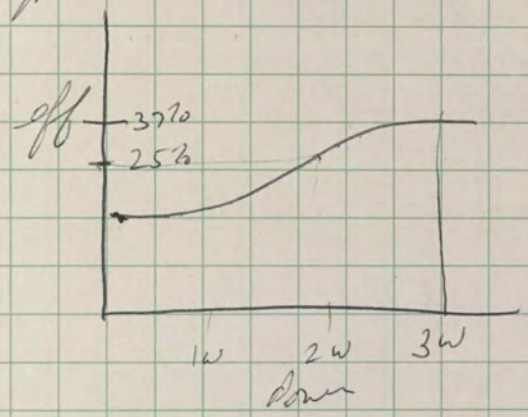
Can consider a box



a frequency multiplier box, single knob tuning

This is a not presently available black box – because it is broad band.
Present S of A is a few %

For a "typical" case in lab tripling 1 → 3 KMC



We are nominally a ~~month~~ month from knowing where we sit.

Mfg needs quality mechanical production – mostly machining

Discussion c̄ Kabell + Smith abt Inst. type products July 23, 1962

Big Inst

1. DVM (In Mfg)
2. Densitometer I.S.
3. FET VM R.P.D.
4. Ramp generator RPD
5. EDM RPD
6. Lab decade amp RPD
7. Sweep frequency generator RPD
8. μ tape system IS
9. ESP IS
10.

Small package

1. Const current source RTF
2. V-2 Op. amp RTF
3. 0-drift differential amp. RTF
4. Differential to Single Ended RPD
5. D.C. → D.C. Transformer IS
6. Voltage to current converter RPD
7. RC active filters, LBP IS
8. Std cell replacement RPD.
9. Temp. Xducer RTF
10. Log amp (needs thermistor) RPD

Other

1. Pressure Xducer family IS
2. Optical displacement Xducer RPD

Legend:
RTF - ready to file
RPD - " for product development
I.S. - Investigative stage
N.B. - Needs breakthrough

In addition we should consider μ wave stuff.
~~other transistor production equipment.~~

BIG MACHINES

1. DVM (+ accessories)
2. Ramp Generator (Function Generator)
3. Lab Decode Amplifier
4. Sweap Frequency Generator (Low Frequency)

SMALL PACKAGES

1. Constant Current Source
2. V-2 Op. Amplifier
3. O-Shift Differential Amplifier
4. Dif. → Single Ended
5. Voltage → Current Converter
6. Std. Cell Replacement
7. Log Amplifier (Crystal Oven)

Inst. Mtng - Review July 23, 1962

Martin Russell
Hubbell Moss
Speck —
Swindle Moore
Bay Storey
Magid

Their products:

	Sales $ ea.	J-D 62	J-D 63	Shipped to date outside FSC	
Model 10 - LV $_{CE}$ 0, A, S tester	2K	2	12	1	
Model 20 - Low leakage 1μμa → 10μa	2K	11	12	3	
" " , wide range 1μμa - 10ma	3K	0	30	0	
Model 50 - h_{FE} pulsed to 1 amp	5K	32	48	8	→ but ~10% profit.
50a - to 10 amp (probably about 15K)					
Series 100 - Diode tester	38.5	0	6	0	short feeder
300 - Xstr & diode bias logic	25K		16		
200 - Auto Xstor (24 parameter)	38.5		6	1	
Series 500 - Readout Xstor tester (with data log)	33-39K	6	9	0	1 complete, 2 half complete
Series 900 - Punch card & Data log					

Sales prices are generated as follows:

1. Unit forecast to get $ mfg cost.

We will do a job to crank out V-2 op amps and 0-drift diff amps.

Ed will cooperate on the packaging.

In 6 weeks we will have 1st 10 ea. of these - ie, by the middle of Sept.

July 23, 1962 ROBB

Davis
Hill
Yost
Moore

Implentation of masking is in the mill. Will be in in three weeks.

It is shown that polished wafers have fewer KPR pinholes. Paul Hill is strongly in favor of going to polished wafers

KOR should be considered – this is a new high speed, visible light sensitive material.

In the new KPR room in Mtn View there is a completely enclosed line!

'Why doesn't Hill know this?

July 25, 1962   San Rafael

Grinich
Bay
Ready
Brown
Ferguson

Sporck
Graham
Beadling
Duvall

Review of diode products:

FD-1   ~~75,000~~ 50,000 seals/day   10.8¢ prime   50-50 (l & m)

Some indication of forward drift on life for weeks 22-25. Up to 1.5% failure rate. This is new. It had disappeared after last Oct. Problem seems to be in assembly.

Run 85% FD-100 yield seal to classification.

The visual yield after classification makes 40% of these industrial.

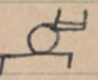
A fair % of the 15% shrinkage makes 30v — ∴ 94% overall.

94% yield to valued inventory.

The visual sort after classification is on the basis of 20 criteria. It finds some (but a small %) of units that we know are reliability problems — (ie, Sn over Au ball).

[The visual inspection is 500/hr, ∴ $\frac{\overset{5000}{\cancel{75,000}}}{500\ 7.5}$ = 10 girls]

The "catastrophic criteria" are:

1) Sn over 0.9 of ball (Must see Au all the way around)
2) Cracked dice (obvious ones)
3) Washer not on top of ball 
4) Cracked glass, gross, not striations

Actually this is not a 100% inspection, but when Q.C. rejects a lot it is 100%ed. This runs to 70-80% of lots.

I-D-1, cont

⊙ Prime cost data

	Proj for end/sq Labor	Material	Σ	Present. Mat	Labor
After dicing	~~1.6~~ 0.16	2.1	2.26	0.	
After seal	1.65	4.19	5.84	4.04	1.8
After classif'n	2.05	4.51	6.56		
At end	3.91	5.10	9.01	5.2	5.6
				10.8	

With the present package we cannot see a major improvement over this 9¢ figure.

Package parts:	1st seal	1.462
	whisker lead	1.495
	preform	.385
	gold ball	.180
		3.522

.575
.2
1.150

On the ADAM the material looks like ~~3.5-4.0¢~~, ~2.5¢

Studs (2)	.575	=	1.15
Glass	0.215		.215
leads (2)	@ .301	=	.602
			1.957 – right now

The prime cost forecast for end of Dec is 11.3¢

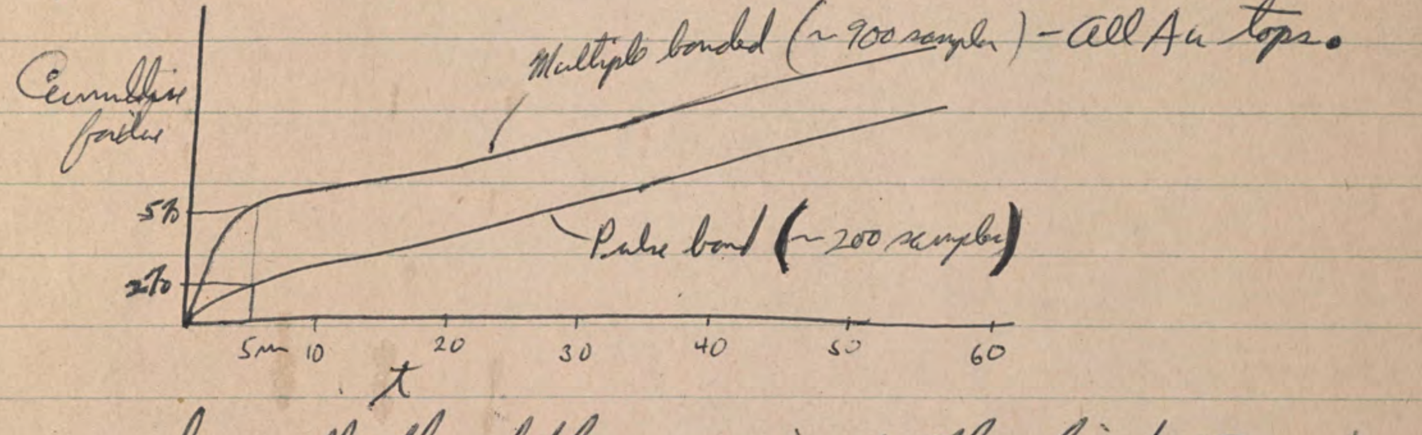
-2

Running at ~5,000/day seals
Prime cost runs 15-16¢. Difference is yield.
yield runs ~50% FD-200.
drop for leakage > μa ; BV < 200v.
~80% is salable (vs 94% for the FD-1)

There is a problem with drift of final leakage ~~drift~~ with time that makes lo quality of lots unpredictable. This problem has been with us ~~forever~~ always.

No data on tc bonded units or on ADAM units. Most of these failures came out @ 250 hours of soak at °C.

Data was presented to show that Multiple bond on Au is ~~better than~~ worse than pulse bond for first 5 min in paint shaker



Ie, all the difference is in the first 5 mins.
* No data was produced on Au balls on Al, single dot.
Hearsay says Multiple better than single on FD-6.
* Data on FD-6 shows show 750% failed of both multiple and single in shaker. BUT all for IR, not for balls off.

Ray has preliminary data on ADAM-type die in std. package. "It looks good". Problems with large-scale test are:

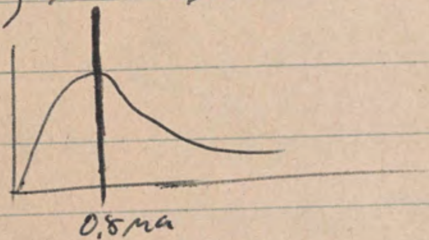
1. Need higher T solder
2. Must center on die rather than on ball.

THIS LOOKS TO ME LIKE A PRODUCTIVE PLACE TO EXPEND ENGINEERING.

FD-3

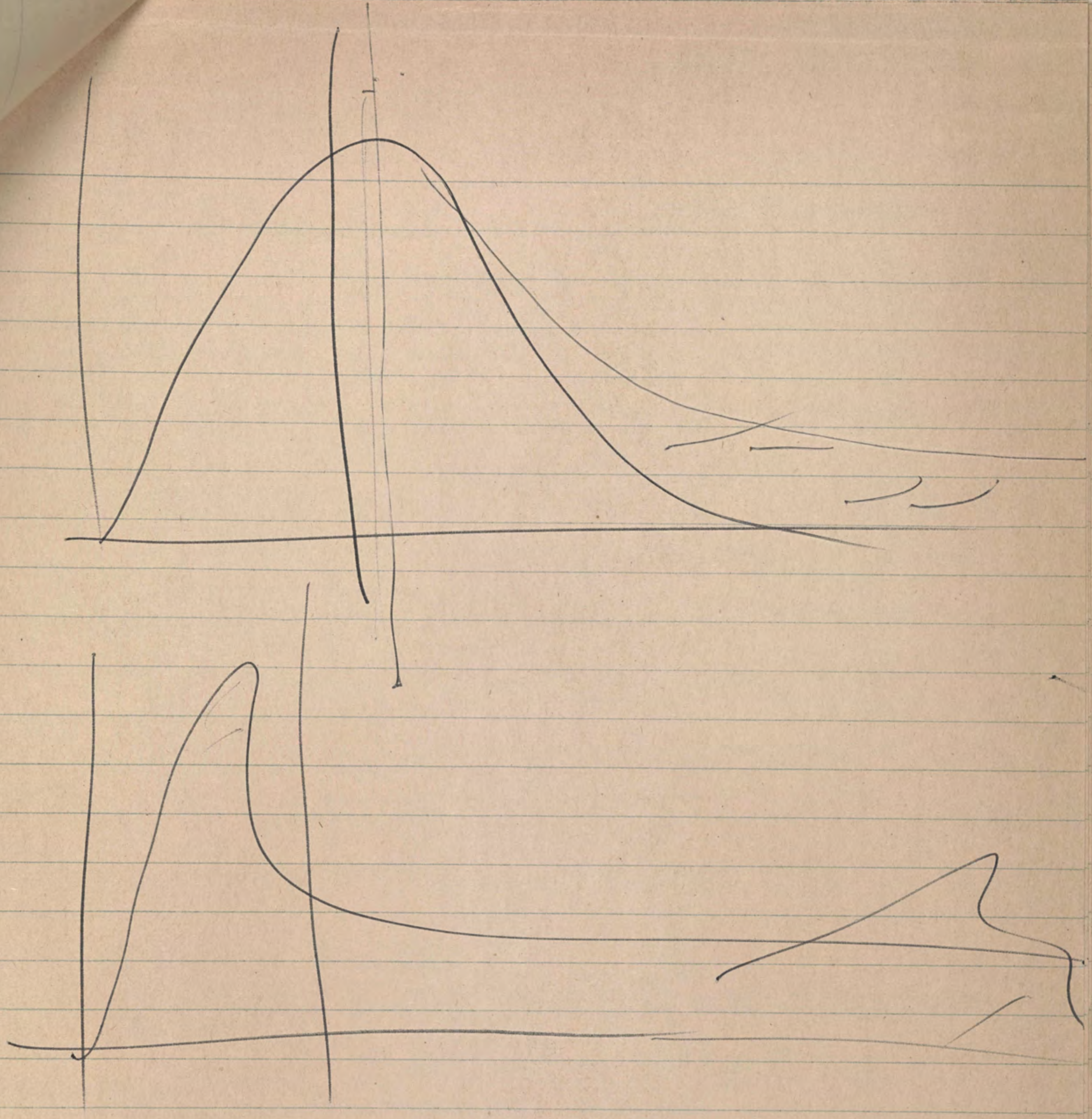
Inconsistent on low leakage
30% to FD-300 (2% – 85%)

This looks like too tight a spec for the distribution, not like a high maverick incidence.



We are diddled on our own spec. at t=0
They also degrade badly, say 15%/1000 hours.

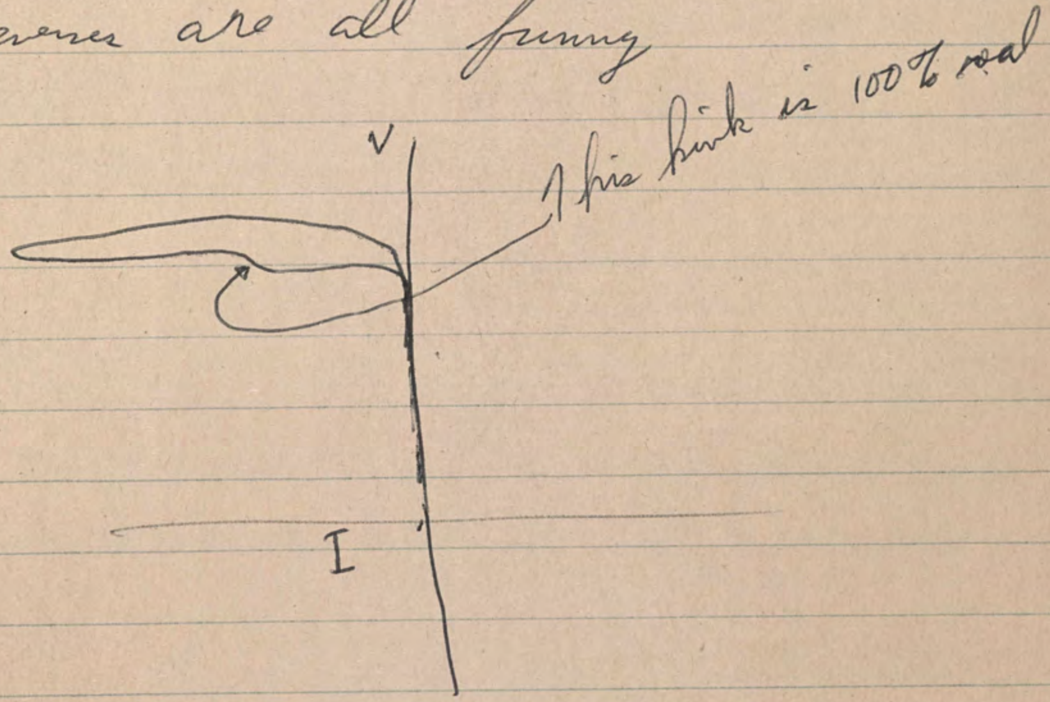
We have never run many TC's (or ADAMS)



FD-6

The I_R degrades
a) on paint shaker
b) on operating life (> eq. temp storage)

The reverses are all funny



Run 45% salable yield. Run 20% to FD-600.
Loose on low BV. C min ~ 1.5pf. -ok
Low forward
High leakage

Thought to be a material problem.

FD-6, con't

They now groove 100% of wafers, but are trying to get down to a sample. Wafers are sorted to thickness ranges and the diffusion is adjusted appropriately.

Die sort sure sounds like the way to fly!
This will be tried on the plate after ball bonding – a time where the reverse characteristic only can be checked.

There are IR degradation problems. << FD-3, say 1-2%.

John Ready would like "word garbage" about the lousy reverse characteristics.

On this device it looks like burn-in (power) perform a real screening. – Hearsay from Q.C. thru Brown.

FD-7 - Shut down

Problems: BV, Forwd, Z_K, C

Material is running in the lab on the process variables.

1. Dif. time
2. Au from the top

San Rafael has run good material - a long time ago.

If after the next runs come through the problems are still up in the air, then we will consider firing up again and supplying wafers.

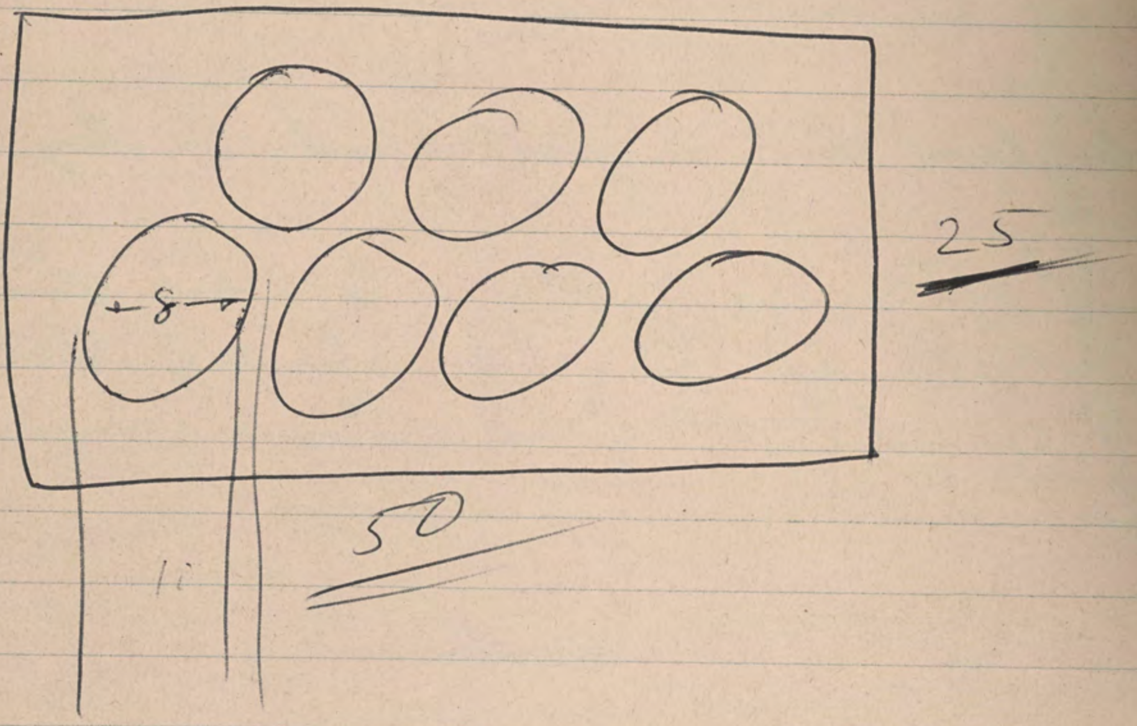
FZ-1 Ready to sample.

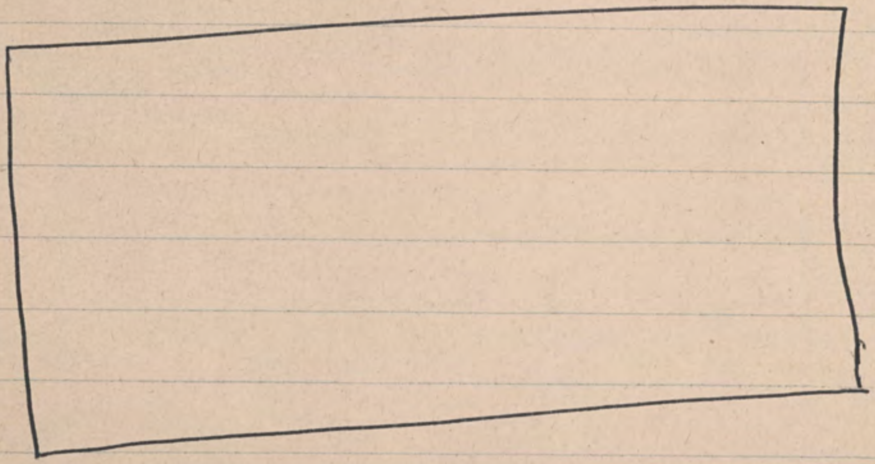
60% < .005
40% < .001 ~~[illegible]~~ 25°-125°

FZ-2

Aim at dice 15 Aug
Chop off Nov 1

G.P. Zener Dice early ~~Sept~~ Nov 1, End cut on Jan 1


8
25
50



SCR – 3 - Problem is getting 400 v in both directions. Prices ready, everything else is ok.
Uses 5 mil Au ball bond.

Spork suggests making part of power xstor group.

Samples meeting everything next Month.
JPF is aiming for Oct – this is overly optimistic in my opinion.

Sandia - they pay fantastic prices for large quantities – say $5 ea @ 125,00/MO.

We will make a quick cut through to try to give them units to look at.

XP-3
~~FD-3~~ - Samples to THB
Life test must be done
Find out units by Oct.

July 31, 1962 — Section Meeting

Fok
Van Ness
Blume
Engell
Santer

The new S&R ~~pl~~ camera chuck doesn't work well yet — needs rework.

Except for this its ok.
Still must focus individual.

Scribing, etc, to get to glass — 12 hrs

Copy ~~camera~~ camera —— 2 hrs — involves several copy steps

S&R camera — prep to step (10) —— 4 hrs

Stepping time —— (4 hrs @ 25 mil)

S&R — then finished master —— ~~12 hrs~~ 1 hr

Submaster from master —— 12 hrs or so

+ Working plate —— 4-6 hrs

Alignment check — To be eliminated — ~~[illegible]~~ (Now takes 1 day)

Working plates —— 8 hrs (~100 plates)

Waxing, etc. —— 8 hrs (~100 plates)

~ 60 hrs/set.

Santer & Fok will get 1st order std estimates by next week.

KPR area:

Dust free hood is installed

Mechanical mask alignment should be done in ~ 4 hrs.

We are looking at new materials such as PVOH and $K_2Cr_2O_7$ for resist.

Or What are criteria for comparing results

< Definition
Adhesion
~~[illegible]~~ Cut
Stripping
< Pin holes (visual)

Lets put together a program plan — Art by next time

Permanent masks:

Got good definition on Cr - but some undercutting.

Cr is only thing to date.

Nichrome resistors

[illegible]
Ferguson
Tripp
Campbell
Talbert

Waits
Moore
Sah

Reproducibility: (1 mil or 2 mil width)

75% ± 5% of mean

90% ± 10%

There were ~ 7K resistors, 1 mil stripes

There is some etch-out problem on 1 mil space between 1 mil and 2 mil. patterns.

All resistors the same width in mils. - 1 mil lines 42 mil

One should consider to use of original masters.

Aim at 150 Ω/□. - best compromise between etching and stability.

Accd to Tripp, we should avoid Au on the Nichrome.

Al wire contacts look "fine." - Data seen - 300° gave 2%/1 khr

Au don't look so good. - It sure doesn't @ 300°C!

We can use existing R-C network masks to make immediate reliability ~~tests~~.

We will immediately crank in several runs of resistors to make units with existing masks. These will be life-tested
a) at 300°C storage
b) @ 200°C "
c) on power age

They will represent both Au & Al bonds

Meeting 8/1/62 — μL failure discussion

Alport
Bergh
Vogel
Cone
Smith
Ferguson
Moore

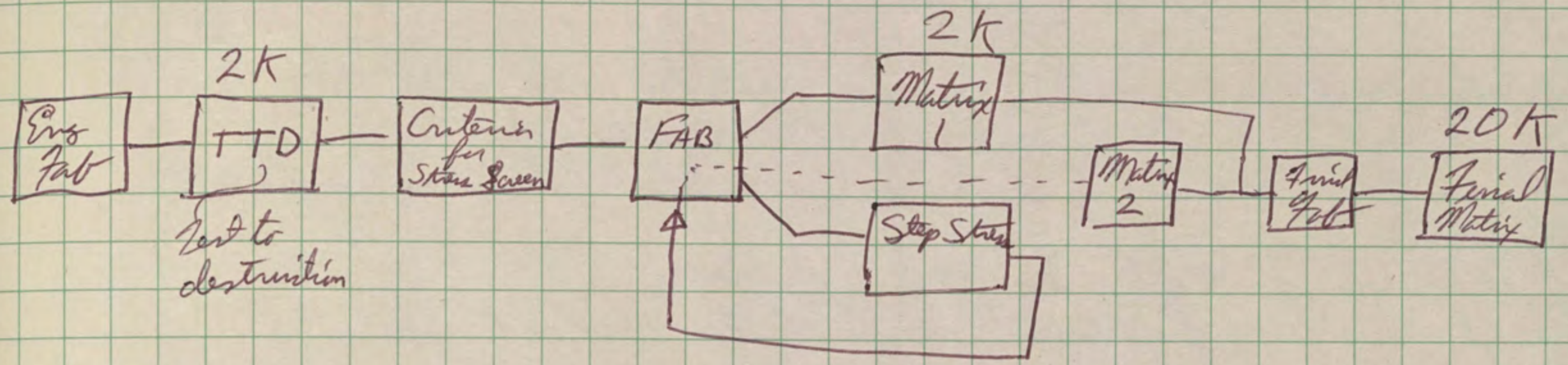
1. AC Spark have seen ~ 10 early failures

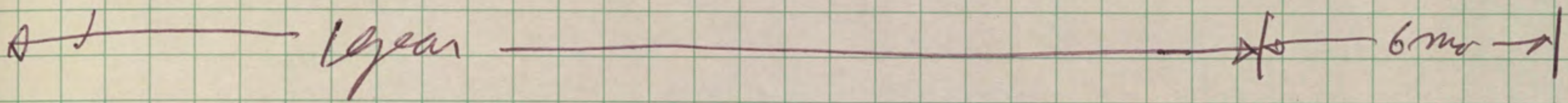
2. On our life tests of ~~failure~~ scratched units:

No failures out of 5 in 4500 hrs @ 150°C
" " " " 16 " 4000 " @ 150°C

~~58~~
1 failed 23 in 4000 hrs @ 300°C at the 4000 hrs reading

Autonetics – from VHG





The first year on all circuits. The rest for a single representative block from each family.

14 from computer & data processing

4 from inertial navigation

~~Jn~~ Aug 1, 1962 — Epitaxial ~~Wafer~~ Project

Wigton
Sah
Roder
Moore

Evaluation tech:

A Ga furnace is being set up @ 1250°C. First wafers into furnace tomorrow morning.

Run 1-307 of epitaxial material $\bar{c}$ recorded substrates.

The following will be measured

1. ρ substrate (center of each wafer)
1a) ρ gradient across wafers known to below measurable
2. V_B on layer by B emitter predep on 1 wafer of each row, ½ masked and measured. This was a std. evaluation.

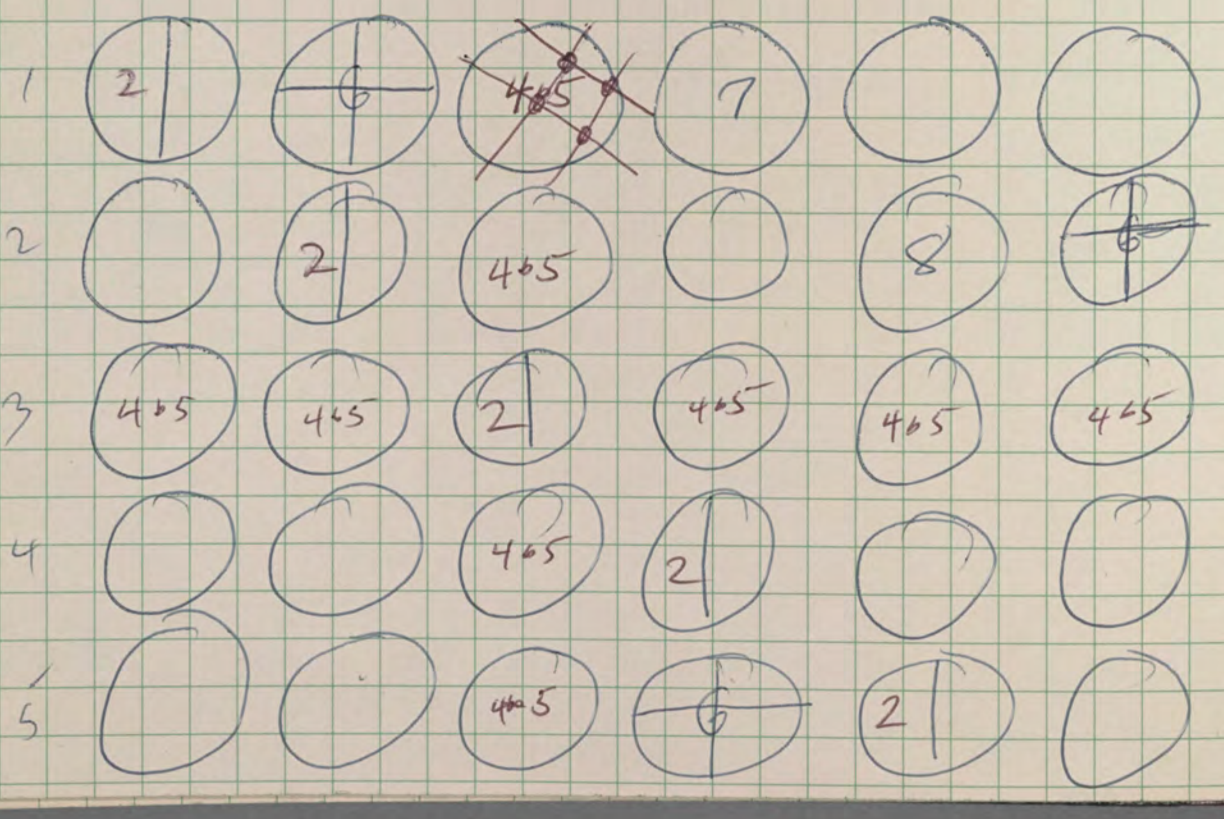
3. One measure on ~~each one wafer~~ each wafer by IR for $t_f^{(IR)}$. Most of these were by "fast scan" which has time const problem.
~~4~~. Only 2 were done on "slow scan".
4. Groove and stain two parallel stripes for t_f (stain).

5. Ga profile at 4 pts/wafer — by photo $\bar{c}$

6. Meas of substrate difference by pre-cook in Ga furnace

7. Uniformity across wafer by multi groove 1 on rows 1, 2, 3, 4 & 1a (not 1) on row 5
8. Stacking fault depth meas.

We will have this: — ~~1 and~~ 3 on each, center
4 & 5 one at 4 points



Epitaxial, cont.

Pyramids - Can photograph orange peel by vert. ill.

For a horizontal we are getting a quartz-enclosed graphite for use c̄ a r.f. furnace. We are using the 10 KW, dual unit for this.

Next meeting is Wed @ 2:00 next week. Aug 8.

Autonetics discussion: @ Aug 1, 1962

Grinich
Ferguson

Analysis of the problems:

Within our ability?

Ckt 1: 20K ± 12% resistor is worst. 12 leads ^ — looks fairly good — ok
10 diodes in 2 region 1 Xstor for ~ 102 points
28KΩ in 3 pieces

Ckt 2: no real problems, possibly 0.5v @ 14 ma @ 85°C — ok
~ 60 points

Ckt 3: Total R = 102 KΩ in 12 pieces 126
8 diodes in 6 isolated regions 30
11 leads 44
4 C's, total 420 pf @ 3v ?
2 T's. 10
210 + the capacitors

Ckt 4: 66 K in 6 pieces 78
7 leads 28
120 pf in 2 regions
2 Xstors 10
116 + the capacitors

Ckt 5: 26 K in 2 30
9 diodes in 2 areas 15
1 Big, fat Xstor 20
11 leads 44
109 — ok

Ckt 6: ~~58~~ 67 K in 10 ~~76~~ 87
5T 25
1ZD (7v) 5
5D in 4 regions 20
10 leads 40
~~166~~
177

Autonetics, cont

Cht 7:

176 KΩ in 14 pieces = 204
5 NPN's = 25
1 PNP
1 ZD (18v) = 15
100pf in 3 pieces
6 leads = 24
268 + C + PNP

Also problem of 27 volts

Cht 8:

22KΩ in 2 pieces
2-1613 Xstor
1-1132 Xstor
1-1N659 diode
1-220pf C

Cht 9:

6KΩ in 2 pieces = 10
1 Xstor 5
15 points
4 leads 16
31 points

This sees a ~~that~~ max voltage difference of 15v.

ok

Cht 10

16KΩ ~~in~~ 4 pieces 24
1 NPN 5
1 PNP
5 D in 3 regions 15
7 leads 28
72 + PNP

Cht 11

18KΩ in 6 pieces 30
1 NPN 5
1 PNP
1 D 5
7 leads 28
68 + PNP

Automation, cont, Aug 1, 1962

Ckt 12

16K in 4 pieces	24
1NPN	5
1PNP	
5D in 3	15
7 leads	28
	72 + PNP

Ckt 13

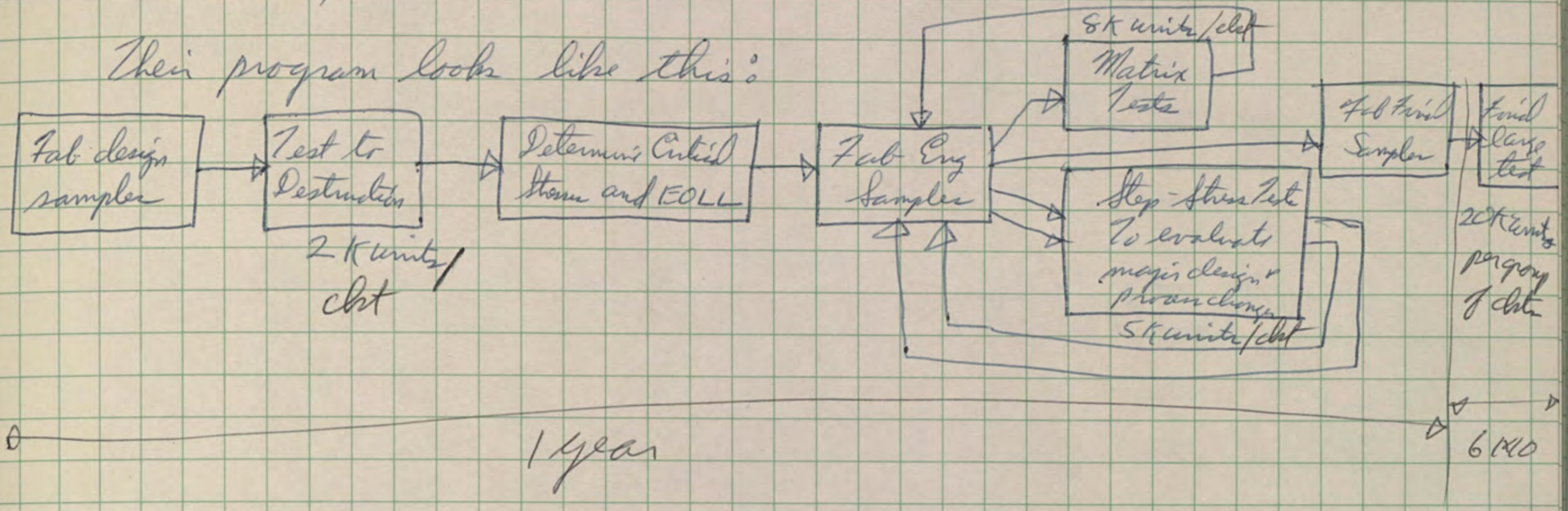
est 17 KΩ in 4 pieces	25
1NPN	5
1PNP (can be v. low β)	
3D in 2 regions	10
5 leads	20
	60 + PNP

Summary

Ckt	Points	PNP	C	V problem	Status
1	102		0		ok
2	60		0		ok
3	210		4 @ 420 pf		probably not
4	116		2 @ 120 pf		?
5	109		0		ok
6	177		0		probably
7	268	yes	3 @ 100 pf	27 volts nec	NO!!
8	Ckt to change				
9	31		0		ok
10	72	yes	0		?
11	68	yes	0		?
12	72	yes	0		?
13	60	yes	0		?

Autonetics, cont.

Their program looks like this:



XP-3 Aug 2, 1962

Kafell
Grinich
Moore

1. We have not really gotten in contact c̄ IBM
2. The assembly is a 98% yield type operation
3. The assembly labor input is presently high — ~60 units per hour.
   Jack sees only a 2-fold increase.

The new structure c̄ the extra diffusion mask is still needed.

An interesting defect that appears to be do to poor NaOH removal after metal etch was tracked down. This device is the most sensitive we make.

An attempt to get thru c̄ only the a heavier base diffusion is in the mill.

The darlington structure is pretty slow — but solid @ 2KC

Jacks cost estimates:

sq. pkg

this goes up for a match stick package

Die	8¢	M&L
	M	L
leads	1	4
Molds	.1	2
Epoxy pot	.15	
Test (98%)		.5

8¢ pf
\+ 1.15 M
6.5 L

What is our life test program?

Condition: 100°C in high humidity with operating light.

A program will be laid out.

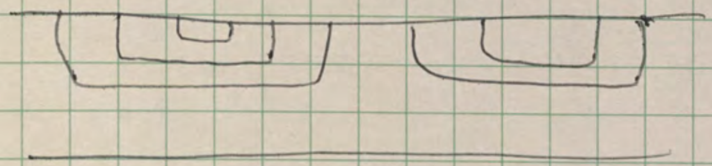
We will give 10 samples to IBM San Jose. (Square only.)

Meeting Aug 6, 1962 — NPN + PNP

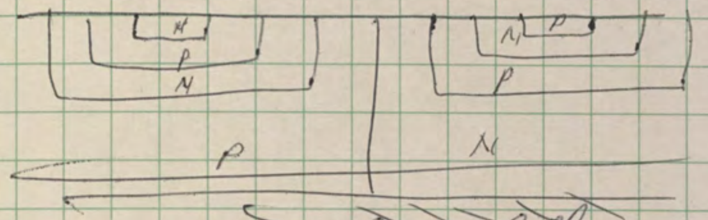
Farina
Ferguson.
Carlson
Triggs

Porter
Grinich
Moore

1. T.I.

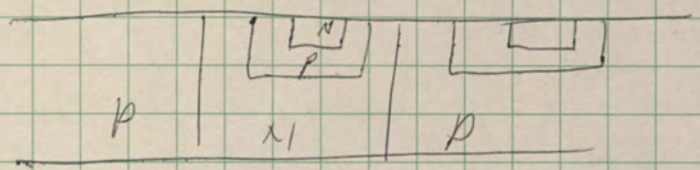


2.

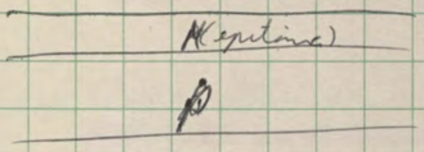


glass bottom (oil, no slant

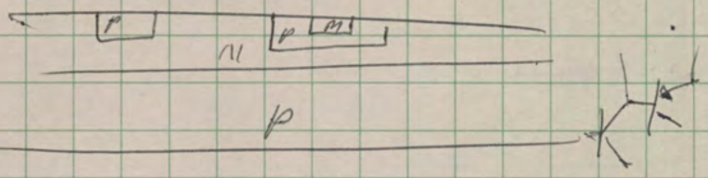
3.



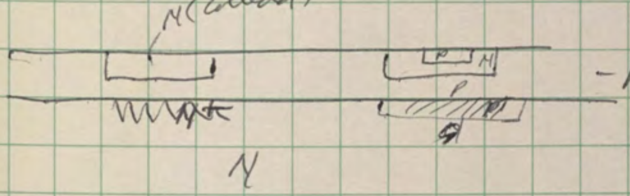
4. We have made (TI-epitaxial)



diffuse



5.



-P-epitaxial

Spinel
Fergum
Farina

Aug 6, 1962 — Autonetics TFX job. (1700 fighters)

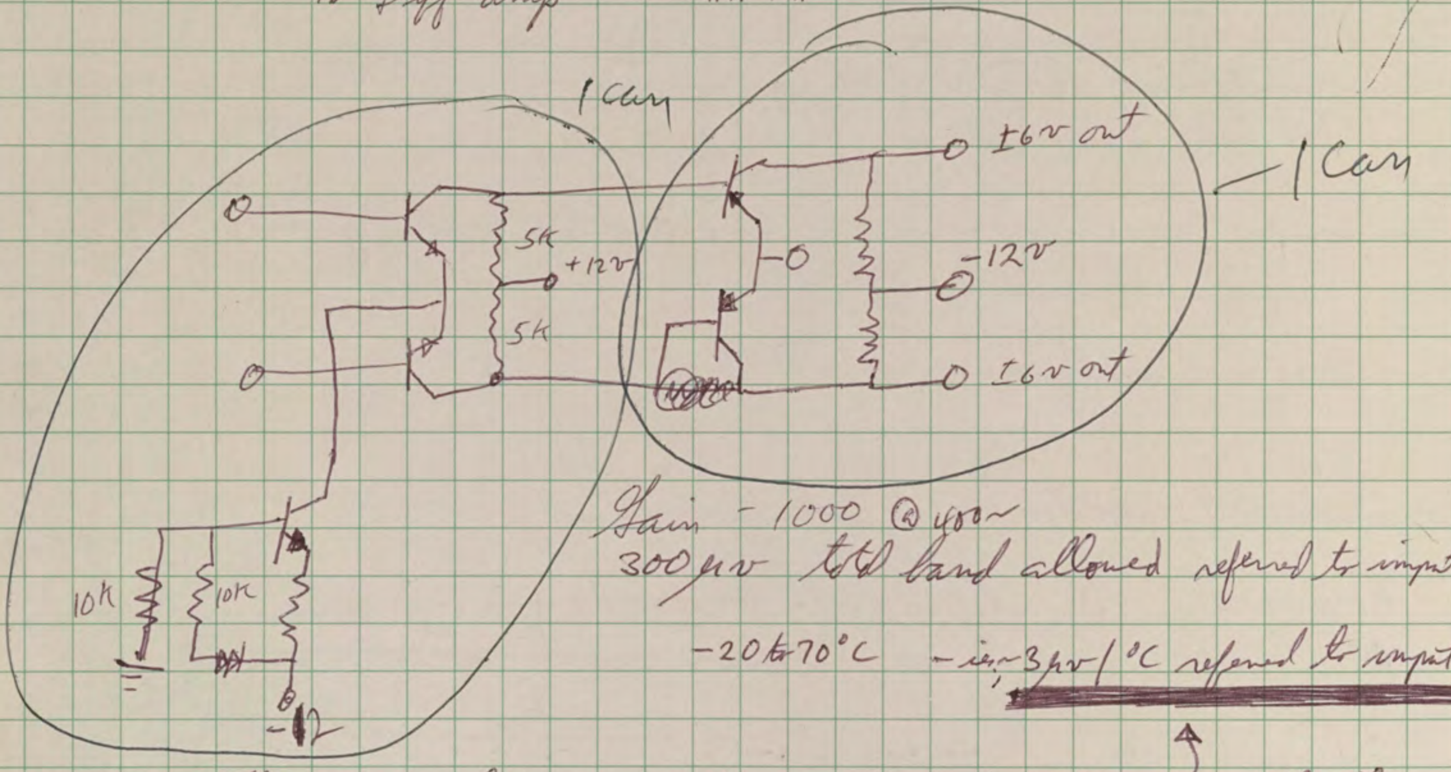
From Farina trip to Autonetics last Sat.

Needs parts in June, 1963. (first evaluation samples)
prototype to be delivered by them in Dec '63.
Autonetics expects contract in Dec, 1962.

Production after June '64 is estimated at 2,000 differential amp per week.

They will send up ckts — 3 or 4. They want price & delivery including a recommendation re: approach.

1. Diff amp — NPN-PNP

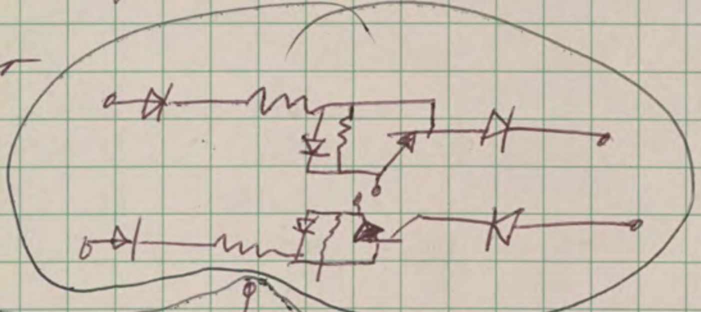


Gain - 1000 @ 400~
300 µv total band allowed referred to input

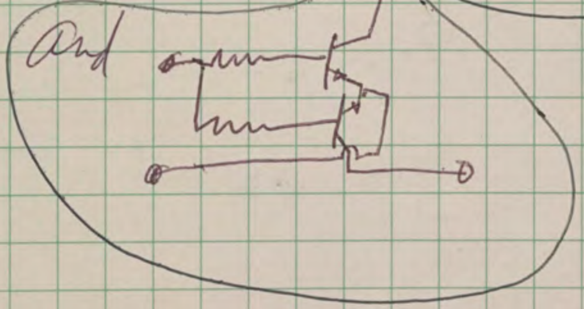
-20 to 70°C - i.e., 3µv/°C referred to input

VHG says that we will never make this → with this ckt.

Also

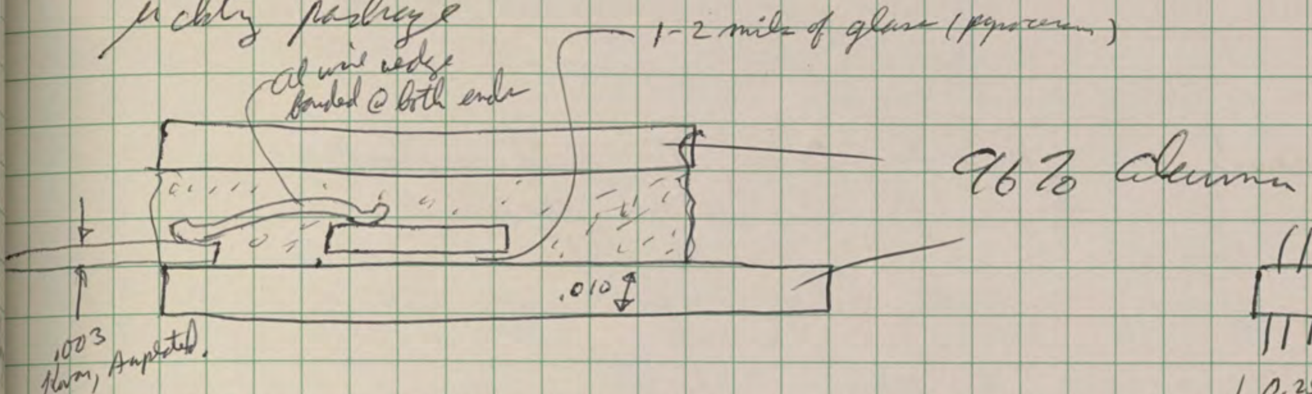


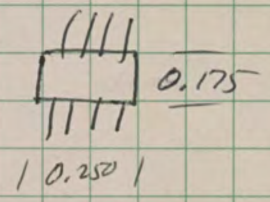
And



Project Review – Packaging   Aug 7, 1962

Ferguson
Haenichen
Waring
Darnell
Saddick
Brown





Reliability data – good gates

100 hrs
300°C – 5 units
200°C – 5
125°C – 5

Operating rig @ 125°C ambient – 11 units

Thermal shocks 3 shocks, 3 units −65°C to +150°C
(dry ice, acetone) (hot oil)

R_{TH} 200°C/watt (free air
130°C/watt (?) in a heat sink.

Once we get the devices in and get it checked, we have not lost a lead.

We have put ~150 gates together finished. We loose 20-50% on very thin ones.
We loose ~10% ($\frac{4}{40}$) on the thicker ones.

There is a socket problem.

We are all concerned about the Al lead bonds. No one has yet tried to do the Au lead bond over the oxide. They have a ceramic with backside contact possibility, so (except for solderdown) one could try the Au with the present gate.

If we go to the TI size, we are limited to a 65 mil dimension.

JPF — As we now sit, we have a brute-force technique to make packages. Phil thinks we shouldn't put this into the factory unless we are pushed.

VHG says we are presently being pushed.

Package, cont

What reliability testing must be done before we are happy?

Step stress:

1. Thermal shock. Stress: ΔT, T_L held constant
Indicator: a) Post stress electrical
b) Radiflo (?)
c)

Independent variable: number of cycles

2. T, t

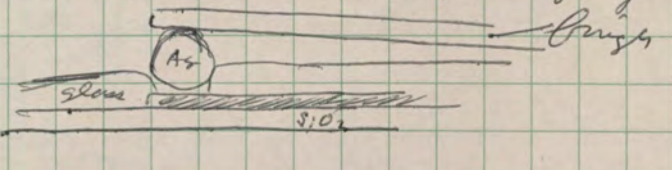
Necessary to put into plant.

Etch preforms
Plating
Hot stage - any modification of die attach
Lead bond - std Al wedge bond c̄ different anvil.
Ceramic glazing. (mass air link)
Test fixtures.

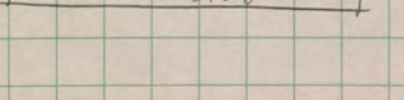
Special products is starting to pick up the technology.

Assembly techniques which eliminate lead bonds:

1. Contoured leads over die
Glaze over die. (low temp)
Open holes over contacts
Apply Ag balls (Or Au) on Al metallization or Ag on Al. 2000Å on 3000Å
Bond or solder Au plated fingers to balls.



2. or ~~replace~~ replace the Ag ball with a metal film spot by KPR mask

 or an alloy and wipe-off technique.

3. Make the bump by plated pads.
make thin ~~Al. film~~ Al – Ag film
~~Make KPR film c̄ holes~~ Actually it need double KMER.
Plate thick buttons of Ag(?)

(The plating is a good way to find pinholes in the resist film)

Any of the upsidedown ideas are still much further away.

For this we have the ability to put ½ - 2 mil films of glass on the wafer.

I want to reconvene this meeting with the follow.

ROBE - Aug. 7, 1962

Hill Bloom
Fok Engsall
Compton Moore

Hill rundown on implementation:

The 4200 is moving into the doughnut tomorrow. They want to change to the new one.

Paul has been monitoring pinholes on the present existing process. He has been looking at the new one in his line

Looking at 45 mil squares (10 at random). Often get >>100, some as low as 15 (with present process). Run from 10-60 in new process.

This is the film only. It neglects other problems, for example the surface and the environment.

Experiment made to look at mask deterioration in 50 wafer jumps. No detectable deterioration to 300 wafers at least by enlarger.

Paul Hill will send me
a) the data on pinhole count
b) His summary on ~~problem causes~~ defects and their causes.

Mtn View is separating B & P diffusion.
Peterson is starting to supply oxidized wafers.

Diffusion:
pl uses all methyl borate
4500 emitter to " "

Probably Methyl borate with BBr_3 backup.

For the n-type, there is a trend toward the use of Methyl phosphate with P_2O_5 backup. No consideration to $POCl_3$ because it was thrown out a long time ago on early Process Eng. data.

Hill will take a look at pinholes in KMER vs KPR in the same thickness.

Art Engvall points out that a mono-chromatic light source is useful for inspecting the wafers.

Sam on "permanent masks".

We have made some 4200 masks in Cr. They look good. These aren't ~~not~~ scratched by my knife.

Schedule another meeting in 3 weeks. At that time we should look at the diffusion plans.

Section Meeting Aug 8, 1962

Fok
Engvall
Van Ness
Blome
Hunter

— Time estimates will be ready by next section meeting. - Hunter & Fok

The new S&R is essentially out of service. We are using the old camera. The guy will be out next week.

Engvall on his program:

Problem ~~Metal need masks for permanent masks~~

— 1. Permanent masks
    1. Etched metal films

— 2. Other resists
    Blome is looking at patents

3. Improvement & standardization of coating techniques

4. Adhesion difficulties study - looks like bad surfaces - P glass, Metal

— 5. Definition improvement. - aim @ 0.1 mil

6. Residue and/or scum.

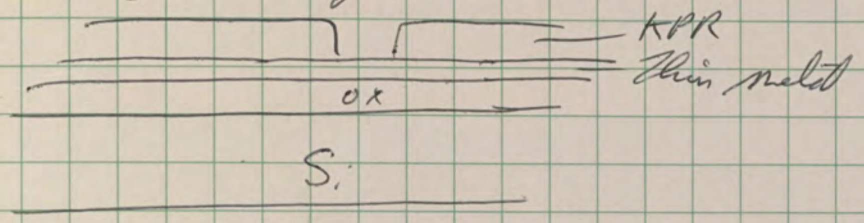
7. Optical jig improvement

— 8. Metal mask making - especially electrolytic etching.

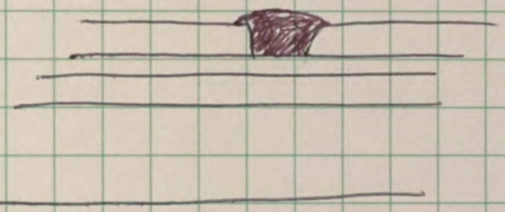
— 9. New thin films.

Our problems justifying looking at new materials are 1. pinholes, 2. resolution.

(This was followed by some rather free thinking concerning ways of living c̄ pinholes, such as filling them by electroplating. ~~Ex~~, Eg.

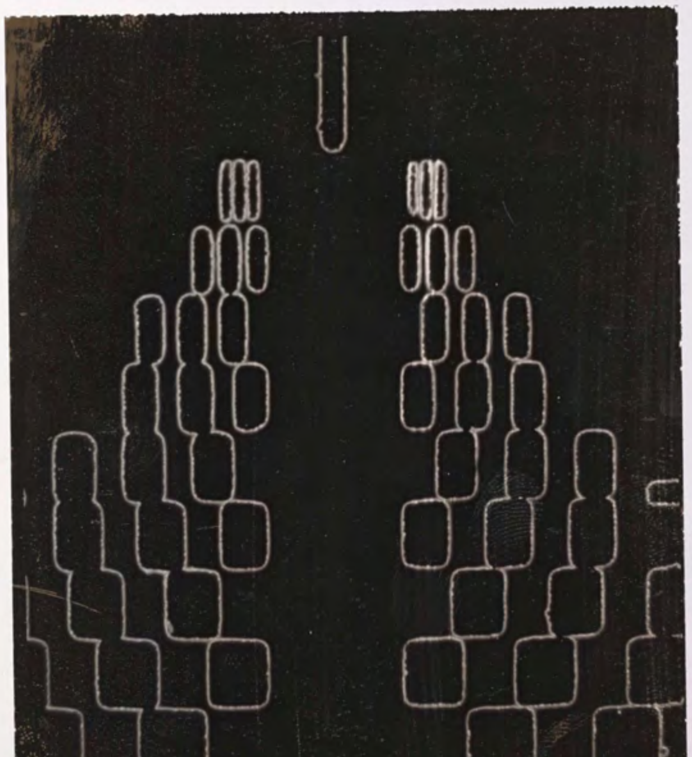


Then electroplate



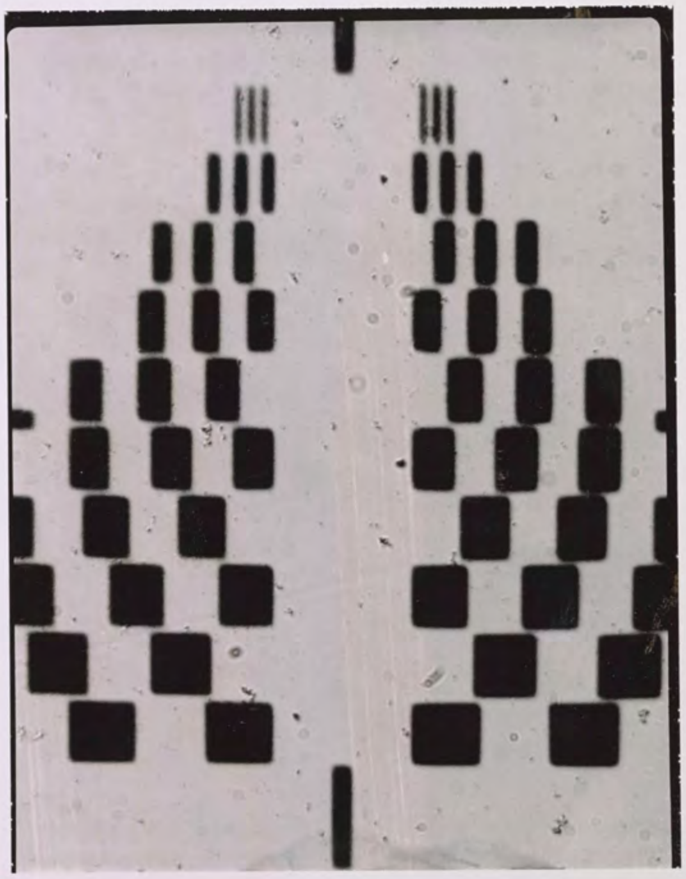
Re-coat and photo engrave.)

ETCHED WAFER



351X

MASK TPI-3



50X

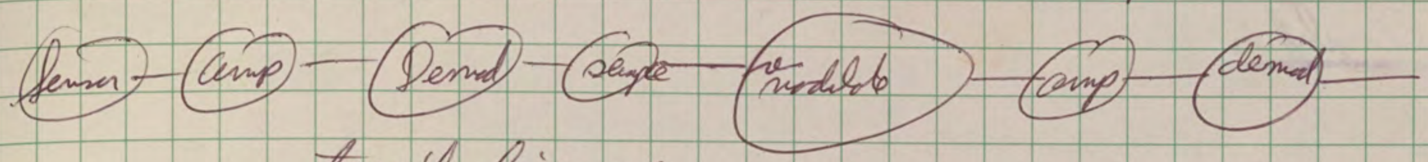
Aug 8 - Epitaxial

Roder
Wigton
Sah

Furnace still being profiled for Ga.

George Dyer

Discussion 8/8/62 with Autonetics (See Opposite page)



typical line-up.

Ckts we are discussing are on a suggested basis.

<u>Time</u> <u>Scale</u> Quote Aug 10

15-20 weeks to get prototype units

AA-501 – Gen. Purpose Diff Amp.

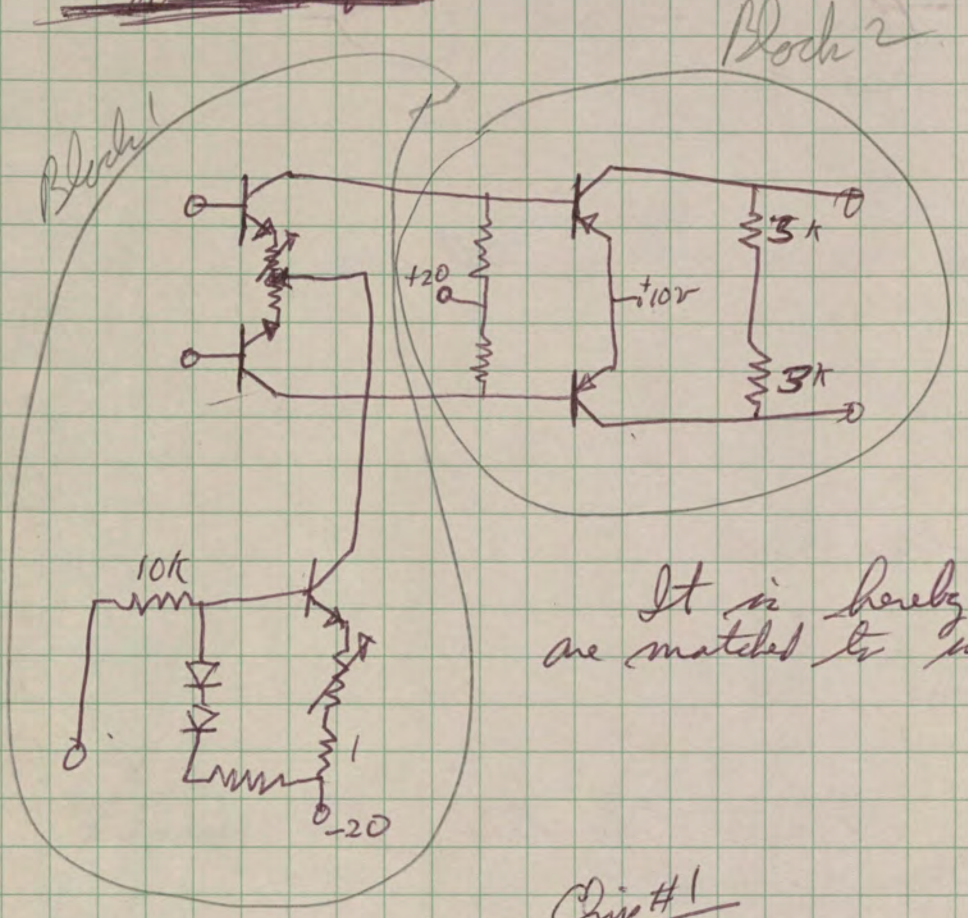
Must be in flat package, but will take two. They desire particularly that needs the interconnection.

1) Diff Amp.
2) Sig Coupler
3) Demodulator (4 Xstor)
4) Chopper
5) Valve drivers

	Demod	Dual Xstor Chopper	Single Xstor chopper
Switch config	full wave	½ wave (but still like 2/pkg	half wave
Max peak sig. I	15 ma	2 ma	200 µa
Offset	2 mv @ I_B = 1.5 ma	50 µv @ 1.5 ma	50 µv @ I_B ≤ 1.5 ma
R series on	80 Ω	200 Ω	200 Ω
Max input V	±20 v	±5 V	±200 mv
Switch sig input	coupler	coupler	line
Temp	0-70°c	0-70	0-70

Discussion afterwards: ($\bar{c}$ JPF, VHG) 8/8/62

Diff. Amplifier



It is hereby decreed that nichrome resistors are matched to within 1%.

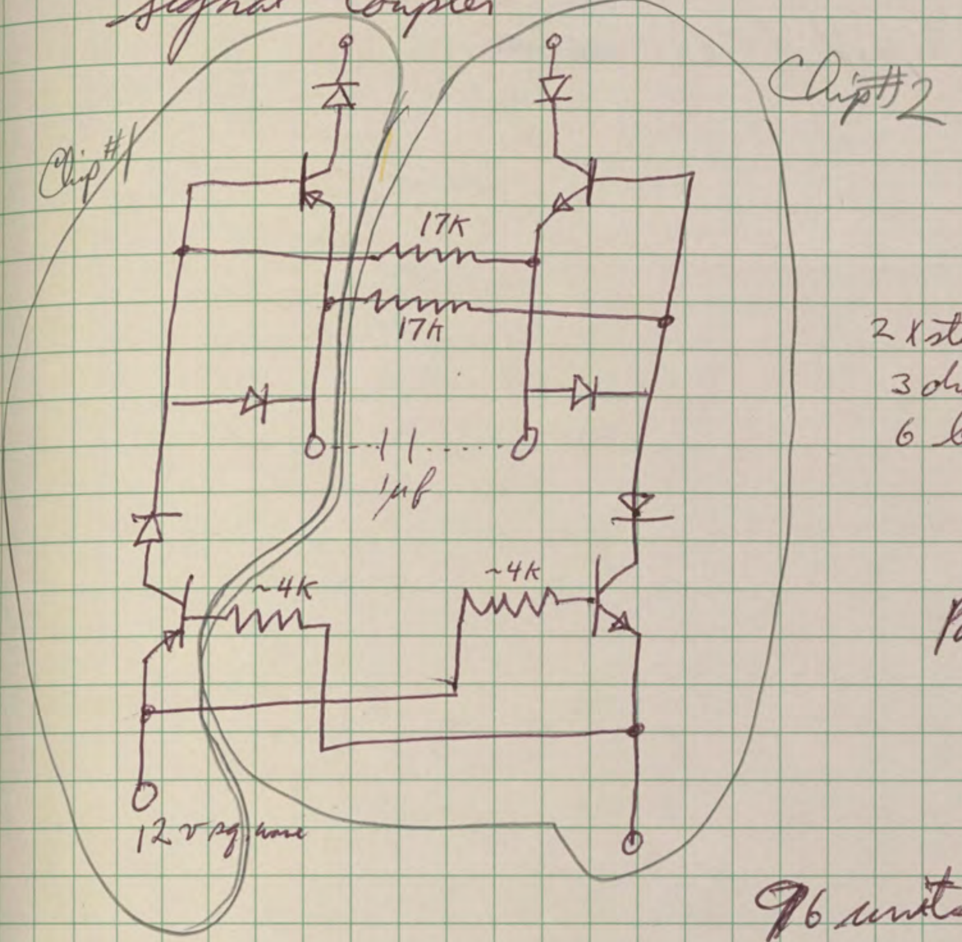
	Chip #1
3 tstors —	15
2 diodes —	8
4 resistors 30K —	38
2 adj R's —	20
6 leads —	24
	105
R @ 1% 30	30
	135

	Chip #2
2 PNP 20	20
4 R = 75K (1% match) =	158
6 leads	24
	202

We get really clobbered by needing a fantastic β match. It may be necessary to use a FSP 30 (separate NPN chips) for input.

It looks like 150 K$ for 76 of them

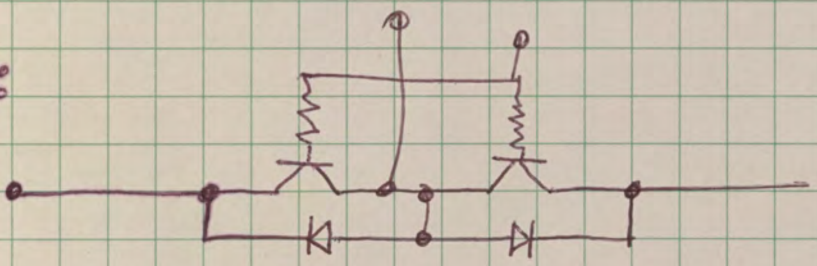
Signal Coupler



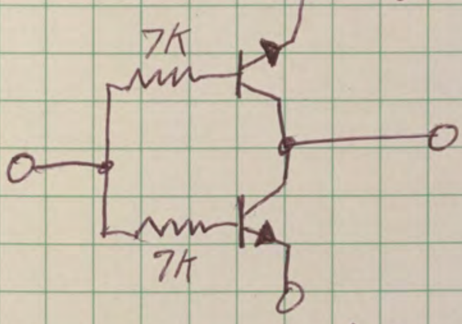
Chip #1		Chip #2	
2 Xstr (PNP) @10	= 20	2 Xstr (NPN) @ 5	= 10
3 diode 8	= 24	3 diode @4	= 12
6 leads @4	= 24	6 leads @4	= 24
	68	42 KΩ in 4 pair	50
			96 pt
Possibly	+ 8		+ 4
	76		100

96 units for ~~24K~~ 33K

Chopper:



or actually



"This looks ideal for upsidedown nichrome, epitaxial."

leads 4 X 4 = 16
14K @ 2K/2 = 18
2 Xstr @ 20 ea = 40
74 X 2 = 148 parts

or it could be a single Xstor

For 76 packages with 2 ea per package = 28 K

It may not use a ~~diff~~ Nichrome (possibly diffused)

Valve driver:

41 of them by special products @ ~~160ea~~ $16,000

Valve driver:

$16.000

25

	Dev K$	Eng Feb. Mar. 63	Eng Prototypes AM	~J-D	1st Prod. (243) '64	2nd Prod 6	3rd	4th	5th 91
AA-501 Dif Amp	150	76 ←	372 $200	2350 2796 559. →	22,842 $55	47,000 $30	47 $22	47 $21	$20
AA-502 Sig Corp	33	96 ←	494 95	2375 2965 282. →	23,085 ← 30 →	47,500 ← 18 →	47.5 ← 14 →	47.5 ← 13 →	12
AA-503 Demod	28	71 ←	297 90	1425 1793 161. →	13,851 ← 20 →	25,500 ← 10 →	28.5 ← 5 →	28.5 ← 4 →	4
AA-504 Valve driver	20	41 ←	71 85	350 462 39. →	3,402 ← 20 →	7,000 ← 10 →	7.0 ← 6 →	7.0 ← 4 →	4
	231								

Xfer to Production

To be by end of prototype

501 {135 202}

502 {76 100}

503 {148}

504 {~75}

Summary of Micrologic Lifetest Data

Aug 14, 1962

From discussion c̄ Murray Siegel:

~~Test #101: Good gates~~

Test #	# of units	Type	hrs/unit	T	# Failures	Reason
101						
	8	good G's	5700	300	0	
	50		4000	300	2	lead off, post lead off
	16		4650	300	0	
	10		4000	300	1	Metal open
	8		3000	150		
102		bad glued reject				
	12		4000	300	2	
	23		2000	300	2	
	24		2500	300	2	
	16		4000	150	0	
	28		4500	150	0	
103		no backside isolation				
	26		2000	300	1	
	26		2000	150	0	
104		Open cans				
	39		2500 ~~2400~~	~~2500~~ 150	1	
	39		2500 ~~2130~~	~~2500~~ 300	1	
107		Graded base				
	19		4000	~~4000~~ 300°	2	
	20		4000	~~4000~~ 300°	3	

Total 150° hrs = 363,5K c̄ 1 failure - but on an open can unit.
839.5K c̄ 16 failures

µL lifetest data, cont.

From talk with Don Thorn

Old R&D units – anything that ran 405 units for 3,838,000 hrs total with ~ ~ 50 failures at 125° operating.

Production devices:

A. 310 gates for 1,581,871 hours no failures
at 125°C operating
272 of these were early Mtr Vsn
48 were on weekly QA.
All had gone through environmental testing per prod. spec,

B. 1272 Class B gates except for high leakage for 2,623,956 hours @ 125°C operating – no failures

There were B units except for 3v leakage current. They were < 200 µa @ 0.8v.

C. 479 F elements (except low I_a, ~2.7 ma vs spec of 3.2) for 931,896 hrs with no failures.

→ Σ = 2061 units for 5,137,723 unit hours with no failures.

35 G's & 35 S's were stored for 5000 hrs @ 150°C with no parameter change (these were high r_e units).

128 G's on 347,136 with no failures for Murray Siegel.

Reported to Ashby:

5,484,859 unit-hours of operating life on production units without a failure at 125°C ambient.

839.5 K hrs @ 300°C storage c̄ 16 failures = 52,500 hrs MTF

363.5 K hrs @ 150°C storage c̄ 1 failure, but it was on a special unencapsulated test. No failures in sealed package for 266,000 hours.

QA line data on process shrinkage at present is running better than MM, even though there are many more leads.

+142,000 unit hours @ 150°C storage — no failures except 4 units had leads broken off by frequent testing for data logging.

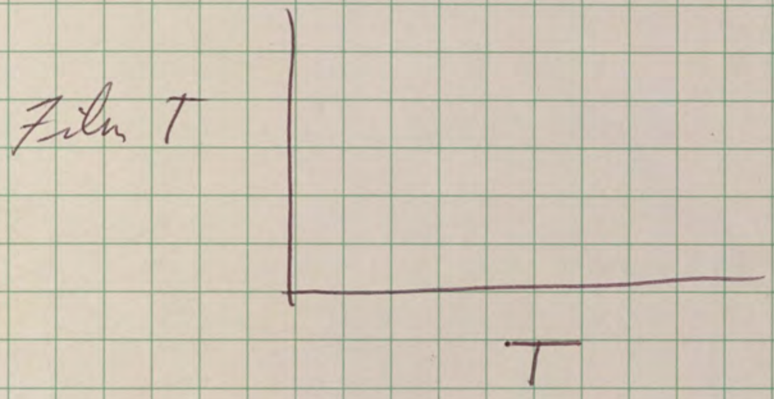
Epitaxial — Aug 15, 1962

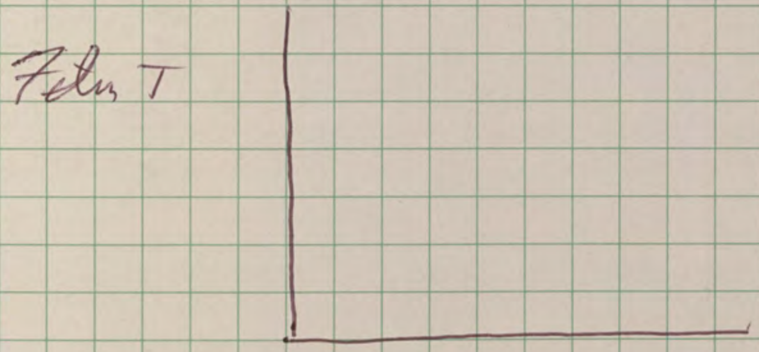
We have a Ga furnace going. We are about ready to stick in epitaxial wafers.
There will be some by next time (or before) to look at.

We have tried to use Dash ☒ projection to no avail

We are running up to 4 μ/min growth @~1250°C (in the Research reactor). This does not seem to affect the ~~spu~~ pyramids appreciable.

Const H_2 rate, Const total Silane





Hank is going to establish rate pt at which we get pyr growth

88

Aug 16, 1962 - Large Geometry Product Planning

Bay
Sparks
Yost
Hogret
Schroeder
Lamond
Hill.

Grinich
Pellegrini
Mays
Peters
Uhlahl
Graham
Reichard

	Status (Present)	Problems
3001	Making ~5000 per week TC pkg, 2 mil wire LV_{CEO} 35 min	has poor low current β. ∴ not a 4200 substitute.
~~3000~~ 4405	Running a few. Producibility not yet known. 30/1, -55 → +125°C @10ma V_{BE} ~20 v.	
6200	dead	
6201	dead	
6206	meets 2N1978 spec some has been made in the	
4011, 6		
4205 (150 v LV_{CEO})	Units delivered for T.V. market	
4300		
7000		Needs material.
3006	LV_{CEO}=60 - very low yield 1v @ 1/2 amp	Materials problem - but not looked at
4015 (Large triplet)	1 run came thru. good device.	Effects the R_{TH}. Must be studied for replacement. Must match double ended β 10 ma → 500 ma

We will make the large, epitaxial tridents. These will be made in time to make a decision & transfer by end of Oct.

Small Geometry.
New Product Meeting 10/19/62

1. 1312/15 - High Voltage ($LV_{CEO} \geqq 15V$) units look good as 2N2368/69 direct repacement 2 M.V runs.

   R&D 1312's evaluated -

   MV running 2 1312 runs - data by 11/15.

2. 3011 - 3111 - 3011 dropped. Conc on 3111. High current (500ma) $V_{CE(S)}$ a problem.

   1 run with 1045°C $POCl_3$ Em & Contr. Diff had τ_s 30-40 ns.

   2 More runs in Applications, probably N.G. due to 920°c reox after contr diff.

3. 1250 - Spec rewritten - 2272 units tested yields approx 74% O.A. . HA-3.7%, HB-3.5%, HC-9.6%, HD-.5.2%, MC 1.7%, MB-12.5%, MD-.8%, LD-32%. LD's were misclassified - will not all be LD's.

4. U-1/2

   1st MV U-1 runs (3) are U-1 except for Noise figure, due to poor contact etch. 3 more runs at 4th mask - data by 10/26. Problem - big demand now for "B" unit in TO-51 package. "B" spec is I_{SDO} .2 to .6 ma. vs normal

I500 of .2 to .9 ma. This drops die sort yield from 35 to 20% (approx). We think we Know what caused noise problem - answer on run eval. by 10/26.

u-2 6500 R&D dice gave 7% D.S. yield. all assembled and in Applications. will not start M.V. runs until u-1 process looks OK.

5. 0002 - No MV Activity. will have to wait until pressing production problems are under control. Probably 11/15/62, before any material started.

6. 1310/1311

7. 1340

8. 1341

9. 1321

10. 1324

11.

12.

13.

14.

On the 4015 Mtn View will run ~ 2 runs per week on this to the FSP-30 spec. After middle of Sept application will have enough data for the decision to switch or not.

Hill on 4405 - Last rept March 31

Decided to spec h_{FE} @ -55 20 min
" @ +125 80 max

250 going to applications
Runs 8-10% die sort yield

It is an extremely difficult device to make. Emitter V/I ~~is~~ needs special control

It is in the hands of A.E. for now. No new starts are being made.

We will try to make some 1450's (5 runs) @ die sort in 4-5 weeks.
Start c̄ 1250 material.

→ 4207

150 v 4205 ~~have~~ V_{CE} that depends upon wafer thickness.

These were 14 Ω-cm. With the As-doped solder ~~we~~ have no problem on switching.

6200, 6201, 6206
Udelhal says the 6200 is a dog.
He has made some 6206
~90 v LV_{CEO}
0.45 v @ 1 amp

This uses thinner epitaxial material than 7000.

He has ~~~~ 230 dice put in the 7/16 hex package

Schedule: Quantities of dice at die-sort by 10/1.
~~Wafers~~ Final devices - use 7/16 if available, something else otherwise.

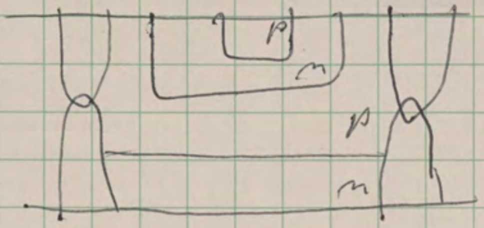
7000 150 v min material, >35 μ thickness
Aim at 100 good dice/week by the end of Sept.

SCR's

We need 25-30 Ω-cm material which we have not yet gotten.

It is a 70 mil die

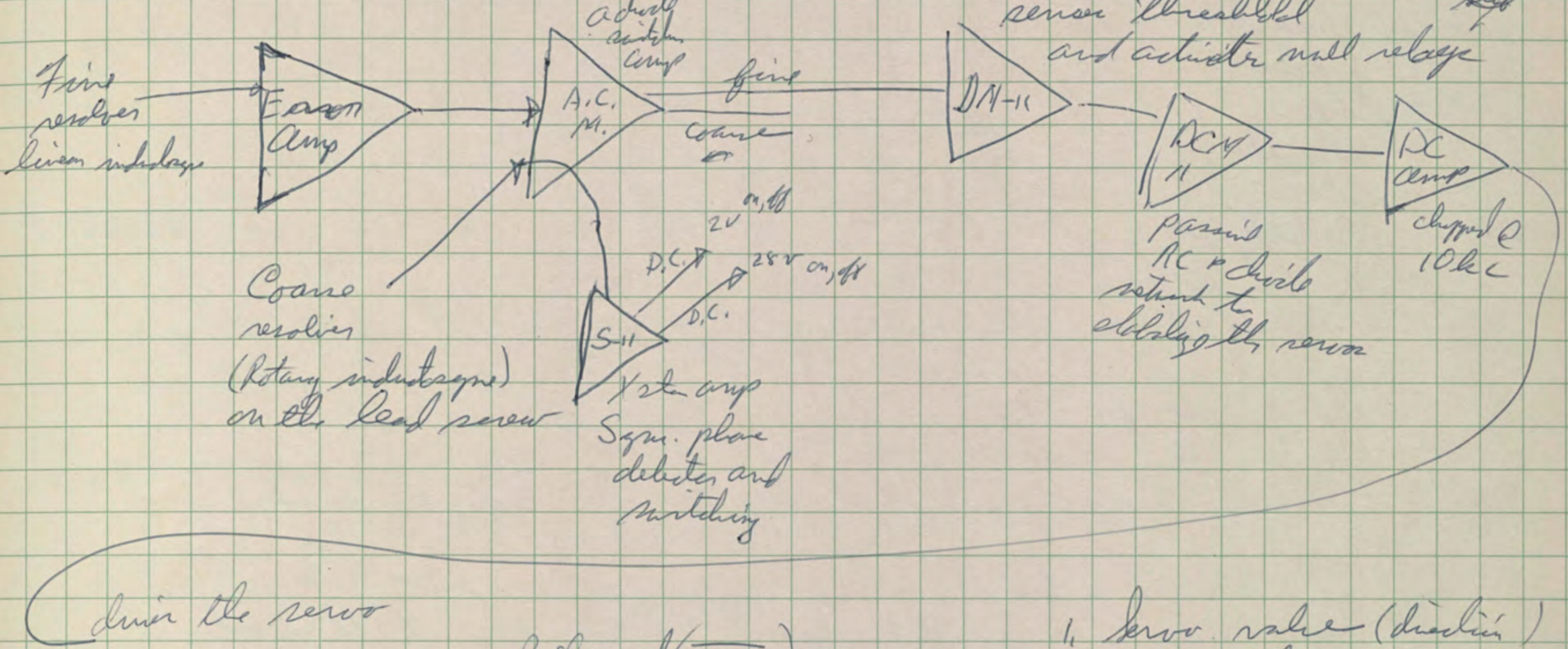
We must try centrifuge and/or shock.

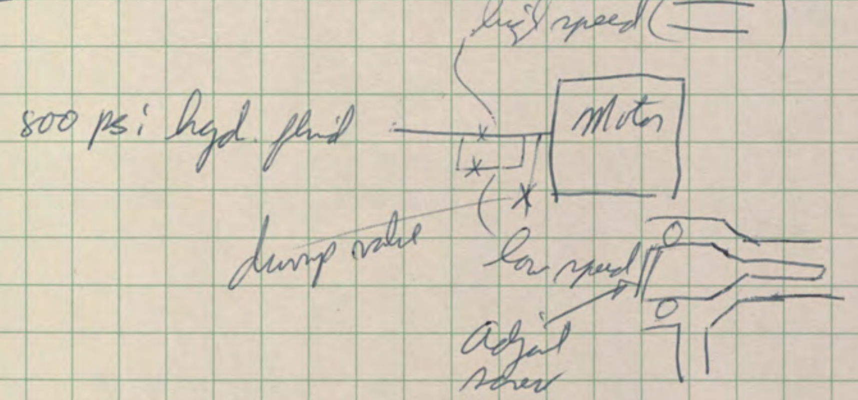


We need a guy in Oct.

Aug 27, 1962 Summary of the Farrand S+R situation

Block diagram





1. Servo valve (direction)
2. On-off hydraulic
3. Speed control valve
4. dump valve

Aug 28, 1962 Section Meeting everybody here

Capacity and time scale for mask making schedule
max min

	hr
On drawing board	14
" copy	1½
S&R	2½
Sub master	14
align	8-12
Working plate	8
To Q.C. & Waxing	8 -
Complete schedule	

We say 64-72 hrs

Mtn. View has done a 35 hr job
16 Scribe
3 Copy
8 S&R
8 Wafer out

We did one in 40 hrs. - the pL gate.

The mylar scribing material cos $4/sheet.

Swing shift is not busy now.

Mask making look good.

Permanent masks: The ones we made ~~didn't~~ couldn't be aligned.

The Rh films don't stick
New Cr look good - even harder than before.

Resists:
Room finally buttoned up.

Etching trouble on thick Al on power devices using ~1.5% NaOH
But
we accidentally used some Au etch soln and it worked beautifully. 1½ min vs 7 min. This was used at ~80°C.

Alignment of special 4200 masks in Box frames for SGS

The development of KPR c̄ the thicker coating has not worked in production.

Aug 28, 1962 – ROBE

Ferguson
Yost
Sang
Moore

Hill
Davis
McCall

Hill review:

4500 & 4200 use new masking
As of Aug 27 4500 did fine (over 12,000 wafers)

4500 have made some minor variations.

On the test wafer 4500 runs 0.6 – 7.4 pinholes / 45 mil square.

On the 4200 the thing got complicated – several "small" problems.

4200 runs ~ 8 pinholes / 0.045" square
small geometry runs ≈ 40. (without the new process

Should we do pinhole checks? (in R&D)

On the chrome masks looking at 441 pattern: 21 ~~pattern had pinholes.~~

On all together these 4 masks get ~12 % rejects.

Hill gives us ~~glass~~ a mask. We will get made to Min Vie in a week.

They have been doing some work on modifying patterns to get clean etching. Their working plates are very much worse than our masters.

RECEIVED
AUG 30 1962
GORDON E. MOORE

PIPE GENERATION AND ELIMINATION
NPN DEVICES

by Paul Hill

Pipe Source	Agent Causing Pipes	Contaminating Mechanism	Corrective Action	Remarks
1) Vacancy cluster in oxide layer.	Centers for donor dopant segregation.	Understood to be characteristic of oxide layer in segregating to concentrating impurities.	No known	Theory of one pipe formation method.
2) Surface contamination by ambient dust.	Factory ambient of air born particles handling contamination and people, lint and dust.	Fall out from air, contact with dust and lint carrying equipment and people.	1)Ambient filtration 2)Fall out shield protection 3)Rigid cleaning of handling equipment 4)Rigid wafer surface cleaning throughout processing.	
3) Incomplete oxide removal at first and second masks.	1) Small oxide patches form masks thru which boron cannot penetrate. 2) Causes concentration gradient	1)Leaves "pipes" or "**veins**" of N type material thru base area which later on cause low breakdown junctions. 2)Concentration gradient causes lower break down than that encountered at regular junction.	1) Masking techniques a. Exposure. b. Developing. c. Etching until all oxide is removed. d. Double masking.	1) Mask technique standardization.
4) Material defects	1)Dislocations	1)Preferential diffusion of unwanted contaminant causing concentration gradient. 2)Leave pits and depressions for dirt and surface contaminants to reside in.	1)Discard crystals and wafers exhibiting excessive occurance of this defect. 2)Cut slices thick enough so that they can be etched to a smooth surface.	1)Material prep standardization
5) Phosphorous Contamination	Small particles of phosphorous which are allowed to settle on the wafer surfaces	Absorbtion of water by P_2O_5 forms phosphoric acid droplets. Rapid diffusion of phosphorous thru oxide to form N+ regions near junctions which cause low breakdown or emitter - collector short failures.	Keep wafers covered when not being processed 1. N_2 ambient 2. Petri dish Isolate phosphorous operation from other process operation	

PIPE GENERATION AND ELIMINATION

NPN DEVICES

Pipe Source	Agent Causing Pipes	Contaminating Mechanism	Corrective Action	Remarks
6) Mask Defects	Reproducable flaws in mask which print on KPR.	At second mask, make small improperly placed emitters which cause low breakdown and emitter-collector short failures.	Mask inspection to reject unsuitable masks.	

8/29/62
cc: CT Sah
P. Flint

Package Xafer:

What: a flexible plug. useful for μckting and.

Xafer: 1. Etching
2. Three stage assembly.
3. Test fixtures
4. Life tests
5. Pedegg - must have round leads.
6. Ceramics

Etching - **Paul Hill** (number in Peterson area) from Morrie Focht

Mel would like to start immediately on a special product.

Ceramic pieces - ~ 6-8 weeks delay in getting new ceramics.
but they are 1 - 1.5 ¢ each.

Process Xafer plan by

We will set up to supply parts as necessary.

Aug 30, 1962 - Discussion c̄ CTSah re: Physics Section Program.

G. Moore

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

To: Don Yost Paul Hill	cc: G. Livingston P. Wilson R. Fouquet	F. Durand R. Crosby E. Krueger	October 11, 1962

From: W. K. Tsang

Subject: Methyl Borate Doping Process

The process specification for emitter (4500) doping and base (4200) doping has been completed.

The methyl borate furnace in PNP area is ready for operation and the furnace in the NPN area is expected to be ready for operation by October 12.

The evaluation of the 4200 and 4500 duplicating runs will be followed in a later report.

W.K. Tsang

W. K. Tsang

WKT:ch

Attachment proposed specification.

FAIRCHILD SEMICONDUCTOR

Process Specification

No. __________
Pg. 1 of 12
Date __________

I. TITLE

Pretreat Boron

II. PURPOSE

To deposit boron on the wafer surface in a layer of uniform concentration.

III. PRODUCT PARTS

A. Silicon Wafer, Oxidized except for the Base (NPN) or Emitter (PNP) Pattern.
   1. Source - Process Specification 1250, "Inspect Wafer"

IV. MATERIAL AND SUPPLIES

A. Tri Methyl Borate $(CH_3O)_3B$, *
   1. Source - M & SS
B. Nitrogen Gas
   1. Source - M & SS 49
C. Oxygen Gas
   1. Source - M & SS 50
D. Trichloroethylene (TCE)*
   1. Source - M & SS 35
E. Acetone*
   1. Source - M & SS 32
F. Hydrofluoric Acid (HF), Electronic Grade*
   1. Source - M & SS 36

V. EQUIPMENT AND TOOLS

A. Diffusion Furnace, Complete with Quartz Tube, Manifold, and Necessary Electrical Controls
   1. Source - FSC Fabricated
   2. Drawing No.
B. Gas Manifold
   1. Source - FSC Fabricated
   2. Drawing No. 0723
C. Quartz Wafer Boat, Slotted
   1. Source - FSC Fabricated
   2. Drawing No. 0734-1

* SEE LIST OF HAZARDOUS MATERIALS

D. Quartz Pull Rod
   1. Source - FSC Fabricated
   2. Drawing No. SKB-2358

E. Quartz Boat Rack
   1. Source - FSC Fabricated
   2. Drawing No. SKB-2363

F. Tweezers
   1. Source - California Safety & Supply Company
   2. EREM No. - 11

G. Microvoid Dust Hood
   1. Source - Air Shields Inc.
   2. Series No. 11-600-71

H. "White Elephants"
   1. Source - FSC Fabricated

J. Refrigerator
   1. Source - L.P. Klein or Equivalent

K. Teflon Slotted Boat
   1. Source - FSC Fabricated
   2. Drawing No. 0950-1-2-3

L. Ultrasonic Cleaner
   1. Source - National Ultrasonic Corporation or Equivalent
   2. Generator Model G-100
      Tank Model G-100

M. Pyrex Beaker, 1500 cc
   1. Corning or Equivalent

N. Spinner Motor
   1. Source - FSC Fabricated
   2. Drawing No. 0950-1-2-3

VI. REQUIREMENTS

A. Control and Acceptance Limits
   1. The mean V/I ($\overline{X}$) often readings (two readins from each of 5 wafers) shall be within the limits given in Table I.
   2. The range R, shall not exceed the limit given in Table I.

VII. OPERATING PROCEDURE

A. Operating Instructions

1. Cleanliness of all material going into the furnace is extremely important. Anything going into a furnace shall be touched only with clean nickel tweezers, vacuum pickup, or clean push rod.

2. Check to verify that furnace was profiled at start of shift and the flat zone is a temperature as indicated in Table 1, with a maximum allowable difference of no more than 3°C over the center 12" flat zone. The flat zone is from 12" to 24" from the front of the furnace. If the profile is not correct, notify supervisor before proceeding with any other steps in this procedure.

3. Check gas pressure gauge.

   a. Nitrogen pressure - 5 ± 0.25 psig; Nitrogen panel valve must be fully open.

   b. Oxygen pressure - 5 ± 0.25 psig; oxygen panel valve must be fully open.

4. Fill the constant temperature bath with acetone to the brim, check to make sure that the refrigeration system is on. At least 30 minutes prior to processing the runs, check to verify that the source temperature is at -18 ± 1°C.

5. Check the exhaust bubbler attached to the source flask for water level, and fill if required, according to the maintenance procedure.

6. Check flow meters and stopcocks for standby positions as shown in Table II, check the gas manifold to make sure that all joints are tightly sealed.

7. Prior to loading the wafers, the wafers shall be cleaned as follows:

   a. Fill up a 5" x 5" x 5" plastic container with 10:1 Hydroflouric Acid* so that the acid would cover the teflon holder with wafers for at least 3/4" ± 1/4".

   b. Fill up a second plastic container with running DI water. Leave the DI water running.

   c. Load two runs of wafers into the slotted Teflon holder with clean nickel tweezers.

   d. Immerse the holder into the 10:1 Hydroflouric Acid* gently so that wafers will not float up. Gently rotate the holder in the 1:0 Hydroflouric Acid* for 7 ± 2 seconds.

   e. Remove the holder from the acid container and immerse in the DI water container and rotate gently for at least 30 seconds.

   f. Fill up three 5" x 5" x 5" plastic containers or 1000 ml/beaker with fresh TCE, acetone, and DI water in that order.

   g. Remove the teflon holder from the DI water, drain any excess water and immerse the holder in the acetone container. Rotate the holder for at least 30 seconds. Remove the holder and rinse wafers with acetone squirt bottle.

* SEE LIST OF HAZARDOUS MATERIALS

h. Immerse the holder in the TCE container and ultrasonically clean for 5 minutes.

i. Remove the holder, drain excess TCE rinse wafers with acetone squirt bottle.

j. Ultrasonically clean wafer in Acetone for five minutes.

k. Remove holder from acetone, drain off excess acetone, and rinse wafers and holder under running DI wafer.

m. Ultrasonically clean wafers in DI water for five minutes.

n. Remove holder and rinse wafers thoroughly under running DI water.

o. Spin wafers until dry.

Note: Section 7 for base doping process only.

8. Wafers shall be loaded on slotted quartz boats at least 6" inside a sterishield. Use clean nickel tweezers only. The loading pattern on 13 slot quartz boat shall be as follows:

1. Emitter

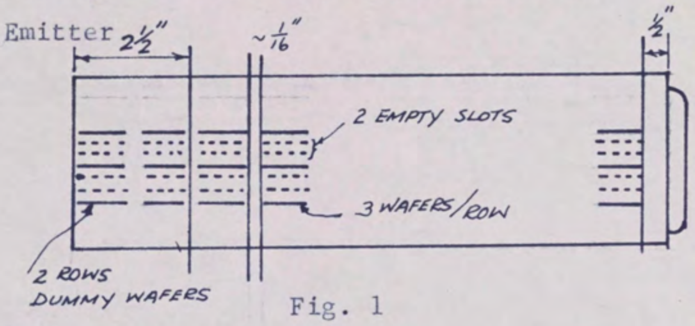


Fig. 1

2. Base

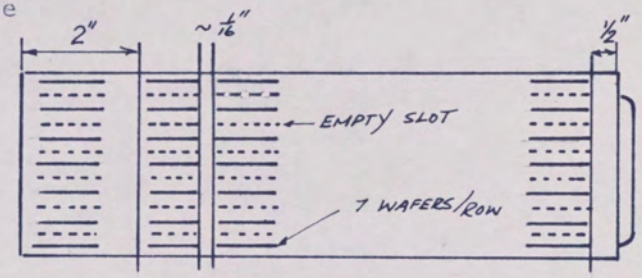


Fig. 2

3. Load wafers at the source end of the boat first work toward the handle. Load as far as the temperature profile permits but there should be a minimum empty space of 1/2" at the handle end.

4. The wafers shall be orientated so that they all lean to the right on looking down the boat holder as shown in Figure 3.

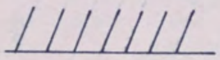


Fig. 3

5. The run number shall be in the numerical order on the boat with lowest numbered run nearest the source. For emitter use no more than 25 wafers per boat and for base use no more than 50 wafers per boat load. At the beginning of each shift and before processing any runs in the furnace, sort out the run travelogs into numerical order for each product. All products should be processed in numerical order.

6. The wafer pattern shall face the right hand side on looking down the handle end of the boat.

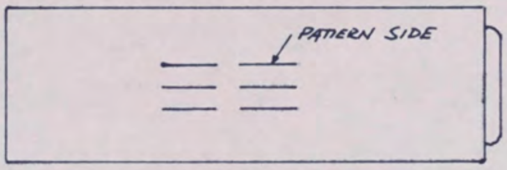


Fig. 4

7. Record the run number, number of wafers in, and date on the run sheets, and in the emitter pretreat log.

9. A test run must be run prior to processing any runs, if the furnace was not used during the previous 8 hours, as the boat was cleaned or the the thermocouple was changed or the tube and manifold was cleaned or changed. Six freshly etched, non masked wafers, two in the front of the boat two in the middle of the boat, two in the rear of the boat, shall be loaded as indicated in paragraph(8). The wafers should be chips, if available, rather than whole wafers. Check flowmeters, stopcocks for standby position.

10. Transfer the boat load of wafers quickly to the furnace in the "white elephant". Hold the "white elephant" in line with the tube without actually touching. Using the quartz push rod, for this furnace, push the boat smoothly into the furnace until the index mark on the rod is even with the end of the tube. Make certain that the boat is slightly inclined from horizontal position so that all wafers are inclined to one side. Do not use an end cap.

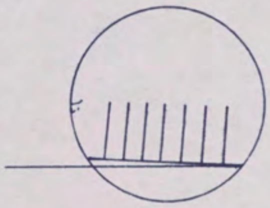


Fig. 5

11. Turn on the timer for preset cycle as given in Table II.

12. Turn on flowmeter (I) and after 2 seconds turn stopcock (c) to "on" position, gas should be bubbling through the water bubbler. Make certain

that the flowmeter (I) is turned on before the stopcock to prevent the water from sucking back into the system. Adjust the flow on flowmeter (I) to scale as indicated in step (2) of table.

13. When the preheat period is over, as indicated in Step (3) of Table II, turn stopcock (a) to "1" position, and turn stopcock (c) off in that order. See Note.
14. When the doping period, as indicated in step (4) of Table II, is over turn off flowmeter (I), and turn stopcock (a) to "2" position.

15. Start to pull the boat when the buzzer sounds. The pull time shall be one minute.

16. When the wafers and boats have cooled, remove the wafers from the boat and place them in their respective dishes. Replace the lid on the dish immediately. Store the quartz boat in sterishield.

17. The V/I of each run shall be measured as per specification V/I after base or emitter predeposition. The runs shall be accepted or rejected as per specified acceptance limits.

18. If the V/I is not acceptable, do not process any further runs in the furnaces. Inform the foreman of irregularity. Furnace checks and test runs must be made before proceeding with any more production lots.

19. Allow a minimum of 15 minutes "stand-by" cycle between runs.

Note: Section (13) and (14) for emitter doping process only for base doping process. (13) and (14) should read as follows:

(13) When the preheat period is over, as indicated in step (3) of Table II turn stopcock (b) then (a) to "1" position and turn stopcock (c) off in that order.

(14) When the doping period as indicated in step (4) of Table II is over turn off flowmeter I and turn stopcock (a) and (b) to "2" position in that order.

TABLE I OPERATING TEMPERATURE AND DEVICE

V/I Limits at Predeposition

Device	Temperature	V/I	R
4500	1188 - 1192	.5 - .7	.20
4200 Series	958 - 962	15 - 20	5.0

TABLE IIA DETAIL OF PREDEPOSITION CYCLE

Device 4500

PERIOD	TIME REMAINING	FLOWMETER SETTING AND STOPCOCK POSITION
1) Total cycle (stand by)	22	Source N_2 (I) = Off Small N_2 (II) = 5.0 ± 0.1 Large N_2 (III)= 11 ± 0.1 Oxygen (IV) = 10 ± 0.1 N_2 (VI) = 6.0 ± 0.1 Stopcock a (2 position) Stopcock c (Off position)
2) Boat in	22	Source N_2 (I) = 5.0 ± 0.1* Small N_2 (II) = 5.0 ± 0.1 Large N_2 (III) = 11.0 ± .1 Oxygen(IV) = 10 ± .1 N_2 (VI) = 6.0 ± 0.1 Stopcock a (2 position) Stopcock c (On position)
3) Preheat	22 - 15 (Actual time 7 minutes)	Same as 2)
4) Doping	15 - 8 (Actual time 7 minutes)	Source N_2 (I) = 5.0 ± 0.1* Small N_2 (II) = Off Large N_2 (III) = 11 ± 0.1 Oxygen (IV) = 10 ± 0.1 N_2 (VI) = 6.0 ± 0.1 Stopcock a (1 position) Stopcock c (Off position)
5) Flush	8 - 0 (Actual time 8 minutes)	Source N_2 (I) = Off Small N_2 (II) = 5.0 ± .1 Large N_2 (IV) = 11 ± .1 Oxygen (IV) = 10 ± .1 N_2 (VI) = 6.0 ± .1 Stopcock a (2 position) Stopcock c (Off position)
6) Pull	1 minute	Same as 5)

Note 1 - Individual flowmeters should be set with eye on the same level as the float.
2 - Stopcocks should be in their exact positions.

*See Detail Procedure

TABLE IIB DETAIL OF PREDEPOSITION CYCLE

Device 4200 Series

PERIOD	TIME REMAINING	FLOWMETER SETTING AND STOPCOCK POSITION
1) Total cycle (stand by)	15	Source N_2 (I) = Off Small N_2 (II) = 5.0 ± 0.1 Large N_2 (III)= 11 ± 0.1 Oxygen (IV) = Off N_2 (V) = 5.0 ± 0.1 N_2 (VI) = 6.0 ± 0.1 Stopcock a (2 position) + Stopcock b (2 position) + Stopcock c (Off position)
2) Boat in	15	Source N_2 (I) = 5.0 ± 0.1 * Small N_2 (II) = 5.0 ± 0.1 Large N_2 (III) = 11.0 ± .1 Oxygen (IV) = Off N_2 (V) = 5.0 ± 0.1 N_2 (VI) = 6.0 ± 0.1 Stopcock a (2 position) + Stopcock b (2 position) + Stopcock c (On position)
3) Preheat	15 - 8 (Actual time 7 minutes)	Same as 2)
4) Doping	8 - 6 (Actual time 2 minutes)	Source N_2 (I) = 5.0 ± 0.1* Small N_2 (II) = Off Large N_2 (III) = 11 ± 0.1 Oxygen (IV) = 5 ± 0.1 N_2 (V) = Off N_2 (VI) = 6.0 ± 0.1 Stopcock a (1 position)** Stopcock b (1 position)** Stopcock c (Off position)
5) Flush	6 - 0 (Actual time 6 minutes)	Source N_2 (I) = Off Small N_2 (II) = 5.0 ± .1 Large N_2 (IV) = 11 ± .1 Oxygen (IV) = Off N_2 (V) = 5.0 ± 0.1 N_2 (VI) = 6.0 ± .1 Stopcock a (2 position) + Stopcock b (2 position) + Stopcock c (Off position)
6) Pull	1 minute	Same as 5)

Note 1 - Individual flowmeters should be set with eye on the same level as the float.
2 - Stopcocks should be in their exact positions.

* See Detail Procedure ** Black Down + Black Up

TABLE III

V/I After Diffusion

Device	Temperature	Cycle	V/I	R
4200 Series	1215°C	2 hrs. (Dry 0_2=7 55 min.(Wet Water Temperature =98±1 5 min. (Dry 0_2=7	23-28	5.0

FIG. 6 A.

EMITTER PROCESS FLOW DIAGRAM.

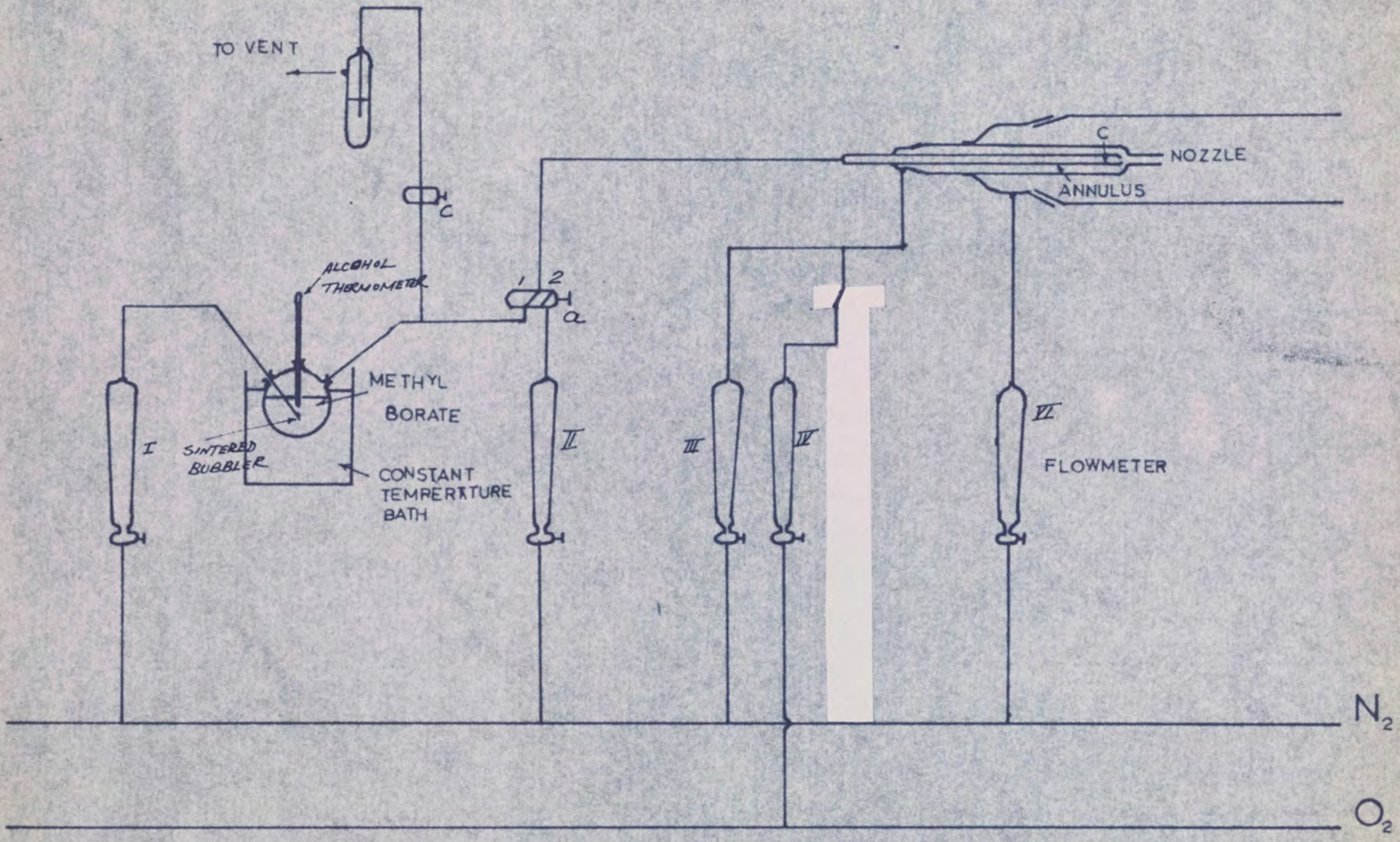
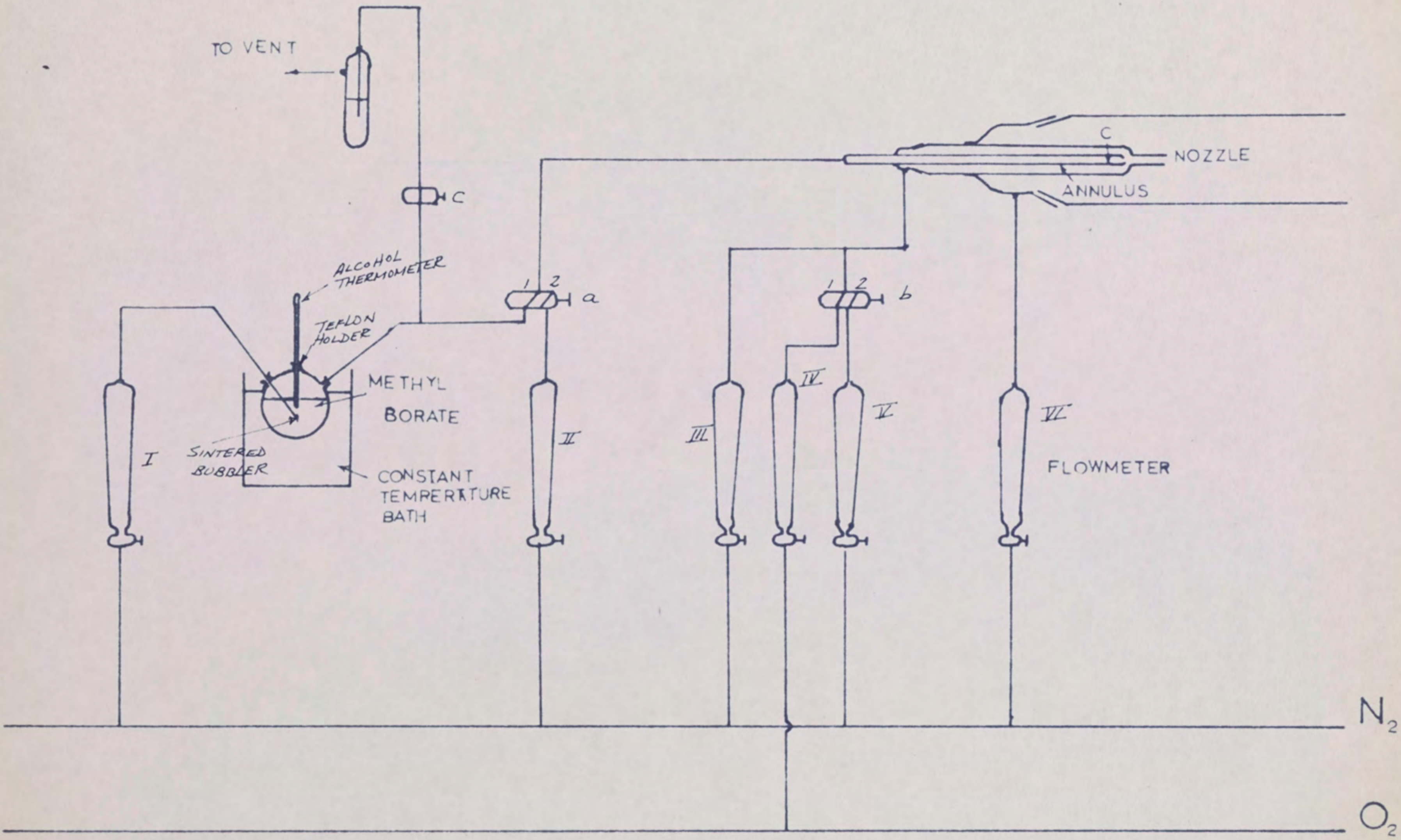


FIG. b B

BASE PROCESS FLOW DIAGRAM



B. Detail Procedure

1. The temperature profile shall be taken each shift just prior to processing any runs and with the gas flow as specified in section 1 of Table II.
2. The profile shall be taken as per process specification 5017.
3. The furnace controller and rheostat shall be adjusted as per process specification.
4. The doping level (V/I should be consistantly as indicated by the temperature - V/I Table I. When a new furnace or manifold is assembled the following points shall be checked out.
   a. Mixing nozzle
      1) The blendor should extend approximately 1" into the furnace.
      2) The blendor tube A should be aligned perfectly concentric with nozzle B.

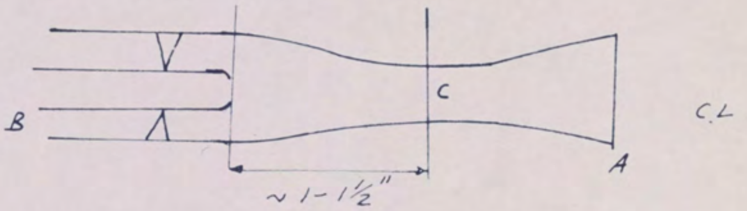


Fig. 7

      3) The tip of the nozzle tube B should be approximately 1" - 1-1/2" from point C. The relative position of the various parts shall be measured and recorded so they can be can returned to the exact position after being cleaned.
      4) The position of tube B should be adjusted until a random and well mixed gas pattern as shown in Fig. is obtained with gas flow rate specified in Step 1) of Table II.

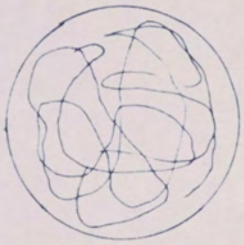


Fig. 8

      5) The V/I spread along the boat should be insignificant.

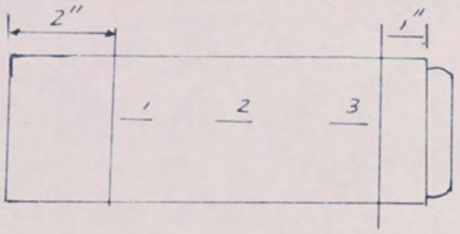


Fig. 9

If V/I at position (1) is higher than positions (2) & (3), it indicates that the gas is flowing too fast, and vice versa if V/I at position (1) is significantly less than positions (2) & (3). The tube B should be adjusted 1/4" at a time until there is a difference of less than 5% in V/I readings at point (1) and point (3).

6) The nozzle should be cleaned once a month as follows.

   a) Disconnect all connecting glass tubing.
   b) Remove the nozzle very carefully from the furnace tube.
   c) Remove the nozzle holder from the blender. (See Fig. 14)
   d) Remove the nozzle from the holder by slipping out the rubber tubing very carefully
   e) Wipe off excessive grease from the joints.
   f) Rinse all parts in TCE*thoroughly. Rinse with acetone and DI water thoroughly.
   g) Rinse the blender until all the white deposit is gone. Rinse well with DI water.
   h) Clean all parts well again with TCE, acetone, and DI water.
   i) Blow dry completely with nitrogen blow gun.
   j) Proper the joints carefully with a thin film of silicone vacuum grease. Do not grease the last 1/4"

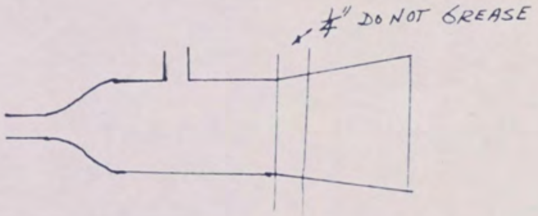


Fig. 10

   k) Replace, the nozzle, nozzle holder, and blender.

b. Thermocouple - When a thermocouple is changed, a test run must be run to check out the thermocouple. If the V/I readings do not agree with the "temperature - V/I" table, a correction factor should be applied to the thermocouple. V/I should always be used as the criteria. However, once a correction factor for the thermocouple is established, it should not be changed until the thermocouple is changed. The thermocouple should be changed at least once every two weeks for furnaces with temperature over 1100°C, or once every 6 months for furnaces with temperature under 1100°C.

c. Source

   1) The source should be changed at least once every month or when frothing on the surface is noticed.
   2) Source change.

      a) Remove source flask from the refrigerator.
      b) Drain the content into the sink.
      c) Rinse the flask thoroughly with DI water to remove all boron hydroxide precipitate.
      d) Clean off all remaining silicone grease from the joints with paper towels.
      e) Rinse the flask and joints thoroughly with TCE*twice.
      f) Rinse the flask and joints with acetone twice.
      g) Rinse the flask and joints with running DI water for at least one minute.
      h) Drain off excess water.
      i) Dry the flask completely with N_2 blow gun.

*SEE LIST OF HAZARDOUS MATERIALS

j) When it is sure that the flask and the joints are absolutely dry, reassemble the flask as follows.

(1) Both the male and female tapered joints of the flask and the "inlet" and "outlet" should be applied with a smooth film of silicone vacuum grease except the last 1/4" as shown.

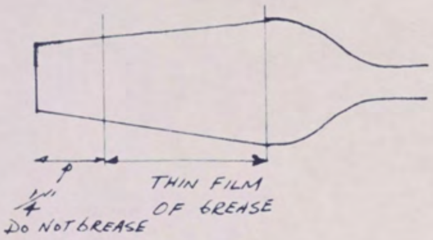


Fig. 11

(2) The ball joints sockets should have a thin film of grease. Make sure that no grease gets into the glass tubing.

(3) Replace the "inlet" and the "outlet" to the flask. Rotate the joints until a firm seal is obtained.

(4) Open a fresh and sealed 250 g bottle of methyl borate. Wipe the bottle top off any white deposit. Pour the entire bottle of methyl borate quickly into the flask through the thermometer holder opening. Replace the thermometer holder quickly.

(5) Replace the source bottle in the refrigerator and reassemble all connections.

(6) The source temperature should be at - 18 ± 1°C and free of frozen methyl borate.

3) The nitrogen source carrier gas should be between 4.8 - 5.4 (1-F-1/8-12-5).

a) For a new system and a new bottle of source, the flow rate should be established during the first test run.

b) Boron skin will form on the wafers if too much source is used. The idea source level should give just a tiny try of brown boron color on tip of wafer.

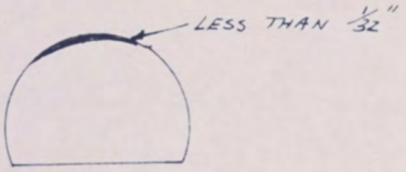


Fig. 12

c) If a V/I gradient is noted from top to bottom it

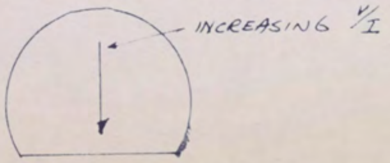


Fig. 13

indicates that the source flow is not enough.

d) Use a nitrogen flow of 5.0 (FP-1/8-12-5) for a start and change by 0.2 at a time if necessary

5. Quartz Boat.

a. 13 slots quartz boat should be used.

b. The quartz boat should be cleaned in HF for 30 seconds at least once a week.

c. The boat should be doped once with boron after being cleaned.

d. A new boat should be doped at least three times before processing any runs.

e. A boat should be doped once if it has not been used in the last 24 hours.

6. Quartz Tube.

a. Tube should be cleaned or changed once a month or when severe sticking of the boat is observed.

b. A new tube should be doped three times before processing any runs.

7. Refrigerator.

a. Coolant temperature of the bath should be at - 29 to - 30°C.

b. The constant temperature bath shall be filled with the coolant every morning.

c. The coolant shall be syphoned out and the bath refilled with fresh coolant when the coolant has more than 1/4 of water content.

d. If the source does not attend the specified temperature of -18±1°C with the coolant set at -29°C, extra insulation should be provided for the refrigerator pot.

e. If a source temperature of -18±1° can not be attended without freezing, the following correction on the source flow should be used:

Source temperature	- Specified Source Flow
-16°	-0.2
-15°C	-0.3

8. Flowmeters:

	Base	Emitter
I	FP-1/8-12-5	FP-1/8-12-5
II	FP-1/8-12-5	FP-1/8-12-5
III	FP-1/4-20-5	FP-1/4-20-5
IV	FP-1/8-12-5	FP-1/16-20-5
V	FP-1/8-12-5	None
VI	FP-1/8-12-5	FP-1/8-12-5

The flowmeters shall be cleaned once a month as follows:

a. Disassemble all flowmeters.

b. Remove the teflon plug, sapphire float, needle valve and valve holder and soak in numbered beakers filled with acetone.

c. Wipe out all grease from the joint sockets.

d. Flush each flowmeter with TCE for at least one minute each.

e. Rinse each flowmeter with acetone for one minute each.

f. Remove each flowmeter with DI water for at least 1 minute.

g. Blot dry the sapphire floats, and dry all other parts with N_2 blow gun.

h. Replace floats and valves.

i. Grease the joints carefully with a thin film of silicone vacuum grease and reassemble.

j. <u>Never</u> clean flowmeter with HF* of any form.

9. Thermocouple sheath

The thermocouple sheath shall be changed every three months or when the transparent quartz turned white due to doping and devitrification.

10. Glass tubings

Glass tubings shall be cleaned off all vacuum grease and rinsed with TCE,* acetone*, and DI water for at least 30 secons each and blow dry.

*SEE LIST OF HAZARDOUS MATERIALS

VIII. INSPECTION

1. The doped wafer shall have no rainbow effect on boron skin.

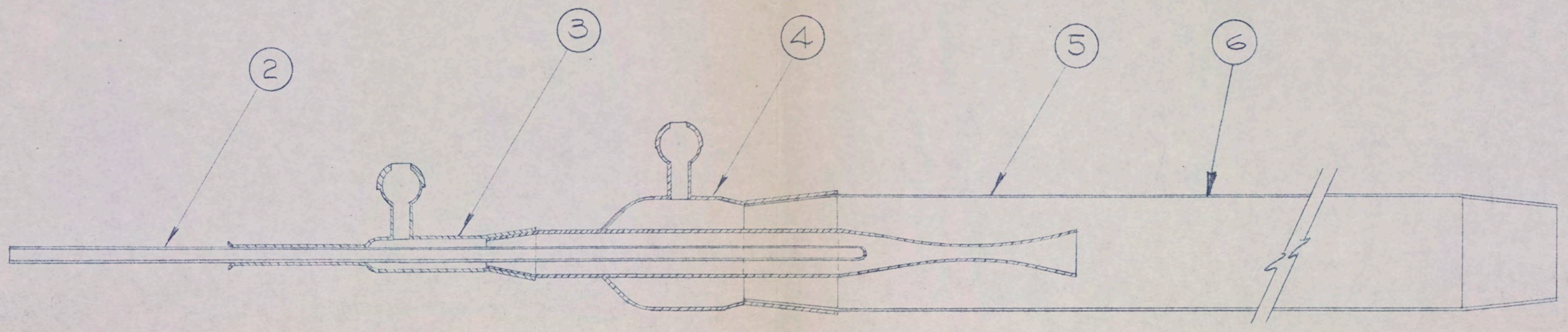
2. Emitter doped wafers shall have a brown to blue oxide.

3. Base doped wafers shall have none to light brown color oxide, possible a stripe of blue oxide on time of wafers.

W.K. Tsang
Writer

____
Approved

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	DET. 6 ADD.	8.8.61	C. Cooke



DET. 5 CAN BE
SUBSTITUTED WITH DET 6.

ASSEMBLY

FABR. ITEM	PURCH. ITEM	SHEET NO.	PART NUMBER	QUANT. REQ'D.	PART NAME	DESCRIPTION	SUGGESTED SOURCE
6		2		1	FURNACE TUBE		
5		2			FURNACE TUBE		
4		2		1	BLENDER - QUARTZ		
3		2		1	NOZZLE - HOLDER - QUARTZ		
2		2		1	NOZZLE - QUARTZ		
1		1		1	ASSEMBLY - FURNACE MANIFOLD		

MATERIAL:

FINISH:

TOLERANCES AND NOTES
UNLESS OTHERWISE SPECIFIED
DECIMAL .XX±.015 .XXX±.005
FRACTIONAL ± 1/64
ANGULAR ± 0° 30'
BREAK ALL SHARP EDGES .010
ALL DIMENSIONS INCHES
DO NOT SCALE THIS DRAWING

DRAWN D.H. DATE 8.25.60
CKD DATE
ENGR Aloder DATE
APPD DATE
APPD DATE
RELEASED C. Cooke DATE 8-8-61

FAIRCHILD
SEMICONDUCTOR CORPORATION
MOUNTAIN VIEW, CALIFORNIA

FURNACE MANIFOLD

SCALE 1/2
DWG. SIZE C
0723A
SHEET 1 OF 2

TOOL DESIGN

PRODUCT DEFINITION

1210	2 stripe, 1-1/2 x 2 mil emitter	
1211	3 stripe, 1-1/2 x 2 mil emitter	epitaxy $0.5\,\Omega^{cm}$, 6μ
1221	5 stripe, 2-1/2 x 3 mil emitter	epitaxy $0.5\Omega^{cm}$, 6μ
1310	1210	
1311	1211 geo., epitaxy $0.1\Omega^{cm}$, 6μ	
1321	1221 geo., epitaxy $0.1\Omega^{cm}$, 6μ	
1312	3 stripe, 2-3/4 x 3 mil emitter	epitaxy $0.5\Omega^{cm}$, 6μ
1324	5 stripe, 2-1/2 x 3 mil emitter	epitaxy $0.5\Omega^{cm}$, 6μ

0000	5 stripe, 2-3/8 x 1-2/3 mil emitter	non-epitaxy 2Ωcm
0001	5 stripe, 2-3/8 x 1-2/3 mil emitter	epitaxy 0.5Ωcm, 6μ
0002	4 - 1221 geometry 1221 material	
0003		
0006	6 (3 stripe, 1-1/2 x 8 mil emitter	epitaxy 0.5Ωcm - 6μ)

3010	1240 diffusion - some 1240/1243 replacement 4200 diffusion - some 4200 replacement	
3011	1240 diffusion (TRI-1). 0.8 Ω cm, 12μ	$LV_{ceo} > 15$
3012	1240 diffusion (TRI-1) 2Ω cm, 12μ	$LV_{ceo} > 30$
3016	1240 diffusion (TRI-1) 5Ω cm, 12μ	$LV_{ceo} > 30$ V. τ_s <20n)

COMPANY PRIVATE

FAIRCHILD SEMICONDUCTOR DIVISION

Inter-Department Correspondence

To: D. Yost October 19,1962

From: R. Fouquet

Subject: Power Devices

The production schedule for 7000 and 6206 devices published earlier this month will not be met due to serious process problems with the backside pretreat and diffusion steps.

The schedule of 1800 lead welds by 10-28 was based on anticipation of only minor process problems which would be solved concurrently with the production build-up. The backside diffusion step was added to the process when it became apparent that adequate epitaxial material would not be available. The technique of this step had not been developed as part of the original process.

The problem is pipes induced in the device side during the 40-hour backside diffusion. Phosphoric acid attacks the oxide protecting layer of the device side, leaving pits which subsequently diffuse in. Intensive work in the past ten days has reduced the average number of pipes per unit area ten fold, but because these are large area devices, this did not materially raise the yield. Evaluations of improved pretreat and diffusion techniques are in process but at best this is not expected to eliminate these pipes, although significant reductions should result.

An alternate solution is to start with double thickness wafers, diffuse into both sides, lap and polish one side to produce a fresh device side. This is an involved process with problems of its own and would require a month or more to develop it into a production process.

The last and most desirable alternate is the use of epitaxial wafers as originally planned. One-hundred wafers, said to be of the correct thickness and resistivity, were received from Westinghouse today. If these pass evaluation satisfactory we are in business to whatever extent the supply can be assured for the future.

Meanwhile, we are processing all that comes through, both to get the units and to get experience in assembly operations. Yields are low. At best, 100 units per week will be assembled during this period.

R. Fouquet

R. Fouquet, Head
NPN Planar Section

RF/m
cc: C. Sporck ✓
P. Ferguson
W. Richmond
M. Oudewaal
J. Magarian

PRODUCT DEFINITION

1210	2 stripe, 1-1/2 x 2 mil emitter	
1211	3 stripe, 1-1/2 x 2 mil emitter	epitaxy 0.5 Ω^{cm}, 6μ
1221	5 stripe, 2-1/2 x 3 mil emitter	epitaxy 0.5 Ω^{cm}, 6μ
1310	1210	
1311	1211 geo., epitaxy 0.1 Ω^{cm}, 6μ	
1321	1221 geo., epitaxy 0.1 Ω^{cm}, 6μ	
1312	3 stripe, 2-3/4 x 3 mil emitter	epitaxy 0.5 Ω^{cm}, 6μ
1315 1324	5 stripe, 2-1/2 x 3 mil emitter	epitaxy 0.5 Ω^{cm}, 6μ
0000	5 stripe, 2-3/8 x 1-2/3 mil emitter	non-epitaxy 2 Ωcm
0001	5 stripe, 2-3/8 x 1-2/3 mil emitter	epitaxy 0.5 Ωcm, 6μ
0002	4 - 1221 geometry 1221 material	
0003		
0006	6 (3 stripe, 1-1/2 x 8 mil emitter	epitaxy 0.5 Ωcm - 6μ)
3010	1240 diffusion - some 1240/1243 replacement 4200 diffusion - some 4200 replacement	
3011	1240 diffusion (TRI-1). 0.8 Ω cm, 12μ	$LV_{ceo} > 15$
3012	1240 diffusion (TRI-1) 2 Ω cm, 12μ	$LV_{ceo} > 30$
3016	1240 diffusion (TRI-1) 5 Ω cm, 12μ	$LV_{ceo} > 30$ V. τ_s <20n)

I Immediate practical importance

COMPANY PRIVATE

PROJECTS IN PHYSICS SECTION

SUPPORTING RESEARCH

This catagory includes research and development projects which are aimed to improve the understanding of the properties of materials on the characteristics of devices and to improve the yield and extend the present device technology.

I. GOLD IN SILICON:
   1. Solubility: Neutron activation analysis (Flint)
   2. Diffusion: and Segregation on surface of Si-SiO_2 interface, lifetime of carrier in transistors and collector leakage current. (Flint)
   3. Recombination properties in heavily gold doped junctions. (MTS - 1)

II. DETERMINATION OF THE CONCENTRATION AND THE TYPE OF IMPURITIES (MTS -2)
   1. Hall Effect Measurements (Leistiko)
   2. Spin Resonance (MTS -2)

I III. PHOSPHORUS AND OTHER PIPES IN SILICON (Flint - Lawrence - Tucker)
   1. Diffused slice
   2. Effect of oxygen

IV. GETTERING OF JUNCTIONS BY METALS (Tucker - Flint)
   1. Nickel, Au, Cu and other metals
   2. Junction characteristics, avalanche multiplication characteristics
   3. Etch pits before and after gettering
   4. Infrared transmission
   5. Light emission from reversed biased junction
   6. Electron microprobe of impurity concentration after gettering

V. SLOW COOL JUNCTIONS (Tucker - Flint)
   1. Electrical characteristics versus cooling schedule, avalanche multiplication factor
   2. Oxygen by infrared after slow cool after and before gettering
   3. Light Emission

I VI. PYRAMIDS IN EPITAXIAL FILMS (a good first project for Lawrence)
   1. Determine the nature of the pyramids (Lawrence - Flint)
      A. Sectioning, impurity profile, Xtal structure
      B. Diode characteristics of ~~a~~ junctions with pyramids, avalanche multiplication factor.

C. Light emission from reversely biased junctions, photograph
D. Electron microprobe of pyramid
2. Locating the Origin of Pyramids (Wigton + MTS - 3)

VII. GRAIN BOUNDARY AND DISLOCATION
1. Correlation of defects and crystal growth condition

VIII. DIFFUSION DURING EPITAXIAL GROWTH (Roder - Wigton - Sah)
1. Gallium Diffusion to get impurity profile (Roder)
2. Capacitance method to get impurity profile
3. Diffusion mechanism into the epitaxial layer from substrate, diffusion coefficient (Roder - Sah)

IX. GROWTH OF SILICON OXIDE - GROWTH KINETICS (Flint - Reid)
1. In high pressure steam
2. In dried oxygen
3. In wet inert gas
4. Electrical and surface properties of the various oxides

X. IMPURITY SEGREGATION BETWEEN SILICON OXIDE AND SILICON (Roder - Leistiko - Sandor - Sah)
1. Gallium diffusion techniques to get the impurity profile in silicon (Roder)
2. Neutron activation analysis to get the total impurity segregated into the oxide. (Sandor) — One shot to see total in oxide.
3. Out diffusion profile of compensated crystals for FET (Roder - Leistiko)

XI. EPITAXIAL GROWTH KINETICS (Wigton - MTS - 3)
1. Horizontal system (Schulenburg)
2. Vertical system
3. Diffusion Furnace (Schulenburg)

XII. SURFACE DIFFUSION AT Si-SILICON OXIDE INTERFACE (Tucker - Flint)

XIII. COOPERATIVE DIFFUSION

XVI. PHYSICAL PROPERTIES OF MAGNETIC THIN FILMS (MTS - 4 - Sah)

XV. PHYSICAL PROPERTIES OF METAL AND METAL-DIELECTRIC FILMS (MTS - 4 - Sah)

DEVICE RESEARCH & DEVELOPMENTS

This catagory includes all research and development work on devices including both junction and thin film active and passive devices.

I. FIELD EFFECT TRANSISTORS: OPTIMIZING GEOMETRY FROM DESIGN THEORY (Bittmann)

1. Design theory: extended into the saturation region (Sah, Bittmann)
2. Numerical Design and Optimum Impurity Profile (Bittmann)

II. NOISE IN FET (Lauritzen)

1. Measurements (Lauritzen) variables are T, V_G, V_{DS}
2. Theoretical Model and Analysis (Sah, Lauritzen)
3. Equivalent Circuit and Optimum Circuit Design (Lauritzen)

IIa - Thin films

III. SC-FET (Sah)

1. Drift Problem Experimental (Leistiko & Tremere)
2. Drift Problems, Theory (Sah, Tremere, Leistiko)
3. Design Theory of SC-FET (Sah, Tremere)

IV. SURFACE CONTROLLED TETRODE

1. Design Theory
2. Noise

V. TUNNEL EMISSION DEVICES (Saxena)

1. Diode
2. Triode

VI. DESIGN OF INTEGRATED PARAMETRIC FREQUENCY CONVERTER PLUS OSCILLATOR (Bittmann)

VII. P-N JUNCTION INDUCTANCE (MTS - 1 + Sah)

1. Measurements using Wayn-Kerr Bridge into High Level of Forward Bias (MTS - 1)
2. Theory
3. Effect of Heavy gold doping (see also Supporting Research I.3)

VIII. P-N JUNCTION ADAPTIVE ELEMENT (Wanlass + Sah)

1. Lithium Diffusion Technology
2. Capacitance Measurements
3. Memoristor Elements

IX. IMPACT IONIZATION NEGATIVE RESISTANCE DIODE (MTS - 1 + Sah)

1. Fabrication of Devices
2. Extension of Design Theory, small signal r. f. analysis

X. RADIATION DAMAGE IN SILICON TRANSISTORS AND DIODES (Lauritzen & Fitzgerald)

XI. RC THIN FILM NETWORK (Waits & Price)

XII. MOS CAPACITANCE
  1. Silicon-Silicon Oxide (Price)
  2. Other high dielectric constant material (Sandor)

XIII. HIGH RESISTANCE THIN FILM ELEMENTS (Campbell)
  1. Oxide Covered Nichrome Resistance (Waits)
  2. TiO_2-Ti resistors (Sandor, Waits)
  3. Metal-Dielectric Mixture (Sandor)

XIV. THIN FILM INDUCTANCE (Campbell)
  1. Classical Appraches (Campbell)
  2. Others

XV. THIN FILM FET
  1. Silicon (Campbell, Geer) — Make Hall meas.
  2. CdS (Wanlass)

XVI. MAGNETIC THIN FILM MEMORY (Hale + MTS - 4)

XVII. PIEZOELECTRIC INDUCTANCE AND TUNNING ELEMENTS (Campbell)

XVIII. FERROELECTRIC TUNNER (Campbell)

XIX. DISTRIBUTED EFFECTS: ELECTRON-PHONON TRAVELING WAVE TYPE INTERACTION (MTS - 5)

XX. SEMICONDUCTOR PLASMA (MTS - 5)

XXI. GALLIUM ARSENIC DIODES AND TRANSISTORS (Broze)

XXII. APPLICATION OF DISLOCATIONS AND GRAIN BOUNDARY STRUCTURES TO DEVICES (Tucker or MTS -6)

Reddi MTS-1 Ph.D. Solid State Physcist or Electronic Engineer with strong solid state electronics background

Projects:

- S-I.3. Recombination properties in heavily doped junction
- D-VII. P-N junction inductance effect
- D-IX. Impact ionization negative resistance diode

MTS-2 Ph.D. Solid State Physcist with some background in electronics

Projects:

- S-II. Determination of the concentration and the type of impurities using Hall effect and spin resonance
- D-XXIII. Application of Hall effect to devices

MTS-3 M.S. or Ph.D. in Physical Chemistry or Chemical Engineering (Req.Approved)

Projects:

- S-XI. Epitaxial growth kinetics
- S-VI. Origin of pyramids in epitaxial layers

MTS-4 Ph.D. Magnetic Solid State Physicist (Req. Approved)

Projects:

- S-XVI. Physical Properties of magnetic thin films
- S-XV. Physical properties of dielectric and magnetic films
- D-XVI. Magnetic thin film memory

MTS-5 Ph.D. Solid State Physcist or Electronic Engineer with Strong Device Background

Projects:

- D-XIX° Distributed effects: electron-phonon traveling wave interactions
- D-XX. Semiconductor plasma

1963 Product Planning

The trident vs the star:

Star specs are

LV_{CEO}
60 v
40 v
30 v
all large star, no Au

the small trident made with these same ρ epi wipes them out.

Small star
$LV_{CEO} = 30$ v
$\tau_s = 20$ ns, $C_{OB} = 10$v 8 pf $V_{CE} = 0.6 @ 150$
$1.5 @ 500$

Here is trident family layout

Epitaxial

LV_{CEO}	T_1 (1340 dif)	T_2 (4200 dif)	T_2 (1340 dif)
12 - 30	no Au X Au ✓ <10ns 3111	X X	X X
30 - 60	FALL OUT <20ns ✓ 3112	X X	X X
>60	✓ 3016 X	✓ 4016 X	X X
>100			

Non Epitaxial

LV_{CEO}	T_1 (1340)	T_2 (4200)
12-30	X X	X X
30-60	X X	4010 X
>60	X X	4015 X

Status: (as of now)

Priority (need)
0 4010, 4015 in production
4 3111 – hasn't been made. Will replace 1341 except for CTE. (excellent film driver)
1 3112 – made in R&D. Has usual high ρ epi problems.
2 3016 – never made. Suffers bad material problem.
3 4016 – some made on ______ material. Needs material supply.

3112 needs five runs using Peterson material to be ready. This means it will be Nov for card cutting. By then we will deliver to them the extra dice from the 5 runs and wafers for 5B runs of their own.

3016, 4016

Sept. 4, 1962 ROBE

Berliner
(Flint)
Grinich
Hill

Blome
Ferguson
Davis
Tsang
[illegible]
[illegible]
Moore

Discussion of causes of losses in production:

4200

Die Sort		Classification	% (3 lots each)
1. Low Breakdown	41.2, 36.9, 57.4	1. I_{CBO} (25°C)	8.5, 9.1, 6.2
2. Soft	7.5, 11.2, 10.0	2. $BV_{CEO/S}$	2.4 - 4.8 - 3.4
3. EB	1.5 1.7 1.5	3. $LV_{CER/O}$	2.0, 1.2, 4.5
		4. V_{CE} (SAT)	2.5, 2.5, 2.5
		5. Other	

Elect good 24.4, 24.7, 35.8
Vis. rej 2.7-3.1

	1310 (die sort)	1321 (die sort)
Lo Breakdn	36%	32%
BV_{CES} (Rumbling)	64%	16%
low h_{FE}	48%	12%
BV_{EBO} short		12%

Class

	1310	1210	1321	1340
good	~50%	55	55-70 ↓	80%!

Visual:
Incomplete Al pattern 100%
spots
bridging
etc

good ~20% up to 45% or so

There is no major difference in the die sort criteria. (

The 1310 uses big wafers.

At diode check, ~ 20% of all diodes have spots that light up. the other 10% are soft.

Phil Flint will increase emphasis on some of these problems!

The wafers are 1¼" (in theory) actually average ~1 1/32".

Paul Hill wants to start with 4200 diffusion.

For next time:

Paul Hill will review program
will discuss observables to see when process improvement
is being made. These should include checks for
point defects.

Phil Flint will describe the Mtn View type problem
at diode check and compare with our results.

(Sam gave them some $1\frac{3}{16}$ x 3 glass with relatively poor
pattern on them because of soft, scratched glass.)

Staff Meeting – Sept 6, 1962

1. R-element   to Mtn View to do
2. C ICC device   "   "   "   "
3. Patent on flat package?
4. "Photochromic" process? for masks, etc.

Nichrome resistor meeting 9/10/62

Sah　　Lamond
Forman　　Ferguson
Price　　Moore
Waits　　(Campbell - late)
Talbert

Waits: – his technical report
(all cold substrate)

Sheet resistance　~ 0.5% for 100 Ω/□
　　　　　　　　　~ 3% " 200 Ω/□

Run to run　~ 6% for 100 Ω/□ (old-type monitor) - should improve
　　　　　　~ 4% for 200 Ω/□ " " "

Mask variation　1 → 1.15 ± 0.07 in working plates.
　　　　　　　　2 → 2.15 ± 0.07

Alloy cycling　$^{+13\%}_{-15\%}$ on 100 Ω/□　on quartz plate boat 3 min @ 550°C.

$^{-4}_{-39}$ % on 200 Ω/□

It is not known if the change on heat cycle is contacts or the film itself.

Dev Dev: (Dave Talbert)

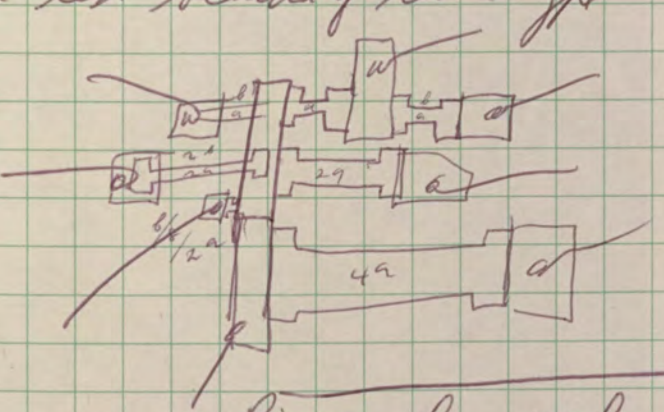
Started ~ Aug 23

± 2-3% on monitor after opening to air over 20 runs.
This is all cold substrate stuff.

They are being made into 1-mil DA resistor patterns.

Bob Martin did hot substrate stuff earlier, but claimed he got no trouble.

A test vehicle of the type



Should be done on reg. resistors and on those on P-diffused substrates.

Pierre has 100 hrs @ 25,000 watts/~~cm~~ inch with no measurable change and an indicated temp of >200°C, probably 400°C.

Also some encouraging 300°C storage.

Meeting 9/11/62 — Microlite, etc

Graham
Schultz
Ferguson
Grinich
Moore

Section Meeting 9/11/62

SoR Camera is still full of bugs. There is too much gain in the feedback loop giving hydraulic hunting (vibration).

The problem of resistors was discussed. We need as much precision as possible. A program will be started to track down the origin of the variations.

—Check next time

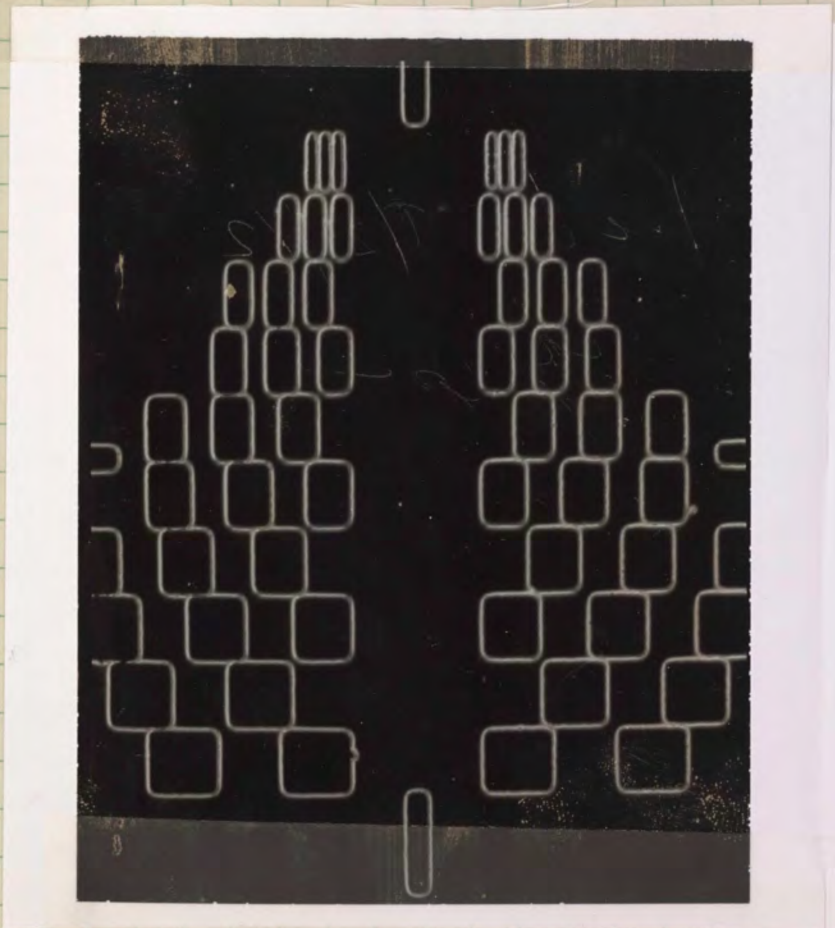
Chromium masks: If these are ok, then Sam would like to try KOR in SoR camera.

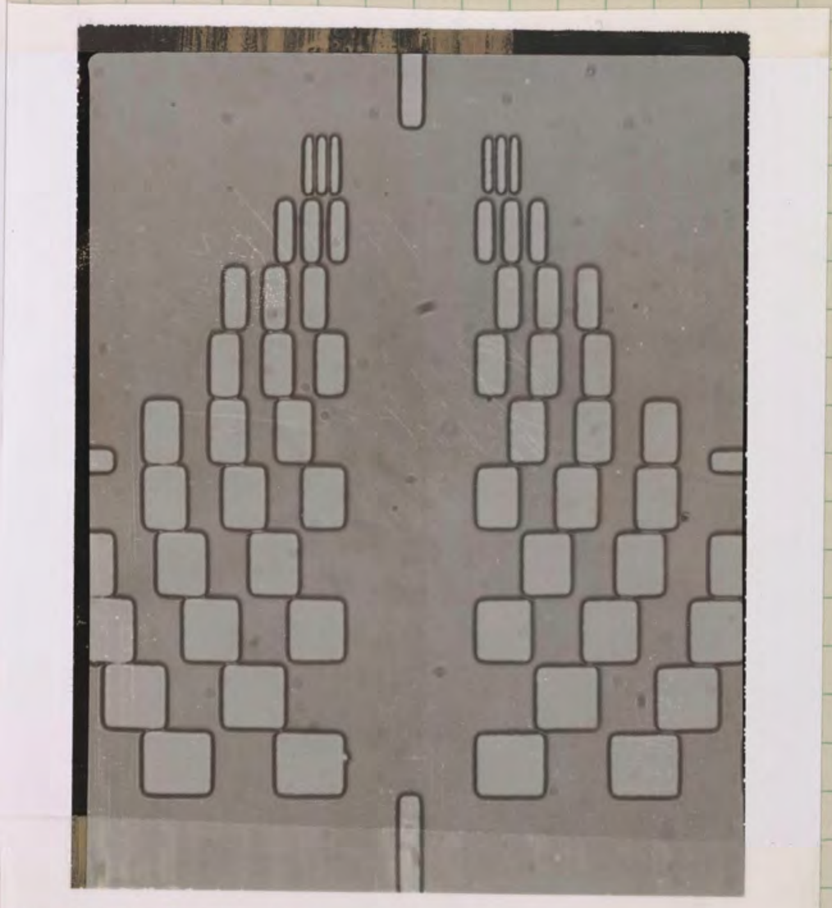
Pictures show that the pyramide still scratch the film badly! It is not really scratching, but rather puncture wounds.

Set up:

1. to try Al_2O_3 substrate for the Cr.
2. Projection printing
3. Point source printing

Chet will dig out old stuff on projection printing.
Sam will try to get the Al_2O_3 plates.





RNN Staff Meeting – 9/12/62

1. Diode has an ADAM reliability problem. – Check this.

2. Can we die-sort to Autonetics (and Nortronics) spec.

3. The FD-1 has lost control of C on FD-1. 600,000 diodes for Nortronics during 4th Quarter is tough on this basis.

Non - regular products 9/12/62

Hafell
Shunick
Moore

Photo devices:
XP-D (The collector-base diode of XP-3) — No schedule
XPDT (To make smaller chips) — " "
FSP-100 The collector-base junction of a 4200 in a TO-5
This should be made in an XP-3 version.
XPS-3 Photoswitch — must be developed.
Lateral photo device (linear type needed) - should combine uses.
The above stuff should be part of a project review — not for schedule

Microtape reader system — in limbo (needs interest) Awaits a surge of public demand.

Electrostatic printing - no work done in last 6 MO - to start again

~~Digital encoder matrix~~ — ~~NSA?~~ - ~~no interest yet~~ — ~~looks like fun~~

Digital encoder matrix (Optical wafer arm)

~~Coder - decod~~ Photo cross point — looks like fun (NSA, etc)
needs μc tape transport to be useful for μc programming.

EDM — We will package a version of it - Needs H.B. + tech back.

DVM — re-Xsfer date Nov 1. Model 2 works or we chop our heads off.

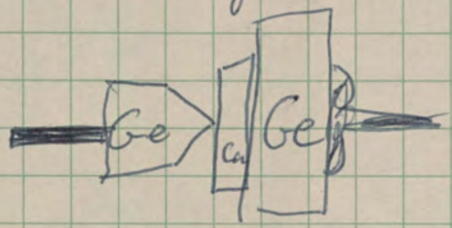
Blocks:
1. Xstor dif amp - 10 made, and offered to Ed, 1 accepted, one to Ed Russel — Xfered - 10 offered, 1 taken.
2. FET operational - (differential input) — 3 done by end of MO. # limited because of parts problems. Oct 1
Russell to make 10.

Revised current source — Ed can do - needs memo
3. 3-stage dif amp — 3 by Oct 31 for E Russel
V→I converter (no special adv., but this is it here)
Std cell replacement
log amp

106 Sept 13, 1962 – Metal based amplifier & tunnel emission device

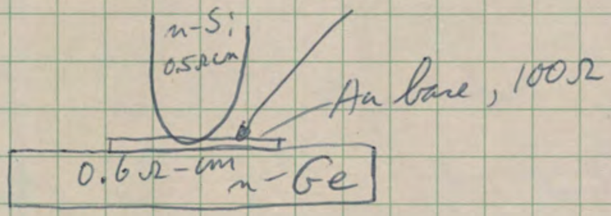
Saxena
Bittman
Sah
Thimil
Moore

Review of device conference structures



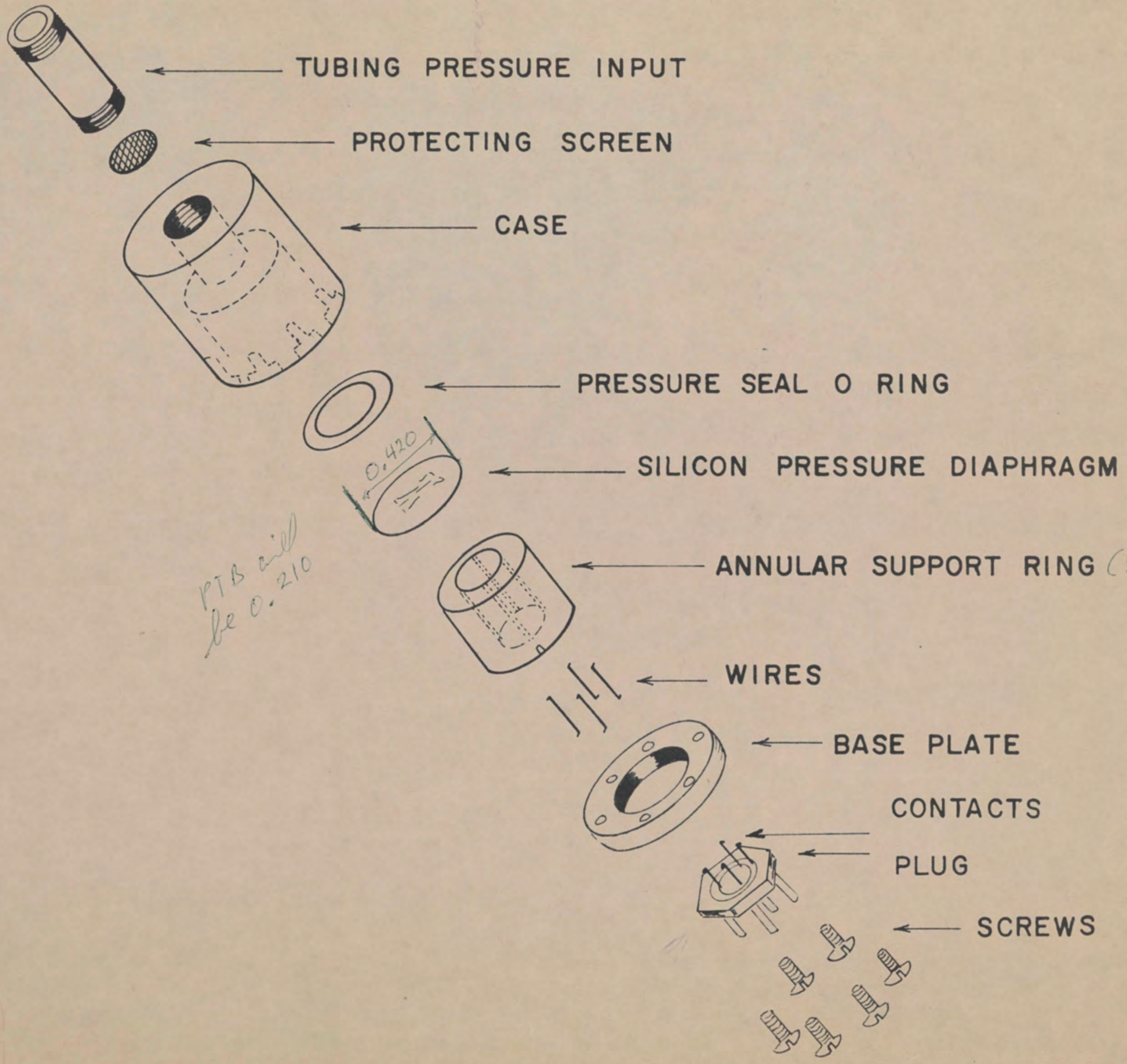
from Geppert @ SRI

Atalla & Kahng (BTL)



α of 0.01-0.4 at I_E ~ 70 ma

This is also a point contact



PTB will be 0.210

Sept 17, 1962 Pressure Xducer Meeting

Bill Bly
Norm Zinsky
Pearson
Grinich
Moore

Two packages as per exploded drawing, one of each sex connector

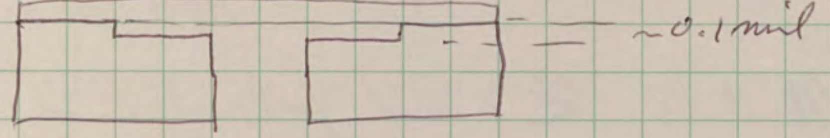
Comparison c̄ 356

	356	PT-A
Range)	0-100 to 0-10,000	0-200 tested, can probably get 0-50 → 0-10,000. For 0-10 psi need ~ 64μ on a 100 mil diameter.

$$q_0 = 6d_2 \left(\frac{\text{radius}}{\text{thickness}}\right)^2$$

Overpressure 300% c̄ out damage / 500% c̄ out rupture   figure on about 300% (can be traded for sensitivity.)

To prevent shock problem, go to

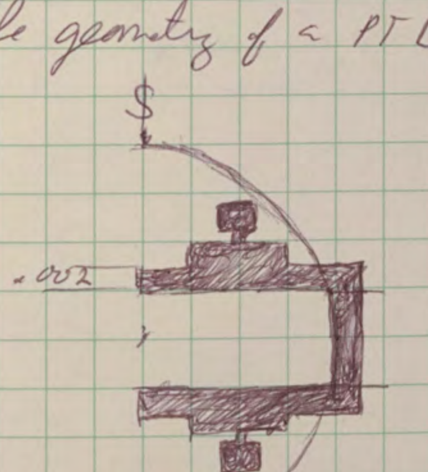


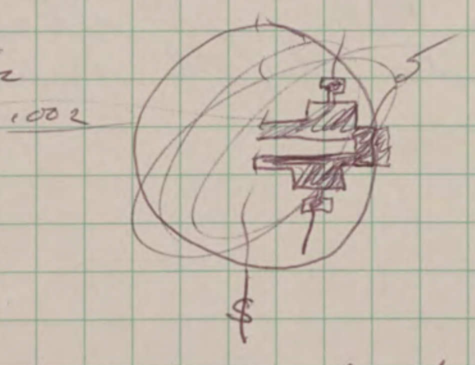
Voltage ~~15 volts~~   15 v (Our tests are at 10 v c̄ no noticeable warm-up time on PTA. PTB is still unknown.)

Output voltage   PTA Measured 250 mv @ 500μ strain + 10 v
PTB (with different pattern)

The PTB has an asymmetric pattern necessary to make max use of the strain pattern. Because of the pattern, the gauge should be non-linear for const voltage, but should be ok for a const current source.

The geometry of a PTB is





∴ get ~ 2× the output, but we will have a 0-point problem.

Hope to get 1 v out c̄ 15 v in and/or 1000μ strain [illegible], inc. 9/17

To me this asymmetry giving a 0-point offset looks sick.

(P)

Input - output impedance

1K on PTB
7-8K on PTA
(350Ω on 356)

This is too high for ordinary sleep recorders without a buffered output. But, because of T dependence on impedance, not worth trying to level.

Sensitivity — 356 is within 2% of nominal - using a knob.

On the raw diaphragm assembly we can hope for ±20%?.

~~Zero~~ balance - PTA - 400 ± 30 mv

Must be $\lesssim$ 3% of full scale - it is for 356?

Linearity + hysteresis

linearity of -0.2% on sample 1
-0.4% " " 2

These are total mid-range deviations. They represent 2 units with polished diaphragms, but are not selected.

Thermal hysteresis is great

→ Zero shift, however, is not ~~so great~~ good (~0.1%/°F, or an order of magnitude > 356 and too bad.

On PTA-sized shear gages this was greatly improved — down to the necessary requirements.

Xducer, con't 9/17

In summary:

device	limitation
1. PTB - epoxy mounted ©	needs current source © thermal zero-shift 1K output impedance
2. 1+ electronic package	
A. Current source & resistor + emitter follower stage	— 3 diddle points
B. " " + Hilbert current out.	" " "
3. Flush diaphragm c̄ shear — stupid - low output. LOH?	
4. Shear gauge c̄ electronic	— 1 " " only

Rough cost estimates:

	My pocket exp. over
PTB Diaphragm, 7 possible, 50% divider, = 3.5/wafer @ $20/wafer =	$7 each
Diaphragm mount (assume prime material) = 100/xtal + labor	$3 each
Machined mech. parts Case @ 45 min/unit weight = (w/small quantity est ×2)	$7 ($14)
Connector (Hermetic)	2½
O-ring	½
Mating connector	1½
Bonding and other assembly 15 min	$2
Test - 1 hr	$8
	$31

Electronics look near the op. amp costs ——— ~$50

Micrologic production review: 9/17/62

Blough
Yost
Schultz
Farina

Seeds
Ferguson
Grinich
Moore

Adgenda:

1. Review of present production (& sales) situation
2. Present problem
3. 1st results on new masks
4. Action Items
    - a) new structures?
    - b) base V/I
    - c) scheduled throughput.

1. Making μL + kits
Run ~3,000 F.S./week
Increase to ~10K by end of Nov.
5-6K by end of this month

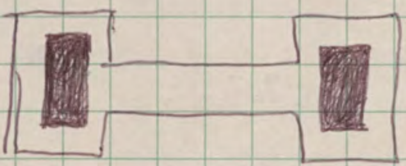
Class yield looks like ~50% to total A+B (~½ ∘ ½).

2. a) Material quantity supply has about cleared up - using Futurecraft material. Using ~1" wafers. ~~Only~~ Get a lot of reject upon etching.
For 10K scale need 3K wafers

b) Isolation run ~60% yield for a large number of causes.

c) Base predep. varies depending on element. New masks should all be done someday. Only S's have been made, G mask is done. All new masks will be in this week and out in ~3 weeks.
The new masks have all bottle Xstors, all same R's.

All but the S & G will have dog bone resistors.



They are using 150Ω/□ (as near as can be measured?)

d) Bad mask alignment at emitter oxide removal - To be removed by new masks.

(We get ~ 10 good "S" dice per starting wafer)

9/17/62 – μL, cont

e) Metallization – The metal etch is a one wafer at a time operation with very critical control. (Due to life on the leaving edge of lifting).

f) Wafer check after alloy for R_c lead resistor and β. At this time we loose ~50%. The 1340 spread is at least as large, however. "Just" a process control problem

g) Die sort
Tough correlation problem
probes tough

Gates – 25% now, a lot is bad mark of 175 possible
~~&~~ S, C – 10% " 130 "

Major loss of yield is a general shorting
another is that optical rejects for bad metal are widespread.
The bad metal is because damage, breaks, lifting.

h) About 80% come thru assembly and the subsequent optical inspection. The major loss is metal off. This can improved by ion bombardment at metallization.

i) Classification – Major problem is strongly man-oriented.

Metal protection schemes can help a factor of 2.

1. Anodization: Metallize, etch, completely metallize, protect $\bar{c}$ KPR the pads, anodize the 2nd Al layer completely.

2. Glass spraying – tried tomorrow
S; O evaporation –

3. We are still checking on the Chromium.

There is a serious problem on the punch-through for kit components.

112 μL, cont.

Production forecast, μL only

	N	D	J	F	M	A	M	J	J	A	S
Forecast (in 000)	3.5	4.0	7.0	12.0	7.0	11.0	8.0	10.0	12.0	14.5	16.0
but, in most likely Possible (in 000)	8.5	7.5	13.5	19.5	14.0	19.2	13.0	10.5	19.0	15.0	24.5

Est split	B	C	F	G	H	S&S,
	5%	15%	2%	18%	20%	40%

This does not include any special ckts on DPW

3. New masks
- Intent: To add design tolerance for
  - a) Additional mask. tolerance
  - b) Improved yield

I.e., to convert B's to A's and give noise immunity.

Uses K-2 which was thought to be lower in V_{CE} than μL's.

The kit IC components gave headroom as advertised.

The integrated units using 100 Ω/□ base instead of 150 Ω/□, however, had

1. Higher $V_{CE}(sat)$ at 125° than μL
2. 70 mv lower V_{BE}

The design changes suggested by C.P.'s experiment will be compared with Farina & Ferguson this week. This will result in the design of new masks to be made at Mtn View and run at Palo Alto.

GENERAL PHASES

I. Maximum potential from present equipment and dopant systems.

II. Modifications to equipment and procedures.

III. Innovations in equipment, dopants, and procedures.

OBJECTIVES:

1. Consistantly repeatable V/I level and range.
2. Minimize operator influence on diffusion processing.
3. Prepare processes with fewest steps, simplist equipment operation, and install best general diffusion practices in all diffusion areas.

PHASE I - Improve operating procedure on present processes.

List of critical operations in diffusion.

a. Temperature control.
b. Optimum predepositions of specific dopant sources.
c. Cleaning and cleanliness (wafers and area)
d. Diffusion parameter measurements and controls (correlations to beta levels, etc)

DETAILED PHASE I

1. Temperature Control (review already known work, and start implementation).

   a. Maintenance of furnace control mechanism.
      i.e., qualified technicians, written adjustment procedure, periodic control tuning such as controller response, damping, overshoot and the like.

   b. Thermocouple calibration and control procedure
      i.e. range of calibration validity, length and fabrication of thermocouples.

   c. Profile procedure, frequency, and determination of usable zone

   d. Tube and jungle cleaning and replacement
      i.e. low temperature washing and high temperature tube changing procedure and frequency, teflon joints and tight values, etc.

   e. Boats, pull rods, thermocouple sheeths, tweezers, and handling equipment useage.
      i.e. best usage, cleanliness, etc.

If diffusion control and analysis of losses in diffusion

1. Electrical; V/I average, range, selection of test points, method of recording, etc,

2. Diode; test conditions, reject levels, classification of defects, etc.

3. Mechanical; prevention of wafer handling breakage, etc.
4. Test 70 or equivalent electrical test; selection of parameters and their test conditions for maximum diffusion control, correlation between major losses and diffusion operations, realistic reject limits.

DETAILS OF PHASE II

Sept 18, 1962 - ROBE

Baldwin
Roder
Sandy
Hill
Engall

Fole
Bloom
Feynman
Moore

Hill on old business

Masking:

(1) Hard Chrome

2. Resolution c̄ small geometry, thick coating

1210 emitter can be done now on thick KPR by control of exposure. Paul is convinced that this can go into production.

Masks:

The edges are wavy on the ones we gave them, ∴ 4200 people have not tried them. Our new ones are much cleaner, but they have a little more pinhole problem.

Sam would like 2x2 if possible.

→ We will do some current 1210 structures. By then we will have data on pattern size, etc.

The 4200 & 4500 are using the ~~[illegible]~~ new masking technique with good results — like 48-50% die sort on the first couple of runs to come through. No lifting!!

The program: See outline.

Pinhole checks have been stopped on regular twice-daily basis. They will run still on ~~the~~ a 2X weekly basis.

Next meeting in 2 weeks.

$\frac{2}{20}$ $\frac{1.74}{1.5}$ $\frac{1.3}{1.1}$ 3. 2

1.8 ~ 10

Spork
Berliner
Forgan
Hans Paulson
Jean Le Galle
Brown
Bisalet

Diode review: 9/19/62

Start Jan 15

March got 1000 good FD-700

Made a couple of ~~one~~ good lot here

by Middle of May it went dead!

C. Parker spent a few days here

went to 4½ min epitaxial, still no FD-7

Typical now now — original

7-15 v	~>20
1.2-1.5 pf	< 0.8

Using everyone material, now only a small scattering (total 3-wafers) that gave good stuff. This was Peterson material.

They are still fat on forward.

The mask is now $1\frac{1}{4} \times 1\frac{1}{4}$ with a $(0.8)^2$ cut.
This has confirmed that C's are still ok.
Normal process aims at 16 min with A and B diffusion.
The good ones we made were long diffusions, but all the long ones aren't good.
This is a ~15 Ω V/I B diffusion

Action:

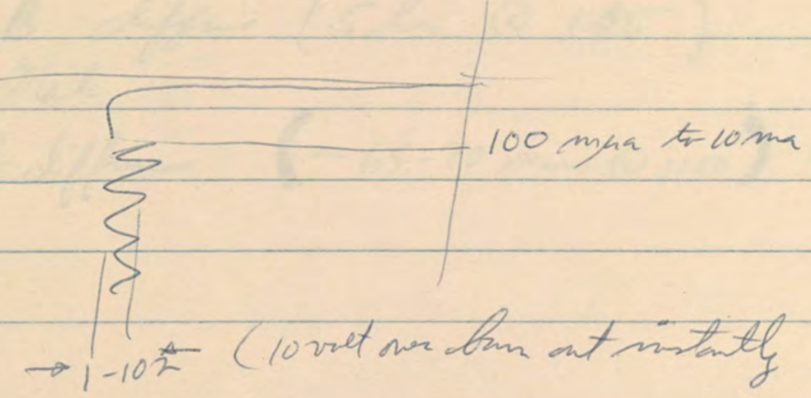
1. Make 20 mil masks!!
2. Jean will come to R+D to work c̄ b. Parker to establish
   - a). That we can still make it
   - b) A supply of good material.
3. R+D will make runs until its going back up here.
4. Assembly at S.R.

FD-6

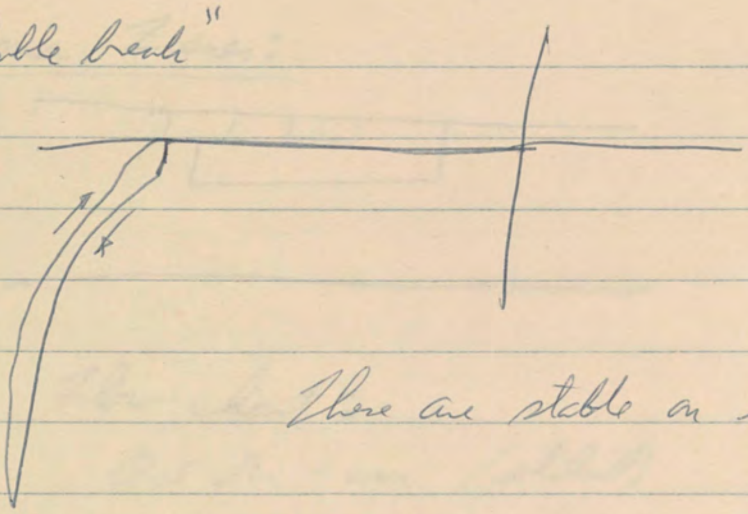
Getting ~ 30-40 75 v units / starting wafer
100-125 "saleable" units / " "

Problems that are seen:

Oscillations: ~30% of the units do this, especially high volt.



"Double break"



These are stable on life, however.

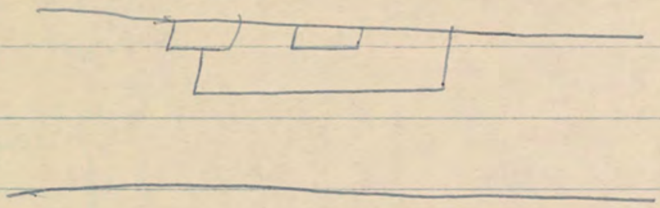
The FD-6 has reliability problems. I_R + V_f.
They look sick at > 150°.

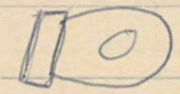
The I_R problem looks like soft.

Zener (100μ amps)

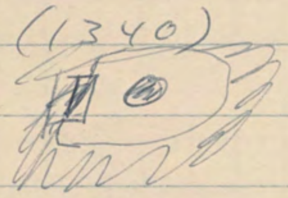
~~Ox (like FD-1)~~
1. P-diffuse a lapped - ~~polished~~ sawed wafer
2. Polish the sawed side (to ~125μ)
3. Ox
4. Mask
5. B diffuse (5 hr @ 1145)
6. Mask
7. P-diffuse (~65-70 mins @ 1100) (Use only the phosphorus gettering)
8.

7.5 ma Zener:





Flow chart:
0.5 Ω-cm (etched)
Ox
Mask
Base diffn (1340) (std tempg)
Mask



Emitter dif. & plan - dot
Oxide removal

Ni in R&D — Ray
worried abt the reliability

S.R. has serious doubts on the ability to assemble Ni'ed units. This relates to their very bad FO-3 experience.

Dice Oct 15
Proven 1 Nov. — Ni if no contrary data

Xsfer meeting on the U-2 — Sept 25, 1962

Yost
Grinich
JRF
Schutz
Lamond
Shidley
Kabell
Santen
Rogel
Baiger
Knudsen

U-1: 5-run started @ Mtn View (total ~45 wafers)
Made 1 wafer c̄ 10% device yield — very noisy

The 3, 4 & 5th are at die sort (~30%) no data

Our runs have averaged 40%

Their runs have not been double masked. We feel that double masking is important.

Their process has deviated in many, many respects from what we have done in R&D.

They get 6700 good die. Yet only 40-70% ~~overall~~ class yield.
(The Al was not easy to bond to & a lot were opens.

Meeting on the Autometer Sept 26

And again on Oct 1.

Shaul
Hane
Schultz
Ferguson
Farrin
Trotter

Oct 27

We can eliminate speed-up capacitors

Down to ~ 175 points – still needs two small C's. which are included in the point count.

It was breadboarded and worked

Take exception to breakdown voltages.

Oct 2, 1962 – <u>Section Meeting</u>   Everybody but Chet:

The 10 pos. discrete is tilting.

The growing exp is not yet started.

Plastic-coated masks for epitaxial pyramids: We have found one lacquer that works fine. c̄ a ½ – 1 mil coating.

Applied by dip & drain

Art is writing some stuff down for tech repts.

ROBE Oct 2, 1962

Sang JPF
Hill BLOME
Moore FOK

The Cr masks provided last time still have not gotten results. It was decided that only 10 experimental runs would be tried. Paul Hill thinks that most (or at least many) of these were lost by a general KPR scum problem.

Sang on opt. dif.

$(CH_3O)_3B$ is going into production

µL – all over
4200 – setting up, ovens in 1 or 2 wks
4500 = " " , 2 weeks
S.G. –

By next time P.H. will have an implementation schedule so that we can convert over up here.

We'd have a steam controller to control T

Chromium masks:

We can hold etching to a greater extent (± .04 mils)

We supplied ~~two sets~~ a set of masks (Cr) c excellent resolution;

56-800

Project review, Oct 4, 1962 - Epitaxial

Roder
Schlesberg
Wrigton
Sah
Yain

Roder on the profiling:

Still the spikes at the surface

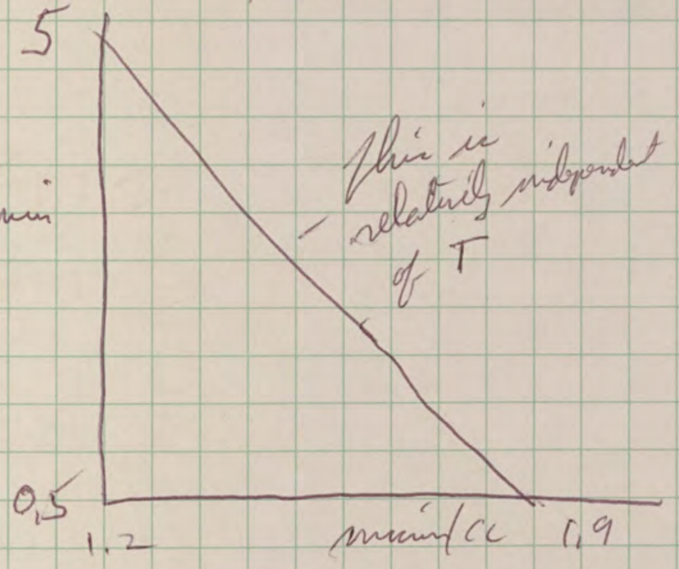
We will do a curve fitting job on some of the profiles to evaluate t_f and $\sqrt{Dt}$. These will be compared with

t_f from sectioning and from stacking faults

$\sqrt{Dt}$ from t-T cycle.

Wrigton on growth rate.

T (corrected)	Max growth rate ΔH ~ 200 kcal	D (for As) ΔH ~ 38 kcal
1230	1.33 μ/min	0.45
1265	6 μ/min	0.6



This was on a 1-tier unit.

We are going to need hydrogen purification capacity, ~$13,000

We will do the symmetry experiment to check a gas phase transport.

We will check growth rate vs hole size.

We will go back and get a low dislocation count xtal and look again at the perfection.

Hank says our materials people are growing @ 6"/hr, which is way above the 2½ generally accepted as max for low dislocation density.

Ge continued 10/5/62.

Surface prep.

We do much better on our mech. polished than on our chem pol. On the Westinghouse wafer we got only 3 pyramids. Washed c̄ TCE, acetone and D.I. water.

October 5, 1962

PROJECT 172 - ADVANCED MICROCIRCUITRY TECHNOLOGY - J. Campbell

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PROJECT OBJECTIVES

1. Resistor Technology

   Development of a resistor technology capable of producing resistors within four major categories

   Done

   A. Resistivity 30-300 Ω/sq, minimim line width 1 mil, TCR ~ 200 ppm/°C, ± 5% tolerance

   B. Same as (A) but tolerance better than 1%, may be individually adjusted

   ~1-10 kΩ/□, 1 mil line width, ±10% or so

   C. $\geq$ 100 KΩ in 100 mil square, TCR < 5000 ppm/°C, tolerance ± factor of 2.

   D. ≃ 10 KΩ/sq or 1 meg in 100 mil square, TCR low as possible, ± 10% tolerance. To be used by Special Products

2. Capacitor Technology

   Development of a capacitor technology capable of producing capacitors having a figure of merit of $6 \frac{\mu fd\ V}{cm^2}$, corresponding to 4 pf/mil^2 for a rating of 10 volts. Tolerance should be ± 5% for the 100 pf size.

   This is about the limit of the materials. For the higher ε materials, the B.V. fields are lower.

3. Large Integrated Devices

   Development of an array of diodes, each having a forward equivalent resistance less than 20 ohms at 1 ma current and having a reverse breakdown greater than 20 volts. The diodes are to be connected in a criss-cross array, and provision is to be made to change the number of active diodes electrically after construction of the matrix. In a variation of this a decimal-binary converter having permanent connections is to be constructed.

4. Evaporated Field-Effect Devices -

   Development of a field-effect device having all components, including the active regions, formed by the evaporation of material onto an appropriate substrate.

5. Way-Out Devices

   A. Tuned Circuits

   Development of an integrated device capable of having a tuned response with an equivalent Q of at least 50. Such a device should have a stability comparable with existing LC circuits. An arbitrary test vehicle will be construction, in part, of a 60 mc IF strip.

   B. Integrator

   Development of a device capable of integrating an input signal with a time constant of a least several hours.

PROPOSALS FOR CONTINUED PROJECTS

1. Resistor Technology

A. Metal Film (R. Waits)

At present there is a large run-to-run variation in the values of nichrome resistors (100 - 200 Ω/sq). Within a single run 65-90% of the resistors are within ± 5% of the run average, but over a series of nine runs only 33-43% were within ± 5% of the over-all average. The variation in sheet resistance from run to run is 4 to 6%; within a single run the sheet resistance varies from 0.5 to 3%. Alloying for 3 minutes at 550°C causes a large variable change in resistance; + 13.5 to -15.1% for 100 Ω/sq resistors and -5 to -39% for 200 Ω/sq resistors.

The effect of 200° and 300°C storage is being evaluated for 200 resistor arrays (~ 500 resistors) and 150 single resistors.

Thin nichrome films that have been protected with silicon monoxide show promise as resistors in the 1 - 5 kΩ/sq range. The maximum TCR of 2 KΩ/sq resistors is -190 ppm/°C in the range 30° - 100°C. From 100°-300°C the TCR is less than 80 ppm/°C. It is proposed that the study of metal film resistors be continued with the aims of

a. producing stable resistors in the range 2-10 KΩ/sq and
b. improving the stability and life of nichrome resistors in the range 100-200 Ω/sq.

Other possible metallic films, such as evanohm, tantalum, or rhenium will be investigated as time permits.

Studies of these films must be made to show complete compatibility with respect to present device fabircation techniques.
In addition, further work needs to be done on individual adjustment to fulfill the needs of part 1b of the objectives.

B. Oxide Film (H. Geer and J. Campbell)

Little work has been done on this project during this period because of the discouranging results obtained with previous methods of deposition. Recent results with reactively sputtered films of tin oxide have been more promising; films of about 8000 Ω/sq being being produced in approximately 15 minutes of sputtering time. The resistivity of the film is ~ 10^{-1} Ωcm, the TCR is -10^4 ppm/°C over the range 30° to 100°C. Uniformity is approximately 20% over a 4" diameter area within the deposition apparatus; run-to-run reproducibility appears to be in the range ±20%. Note that here, as in the metal films, the possibility exists of monitoring the resistivity during the run. If developed, this technique should fulfil part 1c of the objectives.

Can eliminate for now

C. Resistor Compositions (J. Price)

a. Silk-Screen Techniques

Using KMER techniques, line patterns 7 mil wide and up have been successfully applied to the 400 mask stainless steel wire screen. Ink printings tended to spread out wider than the KMER pattern, giving minium line widths of 12 mils. Film resistivities have been recorded up to 30 KΩ/sq. The best control of print thickness which can be expected with screen printing is 10 - 15%. Also, precision registration with the screen printer is difficult.

b. Alternative Printing Techniques

A printing method has been tried which uses selectively etched copper (electroplated onto alumina) as the mask for the ink. It was hoped to improve pattern resolution with this technque, but so far, due to several pronlems, results have been negative. Another technique, using SiO as a mask, and etching the ink film in CP-6 was tried, without success.

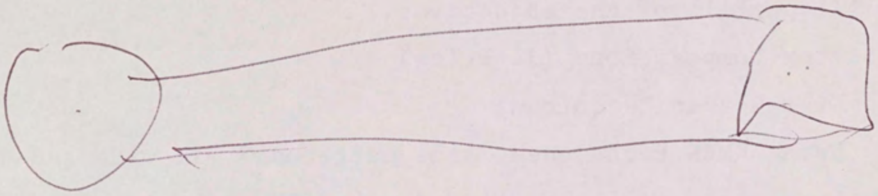
This technique should fulfill part 1d of the objectives.

D. Cermets -(J. Campbell)

In order to obtain surface resistivities in the range of 10^4 Ω/sq thickness (~ 200 Å), it is necessary that the resistance material have a minimum resistivity of 2.10^{-2} Ω-cm, neglecting edge-scattering effects. This immediately rules out all metals, and we are left with semiconducting materials or metal-dielectric mixtures. Of the latter, the chromium - silicon monoxide system offers a possibility. It is proposed that this and similar systems be explored for their possible value toward fulfillment of part 1c of the objectives.

E. Tantalum Nitride

Gerstenberg has shown that sputtered tantalum nitride has a resistivity of about $2.5.10^{-4}$ Ω-cm. While this is somewhat lower



$$R = \rho \frac{\cancel{10}\,10^{-5}}{(10^{-4})^2} = \rho \times 10^{3}$$

$$\overset{100}{\boxed{10\,\Omega}}$$

than is desirable (for 10^4 Ω/sq, t = 2.5 Å) the film still has the desirable property of low TCR. It is proposed that the properties of this film be investigated as time and equipment permits.

2. Capacitor Technology - J. Price

Thus far, MOS techniques have been used exclusively for capacitors. Dielectrics have been formed both by thermal oxidation and by anodic oxidation of the silicon. Until recently very little success was achieved with thermal oxidation, the oxide shorting out at very low voltages, despite the various cleaning methods and photoresist techniques which were tried.

1000-1100Å

600 sq mil

However, the latest run using thermal oxidation was far more successful, with over 80% non-shorted capacitors, and typical oxide breakdown at 80 volts [illegible] ($\sim 8.10^6$ v/cm). This improvement may be due to better starting material. XXXX Within this run, 90% of all units were within 5% of the median.

A number of anodic oxide capacitors have been canned and lift-tested. Unloaded capacitors showed no drift after 500 hours at 300°C, but with 20 volts applied bias, at 300°C, all shorted in under 50 hours. These units were not hermetically sealed. Further testing will be done on fully sealed units.

It is to be noted that with present SiO_2 techniques we can expect capacitor figures of merit of about 4 $\frac{\mu fd\ v}{cm^2}$, while going to other dielectrics such as TiO_2 would yield figures of merits at most of about 6 μfd v/cm^2, assuming a rating of 50% of breakdown. These figures are about at the project objective (±x2) and it appears we have reached a fundamental limitation in technology. (J. Price)

3. Large Integrated Devices

A. Diode Matrix - (J. Price)

8x8

Work on this project was held up until recently due to the unavailability of methyl borate furnaces. Individual isolation yield figures should give an overall matrix yield of about 75%. Thin Alumnium fuses which have fusing currents around 1A show no change after 100 hours storage at 250°C.

Breakdown voltage of both isolation and diodes is typically 150 volts in 8 Ω cm bulk silicon.

B. Binary - Decimal Converter

This device has 40 diodes, with 8 inputs and 10 outputs, on a 125 x 75 mil dia. First runs showed unwanted transistor action in the NPN structure, which can cause incorrect logical operation, but with heavy gold doping, electron injection into the collector region can be reduced to a negligible level. For the high voltage converter, means of achieving deep, high resistivity p-layers are being inevestigated. A radial, 18 lead metal preform is being made, to be bonded directly to the Aluminum pads and mounted in a flat circular package.

4. Evaporated Field Effect Devices - (H. Geer)

To date gains of 100 μ mhos have been achieved with this device operating in the enhacement mode. The devices have been fabricated on sapphire substrates and have a silicon film thickness of about 1 micron. Pyrolytic oxide (~ 2000 Å) is used as gate insulation, giving breakdowns greater than 200 v and a d. c. input impedance greater than 10^{14} ohms. Gate leakage has been eliminated as a source of transconductance in the latest runs. The pinch-off voltage of the device appears to be equal to the applied bias. Biases of 45 volts having the same polarity as the drain were necessary to obtain appreciable gain. Drift of source-to-drain current overnight with ~~22½~~ 45v volts applied to the gate were about ~~4%~~ 40%

A new mask offering improved geometry is being made for this device.

5. Way-Out Devices

A. Tuned Circuit

It is proposed that studies and simple experiments be done toward solution of the problem of the integration of tuned circuit elements with our present microcircuitry efforts.

B. Integrator

It is proposed that studies and simple experiments be done toward the production of a device which will perform an integration. This will be used both for more conventional circuits as well as for adaptive circuitry.

C. Field Emission Triode

It is proposed that studies and simple experiments be made toward production of a three-terminal divce utilizing field emission into a vacuum.

PROJECT 172

PROJECT SCHEDULES

1. <u>Resistor Technology</u>
    - A. Metal Films
        - Completion of 1000 hr life tests (12/1/62)
        - Initial Studies of Ultra-thin films (1/1/63)
        - Accelerated life & power-life studies of standard NiCr (1/1/63)
        - Initial studies of Re films (2/1/63)
    - B. Oxide Films
        - Reproducibility and TCR studies (11/15/62)
        - Accelerated life tests (2/1/63)
    - C. Resistor Compositions
        - Reproducibility and TCR studies (1/1/63)
    - D. Cermets
        - Deposition studies (12/15/62)
    - E. Tantalum Nitride (1/1/63)
2. <u>Capacitor Technology</u>
    - A. MOS capacitors
        - RC Network-accelerated life tests (1/1/63)
        - (This must compare thermally with anodically grown oxide)
    - B. Evaporated Oxide
        - Initial studies (11/1/62)
3. <u>Large Integrated Devices</u>
    - A. Diode Matrix
        - Package development (12/15/62)
        - Accelerated life test (2/15/63)
    - B. Binary-Decimal Converter
        - Package development (11/15/62)
        - Accelerated life tests (1/15/63)
4. <u>Evaporated Field-Effect Devices</u>
    - A. Parameter study (1/1/63)
    - B. Packaging (1/1/63)
    - C. Accelerated life tests (3/1/63)
5. Way-Out Devices
    - A. Tuned Circuit (indef)
    - B. Integrator (indef)
    - C. Field Emission Triode - Feasibility study (1/1/63)

MANPOWER REQUIREMENTS (6 months)

		R. Waits	1000 hours
J. Campbell	800 hours	H. Geer	1000 hours
J. Price	1000 hours	O. Uyeda	1000 hours

Technician (to be hired)	800 hours
Assembler (to be hired)	900 hours

EQUIPMENT REQUIREMENTS

Modifications to sputtering jig	$350
Constant-Current Network	$300
High-Temperature Oven	1200
Capacitance Bridge	1150
Switch for Delta Oven	~ 900

Project 172

Oct 5, 1962 - Project Review, Thin film

Price
Warden
Waits
Campbell
Sah

Grey

Oxide, BV ~ thickness is 10^7 v/cm from 500 - 2-5000 Å.

Resistors:

At 200°C largest change was 0.5% except for one that was 20%

At 300°C changes were erratic 3~4%, 10% in worst cases. After 200 hrs ~10% bonds failed.

We don't know what the variations are - if its contacts or if its the film. Waits will find out.

For the thin ones, there is a large change during aging. In all cases it comes out 1.5-2.5 K/□.

For other films, Rhenium. Re looks very good.

On the high resistors we have several schemes:

a) thin Ni+Cr under SiO_x
b) SnO_2
c) Cermet ($Cr + SiO_x$)
d) Saffley's $Al + SiO_2$

Cl_2

John Price's yield corresponds to ~20 p.h./cm² - after an oxide etch.

Further out, can we use the third dimension.

Price will see that the Cl_2 etch is tried.

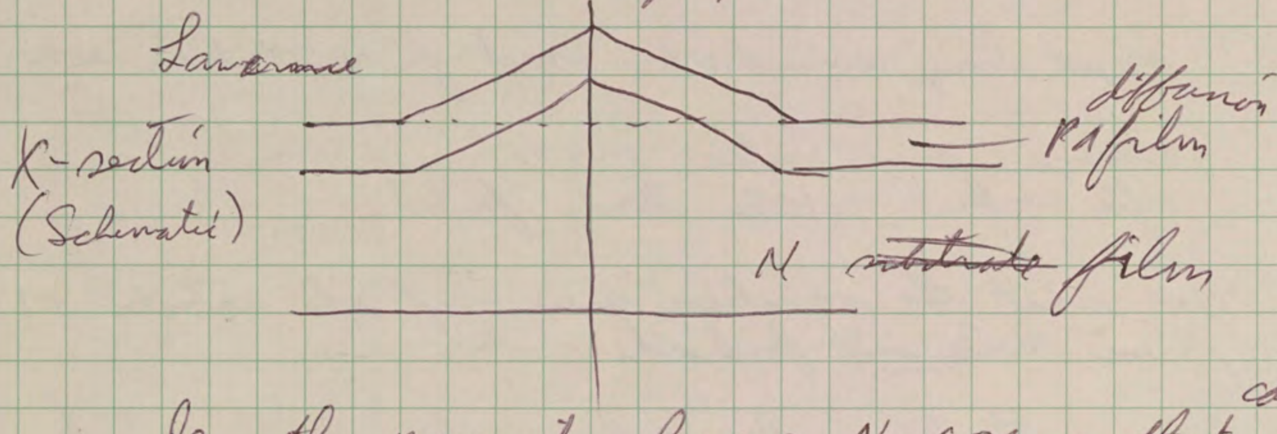
On diode arrays, the back-to-back diode technique hasn't worked as well. We will package some of these

Oct 8, 1962 Project Pyer, etc

Lawrance Wigton
Tasker
Soly
Flint

1. Pyramids:

Summary: Seem to be twinning,
Originate at substrate
Make soft junction, but not L.B.



Ie; the pyramids have a N-core that ^can^ extends [illegible] above the surface of the film.

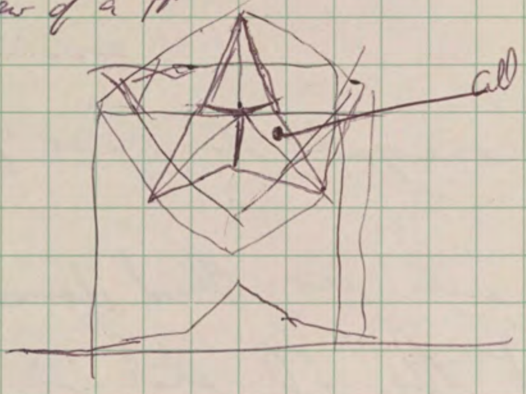
The first type pyramid is the uniaxial tricrystal (20%)

Mesa diodes were soft when a pyramid was included, those without were not. The avalanche B.D. ~ the same

Mesas which cut a P in half were always short.

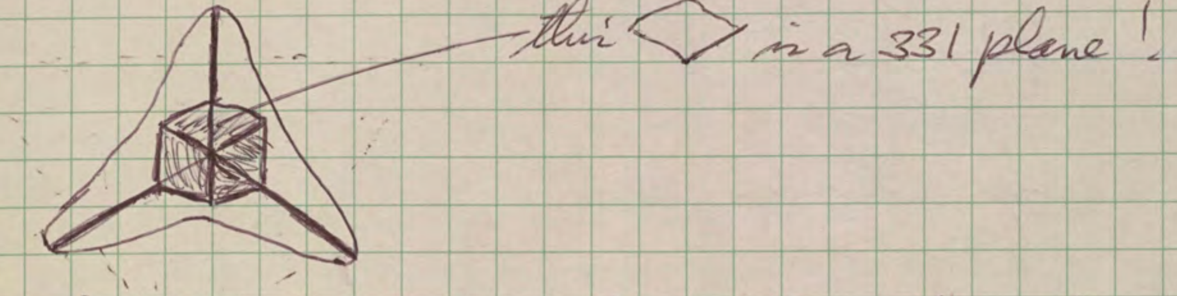
The low, flat-topped features, equilateral Δ's, also cause the same problem.

The top view of a P

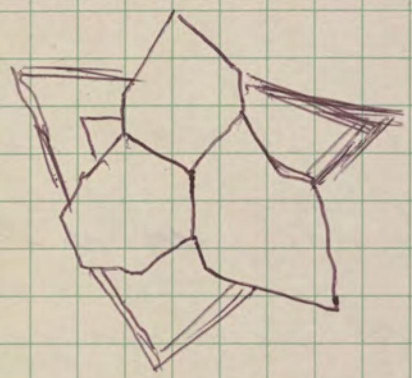


all of these are eq. to 110 planes

Some Ᵽ's have a depressed center — triaxial triangular (80% are multiaxial)

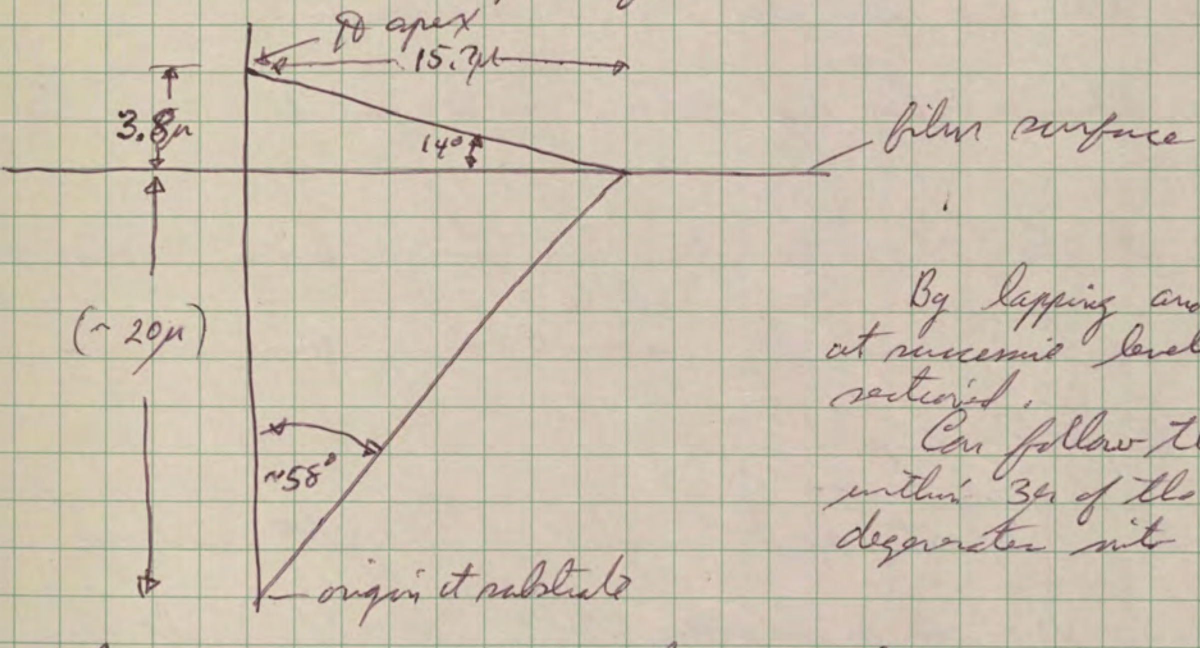


These Ᵽ's can be followed clear down to the substrate. After pitting etch of ground into film Ᵽ, get a trace



The trace gets smaller c̄ depth and vanishes at the boundary.

Now consider the origin of Ᵽ's —



By lapping and staining (or pitting) at successive levels this has been sectioned.

Can follow the Ᵽ geometry to within 3μ of the bottom, then it degenerates into an etch pit.

For many cases the Ᵽ stops at the substrate — no continuing of the pit. i.e. No correlation of the Ᵽ c̄ substrate defects (that etch)

From the above geometry, $t_f \cong 3.65\, h_{Ᵽ}$, where $h_{Ᵽ}$ is the peak height of the Ᵽ, no matter how many peaks.

Everything we know & have done is consistent with the postulate that Ᵽ are caused by surface defects on the substrate.

Plans:

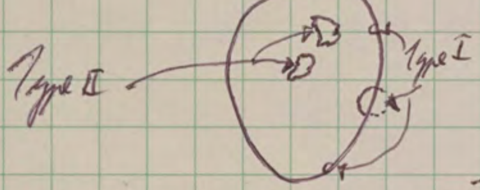
Light emission from junction
Cu decoration

We will write up what we know now as a tech rept.

Work will aim at
1. What are causes
2. Can we tie together a reasonable publication.

Other defects — Pipe problems

Summary of production defect problems:



At base diffusion we get pipes on the edge

We have always seen these. They are points of low breakdown.

Flint thinks these are there on nearly all structures.

Now, in addition, they are getting pipes in the middle of the structure.

The ones at the edge are sensitive to cleaning before predep.

Pipe incidence has always been ~~substrate~~ bulk doping sensitive.

Flint suspects the predep. step.

He will present a report next Tuesday at the ROBE meeting

After base diffusion the run on the average 80% (60-90%). It seems to have a run correlation.

From what Flint says, we should consider trying an etch after opening the window. This would be a good experiment.

GEM - Master copy

NEW PRODUCT FORECAST FOR 1963

MICROCIRCUITRY:

Device & Description	New Technology	Major Equipment	Transfer Target Dates									
			N	D	J	F	M	A	M	J	3Qtr.	4Qtr.
1. Integrated Ckt. Component junction capacitor	None	None	/									
2. ICC - film resistor	Nichrome evaporation, nichrome etching	Evaporator, digital ohmeter		/								
3. Low power logic gate, 1st of family - (M. V. to complete family)	Nichrome resistor with other processing.	See 2.			/							
4. High Speed logic gate, 1st of family - (M. V. to complete family)	Nichrome, inline epitaxy	Sb predep furnace, epitaxial grower				/	/	/				
5. ICC - epitaxial transistor (from 4)								/				
6. Differential amplifier	Very stable film resistors, resistor adjustment	Airbrasive unit, digital ohmeter					/					
7. No lead-bond assembly, single chip	Assembly technology							/				
8. Diode array	Packaging								/			
9. Inverted Transistor Circuitry	In-line epitaxy (see 4)	4 new diffusion furnaces										
10. New resistor technology (high value)	Sputtering, new etching										/	
11. Multiple chip, no lead bond assembly	Ceramic metallization										/	
12. NPN + PNP on same chip	Diffusion schedules	~ 16 furnaces										/
13. – 22. 10 proprietary circuits using existing technology		Test equipment										
23. – ∞. Custom circuits for customers Litton, Autonetics, DWP, etc., etc.												

GEM:hb
9/6/62

New Product Forecast for 1963 - Page 2

TRANSISTORS:

Device & Description	New Technology	Additional Major Equipment	Transfer Target Dates									
			N	D	J	F	M	A	M	J	3Qtr.	4Qtr.
SMALL GEOMETRY A. Field Effects												
1. U-2 (chopper)	Material supply (same as U-1), out-diffusion	Epitaxial grower, diffusion furnace	/									
2. U-3 (100Ω on impedance)				/								
3. U-4 (high frequency)	Improved masking									/		
4. U-5 (high voltage)												/
5. U-6 (P-channel)	Special epitaxial starting material											/
B. R.F. Transistors												
1. ~~0000~~ UHF AGC, non-epitax.	3/8 mil masking (needs life test!)			/	/	[Take the rest]						
2. 0001 VHF RF	3/8 mil masking, thin epitaxial			/	/							
3. 0002 1 watt, 500 Mc	None		(transfer Sept. 1962)									
4. 0006 2.5 watt, 500Mc							/					
5. VHF-UHF Power Osc. ($>$ 5 watts)	Assembly structure											/
6. Strip-line package	Assembly techniques	Furnace, test jigs									/	
C. Switching												
1. 0003 (1ns prop. delay optimum logic switch)	Masking improvement							/	/			
2. Film driver (2ns to 1 amp, LVCEO = 10v)	Epitaxial control, ultra-thin base								/	/		
3. NoAu replacement for 1324	Abrupt epitaxial, pre-growth diffusion	Diffusion furnace										
4. 3112 (30 v, 20ms trident)			/									
5. 3016 (60 v, low VCE(SAT)	Special high voltage epitax.				/	/						
6. Radiation resistant Xstor	?											/

9/6/62

New Product Forecast for 1963 - Page 3

Device & Description	New Technology	Additional Major Equipment	Transfer Target Dates									
			N	D	J	F	M	A	M	J	3Qtr.	4Qtr.
D. Planar												
1. 4016 4200 diffusion, > 60v epitaxial	High voltage epitaxial				/							
2. SCR-1 400v, 3 amp	High voltage junction	Test equipment, diffusion furnaces	/	/								
3. SCR-2 400v, 20 amp	Assembly, packaging	Test equipment					/	/	/			
4. SCR-3 10 amp in 2ns pulse, 200v	Special epitaxial											/
5. SCR-TV yoke driver											/	
6. 8000-20 amp power, 100v LVCEO	Solve switchback	Test equipment										/
7. Low cost power package (<25 cents total)											/	
E. PNP												
1. 1713 (best present PNP silicon switch)	Sales push	None	/									
2. 0005 (low storage PNP switch)	(Still being invented)										/	
3. 0007 (low storage, med. geometry)	(Still being invented)											/
4. 7500					/	/	/					
5. 4511	Switchback, high current		No Schedule									
6. 7501	Switchback, high current		No Schedule									
DIODES:												
1. FZ-2 (7.5ma voltage ref)			/									
2. FZ-3 (gen. purpose 6-30v glass package)	Needs life tests				/	/						
3. Sandia diode						/	/	/	/			
4. XP-3	New assembly											
5. Med. Power Zener family											/	
6. High power Zener family												/

GEM:hb
9/6/62

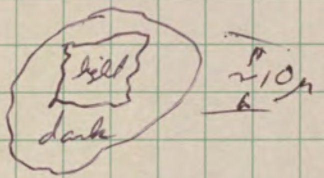
Defects, cont 10/8/62

On the μ probe exp:

1. Oxidized wafers
2. Ox, etched, B-Predeped.

No pipes were delineated ahead of time electrically

On both of these metal segregates were observed. One, for example



for back-scattered electrons
light means heavy metals
dark usually means oxide

The light were, in some cases, Fe. This was present as early as the oxidation step.

The ~~unoxidized~~ wafer is being run now.

It is interesting that the two groups of metals often found,
Cu and Zn
Fe and Ni
are the composition of bronze (saws) and steel (lapping plate?)

~50 % of the pipes show metals in them.
They all have high P concentrations

We have tried synthesizing pipes in several ways. We got them c̄ such things as

$Fe(SO_4)$ spray
$CaCl_2$

But these made pipes only at high bulk doping!
That is, pipes @ 0.01 Ω-cm
none @ 0.5 Ω-cm

The one thing we know is that P is always present in pipes.

Defects, cont., 10/8/62
Program Plan:

1. Electron beam probing as process stages to try to see where metals and P come in.

2. a) Look for loops and see if it correlates c̄ oxygen diffusion
b) Do loops correlate c̄ segregation

3. Keep in touch c̄ Mtn View.

Oct 11, 1962 - Resistor c̄ Al+SiO₂

Lofly
Hubell
Campbell

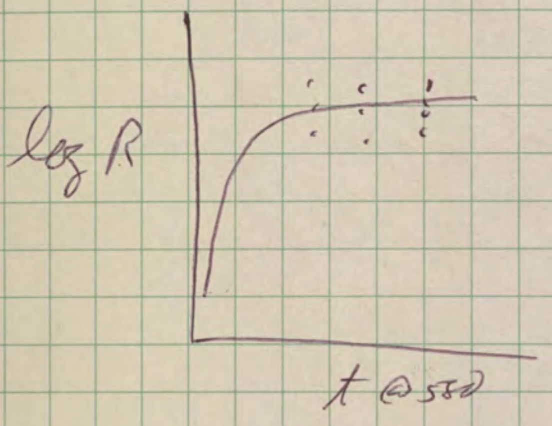
There are p-type films - but can convert to n-type in a P-dif furnace

The P-type films have a ~ −0.17 %/° T.C 10 − 110°C.

~~All meas~~ Most meas are c̄ points. Some are the STB pattern with subsequent Al contacts.

Variables: t, T, thickness, composition (up to 11% Si)
500-1000 75-4800Å

600 Å in 3 comp for reproducibility



The final value is roughly the same independently of temp.

$\frac{96}{216}$ were between 0.5 and 1.0 MΩ

~~Out of~~ 5/22 of pairs on one wafer are well matched.
8/23 " " another "

Problems:

1. De wetting
2. Doped oxides charge cause opens
3. Indication of contact problems
4. Noise

Section Meeting: Oct 9, 1962

The S&R and 10 position are going ok now.

Mtn View is trying a jury-rig interim 1000:1 scheme.

Sid has used lacquer-coated masks and it has solved his problems.

On the chrome masks, there is a substrate cleaning problem.

We see 100-200 visual pinholes ($>$1 mil). We get ~~[illegible]~~ many more at 400X.

The proprietary Au etch is good for Al. We will follow up.

Art will make pinhole counts on some of our stuff.

We will someday try to evaluate the effect of separation of mask - wafer.

Sam will check on the cost to make a printed ckt board
a) 1st of a kind
b) subsequent.

ROBE

Oct 16, 1962

Sang on trouble areas in spreading diffusion.
Recommended new process.

Wafers are delivered oxidized from Materials. 5 fringes of oxide
Lapped on one side only
Etched on both sides - 50μ from each side removed.

After 1st masking the wafers are stored before KPR strip. They are then stripped just prior to loading the furnace

Cleaning or diode check is being studied.

The FSC furnaces can vary 5 - 10 degrees in 24 hrs.

Sang shows that the furnaces don't recover well at all (10 min delay)

The "Heviduty" Hagen furnaces recover much faster. It does very little diff-

Paul Hill is interested in low mass boats.

Thermocouple: Calibrate $\bar{c}$ Cu melting point. - 4 MO to set up.

4-Point probe - Getting ~ ±5% reproducibility

Ox slides: They need ~ 200 slides per month.

We will supply ~ this many for an indefinite time.

Oct 18, 1962 Noyce's Staff Meeting

See RNN:

1. Any paper whose existence depends upon the properties of a new device should have the device developer name on it.

2. Reine.

3. See Campbell re Yurad.

MINUTES OF MEETING

LONG RANGE TRANSISTOR PRODUCTION PLAN

October 3, 1962

I. LOGIC SWITCH

(a) npn

50-100 ma	1321, 1312 and 0003(100 ma ?) increase. $\frac{I}{C_{ob} + C_{stray},}$ decrease τs, $LV_{ceo} > 10V$.
.5ma-5ma	No need to work in this field. 50-100ma takes care.
100 μa	1250, improvement. Question of Ae to I_e need information--get from Sandia contract. Highest β at low current with max. f_t (minimize C_{te}, C_{ob})

(b) pnp	same as above npn pnp version of 1250 or improved version with lower C_{ob}, C_{te}

II. DRIVERS

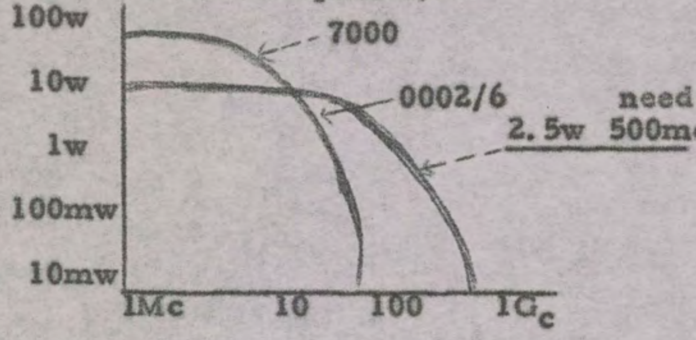
(a) Core Driver	500 ma, want $LV_{ceo} > 60V$, but consider salable 35V, $V_{ce(sat)}$ low and constant with temperature
3511	$f_t \approx 400mc$ $\tau s(150/15/15) < 25ns$
3111	Want npn and pnp complement
(b) Thin Film Driver	$LV_{ceo} > 10V$. 700 ma. $f_t > 600mc$. $t_{rise} < 5ns$? Lower voltage. Want both npn and pnp.

III. RF AMPLIFIER-SMALL SIGNAL

0000/1 and improvements for VHF/VF for P.G., N.F., AGC, cross modulation.

R. Shultz will get us information as to whether 1ma operating pt. o.k. for all sockets in VHF receiver.

Power Amplifier/OSC



need breakthrough (metal-glass-metal-sandwich?)

IV. GENERAL PURPOSE

low speed switch
audio etc. amp.
analogue devices

for low current gain (?)
3010/3011
3510/3511

V. POWER

7000 and 8000 will strain us for quite awhile.

$LV_{ceo} > 80V$. Blast out switchback units in an old type "agregate."

VI. SPECIAL PURPOSE

High Voltage Nixie Driver

High Voltage Solenoid Driver

Chopper Type - we will look at X3L structure for good B_n and B_I

Pre Product Planning Meeting Meeting, NPN small geometry

MHb
JPF

Ref Avg (?

	Being done by	Sept D.S.	Problem
1340	P		h_{FE}s, v. l. yield (8% 708's), V_{CE} (125°)
1341	P		
1240			
1243	P		
1250	P	[illegible]	
1251			
1440			
1244			

1210
1211 (Won't make 2N917's because of high leakage
1221
1310 } 1311 two stage
1311
1321 } 1312
1312
1324 Xfeed now?

0000 AGC 3/8
0001 RF 3/8
0002 Agg 4, ½ mil 1 cell
0003 - 1ms - to be dev.
0006 - 2½ w @ 500

U-1 first good one the Mtg [illegible] not [illegible]
U-2
U-3

3010
3011
3012
3016
3111

Small Geometry P.P.M.

1. Use 1312 with 15v

Boz
Spink
Schultz
Ferguson
Jamil
Reiz

Richmond
Stanberg
Jagg
Steidler

MINUTES OF MEETING

LONG RANGE TRANSISTOR PRODUCTION PLAN

October 3, 1962

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Minutes of Meeting
Long Range Transistor Production Plan

October 3, 1952

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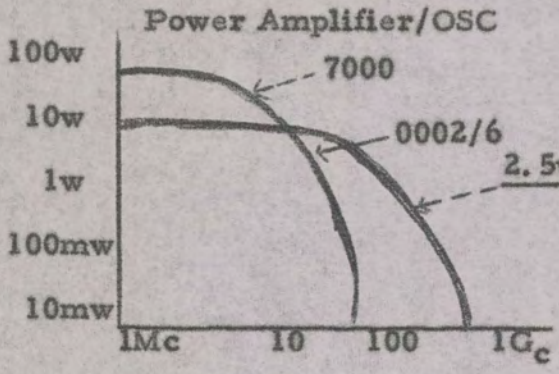

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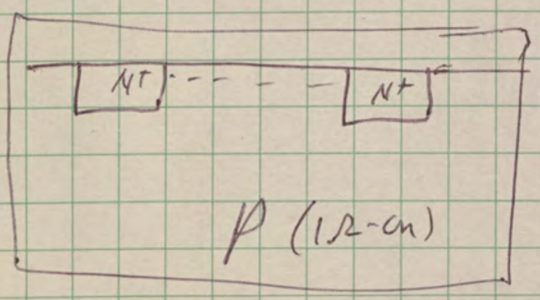
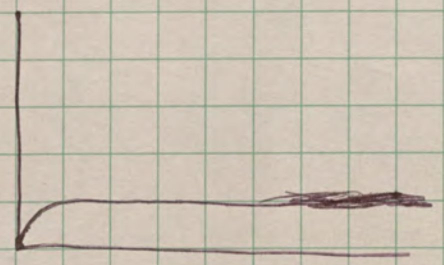
Surfaces - Project Review - Oct 23, 1962





Discussed the oxide for a while. The semantic problem is overwhelming

PPPMM — NPM
should we?

4200 →? 4010 } eventually 4016 →
4205 →? 4015 — (will not make 4200 sat, there may be a low I/β problem)

4300 ✓→ Planning on 4110 (our mill is 1340 dif)

3001 (30v) ✓→ 4016/16 (R_{TH}?) → Could be 4011 if adequate material was available

6206 — They are flying

4116 — 1340 dif, Trident II geo — proposed new product w/ TI Blizzard
Need >30v LV_{CEO}.

7000 — What is life data?

SCR-1 (400v - 3a) — Ready for qual.
-2 (
-3 (

P-3 — We are running 5K, — Ready for qual.

Planar, Low cost, power
Low cost, low power.

PPM — 10/26/62

Power Xstr

7000 — No epitaxial material
Triple diffused is causing problem

We will meet Nov 15 to check data

1. M.O. on
   a) Triple diffused c̄ lap
   b) Westinghouse epi
   c) Std, non epi, non triple

2. JPF on reverse PNP epi data.

SCR-1 — A man will come up — Yost will tell when.

K/wk Sched PNP —

40/40 4500
0.1/2 4511 — Run
0/2 3571 — "Easy" to do, no order, run 0–2 K/wk
0.1/1 1712, 1713 — Aim at 1713 (20V, thin film) — aim at 5 K/week
5/15 { 1741
1746 } ok
7500 — We run for MIT, consider in 4 MO.

Oct 29, 1962 — μ electronics

Graham
Ferguson
Schultz
Hoerni
Phelps
Bay
Moore

Status of μL:

We have more business than we can handle
" can see more than we can build up to handle —
at present yields.

Motorola is delivering the complex special products.
TI is producing "hacked together" Master Slice units

JPF on yields

Isolation — 70% (loss by lack of, etc)

Contact dif — 70% (loss by thickness giving way)

Electric Die sort — 20% electrical — 1/2 metal-related
1/2 other electrical and — β is a problem

Optical sort — 50% surface of metal.

Optical in line — 75%

A+B Class yield — 40% (Gates — 50-60%) (f — ~5-10%)

Point: — The technology is limiting for any ckt — Not the ckt per se.

Decision — Make some Seeds ckts.

Nov. 4 (1 mil R's) 1. Seeds, Ferguson, Schultz and Hoerni will decide on one option for the ckts

by Nov 15 2. R&D will lay out and make masks

Dec 1 3. Ferguson & Plough will decide ~~who will~~ that Plough will run.

4. Seeds will characterize

5. Ferguson will look at this NAND logic for new technology

INTERNAL CORRESPONDENCE

FAIRCHILD SEMICONDUCTOR CORPORATION

To: MOORE, G.✓
GRINICH, V.
SHULTZ, R.

Date: October 23, 1962

From: Mel Phelps

CC: Bay, T.
Graham, R.

Subject: μE Product Planning Meeting

RECEIVED
OCT 23 1962
GORDON E. MOORE

This meeting will be held in the small conference room at R & D at 9:00 A.M., Monday, October 29, 1962, for the purpose of reexaming the direction we are taking in Microelectronics. Meanwhile, here are some questions to be thinking about.

1. Should a new family using Micrologic I diffusion schedules and techniques be introduced?

2. If so, what logic form is best?

3. Do the Defense Products Division circuits (μE-2X, μE-3X, etc.) represent the kind of product we collectively feel should constitute our second family?

4. Should we offer one gate from each logic form (any Logic) with present technology?

5. Are we offering enough with the new technology to be competitive?

   a) High enough voltages?

   b) High enough speeds?

   c) Adequate tolerances?

6. What preparation should be made for test equipment in Custom and Standard Integrated Circuits? Who is responsible?

These subjects and others should be aired for comment. I have my ideas and would normally proceed with Marketing plans, but I feel we should all have a chance at improving our product image when timing permits.

Also please invite those you feel necessary from your area to attend.

Regards,

Mel
Mel Phelps

MHP:mab

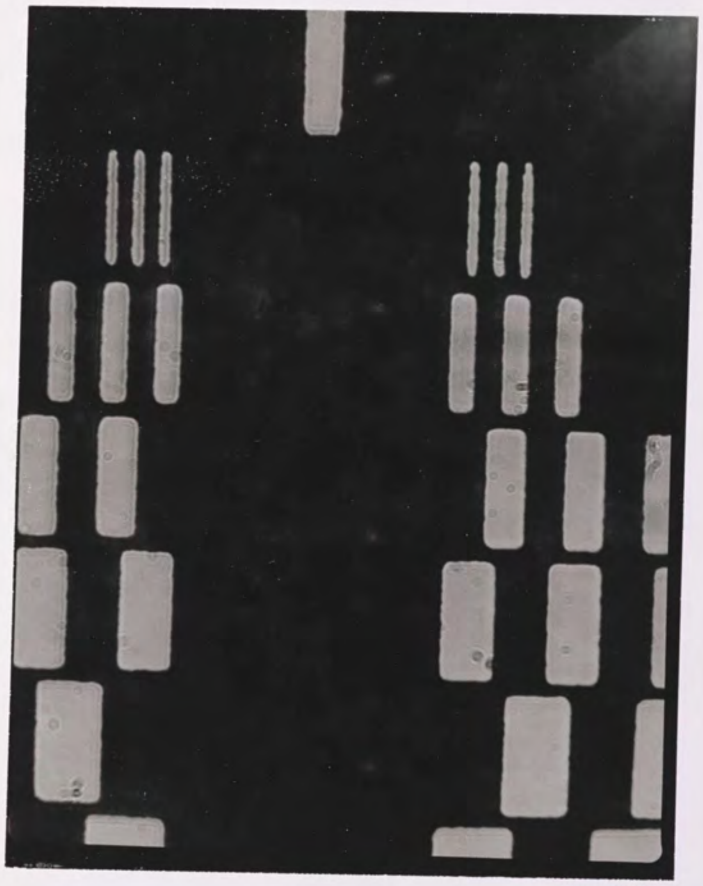
FORM 5121

Oct 30, 1962 — Section Meeting

The ½ mil laquer coat does not result in ~~appre~~ measurable loss of resolution, even c̄ 0.1 mil lines and spaces.

The new camera is working! — Infact it is working well!

Cr masks are being used, but no facilities or space allotted.



SINGLE KMER COAT
COATED @ c̄ DFL 6" SPIN
COATER USING 1:2
KMER
EXPOSURE 40 SEC.
ETCHED c̄ 3N HCl
+ 0.5% FC-95 & ULTRA-
SONICS

Cr MASK

700X

10-23-2

Oct 3

The ½ mil ~~type~~ measurable.
lots of ren l spaces.

The new cam well.

Cr marks now alloted.

C20717

POLAROID

MASK
TR-3

700X

10-19-2

ROBE — 10/30/62

Hill | Folz
Sang | Moore
Robinson | Talbert
McCall | Bloome

1. Cr masks: (Robinson)

4200 —

after ~ 1000 wafers got poor edge definition - cleaning restored.
Photo shows masks after 1700 wafers — 52/110 show visible defects.

1.2% start → 6.8% after 1700 wafers · flaws that reproduce.

This is ~ 5X the life of photographic mask.

4200 families is now all Cr.

2. Good practices
a) KPR removal just prior to diffusion — no bad affects
b) Furnace recovery is ~7 min to 5°. — So in Reliability.
c) Thermocouples; — getting some from S.R. — M.V. will take over entire supply.

Nelly / Basteon 4,5 70 emitter - run I 5%

Also for next time get ready to plan program on other defect elimination.

DATE 10 - 26 19 62
EQUIP. USED
TAKEN BY M. LAWRENCE
REQUESTED BY B. BARRANGER

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ENGINEERING DATA

( ) I. a-1 CLASS
REMARKS
CUSTOMER
GROUP Appl. ENG.

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP.	SP.	

~~LOT~~ No. VGD=	UNIT No.	0 HRS IGDS μμA TA = 25°C	0 HRS. mμA TA = 100°C	15 min. mμA 100°C	30 MIN μμa 100°C	45 MIN μa 100°C	1 hr 45 MIN μa 100°C	2 HR μa → 100°C	↓	2½ hR. 100°C	
30V	01	32	3.4	μA 12	μa 62	160	300		340	400	
	02	2400	6.0	μA 36	μa 38	62	160		280	320	
	03	70	6.4	9	μa 5	48	180		250	360	
	04	40	5.2	5	5	μμa 6.6	120.0 μμa	μμa	380	420 μμa	
	05	50	4.2	5	7	μμa 15	40.0 μμA	μμa	70	150 μμa	
	06	130	5.2	μA 72	μa 300	320	500		520	560	
	07	100	5.8	32	μa 2	46	250		340	420	
	08	225	5.4	6	600	3.6	52		98	150	
	09	91	5.6	5	8	1.1	15		25	38	
	10	1400	5.4	26	1200	1.1	21		46	840	
20V	11	380	6.4	μA 22	μa 160	520	980	MA	1.4	1.3 MA	
	12	140	4.2	600	μa 13	66	220		270	300	
	13	42	4.0	80	μa 3	38	170		250	320	
	14	82	3.4	5	6	μμa 8	15 μμa	μμa	20	29 μμa	
	15	159	3.8	μA 280	μa 620	MA 1.3	1.7 MA	MA	1.7	1.8 MA	
	16	28	4.4	4	4	μμa 5	400 μμa	μμa	1200	260 μμa	
	17	61	4.2	μA 3	μa 120	520	1.2 MA	MA	1.4	1.5 MA	
	18	60	2.2	4	780	16	64		86	110	
	19	28	3.0	8	8	μμa 700	6.2 μμa	μμa	6.2	6.8 μμa	
	20	86	3.1	22	μa 7.4	90	420		520	620	
10V	21	13	2.2	2	2.4	2.4	2.4		2.4	2.3	
	22	17	2.8	3	2.4	3.0	2.9		3.0	3.0	
	23	35	2.6	3	2.6	2.6	2.6		2.7	2.6	
	24	27	1.6	2	1.6	1.7	1.6		1.6	1.7	
	25	19	2.1	2	2.2	2.5	2.5		2.5	2.5	
	26	42	2.2	3	14.0	1.2	880		200	460	
	27	32	1.1	2	1.4	1.2	1.4		1.4	1.5	
	28	26	1.3	2	1.3	1.3	1.3		1.3	1.3	
	29	15	1.5	2	1.7	1.8	1.9		1.9	1.9	
	30	16	1.4	2	2.4	11.0	15.0		25.0	42.0	
	31										
	32										
	33										
	34										
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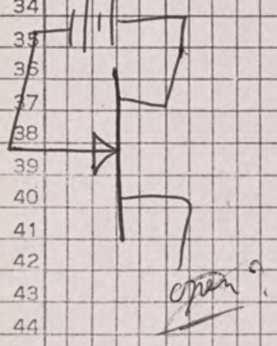
	48										
	49										
	50										

μμa



S 994

FT. ____ CLASS ____

REMARKS ____

GROUP ____

FAIRCHILD
SEMICONDUCTOR CORPORATION

ENGINEERING DATA

DATE ____ 19 ____

TAKEN BY ____

EQUIP. USED ____

REQUESTED BY ____

LOT No.	DE.	OP.	GR.	TYPE No.	CL.	TE.	COND.	DATE	ELAPSED TIME	SP	SP	

LOT No.	UNIT No.	0 3 HR 100°C ma	3½ hR 100°C ma	2 100°C 13½ hR ma	3	4 25°C 13½	5	6	7	8	9
		←			30 VDG					→	
	1	420	480	700		230	μa				
	2	420	500	MA 1.6		270	μa				
	3	510	620	890		230	μa				
	4	1.7	25	12		3.2	μa				
	5	Mμa 400	1.0	150		68	μa				
	6	600	620	560		190	μa				
	7	560	640	810		220	μa				
	8	240	360	MA 1.1		260	μa				
	9	59	78	230		130	μa				
	10	150	230	MA 1.7		2	MA				
←					20 VDG						→
	11	MA 1.4	MA 1.6	MA 1.7		290	μa				
	12	320	340	400		220	μa				
	13	440	560	MA 1.3		290	μa				
	14	Mμa 54	MμA 110	23		58	μa				
	15	MA 1.9	MA 1.8	MA 1.8		300	μa				
	16	Mμa 580	1.1	21		17	μa				
	17	MA 1.8	MA 1.8	MA 1.8		300	μa				
	18	130	160	270		180	μa				
	19	μμa 7.8	MμA 20	10		54	μa				
	20	720	800	MA 1.4		290	μa				
←		MμMA	MμA			10 VDG					→
	21	2.3	2.3	92		200	μμa				
	22	3.0	3.0	34		14	μμa				
	23	2.7	2.7	190		23	Mμa				
	24	1.7	1.6	1.6		10	μμa				
	25	2.6	2.7	7.8		120	μμa				
	26	1500	MA 4	μa 420		82	μμa				
	27	1.7	1.9	74		6	Mμa				
	28	1.4	1.4	1.5		7.8	Mμa				
	29	2.0	2.1	64		120	μμa				
	30	84.0	110	μa 180		110	μa				

NS – 277 C

Form: AE – 0006a

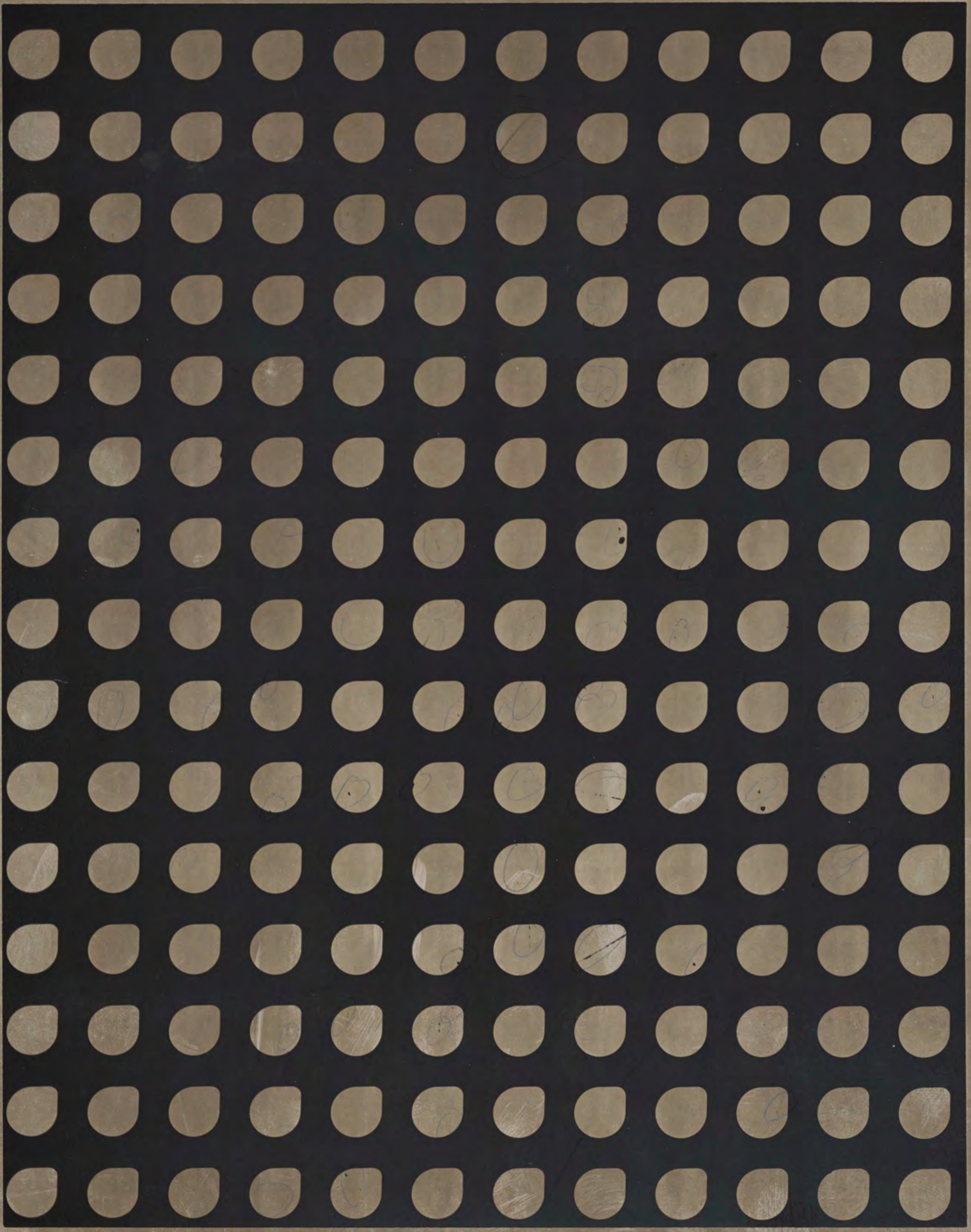


Photo of base mask after 1700 wafers

AGENDA Standardization Meeting October 30, 1962

1) Good Practices (Phase I)

   a) Put listed practices into a processing system.
   b) Apply to Process Development Facility for check out and determine quantitative improvement where possible.
   c) Recommend practices to production areas.

   Reports:

   ✓1) KPR removal immediately prior to furnace operation (Process Development area)
   ✓2) Profiles with boat inserted (Process Development area)
   ✓3) Teflon joints in glass jungles
   4) Continued profiling with recorders attached
   ✓5) Thermocouples (possible re-location of supplier)

✓2) Chrome Masks (Phase II)

   a) Results of 4200 runs.
   b) Transfer process to Mountain View.

3) Standard ~~Masking~~ Diffusion (Phase III)

   a) M-B on 4500 emitter (parameter dist. and life test)
   b) M-B on 4200 base (parameter dist. and lift test)
   c) M-B on Small Geometry (1243 & 1340 in Process Development)

Data on FET's — Nov 2, 1962

Lamond
Sah
Ferguson
Grinich

Pogel
Leistiko

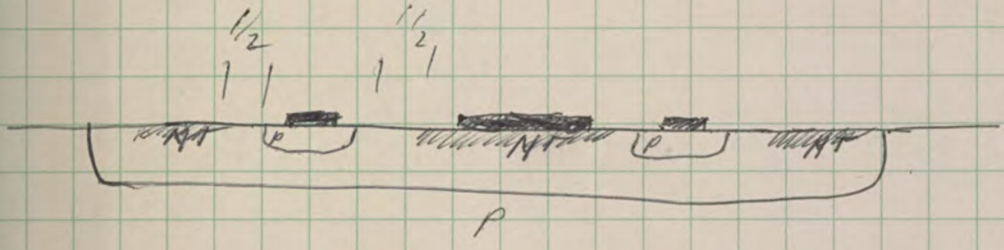
Data from sheet:

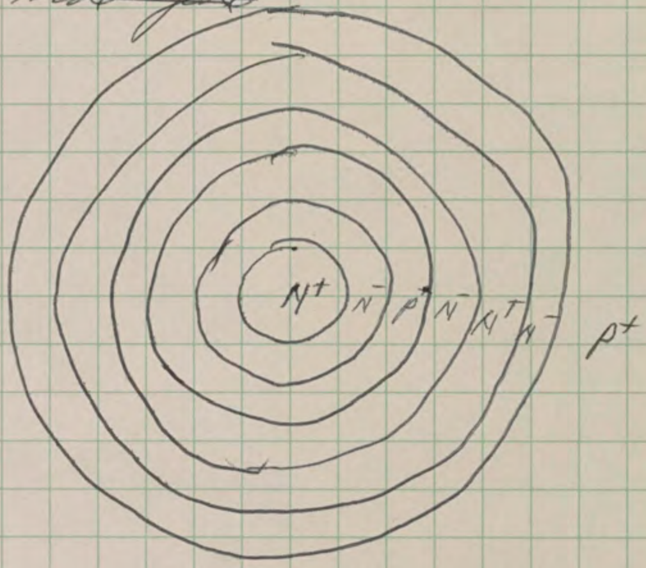
At 20 v or greater, the channel dev. is a 100% effect.

[3×10^{15} is seed end P conc. The Al is 3×10^{16}.
at the end ~ 10^{16} ~ 10^{17}]

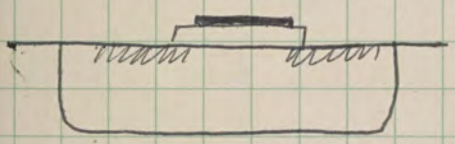
The channeled FET's will recover in 300°C age.
The PNP Xstors made in out-diffused structures like FET's develop channels.

One ~~do~~ SCFET was tried c̄ ~~both side gate~~





One of these c̄ voltage adj on the back gate biased at adj 10 v (as high as possible) showed no change in ~~6~~3 hrs @ 150°C.



But, Q thru is ~30 min @ 1250°C outdiffusion
the regular one is 15 hrs @ 1250

	P+ top	Al over oxide top	Gauss. sampled	15 hr out	30 min out	Dep. in	Shallow in	Sep. top gate
U-1	✓					✓		
SCFET		✓			✓		✓	✓
Q-0	✓		✓	✓		✓		
XFE 506 FET-3	✓			✓		✓		
Q-1	✓				✓		✓	✓
Q-2				✓		✓		
Q-3		✓		✓		✓		
Q-4							✓	
Q-5	✓				✓	✓		

All data by next Friday to look at

Q-6 : a U-1 with stripped oxide after outdiffusion followed by regrown oxide.

Nov 5, 1962 – Mag. Film Memory.

Hale
Sah
Schmidt
Perlman

Grinich

What do we need to be able to do?

Problems:

A. "Almost" solved
  1. High speed pulse using R&D devices
  2. Film that switch.
  3. Need coercive force of ~ 8 Oe for small spots (Needs impurities)
  4. ~~Need~~ Ability to deposit individually the various things to make a plane.
     a) SiO_2 & SiO_x
     b) Ni-Fe
     c) Cu
     d) Ag
  5. Primitive masks only to date
  6. Sense amplifier using tunnel diodes

B. Nebulous
  1. "Small" film spots with usable characteristics (10 x 20 mil)
  2. Multilayer deposition
  3. Connections to outside world (size & material problem)
  4. Masks for large planes.

Problems:
  1. Competent people to make evap.
  2. Jigging, (which relates to 1).

With two pump-downs we can go to a 5-layer structure that can be checked by HSME.

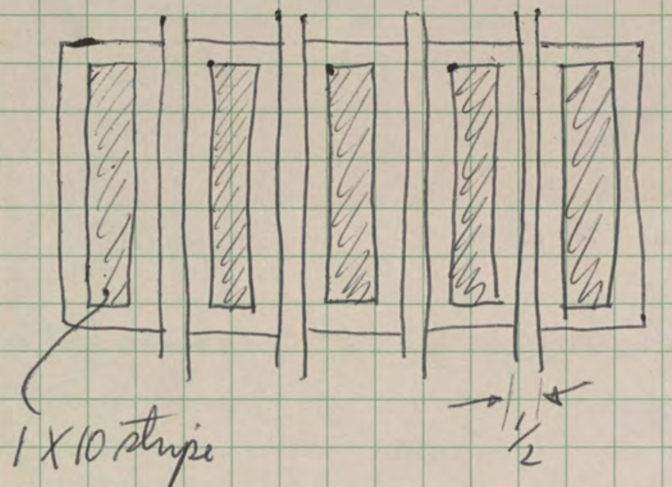
There are many people & cleanliness problems.

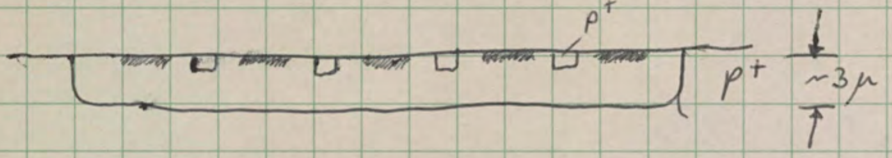
Nov 5, 1962 More FET data.

Ragel
Leistiko
Sah

Grinich
Ferguson
Lamond

The device structure (U-2 mask)





8 units stored @ 10v @ 200°C over weekend – no change
These units look ~1NA I_{SGO}, ~30v BV, etc.
No noise ~~structure~~ meas. yet.

Decision: it looks good enough – Start ~100 wafers thru.
Give priority thru epitaxial
Get units by two weeks
Don't interfere $\bar{c}$ present program.

FAIRCHILD SEMICONDUCTOR
DIODE PLANT

Week Ending 11-2-62
Prepared By R. Lous
Approved By

RECAP WEEKLY STATUS REPORT

FD ..100..

QUALITY ASSURANCE ENGINEERING

A = Acceptable
NA = Not Acceptable
⧅ = Complete
☒ = Complete, No Failures

Week	Type Package	Subgroup II	Subgroup III	Subgroup IV	Subgroup V	Subgroup VI (HTS) 200° C	Subgroup VI -65°C	Subgroup VII	Status	RECAP		Acc. Tab Run	1401 Print Out
229	G	☒	☒	☒	☒	☒	☒	☒	⧅	A			
230	G	☒	☒	☒	☒	☒	☒	☒	⧅	A			
231	G	☒	☒	☒	⧄	1 IR cat	☒	☒	⧅	A			
232	G	☒	☒	☒	40 units 1 IR cat	⧄	☒	☒	⧅	A			
233	G	Thermal Shock No Fail	☒	☒	☒	⧄	⧄	⧄	Inc.	A			
234	G	☒	☒	☒	Pretest	☒	⧄	⧄	Inc.	A			
235	G	☒	☒	☒	☒	☒	750 hrs. No Fail	⧅	Inc.	A			
236	G	☒	Centrifuge No Fail	Pretest	☒	750 hrs. No Fail	750 hrs. No Fail	750 hrs. 1 VF cat	Inc.	A			
237	G	☒	☒	☒	☒	500 hrs. No Fail	750 hrs. No Fail	750 hrs. No Fail	Inc.	A			
238	G	Thermal Shock No Fail	Shock No Fail	☒	☒	250 hrs. No Fail	Pretest	250 hrs. No Fail	Inc.	A			
239	G	☒	Centrifuge No Fail	☒	Pretest	250 hrs. No Fail	250 hrs. No Fail	250 hrs. No Fail	Inc.	A			
240	G	Shock No Fail	Pretest	Pretest	Pretest	500 hrs. No Fail	250 hrs. No Fail	250 hrs. No Fail	Inc.	A			

FAIRCHILD SEMICONDUCTOR
DIODE PLANT

Week Ending 11-1-62
Prepared By R. Lons
Approved By

RECAP WEEKLY STATUS REPORT

FD .200....

QUALITY ASSURANCE ENGINEERING

A = Acceptable
NA = Not Acceptable
⧅ = Complete
☒ = Complete, No Failures

Week	Type Package	Subgroup II	Subgroup III	Subgroup IV	Subgroup V	Subgroup VI (HTS) 200° C	Subgroup VI 150°C	Subgroup VII	Status	RECAP	Acc. Tab Run	1401 Print Out
226	S	☒	☒	1 Fail	2 IR cat	9 VF cat	☒	4 IR cat 1 VF cat	⧅	NA		
227	S	☒	☒	☒	☒	2 IR cat 9 VF cat	1 IR cat	6 IR cat 2 VF cat	⧅	NA		
228	S	☒	☒	☒	☒	☒	1 VF cat	2 VF cat 10 IR cat	⧅	NA		
229	S	1 IR cat	2 IR cat	☒	☒	1 IR cat 8 VF cat	☒	☒	⧅	NA		
230	S	☒	☒	☒	1 IR cat	1 IR cat 5 VF cat	⧅	7 IR cat 1 VF cat	⧅	NA		
231	S	☒	☒	☒	☒	750 hrs. 1 VF cat	☒	750 hrs. 3 IR cat	Inc.	NA		
232	S	☒	☒	☒	☒	1 IR cat 2 VF cat	☒	☒	⧅	NA		
233	S	1 IR cat	☒	☒	☒	750 hrs. 2 VF cat	750 hrs. 1 IR cat	750 hrs. No Fail	Inc.	NA		
234	S	1 IR cat	☒	☒	2 IR cat	750 hrs. No Fail	750 hrs. No Fail	750 hrs. 2 IR cat	Inc.	NA		
235	S	☒	☒	☒	☒	500 hrs. No Fail	750 hrs. No Fail	750 hrs. 2 IR cat	Inc.	NA		
236	S	☒	Centrifuge No Fail	☒	1 IR cat	750 hrs. No Fail	750 hrs. No Fail	750 hrs. 1 IR cat	Inc.	NA		
237	S	☒	Centrifuge No Fail	☒	☒	500 hrs. 1 VF cat 1 IR cat	500 hrs. No Fail	500 hrs. No Fail	Inc.	NA		

FAIRCHILD SEMICONDUCTOR
DIODE PLANT

Week Ending 11-2-62
Prepared By R. Lous
Approved By

RECAP WEEKLY STATUS REPORT

FD 300

QUALITY ASSURANCE ENGINEERING

A = Acceptable
NA = Not Acceptable
⧅ = Complete
☒ = Complete, No Failures

Week	Type Package	Subgroup II	Subgroup III	Subgroup IV	Subgroup V	Subgroup VI (HTS) 200° C	Subgroup VI 150°C	Subgroup VII	Status	RECAP		Acc. Tab Run	1401 Print Out
229	S	☒	☒	☒	☒	2 VF cat ⧅	☒	☒	⧅		NA		
230	S	2 IR cat ⧅	2 IR cat ⧅	☒	☒	1 VF cat ⧅	☒	1 VF cat ⧅	⧅		NA		
231	S	☒	☒	☒	1 Fail ⧅	1 VF cat ⧅	☒	750 hrs. 1 IR cat	Inc.		NA		
232	S	1 VF cat ⧅	☒	☒	1 VF cat ⧅	3 IR cat 8 VF cat ⧅	1 IR cat ⧅	1 BV cat ⧅	⧅		NA		
233	S	☒	☒	☒	☒	1 IR cat 5 VF cat ⧅	☒	2 IR cat ⧅	⧅		NA		
234	S	1 IR cat ⧅	☒	☒	☒	750 hrs. 2 IR cat	3 IR cat ⧅	750 hrs. No Fail	Inc.		NA		
235	S	☒	☒	☒	☒	750 hrs. 1 IR cat	500 hrs. 1 IR cat	750 hrs. 1 IR cat	Inc.	A			
238	S	1 IR cat ⧅	Shock No Fail	Pretest	☒	250 hrs. 1 IR cat	250 hrs. No Fail	250 hrs. No Fail	Inc.		NA		
239	S	STARTED											

DNS 612, 9/62

FAIRCHILD SEMICONDUCTOR
DIODE PLANT

RECAP WEEKLY STATUS REPORT

FD 600

Week Ending 11-2-62
Prepared By R. Lous
Approved By

QUALITY ASSURANCE ENGINEERING

A = Acceptable
NA = Not Acceptable
⧅ = Complete
☒ = Complete, No Failures

Week	Type Package	Subgroup II	Subgroup III	Subgroup IV	Subgroup V	Subgroup VI (HTS) 200° C	Subgroup VI	Subgroup VII	Status	RECAP		Acc. Tab Run	1401 Print Out
226	S	☒	☒	⧅ 1 IR cat.	☒	1 IR cat ⧅ 4 VF cat	⧅ 1 VF cat.	1 VF cat ⧅ 1 IR cat.	⧅		NA		
227-231		NO	PRODUCTION										
232	S	⧅ 2 IR cat.	Centrifuge No Fail	⧅ 1 Fail	⧅ 2 IR cat	750 hrs. 1 IR cat 4 VF cat	⧅ 1 IR cat.	750 hrs. 5 IR cat 1 BV cat	Inc.		NA		
233	S	⧅ 1 IR cat	☒	☒	☒	750 hrs. 1 IR cat	☒	⧅ 2 IR cat.	Inc.		NA		
234	S	Thermal Shock No Fail	☒	☒	☒	☒	750 hrs. 1 IR cat	750 hrs. 3 IR cat	Inc.		NA		
235	S	⧅ 2 IR cat.	⧅ 1 IR cat.	☒	☒	⧅ 4 IR cat	☒	750 hrs. 5 IR cat	Inc.		NA		
236	S	☒	☒	☒	☒	750 hrs. 3 VF cat	750 hrs. 2 VF cat	750 hrs 2 IR cat	Inc.		NA		
237	S	⧅ 1 VF cat	⧅ 1 IR cat	☒	Pretest	750 hrs. 1 VF cat	750 hrs 1 Vf cat	750 hrs. 3 IR cat	Inc.		NA		
238	S	⧅ 1 IR cat.	Centrifuge 2 IR cat	☒	Pretest	250 hrs. 2 IR cat	250 hrs. No Fail	250 hrs. No fail	Inc.		NA		
239	S	Thermal Shock No Fail	Centrifuge No Fail	☒	Pretest	250 hrs. No Fail	500 hrs. No Fail	500 hrs. 1 IR cat	Inc.	A			
240	S	STARTED											
241	S	Pretest	No Fail	Pretest	Pretest	Pretest	Pretest	Pretest		A			

Q.A. Engineering.

Military Diode Acceptance Report.*

Date: 11-2-62

											WEEKS																									
	223		224		225		226		227		228		229		230		231		232		233		234		235		236		237		238		239		240	
FD 100	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA
JAN IN 251	D		D		D		D		D		D		D		D		D		D		D		D		C		C		C		A		A		A	
USN IN 914	D		D		D		D		D		D		D		D		D		D		D		D		C		C		C		A		A		A	
USN IN 3064	D		D		D		D		D		D		D		D		D		D		D		D		C		C		C		A		A		A	
USA IN 662	D		D		D		D		D		D		D		D		D		D		D		D		C		C		C		A		A		A	

	220		221		222		223		224		225		226		227		228		229		230		231		232		233		234		235		236		237	
Fd 200	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA
USN IN 3070	D		D		D		D		D			X		X		X		X		X		X	C		D		C		C		C		C		B	
USA IN 643	D		D		D		D		D		D			X		X	D		D		D		C		D		C		C		C		C		B	
USA IN 663	D		D		D		D		D		D			X		X	D		D		D		C		D		C		C		C		C		B	
USA IN 658	D		D		D		D		D		D			X		X	D		D		D		C		D		C		C		C		C		B	
USA IN 662	D		D		D		D		D		D			X		X	D		D		D		C		D		C		C		C		C		B	

	208		209		213		214		215		216		217		218		219		221		229		230		231		232		233		234		235		238	
FD 300	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA	A	NA
JAN IN 457	D		D			X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X
JAN IN 458	D		D			X		X		X		X		X	D		D			X		X	D		C			X		X		X	B		A	
JAN IN 459	D		D			X		X		X		X		X	D		D			X		X	D		C			X		X		X	B		A	
US N 483B	D		D		D		D			X		X		X	D		D			X		X	D		C			X		X		X	B		A	
US N 485B	D		D		D		D			X		X		X	D		D			X		X	D		C			X		X		X	B		A	
US N 486B	D		D		D		D			X		X		X	D		D			X		X	D		C			X		X		X	B		A	

* This report reflects the present failure status of the weekly tests in Q.A. Lab. and does not determine final acceptance for military shipment.

Diode - High Voltage - San Rafael RD 11/6/62 Bialek Ferguson Moore Pante

Latest month:

150v, 1 ma (75v), 200v - 19%
150, 5 (125v), 200 - 40% additional (most
100, 5 (75v), 200 + 7% more
100, 1 (75v), 200 7% "

As of last May, this was 54% to 150, 1, 200.

200°C storage life data
80 diodes/week, 1000 hr

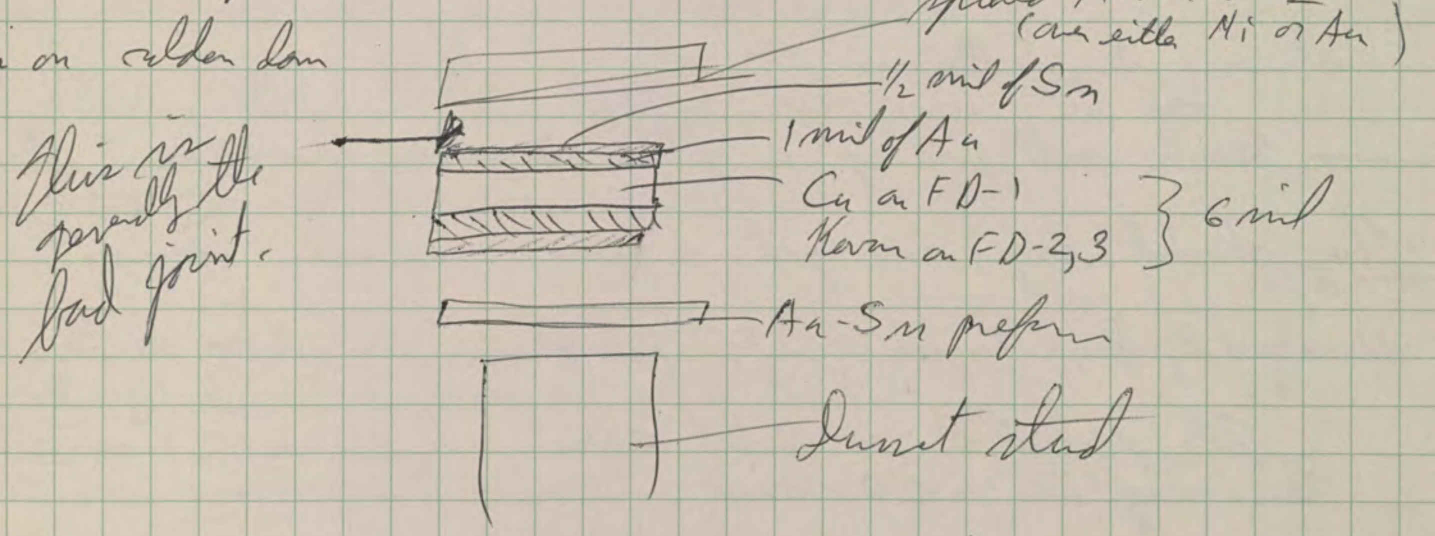
Vf catastrophic (100 mv or more change)

Vf		IR catastrophic	Op life: 80/wk Vf	Op life: 80/wk IR
2	1st week	0		
1	2nd wk	0	1	
1	3rd wk	0		1
8	4th	3		1
5	5th	1		2
0	6th	2		

~~Op~~ The FD-2's show the same Vf problem.

There is indication that solder down is bad on FD-3 — It bad on all products.

Materials on solder down



The FD-2's are same as FD-1's up to B diffusion

Types	BV	If
2	225	200
3	175	200

Data on a three-wafer split assembly run showed that the FD-3 problem was primarily associated with degradation during assembly.
Ag buttons gave 62% to 200v, 1ma, 200 ma
P.B. " 0% to " " "
T.C. " few % " " " "

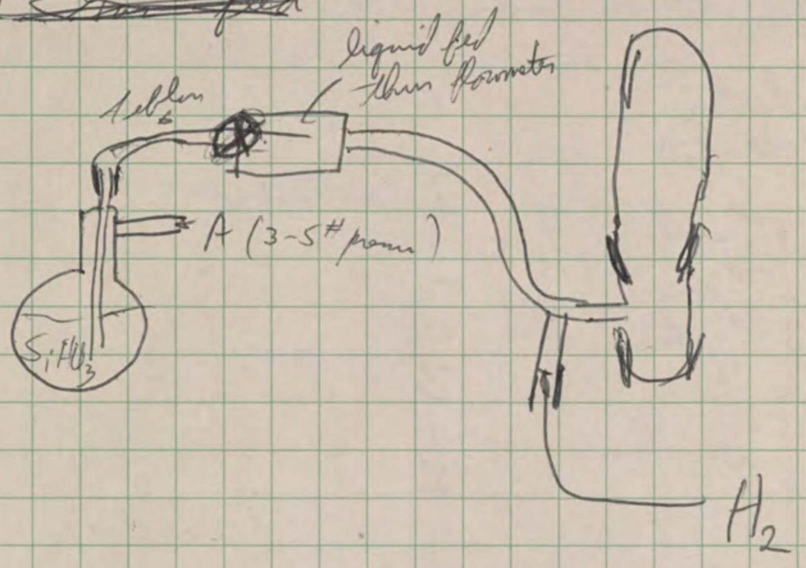
Epitaxial : Coordination Meeting 11/6/62

Cole
Schmidt
Shapton
:
:

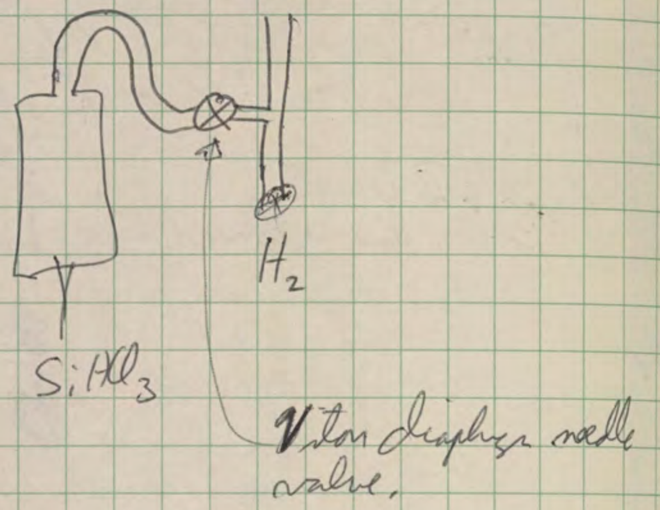
Wigton
Sah
[illegible]

Random or Prod.

Two ~~[illegible]~~ Systems :
1. Liquid feed -
2 ~~Gas feed~~



Corrected detail



H_2 from de-oxo and molecular sieve. - Get ~10ppm

$SiHCl_3$ is ~~not~~ used not distilled.

Schroeder in a strong $SiCl_4$ man)

— Hank will set up a still c̄ operating procedure at Sterling Rd.

— They should try to get a max inventory time.

It is probably cheaper to use quartz ~~[illegible]~~ flasks than to see if they are necessary.

The pedestal is etched approx every 5 runs. Eventually it cracks. This may be ~ 20 runs.

— The mandrel situation is confused. Hank and — will see that the situation is clarified by next time.

~~Purge~~ Trap :- Oil, - none - Purge is like ours - 3 pump down to ~1/2" pressure, then flush 10 min.

Heat cycle to run:
6 min preheat – at run temp (+5°) 1250 optical (often necessary to cool off and reheat)

They do not vapor etch now. It was hard to do because of complex valving. They did only the case where $SiHCl_3$ was added at the same time.

They had relatively little pyramid problem on the vapor etched stuff.

— Next time – lets look at vapor etch in more detail. Hank will get data from us.
They run much hotter than we do.

Substrate preparation:

Mtn View was 2 step of CP-6 $\bar{c}$ HAc. Gupta claims no pits. We use CP-8.

— Hank will look at same Gupta.. If they don't agree, bring sample.

Hank ~~[illegible]~~ says that As diffusion is ~5× ~~[illegible]~~ bulk in the film.

He still thinks that vapor phase Xfer of As is worse than Sb.

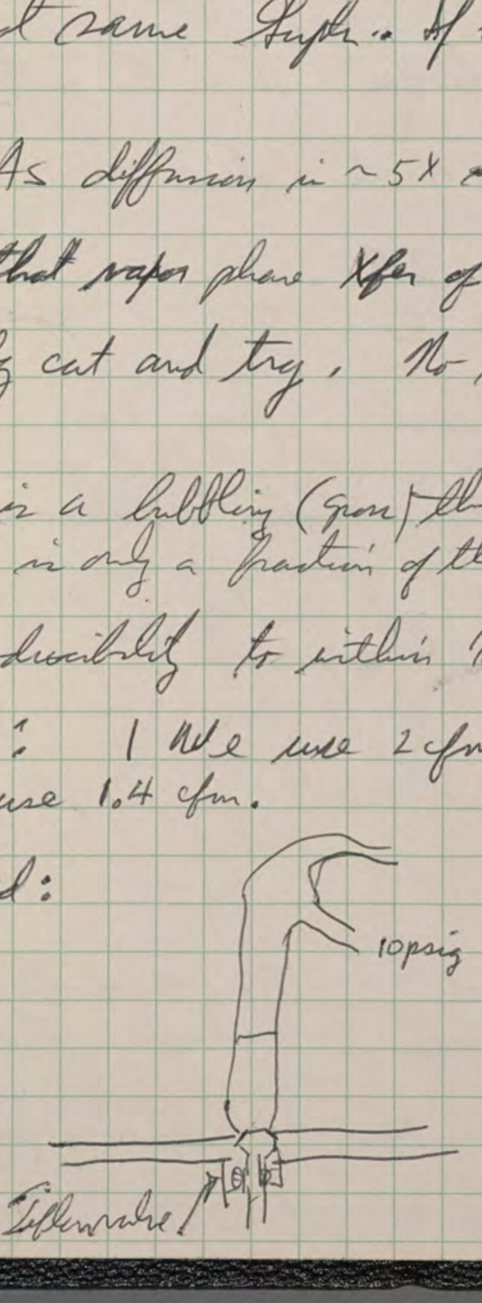
They mix stuff by cut and try. No specs.

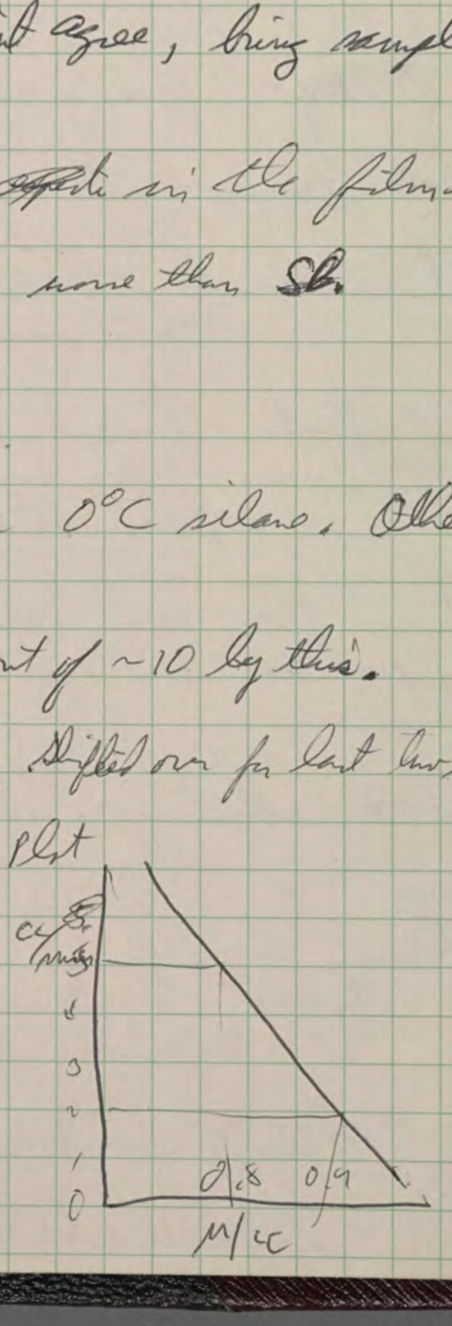
The gas phase is a bubbling (gross) through a 0°C silane. Otherwise it is the same. This is only a fraction of the H_2

They claim reproducibility to within ½ μ out of ~10 by this.

Differences in system: 1 We use 2 cfm, they shifted over for last two weeks, they used to use 1.4 cfm.

Hanks burette feed:





Hank is going to try Hg pump.

We have used Burnettes for ~ 7 MO.

If they aim at 1341 material, they ~~aim~~ get ~ 20% yield.

~~[illegible]~~

1341 – 60-80 volts, 6-10 μ. We need 150 substrates.
We will evaluate 5 wafers / run.
" " give them 5 " / run.

We will get substrates, ~~1~~75 by Fri. – 1500 μ, ~~[illegible]~~ unlapped.
Eval. wafers to Sterling by end of next.
Eval complete by two weeks from today.

Data for meeting, including evaluation of their 1341 runs made in the meantime.

Evaluation:

1 ~~They~~ – make mesa diodes, 10 in "S" pattern, average these.
Diffusion – base type a la Rodens.

2 Thickness: 90% ~~uses~~ IR.
Gupta says above 10μ the IR goes to pot

3 Rect. check – 4-point probe, pass 1 ma, if the voltage ~~is~~ across the center points goes high, reject as rectification.
Then stain, give diodes, etc.

Now every shift the mandrels get etched and this problem is virtually disappeared.

4. A subjective, visual inspection for anything that looks funny,

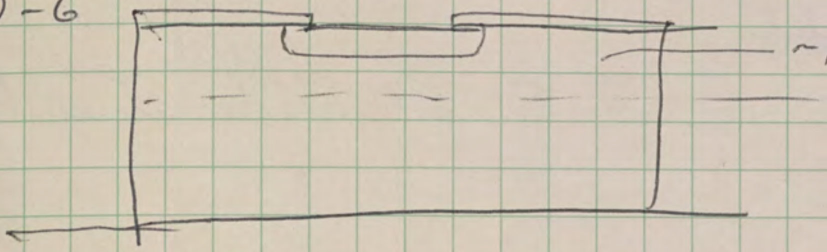
Ours:
Diode: Emitter pred. – 10 random diodes over ½ of the wafer,
We report the average ≥ 7 diodes that show avalanche

Thickness: IR when possible. – We have no good data to say yes or no.
— Look at the IR, try to explain the anomalous results. Wyler & Gupta.

Meeting on snap off diode. 11/7/62

Ferguson
Solt
Grinich
Moore

FD-6



~1Ω-cm (110v epitaxial), n ed 9-15μ

Au @ ~1040°C, 15 min (relatively low)

Selected for high conductance, high voltage; no good correlation.

Solt will hire a tech. He will be assigned to Grove in JPF's section where he will make devices to try. JPF will supply schedule. He will also get ADAM.

Metal-based Notes - 177

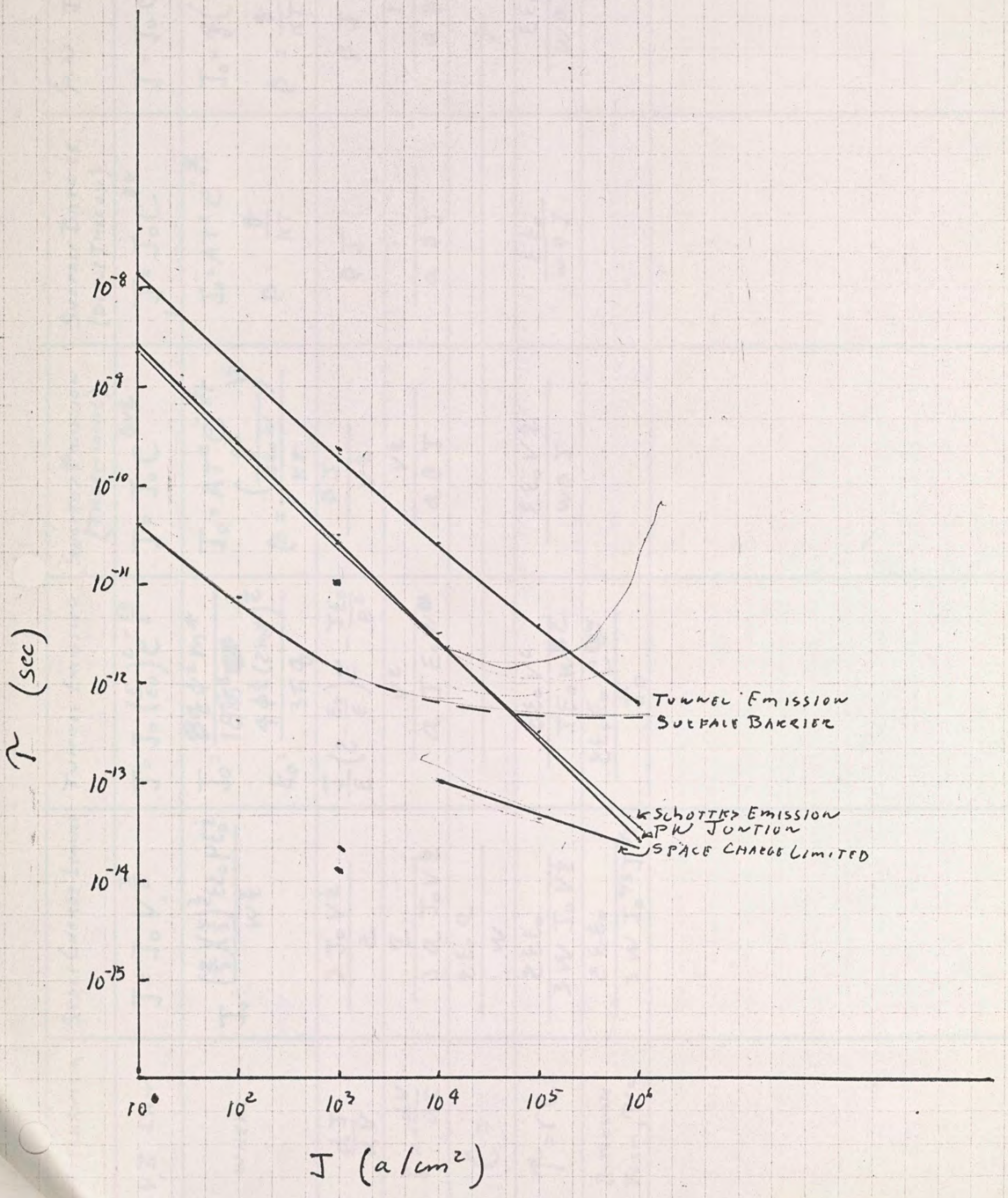
METAL BASE TRANSISTOR PROGRAM

	DESIGN THEORY	TECHNOLOGY	EVALUATION	CONTACTS
EMITTER	1. ADEQUATE FOR SCHOTTKY EMITTER	1. EVAP. AU ON CLEAVED SI. 2. EVAP. AU ON CLEAVED, OXIDIZED SI. 3. EVAP. AU ON PHOTORESISTED ETCHED SI. 4. GE INSTEAD OF SI. 5. DISPLACEMENT PLATE ON SI. 6. EVAP CDS. (REVERSE STRUCTURE)	1. I AND C VS V 2. PHOTO RESPONSE 3. DEVICES	1. EASY ON EPITAXIAL SI (TRANSISTOR TECH.)
BASE	1. ADEQUATE - REQUIRE VERY THIN FILM. PREFER GOLD	(SEE ABOVE)	1. ELECTRICAL RESISTIVITY 2. ELLIPSOMETERY 3. INFRA RED TRANSMISSION AND REFLECTION ON GLASS SLIDES	1. MAJOR PROBLEM a. METAL OVER OXIDE b. SAXENA EFFECT - bump in V/I characteristic
COLLECTOR	1. REQUIRE DESIGN THEORY AS TO REFLECTION AT COLLECTOR a. EFFECT OF BARRIER HEIGHT	1. EVAP. CDS. 2. REVERSE STRUCTURE (AU-SI). 3. EVAP. GE.	1. I AND C VS V 2. DEVICES	1. FOR CDS COLLECTOR - USE INDIUM (PHOTOCELL TECH.) 2. FOR REVERSE STRUCTURE USE TRANSISTOR TECH.

11-8-62 C A Bittmann

A N Saxena

Metal-Based Xster — 177



itter.

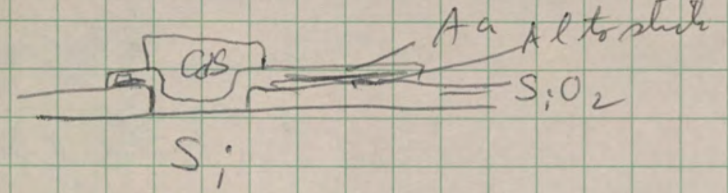
and

MECHANISM	SPACE CHARGE LIMITED	TUNNEL EMISSION	SCHOTTKY EMISSION (THERMIONIC)	SURFACE BARRIER (DIODE THEORY)	p-N JUNCTION
V,I LAW	$J = J_0 V^{\frac{3}{2}}$	$J = J_0 \left(\frac{E}{E_0}\right)^2 e^{-\frac{E_0}{E}}$	$J = J_0 e^{\beta V^{\frac{1}{2}}}$	$J = J_0 e^{\beta V}$	$J = J_0 e^{\beta V}$
WHERE	$J_0 = \frac{\left(\frac{2}{3}\right)\left(\frac{5}{3}\right)^{\frac{3}{2}} \varepsilon\varepsilon_0 \mu E_0^{\frac{1}{2}}}{W^{\frac{5}{2}}}$	$J_0 = \frac{8 q \phi^2 m^*}{18\pi\hbar^3}$ $E_0 = \frac{4\phi^{\frac{3}{2}}(2m^*)^{\frac{1}{2}}}{3\hbar q}$	$J_0 = AT^2 e^{-\frac{\phi}{kT}}$ $\beta = \frac{\left(\frac{q^3}{\varepsilon\varepsilon_0 W}\right)^{\frac{1}{2}}}{kT}$	$J_0 = AT^2 e^{-\frac{\phi}{kT}}$ $\beta = \frac{q}{kT}$	$J_0 = q\left(\frac{D_n n_p}{L_n} + \frac{D_p p_n}{L_p}\right)$ $\beta = \frac{q}{kT}$
$\frac{dJ}{dV}$	$\frac{3 J_0 V^{\frac{1}{2}}}{2}$	$\frac{J}{E}\left(2 - \frac{E_0}{E}\right) \cong -\frac{J E_0}{E^2}$	$\frac{\beta J}{V^{\frac{1}{2}}}$	βJ	βJ
$r = \frac{dV}{dI}$	$\frac{2}{3 a J_0 V^{\frac{1}{2}}}$	$\frac{V^2}{a J E_0 W}$	$\frac{V^{\frac{1}{2}}}{a \beta J}$	$\frac{1}{a \beta J}$	$\frac{1}{a \beta J}$
$C =$	$\frac{\varepsilon\varepsilon_0 a}{W}$	———	———	———	——→
$\tau = rC$	$\frac{2\varepsilon\varepsilon_0}{3 W J_0 V^{\frac{1}{2}}}$	$\frac{\varepsilon\varepsilon_0 V^2}{J E_0 W^2}$	$\frac{\varepsilon\varepsilon_0 V^{\frac{1}{2}}}{W \beta J}$	$\frac{\varepsilon\varepsilon_0}{W \beta J}$	$\frac{\varepsilon\varepsilon_0}{W \beta J}$
ALTERNATE FORM, $\tau =$	$\frac{2\varepsilon\varepsilon_0}{3 W J_0^{2/3} J^{1/3}}$	$\frac{\varepsilon\varepsilon_0 E_0 e^{\frac{E_0 W}{V}}}{J_0}$			

Metal-Lined Notes - 177

Metal-based Xster — 177

Sandman
Biltman
Sah



The Si will act as the emitter.

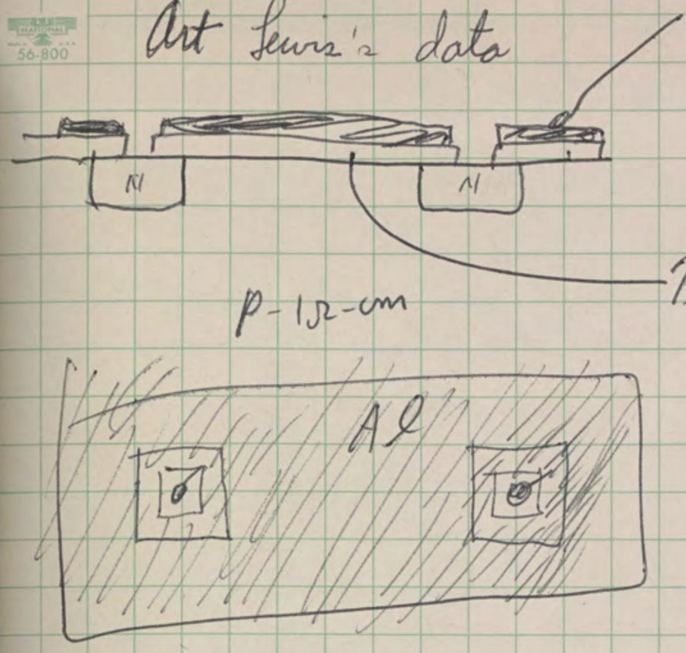
We have made barriers.

We will do photo response of barrier

By the time CTS comes back we will have samples and hopefully the photo response.

Charlie describes a transistor with a heavily doped base and a Schottky emitter.

Art Lewis's data



Thermal oxide here, anodically re-oxidized
The original thermal oxide was tapered by a HF dip.

The channel that had been under the thermal oxide

Preparation for ROBE meeting:

My summary of pipe problems:

Definition: A "pipe" is a defect in the structure where anomalous concentrations of impurities occur (either high, low or foreign) that result in such electrical problems as low breakdown or shorts at subsequent tests.

Found at:
Ide 70 D.S. Sources: (4200 type device)

✓ (✓) (✓) 1. Bad region in the original material

✓ (✓) (✓) 2. Contamination during etching and cleaning

✓ (✓) (✓) 3. Oxidization may concentrate impurities of crud-up spots
(✓) ✓ 3a. The water-bubbler effect.
? 4. There may be holes in the oxide

✓ 5. Spots of oxide left in clear field during 1st mask

(✓) ✓ 6. Incomplete cleaning during and especially after 1st mask to remove all residue

✓ 7. Pitting during base predep.

✓ 8. Pinholes in oxide near collector junction prior to emitter predep.
8a. a) KPR - film
b) Dust particles
c) Mask defects

✓ 9. Stress pinholes to short base to collector or base to emitter.

✓ 10. Emitter predep oxide penetration.

II.

NOV 13 1962

FAIRCHILD SEMICONDUCTOR DIVISION

Inter-Office Correspondence

To: D. E. Yost
cc: P. Hill
M. Oudewaal
P. Perry
November 13, 1962

From: R. Fouquet

Subject: Chromium Masks

We have run several tests of chromium masks on the 4200 line. The last set of 45 mil spaced masks was used approximately 2500 times before being discarded. Apparently, with frequent cleanings in production (with camels hair brush) and with chemical cleaning daily, perhaps 3000 is not unrealistic as a life time of the chromium mask.

While the life time appears satisfactory, pattern definition is a problem. With the chromium masks we see fringeing or scalloping, while emulsion masks run at the same time show clean, sharp patterns. This scalloping has been observed on the chromium masks themselves to some degree, but this fault reproduces on the wafers to an even greater extent, possibly due to halation associated with bright metal as compared to emulsion.

More extreme halation causes the KPR to mask more area than intended. This means bases, emitters, and oxide cut-out for metal are smaller than normal while the metal area itself is larger than normal.

The pictures accompaning this report illustrate these defects. The wafers shown were selected as being representative of those in process at the time. (We are not comparing the worst of chromium masks with the best of emulsion masks.)

Picture 1A is a fourth mask using an emulsion mask. It shows the usual clear patterns characteristic of the emulsion masks.

Picture 1B is a fourth mask using a chromium mask. In it can be seen the irregular patterns in first, second and fourth masks. What appears to be incomplete metal removal actually resulted from the KPR film over the metal being larger than normal due to the halation effect.

Picture 2A shows a third mask made with an emulsion mask.

Picture 2B is a third mask made with a chromium mask and again shows in close-up irregular pattern definition and scalloping.

Pictures 4 and 5 are of wafers made with chromium masks. They illustrate the results of halation in that the oxide cut-out at third mask is narrowed and the metal area at fourth mask is widened. In Picture 5, the KPR pattern has partly lifted leaving the 3rd mask cut-out exposed. In it one can see how much wider the metal base ring is than the oxide cut-out.

I have no information to indicate what effect, if any, the indistinct patterns have on die sort yield or on parameter distributions of the finished product. We will gather this information as these units get down to classification. Recent experience in process does indicate, however, that the chromium-masked wafers are more susceptible to lifting than the emulsion-masked wafers. This probably results from the fact that the pattern borders exposed by halation are not fully exposed and provide a place for lifting to start. I recommend that further work be done towards improving pattern definition before chromium masks are put in across the board.

R. Fouquet

R. Fouquet, Head
NPN Planar Section

Att.
RF/sm

FOR ROBIE

RECEIVED
NOV 21 1962
GORDON E. MOORE

FAIRCHILD SEMICONDUCTOR

Inter-Office Correspondence

To: G. Moore	Mountain View Technical File	November 16, 1962
D. Yost	R&D Technical File	

From: Paul Hill

Subject: Standardization Meeting Notes: November 13, 1962

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1) Chrome masks:

   a) Process for making chrome masks in a transfer to Mountain View (except glass preparation) with estimated November 30, as R&D mask making cut-off date.

   b) Results of 4200 chrome masks and major degradation factors:

      1. Accumulation of KPR giving poor contact

      2. Suggestion that contact would be more difficult due to very thin chrome image with respect to relatively thick emulsion image, 7 microns vs. 0.1 micron.

   c) Special plating on L-frames to permit chrome mask periodic clean up:

      1. Warm chromic acid is used to clean accumulations of KPR on masks about every 400 - 600 wafers.

      2. Mounted chrome masks can not be cleaned easily because L-frame will not tolerate chromic acid dip.

      3. Special plating on frame is being considered.

2) Implementation of "good practices":

   a) Process Development has incorporated a series of "good practices" in diffusion, masking, and wafer preparation.

   b) No runs have yet completed processing to die sort. Runs are 4200 and 1340 types.

3) Pipe Reduction (NPN types as test bed)

   Definition of pipe (G. Moore): local bulk or surface contamination at or very near a junction which generates a defective cb diode. Softs are not included in electrical criteria of pipe.

   Considered pipe generating areas (G. Moore):

      1. Bad regions in original material

      2. Contamination during etching to cleaning

      3. Contamination (or concentration of them) during oxidation which are deposited by steam, gases, water boilers, etc.

      4. Holes in oxide

5. Spots of oxide left in field after first mask:

    a. Pin holes in mask

    b. Incomplete KPR removal in cutout before etch.

6) Incomplete cleaning after first mask

7) Pitting during base diffusion and predeposition

8) Pinholes in oxide near collector functions prior to emitter predeposition:

    a) KPR film pin holes

    b) Dust particles (reproduced during exposure and development)

    c) Mask defects

9) Emitter predeposition oxide penetration (as functions of oxide thickness, pinholes, P_2O_5 condensate, etc.)

10) Nickel and emitter diffusion

    a) Nickel diffusion process

    b) Nickel plating solutions

    c) Evaporation vs. plating

Note: R&D will assume basic or fundamental work on all items above, and in particular items 1, 2, and 3.

Paul Hill

PH:ch

ROBE Meeting 11/13/62

Hill
Yost
Serg

Blome
Ferguson
McCall

Chrome masks:

Being set up in Mtn View
Criteria used for inspection is same as emulsion masks

Good practice to date data into one system in process development
or production techniques

Chrome masks give poor patterns after ~500 wafers. This is probably a dirt problem.

Next step is to verify that it is the KPR and not burning.
Clean up of masks is expected to help.

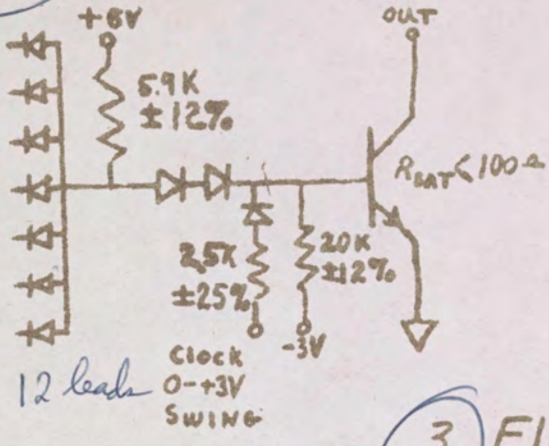
The program on p. 150 was laid out by me and discussed.
We will do our part.

≈800 □mils for R

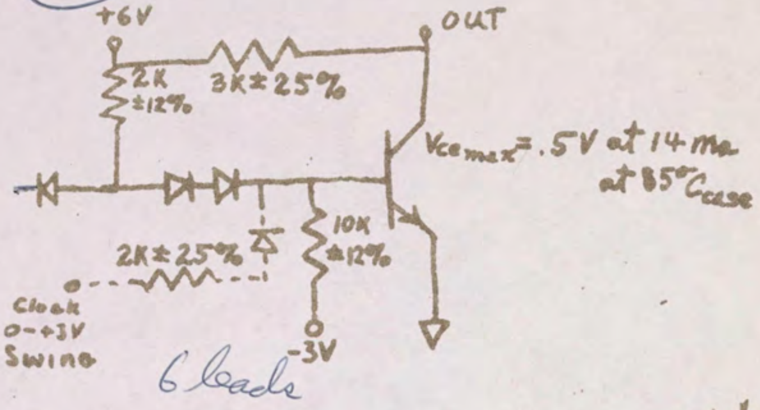
100 ns propagation delay
~~[illegible]~~ −40 to +115°C operation
150°C/watt (∞ heat sink)

170 □mils for R

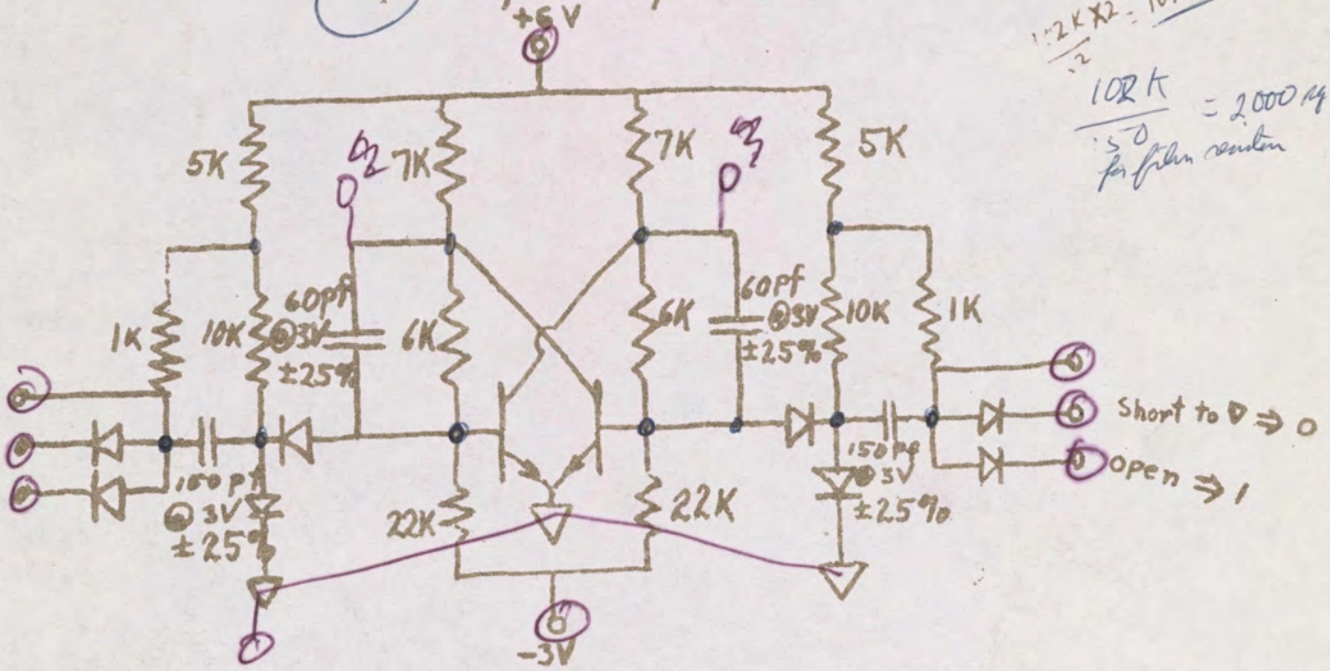
1 Low Gain Nand



2 High Gain Nand



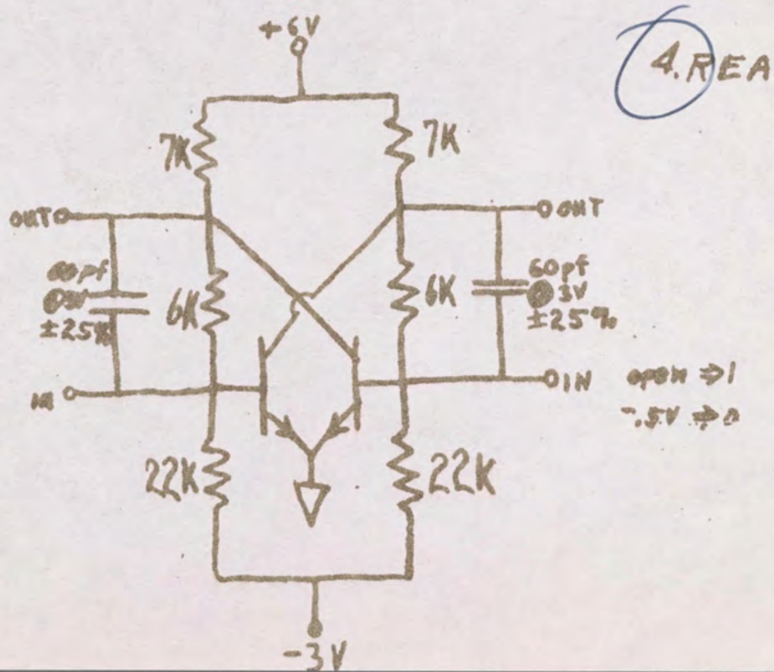
3 Flip Flop



1.2K × 2 / .2 = 1020 □mils for R

10ΩK / .50 = 2000 sq mil for film resistor

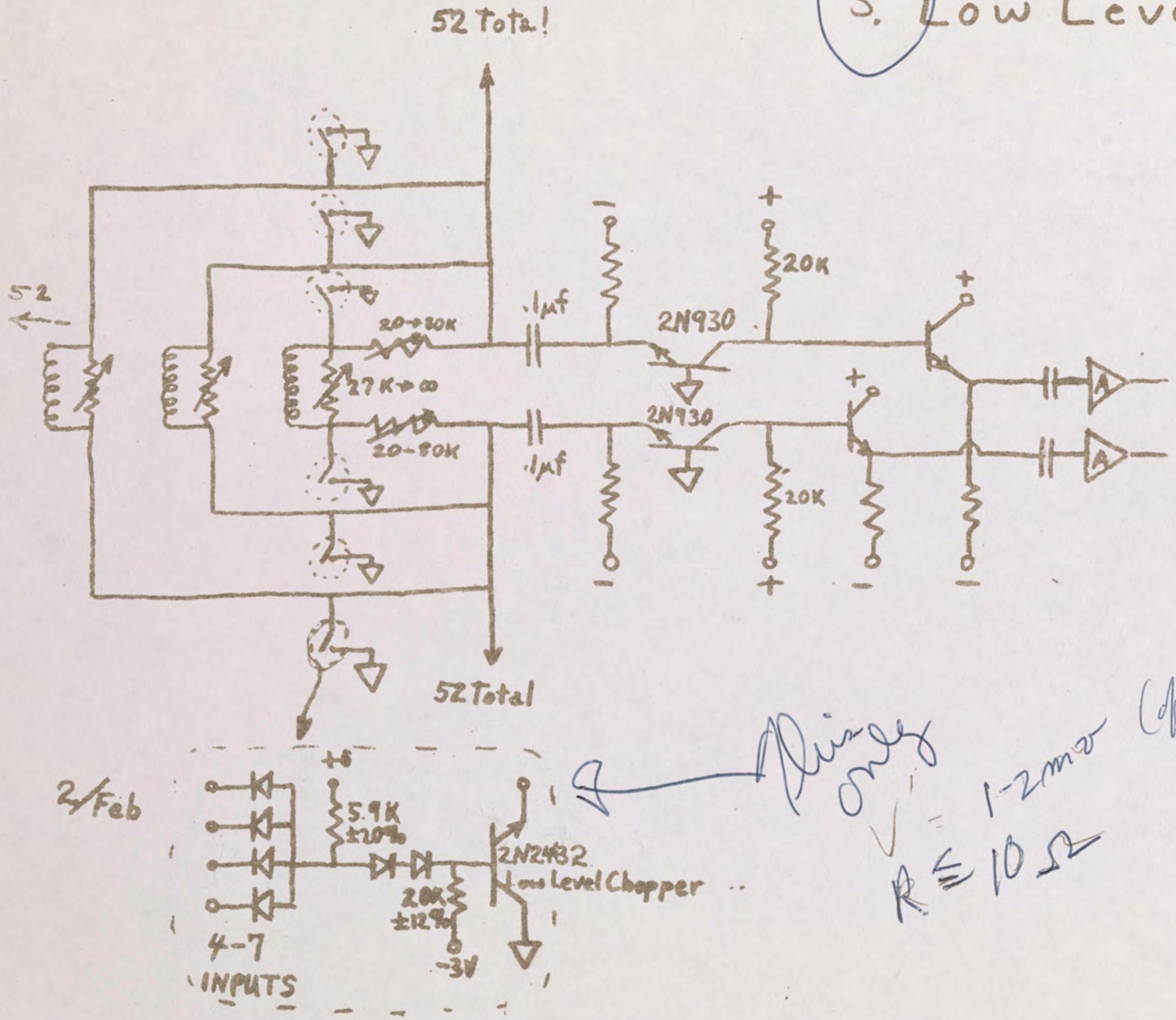
4. READ FLIP FLOP



Power Supply
tolerances ±5%

Resistor Values ±25%
unless otherwise
indicated

5. Low Level Switch

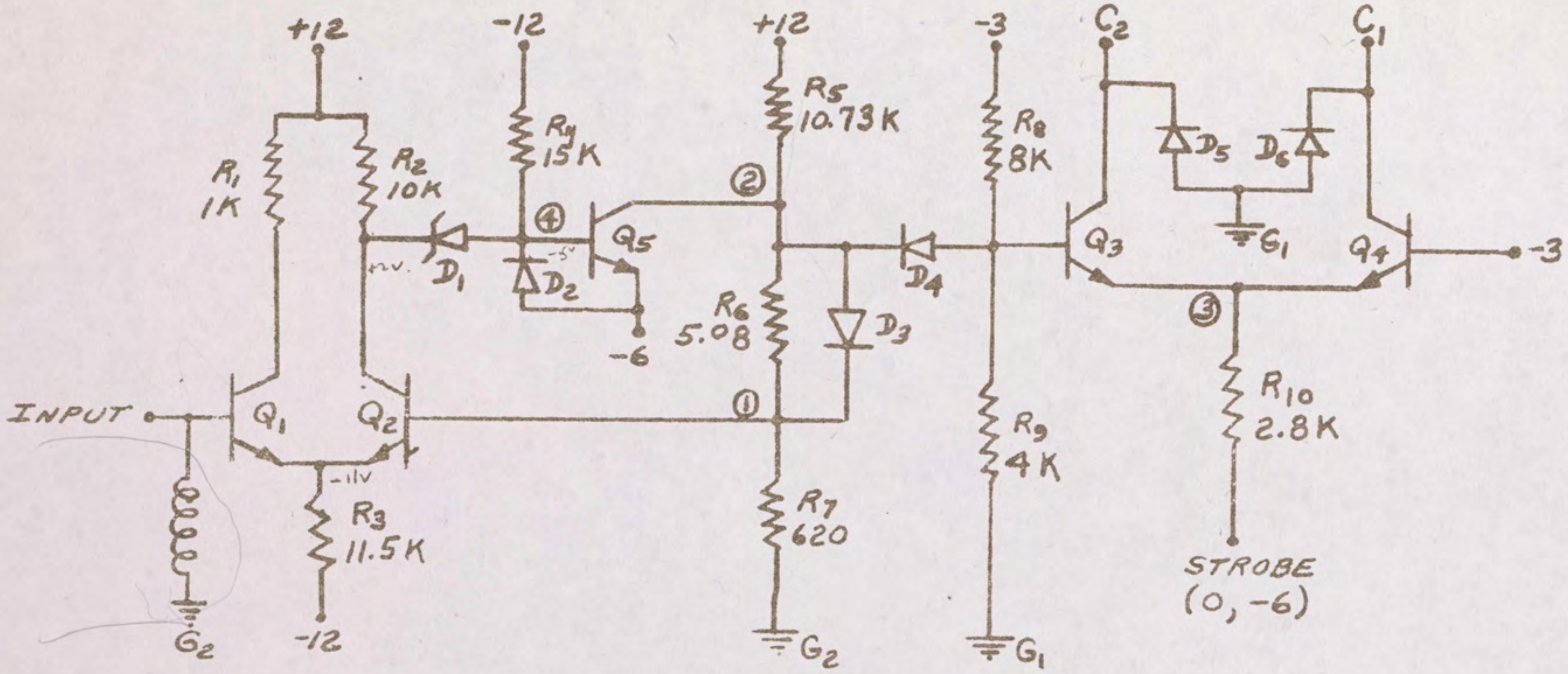


2/Feb

This only

V = 1-2mv Offset

R ≤ 10 Ω



① THROUGH ④ - TEST POINTS

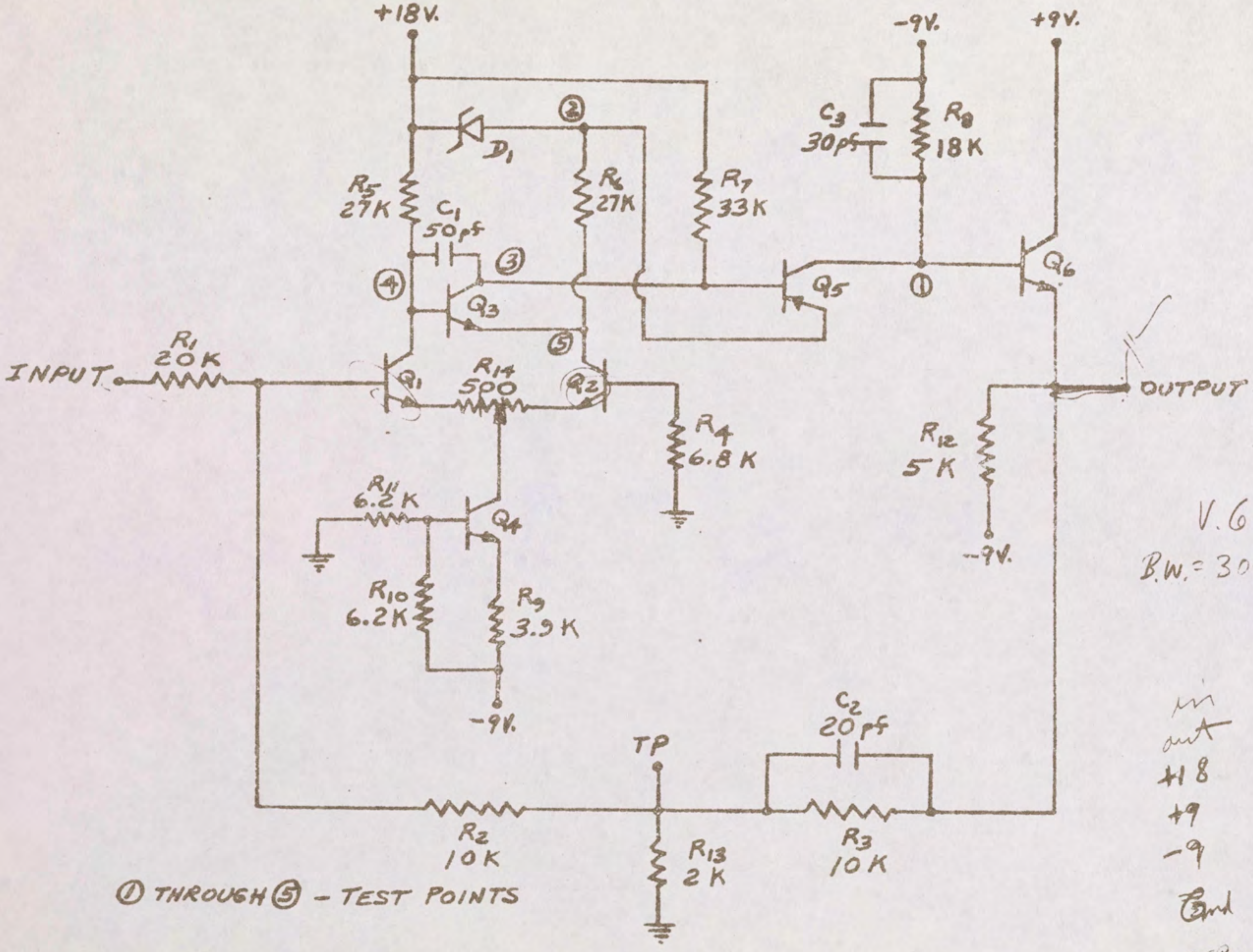
G_1 AND G_2 - ISOLATED GROUNDS

C_1 AND C_2 - OUTPUTS

FIGURE 1

6, SCHEMATIC - LEVEL DETECTOR & STROBE GATE

+12
-12
6
-3
G_1
G_2
in
out C_1
out C_2
strobe



① THROUGH ⑤ - TEST POINTS

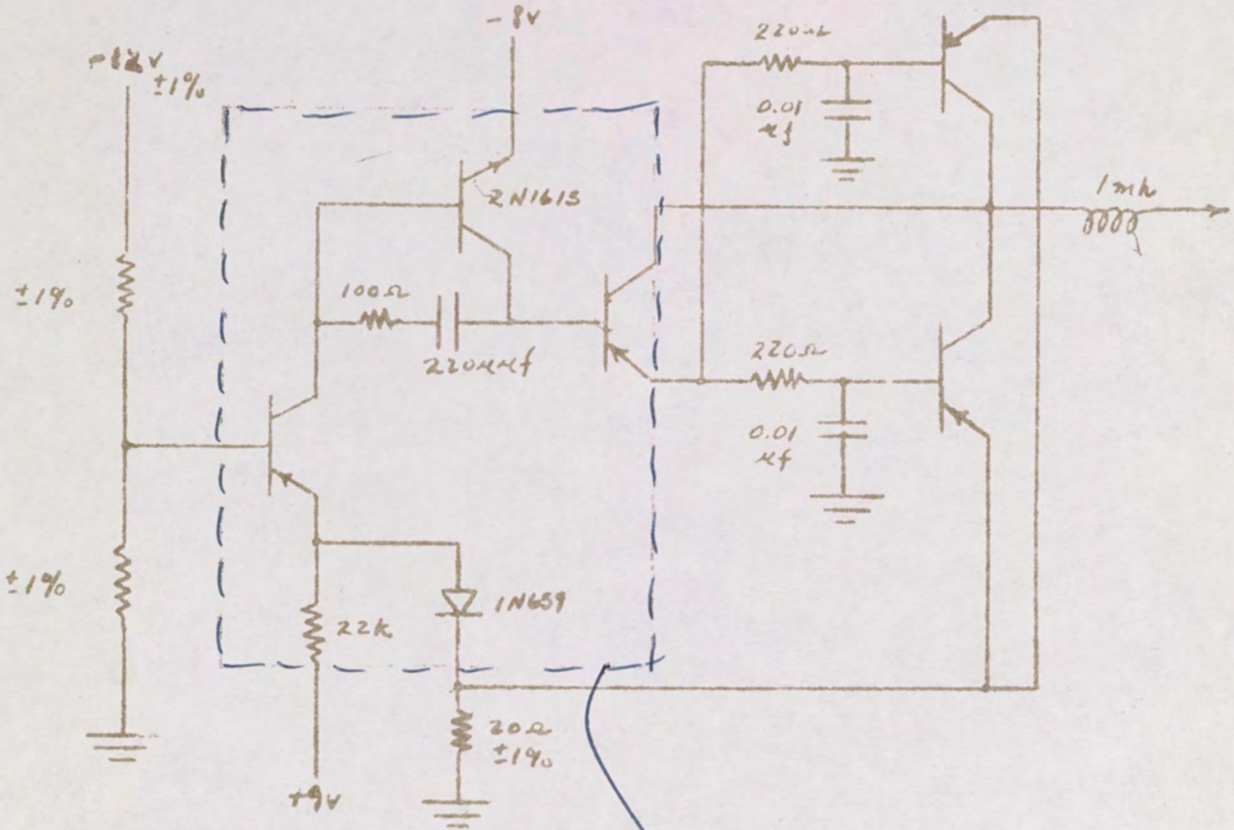
V.6 = 20

B.W. = 300kc

in
out
+18
+9
-9
Gnd
5TP

FIGURE 1

7. SCHEMATIC - READ PRE-AMPLIFIER

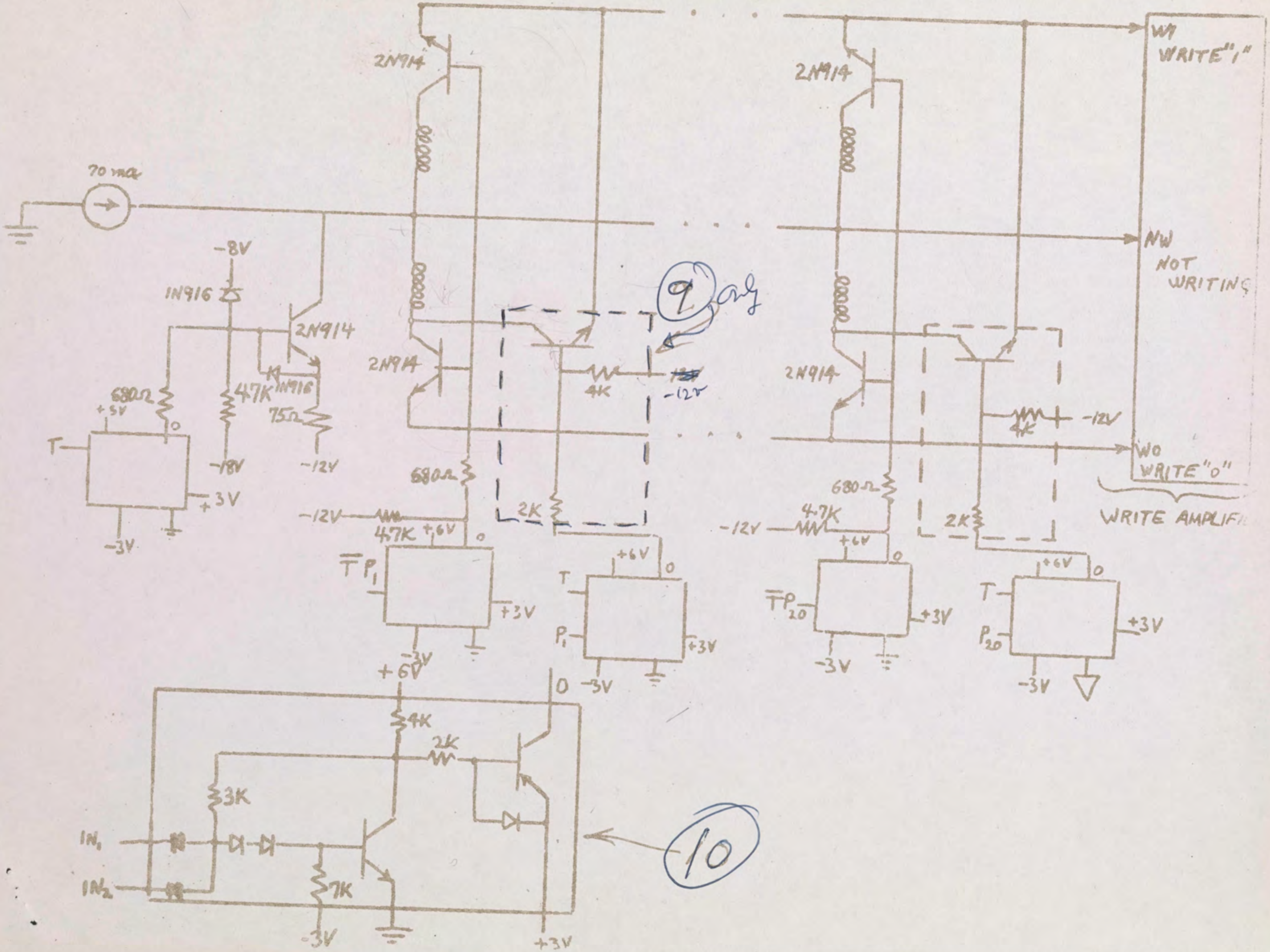


All PNP Transistors 2N1132

This only

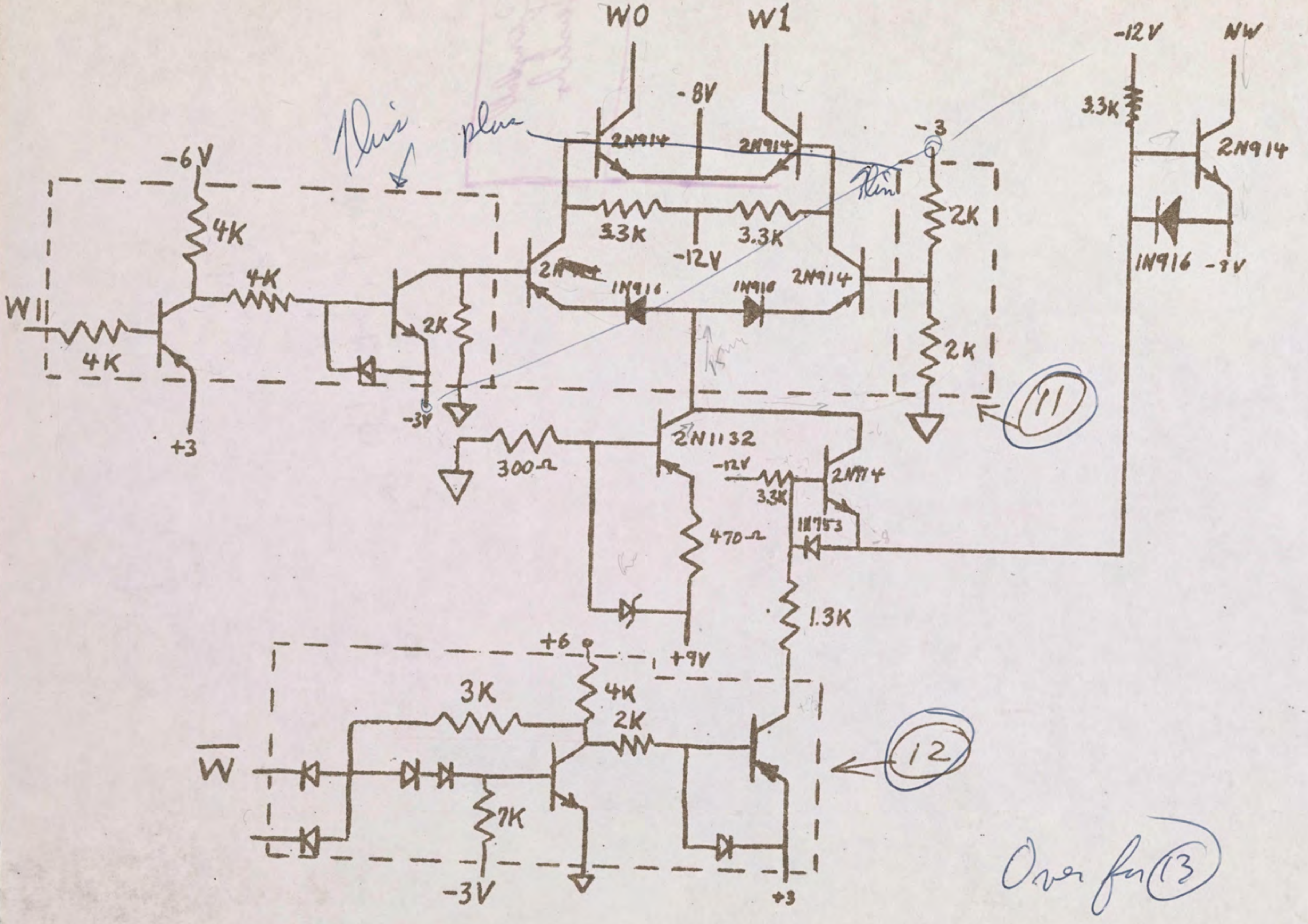
8- Figure 1 Diagram of 70 Milliampere Current Source

COLD STORAGE CHANNEL DIAGRAM



9 orig

10



This plus this

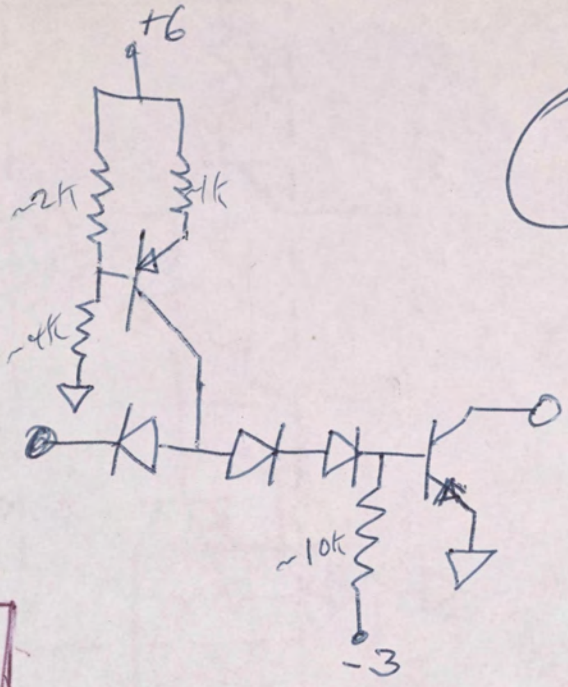
(11)

(12)

Over for (13)

Write Amplifier

13



Campbell
Leistiko