PREFACE

This is the first book to be written specifically on miniature constructions for electronic equipments; microminiaturization techniques have also been included because of their importance in future developments.

Electronic equipments have become smaller and smaller over the years for many reasons—increased complexity, reduction in space, reduction in weight, etc., and many miniature and subminiature valves and components have been developed to meet these requirements. Obvious uses for miniaturized electronic equipments are mobile computers, desk calculators, industrial control devices, aircraft and guided weapons systems, satellites and medical applications.

This book deals with the philosophy of miniaturization, space utilization and the construction of miniature equipments such as transistor receivers, deaf-aid amplifiers, medical electronic devices, etc. A chapter is also devoted to printed wiring and potted circuit techniques in view of their importance in miniaturization, and some examples of miniature potted constructions are given.

Because of the vital part played by the transistor in miniaturization and microminiaturization, the constructions of 34 types of transistors and diodes are described in simple outline form. Although there are many admirable books on semiconductors and transistor theory, these are mostly written by physicists for physicists and are necessarily too detailed for many electronic engineers who wish to obtain only a general knowledge of the working of the transistor. The authors have therefore included a simple theory in which mathematics are eschewed and physical processes are described in terms of charges moving through a crystal.

This book describes the three main systems of microminiaturization: micromodules (stacked individual components); microcircuits (flat or evaporated components); and solid circuits (integrated components or molecular electronics). Although developments in these techniques are rapid and changes inevitably take place, it is felt that this book will provide a basic background in the increasingly important field of miniaturization.
ACKNOWLEDGMENTS

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The views expressed in this book do not necessarily represent those of the Ministry of Aviation, and the authors have endeavoured to be impartial in their assessment of the techniques described.

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The R.C.A. DM0027A is a complete pulse amplifier stage intended for use in digital applications. This module incorporates a micro-element transistor in a common-emitter configuration. The DM0027A is driven into conduction by a negative pulse applied to the base of the transistor. The output is a positive, squared pulse which may be used in triggering applications. When driven by the R.C.A. DM0026B Pulse Shaper, the output amplifier may be used to trigger the R.C.A. DM0013A Binary Divider module.

Chapter 8

SOLID CIRCUITS OR THREE-DIMENSIONAL TECHNIQUES

The last of the three systems of microminiaturization to be described has a variety of names: solid state circuits, solid circuits, microelectronics, molecular engineering, molecular electronics, functional electronic blocks, moletronics, semiconductor networks and others. In this chapter, the term “solid circuit”* will be used.

The solid circuit technique of microminiaturization is more complex than the microcircuit and micromodule systems. However, provided the elements of semiconductor theory are known, solid circuits can be explained quite readily.

Semiconductor solid circuits are electronic devices formed in single crystal wafers of semiconductor. Each wafer performs the function of some standard circuit that uses several conventional active and passive components. Paths are fashioned on and through each wafer to produce active elements such as transistors, non-linear elements such as semiconductor diodes, and passive elements such as resistors, capacitors and distributed parameter networks. By changing the types of paths and their routes, an unlimited variety of circuits is possible. These circuits give the greatest reduction of size and weight of any of the microminiaturization systems so far described.

This chapter describes the technique and processes used in solid circuit technology, and concludes with descriptions of some solid circuits that have been produced to date.

The first published reference to possible solid-circuit techniques was made as long ago as 1952 by G. W. A. Dummer. Speaking at the Symposium on Progress in Quality Electronic Components held in Washington (see Bibliography) he said: “At this stage, I would like to take a peep into the future. With the advent of the transistor and the work in semiconductors generally, it seems now possible to envisage electronic equipment in a solid block with no connecting wires. The block may consist of layers of insulating, conducting, rectifying and amplifying materials, the electrical functions being connected directly by cutting out areas of the various layers.” Time has proved this prognostication to be correct.

* Since this chapter was written, it has been pointed out that the term “solid circuit” has now been registered as a trade mark of Texas Instruments Inc., Dallas, Texas, U.S.A.
Some Solid Circuit Elements

Although complex semiconductor devices may be analysed from the basic principles governing current flow in solids, their three-dimensional nature complicates the problem. The fact that accurate mathematical treatments are not available for many common transistor structures is an indication of the complexity of three-dimensional device mathematics. Consequently, there are no simple theoretical procedures that can be used to translate a desired circuit into a functional device.

For this reason, semiconductor solid circuits are designed by relating sections within a semiconductor to conventional circuit elements. Certain regions are considered as resistors, others as capacitors, or diodes, or transistors, or as any other device which can be formed from a semiconductor. Any number of such regions may be arranged to form a desired circuit. Since these regions may lie entirely within a single semiconductor wafer, the resulting structure is fully integrated.

Although it is often impossible to identify the individual regions in a functional device, this design concept (i.e. to talk in terms of known circuit elements) makes it possible to translate an existing circuit into an equivalent solid circuit. If electrical properties of the various regions are known, performance of the finished device can be calculated. As an alternative, the regions may be simulated with conventional components and the circuit bread-boarded for evaluation.

1. Resistors. The region between any pair of ohmic contacts on a homogeneous semiconductor will act like a resistor, where the equivalent value of resistance is a function of material resistivity, the length, and the cross-sectional area of the region, as in the equation

$$R = \frac{\rho l}{a}$$

where

- $\rho$ = the resistivity in $\Omega \text{ cm}$,
- $l$ = the length of the bar,
- $a$ = the cross-sectional area.

Such resistors are quite linear and closely follow Ohm's Law for the voltages encountered in transistor circuits. Since current conduction takes place within the bulk of the material, these resistors are not subject to many of the changes with time and load which occur in deposited thin films. With the proper selection of material, the resistance temperature coefficient may be accurately controlled. For example, if high-resistivity silicon is used, the resistance may increase by as much as 7,000 p.p.m./$^\circ$C; it will be less for heavily doped low-resistivity material.

Resistance regions may be formed from a uniformly doped wafer as shown in Fig. 8.1, or diffusion techniques may be used to produce a very thin surface layer of opposite conductivity type, shown in Fig. 8.2. In the latter, the resultant $p$–$n$ junction is a barrier that confines

![Fig. 8.1. Bar Resistor](image1)

![Fig. 8.2. Diffused Layer Resistors](image2)

(a) Oxide-masked diffused resistor. (b) Mesa-etched diffused resistor.
High-resistivity material is usually used for bulk resistors, while diffused-layer resistors may use very low-resistivity material. Resistors produced by either process are formed from single-crystal material. This means they have extremely good noise properties, because current conduction is entirely within one crystal (i.e., conduction does not take place between individual particles of resistance material). There is no absolute limit on the resistance value which may be produced by diffusion techniques; however, size restrictions and typical material resistivities make it desirable to limit maximum values to about 40,000 Ω for bulk resistors.

2. Variable Resistors. A method of fabricating a semiconductor variable resistor between electrodes A and B is shown in Fig. 8.3. The structure is essentially the same as that of the unipolar transistor described in Chapter 2. The resistance is determined by the spread of the space charge layer when the p-n junction control electrode is back-biased. As for the unipolar transistor, it is possible to obtain a very high resistance if the resistor channel is thin enough to permit pinch-off at high biases. The resistance is, of course, shunted by the junction capacitance.

3. Capacitors. Capacitors may be made with semiconductors by two methods. A p-n junction capacitor is shown in Fig. 8.4. As described in Chapter 1, a well-formed reverse-biased p-n junction has capacitance and low leakage current due to the separation of the charge carriers by the depletion layer at the junction. The capacitance obtained from a diffused junction is given by the relation

\[ C = AK(qa/12KV)^1 \]

where

- \( C \) = the capacitance in pF,
- \( A \) = the junction area in cm²,
- \( K \) = the dielectric constant,
- \( q \) = the electronic charge,
- \( a \) = the impurity gradient at the junction,
- \( V \) = the applied voltage in volts.

It will be noted that the capacitance is a function of the applied voltage. It is this property which is utilized to make variable capacitors for electronic tuning and other purposes. For many applications, however, this effect is a disadvantage. Furthermore, a solid circuit employing a p-n junction capacitance must be so arranged that the junction is always reverse biased under all conditions of operation. Should the p-n junction become forward biased the effect would be to short-circuit two parts of the circuit.

For silicon junctions with heavy doping on both sides of the junction, capacitance values up to 100,000 pF/cm² can be reached. Such capacitors would be useful only for low voltage working, as avalanche or Zener breakdown would occur with only a few volts applied. By decreasing the doping level on one side of the junction, capacitors capable of withstanding several hundred volts can be made; though these will provide only a few thousand pico-farads of capacitance/cm².

Junction capacitance, being dependent on the total number of ionized impurities, is substantially independent of temperature. In parallel with the junction capacitance there is the conductance of the junction which is about \( 5 \times 10^{-4} \) mhos/cm² under zero bias for a silicon unit, though much less at reverse biases. There is also the series resistance of the material beneath the junction which causes deterioration at high frequencies. High Q silicon junction capacitors are most easily obtained at frequencies less than 1 MHz.

The other type of silicon capacitor, shown in Fig. 8.5, is formed by thermally oxidizing the surface of the silicon wafer and using this oxide layer as the dielectric. Because the oxide is formed on a single-crystal substrate, it is unusually free of defects. The top counter electrode is a metal film deposited through a suitable mask by vacuum evaporation. Capacitors with an 8,000 Å silicon oxide layer have been made which withstand 90 V without breaking down. The oxide formed is thought
to be silicon dioxide, which is very stable with temperature. Tests
have shown that the temperature characteristic of these capacitors
is quite flat up to 150°C. The dielectric content of silicon dioxide is rather
low, about 4-5 per cent, but even so, capacitors up to 10,000 pF/cm² can
be readily obtained.

The big advantage of these capacitors compared with the junction
capacitors is their relative insensitivity to changes in applied voltage.
Furthermore they are non-polar. For these reasons, silicon dioxide
capacitors are preferred in solid circuits where particularly stable
elements are required.

4. Distributed Parameter Networks. Distributed parameter networks
have been described in Chapter 6 with reference to microcircuit con-
structions. These networks can also be made in a semiconductor and
used in solid circuits. A distributed parameter R.C. network is shown
in Fig. 8.6. This uses a p-n junction capacitor which must be main-
tained at a reverse bias when used operationally. An alternative
construction is to use a silicon oxide capacitor of the kind shown in
Fig. 8.5, which has the advantage of being non-polar.

Such elements may be used as a phase-shifting network, a low-pass
filter for a signal entering terminals AC and leaving terminals BC or,
by connecting terminals B and C, as an easily made resistance with a
by-pass capacitance. The theory of the network is a simplification of
general transmission line theory, since leakage conductance and
inductance can frequently be neglected.

It is evident that, by suitably shaping the semiconductor wafer,
the counter-electrode or the diffused layer, many variations on the
simple R.C. distributed parameter network are possible.

5. Inductors. The remaining passive circuit element to be dis-
cussed is the inductor. Inductance is a measure of flux-linkages per unit
current. Since a finite volume is required to link lines of flux, it is
difficult to imagine an inductor comparable in size to a match-head.

One possible solution is to simulate the required function. For
example, semiconductor delay lines may be used to replace an inductor
in a time-delay circuit. R.C. networks may be used in place of L.C.
tuned circuits; field-effect devices may replace chokes; or impedance
matching by circuit design may replace transformers. Also, a small
spiral of semiconductor material may be built actually to realize an
inductor. However, when henries of inductance are necessary or if the
skirt selectivity of an L.C. network cannot be sacrificed, the best solution
is to build a hybrid unit which combines a solid circuit with a separate
inductor.

6. Transistors. In principle, nearly all types of transistors can be
incorporated in a solid circuit. A very convenient type is the diffused-
base transistor, because it requires only a single diffusion and is thus
compatible with the rest of the solid-circuit elements. This transistor,
which has been described in Chapter 2 is shown in cross-sectional view
in Fig. 8.7. A three-dimensional diagram of the transistor die is
illustrated in Fig. 8.15.

Briefly, the processes in making a diffused base transistor are as
follows. A silicon wafer is subjected to a controlled diffusion cycle to
obtain a diffused layer of known depth and impurity gradient. Then,
by masking and evaporation, small-area emitter and collector electrodes
are deposited on the surface and lightly alloyed. Assuming a p-type
parent crystal and an n-type diffused layer, then a suitable emitter
the electrode would be of aluminium to give a p-n junction after alloying, and a suitable base electrode would be of doped gold to give an n-n+ junction. Typical areas of the emitter and base electrodes are $1 \times 3$ mils. The region round the electrodes is masked, and the wafer is etched to isolate the transistor and make a small-area collector junction. Connexions can be made to the top electrodes by thermo-compression bonding. The collector region, being the body of the semiconductor, is automatically joined to the rest of the solid circuit.

The diffusion process is extremely flexible and is currently used in transistor manufacture to produce some of the highest power units and some of the highest frequency units. Furthermore, it is potentially the cheapest method of transistor fabrication.

Diffused emitter and base transistors and alloy transistors (see Chapter 2) could also be used in solid circuits. The former has the disadvantage of requiring more than one diffusion, and the latter adds some complications to the layout of the circuit.

7. Diodes. Without doubt, the most suitable diode for solid-circuit application is the diffused type. As described in Chapter 2 and shown in Fig. 8.8 (a), the diode requires a single diffused layer. The fabrication process is similar to that used for a diffused base transistor except that only one electrode is deposited and alloyed. Connexion has to be made to this electrode, the other side of the junction being an integral part of the solid circuit.

Another type of diode is shown in Fig. 8.8 (b). This is an alloy junction on the diffused layer and corresponds to the emitter diode of the aforementioned transistor. This diode may be used in conjunction with a surface resistive layer. Because of the high doping concentrations on each side of the junction the surface alloyed diode has a breakdown voltage which may be as low as 1 V. This contrasts with the previous diode which, being a junction between the diffused layer and the parent crystal, may have a high breakdown voltage.
Diodes produced by alloying directly to the parent semiconductor can also be incorporated in solid circuits, but they are not so convenient as they require another processing stage.

Many other types of devices may be formed in a solid circuit. For instance, unipolar transistors, tunnel diodes, p-n-p-n devices, solar cells and thermo-electric elements are all possible.

8. Solid-circuit Components. The various component parts of solid circuits described in this section are shown together in Fig. 8.9. These represent, of course, only a few of the possible components that can be incorporated in a solid circuit, in particular many other types of active components are possible.

Fabrication

(The contents of this section and those on "Design Example" and "Interconnexions and Sub-assemblies" are based on an article by the staff of Texas Instruments Inc. and are printed here by permission of Electronics, a McGraw-Hill publication.)

The processes used in fabricating any semiconductor device are largely determined by yield considerations consistent with the desired operating characteristics of the finished unit. These characteristics include not only the electrical parameters, but such items as reliability and temperature stabilization. In fabricating solid circuits there are two additional considerations: design versatility and functional optimization. Since each solid circuit is a complete circuit rather than a single component, an almost infinite variety of designs is possible. In order to satisfy any percentage of the possible applications a large number of different types needs to be fabricated.

Solid-circuit construction processes must therefore lend themselves to design change without costly and time-consuming mechanical tooling. On the other hand, the processes must allow the circuit to be functionally optimized. Complete optimization of a transistor is always opposed by design compromises. For example, the transistor designer must compromise between low base resistance and high current gain. The circuit designer, however, may use transistors with both low base resistance and high current gain in the same circuit to achieve better performance. For the same degree of optimization in a solid circuit, both transistor characteristics must be fabricated on the same semiconductor wafer. This introduces an additional degree of process control that is not necessary in conventional transistor production.

To meet the foregoing considerations unconditionally and make practical the production of solid circuits, unique combinations of techniques which include photographic resist, oxide masking, and gaseous diffusion have been used. Although many of these techniques have been used in mesa transistor fabrication, their full technological capability becomes apparent in solid circuits.

The sequence of operations outlined in Fig. 8.10 will be recognized by semiconductor-device engineers as being applicable to many types of devices. Since the basic techniques are well known, they will be only briefly reviewed here; the major emphasis will be placed on their adaptation to solid circuits. It is significant to note the steps in which the units are simultaneously processed versus those in which they are individually processed. For uniformity, reliability and good yield, as many of the steps as possible should involve simultaneous processing, i.e. fabrication of large numbers of units at the same time under the same conditions and on the same wafer.

1. Material Preparation. The semiconductor material is grown as a single crystal and then sliced, lapped, and polished in exactly the same way as other devices. This processing step can be eliminated if dendritic crystals become economical to produce. Whereas both silicon and germanium have been used for solid circuits, silicon seems to be superior because of higher intrinsic resistance, ease of forming selective masking against diffusion and better results in surface stabilization. Diffusion masks have been formed on germanium by using evaporated coatings, but this adds complexity to the operation. The discussions will therefore be limited to the use of silicon material.

For a given geometry, resistivity of the starting material affects the value of any bulk resistors in the finished device; therefore, material resistivity must be accurately controlled. Material resistivities around 10 Ω-cm are quite satisfactory for the resistance values found in most computer-type applications. Also, resistivities in this range have been quite insensitive to subsequent processing.
2. Junction Formation. Controlled amounts of impurities must be introduced into a bulk semi-conductor to form p-n junctions. Two common techniques for adding these impurities are alloying and diffusion. In alloying, an impurity metal such as aluminium is first deposited on the semiconductor surface. The wafer is then heated to melt the metal and dissolve some of the semiconductor. Upon cooling, the molten region solidifies in single-crystal form with the same orientation as the original semiconductor. Included in the crystalline lattice of the recrystallized region are impurities of the deposited metal which give the recrystallized region the desired conductivity type. For p-n junction formation this would be a type opposite to the bulk type. Because alloying is a melting and freezing process, it occurs quite rapidly and is somewhat difficult to control in depth. The amount of impurity included in the recrystallized layer is a function of the metallurgical properties of the metal-semiconductor system (phase diagram) plus the thermodynamics of the heat cycle (departures from equilibrium). In practice, these considerations limit the impurity concentrations to a rather narrow range of values.

Diffusion, as contrasted with alloying, is a relatively slow method of introducing impurities into a semiconductor so that better depth and concentration control are obtained. The diffusion process consists of heating the silicon to approximately 1,200°C in the presence of an impurity gas. The gaseous impurities strike the surface and diffuse into the wafer to form an n- or p-type layer, depending on the characteristics of the impurity. In diffusing n-type junctions into p-type (parent) silicon the diffusant may be antimony, arsenic, bismuth or phosphorus. In diffusing p-type junctions into n-type (parent) silicon the diffusant may be aluminium, boron, gallium, indium or thallium. Selection of a particular diffusant depends on the penetration and surface concentration of impurity atoms required. Different impurities diffuse at different rates; thus, two impurities may be diffused simultaneously to form two p-n junctions at the same time. Diffused junction depths in silicon may be accurately controlled from hundredths of a mil to several mils.

In order to control the surface concentration it is necessary to control the number of impurity atoms which reach the silicon surface during the diffusion cycle. This can be done by vacuum sealing the diffusant together with the wafers in a tube (closed-tube method); or by controlling the temperature, hence the vapour pressure, of the diffusant independent of the silicon temperature (open-tube method); or by applying the diffusant direct to the wafers before heating (“paint-on” method). Each diffusion technique has certain advantages. The particular method used depends on the device to be fabricated and the accuracy that is needed to secure good control on the device parameters.

A closed-tube diffusion furnace is sketched in Fig. 8.11. The silicon wafers are placed in the quartz capsule, the spacer is inserted, and then the small quartz boat containing the diffusant is inserted. The quartz tube is then evacuated, sealed, and placed in a furnace so that the wafers and diffusant are at the same temperature.

A sketch of open-tube diffusion equipment is shown in Fig. 8.12. Open-tube diffusion requires two furnaces in tandem. The smaller furnace is the source furnace and the larger furnace is the diffusion furnace. A carrier gas—argon, hydrogen, nitrogen, or oxygen—flows at a controlled rate into the quartz furnace tube at the source-furnace inlet side. The diffusant is heated in the source furnace and evaporates at a controlled rate. The “carrier” gas picks up the diffusant as it
passes over the heated source boat and carries it to the heated semiconductor wafers where it is deposited. The wafers are at a higher temperature than the evaporating diffusant. Temperature is controlled in both the source and diffusion furnaces with the same accuracy as in the closed-tube system.

The “paint-on” method utilizes a diffusant-enriched solution which is painted on the semiconductor wafers. In some cases the wafers may be dipped into the solution. The wafer is then placed in a furnace and diffusion occurs at an elevated temperature.

3. Oxide Masking. The junction area of alloyed devices can be controlled by limiting the regions where the impurity metal is deposited. In diffused structures the junction areas may be controlled by forming an oxide mask on the silicon (Frosh and Derick, see Bibliography). If silicon is heated in an oxidizing atmosphere, the resultant layer of oxide will mask against diffusion impurities such as boron and phosphorus. By selective removal of this silicon oxide layer, which forms uniformly over the surface, area control of the diffused layers can be achieved.

The selective removal of an oxide mask is accomplished by photo-etching techniques similar to that used in making etched-circuit boards. This process is illustrated schematically in Fig. 8.13. The photographic resist is applied in liquid form, usually by dipping. After drying, the resist forms a thin plastic film which is photographically sensitive to ultra-violet light. Exposure is accomplished by contact printing through a photographic negative that has been produced by laying out the desired pattern at 50 to 100 times actual size and then photographically reducing it. Thus, the only “tooling” required to produce a different oxide mask is to change the photographic negative.

An exposure jig permits alignment of the negative with respect to patterns already on the wafer. Exposure of the photo-resist causes it to be insoluble in the developer. Therefore, resist under the opaque areas of the negative will be removed by the developer, while resist under the clear areas will remain. If the wafer is now placed in a hydrofluoric acid bath, the oxide will be removed where it is unprotected by the resist. Hydrofluoric acid attacks only silicon oxide, and not the underlying silicon or the photo-resist.

In addition to controlling the junction geometry, oxide masking may also be used to control the impurity concentrations. By oxide masking certain areas during only part of the diffusion cycle, while exposing others during the entire cycle, surface layers of different concentrations and depths may be obtained. For example, a series of diodes having different breakdown voltages can be formed on the same wafer.

4. Contact Attachment. The active areas are completed once the junctions have been formed. In the finished device, electrical connections must be made to these various p- or n-type layers and to the bulk material. Often, the current path is through the semiconductor itself, but ultimately some outside connexion is required. Two steps are involved in making these connexions: first, a non-rectifying low-resistance metallic contact is made to the semiconductor; second, leads are attached to these contacts. The contacts are made by depositing metal on the semiconductor surface and then forming an alloy by heat treatment. This is the same process previously discussed for making alloyed p–n junctions, only in this case the impurity metal involved is of the same conductivity type as the semiconductor. Thus, p–p⁺ or n–n⁺ junctions are formed (the + notation indicates a much higher impurity concentration).

This process, like the others involved in semiconductor network fabrication, is easy to change for different designs. The contact placement will be different for each type of circuit, and the metals will
vary with the conductivity type of the semiconductor layers. Fortunately, both electrochemical and vacuum deposition may be adapted to this requirement by using photo-processing techniques. For electroplating metals, a photo-resist mask can be photographically formed directly on the unoxidized semiconductor. The resist mask then confines the current flow, hence the deposition, to only those areas not masked. Vacuum deposition is done most conveniently through a metal mask that limits the deposited contacts to those areas not covered by the mask. Metal masks are etched from thin sheet stock using a photo-resist coating to limit the etching. Here again, the only change in “tooling” for a new circuit is a new photographic negative.

5. Wafer Shaping. After forming the junctions and making the contacts, the wafers may be separated into individual pieces having the required geometry. This geometry is largely determined by the desired current paths within the semiconductor and will vary from one circuit design to another. Sawing, or scribing and breaking the wafers, are logical methods of separation, but they are limited to straight-line geometry. Ultrasonic cutting is possible; but it requires expensive tooling for design changes. A satisfactory technique is to etch the units apart, using photographic processing. In particular, a photo-resist mask is applied as in the oxide removal procedure of Fig. 8.13, but an etch that will attack the silicon is used. The wafer is etched completely through where it is not protected by the resist, thus separating the units. At this step in the process, mesa areas are facilitated, where desired, by etching away unwanted diffused layers. The examples in Fig. 8.14 illustrate the complexity of design that can be accomplished by photo-etching techniques.

6. Lead Attachment. The individual units are now ready to have leads attached. For the bulk material, the leads can be Kovar strips upon which the unit rests. For the diffused layers, lead wires are thermal-compression-bonded to the deposited and alloyed contacts. The Kovar strips are formed in a picture-frame assembly by photo-etch techniques as illustrated in Fig. 8.15. Different circuits may require a different placement of the leads, and by using photo-etch fabrication the need for costly stamping dies is eliminated.

A mounting base, which corresponds to the header of a conventional transistor, is formed by sandwiching the Kovar lead-frame between a ceramic and a Kovar ring. Conventional high-temperature glass-to-metal sealing techniques are used for this step. After firing, the leads are gold plated and the individual silicon units are placed in position. The units are then run through an alloying cycle to bond the semiconductor to the gold-plated Kovar. In a conventional mesa transistor this step would correspond to alloying the collector to the header.

7. Thermo-compression Bonding. Connections between different points of a solid circuit and between the solid-circuit blocks themselves are often made with thin (~1 mil) wires attached to the wafer by a process called thermo-compression bonding.

As described by Christensen (see Bibliography) the process involves heating the wire and the semiconductor while pressing the wire with a wedge as shown in Fig. 8.16. A 5,000 to 10,000 lb/in² pressure, 200° to 300°C temperature range and a 5 sec time interval are appropriate conditions for forming a bond between a gold wire and a block of germanium. Similar conditions apply for bonding to silicon. Bonds of gold, silver, aluminium and various alloys of these metals may be made directly to the semiconductor or to a plated area on the semiconductor. The bonding action does not involve melting the materials as in an alloy cycle, and the penetration of the wire into the semiconductor is very slight; this makes the process ideal for connecting wires to a diffused layer a few microns thick. The bonds are very strong, and when a bonded wire is pulled, either the wire breaks or a bit of the semiconductor is pulled away from the surface; the bond itself remains intact. Using a wire containing donor or acceptor impurities it is
possible to make n-n+ or p-n junctions with n-type germanium and
p-n or p-p+ junctions with p-type germanium.

The principal use of thermo-compression bonding is in diffused
transistor production, but it lends itself admirably to solid-circuit
fabrication.

8. Packaging. The "header" to which the semiconductor pieces are
fastened is also part of the package. The assembly must be hermetically
sealed in a suitable manner for protection against adverse ambient

atmospheres. Probably the best method is to seal in a separate can,
but other possibilities exist. This step in the fabrication process is
probably the most important because on it depends, to a large extent,
the ultimate reliability of the unit.

**Design Example**

In designing a solid circuit the material and diffused layers are chosen
to produce an optimum transistor structure for the particular circuit
application. Since the transistor is an integral part of the circuit, exact
operating conditions are known. Thus, the transistor design may be
accurately tailored to a particular application, which reduces the
required number of compromises. This procedure may be used to
improve the performance of a circuit or to maximize the yield of
acceptable devices. For circuits requiring both transistors and diodes,
the normal design procedure is still to optimize transistor performance.

The diode characteristic of an emitter-base junction usually differs
from that of a collector-base junction. In particular, the emitter
junction is relatively abrupt and has a low breakdown voltage, while
the collector junction is more gradual and may have a high breakdown
voltage. At the same time that each transistor junction is being
formed by diffusion, any number of individual diodes (with character-
tistics like either of the transistor junctions) may be formed elsewhere
on the wafer. Special diffusions may also, of course, be used on the
same wafer to produce other devices.

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**Fig. 8.16. Thermo-compression Bonding Process**

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**Fig. 8.17. Development of a Solid Circuit**

(a) Schematic diagram of NOR circuit. (b) Three-dimensional schematic
of NOR circuit. (c) NOR solid circuit.

*Laughrup et al. and "Electronics"*

As an example of the design procedure, consider the "NOR" circuit
shown in Fig. 8.17 (a). The circuit has four diodes, three resistors, a
capacitor, and a transistor. All component values are within specified
design limits; therefore, the circuit can be translated directly into a
solid circuit. It is desirable to change the lumped resistor-capacitor
combination shown in the transistor base circuit to a distributed R.C.
network. Also, since the polarity of voltage applied to the capacitor does not change, a p-n junction-type capacitor may be used.

Although this circuit can be designed on a single wafer, in practice it is desirable to separate the resistors in the input circuit from the collector load resistor. When this is done, all the resistors are formed from two pieces of material. Typical values for $R_A$, $R_B$, and $R_C$ are 4, 10, and 2 kΩ respectively. For 10 Ω cm silicon, 2-mils thick, the required areas for these resistors will be 10 by 20 mils for $R_A$, 10 by 50 mils for $R_B$, and 10 by 10 mils for $R_C$.

These resistors may be arranged, along with the other necessary components, in the configuration shown in Fig. 8.17 (b). The starting wafer of n-type silicon forms the transistor collector region, all resistors, and the cathode of each diode. A diffused p-p layer is then used to form the transistor base region, the diode anodes, and the capacitor overlying $R_A$.

Next, an n-type diffusion is required for the transistor emitter region. These fabrication steps are applied to a large-area silicon wafer, typically 210 by 440 mils. After appropriate contacts are deposited, the wafer is separated into enough silicon bars to make 16 complete NOR circuits. This is a practical production process because it provides many units with identical characteristics. The final step is to provide input and output connections and a few "jumpers" to connect some of the internal elements, as shown in Fig. 8.17 (c). The latter connections are made with thermally-bonded gold wires.

There are many alternative layouts theoretically possible for this design example. The proper selection of an optimum layout requires a thorough knowledge of available manufacturing techniques and their limitations. This job is performed by a solid-circuit design engineer.

**Interconnexions and Sub-assemblies**

Because of the very small size of finished units, almost any form of interconnexion will permit a worthwhile reduction in size and weight when compared with an assembly of conventional components. However, some effort is required to design a system in which the interconnexions should occupy less volume than the solid circuits. One way to achieve this is to stack the units as shown in Fig. 8.18. Connexions between units are provided by sheets of 2 mil thick copper-clad teflon. Due to close spacing between the leads, all the wiring cannot be provided in a single plane. Multiple sheets are therefore used. Each required supply voltage is connected to a separate sheet that has a grid pattern with holes providing electrical and mechanical clearance for the leads.

A lead may pass either straight through a sheet and be insulated from it, or be bent over and welded to provide an electrical connexion.

After all supply voltages have been connected, the top sheet is added to form the signal paths. If crossovers are necessary, a second signal sheet may be used. When solid circuits are to be assembled in this manner, the designer should attempt to alternate the location of supply and signal leads on each package, thus increasing the spacing between adjacent terminals on the top sheet. Note that individual sheets may be used for shielding or as a ground plane. Also, this assembly technique may be useful for solid-circuit v.h.f. applications, where the copper-clad teflon sheets could become microstrip transmission lines.
paths to heat sinks can easily be provided. For the stacked sub-assembly in Fig. 8.18, this may be done by placing between the units metal strips which are tied to heat sinks on the two open sides of the sub-assembly. Furthermore, the degrees of design freedom offered by solid circuits may produce new circuits that require much less power for operation.

Solid-circuit Construction

Texas Instruments Inc. An example of a Texas Instruments' solid circuit as described by Kilby (see Bibliography) is shown in Fig. 8.19 (c). This is a multivibrator circuit containing eight resistors, two capacitors and two transistors; the conventional circuit diagram is shown in Fig. 8.19 (a). This circuit is redrawn in Fig. 8.19 (b) to correspond with

![Comparison of Conventional Circuit with Solid Equivalent](image)

(c) Bistable multivibrator typical of conventional circuits that are readily adaptable to solid-circuit techniques. (b) Redrawn version of circuit in (a) showing approximate layout arrangement of actual semiconductor circuit. (c) Magnified view of complete bistable multivibrator unit, which after hermetically sealing will be only 0.24 x 0.12 x 0.25 in.

*Kilby and "Electronics"*
the physical layout of the solid circuit; the only difference is that distributed parameter R.C. networks are used instead of separate resistors and capacitors in the feedback branches. With the aid of this circuit and the schematic diagram of the multivibrators, shown in Fig. 8.20, the equivalent component parts of the solid circuit can be traced.

The multivibrator consists of a semiconductor wafer with a slot in the centre to provide the necessary isolation between components. The resistive areas are round the outside of the wafer; the capacitors and the transistors lie on the surface of the resistors. The transistors and capacitors are slightly proud of the surface, due to the action of the selective etching used in the fabrication process. A convenient way of tracing out the solid circuit is as follows. Begin at the +3 V terminal; from here branch out to the two 3000 Ω resistors; each resistor goes to a distributed R.C. network; the other ends of the two R.C. networks are connected by a chain of 300-Ω resistors; the collector junction of each transistor is part of the upper boundary of the resistor chain; cross-connexionss are fine wires bonded to the correct parts of the wafer. The terminals are bonded to the wafer in the appropriate places and insulated from each other.

The size of the finished hermetically-sealed multivibrator is 0.240 × 0.120 × 0.025 in. Excluding the leads, the volume of the sealed package is 0.0007 in.³; this would mean a packing density of about 20,000 components/in.³.

The schematic diagram and circuit of a phase-shift oscillator are shown in Fig. 8.21. Also illustrated is the physical arrangement of the components, to aid tracing out the component elements of the solid circuit. This circuit consists of a semiconductor wafer produced with a single diffused layer which has been selectively etched to give the transistor and capacitor. The body of the wafer forms the resistor chain. Again cross-connexionss are fine wires bonded to the wafer and the Kovar terminals.

At the time of writing, Texas Instruments Inc. have a solid-circuit available commercially. This is the Type 502 unit and may be
Other circuits that have been made in solid-circuit form by Texas Instruments Inc. include—

1. Inverters.
2. Flip-flops.
3. “And” gates.
4. “Or” gates.
5. NOR circuits.
6. Filters.
7. Audio-amplifiers.

For logic elements, inverters and binary counters, Texas Instruments Inc. found that the switching speeds of solid circuits frequently exceed the performance of a bread-board circuit with conventional components. This indicates that when a transistor wafer is designed into a semiconductor block instead of mounting it on a header, the decreased collector capacitance and elimination of lead inductance allow a faster switching response.

The Plessey Company. As further examples of solid circuit construction, descriptions are given of two paper studies made by the Plessey Co. to assess the practicability of solid circuits. Fig. 8.24 shows another design of a phase-shift oscillator using solid-circuit methods of construction. The emitter, the collector and the capacitance are formed by a deep diffusion into a wafer of p-type silicon. The diffusion is limited by an oxide mask which is etched away in the desired regions using a further mask formed by photo-lithography. Conductive wiring is by evaporated gold tracks which are insulated from the silicon by the oxide layer. n+ regions are formed where the emitters, collector and capacitor reach the surface, and p+ regions are formed.

**Mechanical Data**

Solid circuit semiconductor networks are mounted in a glass-to-metal hermetically-sealed package. Loads are gold-plated nickel-flashed Kovar. Weight: 0.05 g.

**Maximum Ratings at 25°C Ambient**

- Maximum supply voltage: 8 V
- Maximum trigger voltage: 8 V
- Storage temperature: -55° to +125°C

**Design Characteristics**

- Design supply voltage: 6.0 V ± 5%

**Output voltages—**

- ON: 0.7 V max
- OFF: 4 V min

- With 10 k-Ω load to ground
- With 10 k-Ω load to V,

**Operating temperature range:**

- -40°C to +85°C
Single silicon wafer containing a deep diffused junction. Typically, one might envisage a 7.5 mil wafer of p-type silicon into which phosphorus has been diffused to give a junction 2.5 mils deep on both sides. The n-type region is then lapped off one side and a shallow p-type region diffused on the same side, for instance by the paint-on technique. Good ohmic contacts can now be obtained by nickel plating. Two

T-shaped channels are cut to a depth of, say, 3 mils, as shown in Fig. 8.25 (b) and (c). The rectifying regions are separated by removing the nickel from the edges of the wafer except for the straps joining $R_1$ to $R_2$ and $R_3$ to $R_4$. These straps short out the two p-n junctions in the centre of the assembly, leaving only four active p-n junctions, one at each corner of the wafer. The nickel is removed, where required, by masking the areas which are to remain plated. The nickel areas are now tinned with solder and the unit etched. Leads, and heat sinks if required, are attached to the soldered areas.

**Fig. 8.26**

(a) Conventional thyristor circuit. (b) Thyristor circuit with semiconductor delay line. (c) Integrated thyristor shift register.
Radio Corporation of America. An approach to solid-circuit construction adopted by the Radio Corporation of America is the use of active devices connected together to form digital circuits. The circuits studied by Wallmark and Marcus (see Bibliography) incorporate either thyristors or unipolar transistors. Both devices have been described in Chapter 2.

The thyristor (Mueller and Hilibrand, see Bibliography) has been used to make an integrated shift register. One stage of a conventional thyristor shift register is shown in Fig. 8.26 (a). The thyristor has a negative resistance characteristic for certain ranges of applied circuit and voltage and may, therefore, be used as a bistable element to store one digit. When the stage is turned ON, a pulse is sent through the R.C. circuit to an adjacent stage, turning that on. The R.C. circuit should have a time-constant long enough to store the information while the stages themselves are being cleared so that they are ready to receive new information. The R.C. circuit is the memory store.

In Fig. 8.26 (b) the R.C. circuit is replaced by a delay line consisting of a small bar of germanium. The shift pulse is applied along this bar, which draws minority carriers from the stage which is ON, down the bar. After a time equal to their transit time, the minority carriers reach the end of the bar, where they can be used to trigger the next thyristor stage ON.

Fig. 8.26 (c) shows a version of a complete shift register. The states are propagated along the bar by a shift voltage applied to the two end contacts. In this manner, a binary number stored in the register may be shifted. Each stage is provided with a base contact for the write-in of information.

Another integrated device, which this time utilizes the unipolar transistor, is called the direct-coupled unipolar transistor logic or DCUTL. Fig. 8.27 shows a multiple AND circuit using DCUTL. It consists of five unipolar transistors fabricated in one piece of silicon, four of which serve as active devices, the fifth being a passive component, in this case a fixed resistor. The bar is shaped so that the gate regions of the transistors are separated, and each transistor is connected to the next by a silicon bridge. A voltage applied to the end contacts of the bar results in a current through the bar, and consequently an output signal if all four gate regions are, simultaneously, only slightly reversed-biased. On the other hand, if one or more of the gate regions are strongly reverse biased, no circuit will flow along the bar and no output signal is obtained. Various other types of DCUTL solid circuits, using building bricks of integrated unipolar devices are possible; these are described in the reference.

Royal Radar Establishment. The unijunction transistor (Suran, see Bibliography) is the active element in the first solid circuits constructed at the R.R.E. The important property of this transistor is its negative resistance input characteristic, which makes it suitable for such applications as oscillators, relays, sawtooth generators and regenerative pulse amplifiers. The unijunction transistor is a bar of silicon or germanium with ohmic contacts at each end and a p-n junction near one of the ohmic contacts (see also Chapter 2). For some of the applications the associated passive components have values small enough to be incorporated in a solid circuit.

Fig. 8.28 (a) is an example of an oscillator or trigger circuit using a unijunction transistor. The circuit is redrawn in Fig. 8.28 (b) to correspond with the solid-circuit version in Fig. 8.28 (c). A more practical layout for the solid circuit is shown schematically in Fig. 8.28 (d).

At the onset of the work the only unijunction transistors known were those made by the alloy process using silicon or germanium as the bar material. The envisaged solid circuit had to be made by diffusion techniques if possible as these are the most suitable and permit design freedom. As a result it was necessary that unijunction transistors could be made with diffused p-n junction emitters. Preliminary work showed this to be possible.

30-ohm/cm n-type silicon was subjected to a boron diffusion, plated
and cut into bars of dimensions $10 \times 15 \times 60$ mils. Masking and selective etching was employed to make the emitter junction and the two ohmic base contacts. The mesa height was critical as the junction must not be removed too far from the sweeping field existing between the two base contacts. Oscillation frequencies up to 650 Kc/s were obtained when the transistor was connected in circuit as shown in Fig. 8.28 (a).

Having shown that a diffused unijunction transistor could be made, the solid circuit was then fabricated. 30-ohm/cm n-type silicon, boron diffused, was cut into pieces of dimensions approximately $200 \times 200 \times 10$ mils. The die was masked and selectively etched to form the capacitor, emitter and two base contacts. The slot was cut with a wire saw, and soldered contacts were made to the appropriate regions. The unit was tested electrically; the unijunction transistor or the resistor parts of the material being selectively etched until oscillations were obtained. With a capacitor of this area (approx. $180 \times 120$ mils), a slightly degraded saw-tooth waveform was obtained at the emitter. This was the first solid circuit to be made in the U.K.

**Westinghouse Electric Corp.** Work on solid circuits at Westinghouse, supported by a 2-million dollar U.S. Air Force contract, represents one of the biggest concentrations of effort in this form of microminiaturization. Unfortunately, at the time of writing, no detailed accounts of their research and development have been published. It has, however, been announced that eight classes of solid circuits have been constructed as follows:

1. A 5-W directly-cascaded audio-amplifier.
2. A two-stage video-amplifier.
3. A frequency-selective amplifier with notch filter in a feedback loop around the amplifier structure.
4. A variety of multivibrators; bistable, monostable and astable.
5. A variable potentiometer based on the logarithmic addition of two inputs.
6. A variety of multiposition switches; including an OR switch, a multiple $n-p-n-p$ diode switch and a multiple $n-p-n-p$ triggered diode switch.
7. An analogue-to-digital converter employing an $n-p-n-p$ relaxation oscillator.
8. A two-stage cooler employing the Peltier effect, covering frequencies from 1 c/s or less to 3 Mc/s, for cooling infra-red detectors.

Three examples of Westinghouse solid circuits are shown in Fig. 8.29. These represent an audio-amplifier, a free running multivibrator and a two-stage video-amplifier. At present there is no detailed account of the construction and operation of these units.

A further idea put forward by Westinghouse, again with no details, is the construction of a solid-circuit power supply shown in Fig. 8.30. A resistive domain is used to convert a.c. into heat. The Seebeck effect then converts the heat into d.c. Whether this represents a practicable circuit in terms of conversion efficiency, or does not, it does illustrate how various effects in solid-state physics may be utilized to give a functional device that replaces a conventional circuit stage.

**Fairchild Semiconductor.** Fairchild Semiconductor have under development a family of high-speed, low-power logic building blocks for digital computer applications. The company states that the units are sufficient to handle all logic function requirements of a digital computer operating at bit rates in excess of 1 Mc/s and that no other components would be required in the logic sections.
Bibliography) has made an analysis of the situation and shows that for a solid circuit to be competitive, the shrinkage per equivalent component should not exceed a limit which depends on the number of components and the way in which they are combined. The requirement is rather stringent.

From his analyses, Wallmark reaches the following conclusions—

"It seems that an important requirement for solid circuits is a manufacturing process with a sufficiently low shrinkage. A somewhat higher investment in the fabrication equipment for solid circuits, compared with that of individual components, is justified because of the higher cost of shrinkage of the former.

Furthermore, it is desirable that the solid circuit be designed so that the extent of integration—the number of equivalent components that is integrated into one piece of semiconductor—is flexible and adjusted to the particular shrinkage rate at any one time.

By providing reserve stages and using them to by-pass faulty stages in the fabrication procedure, considerable reduction in shrinkage can be accomplished. It appears that a design that facilitates doctoring of this kind would be desirable in the fabrication of solid circuits."

Clearly, the design of a solid circuit to give a maximum economic yield is rather complex and involves many compromises. In many cases it may be preferable to produce a smaller number of equivalent components in several interconnected semiconductor blocks rather than form a large number of components in a single block.

3. Reliability. Texas Instruments Inc. state that only 15 to 20 process steps are needed to convert a semiconductor wafer into a solid circuit. With so few process steps it becomes economical to apply a high degree of process control. Thus, reliability is built into the system. Although complete life-test data is not available to support the claim that reliability has been significantly improved, the following considerations are offered to show that there is every reason to believe that this is true.

(a) The purity level and order of lattice arrangement for the starting material is carefully controlled, whereas in other microminiaturization approaches many dissimilar materials of varying or unknown degrees of purity are used.

(b) By using a single material, up to 80 per cent of the connexions required for a conventional circuit are eliminated. The various regions which form circuit elements are continuous within the one bulk material. This minimizes the mismatch in thermal-expansion coefficients which, usually, is the cause of catastrophic failures. Besides reducing the number of solder joints which inevitably exist between lead wires of conventional components, a reduction is made in the number of connexions where each lead wire is attached to the active element of

the component (e.g. where a resistor lead is bonded to the carbon rod or metal film, or where a capacitor lead is attached to the metal foil or silvered-mica plate). The use of metal contacts alloyed into the semiconductor also reduces the interfaces between dissimilar materials.

(c) The small number of required process steps permit accurate process controls to be economically applied. All the fabrication steps are performed in one plant and on one production line, therefore complete statistical methodology is possible.

(d) Since the entire circuit is hermetically sealed, both active and passive elements are protected against environmental conditions.

(e) Because of its very small mass, the solid circuit is difficult to damage by shock or vibration.

4. Applications. The present higher cost of solid circuits compared with assemblies of individual units suggest applications in which there is a large premium on weight and space. Thus, solid circuits are especially suitable for digital circuitry, particularly where the computer has to be small and, possibly, mobile. Digital circuits are usually repetitive, which permits the construction of large systems with only a few basic building blocks.

Due to the present limitations on component types and values, considerable ingenuity will be required to make all kinds of circuitry in solid-circuit form. The lack of large-value capacitors will inevitably slow the development of a.f. solid circuits of very small dimensions. The lack of inductors means that purely solid r.f. circuits are not possible, though hybrid constructions using separate inductors could be used. It is believed, however, that these restrictions are temporary.

Conclusion

Solid circuits are, without doubt, the most promising form of microminiaturization. The techniques are comparatively new, and the work described in this chapter must be regarded as only laying the foundations of a form of circuit building which may eventually revolutionize electronics. It would seem to be only a matter of time before all the circuit functions at present performed by micro-modules and microcircuits will be performed with equal efficiency by solid circuits. Solid circuits, being formed in single blocks of semiconductor, have advantages over the other microminiaturization systems in that they do not require a sequence of diverse fabrication steps, have few contacts between dissimilar metals, suffer less from the effects of differential thermal expansion, and are relatively easy to heat sink. At present solid circuits are costly, but as transistor-making techniques are used throughout, the more automatized and cheaper these techniques become, the cheaper must solid circuits become. Because of the strong competition in the transistor industry, each year sees a reduction in
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prices, hence, economically, solid circuits have a promising future, and it is confidently predicted by many that the time may not be too far distant when solid circuits are competitive in price with assemblies of conventional components.

However, it is the chance of almost unlimited development that makes the solid circuit concept so attractive. There are many known effects which might still be utilized in solid circuits, and furthermore, research in solid-state physics continues to bring forth new phenomena and techniques which might also have direct applications in this system of microminiaturization. Thus, with the incorporation of old and new effects, the streamlining of the technology, the multiplication of available circuit functions and the promise of increased reliability, the future of solid circuits seems to be assured.

BIBLIOGRAPHY

Miniaturization of Electronic Equipment


Miniature Components


BIBLIOGRAPHY


CATALOGUE: Miniature Electronic Components (Woking).

CATALOGUE: Fortiphone Ltd. (London).


Microminiaturization—General


**Semiconductors**


**Semiconductor Devices, etc.**


**BIBLIOGRAPHY**


**Micromodules**


Ross, R. J. “Role of semiconductors in the army micromodule.” Electronic Design, 7 (Feb., 1959), 46.


Kublin, V. J. “Progress in the army micromodule program.” Electronic Design, 7 (May, 1959), 68.


**Microcircuits**


MINIATURE AND MICROMINIATURE ELECTRONICS


Siddell, G. “Vacuum Deposition of Dielectric Films for Capacitors.” Vacuum, 9, No. 5-6, 274.

Microcircuitry Booklet published by Varo Manufacturing Co. Inc., 2201 Walnut Street, Garland, Texas.

Solid Circuits


“The design, programming and sociological implications of microelectronics.” A series of four integrated and coordinated papers, Western Joint Computer Conf. San Francisco (5th May, 1960).