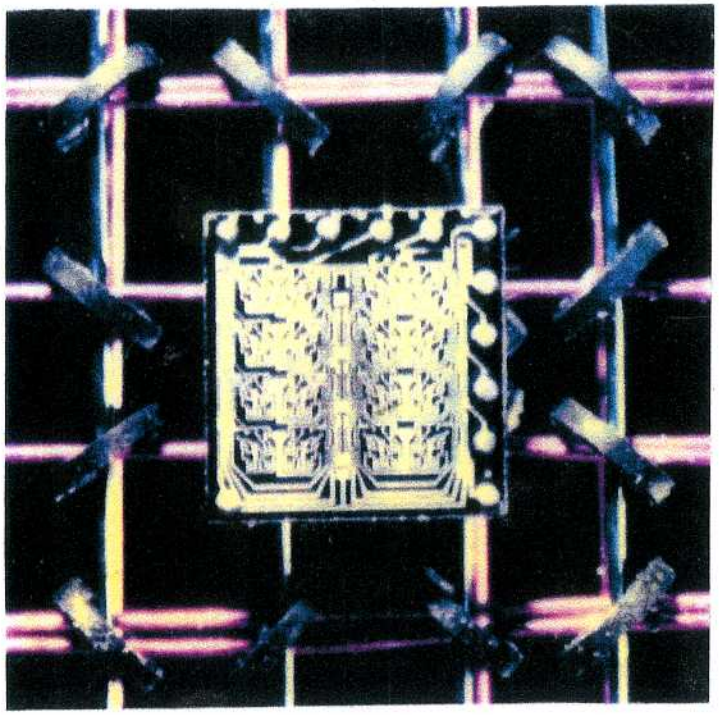
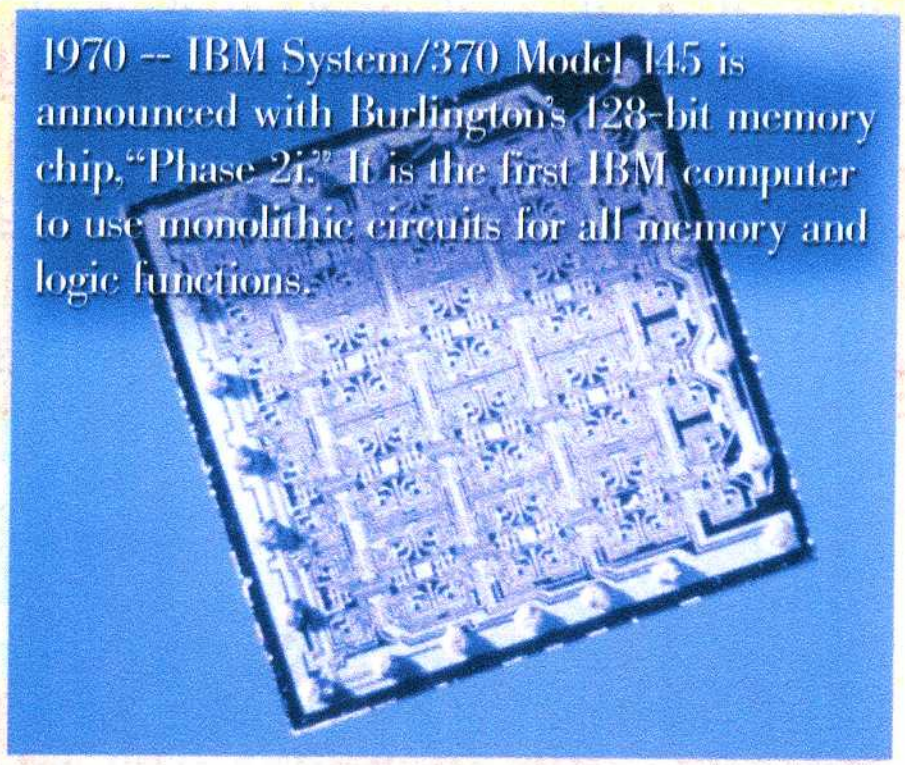
IBM FIRST IN IC MEMORY





IBM SP 95 — Phase 2I Memory

First COMPUTER IC MEMORY SP95- 16 BITS, IBM System 360 Model 95-1965

First COMMERCIAL IC MEMORY
PHASE 2-64 Bits Buffer
PHASE 2I-128 Bits Main Store, IBM System- 370 Model 145 - 1970

IBM NEWS

Volume 3 No. 9 May 10, 1966
Published by International Business Machines Corporation, Armonk, N. Y.

East Fishkill

Developed At East Fishkill

IBM Files Patent Application On 16-Bit Monolithic Chip

IBM has filed applications for a patent on the 16-bit monolithic memory array developed by IBM's component development department at East Fishkill. It is the first application from East Fishkill on a monolithic integrated structure.

Three separate applications were filed—the basic one and two others on inventions used in the monolithic chip which could be used in other monolithic structures.

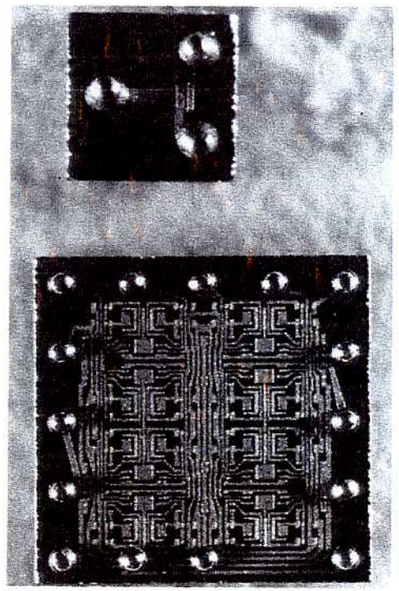
Six men listed as inventors on one or more of the three applications are Dr. Benjamin Agusta, Dr. Paul Bardell, Paul P. Castrucci, Robert A. Henle, Martin S. Hess, and Raymond P. Pecoraro.

Although only two and a half times the size of an SLT chip, each monolithic chip has 80 transistors, in addition to other components. The new chips are completely compatible with SLT and involve almost the same processing techniques.

"Sixteen-bit" refers to the 16 circuits on each chip. Each circuit represents one bit of information by being "on" or "off."

The circuits are called "integrated" because they cannot be broken down into separate components. Integrated circuits on which all electrical elements are fabricated within a single chip of silicon are called "monolithics."

"Filing a patent application indicates a company has great interest in an invention," says Alvin J. Riddles, manager of patent operations, Fishkill. He pointed out that time and expense are involved and that three years or more can go by after filing before a patent is issued.



Monolithic integrated circuit chip, below, on which patent applications have been filed, is only 2½ times as large as SLT chip, above, but contains 80 transistors plus 64 resistors and 4 diodes.

To give IBM the fullest protection on the invention, the basic application covers monolithic structure, package, and fabrication method, said Harry M. Weiss, patent attorney who prepared the application.

United States Patent Office

3,508,209
Patented Apr. 21, 1970

3,508,209

MONOLITHIC INTEGRATED MEMORY ARRAY STRUCTURE INCLUDING FABRICATION AND PACKAGE THEREFOR

Benjamin Agusta, Paul H. Bardell, and Paul P. Castrucci, Poughkeepsie, Robert A. Henle, Hyde Park, and Raymond P. Pecoraro, Poughkeepsie, N.Y., assignors to International Business Machines Corporation, Armonk, N.Y., a corporation of New York

Filed Mar. 31, 1966, Ser. No. 539,210
Int. Cl. G11c *5/04, 11/40;* **H01l** *19/00*
U.S. Cl. 340—173 **14 Claims**

ABSTRACT OF THE DISCLOSURE

A monolithic integrated semiconductor structure is described that has a plurality of functionally isolated individual cells that are electrically interconnected. Each of the cells is an object or mirror image cell that is vertically, horizontally and diagonally displaced from the object cell. The plurality of cells provide a memory array with electrical components of each memory cell composed of active and passive semiconductor devices. Other important aspects of the structure include underpass connections and active devices in a common portion of the structure which are electrically interconnected at the same node potential by means of a highly doped buried region within the common portion of the structure.

This invention relates generally to monolithic integrated structures including the fabrication and package therefor and, more particularly, to a monolithic integrated memory cell that is expandable into a memory array of $q2^n$ x $m2^n$ number of integrated memory cells where q and m are integers and n is either zero or is an integer greater than zero.

Ferrite cores over the years have established an enviable reputation for having electrical characteristics that are not a function of time. However, the metallic wires that thread the cores are subject to corrosion and must be prottected, depending upon the atmosphere in which the array will operate. In some instances, vibration of cores in the array can cause physical damage resulting in a malfunction.

A monolithic memory array containing 64,000 words of 72 bits involves a significant number of components and interconnections. A 5-million bit monolithic memory array utilizing the unit cell of this invention would have 25 million transistors and 20 million other components in the storage array proper. The addition of the drivers and sense and decode circuitry is likely to add another 20% to this component count. Hence, fabrication and reliability considerations must be considered in determining the BOM (Basic Operating Memory) sizes.

The key to the formation of a monolithic memory array is the monolithic memory cell.

Ideally, a monolithic memory cell that is to be expanded into a memory array should have the following qualities and features:

(1) The cell should be capable of being expanded into any reasonable size planar array with minimum degradation of performance.

(2) It should consist of devices that occupy a small planar area so as to obtain maximum arrays per processed wafer.

(3) The cell circuit should consume very little power so as to permit high package circuit densities and minimize power supplies and power line requirements.

(4) The cell should have a fast read capability when expanded into an array.

(5) The cell should have a fast write time capability when expanded into an array.

(6) The cell should have low internal impedances in order to obtain fast switching capability.

(7) The cell should have a fast recovery time after reading or writing operations so as to permit fast repetition rates.

(8) The cell should have non-destructive read capability, thus permitting faster memory operation since reading cycles do not have to be followed by a write cycle.

(9) The memory state of the cell in an array should be AC and DC isolated from the sense line and thereby not be sensitive to spurious signals and other noise generated by read or write operations and noise pulses on the sense line.

(10) The memory cell in an array should be randomly accessible as opposed to serial information storage sources so as to permit fast machine cycle time.

(11) The cell should consist of component devices that permit topological interconnection relief (underpass) such that the final array can be simply fabricated and interconnected. This avoids the need of a costly second conductive level or interconnection layer and reduces the amount of underpass connectors needed.

(12) The cell and array should preferably not have reactive components such as capacitors and/or inductors since these are relatively difficult to fabricate in a monolithic structure.

(13) The cell and array should have device and fabrication specifications that are easily achievable with monolithic batch fabrication techniques.

(14) The cell and array should be operable over a wide temperature range without performance degradation.

(15) The cell should have a complementary output, thus permitting differential sensing, if needed, in large arrays or for logic purposes.

(16) The cell should require a minimum number of low value supply voltages and be consistent with logic circuitry voltages.

(17) In order to obtain universality of usage, the cell and array should be capable of operating over a wide range of voltages without performance degradation. This feature also permits longer life and greater reliability since it is less sensitive to device degradation with time. Also, it can withstand high voltage transients without deleterious effects.

(18) The cell should preferably not contain complementary devices (NPN and PNP), therefore making the monolithic structure easier to fabricate.

(19) The required array, drive, sense and decode circuitry, which will eventually be incopoated in the monolithic integrated chip, must have device requirements compatible with the cell, peferably without the need for additional process steps.

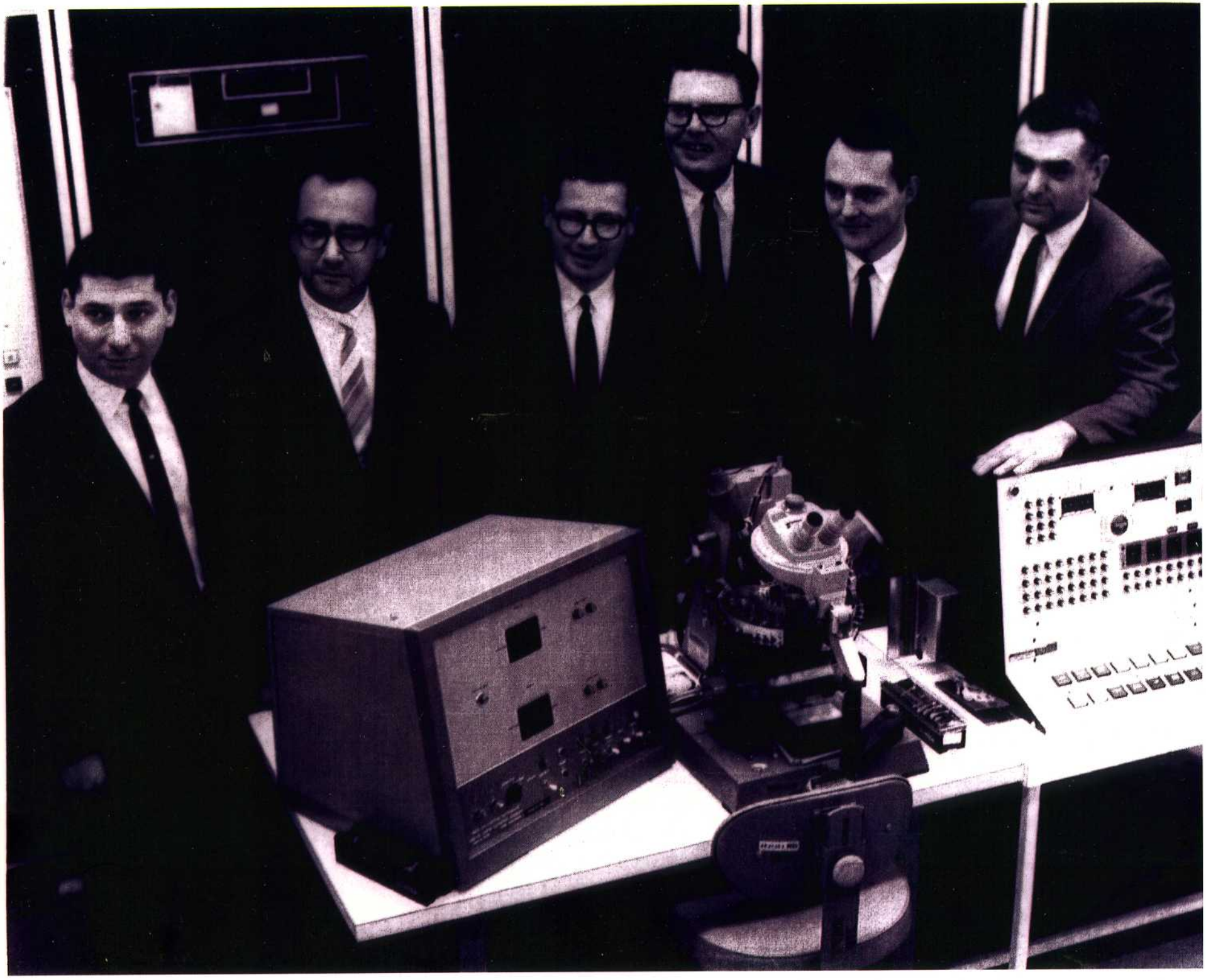
(20) The device specifictions of the array, drive, sense, and decode circuitry should be such that they take advantage of technology improvements, such as closer photomasking and diffusion tolerances which give planar space reduction and/or fast devices that simultaneously improve memory performance and cost.

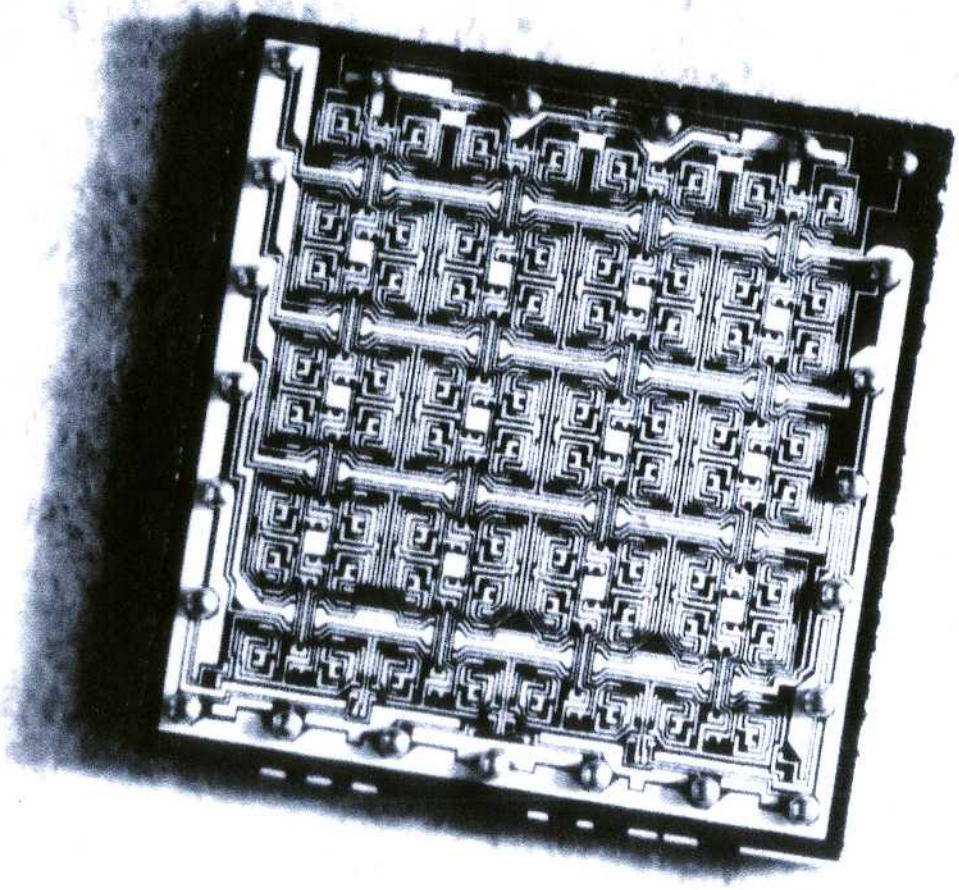
(21) The cell can easily be modified to associative memory applications.

(22) The cell can be easily modified for either 2 or 3 dimensional operation. A 3 dimensional operation takes advantage of the last stage of address decoding. A square 3 dimensional matrix of cells with complementary sense lines results in minimum external contact connections.

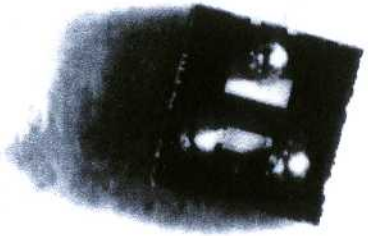
(23) The cell and array should have a minimum number of input-output signal leads.

(24) The cell should have no quiescent sense power,

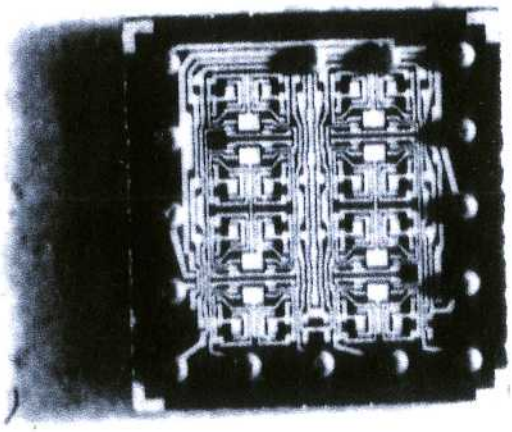




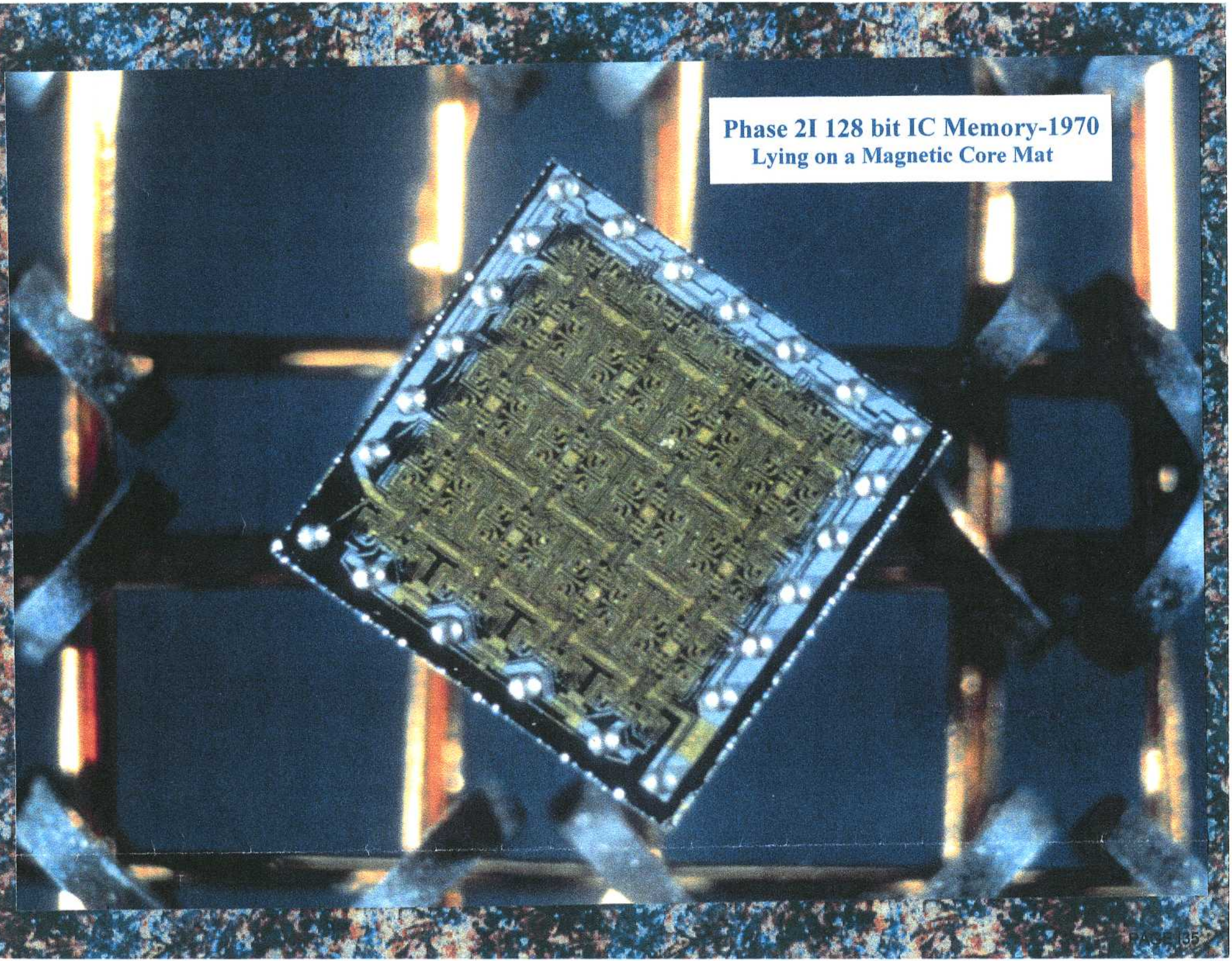
Ø2 MEMORY
1968



SLT
SINGLE TXS
1962



Ø1 SP-95
IC MEMORY 1968


Phase 2I 128 bit IC Memory-1970
Lying on a Magnetic Core Mat

IBM S 360 Model 145, Oct.1970
First computer With
100% Logic & Memory ICs

Buffer & Main Memory Devices
High Volume Production - IBM Essex Junction VT

IBM - COMPONENTS
Dept. 240 - Bldg. 300/75
Ext. 3694 - East Fishkill

July 11, 1967

JUL 1 1 1967

MEMO TO: Mr. P. P. Castrucci

SUBJECT: SP95 Terminal Report

Please express my sincere appreciation to everyone for their part in the SP95 program and, especially, the extra effort to make this illustrious report.

The SP95 program has laid the groundwork for a new technology revolution in IBM.

R. E. Markle
R. E. Markle

REM/cd

cc: Mr. R. P. Pecoraro

40th ANNIVERSARY DINNER
IC MEMORY PATENT
APRIL 3, 20O5

Hello, and welcome to the 40th Anniversary Dinner of the IC Memory Patent. As I look around the room I see a lot of familiar faces and I know that several of you were directly involved in the development and manufacturing of the first integrated circuit memory. I also know that everyone in the room has been touched by the IC Memory. The IC Memory technology has made possible today's digital world. It has affected the way we work play and many other aspects of our lives. How did it happen?

Let's take a walk down memory lane. Our walk will take us from Textile Mills to the Moon - from Winooski in the 50's to Essex Junction in the 90's-A short trip of 40 years. In the 1950's Winooski was experiencing very tough times. The Textile Companies were closing their Mills and moving south. There was widespread unemployment in the area. GBIC (Greater Burlington Industrial Corporation) wanted to attract new businesses to the area to alleviate the unemployment. They put up an industrial building in Essex Junction on the Winooski River. That winter, Tom Watson President of IBM, came to Vermont on a ski trip. GBIC met with Watson and convinced him to start a manufacturing operation in Vermont. IBM started their Vermont operation in 1955 – 50 years ago. The plant's first product was a mechanical, electrical relay – a computer device that was an end of life technology. Vermont was thankful for the IBM plant but it was concerned that the demand for computer relays would diminish and IBM's future in Vermont would be in doubt. Lucky for Vermont, a significant new memory technology was being developed. at IBM East Fishkill.

The 1950's computes utilized magnetic, donut shaped cores for memory, a technology that was lacking in many ways – too slow –too expensive and with very low density. Without the invention of the IC Memory, computers could never be what they are today and IBM could not have grown into a $96 Billion International Company.

A paper written in 1970 by Professor Michael Rappa of the MIT Sloan School states: "The relentless pace of progress in computer Memory Storage is widely recognized as one of the twentieth century's most remarkable technological achievements. What is less known is that it occurred largely within the confines of a single company, IBM." In 1965, the Semiconductor Line in East Fishkill was developing ultra fast high performance transistors that were required to drive High Speed Core Memories.

In the spring of 1965 Eric Bloch, IBM VP of engineering, who later became the Director of the National Science Foundation, called several of us to his office. – Dr Ben Augusta, Ed Hee, Jack Shortel and myself. Ben and I were from the Components Division an Ed and Jack were from the Computer Systems Division. Eric told us that Bob Henley (The Components Division First Fellow) had written a White Paper stating that Integrated Circuits are good for logic applications but even better for Memory applications. Eric told us that IBM would ship a High End, Scientific, System 360, Model 95 to NASA in1966. The Computer had a small Systems Protect Memory for data security. Eric said that he wanted us to build it out of integrated circuits. None off us had any experience with integrated circuits. As we went out of his office, he said "Don't worry if you can't do it, I can build it out of other technologies, even tubes."

Ben and I went to work! Ben decided what circuit design to use and I modified the Silicon, bipolar, wafer, processes in the line to meet the specifications that Ben required. We also developed techniques and processes to produce the photo masks that we needed. We also designed and built the first of a kind tester to electrically check our memory wafers.

Our first SP95 wafers reached electrical test two weeks before Christmas. We couldn't believe our eyes. The circuits were flipping and flopping at speeds that we never anticipated. We packaged the Memory chips and installed the System Protect Memory in the Model 95 Computer. The High End Computer was shipped to NASA in mid 1966. Based on the rapid success of the SP95, IBM, decided to develop IC Memories for their Commercial Computers.

A 64 bit IC Memory was developed for the Buffer Memory and the 128 bit IC Memory for the Main Memory. These first of a kind IC Memories were developed in East Fishkill and transferred to Essex Junction, Vermont for volume production. On October 21, 1970 the New Digital Age was born when IBM announced the Model 145- the first computer with 100% logic and memory electronics. IBM Vermont became the source for the Memory and for the next 20 years became the IC memory capital of the world.

The IC memory is a classical example of "Disruptive Technology". Disruptive Technology dramatically changes the status quo and affects the way we live, work, and play. Examples of disruptive technology are the Automobile, the Electric Light, the Jet Engine and the Microprocessor. Disruptive technologies usually take 10 to 15 years to go from test tube to market place. The IC Memory only took 12 Months from concept to the Market Place. The IC Memory invention enabled the digital age and it dramatically changed man's ability to manage, explore, change, and improve our earthly home. It has also allowed us to explore space, land men on the moon and put robots on Mars.

The best in IC memories is yet to come! When it does, you can be sure that IBM and Vermont will be the leaders for the new technology and for tomorrow's advanced Digital age.

Paul Castrucci