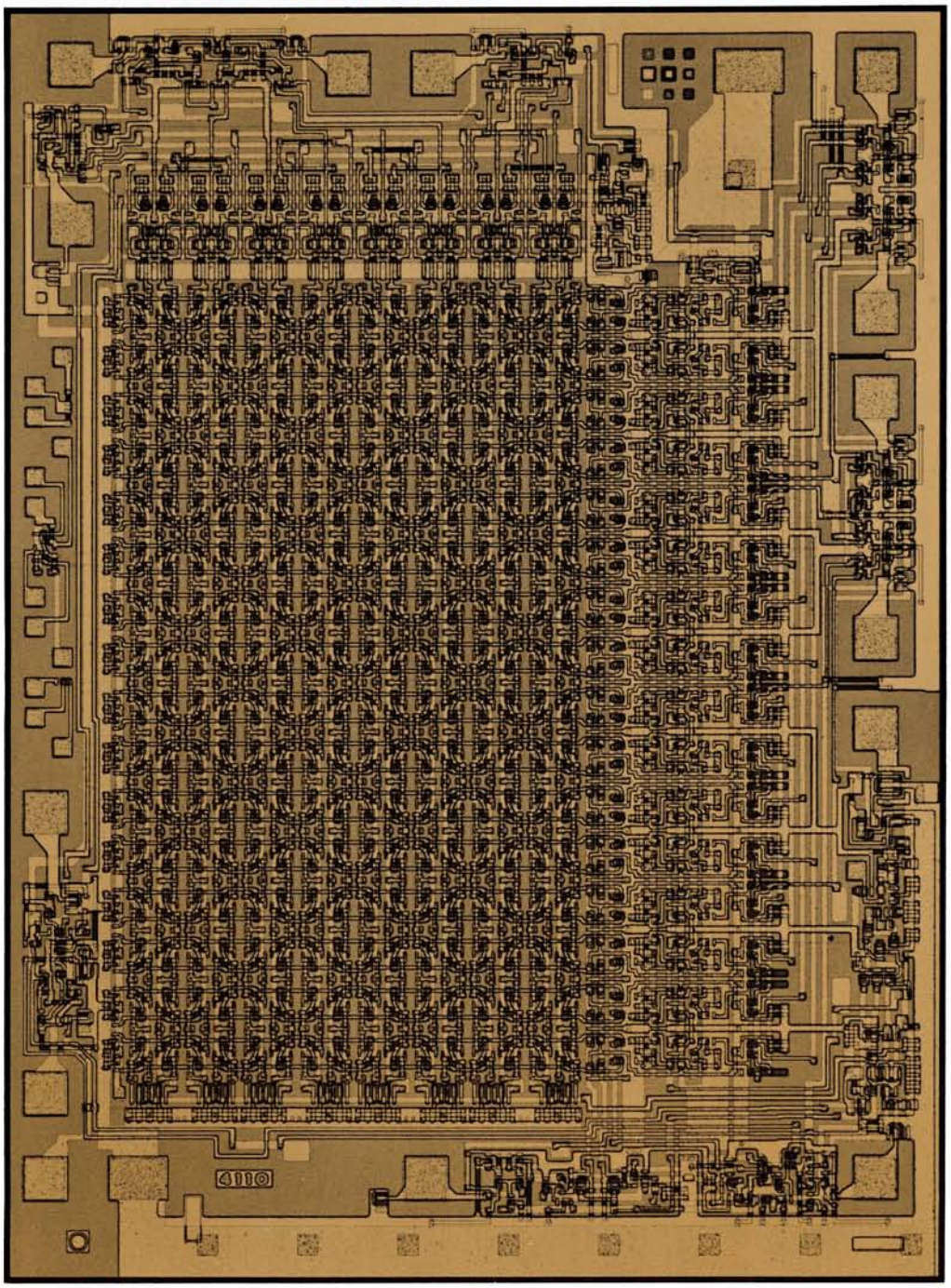
FAIRCHILD SEMICONDUCTOR

THE ISOPLANAR PROCESS



MADE IN FAIRCHILD

OCTOBER 1971

THE ISOPLANAR PROCESS AND ITS IMPACT ON HIGH COMPLEXITY BIPOLAR ARRAYS

With the announcement of the commercial availability of a 256-bit TTL read/write memory, Fairchild Semiconductor has demonstrated that its new Isoplanar process can successfully be applied to a complex integrated circuit. This means that bipolar devices will approach the complexity areas of MOS. Such high density semiconductor arrays with logic level and speed compatibility with the popular TTL and ECL families will open many new application areas for high performance digital systems in the mid 1970's.

Isoplanar is one of the high density bipolar processes now being developed by the semiconductor industry (Ref. 1). Fairchild's announcement of Isoplanar early in 1971 (Ref. 2) indicated that the company was the first to make specific product commitments to such a process.

A 256-bit read/write TTL memory, the 93410, is the first Isoplanar product. The techniques proven on the 93410 are now being applied to more complex products, including 1024-bit and larger TTL and ECL devices.

Ref. 1 "Coming Up Fast From Behind—Denser Bipolar Devices" Electronics, July 1, 1971 p. 76

Ref. 2 "Isolation Method Shrinks Bipolar Cells For Fast, Dense Memories" Electronics, March 1, 1971 p. 52

THE ISOPLANAR PROCESS

By W. D. Baker and D. A. Laws

WHAT IS ISOPLANAR?

Isoplanar is an advanced bipolar integrated circuit fabrication process which offers:

(a) Component density comparable to MOS

(b) Higher yields than conventional bipolar, and

(c) High reliability

plus the familiar bipolar design features of high speed, ease of use, single power supplies and direct logic level compatibility with TTL and ECL.

Essentially an evolution of the Fairchild Planar* process, Isoplanar is a new method of achieving electrical isolation between various components in an integrated circuit. The Isoplanar and Planar processes have many similarities: both use buried collectors, epitaxial layers, base diffusions, emitters and metal interconnect layers.

The Isoplanar process selectively grows a thick thermal oxide in place of the p+ isolation region of the Planar process. The oxide, an insulator, needs no separation from base and collector regions, resulting in a reduction in chip size. Other advantages offered by the Isoplanar process include increased yields due to the elimination of many isolation defect sensitivity problems, greater flexibility of interconnection, and simple masking rules. These lead to increased complexity in a given area at lower cost than conventional bipolar. The result – more functions per dollar.

The size reduction potential of Isoplanar is shown in Figure 1. Two bipolar transistors are shown – one Planar – one Isoplanar. The older Planar process requires a large region for p+ isolation and isolation-to-base clearance because isolation is achieved by means of a reverse biased P-N junction. Isoplanar processing shrinks the first region, filling it with a thick insulating oxide, and eliminates the second. Assuming identical mask design tolerances, the Isoplanar transistor is about half the size of the planar device.

Tighter tolerances than are possible with conventional processing will permit even smaller geometries in the future.

ISOPLANAR PROCESS STEPS

The following figures show the construction of a simple memory word driver. Fig. 2a is a cross-section of a partially complete transistor after buried collector mask and diffusion. The next steps are to grow a p-type epitaxial layer and cover it with silicon nitride. To form the oxidized regions the nitride layer is first masked and etched, then a shallow silicon etch removes part of the epitaxial layer to form the structure in Fig. 2d. A thick thermal oxide is grown in the etched regions. No oxide grows beneath the silicon nitride. Nitride is used for masking as it remains practically inert during the oxidation process.

The surface of the wafer is now divided into islands of p-type epitaxial silicon surrounded by a field region of thick insulating oxide. The thick oxide defines the extent of all the transistors, diodes, and resistors used in the circuit and positions or self-aligns these elements with respect to each other. This feature permits the use of oversized masks during later diffusion steps, simplifying mask alignment problems associated with high performance complex arrays. Pinholes and other defects in these masks have a low probability of destroying a device since the thick oxide protects most of the chip against spurious diffusion.

The next masking step, sink mask, removes a portion of the nitride from the silicon islands, and an n-type dopant is diffused into these openings (Fig. 2e). A simple oversize mask can be used at this stage since the area affected by the dopant is essentially defined by the isolation. This diffusion does not require a masking step since lateral extent of the diffusion is defined by the existing pattern of isolation oxide. The diffusion is used to control resistor values and surface concentration of transistor bases. A thin oxide is grown over the sinks and base regions (Fig. 2f).

Circuit components are completed by conventional oxide masking and diffusing emitters and opening the base and resistor contacts. Metal interconnect layers are deposited and defined by masking to form the completed structure shown in Fig. 2h.

The process described is known as the epitaxial base process. A wider range of circuit components will soon be available with the double diffused process now in development at Fairchild. This process uses an N epitaxial layer in place of the P region. In addition to the NPN transistors it will provide

*Planar is a patented Fairchild Process.

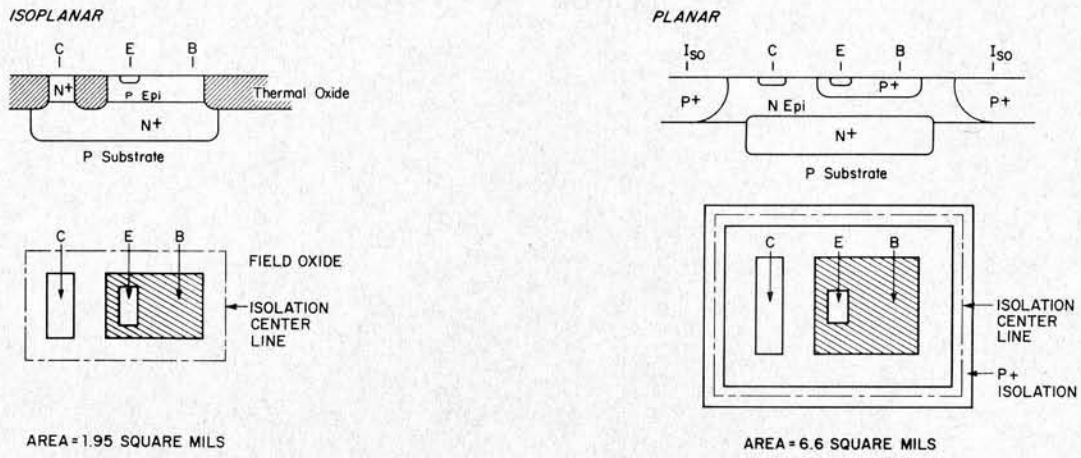
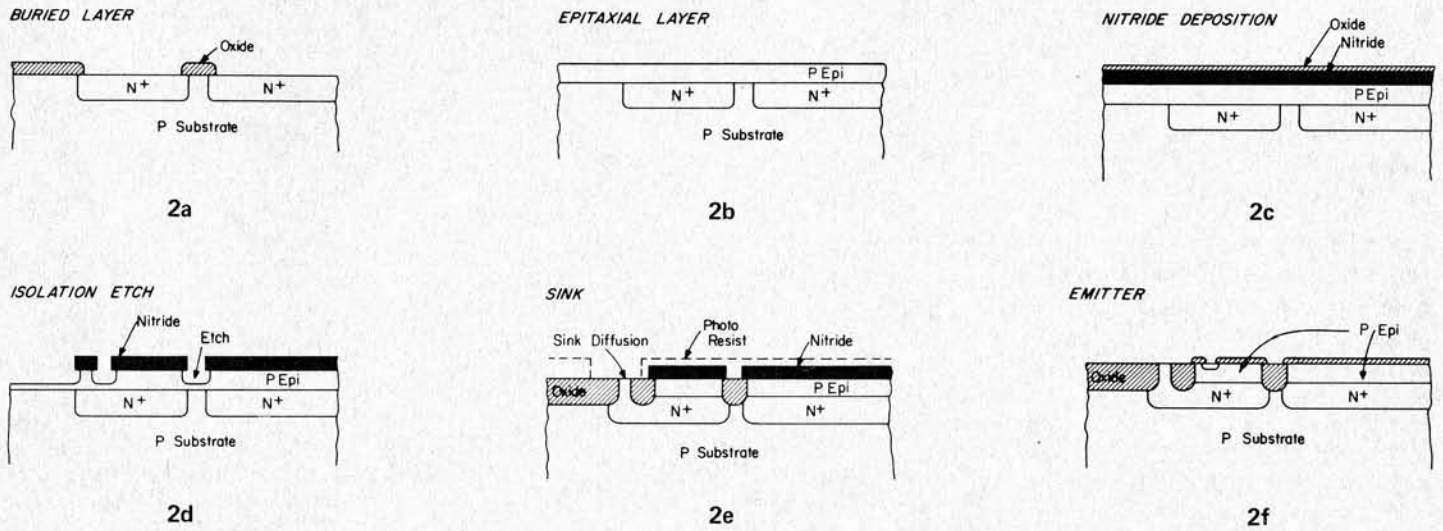


Fig. 1. Cross section and plan of Isoplanar and Planar (conventional bipolar) transistors showing the area reduction achieved. This assumes identical mask layout rules.



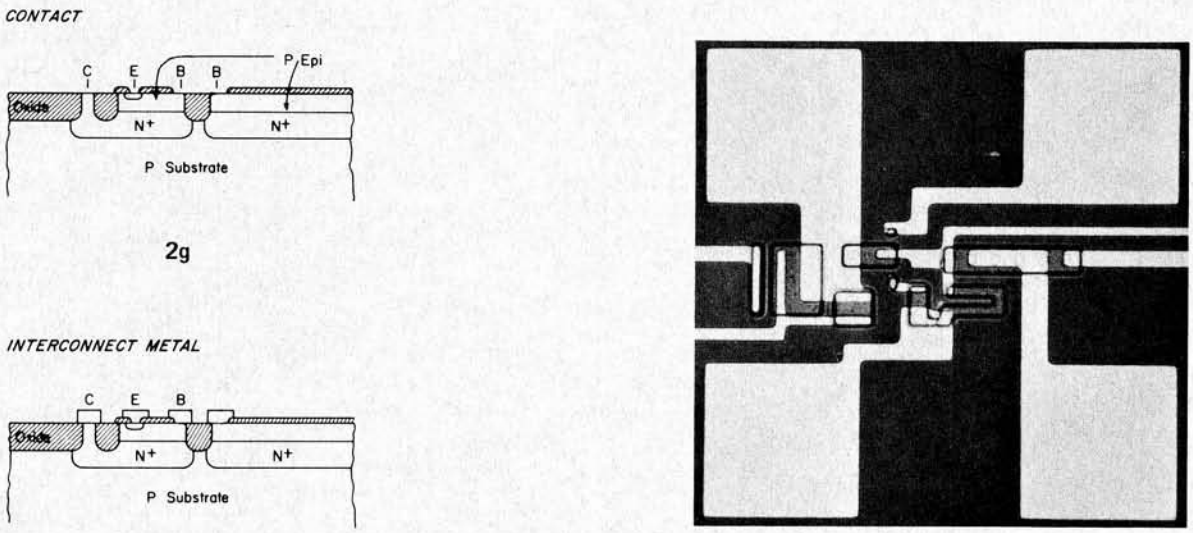


Fig. 2. Isoplanar process steps showing construction of a simple memory decoder/word driver in a 22 mil^2 area.

PNP substrate transistors, Schottky diodes and N epi resistors. These will be important for the design of sophisticated logic arrays.

ADVANTAGES OF ISOPLANAR

Major features of the Isoplanar process which contribute to improved yield and lower cost per function include:

(a) Smaller devices which have a lower probability of containing a defect.

(b) Higher packing density, which means either much more complex elements than before (1K RAMs and above) or smaller (therefore lower cost) chips for the same function.

(c) Oversize masks, providing simpler mask alignment procedures.

(d) Self-aligning masks. Transistor bases, sinks and resistors are positioned with respect to each other and the isolation by the isolation mask. This means either simpler processing or the ability to achieve tighter mask design tolerances.

(e) Higher yields are possible because of the insensitivity to oxide pinholes caused by mask defects.

(f) The essentially coplanar surface simplifies reliable metalization and promises extremely high yield multilayer metal processes. The largest step is at the base contact which is less than 3000Å compared with up to 8000Å on conventional bipolar circuits.

(g) Speed-power performance improvements are achieved because of the reduction of transistor sidewall capacitance.

ISOPLANAR MEMORIES

Fairchild has chosen to use the Isoplanar process in memory design because of the immediate need for high speed, high complexity ECL and TTL read/write storage. Major application areas are high performance microprogram controllers, in cache and buffer storage, and in smaller main memory systems where static operation, direct compatibility with bipolar logic, and single power supply features are advantageous.

An example of Isoplanar process is the 93410 fully decoded 256-bit read/write memory in Fig. 3. The photomicrograph shows one two transistor storage bit, a flip-flop, fabricated in a 15-square-mil area. This is compared with one cell of the familiar 93400 partially decoded 256 bit memory used in the Illiac program. Even using the high density epitaxial resistor approach the Illiac memory cell required 30 sq. mils of area. Thus we achieved 50% reduction in area. Dual layer metal, more easily produced with Isoplanar because of the shallow oxide steps was used on the 93410 to demonstrate its feasibility for more complex products. As cell sizes decrease, their utility becomes limited by the ability of single layer metal to interconnect them. Dual layer is definitely necessary for 1024 bit and larger memories.

The elimination of transistor side wall capacitance insures an improved speed-power product over conventional bipolar devices. In the 93410 this has been combined with ECL internal circuit design to provide a high performance device which should achieve a 50 ns max read access time at 2 mW/bit power dissipation, without the necessity of gold doping or Schottky clamped transistors.

The memory interfaces to the outside world through a level converter and appears as a conventional TTL element to the system designer. This same basic memory design will be used to provide a 256 bit temperature compensated ECL array, the 95410, by merely adding output buffers in place of the converter circuits.

The next generation product will be a fully decoded 1024 bit TTL device, the 93415. This will be designed using the same basic approach but a smaller cell size, 10 sq. mils, making most efficient use of the dual layer metal capability. The 1971–72 chip size curve of Fig. 5a illustrates where the 93415 is in relation to other memory products available today. A square chip is assumed for simplicity. The 1024 bit 93415 will be only about 20% larger than the 256 bit Illiac array. Both the 95410 and 93415 will be available in 1972 and will be made with the epitaxial base process currently in production.

Even greater complexity will come with further sophistications in the process, tighter tolerances, and double diffusion techniques. Performance will improve and a wider range of circuit components will be available. The impact of these improvements can be seen in the 1972–73 curve of Fig. 5b. Thus a 2048 bit device on a reproducible die size should be feasible in 1972–73. Even greater complexity may be possible through further design refinements.

BEYOND MEMORY

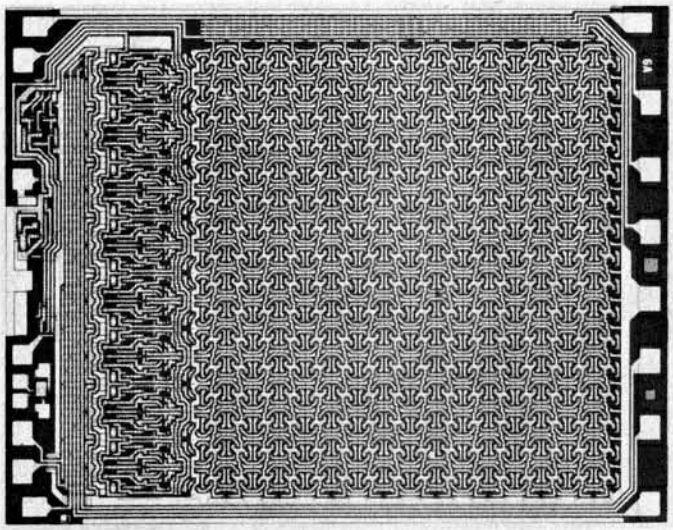
Isoplanar has obvious ramifications far beyond the memory area. Some of these will probably be found in very high speed 9500 ECL logic circuits and high complexity arrays. Here Isoplanar could significantly impact the design of large computer systems intended for the mid to late 70's.

Many other areas of application for the process have been proposed. Some of these were discussed in a recent article in *Electronics*. See page 8 . These applications include linear circuits, discrete devices, radiation hardened products, and improved MOS processing.

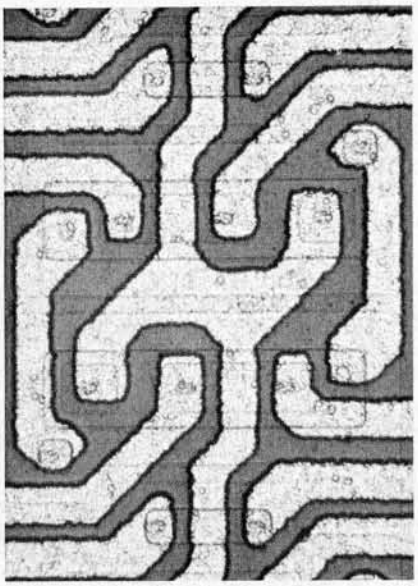
CONCLUSION

The Isoplanar process, as developed by Fairchild, provides the ability to design integrated circuits which combine the complexity of MOS with the performance of TTL and ECL. The first product available today, a 256 bit memory, demonstrates the commercial feasibility of the process. Projected devices for the near future should permit TTL and ECL devices to dominate mainframe and buffer memories where high performance or direct bipolar compatibility are important. MOS products will continue to remain important where low power or very large, relatively slow systems are required. In the long term Isoplanar will impact all areas of integrated electronics because of the advantages of high performance, high reliability and yield improvement which will offer benefits to both the semiconductor vendor and his customer.

CONVENTIONAL BIPOLAR



114 x 145 mils

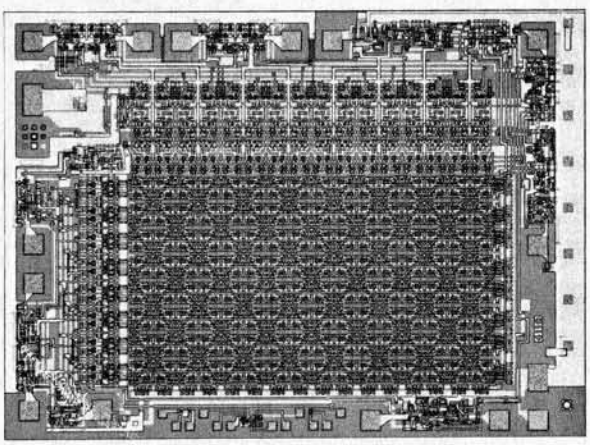


30 sq. mil Storage Cell, Using Epitaxial Resistors

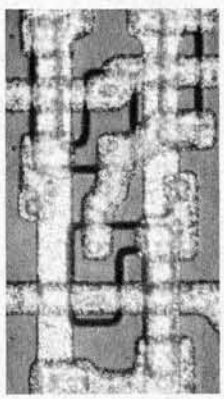
(3a) 93400 Partially decoded 256 bit read/write memory used in Illiac IV.

70 ns access time
2.5 mW/bit

ISOPLANAR



96 x 126 mils



15 sq. mil storage cell

(3b) 93410 Fully decoded 256 bit read/write memory.

50 ns access time
2.0 mW/bit

Fig. 3. Photomicrographs of 256 bit TTL memory devices.

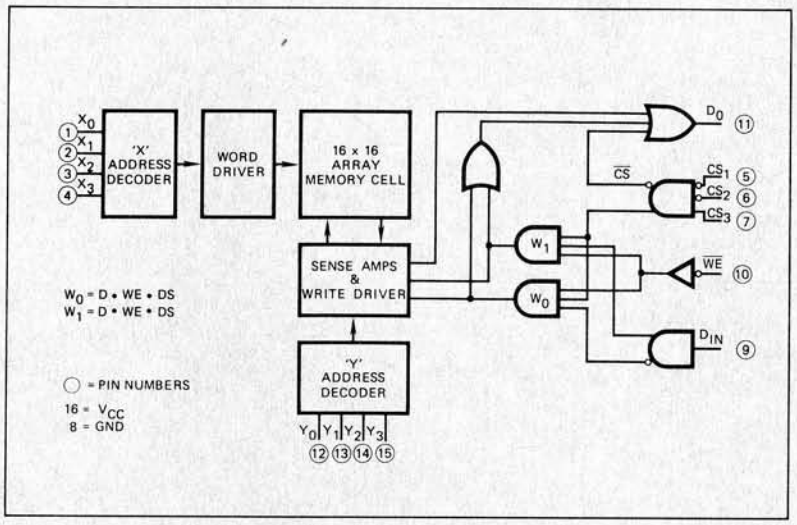
Fig. 4.

ISOPLANAR READ/WRITE MEMORIES

93410 – 256 BIT TTL RAM

GENERAL DESCRIPTION – The 93410 is a high speed 256-bit TTL read/write memory with full decoding on chip. The memory organized as 256 words x 1 bit is designed for scratch pad, buffer and distributed main memory applications.

The 93410 has three chip select lines to simplify its use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.



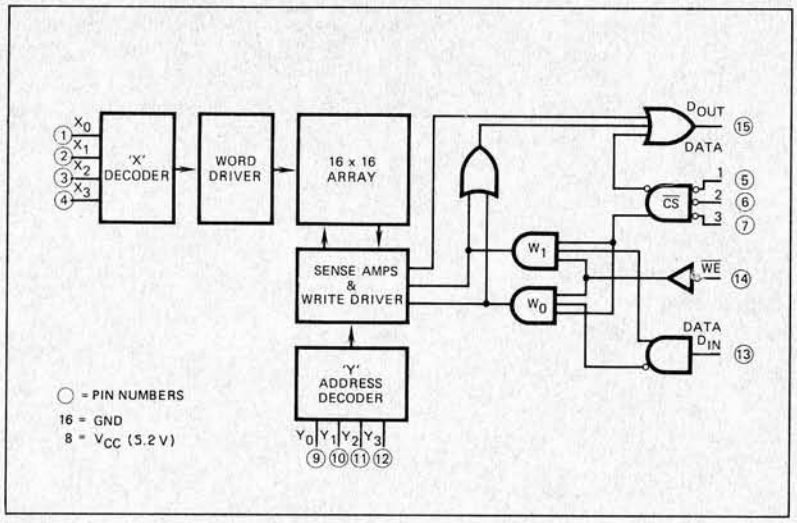
FEATURES
- ORGANIZATION – 256 WORDS X 1 BIT
- THREE HIGH SPEED CHIP SELECT INPUTS
- 50 ns READ ACCESS TIME
- NON INVERTED DATA OUTPUT
- ON CHIP DECODING
- POWER DISSIPATION – 2 mW/BIT
- TTL COMPATIBLE

95410* – 256 BIT ECL RAM

GENERAL DESCRIPTION – The 95410 is a 256-bit read/write random access memory organized 256 words x 1 bit. It has an access time of less than 40 ns and is designed for high speed scratch pad, control and buffer storage applications.

The 95410 includes full decoding on the chip, has separate data in and data output lines and has three active low chip select lines.

The device is fully compatible with the Fairchild 9500 ECL family and includes on chip temperature compensation to permit interfacing with low power gates without any loss of noise immunity.



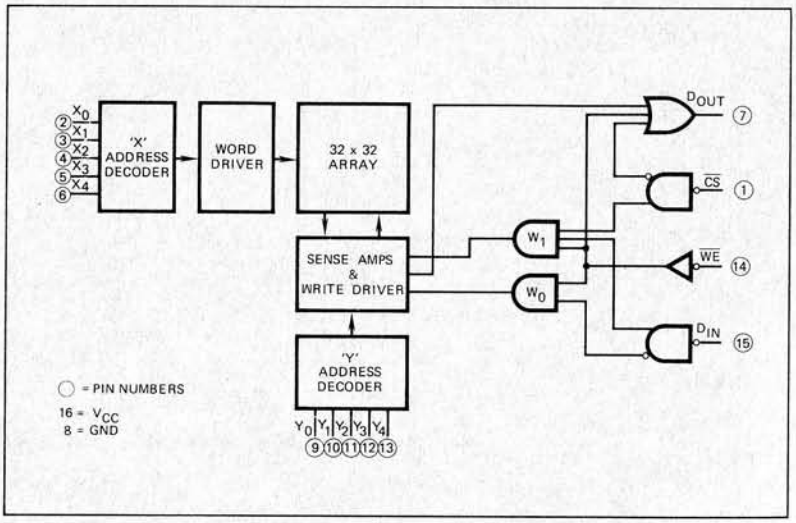
FEATURES
- ORGANIZED 256 WORDS X 1 BIT
- READ ACCESS TIME < 40 ns
- CHIP SELECT ACCESS TIME < 10 ns
- POWER DISSIPATION 2 mW/BIT
- 60 K OHM INPUT PULLDOWN RESISTORS
- WIRE-ORABLE OUTPUTS
- 9500 TEMP. COMPENSATED ECL LOGIC LEVELS

93415* – 1024 BIT TTL RAM

GENERAL DESCRIPTION – The 93415 is a 1024-bit read/write random access memory organized 1024 words x 1 bit. It has an access time of less than 100 ns and is designed for buffer and control storage and distributed main memory applications.

The 93415 includes full decoding on the chip, has separate data and data output lines and an active low chip select line.

The device is fully compatible with the Fairchild 9300 MSI-TTL family and has an uncommitted collector output for ease of memory expansion.



FEATURES
- ORGANIZED 1024 WORDS X 1 BIT
- READ ACCESS TIME < 100 ns
- CHIP SELECT ACCESS TIME < 50 ns
- POWER DISSIPATION 0.5 mW/BIT
- INPUT LOADING 0.25 TTL UNIT LOADS
- UNCOMMITTED COLLECTOR OUTPUTS
- TTL COMPATIBLE

*IN DEVELOPMENT, AVAILABLE 1972.

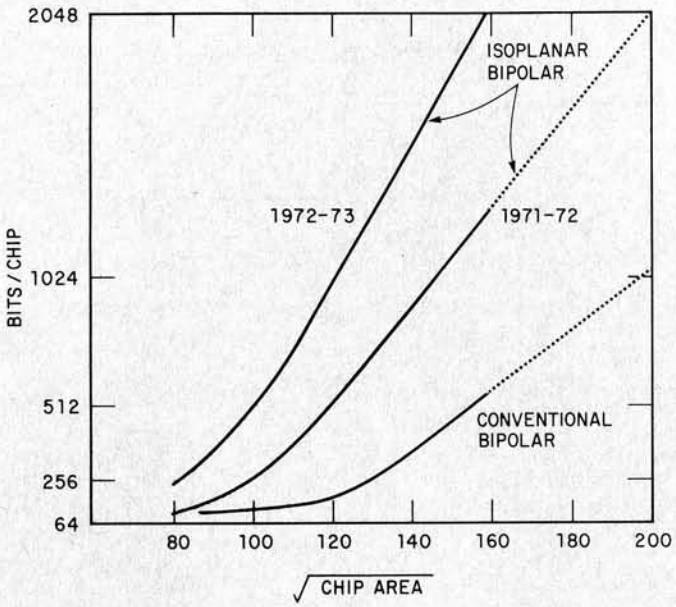


Fig. 5a. Number of bits per chip versus chip area for conventional and Isoplanar memories. (Using mask design rules suitable for high volume, high yield manufacture.)

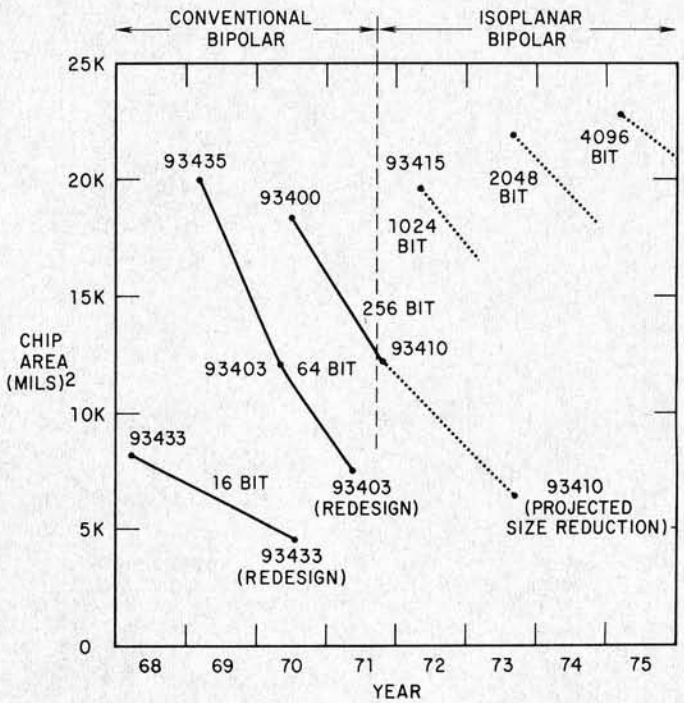


Fig. 5b. Increase in complexity versus time for Fairchild TTL Read/Write Memories.

BIPOLAR READ/WRITE MEMORY CHIP SIZE

Solid state

Isoplanar process stirs IC houses

Originally aimed at fabrication of dense bipolar ICs, Fairchild's method shows promise for high-frequency transistors and diodes—even MOS devices

by Robert Henkel, Managing Editor, News, and Stephen Wm. Fields, San Francisco bureau manager

Soft sell in the hotly competitive semiconductor industry is about as incongruous as a McGovern button on President Nixon's lapel. But in a business where "advances in the state of the art" are announced weekly, Fairchild Semiconductor's disclosure last month of its Isoplanar oxidized isolation process for making bipolar ICs was conspicuously conservative—it even made a point of noting that "there's no assurance that its commercial exploitation would be profitable."

Nonetheless, IC makers feel that Isoplanar is a significant development, and their excitement over oxide isolation for bipolar circuit fabrication is reflected by the growing amount of development work. Many agree that Isoplanar promises more circuit-packing density and higher yields, which could lead to reduced costs. And not only could the process make bipolar more cost-competitive with MOS, but ironically, it also looks very promising for MOS fabrication itself (see panel).

"If anything, Fairchild is being too modest with Isoplanar," declares a top IC circuit designer for RCA. A major West Coast semiconductor maker says that Isoplanar "as a technology, is top-notch. It will do all Fairchild says it will—if they can make it." He calls it "close to the ultimate" in bipolar fabrication.

P. T. Panousis, member of the technical staff at Bell Laboratories' semiconductor device lab in Murray Hill, N.J., says the Fairchild work is "very interesting. It should have a bright future in ICs," he predicts, adding that oxide isolation is "one of the things we are quite hot on now." He maintains no new bipolar process has the potential to compete with oxide isolation structures in packing density.

In the Fairchild approach [*Electronics*, March 1, p. 53], a passive insulator-oxide ring provides isolation between adjacent devices, replacing the active p-type diffusions that isolate conventional bipolar devices. Since the isolation serves as an insulator, the isolation region doesn't have to be separated from the transistor base.

One of the biggest advantages of Isoplanar is that, except for the oxide step, it's processed conventionally, says Panousis. "This is important because most performance-improving devices—emitter-coupled logic for example—require tricky, expensive processing," he notes.

Panousis concurs with predictions of improved yields. As Fairchild has pointed out, with a deep oxide covering much of the silicon, pinholes and defects in the silicon are not as serious as they are in conventional bipolar circuits. In fact, one Fairchild official says it's possible that yields could double.

Another big advantage that's widely acknowledged is improved circuit density, a major factor in lowering costs. "We've tried Isoplanar and it works in saving space between devices," says Sven Simonsen, director of bipolar technology at Advanced Micro Devices Inc., Sunnyvale, Calif. "You can save almost half in some geometries," he adds.

First assessments of the Isoplanar process obtained from other device makers often focused on one problem: growing the thick oxide layers. The length of time required at high temperatures to grow the oxide layers can be a real pitfall, says an official at one top western semiconductor house. However, Doug Peltzer, an Isoplanar developer, replies simply that the diffusion is not done at high temperatures, "so this is not a problem."

Another headache mentioned was the process's thin (1 to 2 microns) epitaxial layers. These require very close control to prevent emitter-collector shorts—the diffusion "pipe" problem. But again, Peltzer says this is not a problem because the base diffusion itself is not thin. Another possible source of trouble is inversion in the base region. "If the base is too lightly doped, it won't get the proper inversion under it," comments Bell Labs' Panousis. Fairchild got around this by putting the collector in the middle, but this cost space.

While Fairchild may have been cautious in announcing Isoplanar, it's moving ahead on products faster than some in industry realize. The first Isoplanar device will be a 256-bit RAM. Next step will be a 1,024-bit RAM, which will occupy the same chip area as a conventional 256-bit bipolar RAM.

C. Lester Hogan, president of parent Fairchild Camera & Instrument Corp, is brimming with enthusiasm: he likens Isoplanar's impact on bipolar technology to the silicon gate on MOS. He predicts that by next year, silicon gate MOS shipments will pass metal gates.

Primary target for Isoplanar is memories and complex functions at the MSI and LSI level, but there are other potential areas of interest for Isoplanar. For example, Bell Labs' Panousis says the Fairchild process can be applied to very-high-frequency discrete transistors as well as ICs. He feels it can be used to attain a frequency above X band, but won't pinpoint it. The high frequency is possible because the oxide isolation technique reduces sidewall capacitance—and low capacitance means higher-frequency operation. Other circuit elements, such as diodes, can be made simply by encircling a piece of p-type material with oxide.

Fairchild also admits that Isoplanar is "more amenable" to combining MOS and bipolar devices on the same wafer in simultaneous diffusion. And another application it already is examining is radiation-resistant circuits. □

All this and MOS too

Fairchild's goal in its hard push on Isoplanar development was to improve bipolar fabrication so it could compete with MOS in density—and thus in price. However, Fairchild now admits that the new process also can be applied to MOS devices. And indeed, other semiconductor companies are interested in Isoplanar or the older, two-step Planox oxide isolation method for their own MOS circuits.

"I think the Isoplanar process is a good one for both bipolar and MOS circuits," says Kenneth Moyle, director of MOS operations at Intersil Memory Corp. It can eliminate an oxide step in MOS, and because it also reduces sidewall capacitance, "we get faster MOS devices." He says Intersil has made devices with the process.

The Hughes Microelectronic Products division, Newport Beach, Calif., has been doing R&D on the Planox process for about a year; it expects first applications to be in new types of high-density complementary MOS circuits. Another top semiconductor maker, which isn't interested in Isoplanar because it says it has its own process, is producing MOS circuits with cells measuring just 6 square mils, and it already has shrunk MOS cell size in the lab to just 1.5 square mils.

FAIRCHILD
SEMICONDUCTOR