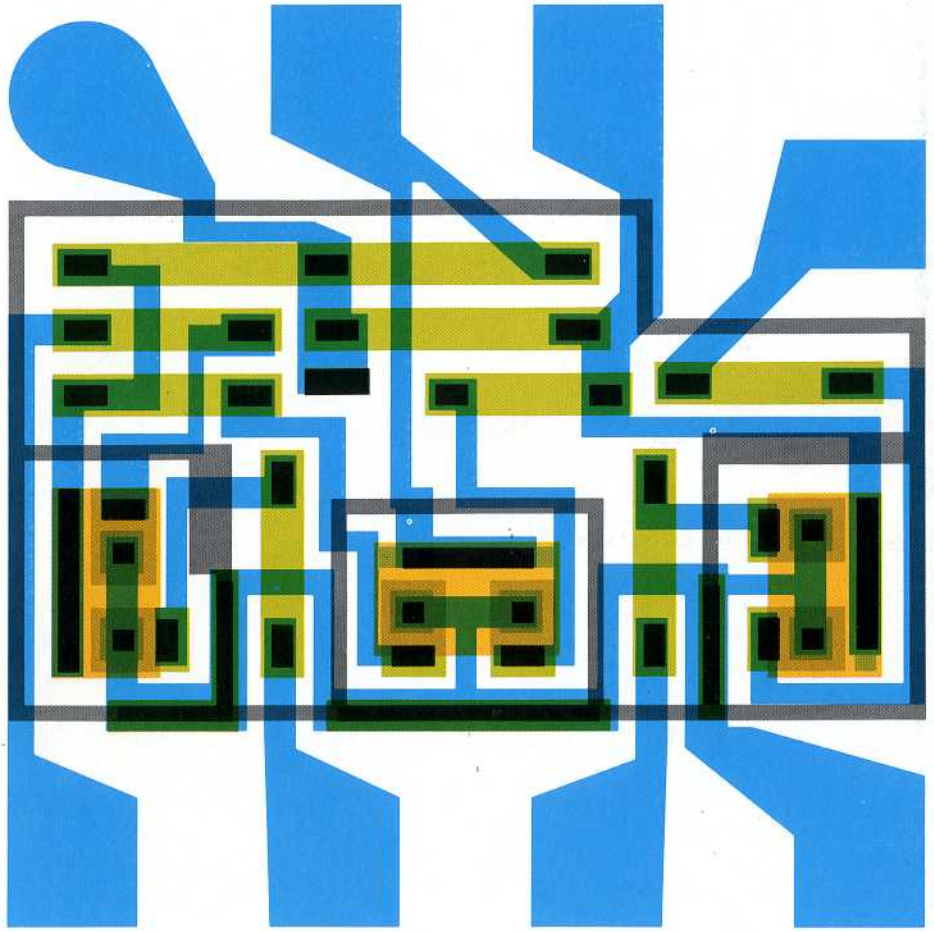
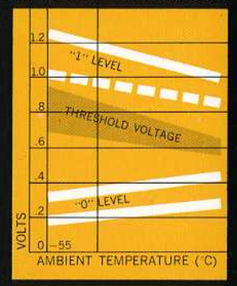
FAIRCHILD EPITAXIAL MICROLOGIC

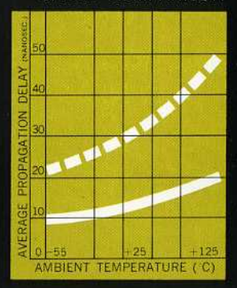


EPITAXIAL
NON-EPITAXIAL

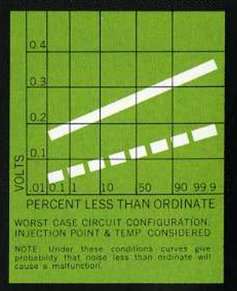
LOGIC LEVEL COMPARISON



SPEED COMPARISON



STATISTICAL DC NOISE IMMUNITY



This brochure describes the process used to produce the most advanced, completely integrated silicon microcircuits available for computer logic applications—Fairchild's EPITAXIAL MICROLOGIC.

Epitaxial Micrologic replaces its predecessor, non-epitaxial Micrologic, because it is faster, more rugged and less expensive. The graphs on the left show significant epitaxial performance superiority. It is more immune to extraneous computer noise, more stable throughout the temperature range—55°C to 125°C, and it exhibits much improved saturation characteristics. Although its development embodies the latest technologies, it is available in production quantities.

The difference between Epitaxial Micrologic and non-epitaxial Micrologic involves both process improvements and performance improvements. This brochure follows the manufacturing process of a typical element, illustrating both sources of improvements.

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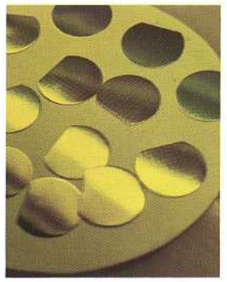
PROCESS INTRODUCTION

The process used to manufacture Epitaxial Micrologic elements is an extension of the Planar* Processes developed by Fairchild to produce Silicon transistors. The elaborations on the original process are pointed out in the following description. The successful integration of many disciplines into an economical and productive process is a major factor contributing to the performance of Fairchild Epitaxial Micrologic.

*PLANAR: A PATENTED FAIRCHILD PROCESS.

CRYSTAL GROWING

The starting point is the growth of high purity silicon crystals by the Czochralski method: A small, perfect seed crystal, carefully selected for low dislocation and imperfection counts, is lowered into molten silicon, and slowly withdrawn under precise control, forming a large single crystal about six-inches long and one-inch in diameter. For Epitaxial Micrologic, the crystal is grown with a boron impurity to make it P-type, rather than the N-type starting material of non-epitaxial Micrologic.



WAFER FORMING

The crystal is sliced with a diamond saw into many wafers each approximately 12 thousandths (.012) of an inch thick. The cut wafer is then lapped flat, using a very fine grit abrasive, and chemically etched to form an extremely smooth shiny surface. The thickness of the finished wafer is about five thousandths (.005) of an inch. Non-epitaxial Micrologic devices require even thinner finished wafers due to the necessity of diffusion from both surfaces. Epitaxial techniques side step this requirement so that thicker, less fragile wafers are produced. The added thickness strengthens the individual wafers resulting in lower wafer loss during the manufacturing process.

OXIDE GROWTH

Many wafers of silicon—representing hundreds of potential Micrologic elements per wafer—are inserted into the grooves of a quartz boat and placed into a furnace containing an oxidizing atmosphere at 1200°C. Oxygen penetrates the crystal lattice at the surface of the wafer, combining chemically with surface silicon atoms to form SiO_2 (silicon dioxide) an inert, stable "glass" which encapsulates and passivates the wafer surface. This step is the key to the reliability and production economy attained through the Planar process.

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COLLECTOR CUTOUT

The passivated wafer begins to take the form of an integrated circuit with the collector cutout step. The wafer is coated with a photosensitive material in a darkroom, and then exposed to light through a high resolution mask. Those portions not exposed are soluble and easily removed with a solvent rinse. At this point, an etch is used to remove the silicon dioxide from those areas not protected by the film of photosensitive material. In this way, cutouts for collector diffusion are photo-engraved through the protective passivating silicon dioxide layer.

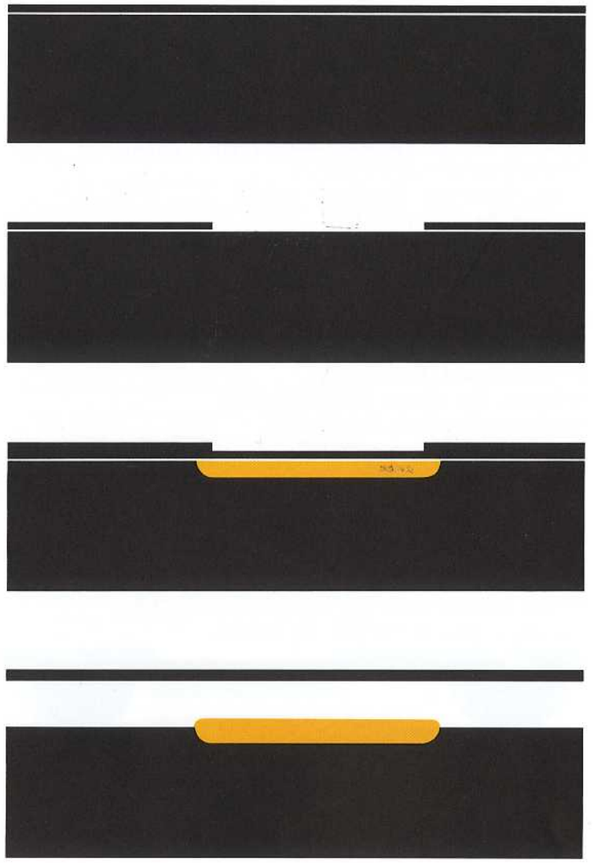
N+ COLLECTOR DIFFUSION

The wafers are placed into a special high-temperature furnace whose atmosphere contains gaseous phosphorus. The temperature is raised and the phosphorus impurity diffuses into the exposed silicon, forming a highly doped N+ region. This N+ diffusion is necessary to create a very low transistor collector resistance.

EPITAXIAL LAYER GROWTH

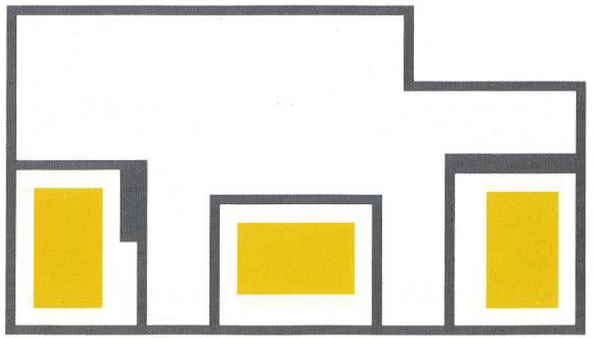
With N+ material diffused within the P substrate, the next step is the growth of the epitaxial layer. This is accomplished in the following manner: First, the passivating surface of silicon dioxide is removed by etching with hydrofloric acid. The wafers are then placed within a thermal reaction chamber where volatile gases are introduced and through chemical reactions, N-doped silicon is grown on the wafer surfaces. Under these conditions, the growing layer assumes the same crystal orientation as the substrate wafer and becomes an addition or extension of this material. The thickness and resistivity of this epitaxial layer affect the speed and saturation parameters of the finished device. After the epitaxial growth, an oxide is grown on the wafer as before, forming a new passivation for the rest of the manufacturing process.

The design developing on the facing page is a simulated mask for the progressing photo etching process.



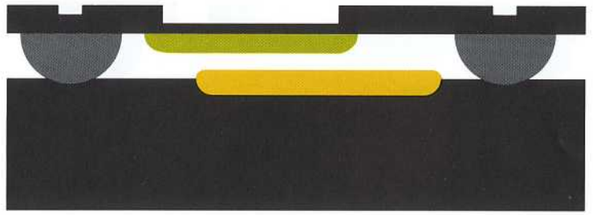
ISOLATION MASKING AND DIFFUSION

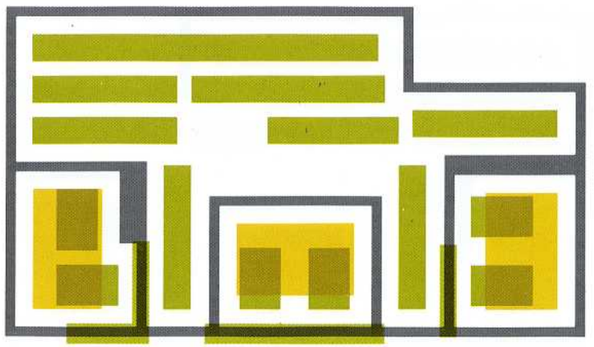
The process now returns to steps similar to the non-epitaxial Micrologic process. Isolation masking and diffusion are performed to electrically isolate transistors and resistors from one another. Bands are etched through the silicon dioxide surface to prepare for the isolation of individual circuit parts. The wafers are then placed into a furnace operating at controlled high temperature in an atmosphere of boron (P-type dopant) for isolation diffusion. The dopant diffuses through the exposed epitaxial N-type layer, forming a highly concentrated P-type region extending through to the P-type substrate. During the diffusion, the silicon dioxide layer regrows over the masked area. In this manner, isolated pockets of N-type material which will become the collector regions or resistor regions, are formed.



BASE MASKING AND DIFFUSION

The wafer is again masked and etched for the simultaneous diffusion of the base region and resistors. Once again boron is used as the diffusing impurity in this high-temperature diffusion. The base region is diffused into the N-type epitaxial layer to form the collector-base diode of each transistor as well as all the resistors in the circuit. The oxygen atmosphere in the furnace re-oxidizes the cutout portions of the wafer surface and seals them against contamination or injury. As the diffusion progresses downward into the wafer, it also proceeds laterally, diffusing into the silicon covered by the original protective oxide.





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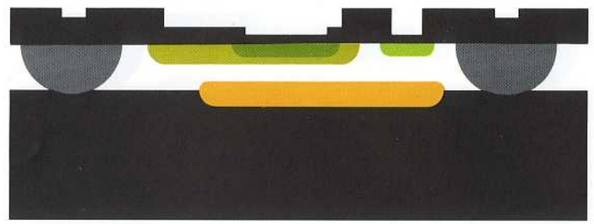
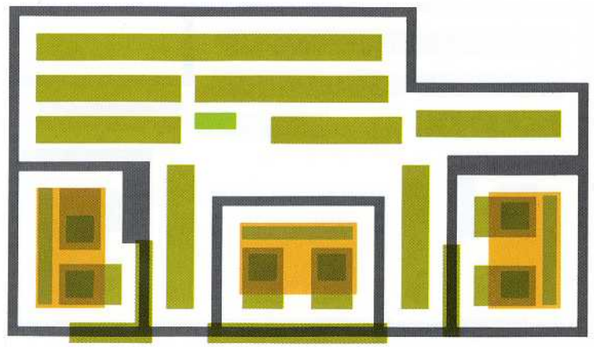
EMITTER MASKING AND DIFFUSION

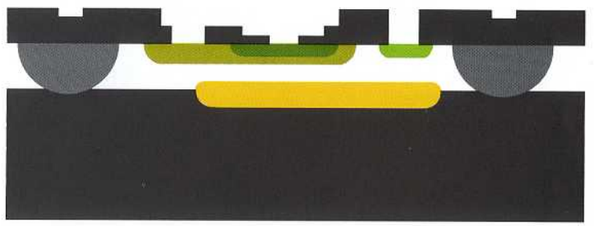
Another precisely indexed masking step is performed to remove oxide for the emitter diffusion and for the top-side collector contacts. In a high-temperature step, phosphorus (an N-type impurity) — is diffused into the surface at 1200°C. This impurity forms the emitter region. Again silicon dioxide forms as the diffusion progresses, covering the photo-engraved area and sealing the surface. Side diffusion carries the junction underneath the protective layer. Notice that in each case the diffused region ends underneath an oxide which existed previously. This oxide permanently protects the actual junctions of the device against exposure to the outside environment.

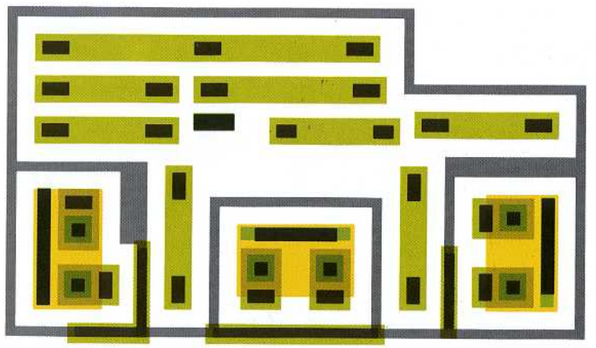




EXPOSURE OF CONTACT AREAS AND METALIZATION

At this point the transitors and resistors of the Epitaxial Micrologic circuit are complete. They must now be intraconnected to form the desired logic circuit. This is done by evaporating metal onto the surface of the silicon wafer using the Metal-Over-Oxide process*. Before this can be done, however, a hole must be photo-engraved over the appropriate regions of the devices so that the evaporated metal can make contact. This is done in a masking step similar to the others. The wafers are now placed into a high vacuum chamber containing a metal evaporator. Aluminum is boiled from a hot tungsten filament forming an atmosphere of metal and other gases. The evaporated metal deposits in a thin, even coat over the entire wafer surface. Many wafers, comprising several thousand Epitaxial Micrologic units, are processed at one time in this fashion.





*METAL-OVER-OXIDE: PATENTED FAIRCHILD PROCESS.

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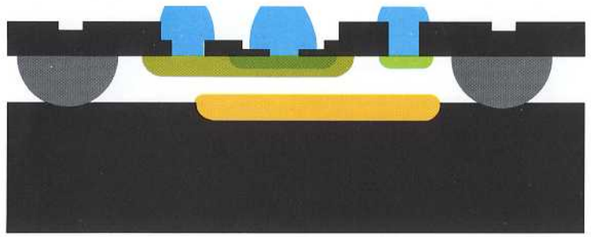
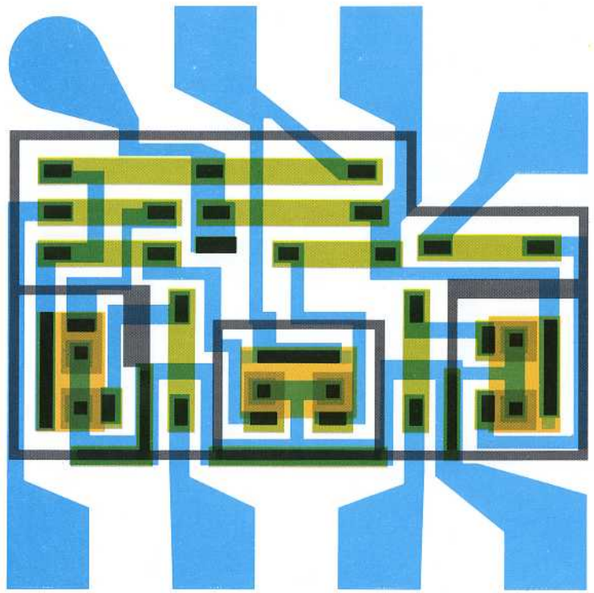
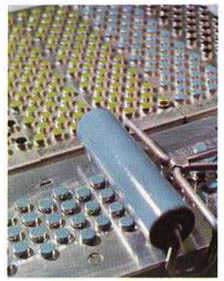
METAL INTRACONNECTIONS

In another precise photo-engraving step, the aluminum layer is masked and selectively etched to leave a pattern of intraconnections between transistor and resistor elements in the logic circuit. The wafers are placed in an alloying oven so that the aluminum intraconnections can be firmly attached to the silicon dioxide surface. The Epitaxial Micrologic wafer is now complete as shown in the figure and needs only to be cut into individual elements and packaged. Up to this point, all operations have been done on many wafers at a time. The elimination of the handling of each device separately is a major factor in the reduction of production costs. This batch processing also increases the reliability and compatibility of devices. All connections to the outside—inputs, outputs, power supply and ground—are brought out to the periphery of the element as large aluminum pads, for easy, reliable connections.







MOUNTING, INSPECTION, CAPPING AND FINAL TESTING

The wafer is cut into small pieces using a technique very similar to the cutting of glass. A diamond scribe is used to make fine scratches on the surface of the wafer between the circuits. The wafer is mechanically separated along these lines into uniform, square dice. The dice are then cleaned thoroughly, dried and inspected for defects under high-power microscopes before expensive hand labor is incurred. The die is then soldered to the center of a header using a high temperature alloy preform and proceeds to a lead-bonding station. Using a capillary ball-bond, proven through four years of production experience at Fairchild, a fine gold wire is attached to each of the input, output and supply pads of the device. Each lead is held against a header post and securely spot-welded. Following lead-weld, a final optical inspection is conducted to guarantee that the die has not been damaged in any manner up to this time. After passing this inspection, the mounted device is thoroughly cleaned and a cap is welded to the header, completing the assembly. Epitaxial Micrologic can share the production line with Planar transistors at any time, since the processes are identical from dicing through final seal. This packaging operation uses techniques whose reliability has been verified extensively on Planar transistors and non-epitaxial Micrologic. After final seal, each Micrologic element is subjected to a number of tests to insure its reliability. They are subjected to mechanical shock tests, temperature cycling, and centrifuge acceleration tests as well as rigorous electrical testing. All Micrologic elements are 100% tested and sorted on Fairchild Series 4000 integrated circuit testers. These machines check all measurable DC parameters and also perform a thorough worst-case functional operation test. Finished units are supplied to Production Control for packaging in boxed stock for shipment to customers. Even after their final electrical tests, devices are continually sampled by Quality Control to confirm their conformance to rigid specifications. Each week a sample of devices is placed on a 125°C operating life test in a continuing evaluation program.

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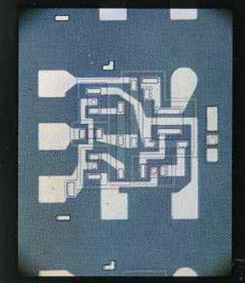
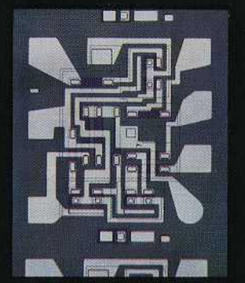
HISTORY

The first production integrated microcircuits were silicon Planar* devices, introduced by Fairchild in 1960. Because these units were manufactured for digital computer logic applications, they were called Micrologic and abbreviated "μL"*. By 1961 the Micrologic family had grown to six basic mutually compatible integrated circuit elements. These consisted of a buffer element ("B" element), a counter adapter element ("C"), a flip-flop element ("F"), a gate element ("G"), a half-adder element ("H"), and a half-shift register ("S"). Using a modified form of direct-coupled transistor NOR logic known as RTL (resistor transistor logic) NOR logic, this family of Micrologic permitted the synthesis of all computer logical functions. The evolution of Epitaxial Micrologic increases this basic family of elements with the addition of two more devices. These are a 4-input gate element ("G_1"), and a dual 2-input gate element ("D"). Photomicrographs of the Epitaxial Micrologic family are shown on the facing page. The higher circuits per wafer ratio of Epitaxial Micrologic on finished wafers is shown in the photographs above. Although Micrologic offered the solution to routine design problems, the demand for special integrated circuit devices stimulated the creation of the custom microcircuits group. Through this facility, Fairchild engineers are able to offer the capability of design and production of special microcircuits manufactured to customer specifications. The epitaxial techniques are also available for these custom microcircuits.



B



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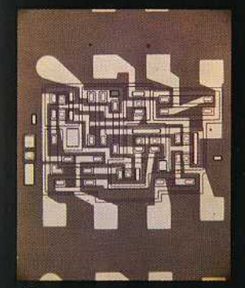

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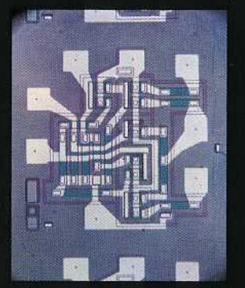

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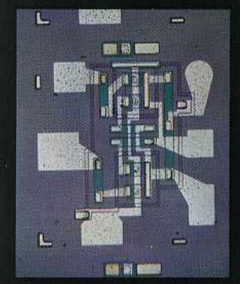
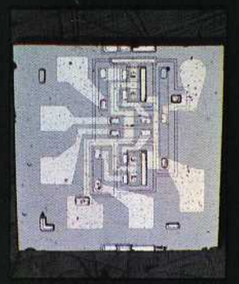
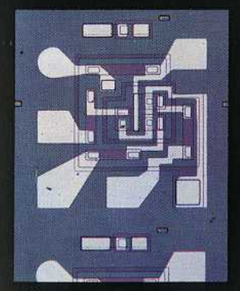


F



G_1



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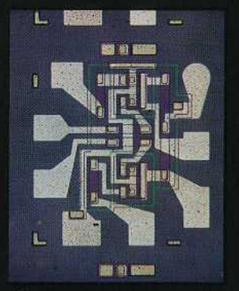

D

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