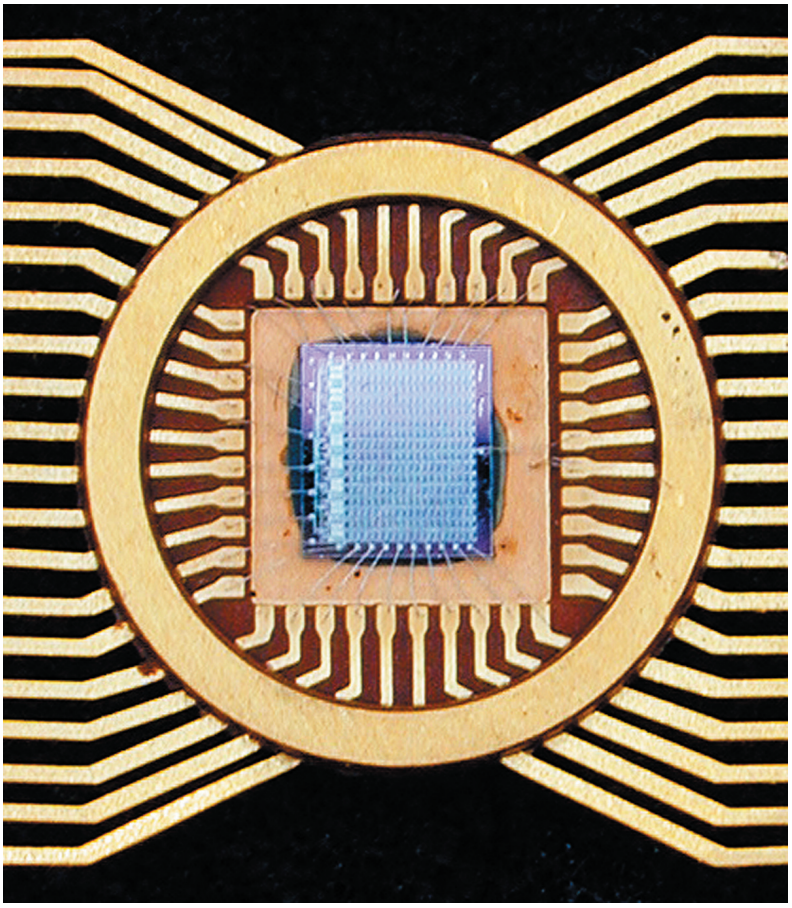
RCA COS/MOS 288-bit RAM Array 1968. Gift of Richard Ahrons



Complementary MOS Memory Arrays

by

C. HANCHETT, S. KATZ, and A. K. YUNG

Reprinted from DIGESTS of Government Microcircuits
Applications Conference, October 1968

Publication No. ST-3814

RCA Electronic Components
Somerville New Jersey

PRINTED IN U.S.A.

COMPLEMENTARY MOS MEMORY ARRAYS*

C. Hanchett, S. Katz, and A. K. Yung
RCA Electronic Components
Somerville, N.J.

This paper describes a large-scale integrated COS/MOS memory that contains 288 memory bits plus an associated decoder and read-write drivers. Complementary-symmetry MOS digital circuits are ideally suited for high-packing-density memory arrays because of their economical use of silicon area, extremely low power dissipation, high-speed circuit operation, and tolerance to large variations in device parameters. Although the inherent speed of operation of COS/MOS circuits is somewhat lower than that of bipolar circuits, their packing density is higher and their power dissipation is much lower. All-p-channel MOS memories are also amenable to high packing density, but they cannot operate at high speeds without complex clocking arrangements, and their standby power dissipation is much higher than that of COS/MOS memories.

A 288-BIT COS/MOS MEMORY SYSTEM

A block diagram of the 288-bit complementary MOS memory array (16 words by 18 digits) is shown in Fig. 1. The memory is word organized and nondestructively sensed. Although word organization makes

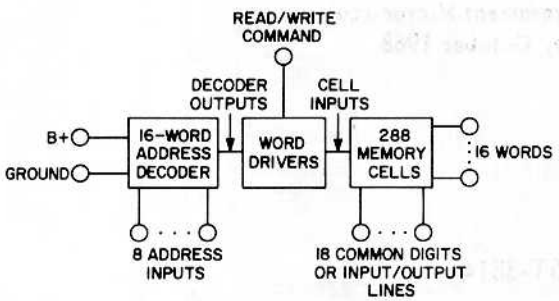


Fig. 1 – Block diagram of 288-bit complementary MOS memory array.

decoding and word-drive circuits more complex, it simplifies the memory cell and, because the number of memory cells is much greater than the number of decoder and word-drive circuits, over-all pellet size is minimized.

The integrated array consists of a 16-output address decoder, 16 word drivers (which also select either the read or write mode of operation), and 288 memory cells. Eight address inputs are required for a high-speed 16-word MOS address decoder when an X-Y-select type of configuration is used, and a read/write command signal is necessary for activation of the word-drive circuits. Information is written into, and read out of, 18 common digit (input-output) lines to minimize external connections to the chip. The memory operates with a single voltage supply. The 288-bit array, consisting of approximately 1850 devices, can be fabricated on a silicon chip 155 mils by 175 mils for mounting in a 30-terminal package. Large memory systems can be constructed through the use of many of these array.

*The work described in this paper was supported by the United States Air Force under contract AF33(615)-3491.

MEMORY CELLS

The memory cell designed for use in the 288-bit memory arrays has two word lines, W_1 and W_2, and one digit line, D, as shown in Fig. 2. Transistors Q_1, Q_2, Q_3, and Q_4 comprise the binary-storing flip-flop, and transistors Q_5 and Q_6 form a complementary transmission gate. When information is to be written into a memory cell, W_1 is set to zero and W_2 to + Vs to activate the transmission gate. The voltage at point A is then equal to that of the digit line. When W_1 is set to + Vs and W_2 to zero, the transmission gate is opened and the flip-flop stores information.

For sensing of the state of the flip-flop, the signals W_1, W_2, and D are set to zero. Under these conditions, Q_5 is biased "on" and Q_6 is biased "off." If the potential at point A is zero, there is no sense current in the digit line. However, if A = +Vs, a current is sensed because transistor Q_5 operates as a source-follower. Transistors Q_3 and Q_4 are made smaller in width than Q_5 to avoid a change in cell state when nondestructive read-out operation is desired and to insure reliable write-in operation. However, the width of Q_3 and Q_4 is adequate to prevent destructive read-out.

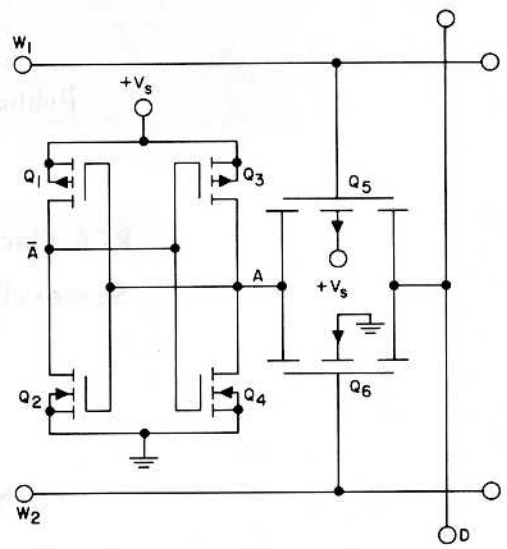


Fig. 2 – Six-transistor memory cell.

DECODER

The 16-word simplified X-Y-select type of address decoder is shown in Fig. 3. This decoder has very fast decoding time, requires few transistors, and occupies little silicon area. The decoder circuit employs a 4-by-4 matrix, i.e., there are four X signals and four Y signals.

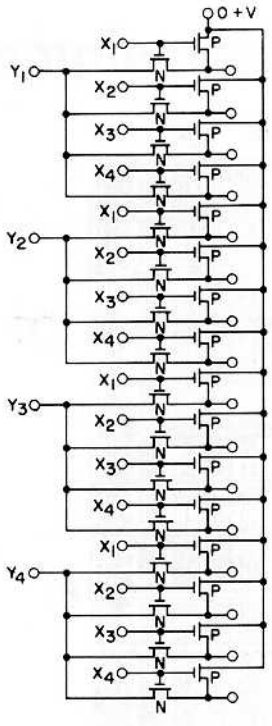


Fig. 3 – X-Y-select decoder.

When one X and one Y signal are selected, only one of the sixteen n-type decoding transistors is biased "on" to perform the decoding function.

If a full binary form of decoder were used, there would be four "on" transistors in the selected path. Because such long series strings lead to slow decoding times, the X-Y-select decoder is preferred for this application. With this type of decoder, the 288-bit memory appears on the outside as a four-by-four X-Y-select memory 18 bits deep.

MEMORY-CELL ARRAYS

An experimental 8-word by 9-digit memory array consisting entirely of circuits of the type shown in Fig. 2 has been designed and fabricated on a 103-mil by 81-mil silicon pellet. Individual cells require about 60 square mils of silicon. The complete 72-bit array consists of 432 MOS transistors and is mounted in a 28-lead flat package. A photomicrograph of the pellet, which contains no decoding or word-drive circuits, is shown in Fig. 4. Several 72-bit memory arrays in which all bits are operational have been fabricated. These arrays have typical write-in times of 40 nanoseconds and read-out times of 30 nanoseconds. The quiescent power dissipation is less than 20 microwatts when a supply of 10 volts is used. The pellets were made by use of the process shown in Fig. 5.

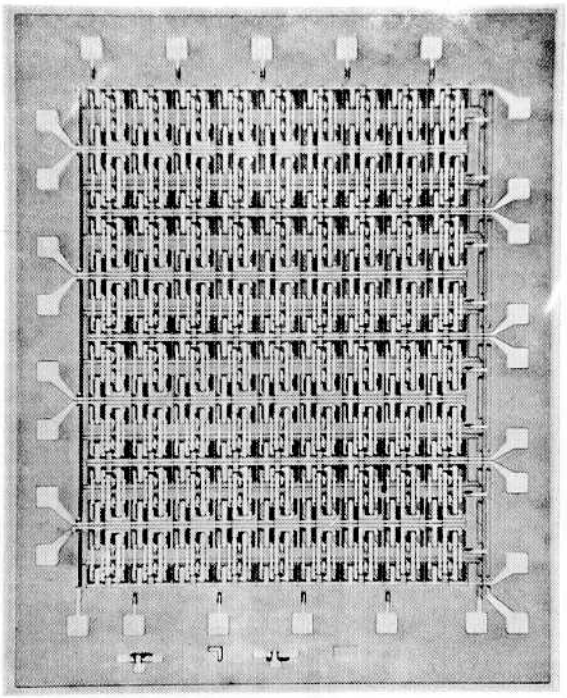


Fig. 4 – Photomicrograph of 72-bit array pellet.

Fig 6 shows a computer-drawn sketch of the 288-bit memory. The decoder and word drivers are shown on the right of the chip, and the 288-bit memory (16 words by 18 digits per word) is shown at the left.

CONCLUSIONS

The feasibility of fabricating large-scale integrated COS/MOS memories has been demonstrated by construction of operable 72-bit memory arrays. Their low quiescent power dissipation, high speed, and high packing density make COS/MOS memory arrays very attractive for future memory systems.

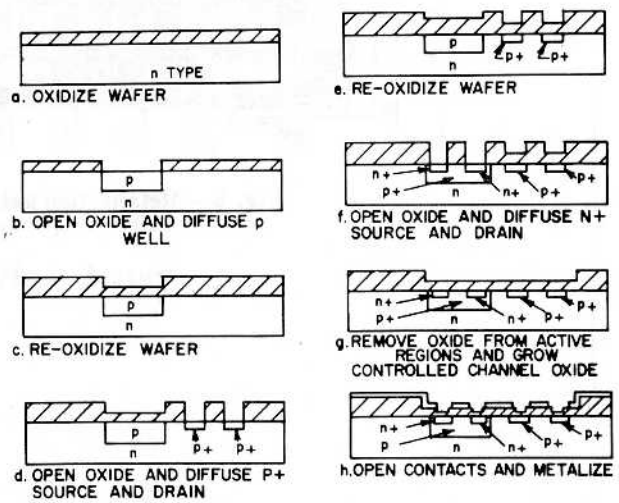


Fig. 5 – Complementary-symmetry MOS transistor processing steps.

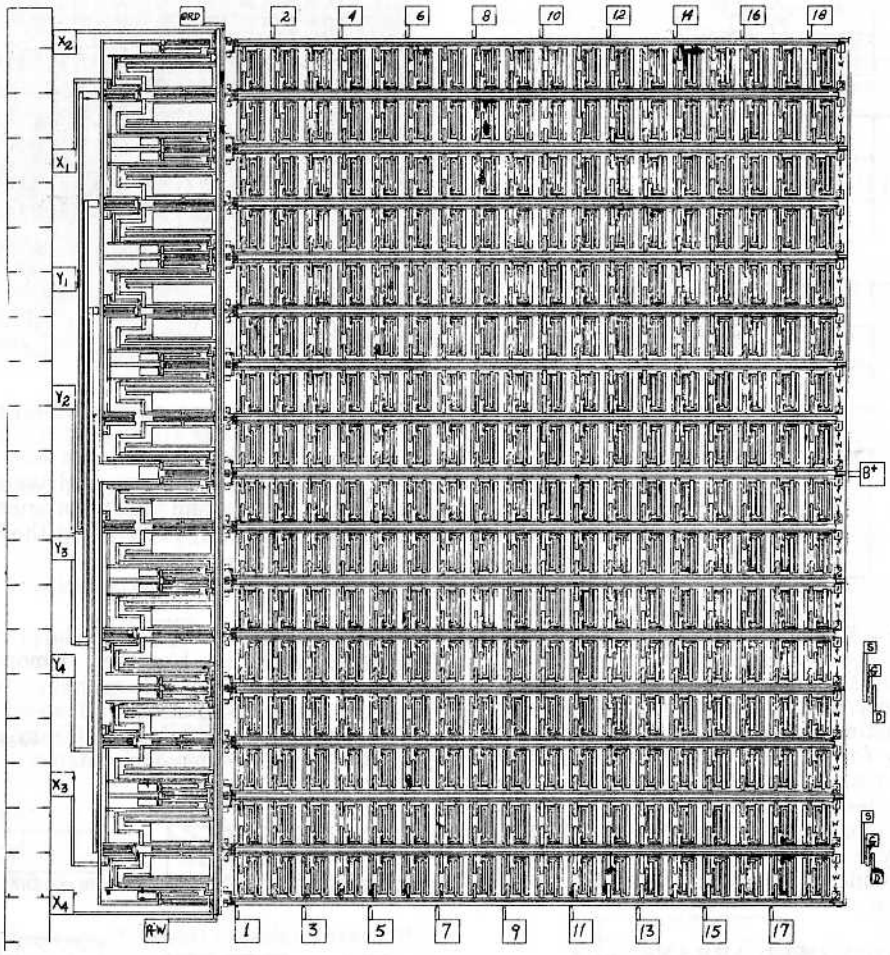


Fig. 6 – Metalization pattern for 288-bit memory.