CONFIDENTIAL

digital INTEROFFICE MEMORANDUM

SUBJECT: COMPUTER ON A CHIP DATE: April 23, 1971

TO: Operations Committee FROM: Roger Dow

cc: Dick Best
Ed Kramer
Howie Painter

DEPARTMENT: Administration

I. General

There has been a lot of talk recently about putting a computer on a single integrated circuit chip. This report deals with what the concept really means and what the implications are for IC manufacturers and small computer manufacturers such as DEC. Information has been gathered by talking with several people within DEC, reading technical publications, and past experience with semiconductor manufacturers; their ideas plus my own combine to give an assessment of the situation.

It would take a very big investment for an IC manufacturer to get completely in the computer business. They have a device orientation which concentrates on producing many thousands of small identical units. To really be profitable in the computer business, the company has to have a computer atmosphere. This holds true for all people, not just design engineers. Testing, documentation, construction and other decisions that have to be made by low level people would suffer. Extensive software is needed to support a computer operation. Fortunately for us, IC manufacturers do not now have these capabilities and probably won't have in the immediate future.

II. Semiconductors

The ICs have been increasing dramatically in complexity and packaging density. Solid state memories are here and will soon offer smaller size and cheaper price, but they are volatile. DEC is staying abreast of this technology. We are currently or will soon be using MOS memories and also two rather complicated IC chips. One is an Arithmatic Logic Unit (ALU) which has 24 pins and can perform over 16 functions for 2 4-bit words. This will be the heart of our new CPU's since it handles addition, subtraction, and other logic operations very easily. Another device, the Universal Asynchronous Receiver Transmitter (UART) is a 40-pin device that contains a complete teletype interface. We have been working with TI on this device, and it is significant to note that we are the ones supplying the logic specification and also uncovering logic bugs of theirs. With the more complex ICs, multiprocessors and microprogramming will be the way of the future. We can make more use of read only memory (ROM) and parallel processing.

If an IC manufacturer, tried today to make a complete computer on a single chip, he would run into all the problems we face concerning design and modification. Would he have to make a new mask every time a logic bug was discovered? The number of leads required for a full blown parallel computer is fairly large, on the order of 100 wires. What type of package could he use? There is also the problem in driving buses and lights. Power would have to be dissipated and this would require separate packages to take care of heat dissipation.

III. Systems

The strength of a computer company over an IC manufacturer is in its depth of computer oriented people, and its ability to define architecture and instruction sets, and to do real logic design and programming. More complex ICs mean less value added on the central processor. New cost tradeoff must be weighed and such factors as packaging, power supply, testing and documentation must be considered. Not everything can be made of ICs. There will always have to be lights, switches and computer peripherals.

One market for the IC manufacturers would be for special purpose controllers. The application should be well defined and have a high usage for them to take advantage of such a situation.

In the future, more attention will have to be paid to communications, terminals, byte handling capability and peripheral equipment. Very possibly, we can make a large computer from many small ones. This also has the advantage in case of failure of using an alternate data path or control mechanism.

IV. DEC's Position

There is a definite difference in marketing strategy and requirements between the OEM and the end user. The OEM can oftentimes get by with a stripped down computer, minimum memory size, and minimum software, but he wants minimum price. The end user tends to buy large systems with many peripherals and mass storage. He often needs all the help he can get in terms of programming, Field Service and documentation. From the foregoing description, it looks like we could lose a good percentage of our OEMs to an IC manufacturer who could sell a simple IC processor. Actually, the OEM, since he has the talent and resources, would probably be in a better position if he would like to compete against us in the small computer market, especially for simpler control applications.

DEC could try to acquire an IC facility, however, there would be many problems with this. We don't really understand semiconductor processes. Also the semiconductor manufacturers Return On Investments (ROI) lately has been very low. We should continue to stress our system and software capabilities, our worldwide field service and our computer experience. We must continue in a strong position with peripherals. We must stay applications oriented.

Right now, we are using complicated ICs when they really become available, to further enhance our position. When IC manufacturers make a computer on a chip, DEC will make better computers.

V. Acknowledgements

I wish to thank Dick Best, Ed Kramer and Howie Painter for their help with this report.

Some of the recent articles of interest are:

Minicomputer networks - a challenge to Maxicomputers
Electronics - March 29, 1971

Little Chips Invade The Memory Market
Fortune - April 1971

The Minicomputer and the Engineer
Electronic Design - April 15, 1971

Guidelines for Minicomputer Selection
Computer Design - April 1971

digital INTEROFFICE MEMORANDUM

SUBJECT: REPORT OF TRIP TO TEXAS DATE: April 23, 1971

TO: Dick Clayton FROM: Rony Elia-Shaoul

DEPARTMENT:

MOSTEK VISIT

The purpose of the trip was primarily to learn more about the company, its capabilities, and whether or not they are serious in building high speed memory chips. The following points were covered in my one day visit:

1. A plant tour which took a short time since the area was small and there were only about 20 employees.

2. The design and layout are done in that compound, along with testing. The processing is done in Worcester, while production packaging is done in Mexico. They have the capability of building a few hundred chips per month on prototype basis in Dallas.

3. They have a few chips they are now producing which include some shift registers, a complex calculator containing about 380 gates and the 1K RAM. They are shipping only 200 units a week of that memory, and they expect the number to be 500 per week in May. They say they are capable of producing a few thousand wafers a week when they hit production in June or July. P channel Ion implementation is the process used on these devices.

4. The final spec on the memory chips is not completely done since they have just changed the mask to produce a lower power device from 600 mw to 400 mw maximum per chip, and the supply voltages are now +5 and -12V only.

5. Mostek has a plan to produce 4K memory chips within the next few months which, in turn, as I see it, will push the priority of high speed chips aside. Right now they are talking of a 300 ns access time for the fast chip with next month, rather than their predicted 200 nanosecond. I believe this chip will be sort of a selected version of their existing memory without a major re-design.

6. Their memory tester is now under the debugging stage since, as Dennis and I found, they are having problems with it. However, their test plans (which we went over in great detail) seems to be very adequate. They test for worst case noise pattern inside the chip and the worst case access time patterns. They do not test in temperature unless requested by customer. However, they do 12 hours baking in 125° C.

7. They have a wirewrap 4K x 18 bit system built and they were in the process of debugging it. Ultimately, it will be built on 2 PC boards of size 4 x 10 inches each. They will be quoting us system price and speed. Specifications of the system were given to me. I think they will sacrifice some of the system speed to get the power switches incorporated in. These switches are aimed to turn off -12V on all the chips except the 1K memory used.

8. EMI is their second source on this memory device, but they are not there yet.

CONCLUSIONS

I think this memory chip is a good candidate for the slow memory system and it should be looked into. It provides the following advantages and disadvantages over the 1103 memory.

a) No need for level shifter at the input.
b) It uses only 2 voltages instead of three.
c) Its control is much simpler, and its address can be changed while reading without the destruction of the data.
d) It uses 16 pins package, rather than 18.
e) Its speed is more sensitive to temperature than the 1103. Its AC spec is given at room temperature only, and it decreases by 1½ ns/°C. The 1103 specs are given over 0°-70°C. Thus, AC spec at room temperature for the system can be faster for the Mostek memory by about 50 ns while it is slower at 70°C by 25 ns.

I am unable to comment on the production capabilities of Mostek since I have not seen their production facilities. However, I have more faith in EMI than in Mostek. Furthermore, I don't think there is any hope for the time being for a high speed device comparable for the 11/40.

VISIT TO TEXAS INSTRUMENTS

The purpose of this visit was primarily to discuss in detail the progress of the Schottky line, its specifications, testing, deliveries, and prices. Secondly, to touch base with the MOS Division for both the single chip and multi-arrays process, and discuss specs, prices, testing, and deliveries.

My first two days were spent mainly with the Schottky Production Engineering people, and especially Pat Buffet who is responsible for that line. The following points were discussed:

1. Progress of the Schottky line. Attached is the update list for deliveries of the components used in the 11/40. Two items were shifted in time which are the 74S181, 74S74. Still, the 74S174 is a few months away from our production schedule.

2. Selection of the 74 174 will give us speed of about 5-10 ns slower than the projected Schottky speed. This question has to be resolved very soon.

3. Discussed with Pat the problem of driving a 25 ohm line, and he suggested that we can drive with two 74S140 gates in parallel and guarantee a 2.2V level for the first voltage step. However, he will not guarantee the deskew between the gates. He was in the process of sending Don Vonada a letter on that subject and his suggestions which tend toward a selection process to be done by DEC. Don has received this letter.

4. Discussed some of the Schottky specs such as output impedance, output voltages, thresholds, AC specs over temperature, minimum rise and fall time, minimum delay specs, etc. Some of the unanswered questions are written in my last letter to Pat, dated April 21st. I found there is a lot we can do with the specs without affecting the cost or the yield.

5. Discussed the glitching problem with JK and D flip flops and the problem of slow rise and fall time. It is important to have the rise and fall time less than 50 ns for the JK flip flop due to some internal race conditions.

VISIT TO TEXAS INSTRUMENTS (CONTINUED)

6. Discussed QC and reliability problems, plus we received some reports on their guard band DC testing for the elimination of the AC test. Dennis O'Connor and I also had a tour on their production testing line. We were unable, however, to talk with the person responsible for designing the AC test jigs for the Schottky as he was not available that week. Dennis will be doing the interfacing with him.

7. Discussed prices and their latest AC specs design goal on the MSI chips. A point of concern here that all the AC specs we have on the MSI chips now are design goals and the actual MSI cells are not yet built to support their prediction. They were hoping that by this week they will have their first characterization data on the 74S74 chip which utilize the MSI cell design. If everything goes well, I predict by the end of April they will have a better idea if their design goals on the MSI chips are really achievable.

CONCLUSIONS

Three devices I found delayed in delivery schedule, but they are still in our time frame.

The business of the 74S174 has to be settled in our group, since it is not available until the first quarter of '72. Yield on the Schottky devices was found to be better than expected as I have been told by Marketing, hence prices will drop (so what else is new??). No second sourcing effort is made by T.I. as they anticipate other companies such as National, Fairchild, and Signetic will do it. National already hired one of T.I.'s Schottky engineers this year, and T. I. thinks that National and Fairchild might use the same process. It was left up to DEC to see the other companies to second source the Schottky line and to watch for the type of process used. Apparently there are few processes in the market these days and most of them unstable, according to T. I.

I have all of T. I. Schottky plans of devices, deliveries, and design goals. Prices will follow in a week or so. As I gathered it, it looks like we are the first major company already committed for a whole processor to the Schottky. However, since business has been picked up considerably by T. I. in TTL products the last couple of months, we were advised to start placing quantity delivery schedule for the devices used in the 11/40.

4. T. I. is running tests now on the Intel 1103 and found some worst case noise patterns, and some parasitic leakage problems noticeable in some patterns.

5. They are using plastic for their MOS devices as well as ceramic. According to T. I., they found a new plastic compound which has a low permability to sodium, excellent thermal expansion matching, and high moisture resistance.

6. 8 bit processor is one of other MOS products. T. I. is building now on one chip. The one chip they are shipping now is a 16 instruction 8 bit processor with 10 usec fetch-execute time. It uses 4 states for timing with 3 clocks per state. Some of the basic instructions are move, arithmetic operations, jump, etc. The size of the chip is 220 mils on sides with 24 pins.

7. On the Bipolar TTL memory area, T. I. is going into the Tri-State business on some of these products. As far as the fusible ROM area, T. I. does not think it is a safe process and they don't have enough data on it yet. However, they think Intersil's technique of making a connection, is the way to go, but they still don't recommend using it in production.

CONCLUSIONS

Overall, my visit to T. I was very informative, educational, and very enjoyable. All of the people there were very cooperative.

digital INTEROFFICE MEMORANDUM

TO: Dick Best

DATE: January 14, 1972

cc: Nick Mazzarese
John Clarke

FROM: Charles Davis C.T.D.

DEPT: Administration

SUBJ: TRIP SCHEDULE, CONTACTS AND DISCUSSION TOPICS

Two trips have already been completed. Gerry Surrette and I visited Mostek (Worcester, Mass.) on 30 December 1971. We talked with the Chief Engineer and toured the plant. In this plant they only process silicon. Design, masking, packaging and assembly are elsewhere. On 12 January 1972 we visited General Instruments (Hicksville, Long Island). The Chief Engineer and several of the product managers talked with us and showed us through the plant. They have a complete facility there but do most of their packaging in Taiwan. Drafts of trip reports are in preparation, but will not be distributed until mid February so information and comparisons can be uniformly presented.

I introduce my purpose to each vendor as a "blue sky" search for where state-of-the-art in MOS LSI is. If he shows capability of handling a complex project, such as ours, I ask him about speed. Invariably he has a few desk-calculator projects and feels these are "computers". The 8 group has prepared two "benchmark" programs which I have written up (see appendix). These are intended to evaluate comparative times and force computer organization and semiconductor technology toward higher speed. A discussion of development and production costs then will give guidance on present feasibility of a MOS LSI computer.

I fly to San Francisco on Sunday 16 Jan. and return Saturday 22 Jan. Five vendor visits have been arranged:

Day	Company	Contact; others scheduled for talk
Monday	National	Jon Stemples; design mgr., custom ckts., QC and TTL. Will also talk about UART
Tuesday	Fairchild	Elvert Moore; MOS then isoplanar design, marketing, and managers of MOS and bipolar.
Wednesday	AMI	I have been assured all arrangements are complete but no contact name is available yet. Will talk about UART.
Thursday	Signetics	Elvin French; MOS bipolar. Signetics has limited interest in custom MOS.
Friday	Intel	Stan Mazor; logic design, layout MOS technologies, general manager.

The week of 24 Jan., I take the maintenance section of PDP8 course.

I fly to Los Angeles on Sunday 30 and return from Dallas Friday evening 4 February. Five vendor visits have been arranged.

Day	Company	Location	Contact; others scheduled for Talk
Monday	Western Digital	Newport Beach	Al Phillips; design, custom MOS, silicon gate, hybrid structures. Will also talk about UART
Tuesday	North American	Anaheim	Bill Wickes; quality control, design and fabrication facilities.
Wednesday	Motorola	Phoenix *	; polycell LSI, custom MOS, preferred technologies, ECL, bipolar LSI.
Thursday	T.I.	Houston *	; custom MOS, facilities. Great care will be taken to observe well and say little.
Friday	Mostek	Dallas	Dave West, Mr. Cash; design techniques, ion implantation consolidation of facilities

* name of contact hasn't yet been established but will be before 26 Jan.

Although bipolar investigation is subordinated to a thorough MOS study, any leads toward a LSI bipolar machine will be collected. Where both technologies are practiced in one plant, time for bipolar discussion has been requested after MOS.

Reports will be finalized and discussion meeting called for late in the week of 7 February. At that time we should be able to estimate the speed of a 1972 LSI MOS computer and calculate its cost.

The next phase of the program (to be pursued if speed and cost are attractive) involves selecting a small number of vendors and obtaining non disclosure documents.

Updated 8 drawings will be given them along with assistance in design and organization of an LSI MOS computer. The design and prototype phase could then follow.

D. Bell

digital

Gentlemen:

Digital Equipment Corporation is attempting to evaluate the speed and organization of state-of-the-art MOS - LSI for possible computer applications. We request you to evaluate your most advanced MOS technology on our two "benchmark" programs for 8, 12 and 16 bit processors.

Time States	Program #1
R	Reg B + 1 ⟶ Reg A
S	Data ⟶ Reg C
V	Ø ⟶ Reg D
	$\overline{\text{Reg D}}$ ⟶ Reg D
	Reg D + 1 ⟶ Reg D
	Shift Reg D Left Twice
Z	Reg A ⟶ Reg B

Time States	Program #2
R	Reg B + 1 ⟶ Reg A
S	Data ⟶ Reg C
T	Reg B + Reg D ⟶ Reg B
W	Data ⟶ Reg C
	Reg C ⟶ Reg B
	Data + 1 ⟶ Reg C
X	Reg C ⟶ Data
Y	Reg A + 1 ⟶ Reg A
Z	Reg A ⟶ Reg B

Please calculate time for each time state and total time for each program using your "optimum" organization for 8, 12 and 16 bit processors. For this analysis at least 4 general purpose registers are required. "Data" is read from/to a 4096 word RAM to be included as part of the system; time in previous state may be used for selecting and enabling the memory.

Time States \ Bits	8	12	16
R			
S			
T			
V			
W			
X			
Y			
Z			
Program 1			
Program 2			
# of chips			
cost			

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digital INTEROFFICE MEMORANDUM

TO: Dick Best

DATE: January 24, 1972

FROM: Charles Davis

DEPT: Administration

SUBJ: INTERIM REPORT ON SURVEY OF SEMICONDUCTOR COMPANIES TO DO LSI FOR CPU'S.

At the half way point of plant visits, AMI stands out as having exceptional fabrication capability, outstanding quality control and considerable knowledge of computer requirements. They state that they are now working on a CPU for "another customer" under a non-exclusive agreement. This is scheduled for first delivery in August. The engineer claims that the N-channel circuits involved can perform each operation of our "benchmark program" in 400 n sec for 8 and 12 bit machines (about 10 percent longer for 16 bits, due to greater propagation delays). Since some operations can be done simultaneously our program #1 would take 2.0u sec and program #2, about 3.2 u sec (10 percent more for 16 bits). These numbers are based on the existing design for a multi chip machine. If DEC expresses sufficient interest a CPU design engineer will visit us to discuss why he believes his approach can give us these speeds. They do not want to reveal more without a reciprocal expression of DEC's intentions.

AMI figures 16 weeks from an acceptable MOS logic diagram through fabrication of first parts. They have a 2 week correction cycle and can produce several thousand a week within 6 weeks thereafter. They are the first company to announce a commercial N-channel LSI device (1K RAM).

They shipped 100 of their UART 3 days after receipt of our P.O. M60798 (August 1971). They stock 200, but could ship "as many as we might want" in 2 weeks by packaging inventoried chips. The DEC part will be ready in March. A synchronous receiver/transmitter and a data scrambler are now in development. They would like input from DEC on desired I/O characteristics for a 4K RAM scheduled for late 1972.

Intel calculates times for a parallel processor of 1.5 to 2.0 u sec for program #1 depending on the number of bits and 2.0 to 3.0 u sec for program #2. These numbers are not based on any hardware approaching our speed requirements. In development they believe that a 2 month period is required for interactions with DEC engineers, 4 months for layout with 3 iterations (considered probable) and 3 months to produce parts. Their N-channel line is producing devices now. They would like to develop a CPU for us and probably could.

Intel claims to start 5700 wafers per week and to have a capability, with existing equipment, twice as great. They had a seven fold growth in facilities in 1971 and shipments have grown from $370K in 1969 to $10M in 1971. The rate of growth still leaves a laboratory atmosphere and appearance is their plants.

National is proud of being an aggressive, profitable semiconductor house. They promised to look over our "Benchmark programs" and advise me. They have had considerable experience with serial MOS LSI processors and have a report called GPC/P (coming to me soon) which describes a processor consisting of 1 - CROM, 4 ALU and 10 bipolar (buffers) with a 4 u sec addition. Parts will be available this summer and should be inexpensive. They have a paper study on the PDP8 which shows how it is possible to reduce the number of chips in the processor from 66 to 56 using National tristate parts (some of these devices have not yet been announced). They have an outstanding high volume semiconductor production capability with good quality control. They have C-MOS although no specifically N-channel or ion implant but are working on both.

National feels that all MOS memories need bipolar input/output buffers so going from a 2K to a 4K RAM does not reduce total chip number by a large factor. As a result they are not now planning a 4K RAM. They have 4 types of UART in the works; the DEC part is due out in March.

General Instruments has probably more (14) different calculator chip contracts than any other vendor I have visited. They have a well organized production facility and are ready to describe a surprising number of the details of their operation. They are working on N-channel and ion implant technologies. I only talked generalities about processors with them.

Signetics has a small MOS operation with room for the several 10's of million dollar expansion budgeted this year. A 2K P-channel RAM is expected out in April and a 1K N-channel dynamic RAM with access time less than 100 n sec and a 1K "TTL compatible" (+5V power supply) this summer. They claim one of the longest histories of MOS processing but admit that they haven't been terribly effective until now. Their policy has been not to take custom MOS work and they feel that the real growth in MOS is in RAM's. I was not able to speak to their logic designer because he was "getting ready for a trip to Europe". The bipolar facility is bursting at the seams to put silicon through the line. They have a new corporate QA structure which promises to improve process control. I was extremely impressed by their packaging techniques.

Fairchild MOS is just moving into new quarters. Their quality control operation has excellent equipment for stress testing devices and analyzing why they failed. Design facilities are comparable with those of smaller houses that I visited. They will look over the "benchmark programs" to determine what speeds they can achieve.

The Fairchild isoplanar process is very credible and offers much denser structures with less capacitance and faster speeds than present structures. Fairchild is building their 1K bipolar RAM in isoplanar ECL and will build a TTL interface on the perimeter for TTL users.

Four-Phase Systems is reported to be building an LSI MOS computer probably in conjunction with Standard Microsystems Corporation (the two companies are very closely related) or Mostek.

There are several very impressive semiconductor houses which I omitted in my visiting plans. These are: Intersil (Cupertino, California), Nortek (chip fabrication house in Santa Clara, California), MOS Technology (Valley Forge, Pennsylvania), Hughes (Newport Beach, California) and MIL (Canada).

Conclusions on MOS LSI:

We must look at the AMI program because they will build a fast LSI MOS processor soon and inexpensively.

Intel with an excellent design staff and precision processing capability can exceed any industry goal, for a price and given enough time.

National offers an excellent design capability but might be difficult to orient to exactly our needs.

General Instruments sees the forthcoming squeeze in the calculator market and is very anxious to diversify.

Products are available today which can reduce parts count in a bipolar computer.

LSI bipolar products will not be available until considerable facility is gained in use of isoplanar (or V-ate) process. This will be in 1974 and will probably be ECL.

cc: John Clarke
Henry Crouse
Tom Kennedy
Bill Long
Nick Mazzarese
Gerry Surrette
Mike Tomasic
Remo Vogelsang
Roger Dow

digital INTEROFFICE MEMORANDUM

TO: Dick Best

DATE: February 7, 1972

FROM: Charles Davis C.P.

DEPT:

SUBJ: PRELIMINARY REPORT ON SURVEY OF SEMICONDUCTOR COMPANIES

I have visited the originally scheduled plants which (except for IBM) include the most powerful design and strongest fabrication groups (85% of U.S. volume). Companies of the second trip were particularly solicitous of our business. The basic conclusions of the first report remain unchanged, but the necessity of a bipolar interface with computer bus must be re-emphasized.

On the latest trip are two extremely well organized computer aided design operations (Texas Instruments and Western Digital) and one with a well deserved reputation for innovative design (Mostek). It has been possible to put together a reasonable list of sales volumes of the MOS industry (See Page 5).

Texas Instruments has the second largest MOS house and has quintupled its sales from 1970 to 1971 (a rate of growth only tied by Motorola and the smallest houses). TI's will be the largest operation in 1972; this statement was volunteered by TI, Motorola and Mostek. A tour of the Houston facility reveals a huge design group with tremendous computation and layout facilities. Large computers are IBM 360, 370 series and small ones all of TI design (the latter are used throughout their device testing operation). There is a machine for assembling a layout on a CRT, using a light pen and incorporating some very comprehensive spacing rules. This permits rapid transfer to plotting table or transmission to Dallas for automatic pattern generation. The "front end" including furnace, etch and metalization is in Dallas; this operation is considered proprietary and few in the Houston operation have seen it. The pilot front end in Houston has few laminar flow hoods; Dallas apparently has many. Houston has two automatic computer controlled thermocompression bonders and a room full of manual ones. They also control considerable "off shore" facilities. Testing is automatic; the computers are unlabelled but obviously T.I. made. They affirm that they really goofed on the UART (they call it 6010). Their story is that they made units well in pilot operation but in production "one node required more capacitance to make the device work". With this corrected they claim good yield. There was no explanation of why production could not be modified to make the original design work or why such a long corrective cycle is consistent with new device design capability. They promised 300 pieces

by the end of the month and 1000 pieces per month starting in April. They gave slightly slower (500 nsec) time cycles for N-channel than AMI, claim no one will have reliable N-channel this year and require more time cycles (7 and 9) for the bench mark programs than AMI. They have some of the finest equipment and skillful engineers and next year their volume should exceed even AMI's but their performance record is poor and they are most assuredly a competitor of ours.

Mostek has the reputation for innovation. Its leadership and engineers are largely from Texas Instruments. Despite functioning in three sequential and geographically separate plants, they have met tough schedules. They do not have N-channel, but are working toward it. Their design and layout are manual and although they claim computer (actually a PDP11/15) aided design, this facility really just checks what the engineers have already done. Their analysis and understanding of individual transistor design and function are ahead of anything else I have seen; their techniques rely heavily on tailoring of thresholds with ion implantation to optimize performance. They now have 22,000 square feet in Carrolton and are moving across the street in April into 120,000 square feet. I expect that this move will be accompanied by acquisition of a number of highly skilled engineers from competition. Ken Davis' answers to the benchmark were similar to T.I.'s but they are anxious to think the problem over and pay us a visit. Although small, they are and will remain a significant element in MOS. They should be able to turn out excellent product on reasonable schedule despite the greater emphasis on circuit element than on automatic circuit layout.

Narmco (North American) is one of the largest MOS manufacturers, but most of its business is with Sharp calculator. Their technology is P-channel metal gate, with or without nitride. Narmco holds several of the basic nitride patents and has excellent ability to use the process. They don't believe N-channel will be used in real production this year and that their pseudo self aligned P-channel nitride offers the same speed. Their clock rate is restricted to no more than 500 to 750 KHZ and 5 clock pulses are required for an add. They have a two bus processor similar to Intel's, except faster.

They suggested that DEC should be more heavily in the "point-of-sale" and data communications areas. These markets do indeed appear to need a technologically strong, yet imaginative competitor (such as DEC). Such units can use the small serial processors which are now inventory items with all large manufacturers.

Narmco has a very powerful silicon on sapphire operation. This could provide an attractive alternative to ROMS. Present capability gives 20 nsec access and 40 nsec cycle time on a 40 x 128 diode array (147 x 169 mil chip in 42 pin package). These are custom encoded by laser and sell now for $64. each in small quantities. They predict 0.1¢ per bit in less than two years and I believe it. Capacitance on each line is less than 3 pf but decoding is external.

Motorola admits to being late making its start in MOS, but itscommitment has indeed been heavy. They have a computer aided design that stresses standard cells but is capable of modifying them greatly. Their hope is that it will be easily enough defined that customers can do their own design on facilities scattered across the country. P-channel silicon gate is a production technique; N-channel metal and silicon gate should both be ready for test runs this summer but they would prefer to wait until January 1973 for custom work. They expect 4 MHZ clock rates on N and 2 MHZ on P-channel. Using P-channel and their two phase system they calculate for 8 bits, 3 usec on our program 1 and 4 usec on our program 2 (add 10% for 12 bits and 20% for 16 bits).

Motorola production is in old space and considerable work is being done to revamp it. Cleanliness does not compare with most companies on the San Francisco peninsula. Product is moving and completion of the renovation can be expected this year.

Motorola lays out gates on a slice and custom wires them to give bipolar LSI. Their present capability is a 133 x 142 mil TTL chip with 112 gates: 98 are 4 input NAND and 14 are 8 input NAND. They are available for $45 each in 1K and $28 each in 10K. Late in 1972 they plan a 160 x 160 mil schottky TTL chip with 210 gates and an effective speed of 10 nsec (at $90.) The first quarter of 1973 they plan a 126 x 126 TRL array of 400 gates at 35-$40. The mid 1973 plan is for 1000 gate arrays.

Western Digital is by far the smallest operation that I visited. However they have computer aided design equipment comparable to the most versatile of Texas Instruments and construct some excellent test equipment (actually one of their products). Testers are built around PDP11/15's (and they have already bought several). They sense signals right at the probe using the same electronics as in a final tester and claim to be able to screen out almost all bad chips at probe. The process facility is as clean and well set up as any I have seen, but very little silicon is actually being processed. UART's already shipped have exhibited higher speed than competitive devices. If Western Digital can survive cash flow problems of start up with their $5.5 million, they will become a significant element in MOS.

CONCLUSION ON MOS LSI

AMI still is the choice to build a DEC compatible processor. They have their own internal "second source" or Mostek could be used.

Intel, Mostek and Western Digital have exceptional capability and could also develop such systems as we desire (probably less rapidly and more expensively).

Texas Instruments is capable of developing any system of this type but our experience indicates: possibilities of long delay due to technical problems, internal interactions between MOS and computer groups that would cause our work to be available to our TI competitor in some fashion regardless of previous legal arrangements.

Silicon on sapphire is available today for ROM type memories. It should be very competitive in two years.

Custom bipolar LSI is available today at costs of 15¢ per gate. This kind of work is best justified by speed requirements and there, ECL is the necessary technology (reference: Fairchild and Motorola). Whole processor units on a bipolar chip are not yet in sight.

cc: John Clarke
Henry Crouse
Tom Kennedy
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Nick Mazzarese
Gerry Surrette
Mike Tomasic
Remo Vogelsang
Roger Dow
Don White
Russ Doane

MARKET SHARE

	1970 sales	1971 sales
American Microsystems Inc. (AMI)	$28.5M	$26M
North American (Narmco)	9M	20M
General Instruments (GI)	6M	4M
Texas Instruments (TI)	5M	24M
National	4M	6M
Intel	4M	10M
Electronic Arrays	3.5M	3M
Fairchild	3.5M	3M
Hughes	3.0M	2M
Motorola	1.5M	8M
RCA	1.5M	6M
Philco Ford	1.5M	--
Mostek	1.0M	4M
Signetics	1.0M	1M
Western Digital	----	.2M
Others *	8.0M	15M
	81.0M	122M

1970 sales estimate based on a report by Blyth and Co. and on article in Electronic News of September 1970.

1971 sales are based on relative growth rates and size estimates of companies visited.

* Includes: IBM, Siliconix, Intersil, Advanced Memory Systems, Nortek and MOS Technology

digital INTEROFFICE MEMORANDUM

TO: Dick Best
Nick Mazzarese

DATE: March 2, 1972

FROM: Charles Davis C.D.

DEPT: Administration

SUBJ: REVIEW OF ACCOMPLISHMENTS AND RECOMMENDATIONS FOR FUTURE ACTION

During the past three months I have visited fourteen vendor plants to ascertain their ability to supply custom LSI MOS and complex custom bipolar. The first two reports were preliminary with an objective of recommending contacts/vendors. The third was a summary of MOS. Subsequent to this last report I visited Microsystems International Limited (MIL) in Canada. Theypresent great technical competence and a powerful contact for Canadian business. I also took the PDP8/E maintenance course during this period.

The first vendor reports showed AMI as the most competent production plant visited. They also have great design capability and considerable knowledge of computer processors. It has been very difficult to get their lead logic designer to visit due to his commitment to another project. MIL has similar semiconductor technologies, an equally strong design team, less production capability, but ready availability for discussion and they offer particular assistance in computer sales in Canada (and UK).

I have partitioned M7821 interface module into two identical custom signal processors, two quad bus drivers (as presently being used) and a single quad gate. The custom signal processors have been discussed with several vendors. Estimates coming back seem to offer direct economic as well as configurational advantages.

MIL offers a new design of a bus switch which promises additional simplification of interface modules.

Knowledge derived from visits has enabled me to help our Quality Control people in selection of a MOS tester.

During the next period I offer my assistance in:

1. final selection of a PDP8 LSI MOS vendor and liaison with the designer;

2. specifying parameters and preparing a purchase specification for the new M7821 chip;

3. selecting a vendor and second source for the M7821 chip;

4. obtaining other parts for interface module simplification;

5. investigating smaller manufacturers who seem to have unique technical ability eg. Nitron claims an ultra stable N-channel process and an exceptionally compact double gate scheme, Intersil has the reputation for rapid inexpensive, reliable design (relative simple parts), Inselek has active as well as passive silicon-on-sapphire (speeds are enormous but price and availability are unknown);

6. assisting Quality Control on selection of a MOS tester;

7. surveying the inexpensive, slow (serial) MOS processor field to find what is available, who is getting units and what they are being used for, in particular, what control functions can they manage. These units could provide us a new market or compete for our simpler applications on a price basis.

digital INTEROFFICE MEMORANDUM

Boot

TO: LSI Committee

DATE: February 7, 1973

FROM: Henry Crouse

DEPT: Purchasing

EXT :

SUBJ: CALCULATORS

I learned the following from a telephone conversation with Al Phillips, who was involved with North American Electric and Sharp for their first calculator:

1. A vendor team from Sharp visited major semiconductor houses during the late summer and fall of 1968.

2. North American signed a components contract for $250,000 in late 1968.

3. Production was initiated in the summer of 1969.

4. Large volume production began at the end of 1969 into 1970. The first world-wide calculator was produced - No. QT8D.

The calculator was comprised of five chips - four large and one small. Al Phillips left Sylvania for North American in 1960. At that time all calculators were IC's or discrete components. All the suppliers that Sharp visited said it would take 8-10 chips. North American claimed they could do it in four chips by May, 1968. The first sample parts were available December, 1968. In effect, it took one year - April, 1968, until April, 1969 - from the development period to the initiation of the product. Al now claims that the contract design cycle is very short and the calculator design chips are readily available. He concludes that a computer chip should take less than one year.

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