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To: David Laws, Director, Semiconductor Special Interest Group, Computer History Museum
Cc: Ms. Leslie Berlin

Dear Dave,

I don't know if you have heard, but Dick Anderson and I found application notes in the Stanford archives referenced by Ms. Leslie Berlin Ref (1) which confirmed the dates which I had been using when discussing Micrologic.

As I have said before, the paper published by the I. R. E. as a reprint of the February 1960 Solid-State Circuits Conference paper, "Solid-State Micrologic Elements", by myself, Isy Haas and Jay Last, was that written by me as a "placeholder". Charlie Plough in manufacturing had not yet produced a single "F" element, Set-Reset Flip-Flop. Fairchild had decided, in keeping with its standard policy on new products, this part would not be announced unless parts were made in manufacturing. Absent such event, the choice was to withdraw the paper, perhaps substituting one describing a DCTL transistor consisting of a Micrologic transistor geometry with a series base resistor, as proposed by Vic Grinich. When manufacturing actually produced the "F." elements, I was authorized to give the paper, which I did, after taking an aspirin for courage facing Doug Engelbarth and Jim Early and the other speakers and a large room full of my peers from years past.

At the time we thought the I. R. E. would publish the actual paper presented rather than the placeholder. While the I.R.E: published the "placeholder", Fairchild published the actual paper as an application note. Thus a copy of the actual paper presented, dated February, 1960 is contained in the Stanford archives, Ref. (2). Also included in these archives are papers by myself, other members of the Micrologic section (Dick Anderson, Don Farina, Dick Crippen) and other members of Fairchild's professional staff notably Jim Nall. A list of the Micrologic application notes included in this collection is attached. Our thanks to Mr. Bruce Deal for his thoughtfulness in placing these materials in the Archives.

Of particular interest is the reprint of Fairchild's presentation to the Bumblebee Conference at Johns Hopkins in June of 1960. Bumblebee was a major Navy air to air missile program... Fairchild Camera who was a Bumblebee contractor asked us to present a paper on Micrologic. The paper included an update on 125° C. operating life test results. These then published materials validate what I had been saying.

It is important to note further that, as previously stated, "F." elements made using chemical isolation failed quickly on 125° C. operating life test. Thereafter, a thermal shock test was

instituted (125° C. to -55° C.) to ensure that such devices could not enter operating life test and contaminate the results. For the same reason, no chemically isolated Micrologic device was ever given to a customer (unless by someone in Dr. Last' organization).

The patent application filed by Dr. Last covering a chemically isolated integrated circuit process did not describe the material used to support the semiconductor islands. The configuration patented was for interconnected transistors with no resistors. Ref.(4)

As has been stated before, the successful use of epitaxial isolation with sub-epi diffusion as achieved by Phil Ferguson on the Fairchild Pilot line using designs by Don Farina opened the manufacturing floodgates. It is these devices, manufactured by Fairchild, General Micro-electronics and Philco that, for example, made it to the moon several times in the logic sections of the Command Module and LEM (Lunar Excursion Module) computers without a failure. It is hard to imagine the scope and significance of that achievement at that time, a credit to MIT Instrumentation Lab and A-C Spark Plug Division of General Motors, El Segundo, developers and builders of those computers

We should all be grateful to Ms. Leslie Berlin for tipping us off to the archive containing these important historical documents and for her assistance in allowing us to see them.

We are all aware of the "success has many fathers" syndrome. All the more reason to gather as much information as we can from those who actually participated while their memories are still working. By the same token, we should not worry ourselves when facts as they are uncovered conflict with some people's memories. We should remind ourselves that differences of a few months 50 years ago while incredibly important then, and now with respect to context and historical accuracy, can easily be lost in that sea of memories we each have of our own activities in that period, and all our individual related activities in the years since. Many of those who produced those first hundreds of diffused isolation parts used in the test-to-failure and life tests and were analyzed to determine causes of failure are no longer with us. The time is long overdue to extend to these men and women the recognition they so richly deserve. They were a vital part of the success of Fairchild’s monolithic integrated circuit program, and of the advent of Silicon Valley.

List of Some Pertinent Fairchild Semiconductor Technical Publications included in the Deal Collection:

TP-7 Solid State Micrologic Elements, Solid State Circuits Conference, Feb 1960, Norman, Last, Haas

TP-10 Status Report on Micrologic Elements, 51st Bumblebee Guidance Conference, June 1960, Norman

TP-11 Application of Micrologic Elements, National Electronics, Oct. 1960, Farina, Nall, Anderson

TP-18 Testing of Micrologic Elements, Western Joint Computer Conference, May 1961, Norman, Anderson

TP-22 Micrologic System Design Considerations, National Conference on Military Electronics, June 1962, Anderson, Crippen, Fok

Ref: (1) Berlin, Leslie, *The Man Behind The Microchip*, Oxford University Press, 2005
(2) Deal, Bruce E., *Papers 1958-1987, Silicon Valley Archives, Call number M1051*, Stanford University Archives
(3) Saxena, Arjun, *Invention of Integrated Circuits*, World Scientific Publishing, 2009
(4) Last, Jay, *Solid State Circuitry Having Discrete Regions of Semi-Conductor Material Isolated by an Insulating Material*, US Patent 3,158,788, filed 8/15/60, ibid.