RCA
ELECTRONIC
301

DATA PROCESSING SYSTEM

PROGRAMMERS' REFERENCE MANUAL

RADIO CORPORATION OF AMERICA

Electronic Data Processing,
RCA - Cherry Hill
Camden 8, N. J.

93-16-000
November, 1966

The information contained herein is subject to change without notice. Revisions may be issued to advise of such changes and/or additions.

Reissued: June, 1964

This manual has been reprinted to include all revisions through November, 1966.

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THE RCA 301 SYSTEM

I — GENERAL DESCRIPTION

INTRODUCTION

The RCA 301 Electronic Data Processing System is a general purpose, stored program, digital processor employing solid-state electronic circuitry. Highly flexible RCA 301 Systems are integrated from a diversified array of input/output devices, a range of memory sizes, and other special features. Each System is tailored to meet the data processing requirements of a specific organization. While each RCA 301 System is complete within itself, a high degree of compatibility has been attained with the medium-scale RCA 501, the medium-scale RCA Realcom 3301, and the large-scale RCA 601.

System efficiency is enhanced by:

- Rapid memory access time
- Character addressability providing completely variable data organization
- Decimally addressed memory
- Built-in and programmed accuracy controls
- Machine code covering full range of numerics, alphabetics, and special symbols
- Automatic and programmed storage in High-Speed Memory of the contents of various Program Control Registers
- Direct and Indirect Addressing
- A powerful programming instruction repertoire including the following:
  - A Translate by Table instruction permitting efficient internal processing of various code structures
  - Locate Symbol instructions permitting an internal search within High-Speed Memory for any character designated
  - Transfer instructions permitting transfer of data to left or right within High-Speed Memory
  - Arithmetic instructions permitting Logical "OR", Logical "AND" and Exclusive "OR"
  - A Repeat instruction permitting the next repeatable instruction to be repeated a specified number of times
  - Automatic programming aids include RCA 301 COBOL, Assembly System, FORTRAN, and a Scientific Interpreter. An extensive library of service and maintenance routines is also available.

The System processes information prepared by a variety of input media for distribution to the appropriate output. The complete compatibility of System elements provides for ease of expansion at a later date, which is part of the System philosophy.

SYSTEM ELEMENTS DESCRIPTION

The RCA 301 Computer comprises a Processor and appropriate Input/Output Control Modules. The latter operate the peripheral devices connected in the system. The Processor is a general purpose, stored program, digital machine which includes the following sub-units: High-Speed Memory, Program Control, Console Panel, and Power Supply. The Simultaneous Mode Control may be included in the system to provide concurrent operation of two input/output devices, or an input/output instruction with a compute instruction.

The **High-Speed Memory** is a random access, magnetic core device which provides storage and work area for programs and data. The memory capacity is 10,000 (Model 303), 20,000 (Models 304 and 354), or 40,000 (Models 305 and 355) alphanumeric characters. Each location is decimally addressable and can store one of the RCA 301 characters. The RCA 301 code includes all the letters of the alphabet, the ten decimal digits, and control and special symbols. (Refer to 301 Code Chart, Appendix A.) The memory cycle time to address, bring into register, and regenerate a diad in its original memory location is 7 microseconds.

The **Program Control** executes the instructions of the program stored in the High-Speed Memory and performs the automatic accuracy checks. The classes of instructions are: Data Handling, Arithmetic, Decision and Control, and Input/Output. Both direct and indirect addressing can be employed.

The **Console Panel** provides for complete monitoring of operation of the Processor. Adequate indicators and controls are provided on the panel to initiate normal computer operation and to facilitate program check-out and maintenance.

The **Power Supply** distributes power to the Processor and to certain Peripheral Equipments which require d-c or regulated a-c power. Other Peripheral Equipments, not requiring d-c or regulated a-c, are supplied from the power mains individually.

The **Simultaneous Mode Control** pemits the operation of one input/output device simultaneously with another operation being performed by the Computer. This other operation being performed by the Computer can be a second input/output instruction or a compute instruction.

The **Record File Mode Control** provides an additional degree of simultaneity so that reading from or writing to one of four Data Record Files can be time-shared with other operations.

The **Input/Output Control Modules** control the peripheral equipment, generally one for each device used in a system. The modules are installed only when their associated input/output devices, described in succeeding paragraphs of this section, are added to the system.

The **Card Reader, Model 323,** reads information punched in 80-column cards for transfer to the Processor. Hollerith card code may be automatically translated to RCA 301 code. It is possible to bypass automatic translation and read cards binarily. Cards are read at rates up to 600 cards per minute. Information may be edited and rearranged under program control.

The **Card Reader, Model 324,** reads information punched in 80-column cards for transfer to the Processor. Automatic translation between Hollerith card code and 301 code is provided under program control. Cards may be read binarily under program control. Reading is performed at a rate of up to 900 cards per minute.

The **Card Reader, Model 329,** reads information punched in 80-column cards for transfer to the Processor. Automatic translation between Hollerith card code and 301 code is provided under program control. Cards may be read binarily under program control. Reading is performed at a rate of up to 1500 cards per minute.

The **Card-Reader-Punch, Model 330,** consists of an 80-column card reader and card punch in the same enclosure. Reading is performed at rates up to 800 cards per minute and punching at rates up to 250 cards per minute. Automatic translation between Hollerith card code and 301 code is provided. Under program control, automatic translation may be by-passed to permit reading or punching binary coded cards. Card reading, punching and editing are performed under complete control of the stored program. Concurrent reading and punching may be performed when the Simultaneous Mode Control is included in the system.

Paper tape input and output is provided by three optional paper tape devices. The **Paper Tape Reader and Punch, Model 321,** is a single unit which permits on-line reading from and punching either 5 or 7-channel paper tape at the rate of 100 characters per second. The **Paper Tape Reader, Model 322,** is a single unit which permits on-line reading from 5, 6, or 7-channel, odd or even parity, paper tape at either 500 or 1000 characters per second. The **Paper Tape Punch, Model 331,** is a single unit which permits punching 5 or 7-channel paper tape at 100 characters per second.

The **High-Speed Paper Tape Punch, Model 332,** is a single unit which permits punching of 7-channel paper tape at 300 characters per second.

Two models of the **On-Line Unbuffered Printer** are available; one printing 120 characters per line (Model 333) and the other printing 160 characters per line (Model 335). The 120-characters per line model has a printing rate up to approximately 1000 lines per minute during synchronous printing, with the ability to print 47 selected characters, and up to approximately 800 lines per minute, with the ability to print 64 characters. The 160-character per line model has a printing rate up to approximately 1075 lines per minute, with the ability to print from 47 selected characters, and up to approximately 835 lines per minute, with the ability to print 64 characters. Two 120-character

or two 160-character printers can be operated simultaneously in the system. Paper can be advanced at the rate of 150 lines a second on both models, independently of normal data processing activity. The printer operation, variations in format, and complete editing are under the control of the stored program.

Two models of the **On-Line Buffered Printer** are available, one printing 120 characters per line and the other printing 160 characters per line. Buffer storage capacity of the 120-character per line model is 184 characters (120-character data line plus 64-character print table); buffer storage capacity of the 160-character per line model is 224 characters (160-character data line plus 64-character table). Scanning references the data line and the print table in the buffer. The Processor mode is free on completion of transfer to the buffer. Data transfer is by diad, at the rate of 14 microseconds per diad. Printing and paper advance are accomplished off-line. Rated speeds for printing and paper advance are the same as specified for the unbuffered models.

The **Monitor Printer, Model 338,** is used for listing intermediate or final totals of a computer program, summary reports or for program testing. The output rate is up to 10 characters per second. All of the 301 characters may be printed.

The **Interrogating Typewriter, Model 328,** is an input/output device, which allows inquiry messages to be entered into the system via a keyboard, and data from the computer to be printed at a rate of up to 10 characters per second. All of the 301 characters are used. The operation is performed under control of the stored program.

The **MICR Sorter/Reader** sorts magnetically encoded documents under control of the stored program. Data is also verified and accumulated for further processing by the Computer. Six-inch documents can be read at rates up to 1560 per minute. A supplementary programmers' reference manual (#93-16-001) is available for use in programming this equipment.

The **Data Record File, Model 361,** provides mass storage of over 4.6 million characters per file. Each file contains 128 magnetic records. From one to 9000 characters may be transferred between High-Speed Memory and the Data Record File, with one instruction, at a transfer rate of 2500 characters per second. As many as six Data Record Files can be used in the system with as many as three of the files being written to or read from simultaneously.

The **Data Disc File, Model 363,** provides rapid random access storage in modules of 22 million alphanumeric characters. Each side of a magnetic disc is divided into 1152 data tracks. The contents of a complete track (1600 characters) can be transferred between High-Speed Memory and the Data Disc File, with one instruction, at a transfer rate of 32,000 characters per second.

The **Hi-Data Tape Group, Model 381,** is composed of a cluster of up to six tape decks with a common set of controls, power supply, and switching circuits. Reading is performed in either the forward or reverse direction. The read/write rate is approximately 10,000 alphanumeric characters per second. Two Hi-Data Tape Groups may be utilized in a system for a total of 12 tape decks. In this case, two tape decks, one from each group, may be operating simultaneously.

The **Hi-Data Tape Group, Model 382,** is composed of a cluster of up to six tape decks with a common set of controls, power supply and switching circuits. Reading is performed in either the forward or reverse direction. The read/write rate is approximately 30,000 alphanumeric characters per second in the 382 Mode and 20,000 alphanumeric characters per second in the 381 Mode. **Two Hi-Data Tape Groups, Model 382,** may be utilized in a system for a total of 12 tape decks. In this case, two tape decks, one from each group, may be operating simultaneously. With a special control module and special features on each tape deck, two tape decks in the same group may be operating simultaneously.

33KC Magnetic Tape Stations are operated through either 33KC Tape Adapters or 33KC Dual Tape Channels. Reading is performed in either the forward or reverse direction. The read/write rate is approximately 33,333 alphanumeric characters per second. Up to 14 33KC Tape Stations may be operated in the system.

66KC Magnetic Tape Stations are operated through either 66KC Tape Adapters or 66KC Dual Tape Channels. Reading is performed in either the forward or reverse direction. The read/write rate is approximately 66,667 alphanumeric characters per second. Up to 14 66KC Tape Stations may be operated in the system.

The **Multiple Tape Lister, Model 340,** is an electro-mechanical printer available in two models. The first model has 6 separate paper feed units and the second has 12 separate paper feed units. The maximum printing rate is 2,000 lines per minute. Printing can take place on any one listing tape or a maximum of two listing tapes simultaneously.

The **Data Exchange Control, Model 377,** enables any two 301 Processors, each equipped with this control to communicate with each other. A second **Data Exchange Control** may be attached to a 301 Processor when it is necessary for this Processor to communicate with two other 301 Processors. Data may be transmitted in either direction but in only one direction at a time. The transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both Processors.

Communications equipment may be included in a system via the **Communications Mode Control, Model 378.** A supplementary programmers' reference manual (#93-16-006) is available for use in programming this equipment.

The **Videoscan Document Reader, Model 5820,** is a high-speed numeric optical character reader which will read documents of various sizes containing numeric data and/or four special symbols. The data is translated automatically for input to the Processor. The reading rate is either 750 documents per minute or 1500 documents per minute as determined by a manual switch setting. A supplementary programmers' reference manual (#93-16-004) is available for use in programming this equipment.

Two additional 301 Processor models are available. The memory capacity is 20,000 (Model 354) or 40,000 (Model 355) alphanumeric characters. In addition to the standard 301 System programming instructions, the enhanced logic of these processors provide high speed fixed point or floating point arithmetics with associated automatic address modification capabilities. A supplementary programmers' reference manual (#93-16-003) is available for use in programming this equipment.

Accuracy Control

Adequate accuracy checking techniques are used in the System to assure correct data processing. Correct parity is ascertained on read-in, during data flow in the Computer, and on write-outs. If a parity error occurs in one of the Computer modes (Normal, Simultaneous or Data Record File) the mode in which the error occurs is stopped immediately. The other modes complete their function.

Accuracy of information from the Card Reader and to the Card Punch is assured by use of two separate reading stations in the Card Reader, and a reading station following the punch unit in the Card Punch. When reading cards in the Translate Mode of operation, any non-RCA 301 Card Code combination (excluding Y/0) is detected, transferred into memory as an octal 57 (57_8), and both the Computer and Card Reader halt after the complete card image has been transferred to memory.

A parity check is made of paper tape characters (odd or even input parity) when transferred to the Computer, and an echo check is made of those characters punched onto paper tape.

With the unbuffered printer, a read error condition (RE) is indicated when the printer table character stored in the control module for scanning the print field has a parity error. With the buffered printer, RE is indicated for a parity error on transfer into the buffer.

With the unbuffered printer, a write error condition (WE) is indicated when either of the characters in the diad sent to the Printer Control module for comparison has a parity error. With the buffered printer, WE indicates detection of an off-line (printer accessing buffer) parity error. WE indication occurs on the next command to the printer.

A DDF occurs if the device is inoperable or a line advance or a page change command is received when a low paper supply exists.

The Data Record File possesses a lock-out feature to prevent writing on a "master" record. An accuracy check also warns of malfunctioning Block or Character Counter.

The Data Disc File checks if the positioner is in the correct track, and it has a bit counter to assure that the bit-serial to character-serial conversion is functioning properly. If a character with faulty parity is read, an octal 57 (57_8) will be stored in memory in place of the faulty character and an indicator will be set which can be sensed at the termination of the read instruction.

Magnetic Tape accuracy features include end of reel stops, both beginning of tape and end of tape warning, dual recording, write lockouts, correct parity of data read and read after write accuracy check.

A parity check is performed on data received from the Interrogating Typewriter. When operated as an output device, an echo check for correct parity is performed between the typewriter and the control module.

Application of Accuracy Checking Techniques

Program Control—The following controls are typical of conditions causing the computer to stop:

1. Incorrect parity in Memory Address Register.
2. Incorrect parity in Memory Register.
3. Incorrect parity in Operation Register.
4. Incorrect parity in N Register.
5. Incorrect parity in Repeat (N_R) Register.

Input/Output—The following are input/output conditions which may cause the Computer to stop:

1. Incorrect parity of data being transferred.
2. Input/Output device inoperable or not following command.
3. Record not on turntable of Data Record File.
4. Attempting to write to record or magnetic tape when lockout device applied.
5. Card equipment input hopper empty or output hopper full.
6. Non-RCA 301 card character read by the Card Reader, when in the Translate Mode.
7. Tape Station reading extra bits in interblock gap.
8. On-Line Printer paper supply low.

THE RCA 301 CODE

The RCA 301 System employs a binary code using seven binary digits, or bits to represent each RCA 301 character. Of the seven bits which make up each of the characters, the highest order bit (2^6) is the parity bit. The remaining six bits are the information bits, with a specific configuration of bits representing each RCA 301 character.

Bit Position	P	2^5	2^4	2^3	2^2	2^1	2^0
Bits	X	X	X	X	X	X	X

(X = 0 or 1)

For ease in presentation, the bit configurations of the RCA 301 Code are divided into four groups with the zone bits (2^5 and 2^4) designating the group, as follows:

RCA 301 GROUP CODE

	2^5	2^4	2^3	2^2	2^1	2^0
Group I	0	0	X	X	X	X
Group II	0	1	X	X	X	X
Group III	1	0	X	X	X	X
Group IV	1	1	X	X	X	X

The following table shows the bit configuration for each RCA 301 character. The parity bit (2^6) is not shown in this table but is inserted in each configuration to indicate an odd parity count.

RCA 301 CODE

Group I	Group II	Group III	Group IV	2^3	2^2	2^1	2^0
2^5 2^4	2^5 2^4	2^5 2^4	2^5 2^4				
0 0	0 1	1 0	1 1				
0	&	— (minus)	"	0	0	0	0
1	A	J	/	0	0	0	1
2	B	K	S	0	0	1	0
3	C	L	T	0	0	1	1
4	D	M	U	0	1	0	0
5	E	N	V	0	1	0	1
6	F	O	W	0	1	1	0
7	G	P	X	0	1	1	1
8	H	Q	Y	1	0	0	0
9	I	R	Z	1	0	0	1
(space)	+	EI	EB	1	0	1	0
#	. (period)	$	, (comma)	1	0	1	1
@	;	*	%	1	1	0	0
(	:	ED	● (ISS)	1	1	0	1
)	' (apostrophe)	EF	=	1	1	1	0

On 80 column cards, the groups are designated by the presence or absence of zone punches. Group I has no zone punch. Group II has a Y zone punch, Group III has an X zone punch, and Group IV has a 0 zone punch.

RCA 301 programs are written using alphanumeric characters. Memory Locations are addressed as follows:

Memory Locations	Addresses	Memory Locations	Addresses
0000 to 9999	0000 to 9999	24000 to 24999	M000 to M999
10000 to 10999	&000 to &999	25000 to 25999	N000 to N999
11000 to 11999	A000 to A999	26000 to 26999	O000 to O999
12000 to 12999	B000 to B999	27000 to 27999	P000 to P999
13000 to 13999	C000 to C999	28000 to 28999	Q000 to Q999
14000 to 14999	D000 to D999	29000 to 29999	R000 to R999
15000 to 15999	E000 to E999	30000 to 30999	"000 to "999
16000 to 16999	F000 to F999	31000 to 31999	/000 to /999
17000 to 17999	G000 to G999	32000 to 32999	S000 to S999
18000 to 18999	H000 to H999	33000 to 33999	T000 to T999
19000 to 19999	I000 to I999	34000 to 34999	U000 to U999
20000 to 20999	—000 to —999 (minus) (minus)	35000 to 35999	V000 to V999
		36000 to 36999	W000 to W999
21000 to 21999	J000 to J999	37000 to 37999	X000 to X999
22000 to 22999	K000 to K999	38000 to 38999	Y000 to Y999
23000 to 23999	L000 to L999	39000 to 39999	Z000 to Z999

ORGANIZATION OF DATA

Definitions

Bit: A bit is a single binary digit, having a value of either zero or one.

Character: An RCA 301 character consists of six information bits and one parity bit combined to represent a decimal digit, a letter of the alphabet, a punctuation or other special mark, or a control symbol.

Item: An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.). In many cases an item is preceded by a symbol to define the beginning of each item.

Record: A record consists of one or more related items with the amount of information in a record being completely variable.

Line: A line is composed of the characters that are to be printed on a single line on the On-Line Printer. One model of the On-Line Printer permits 120 characters to be printed per line. A second model permits 160 characters to be printed per line.

Block: On magnetic and paper tape a block is a group of at least three characters preceded and followed by a blank space called an "interlock gap."

On the Data Record File record a block is defined as the information contained in one cell. From one through 900 characters of information may be recorded in a cell. If the block is composed of less than 900 characters, the last character will be an EB symbol (End of Block). If the block is composed of 900 characters, the last character may or may not be an EB symbol. On the Data Disc File disc a block is defined as the information contained in 1 to 10 sectors. Each sector contains 160 characters.

File: A file consists of any number of related information records and may consist of only a part of a Data Record File record or Data Disc File disc, or several records or discs. On magnetic tape it may consist of several tapes or any part of one tape.

Organization of Data on Paper Tape

In the RCA 301 system, characters are represented on paper tape by combinations of holes punched in rows across the tape. A hole represents a zero bit in HSM; the absence of a hole represents a one bit in HSM (see Figure 4).

Organization of Data on a Data Record File Record

Bits are recorded as magnetic spots on the face of each Data Record File record. Characters are written and read out in bit-serial fashion, the seven bits of each character following each other in a spiral around the disc, as shown in Figure 2.

Each side of the record is divided into two bands; each band is composed of ten cells; each cell has the capacity to store 900 characters. The cells on a record are addressable individually or in groups of consecutive cells up to a total of 10.

Organization of Data on a Data Disc File Disc

Bits are recorded as magnetic spots on the face of each Data Disc File disc. Characters are written and read out in bit-serial fashion. The seven bits of each character following each other in concentric tracks around the discs as shown in Figure 1.

Each side of the disc is divided into nine zones of 128 tracks each. Each track contains 10 sectors of 160 characters each. The sectors are addressable individually or in groups of consecutive sectors up to a total of 10.

Organization of Data on Magnetic Tape

In an RCA 301 system, characters are recorded on magnetic tape as magnetic spots in rows across the tape. On Hi-Data Tape, a magnetized spot represents a zero bit; the absence of a spot represents a one bit. All characters

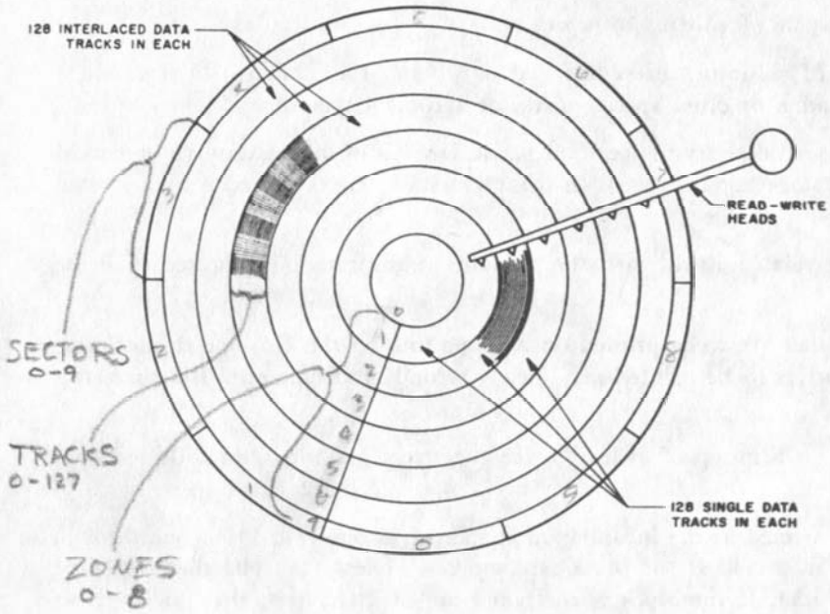


Figure 1—Recording on the Data Disc

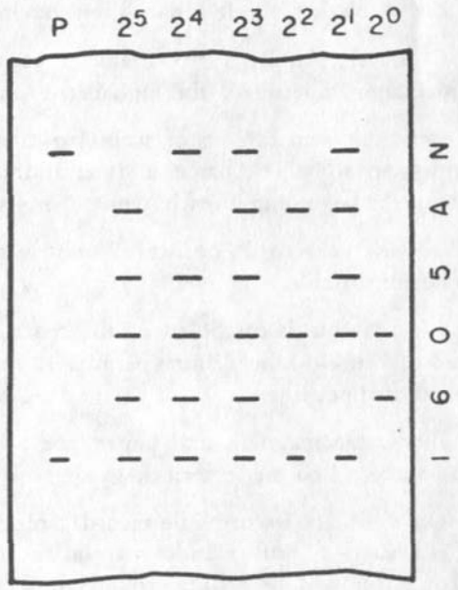


Figure 3—Recording on Hi-Data Tape Model 381

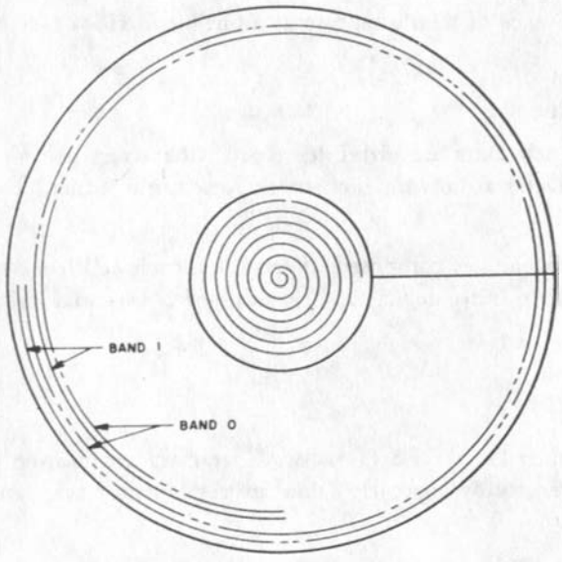


Figure 2—Recording on the Data Record

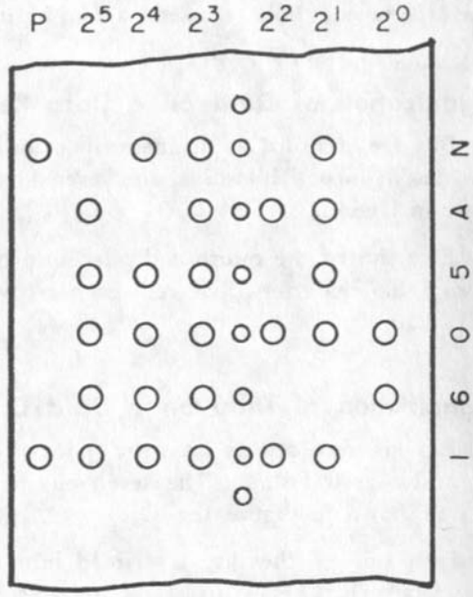


Figure 4—Recording on Paper Tape

are recorded on tape serially so that the characters making up an item follow one another in sequence from most to least significant. Interblock gaps on the Hi-Data Tape Group, Model 381, are nominally .34 inch. Interblock gaps on the Hi-Data Tape Group, Model 382, are nominally .54 inch. All data on 33KC and 66KC magnetic tape is dually recorded. Interblock gaps on 33KC and 66KC tape are nominally .45 inch and .55 inch respectively.

Variable Item and Record Length

Data storage in the RCA 301 system incorporates true variable item length. This concept may be more fully appreciated if prefaced with a definition of fixed and fixed variable word and block lengths.

"Word" is generally defined as a fixed number of consecutive characters or character locations, and "block" as a fixed number of consecutive words. These terms, word and block, are more aptly used with respect to fixed and fixed variable systems.

In a computer system using fixed word length, the number of characters for each word, or the number of words for each block, cannot be changed. In order to store data of a varying nature, redundant zeros or spaces are used to fill out the incomplete words, with uneconomical use of space.

In a fixed variable system, the number of character positions for each item in a record is assigned in accordance with the anticipated maximum length for that item. These lengths may be individually predetermined for each file, but remain constant for each item within the file. Fixed variable word length does provide greater flexibility than does fixed word length.

Data storage in a true variable length system does not have the limitations imposed by fixed or fixed variable systems. In the RCA 301, the use of control symbols and the ability to address each character location individually permits the length of any item in any record to be in strict accordance with that item's actual character count. This allows for total variability of item and record length but does not preclude the use of fixed or fixed variable lengths when the programmer finds this expedient.

In each of these categories—fixed, fixed variable, and variable, the method of internal storage is extended to the external storage. Therefore, if redundant zeros of the fixed and fixed variable systems are used in the computer, they would also appear on magnetic tape or other storage devices. By utilization of true variable length in the RCA 301 system, a characteristic business file requires less space in the Data Disc and Data Record File and less tape footage, and can be read and written out in less time than a fixed or fixed variable system would permit.

II — FUNCTIONAL DESCRIPTION

CARD EQUIPMENT

The punched card equipment includes the Card Reader, Models 323, 324, and 329, two models of Card Punches and the Card Reader-Punch.

The Card Reader, Model 323, will either: (1) automatically convert 80-column Hollerith card code to RCA 301 characters for transfer to the HSM, or (2) read a punch card image into HSM binarily where it can be processed, in any desired manner, under program control. This reader reads by row at a rate up to approximately 600 cards per minute with 20 milliseconds of free computing time between cards. The Card Reader, Model 323, can be instructed to maintain a 300 card-per-minute rate, resulting in 120 milliseconds of free computing time between cards.

The Card Reader, Model 323, feed hopper can hold up to 2,000 cards. Two card reading stations within this reader provide an automatic hole count check. Capacity of the reject stacker is approximately 100 cards. Cards may be loaded and unloaded for continuous operation. The Card Reader, Model 323, has facilities for sensing empty input hopper, full output stacker, full reject stacker and card jams, and will stop the computer if any of these conditions exist.

The Card Reader, Model 324, under program control will: (1) automatically convert 80-column Hollerith card code to RCA 301 characters for transfer to HSM, or (2) read a punch card image into HSM binarily which can be processed in any desired manner. Cards may be read on demand at rates of up to 900 cards per minute. Reading is accomplished by photo-electric sensing diodes.

Normally, the card read instruction occupies the mode (Normal or Simultaneous) for the entire card read time. However, a read release option is available which will permit the feed access time (approximately 18.5 ms) to be used for other operations.

The Card Reader, Model 324, has an input hopper which has the capacity to hold 2,000 cards. This hopper can be replenished while the machine is running provided the card level has not fallen below 100 cards. There are two output stackers—a main stacker and a reject stacker. The main output stacker has a capacity of 2,400 cards. The reject stacker can accommodate 500 cards.

The Card Reader, Model 329, under program control will: (1) automatically convert 80-column Hollerith card code to RCA 301 characters for transfer to HSM, or (2) read a punch card image into HSM binarily which can be processed in any desired manner. Cards may be read on demand at an approximate rate of 1500 cards per minute. Reading is accomplished by photo-electric sensing diodes.

Normally, the card read instruction occupies the mode (Normal or Simultaneous) for the entire card read time. However, a read release option is available which will permit the feed access time (approximately 13 ms) to be used for other operations.

The Card Reader, Model 329, has one input hopper which has the capacity to hold 3,000 cards. There are two output stackers—the accept stacker and the reject stacker. Each of the output stackers has a capacity of 2,000 cards. Cards may be loaded or unloaded while the Card Reader is operating.

One model Card Punch, Model 334, punches by row at a rate of 100 cards per minute. The input and output hoppers have a capacity of approximately 800 cards each. The cards are read after punching to permit an accuracy check of the punched data. The punch stops upon sensing an empty input or full output hopper.

The second model Card Punch, Model 336, punches by row at a rate of 200 cards per minute. The input and output hoppers have a capacity of approximately 2,000 cards each. The capacity of the reject stacker is approximately 100 cards. Cards may be loaded or unloaded for continuous machine operation.

The Card Reader-Punch consists of a card reader and card punch in the same enclosure. The Reader Unit, under program control, will either: (1) automatically convert 80-column Hollerith card code to 301 code for transfer to HSM, or (2) read a card image into HSM for processing or translation by program. Reading occurs a row at a time at rates up to approximately 800 cards per minute, with 10 milliseconds of free compute time per card cycle. When the read-release program option is exercised, an additional 21 milliseconds of compute time per card cycle is available. Two read stations permit a hole count accuracy check to be performed.

The Punch Unit punches 80-column cards in either Hollerith or binary code, as specified by the stored program. Punching is performed at rates up to approximately 250 cards per minute with 22.5 milliseconds of compute time per card cycle. An additional 37 milliseconds of compute time is available when the punch-release program option is utilized. Verification of the punched data by a read station is performed on the succeeding card punch cycle.

The input hopper of the Reader Unit holds 3,000 cards, and the input hopper of the Punch Unit holds 1,200 cards. There are five output stackers. (Two stackers for the reader, two stackers for the punch; the center stacker may be selected by either the reader or punch.) Concurrent card reading and punching operations may be performed when the system includes the Simultaneous Mode Control.

PAPER TAPE EQUIPMENT

The paper tape equipment includes the Paper Tape Reader/Punch, the Paper Tape Reader, the Paper Tape Punch and the High Speed Paper Tape Punch.

The Paper Tape Reader/Punch is mounted on the same base. The Reader and the Punch both operate at a rate of 100 characters per second. The unit writes to or reads from 5-channel or 7-channel paper tape. Gapless tape can be read. The seven channels across the width of the tape correspond to the seven bit positions (six information and a parity bit) of an RCA 301 character. When a character position on paper tape contains a punch in all seven channels, it is interpreted as "delete character," it is not an RCA 301 character and no attempt is made to read it into the Computer. When 5-channel tape is being read, the 2^5 position is interpreted as a zero bit and correct parity is placed in the 2^6 position to result in a 7-bit character being placed in HSM. When punching 5-channel tape, the 2^6 and the 2^5 bits of each character are stripped off after the character is called from HSM resulting in a 5-bit character being punched on tape. Both reading and punching can progress simultaneously if the System has a Simultaneous Control Unit. Parity is checked on all information read and on all information received at the Punch. Packing density is 10 characters per inch. Tape speed is approximately 10 inches per second. The Reader stops on a character and in a position ready to read the next character. The Stop-Start Distance of the punch is 0.3 inch, or 3 sprocket holes, from the last character punched.

The Paper Tape Reader reads 5, 6, or 7-level paper tape at speeds of approximately 500 or 1,000 characters per second. When 5 or 6-level tapes are read, additional bits are added in the most significant bit locations to produce 7-level characters of correct parity to be stored in HSM. At the 500 characters per second rate, the Reader stops on a character and in a position to read the next character. At the 1,000 characters per second rate, the Reader stops in a position to read a character at a maximum of 0.3 inch (three sprocket holes) from the last character read. Packing density on tape is 10 characters per inch, and tape moves at 50 or 100 inches per second. An adjustable guide is provided to handle tape in widths from $^{11}/_{16}$ inch to one inch. Unwind and take-up reels may be used for reading tape lengths up to 1,000 feet. All small Characters are checked for correct parity.

The Paper Tape Punch punches 5, or 7-level paper tape at speeds of approximately 100 characters per second. When 5-level tape is punched, the two most significant bits of each 7-bit character received from HSM are ignored resulting in a 5-bit character to be punched. The Punch stops in a position to punch a character a maximum of 0.3 inch (three sprocket holes) from the last character punched. Packing density on tape is 10 characters per inch, and tape moves at approximately 10 inches per second. All information received at the Punch is checked for parity.

The High Speed Paper Tape Punch, Model 332, punches 7-level paper tape at a speed of approximately 300 characters per second. There is a combined pushbutton control and indicator on the punch unit. When this is set, a three-character gap will be generated between blocks of information. When the indicator is reset, the punch will stop on a character location in position to punch in the next character location.

ON-LINE PRINTER

Both buffered and unbuffered on-line printers are available in the RCA 301 System. The buffered printers provide the advantage of off-line scan-print in addition to off-line paper advance, freeing the processor mode on completion of print table and data line transfer to the buffer. Further, the buffer can be loaded during paper advance for a prior print instruction.

Two models are available in either the buffered or the unbuffered printers. The important differences between the two models are (1) the number of characters that can be printed per line, and (2) the number of lines that can be printed per minute.

One model prints a maximum of 120 characters per line. The printing rate is up to approximately 1000 lines per minute in the Synchronous Mode which permits the printing of 47 selected characters. The printing rate is up to approximately 800 lines per minute in the Asynchronous Mode which permits the printing of 64 characters.

The second model prints a maximum of 160 characters per line. The printing rate is up to approximately 1075 lines per minute in the Synchronous Mode and up to approximately 835 lines per minute in the Asynchronous Mode.

The printers can be operated in the following combinations at the indicated speeds:

No. of Printers	Model	Synchronous Speed (lpm) per Printer	Asynchronous Speed (lpm) per Printer
	Unbuffered		
1	120 Column	1,000 (N or S)	800 (N or S)
1	160 Column	1,075* (N)	835* (N)
1	160 Column	715 (N or S)	600 (N or S)
2	120 Column #1		800 (N or S)
	#2		800 (N or S)
2	160 Column #1		600 (N or S)
	#2		600 (N or S)
	Buffered		
1	120 Column	1,000 (N or S)	800 (N or S)
1	160 Column	1,075 (N or S)	835 (N or S)
2	120 Column #1	1,000 (N or S)	800 (N or S)
	#2	1,000 (N or S)	800 (N or S)
2	160 Column #1	1,075 (N or S)	835 (N or S)
	#2	1,075 (N or S)	835 (N or S)

(N)—Normal Mode

(S)—Simultaneous Mode

* Printing at full speed in the Simultaneous Mode is not possible with the 160-column unbuffered printer due to memory interrupt requirements. If a card read or punch operation is performed in the "S" Mode concurrently with a print instruction in the "N" Mode the rates are reduced to 715 and 600 lines per minute (lpm) respectively.

The following characteristics are common to both printers:

The Printer is a transistorized device which prepares output documents, printing data directly from the High Speed Memory of the Computer. Data editing is accomplished in the Computer under the direction of the stored program. Paper advance is controlled by the Computer program, either directly or through a paper tape loop in the Printer. Paper advance is independent of the Computer activity at a rate of 150 lines a second.

Two Computer instructions are directly associated with the On-Line Printer. One controls the On-Line Printer in the Normal Mode, the other in the Simultaneous Mode. Variations in these basic instructions permit printing, paper advance for a specified number of lines, vertical tabbing, or page change. Certain combinations of these functions are also possible with these instructions.

Ten characters are printed per horizontal inch and six lines per vertical inch.

In the Synchronous Mode, the Printer will print 26 letters of the English alphabet, the numerals (0 to 9), and the following 11 punctuation marks and symbols for a total of 47 available characters.

CR	credit	/	virgule	(SP)	space
'	apostrophe	¤	lozenge	,	comma
*	asterisk	—	minus	.	period
&	ampersand	+	plus		

In the Asynchronous Mode, the Printer will print 26 letters of the English alphabet, the numerals (0 to 9), the above listed 11 punctuation marks and symbols, and the following 17 punctuation marks and symbols for a total of 64 available characters:

@	at the rate of	:	colon	$	dollar sign
%	percent	#	number	)	close parenthesis
"	quote or ditto	;	semicolon	[	open bracket
10	subscript 10	>	greater than	<	less than
(	open parenthesis	÷	divide	=	equal
]	close bracket	↑	up arrow		

For accuracy control, a printer unit inoperable alarm is incorporated which stops both the Printer and the Computer. Also, by means of a micro-switch, the Printer can sense a "low paper" condition and send a warning signal to the Computer.

When the Computer program calls for tape loop control of a page change and a "low paper" signal is present, both the Computer and the Printer stop after accomplishment of the page change and the completion of any instruction in progress in any other mode, to permit replenishment of the paper supply. Thus, printing on a page is completed before the operation is stopped.

MONITOR PRINTER

The Monitor Printer is a typewriter-like output device operated under program control. The Tape Write Normal or Tape Write Simultaneous instructions are used for operation of this device. Characters can be printed at the rate of up to 10 characters per second. Ten characters are printed per inch, 95 characters per line. Paper may be single or multiple sheets, up to 11 inches wide. The following pica type characters may be printed:

ABCDEFGHIJKLMNOPQRSTUVWXYZ
0123456789
@ ( ) = : , % & EB ; EI $ " — . • + * ED EF / '

A carriage return is effected by printing an RCA 301 "ED" character or by setting tab stops.

The information is checked for correct parity in the Processor. If the Monitor Printer is inoperable when addressed, a computer stop occurs.

INTERROGATING TYPEWRITER

The Interrogating Typewriter is an input/output device, operated under control of the stored program, which allows interrogation of the computer files via a keyboard. The replies are received and typed by the same device. The program staticizes the Tape Read Forward Normal or the Tape Read Forward Simultaneous instructions to enter data into the computer. The Tape Write Normal or Tape Write Simultaneous instructions are used to write data from the computer. The Input/Output Sense instruction is used to sense the status of the Interrogating Typewriter.

Inquiries and replies are typed on single or multiple sheet stock up to 15 inches wide, with a maximum of 135 characters to the line, ten characters per inch. The input is a manual keyboard operation, the output printing rate is up to 10 characters per second. The following pica type characters may be printed:

ABCDEFGHIJKLMNOPQRSTUVWXYZ
0123456789
@ ( ) = : / , % & EB ; EI $ " - • ED EF ' . __ *

Note: An ED may be typed for input to the computer; on output, its code effects the carriage return of the typewriter, but is not printed. Each of the following codes will be printed as an underline: $(17)_8$, $(37)_8$, $(57)_8$, $(77)_8$.

When operated as an input device, information is checked at the control module for correct parity. When operated as an output device, an echo check for correct parity is performed between the typewriter and control module. Correct transmission and proper message size may be checked by program.

MICR SORTER/READER

The MICR Sorter/Reader is operated under control of the stored program. The stored program controls the sorting of magnetically encoded documents into 13 pockets at the same time data read from the document is verified and accumulated within High Speed Memory.

The Sorter/Reader reads 6-inch documents at a speed of up to 1,560 per minute.

A separate Reference Manual (93-16-001) is available for programming this equipment.

HI-DATA TAPE GROUP, MODEL 381

The Hi-Data Tape Group, Model 381, is composed of a cluster of six, four, or three tape stations. Each tape station is used for reading and writing information on ½ inch wide magnetic tape in response to programmed instructions. Two 8 inch tape reels are mounted on each station; one a supply reel, and the other a take-up reel. Each reel accommodates 1,230 feet of magnetic tape, providing a minimum of 1,200 feet of usable tape. Tape unit design facilitates the manual interchange of reels.

Written tapes may be interchanged between individual tape stations or between units with complete compatibility.

Each tape station can be instructed to read in either the forward or reverse direction, or to write in the forward direction. Rewinding is at the rate of 90 inches per second, permitting a full reel to be rewound in less than 3 minutes completely independent of computing once initiated.

Each tape station reads or writes at the rate of 10,000 characters per second. It accomplishes this by writing 333 ⅓ characters to the inch while moving the tape at a speed of 30 inches per second. Inter-block gaps are approximately 0.34 inch in length. An automatic write lockout feature is also provided to protect master reels.

Each of the 6 tape stations within a cluster is individually addressable. Up-to-speed time is 9.8 milliseconds and write stop delay is 3.9 milliseconds. Within a given cluster, if the tape station addressed is different from the previously selected tape station, tape switching time is required. Ten milliseconds are needed unless switching from a write to read condition which requires 22.4 milliseconds. The Tape Stations are designed to facilitate the manual changing of tape reels within one minute.

Two Hi-Data Tape Groups, Model 381, can be included in a system. When the Computer is equipped with the Simultaneous Mode Control the two Tape Groups can be operated concurrently.

An automatic accuracy control prevents the tape from running off the feed reel. A write lockout prevents writing of information except on specifically designated reels of magnetic tape. Parity is checked on the information delivered to the write-head and on the tape station address received from the computer. Parity is also checked on information read.

HI-DATA TAPE GROUP, MODEL 382

The Hi-Data Tape Group, Model 382, is composed of a cluster of six, four, or three tape stations having a common set of control, power supply, and switching circuits. Each tape station can read or write binary coded characters on ½ inch wide magnetic tape in response to programmed instructions. Two 8-inch tape reels are mounted on each station; one a supply reel and the other a take-up reel. Each reel holds 1,200 feet of magnetic tape of which a minimum of 1,150 feet are usable. The tape decks are designed to facilitate the manual changing of tape reels within one minute.

Written tapes may be interchanged between individual tape stations or between units with complete compatibility.

Each tape station can be instructed to read in either the forward or reverse direction or to write in the forward direction. Rewinding is at the rate of 120 inches per second and is completely independent of computing, once initiated.

Each tape station reads or writes at the rate of 30,000 characters per second in the 382 Mode. It accomplishes this by writing 500 characters to the inch while moving the tape at a speed of 60 inches per second. Inter-block gaps are approximately .54 inch in length. An automatic write lockout feature is also provided to protect master reels.

Each of the 6 tape stations within a cluster is individually addressable. Up-to-speed time is 4.3 milliseconds and read-after-write stop delay is 5.67 $\pm$ .5 milliseconds. There is no switching time. The tape stations are designed to facilitate the manual changing of tape reels within one minute.

Two Hi-Data Tape Groups, Model 382, may be included in a system. When the Computer is equipped with the Simultaneous Mode Control the two tape groups can be operated simultaneously.

An automatic accuracy control prevents the tape from running off the feed reel. A write lockout prevents writing of information except on specifically designated reels of magnetic tape. Parity is checked on the tape station address received from the computer. Parity is checked on the information written to tape by the incorporation of a read-after-write parity check.

In order to provide compatibility with the Hi-Data Tape Group, Model 381, each tape station will be equipped with two switches. The first switch (381) will permit a tape prepared on a Model 381 Tape Station to be read on a Model 382 Tape Station. The second switch is used in conjunction with the first. When both are set, tapes will be prepared on the Model 382 Tape Station that may be read on a Model 381 Tape Station. In the 381 Mode, each tape station can read or write at the rate of 20,000 characters per second. It accomplishes this by writing 333 characters to the inch while moving the tape at 60 inches per second.

33 KC MAGNETIC TAPE STATION

The 33 KC Magnetic Tape Station is used for reading and writing binary coded characters on ¾ inch magnetic tape at a rate of 33,333 characters per second. Data is recorded at a density of 333 ⅓ characters per inch. The tape speed is 100 inches per second, forward or reverse. Reading is possible in the forward or reverse direction; writing is performed in the forward direction. All characters are dually recorded on tape, and parity is checked on all data read or written. The tape station is designed to facilitate manual interchange of tape reels, which can be accomplished in less than one minute.

The gap between blocks is nominally 0.45 inch. Tape-write-up-to-speed delay is 4.5 milliseconds.

33 KC Tape Stations may be operated in the system through Tape Adapters, Dual Tape Channels or a combination of both. The Tape Adapter connects a single Tape Station to the Computer. Two models of the Dual Tape Channel (2 x 6 switch or 2 x 12 switch) are available which operate up to six, and up to 12 Tape Stations, respectively. One 33 KC Dual Tape Channel and up to two 33 KC Tape Adapters may be connected to the Computer for operation of up to 14 Tape Stations. When the Computer is equipped with the Simultaneous Mode Control two Tape Stations can be operated concurrently.

66 KC MAGNETIC TAPE STATION

The 66 KC Magnetic Tape Station is used for reading and writing binary coded characters on ¾ inch magnetic tape at a rate up to 66,667 characters per second. Data is recorded at a density of 667 characters per inch nominally. The tape speed for reading and writing is 100 inches per second. Tape rewind speed is 150 inches per second.

Reading is possible in the forward or reverse direction; writing (and erasing) are performed in the forward direction. All characters are dually recorded on tape, and each character is read and checked for parity after it is written. There is also a parity check on all characters read. The Tape Station is designed to facilitate manual interchange of tape reels, which can be accomplished in less than one minute.

The gap between blocks is nominally 0.55 inch. Tape-write-up-to-speed delay is 3.5 milliseconds, and the read-after-write stop delay is 2 milliseconds.

66 KC Tape Stations may be operated in the system through Tape Adapters, Dual Tape Channels, or a combination of both. The Tape Adapter connects a single Tape Station to the Computer. Two models of the Dual Tape Channel (2 x 6 switch or 2 x 12 switch) are available which operate up to six, and up to 12 Tape Stations, respectively. One 66 KC Dual Tape Channel and up to two 66 KC Tape Adapters may be connected to the Computer for operation of up to 14 Tape Stations. When the Computer is equipped with the Simultaneous Mode Control two Tape Stations can be operated concurrently.

MULTIPLE TAPE LISTER

The Multiple Tape Lister, Models 340-6 and 340-12, is an electro-mechanical printer having 6 or 12 separate paper feed units (two models). Printing is possible on any one tape or a maximum of two tapes with one instruction. When two tapes are being printed with one instruction, the first (leftmost) tape of the Multiple Tape Lister will always be printed and a designated one of the five or eleven other tapes will be printed. The maximum printing rate is up to 2,000 lines per minute.

Each of the six or twelve printing areas has the same format containing a maximum of 24 print positions. The first 23 positions of each print area will be capable of printing the numerics (0–9) and five symbols (. , # = — (minus)). Position 24 will print a selected group of alphabetical characters (B, C, D, F, L, M, R, S, T, X, Y) and four symbols (¤, C_R, *, +).

Character spacing is 10 columns per horizontal inch and vertical spacing is six lines per inch.

The first character which is always sent to the Multiple Tape Lister is the Control Character. This character supplies information to the Multiple Tape Lister concerning the tape(s) to be printed and paper advance. The next 24 or 48 characters sent to the Tape Lister are the information characters to be printed.

DATA EXCHANGE CONTROL

The Data Exchange Control, Models 377-1 and 377-2 enables any two 301 Processors, each equipped with this control, to communicate with each other. A second Data Exchange Control may be included on a 301 Processor if it is necessary for this processor to communicate with two other 301 Processors.

Data may be transmitted in either direction but in only one direction at one time. Either processor may initiate a data transmission. Transfer of information from HSM to HSM is by diad.

The data transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both processors. For example, if the Normal Mode is used in both processors and nothing else is being done, the maximum attainable transfer rate of 285.6KC (1 out of 1 status levels) can be achieved. The actual transfer rate will be in a range between 285.6KC (1 out of 1 status levels) and 142.8KC (1 out of 2 status levels) depending on the clock synchronization of the two processors. If the Simultaneous Mode is used in both processors and nothing else is being done, the transfer rate will range between 142.8KC (1 out of 2 status levels) and 95.2KC (1 out of 3 status levels) depending on the clock synchronization of the two processors. In a practical system, the actual transfer rate will be dependent upon the available status levels in both processors when other operations are being performed simultaneously with the data transmission.

RANDOM ACCESS COMPUTER EQUIPMENT

DATA RECORD FILE

Data Record Files are available to be used both as an extension of memory and as a medium for input-output.

Each Data Record File consists of 128 records which can be recorded on both surfaces. Each surface contains two bands in which information is recorded in serial fashion in a spiral pattern around the record. Each band

contains 10 cells of 900 characters each. The total capacity of the file is over 4.6 million characters. Data may be stored in each cell in any quantity up to 900 characters. Blocks of one to ten cells may be transferred between HSM and the Data Record File with one instruction, at the rate of 2,500 characters per second.

The records of the Data Record File can be easily removed and exchanged. A single instruction, once initiated, will search for and select a record, put the record on the turntable, and position the arm over the correct band, without interrupting other Processor activity.

A total of six Data Record Files can be used in an RCA 301 System, two through individual Control Modules and four through the Record File Mode Control. Three of the Files can be transferring data at the same time, one in the Normal Mode, one in the Simultaneous Mode, and one in the Record File Mode. A Band Search can be taking place in all six of the files at one time.

A parity check is performed on the information to be written on the record and on the address of the data to be selected. An automatic write lockout feature is provided to prevent accidental writing on master records.

DATA DISC FILE

The Data Disc Files provide large capacity rapid random-access storage for data and computer programs.

Data is recorded on both sides of the magnetic discs. There are 9 zones of 128 tracks on each disc surface, and each track contains 10 sectors of 160 characters. The total capacity of one module is 22,118,400 alphanumeric characters. Blocks of from one to ten sectors may be transferred between High-Speed Memory and the File with one instruction. When the strata concept of data organization is utilized, associated records of data stored within related tracks of each zone on each disc surface are accessible within a single file positioning. There are 108 related tracks per module for each strata.

"Access time" consists of the sum of two functions: (1) moving the read-write heads to the selected track, and then (2) waiting for the disc to revolve to the point that the beginning of data to be read is positioned under the heads. The latter function is termed "latency." Minimum access time to locate and start reading data is 5 milliseconds Access time is as follows:

	Minimum	*Average*	*Maximum*
363-2	70	130	200
363-3	70	150	210
363-4	75	170	235
363-5	75	170	235

Once initiated, a Track Select proceeds independently of other computer processing.

Information is recorded bit-serially in each track. Each zone has one read-write head serving 128 tracks. All read-write heads in a file are moved simultaneously so that when an arm is positioned to a particular track in a particular zone, all arms are positioned to the corresponding track within their respective zones.

Two Files can be transferring data to or from the High Speed Memory at the same time, one in the Normal Mode and one in the Simultaneous Mode.

A parity check is performed on the information to be written on the disc and on the information read from the disc. A check is made to determine that the positioner is on the correct track of the disc. Conversion from bit-serial to character-serial operations are checked by a bit counter.

3488 UNIT

General Description

The Model 3488 Random Access Computer Equipment represents a mass storage device in excess of 5.4 billion characters on line to a 301 processor.

Data is recorded on one side of 16 inch by 4½ inch flexible magnetic cards.

These cards are housed in groups of 256, which are called magazines.

Up to 8 magazines are contained in a basic retrieval unit. Eight additional magazines can be added giving the device a 16 magazines maximum (see figure 1).

The magazines are removable and interchangeable, and they may be removed from one retrieval unit, inserted and processed on other 3488 retrieval units.

A card is removed from its magazine by mechanical grips which are program addressable. Once the card enters onto the transport belts (see figure 2) it moves towards the read/write heads located near a revolving drum (capstan) where data can be read or recorded.

A gate located at this point determines whether the card is to be returned to the magazine where it came from, or to remain at the recording station and be circulated under the read/write heads.

Retrieval Assembly

Each eight-magazine Retrieval Assembly (3488-1) contains, in addition to the magazines, a card transport mechanism, card selection mechanism, read/write station, and all necessary internal addressing and timing logic. The Expansion Assembly (3488-2) can expand the capacity of the unit to 16 magazines. The Expansion Assembly contains a card transport mechanism and a card selection mechanism.

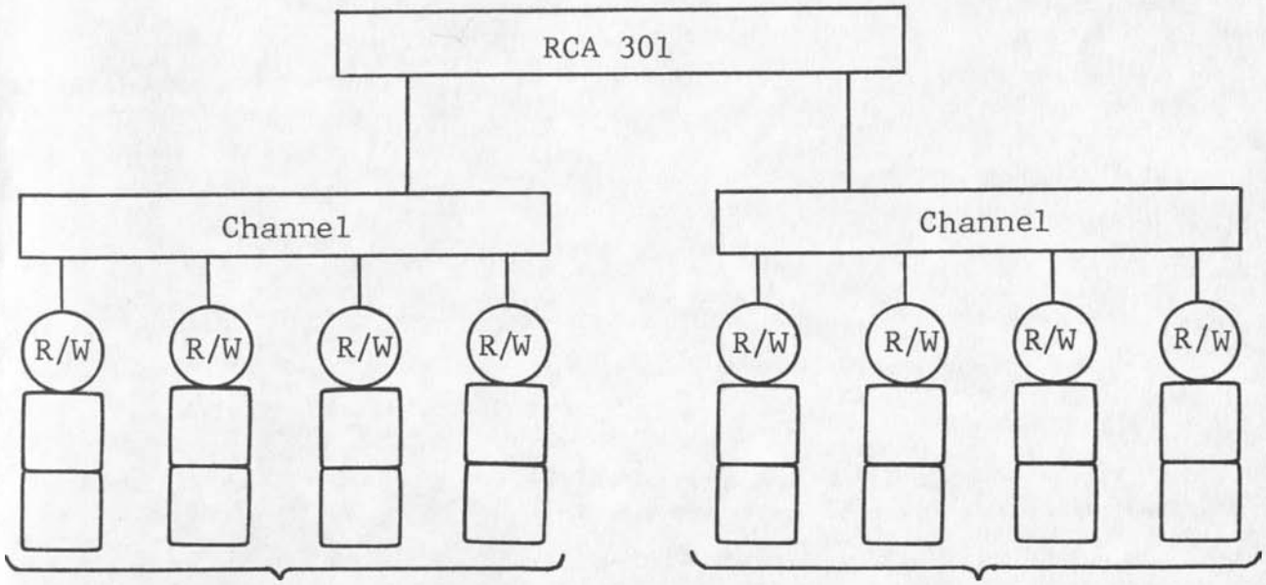
Magazines

Each magazine contains two decks of 128 uniquely addressed cards. Each deck of cards is contained within a separately-addressable half of a magazine. Addressing is independent of the relative position of the cards within each half-magazine. This eliminates the need for a card to be returned to the exact same position within its deck; it is returned to the end of the deck in the half-magazine from which it was extracted.

Card Transport Mechanism

This Transport (Raceway) mechanism provides the means for physically moving the selected card to the read/write station (card feed) and returning the card to the magazine (card return). If the expansion assembly is added, the expansion assembly transport mechanism feeds into the primary card transport mechanism for movement to and from the read/write station.

RCA Computer System with Maximum 3488 Configuration
5.4 Billion Characters



Four 16-Magazine Retrieval Units **Four 16-Magazine Retrieval Units**

Figure 1

Sixteen-Magazine Retrieval Unit
681.6 Million Characters

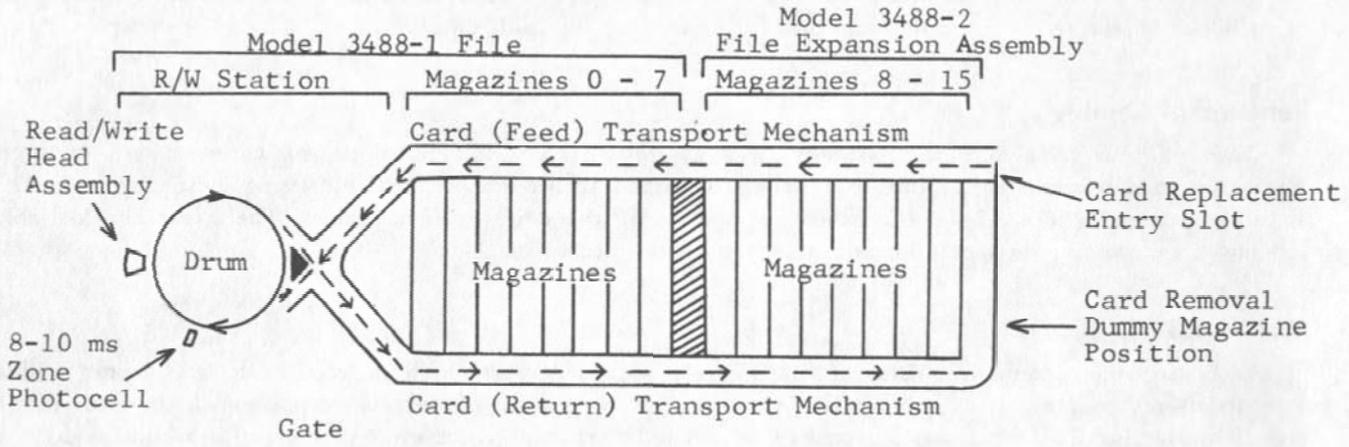


Figure 2

Card Format

Bands — Each 3488 card contains 128 tracks, each of which runs the full length of approximately 14.5 inches of recording area on the card. The 128 tracks are divided into 64 separately addressable bands of 2 tracks each. Characters are recorded bit-serial per track. Two tracks are recorded in parallel, each at a density of 700 bits per inch.

Blocks — Each band (two tracks) of recorded information is divided into 4 blocks of 650 7-bit characters each.

The capacity of the 3488-1 along with the expansion assembly are included below.

UNIT	NO. OF SEVEN BIT CHARACTERS
Block	650
Band (4 Blocks)	2600
Card (64 Bands)	166,400
Magazine (256 cards)	42.6 million
Retrieval Assembly (8 magazines)	340.8 million
Retrieval Assembly Plus Expansion Assembly (16 magazines)	681.6 million

Control

The Model 380 channel acts as the interface between a 301 Processor and up to four Model 3488 random access units. Two Model 380 channels can be used in each 301 System.

The channel permits one-way transfer of data between one of four random access units and the 301 Processor.

The channel enables selection and reading/recording of magnetic cards contained in a random access unit, under program control. Character parity checking and character buffering are performed in the channel.

The Control includes the addressing registers, decoding circuitry, necessary control interface, and buffering.

Addressing

Addressing is a function of the retrieval unit, which contains the required registers as follows:

A full register for selection.

A full register for preselection.

A magazine address register used to return a card to its associated magazine.

These registers permit overlapping of the selection, preselection, and return of cards.

INSTRUCTIONS

The instructions utilized to program the Random Access device include:

Select (SEL)
Read Normal (RFN)
Read Simultaneous (RFS)
Write Normal (TWN)
Write Simultaneous (TWS)
Input/Output Sense (IOS)

These instructions are described on the following pages under the headings:

Select, Reading, Writing, and input/output sense.

The read/write head assembly, which contains eight pairs of heads (one Read, one Write head for each pair), can be moved to one of sixteen positions. Once positioned, the head assembly is capable of reading or writing to one of four bands, each band containing four blocks.

Card Select

The Card Select time (275 ms. nominal) 260 ms. minimum; 290 ms. maximum; is the time required to select a specific card from a magazine and place it into position to be extracted onto the raceway. If at this point of time the card can be placed on the capstan, it will be immediately extracted. Approximately 75 ms. nominal (67–82 ms.) is required to clear a card from the Preselect position through the pinch rollers that place it on the raceway. At this point, another card select is permissible.

Timings (all times are in milliseconds and are nominal)

	Position*	Card Select	Card Feed	Card Return	Reload
3488-1	0A	275	136	170	50
	0B/1A		145	182	
	1B/2A		156	196	
	2B/3A		172	209	
	3B/4A		185	222	
	4B/5A		198	235	
	5B/6A		211	248	
	6B/7A		225	262	
	7B		235	275	
3488-2	8A		275	327	
	8B/9A		288	341	
	9B/10A		302	355	
	10B/11A		313	369	
	11B/12A		324	383	
	12B/13A		335	397	
	13B/14A		346	411	
	14B/15A		357	425	
	15B		368	441	

* where A = 1st half of magazine and B = 2nd half of magazine

Card Feed Time

Card Feed Time is the time required to move a card from the select position until the first block is under the read/write heads.

Card Return Time

Card Return time begins when the leading edge of the card passes under the read/write heads.

Card Reload Time

Card Reload Time is a nominal time required for the card to be reloaded into the designated magazine.

Drum Revolution Time

Drum Revolution Time is 60 ms., i.e., 40 ms. to pass the card and 20 ms. for gap time. Each block of 650 characters requires approximately 8 ms., and the inter-block gap is approximately 1 ms.

Block Select Timing

Under nominal operating conditions, it is possible to read or write to the next consecutive block as long as no read/write head assembly movement is required and the Block Select and Read/Write commands are issued no more than 100 ms. after the end of the preceding block. It is also possible to issue a no head movement Block Select within the card gap time.

When a Block Select requires that the head be moved anywhere within positions 0 to 7 or anywhere within positions 8 to 15, then 20 ms. is required to move the head positioner. When movement is made that crosses over these boundaries, i.e., 7 to 8, 0 to 15, 8 to 7, etc., then 34 ms. is required to move the head positioner.

If a read or write is issued that misses the beginning of its specified block, the operation will be automatically held off until the block approaches on the next revolution.

ACCURACY CONTROL

Address Verification and Card Absent Checking

To determine that the proper half-magazine has been selected, a bail sensor micro-switch is activated. This identification of the selected half-magazine is compared with the requested address (Select instruction). To determine that the proper card has been selected, a set of photocells are located on the track in position for reading the binary coded selection notches on the top of the card. This reading is compared with the requested address (Select instruction) before the card is placed on the capstan.

A head position sensor is mounted on the head assembly. A reading from the sensor is compared with the register specifying the requested head position to insure proper head positioning. A constant check is made for proper head positioning while reading or writing. A format notch is used to select the proper block.

An echo check is made while recording to assure that current is flowing through the selected head. Failure of this check is considered an Address Verification error.

A check is made to ascertain that the returning card returns to the magazine that was originally selected.

Both Address Vertification and Card Absent error conditions will cause device inoperability.

When the Address Verification error occurs on a card that has been extracted, the device will go inoperable immediately, and the card will be returned to its magazine after one revolution on the capstan. When the Address Verification error occurs on a card that is being selected, the device will go inoperable at the time the card extract would be attempted. The card will not be extracted.

When a Card Absent error occurs (First attempt) normal operation of the unit will be allowed until the transport is cleared. Once all the cards are in their magazines, the hardware will make a second attempt to select the card. If the Card Absent indication is received after this attempt, the unit will be made inoperable.

If an attempt is made to select a card from a magazine position that does not contain a magazine, an Illegal Operation indication is given. The fact that a magazine is not present will be sensed by a switch located in each magazine position.

Automatic Removal of Unserviced Cards

Whenever a card remains unserviced for over 32 revolutions of the capstan, the card will be automatically removed, returned to its magazine.

Read and Write Checking

A Read-after-Write parity check and missing bit check is automatically made as each block is written. Failure of this check will cause termination of the Write, and an indication is given.

While reading, each character read will be checked for proper parity. Any single bit error in a specific character will be automatically corrected before being transmitted to HSM. If a parity error occurs that cannot be automatically corrected, an $(57)_8$ will be transferred to HSM, a parity error indication will be set, and the remainder of the information in the block will be transferred but may not be valid. If more than one block is being read, information transfer will resume at the beginning of the next block.

Address Data Checking

Address data is parity checked. When bad parity is detected, the unit automatically become inoperable.

Preamble Checking

A synchronizing preamble is recorded in front of each block written. At the beginning of a Read and Read-after-Write, this preamble is used to synchronize the operation. If synchronization is not accomplished, a preamble error is indicated.

Interlocks

As soon as the first card is fully extracted, a preselect of a second card can be executed. The second card will not be extracted until the first card leaves the capstan. If the card returning is in the raceway (in position to be reloaded into the magazine), the reload will be delayed until the extract is completed. If the reload has been started, the extraction will be delayed until the reload is completed.

If a card is in the return cycle, and there is a card on the capstan and a preselect is attempted, the preselect command will be accepted but not executed until the reload of the card in the return cycle is completed.

If there is a card in the return cycle that has not reached the reload point, and no card is on the capstan, a card may be selected and extracted immediately, while the card on the return path is delayed in its reload operation. At no time will there be more than two cards in motion.

Card Extract Counter

The Card Extract Counter is mechanized by recording a 15-bit binary number in a special track on the card. During normal operations, the count is read, decremented by one, and rewritten. A check is made to indicate when the count reaches zero. When the count reaches zero, a special (equal) bit is recorded. On the next extraction, the system recognizes the equal bit and records an overflow bit. On all subsequent extractions, overflow is reported and no writing takes place.

These indications can be sensed by use of the Standard 301/3301 Sense instruction as follows:

Option $2 - 2^2 = 1$ Test for count equals limit.
$2^3 = 1$ Test for count has exceeded limit. (Set each time card is placed on capstan after the count has been exceeded.)

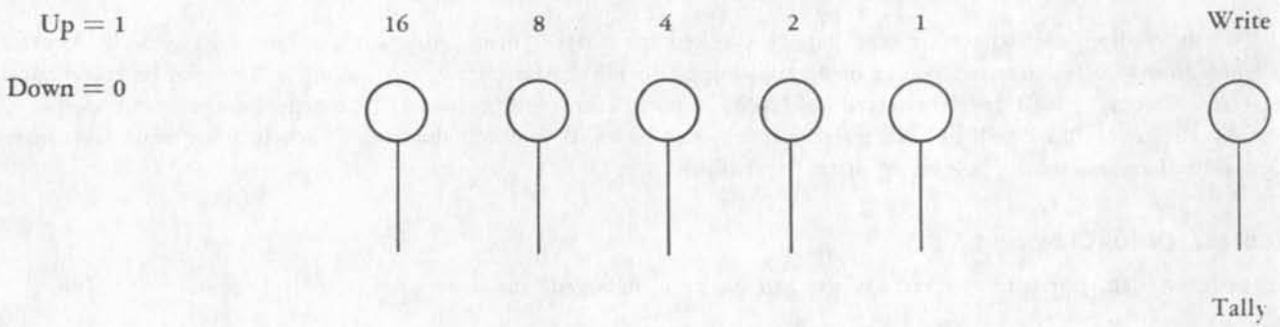
Five (5) toggle switches are used to set up the amount to be prewritten on the card. These switches are located on the rear of the maintenance control panel.

When the Write-Tally switch is in the Write position, every card extracted is prewritten. When the Write-Tally switch is in the Tally position and the device is in "Remote", normal count-down will be performed.

The Tally quantity is always recorded with the ten (10) least significant bits all 0's. The five (5) high order bits are recorded in accordance with the switch setting; therefore, the number is 1,024 times N, where N is the number from 0–31, set into the five (5) binary switches. The maximum number that can be recorded is 31 x 1,024, or 31,744.

All Tally operations occur before the card reaches the Read/Write Head on the first pass of the card. Therefore, a card circulating on the capstan cannot be initialized by setting the Write-Tally switch to Write; the switch must be set before the card reaches the capstan.

The Controlling switches are as follows:



Note: When the "Write-Tally" switch is in the "Write" position, it will cause the amount specified to be written on the card while in either the Local or Remote Mode. Care must be exercised when using this feature in the Remote Mode to avoid overwriting a valid existing Tally count.

III — FUNCTIONAL DESCRIPTION

HIGH SPEED MEMORY

The High-Speed Memory (HSM) in the RCA 301 System consists of 10,000, 20,000 or 40,000 characters. Each 10,000 characters consists of fourteen 50 x 100 matrices of magnetic cores. As each core represents one bit, a matrix of cores represents 5,000 bits and a memory unit represents 70,000 bits. As each 301 character is made up of seven bits, each memory unit can store 10,000 characters in 10,000 individual character locations.

Each location in memory has a unique address, consisting of four RCA 301 characters. Though oversimplified, the HSM may be pictured as a rectangular array of locations, with the smallest address in the upper left-hand corner and the largest address in the lower right-hand corner. The lowest address in the HSM is always 0000. The highest address in a system with a 10,000 character memory is 9999. In the case of a 20,000 character memory the second 10,000 characters are addressed from &000 to I999. In the case of a 40,000 character memory, the third 10,000 characters are addressed from —000 to R999, and the fourth 10,000 characters are addressed from "000 to Z999. If an address greater than the processor's maximum memory location is specified, a Memory Register Parity Error alarm will occur and stop the Computer.

The HSM is constructed so that two characters (14 bits) in consecutive memory locations are accessed in a single memory cycle. The computer cycle is 7 microseconds; this means that characters may be addressed, brought into the memory register, and regenerated in their original locations every 7 microseconds. Each of these groups of two locations, or the contents thereof, is called a "diad." Each diad begins with an "even" decimal address, and ends with the next consecutive "odd" address (such as the diad with addresses 1134 to 1135). Diagrammatic representations of portions of the HSM used throughout this manual are shown below.

5234	5235	5236	5237	5238	5239
D	E	F	G	2	J

The HSM address of each location is shown in the upper portion of the diagram, with the characters stored in each location shown in the lower portion.

The primary purpose of the HSM is the storage of programs and data. These may be stored in any area of the memory except for those locations reserved as Standard HSM Locations (see Appendix E).

THE BASIC INSTRUCTION

Instruction Format

Each of the RCA 301 instructions consists of four parts:

1. Operation Code (one character)
2. N Character (one character)
3. A Address (four characters)
4. B Address (four characters)

An instruction, then, is made up of ten RCA 301 characters with the format:

O	N	AAAA	BBBB
Operation Code	N Character	A Address	B Address

In most cases, the entire A address refers to a HSM location, and the entire B address refers to another HSM location. In some instructions, however, only a portion of the A address or B address is used, or one part of the address may designate one value and the other part another value. The components of the A address are referred to as A_0, A_1, A_2, A_3, and the components of the B address as B_0, B_1, B_2, B_3.

In instructions where the N character is used as a count, the number of the count may be from 0 to 44. As the N character can only contain one character, the following symbols are used to designate the N character for counts from 0 to 44:

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	11	A	22	K	33	T
1	1	12	B	23	L	34	U
2	2	13	C	24	M	35	V
3	3	14	D	25	N	36	W
4	4	15	E	26	O	37	X
5	5	16	F	27	P	38	Y
6	6	17	G	28	Q	39	Z
7	7	18	H	29	R	40	EB
8	8	19	I	30	"	41	, (comma)
9	9	20	— (minus)	31	/	42	%
10	&	21	J	32	S	43	● (ISS)
						44	=

Storage of Instructions

Instructions are stored sequentially in the High Speed Memory. Each instruction is stored in ten consecutive memory locations (5 diads) so that the Operation Code is placed in the first character of a diad.

Staticizing

An instruction can be interpreted and executed by Program Control only after it has been brought out of the High Speed Memory locations in which it has been stored, and its components placed in the proper registers. This process is called "staticizing" and is accomplished in five status levels.

A status level lasts for seven microseconds and is a term applied to a series of pulses which open certain paths over which information can travel. Each status level has a specific function. In staticizing each instruction, the first status level brings the first diad (two characters) of the ten character instruction (ONAAAABBBB) into the Memory Register and automatically regenerates the characters in their original location in the HSM.

The O character is then sent to the NOR Register, and the N is sent to the N Register. This completes the first status level. The second status level brings the next diad (A_0, A_1) into the memory register, regenerates the characters, and sends the A_0, A_1 characters to the A Register. During the third status level the A_2, A_3 characters are transferred in a similar manner, and the fourth and fifth status levels transfer B_0, B_1 and B_2, B_3 to the B Address Register.

The total staticizing time is 35 microseconds, and is constant for every instruction, even when the N count is zero. The number of status levels involved, and their sequence for execution (after staticizing) of a given instruction, depends upon what must be accomplished by that instruction.

Direct and Indirect Addressing

When the least significant character of an address is written as a number, i.e., the zone bits are 00, the address is a direct address. Direct addresses establish the initial register settings for instructions in which they are employed.

When the least significant character of an address has zone bits 01, thus forming one of the following characters:

& for 0	E for 5
A for 1	F for 6
B for 2	G for 7
C for 3	H for 8
D for 4	I for 9

the address is an indirect address. When an indirect address is staticized, the contents of the HSM location addressed by that indirect address replace it in the register. If the replacing address is also an indirect address, it too will be replaced in the register by the contents of the memory locations it addresses. The initial register settings for any instruction, are therefore, not established until both the A and B Registers have been supplied with direct addresses. An indirect address must address the least significant diad of another address. Indirect addressing has proven valuable in reducing programmer effort, processing time, and instruction storage. Each indirect address requires two additional status levels (14 microseconds).

PROGRAM CONTROL

Program Control is the control unit of the system. It interprets and executes the instructions stored in the High Speed Memory, directs the sequence of operations within the system, controls operation of the input/output devices, and performs automatic accuracy checks.

Program Control includes a number of specialized devices. Those which are of interest to the programmer are diagrammed in Figure 5, and are briefly discussed below, along with certain automatic Program Control functions.

Registers

The *Memory Addressing Register* stores the address of the HSM location to be processed. The capacity of this register is four RCA 301 characters.

The *Memory Register* has a capacity of two RCA 301 characters. It receives the diad contents that emerge from or are to be placed in the HSM. A series of Memory Output Gates permit or inhibit entrance into the Memory Register of either or both of the characters that emerge from the HSM.

The *Interchange* links the Memory Register with the Memory Address Bus. It selects the proper bus or busses to which characters are transferred from the Memory Register according to the operation being performed. For example, during staticizing operations, it selects the proper busses for the transfer of two instruction characters (diad) at a time into the proper registers. During an input-output operation, it selects the correct bus for single character transfer of information into and out of the HSM.

The *A Register* has a capacity of four RCA 301 characters. It receives the A address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The *B Register* has a capacity of four RCA 301 characters. It receives the B address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The *P Register* has a capacity of four characters and holds the HSM address of the next instruction in sequence.

The *NOR (Normal Operation) Register* has a capacity of one RCA 301 character. It holds the Operation Code of the instruction currently being executed in the Normal Mode.

The *N Register* has a capacity of one character. It holds the N character of the currently processed instruction.

The N_R *(Repeat) Register* is used by the Repeat instruction to store the count.

When an operation is executed in the Simultaneous Mode, four Registers are utilized:

Simultaneous Operation Register (SOR) (receives OP Code)

M Register (receives N character)

S Register (receives A address)

T Register (receives B address)

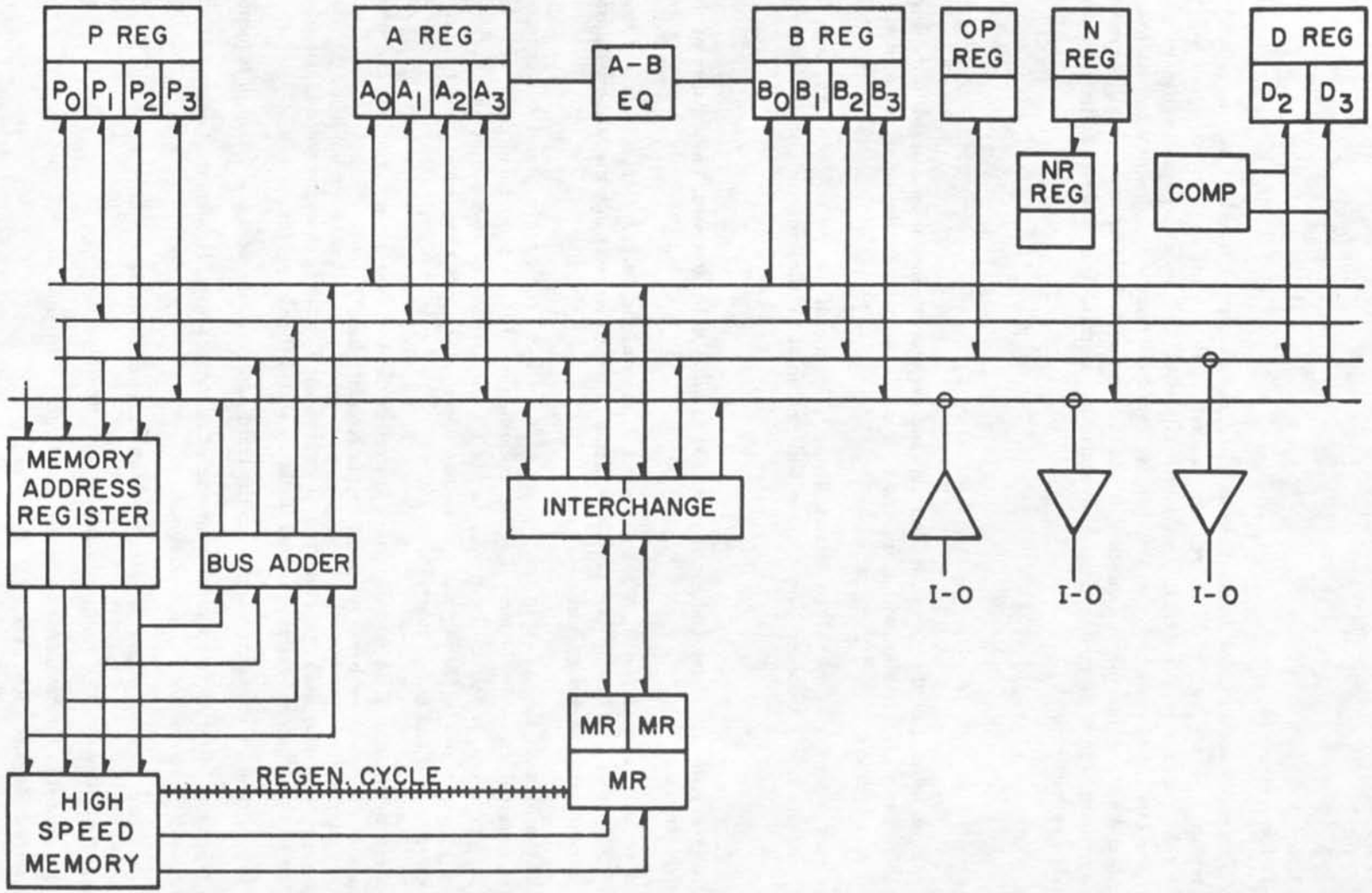


Figure 5—Block Diagram of Basic RCA 301 Computer

These registers assume the function of the NOR, N, A and B Registers respectively.

If an operation is executed in the Record File Mode, the following registers are utilized:

Record File Operation Register (FOR) (receives OP Code)

L Register (receives N character)

U Register (receives A address)

V Register (receives B address)

These registers also assume the function of the NOR, N, A, and B Registers.

The *D Register* has a capacity of two RCA 301 Characters. Comparisons and arithmetic instructions utilize this register.

The *Bus Adder* is used to modify the contents of the various address registers. The Bus Adder can increment or decrement the contents of these registers by either 1 or 2, or leave them unchanged, thus permitting register contents to be directly related to the currently processed characters or diads.

The *A-B Equality Circuit* is located between the A and B Registers and is used to compare their contents. When they are equal, a flip-flop is set indicating to the Computer that the instruction-defined sector has been processed and the instruction can be terminated. In instructions that specify the left and right boundaries of the HSM sector to be processed, the contents of the A Register are always increased toward A-B equality and the contents of the B Register remain unchanged.

The *Memory Address Bus* is a four character pathway between the Interchange, Computer Registers, and Input-Output buffers. The particular pathways used are determined primarily by the Interchange.

The *Previous Result Indicators,* or PRI's are a set of flip-flops which preserve the sign of the result (or the zero result) of an arithmetic operation for automatic reference by a subsequent decision instruction. If the result is positive, the Previous Result Positive (PRP) flip-flop is set; if negative, the Previous Result Negative (PRN) flip-flop is set; if zero, the Previous Result Zero (PRZ) flip-flop is set. The PRI's are set in most of the arithmetic and logical instructions, and in certain search and transfer operations.

The PRI's may be sensed by use of the Conditional Transfer of Control Instruction.

Arithmetic Functions

The arithmetic function of addition and subtraction in the RCA 301 System is performed by the use of arithmetic tables permanently stored in the High Speed Memory (Standard Memory Locations 0000-0199). These locations can be written into only if a special button on the console is depressed, thereby preventing the accidental destruction of these tables. The add and subtract instructions perform arithmetic operations utilizing a table lookup technique where the arguments are the specified operands.

Automatic Storage of Final Contents of the A Register (STA)

STA is an automatic operation which occurs at the conclusion of selected RCA 301 instructions. In STA, the final contents of the A Register are automatically stored in the High Speed Memory locations 0212-0215. This permits the subsequent use of the final A Register contents. It is also a highly convenient programming technique which can be utilized to eliminate memory searching time.

STA is performed in the following list of instructions:

Locate Symbol Left	K
Locate Symbol Right	L
Transfer Data by Symbol Left	#
Transfer Data by Symbol Right	P
Tape Read Forward Normal	4
Tape Read Reverse Normal	6
Block Read Record Normal	F
Sector Read Disc Normal	F

To preserve the final A Register contents of all other instructions, the Store Register instruction can be used.

Automatic Storage of Contents of P Register (STP)

STP is an operation which occurs whenever control is to be transferred; that is, whenever the next instruction to be performed is not the one stored immediately following the current instruction. STP automatically stores the contents of the P Register in standard High Speed Memory locations 0216-0219. The stored address is the address of the instruction that would have been executed if the transfer of control had not taken place. STP is performed in the following instructions, but only when control is actually transferred:

Conditional Transfer of Control

Tally

Input/Output Sense

Repeat Instruction

The Repeat Instruction (RPT) will cause the next one of the following instructions to be performed to be repeated a specified number of times:

Tape Read Forward Normal

Tape Read Reverse Normal

Add

Transfer Data Left

Transfer Data Right

Subtract

Translate by Table

Transfer Data by Symbol Left

Transfer Data by Symbol Right

Logical "OR"

Exclusive "OR"

Logical "AND"

The number of times a repeatable instruction following an RPT is to be repeated is specified in the N character of the RPT. If the N character of the RPT is zero, the repeatable instruction will be executed but not repeated. If the N character of the RPT is one, then the repeatable instruction will be performed twice. Each repeatable instruction, when repeated, requires three additional status levels (21 microseconds) when the contents of the N_R (Repeat) Register exceed zero, and requires one additional status level (7 microseconds) when the contents of the N_R (Repeat) Register equal zero.

Simultaneity in the RCA 301 System

Simultaneity in the RCA 301 Computer is defined as the coincident execution of two or three instructions. Simultaneity is accomplished through the optional control units: the Simultaneous Mode Control Unit and the Record File Mode Control Unit. When an instruction utilizes the circuitry of the Simultaneous Mode Control Unit it is progressing in the "Simultaneous Mode." When an instruction utilizes the circuitry of the Record File Mode Control Unit it is progressing in the "Record File Mode." When an instruction utilizes the Program Control circuitry of the basic computer it is progressing in the "Normal Mode."

The RCA 301 instructions are designed to operate in one of the three modes. Those instructions designed to operate in the Normal Mode will operate in that mode only. If a button, called SMDI (Simultaneous Mode Inhibit), on the Console Panel is not on, those instructions designed to operate in the Simultaneous Mode will operate in that Mode only. If, however, SMDI is on, simultaneous instructions will operate in the Normal Mode as if they were Normal instructions and the Store S Register instruction will store the contents of the A Register in STA locations. Those instructions designed to operate in the Record File Mode will operate in that mode only.

Operation of the Simultaneous Mode

The following instructions are designed to operate in the Simultaneous Mode:

Card Read Simultaneous
Card Punch Simultaneous
Tape Read Forward Simultaneous
Tape Read Reverse Simultaneous
Tape Write Simultaneous
Print and Paper Advance Simultaneous
Block Read Record Simultaneous
Block Write Record Simultaneous
Sector Read Disc Simultaneous
Sector Write Disc Simultaneous

All instructions in the RCA 301 System are staticized in the Normal Mode. When any one of the above instructions is staticized, provided:

1. SMDI is not on,
2. The system is equipped with a Simultaneous Mode Control Unit, and it is free; i.e., some other instruction is not now progressing in the Simultaneous Mode,

then the simultaneous instruction is transferred to the Simultaneous Mode; i.e., the contents of the NOR Register are transferred to SOR, the contents of the N Register are transferred to the M Register, the contents of the A Register are transferred to the S Register, and the contents of the B Register are transferred to the T Register. The instruction is then executed in the Simultaneous Mode with SOR, M, S and T Registers acting as the NOR, N, A and B Registers respectively. The instruction is then processed similarly to a normal instruction. Immediately upon the transfer of an instruction from the Normal to the Simultaneous Mode, the Normal Mode is free to accept the next instruction.

If a simultaneous instruction is staticized and SMDI is on, the instruction is not transferred to the Simultaneous Mode, but is executed in the Normal Mode.

If a simultaneous instruction is staticized and SMDI is not on, but the system is not equipped with a Simultaneous Mode Control Unit, the instruction will be skipped.

If a simultaneous instruction is staticized and SMDI is not on, but the Simultaneous Mode is occupied, the simultaneous instruction will hold off in the Normal Mode until the Simultaneous Mode is free; i.e., the simultaneous instruction will occupy the Normal Mode, but will not be executed therein. When the Simultaneous Mode becomes free, the instruction will be transferred to the Simultaneous Mode to be executed there, freeing the Normal Mode for the next instruction.

All instructions will be executed serially and will take place in the mode desired when,

1. A System is equipped with a Simultaneous Mode Control Unit.
2. SMDI is not on.
3. ISIM (Inhibit Simultaneity) button on the Console Panel is on.

If a parity error occurs while a Simultaneous Mode input/output instruction is being executed, the mode in which the error occurred is stopped immediately and the instructions presently being executed in the other modes are completed before the computer halts. If the error occurs in the Simultaneous Mode, the SAL (Simultaneous Alarm) light will be on as well as another error light which will indicate the type of error.

Operation of the Data Record File Mode

The following instructions are designed to operate in the Record File Mode:

Record File Mode Read
Record File Mode Write

All instructions are staticized in the Normal Mode. When any one of the above instructions is staticized, provided the system is equipped with a Record File Mode Control Unit, and it is free (i.e., some other instruction is not

progressing in the Record File Mode) then the Record File Mode instruction is transferred to the Record File Mode (i.e., the contents of the NOR Register are transferred to FOR, the contents of the N Register are transferred to the L Register, the contents of the A Register are transferred to the U Register, and the contents of the B Register are transferred to the V Register). The instruction is then executed in the Record File Mode with FOR, L, U and V Registers acting as the NOR, N, A and B Registers respectively. The instruction is then processed similarly to a normal instruction.

Immediately upon the transfer of an instruction from the Normal to the Record File Mode, the Normal Mode is free to accept the next instruction.

If a Record File Mode instruction is staticized and the system is not equipped with a Record File Mode Control Unit, the instruction will be skipped.

If a Record File Mode instruction is staticized and the Record File Mode is occupied, the Record File Mode instruction will hold off in the Normal Mode until the Record File Mode is free; i.e., the Record File Mode Instruction will occupy the Normal Mode, but will not be executed therein. When the Record File Mode becomes free, the instruction will be transferred to the Record File Mode for execution, freeing the Normal Mode for the next instruction.

Device Busy Hold-Off

As soon as an input/output instruction is staticized regardless of the mode in which it is to be executed, it senses the input/output device it must use. If the device is busy, the instruction holds off in the Normal Mode until the device is free.

Independent Operations

The following operations are independent operations:

Band selection
Track selection
Rewinding tapes
Paper advancing

Regardless of the mode in which the instructions causing these functions are executed, once any one of these functions is initiated, it continues independent of the Computer. The instruction, then, is considered by the Computer circuitry to have completed itself upon the initiation of the function, and the mode which the instruction occupied is thereby freed for immediate use.

In a system equipped with both the Simultaneous Mode Control Unit and the Record File Mode Control Unit, it is possible to have one instruction progressing in the Simultaneous Mode, another instruction progressing in the Record File Mode, and still another instruction progressing in the Normal Mode and any number of independent operations in progress, all simultaneously.

If a parity error occurs while a Record File Mode instruction is being executed the mode in which the error occurred is stopped immediately and the instructions presently being executed in the other modes are completed before the computer halts. If the error occurs in the Record File Mode, the FAL (Record File Alarm) light will be on as will another error light which will indicate the type of error.

Time Sharing

Simultaneity in the RCA 301 System is accomplished through a technique known as "time sharing." All input/output instructions need to access the High-Speed Memory for only a fraction of the time they are in progress. For most of their execution times, input/output instructions must wait for some mechanical action in the input/output device to occur (e.g., card movement, tape movement, print drum revolution, etc.).

The nominal time ratios that each input/output instruction must access memory are given in the following table:

Device	Instructions Must Access Memory For	Out of Every
Card Reader, Model 323	13.44 ms	100 ms
Card Reader, Model 324	1.12 ms	66.7 ms
Card Reader, Model 329	1.12 ms	40.5 ms
Card Reader-Punch, Model 330		
Reader Unit	13.44 ms	75 ms
Punch Unit	6.72 ms	240 ms
Card Punch (100 cpm), Model 334	6.72 ms	600 ms
Card Punch (200 cpm), Model 336	13.44 ms	300 ms
Paper Tape Reader (1000 cps), Model 322	7 μs	1 ms
Paper Tape Read or Punch (100 cps), Model 321, 331	7 μs	10 ms
Paper Tape Punch (300 cps), Model 332	7 μs	3.3 ms
Printer—Unbuffered:		
120 Column Synchronous Mode	20.069 ms	60 ms
120 Column Asynchronous Mode	27.328 ms	76 ms
160 Column Synchronous Mode, full speed	26.649 ms	55.8 ms
160 Column Asynchronous Mode, full speed	36.288 ms	71.8 ms
160 Column Synchronous Mode, reduced speed	26.649 ms	83.9 ms
160 Column Asynchronous Mode, reduced speed	36.288 ms	100 ms
Printer—Buffered:		
120 Column Synchronous Mode	1.288 ms	60 ms
120 Column Asynchronous Mode	1.288 ms	76 ms
160 Column Synchronous Mode, full speed	1.568 ms	55.8 ms
160 Column Asynchronous Mode, full speed	1.568 ms	71.8 ms
160 Column Synchronous Mode, reduced speed	1.568 ms	83.9 ms
160 Column Asynchronous Mode, reduced speed	1.568 ms	100 ms
Monitor Printer, Model 338	7 μs	100 ms
Data Record File, Model 361	7 μs	400 μs
Data Disc File, Model 363	7 μs	62.5 μs
Hi-Data Magnetic Tape—Read Write (Model 381)	7 μs	100 μs
Hi-Data Magnetic Tape—Read Write (Model 382)	7 μs	33 μs
33.3 KC Magnetic Tape-Read Write	7 μs	30 μs
66.7 KC Magnetic Tape-Read Write	7 μs	30 μs
Multiple Tape Lister, Model 340		
Print One Tape	350 μs	30 ms
Print Two Tapes	686 μs	30 ms

In the RCA 301 System, then, the HSM is time shared; i.e., during the time that an input/output instruction is in progress, but is not using memory, another input/output instruction and/or compute instruction can use the memory.

THE CONSOLE

Register Display

When the computer is not running, no register is displayed. To display a register, it must be selected. To change the contents of a register, it must be selected and then the proper bits (buttons) depressed. These buttons which display the contents of a selected register are the rightmost bank in Figure 6 illustrating the layout of the buttons on the console.

REGISTER SELECTION

Depressing one of the select buttons will cause the display of a register. The registers that can be selected are:

P, A, B, S, T, U, V — four characters in length.

NOR/N, SOR/M, FOR/L — two characters displayed; one is the operation code, the other the N Register or its corresponding registers in the other modes.

MR — Memory Register — two characters.

D — D Register — two characters.

SPECIAL PURPOSE SWITCHES

These are alternate action switches.

1. OCSP — (One Cycle Stop)
   This switch permits "one status level at a time" operation by stopping the computer at the end of every status level.
2. ICSP — (Instruction Complete Stop)
   Permits "one instruction at a time" operation by stopping the computer prior to the staticizing of the next instruction.
3. FPLS — (First Processing Level Stop)
   Stops the computer after staticizing an instruction.
4. RDM — (Read Memory)
   Allows the displaying of any diad in HSM.
5. WRM — (Write Memory)
   Allows the placing of a diad into two locations in HSM.
6. HSMI — (HSM Inhibit)
   Inhibits information from going to or coming from HSM.
7. BAI — (Bus Adder Inhibit)
   Adding or subtracting ability of the Bus Adder is inhibited. Output of the Bus Adder is the same as the input.
8. STLR — (Status Level Repeat)
   Inhibits changing the current status level.
9. ISIM — (Inhibit Simultaneity)
   Causes all instructions to be executed serially although they take place in the mode desired.
10. BCT — (Bypass Card Translation)
    Bypasses the automatic card translation in the card read instruction. Two characters for each column read will be placed in HSM.
11. INT — (Interrupt)
    This button can be sensed by the CTC instruction when N = &.
12. WTAB — (Write to Table)
    When set, this switch allows the arithmetic tables (HSM locations 0000-0199) to be written into HSM. When reset, any attempt to write to the tables will cause an alarm.
13. SMDI — (Simultaneous Mode Inhibit)
    When set, causes all Simultaneous Instructions to be performed in the Normal Mode. It also will store the A Register to STA when the S Register is indicated in the Store Register instruction. If an EF/ED is read, the Normal EF/ED indicator will be set.
14. ALI — (Alarm Inhibit)
    When this switch is depressed the Computer will not stop on any error condition. The alarm indicator, however, will light.

STATUS LEVEL SELECTION (STL)

To select a status level its proper bit configuration must be placed in the buttons 2^6 to 2^0 in the second bank.

Alarm Indicators

PARITY ERRORS

The following errors indicate incorrect parity in the associated register(s):

1. SORM — (Simultaneous Operation or M Registers)
2. NORN — (Normal Operation or N Registers)
3. FORL — (V or L Registers)
4. NRPE — (Repeat Register)
5. MAPE — (Memory Address Register)
6. MRPE — (Memory Register)
7. DPE — (D Register)
8. STLE — (Status Level)

OTHER ERRORS

1. COME — Error in the Comparator.
2. ARIE — Arithmetic Error caused by one of the following:

   Processor with 10,000 or 20,000 character memory:

   a. 2^4 bit is a "one" in MSD of both operands in an Add instruction.
   b. 2^4 or 2^5 bit is a "one" in other than MSD or LSD of either operand.
   c. 2^4 bit is a "one" in the MSD of one of the operands and there is a carry.

   Processor with 40,000 character memory:

   a. 2^4 or 2^5 bit is a "one" in other than the MSD or LSD of either operand.
   b. 2^5 and 2^4 are "one's" in the MSD of both operands and there is a carry.
   c. 2^5 is a "one" in the MSD of both operands.
   d. 2^5 is "one" in the MSD of one operand and 2^4 is a "one" in the MSD of the other operand and there is a carry.
3. WTT — attempted to write to arithmetic table (HSM location — 0000-0199) with WTAB reset.
4. DDF — (Device Does Not Follow)
   The device addressed is inoperable.
5. RE — (Read Error)
   An error has occurred during a "read" instruction or when data is transferred from HSM to the printer output buffer.
6. TAE — (Tape Address Error)
   Parity error in the tape address.
7. CCE — (Card Compare Error)
   The second read station does not compare with the first read station on the Card Reader; or the read station does not compare with the punch on the Card Punch.
8. WE — (Write Error)
   An error has occurred during a "write" instruction or when data is transferred between the Memory Register and an input or output buffer.
9. MCP — (Missing Clock Pulse)
   This is an error on the 33.3 or 66.7 KC Tape Stations.
10. SAL — (Simultaneous Alarm)
    An input/output alarm has occurred and the instruction was in the Simultaneous Mode. When this light is on, another one will also light to indicate the type of error.
11. MPE — (Multipunch Error)
    A non-301 character has been recognized on a card read with the BCT switch off.
12. CIG — (Character in the Gap)
    A block of less than 3 characters has been read.

13. RAE — (Record File Address Error)
    Parity error in the Record File Address Register.
14. FAL — (Record File Alarm)
    An error has occurred in an instruction in the Record File Mode.

MISCELLANEOUS

1. SB — Indicates Simultaneous Mode Busy.
2. FB — Indicates Record File Mode Busy.
3. Power Off — Will turn off power. It is not possible to turn power on from the console. This must be done at the Power Supply.
4. GEN RES — General Reset — Resets all registers and counters and the majority of flip-flops. It sets up the first status level (P1).
5. START — Used to execute status level displayed.
6. All buttons having diamond configurations are reset buttons.

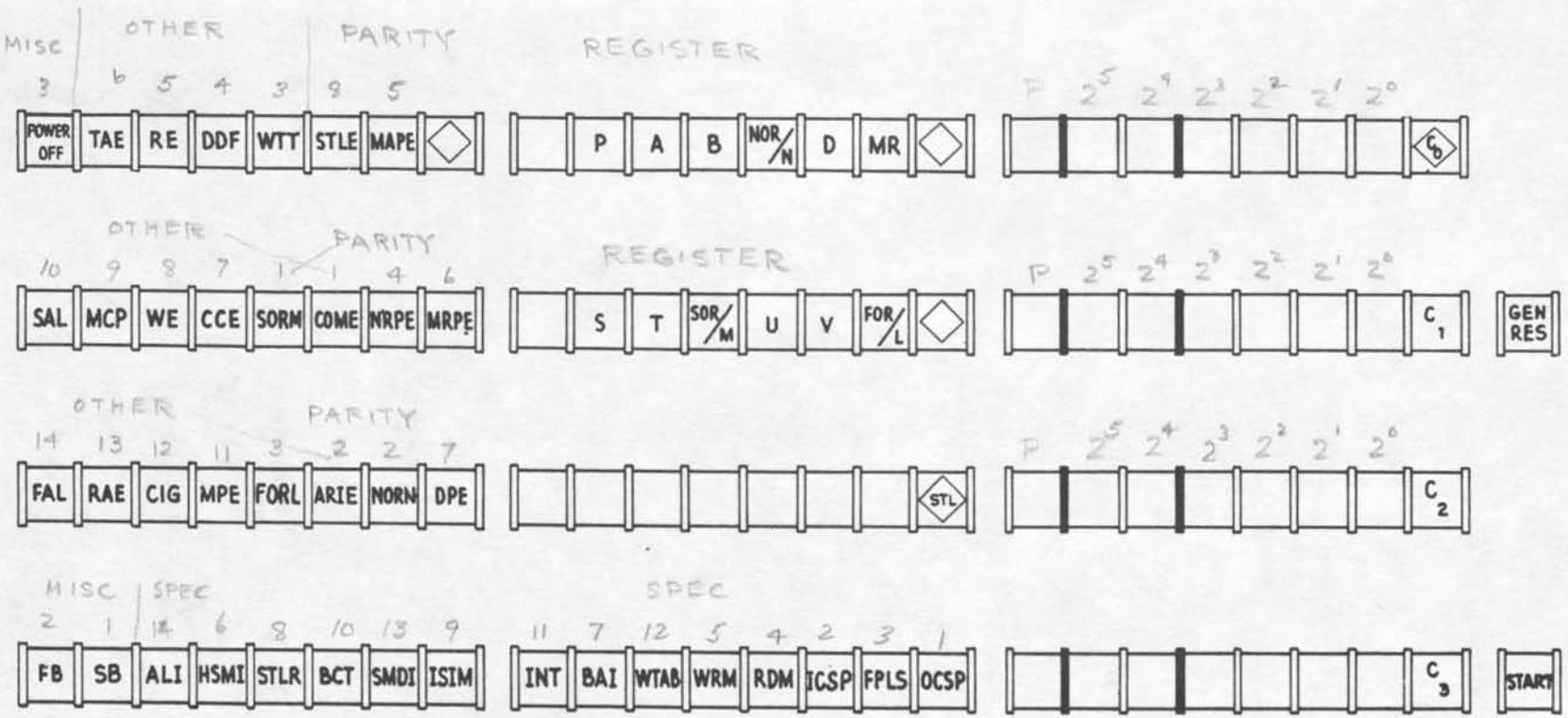


Figure 6—RCA 301 Console Display

IV — GENERAL DESCRIPTION

INTRODUCTION

The RCA 301 Computer operates under the direction of two-address instructions. For descriptive purposes, these instructions may be classified into four general categories: (1) Input/Output, (2) Data Handling, (3) Arithmetic and (4) Decision and Control.

Input/Output Instructions

These instructions enable the Computer to communicate with the peripheral devices. They perform the functions of positioning or searching tapes or disc files, bringing data from an input medium into the computer or sending data from the computer to an output medium.

In the group, certain operations can be executed in the Simultaneous Mode as well as in the Normal Mode, so that operational time for these instructions can overlap that of other instructions. In addition, several instructions can be executed in the Record File Mode.

Rewind to BTC, Band Select and Track Select instructions as well as the paper advance function are initiated by the Computer, but once underway, operate completely independent of the Computer. Any number of tapes may be rewinding while three instructions (unrelated to the rewinding tapes) are being simultaneously executed.

Data Handling Instructions

These are non-arithmetic instructions for manipulation of data stored in the High-Speed Memory. The instructions included in this group permit operational control by symbol, address, or count. The major data handling functions operate from right to left or left to right according to the specific instruction involved.

Arithmetic Instructions

Of the instructions in this group, two are decimal, and three are used to alter the bit configuration of an operand through the use of logical operations.

The decimal instructions operate in accordance with algebraic rules and are designed to handle operands of equal length.

Three instructions, Logical "OR", Logical "AND" and Exclusive "OR" constitute what may be considered as a separate arithmetic category. They are used to alter the bit configuration of an operand by the employment of a second operand to "mask-out" or to insert "1" bits.

The Previous Result Indicators (PRI's) preserve the sign of the result of an arithmetic instruction for reference by a subsequent decision instruction.

Decision and Control Instructions

These instructions influence the sequence of operation. Three instructions enable the programmer to address registers directly and one instruction is conditional; that is, it chooses a path according to selected conditions. One instruction stops the Computer operation. The "Repeat" instruction enables the Computer to execute the same instruction a designated number of times. The Compare instruction enables the Computer to determine the relative magnitude of two operands of equal length.

Description of Instructions

Information pertaining to each instruction is described under the headings as given below. Special explanation for some of these is also included.

Instructive Symbol (OP Code)
Name and Abbreviation of Instruction
Repeatable (if applicable)
General Description
Format of Instruction
Direction of Operation
Standard Location, if used
Outline of Operation
Final Registers Contents
PRI settings (where applicable)
Timing
Example

DIRECTION OF OPERATION

A Direction of Operation subsection appears in all applicable instructions and defines the direction of operation in HSM.

OPERATION

An Outline of Operation subsection supplements the General Description prefacing the instruction. Internal logic is described not in every detail, but only to the extent that it contributes to the attainment of the objectives of a programmers' reference manual: (1) to help the programmer gain a better understanding of Computer operation, (2) to permit the programmer to modify the instructions and their application for individual problem solution and (3) to enable the programmer to develop advanced programming techniques.

TIMING

Due to the variable item length concept in the RCA 301 System, instruction times can be expressed only as a function of the number of characters involved in a given operation. For example, the time required to write out to tape depends on the number of characters to be written, and the time required to add two numbers together depends on the number of digits in the operands.

The time, or timing formula, listed for each instruction includes staticizing time, and STA or STP where applicable. Indirect addressing requires an additional 14 microseconds per indirect address.

Each time a repeatable instruction is repeated there are three additional status levels (21 microseconds) required when the contents of the N_R (REPEAT) Register exceed zero, and one additional status level (7 microseconds) when the N_R (Repeat) Register contents are zero.

EXAMPLES

Wherever possible, the examples that accompany the instruction include representation of the unaffected portion or portions of the High-Speed Memory. The content of the HSM locations are shown by bit values in some of the instructions and as alphanumeric characters in other instructions.

In each example, the subheading "HSM before Instruction is Executed" is to be interpreted as before execution but after staticizing. The contents of the memory locations are not affected by staticizing. The initial register settings of A_1, B_1, T_1, S_1 however, reflect register contents after staticizing.

V — DATA HANDLING INSTRUCTIONS

A Translate By Table (TRA)

Repeatable

General Description

This instruction translates a specified number of characters in an area from one code to another by the use of a translate table. It may be used to translate from one to forty-four characters in memory.

Format

Operation — A
N — number (0-44) of characters to be translated. (See Appendix F-I.)
A Address — HSM location of leftmost character to be translated and result area.
B Address — HSM location of first character of translate table (must end in 00).

Direction of Operation

Left to right.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the contents of the A Register is transferred to the D Register as follows: 2^2, 2^1, and 2^0 bits are transferred to corresponding positions in D_3; 2^5, 2^4, and 2^3 bits are transferred to the 2^2, 2^1, and 2^0 positions, respectively, of D_2; the remaining bits in the D Register are zeros, except parity bits, which are generated properly. The contents of B_0, B_1, D_2, and D_3 are used to address the translate table. The character is read out of the translate table and transferred to the HSM location specified by the contents of the A Register. The contents of the A Register are incremented by one. N is decremented by one and the cycle is repeated.

Final Register Contents

$(A)_f$ = HSM character location one to the right of the last character translated.
$(B)_f = (B)_i$

Timing

Total time in microseconds
= 21n + 35 where n = number of characters to be translated.

Example:

Instruction:

Operation	N	A Address	B Address
A	5	4053	6300

HSM before the Instruction is Executed

4050	4051	4052	4053	4054	4055	4056	4057	4058
1	2	5	7	3	6	4	8	9

Table: (Partial)

	0	1	2	3	4	5	6	7	8	9
630	Z	A	B	C	D	E	F	G		
631	H	I	J	K	L	M	N	O		

HSM after the Instruction

4050	4051	4052	4053	4054	4055	4056	4057	4058
1	2	5	G	C	F	D	H	9

Final Register Contents:

$A_t = 4058$
$B_t = 6300$

Time:

21 (5) + 35 = 140 μs.

K Locate Symbol Left (LSL)

General Description

This instruction searches through the contents of successive HSM locations between and including, two specified addresses. The operation ceases when the rightmost location is reached or upon detecting a non-selected symbol.

Format

Operation — K.
N — Selected symbol.
A Address — Leftmost HSM location to be searched.
B Address — Rightmost HSM location to be searched.

Direction of Operation

Left to right.

Standard Location

STA (0212-0215)

Outline of Operation

This instruction initially sets PRZ, and operates in the following cycle:

The contents of the A Register are placed in the Memory Address Register. The contents of the A Register are compared with the contents of the B Register and if this comparison proves equal ABE (A-B Equality) is set; if the comparison proves unequal ABE is not set. The contents of the A Register are incremented by one.

The contents of the HSM location specified by the Memory Address Register are compared with the contents of the N Register.

(1) If this comparison proves unequal, and the contents of the Memory Address Register are equal to A_1, PRN is set, the contents of the A Register are decremented by two, and the instruction terminates.

(2) If this comparison proves unequal, and the contents of the Memory Address Register are not equal to A_1, PRP is set, the contents of the A Register are decremented by two, and the instruction terminates.

(3) If this comparison proves equal and ABE is set, the contents of the A Register are decremented by one, and the instruction terminates.

(4) If this comparison proves equal and ABE is not set, the cycle is repeated.

Final Register Contents

If a character is found not equal to N

$(A)_f$ = One HSM address to the left of that character.
$(B)_f = (B)_i$

If all characters searched are equal to the contents of N

$(A)_f = (B)_i$
$(B)_f = (B)_i$

PRI

PRN is set when the first character searched is not equal to the contents of N.
PRZ is set when all characters searched are equal to the contents of N.
PRP is set if a non-selected symbol is found in the specified HSM area after a character equal to the contents of N has been found.

Timing

Total time in microseconds
$= 14n + 56.$
n = number of characters searched.

Example #1

Instruction:

Operation	N	A Address	B Address
K	0	1000	1009

HSM before and after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
0	0	0	0	0	1	0	3	0	9

Final Register Contents:

$(A)_f = 1004$

$(B)_f = 1009$

PRI

PRP is set

Time:

$14\ (6) + 56 = 140\ \mu s.$

Example #2

Instruction:

Operation	N	A Address	B Address
K	sp	2010	2019

HSM before and after Instruction is Executed:

2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
sp	sp	sp	sp	sp	sp	sp	sp	sp	sp

Final Register Contents:

$A_f = 2019$

$B_f = 2019$

PRI

PRZ is set

Time:

$14\ (10) + 56 = 196\ \mu s.$

Example #3

Instruction:

Operation	N	A Address	B Address
K	O	3278	3284

HSM before and after Instruction is Executed:

3278	3279	3280	3281	3282	3283	3284
3	2	7	9	0	0	0

Final Register Contents:

$A_f = 3277$

$B_f = 3284$

PRI

PRN is set

Time:

$14\ (1) + 56 = 70\ \mu s.$

L Locate Symbol Right (LSR)

General Description

This instruction searches through the contents of successive HSM locations between, and including, two specified addresses. The operation ceases when the leftmost location is reached or upon detecting a non-selected symbol.

Format

Operation — L.
N — Selected Symbol.
A Address — Rightmost HSM location to be searched.
B Address — Leftmost HSM location to be searched.

Direction of Operation

Right to left.

Standard Location

STA (0212-0215)

Outline of Operation

This instruction initially sets PRZ, and operates in the following cycle:

The contents of the A Register are placed in the Memory Address Register. The contents of the A Register are compared with the contents of the B Register and if this comparison proves equal ABE (A-B Equality) is set; if the comparison proves unequal, ABE is not set. The contents of the A Register are decremented by one.

The contents of the HSM location specified by the Memory Address Register are compared with the contents of the N Register.

(1) If this comparison proves unequal, and the contents of the Memory Address Register are equal to A_i, PRN is set, the contents of the A Register are incremented by two, and the instruction terminates.
(2) If this comparison proves unequal, and the contents of the Memory Address Register are not equal to A_i, PRP is set, the contents of the A Register are incremented by two, and the instruction terminates.
(3) If this comparison proves equal and ABE is set, the contents of the A Register are incremented by one, and the instruction terminates.
(4) If this comparison proves equal and ABE is not set, the cycle is repeated.

Final Register Content

If a character is found not equal to N

$(A)_f$ = One HSM address to the right of that character
$(B)_f = (B)_i$

If all characters searched are equal to the contents of N

$(A)_f = (B)_i$
$(B)_f = (B)_i$

PRI

PRN is set if the first character searched is not equal to the contents of N.
PRZ is set when all characters searched are equal to the contents of N.
PRP is set when a non-selected symbol is found in the specified HSM area after a character equal to the contents of N has been found.

Timing

Total time in microseconds
$= 14n + 56$
n = number of characters searched.

I. Morris CSCP

L. Morris CSCW

Example

Instruction:

Operation	N	A Address	B Address
L	—	1009	1000

HSM before and after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
1	0	3	0	9	—	—	—	—	—

Final Register Content:

$(A)_t = 1005$

$(B)_t = 1000$

PRI

PRP is set

Time

$14\ (6) + 56 = 140\ \mu s.$

M Transfer Data Left (DL)

Repeatable

General Description

This instruction transfers a specified number of consecutive characters from one HSM area to another HSM area. It may be used to transfer from one to forty-four characters in memory.

Format

Operation — M
N — 0-44 characters to be transferred. (See Appendix F-I.)
A Address — HSM location of leftmost character to be transferred.
B Address — Destination address of first character.

Direction of Operation

Left to right.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The contents of the A and B Registers are incremented by one, the contents of the N Register are decremented by one, and the cycle is repeated.

Final Register Contents

$(A)_f$ = Address location one to the right of the last character transferred.
$(B)_f$ = Address location one to the right of the last destination address.

Timing

Total time in microseconds
= 14n + 35, where n equals the number of characters transferred.

Example

Instruction:

Operation	N	A Address	B Address
M	5	1000	1006

HSM before Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011
A	B	A	T	E	—	—	—	—	—	—	—

HSM after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011
A	B	A	T	E	—	A	B	A	T	E	—

Final Register Setting:

$(A)_f = 1005$
$(B)_f = 1011$

Time:

$(14 \times 5) + 35 = 105\ \mu s.$

N Transfer Data Right (DR) — Repeatable

General Description

This instruction transfers a specified number of consecutive characters from one HSM area to another. It may be used to transfer from one to forty-four characters in memory.

Format

Operation — N
N — 0-44 characters to be transferred. (See Appendix F-I.)
A Address — HSM location of rightmost character to be transferred.
B Address — Destination address of first character.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The contents of the A and B Registers are decremented by one, the contents of the N Register are decremented by one, and the cycle is repeated. The A address and the B address will be staticized although N may equal zero.

Final Register Contents

$(A)_f$ = Address of location one to the left of the last character transferred.
$(B)_f$ = Address of location one to the left of the last destination location.

Timing

Total time in microseconds.
= 14n + 35, where n equals the number of characters transferred.

Example

Instruction:

Operation	N	A Address	B Address
N	4	1003	1009

HSM before Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
B	0	0	K	—	—	—	—	—	—

HSM after Instruction is Executed:

1000	1001	1002	1003	1004	1005	1006	1007	1008	1009
B	0	0	K	—	—	B	0	0	K

Final Register Settings:
$(A)_f = 0999$
$(B)_f = 1005$

Time:
$(4 \times 14) + 35 = 91\ \mu s.$

Transfer Data By Symbol Left (DSL)

Repeatable

General Description

This instruction transfers data terminated by a selected symbol from one HSM location to another.

Format

Operation — #
N — Selected symbol on which to stop transferring.
A Address — HSM location of leftmost character to be transferred.
B Address — Destination address of first character.

Direction of Operation

Left to right

Standard Location

STA (0212-0215)

Outline of Operation

This instruction operates in the following cycle:

The contents of the HSM locations specified by the A Register are compared with the contents of the N Register. The character specified by the A Register is transferred to the HSM location specified by the B Register and the contents of the A and B Registers are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(A)_f$ = HSM address location one to the right of the specified symbol in the original area.
$(B)_f$ = HSM address location one to the right of the symbol in the destination area.

Timing

Total time in microseconds.
= 14n + 49, where n equals the number of characters being transferred.

Example

Instruction:

Operation	N	A Address	B Address
#	"	2000	2007

HSM before Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
$	4	3	2	"	—	—	—	—	—	—	—	—

HSM after Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
$	4	3	2	"	—	—	$	4	3	2	"	—

Final Register Contents:

$(A)_f$ = 2005
$(B)_f$ = 2012

Time:

(5 x 14) + 49 = 119 μs.

P Transfer Data By Symbol Right (DSR) — Repeatable

General Description

This instruction transfers data terminated by a selected symbol from one HSM location to another.

Format

Operation — P
N — Selected symbol on which to stop transferring.
A Address — HSM location of rightmost character to be transferred.
B Address — Destination address of first character.

Direction of Operation

Right to left.

Standard Location

STA (0212-0215)

Outline of Operation

This instruction operates in the following cycle:

The contents of the HSM location specified by the A Register are compared with the contents of the N Register. The character specified by the A Register is transferred to the HSM location specified by the B Register and the contents of the A and B Registers are decremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(A)_f$ = HSM address of location one to the left of the specified symbol in the original area.
$(B)_f$ = HSM address of location one to the left of the symbol in the destination area.

Timing

Total time in microseconds
= 14n + 49, where n equals the number of characters being transferred.

Example

Instruction:

Operation	N	A Address	B Address
P	"	3008	3003

HSM before Instruction is Executed:

2999	3000	3001	3002	3003	3004	3005	3006	3007	3008
—	—	—	—	—	"	$	4	3	2

HSM after Instruction is Executed:

2999	3000	3001	3002	3003	3004	3005	3006	3007	3008
"	$	4	3	2	"	$	4	3	2

Final Register Contents:
$(A)_f = 3003$
$(B)_f = 2998$

Time:
$(5 \times 14) + 49 = 119\ \mu s.$

J Transfer Symbol To Fill (SF)

General Description

This instruction inserts a selected symbol into each HSM location between and including the two given addresses.

Format

Operation — J
N — Selected Symbol
A Address — Leftmost location in memory to be filled.
B Address — Rightmost location in memory to be filled.

Direction of Operation

Left to right.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. If this comparison proves equal, the contents of the A Register are incremented by one and the instruction terminates. If the operation proves unequal, the contents of the A Register are incremented by one, and the cycle is repeated.

Final Register Contents

$(A)_f = (B)_i + 1$
$(B)_f = (B)_i$

Timing

Total time in microseconds
$= 7n + 35$, where n equals the number of locations filled.

Example

Instruction:

Operation	N	A Address	B Address
J	0	3001	3009

HSM before Instruction is Executed:

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009	3010
J	—	S	M	I	T	H	—	—	I	I

HSM after Instruction is Executed:

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009	3010
J	0	0	0	0	0	0	0	0	0	I

Final Register Contents:

$(A)_f = 3010$
$(B)_f = 3009$

Time:

$(9 \times 7) + 35 = 98\ \mu s.$

VI — ARITHMETIC INSTRUCTIONS

+ Add (ADD)

Repeatable

General Description

This instruction performs decimal addition in accordance with algebraic rules, providing a non-zero suppressed sum, which is stored in the memory location originally occupied by the augend. The two operands must be equal in length, but may be of any length up to forty-four characters per each operand.

Format

Operation — +
N — Number of characters (0-44) in each operand. (See Appendix F-I.)
A Address — HSM location of least significant digit of augend and sum.
B Address — HSM location of least significant digit of addend.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are transferred to the D_2 portion of the D Register; the contents of the HSM location specified by the B Register are transferred to the D_3 portion of the D Register. The contents of the D Register are used to generate an address in the Sum or Difference Table located in HSM depending on the sign in each operand. If the signs of the operands are alike, the Sum Table is addressed; if unlike, the Difference Table is addressed. The character thus addressed is transferred to the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the cycle is repeated.

The sign of each operand does not require a separate character location, but is indicated by the 2^5 bit of the least significant digit (LSD) of each operand. When a one bit is present in the 2^5 position, the sign is negative. Otherwise it is assumed positive.

In the event there is a carry beyond the most significant digit (MSD) of the sum, a one bit is placed in the 2^4 bit position of the MSD of the sum and the first Overflow Indicator, which is present in all Processors, is set. In a Processor with a 40,000 character memory there may be an additional overflow carry from the 2^4 to the 2^5 position of the MSD of the sum and a second Overflow Indicator set. The 2^4 and 2^5 bit positions of the MSD of the sum then act as a two bit binary counter. Each Overflow Indicator can be sensed by the Conditional Transfer of Control instruction.

When there is a carry beyond the MSD of the sum, and the first Overflow Indicator has already been set in a Computer containing only one Overflow Indicator, the Computer stops on an alarm. When there is a carry beyond the MSD of the sum in a Computer with a second Overflow Indicator and this indicator has already been set, the Computer stops on an alarm.

The only allowable one zone bits in the operands of an addition for a processor with up to 20,000 characters are in the 2^4 bit position of the MSD and the 2^4 and 2^5 positions in the LSD. The only allowable one zone bits in the operands of an addition for a processor with 40,000 characters are the 2^4 and 2^5 bit positions in the MSD and the LSD.

In single character operands, however, a one bit in the 2^4 position of either operand causes an alarm stop on the 40,000 character processor.

If the operands have unlike signs and the larger, in absolute value, is the addend, then this causes the "end around condition" when N equals zero. By the use of the Difference Table, the sum is complemented to give the correct result.

When the ADD instruction is used for address modification, the following special conditions apply:

1. If an indirect address is indicated by a one in the 2^4 bit position of the LSD of either operand, a one is generated in the 2^4 position of the LSD of the sum.
2. Addresses must always be positive.
3. If the result of address addition is greater than 20,000 in a processor containing up to a 20,000 character memory, an alarm stop occurs.
4. If the result of address addition is greater than 40,000 in a processor with a 40,000 character memory, an alarm stop occurs.

Final Register Contents

$(A)_t$ = HSM address of location one to the left of the MSD of the sum.
$(B)_t$ = HSM address of location one to the left of the MSD of the addend.

PRI

PRP is set if the sum is positive.
PRZ is set if the sum is zero.
PRN is set if the sum is negative.

Timing

Total time in microseconds
= 28n + 49, where n is the number of characters in either operand (operands must be of equal lengths).
If an "end around condition" exists, 21n + 14 microseconds must be added to the above.

Example

Instruction:

Operation	N	A Address	B Address
+	5	1006	1012

HSM before Instruction is Executed:

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
A	0	1	1	8	2	B	5	4	3	2	1

HSM after Instruction is Executed:

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
A	5	5	5	0	3	B	5	4	3	2	1

Final Register Contents:
$(A)_t = 1001$
$(B)_t = 1007$

PRI
PRP is set.

Time:
28 (5) + 49 = 189 μs.

Example #2

Instruction:

Operation	N	A Address	B Address
+	4	2018	2023

HSM before the Instruction is Executed:

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
—	2	4	5	7	—	3	2	6	K	—

HSM after Instruction is Executed:

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
—	0	8	0	N	—	3	2	6	K	—

Final Register Contents:

$(A)_t = 2014$

$(B)_t = 2019$

PRI

PRN is set.

Time: (End around condition)

$28\ (4) + 49 + 21\ (4) + 14 = 259\ \mu s.$

Example #3

Instruction:

Operation	N	A Address	B Address
+	3	3356	3352

HSM before Instruction is Executed:

3349	3350	3351	3352	3353	3354	3355	3356	3357
—	3	2	6	—	8	5	1	—

HSM after the Instruction is Executed:

3349	3350	3351	3352	3353	3354	3355	3356	3357
—	3	2	6	—	A	7	7	—

First Overflow Indicator is set

Final Register Contents:

$(A)_t = 3353$

$(B)_t = 3349$

PRI

PRP is set.

Time:

$28\ (3) + 49 = .33\ \mu s.$

— Subtract (SUB) Repeatable

General Description

This instruction performs decimal subtraction in accordance with algebraic rules producing a non-zero suppressed difference which is stored in the memory location originally occupied by the minuend. The two operands must be equal in length, but of any length up to forty-four characters for each operand.

Format

Operation — (minus)
N — Number (0-44) of characters in each operand. (See Appendix F-I.)
A Address — HSM location of least significant digit of the minuend and the difference.
B Address — HSM location of least significant digit of the subtrahend.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are transferred to the D_2 portion of the D Register; the contents of the HSM location specified by the B Register are transferred to the D_3 portion of the D Register. The contents of the D Register are used to generate an address in the Sum or Difference Table located in HSM depending on the sign in each operand. If the signs of the operands are alike, the Difference Table is addressed; if unlike the Sum Table is addressed. The character thus addressed is transferred to the HSM location specified by the A Register. The contents of the A, B, and N Register are decremented by one and the cycle is repeated.

The sign of each operand does not require a separate character location, but is indicated by the 2^5 bit of the least significant digit (LSD) of each operand. When a one bit is present in the 2^5 position, the sign is negative. Otherwise it is assumed positive.

In the event there is a carry beyond the most significant digit (MSD) of the result, a one bit is placed in the 2^4 bit position of the MSD of the result, and the first Overflow Indicator, which is present in all Processors, is set. In a processor with a 40,000 character memory, there may be an additional overflow carry from the 2^4 to the 2^5 bit position of the MSD of the result, and a second Overflow Indicator set. The 2^4 and 2^5 bit positions of the MSD of the result then act as a two bit binary counter. Each Overflow Indicator can be sensed by the Conditional Transfer of Control instruction.

When there is a carry beyond the MSD of the result; and the first Overflow Indicator has already been set in a computer containing only one Overflow Indicator, the computer stops on an alarm. When there is a carry beyond the MSD of the result in a computer with a second Overflow Indicator and this indicator has already been set, the computer stops on an alarm.

The only allowable one zone bits in the operands of a subtraction for a processor with up to 20,000 characters, are in the 2^4 bit position of the MSD and the 2^4 and the 2^5 bit positions of the LSD. The only allowable one zone bits in the operands of a subtraction, for a processor with 40,000 characters, are the 2^4 and 2^5 bit positions in the MSD and the LSD.

In single character operands, however, a one bit in the 2^4 position of either operand causes an alarm stop in a 40,000 character processor.

If the operands have like signs, and the larger, in absolute value, is the subtrahend, then this causes the "end around condition" when N equals zero. By the use of the Difference Table, the difference is complemented to give the correct result.

When the SUBTRACT instruction is used for address modification, the following special conditions apply:

1. If an indirect address is indicated by a one in the 2^4 bit position of the LSD of either operand, a one is generated in the 2^4 position of the LSD of the difference.
2. Both addresses entering the subtraction must be positive.
3. The result must be positive.

Final Register Contents

$(A)_f$ = Address of location one to the left of the MSD of the difference.
$(B)_f$ = Address of location one to the left of the MSD of the subtrahend.

PRI

PRP is set if the result is positive.
PRZ is set if the result is zero.
PRN is set if the result is negative.

Timing

Total time in microseconds
= 28n + 49, where n is the number of characters in either operand (operands must be of equal lengths).
If an "end around condition" exists, 21n + 14 microseconds must be added to the above.

Example

Instruction:

Operation	N	A Address	B Address
—	3	2006	2010

HSM before Instruction is Executed:

2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
A	E	R	9	9	9	3	1	2	3

HSM after Instruction is Executed:

2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
A	E	R	8	7	6	3	1	2	3

Final Register Contents:
$(A)_f$ = 2003
$(B)_f$ = 2007

PRI
PRP is set

Time:
28 (3) + 49 = 133 μs.

Q Logical "OR" (OR) — Repeatable

INSERT BITS

General Description

This instruction is one of three instructions which provides the 301 system with bit manipulation abilities. It operates on equal length operands according to the rules outlined under "Outline of Operation" below.

Format

Operation — Q
N — Number (0-44) of characters in each operand. (See Appendix F-I.)
A Address — HSM location of least significant digit of first operand and result.
B Address — HSM location of least significant digit of second operand.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

Bit in First Operand	*Bit in Second Operand*	*Bit in Result*
0	0	0
0	1	1
1	0	1
1	1	1

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

Example of Rules

(a) 1 00 1001
1 01 0001
0 01 1001

(b) 0 11 0001
0 10 0011
1 11 0011

Final Register Contents

$(A)_f$ = Address of location one to the left of the most significant digit of the result.
$(B)_f$ = Address of location one to the left of the most significant digit of second operand.

Timing

Total time in microseconds
= 21n + 35, where n is the number of characters in either operand (operands must be of equal lengths).

Example

Instruction:

Operation	N	A Address	B Address
Q	2	1003	1005

HSM before Instruction is Executed:

Memory Location	1002	1003	1004	1005
Bits within Each Location	1 00 0000	0 00 0111	0 00 0001	0 01 0101

HSM after Instruction is Executed:

Memory Location	1002	1003	1004	1005
Bits within Each Location	0 00 0001	1 01 0111	0 00 0001	0 01 0101

Final Register Contents:

$(A)_f = 1001$

$(B)_f = 1003$

Time:

$21(2) + 35 = 77\ \mu s.$

T Logical "And" (AND) — Repeatable

General Description

This instruction is one of three instructions which provides the 301 system with bit manipulation abilities. It operates on operands of equal length according to the rules outlined under "Outline of Operation" below.

Format

Operation — T
N — Number (0-44) of characters in each operand. (See Appendix F-I.)
A Address — HSM location of least significant digit of the first operand and the result.
B Address — HSM location of least significant digit of the second operand.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

Bit in First Operand	*Bit in Second Operand*	*Bit in Result*
0	0	0
0	1	0
1	0	0
1	1	1

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

Example of Rules

(a)
```
  1 00 1001
  1 01 0001
-----------
  0 00 0001
```

(b)
```
  0 11 0001
  0 10 0011
-----------
  1 10 0001
```

Final Register Contents

$(A)_f$ = Address of location one to left of the most significant digit of the result.
$(B)_f$ = Address of location one to the left of the most significant digit of second operand.

PRI

PRP is set, if at least one of the information bits in the result is a one.
PRN is set, if all the information bits in the results are zero.

Timing

Total time in microseconds
= 21n + 35, where n is the number of characters in either operand (operands must be of equal length).

Example

Instruction:

Operation	N	A Address	B Address
T	2	1001	1006

HSM before Instruction is Executed:

HSM Location	1000	1001	1002	1003	1004	1005	1006
Bits within Each Location	1 00 0000	1 00 1111	———	———	———	0 00 0111	1 11 0101

HSM after Instruction is Executed:

HSM Location	1000	1001	1002	1003	1004	1005	1006
Bits within Each Location	1 00 0000	1 00 0101	———	———	———	0 00 0111	1 11 0101

Final Register Contents:

$(A)_t = 0999$
$(B)_t = 1004$

PRI

PRP is set.

Time:

21 (2) + 35 = 77 μs.

U Exclusive "OR" (EXO) — Repeatable

General Description

This instruction is one of three instructions which provides the 301 System with bit manipulation abilities. It is executed on operands of equal length according to the rules outlined under "Outline of Operation" below.

Format

Operation — U
N — Number of characters (0-44) in each operand. (See Appendix F-I.)
A Address — HSM location of least significant digit of first operand and result.
B Address — HSM location of least significant digit of second operand.

Direction of Operation

Right to left.

Outline of Operation

This instruction operates in the following cycle:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM location specified by the A Register are combined bit by bit with the contents of the HSM location specified by the B Register. This bit manipulation is combined according to the following rules:

Bit in First Operand	*Bit in Second Operand*	*Bit in Result*
0	0	0
0	1	1
1	0	1
1	1	0

The result of the combination is placed in the HSM location specified by the A Register. The contents of the A, B, and N Registers are decremented by one and the instruction is repeated.

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction.

Example of Rules

(a)
```
  1 10 0111
  1 11 1001
-----------
  1 01 1110
```

(b)
```
  0 01 0101
  0 10 1010
-----------
  1 11 1111
```

Final Register Contents

$(A)_f$ = Address of location one to the left of the most significant digit of the result.
$(B)_f$ = Address of location one to the left of the most significant digit of the operand specified by the B address.

Timing

Total time in microseconds
= 21n + 35, where n is the number of characters in either operand (operands must be of equal length).

Example

Instruction:

Operation	N	A Address	B Address
U	2	1003	1005

HSM before Instruction is Executed:

Memory Location	1002	1003	1004	1005
Bits within Each Location	1 00 0000	0 00 0111	0 11 0010	0 01 0101

HSM after Instruction is Executed:

Memory Location	1002	1003	1004	1005
Bits within Each Location	0 11 0010	1 01 0010	0 11 0010	0 01 0101

Final Register Contents:

$(A)_t = 1001$

$(B)_t = 1003$

Time:

(21) x (2) + 35 = 77 μs.

VII — DECISION AND CONTROL INSTRUCTIONS

V Store Register (REG)

General Description

This instruction places the contents of a specified register P, A, B, S, or U into a HSM location.

Format

Operation — V

N — Register to be stored P, A, B, S, or U. The desired register is specified by the following chart.

Register to be Stored	None	P	A	B	S	U
N	0	1	2	4	8	&

A Address — Address of (right hand diad of a two diad pair) which is to receive the contents of the register specified by N if B, P, S, or U are to be stored. If A is to be stored, the contents of the A Register left by the previous instruction are stored in STA and the A address of this instruction is ignored.

B Address — HSM address of next instruction to be executed if P is being stored. If not P, the B address is zero (0000).

Outline of Operation

The N character is examined in the N Register. If zero the instruction terminates. Otherwise the contents of the designated register are stored appropriately. If the N character selects the P Register, the P Register is stored in the location specified by the A Register and the contents of the B Register are sent to the P Register.

In the event the register selected is B, S, or U, the results are stored in the location designated by the A Register contents. When the B Register is stored, the B address of the instruction is not staticized and the contents of the B Register resulting from the previous instruction are stored. In the case when the A Register is stored, the A address and the B address are not staticized and the contents of the A Register resulting from the previous instruction are stored in the STA standard memory location.

When the S Register is stored, the least significant diad of the S Register is placed in the location specified by the A Register. If a Simultaneous Instruction is being concurrently executed, the contents of the S Register may vary before the most significant diad is stored. The contents of the U Register may also change before being completely stored if a Record File Mode instruction is being concurrently executed.

Final Register Contents

$(A)_f = (A)_i - 2$ if B, P, S, or U is stored; $(A)_f$ of the previous instruction if A Register is stored; $(A)_i$ if N equals zero.

$(B)_f = (B)_i$ if P, S, or U is stored or if N equals zero; if A or B Register is stored, $(B)_f$ of previous instruction.

Timing

49 μs

Example

Instruction:

Operation	N	A Address	B Address
V	4	1005	0000

Assumption — Register B contains 2116 as a result of a prior operation.

HSM before Instruction is Executed:

1001	1002	1003	1004	1005
A	B	C	D	E

HSM after Instruction is Executed:

1001	1002	1003	1004	1005
A	2	1	1	6

Final Register Contents:

$(A)_t = 1003$

$(B)_t = 2116$

Time:

49 μs.

W Conditional Transfer of Control (CTC)

General Description

This instruction senses the PRI's, the EF/ED, Overflow, and Interrupt Indicators, and the Simultaneous Mode. It can choose alternate sets of sequences of instructions.

Format

Operation — W

N — Indicates element to be sensed according to the following chart:

N	Indicator Sensed
0	None
1	PRI's
2	Overflow Indicators
4	Simultaneous Indicator
8	EF/ED Normal Indicator
&	Interrupt Indicator
— (minus)	EF/ED Simultaneous Indicator

A Address — Contains the address of the next instruction if one of the following sets of conditions is true:
N = 1 and PRP set,
N = 2 and the First Overflow Indicator is set,
N = 4 and a "read" is in the Simultaneous Mode,
N = 8 and the EF/ED Normal Indicator is set,
N = & and the Interrupt Indicator is set (INT button on Console Panel is on), or
N = — and the EF/ED Simultaneous Indicator is set.

B Address — Contains the address of the next instruction if one of the following sets of conditions is true:
N = 1 and PRN is set,
N = 2 and neither Overflow Indicator is set,
N = 4 and a "write" is in the Simultaneous Mode,
N = 8 and the EF/ED Normal Indicator is not set,
N = & and the Interrupt Indicator is not set, or
N = — and the EF/ED Simultaneous Indicator is not set.

Standard Location

STP (on Transfer only)

Outline of Operation

The N character is examined in the N Register. The condition is sensed and either the contents of the A or B Register, as indicated above, are transferred to the P Register after the contents of the P Register are transferred to STP. The next instruction in sequence is performed if:

1. N = 0, a register is not being sensed.
2. N = 1, the PRI's are being sensed and PRZ is set.
3. N = 2, the Second Overflow Indicator is being sensed and is set.
4. N = 4, the Simultaneous Mode is being sensed and is found to be unoccupied.

The first Overflow Indicator is set when a one is in the 2^4 bit position of the MSD of the sum. The Second Overflow Indicator (present only in a 40,000 HSM) is set when a one is in the 2^5 bit position of the MSD of the sum.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

49 μs if a transfer of control takes place.
35 μs if no transfer of control takes place.

Y Compare Left (COM)

General Description

This instruction is used to determine the relative magnitude of two operands of equal length. The resulting PRI settings permit alternate sequence of action.

Format

Operation — Y
N — Number (0-44) characters to be compared. (See Appendix F-I.)
A Address — HSM address of leftmost character of first operand.
B Address — HSM address of leftmost character of second operand.

Direction of Operation

Left to right.

Outline of Operation

This instruction initially sets PRZ and operates in the following cycles:

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the contents of the HSM locations specified by the A and B Registers are transferred to the D_2 and D_3 positions of the D Register respectively. The contents of the A and B Registers are incremented by one. The contents of D_2 and D_3 are compared. If the contents of D_2 are greater than the contents of D_3, PRP is set, and the instruction terminates. If the contents of D_3 are greater than the contents of D_2, PRN is set, and the instruction terminates. If the contents of D_2 equal the contents of D_3, the contents of the N Register are decremented by one, and the cycle is repeated.

Final Register Contents

$(A)_f$ = Address of location one to the right of the last character compared in first operand.
$(B)_f$ = Address of location one to the right of the last character compared in second operand.

PRI

PRI set according to outline of operation.

PRZ set Initially
a > b PRP
a < b PRN
a = b PRZ

Timing

Total time in microseconds
= 21n + 35, where n equals the number of characters compared.

Example #1

Instruction:

Operation	N	A Address	B Address
Y	5	1001	1007

HSM before and after Instruction is Executed:

1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012
S	M	I	T	H	—	S	M	I	T	H	—

Final Register Contents:

$(A)_t = 1006$

$(B)_t = 1012$

PRI

PRZ is set.

Time:

21 (5) + 35 = 140 μs.

Example #2

Instruction:

Operation	N	A Address	B Address
Y	4	2000	2006

HSM before and after Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011
1	2	4	5	6	—	1	2	3	6	9	—

Final Register Contents:

$(A)_t = 2003$

$(B)_t = 2009$

PRI

PRP is set.

Time:

(21) 3 + 35 μs = 98 μs.

Example #3

Instruction:

Operation	N	A Address	B Address
Y	4	3000	3005

HSM before and after Instruction is Executed:

3000	3001	3002	3003	3004	3005	3006	3007	3008	3009
4	5	7	8	—	5	5	7	2	—

Final Register Contents:

$(A)_t = 3001$

$(B)_t = 3006$

PRI

PRN is set.

Time:

(21) 1 + 35 = 56 μs.

X Tally (TA)

General Description

This instruction permits looping through a sequence of operations by automatically reducing a pre-stored quantity each time control is transferred to the beginning of the sequence. When the quantity (always a positive numeric) has been exhausted, the Tally ends and the instruction following it is performed. The maximum value of of Tally quantity is 99.

Format

Operation — X
N — 0 (Zero)
A Address — HSM address of the diad containing the quantity to be tested.
B Address — HSM location of next instruction to be performed if quantity being tested has not been exhausted.

Standard Location

STP (on transfer only)

Outline of Operation

The contents of the HSM diad specified by the A Register are transferred to the D Register. If the quantity is 00, the Tally ends and the next instruction in sequence is executed. If the quantity is other than 00, the contents of the D Register are decremented by one and stored in the HSM diad location specified by the A Register. The contents of the P Register are stored in STP, and the contents of the B Register are transferred to the P Register.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

70 μs — When Tally quantity is greater than zero upon starting.
49 μs — When Tally quantity is equal to zero upon starting.

• Halt (HLT)

General Description

This instruction inhibits the staticizing of any further instructions, halting the computer after completion of any instruction in the Simultaneous or Record File Modes.

Format

Operation — . (period).
N — 0 (Zero), may be used to designate type of stop.
A Address — 0000, may be used for numeric constants (0-9).
B Address — 0000, may be used for numeric constants (0-9).

Outline of Operation

If the Simultaneous or Record File Mode is unoccupied the Computer stops immediately. If either of these two modes is occupied, the instruction in these modes will be executed before stopping.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

35 μs

R REPEAT (RPT)

General Description

This instruction causes the next repeatable instruction to be repeated a specified number of times. All non-repeatable instructions which occur between this instruction and the repeatable instruction will also be repeated.

Format

Operation — R

N — Number of times to repeat the next repeatable instruction in sequence. (See Appendix F-II.)

A Address — If zero (0000) or even, does not staticize the A address of any succeeding instruction, except the A address of the first instruction following the repeat instruction the first time it is executed. If one (0001) or odd, the A address of all succeeding instructions are staticized.

B Address — If zero (0000) or even, does not staticize B address of any succeeding instruction, except the B address of the first instruction following the repeat instruction the first time it is executed. If one (0001) or odd, the B address of all succeeding instructions are staticized.

Standard Location

0222-0225

Outline of Operation

The contents of the N Register are transferred to the N_R (Repeat) Register. The contents of the P Register are transferred to HSM locations 0222 - 0225. Indicators are set specifying whether or not the A and B addresses of the instructions following the Repeat instructions are to be staticized as denoted in the Repeat instruction's A and B addresses. The next instruction will then be staticized and executed, disregarding the settings of the indicators. During all successive executions of this instruction, the A and B address will be staticized as specified by the indicators.

If the instruction following the Repeat instruction is a non-repeatable instruction, all successive non-repeatable instructions and the next repeatable instruction are staticized as specified by the indicators and executed.

If the instruction following the Repeat instruction is a repeatable instruction, or when a repeatable instruction is encountered following a non-repeatable instruction, the sequence of instruction execution occurs in the following cycle.

After the repeatable instruction is executed, the contents of the N_R Register are examined. If zero, the indicators are reset and the next instruction is executed. If other than zero, the contents of the N_R Register are decremented by one and the contents of the HSM locations 0222 - 0225 are transferred to the P Register. The instruction immediately following the RPT instruction is staticized as specified by the indicators and is executed. Henceforth, all successive non-repeatable instructions and the next repeatable instruction are staticized as specified by the indicators and executed. When the next repeatable instruction is again encountered, the cycle is repeated.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

49 μs.

Note: Each time a repeatable instruction is repeated there are three additional status levels (21 microseconds) required when the contents of the N_R Register exceed zero, and one additional status level (7 microseconds) when the contents of the N_R Register are zero.

VIII — INPUT/OUTPUT INSTRUCTIONS — CARD

0 Card Read Normal (CRN)

General Description

This instruction reads information from punched cards in the Card Reader, Model 323, into the HSM. Facilities are provided for reading cards at 600, 300, or 200 cards per minute, or for single card feed on demand.

Format

Operation — 0 (zero)

N — Selects the Card Reader, Model 323, and either determines the rate at which cards are to be read or is used in a card cycle ending routine, according to the following:

Card Reader	Result
1	Reads single card or terminates continuous card reading cycle (600 cpm)
2	Used in continuous card ending routine (600 cpm)
4	Used in continuous card reading cycle (600 cpm)
M	Used in alternate card reading cycle (300 cpm)
8	Terminates alternate card reading cycle (300 cpm)

A Address — Address of HSM location to receive the first character read from punched cards.

B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

Initially and thereafter, as the need arises, the instruction automatically directs the Card Reader to place one or more cards in the read station and operates on successive characters in the following cycle:

The character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 code and is placed in HSM in the location specified by the A Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(A)_1 + 79$.

In order to maintain a 600 card per minute rate, a Card Read instruction in which the N character is 4 must be executed for each card read. The successive card read instructions must be staticized before 100 milliseconds have elapsed. Approximately 80 milliseconds are required to read one card leaving 20 milliseconds of compute time between cards.

Continuous card reading is initiated when $N = 4$. Since only the first of the three cards in the card reader transport mechanism is read by this instruction, the continuous card reading cycle must be terminated by two card read instructions in which the N characters are 2 and 1 respectively to avoid a "feed" error.

The card feed rate may be accomplished at 300 cards per minute by staticizing successive card read instructions every 200 milliseconds for each card read. The N character in the card read instructions must be M. Of this 200 millisecond card cycle, approximately 120 milliseconds are free for computing after the card has been read.

This Alternate Card Reading cycle must be terminated by a Card Read instruction in which the $N = 8$.

When Card Read instructions are staticized in which the N character is 1, cards may be read at any rate up to 200 cards per minute. No terminating instruction is necessary since only one card has been fed into the Card Reader transport mechanism by this instruction.

Automatic card translation does not take place if the BCT button on the Computer Console Panel is in the "on" position. Each card column is then split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the A Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at $(A)_i + 79$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0) is read into HSM at $(A)_i + 80$. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at $(A)_i + 159$. The final A Register setting is $(A)_i + 160$.

Final Register Contents

$(A)_f$ = One location to the right of the last character read into HSM.
$(B)_f = (A)_i$ with BCT off.
$(B)_f = (A)_i + 80$ with BCT on.

Timing

Card Feed Rate Per Minute	Time in Milliseconds	Time Free For Computing
600	100*	20*
300	200*	120*
up to 200	300 (Minimum)	20 (Minimum)

* ±1.5%

Example

Instruction:

Operation	N	A Address	B Address
0	4	1000	0000

HSM after Instruction is Executed (with BCT on):

1000	1079	1080	1159
← DATA FROM CARD → (rows 9 through 4)		← DATA FROM CARD → (rows 3 through Y)	
Col. 1	Col. 80	Col. 1	Col. 80

HSM after Instruction is Executed (with BCT off):

1000	1079
← DATA FROM CARD →	
Col. 1	Col. 80

Final Register Contents:

$(A)_f$ = 1160 (BCT on)
$(A)_f$ = 1080 (BCT off)
$(B)_f$ = 1080 with BCT on
$(B)_f$ = 1000 with BCT off

Time:

100 (±1.5%) milliseconds (20 (±1.5%) milliseconds free for computing).

0 Card Read Normal (CRN)

General Description

This instruction reads information from punched cards in the Model 324 and 329 Card Readers into the HSM using the Normal Mode.

Format

Operation — 0 (Zero)
N —

Symbol	Result
K	Binary read mode specified
1	Translate read mode specified

A Address— Address of HSM location to receive the first character read from punched cards.
B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

This instruction directs the Card Reader to place a card in the read station and operates on successive characters in the following cycle:

When the translate mode has been specified (N = 1) the character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 Code and is placed in HSM in the location specified by the A Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(A)_i + 79$.

When the binary mode has been specified (N = K) each card column is split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred successively to HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the A Register. Successive characters representing rows 9 through 4 will be read and placed at $(A)_i + 2, 4, 6$ and so on with column 80 being placed at $(A)_i + 158$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0) is read into HSM at $(A)_i + 1$. Successive characters representing rows 3 through Y will be read and placed at $(A)_i + 1, 3, 5$ and so on with column 80 being placed at $(A)_i + 159$.

Final Register Contents

$(A)_f$ = HSM location of last character transferred to HSM + 1.
$(B)_f = (A)_i$

Timing

Card Reader Model	Card Rate per Minute	Time Between Card Requests (ms)	PROCESSING TIME (ms)	
			Without Read Release	With Read Release
324	900	66.7	0	18.5
329	1500	40.5	0	13

Example

Instruction:

Operation	N	A Address	B Address
0	K	0700	0000

HSM after Instruction is Executed:

0700	0701		0858	0859
Data (Rows 9 through 4) Col. 1	Data (Rows 3 through Y) Col. 1	. . . . .	Data (Rows 9 through 4) Col. 80	Data (Rows 3 through Y) Col. 80

Final Register Contents:

$(A)_f = 0860$

$(B)_f = 0780$

Time:

66.7 milliseconds (Model 324), 40.5 milliseconds (Model 329).

0 Card Read Normal (CRN)

General Description

This instruction reads information from punched cards in the Read Unit of the Card Reader-Punch into the HSM using the Normal Mode.

Format

Operation — 0 (Zero)

N —

Symbol	Result
K	Binary read mode specified
1	Translate read mode specified

A Address — Address of HSM location to receive the first character read from punched cards.

B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

This instruction directs the Card Reader Unit to place a card in the read station and operates on successive characters in the following cycle:

When the translate read mode has been specified (N = 1) the character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 code and is placed in HSM in the location specified by the A Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(A)_i + 79$.

When the binary read mode has been specified (N = K) each card column is split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the A Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at $(A)_i + 79$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0) is read into HSM at $(A)_i + 80$. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at $(A)_i + 159$. The final A Register setting is $(A)_f + 160$.

A card read instruction must be staticized for each card read. In order to maintain an 800 card per minute rate, successive Card Read Instructions must be staticized before 75 milliseconds have elapsed. The 75 milliseconds card cycle is comprised of 21 milliseconds card feed access time, 44 milliseconds card read time, and 10 milliseconds time free for compute. When the read release option is exercised (via the Input/Output Control Instruction), an additional 21 milliseconds of compute time is made available.

Final Register Contents

$(A)_f$ = One location to the right of the last character read into HSM.

$(B)_f = (A)_i$ when N = 1 (Translate Read Mode).

$(B)_f = (A)_i + 80$ when N = K (Binary Read Mode).

Timing

Card Rate per Minute	Time Between Card Requests (ms)	PROCESSING TIME (ms)*	
		Without Read Release	With Read Release
800	75	10	31
600**	100	35	56
480**	125	60	81
400	150	85	106
343**	175	110	131
300**	200	135	156
266	225	160	181

* Allow one millisecond of the available compute time for variation in the motor speed.

** When Reader-Punch includes Early Card Read Feature.

Example

Instruction:

Operation	N	A Address	B Address
0	K	0600	0000

HSM after Instruction is Executed:

0600	0679	0680	0759
← DATA FROM CARD → (rows 9 through 4)		← DATA FROM CARD → (rows 3 through Y)	
Col. 1	Col. 80	Col. 1	Col. 80

Final Register Contents:

$(A)_t = 0760$

$(B)_t = 0680$

Time:

75 milliseconds (10 milliseconds compute time unless read release option exercised in which case 21 additional milliseconds are available).

1 Card Read Simultaneous (CRS)

General Description

This instruction reads information from punched cards in the Card Reader, Model 323, into the HSM in the Simultaneous Mode. Facilities are provided for reading cards at 600, 300 or 200 cards per minute, or for single card feed on demand.

Format

Operation — 1

N — Selects the Card Reader, Model 323, and either determines the rate at which cards are to be read or is used in a card cycle ending routine, according to the following:

Card Reader	Result
1	Reads single card or terminates continuous card reading cycle (600 cpm)
2	Used in continuous card ending routine (600 cpm)
4	Used in continuous card reading cycle (600 cpm)
M	Used in alternate card reading cycle (300 cpm)
8	Used in alternate card ending routine (300 cpm)

A Address — Address of HSM location to receive the first character read from punched cards.

B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

This instruction is initially staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to the SOR Register and the contents of the A and B Register are transferred to the S and T Registers, respectively.

This instruction operates in the Simultaneous Mode. Initially and thereafter, as the need arises, this instruction automatically directs the Card Reader to place one or more cards in the read station and operates on successive characters in the following cycle:

The character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 code and is placed in the location specified by the S Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(S)_1 + 79$.

In order to maintain the 600 card per minute rate, a card read instruction in which the N character is 4 must be executed for each card read. The successive Card Read instructions must be staticized before 100 milliseconds have elapsed. Approximately 80 milliseconds are required to read one card, leaving 20 milliseconds of compute time between cards.

Continuous card feeding is initiated when $N = 4$. Since only the first of the three cards in the Card Reader transport mechanism is read by this instruction, the Continuous Card Reading cycle must be terminated by two Card Read instructions in which the N characters are 2 and 1 respectively to avoid a "feed" error.

The card feed rate may be accomplished at 300 cards per minute by staticizing successive Card Read instructions every 200 milliseconds for each card read. The N character in the Card Read instructions must be M. Of this 200 millisecond card cycle, approximately 120 milliseconds are free for computing after the card has been read. This Alternate Card Reading cycle must be terminated by a Card Read instruction in which the $N = 8$.

When Card Read instructions are staticized in which each N character is 1, cards may be read at any rate up to 200 cards per minute. No terminating instruction is necessary since only one card has been fed into the Card Reader transport mechanism by this instruction.

Automatic card translation does not take place if the BCT button on the Computer Console Panel is in the "on" position. Each card column is then split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the S Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at $(S)_i + 79$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0), is read into HSM at $(S)_i + 80$. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at $(S)_i + 159$. The final S Register setting is $(S)_i + 160$.

Final Register Contents

$(S)_f$ = One location to the right of the last character read into HSM.
$(T)_f = (A)_i$ with BCT off.
$(T)_f = (A)_i + 80$ with BCT on.

Timing

Card Feed Rate per Minute	Time in Milliseconds	Time Free For Other Processing*
600	100**	20**
300	200**	120**
up to 200	300 (Minimum)	20 (Minimum)

* Indicates time available between card cycles. Additional compute time for processing other than this card is also available while the card data is being read into H.S.M.

** ±1.5%.

1 Card Read Simultaneous (CRS)

General Description

This instruction reads information from punched cards in the Model 324 and 329 Card Readers into the HSM using the Simultaneous Mode.

Format

Operation — 1

N —

Symbol	Result
K	Binary read mode specified
1	Translate read mode specified

A Address — Address of HSM location to receive the first character read from punched cards.

B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

This instruction is initially staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to the SOR Register and the contents of the A and B Registers are transferred to the S and T Registers, respectively.

This instruction operates in the Simultaneous Mode. The Simultaneous Mode interrupts the Normal Mode 1.12 milliseconds during the card read time.

This instruction directs the Card Reader to place a card in the read station and operates on successive characters in the following cycle:

When the translate mode has been specified (N = 1) the character in column one of the punched card is automatically translated from RCA Card Code to RCA 301 Code and is placed in HSM in the location specified by the S Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(A)_i + 79$.

When the binary mode has been specified (N = K) each card column is split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred successively to HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the S Register. Successive characters representing rows 9 through 4 will be read and placed at $(S)_i + 2, 4, 6$ and so on with column 80 being placed at $(S)_i + 158$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0) is read into HSM at $(S)_i + 1$. Successive characters representing rows 3 through Y will be read and placed at $(A)_i + 1, 3, 5$ and so on with column 80 being placed at $(S)_i + 159$.

Final Register Contents

$(S)_f$ = HSM location of last character transferred to HSM + 1.

$(T)_f = (A)_i$

Timing

Card Reader Model	Card Feed Rate per Minute	Time in Milliseconds	PROCESSING TIME (ms)	
			Without Read Release	With Read Release
324	900	66.7	0	18.5
329	1500	40.5	0	13

1 Card Read Simultaneous (CRS)

General Description

This instruction reads information from punched cards in the Read Unit of the Card Reader-Punch into the HSM using the Simultaneous Mode.

Format

Operation — 1
N —

Symbol	Result
K	Binary read mode specified
1	Translate read mode specified

A Address — Address of HSM location to receive the first character read from punched cards.
B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Outline of Operation

This instruction is initially staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to the SOR Register and the contents of the A and B Registers are transferred to the S and T Registers, respectively.

This instruction operates in the Simultaneous Mode. This instruction directs the Card Reader Unit to place a card in the read station and operates on successive characters in the following cycle:

When the translate read mode has been specified (N = 1), the character in column one of the punched card is automatically translated from RCA card code to RCA 301 code and is placed in HSM in the location specified by the S Register. The following 79 characters are placed in successive locations in HSM. The final character (column 80) is located at $(S)_i + 79$.

When the binary read mode has been specified (N = K), each card column is split into two groups of six bits each, a parity bit is generated and added to each group, and the resultant two characters are transferred into HSM.

The character represented by rows 9 through 4 in column 1 (row 9 = 2^5, row 4 = 2^0) is read into HSM at the location specified by the S Register. Successive characters representing rows 9 through 4 are also read into memory with column 80 being placed at $(S)_i + 79$. The character represented by column 1, rows 3 through Y (row 3 = 2^5, row Y = 2^0) is read into HSM at $(S)_i + 80$. Successive characters representing rows 3 through Y are likewise read into HSM with column 80 being placed at $(S)_i + 159$. The final S Register setting is $(S)_i + 160$.

A card read instruction must be staticized for each card read. In order to maintain an 800 card per minute rate, successive Card Read instructions must be staticized before 75 milliseconds have elapsed. The 75 millisecond card cycle includes 21 milliseconds card feed access time, 44 milliseconds card read time, and 10 milliseconds free time. The Simultaneous Mode interrupts the Normal Mode 13.44 milliseconds during the 44 milliseconds card read time.

Final Register Contents

$(S)_f$ = One location to the right of the last character read into HSM.
$(T)_f = (A)_i$ when N = 1 (Translate Read Mode).
$(T)_f = (A)_i + 80$ when N = K (Binary Read Mode).

Timing

Card Rate per Minute	Time Between Card Requests (ms)	PROCESSING TIME (ms)*	
		Without Read Release	With Read Release
800	75	10	31
600**	100	35	56
480**	125	60	81
400	150	85	106
343**	175	110	131
300**	200	135	156
266	225	160	181

* Allow one millisecond of the available time for variation in the motor speed.

** When Reader-Punch includes Early Card Read Feature.

2 Card Punch Normal (CPN)

General Description

This instruction enables the Model 334 Card Punch to punch 80-column cards from information contained in the HSM.

Format

Operation — 2
N — Must be zero (0).
A Address — HSM address of first character to be punched.
B Address — HSM address of last character to be punched.

Direction of Operation

Left to right.

Standard Location

0202 - 0205

Outline of Operation

A start signal is sent to the Card Punch. The Card Punch punches the information from HSM between and including the locations addressed by the contents of the A and B Registers, punching 80 columns to a card. When the A and B Registers are equal, the last card is punched and the contents of the A Register are incremented by one.

The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of punching.

Final Register Contents

$(A)_f$ = Address of location one to the right of the last character in HSM punched.
$(B)_f = B_i$

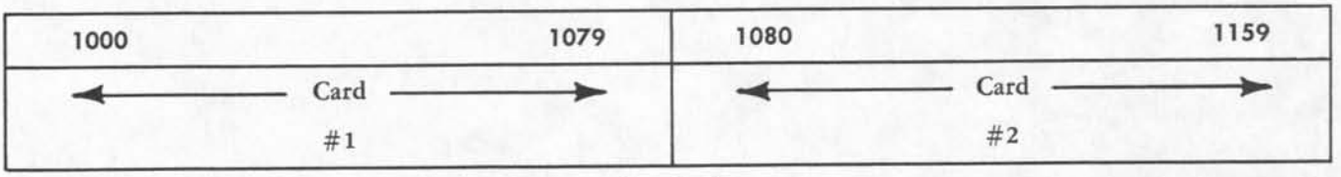
Timing

Cards are punched at the rate of 100 cards per minute.

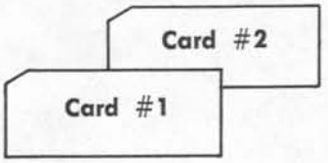
Example

Instruction:

Operation	N	A Address	B Address
2	0	1000	1159



Punched



Final Register Contents:

$(A)_f = 1160$
$(B)_f = 1159$

Time:

1.2 seconds

2 Card Punch Normal (CPN)

General Description

This instruction enables the Model 336 Card Punch to punch 80-column cards from information contained in the HSM.

Format

Operation — 2
N — Determines the rate at which cards are to be punched, or is used in a card cycle ending routine.

N	Purpose
1	Demand card punching, or to terminate continuous card punching
2	Used in continuous card punching ending routine
4	Continuous card punching

A Address — HSM address of first character to be punched.
B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Standard Location

0202 - 0205

Outline of Operation

A start signal is sent to the Card Punch. Initially and thereafter, as the need arises, this instruction automatically directs the Card Punch to place one or more cards in the punch station and operates on successive characters in the following cycle.

The Card Punch punches all the information from the HSM location addressed by the A Register through the next 79 HSM locations. 80 characters are punched in each card. After the card is punched, it is immediately read to verify punching accuracy and placed in the output stacker.

Final Register Contents

$(A)_f = (A)_i + 80$
$(B)_f = (B)_i$

Timing

Cards are punched at a rate of up to 200 cards per minute.

2 Card Punch Normal (CPN)

General Description

This instruction enables the Punch Unit of the Card Reader-Punch to punch one or more 80-column cards from information contained in the HSM using the Normal Mode.

Format

Operation — 2
N

N	Card Punch Mode
&	Binary
0 (Zero)	Translate

A Address — HSM address of first character to be punched.
B Address — HSM address of last character to be punched.*

* When punching in the binary mode, the number of characters defined by the A and B addresses must be a multiple of 160.

Direction of Operation

Left to right.

Standard Location

0202 - 0205

Outline of Operation

A start signal is sent to the Card Punch Unit. The Card Punch Unit punches the information from HSM between and including the locations addressed by the contents of the A and B Registers, punching up to 80 columns to a card. Punching of the last card is completed when the A and B Registers are equal. The contents of the A Register are then incremented by one.

When the binary punch mode is specified (N = &), the A Register denotes the memory location of the character to be punched in column 1, rows Y through 3. Each information bit results in a hole in the card (2^0 = row Y, 2^5 = row 3). Successive characters representing rows Y through 3 are also punched from HSM with column 80 being punched from $(A)_i + 79$. The character present at $(A)_i + 80$ is punched into column 1, rows 4 through 9 (2^0 = row 4, 2^5 = row 9). Successive characters representing rows 4 through 9 are also punched from HSM with column 80 being punched from $(A)_i + 159$.

The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of punching.

Final Register Contents

$(A)_f$ = Address of location one to the right of the last character in HSM punched.
$(B)_f = (B)_i$

Timing

Cards may be punched at the rate of 250 cards per minute.

3 Card Punch Simultaneous (CPS)

General Description

This instruction enables the Card Punch Model 334 to punch 80-column cards from information contained in the HSM, using the Simultaneous Mode.

Format

Operation — 3
N — Must be zero (0).
A Address — HSM address of first character to be punched.
B Address — HSM address of last character to be punched.

Direction of Operation

Left to right.

Standard Location

0202 - 0205

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to SOR Register, and the contents of the A and B Registers are transferred to the S and T Registers respectively, and this instruction is executed in the Simultaneous Mode. The operation of the instruction is as follows:

A start signal is sent to the Card Punch. Punching by the Card Punch is initiated and continues until all the characters between and including the HSM locations specified by the S and T Registers are punched. When the contents of the S and T Registers are equal, the last card is punched and the contents of the S Register are incremented by one. The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of the punching.

Final Register Contents

$(S)_f$ = HSM address of location one to the right of the last character in HSM punched.
$(T)_f = (B)_i$

Timing

Cards are punched at the rate of 100 cards per minute.

3 Card Punch Simultaneous (CPS)

General Description

This instruction enables the Model 336 Card Punch to punch 80-column cards from information contained in the HSM, using the Simultaneous Mode.

Format

Operation — 3
N — Determines the rate at which cards are to be punched, or is used in card cycle ending routine.

N	Purpose
1	Demand card punching, or to terminate continuous card punching
2	Used in continuous card punching ending routine
4	Continuous card punching

A Address — HSM address of first character to be punched.
B Address — Must be zeros (0000).

Direction of Operation

Left to right.

Standard Location

0202 - 0205

Outline of Operation

A start signal is sent to the Card Punch. Initially and thereafter, as the need arises, this instruction automatically directs the Card Punch to place one or more cards in the punch station and operates on successive characters in the following cycle.

The Card Punch punches all the information from the HSM location addressed by the S Register through the next 79 HSM locations. 80 characters are punched in each card. After the card is punched, it is immediately read to verify punching accuracy and placed in the output stacker.

Final Register Contents

$(S)_t = (A)_i + 80$
$(T)_t = (B)_i$

Timing

Cards are punched at a rate of up to 200 cards per minute.

3 Card Punch Simultaneous (CPS)

General Description

This instruction enables the Punch Unit of the Card Reader-Punch to punch 80-column cards from information contained in the HSM, using the Simultaneous Mode.

Format

Operation — 3
N

N	Card Punch Mode
&	Binary
0 (Zero)	Translate

A Address — HSM address of first character to be punched.
B Address — HSM address of last character to be punched.*

* When punching in the binary mode, the number of characters defined by the A and B addresses must be a multiple of 160.

Direction of Operation

Left to right.

Standard Locations

0202 - 0205

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR Register are transferred to the SOR Register, and the contents of the A and B Registers are transferred to the S and T Registers respectively, and this instruction is executed in the Simultaneous Mode. The operation of the instruction is as follows:

A start signal is sent to the Card Punch Unit. Punching by the Card Punch Unit is initiated and continues until all the characters between and including the HSM locations specified by the S and T Registers are punched. Punching of the last card is completed when the contents of the S and T Registers are equal. The contents of the S Register are then incremented by one. The card punched is read concurrently with the punching of the succeeding card to insure the accuracy of the punching.

When the binary punch mode is specified (N = &), the S Register denotes the memory location of the character to be punched in column 1, rows Y through 3. Each information bit results in a hole in the card (2^0 = row Y, 2^5 = row 3). Successive characters representing rows Y through 3 are also punched from HSM with column 80 being punched from $(S)_i + 79$. The character present at $(S)_i + 80$ is punched into column 1, rows 4 through 9 (2^0 = row 4, 2^5 = row 9). Successive characters representing rows 4 through 9 are also punched from HSM with column 80 being punched from $(A)_i + 159$.

Final Register Contents

$(S)_f$ = Address of location one to the right of the last character in HSM punched.
$(T)_f = (B)_i$

Timing

Cards may be punched at the rate of 250 cards per minute.

; Input/Output Control (IOC)

Feature not operable
57

General Description

This instruction performs the Read Release, Punch Release and Stacker Select functions for the Card Reader-Punch, Model 330, and the Read Release function for the Card Readers, Model 324 and 329.

Format

Operation — ;
N — (
A Address — A_0, A_1, A_2 — Must be zeros (000).
— A_3 — designates function to be performed:

A_3	FUNCTION		
	Card Reader—Punch Model 330	Card Reader Model 324	Card Reader Model 329
1	Select Reader Stacker No. 1		
2	Select Reader Stacker No. 2		
3	Select Punch Stacker No. 4		
4	Select Punch Stacker No. 8		
5	Read Release	Read Release	Read Release
6	Punch Release		
7	Read Release and Select Stacker No. 1		
8	Read Release and Select Stacker No. 2		
9	Punch Release and Select Stacker No. 4		
sp.	Punch Release and Select Stacker No. 8		

NOT AVAILABLE

B Address — Must be zeros (0000).

Outline of Operation

The A_3 character is sent to the control module. After the operation is initiated, the registers are available for use by the next instruction.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

42 μs.

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected card device and chooses one of two sequences of instructions.

Format

Operation — S

N — Selects the card device to be tested according to the following:

Device	N
Card Reader or Read Unit of Card Reader-Punch	(
Card Punch or Punch Unit of Card Reader-Punch	)

A Address — A_0 specifies the tests to be performed as follows:

"1" Bit In	Numeric Equivalent	Tests
2^0	1	Is the selected device inoperable?
2^1	2	Is the selected device operating?

— A_1, A_2, A_3 — Must be zeros (000).

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

56 μs if a transfer is executed.

42 μs if no transfer takes place.

IX — INPUT/OUTPUT INSTRUCTIONS — TAPE

4 Tape Read Forward Normal (RFN) — Repeatable

General Description

This instruction brings a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. When reading gapless paper tape, transfer begins with the first character and ends when the specified HSM area is filled or a gap is sensed.

Format

Operation — 4
N — Identification character of Tape Station, Paper Tape Reader, or Interrogating Typewriter. (See Appendix G.)
A Address — Address of HSM location which is to receive the first character read.
B Address — Address of HSM location which is to receive the last character read.

Direction of Operation

Left to right.

Standard Location

STA (0212 - 0215)
P STF (0216-0219)

Direction of Tape Motion

Forward

Outline of Operation

Initially this instruction sends a start signal to the input unit specified by the contents of the N Register. When this input unit is a Tape Station or the Paper Tape Reader, the first character following a gap, or the next character of gapless paper tape, is then placed in the input buffer and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the input buffer is transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are incremented by one. If the comparison proved equal and a gap is passed in sequence, PRZ is set, and the instruction terminates. If the comparison proved equal and a gap is not passed, PRP is set, and the instruction terminates. However, the tape movement continues to gap unless gapless paper tape is being read. If the comparison proved not equal and a gap is passed in sequence, PRN is set, and the instruction terminates. If the comparison proved not equal and a gap is not passed the cycle is repeated.

When reading 66 KC magnetic tape two characters are transferred from tape to the input buffer and then to HSM, and the A Register is incremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from magnetic tape, the EF/ED Normal Indicator is set. The EF/ED Normal Indicator is not set when reading from paper tape.

Final Register Contents

$(A)_f$ = One location to the right of the last character read into HSM.
$(B)_f = (B)_i$

PRI (TAPE)

PRP: The A and B Registers are equal before a gap has been found on tape.
PRN: A gap has been found on tape and the A and B Registers are unequal.
PRZ: At the time a gap has been found on tape the A and B Registers are equal.

Timing

Hi-Data Tapes, Model 381, are read at the rate of 10 KC.

Hi-Data Tapes, Model 382, are read at the rate of 30 KC.

Paper tape is read at the rate of up to 1000 characters per second.

The tape station attached to the Tape Adapter or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

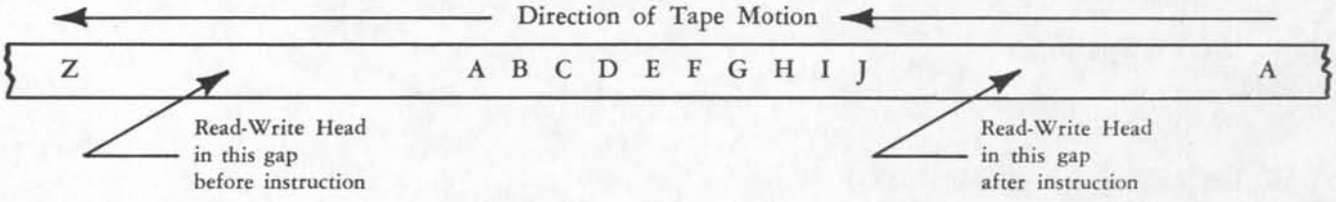
The Interrogating Typewriter prints at a rate up to 10 characters per second.

Example #1

Instruction:

Operation	N	A Address	B Address
4	1	2021	2030

Tape on Station #1:



HSM before Instruction is Executed:

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
—	—	—	—	—	—	—	—	—	—

HSM after Instruction is Executed:

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
A	B	C	D	E	F	G	H	I	J

Final Register Contents:

$(A)_t = 2031$

$(B)_t = 2030$

PRI

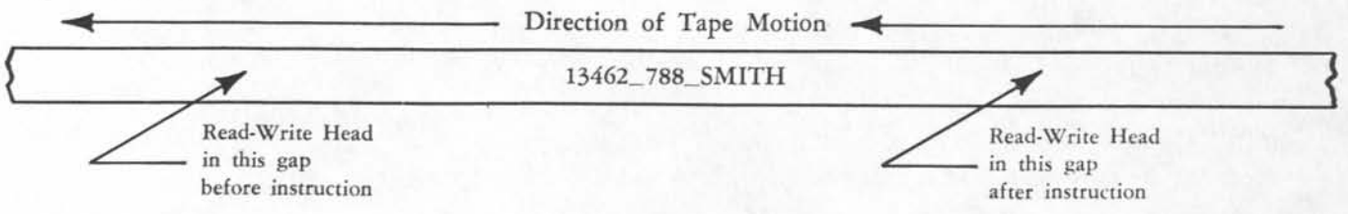
PRZ is set

Example #2

Instruction:

Operation	N	A Address	B Address
4	J	2000	2004

Tape on Station J



HSM before Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008
2	5	7	9	1	—	J	1	M

HSM after Instruction is Executed:

2000	2001	2002	2003	2004	2005	2006	2007	2008
1	3	4	6	2	—	J	1	M

Final Register Contents:

$(A)_t = 2005$

$(B)_t = 2004$

PRI

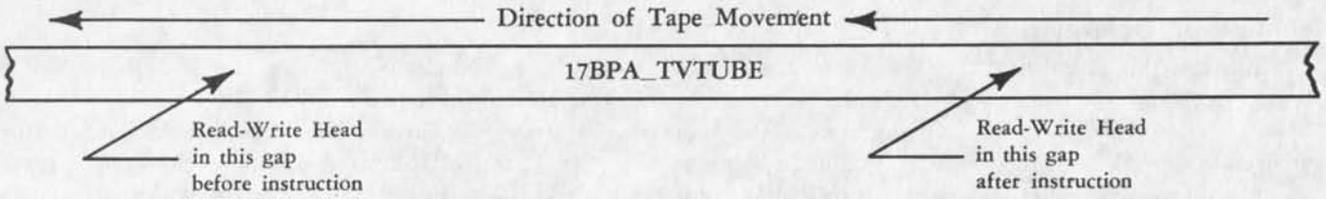
PRP is set

Example #3

Instruction:

Operation	N	A Address	B Address
4	P	4000	4050

Tape on Station P



HSM before the Instruction is Executed:

4000 - 4050 is filled with spaces

HSM after the Instruction is Executed:

4000	4001	4002	4003	4004	4005	4006	4007	4008	4009	4010	4011	4012 — 4050
1	7	B	P	A	—	T	V	T	U	B	E	———————

Final Register Contents:

$(A)_t = 4012$

$(B)_t = 4050$

PRI

PRN is set

5 Tape Read Forward Simultaneous (RFS)

General Description

This instruction brings a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specific HSM area is filled. When reading gapless paper tape, transfer begins with the first character and ends when the specified HSM area is filled or a gap is sensed. This instruction is performed in the Simultaneous Mode.

Format

Operation — 5
N — Identification character of Tape Station, Paper Tape Reader, or Interrogating Typewriter. (See Appendix G.)
A Address — Address of location in HSM which is to receive the first character read.
B Address — Address of location in HSM which is to receive the last character read.

Direction of Operation

Left to right.

Direction of Tape Motion

Forward

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the input unit specified by the contents of the M Register. The first character following a gap on tape or the next character on gapless paper tape is placed in the tape buffer, and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the input buffer is transferred to the HSM location specified by the S Register. The contents of the S Register are compared with the contents of the T Register. The contents of the S Register are incremented by one. If a gap is passed in sequence, the instruction terminates. If the comparison proved equal and a gap is not passed, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

When reading 66 KC magnetic tape two characters are transferred from tape to the input buffer and then to HSM, and the S Register is incremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from magnetic tape, the EF/ED Simultaneous Indicator is set. The EF/ED Simultaneous Indicator is not set when reading from paper tape. If SMDI is set, the EF/ED Normal Indicator will be set.

Final Register Contents

$(S)_f$ = One location to the right of the last character read into HSM.
$(T)_f = (B)_i$

Timing

Hi-Data tapes, Model 381, are read at the rate of 10 KC.

Hi-Data tapes, Model 382, are read at the rate of 30 KC.

Paper tape is read at the rate of up to 1000 characters per second.

The tape station attached to the Tape Adapter or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

The Interrogating Typewriter prints at a rate up to 10 characters per second.

6 Tape Read Reverse Normal (RRN) — Repeatable

General Description

This instruction transfers a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. Though the tape moves in reverse, the characters will be placed in their proper relative position within HSM.

Format

Operation — 6
N — Identification character of Tape Station or Paper Tape Reader. (See Appendix G.)
A Address — Address of HSM location to receive the first character read from tape.
B Address — Address of HSM location to receive the last character read from tape.

Direction of Operation

Right to left.

Standard Location

STA (0212 - 0215)

Direction of Tape Motion

Magnetic tape moves in a reverse direction. Paper Tape will be moved in a forward direction, but the characters read from paper tape will be placed in memory from right to left.

Outline of Operation

Initially this instruction sends a start signal to the input unit specified by the contents of the N Register. After a gap is passed on magnetic tape, the first character is placed in the tape buffer, and this instruction operates in the following cycle:

When reading other than 66 KC tape, the character in the tape buffer is transferred to the HSM location specified by the A Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are decremented by one. If the comparison proved equal and a gap is passed in sequence, PRZ is set, the instruction terminates. If the comparison proved equal and a gap is not passed, PRP is set, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is passed in sequence, PRN is set, the instruction terminates. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

When reading 66 KC magnetic tape, two characters are transferred from tape to the input buffer and then to HSM, and the A Register is decremented by two. Otherwise, the instruction operates as stated above.

If an EF or ED alone is read from magnetic tape, the EF/ED Normal Indicator is set. The EF/ED Normal Indicator is not set when reading from paper tape.

If ETW is passed the ETW flip-flop is reset.

Final Register Contents

$(A)_f$ = Address of location one to the left of the last characters read.
$(B)_f = (B)_i$

PRI

PRP: The A and B Registers are equal before a gap has been found on tape.
PRN: A gap has been found on tape and the A and B Registers are unequal.
PRZ: The A and B Registers are equal at the time a gap has been found on tape.

Timing

Hi-Data tapes, Model 381, are read at the rate of 10 KC.

Hi-Data tapes, Model 382, are read at the rate of 30 KC.

Paper tape is read at the rate of up to 1000 characters per second.

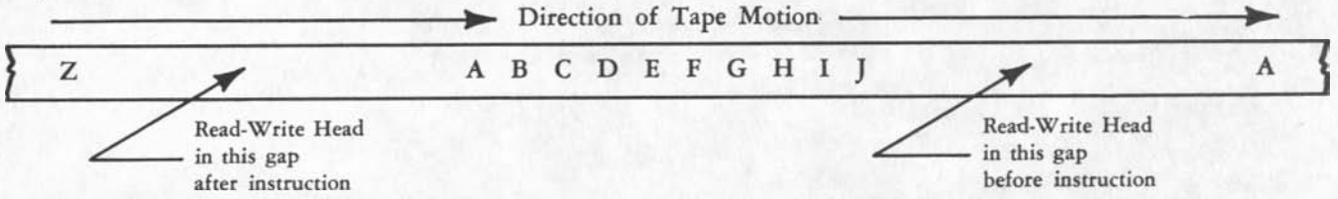
The tape station connected to the Tape Adapter or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station, or 66.7 KC if it is a Model 582 Tape Station.

Example

Instruction:

Operation	N	A Address	B Address
6	3	2030	2021

Tape on Station #3:



HSM before Instruction is Executed:

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
—	—	—	—	—	—	—	—	—	—

HSM after Instruction is Executed:

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
A	B	C	D	E	F	G	H	I	J

Final Register Contents:

$(A)_t = 2020$

$(B)_t = 2021$

PRI

PRZ is set

7 Tape Read Reverse Simultaneous (RRS)

General Description

This instruction transfers a series of consecutive characters from magnetic tape or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. Though the tape moves in reverse, the characters will be placed in their proper relative position within HSM. This instruction operates in the Simultaneous Mode.

Format

Operation — 7
N — Identification character of Tape Station or Paper Tape Reader. (See Appendix G.)
A Address — Address of HSM location to receive the first character read from tape.
B Address — Address of HSM location to receive the last character read from tape.

Direction of Operation

Right to left.

Direction of Tape Motion

Magnetic tape moves in a reverse direction. Paper tape will move in the forward direction but characters read from paper tape are placed in memory from right to left.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the input unit specified by the contents of the M Register. After a gap is passed on magnetic tape, the first character is placed in the input buffer, and this instruction operates in the following cycle:

The character in the input buffer is transferred to the HSM location specified by the S Register. The contents of the S Register are decremented by one. If a gap is passed in sequence, the instruction terminates. If the comparison proves equal and a gap is not passed, the instruction terminates, and tape movement continues to gap. If the comparison proved not equal and a gap is not passed, the cycle is repeated.

If an EF or ED alone is read from magnetic tape, the EF/ED Simultaneous Indicator is set. The EF/ED Simultaneous Indicator is not set when reading from paper tape. If SMDI is set, the EF/ED Normal Indicator will be set.

If ETW is passed the ETW flip-flop is reset.

Final Register Contents

$(S)_f$ = Address of location one to the left of the last character read.
$(T)_f = (B)_i$

Timing

Hi-Data tapes, Model 381, are read at the rate of 10 KC.

Hi-Data tapes, Model 382, are read at the rate of 30 KC.

Paper tape is read at the rate of up to 1000 characters per second.

The tape station attached to the Tape Adapter or Dual Tape Channel is read at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

8 Tape Write Normal (TWN)

General Description

This instruction transfers a specified series of consecutive characters in HSM to a designated Tape Station, a Paper Tape Punch, Interrogating Typewriter, or Monitor Printer.

Format

Operation — 8
N — Identification character of Tape Station, Paper Tape Punch, Interrogating Typewriter, or Monitor Printer. (See Appendix G.)
A Address — Address of the first location in HSM to be written, punched, or typed.
B Address — Address of the last character in HSM to be written, punched, or typed.

Direction of Operation

Left to right.

Tape Motion

Forward

Outline of Operation

Initially this instruction sends a start signal to the output unit specified by the contents of the N Register and operates in the following cycle:

The contents of the HSM location specified by the A Register are transferred to the output unit specified by the N Register. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(A)_t$ = Address of location one to the right of the last character written, punched or typed.
$(B)_t = (B)_1$

Timing

Hi-Data tapes, Model 381, are written at the rate of 10 KC and Hi-Data tapes, Model 382, are written at the rate of 30 KC. Paper tape is punched at the rate of up to 100 or 300 characters per second.

The tape station attached to the Tape Adapter or Dual Tape Channel is written at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

The Interrogating Typewriter and the Monitor Printer type at the rate of 10 characters per second.

Example

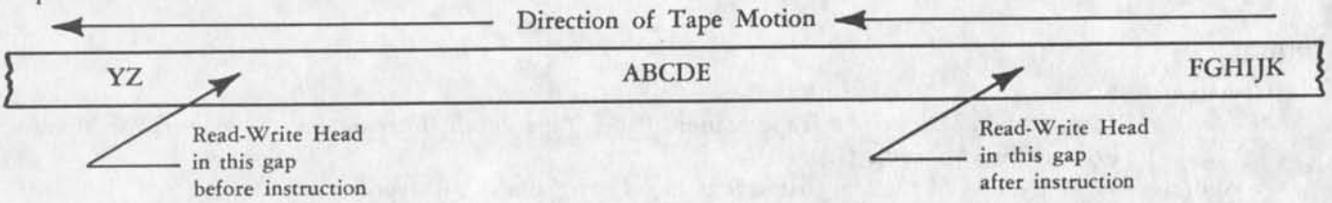
Instruction:

Operation	N	A Address	B Address
8	1	4001	4005

HSM before and after Instruction is Executed:

4000	4001	4002	4003	4004	4005	4006
—	A	B	C	D	E	—

Tape on Station #1:



Final Register Contents:

$(A)_t = 4006$

$(B)_t = 4005$

9 Tape Write Simultaneous (TWS)

General Description

This instruction transfers a specified series of consecutive characters in HSM to a designated Tape Station, Paper Tape Punch, Interrogating Typewriter, or Monitor Printer. This instruction operates in the Simultaneous Mode.

Format

Operation — 9
N — Identification character of Tape Station, Paper Tape Punch, Interrogating Typewriter, or Monitor Printer. (See Appendix G.)
A Address — HSM location of the first character to be written, punched, or typed.
B Address — HSM location of the last character to be written, punched, or typed.

Direction of Operation

Left to right.

Direction of Tape Motion

Forward

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the output unit specified by the contents of the M Register and operates in the following cycle:

The contents of the HSM location specified by the S Register are transferred to the output unit specified by the M Register. The contents of the S Register are compared with the contents of the T Register. The contents of the S Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(S)_f$ = Address of location one to the right of the last character written, punched, or typed.
$(T)_f = (B)_i$

Timing

Hi-Data tapes, Model 381, are written at the rate of 10 KC and Hi-Data tapes, Model 382, are written at the rate of 30 KC.

Paper tape is punched at the rate of up to 100 or 300 characters per second.

The tape station attached to the Tape Adapter or Dual Tape Channel is written at the rate of 33.3 KC if it is a Model 581 Tape Station or 66.7 KC if it is a Model 582 Tape Station.

The Interrogating Typewriter and the Monitor Printer type at the rate of 10 characters per second.

; Rewind to BTC (RWD)

General Description

This instruction causes a designated magnetic tape unit to be completely rewound. Once the operation has been initiated the rewind proceeds totally independent of the Computer, not occupying the Normal, Simultaneous, or Record File Mode. The Computer, after initiating the rewind, is free to execute other instructions.

Format

Operation — ;
N — Identification character of tape station. (See Appendix G.)
A Address — Must be zeros (0000).
B Address — Must be zeros (0000).

Direction of Tape Motion

Reverse

Final Register Contents

After rewind is initiated, the registers are available for use by the next instruction.

Timing

42 μs

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected input/output device and chooses one of two sequences of instructions.

Format

Operation — S

N — Selects the input/output device to be tested according to the following:

Device	N	
	Unit #1	Unit #2
Paper Tape Reader	8	
Paper Tape Punch	9	
Interrogating Typewriter	U	
Hi-Data Tape Group (10 or 30 KC Model)	123456	ABCDEF
Dual Tape Channel (2 x 6 switch 33 or 66 KC Model)[1]	123456	
Dual Tape Channel (2 x 12 switch 33 or 66 KC Model)[2]	123456ABCDEF	
33 KC Adapter	J	N
66 KC Adapter	L	P

Note #1: The 2 x 6 Switch Dual Tape Channel prohibits the inclusion of Hi-Data Tape Group #1.

Note #2: The 2 x 12 Switch Dual Tape Channel prohibits the inclusion of both Hi-Data Tape Groups.

A Address — A_0 specifies the tests to be performed as follows:

Device	"1" Bit In	Numeric Equivalent	Tests
Paper Tape Reader or Paper Tape Punch (100 cps) High Speed Paper Tape Punch (300 cps) High Speed Paper Tape Reader (1000 cps)	2^0	1	Is the selected device inoperable?
	2^1	2	Is the selected device operating?
Interrogating Typewriter	2^0	1	Is the selected device inoperable?
	2^1	2	Has a read parity error occurred? (This indicator is reset by a subsequent read instruction directed to this device.)
	2^2	4	Has "Program Interrogate" been received?
	2^3	8	Has a write parity error occurred? (This indicator is reset by a subsequent read instruction to this device.)
	2^4	&	Has "Message Erase" been received?

(Continued)

A Address — (Continued)

Device	"1" Bit In	Numeric Equivalent	Tests
Magnetic Tape Station	2^0	1	Is the tape station inoperable?
	2^1	2	Is the tape in motion? (Tape motion will not be indicated during a write to read delay.)
	2^2	4	Has ETW been sensed?
	2^3	8	Is the tape positioned on BTC?
	2^4	&	Is the tape moving in a reverse direction?

— A_1, A_2, A_3 — Must be zeros (000).

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_t = (A)_1$

$(B)_t = (B)_1$

Timing

56 μs if a transfer is executed.

42 μs if no transfer takes place.

S Automatic Rollback Control (IOS)

General Description

This instruction will allow the computer program to override the hardware rollback capabilities of the Model 382 and Model 582 Tape Stations. Immediate stopping will occur on all read and/or read after write errors.

Format

Operation — S

N — Selects the device as follows:

Device	N	
	Unit #1	Unit #2
Hi-Data Tape Group, 30 KC	123456	ABCDEF
66 KC Adapter	L	P

A Address — A_0 — Must be zero (0).

A_1 — 4 Allow hardware rollback.

8 Don't allow hardware rollback.

A_2, A_3 — Must be zeros (00).

B Address — Must be zeros (0000).

Outline of Operation

The command called for by the one bits in A_1 are sent to the control module selected by N. If the "don't allow hardware rollback" option is selected, the computer will halt on all read and/or read after write errors. If the "allow hardware rollback" option is selected, automatic hardware rollback will be initiated on all read and read after write errors.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

42 μs.

S Sense Read Error (IOS)

General Description

This instruction is to be used in conjunction with the Read Error Sense Enhancement for Model 381 Tape Stations. It has two functions as follows:

1. Set the Program Control Switch

Format

Operation — S
N — M
A Address — A_0, A_1, A_2 — Must be zeros (000).
A_3 — 1 Set Read Error Sense Enhancement OFF.
— 2 Set Read Error Sense Enhancement ON.
B Address — Must be zeros (0000).

2. Sense for Read Parity Error (RE)

Format

Operation — S
N — M — First Control Module 318 (1 - 6).
& — Second Control Module 319 (A - F).
A Address — A_0 = 4 Sense for Read Parity Error.
A_1, A_2, A_3 — Must be zeros (000).
B Address — HSM location of the next instruction to be executed when the Read Parity Indicator is sensed and found set.

Standard Location

STP (on transfer only)

Note: The A_0 and A_3 options cannot be used in combination. Therefore, an IOS instruction should be used for setting the Programmed Control Switch and another IOS instruction should be given for the test function.

Outline of Operation

The Programmed Control Switch is set ON or OFF by the proper bit setting in A_3. The test called for by the 4 in A_0 is performed on the control module selected by N. If the condition tested (RE) is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

Function 1
42 μs.

Function 2
56 μs if a transfer is executed.
42 μs if no transfer takes place.

X — INPUT/OUTPUT INSTRUCTIONS — PRINTER

B Print & Paper Advance Normal (PAN)

General Description

This instruction can cause the contents of 120 or 160 consecutive HSM locations, beginning with an even hundred HSM address, to be transferred to the On-Line Printer, initiating the printing of one line. It can advance paper a specified number of lines according to the contents of N, or by the punches in the paper tape loop of the printer.

Format

Operation — B

N — Number of lines (0-14) to advance paper if B_3 equals 1:

	Asynchronous Mode															Synchronous Mode*
Number of lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1
First Printer	0	1	2	3	4	5	6	7	8	9	space	#	@	(	)	J
Second Printer	&	A	B	C	D	E	F	G	H	I	+	.	;	:	'	/

*B_3 must equal 1.

A Address — Must be zeros (0000).

B Address — Address of data to be printed from HSM excluding B_3.

B_0 — MSD of address.

B_1 — When this digit is even, printing will occur. If odd, the line will not be printed.

B_2 — *Unbuffered Printer*

$B_2 = 0$ — This will cause 120 characters or 160 characters to be printed depending on the printer model.

Buffered Printer

$B_2 = 0$ — This will cause 120 characters to be printed regardless of the printer model.

$B_2 = 2$ — This will cause 160 characters to be printed on the 160 column printer.

B_3 — Has the function of indicating the type of paper advance as follows:

Type of Paper Advance	B_3
No Paper Advance	0
Paper Advance Using N Register as count	1
Vertical Tab (using tape loop)	2
Page change (using tape loop)	3

Direction of Operation

Left to right.

Outline of Operation

The paper advance information given by B_3 is stored in indicators. The B_3 character is set to zero. If printing is to take place the contents of the B Register are transferred to the A Register. If the printer is a buffered device, the print table is transferred from the standard print table locations to the printer buffer and the data line is transferred to the buffer in accordance with the contents of the A Register. Data transfer is by diad, at the rate of 14 microseconds per diad. The instruction is terminated on transfer of the last diad. Printing is accomplished off-line, with the printer referencing the table and the data line in buffer storage. The buffer can be loaded for the next print line while the printer is executing paper advance for a prior instruction.

If the printer is an unbuffered device, the print table and the data line are accessed in the High-Speed Memory. As the print drum revolves, the printer sends signals to the Computer indicating which character on the print drum will next be in the print position. These printer signals are used to develop an address for an automatic table lookup operation. This operation extracts from the Print Table (see Appendix H) the RCA 301 character which is to be printed next. This character is stored in the Print Register. The diad addressed by the A Register is read out of HSM and checked for the character stored in the Print Register. The contents of the A Register are increased by two and the cycle is repeated. Modification of the contents of the A Register and checking of the addressed diad continue until 120 or 160 consecutive memory locations have been checked. This checking for one character is known as a "scan."

As each character is checked a one bit is sent to the printer shift register for an equality, a zero bit is sent for each non-equality. At the completion of a scan the shift register contains a one bit in every position on the line in which this character is to be printed. The one bits are then used to trigger the corresponding print hammers. The contents of the B Register are again transferred to the A Register, a new character is read from the Print Table, and another scan is begun.

There are two modes of operation, Synchronous and Asynchronous. The Synchronous Mode permits only 47 characters to be printed since a complete line of print and paper advance to the next print line is accomplished during each revolution of the print drum. The letter "A" is always the first character for which HSM is scanned, and the period is the last.

The Asynchronous Mode permits all 64 characters on the print drum to be printed (120 or 160 characters per line) in one full revolution, and paper advance occurs in a portion of the next print drum revolution. Scanning can proceed with the next character in sequence on the print drum at the conclusion of the paper advance function.

Appendix H shows print table containing RCA 301 characters. The code $(17)_8$ is used to inhibit printing of certain characters on the print drum. An inhibited character may be used to specify a non-represented RCA 301 character by substituting the RCA 301 character's bit configuration into the proper print table position. For example, the EB symbol may be printed as "÷" by inserting $(72)_8$ in location 9933, or I933, or Z933 of the print table.

Final Register Contents

$(A)_f$ = Address of location one to the right of the last character printed if printing is done, otherwise it is $(A)_i$.
$(B)_f = (B)_i$ except that B_3 will be set to zero.

Timing

Print and paper advance of one line takes 60 ms. in the Synchronous Mode or 76 ms. in the Asynchronous Mode. When more than one line is to be advanced, paper advancing is done at the rate of 6.67 ms. per line after the first line.

Example

Instruction:

Operation	N	A Address	B Address
B	1	0000	1201

HSM before and after Instruction is Executed:

(First Character Printed) (Last Character Printed)

1200	1201	1318	1319
1	2	8	9

Paper is advanced one line after the printing of the line.

Final Register Contents:
$(A)_f = 1320$
$(B)_f = 1200$

Time:
76 ms.

C Print & Paper Advance Simultaneous (PAS)

General Description

This instruction can cause the contents of 120 or 160 consecutive HSM locations, beginning with an even hundred HSM address, to be transferred to the On-Line Printer, initiating the printing of one line. It can advance the paper a specified number of lines designated by N or by the punches of the paper tape loop of the printer. This instruction is executed in the Simultaneous Mode.

Format

Operation — C

N — Number of lines (0-14) to advance paper if B_3 equals 1:

	Asynchronous Mode															Synchronous Mode*
Number of lines	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	1
First Printer	0	1	2	3	4	5	6	7	8	9	space	#	@	(	)	J
Second Printer	&	A	B	C	D	E	F	G	H	I	+	.	;	:	'	/

*B_3 must equal 1.

A Address — Must be zeros (0000).

B Address — Address of the data to be printed from HSM except for B_3.

B_0 — MSD of address.

B_1 — When this digit is even, printing will occur. If odd, the line will not be printed.

B_2 — *Unbuffered Printer*

$B_2 = 0$ — This will cause 120 characters or 160 characters to be printed depending on the printer model.

Buffered Printer

$B_2 = 0$ — This will cause 120 characters to be printed regardless of the printer model.

$B_2 = 2$ — This will cause 160 characters to be printed on the 160 column printer.

B_3 — Has the function of indicating the type of paper advance as follows:

Type of Paper Advance	B_3
No paper advance	0
Paper advance using N Register as count	1
Vertical Tab (using tape loop)	2
Page Change (using tape loop)	3

* A Simultaneous Paper Advance only instruction is not permitted.

Direction of Operation

Left to right.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, and T Registers respectively, and this instruction is executed in the Simultaneous Mode. The paper advance information given by T_3 is stored in indicators. The T_3 character is set to zero. If printing is to take place the contents of the T Register are transferred to the S Register. If the printer is a buffered device, the print table is transferred from the standard print table locations to the printer buffer and the data line is transferred to the buffer in accordance with the contents

of the A Register. Data transfer is by diad, at the rate of 14 microseconds per diad. The instruction is terminated on transfer of the last diad. Printing is accomplished off-line, with the printer referencing the table and the data line in buffer storage. The buffer can be loaded for the next print line while the printer is executing paper advance for a prior instruction.

If the printer is an unbuffered device, the print table and the data line are accessed in the High-Speed Memory. As the print drum revolves, the printer sends signals to the Computer indicating which character on the print drum will next be in the print position.

These printer signals are used to develop an address for an automatic table look-up operation. This operation extracts from the Print Table (see Appendix H) the RCA 301 character which is to be printed next. This character is stored in the Print Register. The diad addressed by the S Register is read out of HSM and checked for the character stored in the Print Register. The contents of the S Register are increased by two and the cycle is repeated. Modification of the contents of the S Register and checking of the addressed diad continue until 120 or 160 consecutive memory locations have been checked. This checking for one character is known as a "scan."

As each character is checked a one bit is sent to the printer shift register for an equality, a zero bit is sent for each non-equality. At the completion of a scan the shift register contains a one bit in every position on the line in which this character is to be printed. The one bits are then used to trigger the corresponding print hammers. The contents of the T Register are again transferred to the S Register, a new character is read from the translate table, and another scan is begun.

There are two modes of operation, Synchronous and Asynchronous. The Synchronous Mode permits only 47 characters to be printed since a complete line of print and paper advance to the next print line is accomplished during each revolution of the print drum. The letter "A" is always the first character for which HSM is scanned, and the period is the last.

The Asynchronous Mode permits all 64 characters on the print drum to be printed (120 or 160 characters per line) in one full revolution, and paper advance occurs in a portion of the next print drum revolution. Scanning can proceed with the next character in sequence on the print drum at the conclusion of the paper advance function.

Appendix H shows a print table containing RCA 301 characters. The code $(17)_8$ is used to inhibit printing of certain characters on the print drum. An inhibited character may be used to specify a non-represented RCA 301 character by substituting the RCA 301 character's bit configuration into the proper print table position. For example, the EB symbol may be printed as "÷" by inserting $(72)_8$ in location 9933, or I933, or Z933 of the print table.

Final Register Contents

$(S)_f$ = Address of location one to the right of the last character printed if printing is done; otherwise, it is $(A)_i$.
$(T)_f = (B)_i$ except that B_3 will be set to zero.

Timing

Print and paper advance of one line takes 60 ms. in the Synchronous Mode or 76 ms. in the Asynchronous Mode. When more than one line is to be advanced, paper advancing is done at the rate of 6.67 ms. per line after the first line.

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected printer and chooses one of two sequences of instructions.

Format

Operation — S

N — Selects the printer to be tested according to the following:

Device	N	
	Unit #1	Unit #2
On-Line Printer	7	G

A Address — A_0 specifies the tests to be performed as follows:

Device	"1" Bit In	Numeric Equivalent	Tests
On-Line Printer (Unbuffered)	2^0	1	Is the selected device inoperable?
	2^1	2	Is a line being printed?
	2^4	&	Is the paper advancing?
On-Line Printer (Buffered)	2^0	1	Is the selected device inoperable?
	2^1	2	Is the printer busy? (This indicator is set at the start of buffer loading and remains set through completion of the last scan. It is also set when the printer cover is open.)
	2^2	4	Is the low paper flip-flop set? (Has end of paper supply passed the low paper photocell?)
	2^4	&	Is the paper advancing?

— A_1, A_2, A_3 — Must be zeros (000).

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

56 μs if a transfer is executed.

42 μs if no transfer takes place.

XI — INPUT/OUTPUT INSTRUCTIONS — DATA RECORD FILE

D Band Select Normal (BSN)

General Description

This instruction initiates a search of a designated Data Record File for the record containing a specified band, places the record on the turntable and advances the read/write arm to the "ready" position. Once this instruction is initiated (staticizing and establishing a control counter), the data record and band are selected independent of computer operation.

A Band Select Normal instruction must be issued prior to a Block Read (or Write) Record Normal (or Simultaneous) instruction (BRN, BRS, BWN, BWS). These instructions may be used to address one of two Data Record Files controlled through a Data Record File Control.

Format

Operation — D

N — Selects the Data Record File Unit and Band as indicated below:

1st File	2nd File	Effect
0	&	The record on the turntable, if any, will be returned to the cage. The desired record is then placed on the turntable and the indicated band selected.
1	A	The band selected is one of the two on the upside of the record on the turntable. If the B address is even, the first band will be selected; if odd, the second band will be selected.

A Address — Must be zeros (0000).

B Address — B_0 must be zero (0); B_1, B_2, B_3 designate band (000 to 511).

Outline of Operation

Band addresses are numbered from 000 through 511 and are specified by the last three digits of the B address. The contents of the N Register designate the proper Data Record File and specify whether the record on the turntable, if any, is to be returned to the cage or not.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

A. Computer time to initiate selection (staticizing and establishing address counter) in microseconds: 21 (B_1) + 14 (B_2) + 42.

B. Select data record from storage wheel:

Note. Since the 128 position data record storage wheel rotates in either direction, the maximum data record position from the selection point is 64.

Number of Data Record Positions Rotated	Time (in seconds)*
1	1.6
2	1.8
3	2.0
4	2.2
5	2.4
6	2.6
7	2.8
8	3.0
9	2.65
16	2.8
32	3.1
64	3.4

* Variance ±10%

Note: Cage rotation has two speeds

a. slow speed (from one to eight data record positions from selection point).

b. fast speed (from nine to 64 data record positions from selection point). Use straight line interpolation for interim positions on table.

C. Additional timing information

1. To select band on opposite side of data record on turntable (head at ready to head at ready) = 3.4 sec.
2. To select adjacent band of data record on turntable and return head to ready = 0.9 sec.

E Band Select Record File Mode (BSM)

General Description

This instruction initiates a search of a designated Data Record File for the record containing a specified band, places the record on the turntable and advances the read/write arm to the "ready" position. Once this instruction is initiated (staticizing and establishing a control counter), the data record and band are selected independent of computer operation.

A Band Select Record File Mode instruction must be issued prior to a Record File Mode Read (or Write) instruction (RMR, RMW). These instructions may be used to address one of four Data Record Files controlled through the Data Record File Mode Control.

Format

Operation — E

N — Selects the Data Record File Unit and Band as indicated below:

Data Record File Unit				Effect
1	2	3	4	
0	&	—	"	The record on the turntable, if any, will be returned to the cage. The desired record is then placed on the turntable and the indicated band selected.
1	A	J	/	The band selected is one of the two on the upside of the disc on the turntable. If the B address is even, the first band will be selected; if odd, the second band will be selected.

A Address — Must be zeros (0000).

B Address — B_0 must be zero (0); B_1, B_2, and B_3 designate band (000 to 511).

Outline of Operation

Band addresses are numbered from 000 through 511, and are specified by the last three digits of the B address. The contents of the N Register designate the proper Record File and specify whether the record on the turntable, if any, is to be returned to the cage or not.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

A. Computer time to initiate selection (staticizing + establishing address counter) in microseconds: 21 (B_1) + 14 (B_2) + 42.

B. Select data record from storage wheel:

Note: Since the 128 position data record storage wheel rotates in either direction, the maximum data record position from the selection point is 64.

Number of Data Record Positions Rotated	Time (in seconds)*
1	1.6
2	1.8
3	2.0
4	2.2
5	2.4
6	2.6
7	2.8
8	3.0
9	2.65
16	2.8
32	3.1
64	3.4

* Variance ±10%

Note: Cage rotation has two speeds

a. slow speed (from one to eight data record positions from selection point).

b. fast speed (from nine to 64 data record positions from selection point). Use straight line interpolation for interim positions on table.

C. Additional timing information

1. To select band on opposite side of data record on turntable (head at ready to head at ready) = 3.4 sec.
2. To select adjacent band of data record on turntable and return head to ready = 0.9 sec.

F Block Read Record Normal (BRN)

General Description

This instruction reads from a selected cell of the Data Record File to a designated HSM location. From one to ten blocks of information may be transferred from the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information to be transferred. In reading, the end of the block of information is designated by an EB symbol, or a count of 900 characters in the cell.

Format

Operation — F

N — Selects the Data Record File Unit and number of blocks to be read as indicated below:

Number of Blocks to be Read	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address — HSM address where first character is to be placed.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB is sensed or not.

$B_2 = 1$ — block is terminated on counting of 900 characters.

$B_2 = 0$ — count or EB recognition.

If EB sensed before 900 characters have been read, stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right in HSM.

Standard Location

STA (0212 - 0215)

Outline of Operation

A start signal is sent to the Data Record File and the read-write head is placed on the record on the turntable. The contents of the cell specified in B_3 are transferred to the Record File Buffer and from the buffer to the HSM location designated by the A Register. Transfer is accomplished one character at a time, with the contents of the A Register being incremented by one after each character transferred. When the end of a block is reached, determined by B_2, N is decreased by one. When N is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional read or write instructions from the same surface.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character put in memory.

$(B)_f = (B)_i$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N 2^0 = 1)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

G Block Read Record Simultaneous (BRS)

General Description

This instruction reads from the Data Record File controlled by the Record File Control Unit to a designated HSM location. From one to ten blocks of information may be transferred from the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information to be transferred. In reading, the end of the block of information is designated by an EB symbol, or a count of 900 characters in the cell. This instruction is performed in the Simultaneous Mode.

Format

Operation — G

N — Selects the Data Record File Unit and number of blocks to be read as indicated below:

Number of Blocks to be Read	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address — HSM location where first character is to be placed.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB sensed or not.

$B_2 = 1$ — block is terminated on counting of 900 characters.

$B_2 = 0$ — count or EB recognition.

If EB sensed before 900 characters have been read, stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B Registers are transferred to the SOR, M, S, T Registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Record File. The contents of the cell specified in T_3 are transferred to the Record File Buffer and when the Normal Mode is interruptable, from the buffer to the HSM location designated by the S Register. Transfer is accomplished one character at a time, with the contents of the S Register being incremented by one after each character transferred. When the end of a block is reached, determined by T_2, M is decreased by 1. When M is decreased to zero, the operation is terminated. The record does not have to be returned to the cage to perform additional read or write instructions on the same surface.

Final Register Contents

$(S)_f$ = Address of HSM location one to the right of the last character put in memory.

$(T)_f = (B)_1$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N 2^0 = 1)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

H Block Write Record Normal (BWN)

General Description

This instruction writes from a selected HSM location to designated cells of the Data Record File under control of the Record File Control Unit. From one to ten blocks of information may be transferred to the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information. In writing, a block is terminated by an End of Block (EB) Symbol or a cell count of 900 characters.

Format

Operation — H

N — Selects the Data Record File Unit and number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address — HSM address of first character to be written to the Record File.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB sensed or not.

B_2 = 1 — block is terminated on counting of 900 characters.

B_2 = 0 — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer into this cell. If 900 count reached before an EB sensed, stop transfer into this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right.

Outline of Operation

A start signal is sent to the Data Record File and the arm is placed on the previously selected record on the turntable. The contents of the HSM location specified by the A address are transferred to the Data Record File Buffer and from the buffer to the specified cell. The contents of the A Register are incremented by one, and the contents of the next memory location are then transferred. When the end of a block is reached, determined by B_2, N is decreased by one. When N is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional read or write instructions to the same surface.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character written.

$(B)_f = (B)_i$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N 2^0 = 1)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

I Block Write Record Simultaneous (BWS)

General Description

This instruction writes from a designated HSM location to selected Data Record File cells. From one to ten blocks of information may be transferred to the Data Record File with one instruction. A cell may contain a block of one to 900 characters of information. In writing, a block is terminated by an End of Block (EB) Symbol or a cell count of 900 characters. This instruction is performed in the Simultaneous Mode.

Format

Operation — I

N — Selects the Data Record File Unit and the number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&

A Address — HSM address of first character to be written.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB sensed or not.

$B_2 = 1$ — block is terminated on counting of 900 characters.

$B_2 = 0$ — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer to this cell. If 900 count reached before an EB sensed, stop transfer to this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S, T Registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Data Record File and the arm is placed on the previously selected record on the turntable. As soon as the Normal Mode is interruptable, the contents of the HSM location specified by the S Register are transferred to the Record File Buffer and from the buffer to the specified cell. The contents of the S Register are increased by one and the contents of the HSM location now addressed by the S Register are transferred in a like manner. When the end of a block is reached, determined by T_2, M is decreased by one. When M is decreased to zero the operation terminates. The record does not have to be returned to the cage to perform additional reads or writes to the same surface.

Final Register Contents

$(S)_f$ = HSM address of location one to the right of the last character written.

$(T)_f = (B)_1$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N 2^0 = 1)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

* Record File Mode Read (RMR)

General Description

This instruction reads from selected cells located in one of the four Data Record Files connected to the Data Record File Mode Control Unit. From one to ten blocks of information may be transferred from a Data Record File and placed in HSM with one instruction. Each cell may contain a block of information consisting of from one to 900 characters. In reading, the end of the block is designated by an EB symbol or a count of 900 characters in the cell.

Format

Operation — *

N — Selects the Data Record File Unit and the number of blocks to be read as indicated below:

Number of Blocks to be Read	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&
Third File	J	K	L	M	N	O	P	Q	R	— minus
Fourth File	/	S	T	U	V	W	X	Y	Z	"

A Address — HSM location where first character is to be placed.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB sensed or not.

B_2 = 1 — block is terminated on counting of 900 characters.

B_2 = 0 — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer from this cell. If 900 count reached before an EB sensed, stop transfer from this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right in HSM.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Record File Mode is free, the contents of the NOR, N, A, and B Registers are transferred to the FOR, L, U, and V Registers respectively, and this instruction is executed in the Record File Mode. A start signal is sent to the selected Data Record File and the arm is placed on the previously selected record on the turntable. The contents of the cell specified in V_3 are transferred to the Data Record File Mode Buffer, and when the Normal Mode is interruptable, from the buffer to the HSM location specified by the U Register. Transfer is accomplished one character at a time with the contents of the U Register being incremented by one after each character transferred. When the end of a block is reached, determined by V_2, L is decreased by one. When L is decreased to zero, the operation terminates. This record does not have to be returned to the cage to perform other reads or writes on the same surface.

Final Register Contents

$(U)_f$ = HSM address of location one to the right of the last character placed in memory.

$(V)_f = (B)_1$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N 2^0 = 1)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

% Record File Mode Write (RMW)

General Description

This instruction writes from a selected HSM location to designated cells in one of the four Data Record Files connected to the Data Record File Mode Control Unit. From one to ten blocks of information may be transferred to the Record File with one instruction. A cell can contain a block of information of from one to 900 characters. In writing, a block is terminated by an End of Block (EB) Symbol, or a cell count of 900 characters.

Format

Operation — %

N — Selects the Data Record File Unit and the number of blocks to be written as indicated below:

Number of Blocks to be Written	1	2	3	4	5	6	7	8	9	10
First File	1	2	3	4	5	6	7	8	9	0
Second File	A	B	C	D	E	F	G	H	I	&
Third File	J	K	L	M	N	O	P	Q	R	— minus
Fourth File	/	S	T	U	V	W	X	Y	Z	"

A Address — HSM address of first character to be written to the Record File.

B Address — B_0 must be zero (0).

B_1 determines if record stays on turntable after operation.

B_1 = odd — record returned to cage.

B_1 = even — record stays on turntable and arm is placed at beginning of previously selected band.

B_2 specifies whether EB sensed or not.

$B_2 = 1$ — block is terminated on counting of 900 characters.

$B_2 = 0$ — count or EB recognition.

If EB sensed before 900 characters have been written, stop transfer to this cell. If 900 count reached before an EB sensed, stop transfer into this cell.

B_3 addresses cells 1 through 10, with cell 1 specified by zero and cell 10 specified by 9.

Direction of Operation

Left to right in HSM.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Record File Mode is free, the contents of the NOR, N, A, and B Registers are transferred to the FOR, L, U, and V Registers respectively, and this instruction is executed in the Record File Mode. A start signal is sent to the selected Data Record File and the arm is placed on the previously selected disc on the turntable. As soon as the Normal Mode is interruptable, the contents of the HSM location specified by the U Register are transferred to the Record File Mode Buffer and from the buffer to the specified cell. The contents of the U Register are increased by one and the contents of the HSM location now addressed by the U Register are transferred in a like manner. When the end of a block is reached, determined by V_2, L is decreased by one. When L is decreased to zero, the operation terminates. The record does not have to be returned to the cage to perform other read or writes to the same surface.

Final Register Contents

$(U)_f$ = Address of location one to the right of the last character written on the record.

$(V)_f = (B)_1$

Timing

1. Data Record positioned on turntable and read/write arm in "ready" position:	
a. Read/write arm transferred to data record	0.62 to 0.85 sec.*
b. Latency (to reach first character of first cell on data record)	0.2 to 0.4 sec.
c. Inter cell gap	0.04 sec.**
d. Character transfer rate	2,500 char/sec.
(1) Transfer time per cell — (characters and gap)	0.4 sec.
e. Return read/write arm to "ready" position (data record stays on turntable (B_1 = Even), but band select instruction does not follow within 0.4 sec.) (Band select — N $2^0 = 1$)	0.9 sec.*
2. Return data record from turntable to record storage wheel:	
a. Read/write arm on data record (B_1 = Odd)	1.6 sec.*
b. Read/write arm in "ready" position	1.84 sec.*

* The computer is free during these times.

** Fixed time between 900-character cells.

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected Data Record File and chooses one of two sequences of instructions.

Format

Operation — S

N — Selects the Data Record File to be tested according to the following:

Device	N	
	Unit #1	Unit #2
Data Record File (under control of DRFC Unit)[1]	R	Z
Data Record File (under DRFM Control Unit)	#$.,	

Note #1: Data Disc File #1 prohibits the inclusion of Data Record File #1 operated through the DRFC. Data Disc File #2 prohibits the inclusion of Data Record File #2 operated through the DRFC.

A Address — A_0 specifies the tests to be performed as follows:

"1" Bit In	Numeric Equivalent	Tests
2^0	1	Is the selected device inoperable?
2^1	2	Is the selected device reading or writing?
2^2	4	Is a record on the turntable of the selected Data Record File?

— A_1, A_2, A_3 — Must be zeros (000).

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

56 μs if a transfer is executed.
42 μs if no transfer takes place.

XII — INPUT/OUTPUT INSTRUCTIONS — DATA DISC FILE

2 FILES / MACHINE
4 MODULES / FILE
24 DISKS / MODULE
22 118 400 char / Module

STRATA

6 ZONES / DISK SURFACE
9 DATA ZONES / " "
128 TRACKS / ZONE
10 SECTORS / TRACK
160 char / SECTOR

176 947 200 char / 2 FILES

D Track Select (TS)

General Description

This instruction positions the read/write heads over 1 of 128 tracks. Once initiated the track selection is performed independently of computer operation.

Format

Operation — D
N — R (First Data Disc File)
— Z (Second Data Disc File)
A Address — Must be zeros (0000).
B Address — $B_0 = 0$ (zero), will not override a DDF Simultaneous Instruction.
— $B_0 =$ &, will override any DDF Simultaneous Instruction.
— B_1, B_2, B_3 designate track address (000 - 127).

Outline of Operation

The contents of the N Register specify the proper Data Disc File. B_1, B_2, B_3 designate the track address which can range from 000 to 127. All read/write heads within a Data Disc File are positioned concurrently so that 108 zones per module are accessible by the execution of one Track Select instruction.

If this instruction contains a bit in the B_0 2^4 position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

To initiate selection, 42 μsec.

To perform Track Selection (time in milliseconds):

Model	Average	Maximum
363-2	105	150
363-3	125	160
363-4	145	185
363-5	145	185

F Sector Read Disc Normal (SRN)

General Description

This instruction reads from a selected sector of the Data Disc File to a designated HSM location. From one to ten sectors of information may be transferred from the Data Disc File with one instruction. 160 characters are transferred for each sector designated.

Format

Operation — F

N — Specifies additional number of sectors to be read as follows:

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address — Address of HSM location to receive the first character read from the Data Disc File. This address must be an even number (left-hand end of a diad).

B Address — B_0 — designates first sector to be read:

First Sector to be Read	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B_1, B_2, B_3 — specify the zone from which data is to be read:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

Direction of Operation

Left to right in HSM

Standard Location

STA (0212 - 0215)

Outline of Operation

A start signal is sent to the Data Disc File and the contents of the sector specified by the B address are transferred to the Data Disc File Buffer and from the buffer to the HSM location, designated by the A Register. Transfer is effected two characters at a time, with the contents of the A Register being incremented by two after each pair of characters is transferred. When the additional number of sectors has been read, according to the N character, the operation terminates.

If a character with faulty parity is read, an octal 57 (57_8) will be stored in HSM in place of the faulty character. An indicator will also be set and will remain set until another read instruction is started.

If this instruction contains a bit in the B_0 2^4 position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character put in memory.

$(B)_f = (B)_i$

Timing

Characters are read at the rate of 32 KC.

Five milliseconds are required to read one sector.

The average time to get to the designated sector is 25 milliseconds (file latency).

G Sector Read Disc Simultaneous (SRS) not used

General Description

This instruction reads from a selected sector of the Data Disc File to a designated HSM location. From one to ten sectors of information may be transferred from the Data Disc File with one instruction. 160 characters are transferred for each sector designated. However, this instruction may be terminated by any other Data Disc File instruction to the same file when the terminating instruction has the proper B_0 override character.

Format

Operation — G

N — Specifies additional number of sectors to be read as follows:

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address — Address of HSM location to receive the first character read from the Data Disc File. This address must be an even number (left-hand end of a diad).

B Address — B_0 designates first sector to be read:

First Sector to be Read	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B_1, B_2, B_3 — specify zone from which data is to be read:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

Direction of Operation

Left to right in HSM.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B Registers are transferred to the SOR, M, S, T Registers respectively, and this instruction is executed in the Simultaneous Mode. A start signal is sent to the Data Disc File. The contents of the sector, as specified by the T Register are transferred to the Data Disc File Buffer, and when the Normal Mode is interruptable, from the buffer to the HSM location designated by the S Register. Transfer is accomplished two characters at a time, with the contents of the S Register being increased by two after each pair of characters is transferred. When the additional number of sectors has been read, according to the N character, the operation terminates.

The operation may also be terminated by another Data Disc File instruction to the same file when the B_0 character of the overriding instruction ranges from "&" to "I" as specified above.

If a character with faulty parity is read, an octal 57 (57_8) will be stored in HSM in place of the faulty character. An indicator will also be set and remain set until another read instruction is started.

If this instruction contains a bit in the B_0 2^4 position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

Final Register Contents

$(S)_f$ = Address of HSM location one to the right of the last character transferred into memory.
$(T)_f = (B)_i$

Timing

Characters are read at the rate of 32 KC.

Five milliseconds are required to read one sector into HSM.

The average time to get to the designated sector is 25 milliseconds (file latency).

H Sector Write Disc Normal (SWN)

General Description

This instruction writes from a selected HSM location to designated sectors of the Data Disc File. From one to ten sectors of information may be transferred to the Data Disc File with one instruction. 160 characters are transferred for each sector written.

Format

Operation — H
N — Specifies additional number of sectors to be written.

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address — HSM address of the first character to be written. This address must be an even number (left-hand-end of a diad).

B Address — B_0 — designates the first sector to be written:

First Sector to be Written	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B_1, B_2, B_3 — specify zone to which data is to be written:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

Direction of Operation

Left to right in HSM.

Outline of Operation

The contents of the HSM diad specified by the A Address are transferred to the Data Disc File Buffer and from the buffer to the specified sector. The contents of the A Register are incremented by two, and the contents of the next diad are then transferred. When the additional number of sectors has been written, according to the N character the operation terminates.

If this instruction contains a bit in the B_0 2^4 position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character written.
$(B)_f = (B)_i$

Timing

Characters are written at the rate of 32 KC.

Five milliseconds are required to write one sector.

The average time to get to the sector designated is 25 milliseconds (file latency).

I Sector Write Disc Simultaneous (SWS)

General Description

This instruction writes from a selected HSM location to designated sectors of the Data Disc File. From one to ten sectors of information may be transferred to the Data Disc File with one instruction. 160 characters are transferred for each sector written; however, this instruction may be terminated by any other Data Disc File instruction to the same File when the terminating instruction has the proper B_0 override character.

Format

Operation — I

N — Specifies additional number of sectors to be written.

Additional Sectors	0	1	2	3	4	5	6	7	8	9
First File	0	1	2	3	4	5	6	7	8	9
Second File	&	A	B	C	D	E	F	G	H	I

A Address — HSM Address of the first character to be written. This address must be an even number (left-hand-end of a diad).

B Address — B_0 — designates the first sector to be written:

First Sector to be Written	0	1	2	3	4	5	6	7	8	9
Will Not Override Any DDF Simultaneous Instruction	0	1	2	3	4	5	6	7	8	9
Will Override Any DDF Simultaneous Instruction	&	A	B	C	D	E	F	G	H	I

B_1, B_2, B_3 — specifies zone to which data is to be written:

Module	Zone
1	000 to 107
2	108 to 215
3	216 to 323
4	324 to 431

Direction of Operation

Left to right in HSM.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the Simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A and B Registers are transferred to the SOR, M, S and T Registers, respectively; and this instruction is executed in the Simultaneous Mode. As soon as the Normal Mode is interruptable, the contents of the HSM diad specified by the S Register are transferred to the Data Disc File Buffer and from the buffer to the specified sector. The contents of the S Register are increased by two, and the contents of the diad specified transferred in a like manner. When the additional number of sectors has been written, according to the N character, the operation terminates.

The operation may also be terminated by another Data Disc File instruction to the same file when the B_0 character of the overriding instruction ranges from "&" to "I" as specified above.

If this instruction contains a bit in the B_0 2^4 position and the selected Data Disc File is busy in the Simultaneous Mode, the Simultaneous Instruction being performed will be terminated on the next transfer of data to or from the file. The new instruction will then be executed in the normal manner.

Final Register Contents

$(S)_f$ = Address of HSM location one to the right of the last character transferred from memory.
$(T)_f = B_1$

Timing

Characters are read at the rate of 32 KC.

Five milliseconds are required to write one sector.

The average time to get to the sector is 25 milliseconds (file latency).

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected Data Disc File and chooses one of two sequences of instructions.

Format

Operation — S

N — Selects the Data Disc File to be tested according to the following:

Unit #1	Unit #2
R	Z

Note: Data Record File #1 operated through the DRFC prohibits the inclusion of Data Disc File #1.
Data Record File #2 operated through the DRFC prohibits the inclusion of Data Disc File #2.

A Address — A_0 specifies the tests to be performed as follows:

"1" Bit In	Numeric Equivalent	Tests
2^0	1	Is the selected device inoperable?
2^1	2	Is the selected device busy? (This indicator is set during track selecting, reading and writing to the Data Disc File.)
2^2	4	Is the track select complete?
2^3	8	Has incorrect parity been read?

— A_1, A_2, A_3 — Must be zeros (000).

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_t = (A)_i$
$(B)_t = (B)_i$

Timing

56 μs if a transfer is executed.
42 μs if no transfer takes place.

ONLY SENDING COMPUTER CAN SH 0001
A STOPS until B is Ready
IF B HALTS BEFORE COMPLETION, A HALTS
" A " " " B " ≥ 57₈ in B
UNTIL A=B

XIII — INPUT/OUTPUT INSTRUCTIONS — DATA EXCHANGE CONTROL

A → B

SH 1001 .... 0 IOS HAS B STATICISED AN IOS
SH 1000 .... 1 IOS IS B OPER
SH 0001 .... 2 IOS IS CH FREE A_3=1
BH 1000 2000 3 TWN
Sig sent on DXC to B

TRANSMIT MODE WHEN A=B
and ALL DATA IS IN (BUFFER) DXC

B

SH 1000 .... 1 IOS IS A OPER
SH 4000 .... 2 IOS IS DXC_A in TRANSMIT MODE
4H 1000 1998 3 RFN
TRANSFERS UNTIL A=B in A ∝ B
SH 4000 .... 4 IOS IS A IN TRANSMIT MODE
IF YES, A=B was not reached in A — RFN again, (go to 3).

4 Tape Read Forward Normal (RFN)

General Description

This instruction is used to receive data into the HSM of one processor from the HSM of another processor provided both are equipped with a Data Exchange Control. This instruction operates in the Normal Mode. Receipt of data will terminate when the terminate signal is received from the sending computer or by AB equality.

Format

Operation — 4
N — H (first unit)
I (second unit)
A Address — Location in HSM which is to receive the first diad transferred. This address must be even.
B Address — Location in HSM which is to receive the last diad transferred. This address must be even.

Direction of Operation

Left to right.

Standard Location

STA (0212 - 0215)

Outline of Operation

Same as the Tape Read Forward Normal instruction for tape (pg. IX-3) with the following exceptions:

1. The PRI's are not affected.
2. The EF/ED Normal Indicator is not affected.
3. When this instruction is staticized, a flip-flop is set in the sending computer which, when sensed, will indicate that this computer is in the receiving mode.
4. All characters received by the Data Exchange Control are checked for correct parity. If a character with incorrect parity is received, octal 57 is substituted for it and placed in HSM, the IOS flip-flop (A_0 2^3) is set in each Data Exchange Control and the data transmission continues.
5. This instruction is terminated by AB equality or by receipt of a terminate signal from the sending computer.

Final Register Contents

If the instruction is terminated by AB equality.
$(A)_t = (B)_i + 2$
$(B)_t = (B)_i$

If the instruction is terminated by receipt of the terminate signal.
$(A)_t = (A)_i$ + the number of characters transferred + 2.
$(B)_t = (B)_i$

Timing

The data transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both processors.

5 Tape Read Forward Simultaneous (RFS)

General Description

This instruction is used to receive data into the HSM of one processor from the HSM of another processor provided both are equipped with a Data Exchange Control. This instruction operates in the Simultaneous Mode. Receipt of data will terminate when the terminate signal is received from the sending computer or by AB equality.

Format

Operation — 5
N — H (first unit)
I (second unit)
A Address — Location in HSM which is to receive the first diad transferred. This address must be even.
B Address — Location in HSM which is to receive the last diad transferred. This address must be even.

Direction of Operation

Left to right.

Outline of Operation

Same as the Tape Read Forward Simultaneous instruction (pg. IX-6) with the following exceptions:

1. The EF/ED Simultaneous Indicator is not affected.
2. When this instruction is staticized, a flip-flop is set in the sending computer which, when sensed, will indicate that this computer is in the receive mode.
3. All characters received by the Data Exchange Control are checked for correct parity. If a character with incorrect parity is received, octal 57 is substituted for it and placed in HSM, the IOS flip-flop (A_0 2^3) is set in each Data Exchange Control, and data transmission continues.
4. This instruction is terminated by AB equality or by receipt of a terminate signal from the sending computer.

Final Register Contents

If the instruction is terminated by AB equality:
$(S)_f = (B)_i + 2$
$(T)_f = (B)_i$

If the instruction is terminated by receipt of the terminate signal:
$(S)_f = (A)_i$ + the number of characters transferred + 2.
$(T)_f = (B)_i$

Timing

The data transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both processors.

8 Tape Write Normal (TWN)

General Description

This instruction is used to transmit data from the HSM of one processor to the HSM of another processor provided both are equipped with a Data Exchange Control. This instruction operates in the Normal Mode.

Format

Operation — 8
N — H (first unit)
I (second unit)
A Address — Location in HSM of the first diad to be transferred. This address must be even.
B Address — Location in HSM of the last diad to be transferred. This address must be even.

Direction of Operation

Left to right.

Outline of Operation

Same as the Tape Write Normal instruction for tape (pg. IX-10) with the following exceptions:

1. When this instruction is staticized a flip-flop is set in the receiving computer which, when sensed, will indicate that this computer is in the transmitting mode.
2. This instruction is terminated by AB equality. When it is terminated, a terminate signal is sent to the receiving computer.

Final Register Contents

$(A)_t = (B)_1 + 2$
$(B)_t = (B)_1$

Timing

The data transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both processors.

9 Tape Write Simultaneous (TWS)

General Description

This instruction is used to transmit data from the HSM of one processor to the HSM of another processor provided both are equipped with a Data Exchange Control. This instruction operates in the Simultaneous Mode.

Format

Operation — 9
N — H (first unit)
I (second unit)
A Address — Location in HSM of the first diad to be transferred. This address must be even.
B Address — Location in HSM of the last diad to be transferred. This address must be even.

Direction of Operation

Left to right.

Outline of Operation

Same as the Tape Write Simultaneous instruction for tape (pg. IX-12) with the following exceptions:

1. When this instruction is staticized, a flip-flop is set in the receiving computer which, when sensed, will indicate that this computer is in the transmitting mode.
2. This instruction is terminated by AB equality. When it is terminated, a terminate signal is sent to the receiving computer.

Final Register Contents

$(S)_f = (B)_i + 2$
$(T)_f = (B)_i$

Timing

The data transfer rate is dependent upon the mode in which the transfer is made and the availability of status levels in both processors.

S Input/Output Sense (IOS)

General Description

This instruction is used in two ways. The two ways are differentiated by the state of the 2^0 bit of A_3 in the A address. The following are the instruction formats and the corresponding tests to be performed.

IOS ($A_3 = 1$)

Format

Operation — S
N — H (first unit)
I (second unit)
A Address — A_0 specifies the test to be performed as follows:

"1" Bit In	Numeric Equivalent	Test
2^0	1	Has the other computer staticized an I/O Sense ($A_3 = 1$)

— A_1, A_2 — Must be zeros (00).
— A_3 — 1
B Address — Location in HSM of the next instruction to be executed if the test condition is met.

Standard Location

STP (on transfer only)

Outline of Operation

This instruction, after staticizing will perform the test. If the tested condition is met, the contents of the P Register are transferred to STP and the contents of the B Register are transferred to the P Register.

This instruction is both a command and a test to the Data Exchange Control. It is used when a computer desires to initiate a data exchange and it tests whether the other computer has pre-empted the transmission channel for an exchange that it is initiating. If the channel is free, this instruction will set a flip-flop which notifies the other computer that the channel is busy.

Final Register Contents

$(A)_t = (A)_i$
$(B)_t = (B)_i$

IOS ($A_3 = 0$)

Format

Operation — S
N — I
A Address — A_0 specifies the tests to be performed as follows:

"1" Bit In	Numeric Equivalent	Test
2^0	1	Is the other computer non-operable?
2^1	2	Is the other computer in a receiving mode?
2^2	4	Is the other computer in a transmitting mode?
2^3	8	Has a character with incorrect parity been received or sent?

— A_1, A_2, A_3 — Must be zeros (000).
B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

56 μs if a transfer is executed.
42 μs if no transfer takes place.

XIV — INPUT/OUTPUT INSTRUCTIONS — MULTIPLE TAPE LISTER

8 Print Tape Normal (TWN)

General Description

This instruction transfers a specified series of consecutive characters in HSM to the Multiple Tape Lister Buffer.

Format

Operation — 8
N — — (minus)
A Address — Address of the first location in HSM to be transferred to the buffer (Control Character).
B Address — Address of the last location in HSM to be transferred to the buffer.

Direction of Operation

Left to right.

Outline of Operation

This instruction sends a start signal to the Multiple Tape Lister and operates in the following cycle:

The contents of the HSM location specified by the A Register are transferred to the Lister storage buffer. The contents of the A Register are compared with the contents of the B Register. The contents of the A Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(A)_f$ = Address of location one to the right of the last character transferred to the buffer.
$(B)_f = (B)_i$

Timing

Print and paper advance of one line takes 30.0 ms. Paper advance to the top of the form is accomplished at the rate of 18 ms per line.

Note: Appendix I indicates the format of the Control Character and the characters which may be printed.

9 Print Tape Simultaneous (TWS)

General Description

This instruction transfers a specified series of consecutive characters in HSM to the Multiple Tape Lister Buffer in the Simultaneous Mode.

Format

Operation — 9
N — — (minus)
A Address — Address of the first location in HSM to be transferred to the buffer (Control Character).
B Address — Address of the last location in HSM to be transferred to the buffer.

Direction of Operation

Left to right.

Outline of Operation

Initially this instruction is staticized in the Normal Mode. If the simultaneous Mode is free and the SMDI button is not on, the contents of the NOR, N, A, and B Registers are transferred to the SOR, M, S and T Registers respectively, and this instruction is executed in the Simultaneous Mode. This instruction sends a start signal to the Multiple Tape Lister and operates in the following cycle:

The contents of the HSM location specified by the S Register are transferred to the Lister storage buffer. The contents of the S Register are compared with the contents of the T Register. The contents of the S Register are incremented by one. If the comparison proved equal, the instruction terminates. If the comparison proved unequal, the cycle is repeated.

Final Register Contents

$(S)_f$ = Address of location one to the right of the last character transferred to the buffer.
$(T)_f = (B)_i$

Timing

Print and paper advance of one line takes 30.0 ms. Paper advance to the top of the form is accomplished at the rate of 18 ms per line.

Note: Appendix I indicates the format of the Control Character and the characters which may be printed.

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected device and chooses one of two sequences of instructions.

Format

Operation — S
N — - (minus)
A Address — A_0 specifies the tests to be performed as follows:

"1" Bit In	Numeric Equivalent	Tests
2^0	1	Is the Lister inoperable?
2^1	2	Is the Lister busy? (This indicator is set at the start of buffer loading and remains set until the line is printed. It is also set when the "Hold" switch is on.)
2^2	4	Is there a low paper condition in any of the supply bins?
2^4	&	Is paper being advanced?

— A_1, A_2, A_3 — Must be zeros (000).
B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Standard Location

STP (on transfer only)

Outline of Operation

The test (or tests) called for by the one bits in A_0 are performed on the device selected by N. If any one of the conditions tested is present, the contents of the P Register are transferred to STP and the contents of the B Register are then transferred to the P Register. If no tested condition is present, the next instruction in sequence will be executed.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing

56 μs if a transfer is executed.
42 μs if no transfer takes place.

XV — INPUT/OUTPUT INSTRUCTIONS — RANDOM-ACCESS COMPUTER EQUIPMENT

D Select (SEL)

General Description

This instruction must be executed prior to the issuance of each read or write. If the select is omitted, the read or write terminates immediately upon being issued and the illegal operation indicator is set.

Format

Operation — D

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 Channel.
$(64)_8$ to $(67)_8$ on Model 380-24 Channel.

A Address — A_0, $A_1 = 00$ — (Not used — must always be zeros.)

$A_2 - 2^0 = 0$ — *Remove card from drum* after next read or write unless an error is detected.

$2^0 = 1$ — *Leave card on drum* after next read or write.

$2^1 = 1$ — *Unconditional card removal* — Remove card presently on capstan regardless of error condition. Address data is ignored when this option is specified. This bit overrides all other bits and resets the *32 unserviced revolutions* bit. This option is independent of block and card select permissible logic. If a read is in progress, it will be immediately terminated and the card will be removed. If a write is in progress, the unconditional card removal is ignored. (The only indicator reset under this condition is an illegal operation.)

$2^2 = 1$ — *Terminate read* presently in progress. (Address data is ignored.) This option should only be executed after data transfer has been started on a staticized read. If no read is staticized, the option will be ignored.

$2^3 = 0$ — *Card Select* (includes block select information.)

$2^3 = 1$ — *Block Select* only. When this option is taken, it always refers to the card on the capstan. Block selection will bypass any card preselect information stored in the unit.

$2^4 = 0$ — (Not used — must always be zero.)

$2^5 = 0$ — (Not used — must always be zero.)

$A_3 - 2^0, 2^1, 2^2, 2^3$ — Magazine number (1 to 16 magazines, binary notation 0000_2 to 1111_2).

$2^4 = 0$

$2^5 = 0$

B Address — B_0, B_1 = Four bits of both B_0 and B_1 (2^0 to 2^3) designate the card number. (Total of eight bits for 256 cards.) This address should be considered a continuous eight-bit binary number, of which the least significant four bits are in B_1 and the most significant four bits are in B_0.

B_2, B_3 = Four bits of both B_2 and B_3 (2^0 to 2^3) designate the block number. (Total of eight bits for 256 blocks.) This address should be considered a continuous eight-bit binary number, of which the least significant four bits are in B_3 and the most significant four bits are in B_2.

Outline of Operation

The contents of the N Register specify the proper 3488 unit. A_3 designates the magazine number and can range from $(01)_8$ to $(15)_8$. B_0, B_1 designate the card number; B_2, B_3 designate the block number. A_2 specifies the various options as described above. The 2^0 bit of A_2 always specifies whether or not the card is to stay on or leave the drum after the next read or write to the specified unit. The 2^3 bit of A_2 always specifies whether the Select instruction is a Card or Block Select.

The 3488 unit has two levels of storage for card select information, so that a card preselect function can be performed. The card preselected will not be extracted on to the raceway until the trailing edge of the returning card passes the detection station approximately 10ms ahead of the read-write heads.

Card and block selects should only be issued when the device will accept them. If the device can not accept the select, an *illegal operation* occurs. This causes the termination of the Select instruction. A Card Select (or Preselect) is permissible only when the specific unit indicates that the select is permissible. A Block Select (or Preselect) is permissible only when the specific unit indicates that a Block Select is permissible.

A Block Select with no card on the capstan will set the illegal operation bit. The *32 unserviced revolutions* bit remains set if a 32 *unserviced revolutions* condition is present.

Whenever one of the 3488 units completes its card or block selection, the 8–10ms *select complete* indication of the device will be reset.

When a Block Preselect is accepted, Block Select is not permissible until the Block Preselect is executed. Any further block selects to the same unit during this period of time results in an illegal operation. A Block Preselect should not be attempted unless a card is on the capstan. A card leaving the capstan for any reason will cause a *block select not permissible* condition.

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

4 Read Normal (RFN)

General Description

This instruction reads a series of consecutive characters from a magnetic card on a 3488 unit starting at the block previously selected by a Select instruction. The instruction terminates and the transfer of information ends when the specified HSM area is filled or the last character of block 255 is read, whichever occurs first.

Format

Operation — 4

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 channel.
$(64)_8$ to $(67)_8$ on Model 380-24 channel.

A Address — Address of the HSM location that is to receive the first character of the block previously specified by a Select instruction. Must be an even address.

B Address — Address of the HSM location that is to receive the next to last character read. Must be an even address.

Outline of Operation

If all conditions are acceptable, the read begins when the 3488 unit indicates that the beginning of the selected block has been reached. The Block Address Register in the 3488 unit counts up with each block read.

If A-B Equality is not obtained by the completion of the read of the last block of the band, the block address is incremented by one and, if required, the heads are repositioned. When this occurs, the channel will not terminate the instruction. The read continues when the first character of the next block is in position to be read. block address is incremented by one and, if required, the heads are repositioned. When this occurs, the channel will not terminate the instruction. The read continues when the first character of the next block is in position to be read. Reading of a complete block is not mandatory; A-B Equality can be used to terminate the read wherever desired. Reads will automatically terminate after block 255.

When A-B Equality is reached, data transfer and the read instruction are terminated, the Normal Mode and channel are freed; however, the 3488 unit remains busy with the read until the interblock gap is reached. When the interblock gap is reached, the *Test for read or write busy* indicator is reset and a Block Preselect, if any, is executed.

Whether the card stays on or leaves the capstan after a read is terminated is under the control of the Select instruction. If a single bit within a character is missed during a read, the hardware automatically replaces the missing bit, sets the *single bit corrected* indicator, and continues reading. If more than one bit within a character is missed, $(57)_8$ replaces the bad parity character in core memory, the *parity error* indicator is set and the read operation continues; any subsequent bad parity characters are also replaced by $(57)_8$'s. When a read is terminated with the parity error indicator set, the card remains on the capstan even though the Select instruction specified its removal. Information following the first error character within the same block is not reliable.

When a read is illogically issued following either an *unconditional card removal*, or a *conditional card removal* (Select option $A_2 2^0 = 0$) the instruction remains staticized until a card reaches the capstan or the unit goes inoperable.

The channel allows only one read (or write) operation at a time. Use of two channels will allow two reads (or writes or read and write) simultaneously.

If a Read instruction is issued that misses the beginning of its specified block the operation will be automatically held off until the block approaches on the next revolution.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character transferred to memory.
$(B)_f = (B)_i$

5 Read Simultaneous (RFS)

General Description

This instruction reads a series of consecutive characters from a magnetic card on a 3488 unit starting at the block previously selected by the Select instruction. The instruction terminates and the transfer of information ends when the specified HSM area is filled or the last character of block 255 is read, whichever occurs first. This instruction is performed in the Simultaneous Mode.

Format

Operation — 5

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 channel.
$(64)_8$ to $(67)_8$ on Model 380-24 channel.

A Address — Address of the HSM location that is to receive the first character of the block previously specified by a Select instruction. Must be an even address.

B Address — Address of the HSM location that is to receive the next to last character read. Must be an even address.

Outline of Operation

If all conditions are acceptable, the read begins when the 3488 unit indicates that the beginning of the selected block has been reached. The Block Address Register in the 3488 unit counts up with each block read.

If A-B Equality is not obtained by the completion of the read of the last block of the band, the block address is incremented by one and, if required, the heads are repositioned. When this occurs, the channel will not terminate the instruction. The read continues when the first character of the next block is in position to be read. Reading of a complete block is not mandatory; A-B Equality can be used to terminate the read whenever desired. Reads will automatically terminate after block 255.

When A-B Equality is reached, data transfer and the Read instruction are terminated, the Simultaneous Mode and the channel are freed; however, the 3488 unit remains busy with the read until the interblock gap is reached. When the interblock gap is reached, the *Test for Read or Write busy* indicator is reset and a Block Preselect, if any, is executed.

Whether the card stays on or leaves the capstan after a read is terminated is under control of the Select instruction. If a single bit within a character is missed during a read, the hardware automatically replaces the missing bit, sets the *single bit corrected* indicator, and continues reading. If more than one bit within a character is missed, $(57)_8$ replaces the bad parity character in core memory, the *parity error* indicator is set and the read operation continues; any subsequent bad parity characters are also replaced by $(57)_8$'s. When a read is terminated with the *parity error* indicator set, the card remains on the capstan even though the *select* instruction specified its removal. Information following the first error character within the same block is not reliable.

When a read is illogically issued following either an *unconditional card removal,* or a *conditional card removal* (Select option $A_2 2^0 = 0$) the instruction remains staticized until a card reaches the capstan or the unit goes inoperable.

The channel allows only one read (or write) operation at a time. Two channels allow two reads (or writes or read and write) simultaneously.

If a Read instruction is issued that misses the beginning of its specified block the operation is automatically held off until the block approaches on the next revolution.

Final Register Contents

$(S)_f$ = Address of HSM location one to the right of the last character transferred to memory.
$(T)_f = (B)_i$

8 Write Normal (TWN)

General Description

This instruction writes a series of consecutive characters from HSM to a magnetic card on a 3488 unit, starting at the block previously selected by the Select instruction. Transfer of information ends when the last character in the specified HSM area is written or after the last character of block 255 is written, whichever occurs first.

Format

Operation — 8

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 channel.
$(64)_8$ to $(67)_8$ on Model 380-24 channel.

A Address — Address of the HSM location of the first character to be written. Block must be previously selected by Select instruction. Must be an even address.

B Address — Address of the HSM location of the next to last character to be written. Must be an even address.

Outline of Operation

If all conditions are acceptable, the write begins when the 3488 unit indicates that the beginning of the selected block has been reached. Character transfer ends on A-B Equality or when the end of block 255 is reached, whichever occurs first. The Block Address Register in the 3488 unit counts up with each block written.

If A-B Equality is not obtained by the completion of the write of the last block of the band, the block address is incremented by one and, if necessary, the heads are repositioned. When this occurs, the instruction is not terminated. The write continues when the next block is in position under the read-write heads.

When A-B Equality is reached, the Write instruction is terminated and the mode is freed. If the write is not in full block multiples, the remainder of the *last* block is filled with spaces. Note that the mode becomes free prior to the completion of the read-after-write check. This is true even when the A-B Equality is reached on the 650th character of the last block. Because of this, the Input/Output Sense for a read-after-write error can not follow a Write instruction; it must always be preceded by an Input/Output Sense (Test for Read or Write busy) to ensure that the unit is no longer writing. This test is set when the write is issued; it is reset when the read-after-write check is complete for the 650th character of the *last* block.

Whether the card stays on or leaves the capstan after a write is terminated is under control of the Select instruction. When a read-after-write error is detected, the following occurs:

1. The write terminates immediately.
2. The *read-after-write error* indicator is set.
3. The Normal Mode and channel are freed.
4. The *test for read or write busy* indicator is reset.
5. The card remains on the capstan.
6. A Block Preselect, if any, is executed.

When a write is illogically issued following either an *unconditional card removal* or a *conditional card removal*, the instruction remains staticized until a card reaches the capstan or the unit goes inoperable.

A Write instruction can be issued anytime after executing a Card Select, or after a legitimate Block Select. The Normal Mode remains busy while the instruction is waiting to be executed. The channel allows only one (read or) write at a time. Two channels allow two (reads or) writes (or read and write) simultaneously.

Final Register Contents

$(A)_f$ = Address of HSM location one to the right of the last character transferred.
$(B)_f = (B)_i$

9 Write Simultaneous (TWS)

General Description

This instruction writes a series of consecutive characters from HSM to a magnetic card on a 3488 unit, starting at the block previously selected by the Select instruction. Transfer of information ends when the last character in the specified HSM area is written or after the last character of block 255 is written, whichever occurs first. This instruction is performed in the Simultaneous Mode.

Format

Operation — 9

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 channel.
$(64)_8$ to $(67)_8$ on Model 380-24 channel.

A Address — Address of the HSM location of the first character to be written. Block must be previously selected by Select instruction. Must be an even address.

B Address — Address of the HSM location of the next to last character to be written. Must be an even address.

Outline of Operation

If all conditions are acceptable, the write begins when the 3488 unit indicates that the beginning of the selected block has been reached. Character transfer ends on A-B Equality or when the end of block 255 is reached, whichever occurs first. The Block Address Register in the 3488 unit counts up with each block written.

If A-B Equality is not obtained by the completion of the write of the last block of the band, the block address is incremented by one and, if necessary, the heads are repositioned. When this occurs, the instruction is not terminated. The write continues when the next block is in position under the heads.

When A-B Equality is reached, a Write Simultaneous does not terminate. If the write is not in full block multiples, the remainder of the *last* block receiving characters specified by A-B is filled with spaces. The device and the Simultaneous Mode remain busy with the write until the read-after-write check is complete for all characters in the last block including those space-filled.

Whether the card stays on or leaves the capstan after a write is terminated is under the control of the Select instruction.

When a write is illogically issued following either an *unconditional card removal* or a *conditional card removal,* the instruction remains staticized until a card reaches the capstan or the unit goes inoperable.

A Write instruction can be issued anytime after executing a Card Select, or after a legitimate Block Select. The Simultaneous Mode remains busy while the instruction is waiting to be executed. The channel allows only one (read or) write at a time. Two channels allow two (reads or) writes (or read and write) simultaneously.

Final Register Contents

$(S)_f$ = Address of HSM location one to the right of the last character transferred.
$(T)_f = (B)_i$

S Input/Output Sense (IOS)

General Description

This instruction tests the desired status of the selected channel and chooses one of two sequences of instructions.

Format

Operation — S

N — Specifies device number.
$(60)_8$ to $(63)_8$ on Model 380-14 channel.
$(64)_8$ to $(67)_8$ on Model 380-24 channel.

A Address — A_0 specifies the tests to be performed as follows:

"1" Bit in	Numeric Equivalent	Tests
Option 0		
2^0	1	Test for card select (preselect) not permissible.
2^1	2	Test for channel busy with read, write, or select (note 1).
2^2	4	Test for device busy with read or write.
2^3	8	Test for block select (preselect) not permissible (note 2).
2^4	&	Test for specified block *not* within 8–10ms. from heads (note 3).
Option 1		
2^0	1	Test for parity error, read-after-write error, or preamble error.
2^1	2	Test for inoperability (note 4).
2^2	4	Test for card released due to exceeding 32 unserviced revolutions.
2^3	8	Test for illegal operation or magazine absent (note 5).
2^4	&	Test for block 255 exceeded without A-B Equality.
Option 2		
2^0	1	Test for specified block *not* within 6–8ms. from heads (note 6).
2^1	2	Test for single bit corrected error.
2^2	1	Test for count equals limit (set only once).
2^3	1	Test for count exceeds limit* (set each time card is placed on capstan after count has been exceeded).

* This limit is manually set up in the 3488 unit.

— A_1, A_2 — Must be zeros (00).
— A_3 — Specifies Sense Option:
$A_3 = 0$ — specifies option 0.
$A_3 = 1$ — specifies option 1.
$A_3 = 2$ — specifies option 2.

B Address — HSM location of the next instruction to be executed if the condition or conditions being tested are present.

Notes

1. A Select instruction keeps the channel busy for 50ms. after actual termination of the instruction.
2. This sensible bit is set by a Select instruction and reset by a Read or Write instruction.

   When a Read or Write instruction is accepted by the channel, block select becomes permissible. If the read or write is terminated with a card on the capstan, block select remains permissible. If the card is not on the capstan when read or write is terminated, then block select is not permissible.

   When the channel accepts a block preselect, block select is not permissible until a Read or Write and the Block Preselect instructions are executed. Any further block selects to the same unit during this period of time results in an illegal operation. A Block Preselect should not be attempted unless a card is on the capstan. A card leaving the capstan for any reason causes a *block select not permissible* condition.
3. If $2^4 = 0$, the specified block is within 8–10ms. from heads (Select complete). When this sensible bit is set to zero (0) it will remain set until a read or write is executed.
4. Test for inoperability includes device inoperable, address verification error, or card absent error. Both address verification error and card address error will cause device inoperability and set the inoperable bit.

   When the address verification error occurs on a card that has been extracted, the device becomes inoperable immediately, and the card is returned to its magazine after one revolution on the capstan. When the address verification occurs on a card that is being preselected, the device will become inoperable at the time the preselect card extract would be attempted. The card will not be extracted.

   When a card absent error occurs, normal operation of the unit is allowed until the transport is cleared. Once all the cards are in their magazines the hardware makes a second attempt to select the card. If the *card absent* indication is received after this attempt, the unit becomes inoperable and the sense bit (inoperable) is set.
5. If an attempt is made to select a card from a magazine position that does not contain a magazine, an illegal operation sense indication is set. This indication is not received until 50ms. after the Select instruction is terminated. At that time the 8–10ms. bit of the specific device is reset. This condition can be cleared by issuing an *unconditional card removal* command, which will reset the 8–10ms. bit. The illegal operation indication is reset by any subsequent instruction to the device, including the *unconditional card removal.*
6. This bit is reset ($2^0 = 0$) at the same time the option 0–2^4 bit (Test for specified block not within 8–10ms. from heads) is reset; however, it is set to one (1) after a delay of 6–8ms. This bit is reset each time the specified block is within 8–10ms. and then set to one (1) after 6–8ms. The state of this bit is not predictable after the read or write is executed.

Outline of Operation

For each 3488 unit, there is an indicator associated with each of the sense bits (A address, options 0, 1, and 2). Each indicator is set by the existence of the condition that results in a "yes" answer. The indicator is in a reset state if the condition is not present. The test or tests called for by one (1) bits in the A address are performed on the device specified by N. If any one of the conditions is true, the contents of the B Register are transferred to the P Register causing a jump to the address indicated by B. If none of the specified indicators are set (all specified indicators are reset), the next instruction in sequence is executed. General reset will automatically affect the following indicators, provided that all cards are at rest in their magazines. If General Reset is depressed before all cards are at rest, the unit goes inoperable.

These indicators will be reset:

1. Card select not permissible.
2. Card released due to 32 unserviced revolutions.
3. Illegal operation.

These indicators will be set:

1. Block select not permissible.
2. Specified block *not* within 8–10ms.

General Reset will not reset the date error indicator (Option 1–2^0).

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Reading or Writing

Conditions	Instruction Termination	How Indicated To Program	Indicator Clearance	Comments
1. Inoperable on attempt to address device. a. Address Verification on Select. b. Card Absent on Select. c. Malfunction. d. Power Failure.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset by operator	When addressing a unit with a Select instruction, the 8–10ms. indication will also be given.
2. Inoperable during Reading or Writing, or Echo Check during Writing.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset by operator	
3. No Block Select given before Read or Write.	At time detected	Option 1 $A_0 2^3 = 1$ (Illegal Operation)	Next Read or Write Select	
4. Card released prior to Read/Write due to 32 unserviced revolutions.	At time detected	Option 1 $A_0 2^2 = 1$ (32 Unserviced Revolutions)	When unconditional Card Removal command is given	
5. Preamble Error.	At time detected	Option 1 $A_0 2^0 = 1$ (Parity)	Next Read or Write	Instruction is terminated immediately.
6. Parity Error during reading.	Upon completion of instruction	Option 1 $A_0 2^0 = 1$ (Parity)	Next Read or Write	Indicated as soon as error is detected.
7. Read-after-Write error during writing.	At time detected	Option 1 $A_0 2^0 = 1$ (Parity)	Next Read or Write	Indicated as soon as error is detected.
8. Block 255 exceeded during a Write or Read without A-B Equality.	At time detected	Option 1 $A_0 2^4 = 1$	Next Read or Write	

Card Select

Conditions	Instruction Termination	How Indicated To Program	Indicator Clearance	Comments
1. Inoperable before Card Select.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset	
2. Inoperable during execution of Card Select.	No instruction being executed	Option 0 $A_0 2^4 = 0$ and Option 1 $A_0 2^1 = 1$	Manual Reset	Unit goes inoperable at time of extract if Address Verification error on Card Select.
3. Card released due to exceeding 32 unserviced revolutions.				When this Select is executed, the extraction will be held off until the "32 Rev" bit is cleared.
4. Address Verification error on Card selected. Address Verification error on Card pre-selected.	No instruction being executed	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset Manual Reset	Card released to magazine. Becomes inoperable when extract is attempted.
5. Card Absent.	No instruction being executed	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset	Hardware will attempt another Select.
6. Card Select not permissible.	At time detected	Option 1 $A_0 2^3 = 1$ (Illegal Operation)		
7. Magazine Absent.	Upon completion of instruction	Option 0 $A_0 2^4 = 0$	Unconditional Card Removal	Removal Command must be given to set the 8–10ms. indication to "1".

Block Select

Conditions	Instruction Termination	How Indicated To Program	Indicator Clearance	Comments
1. Inoperable before Block Select.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset	
2. Inoperable during Block Select.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset	
3. No card on capstan.	At time detected	Option 1 $A_0 2^3 = 1$ (Illegal Operation)	Next Read Write or Select	
4. Card released due to exceeding 32 unserviced revolutions.	At time detected	A_0 Option 1 $2^2 = 1$ $2^3 = 1$ (Illegal Operation and 32 Revolutions)	Next Read Write or Select	32 Revolution Indicator is cleared by issuing an unconditional Card Removal. Block Select not permissible is set when this occurs.
5. Block Select not permissible.	At time detected	Option 0 $A_0 2^3 = 1$ Option 1 $A_0 2^3 = 1$ (Illegal Operation)	Next Read or Write	

Miscellaneous Conditions

Conditions	Instruction Termination	How Indicated To Program	Indicator Clearance	Comments
1. Card released due to 32 unserviced revolutions.	No instruction in execution	Option 0 $A_0 2^4 = 0$ (8–10ms.) Option 1 $A_0 2^2 = 1$ (32 unserviced revolutions)	When unconditional Card Removal command is given	A card will remain in preselect until 32 revolution bit is set to zero by unconditional card removal command.
2. Select Complete.		Option 0 $A_0 2^4 = 0$ (8–10ms.)		
3. Inoperable and card is on capstan.	At time detected	Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset	If possible, the card will leave the capstan when the unit goes inoperable.
4. Read or Write executed with no card on capstan or on the way and no 32 Revolution indication.				Read or Write with no card on capstan (and no 32 Rev. indicator) will result in a "Silent Death" condition. The instruction will stay staticized until a card reaches the capstan or the unit goes inoperable.
5. Inoperable when no instruction is staticized while unit is in Remote.		Option 0 $A_0 2^4 = 0$ Option 1 $A_0 2^1 = 1$	Manual Reset	
6. Inoperable when no instruction is staticized while unit is in Local.		Option 1 $A_0 2^1 = 1$ (Inoperable)	Manual Reset by Operator	

APPENDICES

APPENDIX A. RCA 301 CODES

Character Description	Symbol	MACHINE CODE								TAPE CODE*								CARD CODE										
		P	Zone		Numeric					P	Zone		Numeric					Punched Rows										
		2^6	2^5	2^4	2^3	2^2	2^1	2^0		2^6	2^5	2^4	2^3	2^2	2^1	2^0		Y	X	0	1	2	3	4	5	6	7	8	9
Zero	0	1	0	0	0	0	0	0		0	1	1	1	1	1	1					1								
One	1	0	0	0	0	0	0	1		1	1	1	1	1	1	0						1							
Two	2	0	0	0	0	0	1	0		1	1	1	1	1	0	1							1						
Three	3	1	0	0	0	0	1	1		0	1	1	1	1	0	0								1					
Four	4	0	0	0	0	1	0	0		1	1	1	1	0	1	1									1				
Five	5	1	0	0	0	1	0	1		0	1	1	1	0	1	0										1			
Six	6	1	0	0	0	1	1	0		0	1	1	1	0	0	1											1		
Seven	7	0	0	0	0	1	1	1		1	1	1	1	0	0	0												1	
Eight	8	0	0	0	1	0	0	0		1	1	1	0	1	1	1													1
Nine	9	1	0	0	1	0	0	1		C	1	1	0	1	1	0													
Space		1	0	0	1	0	1	0		0	1	1	0	1	0	1													
Number	#	0	0	0	1	0	1	1		1	1	1	0	1	0	0								1					1
At the rate of	@	1	0	0	1	1	0	0		0	1	1	0	0	1	1									1				1
Open Parenthesis	(	0	0	0	1	1	0	1		1	1	1	0	0	1	0										1			1
Close Parenthesis	)	0	0	0	1	1	1	0		1	1	1	0	0	0	1											1		1
		1	0	0	1	1	1	1		0	1	1	0	0	0	0		Not used											
Ampersand	&	0	0	1	0	0	0	0		1	1	0	1	1	1	1		1											
A	A	1	0	1	0	0	0	1		0	1	0	1	1	1	0		1		1									
B	B	1	0	1	0	0	1	0		0	1	0	1	1	0	1		1			1								
C	C	0	0	1	0	0	1	1		1	1	0	1	1	0	0		1				1							
D	D	1	0	1	0	1	0	0		0	1	0	1	0	1	1		1					1						
E	E	0	0	1	0	1	0	1		1	1	0	1	0	1	0		1						1					
F	F	0	0	1	0	1	1	0		1	1	0	1	0	0	1		1							1				
G	G	1	0	1	0	1	1	1		0	1	0	1	0	0	0		1								1			
H	H	1	0	1	1	0	0	0		0	1	0	0	1	1	1		1									1		
I	I	0	0	1	1	0	0	1		1	1	0	0	1	1	0		1										1	
Plus	+	0	0	1	1	0	1	0		1	1	0	0	1	0	1		1			1						1		
Period	.	1	0	1	1	0	1	1		0	1	0	0	1	0	0		1				1					1		
Semicolon	;	0	0	1	1	1	0	0		1	1	0	0	0	1	1		1					1				1		
Colon	:	1	0	1	1	1	0	1		0	1	0	0	0	1	0		1						1			1		
Apostrophe	'	1	0	1	1	1	1	0		0	1	0	0	0	0	1		1							1		1		
Plus zero	+0	0	0	1	1	1	1	1		1	1	0	0	0	0	0		1		1									

* Hi-Data Tape Group and Paper Tape

APPENDIX A. RCA 301 CODES (Continued)

Character Description	Symbol	MACHINE CODE								TAPE CODE*								CARD CODE										
		P	Zone		Numeric					P	Zone		Numeric					Punched Rows										
		2^6	2^5	2^4	2^3	2^2	2^1	2^0		2^6	2^5	2^4	2^3	2^2	2^1	2^0		Y	X	0	1	2	3	4	5	6	7	8	9
Minus	—	0	1	0	0	0	0	0		1	0	1	1	1	1	1			1										
J	J	1	1	0	0	0	0	1		0	0	1	1	1	1	0			1		1								
K	K	1	1	0	0	0	1	0		0	0	1	1	1	0	1			1			1							
L	L	0	1	0	0	0	1	1		1	0	1	1	1	0	0			1				1						
M	M	1	1	0	0	1	0	0		0	0	1	1	0	1	1			1					1					
N	N	0	1	0	0	1	0	1		1	0	1	1	0	1	0			1						1				
O	O	0	1	0	0	1	1	0		1	0	1	1	0	0	1			1							1			
P	P	1	1	0	0	1	1	1		0	0	1	1	0	0	0			1								1		
Q	Q	1	1	0	1	0	0	0		0	0	1	0	1	1	1			1									1	
R	R	0	1	0	1	0	0	1		1	0	1	0	1	1	0			1										1
End Information	(EI)	0	1	0	1	0	1	0		1	0	1	0	1	0	1			1			1						1	
Dollars	$	1	1	0	1	0	1	1		0	0	1	0	1	0	0			1				1					1	
Asterisk	*	0	1	0	1	1	0	0		1	0	1	0	0	1	1			1					1				1	
End Data	(ED)	1	1	0	1	1	0	1		0	0	1	0	0	1	0			1						1			1	
End File	(EF)	1	1	0	1	1	1	0		0	0	1	0	0	0	1			1							1		1	
		0	1	0	1	1	1	1		1	0	1	0	0	0	0		Not used											
Quotation Mark	"	1	1	1	0	0	0	0		0	0	0	1	1	1	1			1	1									
Virgule	/	0	1	1	0	0	0	1		1	0	0	1	1	1	0				1	1								
S	S	0	1	1	0	0	1	0		1	0	0	1	1	0	1				1		1							
T	T	1	1	1	0	0	1	1		0	0	0	1	1	0	0				1			1						
U	U	0	1	1	0	1	0	0		1	0	0	1	0	1	1				1				1					
V	V	1	1	1	0	1	0	1		0	0	0	1	0	1	0				1					1				
W	W	1	1	1	0	1	1	0		0	0	0	1	0	0	1				1						1			
X	X	0	1	1	0	1	1	1		1	0	0	1	0	0	0				1							1		
Y	Y	0	1	1	1	0	0	0		1	0	0	0	1	1	1				1								1	
Z	Z	1	1	1	1	0	0	1		0	0	0	0	1	1	0				1									1
End Block	(EB)	1	1	1	1	0	1	0		0	0	0	0	1	0	1				1		1						1	
Comma	,	0	1	1	1	0	1	1		1	0	0	0	1	0	0				1			1					1	
Percent	%	1	1	1	1	1	0	0		0	0	0	0	0	1	1				1				1				1	
Item Separator (ISS)	●	0	1	1	1	1	0	1		1	0	0	0	0	1	0				1					1			1	
Equals	=	0	1	1	1	1	1	0		1	0	0	0	0	0	1				1							1	1	
		1	1	1	1	1	1	1			Indicates Gap							Not used											
Delete (paper tape only)										1	1	1	1	1	1	1													

* Hi-Data Tape Group and Paper Tape

APPENDIX B. LIST OF INSTRUCTIONS

INPUT/OUTPUT INSTRUCTIONS

Op. Code	*Abbreviation*	*Instruction Name*
0	CRN	Card Read Normal (Model 323 Reader)
0	CRN	Card Read Normal (Model 330 Card Reader-Punch)
0	CRN	Card Read Normal (Model 324, 329 Readers)
1	CRS	Card Read Simultaneous (Model 323 Reader)
1	CRS	Card Read Simultaneous (Model 330 Card Reader-Punch)
1	CRS	Card Read Simultaneous (Model 324, 329 Readers)
2	CPN	Card Punch Normal (Model 334 Punch)
2	CPN	Card Punch Normal (Model 336 Punch)
2	CPN	Card Punch Normal (Model 330 Card Reader-Punch)
3	CPS	Card Punch Simultaneous (Model 334 Punch)
3	CPS	Card Punch Simultaneous (Model 336 Punch)
3	CPS	Card Punch Simultaneous (Model 330 Card Reader-Punch)
4	RFN	Tape Read Forward Normal
4	RFN	Tape Read Forward Normal (Data Exchange Control)
5	RFS	Tape Read Forward Simultaneous
5	RFS	Tape Read Forward Simultaneous (Data Exchange Control)
6	RRN	Tape Read Reverse Normal
7	RRS	Tape Read Reverse Simultaneous
8	TWN	Tape Write Normal
8	TWN	Tape Write Normal (Data Exchange Control)
8	TWN	Print Tape Normal (Multiple Tape Lister)
9	TWS	Tape Write Simultaneous
9	TWS	Tape Write Simultaneous (Data Exchange Control)
9	TWS	Print Tape Simultaneous (Multiple Tape Lister)
B	PAN	Print and Paper Advance Normal
C	PAS	Print and Paper Advance Simultaneous
D	BSN	Band Select Normal
D	TS	Track Select
E	BSM	Band Select Record File Mode
F	BRN	Block Read Record Normal
F	SRN	Sector Read Disc Normal
G	BRS	Block Read Record Simultaneous
G	SRS	Sector Read Disc Simultaneous
H	BWN	Block Write Record Normal
H	SWN	Sector Write Disc Normal
I	BWS	Block Write Record Simultaneous
I	SWS	Sector Write Disc Simultaneous

INPUT/OUTPUT INSTRUCTIONS

Op. Code	*Abbreviation*	*Instruction Name*
*	RMR	Record File Mode Read
%	RMW	Record File Mode Write
;	RWD	Rewind to BTC
;	IOC	Input/Output Control

DATA HANDLING INSTRUCTIONS

A	TRA	Translate by Table
J	SF	Transfer Symbol to Fill
K	LSL	Locate Symbol Left
L	LSR	Locate Symbol Right
M	DL	Transfer Data Left
N	DR	Transfer Data Right
#	DSL	Transfer Data by Symbol Left
P	DSR	Transfer Data by Symbol Right

ARITHMETIC INSTRUCTONS

+	ADD	Add
Q	OR	Logical "OR"
− (minus)	SUB	Subtract
T	AND	Logical "AND"
U	EXO	Exclusive "OR"

DECISION AND CONTROL INSTRUCTIONS

R	RPT	Repeat
V	REG	Store Register
W	CTC	Conditional Transfer of Control
X	TA	Tally
Y	COM	Compare Left
S	IOS	Input/Output Sense
S	IOS	Hardware Rollback Control
. (period)	HLT	Halt

APPENDIX C. SUMMARY

Op. Code	Instruction	N	A Address	B Address
A	Translate by Table	Number (0-44) of characters to be translated	HSM location of leftmost character to be translated	HSM location of first character of translate table (must end in 00)
B	Print & Paper Advance Normal	Number (0-14) of lines to advance paper if $B_3 = 1$. Also selects Printer unit and mode	Must be zeros (0000)	Address of data to be printed from HSM excluding B_3: B_0 = MSD of address B_1 = even - print, odd-do not print B_2 — *Unbuffered Printer* $B_2 = 0$ causes 120 or 160 characters to be printed depending on the printer model *Buffered Printer* $B_2 = 0$ causes 120 characters to be printed regardless of the printer model. $B_2 = 2$ causes 160 characters to be printed on the 160 column printer $B_3 = 0$, no paper advance $B_3 = 1$, paper advance indicated by N $B_3 = 2$, vertical tab (using tape loop) $B_3 = 3$, page change (using tape loop)
C	Print & Paper Advance Simultaneous	Number (0-14) of lines to advance paper if $B_3 = 1$. Also selects Printer unit and mode	Must be zeros (0000)	Address of data to be printed from HSM excluding B_3: B_0 = MSD of address B_1 = even - print, odd-do not print B_2 — *Unbuffered Printer* $B_2 = 0$ causes 120 or 160 characters to be printed depending on the printer model *Buffered Printer* $B_2 = 0$ causes 120 characters to be printed regardless of the printer model. $B_2 = 2$ causes 160 characters to be printed on the 160 column printer $B_3 = 0$, no paper advance $B_3 = 1$, paper advance indicated by N $B_3 = 2$, vertical tab (using tape loop) $B_3 = 3$, page change (using tape loop)
D	Band Select Normal	0, selects first file; record returned to cage before selection &, selects second file; record returned to cage before selection 1, selects first file; band selected is on turntable A, selects second file; band selected is on turntable	Must be zeros (0000)	B_0 = Must be zero (0) B_1, B_2, B_3 designate band (000-511)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
				Yes	Operation left to right. Translation in place	$(A)_f$ = HSM address of location one to the right of the last character translated	$(B)_f = (B)_i$
					120 or 160 characters printed if B_1 is even. Print is done first when applicable. Unbuffered Printer: Paper Advance is completely independent of computing. Buffered Printer: Printing and Paper Advance are accomplished off-line. Operation left to right	$(A)_f$ = HSM address of location one to the right of last character transferred. $(A)_f = (A)_i$ when printing is not indicated	$(B)_f = (B)_i$ except that B_3 will be set to zero
					120 or 160 characters printed if B_1 is even. Print is done first if applicable. Unbuffered Printer: Paper Advance is completely independent of computing. Buffered Printer: Printing and Paper Advance are accomplished off-line. Operation left to right	$(S)_f$ = HSM address of location one to the right of last character transferred. $(S)_f = (A)_i$ when printing is not indicated	$(T)_f = (B)_i$ except that B_3 will be set to zero
					The record will be selected independent of computer operation	$(A)_f = (A)_i$	$(B)_f = (B)_i$

APPENDIX C. SUMMARY

Op. Code	Instruction	N	A Address	B Address	
D	Track Select	Specifies Data Disc File to select R (First Data Disc File) Z (Second Data Disc File)	Must be zeros (0000)	B_0 = Must be zero (0) B_1, B_2, B_3 selects track (000-127)	
E	Band Select Record File Mode	$2^0 = 0$, returns record to cage before selection. $2^0 = 1$, band selected is on turntable. Bits 2^4 - 2^5 = Record File from which band is to be selected	Must be zeros (0000)	B_0 = Must be zero (0) B_1, B_2, B_3 designates band (000-511).	
F	Block Read Record Normal	2^3, 2^2, 2^1, 2^0 selects number of blocks to be read. $2^4 = 0$, selects first file $2^4 = 1$, selects second file	HSM address where first character is to be placed	B_0 = Must be zero (0) B_1 = odd — record returned to cage after operation B_1 = even — record stays on turntable and arm is placed at beginning of selected band after operation B_2 = 1 — block terminated on counting 900 characters B_2 = 0 — count or EB recognition. B_3 = addresses cells 1-10	
F	Sector Read Disc Normal	Specifies additional number of sectors to be read and file selected	Address of HSM location to receive first character read	B_0 = designates first sector to be read B_1, B_2, B_3 specifies zone to be read from 2^4 of $B_0 = 0$, prevents override of SRS instruction 2^4 of $B_0 = 1$, permits override of any Data Disc File Simultaneous instruction. B_1, B_2, B_3, specifies zone to be read from.	
G	Block Read Record Simultaneous	2^3, 2^2, 2^1, 2^0 selects number of blocks to be read $2^4 = 0$, selects first file $2^4 = 1$, selects second file	HSM address where first character is to be placed	B_0 = Must be zero (0) B_1 = odd — record returned to cage after operation. B_1 = even — record stays on turntable and arm is placed at beginning of selected band after operation B_2 = 1 — block terminated on counting 900 characters B_2 = 0 — count or EB recognition B_3 = address cells 1-10	
G	Sector Read Disc Simultaneous	Specifies Additional number of sectors to be read and file selected	Address of HSM location to receive first character read	2^3, 2^2, 2^1, 2^0 bits of B_0 designates first sector to be read 2^4 of $B_0 = 0$, prevents override of SRS instruction 2^4 of $B_0 = 1$, permits override of any Data Disc File Simultaneous instruction. B_1, B_2, B_3, specifies zone to be read from	
H	Block Write Record Normal	2^3, 2^2, 2^1, 2^0 selects number of blocks to be written $2^4 = 0$, selects first file $2^4 = 1$, selects second file	HSM address where first character is to be written	B_0 = Must be zero (0) B_1 = odd-record returned after operation B_1 = even-record stays on turnable and arm is placed at beginning of selected band after operation B_2 = 1 — block terminates on counting 900 characters B_2 = 0 — count or EB recognition B_3 = addresses cells 1-10	

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
					Track will be selected independently of computer operation	$(A)_f = (A)_i$	$(B)_f = (B)_i$
					Record will be selected independent of computer operation. This instruction used with files under control of record file mode only	$(A)_f = (A)_i$	$(B)_f = (B)_i$
	Yes				Operation left to right	$(A)_f$ = HSM address one to the right of last character read	$(B)_f = (B)_i$
	Yes				Operation left to right	$(A)_f$ = HSM address one to the right of last character read	$(B)_f = (B)_i$
					Operation left to right	$(S)_f$ = HSM address one to the right of last character read	$(T)_f = (B)_i$
					Operation left to right	$(S)_f$ = HSM address one to the right of last character read	$(T)_f = (B)_i$
					Operation left to right	$(A)_f$ = HSM address one to the right of last character written	$(B)_f = (B)_i$

Op. Code	Instruction	N	A Address	B Address	
H	Sector Write Disc Normal	Specifies additional number of sectors to be written and file selected	HSM address of first character to be written	B_0 designates first sector to be written to 2^4 of $B_0 = 0$, prevents override of Data Disc Simultaneous instruction 2^4 of $B_0 = 1$, permits override of Data Disc Simultaneous instruction B_1, B_2, B_3 specifies zone to be written to	
I	Block Write Record Simultaneous	2^3, 2^2, 2^1, 2^0 selects number of blocks to be written $2^4 = 0$, selects first file $2^4 = 1$, selects second file	HSM address where first character is to be written	B_0 = Must be zero (0) B_1 = odd-record returned after operation B_1 = even-record stays on turntable and arm is placed at beginning of selected band after operation $B_2 = 1$ — block terminates on counting 900 characters $B_2 = 0$ — count or EB recognition B_3 = addresses cells 1-10	
I	Sector Write Disc Simultaneous	Specifies additional number of sectors to be written and file selected	HSM address of first character to be written	2^3, 2^2, 2^1, 2^0 bit of B_0 designates 1st sector to be written 2^4 of $B_0 = 0$, prevents override of Data Disc Simultaneous instruction 2^4 of $B_0 = 1$, permits override of Data Disc Simultaneous instruction B_1, B_2, B_3 specifies zone to be written to	
J	Transfer Symbol to Fill	Selected Symbol	Leftmost HSM address to be filled	Rightmost HSM address to be filled	
K	Locate Symbol Left	Selected Symbol	Leftmost HSM address to be searched	Rightmost HSM address to be searched	
L	Locate Symbol Right	Selected Symbol	Rightmost HSM address to be searched	Leftmost HSM address to be searched	
M	Transfer Data Left	Number (0-44) of characters to be transferred	HSM location of leftmost character to be transferred	Destination HSM address of first character	
N	Transfer Data Right	Number (0-44) of characters to be transferred	HSM location of rightmost character to be transferred	Destination HSM address of first character	
P	Transfer Data by Symbol Right	Selected symbol on which to stop transferring	HSM location of rightmost character to be transferred	Destination HSM address of first character	
Q	Logical "OR"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand	

OF INSTRUCTIONS (Continued)

STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
					A Register	B Register
				Operation left to right	$(A)_f$ = HSM address one to the right of last character written	$(B)_f = (B)_i$
				Operation left to right	$(S)_f$ = HSM address one to the right of last character written	$(T)_f = (B)_i$
				Operation left to right	$(S)_f$ = HSM address one to the right of last character written	$(T)_f = (B)_i$
				Operation left to right	$(A)_f = (B)_i$ + one character location	$(B)_f = (B)_i$
Yes		Yes		Operation left to right PRI's set as follows: PRN if first character not equal to N PRZ if all characters are equal to N PRP if non-symbol is located after a character equal to N is found	If a character is found not equal to N $(A)_f$ = HSM address one to left of that character. If all characters searched are equal to N $(A)_f = (B)_i$	$(B)_f = (B)_i$
Yes		Yes		Operation right to left PRI's set as follows: PRN if first character not equal to N PRZ if all characters are equal to N PRP if non-symbol is located after a character equal to N is found	If a character is found not equal to N $(A)_f$ = HSM address one to right of that character If all characters searched are equal to N $(A)_f = (B)_i$	$(B)_f = (B)_i$
			Yes	Operation left to right	$(A)_f$ = HSM address one to the right of last character transferred	$(B)_f$ = HSM address one to the right of last destination address
			Yes	Operation right to left	$(A)_f$ = HSM address one to the left of last character transferred	$(B)_f$ = HSM address one to the left of last destination address
Yes			Yes	Operation right to left	$(A)_f$ = HSM address one to the left of specified symbol in the original area	$(B)_f$ = HSM address one to the left of symbol in destination area
			Yes	Operation right to left	$(A)_f$ = HSM address one to the left of MSD of result	$(B)_f$ = HSM address one to the left of MSD of second operand

Op. Code	Instruction	N	A Address	B Address	
R	Repeat	Number (0-14) of times to repeat next instruction in sequence	A = 0000 — do not staticize when repeating instruction A = 0001 — staticize when repeating instruction	B = 0000 — do not staticize when repeating instruction B = 0001 — staticize when repeating instruction	
S	Input/Output Sense	Indicates the input/output device to be sensed	A_1, A_2, A_3 = Must be zeros (000) A_0 = specifies tests to be performed	HSM address of the next instruction to be executed if the condition(s) being tested are present	
S	Input/Output Sense (DXC only)	Selects the Unit H — (first unit) I — (second unit)	A_0 = 1, has the other computer staticized an IOS (A_3 = 1) A_1, A_2 = Must be zeros (00) A_3 = 1	HSM address of the next instruction to be executed if the condition being tested is present	
S	Automatic Rollback Control	Selects the device	A_0 = Must be zero (0) A_1 = 4, allow hardware rollback A_1 = 8, don't allow hardware rollback A_2, A_3 = Must be zeros (00)	B = Must be zeros (0000)	
S	Sense Read Error (Function 1)	M	A_0, A_1, A_2 = Must be zeros (000) A_3 = 1 Set Read Error Sense Enhancement OFF A_3 = 2 Set Read Error Sense Enhancement ON	Must be zeros (0000)	
	(Function 2)	M = first Control (318) S = second Control (319)	A_1, A_2, A_3 = Must be zeros (000) A_0 = 4 sense for read parity error	HSM address of the next instruction to be executed if the condition being tested is present	
T	Logical "AND"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand	
U	Exclusive "OR"	Number (0-44) of characters in each operand	HSM address of LSD in first operand (and result)	HSM address of LSD in second operand	
V	Store Register	Specifies Register to be stored: N = 0 — None N = 1 — P Register N = 2 — A Register N = 4 — B Register N = 8 — S Register N = & — U Register	HSM address of rightmost diad to receive contents of register, excluding A Register, specified by N. If A is stored, contents of A Register of previous instruction are stored in STA. The contents of A of this instruction are ignored	HSM address of next instruction if P Register is stored. Otherwise, B address is zero	

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
						$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes				$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes				$(A)_f = (A)_i$	$(B)_f = (B)_i$
						$(A)_f = (A)_i$	$(B)_f = (B)_i$
					Controls the Read Error Sense Enhancement Program Control Switch for 381 Tape Stations	$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes				$(A)_f = (A)_i$	$(B)_f = (B)_i$
			Yes	Yes	Operation right to left. PRN is set if the result is all zeros, otherwise PRP is set	$(A)_f$ = HSM address one to the left of MSD in result	$(B)_f$ = HSM address one to the left of MSD in second operand
				Yes	Operation right to left	$(A)_f$ = HSM address one to the left of MSD in result	$(B)_f$ = HSM address one to the left of MSD in second operand
	Yes (Store A only)					$(A)_f = (A)_i - 2$, if B, P, S, or U are stored. $(A)_f = (A)_f$ of previous instruction if A is stored $(A)_f = (A)_i$ if N equals zero	$(B)_f = (B)_i$, if P, S, or U are stored. $(B)_f = (B)_f$ of previous instruction if A or B Register is stored $(B)_f = (B)_i$ if N equals zero

Op. Code	Instruction	N	A Address	B Address	
W	Conditional Transfer of Control	Specifies element to be sensed: N = 0, None N = 1, PRI's N = 2, Overflow Indicators N = 4, Simultaneous Mode Indicator N = 8, EF/ED Normal Indicator N = &, Interrupt Indicator N = —, EF/ ED Simultaneous Indicator	HSM address of next instruction if one of the following conditions is true: N = 1 and PRP is set N = 2 and first overflow indicator is set N = 4 and a read is in Simultaneous Mode N = 8 and EF/ED Normal Indicator is set N = & and Interrupt Indicator is set (INT button is on) N = — and EF/ED Simultaneous Indicator is set	HSM address of next instruction if one of the following conditions is true: N = 1 and PRN is set N = 2 and neither overflow indicator is set N = 4 and a "write" is in the Simultaneous Mode N = 8 and the EF/ED Normal Indicator is not set N = & and the Interrupt Indicator is not set N = — (minus) and the EF/ED Simultaneous Indictor is not set	
X	Tally	0 (zero)	HSM address of diad containing the quantity to be tested	HSM address of next instruction if quantity has not been exhausted	
Y	Compare Left	Number (0-44) of characters to be compared	HSM address of leftmost character of first operand	HSM address of leftmost character of second operand	
0	Card Read Normal (Model 323)	Selects card reader and reading rate	HSM address of first character read from punched cards	Must be zeros (0000)	
0	Card Read Normal (Models 324, 329 Card Reader — Card-Reader Punch)	Specifies translate or binary mode	HSM address of first character read from punched cards	Must be zeros (0000)	
1	Card Read Simultaneous (Model 323)	Selects card reader and reading rate	HSM address of first character read from punched cards	Must be zeros (0000)	
1	Card Read Simultaneous (Models 324, 329 Card Reader — Card-Reader Punch)	Specifies translate or binary mode	HSM address of first character read from punched cards	Must be zeros (0000)	
2	Card Punch Normal (Model 334 Card Punch)	Must be zero (0)	HSM address of first character to be punched	HSM address of last character to be punched	
2	Card Punch Normal (Model 336 Card Punch)	Determines rate at which cards are to be punched	HSM address of first character to be punched	Must be zeros (0000)	

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
		Yes			The next instruction in sequence is performed if: 1. N = 0 2. N = 1 and PRZ is set 3. N = 2 and Second Overflow indicator is set 4. N = 4 and Simultaneous Mode is unoccupied	$(A)_f = (A)_i$	$(B)_f = (B)_i$
		Yes			Maximum value of tally quantity is 99	$(A)_f = (A)_i$	$(B)_f = (B)_i$
			Yes		Operation left to right PRZ set when content of N decreases to zero PRP set when value of character addressed by (A) > than that of (B) PRN set when value of character addressed by (A) < than that of (B)	$(A)_f$ = HSM address one to the right of last character compared in first operand	$(B)_f$ = HSM address one to the right of last character compared in second operand
					Operation left to right	$(A)_f$ = HSM address one to the right of last character read into HSM	$(B)_f = (A)_i$ BCT off $(B)_f = (A)_i + 80$ BCT on
					Operation left to right	$(A)_f$ = HSM address one to the right of last character read into HSM	$(B)_f = (A)_i$ translate mode $(B)_f = (A)_i$ +80 binary mode
					Operation left to right	$(S)_f$ = HSM address one to right of last character read into HSM	$(T)_f = (A)_i$ BCT off $(T)_f = (A)_i + 80$ BCT on
					Operation left to right	$(S)_f$ = HSM address one to the right of last character read into HSM	$(T)_f = (A)_i$ translate mode $(T)_f = (A)_i$ +80 binary mode
					Operation left to right	$(A)_f$ = HSM address one to right of last character punched	$(B)_f = (B)_i$
					Operation left to right	$(A)_f = (A)_i + 80$	$(B)_f = (B)_i$

Op. Code	Instruction	N	A Address	B Address	
2 330	Card Punch Normal (Card Reader — Punch)	Specifies translate or binary mode	HSM address of first character to be punched	HSM address of last character to be punched	
3	Card Punch Simultaneous (Model 334 Card Punch)	Must be zero (0)	HSM address of first character to be punched	HSM address of last character to be punched	
3	Card Punch Simultaneous (Model 336 Card Punch)	Determines rate at which cards are to be punched	HSM address of first character to be punched	Must be zeros (0000)	
3	Card Punch Simultaneous (Card Reader — Punch)	Specifies translate or binary mode	HSM address of first character to be punched	HSM address of last character to be punched	
4	Tape Read Forward Normal	Specifies Tape Station, Paper Tape Reader, or Interrogating Typewriter	HSM address of first character to be read	HSM address of last character to be read	
4	Tape Read Forward Normal (Data Exchange Control)	H — first unit I — second unit	HSM address of first diad to be read (even)	HSM address of last diad to be read (even)	
5	Tape Read Forward Simultaneous	Specifies Tape Station, Paper Tape Reader, or Interrogating Typewriter	HSM address of first character to be read	HSM address of last character to be read	
5	Tape Read Forward Simultaneous (Data Exchange Control)	H — first unit I — second unit	HSM address to first diad to be read (even)	HSM address of last diad to be read (even)	
6	Tape Read Reverse Normal	Specifies Tape Station or Paper Tape Reader	HSM address of first character to be read	HSM address of last character to be read	

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
					Operation left to right	$(A)_f$ = HSM address one to right of last character punched	$(B)_f = (B)_i$
					Operation left to right	$(S)_f$ = HSM address one to the right of last character punched	$(T)_f = (B)_i$
					Operation left to right	$(S)_f = (A)_i + 80$	$(T)_f = (B)_i$
					Operation left to right	$(S)_f$ = HSM address one to right of last character punched	$(T)_f = (B)_i$
	Yes		Yes	Yes	Operation left to right PRP set when (A) = (B) before gap occurs on tape PRN set when (A) $\neq$ (B) and gap occurs PRZ set when (A) = (B) and gap occurs on tape EF/ED Normal Indicator set if ED or EF alone is read from mag. tape	$(A)_f$ = HSM address one to the right of last character read	$(B)_f = (B)_i$
	Yes				Operation left to right	Instr. terminated on AB equality $(A)_f = (B)_i + 2$ Instr. terminated by receipt of terminate signal $(A)_f = (A)_i$ + the number of characters transferred +2	$(B)_f = (B)_i$ $(B)_f = (B)_i$
					Operation left to right. ED/EF Simultaneous Indicator set if an ED or EF alone is read from mag. tape	$(S)_f \neq$ HSM address one to the right of last character read	$(T)_f = (B)_i$
	Yes				Operation left to right	Instr. terminated on AB equality $(S)_f = (B)_i + 2$ Instr. terminated by receipt of terminate signal $(S)_f = (A)_i$ + the number of characters transferred +2	$(T)_f = (B)_i$ $(T)_f = (B)_i$
	Yes		Yes	Yes	Operation right to left PRP set when (A) = (B) before gap occurs on tape PRN set when (A) $\neq$ (B) and a gap occurs PRZ set when (A) = (B) and a gap occurs EF/ED Normal Indicator is set if an EF or ED alone is read from mag. tape.	$(A)_f$ = HSM address one to the left of last character read	$(B)_f = (B)_i$

Op. Code	Instruction	N	A Address	B Address
7	Tape Read Reverse Simultaneous	Specifies Tape Station or Paper Tape Reader	HSM address of first character to be read	HSM address of last character to be read
8	Tape Write Normal	Specifies Tape Station, Paper Tape Punch, Monitor Printer, or Interrogating Typewriter	HSM address of first character to be written, punched or typed	HSM address of last character to be written, punched or typed
8	Tape Write Normal (Data Exchange Control)	H — first unit I — second unit	HSM address of first diad to be transferred (even)	HSM address of last diad to be transferred (even)
8	Print Tape Normal (Multiple Tape Lister)	— (minus)	HSM address of first character to be sent to buffer	HSM address of last character to be sent to buffer
9	Tape Write Simultaneous	Specifies Tape Station, Paper Tape Punch, Monitor Printer, or Interrogating Typewriter	HSM address of first character to be written, punched or typed	HSM address of last character to be written, punched or typed
9	Tape Write Simultaneous (Data Exchange Control)	H — first unit I — second unit	HSM address of first diad to be transferred (even)	HSM address of last diad to be transferred (even)
9	Print Tape Simultaneous (Multiple Tape Lister)	— (minus)	HSM address of first character to be sent to buffer	HSM address of last character to be sent to buffer
*	Record File Mode Read	2^3, 2^2, 2^1, 2^0 selects number of blocks to be read 2^5, 2^4 selects File Unit	HSM address where first character is to be placed	B_0 = Must be zero (0) B_1 = odd — record returned to cage after instruction B_1 = even — record remains on turntable and arm placed at beginning of selected band after instruction B_2 = 1 — block terminates on count of 900 characters B_2 = 0 — count or EB recognition B_3 = addresses cells 1-10
%	Record File Mode Write	2^3, 2^2, 2^1, 2^0 selects number of blocks to be written 2^5, 2^4 selects File Unit	HSM address of first character to be written	B_0 = Must be zero (0) B_1 = odd — record returned to cage after instruction B_1 = even — record remains on turntable and arm placed at beginning of selected band after instruction B_2 = 1 — block terminates on count of 900 characters B_2 = 0 — count or EB recognition B_3 = addresses cells 1-10
;	Rewind to BTC	Specifies tape station	Must be zeros (0000)	Must be zeros (0000)

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
					Operation right to left ED/EF Simultaneous Indicator set if an ED or EF is read from mag. tape	$(S)_f$ = HSM address one to the left of last character read	$(T)_f = (B)_i$
					Operation left to right Tape motion forward	$(A)_f$ = HSM address one to the right of last character written, punched, or typed	$(B)_f = (B)_i$
					Operation left to right	$(A)_f = (B)_i + 2$	$(B)_f = (B)_i$
					Operation left to right	$(A)_f$ = Address of location one to the right of the last character printed	$(B)_f = (B)_i$
					Operation left to right Tape motion forward	$(S)_f$ = HSM address one to the right of last character written, punched, or typed	$(T)_f = (B)_i$
					Operation left to right	$(S)_f = (B)_i + 2$	$(T)_f = (B)_i$
					Operation left to right	$(S)_f$ = Address of location one to the right of the last character printed	$(T)_f = (B)_i$
					Operation left to right	$(U)_f$ = HSM address one to the right of last character placed	$(V)_f = (B)_i$
					Operation left to right	$(U)_f$ = HSM address one to the right of last character written	$(V)_f = (B)_i$
					Direction of tape motion is reverse and independent of computing	$(A)_f = (A)_i$	$(B)_f = (B)_i$

Op. Code	Instruction	N	A Address	B Address	
;	Input-Output Control	((open parenthesis)	$A_0A_1A_2$ = Must be zeros (000) A_3 designates function to be performed	Must be zeros (0000)	
#	Transfer Data by Symbol Left	Selected symbol on which to stop transferring	HSM address of leftmost character to be transferred	HSM address of destination of first character	
+	Add	Number (0-44) of characters in each operand	HSM address of LSD of augend and sum	HSM address of LSD of addend	
—	Subtract	Number (0-44) of characters in each operand	HSM address of LSD or minuend and difference	HSM address of LSD subtrahend	
•	Halt	0 (zero), may be used to designate type of stop	0000 (zero), may be used for numeric constants (0-9)	0000 (zero), may be used for numeric constants (0-9)	

OF INSTRUCTIONS (Continued)

	STA	STP	Set PRI's	Repeat	Remarks	Final Register Contents	
						A Register	B Register
					Used to control the Read Release and Stacker Select Functions for the Card Reader-Punch, Card Readers, Models 324, 329	$(A)_f = (A)_i$	$(B)_f = (B)_i$
	Yes			Yes	Operation left to right	$(A)_f$ = HSM address one to the right of specified symbol in origin area	$(B)_f$ = HSM address one to the right of symbol in destination area
			Yes	Yes	Operation right to left with the sign in the zone bit 2^5 of LSD. PRI's set as follows: PRP if sum is + PRZ if sum is 0 PRN if sum is −	$(A)_f$ = HSM address one to left of MSD of sum	$(B)_f$ = HSM address one to the left of MSD of addend
			Yes	Yes	Operation right to left with the sign in the zone bit 2^5 of LSD. PRI's set as follows: PRP if result is + PRZ if result is 0 PRN if result is −	$(A)_f$ = HSM address one to left of MSD of difference	$(B)_f$ = HSM address one to left of MSD of subtrahend
					Stops the computer after completion of any instruction in the Simultaneous Mode	$(A)_f = (A)_i$	$(B)_f = (B)_i$

APPENDIX D. INSTRUCTION TIMING*

Op. Code	Instruction	Timing in μs	Expository Notes
A	Translate by Table	21n + 35	n = no. of characters to be translated
B	Print and Paper Advance Normal	a. 60† b. 76† c. 6.67 ms. per line	a. Print and paper advance of one line in Synchronous Mode b. Print and paper advance of one line in Asynchronous Mode c. Paper advance rate after first line
C	Print and Paper Advance Simultaneous	a. 60† b. 76† c. 6.67 ms. per line	a. Print and paper advance of one line in Synchronous Mode b. Print and paper advance of one line in Asynchronous Mode c. Paper advance rate after first line
D	Band Select Normal	a. $21(B_1) + 14(B_2) + 42$ b. 3.1‡	a. To initiate selection b. Average time to perform Band Selection (Band located on record 32 positions from turntable)
D	Track Select	a. 42 *363-2 363-3 363-4 363-5* b. 105† 125† 145† 145† c. 150† 160† 185† 185†	a. To initiate selection b. Average selection time c. Maximum selection time
E	Band Select Record File Mode	a. $21(B_1) + 14(B_2) + 42$ b. 3.1‡	a. To initiate selection b. Average time to perform Band Selection (Band located on record 32 positions from turntable)
F	Block Read Record Normal	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and read a cell c. Average time to begin reading from the fifth cell of a band d. Return record to cage
F	Sector Read Disc Normal	a. 25† b. 32 KC	a. Average File Latency b. Character transfer rate
G	Block Read Record Simultaneous	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and read a cell c. Average time to begin reading from the fifth cell of a band d. Return record to cage

* STA or STP where applicable, and staticizing time included in formulas.

† Time here in milliseconds.

‡ Time here in seconds.

§ Does not include staticizing time, stop-start, or switching time.

APPENDIX D. INSTRUCTION TIMING* (Continued)

Op. Code	Instruction	Timing in μs	Expository Notes
G	Sector Read Disc Simultaneous	a. 25† b. 32 KC	a. Average File Latency b. Character transfer rate
H	Block Write Record Normal	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and write a cell c. Average time to begin reading from the fifth cell of a band d. Return record to cage
H	Sector Write Disc Normal	a. 25 b. 32 KC	a. Average File Latency b. Character transfer rate
I	Block Write Record Simultaneous	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and write a cell c. Average time to begin writing from the fifth cell of a band d. Return record to cage
I	Sector Write Disc Simultaneous	a. 25† b. 32 KC	a. Average File Latency b. Character transfer rate
J	Transfer Symbol to Fill	7n + 35	n = no. of locations filled
K	Locate Symbol Left	14n + 56	n = no. of characters searched
L	Locate Symbol Right	14n + 56	n = no. of characters searched
M	Transfer Data Left	14n + 35	n = no. of characters transferred
N	Transfer Data Right	14n + 35	n = no. of characters transferred
P	Transfer Data by Symbol Right	14n + 49	n = no. of characters transferred
Q	Logical "OR"	21n + 35	n = no. of characters in each operand
R	Repeat	49	
S	Input/Output Sense	a. 56 b. 42	a. If a transfer is executed b. If no transfer takes place
S	Hardware Rollback Control	42	
S	Sense Read Error	a. 42 b. 56 c. 42	a. Set the Program Control Switch b. If a transfer is executed c. If no transfer takes place
T	Logical "AND"	21n + 35	n = no. of characters in each operand
U	Exclusive "OR"	21n + 35	n = no. of characters in each operand

* See Footnotes on page D-1.

APPENDIX D. INSTRUCTION TIMING* (Continued)

Op. Code	Instruction	Timing in μs	Expository Notes
V	Store Register	49	
W	Conditional Transfer of Control	a. 49 b. 35	a. If a transfer of control takes place b. If no transfer of control takes place
X	Tally	a. 70 b. 49	a. When tally quantity is greater than zero upon starting b. When tally quantity is equal to zero upon starting
Y	Compare	21n + 35	n = no. of characters compared
0	Card Read Normal	a. 600 cards/min§ b. 300 cards/min§ c. 800 cards/min§ d. 900 cards/min e. 1500 cards/min	a. If N = 4 } Model 323 b. If N = M } c. Card Reader-Punch d. Card Reader, Model 324 e. Card Reader, Model 329
1	Card Read Simultaneous	a. 600 cards/min§ b. 300 cards/min§ c. 800 cards/min§ d. 900 cards/min e. 1500 cards/min	a. If N = 4 } Model 323 b. If N = M } c. Card Reader-Punch d. Card Reader, Model 324 e. Card Reader, Model 329
2	Card Punch Normal	a. 100 cards/min§ b. 200 cards/min§ c. 250 cards/min§	a. Model 334 Punch b. Model 336 Punch c. Card Reader-Punch
3	Card Punch Simultaneous	a. 100 cards/min§ b. 200 cards/min§ c. 250 cards/min§	a. Model 334 Punch b. Model 336 Punch c. Card Reader-Punch
4	Tape Read Forward Normal§	a. 10 KC b. 30 KC c. Up to 1000 char/sec d. 33.3 KC e. 66.7 KC f. manual keyboard	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of reading Paper Tape d. Rate of model 581 station e. Rate of model 582 station f. Rate of Interrogating Typewriter
4	Tape Read Forward Normal (DXC only)	Depends upon mode in which transfer is made and availability of status levels in both processors.	Rate of Data Exchange Control

* See Footnotes on page D-1.

APPENDIX D. INSTRUCTION TIMING* (Continued)

Op. Code	Instruction	Timing in μs	Expository Notes
5	Tape Read Forward Simultaneous§	a. 10 KC b. 30 KC c. Up to 1000 char/sec d. 33.3 KC e. 66.7 KC f. manual keyboard	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of reading Paper Tape d. Rate of model 581 station e. Rate of model 582 station f. Rate of Interrogating Typewriter
5	Tape Read Forward Simultaneous (DXC)	Depends upon mode in which transfer is made and availability of status levels in both processors.	Rate of Data Exchange Control
6	Tape Read Reverse Normal§	a. 10 KC b. 30 KC c. Up to 1000 char/sec d. 33.3 KC e. 66.7	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of reading Paper Tape d. Rate of model 581 station e. Rate of model 582 station
7	Tape Read Reverse Simultaneous§	a. 10 KC b. 30 KC c. Up to 1000 char/sec d. 33.3 KC e. 66.7 KC	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of reading Paper Tape d. Rate of model 581 station e. Rate of model 582 station
8	Tape Write Normal§	a. 10 KC b. 30 KC c. Up to 300 char/sec d. 33.3 KC e. 66.7 KC f. Up to 10 char/sec	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of punching Paper Tape d. Rate of model 581 station e. Rate of model 582 station f. Rate of M.P. or Interrogating Typewriter
8	Tape Write Normal (DXC)	Depends upon mode in which transfer is made and availability of status levels in both processors.	Rate of Data Exchange Control
8	Print Tape Normal (Multiple Tape Lister)	a. 30.0† b. 18 ms per line	a. Print and paper advance one line. b. Paper advance to top of form is 18 ms per line.
9	Tape Write Simultaneous§	a. 10 KC b. 30 KC c. Up to 300 char/sec d. 33.3 KC e. 66.7 KC f. Up to 10 char/sec	a. Rate of Hi-Data Tape, Model 381 b. Rate of Hi-Data Tape, Model 382 c. Rate of punching Paper Tape d. Rate of model 581 station e. Rate of model 582 station f. Rate of M.P. or Interrogating Typewriter

* See Footnotes on page D-1.

APPENDIX D. INSTRUCTION TIMING* (Continued)

Op. Code	Instruction	Timing in μs	Expository Notes
9	Tape Write Simultaneous (DXC)	Depends upon mode in which transfer is made and availability of status levels in both processors.	Rate of Data Exchange Control
9	Print Tape Simultaneous (Multiple Tape Lister)	a. 30.0† b. 18 ms per line	a. Print and paper advance one line. b. Paper advance to top of form is 18 ms per line.
*	Record File Mode Read§	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and read a cell c. Average time to begin reading of fifth cell of a band d. Time to return record to cage
%	Record File Mode Write§	a. 2.5 KC b. 400† c. 3.04‡ d. 1.6‡	a. Character transfer rate b. Inter-cell gap time and write a cell c. Average time to begin writing to fifth cell of a band d. Time to return record to cage
;	Rewind to BTC	Less than 180‡	Time to rewind full tape
;	Input/Output Control	42	
#	Transfer Data by Symbol Left	14n + 49	n = no. of characters to be transferred
+	Add	a. 28n + 49 b. 21n + 14	a. Time when an "end around condition" does not exist b. Time that must be added to "a" when an "end around condition" exists n = no. of characters in each operand
−	Subtract	a. 28n + 49 b. 21n + 14	a. Time when an "end around condition does not exist b. Time that must be added to "a" when an "end around condition" exists n = no. of characters in each operand
●	Halt	35	

* See Footnotes on page D-1.

APPENDIX E. STANDARD HIGH SPEED MEMORY LOCATIONS

HSM Locations	Use
0000-0099	Sum Table
0100-0199	Difference Table
0202-0205	Card Punch — Temporary storage of address
0206-0209	Arithmetic — Temporary storage of address
0212-0215	STA
0216-0219	STP
0222-0225	Standard Location for Storing P in a Repeat Instruction
	Model 303 Processor:
9900-9977	Print Table
9978-9999	Reserved
	Model 304 Processor:
I900-I977	Print Table
I978-I999	Reserved
	Model 305 Processor:
Z900-Z977	Print Table
Z978-Z999	Reserved

APPENDIX F-I. SYMBOLS USED FOR N CHARACTER COUNTS EXCEPT IN REPEAT AND PAPER ADVANCE INSTRUCTIONS

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	11	A	22	K	33	T
1	1	12	B	23	L	34	U
2	2	13	C	24	M	35	V
3	3	14	D	25	N	36	W
4	4	15	E	26	O	37	X
5	5	16	F	27	P	38	Y
6	6	17	G	28	Q	39	Z
7	7	18	H	29	R	40	EB
8	8	19	I	30	"	41	, (comma)
9	9	20	– (minus)	31	/	42	%
10	&	21	J	32	S	43	● (ISS)
						44	=

APPENDIX F-II. SYMBOLS USED FOR N CHARACTER COUNTS IN REPEAT AND PAPER ADVANCE INSTRUCTIONS

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	4	4	8	8	12	@
1	1	5	5	9	9	13	(
2	2	6	6	10	(space)	14	)
3	3	7	7	11	#		

APPENDIX G. DEVICE IDENTIFICATION FOR INPUT/OUTPUT AND IOS INSTRUCTIONS

IOS INSTRUCTIONS

Device	First Unit	Second Unit
Card Reader	(	
Card Punch	)	
Paper Tape Reader	8	
Paper Tape Punch	9	
On-Line Printer	7	G
Data Disc File	R	Z
Data Record File (under control of RFC Unit)	R	Z
Data Record File (under control of RFM Unit)	#$.,	
Hi-Data Tape Group	123456	ABCDEF
Dual Tape Channel (Model 341, 351)	123456	
Dual Tape Channel (Model 342, 352)	123456ABCDEF	
Tape Adapter, 33 KC	J	N
66 KC	L	P
Interrogating Typewriter	U	
Data Exchange Control	H	I
Multiple Tape Lister	— (minus)	

INPUT/OUTPUT INSTRUCTIONS

Device	First Unit	Second Unit
Card Reader (Model 323, 324, 329) or Reader Unit (Model 330)	2^4 bit = 0	
Card Punch (Model 334) or Punch Unit (Model 330)	0 (zero)	
Card Punch (Model 336)*	1, 2, 4	
Paper Tape Reader	8	
Paper Tape Punch	9	
On Line Printer	2^4 bit = 0	2^4 bit = 1
Monitor Printer	7	
Data Disc File:		
Track Select	R	Z
Read-Write	2^4 bit = 0	2^4 bit = 1
Data Record File:		
Record File Control		
Band Select	2^4 bit = 0	2^4 bit = 1
Read-Write	2^4 bit = 0	2^4 bit = 1
Record File Mode		
Band Select**	$2^4\,2^5 = 00$	$2^4\,2^5 = 01$
Read-Write	$2^4\,2^5 = 00$	$2^4\,2^5 = 01$
Hi-Data Tape Group	123456	ABCDEF
Dual Tape Channel (Model 341, or 351)	123456	
Dual Tape Channel (Model 342, or 352)	123456ABCDEF	
Tape Adapter		
33 KC	J	N
66 KC	L	P
Interrogating Typewriter	U	
Multiple Tape Lister	— (minus)	
Data Exchange Control	H	I

* Also Indicates Speed and Ending Routine

** Third Unit — $2^4\,2^5 = 10$; Fourth Unit — $2^4\,2^5 = 11$

APPENDIX H. PRINT TABLE*

Character	Table Location Memory Size			Character	Table Location Memory Size		
	10,000	20,000	40,000		10,000	20,000	40,000
— Minus	9900	I900	Z900	A Letter	9940	I940	Z940
+ Plus	9901	I901	Z901	B Letter	9941	I941	Z941
Space	9902	I902	Z902	C Letter	9942	I942	Z942
0 Zero	9903	I903	Z903	D Letter	9943	I943	Z943
1 One	9904	I904	Z904	E Letter	9944	I944	Z944
2 Two	9905	I905	Z905	F Letter	9945	I945	Z945
3 Three	9906	I906	Z906	G Letter	9946	I946	Z946
4 Four	9907	I907	Z907	H Letter	9947	I947	Z947
5 Five	9910	I910	Z910	I Letter	9950	I950	Z950
6 Six	9911	I911	Z911	J Letter	9951	I951	Z951
7 Seven	9912	I912	Z912	K Letter	9952	I952	Z952
8 Eight	9913	I913	Z913	L Letter	9953	I953	Z953
9 Nine	9914	I914	Z914	M Letter	9954	I954	Z954
, Comma	9915	I915	Z915	N Letter	9955	I955	Z955
. Period	9916	I916	Z916	O Letter	9956	I956	Z956
@ At	9917	I917	Z917	P Letter	9957	I957	Z957
% Percent	9920	I920	Z920	Q Letter	9960	I960	Z960
: Colon	9921	I921	Z921	R Letter	9961	I961	Z961
# Number	9922	I922	Z922	S Letter	9962	I962	Z962
$ Dollar Sign	9923	I923	Z923	T Letter	9963	I963	Z963
) Close Parenthesis	9924	I924	Z924	U Letter	9964	I964	Z964
" Quote	9925	I925	Z925	V Letter	9965	I965	Z965
$_{10}$ Sub 10	9926	I926	Z926	W Letter	9966	I966	Z966
(Open Parenthesis	9927	I927	Z927	X Letter	9967	I967	Z967
] Close Bracket	9930	I930	Z930	Y Letter	9970	I970	Z970
; Semicolon	9931	I931	Z931	Z Letter	9971	I971	Z971
> Greater Than	9932	I932	Z932	CR Credit Symbol	9972	I972	Z972
÷ Divide	9933	I933	Z933	' Apostrophe	9973	I973	Z973
↑ Arrow Up	9934	I934	Z934	* Asterisk	9974	I974	Z974
[Open Bracket	9935	I935	Z935	& Ampersand	9975	I975	Z975
< Less Than	9936	I936	Z936	/ Virgule	9976	I976	Z976
= Equal Sign	9937	I937	Z937	¤ Lozenge	9977	I977	Z977

* Four of the 64 code configurations will not be available as standard 301 codes but can be generated by computer programming. Also, some of the 301 symbols do not appear in this list so that other symbols may be chosen to represent the 301 symbols. It is advisable to prevent energizing the hammers for spaces by placing the code $(17)_8$ in location 9902, I902, or Z902. In fact, the code $(17)_8$ can be placed in any location in the table when it is desired to prevent printing of the associated character. For this reason, too, any $(17)_8$ codes appearing in the print area will never cause printing of any character.

APPENDIX I. CONTROL CHARACTERS AND PRINTABLE CHARACTERS FOR THE MULTIPLE TAPE LISTER

CONTROL CHARACTERS

	2^3	2^2	2^1	2^0	Tape(s) To Be Printed	Number of Characters Transferred
6-TAPE LISTER	0	0	0	1	1	25
	0	0	1	0	2	25
	0	0	1	1	3	25
	0	1	0	0	4	25
	0	1	0	1	5	25
	0	1	1	0	6	25
	0	0	1	0	1 & 2	49
	0	0	1	1	1 & 3	49
	0	1	0	0	1 & 4	49
	0	1	0	1	1 & 5	49
	0	1	1	0	1 & 6	49
12-TAPE LISTER	0	0	0	1	1	25
	0	0	1	0	2	25
	0	0	1	1	3	25
	0	1	0	0	4	25
	0	1	0	1	5	25
	0	1	1	0	6	25
	1	0	0	1	7	25
	1	0	1	0	8	25
	1	0	1	1	9	25
	1	1	0	0	10	25
	1	1	0	1	11	25
	1	1	1	0	12	25
	0	0	1	0	1 & 2	49
	0	0	1	1	1 & 3	49
	0	1	0	0	1 & 4	49
	0	1	0	1	1 & 5	49
	0	1	1	0	1 & 6	49
	1	0	0	1	1 & 7	49
	1	0	1	0	1 & 8	49
	1	0	1	1	1 & 9	49
	1	1	0	0	1 & 10	49
	1	1	0	1	1 & 11	49
	1	1	1	0	1 & 12	49

$2^4 = 0$

$2^5 = 0$ — paper advance one line on tape or tapes printed.

1 — paper advance to top of form on tape or tapes printed.

APPENDIX I. CONTROL CHARACTERS AND PRINTABLE CHARACTERS FOR THE MULTIPLE TAPE LISTER (Continued)

PRINTABLE CHARACTERS

Print Positions 1 - 23		Print Position 24	
Character To Be Printed	Character In HSM	Character To Be Printed	Character In HSM
0	0	B	0
1	1	C	1
2	2	D	2
3	3	F	3
4	4	L	4
5	5	M	5
6	6	R	6
7	7	S	7
8	8	T	8
9	9	X	9
. (Period)	. (Period)	Y	. (Period)
, (Comma)	, (Comma)	⌑ (Lozenge)	, (Comma)
# (Number)	# (Number)	CR (Credit)	# (Number)
= (Equal)	= (Equal)	* (Asterisk)	= (Equal)
− (Minus)	− (Minus)	+ (Plus)	− (Minus)
Space	Space	Space	Space

APPENDIX J. GLOSSARY OF TERMS

Access Time. A time interval which is characteristic of a storage device, and is essentially a measure of the time required to communicate with that device. The time interval between (1) the instant at which information is called for from storage and the instant at which it is delivered or (2) the instant at which information is ready for storage and the instant at which it is stored.

Address (noun). An expression, which designates a particular location in a storage or memory device or other source or destination of information.

Absolute Address (Direct Address). The specific label assigned by the machine designer to a particular storage location. To code in absolute means to write a sequence of instructions in a computer code.

Address Generation. The development of a 3488 address from control information.

Hardware Address. A 3488 address comprised of device number, magazine number, card number and block number.

Indirect Address. The address of a memory location whose contents contain the address of another memory location to be accessed.

Instruction Address. (Line Number, Location). An expression used in coding to denote the address of a stored instruction. NOT a part of the instruction itself.

Logical Address. The next location relative to the location being processed by key or physicial location, dependent on the mode of processing.

Symbolic Address. A label expressed in a pseudo-code. To code using symbolic addresses implies that the sequence of instructions must be translated into absolute before being executed by a computer. Relative addresses are those symbolic addresses which are translated into absolute by sequencing from some specific "reference" address.

Bails. A mechanical device used to raise a group of 8 cards one of which will be extracted to the capstan on the 3488 Random Access Computer Equipment.

Band. An addressable area on the Data Record File. A band is a spiral groove around the record with a storage capacity of 9000 characters. Each band contains 10 cells of 900 characters each.

Band. The recording surface on a 3488 card comprised of two parallel tracks and containing four blocks.

Batch. Several groups of items in sequence, each separated by a sentinel and the entire grouping terminated by an EF. (This is contrasted to a single group of related items for a message.)

Beginning of Tape Control (BTC). A "window" placed at the beginning of a magnetic tape, where recording of data is not possible and which can be sensed photo-electrically.

Binary Code. A code composed of a combination of entities each of which can assume one of two possible states. Each entity must be identifiable in time or space.

Binary Digit. A digit (0 or 1) in binary notation. See Digit.

Binary Notation. A system of positional notation in which the digits are coefficients of powers of the base two. Synonymous with Binary Representation. See Positional Notation.

Binary Representation. Synonymous with Binary Notation. See Positional Notation.

Binary-to-Decimal Conversion. The mathematical process of converting a binary number to the equivalent quantity in decimal notation. For example: 001-1, 010-2, 011-3, 100-4, 101-5, etc.

Bit. A single binary digit having a value of either zero or one. The word is a contraction of "Binary Digit."

Block. A group of consecutive data considered or transferred as a unit, particularly with reference to input and output. On magnetic and paper tape, a block is a group of at least three characters preceded and followed by a space called an "inter-block gap." On the Data Record File Disc a Block is the information contained in one cell. From one to 900 characters of information may be recorded in a cell.

Bucket. The logical 3488 software addressing unit containing records and/or tags comprised of one or more consecutive blocks and having many of the properties of a batch on magnetic tape.

Home Bucket. The originally specified location of a record.

Visitor/Substitute/Overflow Bucket. The secondary location for the storage of information when the Home Bucket is unable to contain the data record.

Bucket Header. A control field at the beginning of a bucket consisting of 10 characters containing the status (flaw/tag/overflow) of the bucket and the physical limits of the bucket.

Bucket Overflow. A condition that occurs when a record/tag will not fit into a bucket and must be placed elsewhere.

Buffer. A storage device used to compensate for a difference in rate of flow of information or in time of occurrence of events when transmitting information from one device to another, as from an input device to the High-Speed Memory, or from the High-Speed Memory to an output device.

Bus. A main circuit, channel, or path for the transfer of information.

Capstan. (Refer to DRUM.)

Card. Any card adapted for being punched in an intelligent array of holes for the storage of information.

Card (3488 Card). The basic storage element of the 3488.

Home Card. The originally specified card for location of a data record.

Card Column. One of a number of columns in a card into which information is entered.

Card Feed. A mechanism which moves cards one by one into a processing device.

Card Overflow. A condition that occurs when there is no longer room on a 3488 card for the information being processed.

Card Punch. A mechanism which punches *cards.* An automatic card punch punches *cards* according to a stored program.

Card Reader. A mechanism that reproduces the information on cards in another form, usually electrical signals.

Card Stacker. A mechanism that stacks cards after they have passed through a machine.

Carry. (1) A condition occurring during addition when the sum of two digits in the same column equals or exceeds the base number. (2) The digit to be added to the next higher column.

Cell. An addressable area on the Data Record File. A cell may contain from one to 900 characters.

Channel. A Control Module which enables the selection of 3488 cards under program control. It also performs character parity checking and character buffering between a processor and a 3488.

Character. One of a set of elementary symbols which may be arranged in ordered aggregates to express information. These symbols, typewrite symbols, and any other symbols which a computer may read, store, or write.

Code (noun). A system of symbols and rules for their use in representing information. A language.

Pulse Code. The binary representation of characters.

Operation Code. The code representing an operation (add, subtract, transfer, etc.) built into the hardware of the computer.

Complement (noun). A quantity which is derived from a given computer quantity by the following rules:

a. Complement on n (as in tens complement). Subtract each digit of the given quantity from n-1, add unity to the least significant digit, and perform all resultant carries.

b. Complement on n-1 (as in nines complement). Subtract each digit of the given quantity from n-1.

Common Memory. That portion of high-speed memory (HSM) used to store constant information necessary for operation of a program. It is the portion of a program which must never be overlaid and contains instructions necessary to start a program, hardware subroutines, and file parameters.

Constant. A number is said to be a constant if it has the same value under all conditions. For example, in the formula (area of a circle) = Pi X (radius)^2, Pi is a constant, equal to 3.14159- - -, which applies to all circles.

Control Symbol. A character used to indicate the beginning or the end of unit of data (item, record, file, etc.).

Counter. A device (register or storage location) for storing integers, permitting these integers to be increased or decreased by units or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer.

Criterion (Key). A group of characters, usually comprising an item, used to identify a record.

CTC. Conditional transfer of control.

Decimal Number System. See Positional Notation.

Device Control Table. A portion of HSM containing information to be used in the execution of 3488 software accuracy checks and for performing the Rollback function. Contains Card/Block Select/Preselect information.

Device Number. The designation of the 3488 unit to be addressed.

Diad. A unit consisting of two consecutive HSM locations. Each diad begins with an "even" decimal address and ends with the next consecutive "odd" address.

Digit. One of the n symbols of integral value ranging from 0 to n-1, inclusive, in a scale numbering of base n. Examples of various types of digits are:
Binary Digits are 0 to 1
Octal Digits are 0 through 7
Decimal Digits are 0 through 9

Direct Address. The specific label assigned by the machine designer to a particular storage location. Synonymous with *Absolute Address.*

Drum. A revolving cylinder, with friction belts, on which a 3488 card is placed for reading/writing.

EB. End of Block Symbol.

ED. End of Data Symbol.

Edit. To rearrange information. Editing may involve the deletion of unwanted data, the selection of pertinent data, the insertion of invariant symbols such as page numbers and typewriter characters, and the application of standard processes such as zero suppression.

EF. End of File Symbol.

EI. End of Information Symbol.

End Data Symbol. A symbol which the computer interprets as meaning there is no data following the symbol. For example, the last character on a magnetic tape is the End Data Symbol.

End-Around-Carry. A carry in which the overflow from the column of highest order is added to the column of lowest order.

End of Tape Warning (ETW). A warning generated by a metal strip on the tape indicating that approximately 5 feet of usable tape is available.

End File Symbol. A symbol which the computer interprets as meaning all Data pertaining to a file precedes the symbol. For example, the last character in a file is the End File Symbol.

Erase. 1. To expunge, wipe out, or destroy stored information, usually without destroying the storage media.
2. To replace all the binary *digits* in a storage cell by binary zeros.

Error Register. A portion of HSM used to indicate error conditions for use in error recovery.

f. Used as subscript to denote final.

Field. A set of one or more characters which are treated as a whole; a unit of information.

File. The complete group of records to be processed. For example, the data relative to one employee in a payroll application is a record; the total records for all employees constitute a file.

File Mapping. The process used to layout and describe, by unit word, files contained in the 3488.

Flip-Flop. A device having two stable states and two input terminals (or types of input signals), each of which corresponds to one of the two states. (The two states may be considered as corresponding to "off" and "on" or to binary 0 and 1. The circuit remains in either state until it is caused to change to the other state by application of the corresponding signal.

Flaw. A physical defect on the recording surface of a 3488 card that will not permit satisfactory reading/writing.

Flaw Area. Area or bucket containing a flaw.

Flaw Replacement. Bucket to be used as a replacement for a bucket containing a flaw; much the way a visitor-substitute bucket is used.

Gap. A blank space on magnetic or paper tape. The gap is used to separate blocks or other units of data.

High-Speed Memory. Magnetic core storage in the Computer in the RCA 301 System. See also Storage.

High-Speed Memory (HSM) Location. A unit of magnetic core storage (High-Speed Memory) which can store (hold, remember) one RCA character. See Address.

HSM. High-Speed Memory.

i. Used as subscript to denote initial.

Indirect Address. The address of a memory location whose contents contain the address of another memory location to be accessed.

Input. (1) Information transferred into the computer. (2) The device by means of which information is fed into the computer.

Instruction. Information which conveys to a machine where the operands are obtained, what operations to perform, what to do with the result, and sometimes, where to obtain the next instruction.

Instruction Code. An artificial language for expressing the instruction to be carried out by a machine.

Item. An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.). In many cases an item is preceded by a symbol to define the beginning of each item.

Item Separator Symbol (ISS). Control symbol which may be used to designate the beginning of an item.

Jump Table. Record indicating executed transfers out of program sequence.

Justify. Shift an operand to effect right or left columnar alignment.

KC. Thousand characters per second.

Key. See Criterion.

Line. A line is composed of the characters that are to be printed on a single line on the On-Line Printer or Monitor Printer. Each character space to appear in the printed line decreases the maximum line capacity by one.

Line Printer. A printing device capable of printing an entire line of characters at one time.

Location. A storage position in the High-Speed Memory. Each location has a specific address and can hold one RCA character.

LSC. Least Significant (rightmost) character.

LSD. Least Significant (rightmost) Digit.

L to R. Left to right.

Machine Language. The system of coding which a computer "understands" internally.

Magazine. An interchangeable container for 3488 cards.

Magazine Control Card. Normally the last card of a magazine containing an index of all flaws/overflows and flaw/overflow storage areas.

Magnetic Storage. Any device which makes use of the magnetic properties of materials for the storage of information.

Magnetic Tape. A ribbon of paper, metal, or plastic, coated or impregnated with magnetic material on which information may be stored in the form of magnetically polarized areas.

Mask. A pattern consisting of 0 and/or 1 bits, used to alter the bit configuration of an operand.

Memory. See Storage.

Message. The data relative to a single item to be processed. For example, all data relative to a single inventory item is a message. See Record.

Microsecond. A millionth of a second.

Millisecond. A thousandth of a second.

Mnemonic Code. A pseudo-code in which information, usually instructions, is represented by symbols or characters which are readily identified with the information.

MSC. Most Significant (leftmost) character.

MSD. Most Significant (leftmost) Digit.

n. Number of characters (used in timing).

Number System. See Positional Notation.

Octal. See Positional Notation.

Octal Digit. One of the symbols 0, 1, 2, 3, 4, 5, 6, or 7 when used as a digit in octal notation.

Octal Notation. Notation of numbers in the scale of eight. The octal digits can be represented by the eight possible combinations of three binary digits.

Octonary. See Positional Notation.

Operand. Any one of the quantities entering into an operation.

Output (noun). (1) Information transferred from the computer to external storage. (2) The device to which the computer delivers information.

PA. Paper Advance.

Parameter (File). Information necessary to process a designated file (i.e., Memory allocations, etc.).

PC. Page Change.

Positional Notation. One of the schemes for representing numbers, characterized by the arrangement in sequence of digits which are to be interpreted as co-efficients of successive powers of an integer called the base of the number system.

In the *binary* number system the successive digits are interpreted as co-efficients of the successive powers of the base 2, just as in the *decimal* number system they relate to successive powers of the base 10.

In the ordinary number systems the digits are symbols which stand for zero and for the positive integers smaller than the base.

PRI's. Previous Result Indicators.

PRN. Previous Result Negative Indicator.

PRP. Previous Result Positive Indicator.

PRZ. Previous Result Zero Indicator.

Preamble. A pattern of bits recorded by hardware in front of all blocks as they are written. It is used to synchronize the reading timing clock when reading and read-after-write commands.

Preselect. The technique of overlapping card movement within the same Retrieval Unit. While one select is in process another may be readied for extraction. (See Select above.)

Program Control Card. A 3488 card containing information necessary to operate and maintain programs on the 3488.

Program Index. Specifies the Program name and the location of the program within the system.

Program Area Index. Describes the allocated program areas. Contains the file ID and a description of the program area.

Random Access. Access to storage under conditions in which the next position from which information is obtained, or to which it is delivered, is in no way dependent on the previous one.

RCA Character. See the RCA 301 Code, Appendix.

Record. A record consists of one or more related items with the amount of information in a record being completely variable.

Register. A storage device with a specifically assigned function and a given unit capacity. Registers in the computer in the RCA 301 System are of one, two, or four character capacity.

Relative Address. An address which specifies a location sequentially relative to a group of addresses but not a specific storage location.

Rewind. Move a tape in a backward direction to BTC.

Routine. A set of instructions arranged in proper sequence to cause a machine to perform a desired operation.

R to L. Right to Left.

RWD. Rewind.

Sector. An addressable unit of information on the Data Disc File. One sector contains 160 characters. Ten sectors are contained in one track.

Select. (Software usage — see explanations listed below.)

Card Select. The mechanical extraction of a 3488 card from a magazine and placing in on the drum.

Block Select. Placing a specified block under the read/write head while the 3488 card containing that block is on the drum.

Sign Position. The sign of each operand is indicated by the 2^5 bit of the least significant digit (LSD) of each operand. When a "one" bit is present in the 2^5 position, the sign is negative, otherwise it is assumed positive.

Simultaneity. The ability of the computer to execute more than one instruction at the same time.

Slot. An eight-character field in the File Parameter Area containing the address of the User Bucket area.

STA. Store A Register (automatic storage of final contents of A Register).

Standard Memory Locations. Designated locations in the HSM which are used for Arithmetic Tables, automatic storage of the final contents of certain Registers, etc. (See Appendix E.)

Start Time. Time between the command to start an input/output device and the reading or writing of the first character.

Storage (Memory). A device into which units of information can be transferred, which will hold this information, and from which the information can be obtained at a later time.

STP. Store P Register (automatic storage of final contents of P Register).

System. An assemblage of equipment units or instructions, or routines, designed to operate as a whole.

System Control Card. A description of every data file and magazine. Contains the following:

Data File Index. File ID and address of data file description.

Data File Description. Description of a data file. (Number of characters per record, number of blocks per bucket, and record type.)

On-Line Catalogue. Record of the locations of all magazines on-line.

Magazine Serial Number Index. Serial numbers of all magazines in the System.

Magazine Description. Description of all files including the allocated areas.

System Control Magazine. The magazine which contains the System Control Card(s).

Tag (Tag Address Record). Appears in a bucket and represents a Data Record which has been moved to another bucket. It contains the primary key of the moved record and the address of the bucket to which it was moved.

Tag Overflow. A condition where all records have been moved and the bucket contains all tags instead of records.

TRA. Translate by Table.

Track. An addressable area on the Data Disc File. One track contains 10 sectors of 160 characters each, or 1600 characters.

Unwind. Move a tape in the forward direction.

Working Storage. A portion of the internal storage reserved for intermediate and partial results during computation.

Zone. An addressable area on the Data Disc File. A zone consists of 128 tracks of 1600 characters each. One read-write arm services the 128 tracks.

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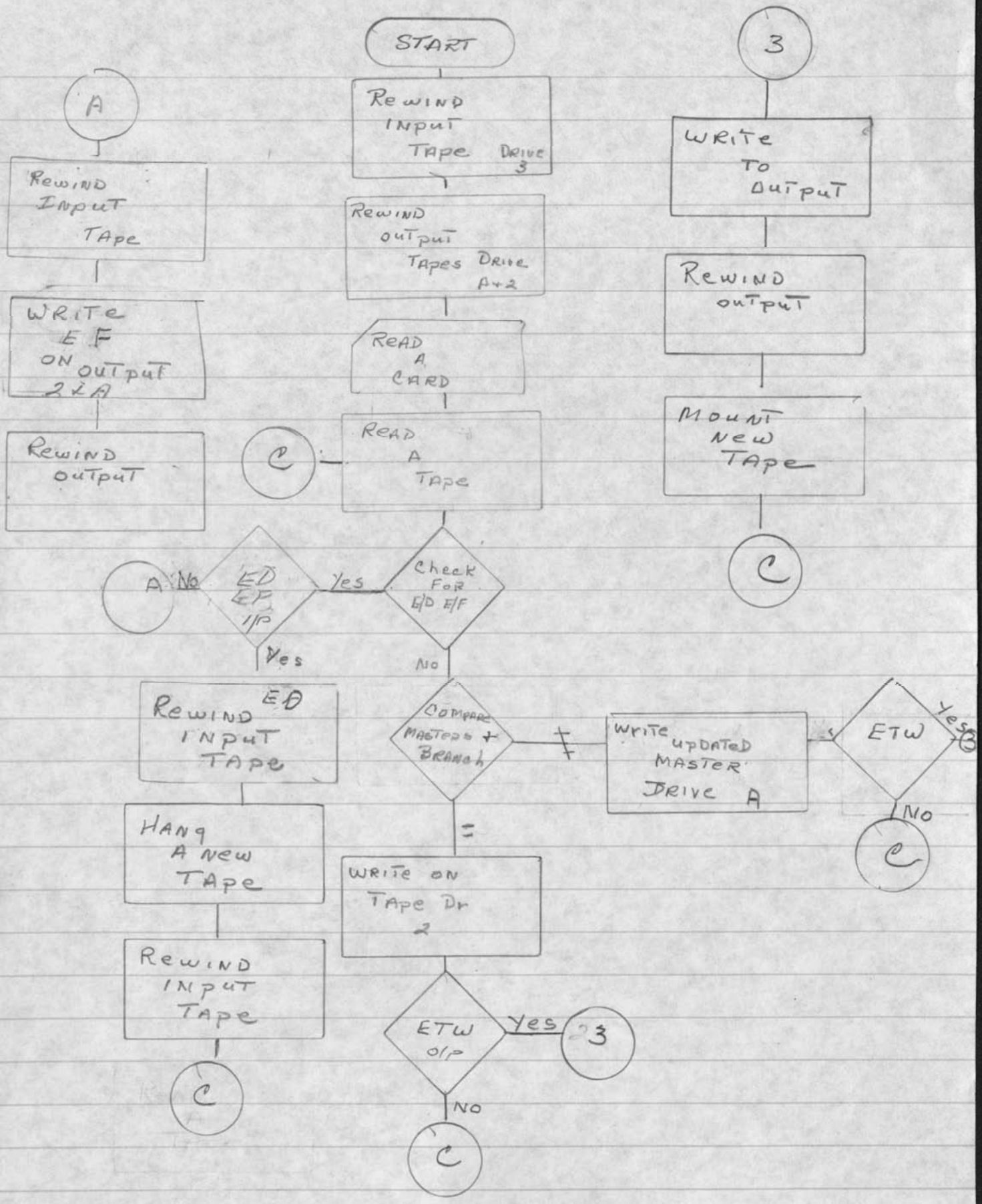
START
Rewind Input Tape Drive 3
Rewind output Tapes Drive A+2
Read A Card
Read A Tape
Check For E/D E/F
Yes
No
E/D E/F I/P
No
Yes
A
Rewind Input Tape
Write E/F on output 2 & A
Rewind output
C
Rewind E/D Input Tape
Hang A new Tape
Rewind Input Tape
C
Compare Masters + Branch
=
≠
Write on Tape Dr 2
Write updated Master Drive A
ETW
Yes
No
B
C
ETW o/p
Yes
3
No
C
3
Write to output
Rewind output
Mount New Tape
C