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4001 Miranda Ave. Dept. 3230
Palo Alto, CA 94304
(415) 858-4296

Gordon E. Moore
FAIRCHILD SEMICONDUCTOR CORPORATION
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#6

Standard B&P Blank Books and Loose Leaf Devices
TRADE MARK REGISTERED

Standard Figuring Book

No. 1602½

2	Columns	to Right,	Units,	Single	Page	Form
3	"	"	"	"	"	"
4	"	"	"	"	"	"
5	"	"	"	"	"	"
6	"	"	"	"	"	"
6	"	Divided,	"	"	"	"
7	"	to Right,	"	"	"	"
8	"	"	"	"	"	"
10	"	"	"	Double	Page	Form
12	"	"	"	"	"	"
14	"	"	"	"	"	"
14	"	Without Name Space	"	"	"	"
16	"	to Right,	"	"	"	"
18	"	"	"	"	"	"
20	"	"	"	"	"	"

Unruled
Quadrille
Faint

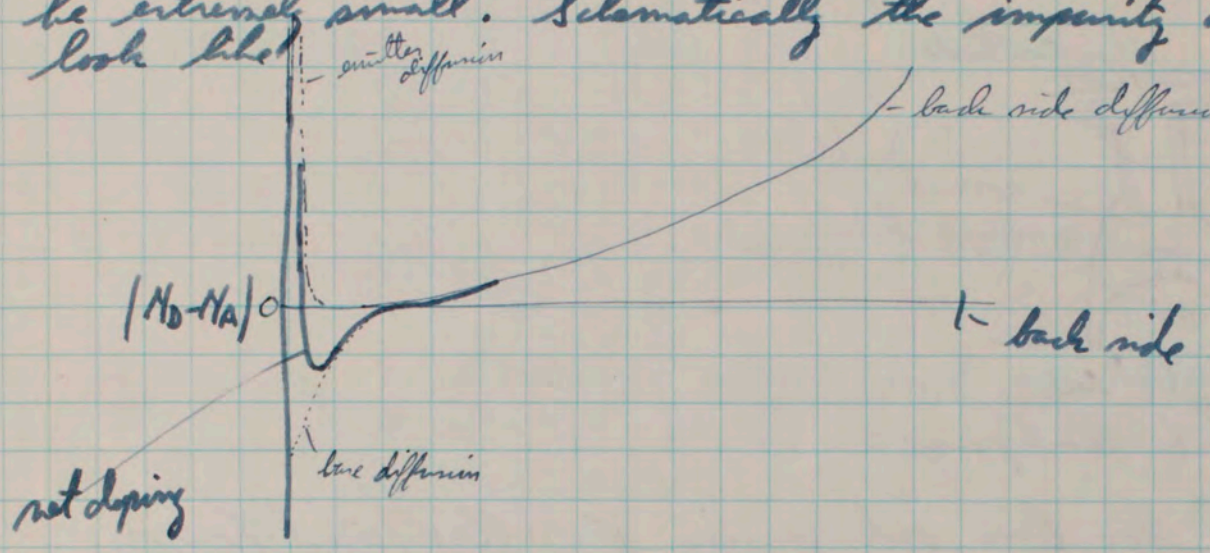
In 150 and 300 Pages

Made in U. S. A.

A BOORUM & PEASE PRODUCT

Oct 23, 1957

Bob Noyce pointed out during a meeting yesterday afternoon that a good way to make a transistor structure is to start with intrinsic material, diffuse deeply from one side and then make an ordinary double-diffused structure on the opposite side of the wafer of semiconductor material. That is, to make a device very similar to the p-i-p or n-i-n, but to let the "i" layer thickness be extremely small. Schematically the impurity distribution would look like:



(I was interrupted)

Oct 25, 1957 - back to the above

In order to produce the above structure Noyce recommended deep diffusion followed by a lapping operation wherein the progress is monitored by 4 point probe measurements and thermal probe measurements until the diffusion front is adequately close to the surface.

I propose that an impurity distribution accomplishing the result, but not requiring the delicate lapping step could be obtained by diffusing a wafer of approximately the final thickness obtained by Noyce method in such a manner that the diffusant source is confined to one surface of the wafer and a sink to pull the concentration of diffusant to very low values maintained at the opposite surface. Any diffusion that would go thru the wafer then gives an impurity distribution of the desired characteristics. It might be pointed out that if the capacity of the sink was very large a similar distribution could be obtained by out-diffusion from a heavily doped Xtal.

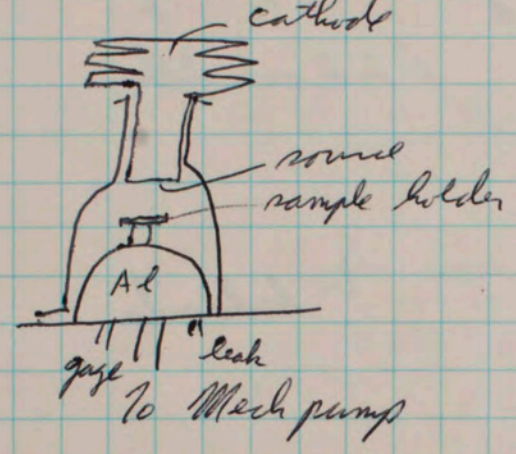
Gordon E. Moore 10/25/57

Read + understood - Jay T. Last 10/25/57

2 Feb. 26, 1958

Sputterer:

We built a sputterer during the last two weeks accd. to the design of R.T. Brown (slightly modified)



A big problem has been out-gassing of rubber and Tygon tubing in the pumping and leak parts of the system. Also the leak enters at the wrong part of the system since it doesn't flush the jar of released contaminants.

It seems reasonable to build a system to put on the large pumping station as soon as the sputtered film is shown to be superior.

Yesterday a run 10 min clean, 5 min sputter (pure silver) gave a sheet ~~con~~ resistivity of ~ 0.04 Ω/□. This ~~was~~ was with I sputter 10-15 ma, P_{Argon} 65μ, distance ~ 2 cm.

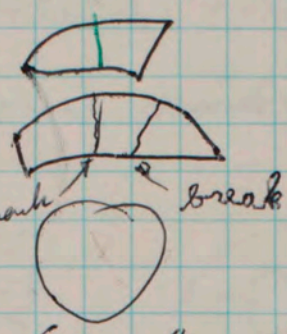
Bob Brown could weld to this film.

A run to test how ohmic pure Ag is to the base and emitter of our n-p-n transistor structure.

Apiece of Ga-2 $C_0 \sim 7.5 \times 10^{18}$

Apiece of P-6 V/I 3.6Ω, $k_j = 3.3$

Also a dummy



Put in Sputterer (pure Ag electrode)

Pumped for 5 min to dry (p = 8 μ @ gage setting 36)
Flushed 5 times with large amount of A_r.

Pressure adjusted to 60 μ and ~~data~~ cleaned for 10 min @ 30 ma (a couple of more flushes were given to get rid of H_2O vapor)

Sputtered 2½ min @ 30 ma (p went up to ~ 75 μ)

V/I on dummy: ~~.028~~ .025, .036, .025, .032, .022
over .040, .032, .020, .028, .038

on P-6 .048, .055, .062
.020, .018, .020

on Ga-2 .026, .022, .024
.100, .080, .054

The diffused wafers were cut as shown in picture. Part were made into mesas as is, part ~~Ag~~ were sent to Roger Mazy for alloying.

The two wafer sides could be distinguished under a microscope through the silver, even though the silver is cloudy appearing, almost flat alloy, on both sides. (Some brown stains).

2/26/58, cont

Un alloyed diode characteristics:

P-diode

V(mv)	I (reading)	scale	I (mm
100	1.4	0.1/ramp	
200	2.4	1.0 "	
300	2.0	10. "	
400	5.8	10'	
500	1.2	100	
600	2.2	"	
700	3.6	"	
800	4.8	"	
900	6.2	"	
1000	8.0	"	0.08
2000	4.2	1 ma	0.42
3000	1.2	10 ma	1.2
3800	1.7	10 ma	1.7

The Ga wafer gives comparable results. Hence, there is no question but that there must be alloyed.

DM 2/26

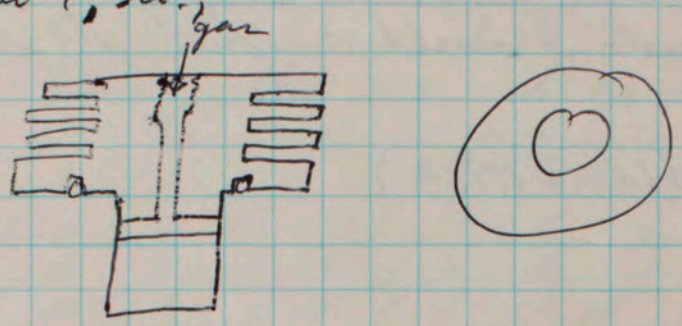
The pair of pairs that were sent for alloying will be checked in the next few days.

A Silver+2% Ga electrode was prepared and some sputtering done with it. Both runs showed a very dark brown layer on top of the deposit. This wipes off leaving Ag and is undoubtedly Ag_2O. This can pretty well gone from the pure Ag evaporations done about 5 th but appeared again later. This suggests that better clean-up is important.

GL Moore — 2/26

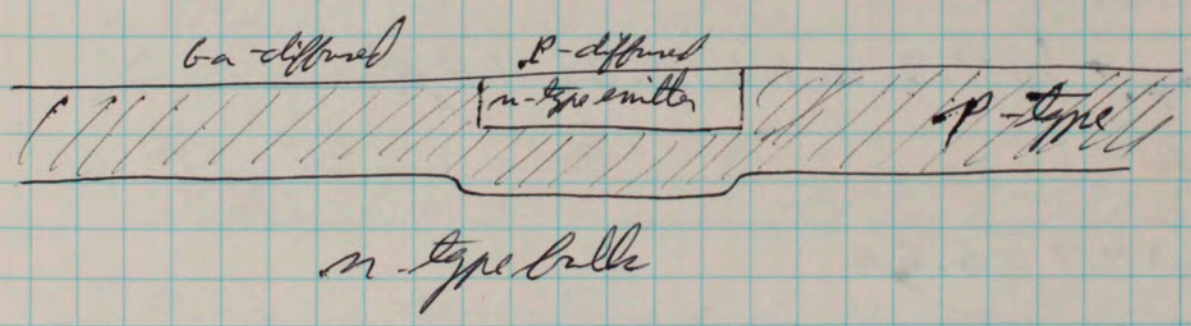
The sputtering of Ag_2O or CaO or BaO seems to come out brown or black in color. This looks like Ag_2O. Bob Noyce has succeeded in dissolving it in KCN (1%) solution - the brown, that is, not the Ag.

The new sputter source made so that the gas flows down through the chamber, i.e.



was put into operation. The gas flowing in this manner seemed to give a sort of focusing effect, concentrating the sputtered Ag near the center of the ~~source~~ sample holder.

Dave Allison observed again (I recall he showed me this once a couple of months ago) that the P-diffused emitter seem to cause the collector junction to go in further. This results in a stain pattern that looks like this:



This can be explained by saying that the P-doped silicon has a lower solubility for Ba than it does without the phosphorus. While this violates my intuition since BaP is a nice stable compound there is no other simple explanation that I can see. Some quantitative estimates of the effect can probably be made from Dave's measurements.

(Note - see next page: 3/4/58)

Gil Moore

6 Feb 28

From the observation described on the previous page (made by Dave Allison) some rough calculations were made. These are summarized below.

The extra driving force for Ga diffusion under the emitter can be represented as an "effective surface concentration" defined as that value of C_o for which an error function impurity distribution with the "ordinary" diffusion constant would account for the extra junction depth.

For the initial Ga diffusion (1 hr @ 1190°)

$\sqrt{Dt} \cong$ ~~1.0 μ~~ 1.1 μ

$\frac{C_{bulk}}{C_o} = \frac{5\times10^{15}}{5\times10^{18}} = 1.0\times10^{-3}$

Hence from curve of C/C_o vs $x_j/\sqrt{Dt}$ one finds $\frac{x_j}{\sqrt{Dt}} =$ ~~4.7~~

Then $x_j \cong$ ~~6.2 μ~~ ~~4.7 μ~~ 5.2

During the 15 min P-diffusion run (¼ hr @ 1190) the gallium diffusion length should increase so that

~~$\sqrt{Dt} = (\sqrt{Dt})_1$~~

$Dt = Dt_{orig.} + \frac{1}{4}\cdot 1.2 = 1.1 + 0.3 = 1.4\ \mu^2$

$\sqrt{Dt} \cong 1.2\ \mu$

or $x_j = 1.2 \times 4.7 \cong 5.6\ \mu$

But observed under the emitter is $x_j = (5.6 + 0.7)\ \mu = 6.3\ \mu$
(The diffuse 0.7 is measured as 0.65 ± 0.15)

Then $\frac{x}{\sqrt{Dt}} = \frac{6.3}{1.2} \cong 5.2$

Giving $C/C_o = 2.5\times10^{-4}$

or $C_o = \frac{5\times10^{15}}{2.5\times10^{-4}} = 2\times10^{19}$ as the "effective C_o."

GMP 2/28

While the extra driving force for Ga diffusion is ~~not~~ supplied by the phosphorus in the emitter region, it seems necessary that in the base region wherein the phosphorus concentration has fallen to nearly zero that this represent a true concentration.

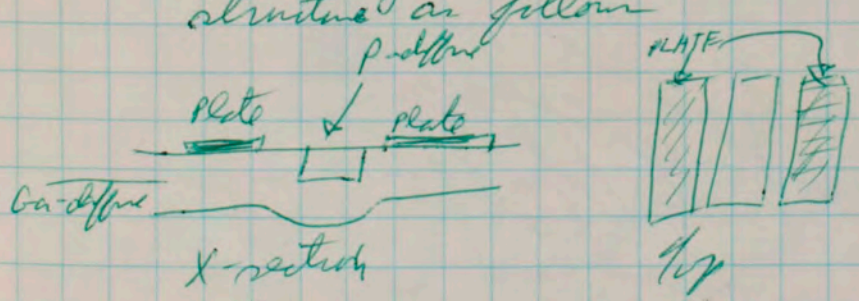
This calculation assumes that the high driving force for gallium diffusion is established immediately and maintained throughout the diffusion. Clearly this cannot be the case, since a time is required for the necessary diffusion to take place to establish the new gradients. Hence the calculated effect yielding a factor of 4 increase in the effective C_o over the original C_o is an average and really requires that the final value be much higher than the calculated one. I feel that even an increase in the gallium concentration of an order of magnitude directly under the emitter junction is not unreasonable to postulate to explain the excess gallium diffusion.

If such a concentration is real, it offers an explanation for some other observation otherwise very difficult to observe and is potentially very important in device design. At least ~~two~~ three methods of checking to see if this is a real concentration build up have been suggested. These are

1. (by GEM) Making a transistor and measuring V_{BE} - While not the most direct way of checking the concentration, it is most closely related to the practical interest.

2. Etching to remove the emitter layer only and making regular sheet conductivity measurements (by C. S. Roberts).

3. Measuring the resistance under an emitter stripe, i.e., make a structure as follows



, then measure the resistance from one side of the plated area to the other (suggested by R. H. Mazur).

(cont on next page)

GEM 2/28

Feb 28, cont'd

The previously unexplained observation that this effect allow one to explain is the apparently low emitter ~~efficiency~~ efficiency observed in some n-p-n transistors even when the emitter efficiency calculated on the basis of Tannenbaum & Thomas (modified to take proper account of the mobility variations) yield much higher values.

(This was pointed out in a striking manner on one transistor structure made by Jane Allison that came through all the diffusion runs with a Ni plated getter on back. Even at low currents of 1 μamp it gave $h_{FE} \sim 8$, but it suggesting that lifetime was high, at least at the emitter diode. However, at higher currents a maximum h_{FE} of ~ 10 was observed. This is most easily explained by low emitter efficiency.)

In case the C_B is concentrated under the emitter, the base doping is much higher than calculated, thus giving much poorer efficiency. Just a concentration by a factor of 10 could explain a large part of the loss observed.

The practical importance of such a concentrating effect, of course, lies in the possibility that lower initial surface concentrations can be used to get the same final base doping level. From our empirical evidence this should mean higher values of h_{FE}.

G. E. Moore 2/28/58

2/28/58

Today the first several transistors were mounted on headers and the first unit capped. This was made possible to a large extent by sputtering since the Ag then holds on (at least pretty well) through the photoetching step.

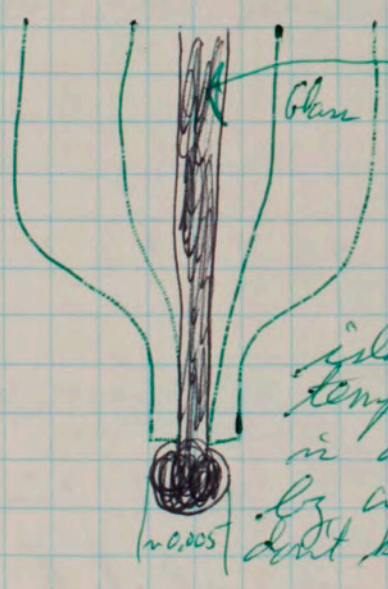
These transistors (n-p-n) came from low h_{FE} material and after mounting had somewhat sloppy collector characteristics. Thorough washing should improve this.

A good feature was the relatively low collector saturation resistance — 15-20Ω, even for the fairly thick wafers employed.

The lead attachment method employed seems to work ok. It is a nice one to mechanize somewhat. Better alloying is needed, but hopefully the new furnace will help here.

The lead attachment used is as follows

A Pyrex glass capillary tube was drawn down to a fine hole and 0.002" dia. wire was threaded through. The wire end was heated in a flame to form a ball, and the ball was pulled up until it hit the bottom of the tube as shown



The gold ball is then pressed to the Au-alloyed islands of the transistor while it is held at a temperature in the 350-400°C range. The ball is deformed ~50% and in the process strikes either by alloying or by thermo-compression bonding — we don't know which at the moment.

A problem is that the bare contact ring is only 0.005" wide, while the gold ball spreads to ~.008" with the usual size ball. Smaller balls or wide spots can help here.

After bonding the glass jig can be slid up the wire, cut, reballed in a flame and used again without re-threading.

G. Moore 2/28/58

March 5, 1958

The first good p-n-p transistor was caused yesterday. Here is some data concerning it:

It was no good when I checked - E-b dead short.

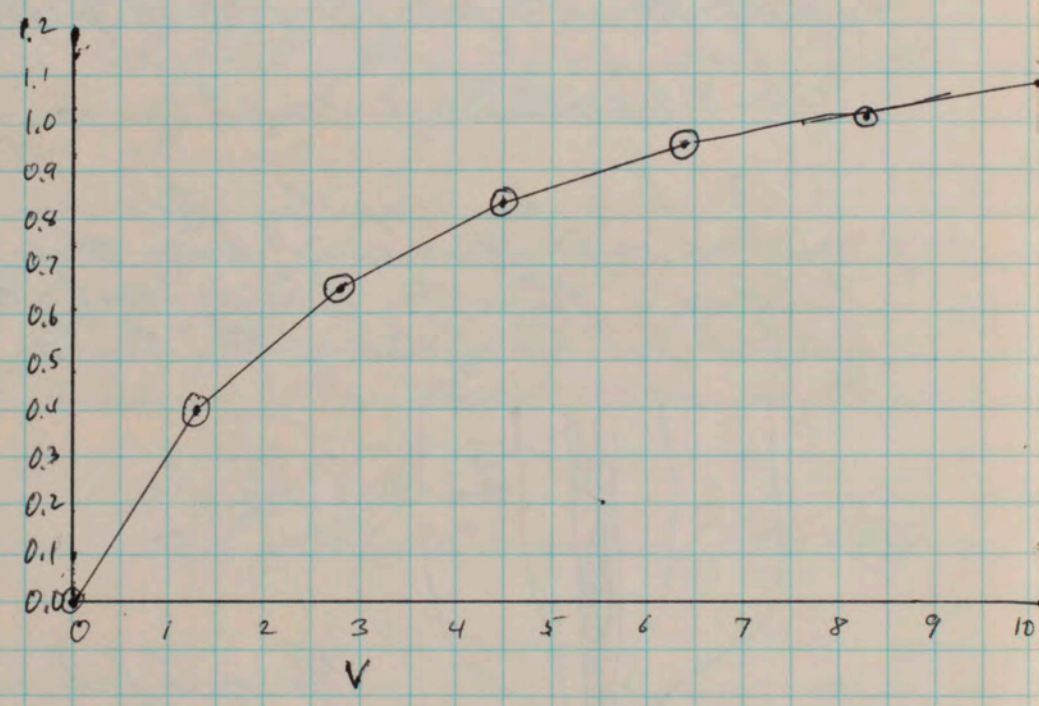
J. R. Moore 3/5

March 5, cont

Data on .002" pure gold wire:

A loop of ~ 8" of wire was welded to a pair of header pins.

Current (amps)	Volts
0.4	1.3
0.65	2.8
0.83	4.5
0.96	6.4
1.02	8.3
1.1	10.4



Pure gold @ 100°C is 2.97×10^{-6}

$\therefore R \simeq \frac{8 \cdot 2.54 \cdot 3 \cdot 10^{-6}}{\pi (25)^2 \cdot 10^{-8}} = 3.1$

We get $\frac{1.3}{0.4} = 3.25$ This is a very good check compared with the accuracy of our measurements.

~~The drop at the 1.0 amp and is $\simeq \frac{10.4 - 6.4}{1.10 - 0.96} \cdot \frac{1.0}{0.14} = 30\Omega$~~ N.G.

~~$\therefore \rho$ is $\sim 30 \times 10^{-6}$~~ @ 1 amp $R = \frac{8.3}{1.02} \simeq 8\Omega$

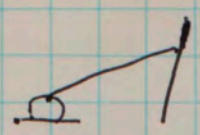
This corresponds to $\rho \sim 8 \times 10^{-6}\ \Omega$-cm

$\therefore T \sim 700°C$. This is no sweat @ 0.5 amp then, I suppose

Some rough calculations can be made regarding the temperature to be expected in the wire center in the transistor.

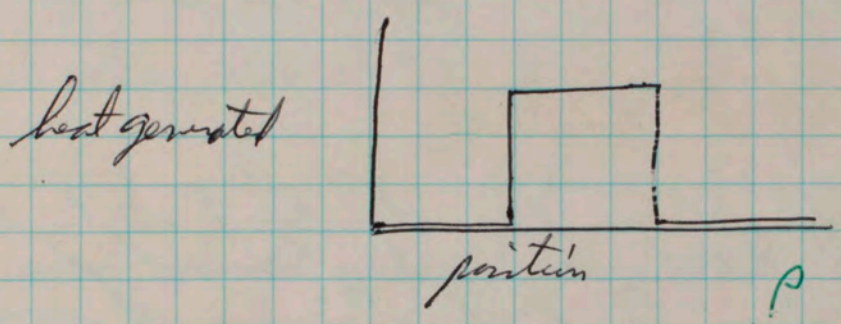
Thermal cond. of Au = 2.8 watts/degree

The lead wire is attached roughly like this:

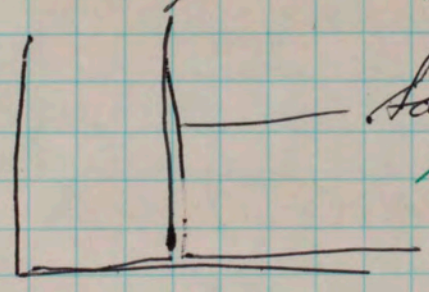


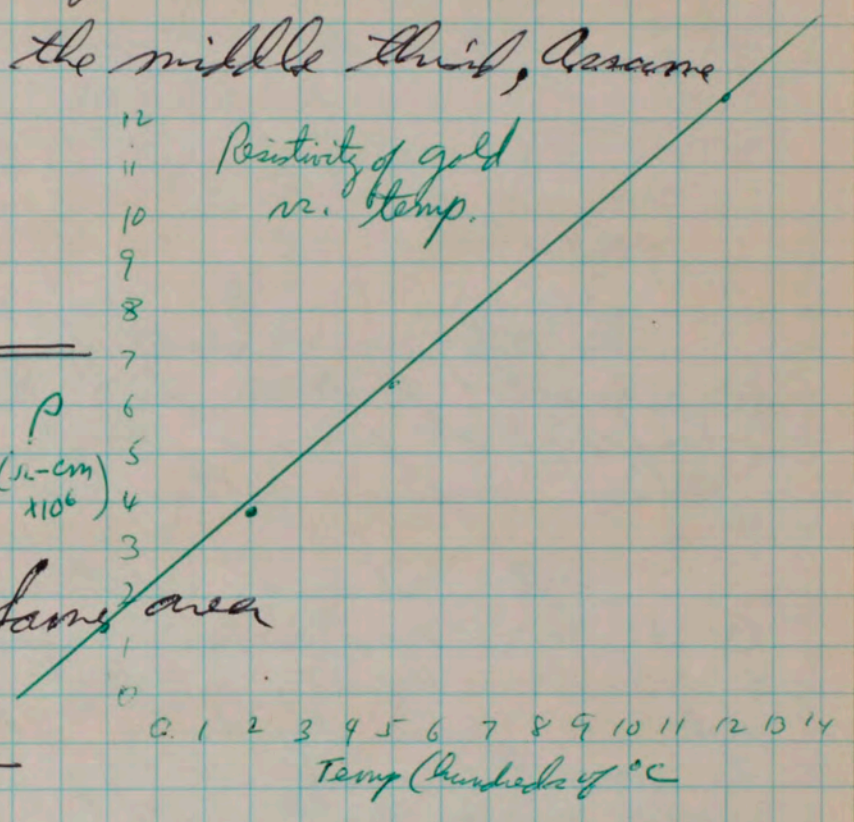
Assume the wire to be ½ cm long

Most of the heat is generated in the middle third, Assume



For calc. purpose change to





$$\text{Heat generated} = I^2 R \quad \left[\text{T.C. of Au, two directions}\right], \approx \left(\tfrac{1}{2}\right)^2 \cdot \frac{6}{8 \cdot 2.54} \cdot \frac{0.5}{3} \approx .012 \text{ watt}$$

$$\text{Thermal conductance} = \frac{2.8 \cdot 2 \cdot (.25)^2 \pi \times 10^{-8}}{\frac{.5}{3}} \approx 2 \times 10^{-4}, \quad \text{Thermal resistance} = \frac{1}{2 \times 10^{-4}} = 5 \times 10^3 \,^\circ\text{C/watt}$$

$$\therefore \text{Temp drop} \sim 5 \times 10^3 \cdot 1.2 \times 10^{-2} = 60^\circ\text{C}$$

$$\text{If } I = 2 \text{ amp}, \quad I^2 R \approx (2)^2 \frac{10}{8 \cdot 2.54} \cdot \frac{0.5}{3} = .3 \text{ watts}$$

$$\therefore \Delta T \sim 1500^\circ\text{C}$$

4/5/58

 March 5, cont.

The alloying of sputtered films is causing problems. Roger today gave me data that indicated that the surface conductivity decreased by a factor of $\sim 10^4$ upon alloying. This is consistent with the appearance of "micro balls" after alloying.

Possible things to eliminate this effect:

1. Cleaner sputtering system
2. Furnace alloying
3. Cleaning of film to remove Ag_2O and Si_2O before alloying (HF).
4. Thinner films
5. Thin sputtered film followed by thicker alloyed film.

Some of these must be tried.

J. G. Moore 3/5/58

3/11/58

The alloying of sputtered films has developed into a considerable problem. L. S. Roberts is working on it from the standpoint of furnace alloying. A brief summary of my feelings regarding the results is as follows:

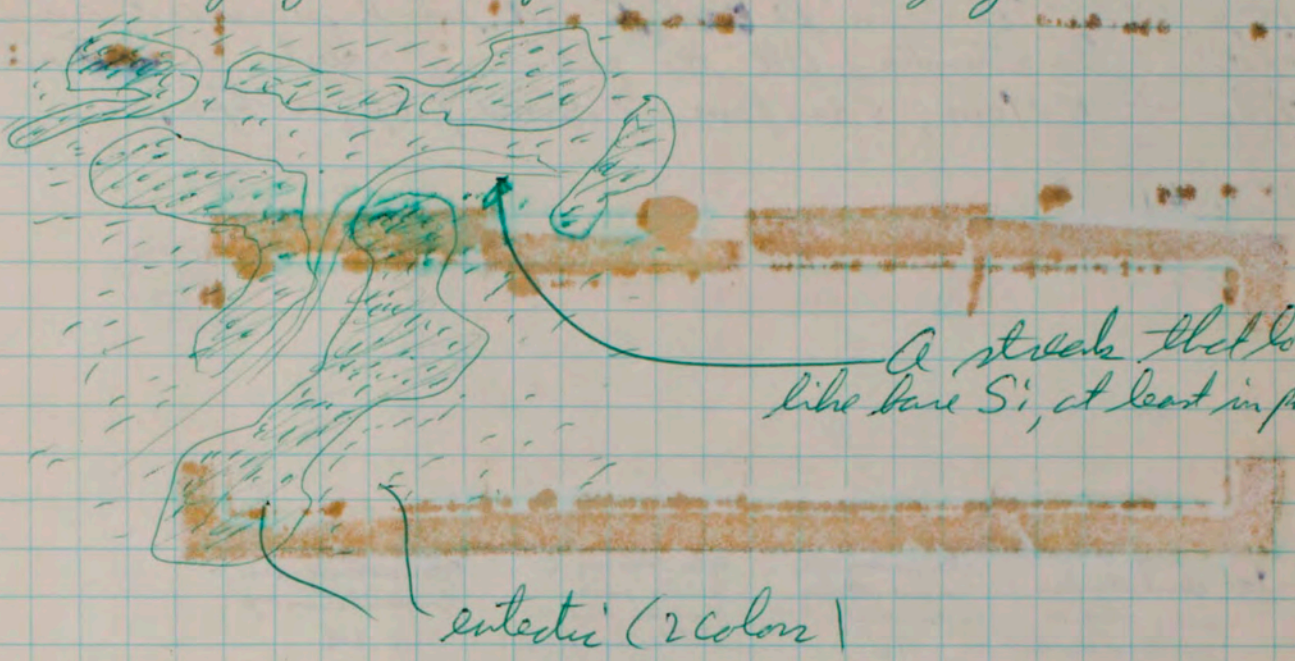
After "ordinary" sputtering, using a 10 min clean cycle @ 30 ma. and pressure near 5μ the silver deposits as a granular deposit. At high magnification (X1000) Holden has detected some dendritic structure. When this is heated to somewhere near the Ag melting point it forms very small balls corresponding roughly to the grain size. Heating to higher temperature pulls it into larger balls, but still of average spacing of ~ 0.1 mm or so. Neither of these conditions looks very different from the original film to the naked eye. Both show very high electrical resistance consistent with the observation of unconnected balls.

One wafer today was accidentally left ~~sputtering~~ clearing for a long time, say ½–1 hr at 45μ pressure and 30 ma. The jar was covered with a black deposit at this time, almost certainly sputtered silicon from the sample. Upon reversal of the current to sputtering position a deposit of silver was eventually obtained that alloyed well ~~between~~ when heated in argon between a pair of strip-heaters. There was a time lag of several minutes before the silver started to deposit

JM 3/11

this time, probably due to the Si that had alloyed on the electrode. After allowing the surface to cool roughly, we follow

(X1000)



This film showed V/I of $\sim \frac{0.1}{10} = 0.01\Omega$.

Evidently the previous surfaces were not adequately cleaned.

The work should proceed along two lines:

1. An attempt to provide better cleaning by
   a) longer time of bombardment
   b) different pressure and, hence, ion energies
   c) different geometry (primarily distance)
   d) faster flushing and better pumping

2. An attempt to produce a mirror-like rather than a granular film
   a) like b, c and d above
   b) try to do on glass for cleaning

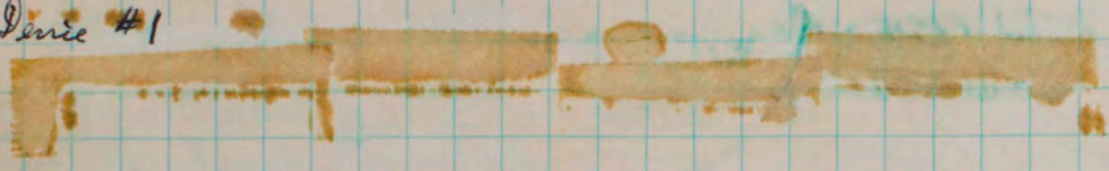
This problem is the big hold-up at the moment!

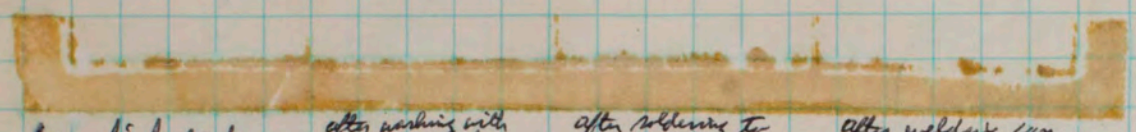
G. E. Moore
3/11/58

14 March 14, 1958

Several fairly good pnp transistor structures exist from the run of sheet #24. There can be used to see which steps are ruining our transistor collector characteristics. All the pictures of collector characteristics below are taken at 5 v/cm, 5 ma/cm, 0.5 ma/step, 12 steps.

Device #1





1a - diod structure using points on Ag alloyed islands

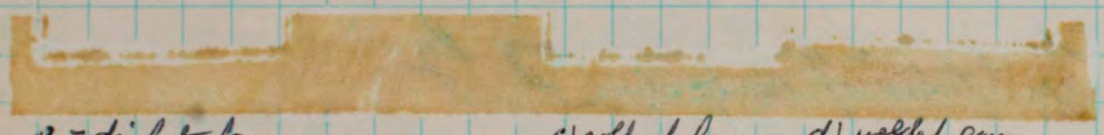
after washing with HF and attaching gold wires
1b

after soldering to header using pure tin and a little rosin flux
1c

after welding can. No special clean-up
1d



#2



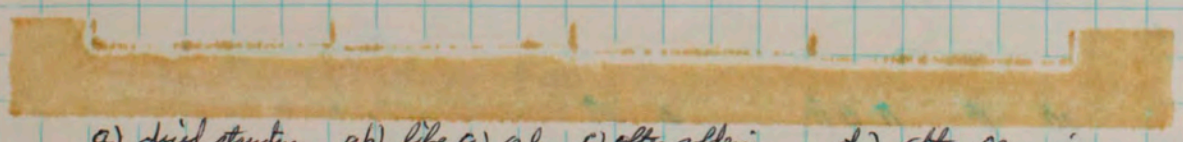
a - diod structure

c) soldered down

d) welded can, no clean up



#3

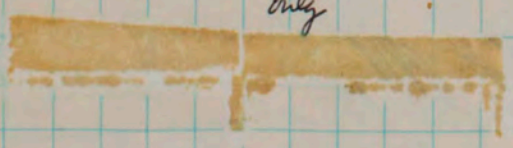


a) diod structure

a,b) like a), only after HF rinse only

c) after soldering down using only H_2 as a flux

d) after canning no clean up



#4



a)

b

a) ~~radiod~~ wafer

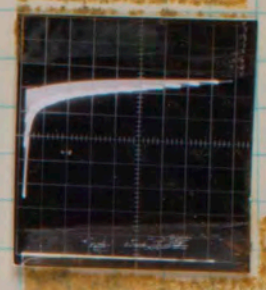
b) with leads attached, no HF rinse

c+d are missing because the base lead pulled off.

JMM 3/14

#5

a) dried wafer | b) after leads, no clean up | c) after soldering to leader, only H_2 as flux | a) after canning, no clean up



0.1 v/cm

5 ma/cm

0.5 ma/step

base voltage or collector current stepped for all five devices shown on pp 14-15. This shows v. good ohmic contact to base region. (Similar curves, see p 17. JJM 3/21/58)

Conclusions and arguments:

compare 1a, 1b - shows deterioration during lead attachment

compare { 3a, 3ab / 4a, 4b ; 5a, 5b } show that the bad step is the HF rinse. No trouble in bonding was found in examples ~~#4 and~~ #5 showing the bad rinse can be eliminated

~~compare 1a, 1b~~
~~2a, 2c~~
~~3a, 3~~

It was shown that H_2 is adequate flux for the pure tin solder.

compare 1c, 1d ; 2c, 2d ; 3c, 3d ; 4c, 4d. These show that the addition of a added can is beneficial. This is an extremely interesting and significant result.

Summary:

1. No HF rinse should be given before bonding (probably never).
2. Pure H_2 can be used for flux to solder dice to leaders with Sn.
3. A good wash and vacuum bake at before canning looks like it might approach being a cure-all.

Note: The partial E-b shorts down by the 10s of µa for the first couple of steps is probably due to incomplete removal of excess silver before alloying.

J. J. Moore
March 14, 1958

Since the last entry considerable progress has been made in cleaning up device characteristics and cleaning devices. In particular it has been found that the parasitic emitter-base shorts prevalent in devices like those whose characteristics are pictured on the preceding pages can be cleaned up by a very light etch in 1:20:: HNO_3:HF followed by a flood of D.I water. Often this raises β to ~30 or so for the first milliamp into the base. There may be some problem with cruddying up collector characteristics during this process. It certainly needs work to get it under control.

A few devices of both n-p-n and pnp polarities have been cleaned and canned. We have finally gotten the high frequency measurements going. A problem seems to be that the light etch in some cases at last, strips the Ag off the base ring while cleaning up the e-b junction. This has resulted in some very high values of $r_{bb'}$. Other parameters are ok.

Today the first attempt at a "production run" was made. Seven dice from 406 were mounted, given a quick 1:20 dip, washed, baked in vacuum, and canned. Yields weren't exceptional, only one had a good e-b diode, 4 looked about like the material before mounting (i.e., e-b short to $I_B = 2 - 1$ ma, $\beta_{max} \approx 10$), one was shorted, one had open base.

Wafer 24 B was in accepted register. Out of the 47 dots 45 looks in register. After dicing 37 remained. (I have no idea what happened to the other ten.) A random sample often of these showed good, very sharp, collector junction and $\beta \approx 10$ with the usual e-b partial shorts. We have some of these mounted and will do the rest. This is a beautiful batch upon which to practice clean-up etching.

A big remaining problem in these e-b partial shorts deal. Yesterday I examined the e-b junction region of some alloyed structures and some before alloying. At X1000 on the metallograph there appear to be small crystallites of silver not removed during the photoresist etch step. These may well be the cause of our problem. I suggested to Parker that either

1. The etch in the $Fe(NO_3)_3$ etch much longer than is necessary to see the Ag disappear, or
2. We try a 1:20 dip after the iron-etch.

Both of these should be done.

Also we should measure e-b diodes before alloying some if they clean up.

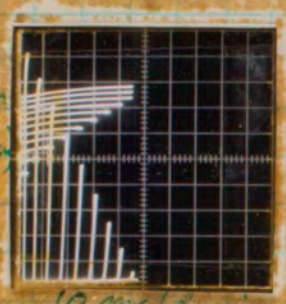
R Moore 3/20/58

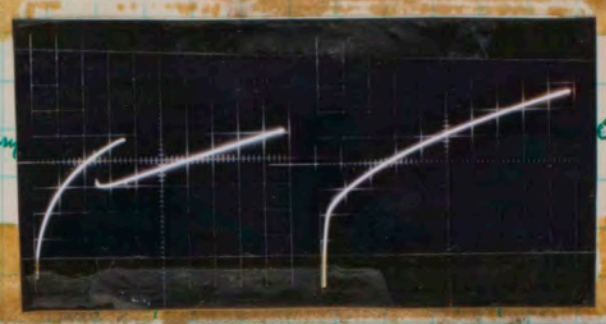
3/21/58 17

During the last couple of days Vic Shmidt has made some rather disconcerting measurements of base spreading resistance (r_b'). I have been trying to pass these off as due to lack of silver on the base ring after the clean-up of the e-b diode in 1:20 as described on p. 16. To wrong a bit later along these lines, I decided to look at the e-b diode characteristics of a transistor before and after clean-up. Because several p-n-p's from run 24b were available today, I chose one of them.

Here is the transistor before clean-up:

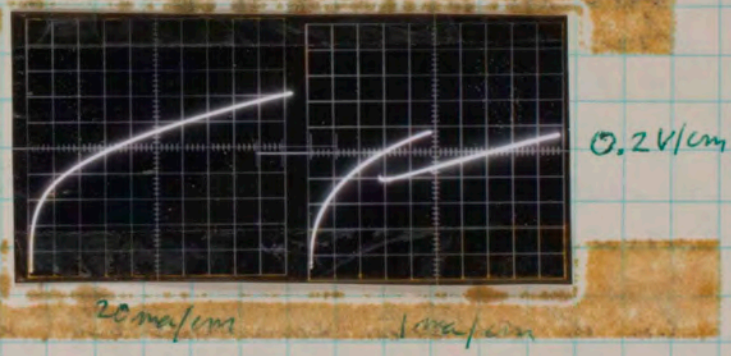
e-b diode, ground board





Here it is after clean up (same scales throughout):





The most significant observation is that there is a "switching" at currents of about ~~50~~ 100 ma for the uncleaned diode and 75 ma for the cleaned one. The only explanation I can think of for this phenomenon are either

1) there is an extra junction and this is transistor avalanche

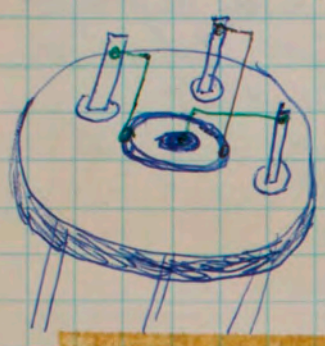
or 2) there are two extra junctions and this is a switching diode action.

In either case, one of the contacts is non-ohmic. By comparing the voltage drop from base to collector with that from e to base at $I_C \sim 150$ ma, ~~the~~ an extra junction must occur, or at least an ~~the~~ non-ohmic contact must occur to the base. ~~(e.g. 3 V from e-c gives 150 ma. this reduces to 10 ma into base. but 10 ma into base $V_{eb} \sim 1.6$ volts. at 150 ma the e-b voltage would be ~~.~~ If it was on the emitter the E-C characteristics should show a switching action instead of nice avalanche characteristics. This must be checked in other p-n-p's and also investigated in n-p-n's.~~

R. Moore 3/21/58

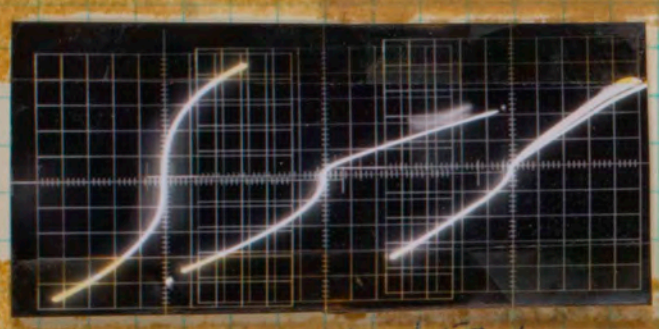
18 3/24/58

A device was made from 24a (pnp) to make some observation regarding the base ring contact. It looked like so:

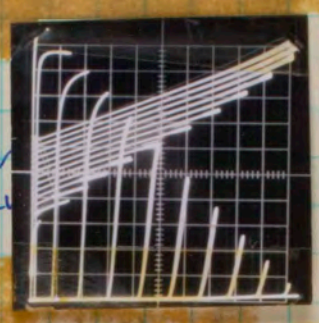


This has two base ring contacts. All contacts were of our usual gold ball type.

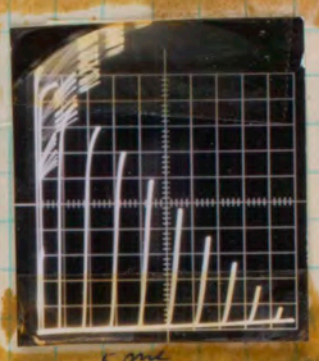
Here are the pictures showing how crappy things are:



5 ma/cm inverted
1V/cm horiz.



5 ma/cm
Δ = 1 ma



5 ma/cm
Δ = 1 ma

50 ma/cm
5 V/cm

5 ma/cm
1 V/cm

1 2 3

Collector lead base; Regular base lead

The above picture show the V-I characteristics between the two base leads. It is obviously non-ohmic, although it improves very slightly after cooking at 7 watts peak power. At this stage such results can mean only either that the Ag ring is non-continuous or else the gold ball is not making an ohmic contact to the Ag-Si eutectic. It is obvious that more work must be done.

The two families of collector curves with superimposed base voltages show the transistor standing with each of the base leads. Obviously the regular base lead was making a much poorer contact.

From picture #2 the final resistance in the best direction corresponds to $R = V/I = \frac{5}{.175} \cong 28\Omega$. This would certainly raise hell with Zi design if there was no higher resistance at lower voltage. For example picture #1 shows a D.C. resistance of $\frac{3}{.01} = 300\Omega$ in the same direction.

J. R. Mars

Some cans were welded for leak testing.

100 Zell splash-ring type with compression seals on setting 2 (black box lacked)
50 Constantan Kovar headers on setting 2 (coded with bare lead dipped)
50 " " " " " 3 (no coding)

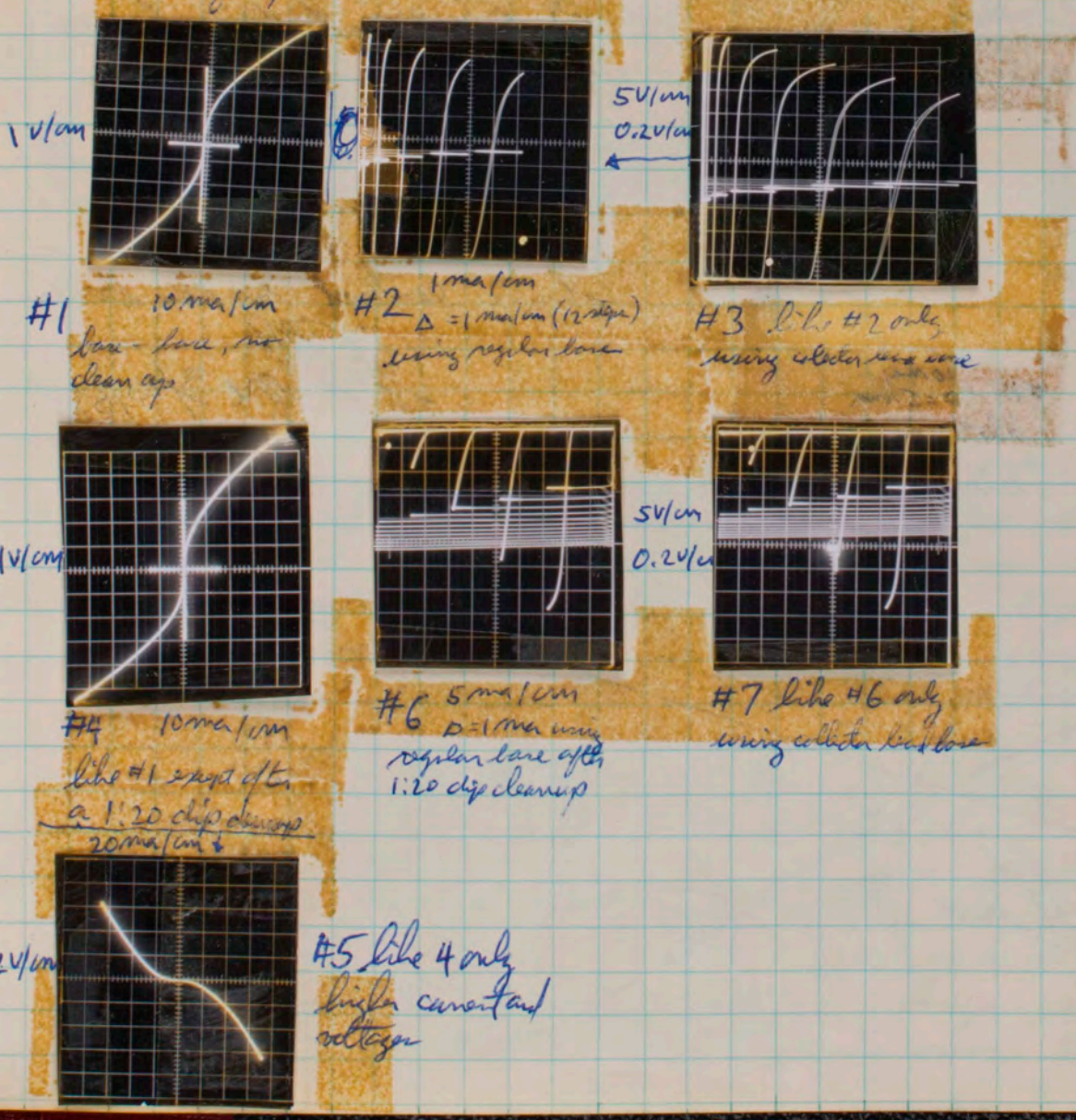
Coincidentally it was determined that my welding rate is a maximum of about 6/min. It took 7 min 50 sec per 50 to weld 50. This looks like a reasonable upper limit for a production worker over a long time. Calculations based on 5/min as the working rate are reasonable.

The cans and headers for the above readings were not cleaned, but were taken from the manufacturers ~~original~~ package with minimum handling, special care being taken not to touch the part of ~~where the~~ weld is made.

J. H. Moore 3/25

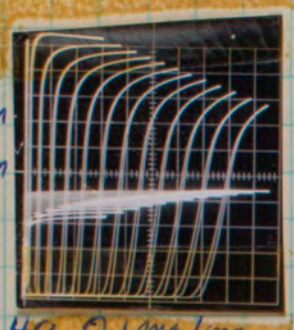
3/25/58, con't

Another device with two base leads like the one described on the previous page was made. This is given the number 24a-11*. Here is a bunch of pictures of it.

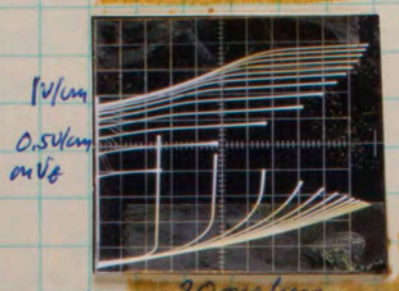


OVER FOR MORE ON THIS.

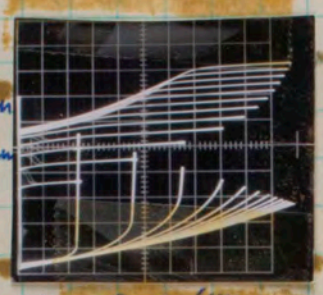
J. H. Moore 3/25/58



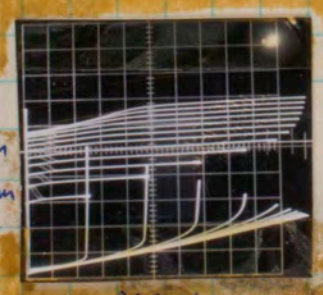
#8 0.1ma/cm
D=0.01ma
12 steps
low current characteristic after canning. Using the regular base lead.



#9 20ma/cm
5ma/step
using base lead only



#10 20ma/cm
D=5ma
like #9 only using the "collector" base lead only



#11 20ma/cm
D=5ma
like 9+10 only using both base leads simultaneously

In #9 @ 150ma I_c, $V_c \cong 1.4$ V
In #10 @ 150ma $V_c \cong 1.4$V
In #10 @ 157ma $V_c \cong 1.2$V

In #9 V_{f_1} @ I_c=150ma, I_f=60ma, $V_{f_1} = 4.3$V
In #10 @ I_c=150, I_f=60, $V_{f_{1,2}} = 4.0$V
In #11 @ I_c=150, I_f=60, $V_{f_{1,2}} = 3.4$V

~~@ 3.4V, Ic~~

Here is a summary of the observation and conclusions I make from these photographs of 24a-11 #:

1. From #1, #4, #5 the base contacts are not connected by an ohmic resistor.

2. From change in α-crowding in #9, 10, 11 the base ring has a high resistance so that it does not ~~have~~ become an equipotential surface.

3. The clean-up is pretty good because after cleaning the β_{12}, etc are identical, #9, 10; #6, 7

4. If we get a good base ring contact V_f, R_{CS}, V_{fs} will all improve as well α-crowding :- #9, 10, 11.

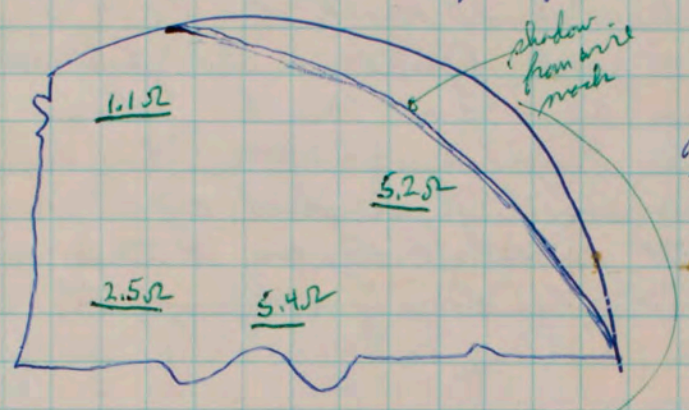
5. One must conclude that the silver ring is non-existent and that it makes a non-ohmic contact to the base.

G. Moore 3/25/58

G. Moore 3/25/58

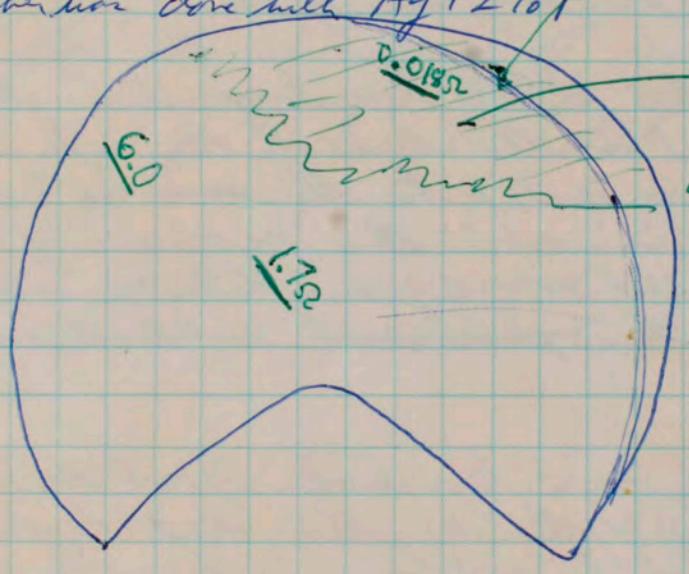
In order to study the ohmic contact problem with pnp transistors some more, I had Roger Mavey evaporate metal onto Sb^+ - p type diodes made in the fashion of the pnp base diffusion.

One wafer was evaporated with pure Ag and alloyed immediately between strip heaters. Here is a map of its surface:



Whole surface balled with some non-balled film. Ball size increasing from right to left in the picture.

The other was done with Ag + 2% P



Region of the prettiest alloying to date by far. Still bright, mirror like on large scale, fine dendritic eutectic on a small scale.

Region of isolated large balls but with a substantial looking film remaining between.

3/25/58 The alloying is still a problem for both polarities. To try to improve wetting in a system perhaps suitable for npn's, a double evaporation was performed. First a light layer of Al was put down followed by Ag. These were then alloyed and the wetting obtained was excellent. Probably ~ 10% of the total metal was Al.

The sheet conductivity was $V/I \sim 0.15$ or $\sim 0.6\,\Omega/\square$

Gold bonding to the metal layer worked very well - the wire broke upon attempting to remove 5 leads out of 5.

Making stripes ~ 3mm long and 1/2 mm wide with a lead on each end, they were ohmic, ~ 3Ω. Upon removal of the metal by CP-8 in the center of the stripe, the resistance became ~ 45Ω, still nice and ohmic. This seems this method makes ohmic contacts to 1Ω-cm, n/ p-type Si.

J. LeMone 3/26

22 4/2/58

During the last few days we have made a few attempts to use the simultaneous and/or successive evaporation of Al and Ag to make contacts. The first batch of n-p-n transistor structures given this "simultaneous evaporation (actually the Al goes down first because of more rapid warm-up of the W wire filament) was alloyed at the usual ~1000°C in a furnace in argon. All these "transistors" were dead e-b shorts. Upon this I examined the phase diagram available for combinations of Ag, Si and Al. An Al-Ag eutectic should melt at ~550°. Pure Al melts some 100° higher. Certainly a good liquid should form at a much lower temperature. Accordingly run 55A was made wherein the alloying was done at a much lower temperature, ~730°C, to limit penetration. This run yielded no shorting, in fact after mesaing they were the cleanest transistors yet produced by us at this stage. This was probably due to no re-evaporation during alloying, the e-b diodes were pretty clean.

This wafer was diced to ~ 30 devices (all that were in index) and some of these have been mounted. They look good.

A problem that appeared is that at the low temperature for alloying no liquid phase was formed on the back of the wafer. This prevented our getting a good adherent contact to the ~~one~~ collector on the first few devices. Later ones circumvented this problem by lapping the back-side of the wafer on glass with 1950 SiC and dedodden nickel plating the lapped surface. These were then ~~plated with~~ soldered with Dixie 229 or a flux.

In summary, the Al+Ag contact on top looks good for n-p-n. Perhaps it can be used on back on top of the Ni getter, but a fresh Ni plate is within reason here too. The contact seemed nicely ohmic, at least qualitatively.

No similar system exists for p-n-p's - Ag+Zn or P alloys about as well as pure Ag. We are still trying such things as "aquadag" to prevent spreading.

R. Moore — 4/2/58

Since the last entry several of the n-p-n transistors from run 55A have been mounted in the usual manner. These yielded pretty good characteristics. In particular the base input voltage looked excellent. People doing the mounting found that the Ni plate on the lapped back surface of the wafers soldered down nicely using Dixie 229 flux. This flux raises hell with the collector junction, but has the advantage that it is cleaned off by a thorough D.I. water rinse restoring the collector junction characteristics.

The principal problem associated with these devices is that either the emitter or ~~collector~~ base lead often comes off. Before final seal ~60% were lost because of this. Upon examination it looks like the metal (Ag mostly) is pulling off the silicon. I do not feel this is a problem that will be solved, but we must watch for it. As before the e-b junction clean-up etch looks like it loosens the contacts. As soon as material is flowing regularly through the line, we must try to give the e-b clean-up etch before measuring. This has the advantages of 1) not hurting any existing contacts and 2) not ending up the collector junction. The main arguments against it are 1) a final clean-up etch is best at a time as near sealing as possible and 2) it is not possible to test immediately after etching to see if the clean-up was adequate. Another ~~cost~~ advantage is that this method allows one to handle an entire wafer at a time. On second thought, it is still possible to check immediately the e-b ~~contact~~ junction.

On 4/4/58 I had Roger make a run aimed at a similar method of making ohmic contacts to p+'s. This consists of a dual evaporation of Al and Ag+2%P. The idea is that while the Al acts as a flux for wetting, the segregation coefficients are probably such that the phosphorus should predominate in the ie growth region. Due to masking problems the Photoresist step didn't work out so the entire wafer containing pnp structures was alloyed. Diodes were made in the region between emitter dots and by block-wax masking. There were then diamond scribed with points on the same traces. They were very pretty - hard in the reverse direction and comparable with the n-p-n transistor base contact in the forward direction. This looks extremely promising and must be pushed for a few days next week.

R. L. Moore

4/5/58

The following is some evaluation of pnp material. It can be completely neglected

90A , 1 wafer

I_{C_0} @ 40V	I_b @ I_C = 10 ma, just above saturation	V_b @ I_C = 10	V_b @ I_C = 0, I_b = 0
		~~2.0~~	~~1.9~~
< 10 μamp	4 1/2	2.0 V	1.9
< 10 μamp	1.0	0.05	0.98
< 10 μamp	6.0	1.6	1.5
"	~250	high	high
"	~1200	V "	" "
	~1200		
	108		
	5.7	1.7	1.6
	0.85	1.7	1.1
	0.9	0.9	0.8
	2.5	~~0.9~~ ??	~~0.8~~
	3.2	1.63	1.58
	1.8	1.54	1.48
	7.0	1.9	1.85

— Shift wafer

Surface	1.2		
no I_b	~~0.8~~		
ε-c short	—		
surface 0.2 mm	0.8	1.4	1.3
.05	1.0	1.1	1.0
< 10 μamp	0.9	0.92	0.85
~~0.2~~ 5 μamp	0.8	0.82	0.78
< < 5 μamps	0.75	1.2	1.1
0.01 ma (excellent to 300)	0.35	5.9	0.8
ε-c partial short	0.7		
ε-c bad short (near hole)			
ε-c " " " "			
ε-c " " " "			
ε-c " " —			
good to ~200 ~~1 ma~~ ε-c ~~partial short~~	0.4		
10 ma ε-c partial short			
6 " ε-c " "			
ε-c short (near hole)			
" " " "			

q-c chert, v. bed
" " " "
partid shst (2mm) 0.4
q-c shale

out 5/2/58

May 2, 1958

Several batches of transistors and three terminal pnpn switches have been mounted. In summary here is roughly the picture:

Pure Al works very well on n-p-n's in all respects. Alloy at ~ 600°.

Al+P is not so good on pnp's

Pure Al is ok on pnp's.

Our main troubles for production are

1. Trouble soldering down the collector. The present nickel plate is not working well. Many are popping off. Others are badly non-ohmic or are of very high resistance.

2. Surfaces are not completely stable. Many devices show surface breakdown which remain a problem.

3. Our final header is not in yet — for that matter final choice has not yet been made.

R Moore — 5/2/58

May 23, 1958

Here is the analysis of our yields from the last few batches of transistors to come off the line. The categories are as follows

	1	2	3	0
BV_{CEO}	≥41	≥21, <41	-	<21
h_{FE} (150 ma, 15 ma)	≥41	≥21, <41	≥11, <21	<11
$V_{BE\,on}$ (150 ma, 15 ma)	≤1.15	~~≤1.45~~, ≥1.15	≤1.65, >1.45	>1.65
C_{OB}, 10 ma, 10 volts	≤29	>29, ≤39		>39

batch #	21	22	23	24	25	26	27	28	29	30	Σ
1111					2	8	4		1		15
1112							1	1			2
1121					2	4	1				7
1122					2	1	10				13
1131						1	5		1		7
1132						1	3				4
1211				2							2
1212											0
1221			1	1							2
1222			1						1		2
1231		1		1				1			3
1232	3							3			6
1311											0
1312											0
1321		1		4							5
1322	1			1							2
1331	1	1		1							3
1332	1										1
2111						5					5
2112											0
2121					3	5	2	1			11
2122					2	1					3
2131							1				1
2132			1				1				2
2211				4							4
2212											0
2221				3							3
2222		1	1								2
2231	1	1	1	4							7
2232	2	1	3					1			7
2311				2							2
2312											0
2321		3		4							7
2322			1								1
2331		4	1								5
2332		1		1							2
											136
open		1			1	1	1				4
b	1				1	1		2			5
2				1							1
0----	1	4	1	6	4	6	4	1	2		29
-0--	1										1
--0-	3	2			1						6
---0	1					2					3

Total number on sheet = 185

Repeats = 49

Clamfoil = 136

% yield = $\frac{136}{185} \times 100 \simeq 73.5\%$

IBM specs as written include

1111
1121
1131
1211
1221
1231

or 36 units

$= 19.5\%$

R. E. Moore
7/23/58

May 24, 1958

Analysis of runs, cont.

It is interesting to see what the distribution is of each parameter.

1 - - -	74	0.544
2 - - -	62	0.456
- 1 - -	70	0.514
- 2 - -	38	0.279
- 3 - -	28	0.206
- - 1 -	30	0.221
- - 2 -	58	0.426
- - 3 -	48	0.353
- - - 1	89	0.655
- - - 1	47	0.345

May 29, 1958

An attempt to see if R_{CS} correlates with h_{FE}. It should if the lifetimes in base and collector vary in the same manner. In general thought the device evaluation data are not sufficient to make this comparison, since the constant circuit bias of 10 gives varying amounts of over-drive, not corresponding to the same amount of degree of saturation.

July 2, 1958

One of the biggest problems at the moment is on line is that surface contamination is knocking yields on both h_{FE} and BV_{CEO}. In an attempt to try to clear this up by cleaning the final sub-assemblies with a light etch, the following series of results were obtained:

Ten structures from Batch # npn-194 were taken. These were selected as existing examples and also because the original "typical H_{FE}" was ~35.

As taken from rack Tester I		After 1 sec etch in flowing 20:1:3 HNO_3:HF etch and a good DI rinse*:	
I BV_{CEO}	I_b for 15ma	II. BV_{CEO}	I_b
30	13.5	2.7	12.5
3	13.2	6.1	12.0
7	15.5	4.2	14.0
0	14.0	5.2	13.5
2	11.5	3.0	12.0
44	16.0	2.6	12.0
2	11.0	4.5	12.0
0	7	-1	5.4
36	13.0	4.5	10.0
4	15	2.6	15.0

J. G. Gilmore 7/2/58

* 10 min cold DI, 30 sec boiling DI, 1 min cold DI (cold after 20 sec rinse after etch)

This looked like the structures were not dry, hence they were baked @ 200°C ±10°C in air for 30 min and remeasured after cooling a short while.

BV_{CEO}	I_b
38	12.0
59	8.8
39	9.7
58	9.5
59	7.6
43	5.7
60	8.0
-1	2.25
41	6.5
38	9.8

While this is an obvious improvement, the h_{FE}'s are still considerably below the 35 called as typical for this material. Hence they were given an additional clean-up — 2 seconds additional CP 20:1 etch, the same DI water rinse, and dried for 30 min at 200°C ±10°C. They were remeasured as

BV_{CEO}	I_b
49	7.6
56	7.5
60	9.4
67	9.0
59	7.4
31	8.3
60	7.0
0.5	2.45
41	6.2
42	9.0

This was still low on h_{FE}, so an additional etch of 2 sec in 1:20 :: HNO_3:HF was tried. This etch has been previously used to increase h_{FE}. After DI rinse as before and drying for 30 min they were remeasured.

7/2

7/2/58, cont from p30

The results were:

BV_{CEO}	I_B
58	9.6
65	9.7
79	11.5
60	12.0
73	9.4
66	11.5
73	9.4
62	14.2
44	12.6
505	8.1

Here 9 of the 10 collectors have been cleared to >40 volts, a very significant improvement over the original. Unfortunately the hFE has dropped. To see what might help further, the first listed device was selected and subjected to 10:1 etch for 2 sec and observed on the curve tracer. hFE dropped. A second etch of 20:1 was tried. hFE dropped further. Evidently enough material has been removed by this time to appreciably affect the geometry of the device, either by making the emitter thinner to lower α, or else by some other means, perhaps by making a groove about at the b-c junction to expose more silicon for surface recombination.

7/2/58

P.S. From this study it looks advisable to try a clean-up etch in the line. For this, we are trying ~50 units with a 2 sec etch in 20:1 ~~is an attempt~~ and comparing with ~50 units unetched.

7/2/58

July 5, 1958. A while back some data was taken to determine how the h_{FE} as measured at various points varies with operating point. The main reason for this was to see if it could be considered possible to measure h_{FE} at one point, say 150ma and 10 volts, and guarentee it at another point, say 100 ma and 2 volts, where I BM wants measurements.

All transistors were from box 1111

Transistor #		I_b 20 ma, 10 v		I_b 100 ma, 2 v		I_b 150 ma, 10 v (Pulsed)	
			Ratio		Ratio		
29	136A-17	0.62	0.178	3.5	0.70	5.0	
31	136B-29	0.51	0.170	3.0	0.73	4.1	
32	136C-16	0.47	0.171	2.75	0.70	3.9	
40	144B-25	0.53	0.156	3.4	0.76	4.5	
31	136B-16	0.45	0.167	2.7	0.73	3.7	
40	144B-24	0.54	0.182	3.25	0.71	4.6	
25	125-1-10	0.29	0.171	1.7	0.74	2.3	
31	136B-28	0.46	0.170	2.4	0.73	3.7	
40	144B-18	0.61	0.174	3.4	0.76	4.5	

B. Moore 7/5/58

Sept 15, 1958

IBM Transistor failures

IBM sent back 5 transistor (2N697's) from the order shipped — 8/1/58. There were given an autopsy

#		
214-30	E-C short, open b	— bare lead burned open in center
F120-24	E+b open	— both leads burned open in center
211-140E	E-C short, open bare	— bare lead burned open in center
1748-8	E-C short, open bare	— " " " " " "
225-13E	E-C short, open bare	— " " " " " "

Conclusion:

These devices were mistreated. Over 2 amps was put through the base of each and the emitter of at least one.

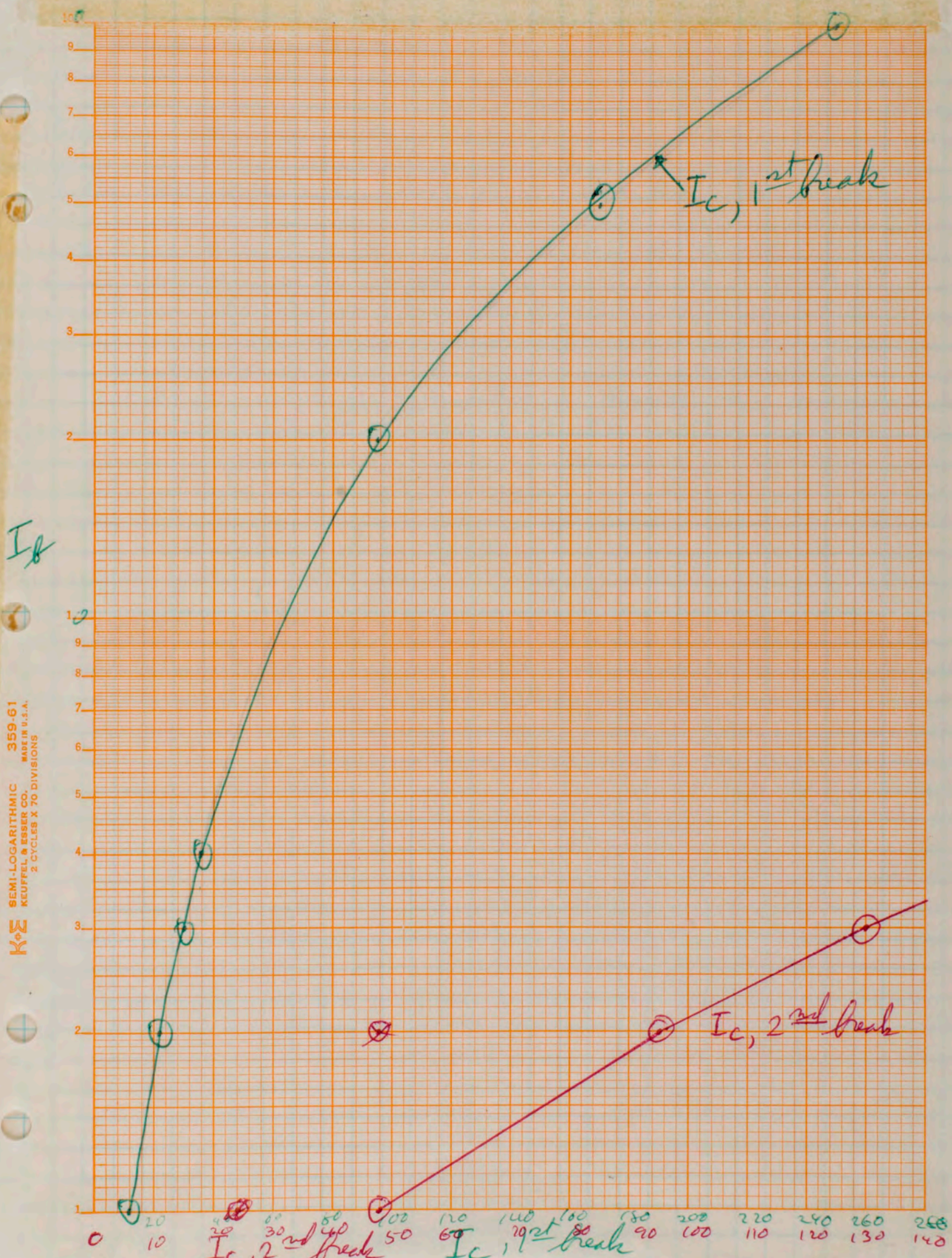
R. More 9/15/58

34 Oct 15, 1958 Data on high resistivity Transistor:

This is concerned with the double-break in the saturation curve

I_b	1st break		2nd break	
	I_c (max)	V_c	I_c	V_c
1	12	0.2	48	2.3
2	22	0.22	95	5.4
3	30	0.28	130	7.0
4	35	0.25		
20	95	0.35		
50	170	0.45		
100	250	0.60		

I_b =	1	2	3	
$\frac{I_{c_1}}{I_{c_2}}$ =	4.0	4.3	4.3	(a constant for this device to within experimental error.)


I_c, 1st break
I_b
I_c, 2nd break
I_c, 1st break
I_c, 2nd break
SEMI-LOGARITHMIC 359-61
KEUFFEL & ESSER CO. MADE IN U.S.A.
2 CYCLES X 70 DIVISIONS

 D Jan 4, ~~1958~~ 1959 gm

Analysis of experiment of baking transistor at 300°C rather than 200°C. This consisted of splitting two lots and baking under 3 sets of conditions:

A: ~200°C for ~3 days
B: ~300°C for 16 hours
C: ~300°C for ~2½ days

Before baking each batch was separated into three sub-batches

A: BV_{CEO} (10 μamp) ≥ 42 v
B ≥ 22, < 42
C < 22

200° bake, 72 hrs

	Subgroup A					Subgroup B					Subgroup C					Σ Σ
	1	2	3	4	Σ	1	2	3	4	Σ	1	2	3	4	Σ	
A's	23	32	28	25	108	1	1	0	0	2	2	1	0	0	3	113
B's incl.	4	2	6	6	18	7	2	8	4	21	0	2	0	0	2	41
BV_{CEO}	1	2			3	2	1	2		5	9	7	3	11	30	38
BV_{BEO}	3		1	4	8											8
Open	1	3	2	2	8											8
I_b	2		6		8	1				1						9
V_{CE}																
V_{BE}																
LV_{CES}																
I_{CO}	2	1	5	4	12	1			1	2						14
Bath tub	~~34~~ 39		43	37	153	1~~7~~ 4		10	4	29	11	10	3	1~~1~~	35	217

Grand total = 217

Jan 4, 1959, cont

300°C bake, 16 hrs

	Subgroup A 1	2	3	4	Σ	Subgroup B 1	2	3	4	Σ	Subgroup C 1	2	3	4	Σ	ΣΣ
A	33	13	31	14	91	0	1	0	0	1	0	0	1	0	1	93
B	0	16	5	15	36	4	7	4	3	18	1	2	0	1	4	58
BV_{CEO}	1	1	1	1	4	1	2	1	0	4	2	~~9~~	3	5	19	27
BV_{BEO}	1	3	4	2	10			~~3~~			2	~~3~~	1	3		13
Open	3	2	3	2	10											10
I_f				7	7											7
V_{CE}												~~3~~	1	1		1
V_{BE}																
LV_{CES}			~~1~~	1	1											1
I_{CO}	0	15	5	15	35		(1)	1	0	2		~~2~~	(1)	3		40
Σ	38	35	44	42	159	5	10	~~5~~	3	23	5	~~11~~	4	8	28	210

ΣΣ 210

300°C bake, 60 hrs

	Subgroup A 1	2	3	4	Σ	B 1	2	3	4	Σ	C 1	2	3	4	Σ	
A'2	28	21	29	27	105	0	1	1	0	2	0	0	0	0	0	107
B'2	10	2	5	3	20	2	2	6	5	15	0	1	2	6	9	46
BV_{CEO}			1	0	1			3		3	9	7	3	5	24	28
BV_{BEO}		2	1	5	8	3	~~4~~		1	4						12
Open		2	2	2	6											6
I_f		~~4~~			4	4				4						8
V_{CE}																
V_{BE}			1		1											1
LV_{CES}	1				1											1
I_{CO}	8	2	4	3	17	2		1	0	3		1	0	0	1	21
Σ	39	31	39	37	146	9	6	7	6	28	9	8	5	11	33	207

ΣΣ 207

One way to ~~see~~ look at the data on the other page is to ask how many passed $BV_{CEO} \geq 42$ v before and after baking. After this includes all rejects and I_{CO}, except 1/2 since only 1/2 are tested beyond BV_{CEO}. Open should not count.

∴

200° bake

before 153 , after 113 + 14 + 8 + 9 = 144 ∴ Δ = −9

300°, 16 hr

before 159 , after 93 + 40 + 13 + 7 + 1 + 1 = 155 ∴ Δ = −4

300°, 60 hr

before 146 , after 107 + 12 + 8 + 1 + 1 + 21 = 150 ∴ Δ = +4

If this analysis is fair, a questionable assumption, it says that the long, 300 °C bake makes most good BV_{CEO}'s.

In any case the experiment suggests very strongly that a three day, 300 °C, bake does not influence the yield markedly.

D. E. Moore
1/4/59

July 3, 1959 39

Tapping test:

Start with units that were de-gilded inside except for a dot of Ag to solder to — stainless steel caps. A — 1 unbuttable Ni plated

FT-4000

323PBOS

Unit #	Collect joint	after 10 taps	after 10 pounds		Analysis
1	v. hard	ok	ok		ok
(2)	.05 ma @ 110v	went to 25v	returned, then bad again		—
(3)	noisy surface (then hard)	ok	ok		ok
4	v. hard (crypt)	ok	ok		ok
5	50v breakdown	—	to 30v		—
6	hard	ok	ok		ok
7	hard (crypt)	ok	ok		ok
8	hard	got sick — 40v	stayed sick		sick
9	hard	ok	ok		ok
10	"	ok	ok		ok
11	"	ok	ok		ok
12	(shorted)				—
13	40v, 0.02 ma	same	same		—
14	med. hard. (crypt)	ok	ok		ok
15	60v, 0.01 ma	same	same		—
16	hard (95v)	same	to 30v	+ 2 taps → same as originally — stayed	sick
(17)	25v, 0.05 ma noisy	same	same		—

∴ 2/11 got sick

Regular units from about same batch (same vacuum bake) (lot 183-71)

ok originally				bad originally				ok originally, went				bad originally went
				tap		pound		tap		pound		tap pound
ok after tap	bad after tap	ok after pound	bad after pound	same	change	same	change	S	C	S	C	S C S C
✓	✓			✓	✓			✓		✓		
✓		✓		✓		✓		✓		✓		7/24 went sick of good ones
✓		✓		✓		✓		✓		✓		
✓			✓		✓			✓				
✓		✓		✓			✓	✓				3/11 of bad originally
	✓			✓		✓		✓		✓		
✓		✓		✓		✓		✓		✓		
✓		✓		✓		✓		✓		✓		
✓		✓		✓		✓		✓		✓		
✓		✓		✓		✓		✓		✓		
	✓							✓				
								✓		✓		

40 7/3/59

More pounding of special units (263 P01A)

#	Originally ok top	Originally ok bot	Originally bad top	Originally bad bot
	S C	S C	S C	S C
1	✓	✓		
2	✓			
3	✓			
4	✓		→	
5	too bad			
6	"	"		
7	✓	✓	✓	
8	✓		✓	
9	✓		→	opened
10	aborted			
11	✓		→	
12				
13	— Stopped - there was no			
14	reason to continue			
15				
16				
17				
18				
19				
20				
21				
22				
23				
24				
25				
26				
27				
28				
29				
30				

7/7/59

O'Keefe specials — emitter bad only 189A.

	Originally ok'd same	Originally ok'd tap changed	Originally bad same	Originally bad changed
1		✓		✓
2	✓			✓
3		✓		
4		✓		
5	✓			
6		✓		
7	✓			

(10 decks if the bare board is the culprit.)

Soldered cans (no weld)

Originally ok'd same	Originally ok'd tap changed	Originally bad same	Originally bad changed
	✓		✓
✓			
	✓		
✓			

Waped cans

Originally ok same	Originally ok change	Originally bad same	Originally bad change
✓			??
✓			
✓		✓	
?			
	✓		
✓			
✓			
✓			
!			

 tapping, cont 7/7/59

4-200 special (no plate at all) — An plate removed from cover and header after tap

	good originally		bad originally	
	same	change	same	change
1	✓			✓
2		✓		
3	✓			
4		V.V. Sick		
5	?			
6		✓ and released		
7		✓		
8		✓		
9	✓			
10		✓		

Unharvested units 189-24

✓ ⟷ went bad after ~100 taps

✓

✓ ✓

✓ ✓

✓ ✓

✓

—Al reward 7/8/59 6-175-31 (Au station)
in NaOH

	same	good change
1		
2	✓	
3	✓	
4	✓	
5	✓	
6	✓	
7		✓
8		✓
9		✓
10		✓
11	✓	
12	✓	
13		✓
14	✓	
15		✓

7/8/59

2 Units opened that went bad from above group. They each showed a flash of crud (it looked like yellow metal) on the top edge of the ~~coin~~ — They were still bad after opening, but the low breakdown ~~was~~ was cured in each case by carefully removing the single particle with a pin under a microscope.

This was repeated with 4 out of 5 of the ones ruined that had no gold plate (p. 39-40). On them the flash looked like a silver metal — ~~probably~~ possibly Al. It looked like Al had chipped on most of them.

One unit had two pieces of translucent crud (dust??). Removal of this (this unit was originally bad) fixed the unit.

44 7/9/59

More Lapping

Good 4205'2 (unselected)

Lap

same ✓ change

1-14 ✓ (all good)

Same, only oxide removed.

1. ✓ (others all rejt)

. Units that are undercut Al (Linde B on die to start)

good to start

1 ✓

2. ✓

3 ✓

4 ———

Same, but no undercut

bad

same ✓ change ✓

✓

✓

4-230 Al and Au (except det) removed

6/7 do through ones mechanical lap.

There is some reason to believe that flaking of the alloyed Al is a contributing cause to the tapping problem. This evidence is

a) some of the specks look like a silvery metal – especially in units where the gold plate was removed

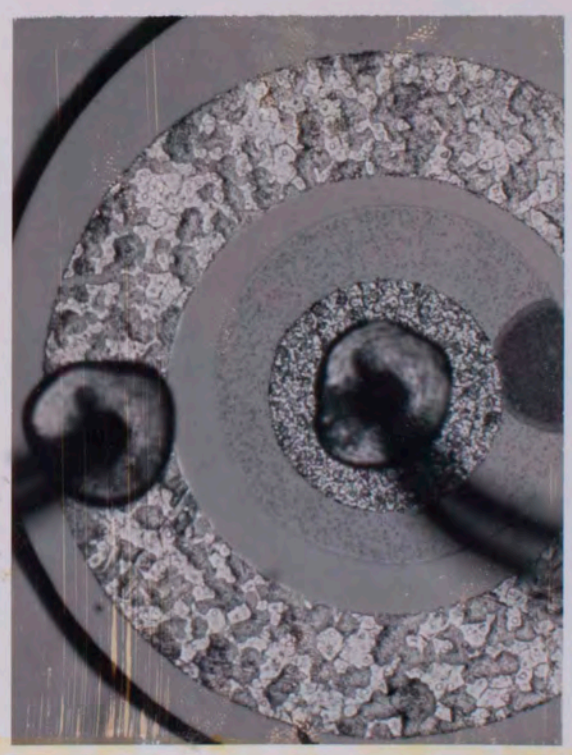
b) some bare lines were observed after tapping to have large voids in them of a type not previously seen.

In order to see if some Al can be shaken off, a series of nine units ready for take-out were photographed, subjected to ~30 sec ultrasonic vibration, and photographed again. Here are the pictures:

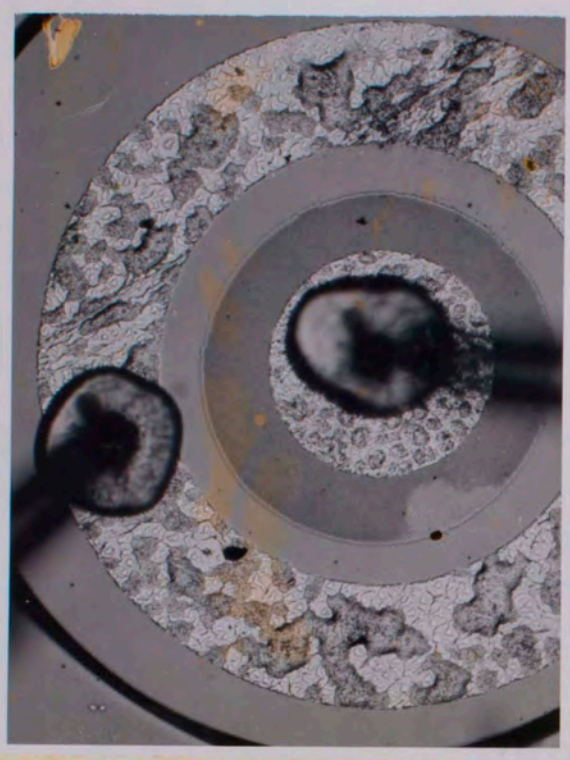
1
Before



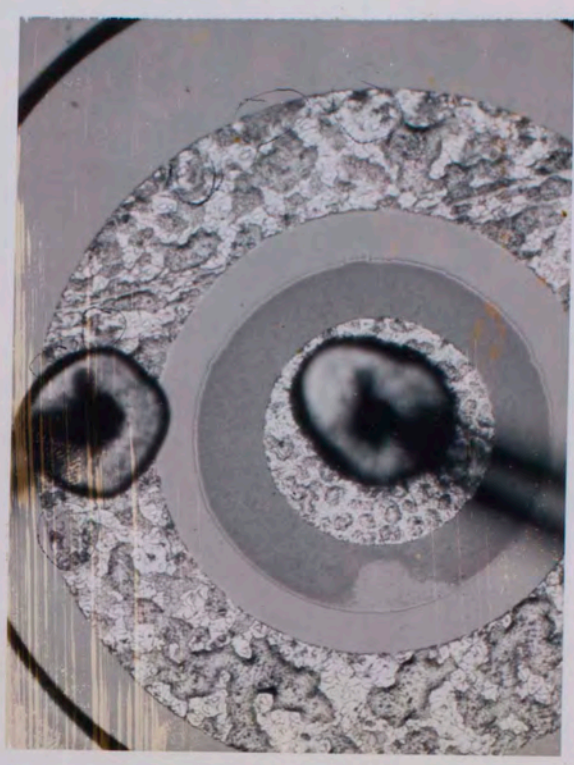
1
After



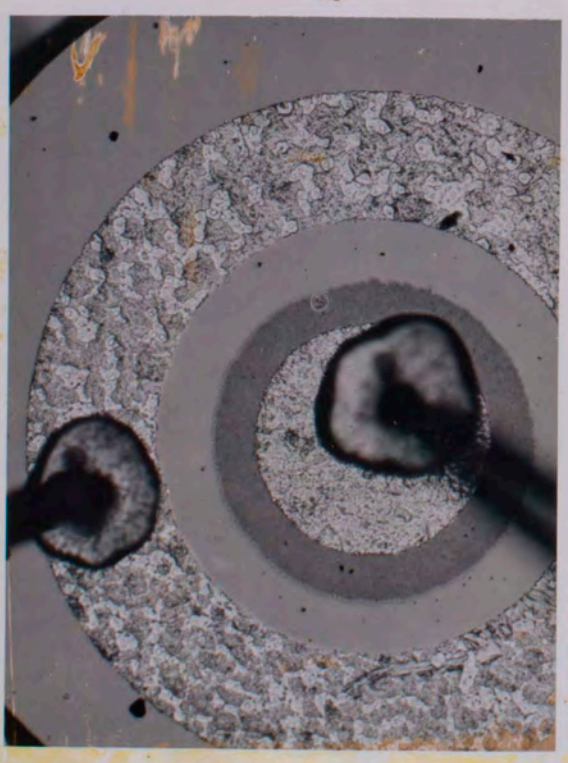
2
Before



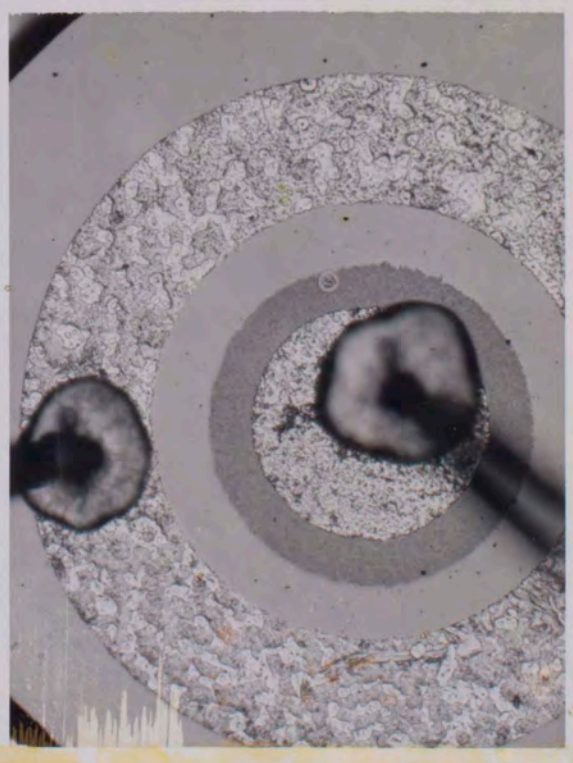
2
After



3
Before



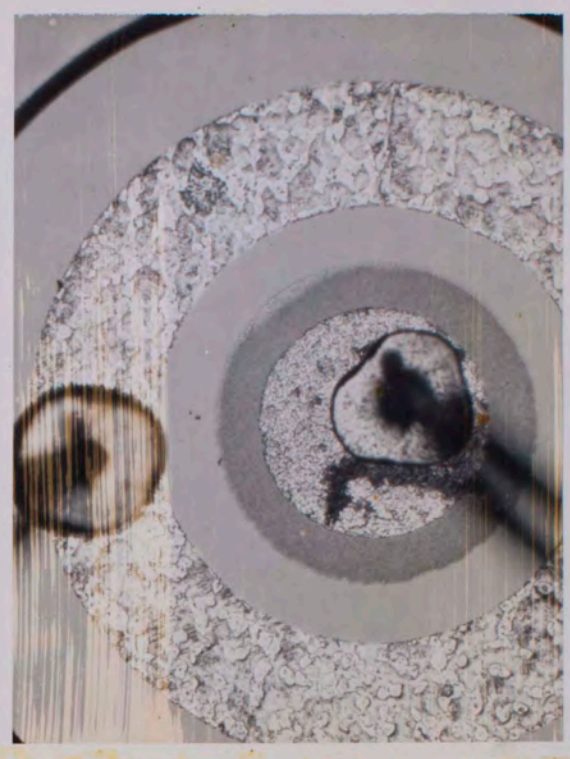
3
After



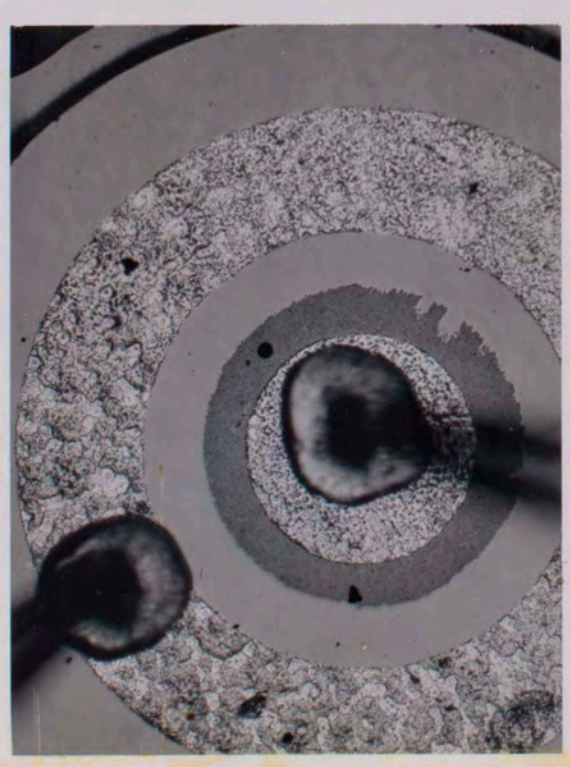
4
Before



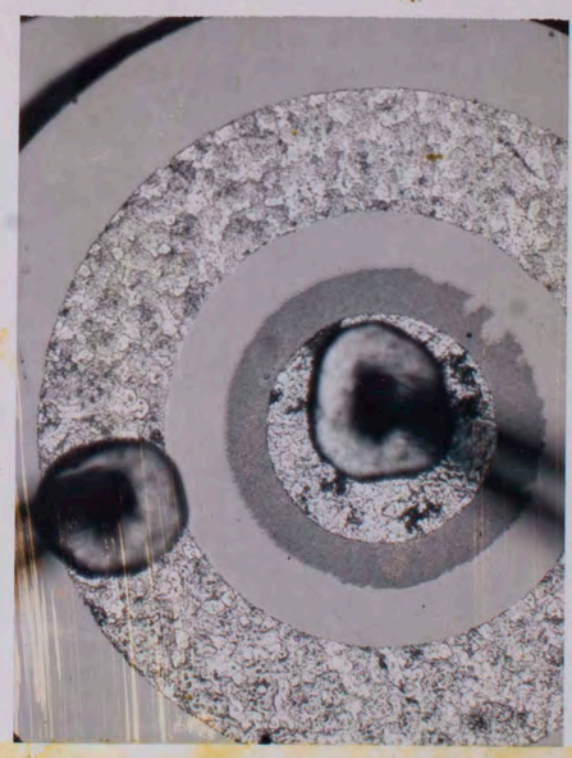
4
After



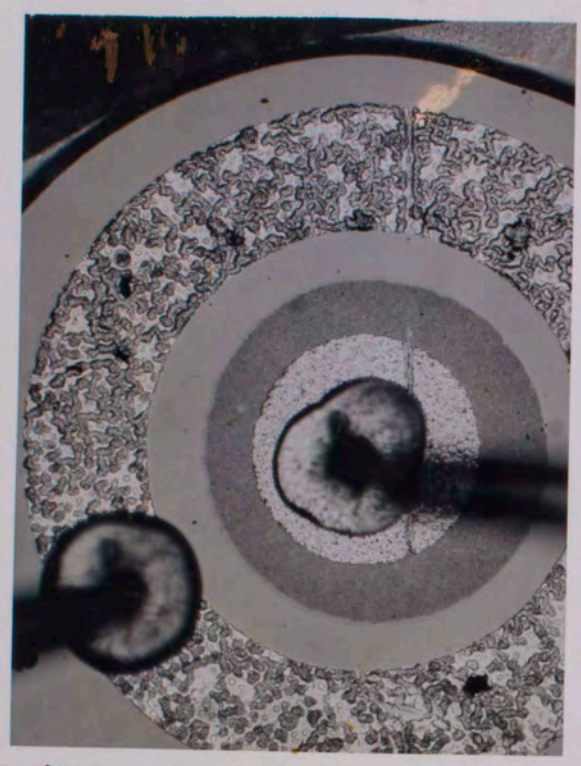
5
Before



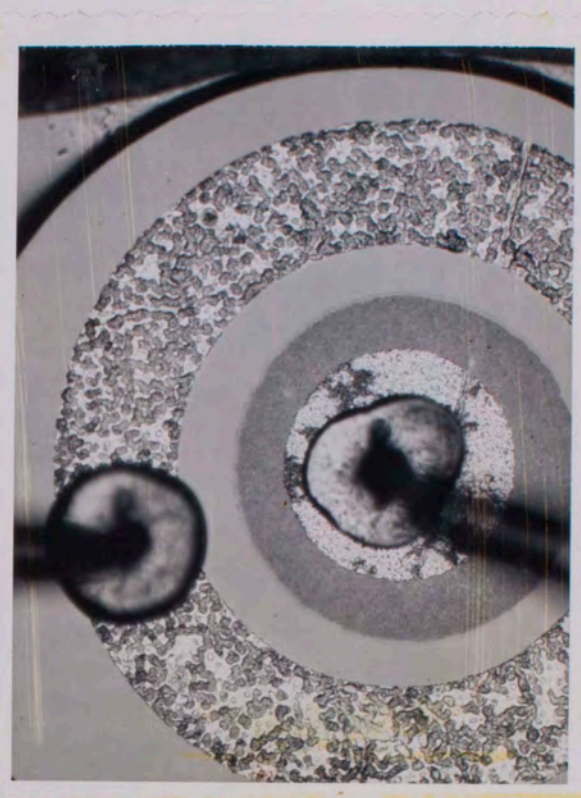
5
After



6
Before



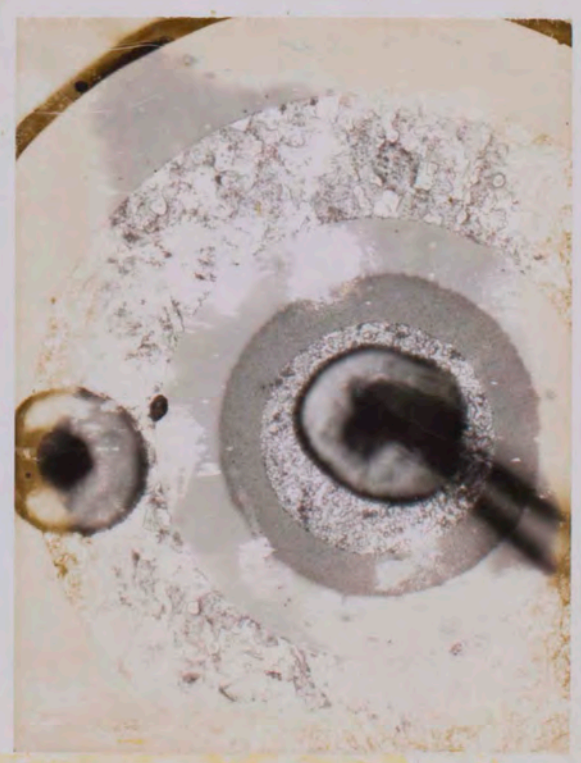
After



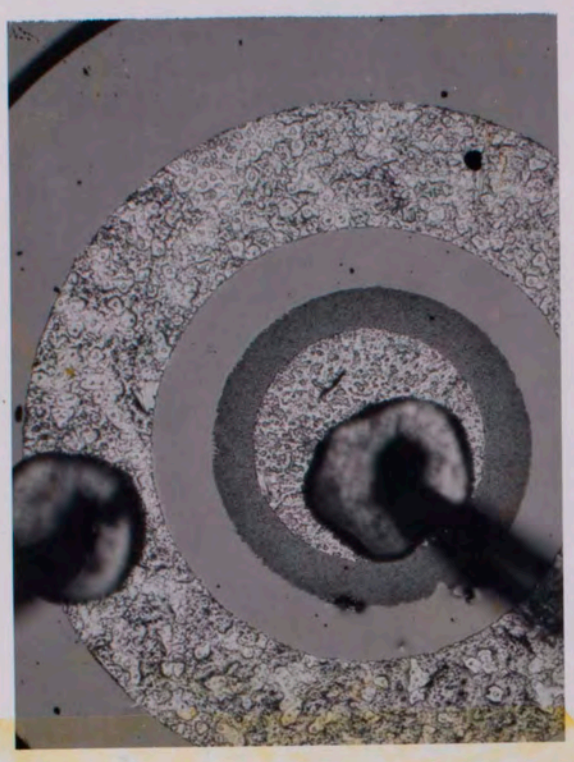
7
Before



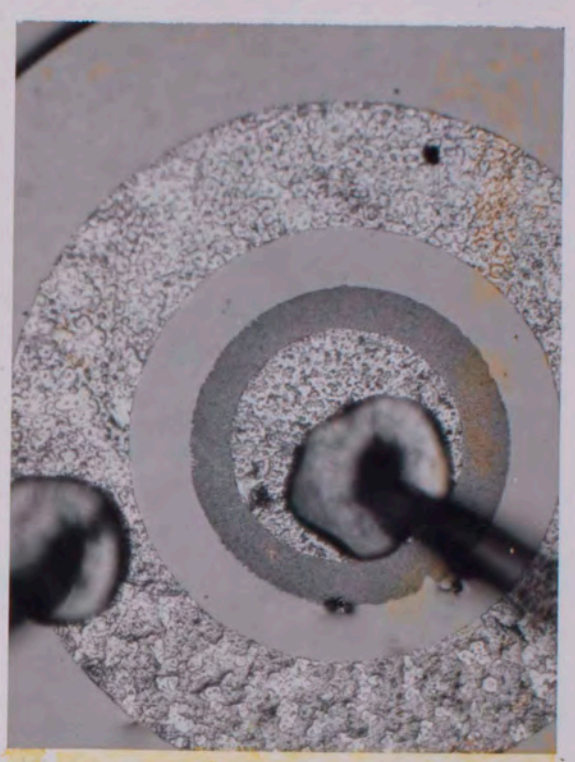
7
After



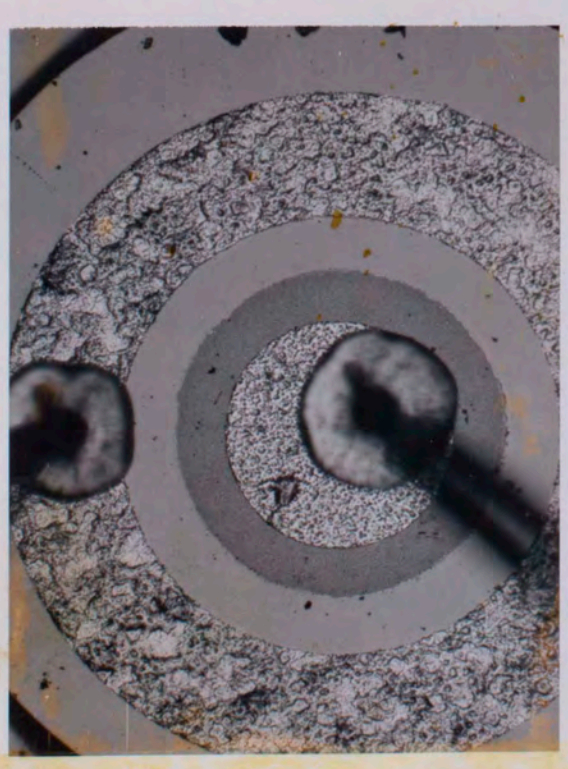
8
Before



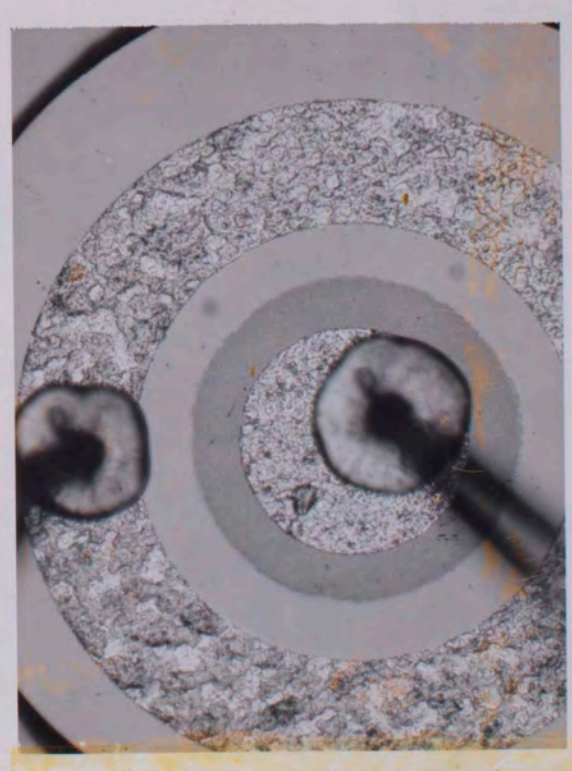
8
After



9
Before

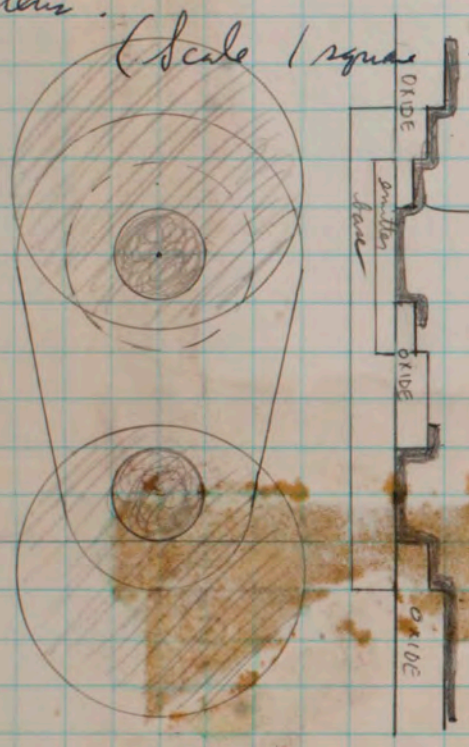


9
After



The recent information obtained from the results of Dick Crary and Dave Allison concerning the ability to alloy Al to Si when the oxide on the Si has been removed, but to maintain an adherent film over the oxide that is continuous electrically (and mechanically) with the alloyed region has stimulated thinking regarding some techniques for making electrically small devices while still employing mechanically large contacts.

For a 1st shot Dave Allison & then Beetle is going to try the apparently simple job of making a unit with ~1/4 the emitter area of the FT-1140. This looks roughly like this.



(Scale 1 square ≅ 0.0005", left picture only
oxide and metal cross-section not to scale

Because of the extrinsic base resistance this might be most useful for DCTL circuits rather than for example, the RMC oscillator. It will, however, be a v. high frequency structure.

In fact it looks practical to go very much smaller than this by an extention of this technique. If only one oxide removal is done for both emitter and base one can make the structure. By using a partial oxide etch between diffusions this is possible. A second photomask (to a ~~1/4~~ indexing error of ± 1/4 of the radius of the dot is adequate) can then remove oxide to extend the base for contact. For example as in Fig 2. A short P-type diffusion (for NPN's with an oxide marked diffusant – say B) at Co ≤≤ emitter Co, but enough for a good contact will then make a structure like in Fig 3

Fig 1 →

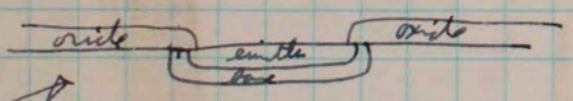


Fig 2 →

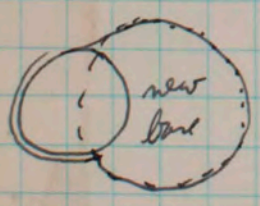
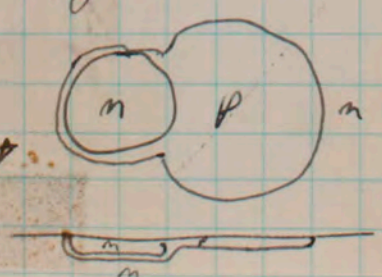


Fig 3 →



Contacts can then be applied as above to the emitter and base. This requires ~~±1/4~~ the emitter dot indexing. (cont'd next page)

By reasonable extentions of our present technique this should allow us to make a transistor with ~ $\frac{1}{64}$ the emitter area of our 2N706 and with a base area equivalent to ~ a 0.002" diameter circle. Such a device should be an extremely fast switch for currents in the 50 - 100 μamp range. Work on this follow immediately after the necessary resistance probe are obtained from the structures shown on the opposite page.

J. R. Mora 1/27/60

52 4/1/60

Analysis of some life test data on DC-997 coated FT-4000 transistors. —See next page!

Comparing 0 hr and 1016 hr data ±

Define: Failure: Change by ≥ ×2 to end up out of original spec.

Change: " " " " " " " " inside of " "

Condition	Parameter	Quantity	Fail	Change	MTF
Shelf	I_{CBO}	25	0	0	>25,000 hrs
	I_{EBO}		0	0	
	either		0	0	
200°C	I_{CBO}	39	0	1	>39,000 hrs
	I_{EBO}		0	5	
	either		0	5	
300°C	I_{CBO}	55	0	1	>55,000
	I_{EBO}		0	3	
	either		0	4	
270 mw 125°C	I_{CBO}	40	3	8	~10,000 hrs
	I_{EBO}		0	1	
	either		0	8	

In addition V_{BE} showed some changes. In particular at 300°C nearly all the units increased ~10%. at 200°C a somewhat smaller, but significant increase occured. B_o dropped slightly, but perhaps not outside the precision of the measurements.

4/1

P.S. Data returned to Wayne Logan

units 212A, 212C

~~# X-1984~~

X-1920 – X 2058

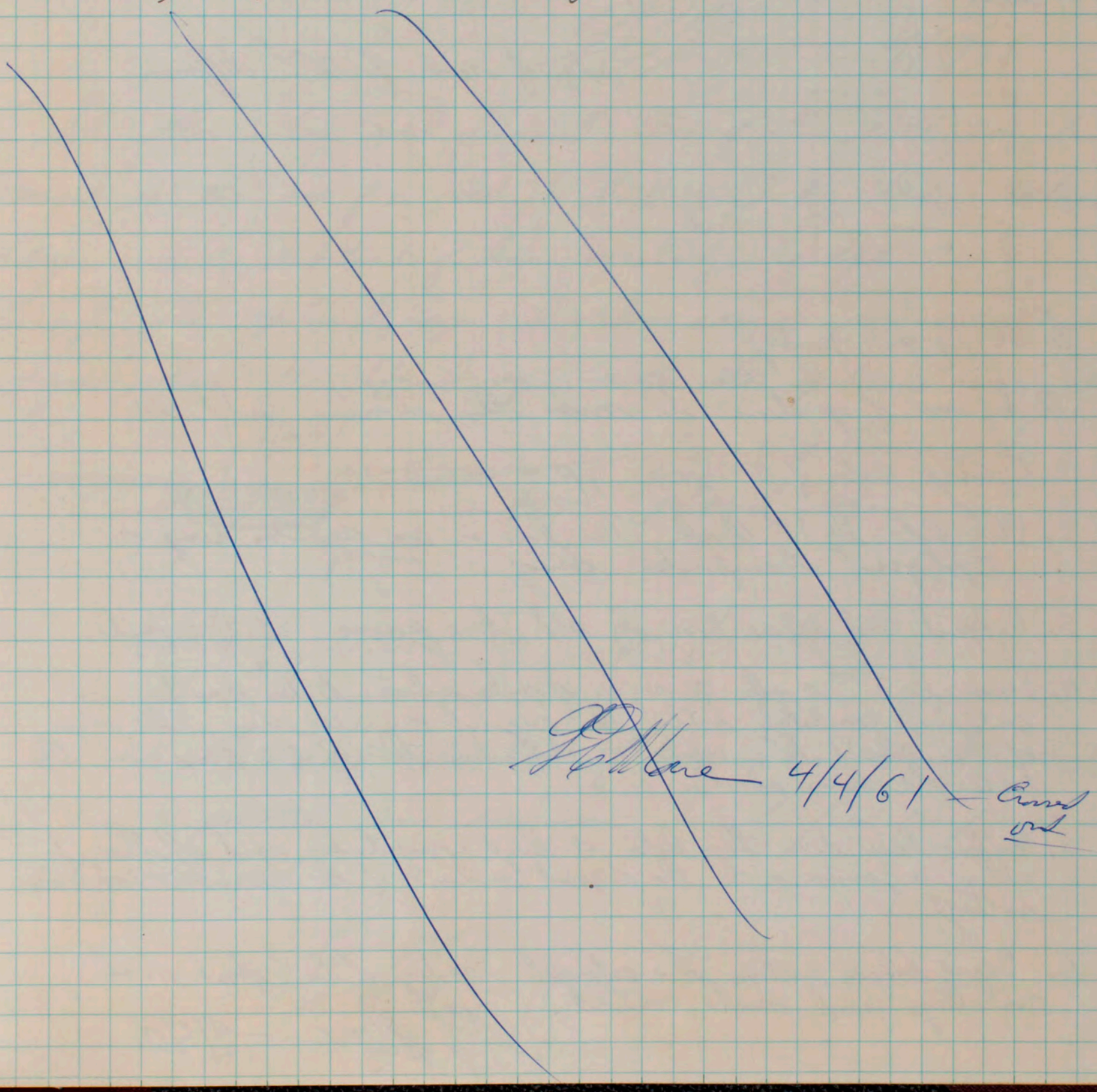
and X – 2067 – X 2086

Coretion to perious page:

Only half the units were coated, the other half were a control. This means that the data must be re-analyzed.

There were only 5 "charged" units (see definition opposite) of coated units including ~~one~~ one "failure", the failure is I_CO @ 270 mμ.

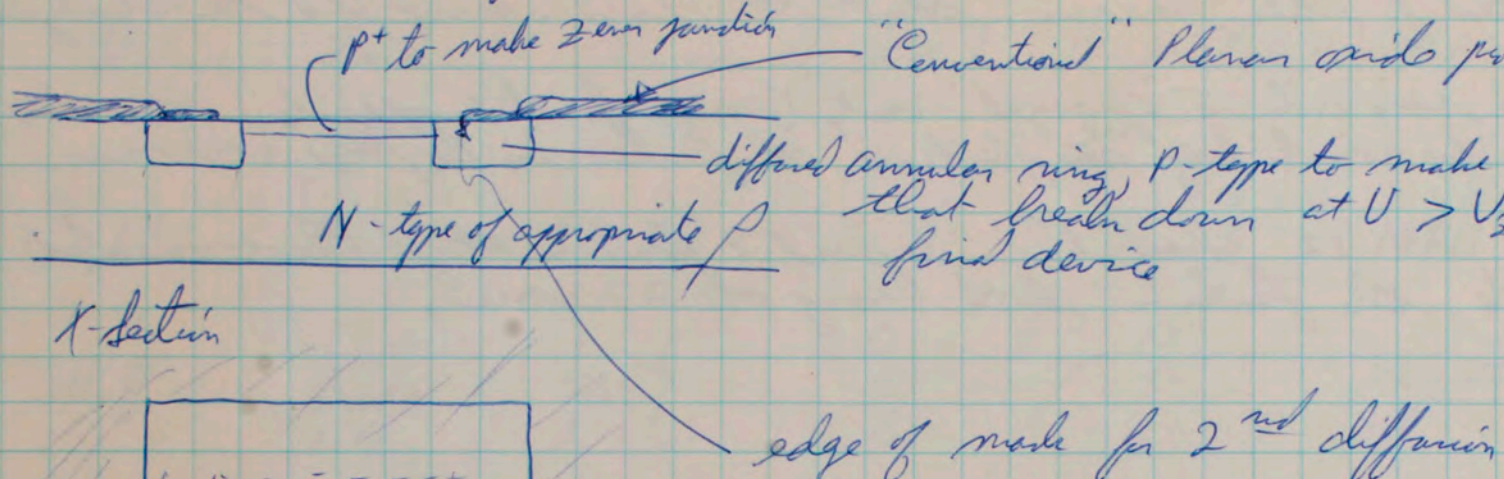
There were 12 "charged" units and 2 failures ~~of~~ of the uncoated units, the "failure" both being at 270 mμ.



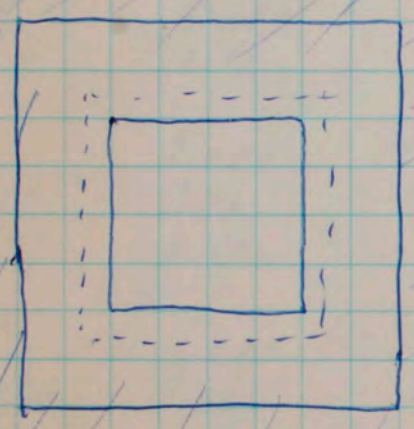
Tom Moore 4/4/61 Cancelled out

4/5/61

While talking about possible methods of making Zener diodes with V.H. Grinich and D.F. Allison the following idea was suggested (by me) to achieve bulk breakdown, but within our usual technological framework:



X-Section



Possible top-side geometry

A sequence of operations to make this structure could be:

1. Oxidize wafer of N-type Si, $\rho \sim 0.05\ \Omega$-cm
2. Etch hole by 1st Mask. This hole is an annular ring or topological transformation thereof
3. Predepsit and diffuse Boron by std. bare process rebuilding oxide.
4. Remove by 2nd mask a region of oxide whose outer boundary is contained completely within the original annular ring. The shape of this should be a circle or deformation there of (a square in the example shown above).
5. Diffuse boron down this hole at high concentration and shallow to achieve a junction with the original material of the desired breakdown voltage
6. Expose silicon within the outermost boundary of the first mask, metallize and make contact.

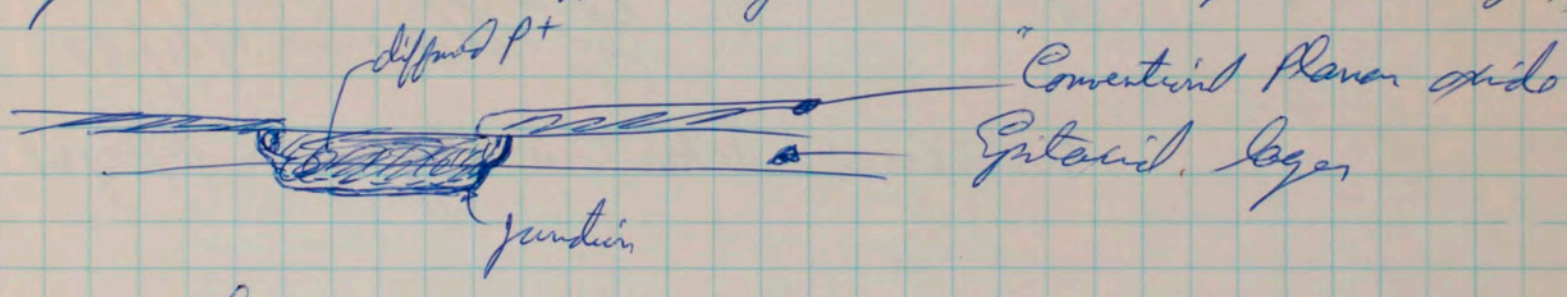
J. E. Moore — 4/5/61

4/5/61, cont

Such a device will breakdown first in the center region where the high concentration diffusion meets the bulk material. All breakdown should be well removed from the surface and the entire junction will be oxide-protected at the surface. This, accordingly, should result in a stable diode capable of operation in the region of avalanche and/or Zener breakdown.

G E Moore — 4/5/61

Some other ideas were discussed. One of these with considerable merit is the use of a relatively high resistivity, thin, epitaxial layer over a substrait of known resistivity. By diffusing clear through the epitaxial layer, breakdown can be restricted to the region where the diffused region meets the epitaxial layer, ie,



Substrait, 0.05Ω-cm N-type, for example

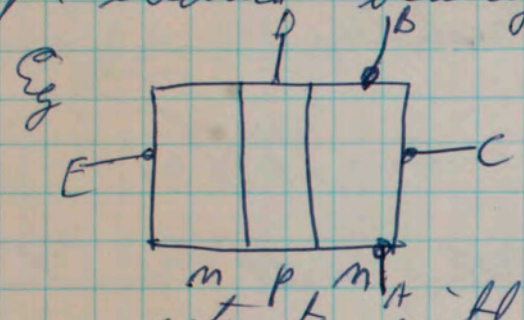
This has the added advantage of very low saturation resistance. It has a ~~potential~~ more unknowns in it from our present state of the art.

G E Moore 4/5/61

56 Oct 16, 1961

While discussing possible gadgets that might have adjustable long ~~term~~ term characteristics and reversible (analogous to the Memistor) with VH Grimes the following ideas came up:

Some rapid diffusers in Si (for example Li, Au) are charged and ~~i~~ are "rectified" by a junction. If one makes a three layer structure like a transistor it is possible that the rapid diffuser can be moved from one end through the center layer to the other by proper electrical biasing, there modulating the conductivity.



saturate with Li
look at resistance from A to B,
use C, D, or E as collector, base and emitter or visa versa
to inject Li into the region where resistance is monitored or
visa versa.

In this way the conductivity can be modulated and it will act as an analogue memory.

GE Moore 10/16/61

Witnessed & Understood VH Grimes 10/14/61

Nov-14, 1961

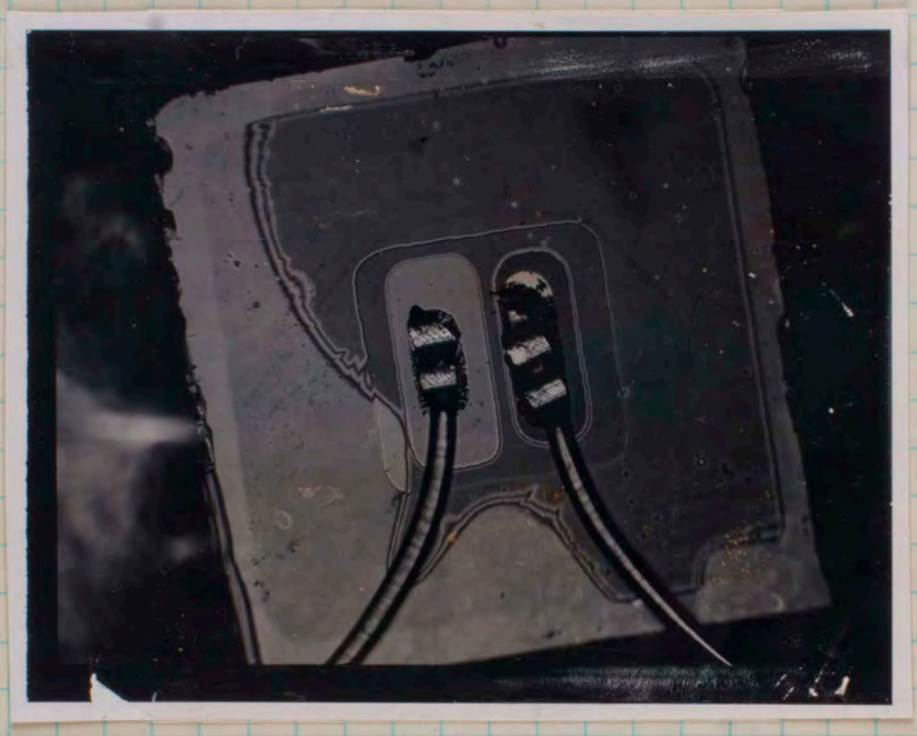
While engaging in a Project Review with CT Sah and J. Sander on Nov-6, 1961 concerning GaAs device structures I invented a novel process for diffusing in materials such as GaAs which have a high decomposition vapor pressure at diffusion temperatures. Basically this process involves growing a SiO_2 layer completely around the GaAs (or GaP or other similar material) wafer by a technique like Stever $Si(OC_2H_5)_4$ pyrolysis. Holes are then opened where the diffusion is desired. ~~It further~~ The source of impurity is then deposited in the holes and more oxide is grown by pyrolysis. Diffusion at 700-900° can then be done with the As contained in the SiO_2 (Arsenic is known from our Si experience that As does not go thru SiO_2 and that SiO_2 is stable at temperatures below ~1200°, even in the presence of Si. In this case it could easily be good up to the melting point, but this would have to be checked. In any case at ordinary GaAs diffusion temperatures we should be in good shape.

J. A. Allen 11/14/61

 Feb 22, 1963

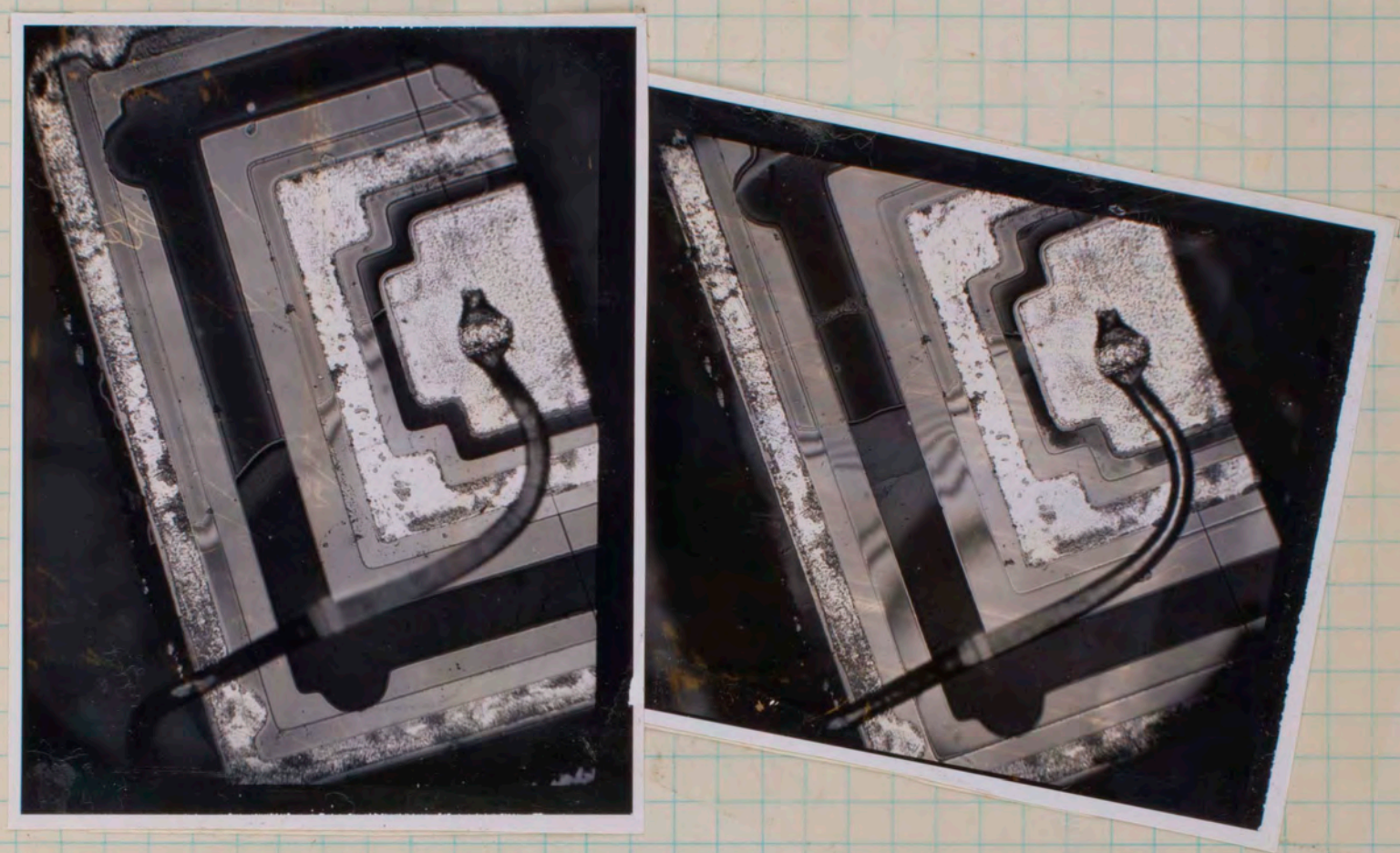
In connection with channel problems on PNP transistors and some of the results obtained with competitor devices, a brief investigation of the structure of the Speny and Motorola units was made.

Here is a photograph of the die of a Speny PNP. This unit had the oxide layer dissolved from a portion of it by wax masking and a 20 sec HF etch.



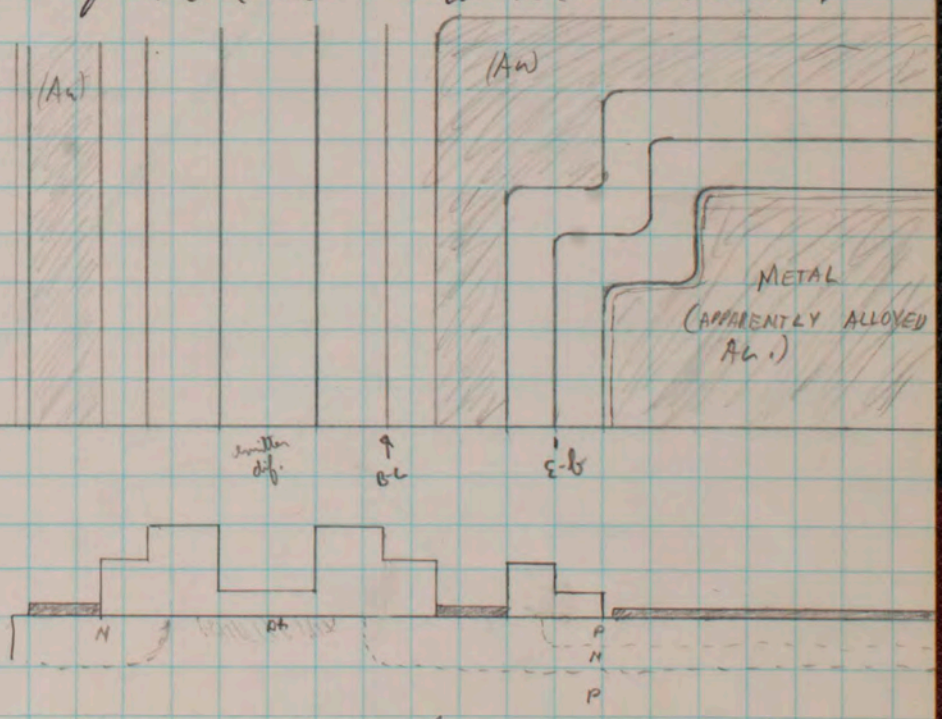
A significant feature is that the oxide thickness over the base region is about 2 or 3 fringes less than over the collector. It is quite thin over both regions.

A Motorola unit was similarly masked and etched for 20 sec and then re-masked and etched ~~for~~ a ~~few~~ one more minute



After 20 sec of etching in HF. (X 1207)

after an additional 2 min in HF.



Vertical X-section of this device (a different sample) are on the ~~other~~ next page.

60 Feb 26, 1963

Vertical section of the Motola device (stained

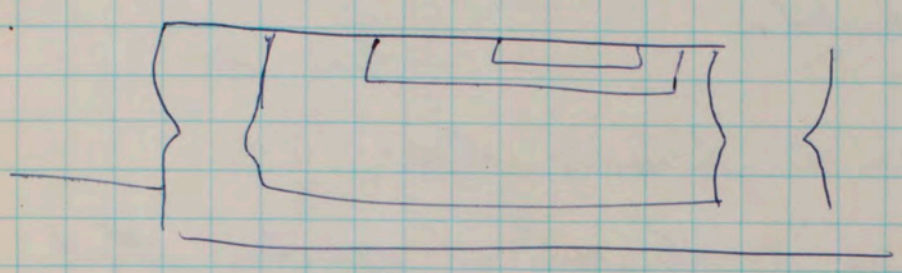


X(~260)

[signature] 2/26/63

Observation of the initial diffusion of some production grade wafers in an attempt to determine the extent of loss because of non-wanted areas of B diffusion.

Yesterday I took several wafers (electrical experts, everything else does for an hour), lapped them a fair lapping about one mil of the surface and stained the patterns in solution as best I could.



A wafer of 6" elements

I estimate I got just below the c-b junction at the deepest part — i.e., much less than halfway through.

Isolation region with no extra area: 99654
" " " " - " " " : 12220

 March 6, 1963

Last night I thought of a way to achieve a relatively high sheet resistivity diffused silicon resistor in a manner completely compatable with our present micro-circuit technology.

This method takes advantage of the facts that

a) Gallium is a very controllable diffusant in the relatively low concentration range, say ~ 10^{17} atoms/cc

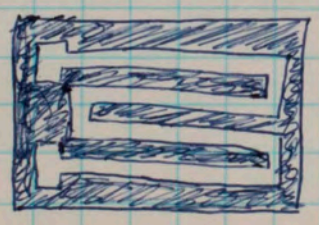
b) It is not oxide masked.

The resistor is prepared by the following steps

1. Everything the same up to the photoresist operation that prepares the holes for P emitter diffusion and collector diffusion

2. Add to the pattern of this mask a region corresponding to that required to remove the oxide from a region completely surrounding the desired resistor in one of the N- type isolation regions

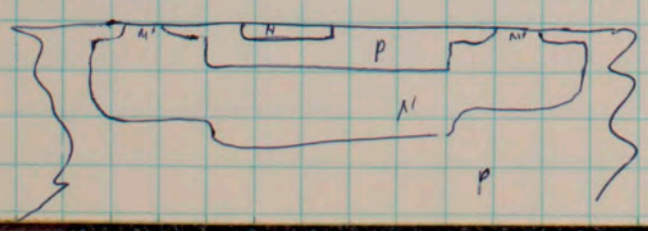
3. For example



where the shaded area is the opaque region on a photographic mask and corresponds to the area from which the oxide is removed.

3. After ordinary emitter diffusion, do a low Co gallium diffusion. This will penetrate the oxide and dope the surface. If done at low T, t combination the rest of the diffusion will not be affected significantly.

The disadvantage is that all exposed N-type bulk regions will develop a p-type channel. In many cases this should not bother the device if proper care is taken to include N+ region to restrict the extention. For example, a complete collector ring would be needed around a transistor, i.e.,



J. P. Moore
March 6, 1963

In order to put some numbers in to estimate what we might be able to achieve consider a typical case

$C_{Bulk} \sim 10^{16}$ n-type

C_o of Ga $\sim 10^{17}$

$\sqrt{Dt} \sim 1\mu$

From Sah's curves in the basic data handbook

$\frac{V}{I} 2\sqrt{Dt} \cong 4 \times 10^{2}\ \Omega\text{-}\mu$

or $\frac{V}{I} \cong \frac{4 \times 10^{2}}{2 \cdot 1} = 200\ \Omega$

or the sheet resistivity $\cong 4.3 \times 200\Omega \cong 860\ \Omega/\square$

Both the C_o and the $\sqrt{Dt}$ could probably be cut by a factor of at least 2. Under that condition the ~~sheets~~ sheet resistance could get as high as 3k or more per square.

J. P. Moore 3/6/63

Witnessed & Understood
V. H. Grinich 3/6/63

 May 26, 1963

San Rafael is being bothered by a failure mode on FD-2 and FD-3 diodes, wherein upon repeated testing there is a quantity that falls out because the characteristics become a short.

They sent me 11 of these units, whose history I do not therein know, for failure analysis.

As received these units had number tags on them.

Curve tracer readings of approximate resistance at origin:

Unit #	~R in KΩ
750	10
751	0.04
752	25 ("channelish")
753	1
754	2
~~755~~	
756	2
757	1
758	10
759	5
760	2
775	2.5

For preliminary analysis the side of the glass to expose the gate of the diode was ground (on the cut off wheel) on three typical units, # 750, 753 and 754.

#754 was unsoldered at the whisker - ball junction, but a quantity of solder got on the ball.

#753 was unsoldered between whisker and ball properly.

Upon microscopic examination the oxide layer over the die was found to have a film of non-uniform thickness and regions where there was a high density of little mounds of something. These were washed off in acetone and disappeared.

It is possible that they are artifacts introduced during desoldering — this must be checked.

The die had no obvious cracks, although the oxide had several pin holes and the edge of the oxide (where scribed) had a very ragged appearance.

5/26, cont

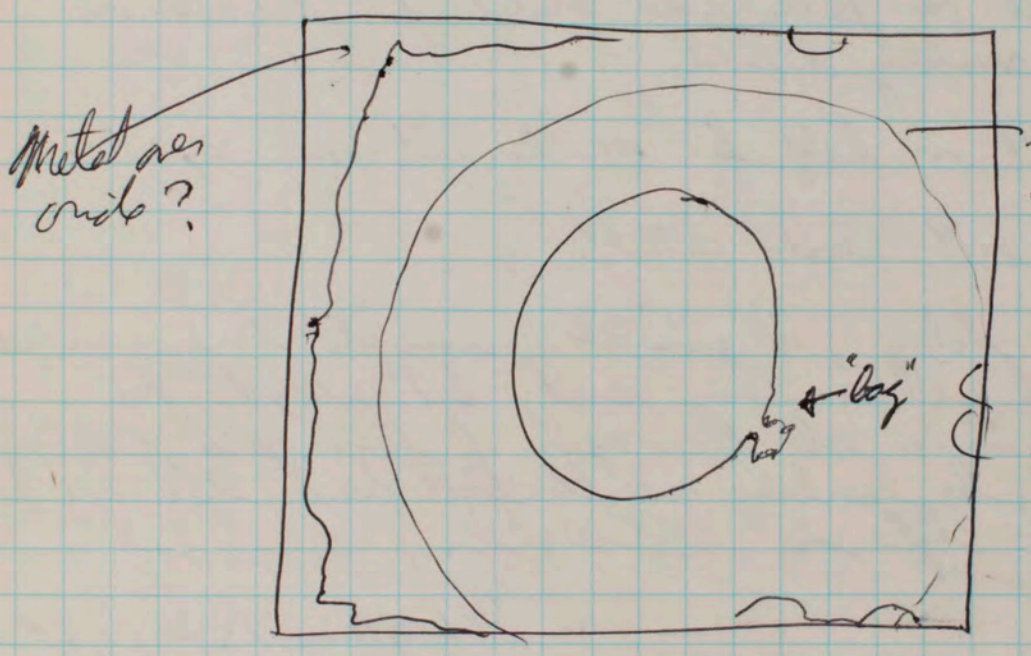
#750 was taken apart between lead and alumina with no heat. The only operations were

1. Wet grind
2. H_2O flush and air dry
3. Glass clipping with knife
4. separation of ball & alumina with knife
5. breaking of phy. in half.

With probe

#754 (ball off, rim all over)	1.5V, 0.5 ma	= 3K
#750 " on	2.5V, .2 ma	= 12.5K
#753		1K

754 after cleaning in acetone + TCE had many oxide flaw. There was a large circle of flaw completely around the active area and a bad "bay" off the circle.



The metal on the emitter dot scratched with the probe and shown no sign of being alloyed!

After HF all but the "bay" and the metal or oxide disappeared. unit was undamaged electrically

after a 3-sec etch in CP-6 the unit was clean except for metal or oxide and had pits at various places.

Masked through half, bay area pressed, & same electrically

By moving again to eliminate the bay, the unit became a diode, after a fashion, with 50 ma at 10 v (ie, 200 kΩ on a substrate lead) & it to ~20 ma at 40 v.

5/26, cont

#750

Oxide removed, ball on — same electrically

Mesa - etched 15 sec in CP-6 using ball for mask. 2.5 V, 30 μamps
Meared another 30 sec — same characteristics.

~~Other piece of the~~

The ball was then broken off with tweezers — this was a difficult job — it hung on for all it was worth. In the remaining small portion of the mesa — the center had all broken out with the ball — the characteristics were greatly improved. For example 20 v and ~1 μamps or more breakdown at ~200 v, <30 μamp.

Conclusions:

1. Neither device 750 nor 754 had a cracked die problem.
2. The problem with 750 was well under the gold ball.
3. The degree to which the balls were bonded to the die on 750 and 754 were completely different.

Take 760 and break it in half to see how it comes apart.

It came apart at the ball-whisker contact!

After removal and etching, it was the same old thing — ~2 μ
The ball was not centered well on this unit but except for that it looked ok. In particular all the region of thick gold penetration should have been removed by sanding out the ball and etching. It becomes apparent that life is not simple.

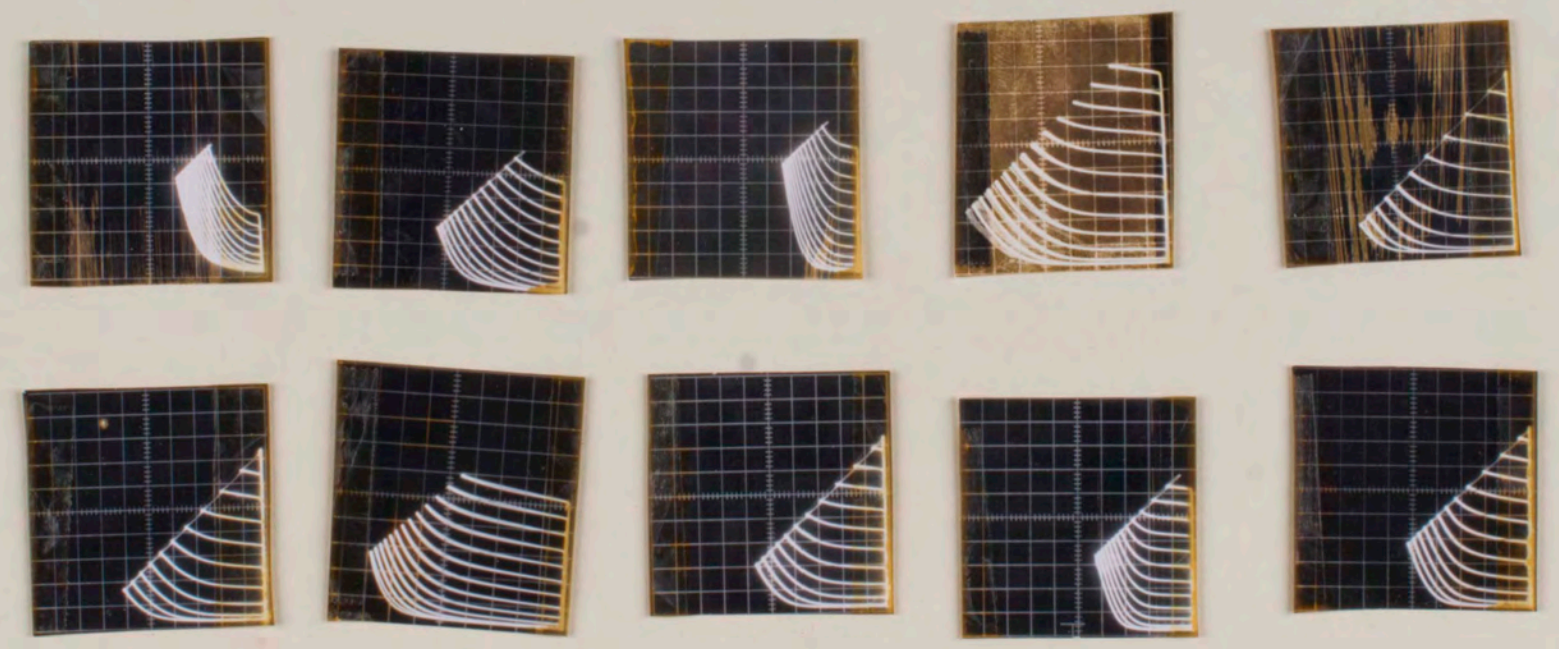
Etching was 15 sec, CP-6.

J. E. Mar

2900 Semiconductor Drive
Santa Clara, CA 95052-8090

National Semiconductor

from pages 14+15
Moore Lab Book
(FSC) #6



NPN	30V V_{CB} I_{CBO} 50°C	BV_{CE} @ 10μa 50°C	BV_{CE} @ 100μa 50°C	BV_{CB} @ 10μa 50°C	BV_{CB} @ 100μa 50°C	h_{fe} @ 150ma 10V 50°C	$V_{CE(SAT)}$ 15ma 150ma	V_{BE} 15ma 150ma
LOT 77 174C-17	.004μa		open					
LOT 67 174C-3	.8μa	46	43	81	88	60	.81	1.1
LOT 67 174C-16	.07μa	45	40	51	65	49	1.4	1.1
LOT 85 174-4	.8μa	40	36	84	85	45	.62	1.0
LOT 69 172-13	18.μa	23	14	53	84	66	.25	1.0
LOT 87 172B-14	.076μa	57	47	89	91	54	.80	.97
LOT 95 175D-7	.07μa	63	52	70	74	65	.84	1.0
LOT 69 172-28	.01μa	62	51	93	95	6.6	.79	.95
LOT 74 174B-12	8.7μa	39	38	75	84	45	.97	1.15
LOT 104 175E-16	.06μa	45	44	47	47	64	.88	1.0

I_{CO} @ 30V V_{CB} / 100°C

BV's 100°C

30V I_{CO}	BV_{CE} 10μa	BV_{CE} 100μa	BV_{CB} 10μa	BV_{CB} 100μa	HFE	V_{CE}	V_{BE}
						←	open
20μa	.4	1.0	1.0	94	5.1	1.0	1.0
.24μa	38	37	54	70	4	1.2	1.0
36μa	.4	.6	.5	94	3.8	.7	.9
.54μa	46	43	85	88	5.5	.84	.9
4.4μa	.6	40	95	96	4.4	1.0	.9
.38μa	71	78	71	78	5.4	1.1	.92
.18μa	60	51	100	100	5.4	.97	.86
7.8μa	.4	1.7	70	90	3.8	1.3	1.0
7.4μa	.8	47	56	60	5.5	1.2	.92

NPN	I_{CO}	BV_{CE} 10μa	BV_{CE} 100μa	150°C BV_{CB} 10μa	150°C BV_{CB} 100μa	h_{fe}	V_{CE} SAT	V_{BE} SAT	I_{CO} @30V	BVce	100μa BVce	200°C 10μa BVcb	200°C 100μa BVcb	H_{FE}	V_{CE} sat	V_{BE} Sat	
																	open
67 - 174 C-B	.3ma BD.	.2	.3	.1	1.6	4.5	1.15	1.1	BD	0	.2	C	.5	3.5	1.6	1.0	
67 174C-16	5μa	.2	.18	61	76	3.6	1.5	1.0	5μa	0	.2	0	54	3.6	2.0	1.0	
85 174-4	B.D	.2	.3	.1	.7	2.6	[illegible].86	.84	BD	0	.2	0	.4	2.4	1.2	.85	
69 172-13	3μa	.4	36	90	93	4.6	.96	.86	7.2μa	0	.2	100+	100+	0	>3	>3	opened
81 172 B-1A	.2ma BD	.2	.4	.2	2.6	3.6	1.2	.85	BD	0	.2	C	.8	2.8	1.6	.8	
95 175D-7	4.3μa	.5	39	68	82	5.2	1.2	.9	46μa	0	.2	.2	83	4.2	1.6	.88	
69 172-28	3.4μa	.4	42	100	100	4.6	1.2	.83	50μa	C	.2	.2	100+	4.0	1.4	.8	
74 174B-12	34μa	.2	.4	.6	93	3.0	1.5	.93	.15ma	0	.2	0	7.0	2.6	1.95	1.0	
104 175E-6	.14ma BD	.2	.5	.2	4.8	4.5	1.4	.86	BD	0	.2	0	1.8	4.0	1.75	.87	