Dataquest®

Semiconductors

Integrated Circuit Packaging Trends

Focus Report

1993

Program: Semiconductors Worldwide
Product Code: SEMI-WW-FR-9301
Publication Date: April 19, 1993

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Chapter 1
Executive Summary

The evolution of microelectronic packaging technology is strongly influenced by the following primary forces:

- Demand for more on-chip functional density, a phenomenon inseparable from advancing submicron device technology
- Continued increase in chip dimensions and decrease in interconnection pitch
- Demand for improved microelectronic system performance, especially functionality, speed, and reliability
- Competitive pressure to achieve system cost reduction

In 1959, Fairchild Camera and Instrument developed the planar technology for making transistors, which later became the basic technology for the manufacture of integrated circuits (ICs). From the beginning of the IC era through early 1983, feature size shrunk 11 percent per year, chip area increased 19 percent per year, and packing efficiency improved by a factor of two per decade. These three factors combined produced a hundredfold increase in devices per chip every decade.* From the beginning of the IC era, a volume of packaging innovations have been introduced as solutions to increased levels of integration from SSI to ULSI. Table 1-1 lists some major package innovations. Continuous innovation in package design, materials, assembly methods, and related technology resulted not only in improved utilization of microelectronic systems, but also in a multiplicity of package designs with increasing levels of complexity.

Semiconductor Package Definitions

Through-hole (TH) and surface mount (SM) are the two basic types of package technologies for purposes of making the package to board connection. The printed circuit board with plated through-holes was developed in 1953 to replace the labor-intensive method of hand-wiring electronic circuits. However, the through-the-board concept of mounting components on copper-etched phenolic or glass epoxy boards with predrilled holes was not implemented until the late 1960s. In TH technology, the metal pins or leads of semiconductor packages are inserted through the plated holes of the printed circuit board for soldering on the back side of the board. The mounting holes and other holes for connecting the interconnect layers are gold-plated to effect reliable contacts for easy solderability. When all of the components are mounted, the printed circuit board is passed through a wave-soldering process. During soldering, liquid solder flows across the bottom of the board and adheres to the leads and walls of the holes. This completes the electrical and mechanical connections. Dual in-line packages (DIPs), zigzag in-line

* J. Meindl, *"Theoretical, Practical, and Analogical Limits in ULSI,"* IEEE International Electron Devices Meeting (IEDM '83), pp. 8-13

Table 1-1
IC Package Time Line

Date	Event
1960	GE develops Minimod (TAB) nonconductive film copper etch surface
1963	Fairchild DIP package developed by Rex Rice
1964	Texas Instruments develops transfer mold and plastic encapsulation for active semiconductor transistors
1968	Philips develops the SO package
1969	Delco develops the SMT module for hybrid voltage regulators
1970	Signetics introduces the SO package into the United States
	AMP develops the premolded chip carrier
1971	IBM introduces the first PGA
1973	3M develops the Chip Carrier for RCA, Texas Instruments, Honeywell, and Motorola
1976	JEDEC standards developed for Chip Carrier
1982	Mostek develops the RAMpak, the first memory module
	Japanese manufacturers introduce the QFP
1986	National Semiconductor introduces TapePak
1987	Fujitsu introduces first SMT PGA
	Mitsubishi, Fujitsu, and Sony standardize the VSOP and VQFP
1989	Olin introduces the metal Quad
	Toshiba introduces the metal PGA

Source: Dataquest (April 1993)

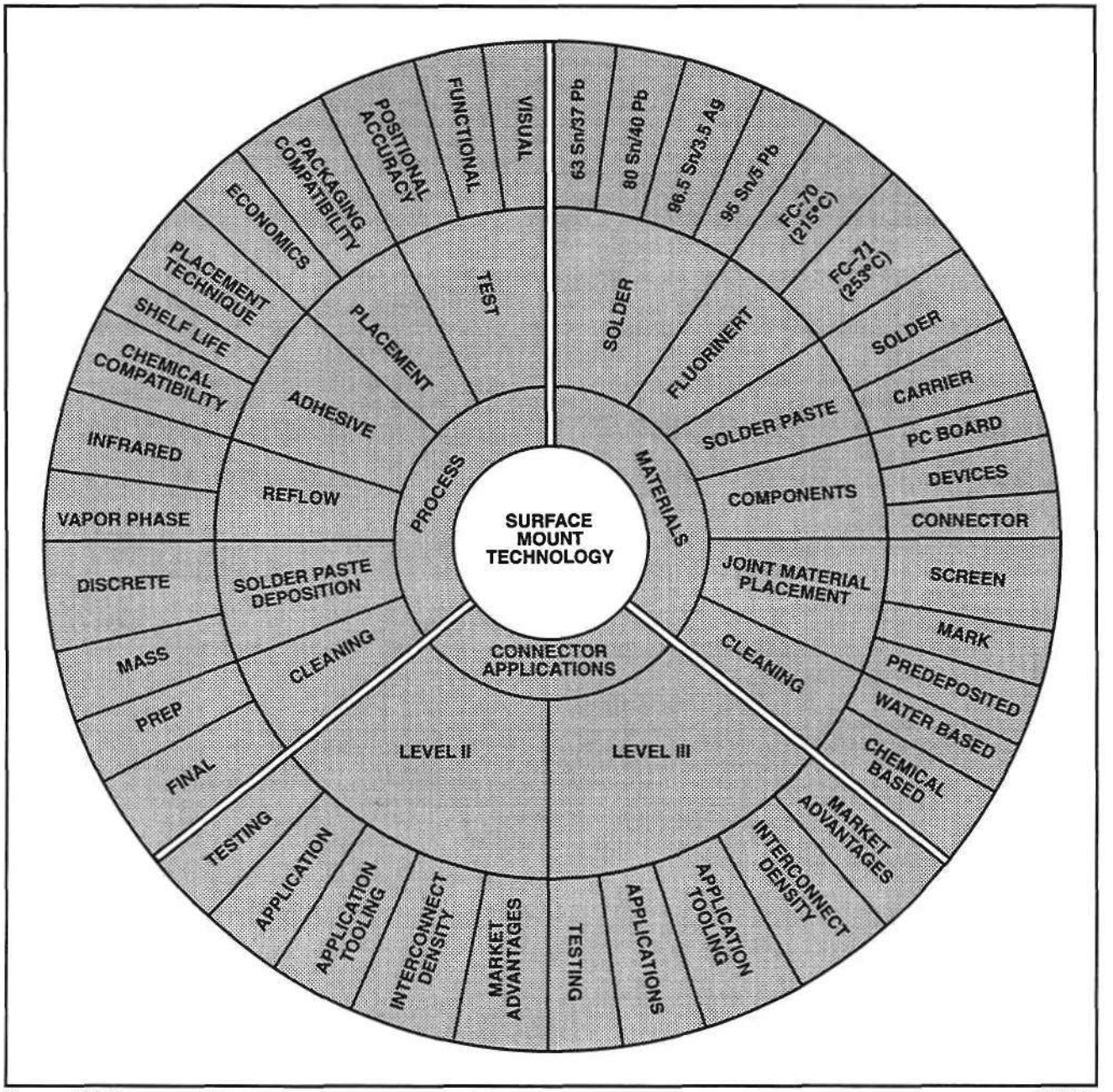
packages (ZIPs), ceramic DIPs (CERDIPs), single in-line packages (SIPs), and pin grid arrays (PGAs) are all classified as TH-types of packages.

Surface-mount packages with pins or pads are attached onto the top or the bottom of the board rather than inserted through the board. This form of assembly was developed in Europe for the Swiss watch industry in the late 1960s. Surface-mount technology (SMT) emerged in the United States in the mid-1960s in the form of surface-attached flatpacks for use in missile-guidance computers. Japanese manufacturers adopted SMT in the early 1970s as the need for miniaturization and cost reduction arose in consumer products such as watches and calculators.

Evolutionary changes in semiconductor technology from LSI to VLSI and ULSI devices continued to drive demand for newer SMT developments. These developments also required a substantial investment in engineering effort dedicated to circuit layouts, substrate and component materials, processes, and assembly equipment. Figure 1-1 shows the relationships among materials and processes involved in and influencing the design of surface-mount packages and the board interconnect.

The onset of SMT also increased the demand for automated assembly lines, which contributed to improved product and board reliability as well as system cost reduction. Although the initial investment for

Figure 1-1
Surface-Mount Technology Materials and Processes



Source: AMP Incorporated G3000291

automated equipment was high, reduced assembly costs were soon realized through less material, less board space, ease of manufacture and test, and overall improvements in package and system reliability. Table 1-2 lists the most commonly used SMT package types.

Table 1-2
Surface-Mount Packages

Abbreviation	Description
SO	Small Outline
SOP	Small Outline Package
SOJ	Small Outline J Lead Package
TSOP	Thin Small Outline Package
PLCC	Plastic Leaded Chip Carrier
LDCC	Leaded Ceramic Chip Carrier
CLCC	Ceramic Leadless Chip Carrier
PQFP	Plastic Quad Flat Package
TQFP	Thin Quad Flat Package
Cerquad	Ceramic Quad Package
MQUAD	Metal Quad Package
CQUAD	Ceramic Quad Package
CQFP	Ceramic Quad Flat Package
QFP	Quad Flat Package
VQFP	Very Small Quad Flat Package
TQFP	Tabbed Quad Flat Package
SQFP	Shrink Quad Flat Package
VSOP	Very Small Outline Package (promoted by EIAJ)
VSOIC	Very Small Outline Package (promoted by Philips)
TSOP	Thin Small Outline Package
TQFP	Tabbed Quad Flat Package (promoted by LSI Logic)
GQFP	Guard Ring Quad Flat Package
TapePak	Molded TAB Package (promoted by National Semiconductor)
MikroPack	Encapsulated TAB Package (promoted by Siemens)
IMP	Bumper Quad Flat Package (promoted by Intel)
SIP	Single In-Line Package
SIMM	Single In-Line Memory Module

Source: Dataquest (April 1993)

Package Design Trends

The DIP package available in a variety of plastic and ceramic (cofired, CERDIP, and ceramic glass) configurations was the mainstay for world-wide IC encapsulation through the late 1980s, growing with LSI developments from 14 to 64 leads. The DIP derived its name from its two rows of in-line leads. The ceramic DIPs incorporated a multilayer ceramic body featuring brazed-on leads and a die-mounting cavity with a solder-sealed metal lid. The sealing techniques were gold-plated metal lids and gold-tin eutectic sealing preform.

More cost-effective ceramic DIPs used a glass seal to attach the lid to the package. CERDIP packages comprised two ceramic body parts and a lead frame. After the IC is attached and wire bonded to the lead frame, the pieces are run through a furnace and fused with a glass seal. CERDIP packages offered the least expensive hermetic technology available. In 1983, Intel Corporation developed a silver-loaded glass system as a nongold die attach substitute in CERDIP packages. The silver/glass system offered significant cost and processing advantages for nonvolatile products. Its performance limited by its 0.100 pitch or lead spacing and pin count, the traditional DIP package was replaced by new generations of shrink-DIP packages with a 0.050-inch center, newer ZIP packages with 2.54mm lead pitch, and eventually the Quad flat packages (QFPs).

As commercial development of surface mount became prevalent in the early 1980s, the Electronic Industries Association of Japan (EIAJ) began to develop its own versions of an old ceramic 50-mil flat package design predominantly used in military applications in the United States. Renamed the QFP, the body of the package was available in either square or rectangular format with pitches of 1.0mm (39.4 mils), 0.8mm (31.5 mils), and 0.65mm (25.6 mils) and in 20 to 240 leads.

Consumer market demands for smaller and low-cost electronic gadgets promoted the development of fine pitch package technologies. Japanese semiconductor manufacturers developed the shrink QFP (SQFP) and the very small QFP (VQFP) as extensions of the EIAJ QFP family of products. Although the standard body sizes are the same, the package is thinner and the lead pitches were reduced to 0.5mm (19.7 mils), 0.4mm (15.7 mils), and 0.3mm (11.8 mils). The pin count range now available is 32 to 520 leads.

A subset of the VQFP product was later developed and called the thin QFP (TQFP). This package has the same 0.5mm, 0.4mm, and 0.3mm pitches as the VQFP, but package thickness has been reduced even further to 50 mils, or 1.27mm. Another variation of the QFP design is the metal quad (MQUAD/Olin trademark) package. The MQUAD is constructed from anodized aluminum piece parts and is assembled using plastic package assembly processes.

Another package development was the very small outline package (VSOP). One version from Japan uses the EIAJ standard body size for the SO but reduces the pitch from 50 to 25.6 mils (0.65mm). A subset of this package is the thin SO package (TSOP), whose pitch is 0.65mm or less and whose thickness has a maximum height of 50 mils (1.27mm). The TSOP has leads on the two narrow ends only and developed into a major package for high-density DRAM devices.

Very similar to the VSOP is the VSOIC, a European version of a fine-pitch SO package. Developed by Philips, the lead counts range from 14 to 56 on 30- and 40-mil center spacings. Texas Instruments also introduced its own version of the VSOP, which featured a 25-mil lead

pitch. The standoff height was increased to 8 to 16 mils for the VSOP. This increase in standoff height was to facilitate board cleanup after assembly.*

During the last five years, the majority of SM ICs have been encapsulated in the SO packages. Growth in the SO package family has been driven by analog, standard logic, and memory devices. The proliferation of the quad configurations has been predominantly driven by the high-density, high pin-count ASICs.

Project Analyst: Mary A. Olsson

*R. Moore, G. Ricci, *"Electrical and Mechanical Attributes of the Fine-Pitch Small-Outline Package,"* Texas Instruments Incorporated, Sherman, Texas, 1988, p. 5

Chapter 2
Integrated Circuit Package History and Forecast

The worldwide packaging forecast discussed in this chapter is an evaluation of the total number of single-chip packaged ICs produced in the four major regions researched by Dataquest. This forecast is based on the following analysis:

- Dataquest's semiconductor worldwide forecast
- Survey of ceramic package suppliers' estimates of yearly package production
- Survey of semiconductor suppliers' estimates of IC products, by package types
- User survey of package designs, by application

The forecast also includes data on bare die shipments. This has been included to follow the potential development of new and emerging interconnect technology, as well as potential displacement or erosion of single-chip package types by other competing package technologies such as 3-D ICs, stackable memory modules, and multichip modules (MCMs).

Dataquest's surveys include data from all suppliers to the merchant semiconductor market. It excludes captive suppliers that manufacture devices solely for the benefit of the parent company. Included, however, are companies that actively market semiconductor devices to the merchant market as well as to other divisions of their own companies. For such companies, both external shipments and internal consumption are included. Shipment is defined as the purchase of a semiconductor device or devices. This definition must be differentiated from actual use of the device in a final product. A regional market includes all devices sold or shipped to that region.

Worldwide Forecast

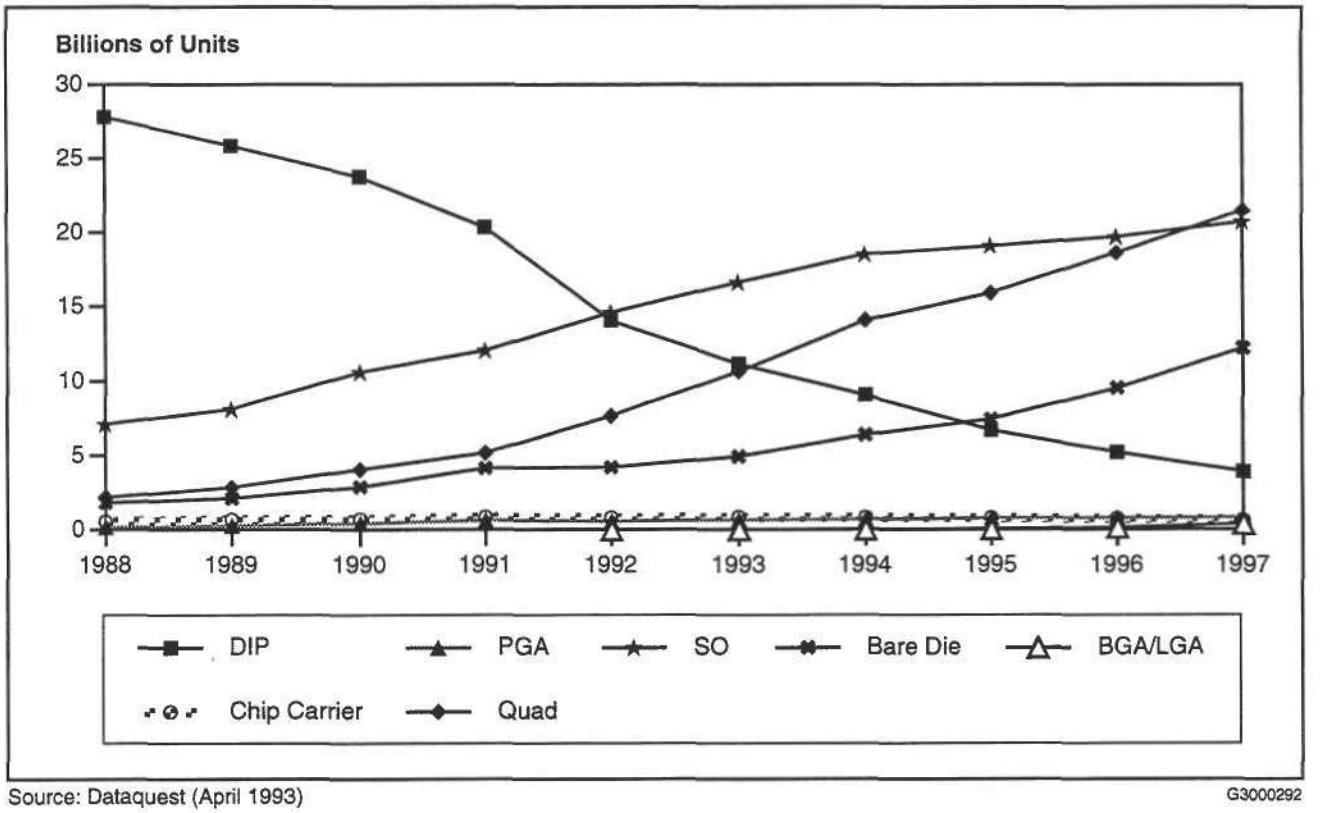
Table 2-1 lists single-chip IC packages as well as available bare die from 1992 through 1997. The DIP packages, both plastic and ceramic, continued to decline, with a final year-end actual production of 14 billion units, compared with our early November estimate of 16.8 billion units for year-end 1992. The SO and quad package category, which includes all the smaller and thinner variations of these two product families, continued to grow in dominance, as reflected in the package life cycle trends shown in Figure 2-1. Ceramic PGA packages, originally forecast to reach 500 million by year-end, dropped precipitously to 165 million units by year-end 1992. Although we have continued to forecast modest growth in the ceramic and plastic PGA packages, there are very strong market indications from package designers and systems houses that a major shift is taking place in microprocessor and ASIC designs from PGA to plastic quads as well as new ball grid array (BGA) designs. The array packages have also been referred to as solder grid arrays, bump arrays, or overmolded plastic pad array (OMPAC), a Motorola acronym. Users

Table 2-1
Estimated Worldwide IC Package Forecast (Millions of Units)

Package	1992	1993	1994	1995	1996	1997
Plastic DIP	11,892	9,242	7,412	5,366	3,956	2,703
Ceramic DIP	2,165	1,907	1,653	1,336	1,193	1,012
Quad	7,739	10,854	14,185	15,798	18,649	21,480
Ceramic Chip Carrier	171	180	162	143	122	92
Plastic Chip Carrier	530	557	561	543	514	441
SO	14,587	16,506	18,210	18,851	19,332	20,219
Ceramic PGA	165	190	210	230	260	290
Plastic PGA	228	260	256	285	293	298
Ball/Land Grid Array	1	5	12	17	44	113
Bare Chip	4,215	4,925	6,245	7,328	9,413	12,234
Total	41,693	44,626	48,906	49,897	53,776	58,882

Source: Dataquest (April 1993)

Figure 2-1
Chip Interconnect Designs Package Life Cycle Trends



Source: Dataquest (April 1993)

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have indicated that this shift from PGA to quads and other grid array designs is being made for purposes of performance and size reduction, as well as significant cost efficiencies of these packages over the PGA.

These are clear signals that indicate an early maturation and potential demise of both ceramic and plastic PGAs.

North American suppliers of semiconductors continue to be the largest producers and consumers of ICs in the traditional DIP package (see Table 2-2). The CMOS gate array devices continue to be the mainstream driver for QFPs and eventually the BGA designs, although we are forecasting modest growth for the BGA designs activity and momentum for this package design is developing through the efforts of Citizen of America, Motorola, IBM, and Intel Corporation. The reported benefits of the BGA over the QFP are as follows:

- BGA has a smaller footprint than a comparable QFP.
- Bumps designed under the chip are used as thermal vias.

Table 2-2
Estimated North American Package Forecast (Millions of Units)

Package	1992	1993	1994	1995	1996	1997
Plastic DIP	5,978	5,001	3,640	2,305	1,644	1,100
Ceramic DIP	1,100	1,000	900	789	690	600
Quad	2,215	3,500	4,800	5,176	5,900	6,500
Ceramic Chip Carrier	111	115	102	88	74	50
Plastic Chip Carrier	370	388	407	401	388	345
SO	2,300	3,070	3,962	4,333	4,500	4,738
Ceramic PGA	60	70	71	80	111	159
Plastic PGA	130	155	150	155	160	163
Ball/Land Grid Array	1	5	10	12	27	71
Bare Die	1,284	1,660	2,390	2,888	3,633	4,629
Total	13,549	14,964	16,432	16,227	17,127	18,355
Percentage of Total						
Plastic DIP	44	33	22	14	10	6
Ceramic DIP	8	7	5	5	4	3
Quad	16	23	29	32	34	35
Ceramic Chip Carrier	1	1	1	1	0	0
Plastic Chip Carrier	3	3	2	2	2	2
SO	17	21	24	27	26	26
Ceramic PGA	0	0	0	0	1	1
Plastic PGA	1	1	1	1	1	1
Ball/Land Grid Array	0	0	0	0	0	0
Bare Die	9	11	15	18	21	25
Total	100	100	100	100	100	100

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

- Die can be mounted cavity down with a heat spreader attached to its back side for efficient heat transfer.
- Resonant frequency can be higher in a BGA.
- Average lead inductance can be reduced via wire bond length.

It was predicted at the Surface Mount International Conference 1992 that the BGA package would be the future package for high-density ICs. The new package technique reportedly had no coplanarity problems and that solder-grid arrays work with standard solder-reflow techniques.* Market acceptance of this new technology over the proven success of the QFP

Table 2-3
Estimated Japanese Package Forecast (Millions of Units)

Package	1992	1993	1994	1995	1996	1997
Plastic DIP	1,700	820	802	702	602	300
Ceramic DIP	488	388	306	215	188	155
Quad	2,817	3,054	3,625	3,700	4,049	4,558
Ceramic Chip Carrier	15	21	19	14	10	9
Plastic Chip Carrier	55	62	54	32	27	20
SO	4,705	4,980	5,304	5,479	5,687	5,940
Ceramic PGA	70	80	85	88	80	70
Plastic PGA	60	55	50	50	45	40
Ball/Land Grid Array	0	0	1	3	11	29
Bare Die	2,310	2,450	2,755	3,000	3,450	3,700
Total	12,220	11,910	13,001	13,283	14,149	14,821
Percentage of Total*						
Plastic DIP	14	7	6	5	4	2
Ceramic DIP	4	3	2	2	1	1
Quad	23	26	28	28	29	31
Ceramic Chip Carrier	0	0	0	0	0	0
Plastic Chip Carrier	0	1	0	0	0	0
SO	38	42	41	41	40	40
Ceramic PGA	1	1	1	1	1	0
Plastic PGA	0	0	0	0	0	0
Ball/Land Grid Array	0	0	0	0	0	0
Bare Die	19	21	21	23	24	25
Total	100	100	100	100	100	100

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

*T. Costlow, *Electronic Engineering Times*, September 7, 1992, No. 709, p. 8(1)

designs will only be decided on by availability, proven cost efficiencies, and successful marketing of the sponsors.

Although IBM could be a major contender in the worldwide production and shipment of DRAMs to the merchant market, Japan is expected to remain the dominant producer and consumer of memory devices. This demand will continue to fuel the growth of TSOP and emerging package options through the end of the decade. Although SO and quad packages represent the volume share of package production in Japan (see Table 2-3), bare die consumption for chip on board (COB) and emerging MCM designs will continue to be fairly strong. COB applications such as memory cards, printers, graphics, calculators, laptops, games systems, and hand-held communicators will be the largest consumer sectors for bare die, combinations of COB/TSOP, and MCM designs.

Table 2-4
Estimated European Package Forecast (Millions of Units)

Package	1992	1993	1994	1995	1996	1997
Plastic DIP	2,400	2,010	1,870	1,570	1,210	900
Ceramic DIP	475	441	399	300	287	231
Quad	1,386	1,751	2,200	2,689	3,400	4,300
Ceramic Chip Carrier	44	43	40	40	37	32
Plastic Chip Carrier	51	50	50	47	44	42
SO	2,656	2,990	3,444	3,673	3,745	3,800
Ceramic PGA	28	30	42	50	55	50
Plastic PGA	33	41	44	68	74	80
Ball/Land Grid Array	0	0	1	2	6	13
Bare Die	388	470	654	914	1,410	2,183
Total	7,461	7,826	8,744	9,353	10,268	11,631
Percentage of Total*						
Plastic DIP	32	25	21	17	12	8
Ceramic DIP	6	6	5	3	3	2
Quad	18	22	25	28	33	37
Ceramic Chip Carrier	1	1	0	0	0	0
Plastic Chip Carrier	1	1	1	0	0	0
SO	35	38	39	39	36	32
Ceramic PGA	1	1	1	1	1	1
Plastic PGA	0	1	0	1	1	1
Ball/Land Grid Array	0	0	0	0	0	0
Bare Die	5	6	7	10	14	19
Total	100	100	100	100	100	100

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Europe, much like Japan, enjoyed an earlier and beneficial shift to SMT than the U.S. manufacturers through its acceptance of the SO package. As shown in Table 2-4, SMT is now the dominant package in electronics in this region. Where we previously estimated that TH technology had a strong foothold in the transportation sector of Europe, automotive manufacturers in Europe are now reporting that 70 percent of the electronics used in engine management and ABS areas are now in SMT. During the last six months, there has also been a significant shift from hybrid technology to QFP and MCM designs in QFPs for use in the communications applications.

The Asia/Pacific region will continue to cater to the low-pin-count package applications through the end of 1993 (see Table 2-5). We expect a gradual shift to occur after this time frame as the Korean manufacturers begin their expected ramp to higher-pin-count ASIC devices in QFPs. Korean manufacturers of memory devices now account for a major portion of TSOPs for DRAMs on SIMMs and add-in boards.

Table 2-5
Estimated Asia/Pacific Package Forecast (Millions of Units)

Package	1992	1993	1994	1995	1996	1997
Plastic DIP	1,814	1,411	1,100	789	500	403
Ceramic DIP	102	78	48	32	28	26
Quad	1,321	2,549	3,560	4,233	5,300	6,122
Ceramic Chip Carrier	1	1	1	1	1	1
Plastic Chip Carrier	54	57	50	63	55	34
SO	4,926	5,466	5,500	5,366	5,400	5,741
Ceramic PGA	7	10	12	12	14	11
Plastic PGA	5	9	12	12	14	15
Bare Chip	233	345	446	526	920	1,722
Total	8,463	9,926	10,729	11,034	12,232	14,075
Percentage of Total						
Plastic DIP	21	14	10	7	4	3
Ceramic DIP	1	1	0	0	0	0
Quad	16	26	33	38	43	43
Ceramic Chip Carrier	0	0	0	0	0	0
Plastic Chip Carrier	1	1	0	1	0	0
SO	58	55	51	49	44	41
Ceramic PGA	0	0	0	0	0	0
Plastic PGA	0	0	0	0	0	0
Bare Chip	3	3	4	5	8	12
Total	100	100	100	100	100	100

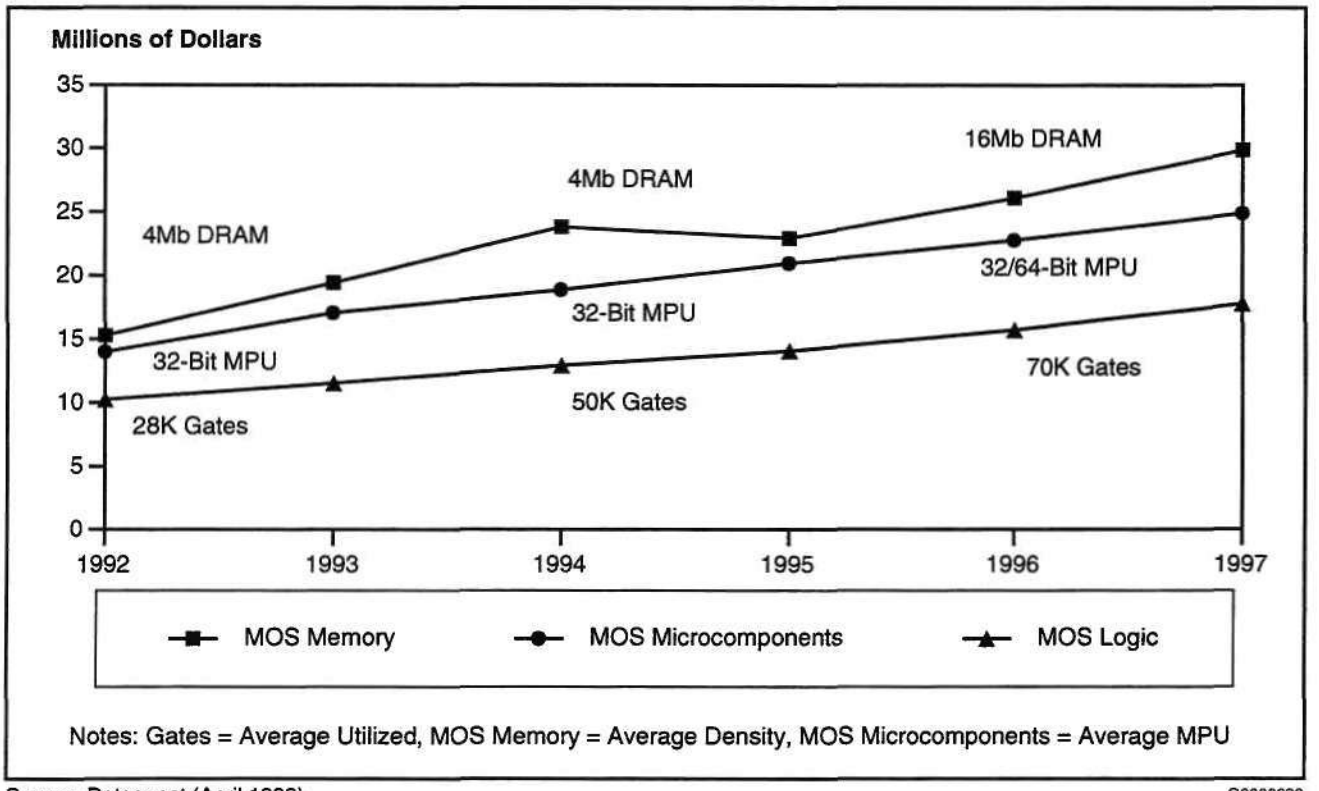
Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Chapter 3
Component Interconnect

MOS digital products represent the largest revenue base for the semiconductor industry (see Figure 3-1) and are also the component drivers for the majority of new smaller/thinner fine- and ultrafine-pitch packages. In 1992, an estimated 80 percent of all circuit boards were manufactured with substantial digital content.* As users anticipate migrating to advanced packaging technologies for memories, ASICs, and microprocessors, a high mix of ultrafine pitch (0.012 to 0.004 inch) processes, BGA, and various high-density interconnect and MCM options are expected to develop. High-density, high-pin-count gate arrays have already pushed pin pitch on QFP designs from 0.65mm to 0.3mm in the TQFP design.

Although the pin-out of memory chips increases only slowly as the number of bits on a chip increases, the package variation is entering its fifth generation of development. Starting with the family of DIPs, memory products, especially DRAMs, have influenced the birth of the SIP, ZIP, SOP/SOJ, and TSOP II, with a potentially new lead-on-chip

Figure 3-1
MOS Digital Forecast, Share by Technology



Source: Dataquest (April 1993)

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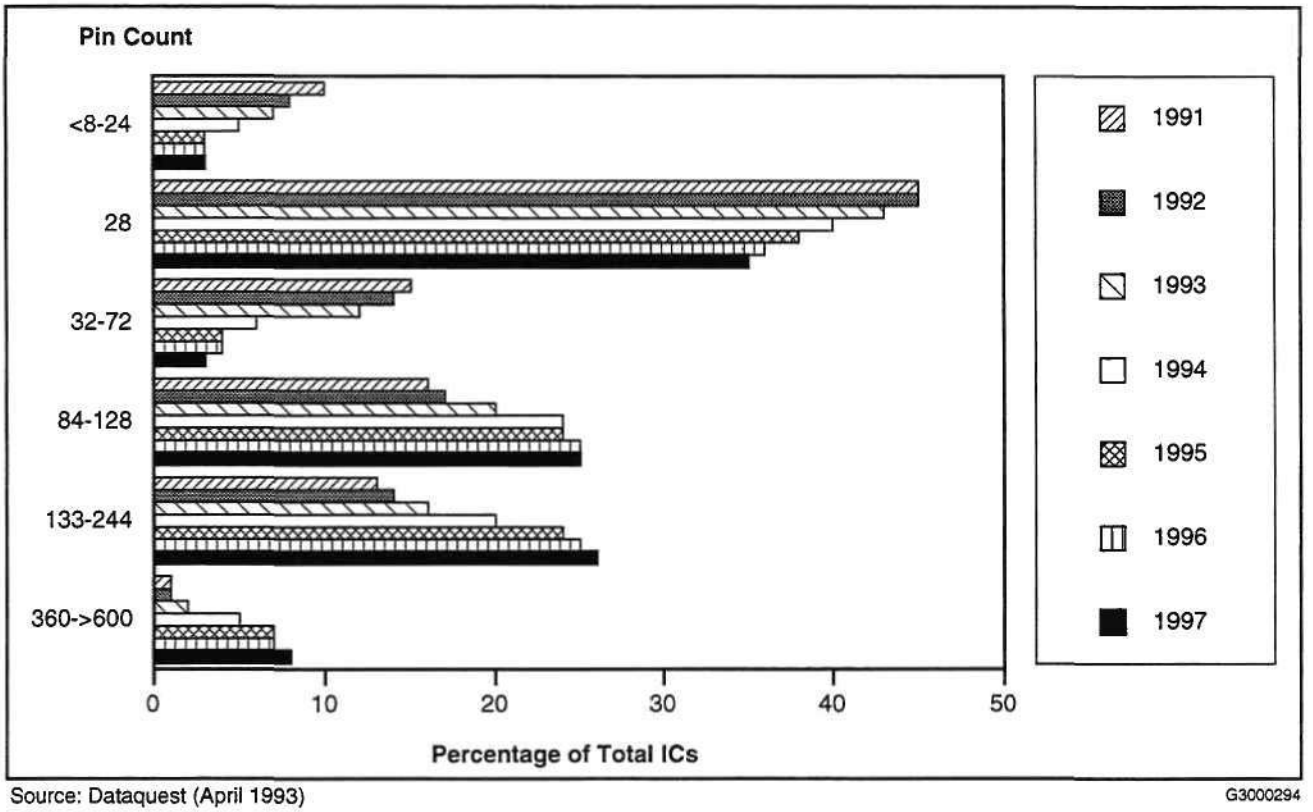
*D.P. Kjosness, "A Manufacturing-Oriented Digital Stimulus/Response Test Instrument," *Hewlett-Packard Journal*, April 1992, Vol. 43, No. 2, p. 39

(LOC) package looming on the horizon. Although 256Mb DRAMs are expected to be in production by the end of the decade, a doubling of the bit capacity will require only one extra address pin. If a memory device has 28 pins, one twice as large would require only 29 pins, representing a pin count increase of only 3 percent as the memory size doubles.

By contrast, the pin count of logic devices follows the rule that the number of pins required is about proportional to the square root of the number of gates. Thus, if the number of gates were to double, the pin count would need to increase by about 40 percent. This relationship is known as Rent's Rule—depending on the system architecture, the pin count can be proportional to the number of gates raised to a power somewhat greater or lesser than the square root. Regardless, the number of pins on a logic chip will increase much more rapidly with chip complexity than the number of pins on a memory chip.

Figure 3-2 shows the strong influence of memory devices on the 28-pin-count growth. Chip complexity increases every two years, but the 28-pin package for memory devices maintains the largest share by pin count through time. Through time, gate arrays, microprocessors, and embedded controllers driving the above-128-pin-count growth will be accommodated in either single-chip QFPs with pins on the periphery of the package or in grid array packages with pins or pads on the bottom of the packages.

Figure 3-2
Worldwide IC Package, by Pin Count (Percentage)



Source: Dataquest (April 1993)

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Memory Packaging

Traditionally, memory chips have been mounted side by side on a PCB. As the system demand for memory increased, the need to package chips as close together as possible promoted chip aspect ratios that declined from 400 and 600 mils to 300-mil package widths, multiple die on memory modules, and add-in memory boards for 40MB to 100MB memory expansion. Table 3-1 shows DRAM package development through time. Table 3-2 lists the DRAM development by module organization, and Table 3-3 forecasts the estimated development of emerging DRAM package technologies. Two of the most innovative DRAM packages will be the stackable memory and the LOC/COL packages.

An example of the stackable memory module is that produced by Irvine Sensors of Costa Mesa, California. Irvine Sensor's product is a thin package of stacked memory chips connected at the top by a "cap chip" that allows a variety of conventional manufacturing techniques such as wire bonding, tape automated bonding, or solder bumps to be used to interconnect the stack with higher levels of assembly. The LOC package shown in Figure 3-3 was patented by IBM. The LOC package is designed to effectively dissipate heat and improve the performance of higher-density devices. The packaged chip has a plurality of lead frame conductors extending through the encapsulating material, which are adhesively joined to the chip. The conductors cover a substantial portion of the chip and thereby serve as conduits for dissipation of heat from the chip. Wires are bonded to the conductors and extend from the conductors to the terminals of the chip. The chip terminals are designed along the center line of the chip, allowing for short connecting wires that in turn contribute to faster chip response (IBM Patent 4,862,245, 1989). The chip-on-lead (COL) technique does away with the die pad and runs the leads directly under the chip. This reduces chip-to-lead spacing by eliminating the space required by the conventional package between the die pad and the inner lead.

Tables 3-4 and 3-5 list the package data for the fast and slow SRAM products. The vast majority of SRAMs greater than 45ns are used in cache applications where standby power would only be used when either a noncached address was being accessed (probably less than 1 percent of all processor cycles), or when the system is powered down (which is addressed in some designs by clearing the cache and removing power from the cache chip completely).*

The majority of high-speed, less-than-70ns SRAMs are being packaged in the new SOJ/TSOP II designs for single-chip or multiple-chip SRAM module designs. AT&T Microelectronics has introduced a selection of high-speed SRAM SIMM and ZIP modules of x8, x32, x36, and x40 widths for 2MB to 8MB storage capacity.

* Jim Handy, *DQ Monday*, January 11, 1992, p. 3

Table 3-1
Estimated Worldwide MOS DRAM Package Forecast (Millions of Units)

	Units	1992	1993	1994	1995	1996	1997
256Kb DRAM		190.00	125.00	85.00	41.00	21.00	10.00
	DIP	130.15	81.88	51.85	20.50	7.46	2.50
	ZIP	23.75	16.25	11.48	5.33	2.63	1.20
	PLCC	27.55	19.38	13.60	9.02	6.30	4.30
	Others	6.65	6.25	7.23	5.74	4.41	1.90
	Die	1.90	1.25	0.85	0.41	0.21	0.10
	SIP/SIMM	13.78	9.69	6.80	4.51	3.15	2.15
1Mb DRAM		750.00	450.00	250.00	115.00	87.00	50.00
	DIP	70.50	35.55	8.00	0	0	0
	ZIP	105.75	60.75	31.75	13.92	10.44	5.50
	SOJ/SOP	547.50	337.50	200.00	95.91	72.21	42.00
	Others	11.25	5.85	2.75	1.15	0.87	0.50
	Die	15.00	10.35	7.50	4.03	3.48	2.00
	SIP/SIMM	328.50	219.38	130.00	62.34	46.94	27.30
4Mb DRAM		435.00	815.00	925.00	670.00	460.00	300.00
	DIP	4.35	0	0	0	0	0
	ZIP	47.85	64.39	69.38	46.90	32.20	21.00
	SOJ/SOP	361.05	712.31	814.00	589.60	402.50	261.00
	Others	17.40	28.53	27.75	20.10	13.80	9.00
	Die	4.35	9.78	13.88	13.40	11.50	9.00
	SIP/SIMM	216.63	463.00	529.10	412.72	281.75	195.75
16Mb DRAM		2.80	35.00	185.00	330.00	585.00	1,050.00
	DIP	0	0	0	0	0	0
	ZIP	0	0	0	0	0	0
	SOJ/SOP	2.21	27.13	134.13	237.60	391.95	697.20
	Others	0.56	7.18	46.25	82.50	175.50	315.00
	Die	0.03	0.70	4.63	9.90	17.55	37.80
	SIP/SIMM	0.44	13.56	80.48	142.56	254.77	453.18
64Mb DRAM		0	0	0	0	3.00	25.00
	DIP	0	0	0	0	0	0
	ZIP	0	0	0	0	0	0
	SOJ/SOP	0	0	0	0	2.67	20.98
	Others	0	0	0	0	0.30	3.75
	Die	0	0	0	0	0.03	0.28
	SIP/SIMM	0	0	0	0	1.74	14.68
256Mb DRAM		0	0	0	0	0	0
	DIP	0	0	0	0	0	0
	ZIP	0	0	0	0	0	0
	SOJ/SOP	0	0	0	0	0	0
	Others	0	0	0	0	0	0
	Die	0	0	0	0	0	0
	SIP/SIMM	0	0	0	0	0	0

Source: Dataquest (April 1993)

Table 3-2
Estimated Worldwide MOS DRAM Module Organization Forecast (Millions of Units)

		1992	1993	1994	1995	1996	1997
256Kb DRAM							
	SIP/SIMM	13.78	9.69	6.80	4.51	3.15	2.15
	x8	2.76	1.74	1.09	0.68	0.47	0.32
	x9	11.02	7.94	5.71	3.83	2.68	1.83
	x32						
	x36						
	x40						
1Mb DRAM							
	SIP/SIMM	328.50	219.38	130.00	62.34	46.94	27.30
	x8	124.83	76.78	39.00	18.70	14.08	8.19
	x9	180.68	127.24	81.90	39.28	29.57	17.20
	x32	3.29	2.19	1.30	0.62	0.47	0.27
	x36	13.14	8.78	5.20	2.49	1.88	1.09
	x40	6.57	4.39	2.60	1.25	0.94	0.55
4Mb DRAM							
	SIP/SIMM	216.63	463.00	529.10	412.72	281.75	195.75
	x8	32.49	69.45	79.37	61.91	42.26	29.36
	x9	151.64	314.84	343.92	255.89	169.05	117.45
	x32	2.17	4.63	5.29	4.13	2.82	1.96
	x36	19.50	50.93	68.78	61.91	45.08	31.32
	x40	10.83	23.15	31.75	28.89	22.54	15.66
16Mb DRAM							
	SIP/SIMM	0.44	13.56	80.48	142.56	254.77	453.18
	x8	0.18	5.43	31.39	54.17	91.72	163.14
	x9	0.24	7.87	45.87	79.83	135.03	235.65
	x32	0	0	0.80	1.43	2.55	4.53
	x36	0.02	0.27	2.41	7.13	25.48	49.85
	x40	0	0	0	0	0	0
64Mb DRAM							
	SIP/SIMM	0	0	0	0	1.74	14.68
	x8					0.52	4.85
	x9					0.61	5.14
	x32					0.03	0.29
	x36					0.09	0.73
	x40					0.43	3.67
256Mb DRAM							
	SIP/SIMM	0	0	0	0	0	0
	x8						
	x9						
	x32						
	x36						
	x40						

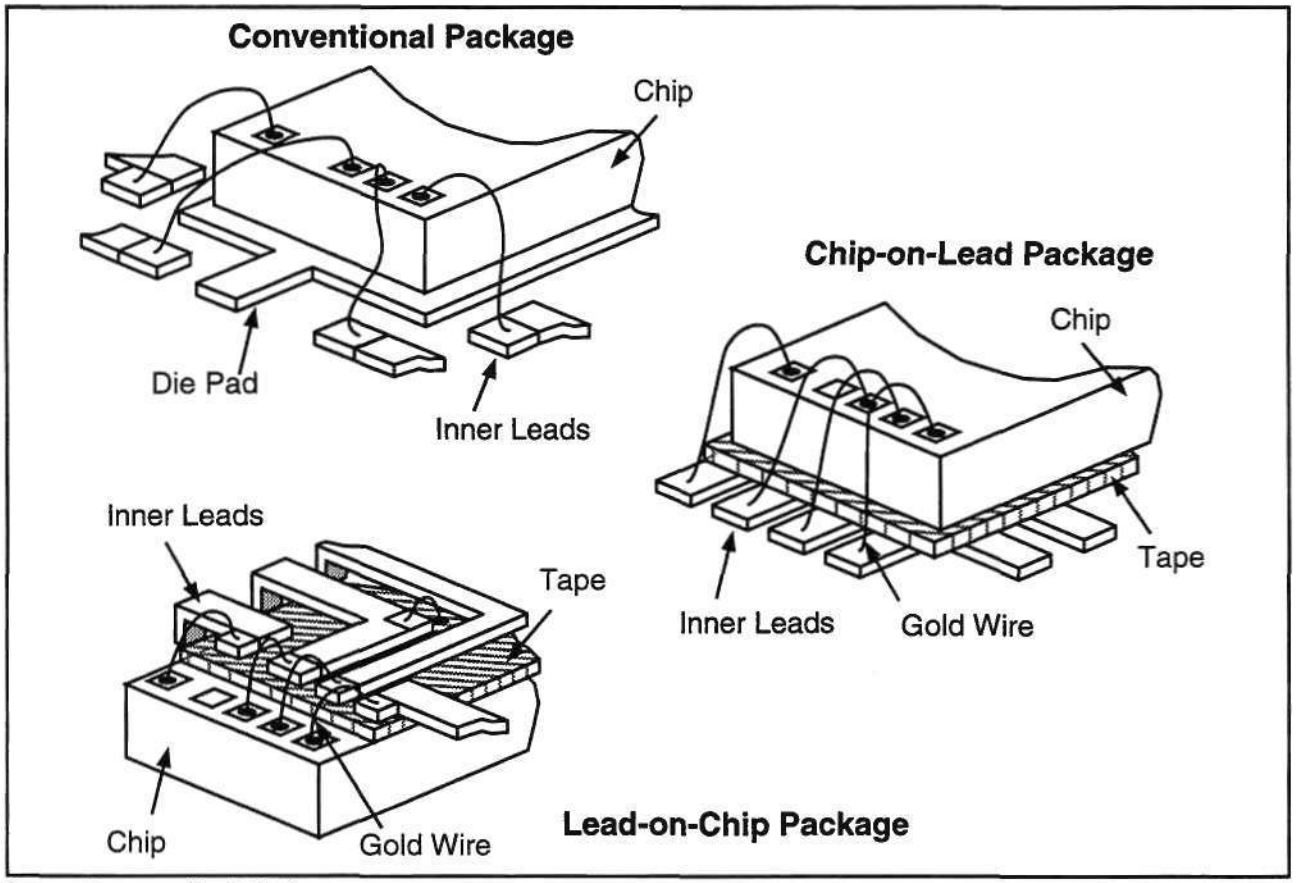
Source: Dataquest (April 1993)

Table 3-3
MOS DRAM Emerging Package Technologies Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
SO	910.76	1,076.94	1,148.13	923.11	869.33	1,021.18
SOJ	728.61	753.85	688.88	369.24	347.73	306.35
TSOP	182.15	323.08	459.25	553.87	608.53	714.82
Others	35.86	47.80	83.98	109.49	194.88	330.15
Lead on Chip	5.38	9.56	20.99	32.85	77.95	165.08
TAB	0.72	0.96	2.52	3.28	5.85	9.90
Stacked Lead on Chip	0.36	0.96	4.20	5.47	13.64	23.11
Die	21.28	22.08	26.85	27.74	32.77	49.18

Source: Dataquest (April 1993)

Figure 3-3
Conventional and Advanced Memory Packaging



Source: Dataquest (April 1993) G2000656

Table 3-4
Estimated Worldwide Slow (>70ns) SRAM Package Forecast (Millions of Units)

		1992	1993	1994	1995	1996
16Kb						
	DIP	11	6	3	1	0
	SOG/SOP	11	7	5	3	2
	Bare Die	0	0	0	0	0
	Total	22	13	8	4	2
64Kb						
	DIP	49	11	7	3	1
	SOG/SOP	108	27	22	11	7
	Bare Die	2	0	1	0	0
	Total	159	38	29	14	8
256Kb						
	DIP	47	32	8	1	0
	SOG/SOP	153	162	81	37	38
	Bare Die	4	8	6	5	4
	Total	204	203	95	43	43
1Mb						
	DIP	10	14	11	2	0
	SOG/SOP	48	100	103	85	124
	Bare Die	2	6	10	15	12
	Total	60	120	124	103	149
4Mb						
	DIP	0	0	0	0	0
	SOG/SOP	0	8	30	45	61
	Bare Die	0	1	8	15	26
	Total	0	10	38	60	88

Notes: Pseudo-static RAMs are not included at the 1Mb and 4Mb densities.
Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Tables 3-6 through 3-9 summarize the package trend data for the EPROM, ROM, EEPROM, and flash families. Most notable of all changes seen in the nonvolatile product families is the general shift to TSOP designs. Nonvolatile products, specifically EPROM and EEPROM, traditionally were encapsulated in ceramic packages for hermeticity and UV window design. Both low- and high-density EEPROMs for consumer applications are driving demand for plastic TSOP packages. Flash products are commanding a stronger percentage of TSOP designs for solid-state mass storage. Flash displacement of EPROM/OTP in new memory card and board designs is signaling the expansion of nonvolatile memory beyond the single-chip 1Mb-to-4Mb designs.

Table 3-5
Estimated Worldwide Fast (<70ns) SRAM Package Forecast (Millions of Units)

		1992	1993	1994	1995	1996
16Kb						
	DIP	11	7	5	4	3
	CLCC	1	1	0	0	0
	Bare Die	1	1	1	0	0
	Total	14	8	6	5	3
64Kb						
	DIP	27	18	10	3	1
	CLCC	2	1	1	0	0
	SOJ	31	25	21	14	9
	Bare Die	22	22	20	10	6
	Total	82	67	52	27	16
256Kb						
	DIP	42	39	56	33	19
	SOJ	60	82	134	97	95
	Bare Die	18	24	42	34	20
	Total	119	145	232	164	134
1Mb						
	DIP	7	12	17	38	29
	SOJ	13	28	48	150	194
	Bare Die	4	9	16	50	67
	Total	24	50	80	238	290
4Mb						
	DIP	0	1	1	3	4
	SOJ	0	3	7	31	60
	Bare Die	0	1	2	14	36
	Total	0	4	11	48	99

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Logic Packaging

With the advent of CMOS technology and system demand for high-speed data flow, users found it impractical to use only lower levels of SSI (less than 12 gates) and MSI (12 to 100 gates) devices (see Table 3-10). The standard logic families represented the earliest shift to SMT after analog. For the logic designer, the shift to SMT also opened the doors to higher-gate-count packaging. Tables 3-11 and 3-12 provide the actual and estimated pin count and package trends by percentage of design starts for gate arrays. The actual data and forecast have been collected from gate array suppliers surveyed for package design start data since 1990. The majority of gate array designs were accomplished with 1.0µm technology, and gate counts averaged 28,000 in North America and 18,000 in

Table 3-6
Estimated Worldwide MOS EPROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide Total	423	463	458	458	441	404
Package Total	423	463	458	458	441	404
DIP	317	326	309	288	270	248
Chip Carrier	80	87	87	85	81	74
SO	19	37	41	53	51	47
TSOP	6	13	22	32	40	36
Total by Pin Count	423	463	458	458	441	404
24-Pin	12	9	5	2	0	0
28-Pin	375	410	406	403	390	357
32-Pin	21	23	23	23	22	20
40-Pin	4	9	14	18	18	16
44-Pin	10	12	11	11	11	10

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Table 3-7
Estimated Worldwide MOS ROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide	367	370	319	277	255	240
Package Type	367	370	319	277	255	240
DIP	45	26	12	5	3	1
SO	268	266	224	191	170	168
Quad	0	0	0	0	0	0
Bare Die	54	77	83	80	83	71
Pin Count	367	370	319	269	255	230
24-Pin	0	0	0	0	0	0
28-Pin	256	238	168	123	110	98
32-Pin	55	52	64	61	55	52
40-Pin	1	2	3	3	5	6
44-Pin	1	1	1	2	3	4
Bare Die	54	77	83	80	83	71

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Table 3-8
Estimated Worldwide MOS EEPROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide Total	282	350	423	471	524	641
Package Type	282	350	423	471	524	641
DIP	65	49	35	23	10	6
Chip Carrier	52	57	63	59	44	36
SO	146	220	296	353	424	534
PGA	0	0	0	0	0	0
Bare Die	19	24	29	36	45	65
Pin Count	282	350	423	471	524	641
8-Pin	155	214	280	309	331	373
14-Pin	29	37	35	33	30	30
24-Pin	38	31	28	26	24	22
28-Pin	34	35	42	59	86	144
32-Pin	7	9	9	8	8	7
Bare Die	19	24	29	36	45	65

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Table 3-9
Estimated Worldwide Flash Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide Total	33	77	163	269	350	370
Package Total	33	77	163	269	350	370
DIP	28	60	105	139	118	88
Chip Carrier	1	3	7	9	10	13
SO	1	4	9	13	24	33
TSOP	2	10	38	98	173	200
COB	0	1	4	10	24	37
Pin Count	33	77	163	269	350	370
28-Pin	7	15	20	20	14	10
32-Pin	26	62	139	239	312	323
Bare Die	0	1	4	10	24	37

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Table 3-10
Estimated Worldwide Standard Logic Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide Total	3,740	3,924	4,046	4,118	4,202	4,164
DIP	303	248	237	233	229	221
Plastic	186	155	148	143	140	133
Ceramic	99	79	77	77	76	74
Side Brazed	18	14	13	14	14	13
Flatpack	38	37	36	36	36	35
Ceramic	35	33	33	33	32	32
Side Brazed	4	3	3	3	3	3
Chip Carrier	63	82	102	129	166	212
Plastic	5	5	5	5	5	5
Ceramic	58	76	96	124	161	207
SO	2,736	2,922	3,037	3,103	3,173	3,150
Quad/SQFP	600	636	634	615	597	545
CMOS	709	721	737	744	742	728
DIP	3	3	3	3	3	3
Plastic	2	2	2	2	2	2
Ceramic	1	1	1	1	1	1
Side Brazed	0	0	0	0	0	0
Flatpack	4	4	4	4	4	4
Ceramic	3	4	4	4	4	4
Side Brazed	0	0	0	0	0	0
Chip Carrier	2	2	2	2	2	2
Plastic	1	1	1	1	1	1
Ceramic	1	1	1	1	1	1
SO	701	712	728	734	733	719
Bipolar	1,308	1,277	1,246	1,237	1,239	1,213
DIP	299	244	234	230	226	218
Plastic	183	153	145	140	137	131
Ceramic	98	78	76	76	75	74
Side Brazed	18	13	13	13	13	13
Flatpack	35	33	32	32	31	31
Ceramic	31	29	29	29	28	27
Side Brazed	3	3	3	3	3	3
Chip Carrier	9	9	9	9	10	10
Plastic	4	4	4	4	4	4
Ceramic	5	5	5	5	5	5
SO	965	991	971	966	972	954

(Continued)

Table 3-10 (Continued)
Estimated Worldwide Standard Logic Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
BICMOS	111	197	298	399	514	604
DIP	1	1	0	0	0	0
Plastic	1	1	0	0	0	0
Ceramic	0	0	0	0	0	0
Side Brazed	0	0	0	0	0	0
Flatpack	0	0	0	0	0	0
Ceramic	0	0	0	0	0	0
Side Brazed	0	0	0	0	0	0
Chip Carrier	0	0	0	0	0	0
Plastic	0	0	0	0	0	0
Ceramic	0	0	0	0	0	0
SO	110	193	294	393	507	596
Quad/SQFP	1	2	4	6	8	9
GaAs	52	71	91	119	156	201
DIP	0	0	0	0	0	0
Plastic	0	0	0	0	0	0
Ceramic	0	0	0	0	0	0
Side Brazed	0	0	0	0	0	0
Flatpack	0	0	0	1	1	1
Ceramic	0	0	0	1	1	1
Side Brazed	0	0	0	0	0	0
Chip Carrier	52	70	90	118	155	200
Plastic	0	0	0	0	0	0
Ceramic	52	70	90	118	155	200
SO	0	0	0	0	0	0
Other MOS	1,560	1,659	1,673	1,619	1,551	1,418
SO	961	1,026	1,043	1,010	962	882
Quad/SQFP	599	633	630	609	589	536

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Japan in 1992. However, performance-driven RISC/CISC-based systems with higher operating frequencies drove increased demand for complex embedded arrays with up to 600,000 gates and I/O greater than 800, based on 0.60µm (drawn; 0.45µm effective) technology. The majority of complex high-I/O gate arrays are encapsulated in QFP and ceramic PGA packages incorporating wire bond, TAB, and flip TAB attachment methods. Table 3-13 shows the various interconnect parameters and the trade-offs associated with these attachment methods.

Table 3-11
Estimated Worldwide Gate Array Design Starts, by Package Type (Percentage)

Worldwide Total	1992	1993	1994	1995	1996	1997
Technology	100	100	100	100	100	100
MOS	70	72	73	73	72	72
Bipolar	25	21	18	14	11	9
BICMOS	6	7	9	13	16	20
Package Type	100	100	100	100	100	100
DIP	6	1	0	0	0	0
Quad	59	65	67	68	67	65
Chip Carrier	13	8	5	3	2	1
PGA	20	20	20	17	15	13
Ball/Land Grid Array	0	1	2	3	4	6
MCM	1	2	4	5	8	9
COB	1	1	2	3	4	5
Others	0	0	0	1	1	1

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Table 3-12
Estimated Worldwide Gate Array Design Starts, by Pin Count (Percentage)

	1992	1993	1994	1995	1996	1997
Pin Count						
<44	3	1	1	0	0	0
44-83	16	7	3	1	0	0
84-132	16	13	11	9	7	5
133-195	31	36	36	33	30	27
196-244	22	25	28	30	32	33
244-360	8	10	12	15	16	17
361-524	3	7	9	10	12	14
525-600	0	0	1	2	2	3
>600	0	0	0	1	1	2
Total	100	100	100	100	100	100

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

The die bond pads for wire bond, TAB, flip TAB, flip chip, or MCM perform the role of a "space transformer." They provide the interface between the dense metal lines on the chip and the much less dense metal lines on the PCB or high-density substrates, such as MCM, to which the chips will be attached. Vendors of I/O-intensive gate array designs are resorting to staggered I/O pads for greater gate utilization, silicon efficiency, reduced die area, and decreased capacitance.

Table 3-13
Comparison of Interconnect Technologies

	Wire Bonding	TAB	Flip-TAB	Flip Chip	MCM/HDI
Attribute					
Minimum Die I/O Pitch (Mils)	4 to 7	3 to 4	3 to 4	10 to 15	1 to 2
Maximum I/O Count	300 to 500	500 to 700	500 to 700	More than 700	More than 700
Lead Inductance (nH)	1 to 2	1	0.1	0.05 to 0.1	Less than 0.05
Mutual Inductance between Leads (pH)	100	5	5	1	Less than 1
Qualitative Attributes					
Area Array Potential	Difficult/Possible Multi-Height Loops	Moderately Difficult, Multilayer Tape	Moderately Difficult, Multilayer Tape	Yes	Yes
Package Efficiency	Medium	Medium	Medium	High	High
Pretestability in Fine Pitch	Difficult	Good	Good	Difficult	Difficult
Loop Control	Fair	Good	Good	Good	Good
Manufacturing Process Flexibility	Excellent	Poor/Gang Bonding Good/Single Point Bonding	Poor/Gang Bonding Good/Single Point Bonding	Poor	Good
Die Availability	Excellent	Fair	Fair	Poor	Excellent
Tool Availability	Excellent	Fair	Fair	Fair	Fair

(Continued)

Table 3-13 (Continued)
Comparison of Interconnect Technologies

Attribute	Wire Bonding	TAB	Flip-TAB	Flip Chip	MCM/HDI
General Information					
Technology Maturity	Excellent	Fair	Fair	Good	Fair
Market Share, by Technology (%)	98	Less than 2	Less than 1	Less than 1	Less than 1
Dominant Failure Mechanisms	Fatigue, Bond Pad Erosion	Lead Fatigue, Interdiffusion	Lead Fatigue, Interdiffusion	Solder Joint Fatigue	Electro-migration Corrosion
Manufacturing Process Complexity	Low	Medium	Medium	High	Medium
Heat Dissipation	Good (Die Bonded to Substrate)	Good (Die Bonded to Substrate)	Poor (Die Not Bonded to Substrate) Excellent (Back-Side Attach to Heatsink)	Poor (Die Not Bonded to Substrate) Excellent (Back-Side Attach to Heatsink)	Good (Die Bonded to Substrate)
Reworkability	Difficult	Fair	Good	Good	Good
Cost	Low	Medium	Medium	High (Potentially Low)	High (Potentially Low)

Source: CALCE Electronic Packaging Research, University of Maryland

Microprocessors

Table 3-14 contains the microprocessor forecast for package production and pin count. Figure 3-4 shows the activity level by microprocessor type.

In the performance arena, high-end microprocessor performance levels have been doubling every 12 to 18 months.* For the HP9000 series 700 workstation, the CPU contains 577,000 transistors with a 640,000-transistor floating point coprocessor and a memory and I/O controller with 185,000 transistors. The CPU was packaged in a 408-pin CPGA. The CPGA contains multiple power and ground planes to reduce inductance and maintain high-speed switching of more than 200 outputs. Power supply bypass capacitors are used on the package substrate to minimize switching noise. Hewlett-Packard's high-frequency package design integrates both function and scaling that did not push the limits of the chip density or speed, proving that there is no advantage in speed if the power cannot be dissipated. This CPU design achieves speed in excess of 66 MHz with power dissipation of 8W.

The new MIPS 64-bit R4400 introduced in November 1992 was designed for high-performance computer, network server, and fault-tolerant systems. Designed with a 0.6µm process with a 75-MHz external clock speed, the R4400 contains 2.3 million transistors and is available in 3.3V

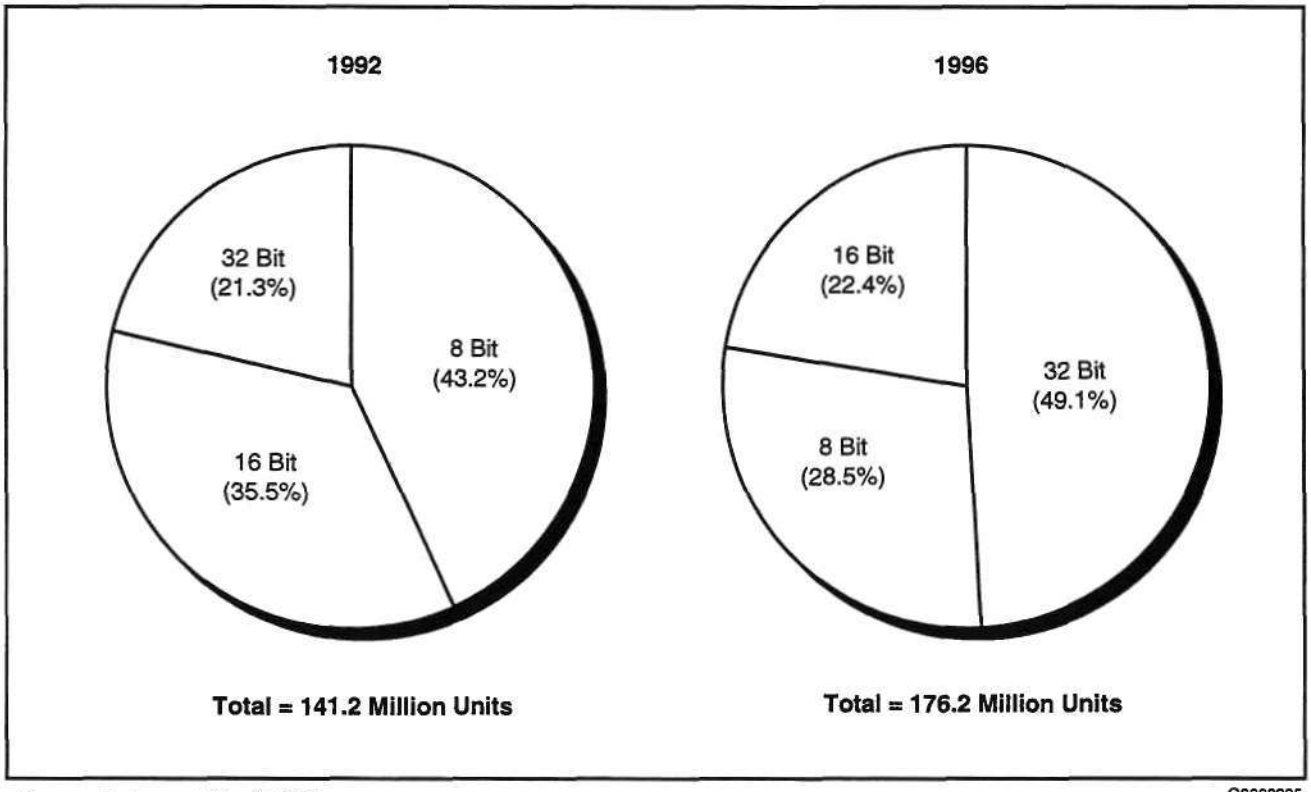
Table 3-14
Estimated Worldwide Microprocessor Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide Total	141.2	154.2	158.3	165.4	176.2	192.8
Package Total	141.2	154.2	158.3	165.4	176.2	192.8
DIP	8.0	4.0	2.4	1.0	0.3	0
Quad	5.4	6.6	6.9	10.0	9.1	9.8
Chip Carrier	22.1	17.1	13.0	8.1	4.8	1.4
PGA	103.7	122.0	125.6	119.4	118.7	104.0
Ball/Land Grid Array	0.1	0.8	3.0	7.0	11.0	21.0
Bare Die	1.9	3.7	7.4	19.9	32.3	56.6
Pin Count						
40-48	8.1	4.1	2.4	1.0	0.3	0
52-68	54.6	41.5	26.3	13.3	7.4	2.4
72-84	38.5	42.7	35.9	29.7	23.4	15.1
114-128	22.0	27.4	34.1	38.1	33.8	30.0
132-175	12.0	20.0	25.1	28.0	33.0	35.0
More than 179	2.0	7.0	14.0	18.4	25.0	29.0

Source: Dataquest (April 1993)

*C.A. Gleason et al., "VLSI Circuits for Low-End and Midrange PA-RISC Computers," *Hewlett-Packard Journal*, August 1992, Vol. 43, No. 4, p. 12

Figure 3-4
Worldwide Market Share of Microprocessor, by Product Type



Source: Dataquest (April 1993)

G3000295

and 5V versions. With secondary cache, the device is available in 447-pin CPGAs. The R4000 device introduced in 1991 contained 1.3 million transistors and generated 10W of power.

Although the 8-bit and 16-bit microprocessors dominated the less-than-72-pin package market through 1992, a gradual shift from 128-pin and 179-pin for 16/32-bit architectures to 200-to-400-pin PGAs, QFPs, and BGAs has begun as users quickly shift to full 32-bit and new 64-bit architectures.

Analog

Linear and mixed-signal circuits continue to represent a growing segment of the semiconductor market. A large portion of this growth is driven by microcontroller usage in the consumer and automotive segments. The analog product was the earliest to adapt to SMT. In 1991 and through the end of 1992, demand for SM devices outstripped supply in almost all regions. The linear and mixed-signal products are expected to experience increased growth from compact disc, automotive engine control, air-bag systems, antilock brake systems, graphics workstations, electronic test equipment, and data acquisition systems. Mixed-signal designs have also been targeted for MCM designs that will begin to appear in the merchant market in late 1993 and early 1994. Table 3-15 lists the pin count and package forecast for the analog products.

Table 3-15
Estimated Worldwide Analog Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Worldwide						
Mixed-Signal	2,800	3,300	3,900	4,500	5,200	5,900
Linear	12,700	14,100	15,700	17,300	18,800	19,400
Total	15,500	17,400	19,600	21,800	24,000	25,300
Package Type						
Plastic DIP	3,026	2,653	1,978	1,588	1,289	1,067
Ceramic DIP	46	26	14	5	0	0
Quad	1,021	1,312	1,654	2,078	2,524	2,815
Plastic Chip Carrier	348	377	355	272	195	94
Ceramic Chip Carrier	4	0	0	0	0	0
SO	8,905	10,504	12,893	14,798	15,803	16,501
Others	671	788	806	753	689	564
Bare Die	1,480	1,740	1,900	2,306	3,500	4,258
Total	15,500	17,400	19,600	21,800	24,000	25,300
Pin Count						
<8-Pin	77	87	98	119	130	141
8-Pin	5,988	6,200	6,089	5,988	5,845	5,765
14-Pin	4,960	5,800	6,454	6,855	6,743	6,601
16-Pin	1,245	1,212	1,083	1,001	933	900
20-Pin	2,468	2,865	3,376	3,954	4,544	4,771
24-Pin	118	133	143	153	174	207
28-Pin	489	581	601	630	755	903
44-Pin	155	522	1,756	3,100	4,876	6,012

Note: Some columns do not add to totals shown because of rounding.
Source: Dataquest (April 1993)

Chapter 4
Emerging Package Technologies

Although device packaging continues to evolve at a rapid pace with major benefits to system performance, user resistance to change that plagued surface-mount acceptance in the early 1980s continues to plague designers of advanced interconnect techniques such as MCM, COB, chip on flex (COF), chip on glass (COG), as well as TAB and flip chip attach technology. A few of the hurdles to acceptance of these emerging technologies are as follows:

- Lack of standardization
- Investment in test and automated optical inspection (AOI) equipment
- Electrical, thermal, and mechanical requirements
- Known good die availability and test strategy

For many of the future portable electronic applications, users will need to go beyond the SMDs available today to attain the miniaturization and density that will be required for competing in the world of hand-held communications and computer devices. TAB technology offers many benefits in both semiconductor packaging and board-level assembly. As shown in Table 3-12, there are various trade-offs for selecting TAB as an interconnect method for die. COB technology, which has been available for many years, involves direct chip attach onto PWB using ultrasonic or thermocompression bonding. Encapsulation for physical protection usually is provided by applying a blob of epoxy that will spread over the chip and leads. COB packaging has also been used to interconnect an LCD panel. The advantage of COB in LCD applications is a reduction of the peripheral area of the display. Test of the ICs for defective die can be done by test of the COB module before it is connected to the LCD panel.

COF is a fairly new and unique subset of COB technology. Mitsubishi Electric Corporation designed and uses COF for packaging LCDs with TAB. Arrangement of up to 200 pins has been achieved, and the entire process from test through assembly can be accomplished via tape and reel. One trade-off with COF, according to SMOS (a company of Seiko Epson), is that it uses about the same amount of board space as a standard QFP. COF is reportedly being used for low-yielding die on boards too expensive to scrap. Compaq Computer Corporation is reportedly using the COF/TAB packaging in its latest portable computer. COG packaging has also been attempted by Mitsubishi in LCD panels. Although it has reported that COG can minimize connection pitch, the disadvantage is that it requires additional area for the ICs and bus lines, enlarging the peripheral area of the display.

Solder flip chip was developed by IBM in the 1960s and is a proven process for good die connection. Resin flip chip technology is still an emerging technology in the United States and Japan. During resin flip chip, gold bumps with a very fine pitch (1 to 3 mils) are put on the chip. The chip is flipped and connected to the substrate with resin. In some

processes, the resin is an anisotropic conductor, and in other cases the gold bumps make contact with the substrate by a combination of pressure and shrinkage of the resin.

Low-volume merchant market production of MCMs began in 1992, after being predominantly captive from the early 1980s. MCM designers have proven that, as an emerging package technology, compared to single-chip packaging, there are significant cost savings and performance improvements in MCM, depending on the system application and the design of the MCM.

The first JEDEC JC-11 MCM package standard announced in 1993 is the MCM CQFP, ceramic quad flatpack. The package standard offers the following:

- Four lead pitches (0.40, 0.50, 0.65, and 0.80mm)
- Six body sizes of 4mm increments (56, 60, 64, 80, 96, and 112mm)
- Square packages only
- Untrimmed, unformed leads
- Tie bar defined but style not specified

Table 4-1 shows the JEDEC MCM CQFP matrix.

Within the MCM domain, the largest investment and assembly of MCMs is being made by captive systems houses. For 1992, MCMs sold or consumed into captive equipment represented more than 95 percent of the total MCM revenue worldwide. The remaining 5 percent was distributed among MCM start-ups, subcontract assembly houses, and bare die distributors. Table 4-2 lists the MCM vendors and their services. The majority of the captive supply and demand was met by AT&T, IBM, MMS (Digital Equipment Corporation spin-off in June 1992), and Motorola. Most of the captive production was for MCM-C (ceramic) and MCM-D (deposited) configurations. Most of the subcontract assembly houses and bare die distributors catered to the low-end MCM-L products. Further analysis of the MCM market can be found in Dataquest's *Multichip Module* report, which was published in June 1992.

Table 4-1
JEDEC MCM CQFP Matrix

Body Size (mm)	Pitch (mm)	Lead Count
56	0.80	260
56	0.65	320
56	0.50	416
56	0.40	520
60	0.80	280
60	0.65	344
60	0.50	448
60	0.40	560
64	0.80	300
64	0.65	368
64	0.50	480
64	0.40	600
80	0.80	380
80	0.65	464
80	0.50	508
80	0.40	760
96	0.80	460
96	0.65	560
96	0.50	736
96	0.40	920
112	0.80	540
112	0.65	656
112	0.50	864
112	0.40	1,080

Source: JEDEC

Table 4-2
MCM Vendors

Vendor	Location
ACX Technologies	United States
ArcSys Inc.	United States
AT&T	United States
Boeing	United States
British Telecom	Europe
Bull	Europe
Carborundum/BP	United States
Chip Supply	United States
CNET	Europe
Cray	United States
Crosscheck	United States

(Continued)

Table 4-2 (Continued)
MCM Vendors

Vendor	Location
Dassault Electronique	Europe
DEC/MicroModule Systems	United States
Dow Chemical/Polycon	United States
Fujitsu	Japan
General Electric	United States
GEC-MRC	Europe
Harris	United States
Hewlett-Packard	United States
Hitachi	Japan
Honeywell	United States
Hughes	United States
Ibiden	Japan
IBM	United States
IMI	United States
Integrated System Assemblies	United States
Intergraph	United States
Irvine Sensors	United States
IST	United States
Kyocera	Japan
LSI Logic	United States
MCC	United States
MCNC	United States
MicroModule Systems	United States
nChip	United States
NEC	Japan
NTK	Japan
NTT	Japan
Quadrant	United States
Rockwell	United States
Shinko Electric Industries	Japan
Siemens	Europe
Silicon Connections	United States
SMI	Japan
Sumitomo Metal & Mining	Japan
Tektronix	United States
Texas Instruments	United States
Thorn-EMI	Europe
Toshiba	Japan
Unisys	United States
VLSI Technology	United States
W.R. Grace	United States
Z-Systems	United States

Source: Dataquest (April 1993)

Chapter 5
Subcontract Assembly Issues

Through the end of the 1980s, most single-chip IC assembly by subcontractors was concentrated in the area of DIP, although demand for SO, quad, and chip carrier packages was increasing. In that time frame subcontract assembly represented about 20 percent of total worldwide assembly capacity. Subcontract assembly tripled from 1985 through 1989 in the United States. This growth was attributed to semiconductor manufacturers who passed their business to onshore subcontractors to avoid the high cost of investment in upgrading their assembly lines, and systems companies that increased their demand for quick-turn custom designs. According to *Electronic Business*, the contract assembly industry attained more than $6 billion in revenue and grew 20 percent from 1990 through 1991; 10 to 15 percent annual growth is projected through the 1990s. Key services provided by contract assemblers can include the following:

- Printed circuit board design
- Component engineering and procurement
- Component preconditioning and testing
- Board assembly and testing
- System assembly and testing

Growth in the contract manufacturing industry in the 1990s is being fueled by three principal factors:

- The need for formerly large vertically integrated manufacturers such as Sun Microsystems, Hewlett-Packard, and Digital Equipment Corporation to reduce overhead such as purchasing, warehousing, receiving, inspection, cost accounting, logistics, excess, and attrition. This also allows the system vendor to focus on R&D, engineering, marketing, and sales.
- The needs of very small manufacturers with no resources for the immense capital equipment expenditure for assembly and component testing equipment. State-of-the-art pick-and-place and test equipment are now averaging more than $400,000 and $1 million respectively.
- Increasing miniaturization in system and board real estate is driving the need for capital-intensive investment in expensive automated testing and assembly equipment supporting fine-pitch designs. System vendors increasingly rely on contract manufacturers to debug new manufacturing processes.

The primary limiting factor to further growth of subcontract assembly in North America is increased competition from competitors in Southwest Asia, where there are still significant labor cost advantages and fewer environmental limiting bureaucracies. The fact that Solectron, one of the largest assemblers in North America, expanded operations in Malaysia in 1991 is testimony to this. Labor cost advantages for this region are

particularly well suited for "kitted" as opposed to "turnkey" system development, whereby the vendor supplies the manufacturing contractor with parts. Over the long term this labor advantage is expected to disappear as fine-pitch and ultrafine-pitch placements become more common.

The largest subcontract assemblers in North America are Avex Corporation, SCI Systems, and Solectron. Avex Corporation, headquartered in Huntsville, Alabama, posted $400 million in revenue for 1992, a record 50 percent increase in revenue over 1991. Avex expanded its subcontract business into Canada in 1992. Avex was formerly known as Avco Electronics. Avco Electronics had offered contract manufacturing and engineering services to the industry since 1955.

SCI Systems of Huntsville, Alabama, formed in 1961, recorded $800 million in sales in fiscal 1993's first six months, up 74 percent from $460 million in the first six months of sales in 1992. SCI's product division consists of the connector and packaging business, while the systems division supports the manufacturing control systems and peripherals business. SCI established a new manufacturing facility in Quebec, Canada to offset Canadian content and labor rules for the building of PC-based products.

Solectron, of Milpitas, California, reported 1992 sales revenue of more than $328 million. Solectron was founded in 1977 and derives its sales from workstation, computer peripherals, and minicomputer and peripherals systems and subsystems. Solectron ships more than 2 million flexible, surface mount, and mixed-technology assemblies per month. Solectron acquired IBM's production facilities in Bordeaux, France and Charlotte, North Carolina in 1992 in exchange for an equity position in Solectron. As part of the alliance, Solectron will also supply subassemblies to IBM as well as gain access to select IBM technologies and processes.

Table 5-1 lists leading board and package subcontractors.

Table 5-1
Worldwide Subcontract Assemblers

Company	Corporate Location	Package Subcontractor	Board Subcontractor
A.B. Electronics	Europe		x
ADCO Circuits Inc.	United States		x
ASE	Taiwan	x	x
ICG Electronics	U.S. Subsidiary	x	x
A.J. Electronics	United States		x
Anam	Korea	x	x
Amkor	U.S. Subsidiary	x	
ASAT	Hong Kong	x	x
ASP	United States	x	
AT&T	United States	x	x
Avex Electronics	United States		x
Benchmark Electronics	United States		x
Carsem/Carter Semiconductor	Malaysia	x	x
Chip Supply	United States	x	x
Chinteik	Thailand	x	x
Cirtek Electronics Corporation	Philippines	x	x
Citizen	Japan	x	x
Comptronix	United States		x
Diacon	United States	x	
Dover Electronics	United States		x
Dyne-SEM Electronics	Philippines	x	x
Euro-Technology	Spain	x	x
Eurasem	Netherlands	x	x
Fine Products Microelectronics	Taiwan	x	x
Flextronics	Singapore		x
Hana Semiconductor	Thailand	x	x
EM2 Hana	U.S. Subsidiary	x	
Hyundai Electronics	Korea	x	x
IBM	United States	x	x
IMI	Philippines	x	x
Itaucom	Spain	x	x
Iteq	Scotland	x	x
Jabil Circuits	United States		x
Kyocera	Japan	x	x
Kyocera America	U.S. Subsidiary	x	x
Lingsen Precision	Taiwan	x	x
Microelectronic Packaging Inc.	Taiwan	x	
MPI America	U.S. Subsidiary	x	

(Continued)

Table 5-1 (Continued)
Worldwide Subcontract Assemblers

Company	Corporate Location	Package Subcontractor	Board Subcontractor
Olin	United States	x	
Orient Semiconductor Electronics	Taiwan	x	x
Pantronix	United States	x	x
Philips Circuit Assembly	Netherlands		x
ROHM	Japan	x	x
SCI Systems	United States		x
Seiko Epson/SMOS	Japan	x	x
Semiconductor Devices Ltd.	Hong Kong	x	x
Solectron	United States		x
Swire Technologies	Hong Kong	x	x
Team	Philippines	x	
Texas Instruments	United States	x	x
Triam	Singapore		x
Vermont Semiconductor	United States	x	
VLSI Packaging	United States	x	

Source: Dataquest (April 1993)

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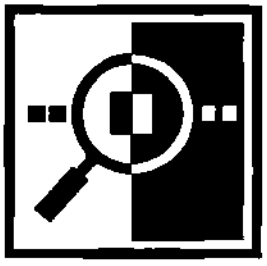

Focus Report

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Chapter 1
Executive Summary

The trends to miniaturization—lower cost per function and increased reliability—that were embodied in surface-mount package design and assembly have revolutionized the entire electronics industry during the last 10 years. Advancements in surface-mount technology (SMT), embodying the IC design philosophy of "faster, cheaper, and better," drove developments in the following areas:

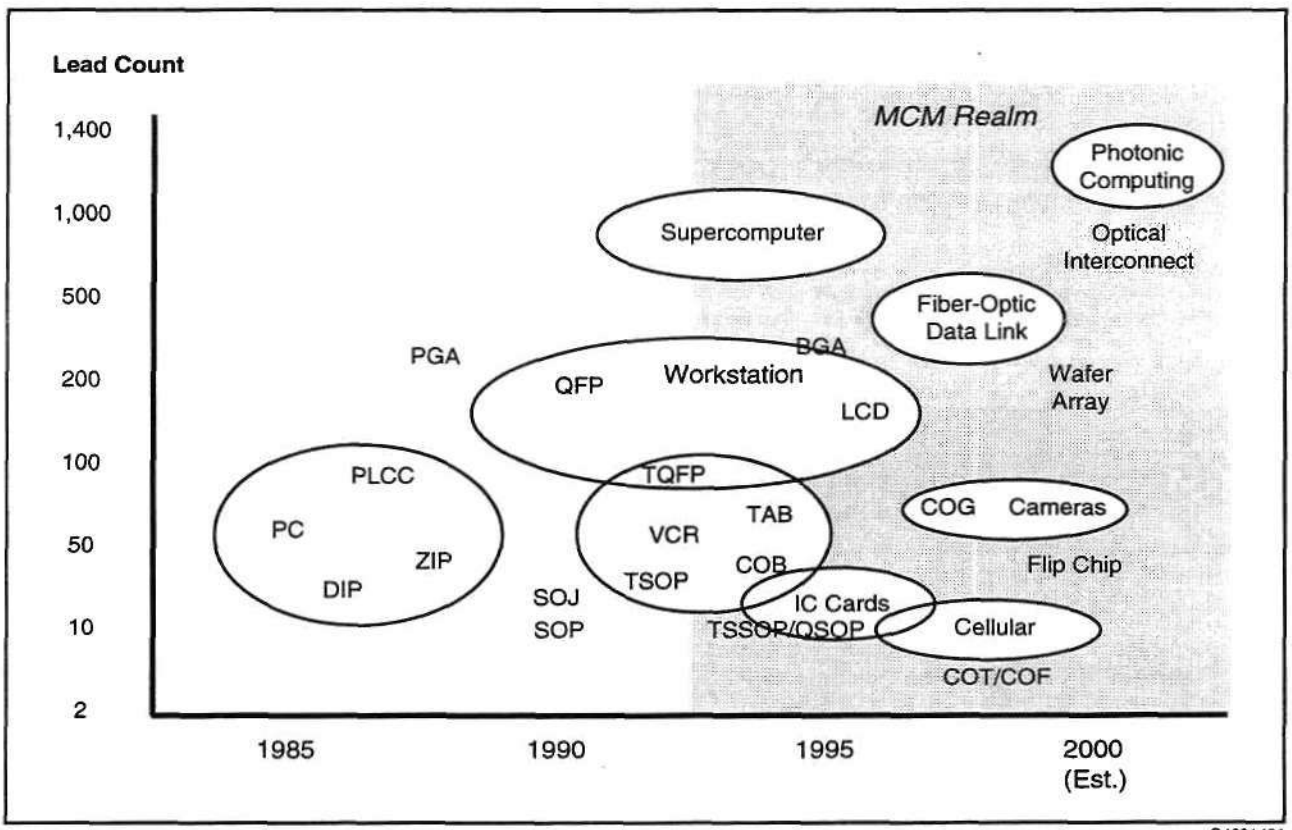
- Robotics, by increasing the need for automated placement and assembly methods
- PCB fabrication, lamination, and inspection techniques for ultrafine (0.015 to 0.020 inches) four-layer and multilayer PCMCIA board/card markets
- Ultrafine pitch attach methods for next-generation tape-automated bonding (TAB), flip chip, and direct chip attach components
- Lower-cost, thinner package (1.4 to 1.0mm) profiles for portable application markets
- Package reliability via emphasis on stress analysis, thermal analysis, and electrical analysis tools
- Turnaround and cycle time via 3-D design to simulation software tools

In 1983, the Philips Electronic Components Division stated in a company publication, "...the effect that this new component and assembly technology will have on the way manufacturers think about their products is enormous. The '80s and '90s are a period of transition which will see the innovation of technological processes reach a finite limit and thus change historically engineering-led product development to an application led approach."[1]

- As shown in Figure 1-1, advancements in low-profile and thin single-chip design technologies enhanced the design scales for weight, size, and processing power at the system level, creating a pathway to multi-chip module (MCM) and direct chip attach. The packaging hierarchy of first level chip-to-package, second level package-to-card, and third level card-to-board no longer can be viewed as separate tasks that can be handled at distinctly separate stages. The increased activity and growth to thin and ultrathin packages, cards/modules, and boards, and the tight dimensions of the PCMCIA, dictate more cooperation and more interface between system designer and materials supplier, as the industry begins to reach the finite limits of its own technology.

[1]Philips Electronic Components and Materials Division, Eindhoven, The Netherlands, page 1, October 1993.

Figure 1-1
Application Drivers



Source: Dataquest (March 1994)

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Package Design Trends

The dual in-line processing (DIP) package available in a variety of plastic and ceramic (cofired, CERDIP, and ceramic glass) configurations was the mainstay for worldwide IC encapsulation through the late 1980s, growing with LSI developments from 14 to 64 leads. The DIP derived its name from its two rows of in-line leads. The ceramic DIPs incorporated a multilayer ceramic body featuring brazed-on leads and a die-mounting cavity with a solder-sealed metal lid. The sealing techniques were gold-plated metal lids and gold-tin eutectic sealing preform. More cost-effective ceramic DIPs used a glass seal to attach the lid to the package. Ceramic dual in-line packages (CERDIPs) consisted of two ceramic body parts and a lead frame. After the IC is attached and wire-bonded to the lead frame, the pieces are run through a furnace and fused with a glass seal. CERDIP packages offered the least expensive hermetic technology available. In 1983, Intel developed a silver-loaded glass system as a nongold die attach substitute in CERDIP packages. The silver/glass system offered significant cost and processing advantages for nonvolatile products. The traditional DIP package's performance was limited by its 0.100 pitch or lead spacing and pin count, and it was replaced by new generations of shrink-DIP packages with 0.050-inch centers, the newer zigzag in-line packages (ZIPs) with 2.54mm lead pitch, and eventually the Quad flat packages (QFPs).

As commercial development of surface mount became prevalent in the early 1980s, the Electronic Industries Association of Japan (EIAJ) began to develop its own versions of an old ceramic 50-mil flat package design that was predominantly used in military applications in the United States. Renamed the QFP, the body of the package was available in either square or rectangular format with pitches of 1.0mm (39.4 mils), 0.8mm (31.5 mils), and 0.65mm (25.6 mils), and was available in 20 to 240 leads.

Consumer market demands for smaller and low-cost electronic gadgets promoted the development of fine pitch package technologies. The Japanese developed the shrink QFP (SQFP) and the very small QFP (VQFP) as extensions of the EIAJ QFP family of products. Although the standard body sizes were the same, the package was thinner and the lead pitches were reduced to 0.5mm (19.7 mils), 0.4mm (15.7 mils), and 0.3mm (11.8 mils). The pin count range now available was 32 to 520 leads.

A subset of the VQFP product was later developed and called the thin QFP (TQFP). This package has the same 0.5mm, 0.4mm, and 0.3mm pitches as the VQFP, but package thickness has been reduced even further to 50 mils, or 1.27mm. Another variation of the QFP design is the metal QUAD, introduced by Olin Corporation, which is constructed from anodized aluminum piece parts and is assembled using plastic package assembly processes.

Another package development was the very small outline package (VSOP). One version from Japan uses the EIAJ standard body size for the small outline (SO) but reduces the pitch from 50 mils to 25.6 mils (0.65mm). A subset of this package is the thin SO package (TSOP), whose pitch is 0.65mm or less and whose thickness has a maximum height of 50 mils (1.27mm). The TSOP has leads on the two narrow ends only and developed into a major package for high-density DRAM devices.

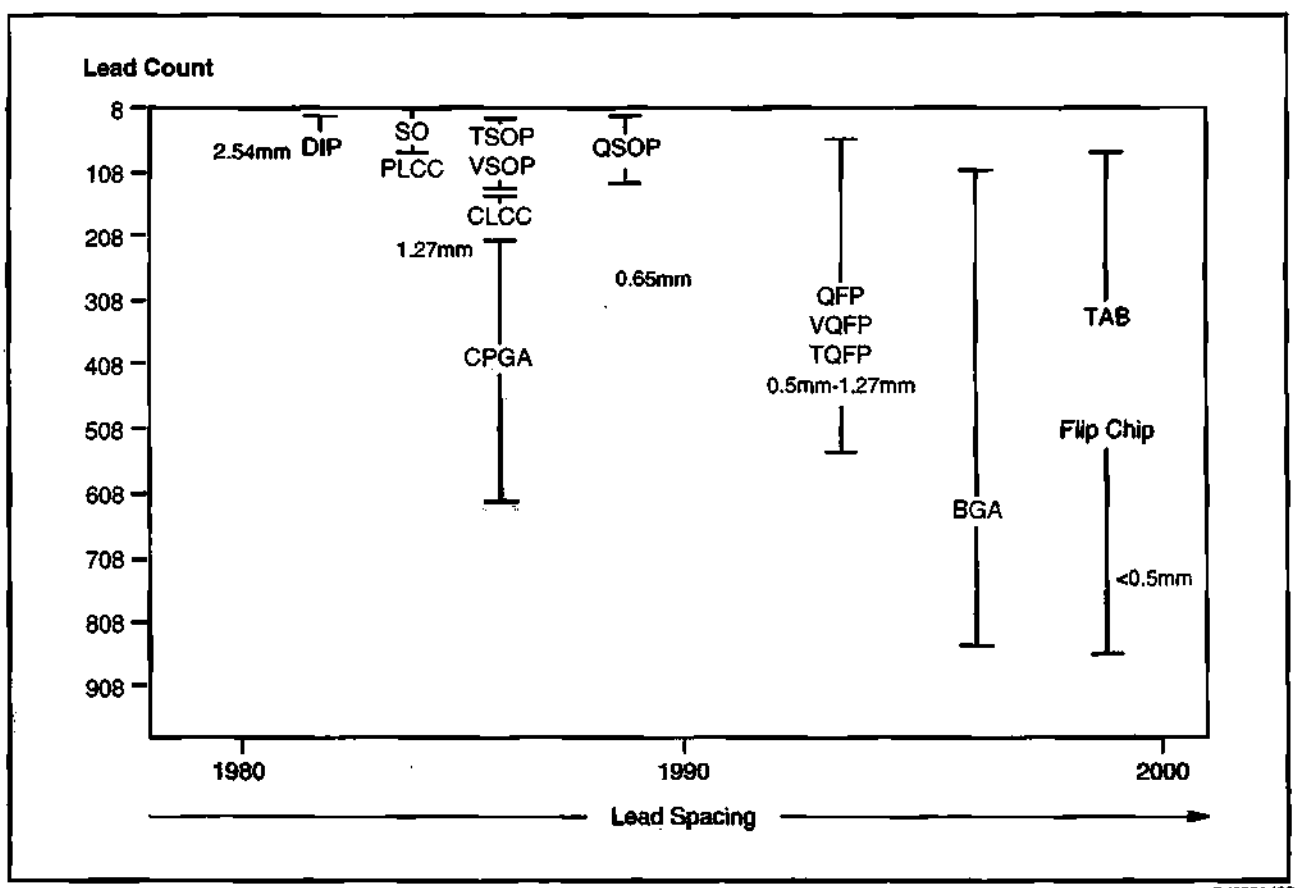
Very similar to the VSOP is the VSOIC, a European version of a fine-pitch SO package. Developed by Philips, the lead counts range from 14 to 56 on 30- and 40-mil center spacings. Texas Instruments also introduced its own version of the VSOP, which featured a 25-mil lead pitch. The standoff height was increased to 8 to 16 mils for the VSOP to facilitate board cleanup after assembly.[2] During the first quarter of 1994, IDT introduced an ultraspace-saving 20- and 24-pin surface-mount package called the Quarter Size Outline Package (QSOP) for its high-speed FCT CMOS Octal Logic products, to complement its Thin Shrink Small Outline Package (TSSOP) products. The QSOP packages, accepted as standard packages in 1993, have a 0.025-mil (0.635mm) pin pitch and a 0.0645-inch height from the board. The QSOPs, at a 0.340-inch body length and a 0.153-inch body width, are half the length and half the width of industry-standard SOIC packages.

[2]R. Moore, G. Ricci, "Electrical and Mechanical Attributes of the Fine-Pitch Small-Outline Package," Texas Instruments Incorporated, Sherman, Texas , 1988, p. 5.

The majority of SM ICs have been encapsulated in the SO packages during the last five years. Growth in SO package variations, especially the TSOP and TSSOP, has been driven by analog, standard logic, and memory devices. The proliferation of Quad configurations initially was driven by high-density, high-pin-count ASIC products (see Figure 1-2) and eventually became a more cost-efficient package for 16- and 32-bit microprocessors. As the lead pitch of QFPs drops to less than 0.5mm, and 0.4mm manufacturing process yields diminish.[3] Other packages leading the way to high I/O densities are area-array interconnection techniques such as ball grid array (BGA) and solder ball connect (SBC), as well as direct chip attach via wire bond, flip chip or TAB.

Project Analyst: Mary A. Olsson

Figure 1-2
Emerging Packaging Trends



Source: Dataquest (March 1994)

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[3]R. Joel Weldon, "3-D Inspection of Solder Paste for High-Quality BGA Assembly," Celestica Inc., North York, Ontario, Canada, 1994 ITAP & Flip Chip Proceedings, p. 52.

Chapter 2
First-Level IC Package History and Forecast

The worldwide packaging forecast discussed in this chapter is an evaluation of the total number of single-chip ICs packaged in both plastic and ceramic that are produced in the four major regions researched by Dataquest. This forecast is based on the following analysis:

- Dataquest's semiconductor IC worldwide forecast
- Survey of ceramic package suppliers' estimates of yearly package production
- Survey of semiconductor vendor estimates of IC products by package types
- User survey of package designs by application
- Survey of subcontract assemblers' estimates of board assembly technologies

The forecast also includes data on bare die shipments. This has been included to follow the potential development of new and emerging chip-to-substrate interconnect schemes such as the following:

- MCM formations of 3-D ICs, stackable memory modules, and MCM-L(aminate), MCM-C(eramic), MCM-D(eposited) configurations
- Direct chip attach via flip chip on board (FCOB), wire bond, and TAB

Dataquest's surveys include data from all suppliers to the merchant semiconductor market. The survey excludes captive suppliers that manufacture devices solely for the benefit of the parent company. Included, however, are companies that actively market semiconductor devices to the merchant market as well as to other divisions of their own companies. Both external shipments and internal consumption are included for such companies. Shipment is defined as the purchase of a semiconductor device or devices. This definition must be differentiated from actual use of the device in a final product. A regional market includes all devices sold or shipped to that region.

Worldwide Forecast

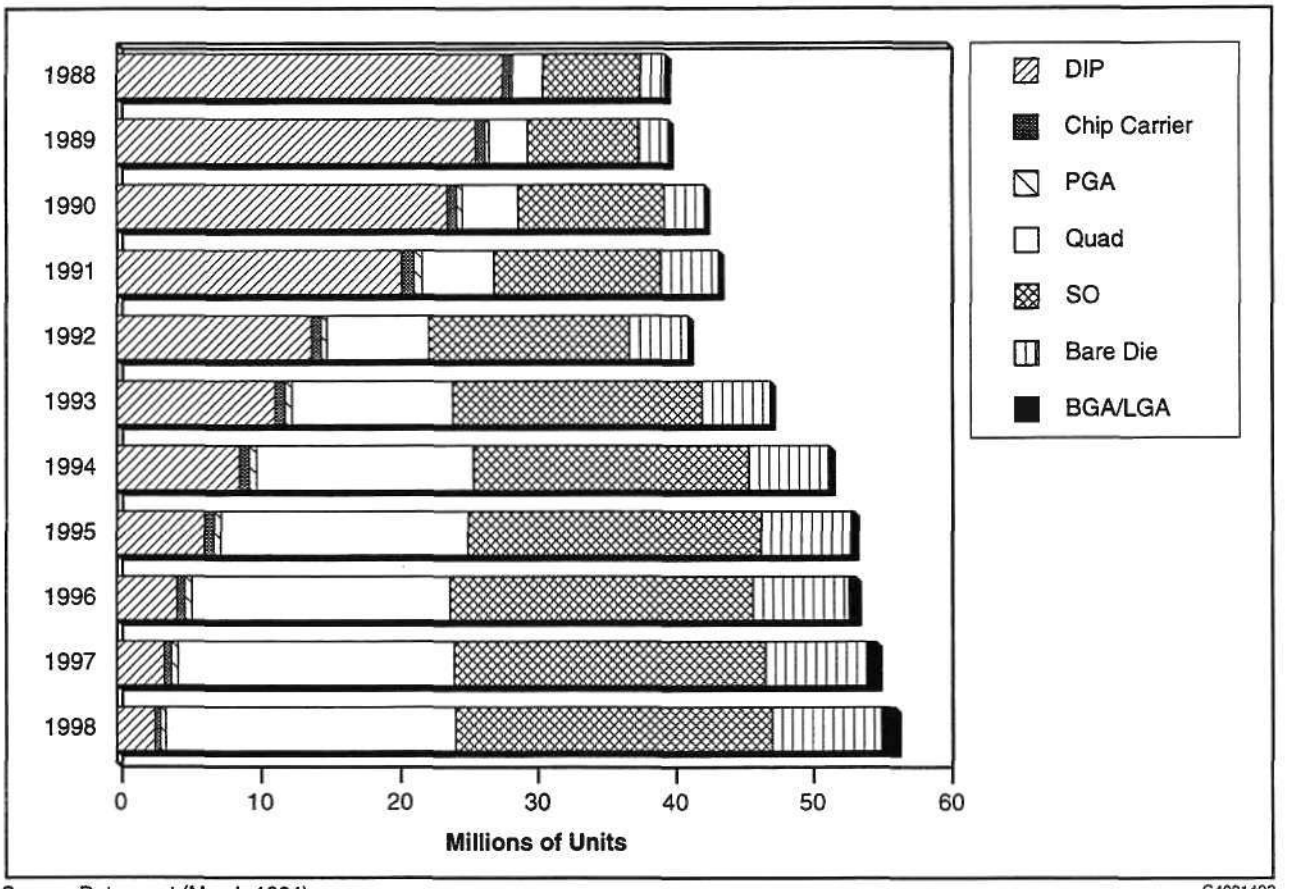
Table 2-1 lists single-chip IC packages as well as available bare die from 1992 through 1998. The DIP packages, both plastic and ceramic, continued to decline with a final 1993 actual production of 11.2 billion units, in comparison with 13.8 billion units for year-end 1992. The SO and Quad package category, which includes all the smaller and thinner variations of these two product families, continued to grow in dominance (see Figure 2-1). Ceramic pin grid array (PGA) packages reached 198 million units by year-end 1993, driven by increased production of high-end Pentium microprocessors. High-performance MIPS' TFP and R4400, Alpha, PA-RISC, and next-generation Pentium products will stimulate growth in both ceramic PGAs and ceramic QFPs in 1994.

Table 2-1
Worldwide Estimated Package Production (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Plastic DIP	11,761	9,357	7,166	5,030	3,233	2,511	2,045
Ceramic DIP	2,110	1,894	1,628	1,318	1,091	897	689
Quad	7,397	11,603	15,637	17,670	18,497	19,849	20,815
Ceramic Chip Carrier	171	171	153	136	114	96	56
Plastic Chip Carrier	530	550	552	522	498	447	386
SO	14,634	18,132	20,011	21,191	22,009	22,582	23,038
Ceramic PGA	165	198	227	236	240	226	201
Plastic PGA	228	259	256	252	256	244	229
Ball/Land Grid Array	1	14	67	196	443	734	1,035
Bare Chip	4,247	5,045	5,846	6,519	6,986	7,284	7,915
Total	41,244	47,223	51,543	53,070	53,367	54,870	56,409

Source: Dataquest (March 1994)

Figure 2-1
Package Technology Trends



Source: Dataquest (March 1994)

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Although we have continued to forecast modest growth in the ceramic and plastic PGA packages, there are very strong market indications from package designers and systems houses that a major shift is taking place in microprocessor and ASIC designs, from PGAs to plastic/ceramic Quads, as well as new plastic/ceramic BGA designs. The array packages have also been referred to as solder grid arrays, bump arrays, land grid arrays, or overmolded plastic pad array (OMPAC), a Motorola acronym. Users have indicated that this shift from PGA to Quads and other grid array designs is being made for purposes of performance and size reduction, as well as for the significant cost efficiencies of these packages over the PGA. These are clear signals that indicate an early maturation and potential demise of both ceramic and plastic PGAs. Motorola has also combined BGA technology with flip chip. The "slightly larger than IC carrier" (SLICC) is a combination of attaching flip chip ICs on a substrate and using BGA connections to attach the assembly to the circuit board. The SLICCs have a pad pitch of 0.035 inches and are offered as cost-effective packages for pin counts of 30 to 150.

North American suppliers of semiconductors continue to be the largest producers and consumers of ICs in the traditional DIP package (see Table 2-2). The CMOS gate array devices and higher-than-50-MHz microprocessors are now the drivers for higher-pin-count plastic/ceramic QFPs and plastic/ceramic BGA designs. We have increased our long-range forecast for the BGA designs, based on user satisfaction with the package and on ASIC vendor long-range projections for BGA designs. However, we do not expect tremendous activity and momentum to build for this package until 1995. IBM is promoting both plastic and ceramic BGA packages and TAB BGAs for ASIC designs. IBM offers BGAs in an I/O range of 192 to 736, and 10 body sizes, with an average cost of 3 to 7 cents per I/O. Motorola is marketing its OMPAC package via license agreements with Amkor, ASAT, and Universal Instruments. It has also made arrangements for marketing of its product with Citizen of America, Pacific Microelectronics for MCM designs, and with Shinko. The reported benefits of the BGA over the QFP are as follows:

- BGA has a smaller footprint than a comparable QFP.
- Bumps designed under the chip are used as thermal vias.
- Die can be mounted cavity down with a heat spreader attached to its back side for efficient heat transfer.
- Resonant frequency can be higher in a BGA.
- Average lead inductance can be reduced via wire bond length.

Table 2-2
North American Estimated Package Production (Millions of Units)

Packages	1992	1993	1994	1995	1996	1997	1998
Plastic DIP	5,978	5,001	3,600	2,300	1,500	1,100	900
Ceramic DIP	1,100	1,000	900	789	680	550	400
Quad	2,314	4,162	6,049	6,500	6,620	6,770	6,941
Ceramic Chip Carrier	111	115	102	88	74	60	25
Plastic Chip Carrier	370	388	407	401	388	345	300
SO	2,540	3,888	4,900	5,500	5,860	6,267	6,577
Ceramic PGA	60	75	85	90	91	93	95
Plastic PGA	130	155	152	150	145	140	130
Ball/Land Grid Array	1	11	58	175	400	670	930
Bare Die	1,346	1,710	2,154	2,645	3,010	3,400	3,840
Total	13,950	16,505	18,407	18,638	18,768	19,395	20,138
Percentage of Total	**1992**	**1993**	**1994**	**1995**	**1996**	**1997**	**1998**
Plastic DIP	42.9	30.3	19.6	12.3	8.0	5.7	4.5
Ceramic DIP	7.9	6.1	4.9	4.2	3.6	2.8	2.0
Quad	16.6	25.2	32.9	34.9	35.3	34.9	34.5
Ceramic Chip Carrier	0.8	0.7	0.6	0.5	0.4	0.3	0.1
Plastic Chip Carrier	2.7	2.4	2.2	2.2	2.1	1.8	1.5
SO	18.2	23.6	26.6	29.5	31.2	32.3	32.7
Ceramic PGA	0.4	0.5	0.5	0.5	0.5	0.5	0.5
Plastic PGA	0.9	0.9	0.8	0.8	0.8	0.7	0.6
Ball/Land Grid Array	0	0.1	0.3	0.9	2.1	3.5	4.6
Bare Die	9.6	10.4	11.7	14.2	16.0	17.5	19.1
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Source: Dataquest (March 1994)

Market acceptance of BGA technology over the proved success of the QFP designs will only be decided on by availability, proven cost efficiencies, and successful marketing of the sponsors. Current users of BGA designs are as follows:

- Xilinx for FPGAs
- IBM for ASIC devices
- Motorola for ASIC, SRAMs, and microcontrollers
- Compaq for ASIC in desktop and server applications
- Altera for FPGAs
- Hestia Technologies for MCM-L designs
- VLSI Technology Inc. for ASICs
- LSI Logic Inc. for ASIC designs
- Tessera for MCM-L designs

Although IBM could be a major contender in the worldwide production and shipment of DRAMs in SIMMs and PCMCIA designs to the merchant market, Japan is expected to remain the dominant producer and consumer of memory devices in SIMMs for the portable market. This demand will continue to fuel the growth of TSOP and emerging package options through the end of the decade. Although SO and Quad packages represent the volume share of package production in Japan (see Table 2-3), bare die consumption for COB, chip on flex (COF), TAB, and emerging MCM designs will continue to be fairly strong. COB applications such as memory cards, printers, graphics, calculators, laptops, games systems, and handheld communicators will be the largest consumer sectors for bare die, in combinations of COB/TSOP and MCM designs. Although investment in BGA package design is low in comparison to the PQFP package, the interest level is high for the more-than-244-pin package as demand increases for BGA product in North America.

Table 2-3
Japanese Estimated Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Plastic DIP	1,600	820	721	600	344	211	105
Ceramic DIP	450	388	288	201	104	90	70
Quad	2,820	3,416	3,712	3,700	3,893	4,000	4,002
Ceramic Chip Carrier	15	12	10	9	5	3	2
Plastic Chip Carrier	55	55	45	28	20	20	10
SO	4,705	5,200	5,324	5,259	5,300	5,400	5,500
Ceramic PGA	70	85	90	85	80	70	55
Plastic PGA	60	54	50	45	45	35	30
Ball/Land Grid Array	0	1	4	11	24	35	65
Bare Die	2,310	2,490	2,534	2,400	2,300	2,040	2,000
Total	12,085	12,521	12,778	12,338	12,115	11,904	11,839
Percentage of Total	**1992**	**1993**	**1994**	**1995**	**1996**	**1997**	**1998**
Plastic DIP	13.2	6.5	5.6	4.9	2.8	1.8	0.9
Ceramic DIP	3.7	3.1	2.3	1.6	0.9	0.8	0.6
Quad	23.3	27.3	29.0	30.0	32.1	33.6	33.8
Ceramic Chip Carrier	0.1	0.1	0.1	0.1	0	0	0
Plastic Chip Carrier	0.5	0.4	0.4	0.2	0.2	0.2	0.1
SO	38.9	41.5	41.7	42.6	43.7	45.4	46.5
Ceramic PGA	0.6	0.7	0.7	0.7	0.7	0.6	0.5
Plastic PGA	0.5	0.4	0.4	0.4	0.4	0.3	0.3
Ball Grid Array	0	0	0	0.1	0.2	0.3	0.5
Bare Die	19.1	19.9	19.8	19.5	19.0	17.1	16.9
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Source: Dataquest (March 1994)

SMT is now the dominant package in electronics in the European region (see Table 2-4). Automotive and telecommunications applications continue to drive consumption of QFP and MCM designs in QFPs for use in the LAN and wireless applications.

Table 2-4
European Estimated Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Plastic DIP	2,400	2,136	1,875	1,500	989	900	800
Ceramic DIP	475	441	395	298	287	231	200
Quad	1,422	1,870	2,433	2,900	3,100	3,091	3,122
Ceramic Chip Carrier	44	43	40	38	34	32	28
Plastic Chip Carrier	51	50	50	45	44	42	41
SO	2,706	3,400	3,567	3,745	3,899	3,815	3,811
Ceramic PGA	28	30	42	49	55	50	40
Plastic PGA	33	41	42	45	52	54	55
Ball/Land Grid Array	0	1	2	4	9	15	22
Bare Die	388	550	712	914	988	1,004	1,050
Total	7,547	8,562	9,158	9,538	9,457	9,234	9,169
Percentage of Total	**1992**	**1993**	**1994**	**1995**	**1996**	**1997**	**1998**
Plastic DIP	31.8	24.9	20.5	15.7	10.5	9.7	8.7
Ceramic DIP	6.3	5.2	4.3	3.1	3.0	2.5	2.2
Quad	18.8	21.8	26.6	30.4	32.8	33.5	34.0
Ceramic Chip Carrier	0.6	0.5	0.4	0.4	0.4	0.3	0.3
Plastic Chip Carrier	0.7	0.6	0.5	0.5	0.5	0.5	0.4
SO	35.9	39.7	38.9	39.3	41.2	41.3	41.6
Ceramic PGA	0.4	0.4	0.5	0.5	0.6	0.5	0.4
Plastic PGA	0.4	0.5	0.5	0.5	0.5	0.6	0.6
Ball Grid Array	0	0	0	0	0.1	0.2	0.2
Bare Die	5.1	6.4	7.8	9.6	10.4	10.9	11.5
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Source: Dataquest (March 1994)

The Asia/Pacific regional package data in Table 2-5 continues to support the low pin count and predominantly plastic package applications. Consumption of gate arrays is expected to grow from 5.4 percent of the total world consumption to 9.1 percent by 1997. Korean manufacturers are encapsulating their higher-pin-count ASIC devices in QFPs, and are large producers of TSOP and SIMM configurations for PC cards and 486 motherboards. As demand and expertise increases for their complex programmable logic device (CPLD) and field-programmable gate array (FPGA) products, we expect to see demand increase for plastic BGA (PBGA) designs.

Table 2-5
Asia/Pacific Estimated Package Forecast (Millions of Units)

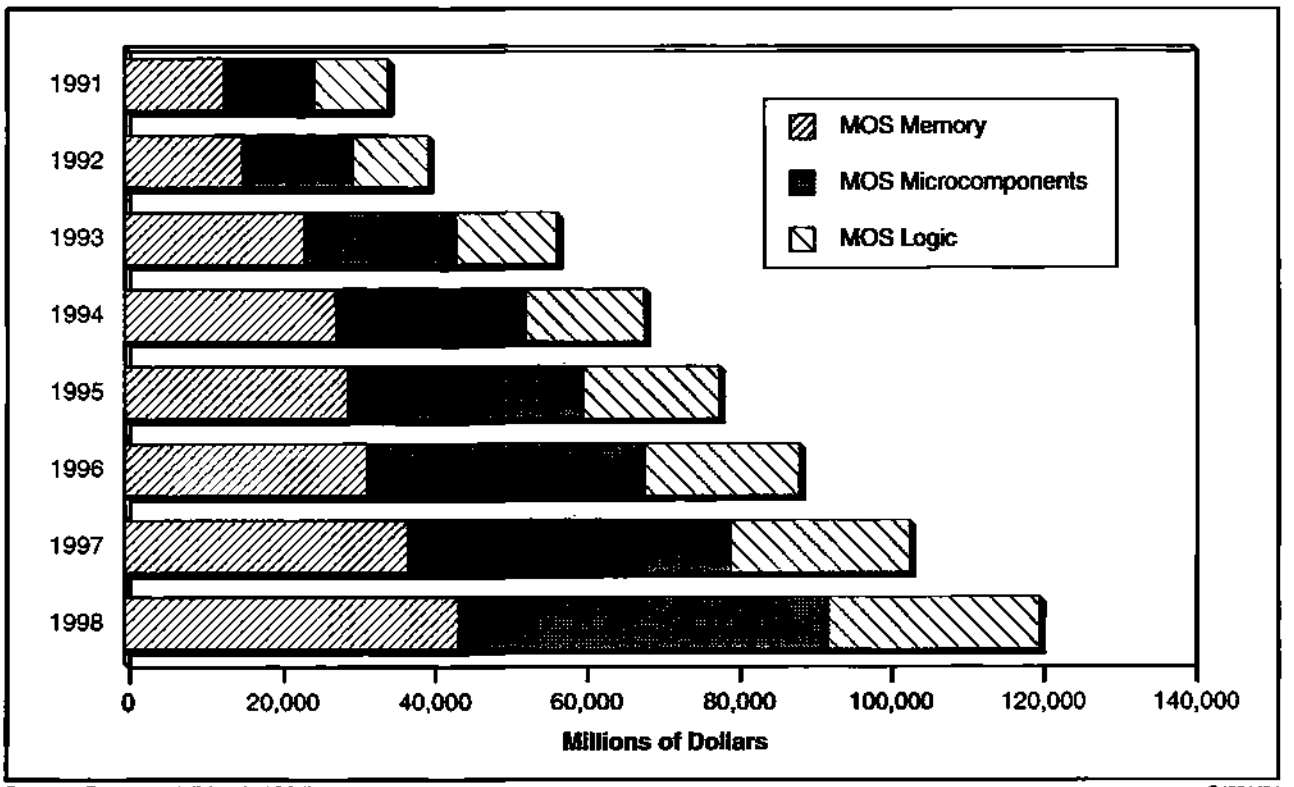
	1992	1993	1994	1995	1996	1997	1998
Plastic DIP	1,783	1,400	970	630	400	300	240
Ceramic DIP	85	65	45	30	20	26	19
Quad	841	2,155	3,443	4,570	4,884	5,988	6,750
Ceramic Chip Carrier	1	1	1	1	1	1	1
Plastic Chip Carrier	54	57	50	48	46	40	35
SO	4,683	5,644	6,220	6,687	6,950	7,100	7,150
Ceramic PGA	7	8	10	12	14	13	11
Plastic PGA	5	9	12	12	14	15	14
Ball Grid Array	0	1	3	6	10	14	18
Bare Chip	203	295	446	560	688	840	1,025
Total	7,662	9,635	11,200	12,556	13,027	14,337	15,263
Percentage of Total	**1992**	**1993**	**1994**	**1995**	**1996**	**1997**	**1998**
Plastic DIP	23.3	14.5	8.7	5.0	3.1	2.1	1.6
Ceramic DIP	1.1	0.7	0.4	0.2	0.2	0.2	0.1
Quad	11.0	22.4	30.7	36.4	37.5	41.8	44.2
Ceramic Chip Carrier	0	0	0	0	0	0	0
Plastic Chip Carrier	0.7	0.6	0.4	0.4	0.4	0.3	0.2
SO	61.1	58.6	55.5	53.3	53.4	49.5	46.8
Ceramic PGA	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Plastic PGA	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Ball Grid Array	0	0	0	0	0.1	0.1	0.1
Bare Chip	2.6	3.1	4.0	4.5	5.3	5.9	6.7
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Source: Dataquest (March 1994)

Chapter 3
Component Interconnect

MOS digital products continued to represent the largest revenue base for the semiconductor industry (see Figure 3-1). While memory devices specifically DRAMs are the technology driver for the smaller, thinner ultrafine pitch packages, performance driven microprocessors and high I/O ASICs are driving the growth of new 0.3 mm and 0.4 mm TQFP/VQFPs, and single/multilayer BGA designs.

Figure 3-1
MOS Digital Forecast, Share by Technology



Source: Dataquest (March 1994)
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Memory Packaging

Tables 3-1 through 3-9 list the package development for DRAMs, SRAMs, and the nonvolatile product families, ROM, EPROM, EEPROM, and flash. Although the majority of single-chip commodity DRAMs are packaged in a variety of plastic molded packages (ZIP, SOP/SOJ, and TSOP) averaging 28 pins, the next-generation of 3V 16Mb, 64Mb, and 256Mb DRAMs will be encapsulated not only in the standard SOP/TSOP designs but also in the emerging packages listed in Table 3-3.

Table 3-1
Worldwide Estimated MOS DRAM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
256K DRAM	194.0	123.0	88.0	48.0	25.0	8.0	5.0
DIP	106.7	60.3	39.6	16.8	6.4	2.0	0.8
ZIP	21.3	18.5	11.9	6.2	3.1	1.0	0.4
PLCC	54.3	36.9	28.2	18.2	10.0	3.4	2.9
Others	9.7	6.2	7.5	6.2	5.3	1.5	1.0
Die	1.9	1.2	0.9	0.5	0.3	0.1	0.1
SIP/SIMM	43.5	29.5	20.3	9.1	5.0	1.7	1.5
1Mb DRAM	822.0	549.0	345.0	225.0	85.0	56.0	40.0
DIP	74.0	38.4	11.0	0	0	0	0
ZIP	115.9	75.2	43.8	27.2	10.2	6.2	4.0
SOJ/SOP	600.1	411.8	276.0	187.7	70.6	47.0	33.6
Others	14.0	11.0	3.8	2.3	0.9	0.6	0.4
Die	18.1	12.6	10.4	7.9	3.4	2.2	2.0
SIP/SIMM	405.0	296.5	208.4	131.4	49.4	30.6	21.8
4Mb DRAM	449.0	791.0	866.0	650.0	465.0	303.0	180.0
DIP	0	0	0	0	0	0	0
ZIP	31.4	62.5	65.0	45.5	32.6	21.2	12.6
SOJ/SOP	395.1	691.3	762.1	572.0	406.9	263.6	155.5
Others	18.0	27.7	26.0	19.5	14.0	9.1	5.4
Die	4.5	9.5	13.0	13.0	11.6	9.1	6.5
SIP/SIMM	134.3	313.2	350.6	400.4	284.8	197.7	116.6
16Mb DRAM	2.0	21.0	145.0	357.0	650.0	870.0	1,100.0
DIP	0	0	0	0	0	0	0
ZIP	0	0	0	0	0	0	0
SOJ/SOP	1.6	16.5	105.9	257.4	438.8	582.0	669.9
Others	0.4	4.3	37.0	92.1	195.0	261.9	391.6
Die	0	0.2	2.2	7.5	16.3	26.1	38.5
SIP/SIMM	0	1.2	40.2	115.8	241.3	320.1	435.4
64Mb DRAM	0	0	0	0	3.0	40.0	125.0
DIP	0	0	0	0	0	0	0
ZIP	0	0	0	0	0	0	0
SOJ/SOP	0	0	0	0	2.7	33.6	98.3
Others	0	0	0	0	0.3	6.0	25.0
Die	0	0	0	0	0	0.4	1.8
SIP/SIMM	0	0	0	0	0.8	11.1	39.3
256Mb DRAM	0	0	0	0	0	0	2.0
DIP	0	0	0	0	0	0	0
ZIP	0	0	0	0	0	0	0
SOJ/SOP	0	0	0	0	0	0	1.3
Others	0	0	0	0	0	0	0.7
Die	0	0	0	0	0	0	0
SIP/SIMM	0	0	0	0	0	0	0.8

Source: Dataquest (March 1994)

Table 3-2
Worldwide Estimated MOS DRAM Module Organization Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
256K DRAM, SIP/SIMM	43.5	29.5	20.3	9.1	5.0	1.7	1.5
x8	8.7	5.3	3.2	1.4	0.8	0.3	0.2
x9	34.8	24.2	17.1	7.7	4.3	1.4	1.2
x32	-	-	-	-	-	-	-
x36	-	-	-	-	-	-	-
x40	-	-	-	-	-	-	-
1Mb DRAM, SIP/SIMM	405.0	296.5	208.4	131.4	49.4	30.6	21.8
x8	153.9	103.8	62.5	39.4	14.8	9.2	6.6
x9	222.8	163.1	114.6	72.3	27.2	16.8	12.0
x32	4.1	3.0	2.1	1.3	0.5	0.3	0.2
x36	16.2	20.8	25.0	15.8	5.9	3.7	2.6
x40	8.1	5.9	4.2	2.6	1.0	0.6	0.4
4Mb DRAM, SIP/SIMM	449.0	791.0	866.0	650.0	465.0	303.0	180.0
x8	44.9	79.1	86.6	65.0	46.5	30.3	18.0
x9	188.6	316.4	346.4	260.0	186.0	121.2	72.0
x32	26.9	47.5	52.0	39.0	27.9	18.2	10.8
x36	166.1	308.5	337.7	253.5	181.4	118.2	70.2
x40	22.5	39.6	43.3	32.5	23.3	15.2	9.0
16Mb DRAM, SIP/SIMM	0	1.2	40.2	115.8	241.3	320.1	435.4
x8	0	0.3	12.1	29.0	60.3	80.0	108.9
x9	0	0.6	14.5	44.0	86.9	105.6	143.7
x32	0	0	0.4	1.2	2.4	3.2	4.4
x36	0	0.2	12.9	40.5	89.3	128.0	174.2
x40	0	0	0.4	1.2	2.4	3.2	4.4
64Mb DRAM, SIP/SIMM	0	0	0	0	0.8	11.1	39.3
x8	-	-	-	-	0.2	2.2	7.9
x9	-	-	-	-	0.2	3.3	11.8
x32	-	-	-	-	0	0.2	0.8
x36	-	-	-	-	0.2	2.8	9.8
x40	-	-	-	-	0.2	2.5	9.0
256Mb DRAM, SIP/SIMM	0	0	0	0	0	0	0.8
x8	-	-	-	-	-	-	0.1
x9	-	-	-	-	-	-	0.3
x32	-	-	-	-	-	-	0
x36	-	-	-	-	-	-	0.3
x40	-	-	-	-	-	-	0.1

Source: Dataquest (March 1994)

Table 3-3
MOS DRAM Emerging Package Technologies Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
SO	996.8	1,119.6	1,143.9	1,017.0	918.8	926.2	958.6
SOJ	897.1	895.7	800.8	610.2	450.2	370.5	287.6
TSOP	99.7	223.9	343.2	406.8	468.6	555.7	671.0
Others	86.7	79.9	94.9	132.1	220.1	281.0	426.0
LOC*	13.0	16.0	23.7	39.6	88.0	140.5	213.0
TAB	1.7	1.6	2.8	4.0	6.6	8.4	12.8
Stacked LOC	0.9	1.6	4.7	6.6	15.4	19.7	42.6
Die	32.3	28.5	33.0	34.6	36.6	39.4	49.7

*Lead on chip
Source: Dataquest (March 1994)

Table 3-4
Worldwide Estimated >70ns SRAM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
16K							
DIP	34.8	3.6	1.8	0.6	0.3	0.1	0
SOG/SOP	52.2	8.4	5.3	2.4	1.7	0.9	0
Bare Die	0	0	0	0	0	0	0
Total	87.0	12.0	7.0	3.0	2.0	1.0	0
64K							
DIP	62.9	36.1	7.0	2.5	1.3	0.6	0.1
SOG/SOP	151.9	91.6	21.5	10.3	7.6	5.3	1.9
Bare Die	2.2	1.3	0.6	0.3	0.2	0.1	0
Total	217.0	129.0	29.0	13.0	9.0	6.0	2.0
256K							
DIP	51.6	50.5	19.5	0.8	0	0	0
SOG/SOP	193.5	336.8	222.4	67.2	43.2	43.2	18.4
Bare Die	12.9	33.7	36.1	16.0	10.8	10.8	4.6
Total	258.0	421.0	278.0	84.0	54.0	54.0	23.0
1Mb							
DIP	4.3	8.5	3.7	0	0	0	0
SOG/SOP	36.6	104.9	162.9	108.0	137.8	115.6	91.0
Bare Die	2.2	8.5	16.5	19.1	30.2	25.4	20.0
Total	43.0	122.0	183.0	127.0	168.0	141.0	111.0
4Mb							
DIP	0	0	0	0	0	0	0
SOG/SOP	0.2	3.4	8.7	29.3	51.1	87.5	112.7
Bare Die	0	0.6	2.3	9.8	21.9	37.5	48.3
Total	0.2	4.0	11.0	39.0	73.0	125.0	161.0
16Mb							
DIP	0	0	0	0	0	0	0
SOG/SOP	0	0	0	1.6	6.4	26.4	54.4
Bare Die	0	0	0	0.4	1.6	6.6	13.6
Total	0	0	0	2.0	8.0	33.0	68.0

Source: Dataquest (March 1994)

Table 3-5
Worldwide Estimated Fast <70ns SRAM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
16K							
DIP	15.8	5.6	3.5	2.0	0.9	0.1	0
CLCC	1.9	0.7	0.6	0.4	0.2	0.1	0
Bare Die	3.4	1.7	2.9	2.1	1.9	0.8	0
Total	21.0	8.0	7.0	5.0	3.0	1.0	0
64K							
DIP	22.8	6.7	2.6	2.1	0	0	0
CLCC	2.3	1.3	0.5	0.4	0.2	0	0
SOJ	54.7	35.5	28.1	22.1	9.4	7.2	3.0
Bare Die	34.2	23.5	20.8	16.4	6.4	4.8	2.0
Total	114.0	67.0	52.0	41.0	16.0	12.0	5.0
256K							
DIP	16.8	21.9	20.9	11.6	1.3	0	0
SOJ	50.4	93.4	146.3	173.3	105.1	83.2	68.0
Bare Die	16.8	30.7	41.8	46.2	26.6	20.8	17.0
Total	84.0	146.0	209.0	231.0	133.0	104.0	85.0
1Mb							
DIP	1.7	3.1	3.3	0	0	0	0
SOJ	7.4	21.7	59.0	121.0	195.8	269.6	238.6
TSOP	0.1	0.6	3.3	10.1	23.2	46.0	54.3
BGA	0	0	0.8	1.7	4.4	6.3	5.8
Bare Die	1.9	5.6	15.6	35.3	66.7	96.1	89.2
Total	11.0	31.0	82.0	168.0	290.0	418.0	388.0
4Mb							
DIP	0	0	0	0	0	0	0
SOJ	0	0	3.2	4.9	13.4	33.4	51.2
TSOP	0	0	0.7	1.8	6.8	22.3	35.6
BGA	0	0	0	0	0	0	0
Bare Die	0	0	0.7	1.8	6.8	22.3	35.6
Total	0	0	4.0	7.0	22.0	62.0	99.0
16Mb							
DIP	0	0	0	0	0	0	0
SOJ	0	0	0	0	0	3.1	5.1
TSOP	0	0	0	0	0	3.2	6.3
BGA	0	0	0	0	0	0.1	0.5
Bare Die	0	0	0	0	0	2.7	5.1
Total	0	0	0	0	0	9.0	17.0

Source: Dataquest (March 1994)

Table 3-6
Worldwide Estimated MOS EPROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Worldwide Total	424.0	433.0	438.0	396.0	382.0	336.0	300.0
Total by Package Type	424.0	433.0	438.0	396.0	382.0	336.0	300.0
DIP	319.0	303.0	293.0	248.0	228.0	199.0	177.0
Chip Carrier	73.0	82.0	83.0	73.0	70.0	62.0	56.0
SO	25.0	36.0	40.0	47.0	46.0	41.0	37.0
TSOP	7.0	12.0	22.0	28.0	38.0	34.0	30.0
Total by Pin Count	424.1	432.9	438.0	396.0	382.0	336.0	300.0
24-Pin	12.3	8.7	4.4	2.0	0.4	0.3	0.3
28-Pin	376.4	383.1	387.6	348.5	337.7	297.0	265.2
32-Pin	20.9	21.7	21.9	19.8	19.1	16.8	15.0
40-Pin	4.2	8.7	13.1	15.8	15.3	13.4	12.0
44-Pin	10.2	10.8	11.0	9.9	9.6	8.4	7.5

Source: Dataquest (March1994)

Table 3-7
Worldwide Estimated MOS ROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Worldwide	418.0	434.0	457.0	402.0	439.0	482.0	515.0
Package Type	418.0	434.0	457.0	402.0	439.0	482.0	515.0
DIP	49.1	30.5	13.4	5.0	2.5	1.4	1.0
SO	280.9	297.5	327.6	267.0	314.5	368.6	394.0
Quad	4.0	9.0	12.0	15.0	26.0	32.0	44.0
Bare Die	84.0	97.0	104.0	115.0	96.0	80.0	76.0
Pin Count	418.0	434.0	457.0	402.0	439.0	482.0	515.0
24-Pin	0	0	0	0	0	0	0
28-Pin	66.8	48.0	31.0	25.0	11.0	5.0	1.0
32-Pin	123.0	82.0	51.0	37.0	22.0	12.0	5.0
40-Pin	117.2	142.0	181.0	92.0	63.0	41.0	34.0
44-Pin	27.0	65.0	90.0	133.0	237.0	334.0	395.0
Bare Die	84.0	97.0	104.0	115.0	106.0	90.0	80.0

Source: Dataquest (March 1994)

Table 3-8
Worldwide Estimated MOS EEPROM Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Worldwide Total	300.0	384.0	457.0	548.0	600.0	685.0	765.0
Package Type	300.0	384.0	457.0	548.0	600.0	685.0	765.0
DIP	49.0	41.0	38.0	25.0	12.0	5.0	1.0
Chip Carrier	50.0	61.0	67.0	64.0	54.0	45.0	35.0
SO	182.9	259.9	323.9	423.0	488.0	580.0	678.0
PGA	0.1	0.1	0.1	0	0	0	0
Bare Die	18.0	22.0	28.0	36.0	46.0	55.0	51.0
Pin Count	300.0	384.0	457.0	548.0	600.0	685.0	765.0
8-Pin	165.0	221.0	284.0	314.0	346.0	386.0	455.0
14-Pin	29.0	37.0	35.0	33.0	30.0	30.0	10.0
24-Pin	41.0	33.0	30.0	27.0	21.0	20.0	21.0
28-Pin	40.0	61.8	71.0	129.6	151.0	186.8	228.0
32-Pin	7.0	9.2	9.0	8.4	8.0	7.2	7.0
Bare Die	18.0	22.0	28.0	36.0	44.0	55.0	44.0

Source: Dataquest (March 1994)

Table 3-9
Worldwide Estimated Flash Memory Package Production (Millions of Units)

	1992	1993	1994	1995	1996	1997	1998
Total	28.0	76.0	141.0	235.0	333.0	461.0	570.0
Package Total	28.0	76.0	141.0	235.0	333.0	461.0	570.0
DIP	12.0	34.0	54.0	47.0	41.0	31.0	28.0
Chip Carrier	1.4	5.0	11.0	19.0	22.0	21.0	19.0
SO	6.4	15.0	28.0	50.0	74.0	115.0	142.0
TSOP	8.0	21.0	44.5	110.0	172.0	256.0	330.0
COB	0.2	1.0	3.5	9.0	24.0	38.0	51.0
Pin Count	28.0	76.0	141.0	235.0	333.0	461.0	570.0
28-Pin	7.0	15.0	20.0	20.0	14.0	10.0	8.0
32-Pin	14.8	45.0	63.5	98.0	87.0	80.0	49.0
40-Pin	5.0	9.0	22.0	44.0	71.0	91.0	111.0
44-Pin	1.0	4.0	11.0	24.0	44.0	68.0	91.0
48-Pin	0	2.0	21.0	40.0	93.0	174.0	260.0
Bare Die	0.2	1.0	3.5	9.0	24.0	38.0	51.0

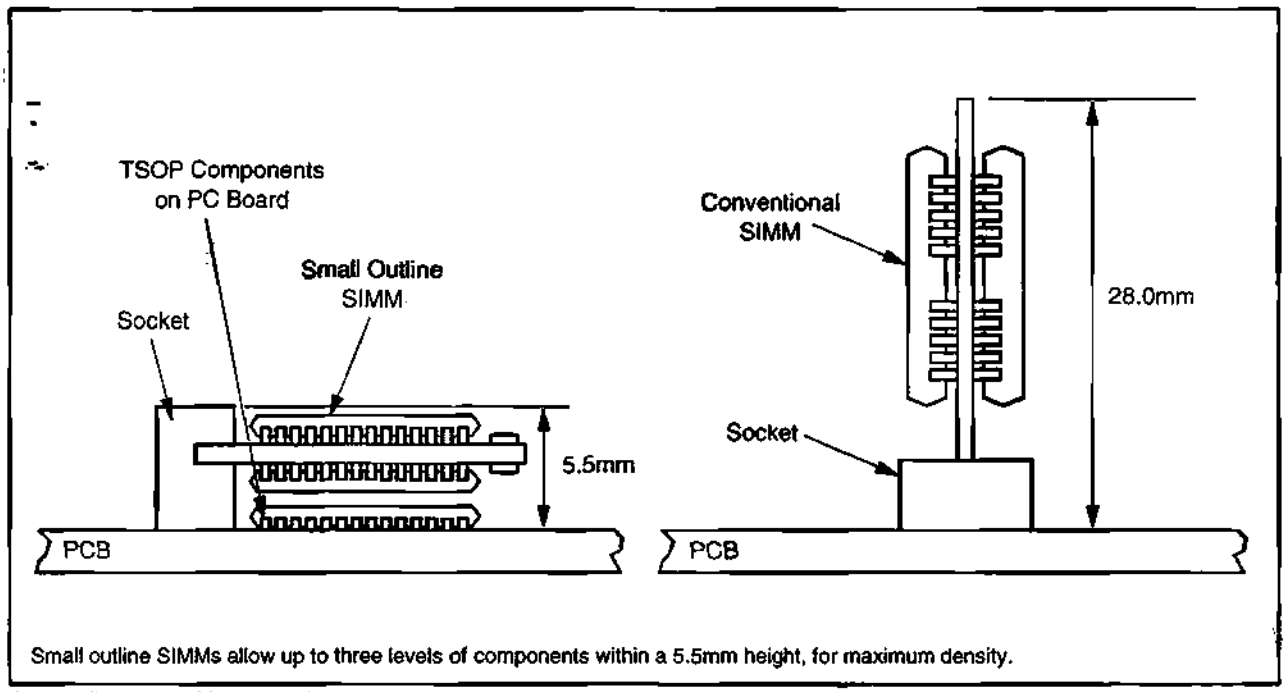
Source: Dataquest (March 1994)

In memory enhancement products, such as SIMMs, which are used to replace the lower-margin, multisourced standard parts, the product mix is evolving toward the x36 SIMM width, with the parity (ninth) bit in some PC clones being eliminated. The transition from the x9 to the x36 configuration is largely because of the rapid design change to x36 modules for high-performance systems requiring a 36-bit (or 32-bit) memory configuration.

To accommodate new low-profile, portable system, and application software demands, some system designers are incorporating new 512K/1Mbx32 small outline SIMMs in an AMP Incorporated M3 socket. The SO SIMM is horizontally mounted in comparison to a vertically mounted standard SIMM (see Figure 3-2). The horizontal SO SIMM allows stacking of three layers of TSOP packaged ICs within 5.5mm, while a standard SIMM height from top to board is 28.0mm. The SO SIMM offers an estimated 50 percent reduction in board space when compared to a standard SIMM and a 30 percent reduction in space in comparison to memory cards.

In the long run, SIMM configurations for DRAMs may not be able to address system demands for higher performance, smaller form factors, and lower power utilization. As vendors are pressured to supply large amounts of memory into smaller confines, newer higher-density DRAM modules such as those shown in Table 3-3 lend a view to stackable modular development for the 64Mb and 256Mb generation of devices expected to emerge in the year 2000 time frame.

Figure 3-2
SO SIMM versus Conventional SIMM



Small outline SIMMs allow up to three levels of components within a 5.5mm height, for maximum density.

Source: Dataquest (March 1994) G4001495

Tables 3-4 and 3-5 list the package data for the slow and fast SRAM products. The slow SRAM products are the slower-than-70ns product categories. The majority of these slow SRAMs continue to serve as inexpensive storage in a variety of applications ranging from consumer, telecommunication, office equipment, and data processing equipment. Although 256K and 1Mb slow SRAMs are still in volume supply, the 4Mb is expected to have some fairly good volume ramp-up in 1994 after early announcements in midyear 1993.

Hitachi, Samsung, and Toshiba were early entrants to the 4Mb slow SRAM market. Certain difficulties with the device include designing with 6T cells. To keep the 6T cell small, the pull-up transistors are being made in the same polysilicon layer that would have been used to make pull-up resistors. The thin-film transistor (TFT) is used only in the manufacture of 4Mb SRAMs and active-matrix LCDs, both of which are emerging technologies. The TFT is effectively used to turn a 4T cell into a 6T cell. The advantages of the 6T cells are reduced power consumption and better soft error rates. The difficulties will be moving to a tighter process and mastering a new technique. The fast SRAMs, specifically the 1Mb and 4Mb densities, are encountering greater changes in package technologies based on the Joint Electronics Device Engineering Council's (JEDEC) "revolutionary" pinout, which departs from the traditional pinouts for the sake of improved noise and speed, and the drive for low-voltage products.

Motorola is offering its family of fast SRAMs in BGA packages to satisfy the need for high-pin-count designs and the new JEDEC revolutionary pinout designs. The revolutionary pinout package has power and ground pins in the center of the package, rather than at the corners. The revolutionary pinouts are being supported by some companies in Japan but are not very popular outside of Japan, where there seems to be a regional preference for the 9-bit width. Acceptance of revolutionary devices such as the 3.3V products is taking longer than anticipated.

Of the nonvolatile products listed in Tables 3-6 through 3-9 , flash memory devices will continue to sustain the greatest package development changes over the traditional EPROM, EEPROM, and ROM families of products. The EPROM market continues to decline slowly. EPROMs are predominantly contained in CERDIP packages with a small percent of OTP EPROMs in TSOPs. AMD, National Semiconductor, SGS-Thomson, and TI are the largest suppliers to the EPROM market. From a unit volume standpoint, the low-density serial EEPROMs continue to maintain volume growth of the EEPROM low-pin-count (8-pin) densities.

The majority of new flash memory announcements have been products available in chip carrier and TSOP packages. The most innovative announcement is from Intel with its new 16Mb dual-die packaging technology. The 16Mb flash memory device is expected to be the battlefield for companies that have not been significant players so far, and most of the new 16Mb announcements have been made supporting TSOP packages.

The low-profile TSOP package is a natural fit for portable computing, telecommunications, automotive, and emerging PCMCIA solid-state storage developments, and those are the market drivers for flash growth.

Logic Packaging

Table 3-10 provides the estimated package type and pin-count percentages for the standard logic families. A survey of the larger standard logic vendors proved startling in that a very large portion (38 percent in 1993) of the product was still produced and consumed in plastic DIPs. There are multiple reasons for this slow switch to surface mount. Bipolar standard logic production represented 48 percent of standard logic in 1993. Of the bipolar products, 41 percent were packaged in DIPs and 58 percent were of SMT. Although vendors were making significant investment to improve capacity to satisfy increased demands for CMOS standard logic families, capacity as yet cannot support demand. As such, the larger systems houses are bearing the cost of new SSOP and TSSOP design development, especially in the higher-performance ABT and AC/ACT fast family of products. Although the SSOP/TSSOP-designed products are doing well in notebook products, PCMCIA designs, and 3V products, the volume is small, and the small designs have created handling problems. Most of the standard logic users (both large and small) remained locked into the older SOIC packaged families, preferring to keep their costs low and maintain a sufficient flow of product. Suppliers of PC modem and LAN cards that follow the PCMCIA dimensions stayed within the more cost-efficient and available HC/HCT family of products, preferring not to pay the hefty price premiums of the AC/ACT products.

Overall, suppliers of standard logic families believe that the greatest transition in standard logic products will begin in the 1994 through 1995 time frame, as a result of transition to 3V designs, a user shift to CMOS/BiCMOS products, and more standard logic capacity. Thus, although the logic vendors are still trying to gauge market shifts, their profit margins are high as long as the need for newer SSOP/TSSOP demand supports their investment. Users incorporating new SSOP/TSSOP board-level designs, unfortunately, can expect to pay hefty price premiums for the next six months.

Tables 3-11 and 3-12 provide the actual and estimated package and pin-count trends by percentage of design starts for gate arrays. Almost 45 percent of 1993 gate array designs in North America were in the 0.9µm-to-1.9µm range and utilized gate counts averaged 38,000, up from 28,000 in 1992. The majority of the low-cost and medium-performance gate arrays continues to be encapsulated in metric QFPs and TQFPs with an outer lead pitch of 0.5mm, with an increased focus on and design of the 0.4mm lead pitch. There was some shift to PBGA packages in the latter part of 1993, as the more than-244-pad PBGA reached price parity with the more-than-240-pad PQFPs.

Table 3-10
Worldwide Estimated Standard Logic Package Forecast

	1992	1993	1994	1995	1996	1997	1998
Total Revenue ($M)	2,492	2,907	3,210	3,445	3,600	3,792	3,749
Percentage of Units							
DIP	42.00	38.00	34.00	30.00	25.10	20.00	15.00
Plastic	70.00	79.50	90.00	95.00	97.00	97.00	99.00
Ceramic	24.00	15.00	5.00	1.00	0	0	0
Side Brazed	6.00	5.47	5.00	4.00	3.00	3.00	1.00
Flatpack	0.50	0.30	0.10	0	0	0	0
Ceramic	90.63	90.60	90.64	0	0	0	0
Side Brazed	9.37	9.40	9.36	0	0	0	0
Chip Carrier	2.00	2.30	2.40	2.00	2.00	2.00	2.00
Plastic	68.00	80.00	88.00	95.00	98.00	100.00	100.00
Ceramic	32.00	20.00	12.00	5.00	2.00	0	0
SO	55.00	58.00	62.00	66.00	69.00	73.00	76.00
Quad	0.50	1.00	1.60	2.00	3.50	5.00	7.00
CMOS	47.80	50.00	55.00	58.40	63.50	68.80	73.50
DIP	35.00	31.00	27.00	24.30	18.00	14.40	11.10
Plastic	64.50	67.89	67.76	67.37	67.08	66.68	66.18
Ceramic	25.31	22.92	23.01	23.29	23.49	23.78	24.13
Side Brazed	10.18	9.19	9.23	9.34	9.43	9.54	9.69
Flatpack	0.26	0.24	0.15	0.11	0.04	0.03	0.01
Ceramic	87.30	88.24	81.82	75.00	0	0	0
Side Brazed	12.70	10.94	17.35	24.31	0	0	0
Chip Carrier	0.33	0.28	0.27	0.27	0.27	0.27	0.28
Plastic	50.00	50.00	50.00	50.00	50.00	50.00	50.00
Ceramic	53.85	50.00	50.00	50.00	50.00	50.00	50.00
SO	64.00	68.10	72.10	74.80	81.20	84.70	88.00
SO	94.00	92.00	88.00	81.00	74.00	65.00	57.00
SSOP	3.00	3.50	5.00	7.00	8.00	10.00	12.00
TSOP	2.50	3.00	5.00	9.00	12.00	17.00	21.00
TSSOP	0.50	1.00	1.50	3.00	6.00	8.00	10.00
Quad	0.44	0.40	0.43	0.49	0.51	0.61	0.59
Quad	99.50	99.00	98.00	93.00	90.00	85.00	80.00
TQFP/VQFP	0.50	1.00	4.00	7.00	10.00	15.00	20.00
Bipolar	51.50	48.00	43.00	37.00	27.00	19.00	11.00
DIP	43.00	41.00	40.00	38.60	37.30	36.00	35.40
Plastic	71.70	82.60	86.00	95.80	96.70	98.00	100.00
Ceramic	22.00	12.00	9.00	0	0	0	0
Side Brazed	6.32	5.44	5.00	4.20	3.30	2.00	0

(Continued)

Table 3-10 (Continued)
Worldwide Estimated Standard Logic Package Forecast

	1992	1993	1994	1995	1996	1997	1998
Flatpack	0.60	0.20	0	0	0	0	0
Ceramic	90.00	90.00	90.00	90.00	90.00	90.00	90.00
Side Brazed	10.00	10.00	10.00	10.00	10.00	10.00	10.00
Chip Carrier	0.73	0.73	0.74	0.76	0.77	0.78	0.80
Plastic	44.18	44.89	44.40	43.59	43.45	43.01	42.62
Ceramic	55.82	55.11	55.60	56.41	56.55	56.99	57.38
SO	55.70	58.10	59.30	60.60	61.90	63.20	63.80
BiCMOS	1.00	1.50	2.30	5.00	9.10	12.00	15.00
DIP	44.00	37.70	30.60	25.50	20.50	14.50	10.60
Plastic	100.00	100.00	100.00	100.00	0	0	0
Ceramic	0	0	0	0	0	0	0
Side Brazed	0	0	0	0	0	0	0
Flatpack	0	0	0	0	0	0	0
Ceramic	0	0	0	0	0	0	0
Side Brazed	0	0	0	0	0	0	0
Chip Carrier	0	0	0	0	0	0	0
Plastic	0	0	0	0	0	0	0
Ceramic	0	0	0	0	0	0	0
SO	55.00	61.00	68.00	73.00	78.00	84.00	88.00
Quad	0.96	1.25	1.44	1.46	1.48	1.45	1.44

Note: Columns may not add to 100 percent because of rounding.
Source: Dataquest (March 1994)

Table 3-11
Worldwide Estimated Gate Array Design Starts, by Package (Percent)

	1992	1993	1994	1995	1996	1997
Total Technology	100.0	100.0	100.0	100.0	100.0	100.0
MOS	79.8	81.3	82.2	82.4	81.9	80.3
Bipolar	15.6	13.0	10.6	8.4	6.3	4.4
BiCMOS	4.6	5.7	7.2	9.3	11.9	15.2
Package Type	100.0	100.0	100.0	100.0	100.0	100.0
DIP	6.0	1.0	0	0	0	0
Quad	59.4	67.0	70.0	72.0	70.0	68.0
Chip Carrier	13.2	8.0	5.0	3.0	1.0	0
PGA	19.7	19.7	16.9	13.4	11.6	10.3
Ball/Land Grid Array	0	1.0	2.0	4.0	6.0	8.0
MCM	0.8	2.0	3.6	4.1	6.7	8.0
COB	0.7	1.0	2.0	3.0	4.1	5.0
Others	0.2	0.3	0.5	0.5	0.6	0.7

Source: Dataquest (March 1994)

Table 3-12
Worldwide Estimated Gate Array Design Starts, by Pin Count (Percent)

	1992	1993	1994	1995	1996	1997
Less than 44	3.0	1.0	0	0	0	0
44-84	14.0	4.0	1.0	0	0	0
85-132	16.0	12.0	9.0	5.0	2.0	1.0
133-195	30.0	34.0	30.0	27.7	25.0	22.0
196-244	22.0	26.0	30.0	32.0	30.0	28.0
244-360	12.0	15.0	17.0	18.0	21.4	23.6
361-524	3.0	7.5	11.0	14.0	17.0	19.0
525-600	0	0.5	1.5	2.3	3.3	4.4
More than 600	0	0	0.5	1.0	1.3	2.0

Source: Dataquest (March 1994)

There are companies qualifying their 1994 gate array and FPGA products in single-layer PBGAs up to 396 pads. Cypress is offering its 8K gate FPGAs in BGAs, and Xilinx is offering a selection of PLDs in a 255-pad PBGA. The more complex high-I/O gate arrays are being supported by the more-than-400-pad TAB BGA, the more-than-390-pad ceramic BGA, and the 500-pin ceramic PGAs. High I/O designs are also being supported in PQFPs with copper heat sink spreaders or heat sinks designed to dissipate heat generated by high-performance microprocessors and peripheral ICs with clock speeds as high as 100 MHz. Compaq has designed-in a 208-pad-plus PBGA gate array for a 66-MHz Pentium-based desktop system.

Microprocessor Packages

Table 3-13 shows the microprocessor forecast by package type and pin count. Figure 3-3 shows the level of activity expected by microprocessor type. From 1992 to 1993, 32-bit microprocessor share increased from 21.3 percent to 51.4 percent. This increased share of growth is expected to continue through 1995 to 61.5 percent. Package styles are expected to shift dramatically in that time frame from ceramic PGA to plastic and ceramic QFP, plastic/ceramic BGA and TAB BGA, and TAB and flip chip to the board designs.

IBM has introduced its latest workstation-based PowerPC products in CQFP packages. The desktop-designed PowerPC 601 with a 10.95mm x 10.95mm die size generates 7W of power, while the 603 low-power version designed for portable applications generates 2W. The next-generation 604 and the 64-bit 620 package designs have not been specified.

AMD's 486SX2 50-MHz processor is being shipped in a 168-pin PGA, while TI is shipping its 486SXL2 66-MHz available in a 100-pin QFP. Overall, increased die size and multilevel cache designs continue to increase microprocessor pin count. At the higher-performance 64-bit RISC superscalar level, the MIPS' 75-MHz TFP (17.2mm x 17.3mm die size) with pipelined cache uses a 591-pin ceramic PGA with 382 signal pins. This and other high-performance 64-bit processors are designed for multitasking supercomputer performance demands.

Table 3-13
Worldwide Estimated Microprocessor Package Forecast (Thousands of Units)

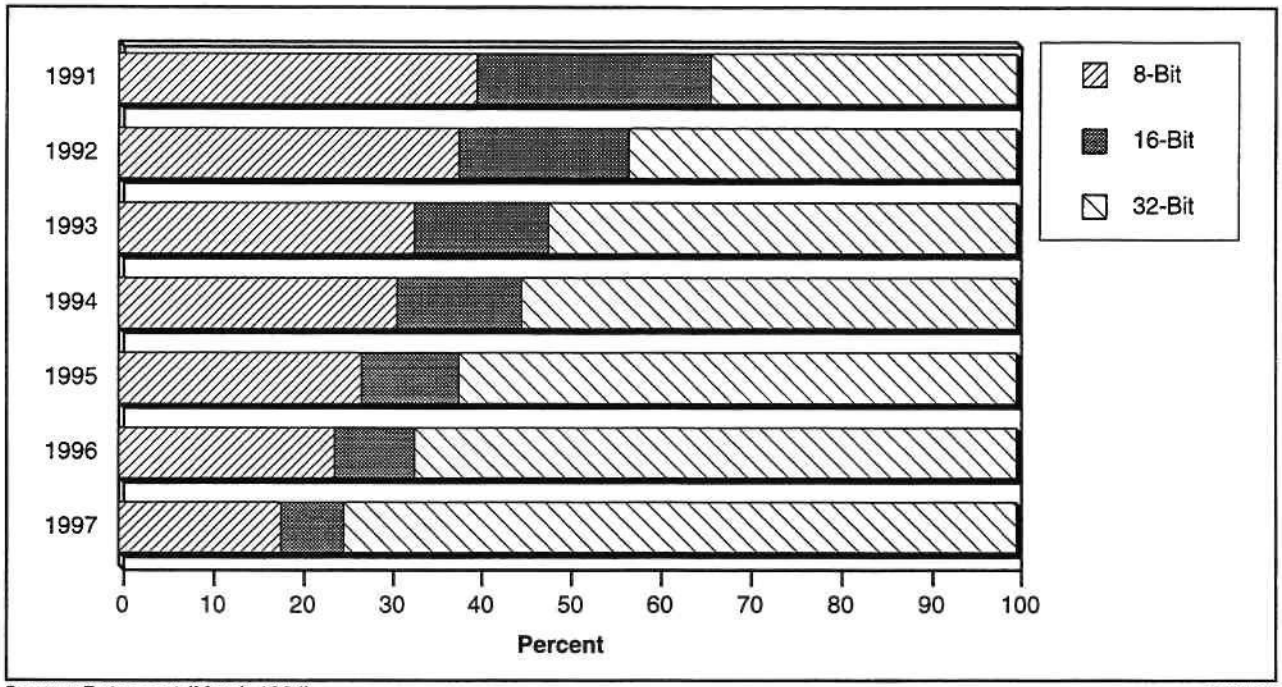
	1992	1993	1994	1995	1996	1997	1998
Total	148,455	180,803	201,965	223,019	245,756	288,885	324,996
Package Total	148,455	180,803	201,965	223,019	245,756	288,885	324,996
DIP	891	362	0	0	0	0	0
Quad	21,378	40,319	47,866	49,733	51,609	57,110	56,649
Chip Carrier	20,932	17,899	12,724	5,352	737	0	0
PGA	103,919	119,330	131,277	147,862	163,919	179,109	175,498
Ball/Land Grid Array	594	1,808	8,079	15,611	22,118	34,666	55,249
Bare Die	742	1,085	2,020	4,460	7,373	18,000	37,600
Pin Count							
40-48	15	2	0	0	0	0	0
52-68	24,500	18,988	9,000	1,000	300	0	0
72-84	35,831	37,704	34,433	26,890	21,000	19,985	14,500
114-128	44,500	54,661	52,300	49,800	45,000	44,700	42,000
132-175	18,566	30,805	47,500	57,611	55,466	55,100	54,100
179-208	16,878	24,543	32,333	43,212	55,718	62,100	61,500
208-408	7,423	12,897	24,211	38,566	53,000	60,100	59,296
408-600	0	18	168	1,480	7,899	28,900	56,000

Source: Dataquest (March 1994)

Analog Packages

Table 3-14 lists the pin count and package forecast for the analog products covered, the linear and mixed-signal product categories. As the analog product was the earliest of the IC product families to adopt SMT, it should not be a surprise to learn that the majority of product consumed in 1993 was available in some form of SMT. More than 90 percent of product produced in 1993 was in the 8-to-24-pin range, with an estimated 12.8 billion units in SO packages. Although mixed-signal designs are targeted for new MCM designs, more than two-thirds of single-chip mixed-signal ICs will be consumed in computer, commercial, and consumer market applications in 1994, with buildup in MCM designs expected to occur in 1995.

Figure 3-3
Worldwide Market Share of Microprocessor, by Product Type



Source: Dataquest (March 1994) G4001496

Table 3-14
Worldwide Estimated Analog Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Mixed-Signal	2,800	3,100	3,400	3,800	4,200	5,000
Linear	12,700	13,800	15,000	16,000	16,500	17,100
Total	15,500	16,900	18,400	19,800	20,700	22,100
Package Type						
Plastic DIP	3,144	2,704	1,656	1,188	1,242	1,105
Ceramic DIP	46	21	10	0	0	0
Quad	1,121	1,352	1,472	1,584	1,863	2,210
Plastic Chip Carrier	348	338	358	198	104	88
Ceramic Chip Carrier	4	0	0	0	0	0
SO	9,122	10,478	12,880	14,652	15,215	16,266
Others	671	845	736	792	828	884
Bare Die	1,045	1,162	1,288	1,386	1,449	1,547
Total	15,500	16,900	18,400	19,800	20,700	22,100

(Continued)

Table 3-14 (Continued)
Worldwide Estimated Analog Package Forecast (Millions of Units)

	1992	1993	1994	1995	1996	1997
Pin Count (Percent)						
Less than 8-Pin	0	1	1	1	1	1
8-Pin	39	36	33	30	28	26
14-Pin	32	34	35	34	32	30
16-Pin	8	7	6	6	5	4
20-Pin	16	16	18	18	20	21
24-Pin	1	1	1	1	1	1
28-Pin	3	3	4	3	4	4
44-Pin	1	2	3	7	9	12
More than 44-Pin	0	0	0	0	0	1

Source: Dataquest (March 1994)

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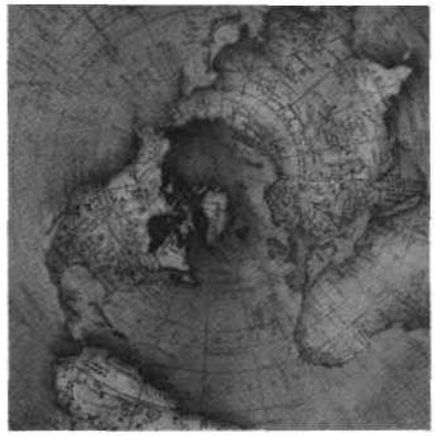

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Integrated Circuit Packaging

Focus Report

Program: Semiconductors Worldwide
Product Code: SEMI-WW-FR-9501
Publication Date: April 24, 1995
Filing: Focus Studies

Integrated Circuit Packaging

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Chapter 1
Introduction

Worldwide Packaging Overview

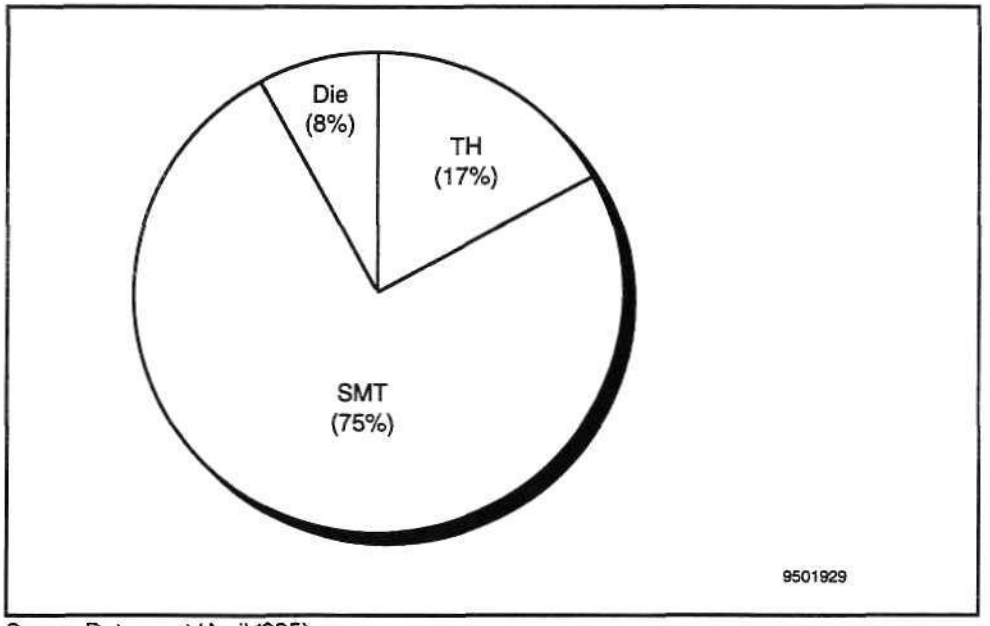
Although it is certainly not surface mount technology (SMT) alone that has created a successful migration path for ICs into new end markets, as a new interconnect technology it did provide competitive cost advantages to leverage entry into developing market applications. SMT enabled much higher density and smaller form factor, and eventually became more cost-effective than its through-hole (TH) counterparts. Eventually it set the stage for quantum leaps in miniaturization and system performance architecture. SMT now represents about 75 percent of total packaged ICs shipped in 1994, with TH technologies declining to 17 percent of total market share (see Figure 1-1). The top performers among the myriad packages are the Quad flat packages (QFPs) and the small outline (SO) packages, as shown on Figure 1-2.

While the suppliers of commodity memory products and low-gate-count ASICs continue to focus on the newer, low-profile, fine-pitch Quarter Size Outline Package / thin SO package (QSOP/TSOP) and thin QFP/very small QFP (TQFP/VQFP) (0.5mm, 0.4mm, and 0.3mm) packages, the 16M SRAMs, 64M-and-above DRAMs, and higher-order ASICs are driving advanced package developments and solutions via 3-D stacked modules and various evolving ball grid array (BGA) configurations. As noted on Figure 1-2, the BGA package represents less than 1 percent of the current market, and bare die represents 10 percent of the 1994 market. Although year-to-year growth for both areas is expected to be quite strong during the next five years, the majority of package designs will be supported by innumerable SO and QFP package styles. The SO family of packages continues to be the mainstay package for analog, standard logic, MOS logic, and MOS memory products. Volume demand and cost efficiencies inherent to the QFP make it the package choice among gate array, microprocessor, and high-density memory and mixed-signal product designers. The QFP package is the current answer to high-performance requirements offering:

- Excellent thermal management
- Reduced inductance
- Standardized package selections
- Proven reliability

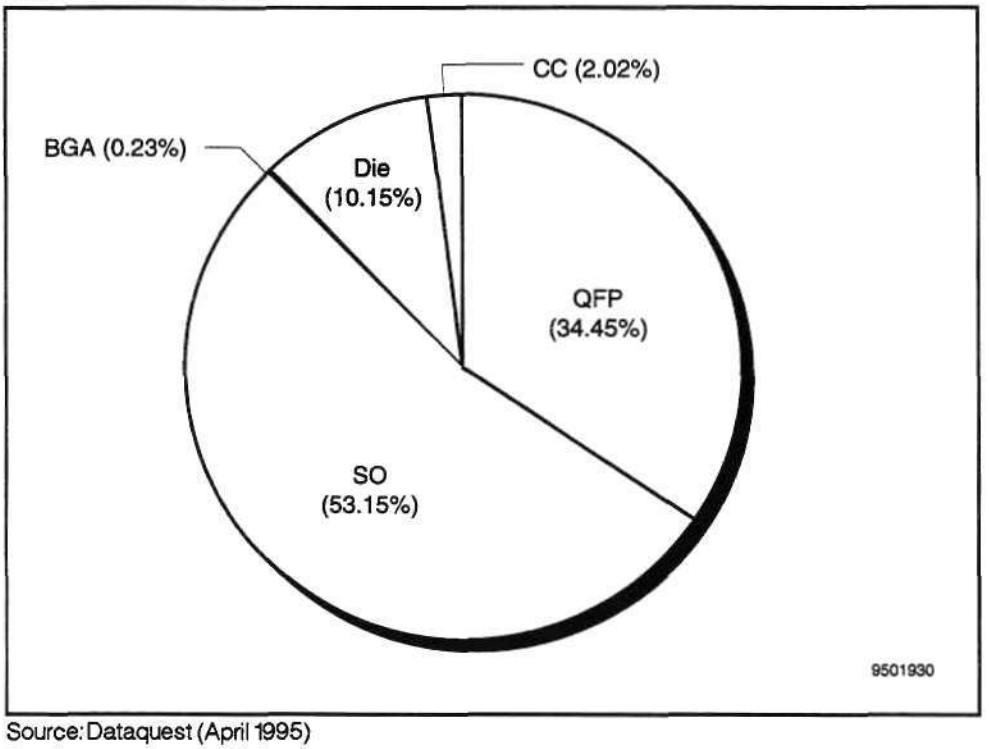
A variety of low-cost thermally enhanced QFPs, available with heat sinks or heat spreaders, in die up or down configurations, are displacing both plastic and ceramic pin grid array (PGA) designs. QFPs and new BGA designs will coexist in the next five years, with QFP remaining the dominant package in volume consumption. BGAs are expected to displace not only ceramic and plastic PGAs in the long term, but also the QFP designs above the 208- to 304-pin-count ranges.

Figure 1-1
SMT Marches On



Source: Dataquest (April 1995)

Figure 1-2
SMT Distribution



Source: Dataquest (April 1995)

BGA Developments

To pinpoint the actual developments of the evolving BGA package use, Dataquest conducted a recent survey to determine direction and use of various BGA package styles. The majority of package suppliers and users stated that new BGA package designs would displace the traditional ceramic and plastic PGA packages, QFPs beyond 300 pins, and quite possibly tape-automated bonding (TAB).

In terms of actual use, as shown in Table 1-1, the majority of volume shipped in 1994 was in the single-core plastic BGAs (PBGAs), or what are often referred to as the OMPAC style, a Motorola acronym.

As the lead pitch of QFPs drops to less than 0.5mm and 0.4mm, the cost efficiencies of QFPs increase and the manufacturing process yields diminish. Table 1-2 lists the production of BGAs by various lead pitch ranges for 1994.

Although the majority of high-pin-count ASIC users are quite comfortable using QFPs at the 160- to 208-pin-count range for the average gate count use required today, a new set of innovative BGA packages are entering the market to accommodate the above-400-pin-package complexity and half-million-gate devices, as well as high-frequency (150-MHz) designs. Table 1-3 lists the average pad count range for suppliers and users of BGA packages in 1994.

Table 1-1
1994 BGA Production

BGA Product	Percentage of Production
Plastic BGA (Single Core)	87
Plastic BGA (Peripheral Array)	10
Enhanced PBGA (Multilayer)	0
µBGA (Tessera Compliant Chip, or TCC)	1
Ceramic BGA	1
Ceramic Column Grid Array (CGA)	0
Tape BGA	1

Source: Dataquest (April 1995)

Table 1-2
Lead Pitch Range (Percentage of Total Production)

Lead Pitch	Percentage in 1994
0.060 Inches	55
0.050 Inches (1.27mm)	14
0.040 Inches (1.00mm)	12
0.020 Inches (0.5mm)	19
0.010 Inches (0.25mm)*	0

*Pitch of direct die mount via flip chip (0.25mm) and TAB (pitch varies from 0.16mm to 0.30mm)
Source: Dataquest (April 1995)

Table 1-3
1994 BGA Pad Count Range (Percentage of Production)

Pad Count	Percent
Less than 44	1
44-84	5
85-132	10
133-195	8
196-244	54
245-308	10
309-475	8
476-672	1
More than 672	3

Source: Dataquest (April 1995)

Although ASICs, specifically field-programmable gate array (FPGA) and gate array products, are expected to be the driving momentum to BGA growth, the survey response shows that the BGA by product use is wide and varied (see Table 1-4).

Table 1-5 shows actual estimated use of BGAs in 1994 in the end system.

Table 1-4
1994 BGA Consumption by Product Technology

Product	Percentage of Total BGA Use
Microprocessor	12
Microcontroller	11
Microperipheral	10
Memory	10
Logic	53
Analog	3
Discrete	1
Multichip Module	Less than 1

Source: Dataquest (April 1995)

Table 1-5
1994 BGA Market Application

Application	Percentage of BGA Production
Data Processing	61
Telecommunications	38
Industrial/Medical	Less than 1
Automotive/Transportation	Less than 1
Military/Aerospace	0

Source: Dataquest (April 1995)

Chapter 2
Worldwide Market Forecast

The worldwide IC packaging forecast and regional developments discussed in this chapter consolidate the IC package products and forecast data for four IC product categories—memory, microcomponents, logic, and analog. Package developments for discrete and optical semiconductors are not available. The product by package type is included in Chapter 3. The regional forecasts and product-specific forecast data are based on the following analysis:

- Dataquest's preliminary 1995 semiconductor IC worldwide forecast
- Dataquest product forecasts
- Survey of ceramic package suppliers' estimates of IC products by package types
- Semiconductor product suppliers' estimates of current and future package designs

The forecast also includes data on bare die shipments. This has been included to follow the potential development of new and emerging chip-to-substrate interconnect schemes that will demand use of bare die and Known Good Die (KGD). These new developments will include 3-D ICs, stackable memory formations and modules, multichip modules (MCM) configurations, chip on tape (COT), flip chip, and TAB.

Dataquest's surveys include data from all suppliers to the merchant semiconductor market. Included are companies that actively market semiconductor devices to the merchant market and to other divisions of their own companies. Both external shipments and internal consumption are included for such companies. Shipment is defined as the purchase of a semiconductor device or devices. This definition must be differentiated from actual use of the device in the final assembled product. A regional market includes all devices sold or shipped to that region.

Worldwide Forecast

Table 2-1 lists all single-chip IC packages and available bare die from 1994 through 1999. A significant decline occurred in all of the through-hole categories (dual in-line package, or DIP, and PGA) in 1994. Although the ceramic PGA market continued on a stable path, buoyed by the growing installed base of the higher-performance Pentium, Alpha, and MIPS processors, the plastic package categories and new enhanced BGA packages are expected to continue to erode the ceramic package base, long a mainstay in hermetic package categories. Figure 2-1 illustrates the market shift from through-hole to the dominant SMT, controlled by small outline and Quad packages.

Table 2-1
Worldwide Package Forecast (Billions of Units)

	1994	1995	1996	1997	1998	1999
Plastic DIP	5,268	4,052	2,967	2,227	1,546	965
Ceramic DIP	1,280	959	623	443	246	178
QUAD	11,167	14,683	17,214	19,152	22,062	24,097
Ceramic Chip Carrier	104	71	60	42	30	16
Plastic Chip Carrier	552	522	494	447	387	320
SO	17,226	20,847	21,748	22,979	24,656	26,730
Ceramic PGA	105	115	120	121	122	118
Plastic PGA	112	117	113	95	83	65
Ball Grid Array	75	253	527	970	1,549	2,420
Bare Chip	3,291	4,617	6,216	7,399	8,435	9,577
Total	39,180	46,236	50,082	53,875	59,116	64,486
Percentage of Total						
Plastic DIP	13.4	8.8	5.9	4.1	2.6	1.5
Ceramic DIP	3.3	2.1	1.2	0.8	0.4	0.3
QUAD	28.5	31.8	34.4	35.5	37.3	37.4
Ceramic Chip Carrier	0.3	0.2	0.1	0.1	0.1	0
Plastic Chip Carrier	1.4	1.1	1.0	0.8	0.7	0.5
SO	44.0	45.1	43.4	42.7	41.7	41.5
Ceramic PGA	0.3	0.2	0.2	0.2	0.2	0.2
Plastic PGA	0.3	0.3	0.2	0.2	0.1	0.1
Ball Grid Array	0.2	0.5	1.1	1.8	2.6	3.8
Bare Chip	8.4	10.0	12.4	13.7	14.3	14.9
Total	100.0	100.0	100.0	100.0	100.0	100.0

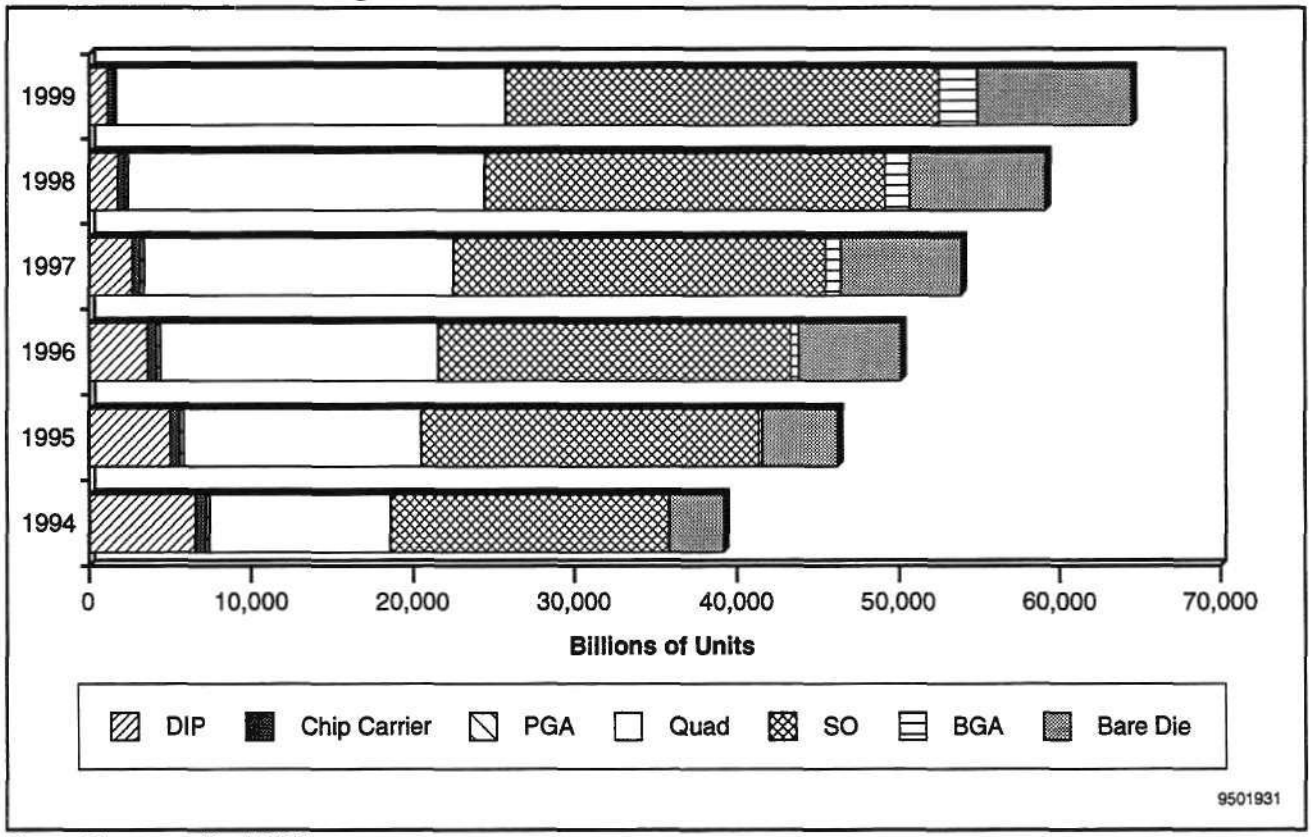
Source: Dataquest (April 1995)

Regional Summary

Table 2-2 lists the IC package use for North America. Although still the largest consumer of TH packages—both DIP and PGA—the region is expected to be the larger consumer of BGA designs during the next five years as Apple, Compaq, IBM, Hewlett-Packard, and Motorola increase BGA system design wins. Table 2-3 lists BGA supplier developments and Table 2-4 lists BGA product designs.

Japan continues to be the largest consumer of SO packages for memory single-chip packages or SIMM configurations for the desktop and portable/handheld market. The forecast demand for bare die, as shown in Table 2-5, has been downgraded from previous forecasts because the original estimate for chip on board (COB)/COT/chip on glass (COG) consumption did not reach the original expectations. Although consumer applications continue to be the largest potential end-use market for bare die, next-generation TSOP/very small outline package (VSOP) and TQFP/VQFP packages continue to sufficiently meet the dimensional board requirements of these applications. Although QFP will continue to be the largest package in demand for high-performance applications in Japan, significant interest and investment are being made in BGA designs by the ASIC suppliers in Japan.

Figure 2-1
Worldwide SMT Package Dominance



Source: Dataquest (April 1995)

Table 2-2
North America Package Forecast (Billions of Units)

	1994	1995	1996	1997	1998	1999
Plastic DIP	2,300	1,800	1,500	1,100	901	655
Ceramic DIP	750	540	320	250	100	85
QUAD	4,062	5,594	6,622	7,041	7,503	8,001
Ceramic Chip Carrier	75	50	44	30	20	11
Plastic Chip Carrier	407	401	384	345	301	245
SO	4,234	5,555	5,890	6,488	7,200	7,432
Ceramic PGA	78	82	85	91	95	96
Plastic PGA	70	74	67	55	45	30
Ball/Land Grid Array	62	225	475	881	1,400	2,120
Bare Die	1,500	1,900	2,570	3,334	3,843	4,555
Total	13,538	16,221	17,957	19,615	21,408	23,230

Source: Dataquest (April 1995)

Table 2-3
BGA Supplier Developments

BGA Suppliers	BGA Products	License
Amkor/Anam	PBGA/PowerQuad SuperBGA (Amkor)	Motorola
ASAT	PBGA/EDQuad	Motorola
Citizen	BGA	Motorola
IBM	CBGA/TBGA/CCGA/PBGA	IBM patents
iPAC	PBGA	Motorola
Kyocera	CBGA	-
Shinko	PBGA/µBGA	Motorola/Tessera
SMOS	PBGA	-
Solectron	PBGA	-
Swire	PBGA	Motorola
Tessera	µBGA	Tessera patent

Source: Dataquest (April 1995)

Table 2-4
BGA Product Designs

Company	BGA Products	Market Application
Altera	EPLD	Desktop/workstation
Compaq	ASICs	Desktop
Hitachi	ASIC/DRAM	Desktop/PCMCIA; servers/workstations
IBM	ASIC/DRAM/MPUs	Laptop/desktop/servers; workstations/PCMCIA; communications
Intel	MPU	PCMCIA/desktop; workstation
LSI Logic	ASIC	Workstation/servers
MicroModule Systems	SRAM/SPARC modules	FDDI/CDDI/servers; workstations/cellular
Micron	DRAM/SRAM	Desktop/palmtop; PCMCIA
Motorola	SRAM/PowerPC/MCUs	Desktop/servers; communications
Pacific Microelectronics	BGA modules	Server/desktop/PCMCIA; communications
Samsung	DRAM evaluation	
Texas Instruments	SRAM/DRAM/DSP	
VLSI Technology	ASIC	Workstation/servers; desktop
Xilinx	EPLDs	Workstation

Source: Dataquest (April 1995)

Table 2-5
Japanese Package Forecast (Billions of Units)

	1994	1995	1996	1997	1998	1999
Plastic DIP	700	600	344	211	105	88
Ceramic DIP	250	198	98	80	62	44
Quad	3,189	3,700	3,890	4,204	4,441	4,601
Ceramic Chip Carrier	10	9	5	3	2	0
Plastic Chip Carrier	45	28	20	20	10	5
SO	4,829	5,433	5,459	5,491	5,800	6,093
Ceramic PGA	20	25	25	20	20	15
Plastic PGA	25	27	30	25	25	22
Ball/Land Grid Array	8	17	34	63	111	223
Bare Die	1,033	1,526	2,126	2,400	2,642	2,800
Total	10,109	11,563	12,031	12,517	13,218	13,891

Source: Dataquest (April 1995)

The European chip card market reached $373 million in 1994. The ever-strong automotive and communications markets are the driving factors for continued strong growth in the SO market (see Table 2-6). As noted in the *Dataquest Perspective* article entitled, "Chip Card Production in Europe" (SAMM-EU-DP-9404), the semiconductor market for chip cards will grow from slightly more than $440 million this year to almost $1.3 billion in 1998.

Table 2-6
European Package Forecast (Billions of Units)

	1994	1995	1996	1997	1998	1999
Plastic DIP	1,550	1,152	723	616	300	100
Ceramic DIP	245	200	187	101	75	45
QUAD	1,976	2,655	3,202	3,692	4,344	4,917
Ceramic Chip Carrier	18	11	10	8	7	5
Plastic Chip Carrier	50	45	44	42	41	40
SO	3,163	3,800	4,096	4,200	4,555	4,899
Ceramic PGA	5	6	7	7	5	5
Plastic PGA	11	10	10	10	9	9
Ball/Land Grid Array	2	4	9	15	22	55
Bare Die	412	721	850	905	1,060	1,122
Total	7,432	8,604	9,138	9,596	10,418	11,197

Source: Dataquest (April 1995)

The number of packages in the Asia/Pacific region declined (see Table 2-7) because of a correction and increase in the industrywide average selling price used to arrive at the actual package production. The Asia/Pacific region now accounts for about 20.4 percent of the worldwide semiconductor consumption, 67.6 percent of which is attributed to consumption in China, Hong Kong, Taiwan, Singapore, and South Korea. The level of growth in SO demand for memory continues to be the largest area of growth for Asia/Pacific because the Korean DRAM suppliers have become fierce suppliers and competitors in the PC market in their region.

Table 2-7
Asia/Pacific Package Forecast (Billions of Units)

	1994	1995	1996	1997	1998	1999
Plastic DIP	718	500	400	300	240	122
Ceramic DIP	35	21	18	12	9	4
QUAD	1,940	2,734	3,500	4,215	5,774	6,578
Ceramic Chip Carrier	1	1	1	1	1	0
Plastic Chip Carrier	50	48	46	40	35	30
SO	5,000	6,059	6,303	6,800	7,101	8,306
Ceramic PGA	2	2	3	3	2	2
Plastic PGA	6	6	6	5	4	4
Ball Grid Array	3	7	9	11	16	22
Bare Chip	346	470	670	760	890	1,100
Total	8,101	9,848	10,956	12,147	14,072	16,168

Source: Dataquest (April 1995)

Chapter 3
Component Interconnect

MOS Memory

Chip scale packaging, 3-D modules, mBGA, and mSMT package designs may be on the horizon as the next generation of packages for MOS memory products, especially with DRAM in the driver seat, but for now both suppliers and users are happy if they can get ample supply of TSOP package designs for single-chip or SIMM/DIMM production. Tables 3-1 through 3-8 list the package data for all of the DRAM, SRAM, EPROM, EEPROM, ROM, and flash products. For DRAMs, as shown on Tables 3-1 and 3-2, the area of greatest change is taking place in the SIMM area, where a significant shift from x9 to x32, x36, and x40 occurred during the fourth quarter of 1994. The product mix began a shift toward the x36 SIMM width in early 1994, with the parity (ninth) bit in PC clones eliminated. The horizontal SO SIMM, which contributed to a 50 percent reduction in board space, continued to grow in use in desktop applications. The dual in-line memory module (DIMM) is a fairly new module design. The 72-pin SO DIMM body width is smaller than the 72- and 80-pin SIMM. The 168-pin, 8-byte DIMM is wider than the 72-pin SIMMs, but will accommodate the third-generation 4M DRAMs, as well as the 400-mil and 300-mil 16M DRAMs and the 500-mil and 400-mil 64M DRAMs in the 1995 and 1996 ramp-up phase. DIMM production represented less than 1 percent of new memory module designs for 1994, according to Dataquest's preliminary survey estimates. DIMM use is expected to grow from 2 to 5 percent in 1995.

Table 3-1
Estimated Worldwide MOS DRAM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998	1999
256K DRAM	89.0	48.0	25.0	8.0	3.0	1.0
DIP	22.3	7.2	1.3	0.1	-	-
ZIP	13.4	6.7	2.5	0.4	0.1	-
PLCC	43.6	27.4	15.8	5.8	2.3	0.8
Others	8.9	6.2	5.3	1.6	0.6	0.2
Die	0.9	0.5	0.3	0.1	-	-
SIP/SIMM	31.4	13.7	7.9	2.9	1.2	0.4
1M DRAM	569.0	353.0	137.0	70.0	46.0	18.0
DIP	16.5	3.5	-	-	-	-
ZIP	56.9	17.7	4.1	0.7	-	-
SOJ/SOP	472.3	317.7	127.4	66.5	44.2	17.3
TSOP	5.7	3.5	1.4	0.7	0.5	0.2
Others	0.6	-	-	-	-	-
Die	17.1	10.6	4.1	2.1	1.4	0.5
SIP/SIMM	283.4	206.5	82.8	43.2	28.7	11.2

(Continued)

Table 3-1 (Continued)
Estimated Worldwide MOS DRAM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998	1999
4M DRAM	1,047.0	958.0	750.0	382.0	338.0	155.0
DIP	-	-	-	-	-	-
ZIP	62.8	47.9	37.5	15.3	6.8	1.6
SOJ/SOP	848.1	766.4	562.5	279.2	244.4	109.3
TSOP	94.2	100.6	105.0	61.1	60.8	31.0
Others	10.5	4.8	3.8	1.9	1.7	0.8
Die	31.4	38.3	41.3	24.4	24.3	12.4
SIP/SIMM	508.8	563.5	433.9	221.2	198.4	91.2
16M DRAM	105.0	308.0	643.0	907.0	789.0	501.0
DIP	-	-	-	-	-	-
ZIP	-	-	-	-	-	-
SOJ/SOP	73.5	194.0	353.7	362.8	236.7	100.2
TSOP	24.2	83.2	192.9	362.8	347.2	240.5
Others	2.1	6.2	12.9	18.1	15.8	10.0
Die	5.3	24.6	83.6	163.3	189.4	150.3
SIP/SIMM	52.9	160.8	327.9	449.9	379.5	238.5
64M DRAM	-	-	5.0	35.0	209.0	401.0
DIP	-	-	-	-	-	-
ZIP	-	-	-	-	-	-
SOJ/SOP	-	-	3.0	19.3	94.1	160.4
Others	-	-	0.5	5.3	41.8	100.3
Die	-	-	1.5	10.5	73.2	140.4
SIP/SIMM	-	-	0.9	6.4	37.6	72.2
256M DRAM	-	-	-	-	2.0	20.0
DIP	-	-	-	-	-	-
ZIP	-	-	-	-	-	-
SOJ/SOP	-	-	-	-	1.1	8.0
Others	-	-	-	-	0.4	6.0
Die	-	-	-	-	0.5	6.0
SIP/SIMM	-	-	-	-	0.3	2.4

Source: Dataquest (April 1995)

Table 3-2
Estimated Worldwide MOS DRAM Module Organization Forecast (Millions of Units)

	1994	1995	1996	1997	1998	1999
256K DRAM, SIP/SIMM	31.4	13.7	7.9	2.9	1.2	0.4
x8	5.0	2.1	1.2	0.4	0.2	0.1
x9	26.4	11.6	6.7	2.5	1.0	0.3
x32	-	-	-	-	-	-
x36	-	-	-	-	-	-
x40	-	-	-	-	-	-
1M DRAM, SIP/SIMM	283.4	206.5	82.8	43.2	28.7	11.2
x8	42.5	24.8	8.3	3.5	2.0	0.6
x9	164.3	113.6	45.5	23.8	15.8	6.2
x32	2.8	2.1	0.8	0.4	0.3	0.1
x36	70.8	64.0	26.5	14.7	10.0	4.2
x40	2.8	2.1	1.7	0.9	0.6	0.2
4M DRAM, SIP/SIMM	508.8	563.5	433.9	221.2	198.4	91.2
x8	25.4	11.3	4.3	1.1	0	0
x9	50.9	28.2	17.4	10.0	9.9	4.6
x32	254.4	326.9	260.3	132.7	119.0	54.7
x36	152.7	169.1	130.2	66.4	59.5	27.4
x40	25.4	28.2	21.7	11.1	9.9	4.6
16M DRAM, SIP/SIMM	52.9	160.8	327.9	449.9	379.5	238.5
x8	0.5	1.6	3.3	4.5	3.8	2.4
x9	2.1	6.4	13.1	18.0	15.2	9.5
x32	31.8	96.5	196.8	269.9	227.7	143.1
x36	15.9	48.2	98.4	135.0	113.9	71.5
x40	2.6	8.0	16.4	22.5	19.0	11.9
64M DRAM, SIP/SIMM	-	-	0.9	6.4	37.6	72.2
x8	-	-	-	-	-	-
x9	-	-	-	-	-	-
x32	-	-	-	0.1	0.8	1.4
x36	-	-	0.5	3.2	18.8	36.1
x40	-	-	0.4	3.0	18.1	34.6
256M DRAM, SIP/SIMM	-	-	-	-	0.3	2.4
x8	-	-	-	-	-	-
x9	-	-	-	-	-	-
x32	-	-	-	-	-	-
x36	-	-	-	-	0.2	1.2
x40	-	-	-	-	0.2	1.2

Source: Dataquest (April 1995)

Tables 3-3 and 3-4 list the package data for the slow and fast SRAMs. Tables 3-5 through 3-8 list package data for all nonvolatile products. The TSOP package is the largest-growing package design for all memory products. The most unique package developed for memory products in 1994 was Intel's 32M flash (16M back-to-back), 56-lead TSOP for use in Type I PCMCIA cards.

Table 3-3
Estimated Worldwide (Slow) >70ns SRAM Package Forecast (Millions of Units)

	1994	1995	1996	1997	1998
16K					
DIP	6.3	3.0	1.8	1.0	0
SOG/SOP	14.7	7.0	5.3	4.0	0
Bare Die	0	0	0	0	0
Total	21.0	10.0	7.0	5.0	2.0
64K					
DIP	40.5	16.2	7.2	4.2	1.8
SOG/SOP	36.5	18.0	9.9	7.2	3.9
Bare Die	4.1	1.8	0.9	0.6	0.3
Total	81.0	36.0	18.0	12.0	6.0
256K					
DIP	24.3	4.2	0.6	0	0
SOG/SOP	145.8	49.8	37.2	30.6	20.4
TSOP	60.8	22.4	18.0	12.8	6.8
Bare Die	12.2	6.6	6.2	7.7	6.8
Total	243.0	83.0	62.0	51.0	34.0
1Mb					
DIP	6.5	3.5	1.6	0	0
SOG/SOP	96.8	115.5	98.4	75.6	50.4
TSOP	19.4	43.8	52.5	53.2	44.1
Bare Die	6.5	12.3	11.5	11.2	10.5
Total	129.0	175.0	164.0	140.0	105.0
4Mb					
DIP	0	0	0	0	0
SOG/SOP	10.2	18.3	24.4	24.2	31.1
TSOP	20.4	43.8	73.2	88.6	113.9
Bare Die	3.4	11.0	24.4	48.3	62.1
Total	34.0	73.0	122.0	161.0	207.0
16Mb					
DIP	0	0	0	0	0
SOG/SOP	0	0.5	1.8	3.2	4.4
TSOP	0	0.3	1.1	3.2	4.4
Bare Die	0	0.3	1.1	3.2	4.4
Total	0	2.0	7.0	16.0	22.0

Source: Dataquest (April 1995)

Table 3-4
Estimated Worldwide (Fast) <70ns SRAM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
16K					
DIP	6.7	4.8	3.8	1.0	1.0
CLCC/PLCC	0.1	0.1	0	0	0
SOJ	0.1	0.1	0	0	0
Bare Die	0.2	0.2	0.1	0	0
Total	7.0	5.0	4.0	1.0	1.0
64K					
DIP	10.1	4.3	0.9	0.1	0.1
CLCC/PLCC	0.7	0.4	0.2	0	0
SOJ	38.2	25.4	11.3	9.4	7.3
SOP	14.7	10.8	4.7	3.8	3.1
Bare Die	3.4	2.2	0.9	0.7	0.6
Total	67.0	43.0	18.0	14.0	11.0
256K					
DIP	19.9	11.1	1.4	0	0
CLCC/PLCC	19.9	17.8	6.8	1.1	0
SOJ	129.4	158.7	105.3	89.9	68.8
SOP	26.9	28.9	16.2	11.8	8.0
BGA	2.0	2.2	1.4	1.1	0.8
Bare Die	1.0	2.2	2.7	2.1	1.6
Others	0	1.1	1.4	1.1	0.8
Total	199.0	222.0	135.0	107.0	80.0
1Mb					
DIP	0.7	0	0	0	0
PLCC	1.4	1.6	2.8	4.1	0
SOJ	56.0	123.2	205.6	285.5	245.6
SOP/TSOP	2.8	6.2	11.0	16.2	15.0
BGA	0.7	1.6	4.1	6.1	5.6
Bare Die	7.0	18.7	41.4	72.9	86.3
Others	1.4	4.7	11.0	20.3	22.5
Total	70.0	156.0	276.0	405.0	375.0
4Mb					
DIP	0	0	0	0	0
SOJ	1.4	4.2	10.0	24.8	56.1
SOP/TSOP	0.1	0.2	0.6	1.9	5.6
BGA	0	0.1	0.2	0.7	3.7
Bare Die	0.2	1.1	4.6	16.7	61.7
Others	0.3	1.5	4.6	17.9	59.8
Total	2.0	7.0	20.0	62.0	187.0

(Continued)

Table 3-4 (Continued)
Estimated Worldwide (Fast) <70ns SRAM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
16Mb					
DIP	0	0	0	0	0
SOJ	0	0	0	0.8	4.3
SOP/TSOP	0	0	0	2.4	12.9
BGA	0	0	0	0.8	4.3
Bare Die	0	0	0	2.4	12.9
Others	0	0	0	1.6	8.6
Total	0	0	0	8.0	43.0

Source: Dataquest (April 1995)

Table 3-5
Estimated Worldwide MOS ROM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
Package Type	461	447	431	457	480
DIP	138	89	43	23	5
SO	231	250	261	320	379
QUAD	12	15	26	32	44
Bare Die	80	93	101	82	52
Pin Count	461	447	431	457	480
24-Pin	0	0	0	0	0
28-Pin	28	21	11	5	1
32-Pin	40	27	19	12	5
40-Pin	125	84	48	31	24
42-Pin	98	112	127	151	160
44-Pin	90	110	125	176	238
Bare Die	80	93	101	82	52

Source: Dataquest (April 1995)

Table 3-6
Estimated Worldwide MOS EPROM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
Total by Package Type	443	406	347	315	294
DIP	258	219	159	126	102
Chip Carrier	80	68	60	53	50
SO	70	73	70	65	62
TSOP	30	35	40	46	50
Bare Die	5	11	18	25	30
Total by Pin Count	443	406	347	315	294
24-Pin	4	2	0	0	0
28-Pin	387	346	289	253	230
32-Pin	22	20	17	16	15
40-Pin	13	16	14	13	12
44-Pin	11	10	9	8	7
Bare Die	5	11	18	25	30

Source: Dataquest (April 1995)

Table 3-7
Estimated Worldwide MOS EEPROM Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
Package Type	460	541	585	683	700
DIP	58	41	34	28	15
Chip Carrier	64	57	51	45	35
SO/TSOP	310	407	454	555	599
PGA	0	0	0	0	0
Bare Die	28	36	46	55	51
Pin Count	460	541	585	683	700
8-Pin	230	253	264	288	304
14-Pin	35	33	30	30	10
24-Pin	30	27	21	20	21
28-Pin	107	130	139	182	190
32-Pin	9	8	8	7	7
40-Pin	14	29	42	57	66
42-Pin	11	25	35	44	51
Bare Die	24	36	46	55	51

Source: Dataquest (April 1995)

Table 3-8
Estimated Flash Memory Package Forecast (Millions of Units)

	1994	1995	1996	1997	1998
Package Total	135.0	206.0	301.0	407.0	545.0
DIP	48.0	38.0	30.0	22.0	17.0
Chip Carrier	10.0	16.0	20.0	21.0	19.0
SO	29.0	64.0	79.0	119.0	142.0
TSOP	44.5	78.0	148.0	207.0	316.0
Bare Die	3.5	10.0	24.0	38.0	51.0
Pin Count	135.0	206.0	301.0	405.0	545.0
28-Pin	15.0	12.0	10.0	8.0	5.0
32-Pin	51.0	68.0	72.0	80.0	55.0
40-Pin	22.0	44.0	62.0	81.0	72.0
42-Pin	11.0	20.0	28.0	36.0	52.0
44-Pin	11.5	22.0	41.0	58.0	80.0
48-Pin	21.0	30.0	64.0	104.0	230.0
Bare Die	3.5	10.0	24.0	38.0	51.0

Source: Dataquest (April 1995)

The area of greatest change in memory device packaging is taking place in SRAMs, specifically high-speed, high-density SRAMs being developed for 100-MHz-and-higher systems. Most of the fast SRAM suppliers all indicated a shift at the 1M-and-above SRAMs to other emerging packages including BGA and TAB. Although most of the memory manufacturers surveyed are either shipping bare die or preparing to ship bare die in 1995, most of the bare die designated as KGD is about less than 1 percent of the total die shipped in today's market. Most of the bare die activity continues to be generated from the SRAM and DRAM suppliers.

The expected ramp in PCMCIA applications and high-performance PCs and workstations, as well as portable computer and communications devices, is expected to promote extensive use of PCMCIA cards and package designs for those applications. Package developments include new microBGAs such as those being developed by Tessera, Hitachi, and Shinko; chip size packaging such as that being developed by Micro SMT Inc., Motorola, and Mitsubishi; and 3-D stacking such as that from Cubic Memory, Irvine Sensors/IBM, and Dense-Pac, to name a few. Although most of the early development in PCMCIA applications was for memory and storage applications, PCMCIA card formats now include the following applications:

- Memory cards: Including ROM, SRAM, DRAM, flash, and EEPROM
- Mass storage
- Modems and fax modems for mobile computers
- LAN adapters for mobile computers
- Wireless LANs

- Wireless wide area network modems
- Combination cards that combine memory with a modem or modem/ LAN adapter technology
- Special-purpose cards with sound capabilities

As noted in Dataquest's *Mobile Computing Worldwide* Focus Report (MBLC-WW-FR-9402), flash memory is a key enabling technology for mobile computers, most specifically standard handhelds and the nearly limitless number of future mobile product paradigms. Some core applications for flash cards are primary storage in the handheld market and as a data transfer medium between mobile computers and desktops. The standard handheld market is expected to take off in 1995, with a total market of 8 million units shipped by 1998. The portable PC and cellular handheld market in the United States reached more than 7 million units in 1994.

The PCMCIA modem cards are expected to achieve the largest area of growth in the long run. Modem vendors shipped 1.4 million PCMCIA base modems in 1994. Portable computers and PCMCIA-based network interface cards grew substantially from 1993 to 1994, with worldwide shipments growing more than 200,000 units by the end of 1994.

Wireless LANs and combination cards represent a significant enhancement in functionality for users' ability to send and receive data and implement multiple technologies on a single card. The special-purpose cards are expected to be the avenue by which desktop functionality such as sound and enhanced video capabilities are added to a mobile computer environment.

As noted in Dataquest's *Removable Magnetic Disk Drives Worldwide* Market Trends report (RMDD-WW-MT-9401), removable storage products potentially will be manufactured by dozens of companies and distribution will work its way through nontraditional channels. It is realistic to imagine that PCMCIA storage cards someday in the near future will be found shrink-wrapped and on shelves. It is also realistic to imagine that all will contain some form or combination of MOS memory devices in single packages, bare die, or stacked die configurations.

MOS Logic

Table 3-9 provides the estimated package and pin-count forecasts for standard logic products. Although vendors continue to make substantial investment in improving TSOP capacity for CMOS standard logic families, the shift to TSOP from small-outline IC (SOIC) continues to move at a very slow pace. Lack of TSOP capacity and the high cost of redesign continue to be the causes behind user resistance to change. Most of the portable PC standard logic users began design-in of SSOPs, TSOPs, and TSSOPs during the second half of 1994.

Table 3-9
Estimated Worldwide Standard Logic Package Forecast (Percent)

	1994	1995	1996	1997	1998
Total Revenue ($M)	3,210	3,445	3,600	3,792	3,749
Percent of Units					
DIP	37.0	35.0	32.0	28.0	21.0
Plastic	90.0	95.0	97.0	97.0	99.0
Ceramic	5.0	1.0	0	0	0
Side Brazed	5.0	4.0	3.0	3.0	1.0
Flatpack	0.1	0	0	0	0
Ceramic	90.6	0	0	0	0
Side Brazed	9.4	0	0	0	0
Chip Carrier	2.0	2.0	1.0	1.0	0.5
Plastic	88.0	95.0	98.0	100.0	100.0
Ceramic	12.0	5.0	2.0	0	0
SO	60.0	62.0	66.0	70.0	77.0
SOIC	84.0	81.0	80.0	78.0	76.0
SSOIC	9.0	10.0	10.0	10.0	11.0
TSOP	6.0	7.0	8.0	9.0	10.0
TSSOP	1.0	2.0	2.0	3.0	3.0
QUAD	1.0	1.0	1.0	1.1	1.2

Source: Dataquest (April 1995)

Table 3-10 lists actual and estimated package and pin-count trends by percentage of design starts for gate arrays. About 30 to 35 percent of 1994 gate array designs in North America were in the 0.7mm to 0.8mm range, and used gate counts averaged 45,000, up from 34,000 in 1993. The majority of medium-gate-count gate arrays consumed today are packaged in the 160- to 208-pin PQFPs. Although there are numerous announcements in new BGA package developments for gate arrays, the BGA market for gate arrays is expected to range from 5 to 9 percent of the total market in 1995.

To accommodate the 280- to more-than-700-lead-count range, both LSI Logic and VLSI Technology Inc. have introduced state-of-the-art products in tape ball grid arrays (TBGAs). Although the low-end PBGA package is addressing the low-cost lower end of the gate array pin-count spectrum (208 pins and below), the ceramic, TBGA, and newer enhanced BGAs are being designed in to new product announcements. Hitachi entered the BGA market using the mBGA package developed by Tessera. The 672-pin BGA is being used for its 3.3V gate array and embedded function array family of 423K-, 545K-, and 667K-gate ASICs. The electrically and thermally enhanced BGAs and TBGAs, and micro BGAs, eventually will lead the ASIC suppliers to flip chip area array attach BGA, and MCM designs.

Table 3-10
Estimated Worldwide Gate Array Designs Package Forecast
(Percentage of Worldwide Design Starts)

	1994	1995	1996	1997	1998
Consumption by Technology	100.0	100.0	100.0	100.0	100.0
MOS Gate Array	79.5	82.5	84.5	86.3	87.5
Bipolar Gate Array	15.0	11.5	8.7	6.3	4.4
BiCMOS Gate Array	5.5	6.0	6.8	7.4	8.1
Package Type	100.0	100.0	100.0	100.0	100.0
DIP	1.0	0	0	0	0
QUAD	69.9	70.0	66.0	58.3	48.5
Chip Carrier	6.0	3.0	1.0	0.8	0.5
PGA	15.0	13.0	11.0	8.0	5.0
Ball/Land Grid Array	4.5	9.0	15.2	22.0	32.0
MCM	2.1	2.8	4.0	6.4	8.0
COB	1.0	1.7	2.2	3.8	5.0
Others	0.5	0.5	0.6	0.7	1.0
Pin Count					
<44	0.5	0	0	0	0
44-84	3.5	1.0	1.0	1.0	1.0
85-132	10.5	8.8	7.0	6.0	5.0
133-195	30.0	27.7	25.0	22.0	18.0
196-244	25.0	28.2	28.3	27.2	26.0
245-308	17.3	18.0	19.3	21.0	23.0
309-475	11.2	13.0	15.0	16.4	18.0
476-672	1.5	2.3	3.1	4.4	6.0
>672	0.5	1.0	1.3	2.0	3.0

Source: Dataquest (April 1995)

MOS Microcomponent

Tables 3-11 and 3-12 show the microprocessor and microcontroller package forecasts. Although microprocessors consume the largest share of ceramic PGAs of all the ICs tracked by Dataquest, the plastic QFP and the emerging ceramic and plastic BGA packages are expected to eventually displace the ceramic PGA as the package of choice. Intel is the largest consumer of ceramic PGAs for its high-end Pentium and emerging P6 products. Intel's shift of the 75-MHz Pentium using a tape carrier package for mobile computing applications signifies a change in tempo for both the market and Intel's package direction. Intel's new TCP Pentium runs on 3.3V power. The weight, size, and cost of the ceramic PGAs over other emerging ceramic or alternate technologies is sounding the death knell for the ceramic PGA.

Table 3-11
Worldwide Microprocessor Package Forecast
(Thousands of Units)

	1994	1995	1996	1997	1998
Package Total	187,820	202,000	220,627	242,862	268,518
DIP	0	0	0	0	0
QUAD	69,637	73,991	75,485	73,112	59,759
Chip Carrier	7,010	4,848	662	0	0
PGA	108,344	114,200	124,000	134,200	145,000
BGA	1,812	6,122	15,466	25,678	45,648
TAB	15	28	41	72	111
Bare Die	1,002	2,811	4,973	9,800	18,000
Pin Count*	186,818	199,189	215,654	233,062	250,518
40-48	0	0	0	0	0
52-68	6,100	800	125	0	0
72-84	28,998	18,000	8,000	3,300	1,000
114-128	50,000	45,000	35,027	16,000	10,000
132-175	44,700	57,111	55,103	50,300	39,218
179-208	32,414	40,378	55,899	66,700	60,300
>208-408	24,433	36,400	54,000	72,985	72,000
>408-600	173	1,500	7,500	23,777	68,000

*Does not include bare die
Source: Dataquest (April 1995)

Table 3-12
Preliminary Worldwide Microcontroller Package Forecast
(Thousands of Units)

	1994	1995	1996	1997	1998
Total Units	2,433	2,765	3,248	3,895	4,665
4-Bit	925	850	790	735	650
Plastic DIP	65	51	32	22	7
Shrink DIP	74	51	24	15	7
Ceramic DIP	19	9	8	7	0
CLCC	19	17	16	15	13
QFP	749	723	711	676	624
8-Bit	1,425	1,800	2,300	2,950	3,750
Plastic DIP	228	252	276	295	300
Ceramic DIP	143	144	138	118	75
PLCC	257	288	322	354	300
CLCC	29	36	46	59	75
QFP/TQFP	684	936	1,288	1,829	2,625
VSO	86	144	230	295	375

(Continued)

Table 3-12 (Continued)
Preliminary Worldwide Microcontroller Package Forecast
(Thousands of Units)

	1994	1995	1996	1997	1998
16-Bit	83	115	158	210	265
PLCC	27	36	47	61	74
CLCC	2	2	3	4	5
QFP	33	44	60	80	101
SO	22	33	47	65	85
Pin Count	2,433	2,765	3,248	3,895	4,665
20	24	28	32	39	47
24	97	111	130	156	187
28	170	194	227	273	327
40	462	525	617	740	886
42	365	415	487	584	700
44	706	802	942	1,130	1,353
48	122	138	162	195	233
52	49	55	65	78	93
56	49	55	65	78	93
64	195	221	260	312	373
80	170	194	227	273	327
84	24	28	32	39	47

Source: Dataquest (April 1995)

Sun Microsystems' SPARC Technology Business introduced its UltraSPARC at 140 MHz to 200 MHz. It will be packaged in a 521-pin BGA. IBM's PowerPC products are being introduced in both ceramic QFP and ceramic BGAs. The PowerPC 620 is encapsulated in a 625-pin BGA. Both products are targeted for the high-performance workstation market. Sun Microsystems ranks as the No. 1 supplier of workstations for 1994, and IBM was listed as No. 3, behind Hewlett-Packard. HP has made substantial investment in both the TAB and BGA market for high-performance workstation end-market applications. Sun's SuperSPARC module 312 I/O for UNIX environments is an MCM (11-die) configuration constructed in a BGA.

The microcontroller package forecast is a new addition to the microcomponent product area in this report. The forecast has been marked "preliminary" because not all survey results were available in time for publication. Dataquest will continue to include microcontroller products in future package reports and will be able to provide further assumptions at that time.

Analog

Table 3-13 lists the pin count and package forecast for the analog products, both linear and mixed-signal. The majority of the analog mix of products are packaged in SO configurations, with the majority in the 8- to 14-pin-count range. The consumption of mixed-signal devices in chipset and MCM designs is moving at a slow but steady pace, with greater market development expected in the 1996 time frame.

Table 3-13
Estimated Worldwide Analog Package Forecast
(Millions of Units)

	1994	1995	1996	1997	1998
Mixed-Signal	3,400	3,800	4,200	5,000	6,650
Linear	15,000	16,000	16,500	17,100	19,100
Total	18,400	19,800	20,700	22,100	25,750
Package Type					
Plastic DIP	1,656	1,188	1,242	1,071	1,040
Ceramic DIP	10	0	0	0	0
QUAD	1,472	1,584	1,863	2,210	2,970
Plastic Chip Carrier	358	198	104	88	76
Ceramic Chip Carrier	0	0	0	0	0
SO	12,880	14,652	15,215	16,200	17,905
Others	736	792	828	984	1,380
Bare Die	1,288	1,386	1,449	1,547	2,380
Total	18,400	19,800	20,700	22,100	25,750
Percentage by Pin Count	100	100	100	100	100
<8-Pin	1	1	1	1	1
8-Pin	33	30	28	26	22
14-Pin	35	34	32	30	30
16-Pin	6	6	5	4	3
20-Pin	18	18	20	21	22
24-Pin	1	1	1	1	1
28-Pin	4	3	4	4	4
44-Pin	3	7	9	12	16
>44-Pin	0	0	0	1	1

Source: Dataquest (April 1995)

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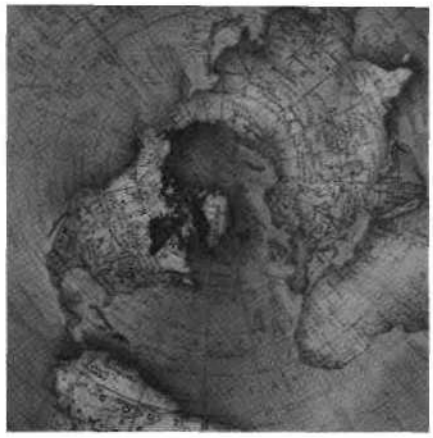

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Integrated Circuit Packaging 1996

Focus Report

Program: Semiconductors Worldwide
Product Code: SEMI-WW-FR-9601
Publication Date: May 6, 1996
Filing: Reports

Integrated Circuit Packaging 1996

Focus Report

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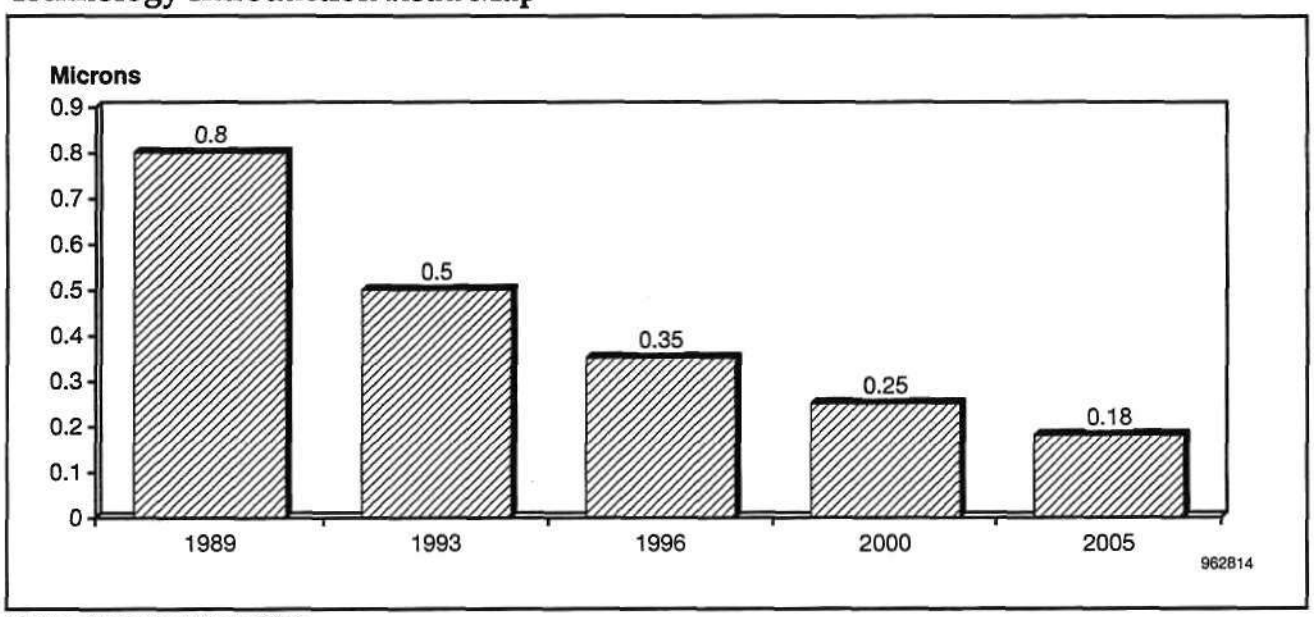
Chapter 1
Reaching the Finite Levels of Technology

System designs integrating gigabits of information and high-speed network switching are driving demand for cost-efficient, high-performance, high-density interconnect solutions. As system, component, and package designers enter the age of networking, they will have to coordinate their efforts in developing packaging, interconnect, and thermal management schemes for next-generation, 0.35-micron to 0.25-micron technology road maps. The road maps of 2000 and beyond, as shown in Figures 1-1 and 1-2, will have to accommodate designs that will be bundling feature-crammed functions in high-speed switching environments that will target the following:

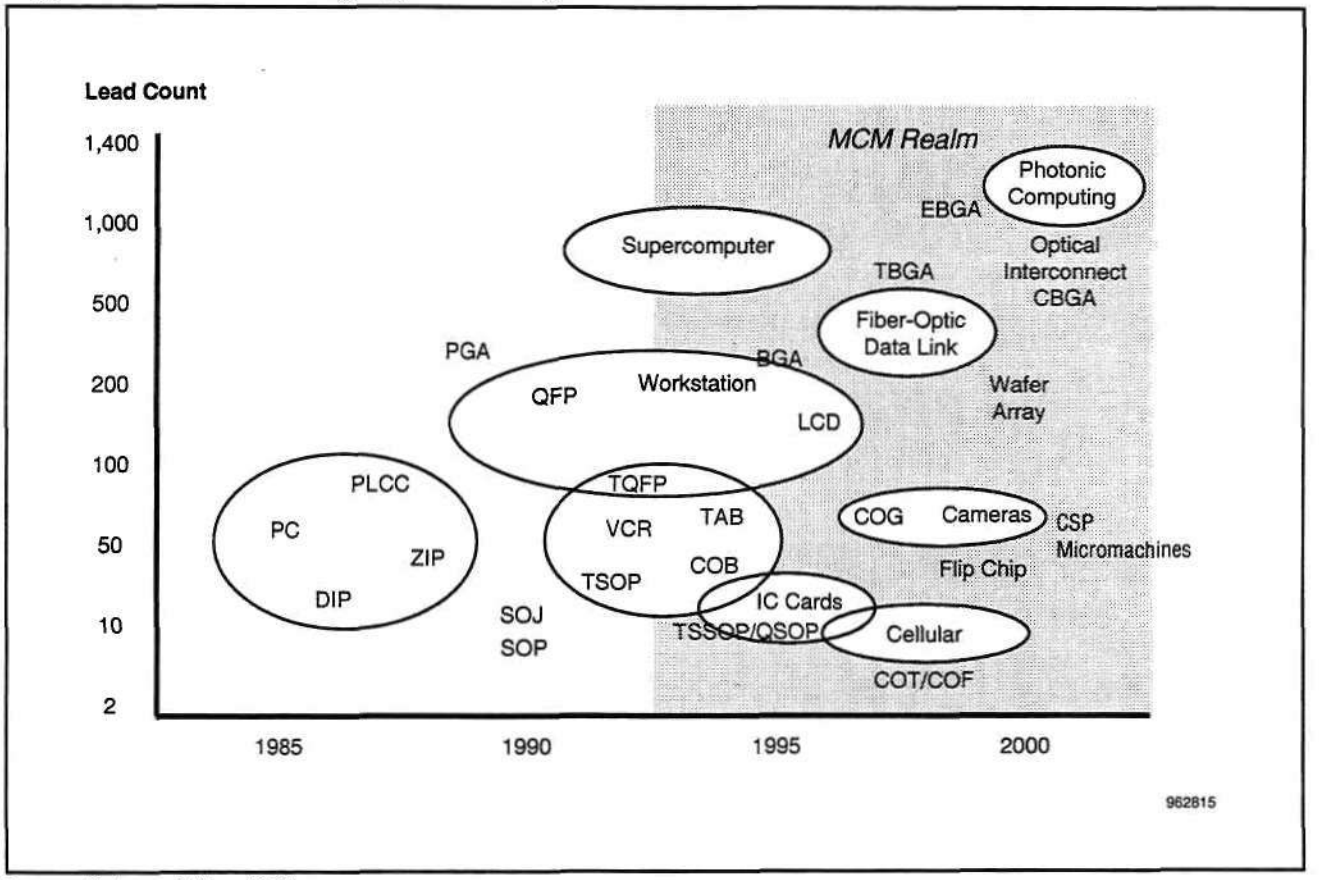
- Advanced video features using 64-bit processing
- Digital video drives
- Voice/data modems
- 3-D graphics
- High-speed Internet-access software

Figure 1-1
Technology Introduction Road Map



Source: Dataquest (May 1996)

Figure 1-2
Application and Packaging Road Map



Source: Dataquest (May 1996)

This complexity of systems and components dictates a cross-functional development effort from design engineering through purchasing that will yield the following:

- Lower cost
- Faster design-cycle time
- Increased manufacturability
- Higher quality products
- Shorter time to market

Although gigabit designs and speeds over 200 MHz are already achievable, as Mitsubishi illustrated in its ISSCC paper on a 1Gb SDRAM prototype in a 0.14-micron process, increasing I/O speed was and will continue to be a challenge. The Mitsubishi prototype exemplifies many of the emerging and future device technologies. Like a feature-crammed system today, the Mitsubishi device is designed in memory blocks with control and clock-generator circuits in each block. The peripheral-circuit blocks include sub-block-generation circuits, array-control circuits, built-in self-test (BIST) circuits, and pad/buffers for wafer test. The peripheral-circuit blocks are connected to global clocks by low-impedance wiring. This is to provide minimum length from pins to memory, minimizing signal delay

while increasing high-speed and high-power performance. Mitsubishi has packaged this device into a new chip-scale package (CSP). According to the company, the use of multiple memory banks, the proximity clock circuitry, and a new chip-scale package design enabled a 40 percent improvement in time from row-address states to data output.

New package developments and strategies such as CSP, flip-chip interconnect, use of known good die (KGD), and multichip modules (MCM), as well as various high-I/O ball-grid arrays (BGAs) will be discussed in this report. Most of these alternative packages to existing surface mount technologies (SMTs) are in the R&D phase or just entering the early life-cycle stages within the electronics industry. These innovative package technologies offer the following:

- Improved package real estate
- Improved performance for higher I/O (>300 I/O)
- Improved power dissipation

Bare Die/KGD

Historically, the majority of semiconductor suppliers have produced bare die products—unencapsulated individual silicon chips shipped with minimal testing. Most of the bare dice shipped worldwide have been consumed in the hybrid market, with growing numbers consumed as chip-on-board (COB), wire-bonded to the board with a glob-top coating; chip-on-tape (COT); chip-on-flex (COF), direct bonding of a device to a flex substrate; and in MCMs. Most of the COB and COT dice are designed in consumer (games, cameras, and appliances), mobile, and communications (fax/modem cards and cellular) applications. COF is one of the more innovative developments for use in military, pager, and computer (handheld, organizer, and subnotebook) applications.

Aside from the experienced MCM system designers such as Boeing, Hughes, IBM, Fujitsu, NEC, Texas Instruments, Motorola, Digital Equipment Corporation, and Unisys, there was no market, no consensus, and no standard for KGD in the merchant market through 1992. The KGD Project of the United States-based consortium Microelectronics and Computer Technology Corporation (MCC) was established in 1993 and supported by a $500,000 Advanced Research Projects Agency (ARPA) contract. Phase I of the KGD Project was established to assess approaches for KGD and to develop KGD guidelines. Two KGD workshops later, MCC entered Phase II of the project, with strong support from Sematech, the Electronics Industries Association (EIA) Multichip Module Division, and a host of industry participants.

By 1995, attendance at the KGD Workshop had doubled in size over the 1994 KGD Workshop. The 1995 workshop was a combined effort of MCC and Sematech with membership support from the Multichip Module Division of the EIA. The workshop sessions covering KGD markets and technologies were chaired by semiconductor suppliers and systems users of KGD, CSP, and flip-chip interconnect.

Potential users would prefer to define KGD as unpackaged products priced below packaged parts. However, cost, test, and even supplier definitions for KGD vary by supplier and application. A general definition for KGD is unpackaged IC chips, ready for assembly, and guaranteed to meet performance and reliability requirements. For some products and applications, KGD parts have been tested like packaged parts (full AC/DC testing), and they function over a specified speed and temperature. But the levels of testing needed for KGD also vary by supplier and application. Burn-in is the process whereby packaged devices are operated for a period of time in a harsh environment to cause the weak devices to fail. Again, the level of burn-in required will vary by product and application.

There is now a small, but emerging group of KGD suppliers to the merchant market. Table 1-1 lists a selection of semiconductor suppliers that currently offer various KGD products. Consensus by the participating suppliers is that, although there are varying degrees of KGD definitions as well as products on the market, KGD usage is increasing.

The following are bare die distributors and their carrier technology:

- Chip Supply Inc.
  - SofTab
- Die Technology Ltd. (United Kingdom)
- ELMO Semiconductor Corporation (acquired by Kimball International Inc. in March 1996)
- EPI Technologies Inc.
  - EPIK
- Minco Technology
  - EPIK, DieMate
- Semi Dice Inc.
  - ETEC

Phase II of the KGD Project is the evaluation of commercially available carrier technologies for unpackaged dice. As defined by Sematech/MCC, a carrier is a vehicle that would allow a die to be loaded and transported through a typical packaged IC production burn-in and test process. It would support burn-in and test functions, yielding fully conditioned dice. It would also mimic the characteristics (environmental protection, electrical contact, and handling) provided by an IC package. Carrier technologies being evaluated are as follows:

- Soft connection—a nonstandard connection to a reusable standard package type (any metallurgical connection is a soft connection). Examples include Chip Supply's SofTab and ETEC's Flip Chip Interconnect (FCI) process.

Table 1-1
Suppliers of Bare Die/KGD Products

	Logic			Microcomponents				Memory		
	Chipsets	Standard Logic	ASIC	MPU	MCU	Micro-peripheral	Analog/ Discrete	DRAM	SRAM	Nonvolatile
Advanced Micro Devices				x						
American Microsystems Inc.			x							
Analog Devices Inc.							x			
Atmel			x							
AT&T			x							
Fujitsu			x							
Harris		x	x							
Hitachi								x		
Honeywell SSEC			x						x	
IBM			x	x					x	
Integrated Device Technology				x					x	
Intel	x			x						x
International Rectifier							x			
LSI Logic			x							
Micron								x	x	
Motorola				x					x	
National Semiconductor		x					x		x	x
NEC				x				x		
Paradigm									x	
Philips							x			
Samsung								x		
Siemens								x		
Siliconix							x			
Texas Instruments		x						x		
Toshiba								x		
Unitrode							x			
Xilinx			x							

Source: Dataquest (April 1996)

- Temporary contact—microprobe sets are built into carriers that are made to mimic standard packages (can be assembled with or without a metallurgical joint). Examples include Aehr Test System's DiePak, IBM's Dendrite, Packard-Hughes Interconnect's contractor membrane probe, Sandia National Laboratories' MiniBGA, Texas Instruments'/MMS' DieMate, and the Yamaichi application-specific material (ASMAT) thin-film interconnect. IBM's dendrite technology was qualified in 1994. It provides a mechanical interconnection between the die C4 ball and dendrite on a ceramic carrier. IBM's dendrite technology has finger-like contacts that are plated with palladium, resulting in a conductive, stalagmite-like topology. The ASMAT interconnect was developed by Nitto Denko Corporation. ASMAT interconnect is also the basis for the Aehr Test System carrier.
- Chip-scale packages or minimally packaged devices are thin packages that are chip-size or part of the die. Examples include Tessera's microBGA, ChipScale Inc.'s chip-scale package, and Mitsubishi's chip size package, which has surface pads similar to those on a BGA package.

Other new carrier products include waffle packs and a new technology involving vacuum release trays. One vacuum release tray that is readily accepted by die/wafer suppliers and distributors is the Gel-Pak carrier. Gel-Pak, a division of Vichem Corporation, manufactures a tray containing a gel membrane that holds components or wafers that are released at the assembly site by drawing a vacuum under the tray. Dice or wafers are released from the membrane mask and can be lifted off of the tray with either tweezers or vacuum pickup tools. Another carrier technology approach is the QC^2, a no-socket approach developed by National Semiconductor Corporation and Fresh Quest Corporation.

Sematech also established its Low-Cost KGD Project in 1995. The project focuses on low-cost manufacturing and total system (module) solutions. The Sematech KGD project consists of members from Advanced Micro Devices, AT&T, Digital, Hewlett-Packard, IBM, Intel, Motorola, National, Rockwell, and TI.

The Wafer-Level KGD Consortium funded by ARPA in 1995 includes AMD, Harris, Hewlett-Packard, Motorola, and National Semiconductor. The project centers around a probe technology that would produce wafer-level probe cards for burn-in. Phase I Test Program WL/KGD, begun July 1995, is the evaluation of probe coupons. The goal is to evaluate probe coupons for 8-inch wafers of memory die product. The target bond pad metallurgy is aluminum.

Diamond Tech One Inc. (DTO), a subsidiary of Diamond Technology Inc., is working with Aehr Test Systems in a technology development agreement on advanced substrates to be used in wafer-level test and burn-in equipment. Aehr Test will build the substrates, and DTO will do the bumping technology. DTO's bumping process deposits flexible polymer onto a substrate and coats in a thin layer of conductive metal (generally gold) to produce a reliable, manufacturable, and reworkable connection. Aehr Test is developing a wafer-level burn-in and test system that will allow burn-in and test before packaging, while the dice are in wafer form.

Potential users would prefer to define KGD as unpackaged products priced below packaged parts. However, the supplier definitions of KGD, which are unpackaged IC chips, ready for assembly, and guaranteed to meet performance and reliability requirements, as well as the cost, vary by supplier and application. For some products and applications, KGDs have been tested like packaged products (full AC/DC testing), and function over a specified speed and temperature. But the levels of testing needed for KGD vary by supplier and application. Burn-in is the process whereby packaged devices are operated for a period of time in a harsh environment to cause the weak devices to fail. But the level of burn-in required will vary by product and application.

The availability and demand for KGD is obviously in a nascent phase, as definition battles are still being waged among industry experts. In addition to a multiple set of activities at the front end from semiconductor suppliers and foundries, additional infrastructure is being added at the back end for KGD. Table 1-2 lists equipment participants currently involved in KGD.

The applications driving semiconductor growth today and into the next decade are smaller, faster, and more cost-driven than ever. Although existing SMTs continue to evolve and satisfy the needs of most system designs, the complexity of ultralarge-scale integration (ULSI) devices, continuous die shrinks, and emerging ICs are making costly demands in evolving package designs. According to most of the major semiconductor manufacturers and board assemblers, a prerequisite for high yield manufacturing in 1996 and 1997 either in the fab or at system and assembly levels is the ability to have reliable die—either as KGD or in a known good package, such as CSP. KGD and CSP reduce rework and the high costs associated with rework. For many package and board assemblers, rework is today's hidden factory. It is an added cost burden that is eroding profits at all levels of the electronics industry. As semiconductor suppliers and users incorporate more complex functions in high-performance ASICs, microprocessors, and memory devices, rework will become cost-prohibitive.

As Gordon E. Moore stated in his paper, "Lithography and the Future of Moore's Law" (SPIE, International Society for Optical Engineering, Volume 2440, page 17, February 1995), by making things smaller, everything gets better simultaneously. As the speed of products goes up, the power consumption goes down, and as we put more of the system on a chip, system reliability improves by leaps and bounds, but especially the cost of doing things electronically drops as a result of the technology.

KGD availability is no longer the essential product for just MCM growth. KGD availability is now essential for other direct chip attach (DCA) applications such as PCMCIA, flat panel displays, and stackable memories. As shown in Figures 1-3 and 1-4 from Intel Corporation, the use of KGD, or SmartDie products, enabled designers to put more functionality within the same PCMCIA form factor. For example, using five die products instead of packaged devices on a fax/modem card resulted in a 2.6:1 area reduction and a 3.4:1 volume reduction. Without the package, a 5:1 reduction in circuit board is possible.

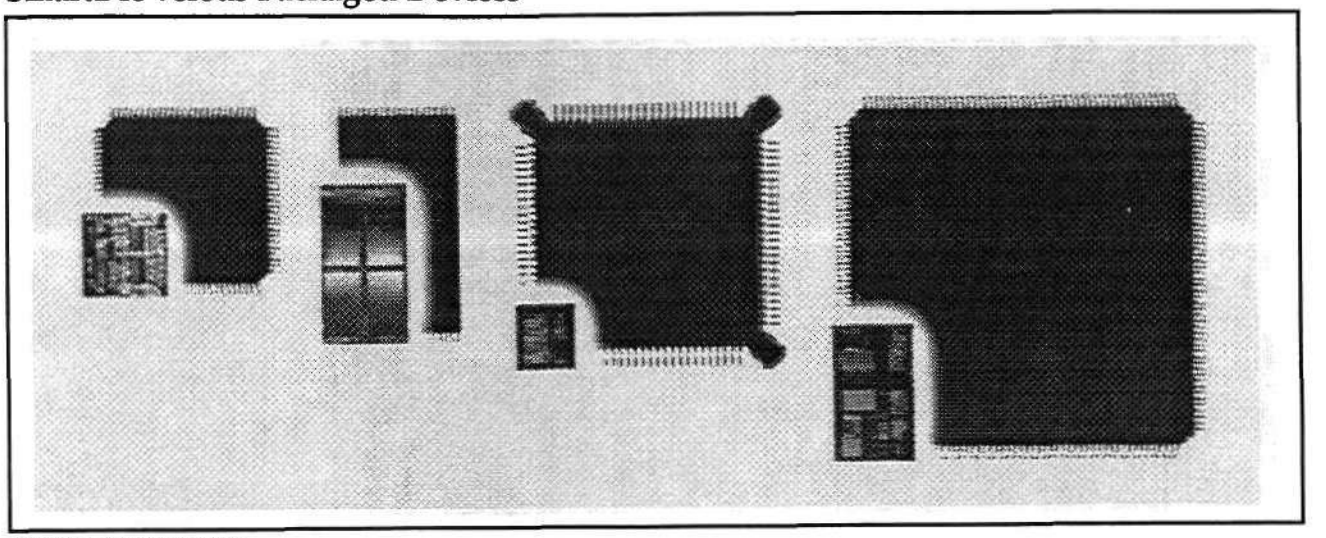
As the KGD infrastructure builds and demand for bare die increases across all applications, we expect KGD volume demand to build in North America. Figure 1-5 is the estimated growth for KGD in comparison with bare die availability.

Table 1-2
Equipment Suppliers for KGD

Company	Burn-In and Test	Die Loaders	Die Shipping	Probe Cards and Interposer	Package Loaders	Tape and Reel	Dicing	Die Test and Inspection
Aehr Test System	x							
AMTI/Zevatech		x						
Cerprobe				x				
Cybex Technology		x						
Delta					x			
Disco Hi Tech							x	
EPI Technologies								x
Fluoroware Inc.			x					
Gel-Pak			x					
Hughes		x						
Intelmatec					x			
Laurier Inc.		x						
MCT					x			
MRSI		x						
Packard-Hughes				x				
Royce Instruments		x						
Tempo						x		
Temptronic	x							
Viking Semiconductor		x						

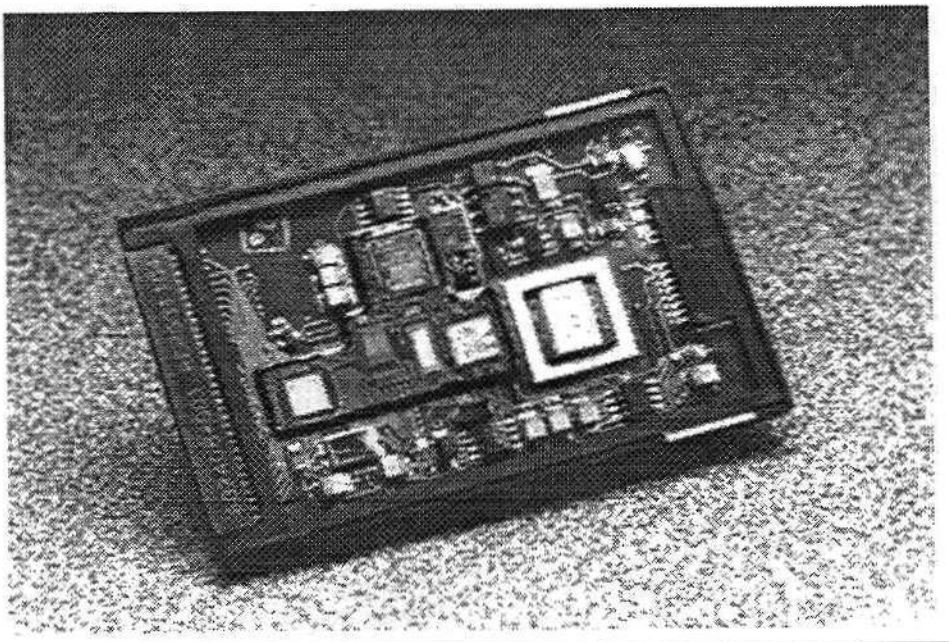
Source: Dataquest (April 1996)

Figure 1-3
SmartDie versus Packaged Devices



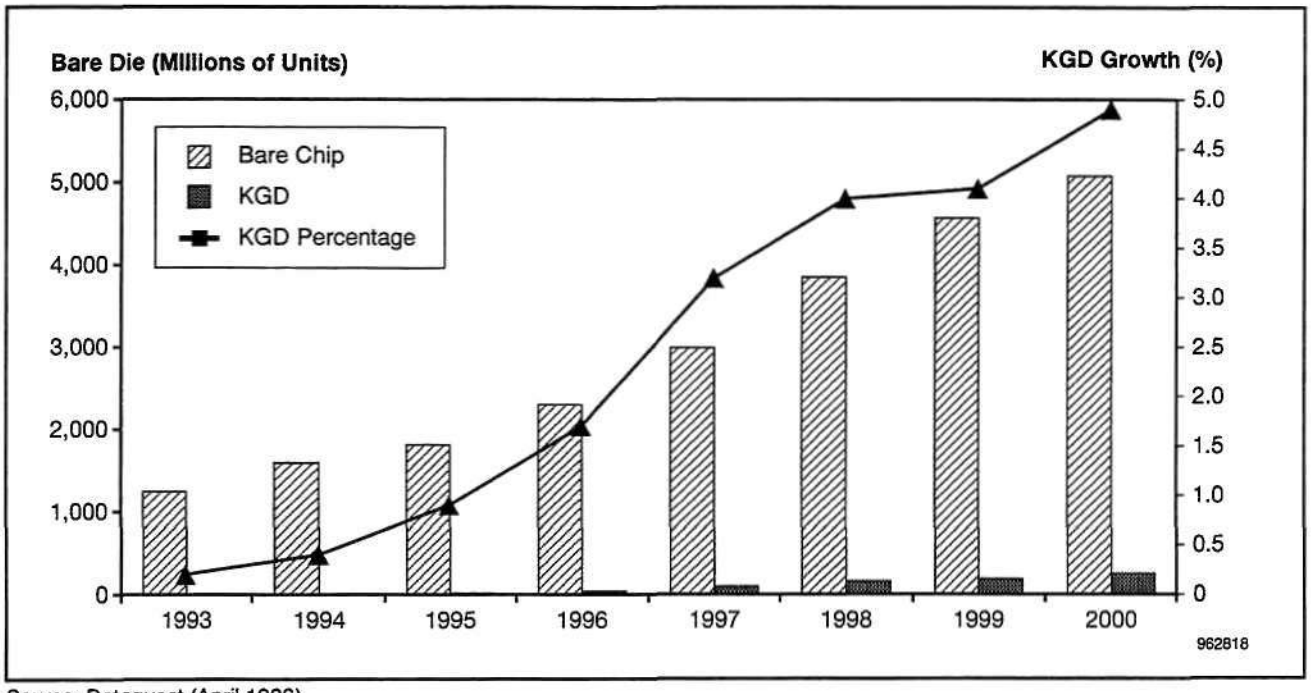
Source: Intel Corporation

Figure 1-4
Fax/Modem Card



Source: Intel Corporation

Figure 1-5
Estimated Growth of Bare Die and KGD



Source: Dataquest (April 1996)

Successful KGD suppliers will be among the companies listed in the first table in Chapter 1, as well as the companies that have formed strong partnership agreements to support the infrastructure. In the formation of its SmartDie program, Intel formed strong alliance agreements with Anam/Amkor, Jabil Circuits Inc., MicroModule Systems, SCI Systems Inc., S-MOS Systems, Solectron, and Valtronic. Micron Semiconductor Inc. and nChip Inc. have a license agreement on Micron's KGD^{plus} technology silicon contact insert method for KGD production. The two companies are also working with 3M Electronic Products (sockets and carriers) and Cybex Technology (loaders/unloaders). An early user of KGD in its mainframe products, IBM has been supplying KGD as well as waffle packs and bumping processes to the merchant market since 1992.

CSP Development

Chip-scale packaging is a minimal package technology. The package is formed either at the wafer-level process, where the package is etched from the wafer from which the IC is formed, or a thin package is formed around the die, with die connections made by a flexible interposer that interconnects to leads or solder balls. Although there have been numerous package developments that are being referred to as CSPs, the package size is usually less than 1.2 times the chip size. CSP technology can enhance the supplier or user capability in test and burn-in, thus offering a known good package, and can be assembled using existing SMT assembly methods. Various chip-scale designs include the Micro SMT (0.2mm pitch) from Chip Scale Packaging, Tessera's MicroBGA (0.5mm pitch), Archistrat's Very Small Peripheral Array (VSPA, 0.5mm to 0.8mm pitch), Mitsubishi's chip-scale package (0.4mm pitch), Motorola's slightly larger than IC chip

carrier (SLiCC), Micro Substrates Corporation's (MSC's) Via/Pak BGA, ShellCase's ShellStack and known good package, and Sandia National Laboratories' mini-BGA package. NEC has also announced development of a CSP design.

The Institute for Interconnecting and Packaging Electronic Circuits (IPC), EIA, and Sematech have released J-Std-012, *Implementation of Flip-Chip and Chip-Scale Technology*, as a working document in development of package, design, and production standards for CSPs. The Joint Electronics Device Engineering Council (JEDEC) JC-11 committee is currently evaluating several documents involving thin fine-pitch BGA or chip-scale package technologies. In terms of market size, CSP is still too close to the prototype to very small production volume level even to define itself as a market. Motorola, with its strength in the discrete market, may drive the initial ramp-up and acceptance of this package technology. The analog and DRAM products are likely candidates for CSP packaging around 1997 and 1998. The 64M device will be entering production levels at that time. Several companies are in CSP prototype stage for their 16M DRAMs. The lead on chip approach can also be included in the CSP category because the memory chip is about 90 percent of the package area. Package spacing is reduced because space required for wire bonding is within the periphery of the chip rather than on the outside of the chip. Originally patented by IBM, LOC is being used by Hitachi and Texas Instruments.

CSP Vendors

Chip Scale Packaging's Micro SMT package, recently licensed to Motorola for discrete package development, was introduced in 1990. The technology has been used in microwave diodes. According to Chip Scale Packaging, future product developments include transistors, radio frequency (RF), stacked memories, and analog and low-lead count ICs. The technology allows for package formation at the wafer fabrication process after the active IC is complete. Volume production of the Motorola Micro SMT product is expected in the third quarter of 1996.

Tessera's MicroBGA package has been licensed by Hitachi, Shinko, 3M and Amkor. Tessera, founded in 1990, has designed a nearly die-size package that can be tested at speed and burned in before final assembly to a substrate. Tessera's technology involves a chip carrier interconnect that is the same size or slightly larger than the chip. According to Tessera, the chip is attached to Tessera's flexible circuit package by a nonconductive elastomeric pad that allows for testing in a socket. Rockwell International is using the microBGA package for a Global Positioning System receiver.

Mitsubishi's chip-scale package uses a thin plastic resin coating around the chip. Signal traces are routed from electrode bumps on the bottom of the IC to solder bumps that have been added after several wafer fabrication levels. Mitsubishi's CSP designs will focus on memory products.

Archistrat's VSPA design has multiple rows of leads around the package. The package base is metal, and side walls are insulated with Vectra, a plastic material. A plastic carrier is molded around the thermal conductor and leads. Leads are stamped to form and plated before insertion. Archistrat has contracted with IBM to build the automated tools for high-speed insertion of pins in the VSPA package.

MSC's Via/Pak BGA is a low-cost ceramic BGA design. The company's patented process uses wafer-scale processing and via-plane thin-film technology. The company uses a substrate 5 inches to 6 inches square to produce the package. The substrate is lapped and polished for planarity and finish. Titanium is sputter-deposited as an adhesion layer, followed by a layer of copper, which is plated with nickel and gold. Photopatterning defines the conductor routing for 2-mil lines and spaces. The package uses tungsten-copper vias for signal, power, and ground pins.

ShellCase, located in Jerusalem, with investment from Toyo Ink Manufacturing and Intex Corporation (both of Japan) offers two chip-scale-like package developments. One package is similar to a shell 100 microns wider and longer than a die. The shell package allows for KGD testing before assembly. The dice are packaged and encapsulated in wafer form.

Flip-Chip Interconnect

Recently referred to as IBM's long-dormant technology, flip-chip interconnect activity worldwide and especially within IBM is far from a state of suspended animation, and this is no longer a technology that only IBM can afford. Initially patented and developed by IBM for the System/360 around 1964, flip-chip attach technology is now widely used by companies for microprocessors, ASICs, and SRAMs, performance-constrained designs, ultrahigh pin count designs, and in pad-limited designs. Table 1-3 lists flip-chip activity by supplier.

Flip-chip is a direct chip attach technology where bare die is attached to a substrate upside down after spheres of solder (50µm to 125µm in diameter) are bumped in an array on the bottom of the chip before attachment to the substrate. Because the solder bumps can be placed over the entire surface of the die, some of the major benefits of flip-chip attach are:

- Enhanced electrical performance
- Reduced silicon real estate
- Higher package density
- Tighter assembly tolerances (<1µm)
- Self-alignment during reflow
- Ease of repair

Flip-chip was originally referred to as the IBM C4 process (Controlled Collapse Chip Connection; patents 3,401,126; 2,961,416; 3,429,040; and 3,401,055). This wet solder reflow method was based on limiting the solderable area of the substrate lands and chip contact terminals so that surface tension in the molten pad and land solder supports the device until the joint solidifies. Substrate pads were coated with tin/lead solder. IBM has expanded flip-chip technology with various substrates and underfills. Various methods of forming solder balls on wafers now include the following:

- Evaporation—IBM C4 process
- Electroplating

Table 1-3
Flip-Chip Technology Activity

Company	Logic/ASIC	MPU/DSP	Analog/ Discrete/Opto	Memory	Bumping	Assembly	Materials	Equipment/ Probe
Adept								x
Alpha Metals							x	
AMTI/Zevatech								x
Aptos					x			
Asymtek								x
AT&T					x	x		
Balzers								x
Celestica					x	x		
Cherry Semiconductor			x					
Coors Electronic Package Co.							x	
CyberOptics			x					
Delco			x		x	x		
Dexter							x	
Epoxy Technology							x	
Flextronics					x	x		
Flip Chip Technologies*					x			
Fujitsu	x	x	x	x	x	x		
General Electric			x		x	x		
GEC-Plessey	x		x					
Gore & Associates							x	
Hewlett-Packard			x		x			x
Honeywell			x					
Ibiden							x	
IBM	x	x		x	x	x		x
IMI					x			
Intel		x						
IRT								x
New Japan Radio Corp.			x		x	x		

(Continued)

Table 1-3 (Continued)
Flip-Chip Technology Activity

Company	Logic/ASIC	MPU/DSP	Analog/ Discrete/Opto	Memory	Bumping	Assembly	Materials	Equipment/ Probe
Kulicke & Soffa								x
Kyocera							x	
Laurier Inc.								x
Matra					x			
Matsushita					x	x		x
Microelectronics and Computer Technology								x
MCNC					x			
Merix							x	
Micro Networks					x	x		
Micro Substrates Corporation					x	x		
Motorola		x	x	x	x			
MPM Corporation								x
MRSI								x
nChip							x	
NEC		x			x			
NexGen		x						
Nextek						x		
NTK							x	
Nippon Telegraph And Telephone					x			
Photo Stencil							x	
Probe Technology								x
Promex						x		
Research Devices Inc.								x
Rockwell					x			
Sanders			x		x	x		
Sandia Laboratories							x	
SanDisk Corp.					x			

(Continued)

Table 1-3 (Continued)
Flip-Chip Technology Activity

Company	Logic/ASIC	MPU/DSP	Analog/ Discrete/Opto	Memory	Bumping	Assembly	Materials	Equipment/ Probe
Semi Dice						x		
SGS-Thomson					x			
Sharp							x	
Sonoscan								x
SRT								x
Stanford Venture Marketing							x	
Texas Instruments		x			x	x		
Toshiba		x						
Uniax Corp.							x	
Unisys	x							
Universal Instruments								x

*Flip Chip Technologies is a joint venture of Delco and Kulicke & Soffa.
Source: Dataquest (April 1996)

- Stencil printing
- Solder jet deposition
- Stud bumping

Motorola licensed the C4 process from IBM. Motorola has used flip-chip bonding in BGA packages for the PowerPC. Motorola has also disclosed R&D efforts in gold-tin-gold (Au-Sn-Au) bumps. Motorola uses flip-chip technology in pagers and cellular phones.

IBM is currently using its C4 process in ceramic and tape BGAs for ASIC, PowerPC, and SRAM products for captive and merchant market applications. The Nitto Denko ASMAT interconnect technology is a process that will accommodate flip-chip and ball grid array dice as well as perimeter contact dice.

Besides the supplier and equipment infrastructure, standards and subcontractor activity are also developing for this market that is poised for the technologies of 2000. *Implementation of Flip-Chip and Chip-Scale Technology,* J-Std-012, lists technical options and issues. Of more benefit is the alliance between K&S (flip-chip bonders) and Delco Electronics Corporation. The two companies have combined equipment and technology expertise to establish a manufacturing facility for bumping, soldering, and assembly for flip-chip. Delco has an extensive background in flip-chip technology, having assembled analog/discrete components using flip-chip technology for engine control modules.

Other companies developing flip-chip assembly lines or flip-chip product strategies are LSI Logic, VLSI Technology, Amkor/Anam, Solectron, SCI Systems, and Alphatec. For flip-chip in tape and reel formats, the bumped dice are being transported in a bumps-up format. Esmeca, Fuji, Tempo, and Zevatech are developing tape and reel methods.

The National Electronics Manufacturing Initiative Inc. (NEMI), an industry-supported consortium, has a Flip Chip Implementation Group. This group will be targeting the following areas for flip-chip:

- Underfill materials and applications
- Wafer bumping technology
- Die level burn-in and test
- Wafer level burn-in and test

Participants in this group include Delco Electronics, Dexter, Dover Technologies/Universal Instruments, Eastman Kodak, HADCO, IBM, K&S, Lucent Technologies, and Motorola.

Multichip Module (MCM)

The worldwide packaging forecast in Chapter 2 is an evaluation of the single-chip package production for active ICs, as well as the available bare die shipped through 2000. Tables 1-4 and 1-5 show Dataquest's projections for the MCM market in North America. The tables of data include the following:

- Value of the semiconductors used in MCM in equipment
- Total value of MCM (semiconductor plus substrate) in the equipment market

The use of MCM technology has moved out of its small-volume custom-design phase of the first half of this decade. The scope of system implementation has gone beyond the data processing, and consumer sectors, into communications, transportation, and industrial application markets. Both users and suppliers of various module substrate and design architectures have disproved the following long-held myths that seem to haunt new technologies, especially MCM:

- Expensive complex technology
- Lack of bare die, tested die, or KGD
- Lack of infrastructure
- Technology needed only for high-performance, high-end applications

Table 1-4
Value of Semiconductors in MCM in North America (Millions of Dollars)

	1995	1996	1997	1998	1999	2000
Data Processing	486	862	1,311	2,302	3,756	5,588
Communications	366	638	1,001	1,374	1,962	2,962
Industrial	25	35	57	86	118	161
Consumer	7	11	15	21	26	21
Military	7	13	17	22	30	39
Transportation	2	4	6	8	10	13
Total	892	1,561	2,406	3,812	5,903	8,784

Source: Dataquest (April 1996)

Table 1-5
MCM Revenue in North America Equipment (Millions of Dollars)

	1995	1996	1997	1998	1999	2000
Data Processing	656	1,146	1,743	3,062	4,996	7,265
Communications	586	982	1,541	2,116	3,022	4,442
Industrial	49	67	110	166	229	252
Consumer	13	20	30	41	51	41
Military	14	25	33	43	57	66
Transportation	4	7	11	15	20	24
Total	1,323	2,247	3,468	5,442	8,375	12,091

Source: Dataquest (April 1996)

As seen by the major efforts made by AT&T, IBM, MicroModule Systems, and nChip, MCM has moved beyond the mainframe and supercomputer into the desktop and laptop market. The greatest challenge to these MCM vendors was not to prove the viability of their technology, but to move it into the merchant arena and market their technology as off-the-shelf product to the above-50-MHz domain. As component technology pushed single-chip packaging beyond the 50-MHz domain to 75 MHz in 1993 and 1994, system designers were still content to pay the high engineering and board costs of using single-chip technology in the form of very expensive ceramic pin grid arrays (PGAs). The advent of the 90-MHz-and-above Pentium, PowerPC, and Alpha processors, coupled with low-cost, off-the-shelf products and MCM system implementation from companies such as AT&T, Chrysler, Fujitsu, Intel, MMS, Motorola, and Nokia, have demonstrated cost efficiencies in MCM versus single chip that have surpassed end-user expectations.

Table 1-6 illustrates a cost comparison example from Chrysler Corporation. National Semiconductor, Motorola, and Texas Instruments are designing modules for the automotive industry, an industry notorious for its demand for the highest component quality available at the lowest of low costs.

Motorola and DSC Communications Corporation have reported the following savings in a telecommunications system using a four-chip MCM versus a single-chip 160-pin quad flat pack (QFP):

- Total system cost reduction using MCM = 35 percent
- Real estate improvement using MCM = 44.3 percent
- Materials cost savings using MCM = 20 percent

Table 1-6
Engine Controller MCM Design Savings

Materials	Current Engine Module	MCM Module	Savings
PCB	4 layers	4/2 layers	$0 to $4
Board Size	7 x 5 inches	7 x 4.5 inches	$1
ICs	$45	$40	$5
Potting	-	10 percent less	$0.25
Manufacturing Process	Two machines	One machine	$0.50
EMI Capacitors	-	30 fewer	$1.50
In-House Yield	-	$25 less	$0.25
Total	-	-	$8.50 to 12.50

Source: Chrysler Corporation

As noted in the previous section on bare die/KGD, availability of a die market is no longer in question. The infrastructure needed from design to completion (CAD, fabs, wafer bumping, rerouting, and test) is available to support this growing market. In the area of CAD, design tool support is available from the following:

- Harris Finesse
- Mentor
- Cadence
- PCAD and AutoCAD (TI)

Companies with MCM fabs include AT&T, Fujitsu, Hughes, IBM, Micro-Module Systems, Motorola, National Semiconductor, nChip, NEC Corporation, and Texas Instruments.

As the market evolved, the MCM categories of laminate (MCM-L), ceramic (MCM-C), and deposited (MCM-D), expanded or merged. The multichip package (MCP), where several chips were mounted on a small printed circuit board attached to a leadframe and mounted into a standard plastic package such as a quad flat pack (QFP) or a BGA, was rapidly accepted into portable cellular and desktop applications as a low-cost answer to MCM. Packard-Hughes Interconnect introduced laminated-film (MCM-LF) substrate technology. Texas Instruments' laminate overlay (MCM-L/O) is a combination of thin-film interconnect technology with printed wiring board (PWB) substrates. It drove volume usage from the low-end market. Thomson-CSF is working with IBM-France and Motorola to build a 3-D vertical module (MCM-V) that would use a PowerPC and 3-D memory block. Thomson's Trimod technology, designed by Alcatel Espace and built by Thomson, uses 16M DRAMs in a block that measures 19 x 19.5 x 11mm.

Chapter 2
Worldwide Package Forecast

The worldwide and regional package forecasts in Tables 2-1 through 2-5 are based on Dataquest's October 1995 forecast, which posted a 1994-to-1999 compound annual growth rate (CAGR) of 22.8 percent and a 22.1 percent revenue growth rate increase in 1996 over 1995. At the time of publication of this document, several changes had taken place in the component and wafer fab arena that now suggest that market growth for 1996 will decline from Dataquest's original forecast expectations. The PC application market, which has been a driver of wafers, declined in the first quarter. DRAM price per bit, a key driver in both the semiconductor and equipment markets, is expected to be flat in 1997 and down in 1998. As of the first quarter of 1996, seven to 10 proposed new fabs were put on delay status. This number could go as high as 20. Most of these are DRAM fabs, and the delay time could last from 15 months to two years. As such, the forecast growth rates for small-outline (SO, predominantly memory) and QFP (ASIC/MPU) packages in 1997 and 1998 could be adjusted downward.

The development and growth of the emerging and advanced package and interconnect technologies discussed in Chapter 1 are in the early phases of their life cycles. However, they have already surpassed existing SMT barriers in performance, assembly-yield, and high I/O count limitations. As shown in Table 2-1 and Figure 2-1, the existing SO and QFP packages represent the largest configuration selection for all ICs worldwide. As shown in Figure 2-2, SMT now represents 82 percent of all packages produced. Figure 2-3 illustrates the SMT breakout for 1996 and the estimated changes for 1998. The growth of the BGA package is the result of high-I/O ASIC and microprocessor products and technology-limited QFP. Market growth expectations for high-speed portable applications, communications (cellular and pagers), PC Cards, workstations, and servers and strong acceptance of early BGA usage in those markets by companies like Cisco, Motorola, and Compaq will reinforce the estimated forecast for BGA packages.

BGA Update

Dataquest's BGA survey results indicate that BGA package designs continue to displace the ceramic and plastic PGAs and QFPs beyond 300 pins. Early indications from users in the beyond-400-pad arena is that demand is already straining worldwide capacity.

In comparison with the 1995 survey, as shown in Table 2-6, the greatest volume shipped in 1995 was in the single-core plastic (PBGA) category. Table 2-7 lists the estimated production of BGAs by various lead pitch ranges for 1995. Table 2-8 lists the estimated average pad count range for suppliers and users of BGA packages in 1995. Tables 2-9 and 2-10 list the estimated BGA use by product and in the end system for 1995.

Tables 2-11 and 2-12 list a selection of BGA supplier developments and product designs that have taken place in 1994 and 1995.

Table 2-1
Worldwide Package Forecast (Millions of Units)

	1994	1995	1996	1997	1998	1999	2000
Plastic DIP	5,358	4,062	2,793	2,009	1,431	913	634
Ceramic DIP	438	171	133	108	87	65	49
QFP	12,038	15,574	17,724	18,789	21,832	24,009	24,579
Ceramic Chip Carrier	104	73	52	37	23	14	6
Plastic Chip Carrier	552	526	494	436	382	312	269
SO	18,916	22,424	23,293	23,902	25,400	26,973	27,369
Ceramic PGA	116	119	109	99	86	67	59
Plastic PGA	111	117	113	95	83	65	49
Ball/Land Grid Array	77	280	703	1,261	2,161	3,351	4,806
Bare Chip	3,461	4,513	5,950	7,183	8,502	9,699	10,703
Total	41,171	47,859	51,364	53,919	59,987	65,468	68,523
Percentage of Total							
Plastic DIP	13.0	8.5	5.4	3.7	2.4	1.4	0.9
Ceramic DIP	1.1	0.4	0.3	0.2	0.1	0.1	0.1
QFP	29.2	32.5	34.5	34.8	36.4	36.7	35.9
Ceramic Chip Carrier	0.3	0.2	0.1	0.1	0	0	0
Plastic Chip Carrier	1.3	1.1	1.0	0.8	0.6	0.5	0.4
SO	45.9	46.9	45.3	44.3	42.3	41.2	39.9
Ceramic PGA	0.3	0.2	0.2	0.2	0.1	0.1	0.1
Plastic PGA	0.3	0.2	0.2	0.2	0.1	0.1	0.1
Ball/Land Grid Array	0.2	0.6	1.4	2.3	3.6	5.1	7.0
Bare Chip	8.4	9.4	11.6	13.3	14.2	14.8	15.6
Total	100.0	100.0	100.0	100.0	100.0	100.0	100.0

Source: Dataquest (April 1996)

Table 2-2
North America Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Plastic DIP	1,810	1,500	1,100	901	655	458
Ceramic DIP	58	35	28	20	15	10
QFP	5,611	6,673	7,200	7,503	8,001	7,989
Ceramic Chip Carrier	55	41	29	18	11	5
Plastic Chip Carrier	405	384	345	301	245	220
SO	6,110	6,317	6,600	7,212	7,432	7,450
Ceramic PGA	70	60	55	43	29	21
Plastic PGA	74	67	55	45	30	22
Ball/Land Grid Array	210	541	945	1,570	2,259	3,065
Bare Die	1,811	2,300	2,991	3,848	4,563	5,070
Total	16,214	17,918	19,348	21,461	23,240	24,310
Yearly Growth Rate (%)						
Plastic DIP	-24.3	-17.1	-26.7	-18.1	-27.3	-30.1
Ceramic DIP	-48.2	-39.7	-20.0	-28.6	-25.0	-33.3
QFP	22.0	18.9	7.9	4.2	6.6	-0.1
Ceramic Chip Carrier	-26.7	-25.5	-29.3	-37.9	-38.9	-54.5
Plastic Chip Carrier	-0.5	-5.2	-10.2	-12.8	-18.6	-10.2
SO	27.5	3.4	4.5	9.3	3.1	0.2
Ceramic PGA	-10.3	-14.3	-8.3	-21.8	-32.6	-27.6
Plastic PGA	5.7	-9.5	-17.9	-18.2	-33.3	-26.7
Ball/Land Grid Array	238.7	157.6	74.7	66.1	43.9	35.7
Bare Die	13.9	27.0	30.0	28.7	18.6	11.1
Total	14.4	10.5	8.0	10.9	8.3	4.6

Source: Dataquest (April 1996)

Table 2-3
Japan Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Plastic DIP	600	170	85	70	46	21
Ceramic DIP	55	45	35	24	12	8
QFP	4,013	3,977	3,900	4,322	4,278	4,008
Ceramic Chip Carrier	9	5	3	2	0	0
Plastic Chip Carrier	28	20	15	10	5	2
SO	6,107	6,102	6,092	6,328	6,400	6,539
Ceramic PGA	20	20	18	17	15	15
Plastic PGA	27	30	25	25	22	15
Ball/Land Grid Array	56	142	286	544	1,000	1,600
Bare Die	1,526	1,930	2,132	2,355	2,600	2,840
Total	12,441	12,441	12,591	13,697	14,378	15,048
Yearly Growth Rate (%)						
Plastic DIP	-14.3	-71.7	-50.0	-17.6	-34.3	-54.3
Ceramic DIP	-72.5	-18.2	-22.2	-31.4	-50.0	-33.3
QFP	22.2	-0.9	-1.9	10.8	-1.0	-6.3
Ceramic Chip Carrier	-10.0	-44.4	-40.0	-33.3	-100.0	-
Plastic Chip Carrier	-37.8	-28.6	-25.0	-33.3	-50.0	-60.0
SO	13.1	-0.1	-0.2	3.9	1.1	2.2
Ceramic PGA	-4.8	0	-10.0	-5.6	-11.8	0
Plastic PGA	8.0	11.1	-16.7	0	-12.0	-31.8
Ball/Land Grid Array	460.0	153.6	101.4	90.2	83.8	60.0
Bare Die	47.7	26.5	10.5	10.5	10.4	9.2
Total	16.0	0	1.2	8.8	5.0	4.7

Source: Dataquest (April 1996)

Table 2-4
Europe Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Plastic DIP	1,152	723	616	300	100	80
Ceramic DIP	48	45	40	38	35	30
QFP	3,180	3,585	3,700	4,550	5,210	5,471
Ceramic Chip Carrier	8	5	5	3	3	1
Plastic Chip Carrier	45	44	42	41	40	31
SO	4,150	4,458	4,410	4,855	5,291	5,482
Ceramic PGA	5	5	4	4	3	3
Plastic PGA	10	10	10	9	9	8
Ball/Land Grid Array	7	11	19	31	64	111
Bare Die	701	1,100	1,300	1,429	1,536	1,633
Total	9,306	9,986	10,146	11,260	12,291	12,850
Yearly Growth Rate (%)						
Plastic DIP	-25.7	-37.2	-14.8	-51.3	-66.7	-20.0
Ceramic DIP	-54.3	-6.3	-11.1	-5.0	-7.9	-14.3
QFP	43.6	12.7	3.2	23.0	14.5	5.0
Ceramic Chip Carrier	-55.6	-37.5	0	-40.0	0	-66.7
Plastic Chip Carrier	-10.0	-2.2	-4.5	-2.4	-2.4	-22.5
SO	24.3	7.4	-1.1	10.1	9.0	3.6
Ceramic PGA	0	0	-20.0	0	-25.0	0
Plastic PGA	0	0	0	-10.0	0	-11.1
Ball/Land Grid Array	250.0	57.1	72.7	63.2	106.5	73.4
Bare Die	43.6	56.9	18.2	9.9	7.5	6.3
Total	19.6	7.3	1.6	11.0	9.2	4.5

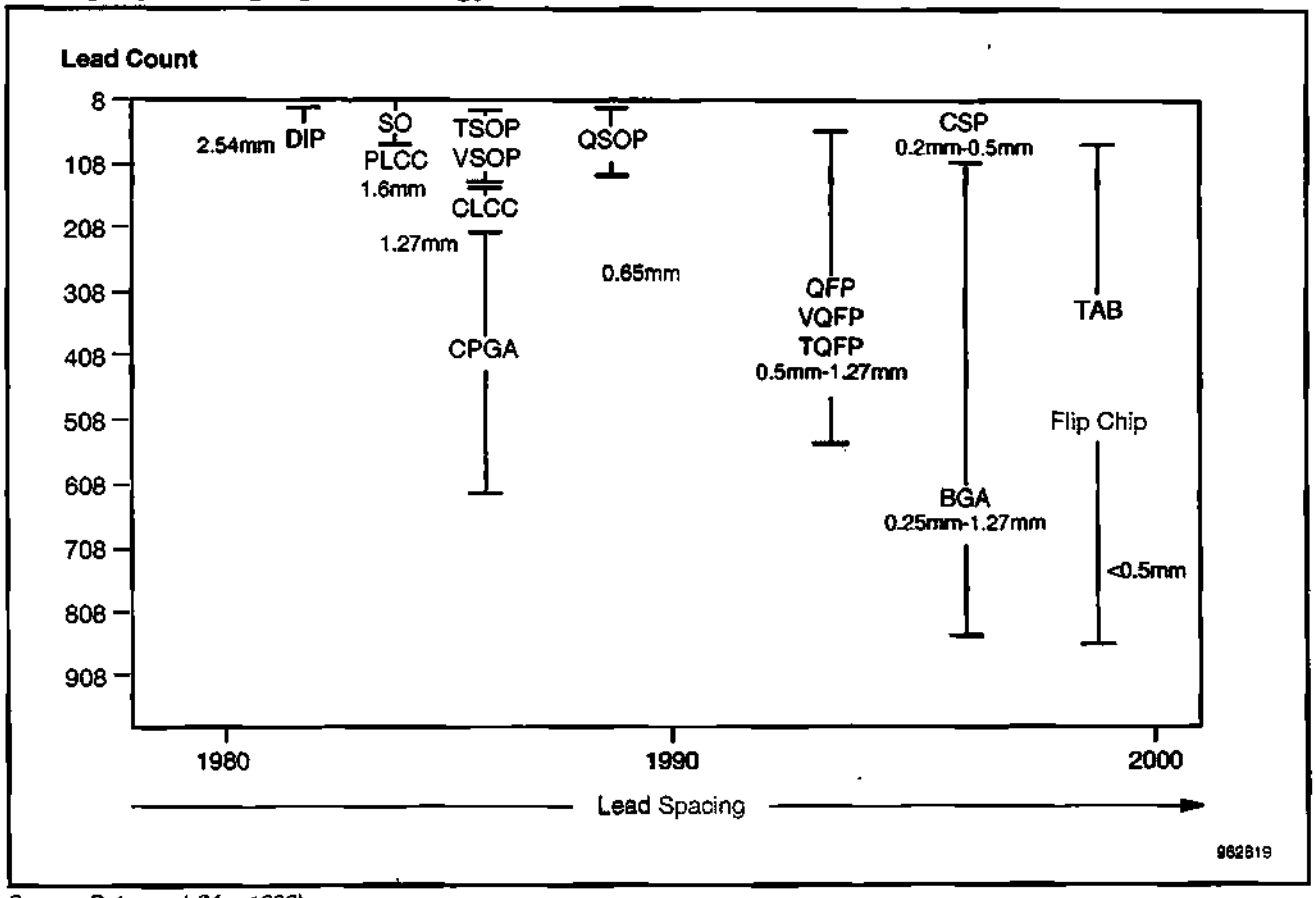
Source: Dataquest (April 1996)

Table 2-5
Asia/Pacific Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Plastic DIP	500	400	208	160	112	75
Ceramic DIP	10	8	5	5	3	1
QFP	2,770	3,489	3,989	5,457	6,520	7,111
Ceramic Chip Carrier	1	1	0	0	0	0
Plastic Chip Carrier	48	46	34	30	22	16
SO	6,057	6,416	6,800	7,005	7,850	7,898
Ceramic PGA	24	24	22	22	20	20
Plastic PGA	6	6	5	4	4	4
Ball/Land Grid Array	7	9	11	16	28	30
Bare Chip	475	620	760	870	1,000	1,160
Total	9,898	11,019	11,834	13,569	15,559	16,315
Yearly Growth Rate (%)						
Plastic DIP	-30.4	-20.0	-48.0	-23.1	-30.0	-33.0
Ceramic DIP	-52.4	-20.0	-37.5	0	-40.0	-66.7
QFP	42.8	26.0	14.3	36.8	19.5	9.1
Ceramic Chip Carrier	0	0	-100.0	-	-	-
Plastic Chip Carrier	-4.0	-4.2	-26.1	-11.8	-26.7	-27.3
SO	12.5	5.9	6.0	3.0	12.1	0.6
Ceramic PGA	100.0	0	-8.3	0	-9.1	0
Plastic PGA	0	0	-16.7	-20.0	0	0
Ball/Land Grid Array	133.3	28.6	22.2	45.5	75.0	7.1
Bare Chip	35.7	30.5	22.6	14.5	14.9	16.0
Total	16.7	11.3	7.4	14.7	14.7	4.9

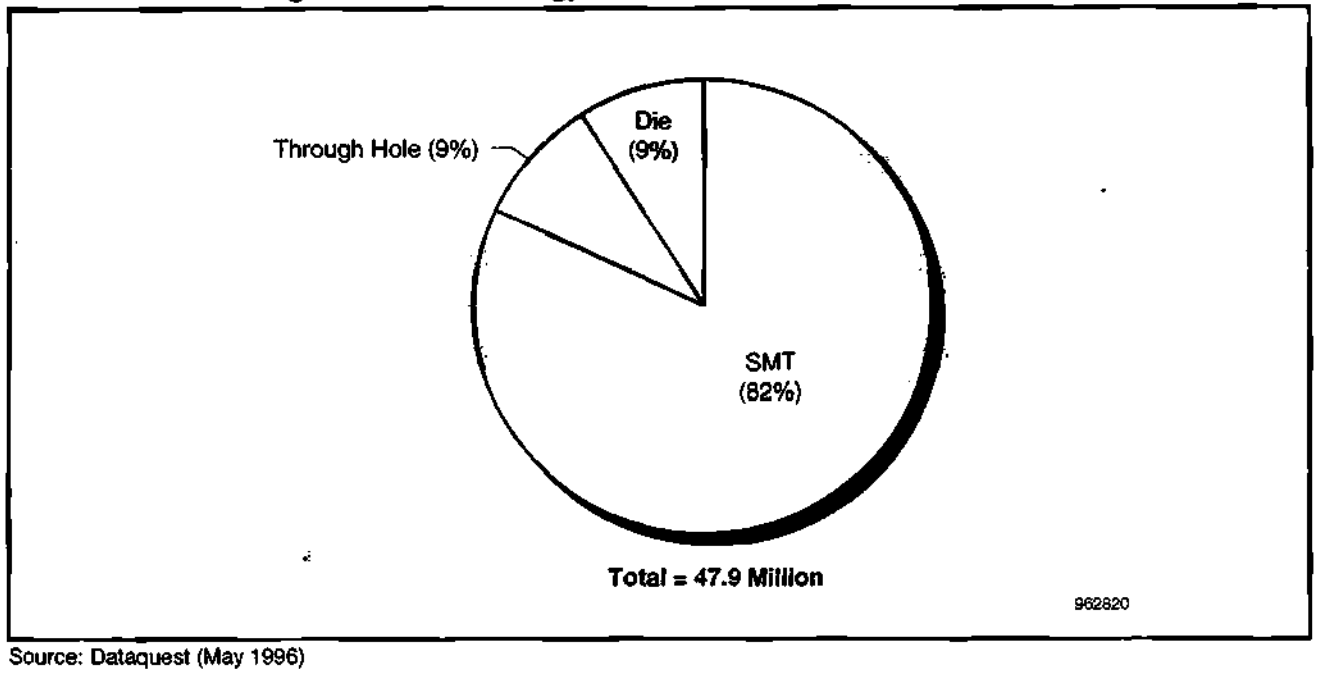
Source: Dataquest (April 1996)

Figure 2-1
Emerging Packaging Technology



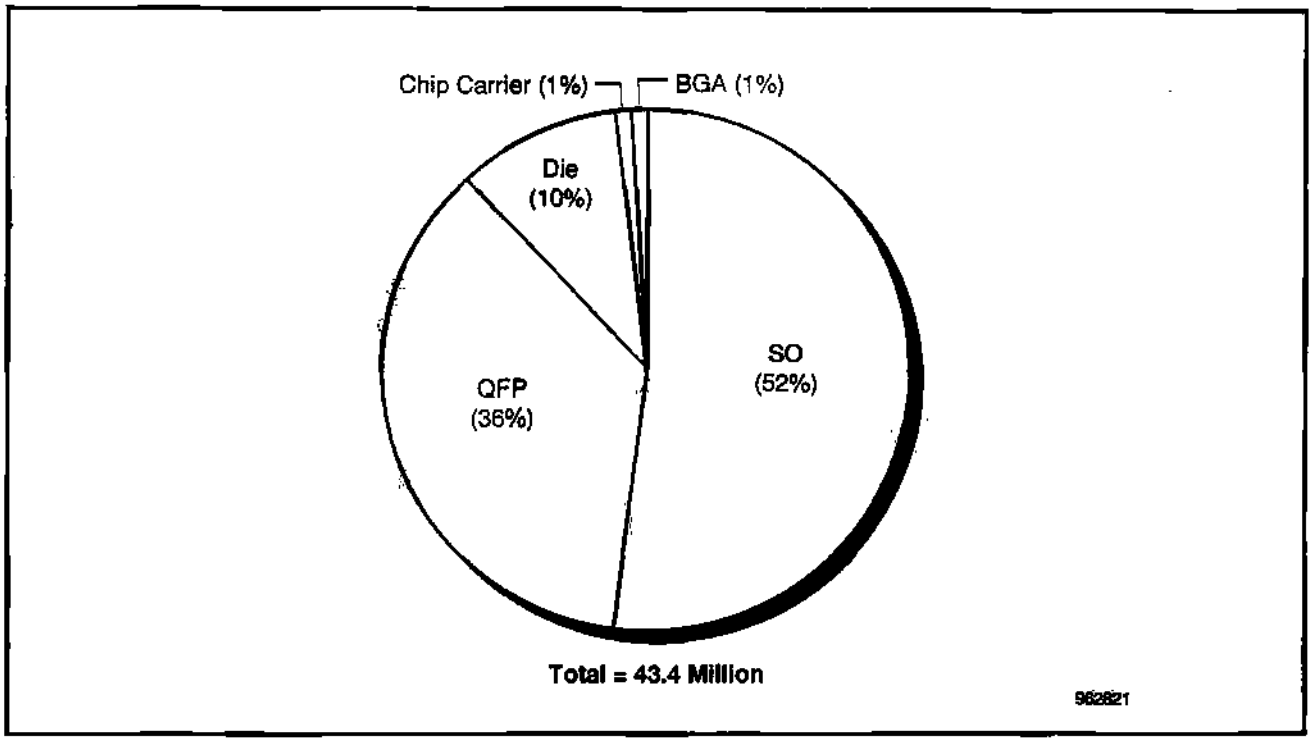
Source: Dataquest (May 1996)

Figure 2-2
SMT versus Through Hole Technology, 1995



Source: Dataquest (May 1996)

Figure 2-3
SMT Distribution, 1995



Source: Dataquest (May 1996)

Table 2-6
Estimated BGA Production, 1995 versus 1994

BGA Product	Percentage of 1994	Percentage of 1995
Plastic BGA (Single Core)	87	90
Plastic BGA (Peripheral Array)	10	5
Enhanced PBGA (Multilayer)	0	1
MicroBGA	<1	<1
Ceramic BGA	1	1
Ceramic Column Grid Array (CBGA)	0	0
Tape BGA	1	2

Source: Dataquest (April 1996)

Table 2-7
Lead Pitch Range (Estimated Percentage of Total Production)

Lead Pitch	Percentage of 1994	Percentage of 1995
0.060 Inches	55	65
0.050 Inches (1.27mm)	14	15
0.040 Inches (1.00mm)	12	10
0.020 Inches (0.5mm)	19	10
0.010 Inches (0.25mm)	0	0

Source: Dataquest (April 1996)

Table 2-8
Estimated BGA Pad Count Range (Percentage of Production)

Pad Count	1994	1995
<44	1	0
44 to 84	5	1
85 to 132	10	3
133 to 195	8	4
196 to 244	54	70
245 to 308	10	10
309 to 475	8	10
476 to 672	1	1
>672	3	1

Source: Dataquest (April 1996)

Table 2-9
Estimated BGA Consumption by Product Technology

Product	Percentage of 1994 BGA Use	Percentage of 1995 BGA Use
Microprocessor	12	10
Microcontroller	11	4
Microperipheral	10	0
Memory	10	1
Logic	53	81
Analog	3	2
Discrete	1	1
MCM	<1	1

Source: Dataquest (April 1996)

Table 2-10
Estimated BGA Market Application

Application	Percentage of 1994 BGA Production	Percentage of 1995 BGA Production
Data Processing	61	74
Telecommunications	38	24
Industrial/Medical	<1	<1
Automotive/Transportation	<1	<1
Consumer	0	0
Military/Civil Aerospace	0	0

Source: Dataquest (April 1996)

Table 2-11
BGA Supplier Developments

Company	Products	License Agreements
Amkor/Anam	PBGA/PowerQuad	Motorola
	MicroBGA	Tessera
	SuperBGA (Amkor)	
ASAT	PBGA/EDQuad	Motorola
		IBM
		Sheldahl
Citizen	CBGA/TBGA/CCGA/PBGA	IBM patents
	PBGA	Motorola
Coors Electronic Package Co.	CBGA	-
Gore & Associates	PBGA	-
Hyundai	PBGA	Motorola
IBM	CBGA/TBGA/CCGA/PBGA	IBM patents
iPAC	PBGA	Motorola
Kyocera	CBGA	Kyocera patents
NTK	CBGA	NTK patents
Olin	Metal (M)BGA	Olin patents
Shinko	PBGA/MicroBGA	Motorola/Tessera
SMOS Systems	PBGA	-
Solectron	PBGA	-
Swire	PBGA	Motorola
Tessera	MicroBGA	Tessera patent
Texas Instruments	Micro StarBGA	Sheldahl Via Grid
Universal Instruments	PBGA	Motorola

Source: Dataquest (April 1996)

Table 2-12
BGA Product Designs

Company	Products	Application
Altera	EPLD	Desktop, workstation
AT&T	ASICs/MCMs	Communications
Compaq	ASICs-PBGA/perimeter-leaded	Desktop
Hitachi	ASIC/DRAM	Desktop, PCMCIA, server, workstation
Intel	MPU	PCMCIA, desktop, workstation
LSI Logic	ASIC (IBM BGA license)	Workstation, server
MicroModule Systems	SRAM/SPARC modules	FDDI/CDDI, server, workstation, cellular
Micron	DRAM/SRAM	Desktop, palmtop, PCMCIA
MIPS Technologies	R5000	Workstation, server
Motorola	SRAM/PowerPC/MCUs	Desktop, server, cellular, pager
NEC	Vr5000 200 MHz	Workstation, server
Pacific Microelectronics	BGA modules	Server, desktop, PCMCIA, SONET
Samsung	DRAM evaluation	-
Standard Microsystems	Cardbus controller	Portable desktop
Texas Instruments	DRAM/SRAM/DSP/ASIC	Micro Star BGA
VLSI Technology Inc.	ASIC PBGA/TBGA	Workstation, server, desktop
Xilinx	EPLDs	Workstation

Source: Dataquest (April 1996)

Chapter 3
Component Interconnect

The forecasts for component by package type are shown in Tables 3-1 through 3-14. The area of greatest change in memory packaging for DRAMs was the growth in the DIMM. DIMM production represented less than 1 percent of memory module designs in 1994, but jumped to 20 percent of total DRAM module production in 1995. The estimated growth for DIMM is expected to increase to 55 percent from 1995 to 1996. Apple Computer was a large user of the 168-pin DIMM in the Power Mac 9500 system in 1995. DRAM vendors shifted production from SIMM to DIMM module configurations for the 4M and 16M densities in the second half of 1995. Another unique horizontal package design is from Toshiba for the Rambus DRAM (RDRAM) design. The Toshiba 8M RDRAM device is packaged in a 32-pin surface horizontal package (SHP). The package is similar to a thin small-outline package (TSOP) in that it is surface-mountable to the board. However, four pins on one side are support pins only. All the signal pins are on the opposite side. This configuration keeps the signal length at a minimum, allowing for a very high-frequency part.

Stacking technology or 3-D memory packaging is still a unique and very small industry compared with the high-volume single-chip or single in-line memory module/dual in-line memory module (SIMM/DIMM) market. Table 3-15 lists the vendors, stackable products, and alliance agreements. Stackable memories as well as stackable processor and analog device applications vary by function and application requirements. They have been designed into laptop and subnotebooks as well as supercomputers and satellites. Users of stackable designs rely on the technology for the following:

- Shorter signal lines
- Signal line capacitance reduction
- Minimizing I/O
- Reduction of manufacturing costs

End users include IBM, Toshiba, Panasonic, Digital, Cray Computer, GEC Marconi Avionics, Intelligent Reasoning Systems Inc. (IRSI), and Loral Federal Systems. Applications have included the following:

- Solid state recorder—data storage in space applications
- Engine modules—automotive
- Memory cubes—supercomputers, laptops, PCMCIA cards, notebooks, cellular phones, camcorders, and microvideo cameras
- Stackable processors—supercomputers

The greatest package design change in all product areas is evident in increased usage of BGA packages. ASIC (gate arrays, EPLDs, and FPGAs) and microprocessor products will continue to drive the growth and variety of high-I/O BGA designs. BGA production for SRAM and DRAM is still in small volumes. High-speed RF devices, discrete devices, and mixed-signal devices are in the early design phases of CSPs and BGAs. In 1995, ASIC vendors expanded BGA strategies into TBGAs and Enhanced BGAs, a move necessitated by system design and increased product I/O.

Microprocessor package changes are minor. The customary packages have been ceramic PGAs or ceramic BGAs for the high-end, above-75-MHz designs, with the majority of the low-end devices in plastic QFPs (PQFPs), with small volumes of PPGAs. Overall, plastic is still the main focus for older generations of products. It is the most cost-efficient package in comparison with ceramic. However, the new microprocessors are compute-intensive. At speeds of 200 MHz to 300 MHz, most players will be designing first-generation products in ceramic (PGA or BGA). Hewlett-Packard has experimented with the metal quad (MQUAD) package in various designs, but chose to design the ceramic PGA package into the PA 7100LC. The MIPS RISC Vr5000 (180 MHz to 250 MHz) and Vr10000 (over 300 MHz) devices are being offered in ceramic PGA and CBGA designs. Intel's Pentium Pro is being designed in ceramic PGA and BGA packages. New ceramic BGA designs will continue to displace ceramic PGA designs. Motorola, IBM, Intel, NEC, and Fujitsu are all incorporating or will be designing with flip-chip attach. Start-ups such as MicroUnity and Exponential are introducing products in 312-lead tape-automated bonding (TAB) and ceramic BGA, respectively.

Although some CSP designs are targeted for new analog and discrete products, most of the analog designs are in small-outline packages (SOT, SSOP, TSOP, TSSOP). Micrel Semiconductor has designed a CSP-like package called IttyBitty. The five-lead SOT-23 SMT package is half the footprint size of an 8-pin SOIC. The package height is 1.2mm, and it fits into a Type I, II, or III PC Card (PCMCIA). As the market need for low-profile parts grew in standard logic, Motorola and Texas Instruments responded with an increased supply of SSOPs and TSSOPs. The SSOP takes up about 45 percent of the space needed for the SOIC package, while the TSSOP is about 30 percent of the space needed for the SOIC. The SSOPs are about 2mm high and the TSSOPs are 1.2mm high.

Table 3-1
Estimated Worldwide MOS DRAM Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
256K DRAM	47.0	22.0	8.0	2.0	2.0	0
DIP	5.6	0.7	0.1	0	0	0
ZIP	13.2	7.5	3.0	0.8	0.8	0
PLCC	18.8	8.8	3.2	0.8	0.8	0
Others	8.9	4.8	1.6	0.4	0.4	0
Die	0.5	0.2	0.1	0	0	0
SIMM	9.4	4.4	1.6	0.4	0.4	0
1M DRAM	365.0	134.0	71.0	44.0	36.0	12.0
DIP	3.3	0	0	0	0	0
ZIP	18.3	4.0	0.7	0	0	0
SOJ/SOP	321.2	118.9	62.1	37.8	31.0	10.2
TSOP	11.0	6.7	5.7	4.4	3.6	1.2
Others	0	0	0	0	0	0
Die	11.3	4.4	2.5	1.8	1.4	0.6
SIMM	218.4	80.8	42.2	26.5	21.7	7.1

(Continued)

Table 3-1 (Continued)
Estimated Worldwide MOS DRAM Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
4M DRAM	1,337.0	1,109.0	891.0	519.0	292.0	120.0
DIP	0	0	0	0	0	0
ZIP	64.2	49.9	33.9	10.4	2.9	0
SOJ/SOP	1046.9	792.9	616.6	344.1	178.1	72.6
TSOP	168.5	215.1	188.9	130.8	89.1	37.2
Others	6.7	5.5	4.5	2.6	1.5	0.6
Die	50.8	45.5	47.2	31.1	20.4	9.6
SIMM	607.7	504.0	418.8	237.4	133.6	54.9
DIMM	243.1	302.4	241.6	142.5	80.2	32.9
16M DRAM	312.0	724.0	1090.0	1145.0	918.0	565.0
DIP	0	0	0	0	0	0
ZIP	0	0	0	0	0	0
SOJ/SOP	202.8	434.4	599.5	572.5	367.2	197.8
TSOP	87.4	217.2	359.7	435.1	394.7	271.2
Others	6.2	14.5	21.8	22.9	18.4	11.3
Die	15.6	57.9	109.0	114.5	137.7	84.8
SIMM	174.1	260.6	287.8	100.8	38.1	0
DIMM	8.7	86.9	179.9	261.1	276.3	189.8
64M DRAM	0	4.0	60.0	279.0	596.0	845.0
DIP	0	0	0	0	0	0
ZIP	0	0	0	0	0	0
SOJ/SOP	0	2.3	31.2	125.6	220.5	304.2
Others	0	0.5	10.8	69.8	196.7	287.3
Die	0	1.2	18.0	83.7	178.8	253.5
SIMM	0	0	0	0	0	0
DIMM	0	1.2	15.6	62.8	110.3	152.1
256M DRAM	0	0	0	1.0	10.0	45.0
DIP	0	0	0	0	0	0
ZIP	0	0	0	0	0	0
SOJ/SOP	0	0	0	0.6	4.0	11.3
Others	0	0	0	0.2	3.0	15.8
Die	0	0	0	0.3	3.0	18.0
SIMM	0	0	0	0	0	0
DIMM	0	0	0	0.3	2.0	5.6

Source: Dataquest (April 1996)

Table 3-2
Estimated Worldwide MOS DRAM Module Organization Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
256K DRAM SIMM	9.4	4.4	1.6	0.4	0.4	0
x8	1.4	0.7	0.2	0.1	0.1	0
x9	8.0	3.7	1.4	0.3	0.3	0
x32	-	-	-	-	-	-
x36	-	-	-	-	-	-
x40	-	-	-	-	-	-
1M DRAM SIMM	218.4	80.8	42.2	26.5	21.7	7.1
x8	26.2	8.1	3.4	1.9	1.1	0.3
x9	120.1	44.5	23.2	14.6	11.9	3.9
x32	2.2	0.8	0.4	0.3	0.2	0.1
x36	67.7	25.9	14.4	9.3	8.0	2.7
x40	2.2	1.6	0.8	0.5	0.4	0.1
4M DRAM SIMM	607.7	504.0	418.8	237.4	133.6	54.9
x8	48.6	25.2	4.2	0	0	0
x9	30.4	20.2	18.8	11.9	6.7	2.7
x32	437.5	352.8	293.2	166.2	93.5	38.4
x36	60.8	80.6	81.7	47.5	26.7	11.0
x40	30.4	25.2	20.9	11.9	6.7	2.7
DIMM	243.1	302.4	241.6	142.5	80.2	32.9
72-Pin	240.7	299.4	239.2	141.1	79.4	32.6
168-Pin	2.4	3.0	2.4	1.4	0.8	0.3
16M DRAM SIMM	174.1	260.6	287.8	100.8	38.1	0
x8	1.7	2.6	2.9	1.0	0.4	0
x9	7.0	10.4	11.5	4.0	1.5	0
x32	104.5	156.4	172.7	60.5	22.9	0
x36	52.2	78.2	86.3	30.2	11.4	0
x40	8.7	13.0	14.4	5.0	1.9	0
DIMM	8.7	86.9	179.9	261.1	276.3	189.8
72-Pin	0.9	8.7	18.0	26.1	27.6	19.0
168-Pin	7.8	78.2	161.9	235.0	248.7	170.8

(Continued)

Table 3-2 (Continued)
Estimated Worldwide MOS DRAM Module Organization Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
64M DRAM SIMM	-	1.2	15.6	62.8	110.3	152.1
x8	-	0	0	0	0	0
x9	-	0	0	0	0	0
x32	-	0	0	0	0	0
x36	-	0	0	0	0	0
x40	-	0	0	0	0	0
DIMM	-	1.2	15.6	62.8	110.3	152.1
256M DRAM SIMM	-	-	-	0.3	2.0	5.6
x8	-	-	-	0	0	0
x9	-	-	-	0	0	0
x32	-	-	-	0	0	0
x36	-	-	-	0	0	0
x40	-	-	-	0	0	0
DIMM	-	-	-	0.3	2.0	5.6

Source: Dataquest (April 1996)

Table 3-3
Worldwide >70ns Slow SRAM Package Forecast (Millions of Units)

		1995	1996	1997	1998	1999	2000
16K	DIP	6.3	2.3	1.2	0.6	0	0
	SOG/SOP	14.7	6.8	4.8	5.4	2.0	0
	Bare Die	0	0	0	0	0	0
	Total	21.0	9.0	6.0	6.0	2.0	0
64K	DIP	65.3	10.2	6.3	2.4	0	0
	SOG/SOP	72.5	22.1	13.7	9.0	5.7	1.9
	Bare Die	7.3	1.7	1.1	0.6	0.3	0.1
	Total	145.0	34.0	21.0	12.0	6.0	2.0
256K	DIP	9.5	1.5	0	0	0	0
	SOG/SOP	113.4	92.4	64.2	42.0	30.0	12.6
	TSOP	51.0	44.7	26.8	14.0	10.0	4.2
	Bare Die	15.1	15.4	16.1	14.0	10.0	4.2
	Total	189.0	154.0	107.0	70.0	50.0	21.0
1Mb	DIP	2.3	1.5	0	0	0	0
	SOG/SOP	75.9	91.8	73.4	55.7	42.0	30.4
	TSOP	28.8	49.0	51.7	48.7	52.5	38.0
	Bare Die	8.1	10.7	10.9	11.6	10.5	7.6
	Total	115.0	153.0	136.0	116.0	105.0	76.0
4Mb	DIP	0	0	0	0	0	0
	SOG/SOP	4.5	14.6	15.3	25.2	20.9	18.7
	TSOP	10.8	43.8	56.1	92.4	115.0	102.9
	Bare Die	2.7	14.6	30.6	50.4	73.2	65.5
	Total	18.0	73.0	102.0	168.0	209.0	187.0
16Mb	DIP	0	0	0	0	0	0
	SOG/SOP	0	0	1.4	3.2	7.6	12.4
	TSOP	0	0	4.2	9.6	22.8	37.2
	Bare Die	0	0	1.4	3.2	7.6	12.4
	Total	0	0	7.0	16.0	38.0	62.0

Source: Dataquest (April 1996)

Table 3-4
Worldwide <70ns Fast SRAM Package Forecast (Millions of Units)

		1995	1996	1997	1998	1999	2000
16K	DIP	6.7	3.8	2.9	1.0	1.0	0
	CLCC/PLCC	0.1	0.0	0.0	0.0	0.0	0
	SOJ	0.1	0.0	0.0	0.0	0.0	0
	Bare Die	0.2	0.1	0.1	0.0	0.0	0
	Total	7.0	4.0	3.0	1.0	1.0	0
64K	DIP	11.1	2.9	0.3	0.2	0	0
	CLCC/PLCC	1.1	0.6	0	0	0	0
	SOJ	65.5	35.9	19.4	13.2	7.7	3.5
	SOP	27.8	14.8	7.8	5.6	2.8	1.3
	Bare Die	5.6	2.9	1.5	1.0	0.6	0.3
	Total	111.0	57.0	29.0	20.0	11.0	5.0
256K	DIP	15.5	2.5	0	0	0	0
	CLCC/PLCC	24.7	12.6	1.9	0	0	0
	SOJ	220.9	193.3	156.6	59.9	44.3	41.8
	SOP	40.2	30.1	21.0	7.3	5.4	5.1
	BGA	3.1	5.0	5.7	3.7	2.7	2.6
	Bare Die	3.1	5.0	3.8	1.5	1.1	1.0
	Others	1.5	2.5	1.9	0.7	0.5	0.5
	Total	309.0	251.0	191.0	73.0	54.0	51.0
1Mb	DIP	0	0	0	0	0	0
	PLCC	0.9	1.6	2.5	0	0	0
	SOJ	73.5	122.2	172.7	180.6	167.0	114.0
	SOP/TSOP	3.7	6.6	9.8	14.0	25.9	22.0
	BGA	0.9	2.5	6.1	11.2	20.2	8.0
	Bare Die	11.2	24.6	44.1	64.4	66.2	50.0
	Others	2.8	6.6	9.8	9.8	8.6	6.0
	Total	93.0	164.0	245.0	280.0	288.0	200.0
4Mb	DIP	0	0	0	0	0	0
	SOJ	0.6	9.0	24.5	91.0	95.9	90.0
	SOP/TSOP	0.0	4.5	12.3	45.5	53.3	56.3
	BGA	0.0	0.9	2.5	18.2	32.0	45.0
	Bare Die	0.2	1.8	4.9	9.1	10.7	11.3
	Others	0.2	1.8	4.9	18.2	21.3	22.5
	Total	1.0	18.0	49.0	182.0	213.0	225.0
16Mb	DIP	0	0	0	0	0	0
	SOJ	0	0	1.1	2.4	7.8	9.7
	SOP/TSOP	0	0	3.3	7.2	23.4	29.1
	BGA	0	0	3.3	7.2	23.4	29.1
	Bare Die	0	0	1.1	2.4	7.8	9.7
	Others	0	0	2.2	4.8	15.6	19.4
	Total	0	0	11.0	24.0	78.0	97.0

Source: Dataquest (April 1996)

Table 3-5
Worldwide MOS ROM Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Worldwide Total	422	350	322	320	350	370
Package Type Total	422	350	322	320	350	370
DIP	151	84	78	64	54	42
SO	207	211	192	206	242	276
Quad	12	15	21	28	34	37
Bare Die	52	40	31	22	20	15
Pin Count Total	422	350	320	320	350	370
24-Pin	0	0	0	0	0	0
28-Pin	25	18	11	6	2	1
32-Pin	27	15	10	5	3	0
40-Pin	64	40	21	24	20	15
42-Pin	149	129	135	145	175	194
44-Pin	105	108	112	118	130	145
Bare Die	52	40	31	22	20	15

Source: Dataquest (April 1996)

Table 3-6
Worldwide EPROM Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Worldwide Total	483	443	448	386	300	240
Package Type Total	483	443	448	386	300	240
DIP	260	227	220	177	115	98
Chip Carrier	74	65	62	54	45	35
SO	90	85	85	76	70	50
TSOP	44	48	56	54	50	42
Bare Die	15	18	25	25	20	15
Pin Count Total	483	443	448	386	300	240
24-Pin	2	0	0	0	0	0
28-Pin	387	335	316	264	195	147
32-Pin	34	38	45	41	37	32
40-Pin	26	30	36	32	28	26
44-Pin	19	22	26	24	20	20
Bare Die	15	18	25	25	20	15

Source: Dataquest (April 1996)

Table 3-7
Worldwide EEPROM Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999	2000
Worldwide Total	722	898	1069	1095	1310	1411
Package Type Total	722	898	1,069	1,095	1,310	1,411
DIP	75	66	50	42	35	19
Chip Carrier	80	78	66	41	38	20
SO/TSOP	531	708	898	961	1,187	1,330
PGA	0	0	0	0	0	0
Bare Die	36	46	55	51	50	42
Pin Count Total	722	898	1,069	1,095	1,310	1,411
8-Pin	289	332	356	340	384	390
14-Pin	45	41	38	30	25	18
24-Pin	53	50	46	39	31	16
28-Pin	211	280	355	344	431	513
32-Pin	11	13	11	10	8	7
40-Pin	29	42	57	66	60	60
42-Pin	48	94	151	215	321	365
Bare Die	36	46	55	51	50	42

Source: Dataquest (April 1996)

Table 3-8
Worldwide Flash Memory Package Production (Millions of Units)

	1995	1996	1997	1998	1999	2000
Worldwide Total	168	237	384	556	814	975
Package Type Total	168	237	384	556	814	975
DIP	30	25	22	17	14	10
Chip Carrier	12	10	9	9	8	8
SO	54	86	148	208	321	396
TSOP	60	90	165	267	411	477
Bare Die	12	26	40	55	60	84
Pin Count Total	168	237	384	556	814	975
28-Pin	12	10	8	5	4	4
32-Pin	49	52	60	55	51	48
40-Pin	34	42	64	74	86	84
42-Pin	18	29	48	68	94	123
44-Pin	15	34	79	129	233	301
48-Pin	28	44	85	170	286	331
Bare Die	12	26	40	55	60	84

Source: Dataquest (April 1996)

Table 3-9
Worldwide Standard Logic Package Forecast, Percentage by Package

	1995	1996	1997	1998	1999
Total MOS/Bipolar	3,765	3,882	3,985	4,092	4,262
Revenue					
Percentage of Units	100	100	100	100	100
DIP	30	25	15	10	5
Plastic	98	100	100	100	100
Ceramic	1	0	0	0	0
Side-Brazed	1	0	0	0	0
Flat Pack	0	0	0	0	0
Ceramic	0	0	0	0	0
Side-Brazed	0	0	0	0	0
Chip Carrier	1	1	0	0	0
Plastic	99	99	0	0	0
Ceramic	1	1	0	0	0
SO	68	73	84	89	94
SOIC	82	75	68	60	50
SSOIC	8	11	12	16	18
TSOP	8	11	16	19	25
TSSOP/QSSOP	2	3	4	5	7
Quad	1	1	1	1	1

Source: Dataquest (April 1996)

Table 3-10
Worldwide Gate Array Package and Pin Count Forecast (Percentage of Design Starts)

	1995	1996	1997	1998	1999	2000
Package Type	100	100	100	100	100	100
DIP	0	0	0	0	0	0
Quad	71	66	58	49	35	29
Plastic QFP	97	97	96	95	96	96
Ceramic QFP	2	3	3	3	3	3
Metal QFP	1	1	1	2	2	1
Chip Carrier	3	1	1	0	0	0
PGA	13	11	7	4	3	1
Plastic PGA	100	100	100	100	100	100
Ceramic PGA	0	0	0	0	0	0
Ball/Land Grid Array	9	16	24	34	44	48
Plastic BGA	97	96	94	92	91	89
Enhanced BGA	1	1	1	2	2	3
Ceramic BGA/CGA	1	2	2	2	3	3
Metal BGA	0	0	0	1	1	1
Tape BGA	1	2	3	3	4	4
MCM	3	4	7	8	10	12
Bare Die/COB	2	2	3	5	8	10
Pin Count						
<44	0	0	0	0	0	0
44 to 84	1	1	1	0	0	0
85 to 132	9	7	6	5	3	1
133 to 196	26	24	21	19	15	10
197 to 244	28	28	26	24	20	17
245 to 304	18	19	21	22	24	27
305 to 352	13	14	15	16	18	19
353 to 476	2	3	5	5	7	10
477 to 672	1	1	2	3	4	6
>672	0	0	0	0	1	1
Bare Die	2	2	3	5	8	10

Source: Dataquest (April 1996)

Table 3-11
Worldwide Microprocessor Package Forecast (Thousands of Units)

	1995	1996	1997	1998	1999
Worldwide Total	240,502	267,752	290,342	324,785	369,656
Package Total	240,502	267,752	290,342	324,785	369,656
DIP	0	0	0	0	0
QFP	101,722	131,000	147,000	165,700	173,524
Plastic	99,586	126,939	140,973	157,249	162,939
Ceramic	2,034	3,930	5,880	8,285	10,411
MQUAD	102	131	147	166	174
Chip Carrier	632	0	0	0	0
PGA	129,000	116,246	104,210	90,539	72,411
Plastic	22,000	18,246	16,100	14,539	12,781
Ceramic	107,000	98,000	88,110	76,000	59,630
BGA/LGA	6,122	15,466	29,188	49,355	95,600
Plastic	918	3,867	11,675	22,210	47,800
Ceramic	5,198	11,584	17,484	27,096	47,704
TBGA	6	15	29	49	96
TAB	25	42	68	91	121
Bare Die	3,001	4,998	9,876	19,100	28,000
Pin Count	240,502	267,752	290,342	324,785	369,656
40 to 48	0	0	0	0	0
52 to 68	0	0	0	0	0
72 to 84	800	25	0	0	0
114 to 128	15,002	7,500	1,200	500	300
132 to 160	80,349	75,246	66,154	64,035	63,056
164 to 208	64,500	75,103	81,800	81,050	81,000
>208 to 432	43,500	60,200	74,322	86,000	101,000
>432 to 504	33,200	44,200	56,100	72,000	90,100
>504 to 600	150	480	890	2,100	6,200
Bare Die	3,001	4,998	9,876	19,100	28,000

Source: Dataquest (April 1996)

Table 3-12
Worldwide Microcontroller Package Forecast (Millions of Units)

	1995	1996	1997	1998	1999
Total Units	3,391	4,134	4,911	5,743	6,725
4-Bit	1,300	1,561	1,713	1,715	1,709
8-Bit	1,834	2,174	2,616	3,190	3,927
16-Bit and Up	257	400	582	837	1,089
4-Bit	1,300	1,561	1,713	1,715	1,709
Plastic DIP	52	31	14	5	0
Shrink DIP	130	78	17	9	0
Ceramic DIP	1	0	0	0	0
CLCC	1	2	0	0	0
QFP	104	173	192	209	239
SO	946	1,168	1,336	1,321	1,282
Bare Die	65	109	154	172	188
8-Bit	1,834	2,174	2,616	3,190	3,927
Plastic DIP	55	11	0	0	0
Ceramic DIP	18	0	0	0	0
PLCC	145	109	78	32	20
CLCC	7	2	0	0	0
QFP/TQFP	954	1,130	1,360	1,659	1,964
SO/VSO	642	900	1,143	1,420	1,787
CSP	0	2	8	16	35
Bare Die	13	20	26	64	122
16-Bit and Up	257	400	582	837	1,089
PLCC	13	4	0	0	0
CLCC	0	0	0	0	0
QFP/TQFP	139	216	308	402	468
SO/TSSOP	100	164	233	335	436
CSP	0	0	6	25	54
Bare Die	5	16	35	75	131
Pin Count					
<20 to 28	387	449	456	512	520
40 to 48	2,050	2,108	2,018	1,912	1,688
52 to 64	373	405	380	304	260
80 to 84	339	620	771	940	1,103
100 to 160	159	406	1,017	1,579	2,344
>160	0	0	54	184	370
Bare Die	83	145	215	311	440

Source: Dataquest (April 1996)

Table 3-13
Worldwide Analog Package Forecast (Percentage of Units)

	1995	1996	1997	1998	1999	2000
Package Type	100	100	100	100	100	100
Plastic DIP	5	4	3	2	1	0
Ceramic DIP	0	0	0	0	0	0
QFP	8	8	8	8	7	7
Chip Carrier	1	1	0	0	0	0
Plastic Chip Carrier	1	1	0	0	0	0
Ceramic Chip Carrier	0	0	0	0	0	0
SO	74	76	76	76	78	79
CSP/BGA	4	4	5	5	6	6
Bare Die	7	7	7	8	8	8
Percentage by Pin Count	100	100	100	100	100	100
<8-Pin	1	1	1	1	1	1
8-Pin	30	28	25	22	21	20
14-Pin	31	30	30	30	30	30
16-Pin	6	5	4	3	3	3
20-Pin	15	17	18	20	21	22
24-Pin	1	1	1	1	1	1
28-Pin	3	4	4	4	4	4
44-Pin	7	8	9	10	10	10
>44-Pin	0	0	1	1	1	1
Bare Die	7	7	7	8	8	8

Source: Dataquest (April 1996)

Table 3-14
MOS DRAM Emerging Package Technologies (Millions of Units)

	1995	1996	1997	1998	1999	2000
Die	78.2	109.2	176.8	231.4	341.4	366.5
Others	21.9	25.3	38.7	95.8	219.9	315.0
3-D Stacked	7.6	8.9	13.5	33.5	81.4	110.2
Chip-Scale	1.1	1.3	1.9	4.8	11.0	15.7
Lead on Chip	10.9	12.7	19.3	47.9	109.9	157.5
TAB	2.2	2.5	3.9	9.6	17.6	31.5

Source: Dataquest (April 1996)

Table 3-15
3-D Stackable Technology Suppliers

Company	Product	Technology Partner
Cubic Memory	DRAM	VisionTek
Dense-Pac Microsystems	DRAM, SRAM	-
Dynamem	FRAMM—Foldable Rigid Assembly Memory Module	-
Integration System Assemblies	Memory 1G solid-state recorder	-
Irvine Sensors	DRAM, SRAM, microprocessor, analog	IBM
ShellCase	SRAM, DRAM, flash, EPROM	-
Staktek	Memory, microprocessors	TRW
Texas Instruments	DRAM	-
Thomson-CSF	DRAM	-

Source: Dataquest (April 1996)

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