DATE DUE

~~David Carroll~~	~~due 6-15-87~~

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8

R. N. Noyce

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Index

February 24 '58

PNIN Switches. Feb 24 '58

In PNIN or PNP⁻N switches, the following effects will be important –

1. ~~Maximum~~ open Voltage
2. ~~Minimum~~ switching current
3. Maximum "On" Current.

In the PNIN or PNP⁻N operating by conductivity modulation, as noted in memo of 2-12-58, Increasing resistivity of P^- region will increase the open Voltage permissable. By increasing resistivity of middle N region, considerable fringing will take place, and consequently a higher current density will flow near the base contact. Thus, a small part of the total area can be used to turn the switch on; thereafter the entire area will be useful for current carrying. Thus, the current necessary for triggering will be essentially independent of ~~netto~~ area, but the total current which may be ~~used~~ switched will be ~~Pro~~proportional to area.

Designs

Let us set these arbitrary design objectives:

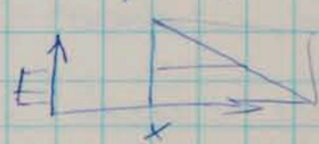
R N Noyce Feb 24, 58

V_{max} = 300 volts.

I_{max} = 100 Amps.

$I_{trigger}$ = 10 ma.

Breakdown fields in silicon are of the order of 2×10^5 V/cm., corresponding to space charge of about 10^{12} electrons/cm². The total voltage across the junction, assuming step junction heavily doped on one side is one half of the maximum field times the width of the space charge region.



$$E_{max} \times W = 600\ V$$

$$2 \times 10^5\ W = 600$$

$$W = \frac{600}{2 \times 10^5} = 3 \times 10^{-3}\ cm = 30\mu.$$

Doping density: $3 \times 10^{-3}\ C_A = 10^{12}$

$$\underline{C_A = 3 \times 10^{14}}$$

Area necessary for power dissipation:

Thermal Resistance of Silicon:

~ 1°C/watt - cm.

for 50μ thick wafer:

$$R_{th} = \frac{5 \times 10^{-3}}{A}\ °C/watt.$$

Furthermore, assuming a copper heat sink;

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The thermal resistance will be approximately

$\frac{1}{3K(\text{cm s})}$ °C/watt

For 100 Ampere use, assuming a voltage drop of 2 Volts:

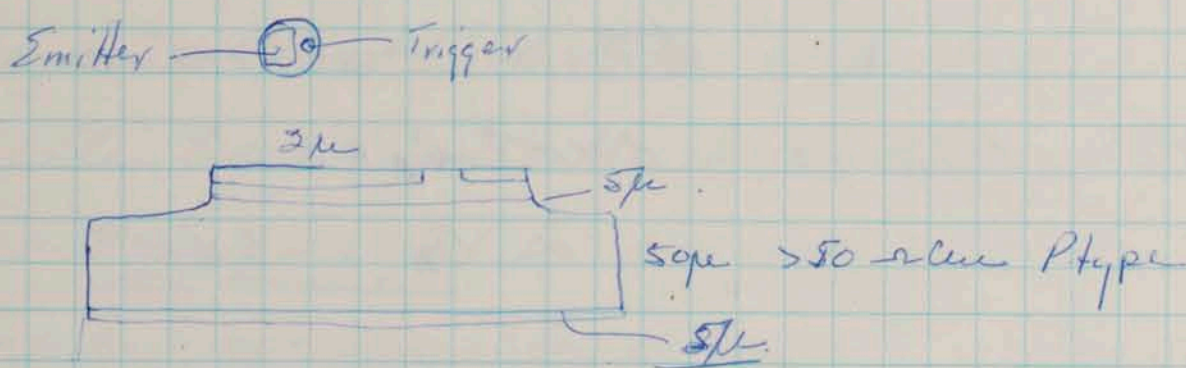
Power = 200 watts.

Limiting ourselves to 50°C Rise, the thermal resistance must be held to ¼ °/watt.

A radius of 1 cm meets this easily, perhaps we could get by with ~~#~~ 5 mm. diam.

Resistivity of Inner n layer: - Not too critical ~ 1000 Ω/sq

Final design:



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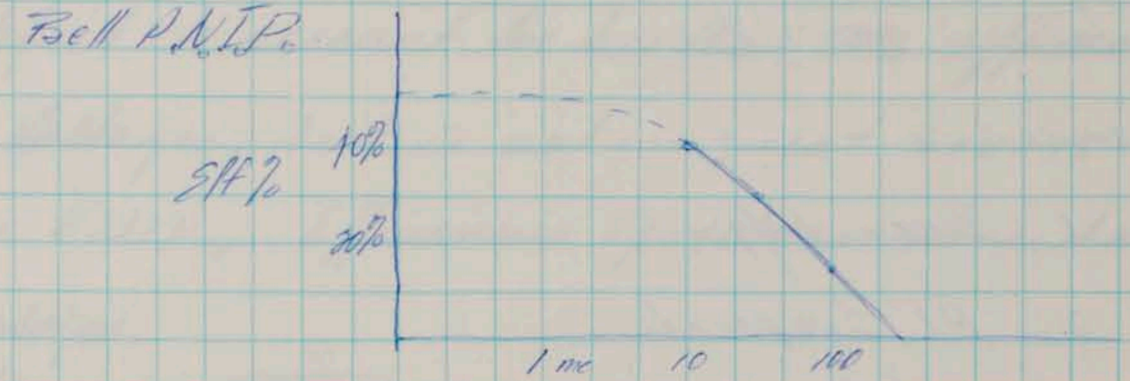
100 MCPS oscillator. – objective: 5 watts output – Design.

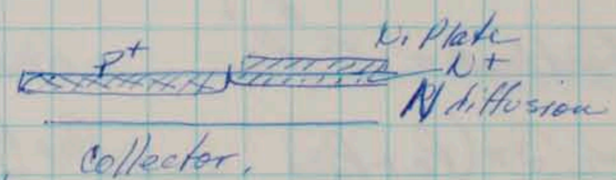
Oscillator Efficiency:

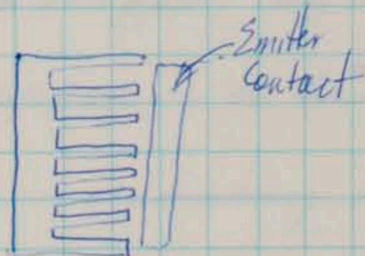


If we make a 300 mcps transistor (f max) we should be able to get 100 mcps 30% efficiency – Looks tough.

Problem will be small geometry – In the small geometry, the main limitation lies in the re indexing to be sure that the oxide mask and contact areas are in proper registration.

This idea occurs: mask say a pnp with electroless Ni plating which will serve as a mask against the diffusion of the emitter and will also serve as contact:





Other possibilities –
AL Evap + Alloy (NPN)

Typical Resistivities of the emitter layer are 5 Ω/□ –
This series resistance is undesirable, but might be tolerable.
If the evaporated film were rectifying to the silicon

RNN. Feb 25

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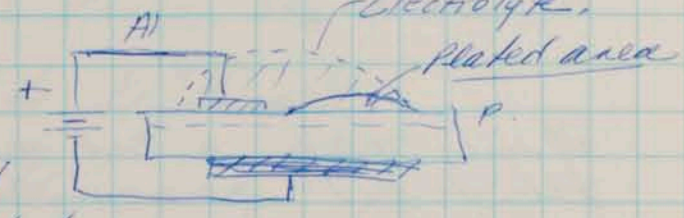
Prior to alloying, as well might be the case, this film could be biased so no plating would occur in its immediate vicinity. this is a possibility for small geometry.

For instance: on NPN.

Sequence:

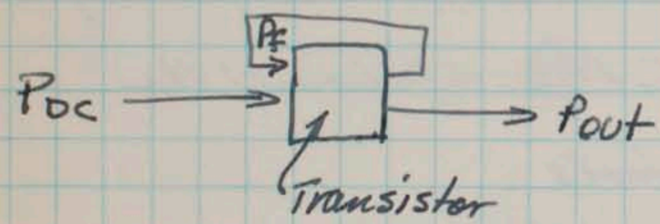
1. Base diffuse
2. Al Evaporate.
3. With bias as shown, plate Phos. bearing metal, which should not plate near Al contact.



4. Diffuse, Mesa Etch + Mount.

Feb. 26.

Pwr. oscillator Efficiency –



gain

$P_{out} + P_{feedback} = G \cdot P_f \qquad P_{out} = (G-1)P_f$

Class A: $P_{DC} = \frac{1}{\eta_0} 2 \times (P_0 + P_f) \qquad P_0 + P_f = P_0\left(1 + \frac{1}{G-1}\right) = P_0\left(\frac{G}{G-1}\right)$

$\text{Efficiency} = P_{out}/P_{DC} = \frac{P_0}{2 P_0 (G/G-1)} =$

$= \frac{1}{2}\left(\frac{G-1}{G}\right)$

If $G = G_0(1 - f/f_{max})$

$E_{ff} = \frac{1}{2}\left(\cancel{\frac{f/f_{max}}{}}\right) \quad \frac{1}{2} \quad \frac{G_0(1-f/f_{max}) - 1}{G_0(1-f/f_{max})}$

If $G_0 >> 1$

~~IBM / Specs /~~ – ~~Design Considerations.~~

Feb 26. Analysis from preceding page should be modified to account for less than 50% efficiency at low Voltages, but is not in great error.

For PNIP, Efficiencies of 40% or more have been realized.

In General. for High frequency Power oscillators – at $\frac{1}{2}$ fmax, 25% Efficiency. This seems a reasonable place to work.

For 100 mcps oscillator, 5 watts – we would need a 20 watt unit with fmax of 300 mcps.

This would give:

8–10 watts at 50 mcps.
2–3 watts at 150 mcps.

Rough design:

$f_\alpha = 250$ mcps. – $r_b' C_c = \frac{2.5\times10^8}{2\pi\times4\times10^{16}} = 4\times10^{-10}$

If $C_c = 100\ \mu\mu f$, $R_b =$ ~~$6.5\ \Omega$~~ $4\ \Omega$

This appears to be the range to work in.

Size necessary for power:

Bell PNIP uses .020 x .15 cm for 10 watts.

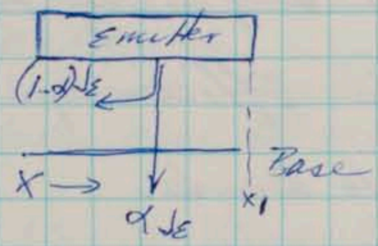
Use .040 x .15 cm = 15 mils x 60 mils.

Another 2x this area would be safer!

Problems: 1). Internal Tetroding.
to work out
2). Tetrode structures; I_{b_2} Grounded.
3). R.F. feedback in internal Tetrode.

The general problem to work out here is this: How much does internal tetroding help or hinder in High frequency power transistors.

Part I. DC current distribution



Assume 1. $J_E = J_{E0}\, e^{qV/kT}$ (neglect $-J_{E0}$ term)

2. Sheet resistance ρ_s

$$\frac{dV}{dy} = \int_x^{x_1} \rho_s J_{E0} e^{qV/kT} (1-\alpha)\, dy$$ (linear geometry, neglecting variation of α with J_E)

$$\frac{d^2V}{dy^2} = \rho_s J_{E0} e^{qV/kT} (1-\alpha)$$

$z'' = e^z$
$z''' = z'e^z$
$z'''' = z''e^z + z'e^z$

See p. 13

3 March '58

Power oscillator →

Output Impedance.

$$R_o = \frac{(1-\alpha_o)^2 + (\omega/\omega_t)^2}{\alpha_o\,(\omega/\omega_t)\,\omega C_i} = \underline{R_L} \text{ for Max gain.}$$

approximations

1. $(1-\alpha_o)^2 << (\omega/\omega_t)^2$

2 $\alpha_o \simeq 1$

Then $R_o = \omega/\omega_t\,\omega C_i$

$= \dfrac{1}{\omega_t C_i}$

Therefore, for Specs Quoted:

$R_L = \underline{300\,\Omega}$ $\underline{60V}$, $\underline{300\,ma}$

If $\frac{\omega_t}{2\pi} = 250$ mcps,

$$C_i = \frac{\cancel{1300\,\Omega}}{300 \times 2\pi \times 2.50 \times 10^6} = \frac{\cancel{1.4 \times 10^{-6}}}{\cancel{250}\,2\pi}\ \frac{100}{47.2}\ \mu\mu f = \underline{2.1\,\mu\mu f}$$

Total capacitance, say 4x or $\underline{10\,\mu\mu f}$ at 28 VDC.

Feedback capacitance $< 3\ \mu\mu f$ –

Calculations of V.H.G.

Geometry:	Diameter (mils)	Area (cm^2)
Emitter	15	1.1×10^{-3}
Collector	30	4.4×10^{-3}
Inner base.	20.5	

Wafer thickness 50μ – uniform Doping.

Transistor	A		B	
C_{oe} – cm^{-3}	3×10^{19}		5×10^{19}	
C_{ob} "	5×10^{18}		5×10^{18}	
C_{wafer} "	4.5×10^{14}	(10 Ω cm)	6×10^{15}	1 Ω cm
$\sqrt{Dt}_e$ cμ	.563		.64	
$\sqrt{Dt}_b$	.834		1.3	
R_{BE} Ω/□	816		411	
$\bar{x}_e$	1.9		2	
$\bar{x}_c$	4.6		6.	
BV_{CB}	140 – 160		65 – 85	
BV_{EB}	14 – 17		6 – 10	
$r_{bb'}$	43.3		23.4	
$r_{cc'}$	45		4.5	
f_{hb}	274		81	
C_{TC} pf@10V	7.8		23.3	
C_{TE} pf@ .5V	70		102	
f_{max}	356		153	
P_{BB}	219		143	
a_E	8.2×10^{21}		356×10^{-12}	
a_C	1.6×10^{19}		1.15×10^{20}	
W_b μ@10V	1.8 μ		3.3 μ.	

for 5 Ω cm .5V off 23×2 V swing

$46 \times 100 = 4.6$ watts $/4 = 1.15$ watts

$\eta = \frac{1.15}{2.8} = 41\%$

for Gain of 5 – $\eta = \frac{4}{5} \times 41. = 32.8\%$

Area necessary for power dissipation:

from hemisphere: $R \propto \frac{1}{r}$

$$R_{th} = \frac{1}{2/3\, \sigma \pi r}$$

$$E = \frac{J\rho}{4/3 \pi r^2}$$

$$V = J\int \frac{\rho\, dr}{4/3 \pi r^2}$$

$$= J \frac{\rho}{4/3 \pi r}$$

σ silicon = .20 cal/cm °C
.84 watts/cm °C.

for r = 7 mils = .00276 cm

$$R_{th} = \frac{1000}{.84 \times 2.76 \times \pi \times \frac{2}{3}} = \underline{208°C/watt.}$$

Cu: σ_{th} .918

Assuming 50μ wafer.

$$R_{th} = \frac{l}{\sigma A} = \frac{5 \times 10^{-3}}{.84 \times 1.1 \times 10^{-3}} = 5.5°/watt$$

Semi-infinite Cu Block:

$$R_{th} = \frac{1000}{\frac{2}{3} \times 4.2 \times .918 \times 3.14 \times 2.76} = 45°/watt$$

Total resistance = 50°/watt.

Fringing will raise the total resistance — For simple geometry, area cannot be smaller than the area given. This is pushing it to the limit. Also, the thermal resistance of the silicon is small compared to that of the copper. Silver is only 10% higher.

For this area, and a capacitance of 1.5 μμf, the space charge region would have to be:

$$C = 10^{-12}\frac{A}{d} = 10^{-12} \times \frac{1.1 \times 10^{-3}}{d} \qquad d = 11\,\mu.$$

Transit time for intrinsic region: $\frac{10^{-3}}{v_{limit}} \sim 10^{-10}$ sec

The output capacitance does look possible. However, it does ~~not~~ not appear to be the best compromise to get power out from a 28V V_{cc} supply. For this, it would be better to ~~[illegible]~~ design to breakdown voltage.

Design to say 70 V_{CBO}.

$E_{max} = 2 \times 10^5$ Volts.

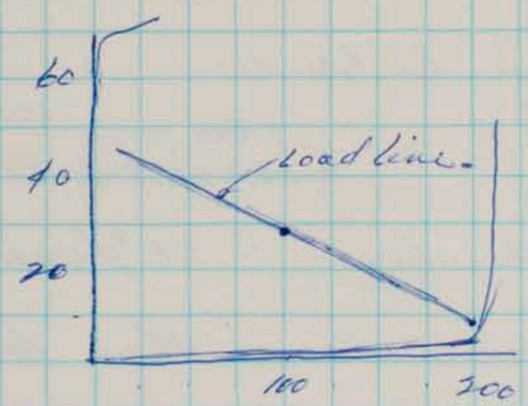
$E_{av.} = E_{max}/2 = 10^5$

for 70V Breakdown, $X_{spchg} = 7\mu$

Capacitance at 70V = 2.36 $\mu\mu f$.

f_T (opt) = $\frac{1}{2.36 \times 10^{-12} \times 200\Omega \times 2\pi}$ = 338 mc

Assuming 10 Ω Rsat, and 200 ma – 2V drop. adding say 5V for [illegible] – 7 volts –



If max Efficiency is limited to, say, 40%, from Page 6:

$$\eta = \eta_0 \left(\frac{G-1}{G}\right)$$

Assuming G = 3 =, $\eta = \frac{2}{3}\eta_0 = \frac{2}{3} \times 40\% = 26.5\%$

for 35% Efficiency Gain = 8 = 9 db – 1½ Octaves.

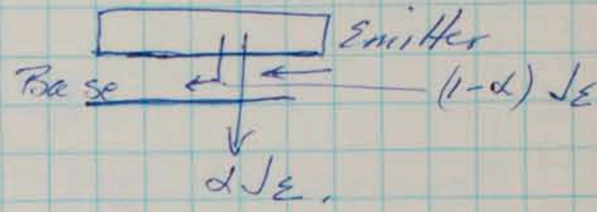
for 30% Eff – 3.33 watts in, 1 watt out

28 V DC Source 118 ma

Internal Tetrode - Effects on feedback, Rc, Etc. - P. 8. cont.

1. Linear, semi-infinite geometry.

2. Circular - ie cylindrical.



Linear case:

$$\frac{dV}{dy} = \int_x \rho_b e^{\frac{qV}{kT}} dy \ (1-\alpha)$$

$p = V$

$\frac{dp}{dz} = e^{\int p\,dx}$

$$\frac{d^2V}{dy^2} = \rho_b e^{qV/kT} (1-\alpha)$$

Circular: $$\left.\frac{dV}{dy}\right|_R = \frac{1}{2\pi R}\int_0^R \rho_b \ 2\pi r \ e^{qV/kT} (1-\alpha)\, dr$$

$$\frac{d^2V}{dr} = \frac{-\rho_b}{2\pi r^2}\int_0^r \qquad + \frac{\rho_b}{2\pi r} e^{qV/kT}(1-\alpha)\, dr$$

$p = \frac{dz}{dy}$ $\quad \frac{d^2z}{dy^2} = \frac{dp}{dy} = \frac{dp}{dz}\frac{dz}{dy} = p'p. =$

$p = e^z$

$\frac{dp}{dy} =$ $\quad p' = \frac{e^z}{p}$ $\quad pp' = e^z$ $\quad p = \frac{dz}{dy}$ $\quad \frac{dz}{\sqrt{e^z}} = dx$

$\frac{p^2}{2} = e^z + C$

$n = ^{-1}$ $\qquad V = p^2$

$y' + p(x)y = q(x)$ $\qquad y = C\left[e^{-\int p\,dx}\right] + e^{-\int p\,dy} e^{\int q(x)} e^{+\int (x)}$

Linear case $\quad \frac{d^2z}{dy^2} = e^z$ $\qquad$ let $p = \frac{dz}{dy}$ $\quad \frac{dp}{dz} = p'$

$pp' = e^z$ $\qquad pp' = \frac{dp}{dy} = \frac{d^2z}{dy^2}$

$\frac{p^2}{2} = e^z + a$ $\qquad$ let $y = z + \ln a$

~~for particular soln~~ $\quad p = \sqrt{2(e^z + a)} = \frac{dz}{dy}$

$$\frac{dz}{\sqrt{2(e^z + a)}} = dy$$

$$\frac{dz}{\sqrt{2(e^z+a)}} = d\psi \qquad \text{let } e^z = y$$
$$e^z dz = dy$$
$$dz = \frac{dy}{y}$$

$$\int \frac{dy}{y\sqrt{2y+a}} = \int d\psi$$

$$\left(\psi + b = \frac{2}{3a^2}(2y+a)^{3/2} - \frac{a}{2}(2y+a)^{1/2} \right)$$ #25 handbook

Check: $e^z = y \qquad \ln y = z$

$$\frac{dz}{d\psi} = \frac{1}{y}\frac{dy}{d\psi}$$

$$\frac{d^2z}{d\psi^2} = -\frac{1}{y^2}\left(\frac{dy}{d\psi}\right)^2 + \frac{1}{y}\frac{d^2y}{d\psi^2}$$

$$\frac{d^2y}{d\psi^2} - \frac{1}{y}\left(\frac{dy}{d\psi}\right)^2 = y^2$$

let $p = \frac{dy}{d\psi} \quad \frac{dp}{d\psi} \quad p' = \frac{dp}{d\psi} \qquad \frac{d^2y}{d\psi^2} = \frac{dp}{dy}\frac{dy}{d\psi} = pp'$

$$pp' - \frac{1}{y}p^2 = y^2 \qquad \text{no help.}$$

Referring to original Eqn:

$$\frac{d^2V}{d\psi^2} = J_0\rho_D\, e^{qV/kT}(1-\alpha)$$

To reduce to $z'' = e^z$: let $z = \frac{qV}{kT} + \ln a$

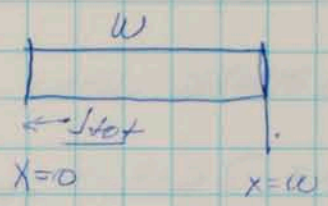
$$z'' = \left(\frac{q}{kT}\right)^2 V'' \qquad e^z = a\,e^{qV/kT}$$

$$z'' = \left(\frac{q}{kT}\right)^2 \frac{e^z}{a}\,\rho_D(1-\alpha)J_0$$

Then $a = J_0\rho_D(1-\alpha)\left(\frac{q}{kT}\right)^2$

This seems to be a solution for linear case OK. Finding inverse function perhaps difficult. Plot ψ vs. y.

Boundary conditions



at $x = w$, $\frac{dy}{d\psi} = 0$, $\frac{d\psi}{dy} = \infty$

at $\psi = 0$, $\frac{dy}{d\psi} = f(y, \rho_b)$ ← given total current

$$d\psi = \left(\frac{1}{a^2}(2y+a)^{1/2} + \frac{1}{4\sqrt{2y+a}}\right)2dy$$

$$2y(w) + a = -\frac{a^2}{4}$$

$$y(w) = \frac{a}{2} - \frac{a^2}{8}$$

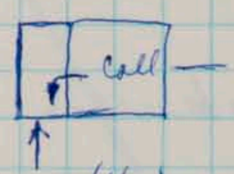
Plan of calculation:

1. Calculate $J(r)$
2. Calculate $\frac{d\,J_{Tot}}{d\,V_{base}}$ (r_b')
3. Calculate $\frac{dJ_{Tot}}{dV_{collector}/\omega}$ (C_c) (small sig, linear) by calculating $V(r)$, integrating $V(r)\,J(r)\,dr$.
4. Reduce to Equiv. ckt values.

$\frac{dy}{dV} \propto y$

$\frac{dV_b}{dV_c} = ?$

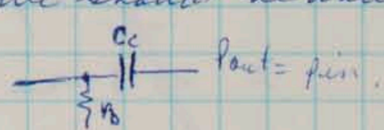
What is $r_{bb'}$ C_c feedback? –



Gain = 1 when
$$\beta = \frac{dJ_{Tot}}{dV_B} \Big/ \frac{dJ_{Tot}}{dV_{coll}} = \frac{dV_c}{dV_b}\Big|_{J_{Tot} = const}$$

If this is correct interpretation, we should be able to predict f_{max} formula correctly

$$\beta = \frac{f}{f_\alpha}$$



Ask Kromer about this.

look up calculations on circular geometry.

March 7 '58.

References on Emitter current distribution:
Gudmundsen - Sigcorps Rept final on SXB1
BTL Eng. Sem. #4 or #5 D. H. Looney.

Simple minded approach to fringing:

1. Characteristic length $= \left[\left(\rho_s I_b / 2\pi r_e \right) \cdot q/KT \right]^{-1}$

In our case:

$I_b = 10^{-2}$ amps
$\rho_s = 800\ \Omega/\square$
$r_e = .0375$ cm

$$l = \left[\frac{800 \times 10^{-2}}{6.28 \times .0375} \cdot 40 \right]^{-1}$$

$$= \frac{1}{1300} = \underline{7.4\,\mu}. \;!!$$

Collector Spreading resistance

$$R = \frac{1\ \Omega\text{cm}}{2\pi \times .0375} \ln \overset{1.9}{\frac{50}{7}}$$

$$= \underline{8.1\ \Omega}.$$ Does not look too bad.

Base Spreading resistance:

under Emitter: $\rho_s \dfrac{7.4}{6.28 \times 375}$

$= .00312\ \rho_s$

$= 2.5\ \Omega$

Series r in base: $\sim 5\ \Omega$
$R_{b\,tot} = 8\ \Omega$.

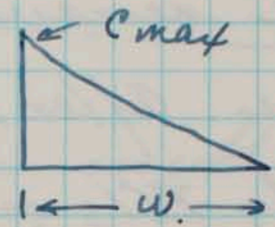
Current density:

assume 200 ma in area $2\pi(.0375 \times .0007)$

$$J = \frac{.2}{6.28 \times .0375 \times .0007} = 1.25 \times 10^3 \text{ amp/cm}^2$$

Characteristic current for base conductivity modulation.

Carrier dist. in base:



for 2μ base width. pnp.

Gradient $= C_{max} \times 5000$ /

$J = q D \, \text{grad} C.$ .2 Ωcm at $10^{17}/\text{cm}^2$

$\mu = 300$

$D = 300/40 = 7.5$

$= 1.6 \times 10^{-19} \times 7.5 \times 5 \times 10^3 \, \underline{C_{max}}^{10^{17}}$

$= 560 \text{ amps/cm}^2$

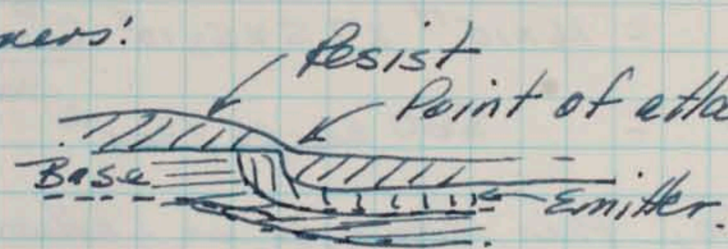
So, this range is getting dangerous for β fall off.

March 10 '58.

Indexing problem:

Here is another approach to the indexing problem which might work.

On oxide removal, we leave some relief on the surface. After further oxidation, or perhaps Erosion by BCl_3 in the diffusion operation, this relief will still be present. Perhaps a resist could be found which had enough surface tension that it would pull away from these sharp corners:



If so, acid Etch would attack first in the area where it is desired to remove metal causing emitter-base shorts. This being the case no reindex would be necessary: the oxide Etching would settle the geometry, both of n + p areas, and of contact areas.

Distribution of current in the base.

Assume: 1. Circular geometry.
2. Uniform base sheet Resistivity.
3. $J = J_0 e^{qV/kT}$.

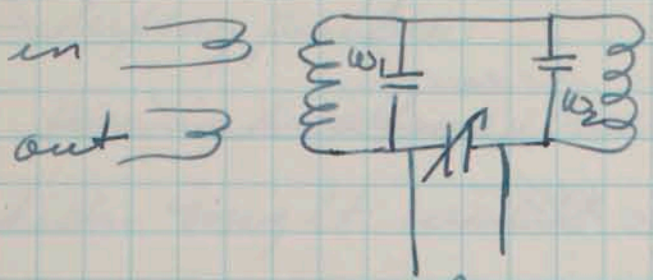
March 14 '58

Discussion this noon with Dean Watkins and Dick Johnson about, among other things parametric amplifiers. Watkins analysis of the situation is this: Masers, although of proven low noise, are narrow band and require liquid helium reservoir. Ferromagnetic parametric amplifiers are tricky in alignment, etc. The semiconductor capacitor, and the electron beam ~~requires~~ parametric capacitors seem to hold the most promise.

The requirement on the semiconductor diode are:

1. High Q i.e. low R_{series}.
2. Low inductance lead arrangement.
3. Low loss package. (Not ceramic, too high dielectric — low loss glass. 707 Seals to W in small size. Seals to 7052

Basic principle of amplifier.



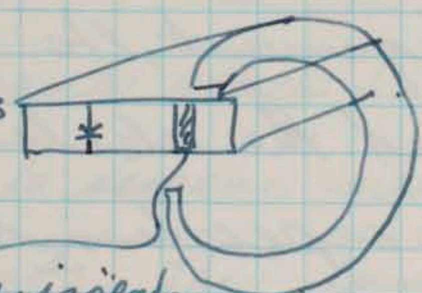
Pump $\omega_3 = \omega_1 + \omega_2$

Pump at ω_3 causes neg resistance across Tank $\omega_1 + \omega_2$. Power can be taken out at Either ω_1 or ω_2.

This amplifier is reciprocal: some isolation is needed, or perfect matching so reflections are not amplified.

Iterated Amplifier:

Require ~~ω~~ $V_{\omega_1} = V_{\omega_2} = V_{\omega_3}$ for this, to work.



ferrite isolator.

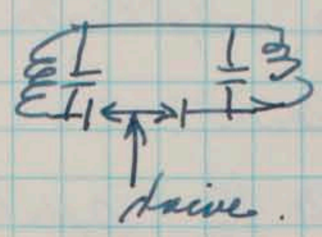
These equal phase velocities are more easily achieved in co-axial

Mar 17 '58 - D. Watkins phoned to give these numbers: on BTL Capacitor for Parametric Amp.

Q at 3000 mcps. 5 to 10

C = .3 ~~μ~~μf near zero bias.

Uhlir discussed the possibility to use doubling by the use of 2 capacitors back to back:



This gives effective drive of twice the frequency actually used: Q of course may suffer.

Mounting similar to 1N23, with small pin at both ends.

April 8 '58.

Problems of Emitter Capacitance.

In the case of the forward biased Emitter junction, the emitter capacitance becomes a little difficult to calculate. Firstly, the straight transition capacitance is important, but we can no longer assume only the ionized impurities, but we must also consider the mobile charges in the space charge region. This argument holds for the diffusion capacitance as well: it is due to mobile charges.

Diffusion capacitance.

Assuming a given distribution of $N_d - N_a$ in the base, and assuming $J_p \ll J_n$

Eqns. for current flow.

$$J_n/q = D_n \frac{dn}{dx} + n\mu_n \vec{E}$$

$$J_p/q = D_p \frac{dp}{dx} - p\mu_p \vec{E} = 0$$

$$p = N_a(x) + n(x) \qquad dp/dx = \frac{dN_a}{dx} + \frac{dn}{dx}$$

$$E = \frac{D_p}{p\mu_p}\frac{dp}{dx} \qquad D = \frac{kT}{q}\mu$$

$$\frac{J_n}{q} = D_n \frac{dn}{dx} + D_n \frac{n}{p}\frac{dp}{dx}$$

$$= D_n\left[\frac{dn}{dx} + \frac{n}{n+N_a}\left(\frac{dn}{dx} + \frac{dN_a}{dx}\right)\right]$$

$$= D_n\left[\frac{2n+N_a}{n+N_a}\frac{dn}{dx} + \frac{n}{n+N_a}\frac{dN_a}{dx}\right]$$

$$\frac{J_n}{qD_n} = \left(1+\frac{n}{n+N_a}\right)\frac{dn}{dx} + \frac{n}{n+N_a}\frac{dN_a}{dx}\Bigg]$$

Scheme for integrating:

x	N_a	$\frac{dN_a}{dx}$
$0\Delta x$		
$1\Delta x$		
$2\Delta x$		

Set up as difference Eqn:

$$\frac{J_n}{qD_n} = \left(1+\frac{n_k}{n_k+N_k}\right)\frac{n_{k+1}-n_k}{\Delta x} + \frac{n_k}{n_k+N_k}\,\frac{N_{k+1}-N_k}{\Delta x}$$

Known: $n_k, N_k, N_{k+1}, \Delta x$ Solve for n_{k+1}

$$n_{k+1} = \left(\frac{n_k+N_k}{2n_k+N_k}\right)\Delta x\left[\frac{J_n}{qD_n} + \frac{2n_k+N_k}{(n_k+N_k)\Delta x}n_k - \frac{n_k}{n_k+N_k}\frac{(N_{k+1}-N_k)}{\Delta x}\right]$$

$$n_{k+1} = n_k + \frac{n_k + N_k}{2n_k + N_k} \Delta x \frac{J_n}{q D_n} + \frac{n_k}{2n_k + N_k}(N_{k+1} - N_k)$$

Perhaps exponentials could be used:

$$N_a = Ae^{-ax} + Be^{-bx}$$

$$\frac{dN_a}{dx} = -aAe^{-ax} + bBe^{-bx}$$

Looks messy. – Difference Eqn better.

We can also calculate transit time from $Q/I = T_{trans}$.

In order to make as general as possible, divide through by x_0, $\underline{N_{a\,max}}$ — J/J_0 - let $J_0 = \frac{q D_n N_b}{x_w}$

Results are still dependent on D, which is not a constant (or μ) However, this should be reasonably good indication of transit time, using mobility appropriate to maximum doping density. Work out for values of J/J_0 = .01, .1, 1, 10 To calculated transit time, the time in going through the space charge region must be added.

Derivation of Formulae for check: this time for pnp.

Consider:
1. pnp transistor.
2. Known $N_d - N_a$ vs $x = N(x)$

approx: 1. Assume Electrostatic Neutrality.
2. $J_n << J_p$.

$$\frac{J_p}{q} = \frac{kT}{q}\mu_p \frac{dp}{dx} + \mu_p p E = \text{Const}$$

$$\frac{J_n}{q} = \frac{kT}{q}\mu_n \frac{dn}{dx} - \mu_n n E = 0.$$

$$n + N(x) = p$$

$$\frac{dn}{dx} + \frac{dN(x)}{dx} = \frac{dp}{dx}$$

$$\frac{J_n}{q} = \frac{kT}{q}\mu_n\left(\frac{dp}{dx} - \frac{dN(x)}{dx}\right) - \mu_n(p + N(x))E = 0$$

$$E = \frac{kT}{q}\left(\frac{dp}{dx} - \frac{dN(x)}{dx}\right) \Big/ p + N(x)$$

Then

$$\frac{J_p}{qD_p} = D_p\frac{dp}{dx} + \frac{p}{p+N(x)}\left(\frac{dp}{dx} - \frac{dN(x)}{dx}\right)$$

$$\frac{J_p}{qD_p} = \frac{2p(x) + N(x)}{p(x) + N(x)}\frac{dp}{dx} - \left(\frac{p(x)}{p(x)+N(x)}\right)\left(\frac{dN(x)}{dx}\right)$$

$$\frac{dp}{dx} = \frac{p(x) + N(x)}{2p(x) + N(x)}\left[\frac{J_p}{qD_p} - \frac{p(x)}{p(x)+N(x)}\frac{dN(x)}{dx}\right]$$

looks OK.

Calculations on actual structure.

C_{oE} 5×10^{20} Gaussian.

C_{oB} 5×10^{18}

x_E $= 2.6\mu$

x_C $= 4.6\mu$

C_{wafer} 5×10^{15}.

From the above:

$\sqrt{Dt}$ base 1μ,

at 2.6μ, $C_B = 3.3\times10^{17}$ $\frac{C_B}{C_{oE}} = .00066$

Calculation for simple case.

assume $N(x) = 0 \qquad x < w$
$\qquad\qquad N(x) = -N_E \qquad x > w.$

$N(x) = ax$
$$\frac{dp}{d\psi} = \frac{p(x)+ax}{2p(x)+ax}\left[J - a\frac{p(x)}{p(x)+a(x)}\right] \qquad \frac{dp}{d\psi} = a$$

Look at Fletcher

for $x < w$.

$$\frac{dp}{d\psi} = \frac{1}{2}\frac{J_p}{q D_p}$$

Then $\qquad p(w) = \frac{1}{2}\frac{J_p}{q D_p}\, w$

for $x > w$

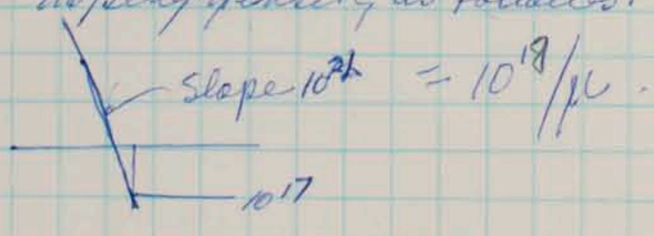
$$\frac{dp}{d\psi} = \frac{p(x) + N_E}{2p(x) + N_E}\,\frac{J_p}{q D_p}.$$

We have to consider the term $\frac{dN}{d\psi}$ which under above approximation is infinite at $x = w$

However, to get order of magnitude of minority carrier density at maximum of Base doping we might use $\quad p = \frac{1}{3}\frac{J_p}{q D_p}\, w$

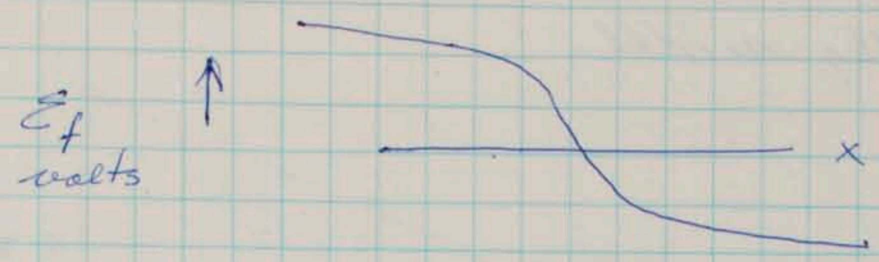
Or conversely, knowing p at this point, which will very nearly be in equilibrium with the Emitter we can calculate the current flow.

1. Assume doping density as follows:

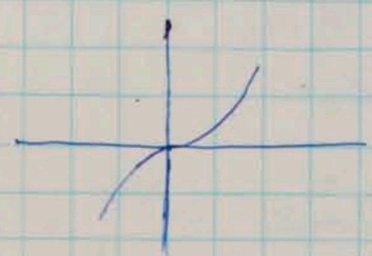


Voltage drop across junction for equilibrium is equal to difference in fermi levels for the material at the edge of the space charge region.

Plot



2. volts vs space charge width



The intersection gives the Equilibrium space charge width. Under forward bias, the current will be given by $I_0 \left(e^{qV/KT} - 1\right)$ where

$$I_0/A = 3q \frac{n_i^2}{N_{B\,max}} D_n/W = \cancel{3\,I_n}$$

For
$n_i = 3 \times 10^{10}$
$W = 2 \times 10^{4}$
$N_{B\,max} = 10^{17}$
$I_0 =$

$.075\ \Omega\,cm$

$\frac{7.5 \times 10^{15}}{9 \times 10^{3}} = 8.3 \times 10^{11}$

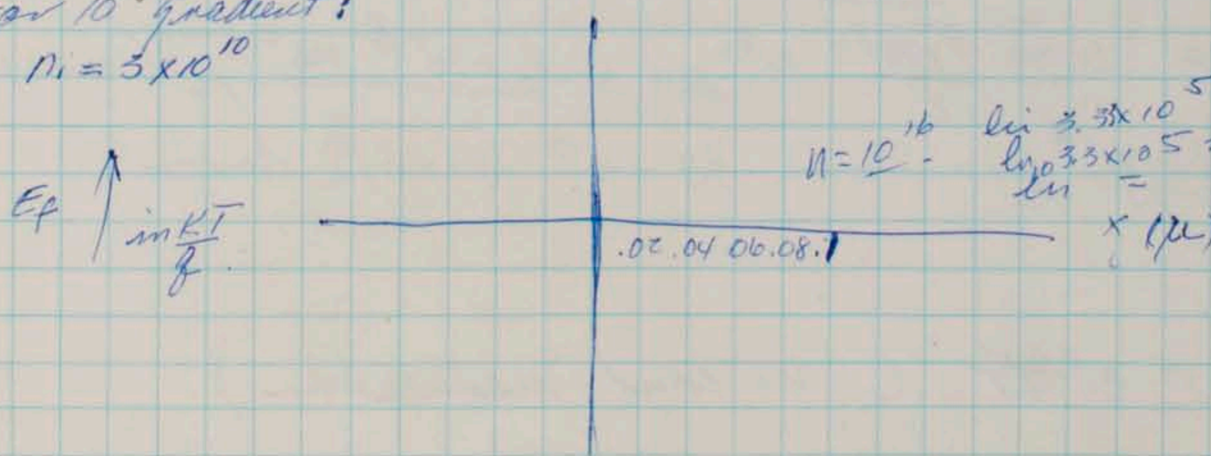
$E = \frac{.078}{.0002} \quad 390\ V/cm$

$$\frac{n_i^2}{N_{B\,max}} = \frac{9 \times 10^{20}}{10^{17}} = 9 \times 10^{3} \qquad 3q \frac{N_i^2}{N_b} \frac{D_n}{W} = \frac{390}{8.3 \times 10^{11}} = 4.7 \times 10^{-10}\ \frac{Amp}{cm^2}$$

$$I_0 = 4.7 \times 10^{-10}\ amp/cm^2$$

For 10^{18} gradient:
$n_i = 3 \times 10^{10}$

2.303
$.06$



$n = 10^{16}$. $\ln 3.33 \times 10^{5} =$
$\log_{10} 3.3 \times 10^{5} = 5.52$
$\ln = 12.7\ KT =$

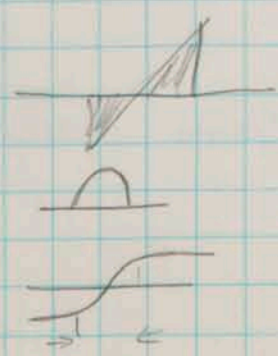
Potential vs. sp. chg width.

$$\cancel{\frac{V}{2} = \int_{-w}^{0}}$$

$$\nabla^2 V = -\frac{\rho}{\varepsilon} = -\frac{qax}{\varepsilon}$$

$$\nabla V = E = -\frac{qax^2}{\varepsilon 2} + \frac{qaw^2}{\varepsilon 2}$$

$$V = -\frac{qax^3}{\varepsilon 6} + \frac{qaw^2x}{\varepsilon 2} +$$



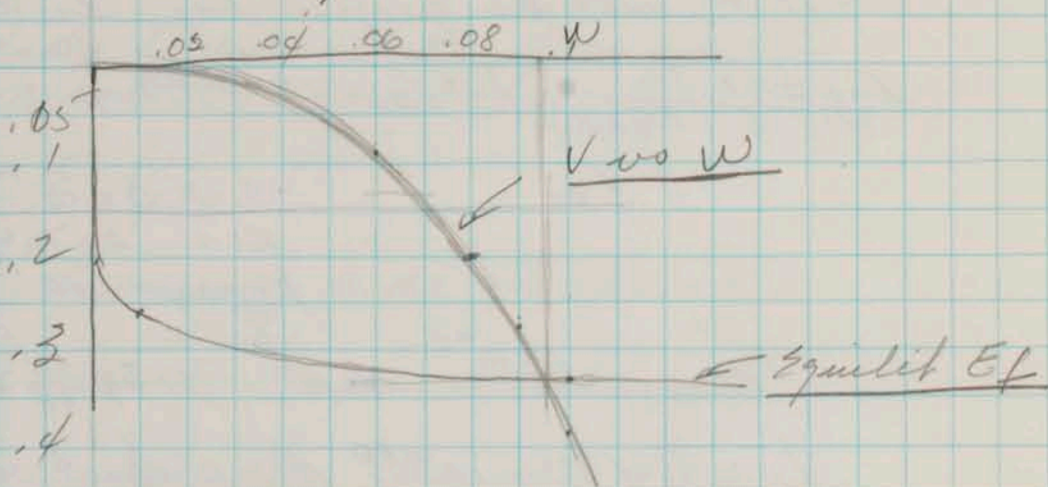
$$\Delta V = 2V(w) = 2\times\frac{qa\,w^3}{\varepsilon\,3}$$

$a = 10^{22}$

Error → $= 2\times\frac{1.06\times10^{-12}}{3}\,a\,w^3 \quad = 2\times 38.7\ w^3 \quad (w \text{ in } \mu)$

$w = \left(\frac{\Delta V}{77.4}\right)^{1/3}$

Equilibrium Built in voltage



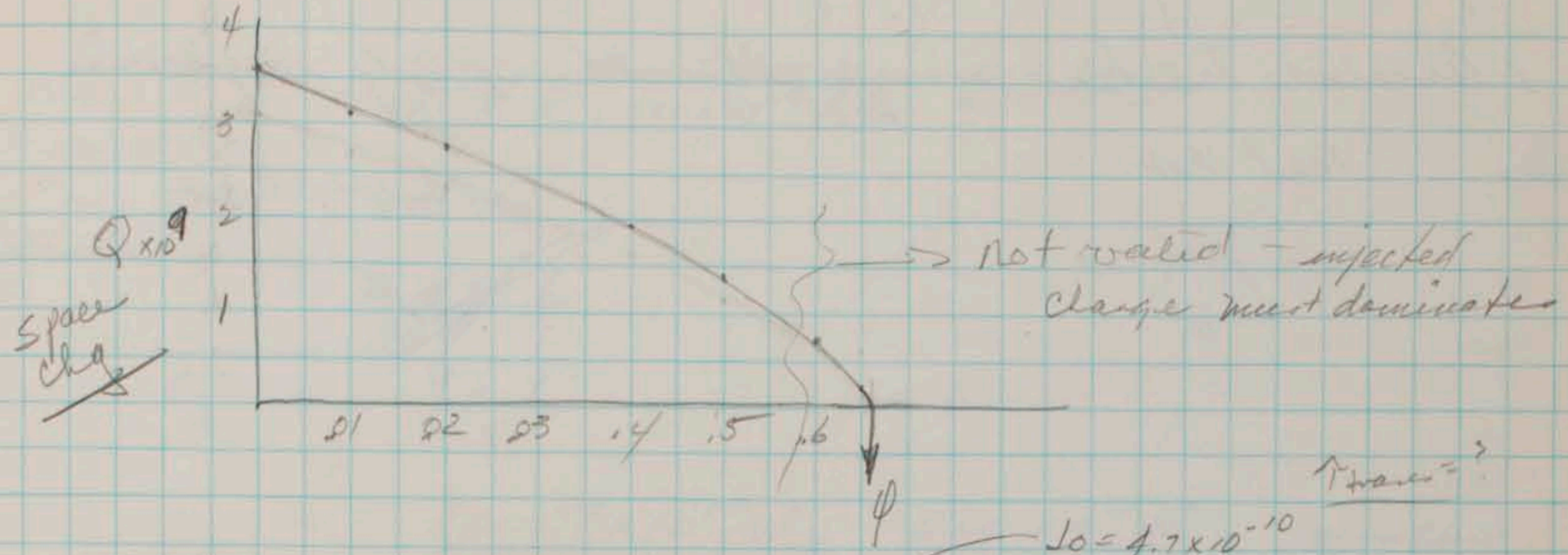
$$Q = \varepsilon E_{max} = \varepsilon E(0) = \frac{qaw^2}{2}$$

$$= \frac{1.6\times10^{-19}\times10^{22}}{2}\,w^2 = 8.\times10^{-6}\,w^2 \,/\text{cm}^2 \,(w \text{ in } \mu)$$

$$Q = 8\times10^{-6}\left(\frac{V_2-V_1}{17}\right)^{2/3}/\text{cm}^2 = \quad = 1.7\times10^{-7}\,(V_2-V_1)^{2/3}\ \text{coul/cm}^2$$

Q vs I:

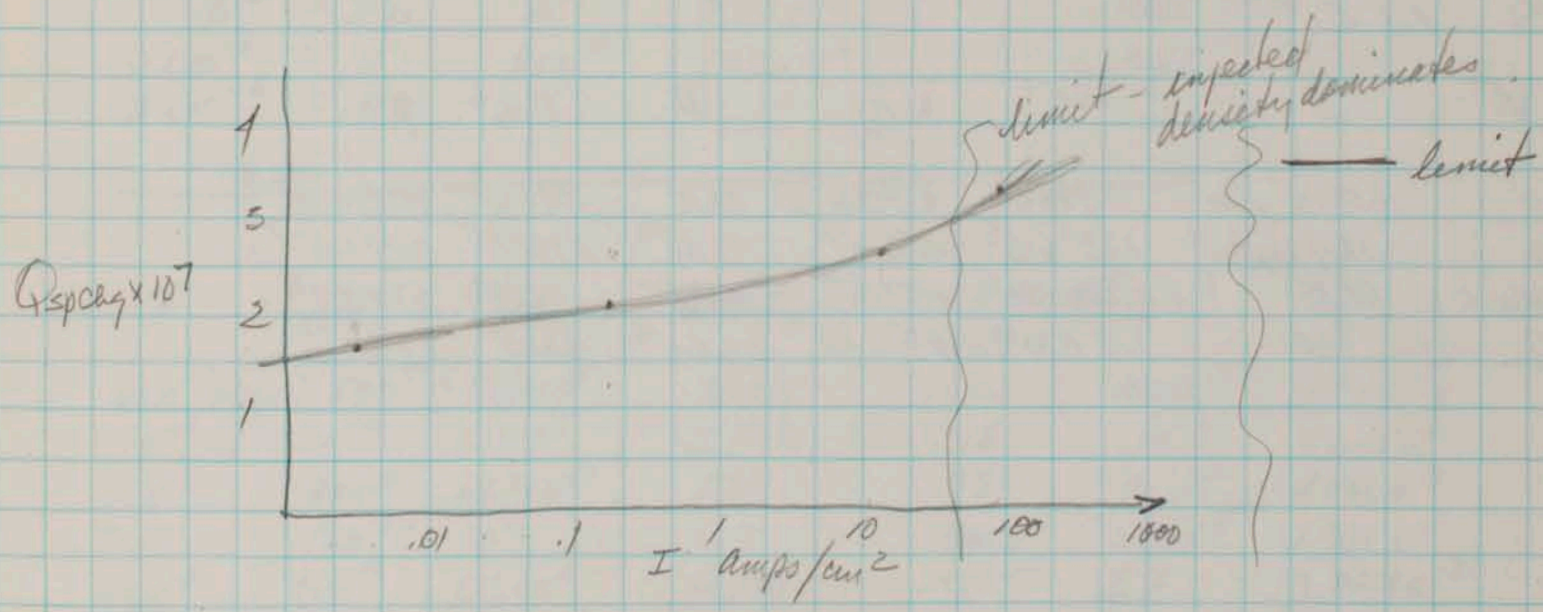
$$I = I_0\,e^{\frac{e\Delta V}{kT}} \quad (\text{ no cond. modulation })$$



↑trans = ?

$J_0 = 4.7\times10^{-10}$

V	φ-V	Q		$e^{40V}-1$		$I_0 e^{V/40} = I$		Q(0) - Q
0	.66	6.1	3.58	1 - 1 = 0		0		0
.1	.56	5.35	3.14	54.6	53.6	2.52×10^{-8}	/cm^2	.44
.2	.46	4.75	2.79	2.98×10^{3}		1.4×10^{-6}		.78
.4	.26	3.25	1.91	8.85×10^{6}		4.15×10^{-3}		1.67
.5	.16	2.35	1.38	4.84×10^{8}		2.27×10^{-1}		2.2
.6	.06	1.22	.718	2.64×10^{10}		1.24×10^{1}		2.76
.65	.01		.219	1.95×10^{11}		9.15×10^{1}		3.36
.66			0					

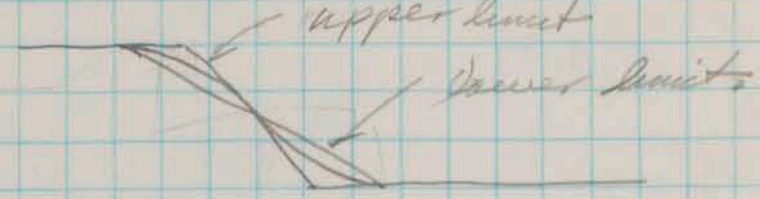


Injected density in sp. chg region:

1. Assume constant imrefs through sp. chg regions.

2. Max Est:

no - plot it.



Approx used (not considering mobile carriers ok until Debye length ~ sp. chg width.)

Forward Bias Debye length =

Order of magnitude calculation of injected charge.

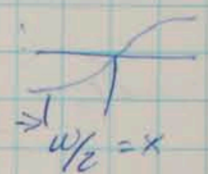
$$Q = n_i e^{qV/2kT} W$$

V	I	$e^{qV/2kT}$	$\times n_i$ (1.3×10^{10})	W	n/cm^2	qn
.4	$1.15\times10^{-3}/cm^2$	2.98×10^3	8.95×10^{13}	8×10^{-6}	7.1×10^8	1.13×10^{-10}
.6	12.4 amp/cm^2	1.63×10^5	4.9×10^{15}	4×10^{-6}	1.96×10^{10}	3.14×10^{-9}
.65	91.5	4.42×10^5	1.3×10^{16}	1.3×10^{-6}	1.7×10^{11}	2.7×10^{-8}
.7	1.3×10^{2} 660	1.18×10^6	3.54×10^{16}	1.3×10^{-6}	4.6×10^{11}	7.4×10^{-8}

Apr. 14. Check on previous Calculation.

Constants. $\frac{kT}{q} = \cancel{}\ 25\ mV.$ $\quad \varepsilon = 1.06 \times 10^{-12}\ f/cm \quad n_i = 3 \times 10^{10}$

$$\Delta V = 2V(w/2)$$



$$= \frac{2}{3} \frac{q a x^3}{\varepsilon}$$

$$\frac{\Delta V}{2} = \frac{q a x^3}{3 \varepsilon}$$

$$= \frac{1.6 \times 10^{-19} \times 10^{22} w^3}{3 \times 1.06 \times 10^{-12}} = 5.04 \times 10^{14} w^3 \quad w \text{ in cms}$$

$$= 5.04 \quad w^3 \quad w \text{ in } \mu.$$

$$Q = 1.6 \times 10^{-19} \frac{a w^2}{2} = 8 \times 10^{12} w^2 (cms) = 8 \times 10^{-6} w^2 (\mu)$$

Equilib Fermi Level

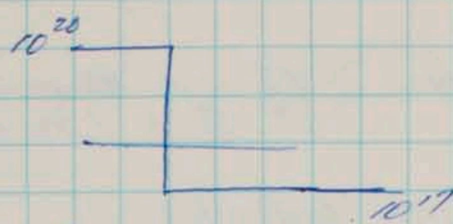
$$\varepsilon_f - \varepsilon_i = \frac{kT}{q} \ln \frac{n}{n_i} = .025 \ln \frac{a \cdot x}{3 \times 10^{10}} = .0576 \log_{10} \frac{ax}{3 \times 10^{10}}$$

x	ax	~~$\varepsilon_f - \varepsilon_i$~~ $\frac{ax}{3 \times 10^{10}}$	.025 ln
$3 \times 10^{-6} = .03\mu$	3×10^{16}	10^6.	.3455V
$10^{-5} = .1\mu$	10^{17}	3.3×10^6	.375
$5 \times 10^{-6} = .5$	5×10^{16}	1.66×10^6	.358
$2 \times 10^{-6} = .02$			

---

x	ax	$\frac{ax}{3 \times 10^{10}}$	$\ln_{10}\left(\frac{ax}{3 \times 10^{10}}\right)$	$\times .0576 = \varepsilon_f - \varepsilon_i$	x^3	$\frac{\Delta V}{2} = x^3 \times 5.04$.	$Q = 8 \times 10^{-6} w^2$
5×10^{-7} (.005μ)	5×10^{15}	1.667×10^5	5.221	.302	1.25×10^{-7}	6.3×10^{-5} V	2×10^{-10}
10^{-6} .01	10^{16}	3.33×10^5	5.522	.318	10^{-6}	5.04×10^{-4}	8×10^{-10}
2×10^{-6}	2×10^{16}	6.67×10^5	5.822	.336.	8×10^{-6}	4.03×10^{-3}	32×10^{-9}
3×10^{-6}	3×10^{16}	10^6	6.0	.3455	2.7×10^{-5}	1.36×10^{-2}	7.2×10^{-9}
4×10^{-6}	4×10^{16}	1.33×10^6	6.124	.3525	6.4	3.22×10^{-2}	1.2×10^{-8}
5×10^{-6}	5×10^{16}	1.667×10^6	6.222	.3580	1.25×10^{-4}	.063	2×10^{-8}
6×10^{-6}	6×10^{16}	2×10^6	6.303	.363	2.16	.1087	2.88×10^{-8}
7	7	2.33	6.367	.367	3.43	.173	3.92
.8	8	2.66	6.425	.370.	5.12	.258	5.12
9×10^{-6}	9	3.0	6.476	.372	7.29	.367	6.48
9.5	9.5	3.166.	6.5	.374	8.5	.428	7.2
1.2					1.72×10^{-3}	.866	11.5
1.5					3.7	1.86	18.0
2.0					8	4.03	32.

Same Calculation for Step-Jun.



$\cancel{V}$ $\mathcal{E}_{f_1} - \mathcal{E}_{f_2} = .0576 \log_{10} \frac{10^{20} \times 10^{17}}{9 \times 10^{20}}$

$= .0576 \log_{10} 1.11 \times 10^{17} = .0576 \times 17.04$

.982 Volts.

$V = \frac{q N_d w^2}{2\varepsilon}$

$\nabla^2 v = q N_d / \varepsilon$

$\nabla v = \frac{q N_d a}{\varepsilon}$

$v = \frac{q N_d w^2}{2}$

$= \frac{1.6 \times 10^{-19} \times 10^{17} w^2}{2 \times 1.06 \times 10^{-12}} =$

$= 7.55 \times 10^{9} w^2 \text{(cm)} = 75.5\, w^2 \ (\mu)$

$Q = 1.6 \times 10^{-19} \times 10^{17} w \text{(cm)} = 1.6 \times 10^{-6} w \ (\mu)$

w	w^2	V	Q
.1 μ			
.01 μ	.0001	.0075	1.6×10^{-8}
.02	.0004	.0302	3.2×10^{-8}
.03	.0009	.0680	4.8
.04	.0016	.121	6.4
.05	.0025	.188	8.0
.06	.0036	.272	9.6
.07	.0049	.370	
.08	.0064	.476	
.09	.0081	.612	
.1	.01	.755	1.6×10^{-7}
.11	.0121	.913	1.76×10^{-7}
.115	.0132	.996	1.84
.12	.0144	1.09	1.92
.13	.0169	1.23	2.08
.14	.0196	1.48	2.24
.15	.0225	1.7	2.40
.17	.0289	2.18	2.72
.2	.04	3.02	3.2
.25	.0625	4.72	4.
.28 .28	.078	5.9	4.48
.3	.09	6.8	4.8

.988

Graphs Qspchg vs I fwd
" vs V reverse.

Graded Jcn: at zero Ext bias .373 x 2 = .746 volts.

Vtotal	Vapplied	Qtotal	Q-Q(0)
	-.746		-6.60
.836	.09	7.2	$.6 \times 10^{-8}$
1.776	1.03	11.5	4.9
3.72	2.98	18.0	11.4
8.06	7.6	32.	25.4

Step Jcn at zero bias. V = .982V Q = 18.25

Vtot	Vapp.		
1.7	.72	24	5.75
3.02	2.04	32	13.75
4.72	3.74	40	31.75
5.9	4.92	~~44~~ 48	~~18.5~~
6.8	5.82	48	39.75

$V_{app} = .0576 \log_{10} J/J_o$ $J_o = 4.7 \times 10^{-10}$
6.60×10^{-8}

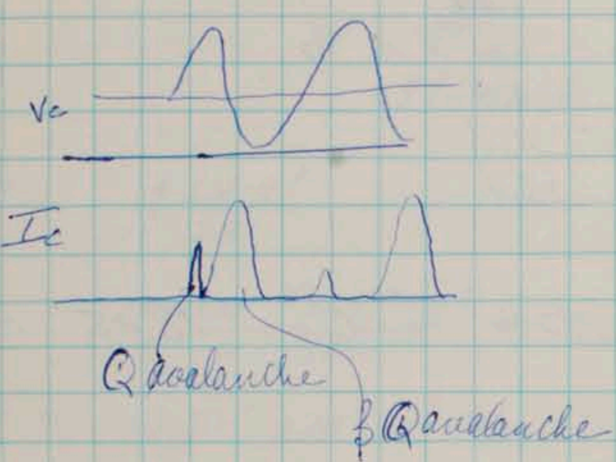
J	ln J/Jo	Vapp	Vapp/2	ΔV .373 - Vapp	Q(ΔV)	-Q(0)	.982-Vapp	Q(V)	18.25-QV
.1	8.326	.48	.24	.133	3.3	3.3	.502	13.1	5.15
.316	8.826	.508	.254	.119	3.05	3.55	.474	12.7	5.55
1	9.326	.537	.268	.105	2.8	3.8	445	12.3	595
3.16	9.826	.566	.283	.090	2.6	4.0	416	11.9	635
10	10.326	.585	.292	.081	2.4	4.2	397	11.6	665
31.6	10.826	.613	.306	.067	2.1	4.5	369	11.15	710
100	11.326	.642	.321	.052	1.8	4.8	340	10.75	750
316	11.826	.67	.335	.038	1.4	5.2	312	10.3	795
1000	12.326	.698	.349	.024	1.0	5.6	284	9.8	845

I	Q Trans = 10^{-10}	Trans = 3×10^{-10}
10	10^{-9}	3×10^{-9}
100	10^{-8}	3×10^{-8}
1000	10^{-7}	$3 \times 10^{-}$

May 5, 1958.

Tetrode Transistor. - Infinite base resistance.

Transistor oscillator - 2 terminals.



For δ fcn I_E, I_c = gaussian centered about transit time later, spread of

Assuming uniform field, $T_{trans} = \frac{w}{\mu E}$

Spread = $\sqrt{D T_{trans}}$.

May 9-58.

Possible HF Transistors.

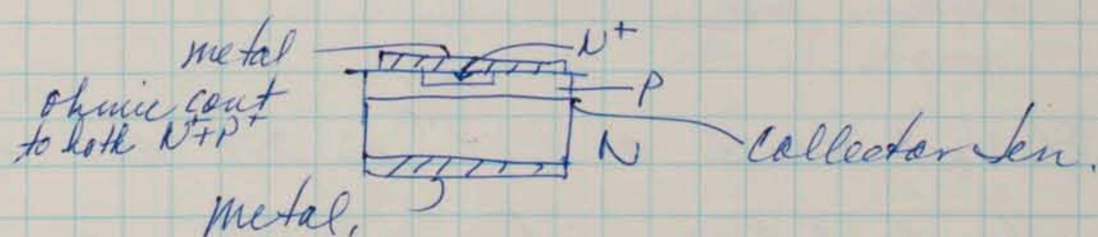
Problem in HF oscillator transistors is to make base lead contacts. We know how to make thin layers, i.e. by diffusion, and we can think in terms of layers a fraction of a micron thick, with transit times of the order of 10^{-11} sec. However, to make good transistor use of these thin base layers, the lateral dimension of the base, l, should be, say, only 10× the base width.

We might avoid this problem by thinking of
1) circuits not requiring external base leads, biased by avalanche at the collector. The avalanche current (average) need be only $1/\beta$ of the average collector current. Base biasing could then be done by collector current source, without serious degradation of performance, i.e. since the avalanche current flowing during the peak of the collector cycle need be only a small fraction of the total current.

2. Transit time diodes
   a. Minority carrier diffusion delay diode.
   b. Avalanche delay diode.

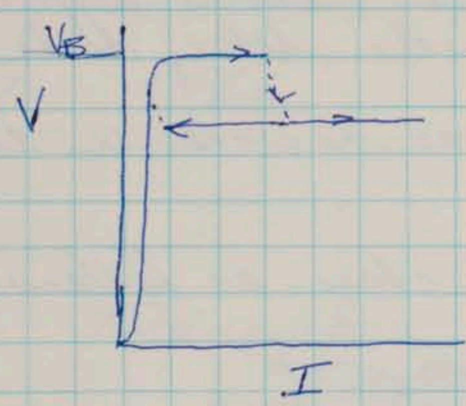
3. Another negative resistance diode is the following:

Assume a structure as follows:



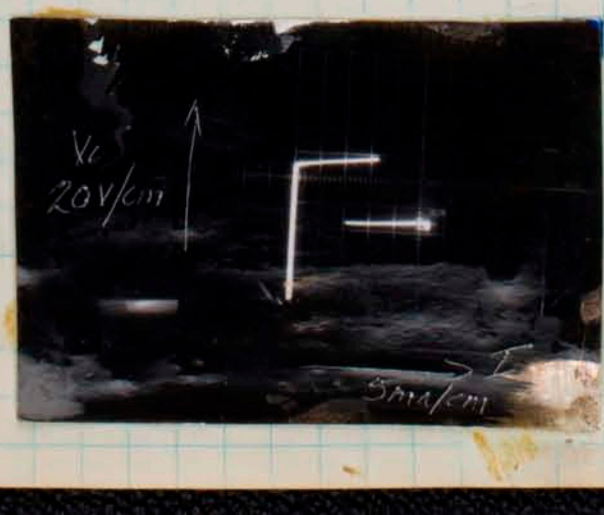
This structure has a negative resistance by virtue of the following argument.

At low voltages across the collector junction, a small current of holes flows into the base by virtue of avalanche, but these holes flow out to the top ohmic contact, without biasing the base under the emitter high enough that ~~holes~~ Electrons flow out of the emitter across the base. At higher voltages, the holes injected into the base will ~~not be~~ create an IR drop in the layer under the emitter, forward biasing the emitter, causing current to flow. These electrons after crossing the base, cause [illegible] avalanche ~~to~~ more holes to flow into this region of the base. This high current condition can then be maintained at even lower collector ~~currents~~ voltages. Thus the I-V characteristic looks like this:



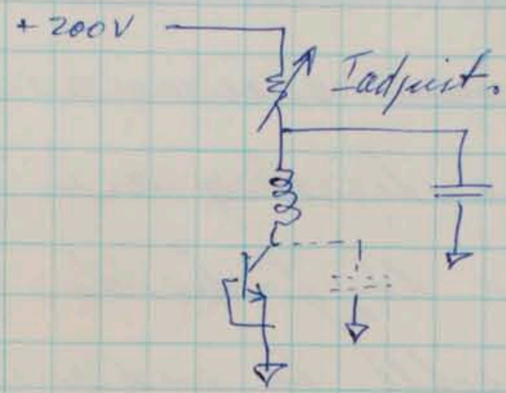
Ratios of V_B to V_{hold} as high as 2:1 are obtained on our standard transistors, shorting Emitter and base leads.

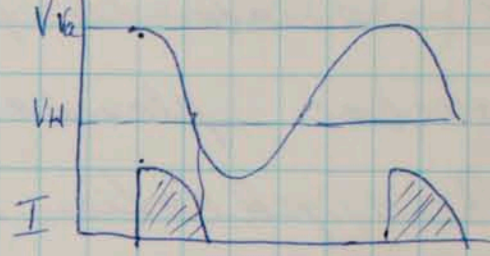
The photo at right is an IV plot of our NPN Transistor, Emitter shorted to base.



Since separate Emitter and base connection are not needed for this device the effective base ~~width~~ dimension l could be substantially reduced.

Oscillator using this device:





Neg. Resist should hold up to about f_{max}, which we should be able to get up above 1000 Mcps

for $W_b = 1\mu$, $l_b = 10\mu$ $\rho_{s_b} = 1000\ \Omega/\square$ $W_{spchg} = 1\mu$.

$$r_b C_c = \varepsilon \frac{1cm \times .01}{d\ .001} \times \frac{.01}{1} \times 1000 \qquad \varepsilon = 1.06 \times 10^{-12}\ f/cm$$

$$= 10^{-11} \times 10$$

$$= 10^{-10}\ sec$$

$$\tau_{trans} = \underline{\sim 10^{-10}\ sec.}$$

f should be up to 1000 mc

Read and understood
Jean A. Hoerni

May 14 '58.

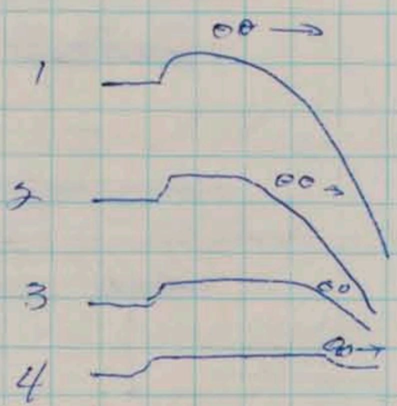
Difficulty with W T Read's negative resistance diode is that the avalanche does not depend solely on the instantaneous field - but rather the avalanche process occurs as a series of micro - plasmas, extending a finite time after the application of a high field.

It may be possible to achieve negative resistance without resorting to this, however, if the current flow can be made to extend over a longer portion of the cycle.

Consider the following: An N^+PN^+ structure, with total number of impurities small enough in the p region that punch through can occur.

Equilibrium 

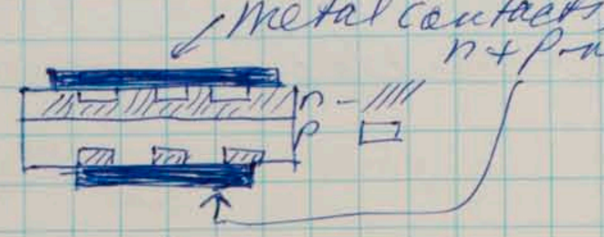
As bias is applied to Collector, Sp chg region widens into the base, with a net decrease in the positive charge in the base, either by injection of electrons or by driving out holes. By proper doping ratios, we should be able to make this primarily hole current. Then, as punch-through occurs, electrons are allowed to flow into the base - the number of electrons in the base building up as long as the voltage is above punch-through voltage. - This number is limited by space charge limitations. These electrons flow to the collector under a high field and remain in a high field region even as the collector voltage drops:-



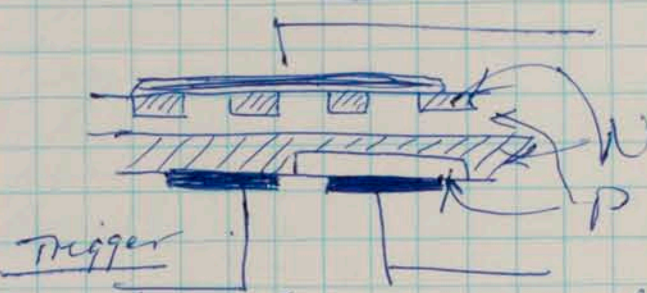
Thus, it may be possible to make a negative resistance device in which the negative resistance holds up for quite reasonable voltage swings on the collector - this may be a good one to look for.

May 14 The technique propounded on 35 + 36 might be useful in the case of the PNPN transistor as well as for an npn or pnp. The alpha of the transistor is effectively made very ~~short~~ low for low currents - this switching current is then increased and actually is controlled then by the geometry of the emitter and base regions. This then is a way to design for switching currents. It also makes the device faster, since we effectively have another way for the stored ~~holes~~ minority carriers to get out of the base:

Two terminal:

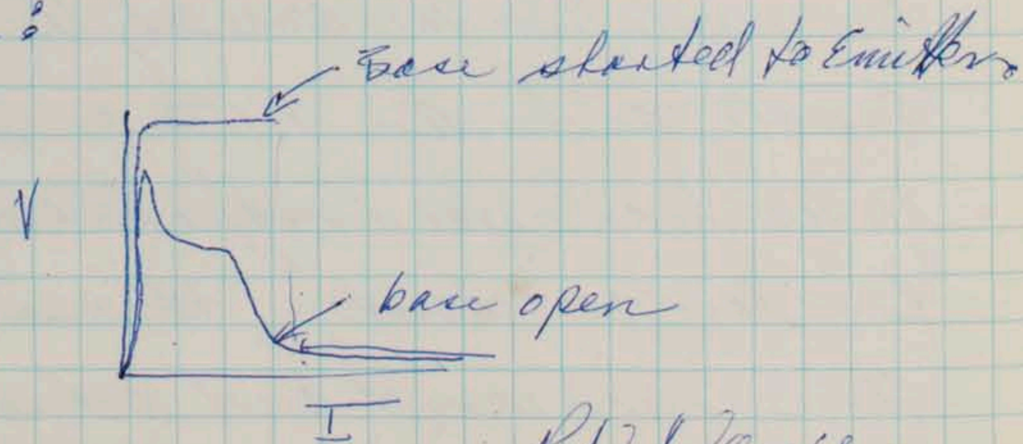


Three terminal:



In the above 3 term. unit, the npn should be the high α transistor,

This also has the advantage of making the switching voltages of the transistors more stable: for low sw. currents it is quite surface sensitive, and also has the "spike" as the alpha of one of the transistors (the npn usually) goes high:



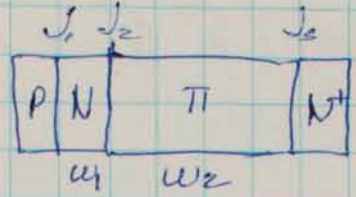
Discussed this with J A Hoerni + G E Moore

Jean A. Hoerni

R N Noyce
May 14 '58

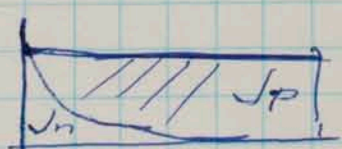
PNPN - Conductivity modulated.

Let us consider the following structure:



Here we assume that the diffusion length of electrons injected across J_3 is much smaller than the base width w_2

As current is forced through this junction, it is made up primarily of electrons at the junction J_3; and of holes far from the junction - Considering only the base W_2 for the time being, let us determine how much of the current is made up of electrons at J_2. Consider first an infinite block.



Conditions: $J_n + J_p = J_{Total}$

$$J_n = q\mu_n\left(\frac{kT}{q}\,\text{grad}\, n + \vec{E}n\right)$$

$$J_p = q\mu_p\left(\frac{kT}{q}\,\text{grad} + Ep\right)$$

$$p = N_A + n \quad \text{(Electrostatic Neutrality)}$$

$$\text{div}\, J_n = \frac{n}{\tau} \quad \text{(constant lifetime)}$$

With boundary conditions:
$J_p = 0$ at $x = 0$

Solve for J_n vs x.

From above Eqns:

$$J_n = J_T - J_p$$

$$= J_T - \left[q\mu_p \left(\frac{kT}{q} \frac{dp}{dy} + pE \right) \right.$$

But $\frac{dp}{dy} = \frac{dn}{dy}$

$p = N_A + n$

$$J_n = J_T - q\mu_p \left[\frac{kT}{q} \frac{dn}{dy} + (N_a + n) E \right]$$

also $$J_n = q\mu_n \left[-\frac{kT}{q} \frac{dn}{dy} + nE \right]$$

Solve for E

$$E = \frac{1}{q\mu_p} \left[J_T - J_n - q\mu_p \frac{kT}{q} \frac{dn}{dy} \right] (N_a + n)^{-1}$$

Subs. in above.

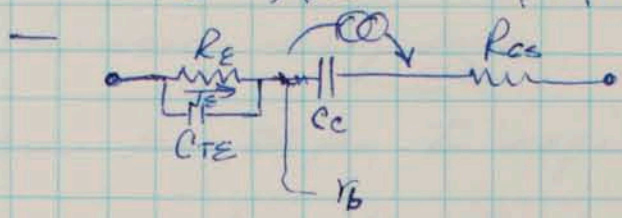
$$J_n = -qD_n \frac{dn}{dy} + \frac{\mu_n}{\mu_p} \frac{n}{N_a + n} \left[J_T - J_n - qD_p \frac{dn}{dy} \right]$$

$$J_n \left[1 + \frac{\mu_n}{\mu_p} \frac{n}{N_a + n} \right] = -qD_n \frac{dn}{dy} \left(\frac{N_a + 2n}{N_a + n} \right) + \frac{\mu_n}{\mu_p} \frac{n}{N_a + n} J_T$$

Transit Time diode.

Effects of R_c', C_{TE}

$J(P,S_2)=\beta J_E$ $\beta = |\beta| e^{-i\omega\tau}$



$$J = J(P,S_2) + J(D,S_2)$$

Extra Effects to consider:

1. Series base + Emitter resistance.
2. Currents through base, carried by majority carriers.
3. Transition capacities (primarily Emitter.)
4. Injection at emitter at high frequencies.
5. Diffusion delay through Em. sp. chg. regions

R_{cs} must be small compared to $\frac{1}{\omega C_c}$

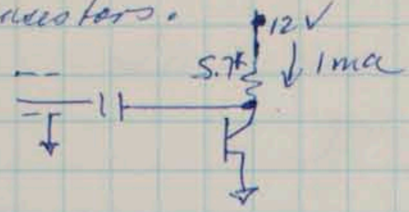
Our structure at 10^9, $R_{cs} \sim 10\,\Omega$, $\frac{1}{\omega C_c} = \frac{1}{2\pi 10^{-9} \times 10^{+10}} = 1\,\Omega$, so we can't make it 6

We must reduce R_{cs}.

Another way of thinking of this device:

As collector bias is changed, in npn, holes are driven from collector sp. chg region to Emitter region, allowing electrons to come in from emitter to neutralize the charge. These drift to collector, arriving later.

Philco Transistors.



#1					#2	
f		G	B			
76		1.4	4.0			
100		1.8	5.3			
150	(1ma)	2.1	8.5			
	(2ma)	3.3	8.3			
	($\frac{1}{2}$ma)	1.6	8.8			
	.2	1.0	8.8			
	.2ma	.7	10	Stub		
	1ma	1.8	9.6		1.5	9.3
200		2.8	13.7			
250		6.0	20			
300		13.6	30.4		12	30

Intrinsic Barrier Transistor design:

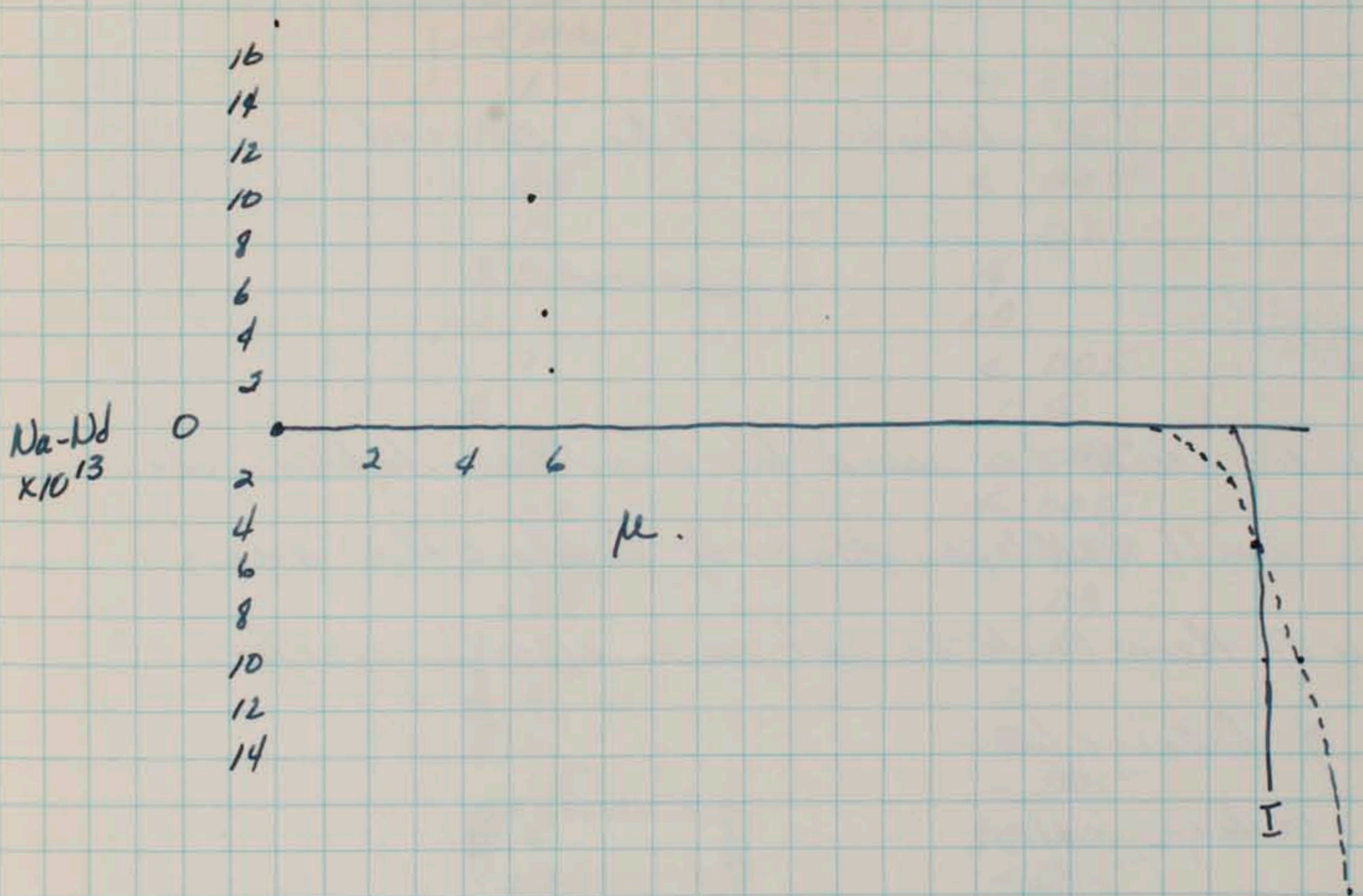
Question: advantage of this structure for having better intrinsic regions

Design for 20μ I region (at 5×10^{15}).

Design I. Collector thickness = 5μ.

Design II Collector thickness = 30μ.

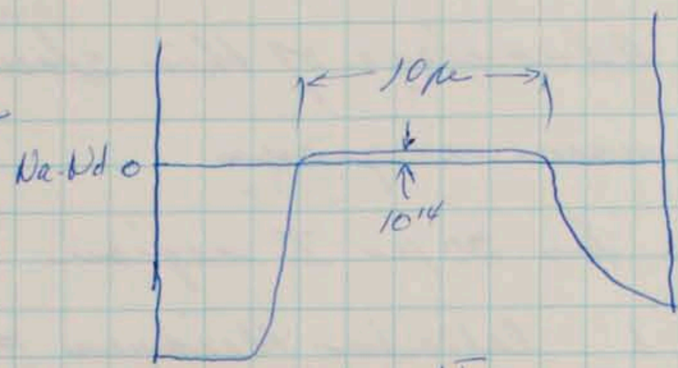
Base:	Collector.	
	I	II
$C_0 = 5\times10^{18}$	$C_0 = 10^{20}$	$C_0 = 10^{20}$
$L_0 = .91\mu$.	$L_0 = 5/7.2 = .695$	$L_d = 30/7.2 = 4.17$



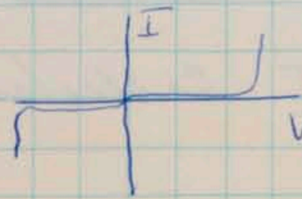
July 1 '58

Punch through diode. - disclosure

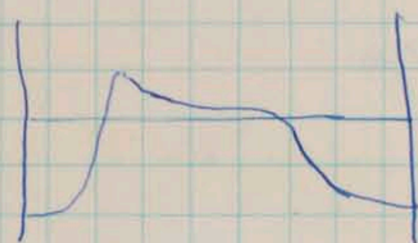
For this structure



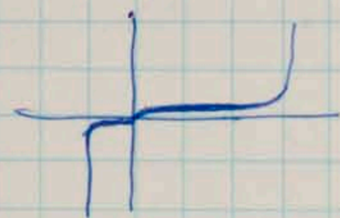
The I-V characteristic will be:



If the density in the center is skewed:



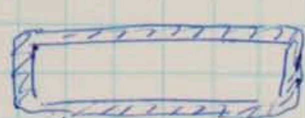
The I-V characteristic will be skewed.



Such diodes could be used for function tables, since each one will be independent of every other one, so many of them could be put on a single wafer.

Method of fabrication:

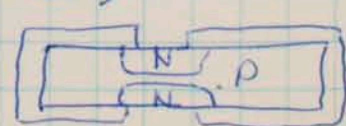
1 oxidize wafer



2 Etch holes in oxide

3. Etch Silicon to thickness (optional)

4 diffuse opposite cond. type



5 Evaporate contact array.

July 3.

C.S.Roberts has observed that under some conditions, at least, the aluminum tends to separate (upon alloying) at the Emitter-base junction. Electrically, the contacts are not well separated, but by etching about 10 seconds in 20 HNO_3 : 1 HF, they may be separated, without increasing the sheet resistance of the Aluminum alloyed layer.

	After 1st Etch (5 sec. 20:1). Current at 0.5 V (ma.)	After 2nd Etch. Same. Reverse Current at 5.0 V	forward Current at 2V Amps.
#1.	.1	< .005	.325
#2	1.0	.15	.35
Etc.	.05	< .005	.425
	.1	.02	.35
	5.0.	4.	.32
	12	60.	.40
	.1	<.005	.43
	4	1.5	.40
	.4	<.005	.25
	.12	<.005	.30
	.22	<.005	.35
	.45	.03	.40
	3.7	.1	.35
	3.5	1.	.40
	8.5	7.	.40
	.15	<.005	.50
	3.5	30.	.50
	.09	<.005	.50
	.27	<.005	.45
	.55	2.0	.45
	2.5	.5	.4
	3.5	.2	.15
	.25	<.005	.4
	1.5	<.005	.4
	.02	<.005	.4
	.45	<.005	.3

This data shows that about half of the Emitter-base junctions have cleared up sufficiently to be usable. This has been done with no sacrifice in the forward resistance. In fact, the forward diode impedances show a significant improvement over those now coming off the line of about 10 Ω, these being about 3 Ω.

The photograph at right shows the separation between Emitter on left and base on right. Separation is about 10 μ.

500x

A finer grain structure on the base is desirable if very small structures are to be made. Emitter is fine grained enough.

July 15, 1958.

Parametric Amplifier Diodes.

The figure of merit of the diode for parametric amplification is the crossover frequency: i.e the frequency at which $X_c = R_s$. (series Resistance).

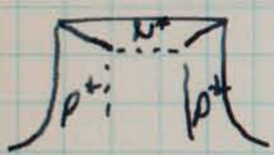
In general, the capacitance varies as $\frac{1}{\sqrt{\rho}}$ and the series resistance varies as ρ, the resistivity as long as the mobility is constant. Therefore, the RC time constant τ varies as $\rho^{\frac{1}{2}}$. This means that this time constant should be reduced by going to higher and higher doping density.

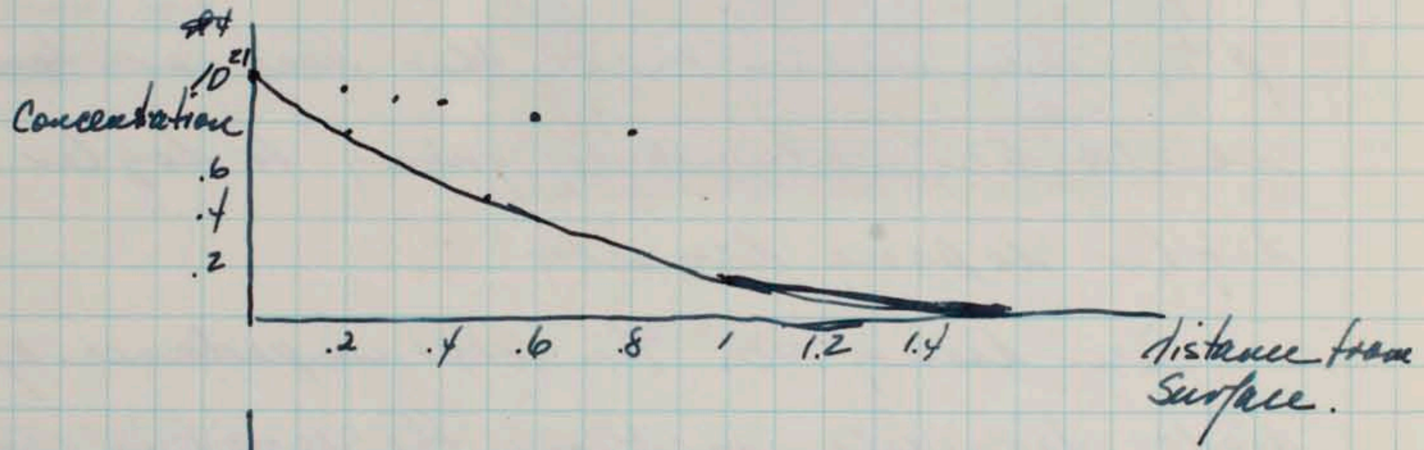
In doing so, the total impedance of the diode decreases, making the unit inconvenient for use. It would be more desirable either to

1. cut area so impedance is $\sim 50\ \Omega$ at operating frequency, say 1KMC.
2. Series a number of units to increase impedance level.

In order to cut impedance levels, we suggest making a linear structure rather than an area structure. i.e. use the capacitance between two surface-diffused areas, one n & one p. In this way, contacts can be made extremely close to the junction, and the capacitance per unit area will be quite high.

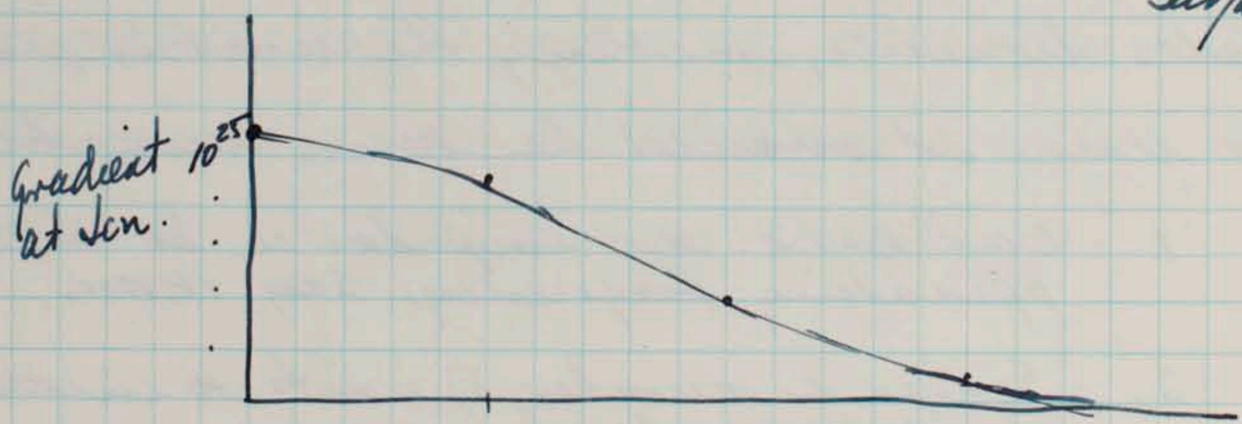
As an example let us look at the following structure: Using 50 Ω cm p type material, Diffuse Phosphorous at 10^{21} for $\frac{1}{2}\mu$. L_D. Remove phos. layer + diffuse Boron 10^{21} $\frac{1}{4}\mu$. We can estimate the capacitance per unit length of this structure:

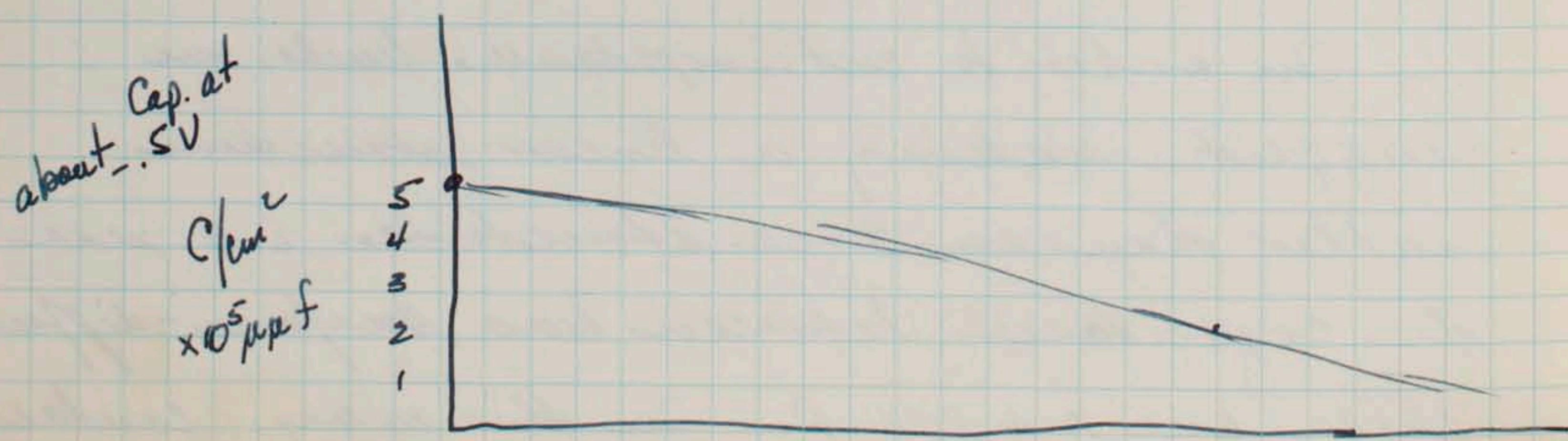




$\frac{5\times10^{-5}}{10^{21}}$

$\frac{dc}{dx} = 2\times10^{25}$ f.





Capacitance will be about 100 $\mu\mu f$ / cm

$\sim 5\times10^{5}\,\mu\mu f/cm^{2} \times 2\times10^{-4}\,cm = 100\,\mu\mu f/cm.$ (1 v). Total.

(make 5 mil dot) (.04 cm long)

Capacitance to 50-Ω cm material:

$C_B = 2.5\times10^{14}$ $\quad \frac{C_0}{C_B} = 4\times10^{6}$

7.2 LD. $\quad \frac{dc}{dv} = 2\times10^{25}\times10^{-6}$

$= 2\times10^{19}$

$C = 5\times10^{3}\,/cm^{2}$

$A = \underline{10^{-4}}\,\underline{cm^{2}}$ $\quad C_0 = .1\,\mu\mu f.$ OK.

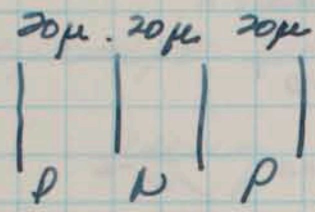
<u>5 mil dot</u>.

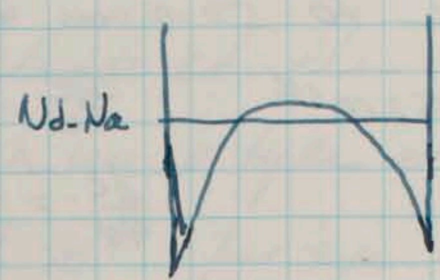
15 mil perimeter, 1 mil better. contacts.

$\frac{1}{15}$ square of 10 Ω/sq — <u>under 1 Ω</u>.

PNP Diodes.

.01 Ω cm N Type.





.01 Ωcm N → $\cancel{5}\times10^{18}$

$C_0 = \cancel{10^{21}}$ $\quad 2\times10^{20}$

$L_D = \cancel{4\mu}. \quad 5\mu.$

Gradient at Jcn ~~5 L_D~~. 4 L_D.

$$\frac{dc}{dx} = 10^{-2}\,\frac{C_0}{4\mu} = \frac{2\times10^{20}}{4\times10^{-4}}\times10^{-2} = 5\times10^{21}$$

C at ~~o~~ −.5 V $\quad 4\times10^{4}$ pf/cm^2

For 10^{-3} cm^2 $\quad C = 40$ pf, $\quad R = .02\,\Omega$

$$RC = .02\times40\times10^{-12} = 10^{12}$$

f cross. = 1.6×10^{11} cycles

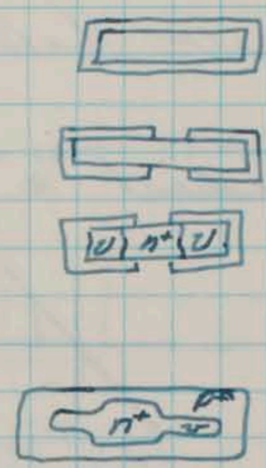
= 160~~0~~ KMC.

Parametric Amplifier Diode Configurations.

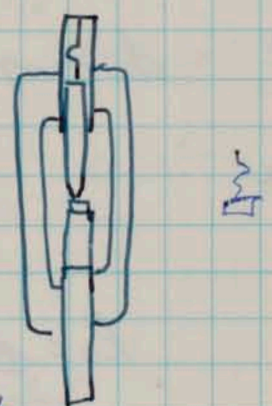
In order to get small effective area:

Symmetrical Structure:

1. Oxidize.
2. Photo etch
3. Diff n^+
4. Remove oxide
5. Diffuse p^+
6. Dice.



Package:



Skin depth: $\delta = \left(\frac{\omega\mu\sigma}{2}\right)^{-1/2}$ $\mu = 4\pi \times 10^{-8}$

σ gold .008 $\Omega/\square$ 1KMC

Cu skindepth 1 mil wire 3×10^{-5} diam.
10^{-2} cm circ

1KMC . .0002 cm .3 long
2μ

.2 Ω 10 mil .02 Ω

Inductance

1" of 5 mil 30 mμh.

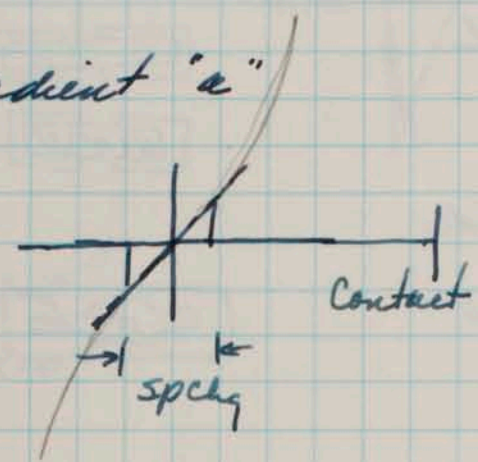
$L = .00508\,\underset{(in)}{l}\left(\ln\frac{4l}{d} - 1\right)\ \mu h.$

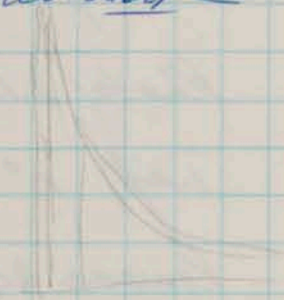
$n\pi n$ - npn Diode.

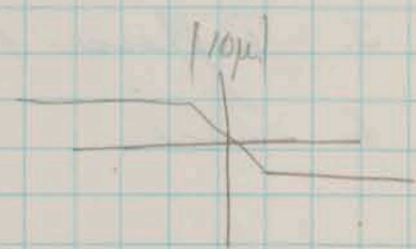
1. 50 Ω cm p-type.

July 23. Resistance through graded diode

1. Assume gradient "a"
2. mobility const.







$$\int R\,dx = \int \frac{1}{ax\,e\mu}\,dx$$

$$= \frac{1}{ae\mu} \ln \frac{x}{x_0} \quad \text{diverges to } \infty$$

Try exponential.

$$\rho = \rho_0\, e^{-ax}$$

$$R = a\,\rho_0 \qquad \rho_0 = \text{resist at Edge of sp. chg region.}$$

Linear: 10μ. then const. $a = 10^{23}$

C.	V	$X_{sp.}$	n edge.	$\rho_0\,\rho$	1 cm², .1μ thick. ρRC:
2.5×10^5 μμf	.1V	4×10^{-6}	2×10^{17}	.17 Ω cm	.46 Ω μμf = μμsec.
1.2×10^5	1V.	9×10^{-6}	4.5×10^{17}	.08	.1
	2V	1.2×10^{-5}	6×10^{17}	.06.	
	5V	1.6^{-5}	8×10^{17}	.05	
$.55\times10^5$	10V	2.0^{-5}	10^{18}	.04	.02

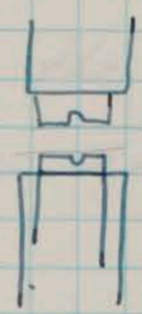
for 1 $\mu\mu f$ at gradient of 10^{23}, 1 v,

$A = 10^{-5}$ cm^2

radius = 3×10^{-3} ~ .001"

Series R. allowable for 160 kmc = 1 Ω

Pedestal mount:



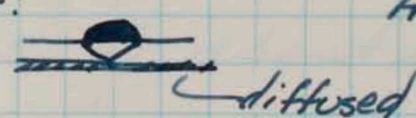
Area of contact for 1 $\mu\mu f$: .001 separation:

$C = \frac{\varepsilon A}{d} = \cancel{.885} \times 10^{-12}$ $.09 \frac{A\,(cm^2)}{d\,(cm)}$ $\mu\mu f$

$A = .02$ cm^2

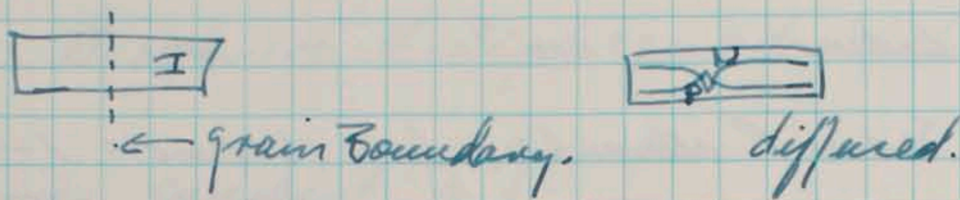
($\frac{1}{2}$ mil spacing) $d = .001$ cm $C = .2$

Use 111 xtal, alloy dot: Au Sb. perhaps.



110 direction lines
100 4 sided pits.

Another possibility is the use of grain boundary for small area high gradient diode



High Efficiency Photovoltaic Cell.

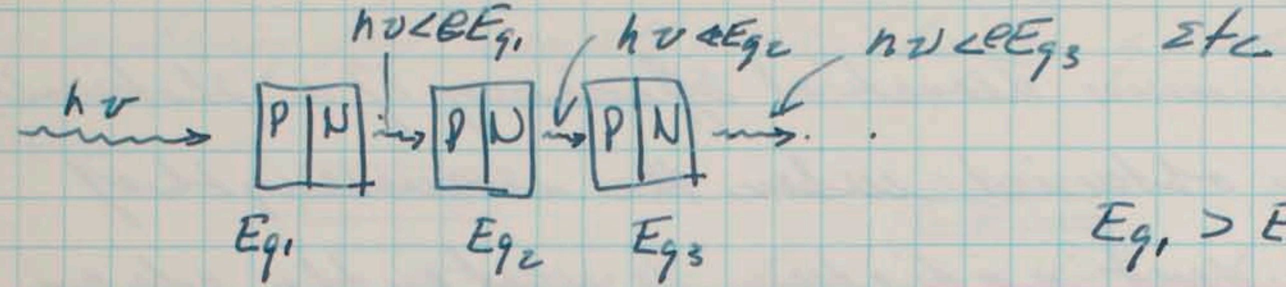
Maximum theoretical efficiency of a photovoltaic cell is obtained when the wavelength of the incident radiation is just on the edge of the intrinsic absorption of the semiconductor. At best only the band-gap energy can be used of the energy of the incident photon.

For a single semiconducting material PN Junction the efficiency is limited by

1. No absorption to produce hole-electron pairs from long-wavelength incident radiation.
2. Inefficient use of short wavelength radiation.

In principle, a higher efficiency converter could be made by utilizing slabs of P-N junctions of differing band gaps stacked in such a way to first use the high energy photons to create pairs in a high gap-material, then the lower energy photons, etc.

Schematically this is as follows.

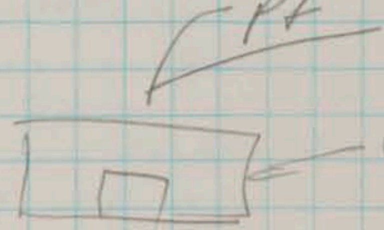


$E_{g_1} > E_{g_2} > E_{g_3}$ etc

Then, since every ~~detector~~ converter is working on a narrower band of energies closer to theoretical efficiencies could be obtained. This may not be practical as long as cells are expensive to fabricate, and materials are expensive. However, If this principle can be used in a single junction detector, or in a multiple junction detector ~~of~~ in a single slab, it may be practical.

One way in which this could be effected in practice would be to grade the energy gap across the single P-N Junction. In this case, If light is incident from the high gap side, the photons will be absorbed at the energy gap energy. Thus they have no excess energy to be lost to lattice vibrations.

Such a cell will respond both to radiation absorbed on the high gap side and the low gap side of the junction. We can show that it will use the high energy radiation more efficiently than the low gap homogenous junction.



Ceramic Boat (covered

$\underline{1300°}$

Sb oxide
not under control

$\underline{\text{50-50 Silica} - B_2O_3}$

<u>Base</u>

<u>Highly pure Alumina</u>

<u>Hydrogen</u>   <u>very dry</u>

<u>2039</u>   <u>2036</u>

Possibility of PIN Diode Varactor. for low loss.

Advantages:

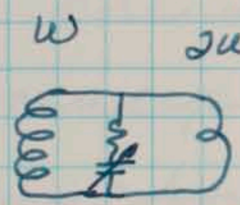
1. Higher impedance for a given Area.
2. Higher Q.

Question: Figure of Merit for Diode Varactor.

A. Energy loss / cycle.

B. Amount of Nonlinearity.

$$M \stackrel{?}{=} \frac{\text{Energy Converted / cycle}}{\text{Energy loss / cycle}}$$



Exp. Run for 3 term neg R.

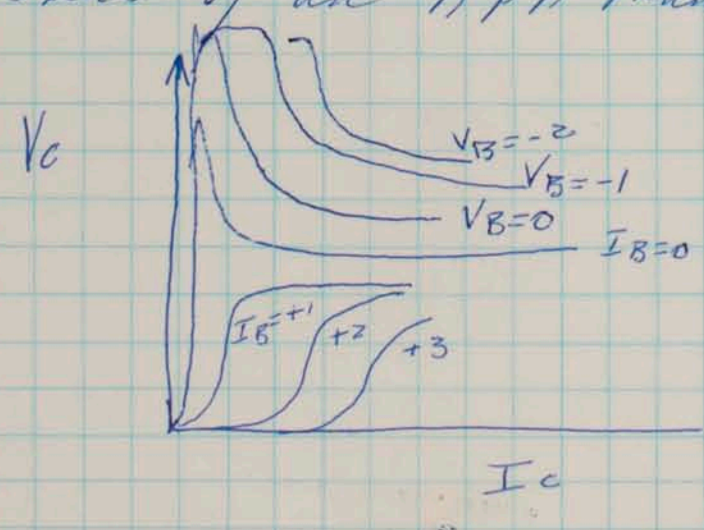
Trans. Char.

Bias	C
0 V	4.7
1	3.1
2	2.5
3	2.0
5	1.68
7	1.25
10	.93
15	.9
20	.88
30	.84
40	.82

Semiconductor Scanning device. January 12 '59.

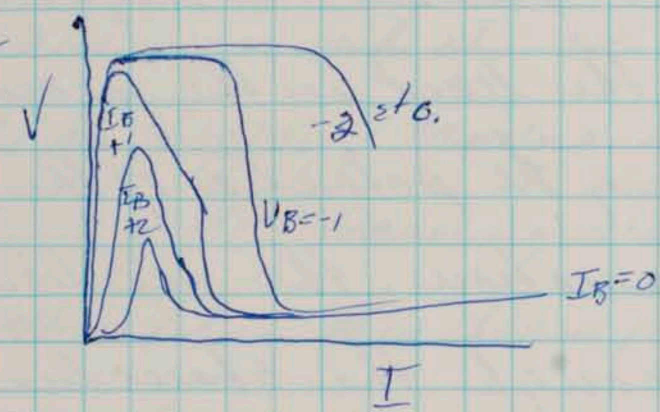
It is the object of this invention to provide a semiconductor device in which the spatial position of the conduction path from one surface to the other may be controlled by the application of proper positioning voltages applied to deflection electrodes. This device could then serve in many of the same applications in which an electron beam devices is used, such as display, camera tubes, beam switching, amplifiers of the traveling wave variety, Etc. For these applications, this beam positioning device might be used in conjunction with photo-conductors, or electroluminescent materials.

To see how the beam-forming part of the device works, let us consider the terminal characteristics of an npn transistor appear:



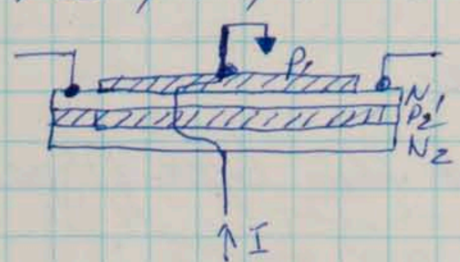
With the base voltage fixed, ~~and with~~ the collector has, over a portion of its characteristic, a negative resistance. However, as the base is biased further in the negative sense (base-emitter junction reversed biased), more collector voltage is required for the same current flow. Thus, if there is a potential gradient in the base layer, the current will tend to flow in the region where the base is biased the least in the reverse direction. Thus, by varying the potential of the base layer, and its spatial variation, the position of the current path through the structure can be varied. Furthermore, if the base is reverse biased at the edges, ~~the current,~~ but forward biased at one point by avalanche current flowing out through the base, the current path will be limited to a very small area.

Jan 14, 1959 ~~It~~ is essential to this type of operation that there ~~to~~ be a regenerative mechanism for the current flow, so that even though the potentials applied to the control electrodes are in the sense to bias the current off, it will continue to flow through the device. The avalanche multiplication which causes the negative resistance region illustrated above has this property. ~~thus~~ Another structure which may be more favorable is the PNPN structure. In this case, the I-V characteristics are similar, but the voltage across the device in the high current state are smaller:



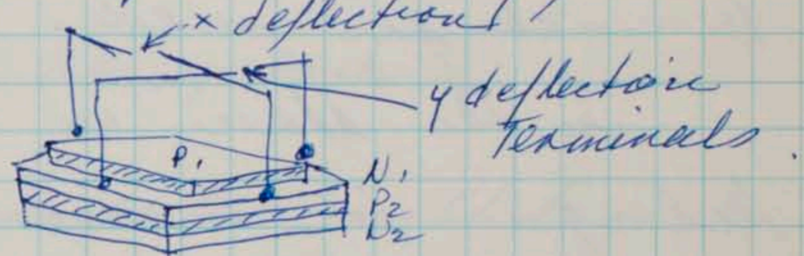
Again, the device does not conduct as readily if the base is reversed biased.

The device ~~then~~ is made in the following way: We use the pnpn as an example:



If a current I is forced through the device, and the terminals on the N_1 layer are reverse biased with respect to the P_1 layer (the ~~discharge will~~ current path will be confined to a narrow region in the middle of the device, its position being centered when the voltages are equal, and moving to the left as the voltage on the right hand terminal is increased (more reverse bias). Thus, the position of the current path can be varied by applying differing voltages between the contacts on the N_1 layer.

It is apparent that the same thing can be done with more than ~~two~~ contacts on the N_1 layer, giving a two-dimensional positioning of the current path:



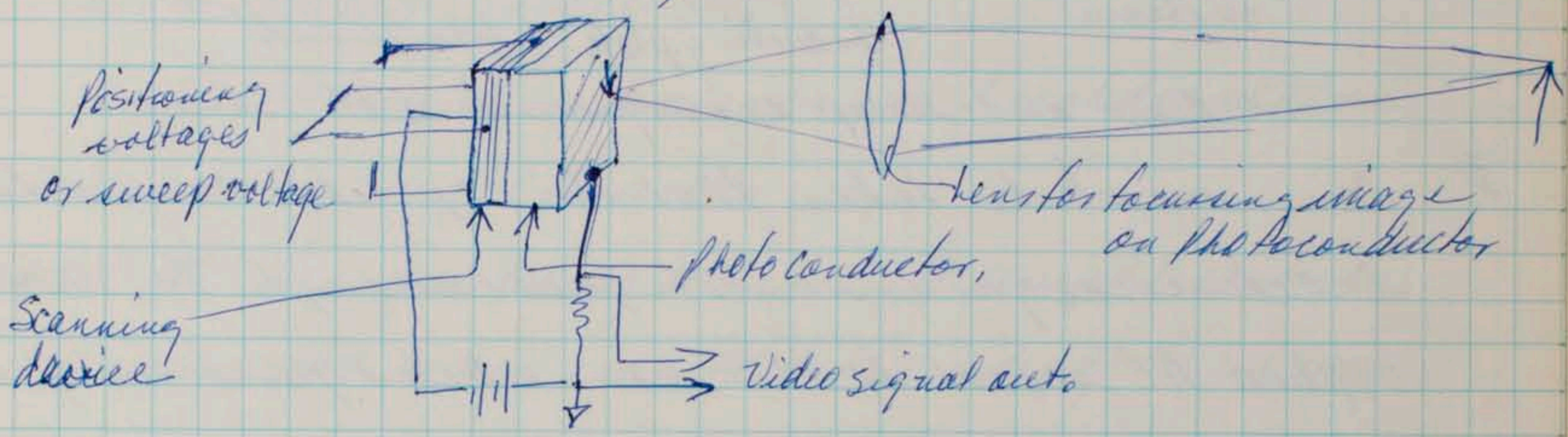
Since only the negative resistance characteristic is required, the same thing can be done with only an n p n structure or a p n p structure. In silicon, the npn structure is preferable, since the differences in the voltage where current starts to flow, and that at which the current is sustained is greater than in the case of the pnp structure.

In the P N P N structure, the device is symmetrical from the two sides, with a change in polarity. Thus, deflection terminals could be made on the middle n layer for, say, the x positioning of the beam, and on the middle y-layer, for y positioning of the beam. This method has an advantage in that the ~~x po~~ the x- and y- position of the beam ~~s~~ is more nearly a linear function of the deflection voltage than in the case where four deflection terminals are made to the same layer.

In the above, we have discussed the technique for 1) confining the current path between two sides of a structure to a small spot and 2) positioning this spot in any position by application of suitable potentials on deflection plates. Now we shall examine some possible applications for such a device.

1. Image pick-up device. ~~The~~ If we take the above disclosed beam positioning device, of either a three layer or four layer variety, in combination with a photoconductive film, the combination can be used to read the conductivity of the film as a function of position. Thus if a video

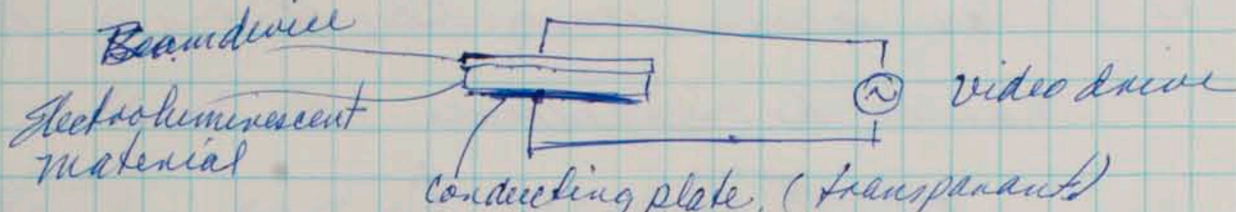
raster scan is applied to the deflection ~~plates~~ terminals, a video signal may be extracted from the device, either a voltage signal by using a constant current through it, or vice versa. In this use the device would be as follows.



Any of a number of photoconductors might be used. The use of the semiconductor body comprising the last layer of the scanning device is one possibility. The device is readily cooled for greater photosensitivity.

3 As an image forming or display device. In combination with some light-emitting material the above device can be used to display an image or any other type of information. There are several possibilities for the light emitting substances:

a. Electroluminescent materials. The above device provides a low impedance path from one surface to ~~[illegible]~~ the other in one chosen spot; elsewhere a high impedance. Thus, if used in the arrangement below, light will be emitted in the chosen spot, not elsewhere.



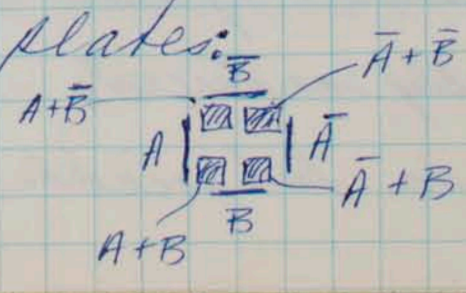
DC Bias and sweep arrangements not shown. Care must be taken that the capacity across the inactive regions is not great enough to short the applied AC signal to the non-selected portion of the electroluminescent material.

b. Some semiconductor materials emit light in the visible region with the passage of DC current, which eliminates the capacity problem referred to above. For instance, if a silicon PN junction has appreciable current flowing in reverse bias, visible light is emitted at the junction. Silicon absorbs visible radiation strongly, so the junction must be at or very near the surface if the light is to be seen. Semiconductor materials with wider energy band gaps, corresponding to energies greater than that of a photon of visible light will be transparent to visible light, and ~~he~~ may be more effective in this application. Silicon Carbide is one example in which visible light has been observed easily. In this case an extra PN junction, reverse biased in the breakdown region could be used; resulting in a PNPNP structure.

Light from a gas discharge, or breakdown of an insulator might be used.

Jan 15, 1959 3. As a switching device. If several contacts are made to one side or both sides of the device, a connection may be made between a selected pair by applying proper positioning potentials.

4. Since the position of the beam is a function of two variables, the deflection voltages; certain logic functions may be performed by proper electrode configuration. As an example: the function A or B, but not A and B would be given by an ~~electrode~~ configuration of 4 contact regions on the back, connected diagonally, with the signals A and B applied to the deflection plates:



This type of logic element can be carried much further by multiple connections for deflection electrodes, and multiple contacts on both front and back surfaces. It would appear that the resulting output voltages are suitable for direct coupling, so many of these elements are possible on one wafer.

January 23 '59

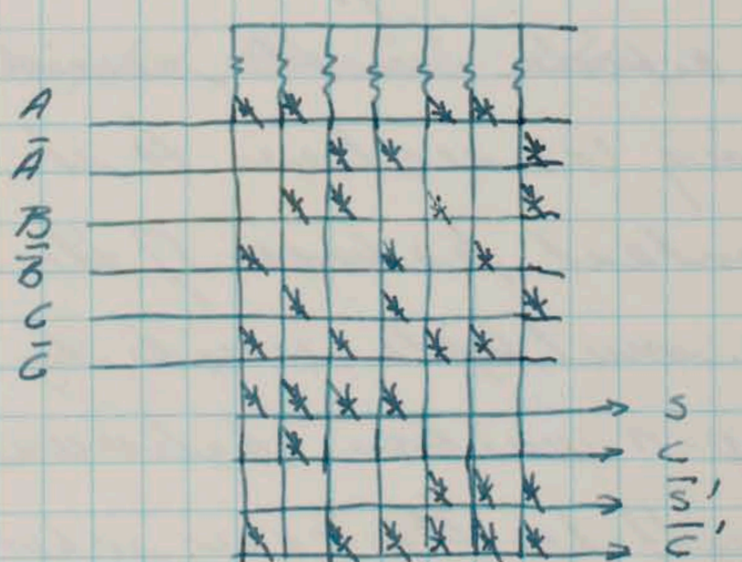
Methods of isolating multiple devices:

In many applications now it would be desirable to make multiple devices on a single piece of silicon in order to be able to make interconnections between devices as part of the manufacturing process, and thus reduce size, weight, etc., as well as cost per active element. Several considerations enter here: First, the blocks of devices which make up one unit should be large enough that the number of external leads is substantially reduced, realizing an economic advantage in fabrication costs. Secondly, either

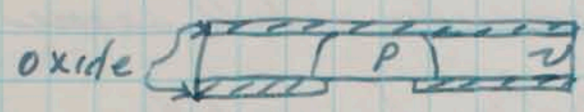
3/4/70

the number of elements must be small, or the yield very high in order that overall yield is high enough to be economic. Some steps may be taken here in transistor and logical design in order to make simple high yield elements. Still some compromise must undoubtedly be made. Third, the method of making interconnections, should fall naturally into the pattern of making the elements. Fourth, some method of surface protection must be utilized.

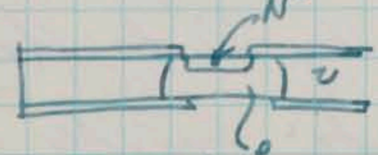
The following seems to meet most of these requirements: Suppose we want to make a diode matrix for a full adder:



We start with, say high resistivity n-type or ν material. Then after oxidizing, a P-type impurity is diffused through holes in the oxide, diffusing all the way through the wafer:



Then, after removing oxide on the top, an n-type impurity is diffused in:



Metal connections are made, by evaporating metal through the holes in the oxide, to interconnect the diodes as desired for a particular circuit.

Resistors might be made by either making two connections to one diffused island, or by coating the oxide with resistive material, and making connections to it.

The important features of the above are
1. Isolating multiple units by including at least ~~1~~ p-n junction between them. More common will be the case where 2 junctions are included between the elements, such that one is always reverse-biased, regardless

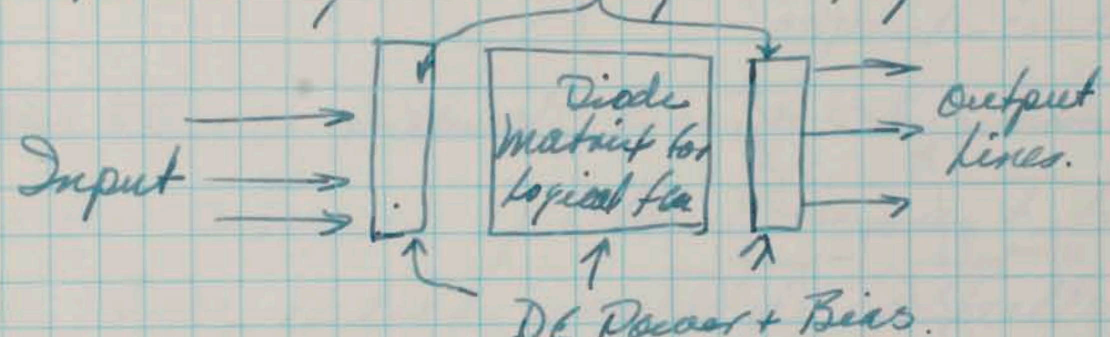
of the polarity of the voltage between the elements.

2. use of the SiO_2 layer as an insulator to isolate contact strips from the underlying silicon. ✓

3. Protection of junctions at the surface with an oxide layer.

The above is applicable to transistors as well as diodes.

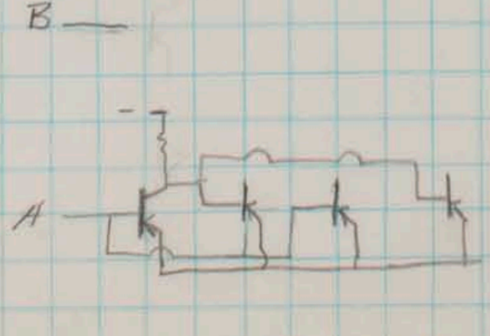
A generalized logic element might be the following:



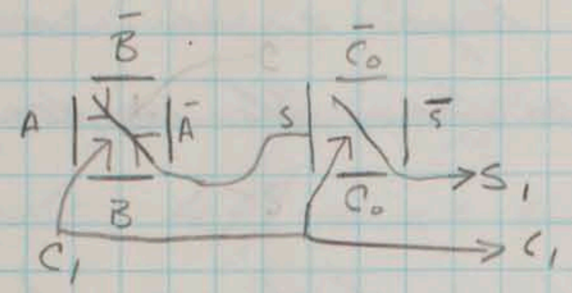
Direct coupled transistor adder: Richards p169

$S = A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}C + ABC$

$C = AB\bar{C} + A\bar{B}C + \bar{A}BC + ABC$

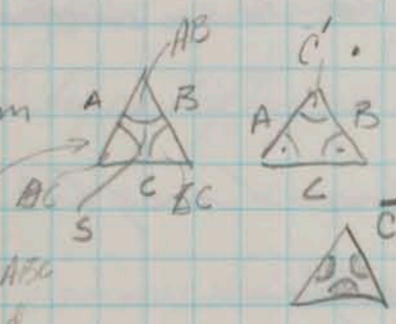


Full adder using Beam switching device:



One Beam device

1 Pulls Beam
0 Pushes "

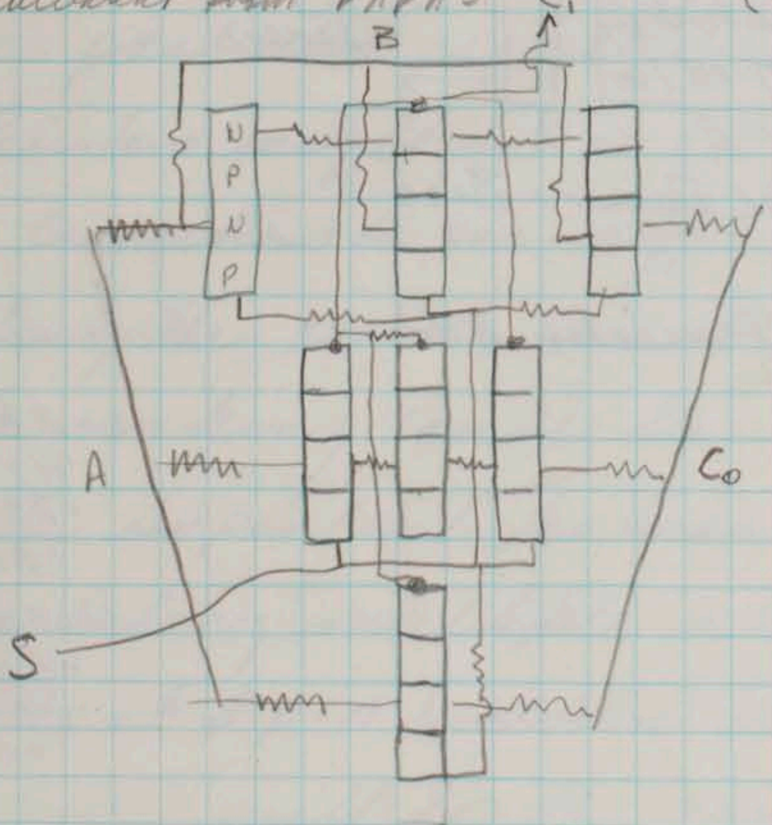


condition ABC looks bad

no carry for ABC

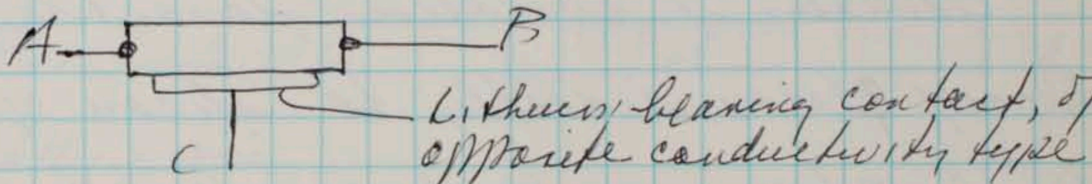
This looks OK

Equivalent from PNPN's $\bar{C_1}$ (could be npn's) (avalanche)



October 18, 1961

Today Gordon E Moore discussed with me the possibility of building a device to serve as a variable gain element in an adaptive system which the resistance of a semiconductor element could be changed by the diffusion or drift under a feild of a light impurity, or a fast moving impurity eg gold, lithium could change the carrier concentration in the element.



Thus the conductivity from $A \rightarrow B$ would depend on the integral of lithium current from C into the bar, which would be controlled electrically if diffusion in the field $C \rightarrow AB$ was rapid enough.

R N Noyce

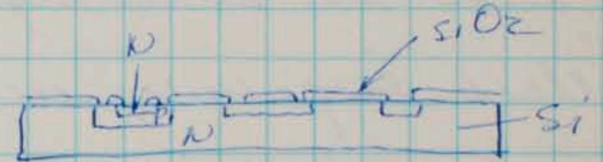
January 30, 1962

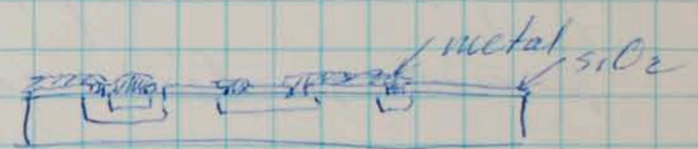
Last week Gordon E. Moore and I were discussing another method of device isolation which seems to have advantage. The disadvantage of isolation with P-N junctions is the extra capacitance across the PN junctions which causes extra time lags.

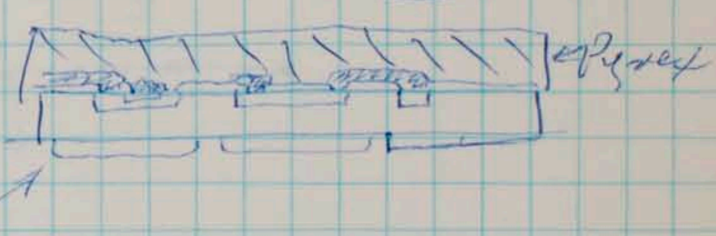
Recently it has been possible to bond Pyrex glass directly to Silicon using temperatures just above the softening point of Pyrex. This can be done with metallized wafers as well. After bonding to completed wafers of integrated circuitry, it is possible to etch away the Silicon to leave isolated regions of silicon containing the active devices. This would substantially reduce the capacitance compared to PN junction isolation.

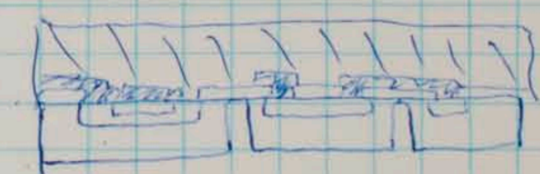
The steps of a proposed process are shown on the next page:

1. Silicon Wafer
↓
oxidize
↓
Etch holes
↓
diffuse resistors, diodes, Xtr bases
↓
oxidize
↓
Etch holes.
↓
diffuse Emitters, Etc,
↓
metallize over oxide for contacts, interconnections
↓
Seal glass over surface
↓
Mask back side
↓
Etch away silicon to isolate.









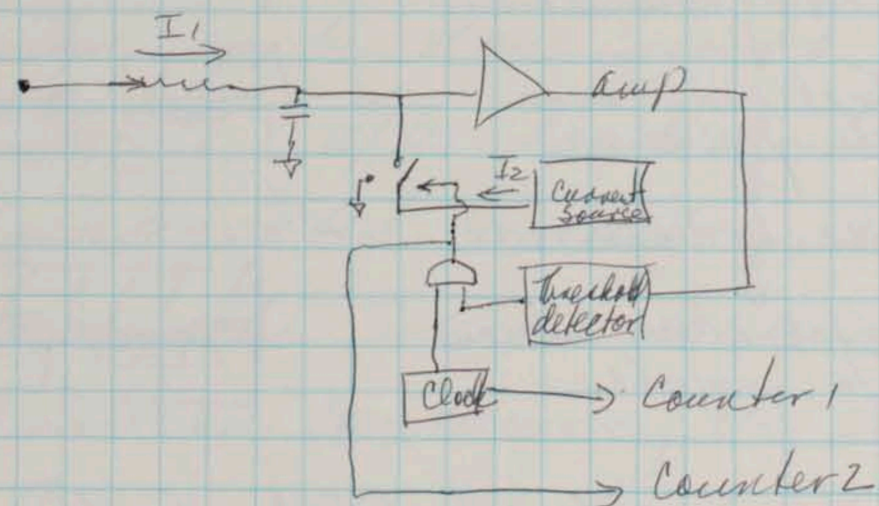
Leads could be attached by further etching through the SiO_2 film and contacting metal film from the bottom.

R N Noyce Jan 30, 1962

Read & Understood G. E. Moore 12/12/62. I also remember discussing this idea with RNN early this year.
GEM

September 30, 1962

Dave Hilpiker has developed a constant current source of accuracy of the order of .01%. Such devices, or any constant current source could be applied as a digital volt meter by measuring time ratios. This measurement could be done digitally. No highly accurate clock frequency would be required, but only stability of frequency over the count period, which could be a fraction of a second.



The ratio of counts in counter 1 + counter 2 would give the ratio of I_1 to I_2 if circuitry of gating element is arranged to leave the switch closed for one cycle.

Clock + counters could be made remote for multi element installations. These ideas, but with frequency stability limitations on the clock have been submitted yesterday by S. Schwartz. His application is voltage to frequency conversion. For the DVM, no such stability is needed.

October 17, 1962 — Adaptive Machines.

In examining methods that might be employed to use the insulated-gate field effect devices, I have been looking at the basic limitations, from a practical point of view, of the adaptive system. Ridgeway, and others have shown that the "Adaline" system does provide optimum convergence, and generalization properties. To realize this system, a large number of "weights" must be used, if the system is to have any potentiality, at all. In the systems built thus far, the total number of weights used has been limited to of the order of 100, resulting in an adaptive system of very little capability compared to what is desired.

The use of the Insulated gate FET (Frank Wanlass) as the analog weight certainly is possible. ~~However~~, The hope is that this device can be made in large numbers on a common substrate, with the interconnection wiring, including the wiring for "adapt" commands. The total number of elements for a system of great capability will, however be very large, and the amount of interconnection wiring will be very large.

Realizing this limitation, we may set these criteria:

1. The total memory must be <u>very</u> large.

2. The memory can be adapted: i.e. changed by the new experience + training.

3. Every memory element participates in every decision made, in the "adaline" system.

~~so that~~ 4. Because of the enormous memory, the present system, which connects through the memory, has an enormous amount of wiring. This is probably the final limitation.

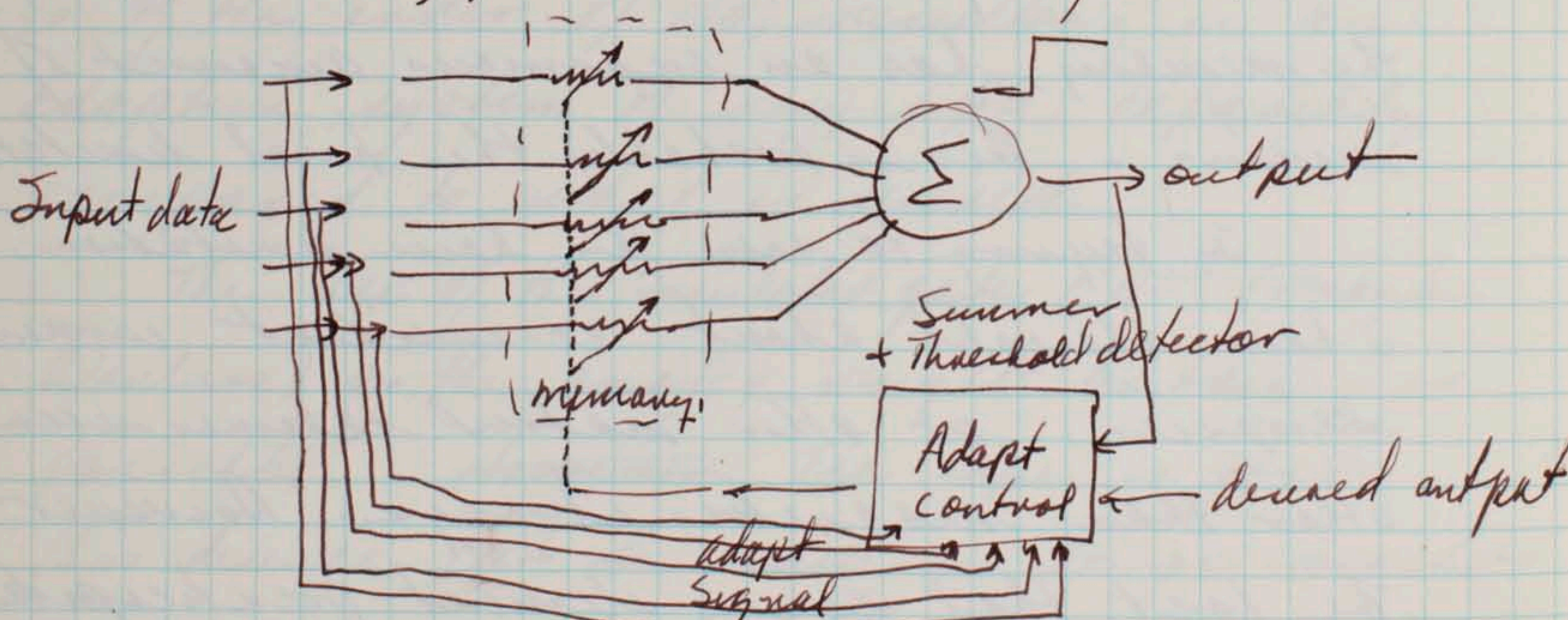
In trying to solve this basic limitation, I have thought about co-incident current memories, or other matrix schemes using other than magnetic storage. However the fact that every element participates in the decision (3 above) makes this

 10/17/62

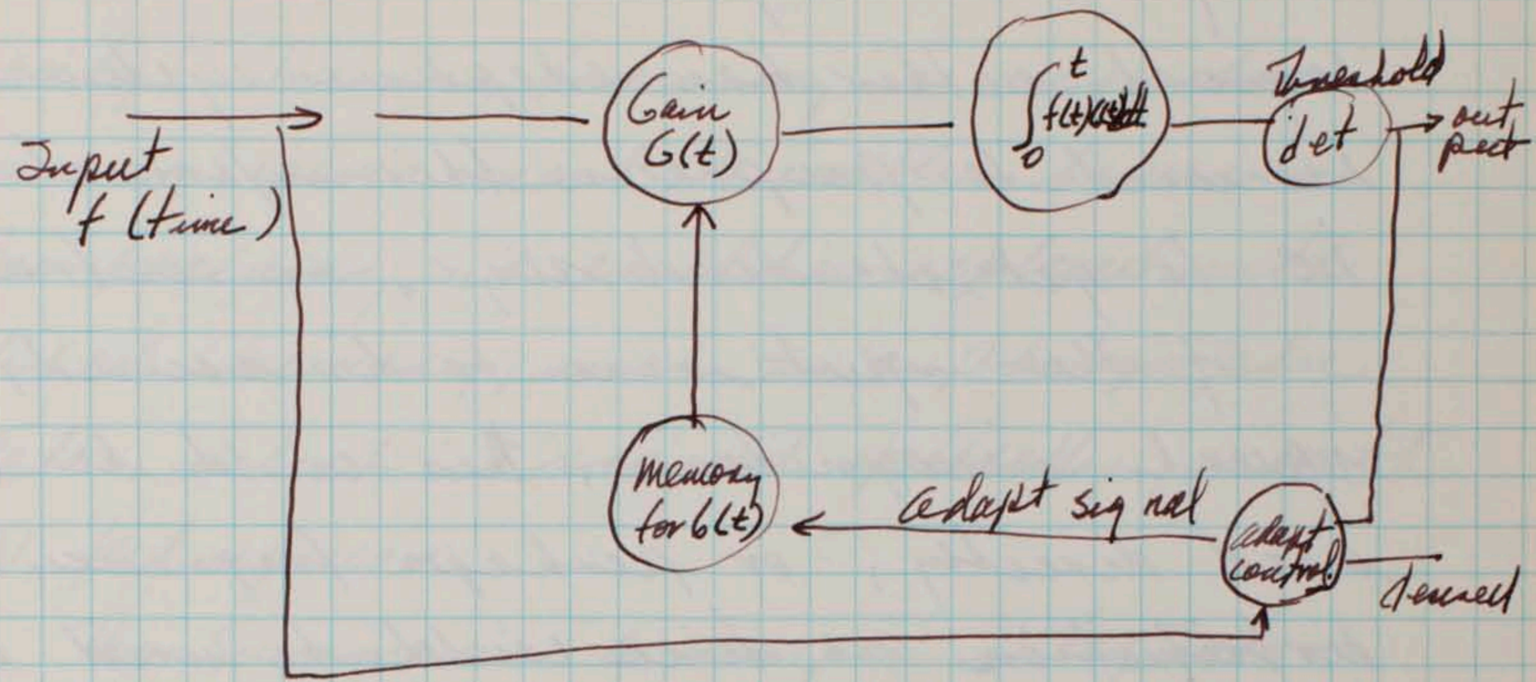
less attractive, since the whole memory must be interrogated, which takes time, and a lot of switching circuits would be required.

The answer which I have found is to use a system which scans the input data, weighting each input sample appropriately. Thus the system uses a serial input rather than a parallel one, the memory can be serially read out in synchronism with the input data.

In comparison, the serial + parallel systems would be schematically shown as follows, for a 1 neuron system.



Parallel input (all memory read at once)



Serial input (serial memory)

The total amount of input data which we would like to handle is large, much more than indicated. Consequently the difference in amount of wiring, i.e. number of connections is much more than ~~integrated~~ indicated.

~~Let~~ Now look at the possible embodiments of the various elements of the serial system.

Input: If we were doing character recognition, we might simply optically or electronically scan the character, using a television type raster. This

 10/17/62

then gives the input function f(t). Some logical, rather than adaptive system might be used to preprocess this information — i.e. to get standard size, or contrast.

If the input were to be sound, for speech recognition, this could be used directly, or perhaps frequency distribution vs. time could be used. Again, standardization of the sound level, for example might be desirable.

Variable gain element: This is an analogue multiplier, which might be simply an amplifier ~~with~~ as used in automatic gain control circuits, with the equivalent of the AGC voltage coming from the memory.

Memory: This memory must be able then to produce a voltage vs time to control the A.G.C. unit. It is read out in time in synchronism with input scan. With these requirements, a simple tape loop or drum for magnetic recording and playback.

10/17/62

could be used, with its large inherent capacity! During training a magnetic memory seems most desirable, however after training, it could be replaced with a fixed memory, such as a photographic plate, which is scanned optically, or with TV techniques.

The Summer: a simple integrator, which can be an operational amplifier with capacitor in feedback loop. After completing the cycle, the output is read, reset to zero.

Adapt system): This system turns out to be very simple. a multiple of the input signal must be ~~fed~~ added to the memory. This multiple is proportional to the (actual output minus desired output). For the memory this is the equivalent of recording sound on sound, a standard technique.

Oct 17, 1962 R. D. Noyce

pages 80-85 Read & Understood G. E. Moore Dec 12, 1962. I remember discussing these ideas with RNN after our usual Thursday staff meeting on 10/19/62. G. E. Moore

October 19, 1962

I have discussed the system described on p 80-85 with Gordon Moore at the lab, and have been studying the problem of convergence if continuous input is used, rather than the discreet input studied by Ridgeway.

Certainly, the conditions of linearly separable functions must be applied, if the single neuron is to distinguish between signals.

It will probably be desirable to standardize the input function. This might be done by setting an initial gain in the input line such that

$$\int_0^t \left[f(t)\right]^2 dt = \text{constant.}$$

In practice the threshold detector on the output will probably be desirable, in order that binary decisions are made. Then the information can be handled by logical means thereafter.

For example, let us suppose we want to perform character recognition.

Assume we want to distinguish between 500 symbols, numbers, letters, etc. The number of binary decisions required would then be 16 since $2^{16} = 512$.

Thus we could use scan of the symbol with continuous input, 16 channels in memory + integration, threshold detectors, + binary output.

Studies on simple machines have shown that redundancy of ~ 100× is desirable. 16 bits would be to decipher: In a decode matrix about 200, so let us use about 20,000 memory elements, or about 1000 per channel. — a 30 × 30 significant bit scan — looks simple.

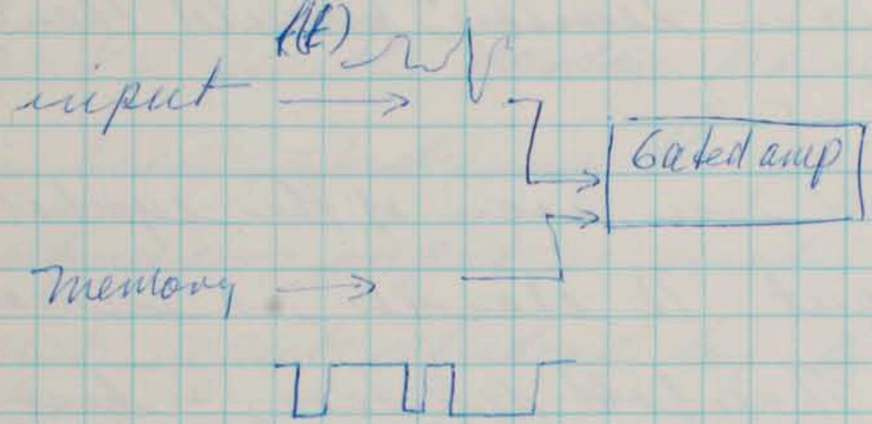
Oct 19, 1962 R.H. Noyce.

Read + Understood J.G. Moore 12/12/62

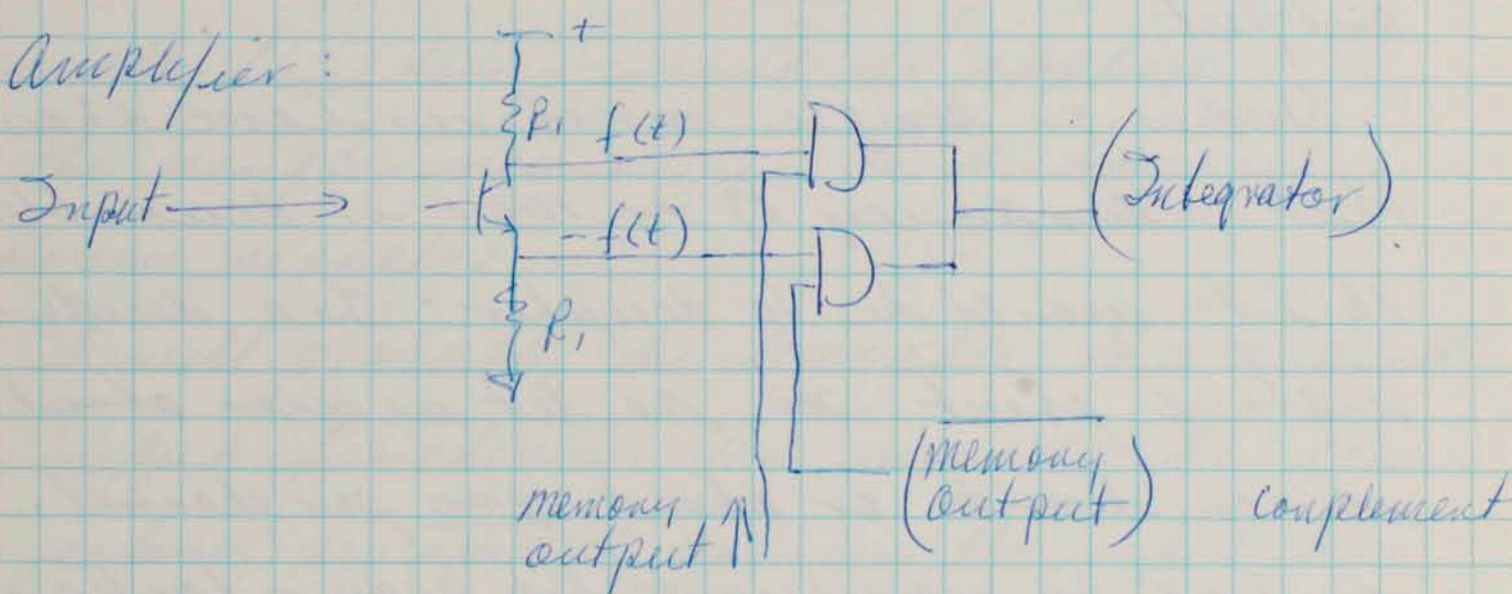
Oct 22 —

Talked to Maurice O'Shea about the gain element + multiplier, and he suggested that the simple time sampling might be best — I think this is a good suggestion — Then the memory could be simple on-off vs time. To get negative weights, the amplifier could be gated to subtract during

One part of the sample, add during the other:



Gated amplifier:



Reading into the memory would then be shifting of the edges of + to - by an amount proportional to (input × error).

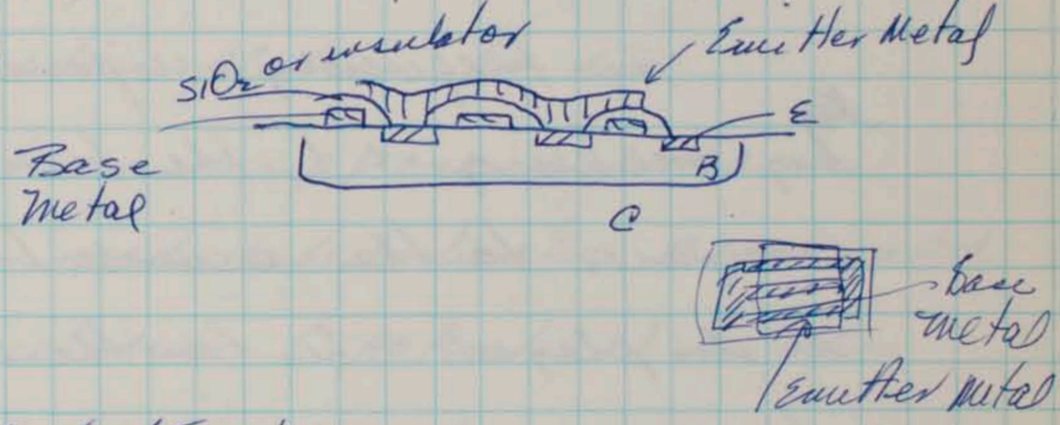
Oct 22, 1962 R N Kaye

Oct 13, 1965 –
Large Arrays sessions

CaF₂ – Negative masking – Filed already –
Extension to 2 layer or more metal should be done.

To reduce size of die for IC's the lead bond area should be put over active ckt – better thermal dissipation & more dice/wafer – Someone has talked about this before. Plough? Alternatively more leads – on 2 levels

HF Power xtr:



Shielded base contact H.F. xtr.

Problems which will appear and need solution –

1. Flexibility to handle many designs –
2. Yeild + redundancy problems.
3. Automatic Flexible Testing.

Read & understood
G.E. Moore 10/13/65
Read & Understood
L. [illegible] 10/13/65

June 6 1966.

Display tube for H F Displays.

In a CRT display of high frequency signals, the deflection sensitivity of the CRT falls as the transit time for the electrons through the deflection plates becomes comparable to the inverse frequency. To a first approximation:

check →

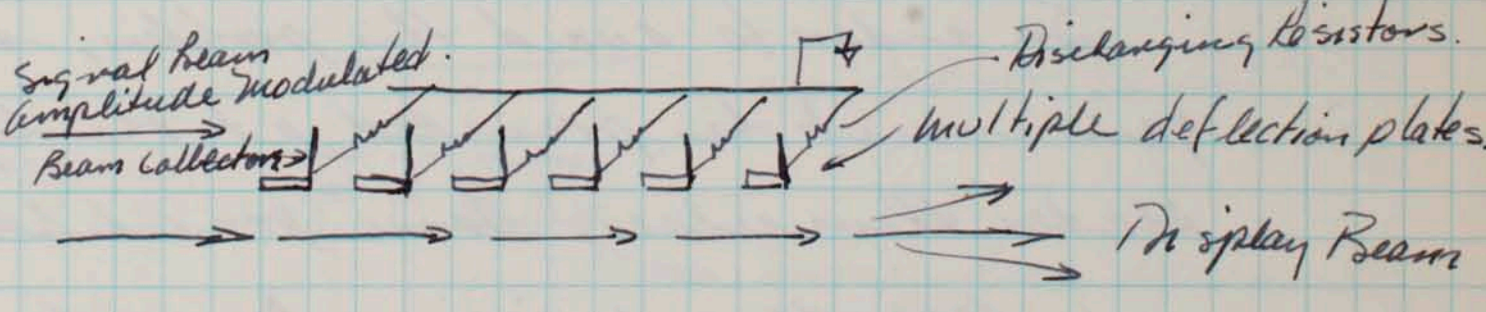
$$\text{Sensitivity}(\omega) \approx \int_0^{\pi} \int_t^{t+\Delta t} \sin \omega t \, dt \, dt \sim \frac{\sin \omega \Delta t}{\omega}$$

where Δt is the transit time between the plates.

The frequency response can be improved by making Δt, the transit time small compared to the inverse frequency which is displayed. This has the undesired effect, however of reducing the sensitivity so there is no net gain.

One way to avoid this is to ~~make~~ use ~~the same~~ multiple deflection plates, such that each has a transit time small compared to $\frac{1}{\omega}$, incorporating them in a transmission line which has the same phase velocity as the electron beam. This is the "travelling wave" C.R.T. The slow wave structures must be heavily loaded in order to ~~[illegible]~~ yield a velocity equal to that of the electron beam, and are quite difficult to achieve. None are in wide spread use. the velocity down the transmission line is fixed by the structure.

One solution to this problem would be to use the electron beam itself to carry the information to the multiple deflection plates. As an example, let us suppose we have an amplitude modulated beam accelerated to the same velocity (potential) as the beam to be deflected, which changes the deflection plates:



Each deflection plate interrupts part of the signal beam, such that a current flows through the discharging resistor, producing the deflection voltages.

The response time of the individual deflection plates is determined by the R-C time constant of the plate capacity and the discharge resistor. Again, the increase in frequency works to the detriment of actual deflection sensitivity. For example, if the plate capacity is 10^{-12} farads, the discharge resistor would have to be $100\,\Omega$ for a 10^{-10} sec response time. Beam current would have to be 1 amp to get 100 v deflection voltage, which is about what is needed. Practical beam currents might be 1 ma per plate, but even this is probably more than could be achieved.

In order to avoid this problem, some current gain must be provided at the deflection plates themselves. Some possibilities are:

1. Secondary emission. Current gains of 10 to 50 could be achieved with metals, and perhaps ten times this with materials

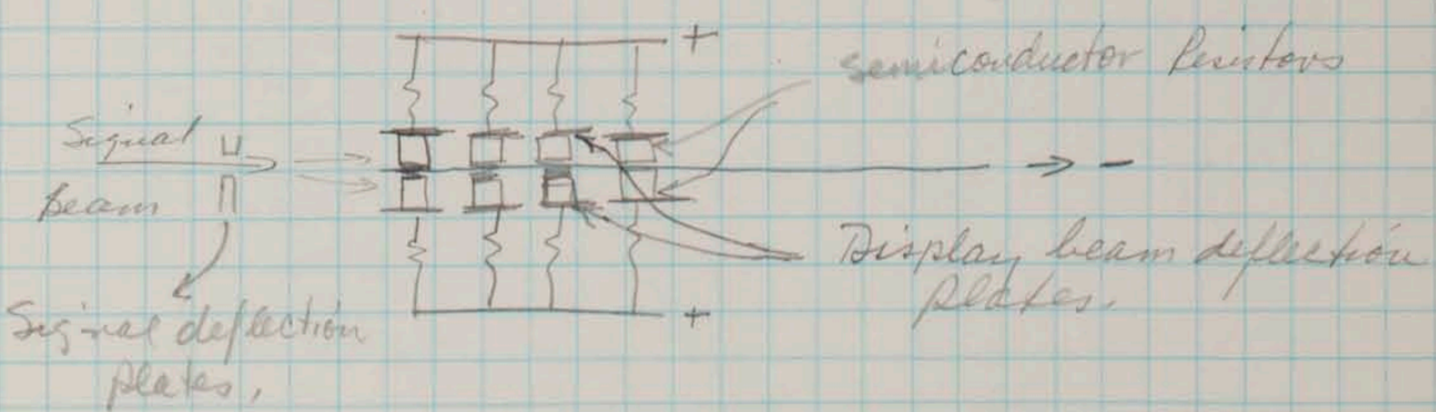
like MgO.

2. Multiplication through ionization in a semiconductor ~~device~~ material, or PN Junction. At 30 v / secondary, gains of several hundred would be available at practical beam voltages. (~10 KV)

3. Bombardment induced conductivity or ionization in high resistivity semiconductors.

In all cases, beam deflection of the signal beam could be used, rather than amplitude modulation.

It is probably desirable to use a balanced arrangement between the two deflection plates. Such an arrangement could be as follows:



Gunn Effect?

Ionization Resistor:

assume $\overset{\text{Try } 3}{30}$ v/pair produced ← check this number.

10 KV → 300 pairs. close.
3000

Sweep out time must be

$\sim 10^{-9}$ sec.

assuming at limiting velocity ← check
of 10^{6} cm/sec.

thickness must be 10^{-3} cm

$= 10\ \mu$.

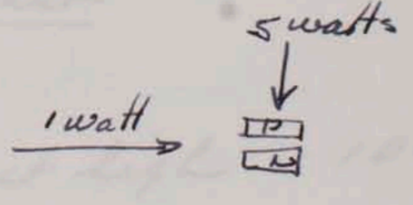
might as well use junctions.

Power in semiconductor.

Incident beam: 1 watt.

$\dfrac{100\text{ ma} - 100\text{ v}}{2}$ $\overset{5}{\cancel{10}}$ watts

secondary current.



and we need low C.

3 - 7 pf / plate.

$\frac{1}{2}$" x 1"

2½KV - 1

Velocity at 2.5KV $\frac{5 \times 10^8}{}$ - cm/sec ← 2 ns.

$\frac{10^9}{}$ $\frac{9 \, 11}{}$ 3in / 4 plates.

666 mc.

Defl. voltages.

3 V / cm - want 20 cm

± 30 V

3 pf 30 V 1 ns.

Si OK. 1 ns sweep out

Phos. beam 2 - 10 μa.

cathode current high 10x

10 ma 10 pf 100 ma

1 V/ns.

want. 100 V/ns.

Assume 1 watt beam Energy:

10 KV

$VI = 1$

$\underline{I = 10^{-4} \text{ amp} = 100 \mu a}$ - total.

Electron velocity at 10^4 volts

1 Electron mass = .5 mev

$$\frac{1}{50} = \sqrt{\frac{v^2}{c^2}}$$

$$v = \frac{c}{7} = \frac{3 \times 10^{10}}{7} = 5 \times 10^8 \text{ cm/sec}$$

for defl plates 1 cm long

$\Delta t = \underline{\underline{2 \text{ ns.}}}$

Time constants - charging.

plate capacitance 1 pf

$R = 10^3 \Omega$ $t = 10^{-9}$ sec

To achieve 100 v defl. voltage.

Need 100 ma current.

or mult. of 1000