# Inside IBM EDA: 50 Years of Innovation

## INTRODUCTION

In the summer of 2011, a small team from IBM's Electronic Design Automation organization and IBM Research interviewed several members of IBM's design automation community, asking they to reflect on the many innovations that have occurred in IBM over the years. The result is a video entitled "Inside IBM EDA: Fifty Years of Innovation". Below are lists of the people interviewed and mentioned as well as the photographs and terms used in the video with short descriptions and references. References [1], [2] provide overviews on much of this history.

## PEOPLE INTERVIEWED, in order of first appearance

1. **Robert Brayton** – IBM Alumni and Professor Emeritus at UC Berkeley
   Robert Brayton received his PhD from MIT in 1961 and joined the Mathematical Sciences Department at the IBM Watson Research Center. He retired in 1987 and became a professor in the EECS Department at UC Berkeley. At IBM his work on the numerical solution of electrical circuits and sparse matrix methods with Gary Hachtel and Fred Gustavson was the foundation of the IBM's program ASTAP. His work in logic synthesis at IBM with Hachtel and Alberto Sangiovanni led to programs ESPRESSO and MIS/SIS, later adopted by most of the commercial logic synthesis software available today. He is a member of the National Academy of Engineering. Awards include the Emanuel Piore, the ACM Kanallakis, the EDAA lifetime achievement, the EDAC/CEDA Phil Kaufman and the ACM/SIGDA Pioneering Achievement award. He has authored over 450 papers, and 11 books and is currently a Professor at UC Berkeley.

2. **John A Darringer** – Research Manager, System-Level Design, Yorktown Heights, NY
   John Darringer received his PhD from Carnegie Mellon University. He worked for Philips in Holland and then joined IBM Research in Yorktown. In the early 1970's he worked in program verification and later started logic synthesis in IBM. He held several management and positions including Director of Technical Planning for the Research Division and Director of Electronic Design Automation in IBM's Systems Technology Group. Currently he is back in Research leading a system-level design tools effort. Dr. Darringer is an IEEE Fellow and Past President of the IEEE Council on EDA.

3. **Dave Lackey** – EDA Distinguished Engineer, Test, Burlington, VT
   Dave Lackey is a Distinguished Engineer in IBM EDA, responsible for DFT Methodologies in STG. Dave joined IBM in 1978 in Poughkeepsie, NY, and holds a BSEE from RPI and a MSCE degree from Syracuse University. Dave's early career consisted of technical and management positions in Design verification and System Design for IBM's high-end server products. In 1994 Dave transferred to IBM in Essex Junction to work in ASIC Methodology, and has made contributions across the entire design flow including DFT and test, verification, physical design, floorplanning, and hierarchical design.

4. **Leon Stok** – Vice President EDA, Fishkill, NY
   Leon Stok is Vice President of IBM's Electronic Design Automation group. In 1986, he graduated with honors from the University of Technology at Eindhoven. He obtained his PhD from Eindhoven in 1991. Leon worked at IBM's Thomas J. Watson Research Center as part of the team that developed BooleDozer, the IBM logic synthesis tool. Subsequently he managed IBM's logic synthesis group and drove the development of PDS, IBM's Placement Driven Synthesis tool. From 1999-2004 he lead all of IBM's design automation research as the Senior Manager Design Automation at IBM Research. Leon has published over 60 papers and holds 6 patents. He was elected an IEEE fellow for the development and application of high-level and logic synthesis algorithms.

5. **Paul Villarrubia** – EDA Distinguished Engineer, Physical Design, Austin, TX

Paul Villarrubia received a BSEE in 1981 at Louisiana State University, and a Masters of Science degree from the University of Texas at Austin in 1988. He is currently a Distinguished Engineer at IBM where he leads the EDA Physical Synthesis Tools development project. As part of academic work at the University of Texas, Paul wrote the CPLACE placement program that is now widely used within the IBM physical synthesis system for both ASIC and Server designs. Early in his career he focused on physical design of microprocessor chips. In 1998 he made a transition from chip physical design, taking on a leadership role in defining and implementing IBM's physical synthesis system. At IBM he received 7 Outstanding Technical Achievement awards in areas related to signal integrity analysis, extraction, physical synthesis, placement, and micro-processor design. External activity includes 26 patents and 20 publications.

6. **John M. Cohn** – IBM Fellow, Distinguished Agitator, Burlington, VT
   John Cohn is currently an IBM Fellow in IBM Microelectronics. John has been an innovator in the area of design automation for both analog and digital custom integrated circuits. John received his undergraduate degree in Electrical Engineering at MIT, and earned a PhD at Carnegie Mellon University. In 2005 he was elected a Fellow of the IEEE. John has authored more than 30 technical papers and has contributed to four books on design automation. He has more than 50 patents issued or pending in the field of design automation, methodology, and circuits

7. **Chandu Visweswariah** – EDA Distinguished Engineer, Sr. Manger, Analysis, Fishkill, NY
   Chandu Visweswariah is a Distinguished Engineer and Senior Manager of Timing and Circuit Analysis in the Systems and Technology Group of IBM. He was previously a Research Staff Member at the IBM Thomas J. Watson Research Center in Yorktown Heights, NY for 19 years. He developed a number of circuit analysis, timing analysis and circuit optimization Design Automation (DA) tools that are widely used in IBM, and pioneered the invention and deployment of statistical timing analysis. He is a Fellow of the IEEE and a member of the IBM Academy. He holds a PhD from Carnegie Mellon University.

8. **Mark Lavin** – Research Staff Member, Manufacturability, Yorktown Heights, NY
   Mark Lavin received BSEE and MSEE degrees from MIT in 1972, and a PhD from the MIT Artificial Intelligence Laboratory in 1977, researching motion vision. He worked two years at Bolt Beranek and Newman, developing applications for Biochemical researchers. He joined IBM Research in Yorktown Heights NY in 1979, working on Robotics, Computational Geometry, Machine Vision, and Object-oriented programming, receiving Outstanding Technical Awards in the last two areas. Since 1990, he has worked on EDA tools, particularly as applied to Manufacturability Enhancement, for which he received an IBM Corporate Award and numerous Patent Awards.

9. **Mary Kusko** – EDA Senior Technical Staff Member, Test, Poughkeepsie, NY
   Mary Kusko is a Senior Technical Staff Member with a passion for DFT. Mary received her BSEE at University of Delaware in 1982 and has held various positions in IBM, including logic design and design verification before discovering DFT. Currently Mary defines and implements Server Test Strategy as well as manages the IBM Test Vendor Relationship. Mary's been on the Program Committee of the International Test Conference for 15 years.

10. **Jason Baumgartner** – EDA Formal Verification, Austin, TX
    Jason Baumgartner joined IBM in 1995, and quickly became involved in applying formal verification tools to find intricate design flaws. These experiences evolved into the pioneering of numerous advanced verification algorithms, which culminated into the SixthSense project and his PhD from University of Texas in 2002 and have been the subject of numerous patents and publications. Today Jason is the Formal Verification Technology Lead within IBM Systems and Technology Group, and a central figure in the external Formal Verification community active in numerous conferences, university collaborations, and the Semiconductor Research Corporation.

11. **Wolfgang Roesner** – IBM Fellow EDA Verification, Austin, TX
    Wolfgang Roesner is an expert in Verification and has architected the verification tools and methodologies being used across all IBM systems. His accomplishments in the world-class

verification methodology allow the design of the company's P7 and zGryphon processors. The Verification methodology Wolfgang put into place is not limited to the IBM processor flows as it was shown to be extensible to games processors like Cell, Waternoose, Vejle as well as a the SoC processor Prism. Wolfgang is well known in the industry for his leading role in verification tools and methodologies. He is frequently invited to deliver keynotes at technical workshops and conferences. His book on "Comprehensive Functional Verification – The Complete Industry Cycle" is the most comprehensive practical verification handbook published and is widely used in the industry.

12. **Daniel Beece** – Research Staff Member, Analysis, Yorktown Heights, NY
    Daniel Beece received the Bachelors of Science in Engineering Physics at Cornell University, Ithaca, New York, and the Masters and Ph.D. in Physics from the University of Illinois in Urbana-Champaign. He has been a Research Staff Member at the T.J. Watson Research Center at IBM since 1982, working in the area of VLSI Computer Aided Design Automation. For many years he worked in the area of functional verification and hardware simulation acceleration. He currently works on circuit timing analysis and parallel software.

13. **Kevin Pasnik** – EDA Simulation Acceleration, Austin TX
    Kevin Pasnik graduated from the Rochester Institute of Technology with a Bachelor's of Science in Applied Mathematics in 1989. Kevin joined IBM's EDA organization that same year, developing software for the Engineering Verification Engine 2.0 (EVE 2.0) hardware accelerator. He later became the software lead for the Awan and AwanNG hardware accelerators, led the team who developed AwanStar, and currently leads the AwanStarPlus development team.

14. **Louise Trevillyan** – Research Staff Member Synthesis, Yorktown Heights NY
    Louise Trevillyan joined IBM in 1974. She has worked in marketing, on optimizing compilers and architectural performance analysis, but most of her time at IBM has been spent in the Research Division working on Design Automation.. In DA, she has concentrated on logical and physical synthesis, but has also done work in high-level synthesis, incremental timing and formal verification. Trevillyan is an IEEE Fellow and a recipient of the Marie Pistilli Award for Women in DA. She is a past associate editor of IEEE Transactions on CAD, general and program chair of ICCAD and was a member of the Board of Assessment on the National Institute for Standards and Technology (NIST).

15. **David S. Kung** – Research Sr. Manager EDA, Yorktown Heights NY
    David Kung received a BA from U.C. Berkeley, M.A. from Harvard, and a PhD from Stanford University, all in Physics. He joined the Advanced Simulation group in IBM Research in 1986 and worked on a massively parallel simulation engine. He moved on to the Logic Synthesis group and contributed to IBM's BooleDozer logic synthesis system. He became the manager of the Logic Synthesis group in 1999 and led the development of the Placement Driven Synthesis tool. He became the Senior Manager of the Design Automation Department in 2004 and is responsible for the Design Automation Strategy for IBM Research. He has won 4 Outstanding Technical Achievement Awards, one Corporate Award, and is a member of the IBM Academy of Technology. He chairs the IEEE Design Automation Technical Committee.

16. **Ruchir Puri** – Research Manager Logic and Physical Synthesis, Yorktown Heights, NY
    Ruchir Puri obtained PhD degree in Computer Engineering and joined IBM Research in 1995 where he leads research on logic and physical synthesis. He spearheaded Large Block Synthesis efforts for microprocessors and has been working on synthesis of IBM microprocessors and ASICs. He has received several awards for his work including Best of IBM Award, Corporate award, and Outstanding Achievement awards. Ruchir is a Member of IBM Academy of Technology, an ACM Distinguished Speaker, an IEEE distinguished lecturer, and has been an adjunct professor at Columbia University, NY, and John Von Neumann professor at Bonn University, Germany. Ruchir is an IEEE Fellow.

**PEOPLE MENTIONED, in order of first reference**

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2. Jack St. Clair Kilbey [4], Robert Norton Noyce, First integrated circuit 1958 [5]
3. Chung-Wen Ho, Pierce A. Brennan, Albert E. Ruehli, Sparse Tableau Method 1971 [6]

4. Gary D. Hacktel , Robert K. Brayton, Fred Gustavson, Modified Nodal Analysis 1975 [7]
5. Edward B. Eichelberger, Level Sensitive Scan Design 1973 [8]
6. Paul H. Bardell, Built in test 1982 [9]
7. Gordon L. Smith, Ralf J. Bahnsen, Harry Halliwell, Boolean Comparison 1982 [10]
8. John Cocke, IBM Fellow inventor of RISC and first simulation engines [11]
9. Richard Malm, Los Gatos Simulation Engine 1983 [12]
10. Monty M. Denneau, Yorktown Simulation Engine 1982 [13]
11. Robert B. Hitchcock, Gordon I. Smith, D. D. Cheng, Static timing analysis 1981[14]
12. William Joyner, First logic synthesis 1980 [15]
13. John Gerbi, James P. Eadie, Logic synthesis for mainframes 1984 [16]
14. Glen Wienert, developed the early shapes checking software [17]

**PHOTOS SHOWN in order of first appearance**

**TERMS USED, in order of first use**

1. Magnetic Core Memory [18]
2. Punch cards [19]
3. JCL – Job Control Language for IBM's mainframe operating system [20]
4. GL/1 – Graphics Language One for describing chip layout [21], [22]
5. Masterslice – An IBM term for gate array chips [23]
6. SYSOUT – System output in IBM's mainframe operating system [24]
7. Sparse Tableau Approach [6]
8. Modified Nodal Analysis [7]
9. ASTAP - Advanced Statistical Analysis Program [25]
10. SPICE - Simulation Program with Integrated Circuit Emphasis [26]
11. LSSD – Level Sensitive Scan Design [8]
12. Chip in Place Test, BIST - Built-In Self Test [27]
13. TCM – Thermal Conduction Module [28]
14. LSI – Large Scale Integration [29]
15. SLT – Solid Logic Technology – Introduced in 1964 and packaged several transistors in a ½" ceramic module for the System 360 [30]
16. Cycle Simulation – [31]
17. BDL/CS – Basic Design Language for Cycle Simulation used for behavioral hardware specification [31]
18. LSM - Los Gatos Simulation Machine [32]
19. YSE – Yorktown Simulation Engine [33]
20. EVE, EVE2 – Engineering Verification Engine [13]
21. SAS – Static Analysis System for proving that a logic network correctly implemented the function specified at the behavioral level [10]
22. Static Timing Analysis [14]
23. Logic Transformations, LSS – Logic Synthesis System [15]
24. BDL/S – Basic design Language for specifying a logic network [31]
25. BooleDozer – Second generation IBM logic synthesis tool for workstations [35]
26. SA-12E – IBM .25 micron ASIC technology for up to 10M gates
27. Macro – A part of the geometric layout of a chip
28. Cplace – A program that does the physical placement of the design netlist onto the chip image, using a variety of placement algorithms. [36], [37].
29. Nutshell – A framework for integrating various design tools around a shared data model and loading them dynamically for execution.
30. PDSrtl - A complete flow that takes the designer register-transfer-level input and produces a placed and optimized design. It is a combination of BooleDozer and PDS. [38]
31. Rapids Rapids - A physical synthesis system, which includes routing-aware optimization. This extends placement-driven synthesis into the routing domain.
32. PDS – Placement Driven Synthesis [1], [39].

33. Pelican – An E-beam postprocessor program that took as design layout data and converted that into the format used by some commercial mask-writing tools, which used a raster-scanned electron beam to pattern photomasks.
34. HPP – Hontas Post Processor – An IBM tool for preparing data for a shaped beam electron beam mask writer.

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