20072 Kilbride Drive
Saratoga, California
September 4, 1966

The Editor
Fortune Magazine
540 North Michigan Avenue
Chicago, Illinois, 60611

Dear Sir;

THIS LETTER IS NOT FOR PUBLICATION!

re: IBM's Gamble, Part I, September 1966

I'm currently an employee of IBM and I was one of the 12th members of the 'SPREAD' committee mentioned in the referenced article. I was very impressed by the general accuracy of the story and the frank portrayal of the leading characters. However, as a witness to the events in discussion I8m surprised that you bought the engineering 'story' with a reasonable marketing 'story' not being represented. Perhaps the following few comments will help clarify several minor points:

'7000' series doing well in 1960.. Not true! The problem got so serious that the 7074 was announced six months early and the 7080 was repriced, the latter being an unpardonable sin in IBM. This took place in a series of Corporate management meetings in April to June of 1960.

The decision of IBM to become a manufacturer of integrated circuits came prior to the 360 decision and SPREAD Committee. In fact, it was a major input assumption.

'360 intended to obsolete virtually all other existing computers'..Up to November 1961 the engineers had failed to recognize the changing use of computers. There had been no basic design concept change since the 701 and 702 with the exception of the 7070. The latter machine had been forced on engineering as a 650 replacement and was generally ignored. The large scale 7090 customers had started to discover that FORTRAN was a tough type of commercial problem with lots of alphabet and input/output. The 7090 had little or no ability with commercial type problems. In short, the earlier machines obsoleted themselves and the 360 just recognized the opportunity.

As I remember it, a major reason that the 8000 never saw the light of day was the poor response it produced in marketing studies, to which Vin Learson was very sensitive.

Mr B O Evans was not an original member of the SPREAD Committee. Rather, he was brought in tb finish the job after John Haanstra was promoted. In retrospect I believe that John Haanstra was most responsible for the clear committee recommendationds built on Fred Brooks' fine plan. At the time, Bo Evans was a major opponent to the plan and was actually creating a state of anarchy in engineering design. That is why the key recommendation of the SPREAD Committee was to give Fred Brooks computer architectural responsibility. With Vin Learson's support that gave Brooks the lever he needed. After that, ironically, Evans changed hats and really supported Brooks.

continued.

I believe that there are three key ommissions in your recounting. The first is the significant programming system concept breakthrough that allowed just three memory size oriented plans to cover the entire processor range. I believe that this was the real brekthrough. Otherwise every processor would need one or several programming packages, despite allthe compatibility pitch - whichwas at the MACHINE language and not the programming language level.
The second ommission in your report was the famous IBM time gap. As is true with every computer manufacturer there must be an 18 to 24 month time gap between plan and announcement. This is followed by an 18 month gap from announcement to initial delivery. In January 1962, the key marketing manage ment (Dawkins and Garrison), recognized that they would have to hold the line of competition and customer needs for a period of 2 to 3 years, and with only minor new product announcements. The great accomplishment was that they did hold the line while engineering finally got rolling under the Brooks' architectural direction.

The third ommission was the guiding philosophy of Vin Learson as quoted to me several times by Fred Brooks. The real objective is to make the decision right, not just to make the right decision.

In summary, the 360 decision was a big one which I believe was fully recognized by the key participants at the time. What wasn't recognized is what I refer to as the Tidal Wave effect. Prior to the 360 there was a large number of computer families in IBM. Changes and significant moves occurred on only one family at a time thereby giving cover and assistance from the other families. With the 360 any move covers the whole line at one time. When programs slip they slip for the entire family ... or am I getting to Chapter two?

This letter is one man's view of a complex series of events, I've fowarded it just to provide a little more background to you about the events. PLEASE DO NOT PUBLISH THIS LETTER.

Very truly yours,

Jerry Svigals

Mr. Y. P. Dawkins
Copy No.

PROCESSOR PRODUCTS

Final Report of SPREAD Task Group

December 28, 1961

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CONTENTS

I. INTRODUCTION

A. Mission and Objectives

1. The SPREAD activity was initiated to establish an over-all IBM plan for data processor products. The plan is to encompass all stored program processor developments in IBM, is to extend to 1970, and must consider the following factors:

   a. Solid Logic Technology (SLT), which promises improved cost/performance and reliability.

   b. New market demands for systems capable of multi-terminal, on-line, real-time, multiprogramming operation.

   c. The explosive growth in applied programming demanded by a larger number of dissimilar systems.

   d. The 15-20 engineering groups generating processor products and the need for the establishment of consistency -- i.e., an IBM "image" in the processor field.

   e. The need to resolve the interactions between present and new processor products across divisional and World Trade lines.

2. Faced with these present problems, the SPREAD task force set as its objectives:

   a. The definition of a new line of processor products.

   b. The establishment of logical design, engineering, and applied programming ground rules, within which a processor product line consistent across divisions and World Trade must be defined.

   c. The creation of a plan for the introduction of these new products which will optimize the conflicting demands of:

      - Market need
      - Impact on present installed processors

   d. The initiation of an appropriate management measurement and control mechanism to assure the implementation of the SPREAD product concepts.

B. Summary of Report

This report recommends a new family of compatible processors for the IBM product line. A summary of the major points follows:

1. IBM customers' needs for general-purpose processors can be most profitably met by a single compatible family extending from the smallest stored-program core-memory machine to the machine for customers growing beyond the 7094 and 7030. There are processor needs above and below this range - it is not yet evident that these can be compatible with the new processor family.

2. Justification for the compatible family has been established with respect to marketing. It is clearly advantageous to development and manufacturing. Competitors appear to be relying heavily on common programming languages to achieve compatibility. The new processor family guarantees to IBM a compatibility level not achievable by common programming languages.

3. Each processor is to be capable of operating correctly all valid machine language programs of all processors with the same or smaller I/O and memory configuration.

4. A range of architectural and engineering ground rules have been developed as the foundation for the new processor family.

5. An applied programming plan is outlined which is independent of the number of processors. It is projected that programming systems will be written for only three configurations of the compatible family.

6. To achieve the revenue and profit growth goals, it is concluded that the new processor family must address itself to new, rather than existing, application markets and incorporate existing 1400 series as subsystems whenever possible.

7. Because of the rapid market expansion forecast for the World Trade Corporation, each element of the new family must consider this market as well as domestic in all phases of development and pricing.

8. For financial reasons, it is concluded that a compatible "hardened" family cannot be developed by FSD.

9. An implementation program is established in the areas of:
   a. Interdivisional control including:
      - Architecture
      - Arbitration
      - Executive Control
      - Design Assignments
      - Product Control Procedure
      - Standards
      - PERT
      - Marketing Requirements

b. Technical Development
c. Programming
d. Marketing
e. Introduction Planning
f. Security

C. Planning Considerations

1. General

Before examining the future strategy proposed for IBM in the design, manufacture, and marketing of electronic data processor equipments, it is instructive to look into our past. Chart I shows, for the past decade, the growth in revenue derived from EDPM central processing units.

The SPREAD group has adopted the following definitions for the elements considered in the report:

ALU: Arithmetic and Logical Unit
CPU: ALU plus memory
Processor: CPU(s) plus I/O Channel(s)

The effects of I/O and peripheral equipments on the processor have been considered but not the I/O equipments themselves.

2. Firm Base Products

Appendix I contains product survival curves for each of the firm base processors for the years 1960 to 1970.

GPD	14LC, 1401
	650
	305
	1620
DSD	1410, 1410X
	7070, 7072, 7074
	704, 709, 7040/44, 7090/94
	705, 705 III, 7080
	7030, 7034

It should be noted that these division product forecasts assume a four-year product life.

Charts II and III show the total GPD and DSD firm base processor points to be installed in Domestic and World Trade respectively over the decade. Charts IV and V show the world-wide processor points installed in the commercial and scientific markets, broken down by small, medium, and large processor products.

Chart VI shows total processor points installed for Domestic, WTC, and IBM total.

3. Corporate Growth Objectives - Processors

A net Corporate growth objective of 20% per annum for processors has been assumed. This rate of growth, projected from the 1961 installed position of 29.1 million points requires 151 million processor points in 1970. If this objective can be achieved, a larger growth rate would be assured for the over-all EDPM area since the trend has been for the systems fraction composed of I/O and peripheral equipment to increase.

4. Market Forecasts

Charts VII, VIII, and IX show forecasts for markets already defined by DPD, WTC, and FSD special systems, capable of absorbing the processor points we project installing through 1970.

In summary, these charts show the following net processor points forecast to be installed:

	Millions of points installed Year End		
	1961	1965	1970
DPD	25.4	51	92
WTC	3.5	25.6	59.4
FSD - special systems	.2	2.4	11.4
	29.1	79.0	162.8

These forecasts give preliminary evidence of our ability to maintain a world-wide 20% growth in EDPM over the balance of this decade.

It is significant to note that the forecast shows an average processor growth rate of 15% for domestic versus 37% for WTC.

5. Military Market Considerations

In addition to those portions of the military market handled by standard equipment, included in DPD above, and by specially packaged airborne and space systems, not included above, FSD forecasts 11.4 million equivalent points of special systems installed at the end of 1970. Of this, 9.1 million points will be ultra-reliable systems employing standard processor organization concepts and 2.3 million points will be environmentally conditioned to military specifications.

6. Transition to the New Product Line

The SPREAD task group has concluded that a compatible line of CPU-processor products is realizable which will:

a. Meet the needs of the commercial, scientific, and communications and control markets;

b. Be competitive;

c. Employ advanced design concepts.

Since such processors must have capabilities not now present in any IBM processor product, the new family of products will not be compatible with our existing processors. While incompatibilities are a marketing disadvantage, it should be noted that systems reprogramming will, in many cases, be required, independent of the processor used. This will occur whenever the user wishes to obtain the benefits of any of the following:

a. Random access rather than batch processing

b. The integration of communication facilities

c. The simultaneous operation of multiple processors

d. Multiprogramming to achieve efficient on-line operation.

The new family of processors must emphasize such new capabilities, so that the attendant reprogramming will be a natural outgrowth of systems improvements rather than be looked upon by the user as a redundant effort dictated by the lack of compatibility between the new line and his installed systems.

7. Impact

The impact of the new processor family on the installed inventory must be controlled. There are various tools for this control, such as the following:

a. The design of the new line must address net new markets.
b. Specifications and delivery schedules of software.
c. I/O configurations provided
d. Applications support packages
e. Marketing programs such as advertising and sales promotion
f. Pricing of new products
g. Trade-in allowances and depreciated sales on current products
h. Timing of announcements
i. Incentives in the sales plan

D. Introduction Timing

1. Objective

The new line of processors must be introduced to meet the following fundamental requirements:

a. Sales must produce net plus new business

b. Existing equipment must not be unduly impacted.

2. Relations to Existing Product Line

The questions of how and when to introduce the elements of the new processor family bring to the fore many problems and paradoxes relative to the existing product line. Some of these are:

a. Our present product lines are distinctly either commercial or scientific in their emphasis - the new line of processors will exhibit dual use capability.

b. In the low performance end of our present product line, we are strong commercially with the 1401-10, but weak scientifically with a gap between the 1620 and 7040/44. At the high performance end of our present product line, we are strongest scientifically, with the 7090/94, and relatively weak commercially with the 7074, 7080. Throughout the line there is insufficient capability for real-time, multiprogrammed systems.

c. In the past, we have been able to direct products to specific market areas by tailoring characteristics of processors, I/O and software. This will be more difficult in the new compatible family with a basic instruction set, consistent I/O handling, and software designed for the entire family.

d. The price/performance of the new processor family must not be allowed to destroy the revenue base.

3. Timing

The specific timing of each element of the new family must be carefully determined by the product and marketing divisions via established procedures. The SPREAD task group has set broad phase-in boundaries for introducing the new family based upon review of the product survival curves, recent and anticipated competitive moves, relation to SMS products nearing announcement, and the need to fill gaps in the product line. The recommendations are expressed in the Implementation section.

II. PROCESSOR DESIGN

A. Processor Product Line

IBM customers' needs for general-purpose processors can be most profitably met by a single compatible family extending from the smallest stored-program core-memory machine to the machine for customers growing beyond the 7094 and 7034. There are processor needs above and below this range - it is not yet evident that these can be compatible with the new processor family.

1. It is recommended that the processor product line comprise five compatible CPU's ranging in internal performance from below that of the 14LC to above that of the 7034. The internal performance ratio between successive entries should be between three and five, with the low end entries having smaller spacing ratios. The approximate performances of these five CPU's is illustrated by a total time for a two-address comparison operation on a five-digit field of 200, 75, 25, 5, 1 us.

   CPU's are most sharply distinguished by their internal performance and by any biasing or tailoring for specific applications. Systems are, however, best measured by their throughput on typical problems. Because of this and because of the economics of multiple-shift usage, it appears wise that the internal performance ratios should not be greater than five.

2. The line of CPU's must each be software supported and equipped with a selection of other devices which affect system performance.

   a. Input-output channels of various data rates and various degrees of memory interference.

   b. Memories of various sizes.

   c. Various complements of I/O devices.

   Further specialization in design for each customer must be achievable through the ability to couple any number and combination of CPU's into a single stored-program-controlled system.

3. Each processor is to be economically competitive at the time it is introduced.

B. Architectural Ground Rules

The following ground rules should be imposed on the groups working on the logical structure of the proposed processors. The mechanism for enforcing and elaborating on these ground rules is proposed in the implementation section.

The group is confident that economically competitive processors obeying the ground rules set forth below can be built with one reservation. It is not evident that downward compatibility can be attained through the whole product range. The group recommends, however, that the design requirement for downward compatibility be stated as a firm ground rule and that development proceed on this basis until the Phase I review. If, at that time, it appears that economically competitive downward compatibility cannot be achieved across the whole processor range, then the range shall be broken into two segments with downward compatibility to be acheived within each segment.

1. Compatibility

   Each processor is to be capable of operating correctly all valid machine-language programs of all processors with the same or smaller I/O and memory configuration.

2. Formats and Addressing

   a. Address lengths are to be variable so that not all high-order zeros in addresses are expressed.

   b. Addressing is to be binary in radix. Efficient use of memory dictates that addressing must be binary or alpha-numeric, in preference to decimal. Between these, binary is more flexible, straightforward, and economic.

   c. Decimal digits and alphanumeric characters will be represented in four-bit and eight-bit bytes.

   d. Variable-length field manipulation, independent of physical memory width, will be standard.

   e. Each four-bit byte is to be directly addressable.

   f. Move and other streaming operations will operate on fields as short as four bits and as long as memory capacity, though length restrictions may be laid on arithmetic operation.

g. Negative data fields will be represented in true, not complement, form with the sign if present appearing at the low-order end of the field.

h. Address modification through additive indexing is to be standard on all machines.

i. The hardware-software package shall provide automatic translation (at least as late as load time) of symbolic address (indirect addressing) at least for the addresses of similar I/O devices.

j. The hardware-software package shall provide for the automatic and independent relocation of program and data, at least as late as load time.

k. A hardware memory protection system shall ensure inter-program protection against any problem-program error.

3. Operations

a. No bit combination shall exert any mandatory control function when it occurs in the data stream of a CPU.

b. All fixed-point arithmetic operations shall be provided for radix 10 and radix 2^n.

c. Floating point arithmetic shall be available for all CPU's, at least as an option.

d. Compatible sterling arithmetic operations will be available for all CPU's, at least as an option.

e. A uniform subroutine linkage mechanism shall be provided.

f. Program interruption upon external signal, program invalidity, or machine malfunction shall be provided as standard in all machines.

g. Facilities for the operation of a supervisory program shall be such that the supervisor can retain positive control over any problem program without manual intervention. Non-stop operation shall be possible.

h. A real-time clock and interval timer shall be available for all CPU's, at least as an option.

4. Input/Output Control

a. I/O shall be programmed through a sequence of channel control words, whether a physically separate channel is used or not.

b. I/O operation shall be logically overlappable with processing, but burst operation may be used for high-data-rate devices.

c. Program-controlled cross-channel switching of I/O devices shall be designed for all systems, but not necessarily as standard equipment.

d. Multiplexing and control of low speed lines and terminals will be accomplished with direct, minimal attachments to standard processors without requiring special-purpose stored-program devices.

e. Operator consoles shall be connected to processors as I/O devices.

f. To any I/O device type, all channels shall appear identical except in data rate.

5. Reliability and Serviceability

a. To meet the demands of the new applications each processor shall attain corporate goals for significant reliability and serviceability improvement.

b. All data paths shall be so completely checked that no single malfunction goes undetected. Controls shall be so checked that the probability of undetected control malfunction is no higher than that of undetected data-path malfunction.

c. Each system portion whose servicing does not prevent system operation shall be furnished with facilities for independent, off-line servicing.

d. Machine language consistency shall extend to maintenance consoles. Each CPU shall be equipped with appropriate portions of a single full-scale maintenance facility.

e. Ultra-reliability shall be achievable by multiple-CPU systems.

6. Engineering Ground Rules

The following engineering ground rules must be imposed on all groups working on the proposed processors.

a. Microprogram controls using a read-only memory shall be employed unless the cost/performance of a conventional control system is less than 2/3 that of a micro-program control system.

b. A single detailed method for memory-CPU coupling shall be developed and applied to all processors.

c. Timing and priority controls shall be so designed that no processor or channel assumes that it inevitably gets the very next memory cycle after a request.

d. All options announced with a processor shall be field installable.

e. When one processor is substituted for a slower one, the I/O gear shall not need to be changed.

f. Each processor shall be designed to accommodate 50-cycle power supplies.

III. SOFTWARE

A. Objectives

Since systems are composed of both hardware and software, there must be an over-all plan for software products which adequately complements the hardware plans. The term "software" includes programming systems and industry application programs.

IBM's objectives in the software area must be the following:

1. Render more effective support to our customers, particularly emphasizing specific industry application programs for new market areas.

2. Through compatibility at the problem statement level, enhance the ability of customers to move from present to future systems and to grow from one new system to another with minimum disruption.

3. Develop techniques to provide software products more efficiently.

4. Design and implement a unified source language for handling scientific, commercial, control, and real-time applications. Once consolidated on this base, we will be in a strong position to push forward on new industry application developments and to establish leadership in industry programming standards.

B. Summary

1. Only three programming systems are required for the processor family. This is a significant reduction over the current practice of producing a programming system for each processor type in the current line.

2. A single IOCS structure will be provided for the entire processor family. Elements of the structure will be designed in an additive fashion so that a substructure specified for a lesser system may be embedded within a larger system.

3. The following list of control programs will be provided:

   a. Console communication.

   b. Stacked job monitor.

   c. Basic skeletal real time control program.

   d. Supermonitor control for multiprogramming using type (b) and type (c) monitors as submonitors.

   e. Multiprocessing monitor(s) for controlling an interconnected processor complex.

4. The programming languages shall permit the user to indicate all possibilities for concurrent operation; the compilers shall use this information for compiling programs which will efficiently use multiple identical processors and multiple input/output channels. The processors must contain the facilities required to permit this mode of operation.

5. The number of industry application programs required to serve the entire processor family for a given application will depend upon the problem structure of the application. It is reasonable to expect that this number will not, in general, exceed three. Industry application development efforts should be directed to a configuration spectrum consistent with that described for the programming systems.

6. Upward and downward compatibility at the machine language level provides program compatibility at the programming language level in the following sense:

   a. Programs prepared for a data processing system having a given configuration will assemble, compile, and run on any data processing system of an equal or larger configuration.

c. Programs written for a given system configuration may be compiled on a larger configuration and run on the given system.

7. Both upward and downward compatibility at the machine language level are assumed. Should downward compatibility not materialize, the number of versions of Applied Programming support packages will be multiplied by the number of processor types having distinct instruction sets.

1. Users will still code in an assembly (1 for 1) language with macro-instructions.

2. Users will require scientific, commercial, and information handling languages which are more expressive and more powerful logically than FORTRAN and/or COBOL.

3. User groups may establish standards for language outside of IBM control.

4. Users with back-up store facilities will require an IOCS type system integrated with the assembly and compiling systems, and open-ended with respect to communicating with I/O facilities.

5. Users will, to provide operational efficiency of data processing systems, depend more and more on monitoring systems such as:

   a. Stack-type monitors integrating I/O control with assembly and compiling programs will make time between problems a function of processor speed.

   b. Conversational mode for on-line inquiries and on-line problem solutions will be required in the monitoring systems.

   c. A significant portion of systems having conversational mode capabilities will require a multiprogramming monitor sufficient to schedule and dispatch on-line requests according to priority rules and to overlap I/O operations for highest over-all systems efficiency.

   d. Routine TELE-PROCESSING applications may be integrated into the operation of a centralized data processing center. Although the action programs will be tailored to the specific applications, functions associated with the operation of the communications system (line polling, code conversion, message assembly, etc.) must be carried out through a monitor.

   e. For large data processing centers, a monitor must provide for the overall management of program and data files.

6. Users will require debugging at the source language level for all processor types. This includes the ability to modify programs readily.

7. TELE-PROCESSING, Process Control, military command and control, information retrieval, and other real time systems will require highly customized software. The trend, however, will be toward isolating functions common to a class of systems and providing general purpose software packages whenever feasible. Some such functions are:

a. System supervision

b. Communication line management

c. Industry oriented source languages

d. Real time utility programs (including switch over and/or graceful degradation of service).

8. Users will ask for more application program packages.

D. Programming Technology

1. The Problem

Central processor compatibility between two data processing systems does not, in general, imply system compatibility. Differing core storage and I/O equipment configurations mean that, in practice, software packages and customer's applications may not be transferred from a larger to a smaller system configuration without substantial or even complete reprogramming.

2. The Present State of the Art

Techniques are now known, that permit input-output control system (IOCS) programming packages to be constructed to allow for (1) an input tape to substitute for card input/or paper tape input equipment, (2) output tapes to replace card or printing output units, (3) disk files to replace intermediate or scratch tape files.

Techniques do not exist, in general, to solve the following:

a. Substitute tape files for random file programs.

b. Substitute card I/O for tape usage.

c. Substitute a lesser amount of core storage and back-up storage for a larger amount of core storage.

d. Substitute a lesser number of tapes for a larger number of tapes.

3. Projected Future State of the Art, 1965 - 1970

The problems of downward system compatibility across various configurations will not be completely solved in the period 1965 - 1970. However, there will be advances in some areas to permit a greater degree of downward compatibility - most likely in the ability to substitute random disk file or tape storage for some core storage with some performance reduction. Work currently under way in Research and the Product Divisions indicates that some progress will be made in this period.

E. Software Products

Programming packages for the compatible processor family should be constructed at three points in the system configuration spectrum. These three points are (very roughly):

Configuration I	Card I/O and 4,000 character core storage
Configuration II	(a) 16,000 characters of core, plus (b) card I/O or two tapes, plus (c) five tapes or disk file.
Configuration III	(a) 128,000 characters of core, plus (b) two tapes, plus (c) five tapes or disk file.

There is upward compatibility among the three configurations in that the Configuration I package can run on Configurations II or III. Downward compatibility will generally be lacking for two reasons:

- the program package for the larger configuration uses all the system components of the given system configuration, and
- the program package for the smaller system will lack some input language features that the larger system package permits.

1. Symbolic Machine Language Facility

a. Configuration I

A simple assembly with severe restrictions on:

(1) pseudo-operations,
(2) arithmetic address expressions,
(3) macro-generative ability, and
(4) data description implication.

Two card passes will be required to obtain a deck containing on each card:

(1) a single original symbolic entry, and
(2) an absolute equivalent for loading and listing purposes. A symbolic table may be optionally punched (or listed) between card passes.

b. Configuration II

An extended assembly language permitting arithmetic address expressions of considerable flexibility will be provided. Output will contain information to permit relocation at loading time. Symbolic dump operations will probably not be available. System macros will be provided for IOCS linkage since normal operation of object programs uses IOCS.

c. Configuration III

Symbolic dumps, flexible programmer macro facilities, multiple symbolic location counters, generalized heading and exotic features will be provided.

2. Scientific Language Facility

a. Configuration I

A simple interpretive subset of the scientific language will be available. There will be:

(1) a restricted set of mathematical functions.
(2) limited input/output editing ability.

b. Configuration II

A scientific language compiler will have the following features:

(1) compiling of individual routines independently
(2) ability of compiled routines (relocatable) to operate with separately assembled routines
(3) limited source language facility for the programmer to specify program and data segmentation
(4) operable within a simple monitor.

c. Configuration III

Additional features are:

(1) high speed execution with some additional compiler complexity
(2) extensive symbolic debugging facility
(3) as comprehensive a set of automatic or semi-automatic problem segmentation and overlay features as the state of the art permits.

3. Business Language Facility

a. Configuration I

A summary-punch, merging, selection and tabulating facility will be provided. This will provide for sequence break-summary line operation, page heading and numbering, cross footing and simple extension operations. Special calculation and control break-in points for inserting machine language coding will be provided.

b. Configuration II - III

A business language compiling facility will be provided for:

(1) disk and tape file creation and updating
(2) report generation
(3) sorting

The highest degree of integration of these functions will be attempted.

4. Combined Language Facility

A single language designed by IBM is recommended in the Implementation section. This language will effectively express a large variety of processing functions, and can be expected to be used for most problems in place of strictly scientific or business languages.

5. Input-Output Control System

As used here, IOCS includes (1) physical selection, (2) transmission checking, (3) re-read or re-write routines for equipment error, and (4) end-file and unusual condition routines. Thus, the IOCS supervises all I/O interrupt activities and handles queueing of pending I/O requests. Frequently the I/O buffering routines are not part of IOCS proper but are an optional extension to it. The buffering routines communicate in two directions:

- to the IOCS controlling hardware, and
- to the operating program which accepts from, and gives to, the buffers blocks of information.

A further level of supporting routines to the I/O buffering provide for conversion and editing of information.

a. Configuration I

Instead of a separate IOCS, a one-ahead card reading and conversion routine, and a one-behind conversion and punching/printing routine will be provided.

b. Configurations II-III

Variants of IOCS and associated routines will handle each I/O unit by type, and as far as possible will provide uniform interfaces to the running program. A major software development effort will be required to handle the wide variety of I/O equipment in the future. I/O control programs must be constructed in modular sections to handle the exact configuration of any particular customer system.

6. Monitor Control

This category refers to programs that automatically sequence control between different jobs or between different parts of the programming system in back-up storage. This function will frequently also allocate specific I/O units to a job or subsystem and will be tied to the installation's computer time accounting system. Console communication will be controlled by part of the monitor.

a. Configuration I

Only minimum console communication will be provided.

b. Configuration II

A stripped-down stacked-job monitor with ability to compile, assemble, and execute sequential jobs will be provided.

Also, (but not for simultaneous usage), there may be provided a skeletal control program for real time usage, if it turns out to be possible to define such a control program to meet widespread requirements.

c. Configuration III

An extensive stacked-job monitor with tape and disk assignment facilities, automatic communication to the operator regarding reel mounting and demounting are expected.

7. Supermonitors

Supermonitor functions of two types will be required.

a. A multiprogramming supermonitor to control as subsystems the stacked-job submonitor, and a real-time submonitor. For example, a supermonitor might control both a GEM on-line real-time design programming system, and a stacked-job operation.

b. A multiprogramming supermonitor to control and sequence a group of processors interconnected to form a single system complex. Multiple processor configurations involving several consistent or inconsistent processors may be anticipated in the period under review.

IV. MARKETING

A. Summary

The marketing implications to DPD, FSD and WTC of a compatible family of processors are:

1. Compatibility in processor logic and applied programming languages for an entire family of processors is a major advance. The assurance of compatible growth will appeal to customers and will sell more processors.

2. A direct advantage of compatibility to marketing appears wherever processor logic or applied programming languages are used to accomplish a marketing function. Examples are the basic education of field personnel in the processor line, and the development of general industry application packages.

3. Compatible processor logic and programming languages will contribute to the development of expanded marketing tools such as processor selection guides, advanced industry application packages, and standard installation procedures. These tools will increase sales team productivity.

4. Processor compatibility will not make IBM a materially better target for competition.

5. Potential problems of compatibility include:

   a. Every product or support announcement may affect all of our customers and, therefore, must be more thoroughly pre-tested.

   b. IBM may be pressured to perpetuate compatibility indefinitely.

   c. Compatibility may force IBM action in product areas where it is not desirable (e. g., having to announce a new feature for the entire family).

6. The hardware price/performance race will continue regardless of compatibility. However, compatibility will improve our ability to cope with the situation.

7. The impact of any new family on current IBM systems will always be a problem regardless of compatibility.

8. The dual purpose nature of the new family complicates transition impact.

9. Compatibility will aid Customer Engineering in education on processor logic, diagnostic programs expressed in compatible programming languages, and consistent maintenance procedures. Customer Engineering will have to service up to five physically different machines.

B. Marketing Considerations of Compatibility

1. General Advantages

   a. Upward compatibility permits an easier and faster sale because:

      1) A smaller processor may be initially justified while the customer is guaranteed investment protection during a growth period.

      2) A phased growth program can be economically and realistically justified.

      3) Incentive to consider competitive growth systems is minimized

   b. Downward compatibility, if achieved, will permit better sales control of a large decentralized user with a centralized methods staff.

   c. Basic processor education covers a wide product span. Compatibility minimizes the retraining problem.

   d. It will be easier to interchange customer-developed application material.

   e. Compatible off-line equipment will be available.

2. General Disadvantages

   a. Once committed to compatibility, it will be difficult to change to another approach.

   b. Every product or support announcement may affect all of our customers instead of a few and, therefore, must be more thoroughly pre-tested.

3. Transition Advantage

   a. Compatibility and new capabilities when and as disclosed will be strong incentive for customers to convert.

4. Transition Disadvantages

   a. Partial announcement may offset the advantages of compatibility.

   b. The compatible family adds one more processor concept to be mastered and supported by the sales team during transition.

   c. The new family will not be compatible with existing processors. Some customers will be dissatisfied unless an alternative is provided to permit utilization of his prior machine investment.

5. Sales Advantages

   a. Compatibility, when disclosed, will be a powerful selling tool.

   b. Compatibility offers maximum protection to customers' future investment.

   c. The customer will receive basic education advantages.

   d. More people in the available labor market will be trained on the same logical organization and programming system languages.

   e. Customer programs can be demonstrated on different size processors.

   f. A large Datacenter or test center processor will be usable for all ranges of customer support.

   g. A compatible line requires less effort to adapt an application or demonstration package to several processors.

   h. Compatibility will permit large volume selling.

6. Sales Disadvantages

   a. Compatibility may lead some customers to demand rapid response to their fluctuating requirements.

   b. Increases the market potential for others in Service Bureau or Datacenter business.

7. Systems Engineering Advantages

a. By knowing the compatibility and optimization rules of the family in advance, one installation job may be made to suffice for several levels of processor growth.

b. Availability of test and Datacenter processors with large configurations will allow central program compiling with more powerful language statements than can be handled on small configurations. This will ease the systems installing problem.

8. Systems Engineering Disadvantages

a. Customers may demand more frequent review of installed equipment performance and more frequent configuration changes.

b. Customers may use compatibility as an excuse for not devoting enough time or personnel to their systems job because they expect a greater contribution from other users.

9. Competitive Marketing Advantages for IBM

a. Competitors appear to be relying heavily on common programming languages to achieve compatibility. The new processor family guarantees to IBM a compatibility level which will not be possible, in the 1965 - 1970 period for a non-compatible family of processors relying on common programming languages.

b. Compatibility will allow easier competitive analysis and education since one logical or applied programming language comparison would be usable over a broader IBM processor span.

10. Competitive Marketing Disadvantages for IBM

a. IBM compatibility may encourage competition to be compatible with us, in order to tap our support efforts.

b. The family concept will allow competition to better anticipate our product line and to react more effectively.

c. Compatibility will make competitive salesmen more productive since their knowledge of IBM processor logic, applied programming

languages, and knock-offs will apply to the entire family.

11. Advantages of Generalization Allowed by Compatibility

Several major problems which are faced by sales and systems engineering personnel may be solved generally because of the compatible processor line. Some examples are:

a. A universal application library.

b. A library of system approaches using formats designed for easy communication.

c. A set of rules for configuration selection and optimization.

d. A set of guides for reviewing installed processor performance and for recommending processor improvement.

e. A set of guides for installation preparation.

f. A set of guides for program assembly, testing and review.

V. FSD - RELATIONSHIP

A. Summary

1. SPREAD has found no way to provide a compatible hardened line of SPREAD processors, nor to provide single compatible hardened processors to augment the SPREAD family.

2. FSD will continue to bid processors for mobile, space, and airborne applications. If it is determined that FSD should provide special or custom non-mobile systems for the remainder of the market effective controls must be established to cause FSD to first market the SPREAD series wherever possible and to prohibit impact on the commercial line.

3. Standard products will satisfy about 32% of the available military market. Whatever special military processor products are sold, the basic objective should be to further penetrate the ultra-reliable portion of the military market with the SPREAD family.

4. A partial solution to the high reliability required by the military may be obtained through multiprocessing configurations. A concentrated effort in defining over-all systems organizations using the SPREAD family in a multiprocessing mode with interconnection units should be a specific responsibility of each group developing a processor in the SPREAD family.

B. Supporting Considerations

A proposal that IBM should produce a hardened line of SPREAD processors must be measured against Federal Government military procurement procedures and IBM policies.

1. IBM products marketed to the government should be either:

   a. commercially announced

   b. priced on a cost disclosure limited profit basis, but designed to be non-competitive with commercially announced products

   c. created by the addition of cost justifiable elements to commercial units.

2. The SPREAD Group has examined these possibilities and concluded:

   a. It is not feasible to provide a single line of processors which satisfies both the military and commercial markets and is commercially competitive.

   b. It is not technically feasible to provide cost-identifiable additions to the SPREAD family which satisfies the military market.

   c. It is technically feasible, but not desireable to make internal modifications to the SPREAD processors which would satisfy the militarized market.

C. Marketing Factors

The projected FSD 1970 military market for processors is distributed approximately as follows:

	Year-End 1970 Equiv. Points	% of Rev.
Special Systems		
Standard DP	2.3 Millions	14
High Reliability	2.3 - 3.6	14 - 23
Ultra-Reliability	6.8 - 5.5	44 - 35
Environmental Conditions		
Ground to Undersea	2.3	14
Airborne and Space	2.3	14
	16.0	100

The new processor family can meet the standard DP and high reliability market areas. Special military characteristics, not present in the new family, are required to serve the other areas.

VI. IMPLEMENTATION

A. Interdivisional Control

- There are a number of groups developing processor products; these groups reside in four areas - DSD, GPD, FSD, WTC.

- There is no management mechanism short of CMC to control and measure related activities since the present areas report to three group executives.

- It is a fact that the designs of different groups will yield non-consistent products unless the programs are constantly controlled and measured against a standard.

It is apparent that IBM needs centralized design control in our divisionalized business. If we are to achieve a single compatible product line, it is clear that one architectural-engineering design office must guide the processor decisions. It is recommended that the Corporate responsibility for processor architectural and engineering control by established immediately in the DS Division. The responsibility will include approval of program funding, product design objectives, product specifications, etc. In addition, this Corporate Processor Control operation must be organized so as to provide continuous participation in all design decisions to insure the compatibility objectives. Justification for this specific recommendation is based upon the fact that most of the processor types fall under the DS Division product scope.

1. Architecture -- A permanent systems architecture group should be established reporting to the manager of the Corporate Processor Control operation (CPC). It will be comprised of appropriate members from each division implementing the new processors to insure that divisional product objectives are achieved. It will be the responsibility of this group to provide the logical specifications of both hardware and software. It is further recommended that this group be formed immediately and charged with completing design objectives by March 31, 1962.

   It is essential that the architectural activity receive maximum and continual technical input from non-implementing divisions such as FSD, ASDD, Research. To assure this, the non-participating divisions should furnish full-time technical liaison participants to CPC.

2. Arbitration -- Disagreements with the decisions of CPC should be umpired through the normal channels of divisional executive management, Group Staff, Group Executives, and CMC as appropriate.

Executive Control -- As a specific tool for executive control, it is recommended that the individual project managers and the manager of the CPC group will report on the status of all projects on a bi-monthly basis at the General Managers' Meeting.

The Group Staff, as a part of their normal activity, will monitor the progress of the SPREAD Program.

4. Design -- Processor development should be assigned within product scopes, as follows:

- Processor 1 - GPD
- Processor 2 - DSD (WTC Subcontract)
- Processors 3, 4, 5 - DSD

Programming Systems implementation responsibility to be assigned by the CPC group.

5. Product Control Procedure -- Corporate Processor Control concurrence must be built into a single interdivisional Product Control procedure. It is recommended that DSD, GPD, and WTC Product Control managers be immediately charged with the joint establishment of an integral hardware/software product control procedure. It is further recommended that the GPD member act as chairman of this group and that the new procedure be completed and approved by March 31, 1962.

The Special Engineering groups of DSD, GPD, and WTC must establish the controls and procedures required to assure rapid and consistent response on a world-wide basis to customer RPQ's.

6. Standards

a. Logical Structure -- The implementing group will concur with the logical specifications manual and changes thereto.

b. Programming -- A programming standards group working under CPC chairmanship will prepare a formal programming standards manual for the new processor family. This manual will include documentation, release, format and maintenance standards.

c. Engineering

1) An engineering standards working committee representing the implementing divisions will be established under the

the chairmanship of CPC. A formal engineering standards manual will be prepared to control engineering implementation and release to domestic plants from WTC laboratories and vice versa.

2) The implementing group is to be responsible for the implementation of the system within the terms of the logical specifications, engineering and programming standards manuals.

7. Program Management

a. The implementing groups will be responsible for establishing a project schedule in PERT form to be approved by CPC. CPC is to coordinate and maintain a single PERT net for the complete product line.

b. Program Phase changes shall be with CPC approval.

8. Marketing Requirements (Product Planning)

a. DSD is to be responsible for consolidating the system configuration, performance and feature requirements of the world market for Processors #2, 3, 4, and 5. GPD has this responsibility for Processor #1.

b. Product objectives and specifications will be written by the implementing groups for approval by CPC.

c. The implementing group will be responsible for scheduling market forecasts and writing forecast assumptions which will have approval by CPC before dissemination.

d. WTC, GPD, and DSD will forecast their respective market areas.

B. Technical Development

Certain imperative technical developments are required of the following groups:

1. The Corporate Memory Group must develop non-mechanical main memories in the 32 to 500 kilobit capacity at a cost 1/10 to 1/2 that presently attainable, with cycle times up to 50 microseconds.

2. The Corporate Memory Group must also develop auxiliary memories for each performance range of main memories as follows:

   a. internal memories of 3-512 words with cycle times 1/4 to 1/10 those of main memory.

   b. read-only memories for control use with capabilities of 2-250 kilobits and cycle times 1/4 to 1/10 of main memory.

3. The Corporate File Group must develop binary-addressed versions of all planned random access files.

4. The Corporate Tape Group must develop tape devices renting for less than $200/month and operating at no less than 5,000 characters/second.

5. DSD Technical Development must develop a crosspoint switch or time-multiplex system for switching I/O devices among channels.

6. Group Staff, aided by divisional system analysis groups must develop machine-organization-independent techniques to measure (a) the internal processor performance, (b) the system throughput on scientific, data processing, and mixed applications and (c) programming systems efficiency. Separate techniques for utmost precision of measurement and for quick measurement are needed.

C. Programming

1. Complete programming compatibility is sufficiently important for the 1965 - 1970 period to warrant an aggressive advanced programming effort within the Product Divisions. Such an effort is immediately required to product configuration-independent programming.

2. The following plan should be implemented relative to procedure languages:

   a. Provide both Fortran and COBOL with the first introduction of the family to assist transition.

   b. Immediately initiate an effort to design a unified language for handling scientific, commercial, and information handling applications.

D. Marketing

The new family encompasses two major responsibilities:

- New market growth must be accomplished to assure IBM growth.
- Impact must be controlled to achieve revenue and profit objectives.

These responsibilities require a plan of action executed concurrently with processor development. The plan must:

- Direct processors to new industry applications.
- Direct processors to existing market gaps.
- Incorporate existing processors as subsystems to the new family whenever applicable.

1. Relation to New Processor Family

The following major steps will be taken:

a. Each marketing organization (DPD, WTC and FSD) and ASDD will appoint a manager responsible to coordinate and supervise proper execution of an application development program for the new processor family.

b. These marketing managers will cooperatively prepare a set of application development ground rules to achieve maximum use of compatibility and features of the new family. This should be accomplished by June 30, 1962.

c. This group will identify industry areas requiring the new family characteristics, and the market potential of each area.

d. A coordinated marketing divisions plan will be established and funded to define and produce applications packages necessary to sell new customers, and to extend processor utilization for industry areas of high potential. The plan should be defined and the implementation programs established commensurate with planned announcements and installations.

e. This market development group will coordinate their work with CPC.

2. Relation to Existing Processor Family

In order to fully exploit the application potential of the new line, it will be necessary to supplement the current processor line with selected special engineering features analogous to the new family. This will prepare the market for the concepts of the new processor family.

E. World Market Considerations

The growth projection for WT indicates a very rapid increase in the processor market for the 1961 - 1970 period. (Approximately 37% of world market for processors in 1970, compared with 12% in 1961). This market and its characteristics must influence all aspects of the development of the new processor family.

In particular, the following present procedures must be revised:

1. Pricing -- each element of the new line should be priced on its combined world market forecast and the combined WTC domestic division expenses.

2. Installation Requirements -- installation and environmental criteria must be suitable for domestic and world conditions.

3. Patents -- WTC and domestic patent operations must be more closely coordinated to ensure that all disclosures receive a single consistent evaluation for US and foreign filing.

4. Manufacturing and Product Engineering -- to facilitate the simultaneous release of a product to US and WT plants: (a) the current WTC, DSD, GPD release formats must be reconciled into a single corporate procedure, (b) a corporate design automation procedure must be established and maintained.

F. Introduction Planning

1. Announcement

The announcement plan will undoubtedly dictate one or more systems being introduced prior to the smallest. It is imperative that the ability to produce the smallest processor be established prior to irrevocably committing the series. It is the conclusion of the SPREAD task group that no system announcement take place until the smallest processor has reached the "A" test entry level. Recognizing that the compatibility decision poses a major problem, it is recommended that the product divisions exert a major effort to carry all processor designs through at least a Phase I level prior to the earliest announcement.

Further, to insure adherence to the compatibility objectives, it is the group's best judgment that announcement of the first entries be planned for 1 Q 64 to permit adequate testing of two or more processors in the range. A firm date should be set following a detailed analysis of a PERT schedule for Processors #1, 2 and 5.

2. Presently Planned Processors

With regard to planned products, SPREAD recommends:

a. That the L^2C development be directed to adhere to the SPREAD architectural ground rules. (It is recognized that this unit may not be economically achievable under SPREAD rules. However, it is recommended that the charge be established until it is positively proven that achievement is not possible.)

b. That 14LC announcement proceed as planned.

c. That 1410X development continue as planned.

d. Since the 7034 would occupy part of the market for which Processor #5 is intended, it should not be announced unless it yields a superior profitability over waiting for Processor #5.

3. Announcement Timing

A great deal of additional information is required to set the precise phase-in plan. Chart X indicates the earliest desirable announcement based on forecasted sales decline and the latest desirable announcement based on declining installations. Recognizing that existing product life extensions are possible, and required in some cases, it is recommended that the responsible divisions establish the processor entry plan.

G. Security

Information requiring protection is as follows:

1. The decision to develop a compatible line.

2. Time table for introduction of, and designation of, the types of processors to comprise the family.

3. Ground rules for compatibility.

4. Instruction set of the family.

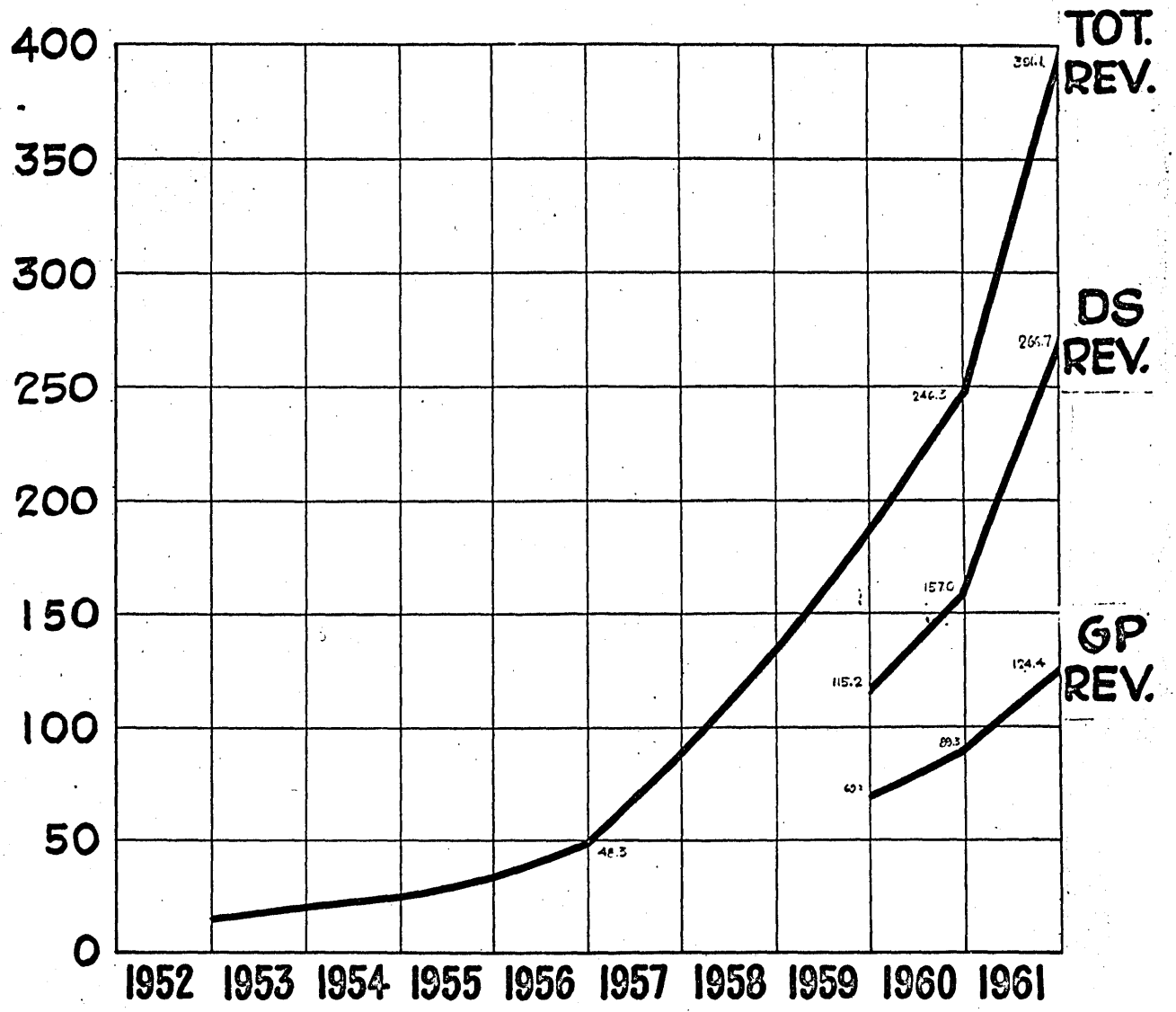
Item 1 must be maintained as company confidential and all documents containing items 2, 3, and 4, must be registered company confidential.

VII. CHARTS

PROCESSOR REVENUE

DOLLARS IN MILLIONS

CHART I



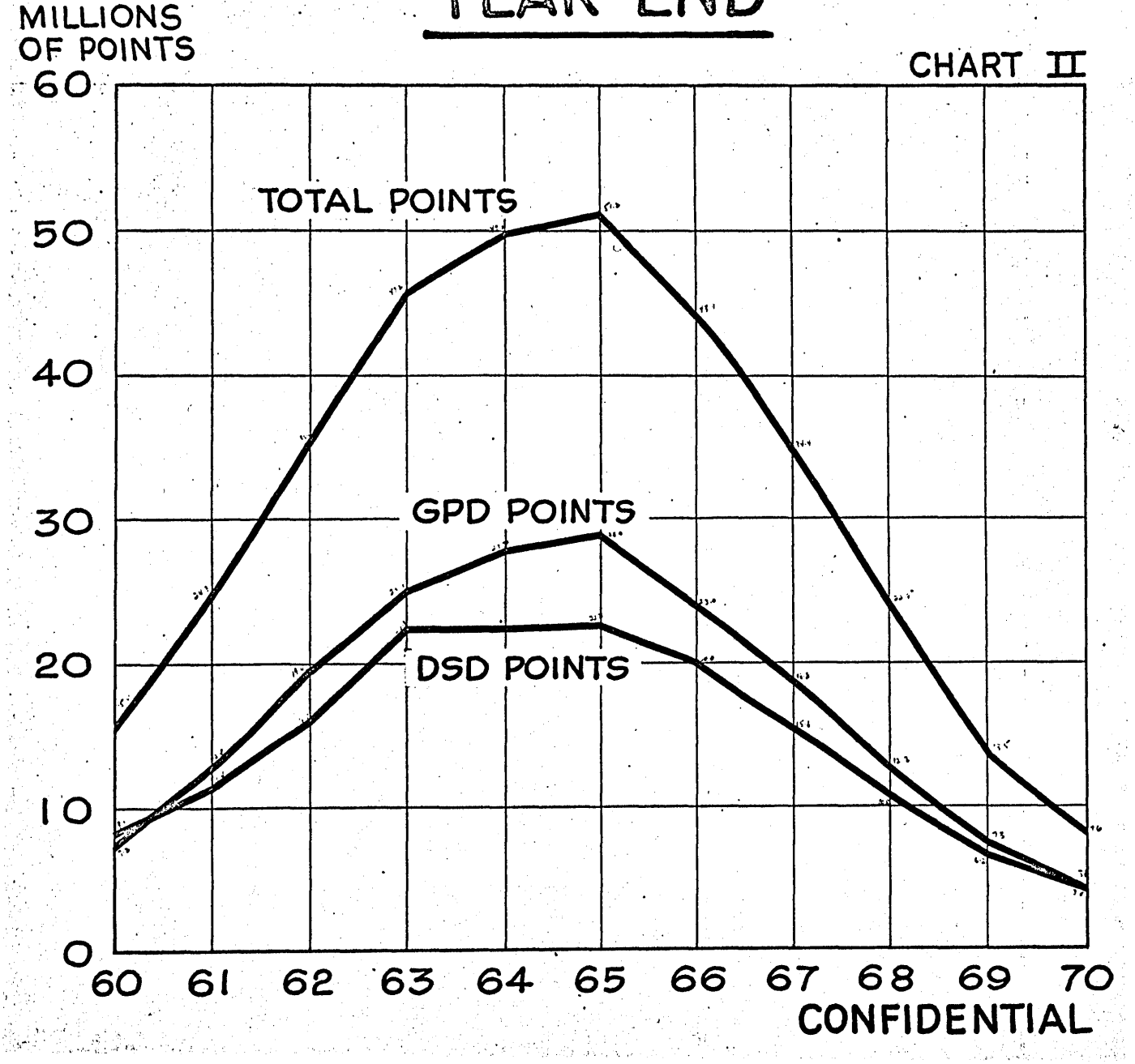
EDP 1ST DELIVERY DATES		701-FEB 607-OCT	650 CARD - DEC	702-FEB 704-DEC	7051-JAN 650-TAPE -DEC	305-NOV	709-AUG	7051I-MAY 7090-NOV.	7070-JUN. 1401-SEP. 1620-OCT.	7080-AUG 7074-NOV. 1410-NOV.

CONFIDENTIAL

DOMESTIC FIRM PRODUCT BASE

PROCESSOR POINTS INSTALLED

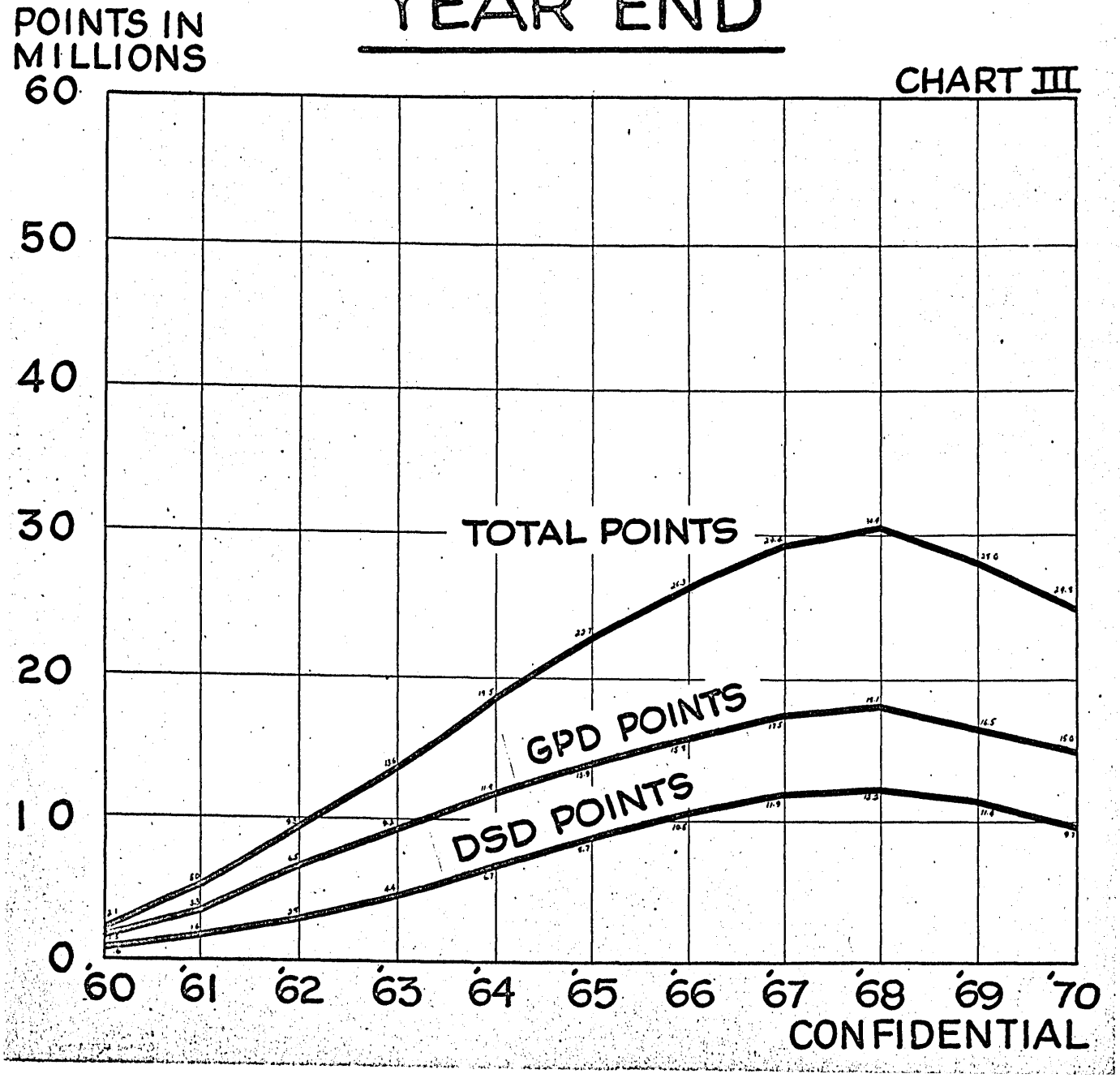
YEAR END



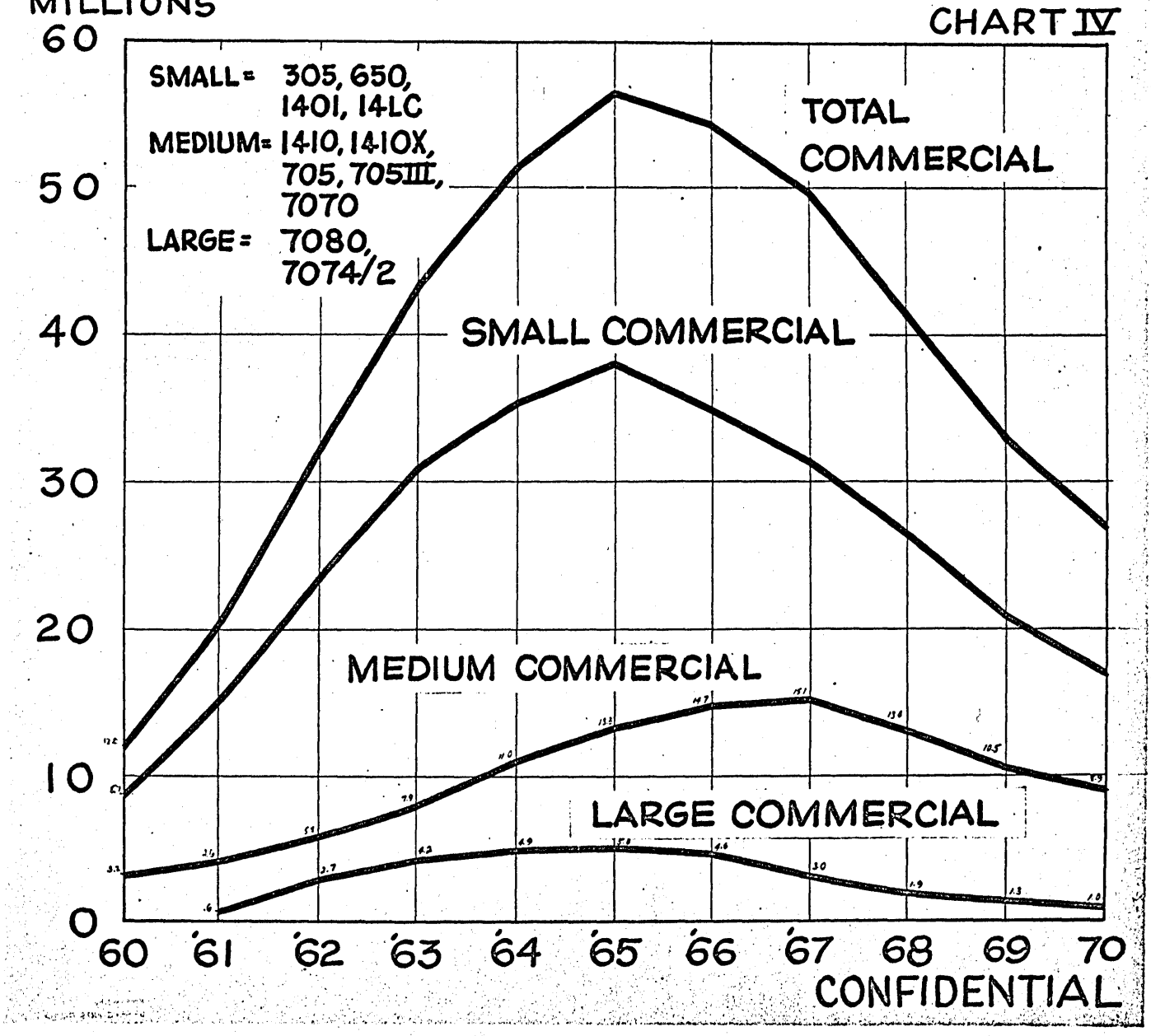
WTC FIRM PRODUCT BASE

PROCESSOR POINTS INSTALLED

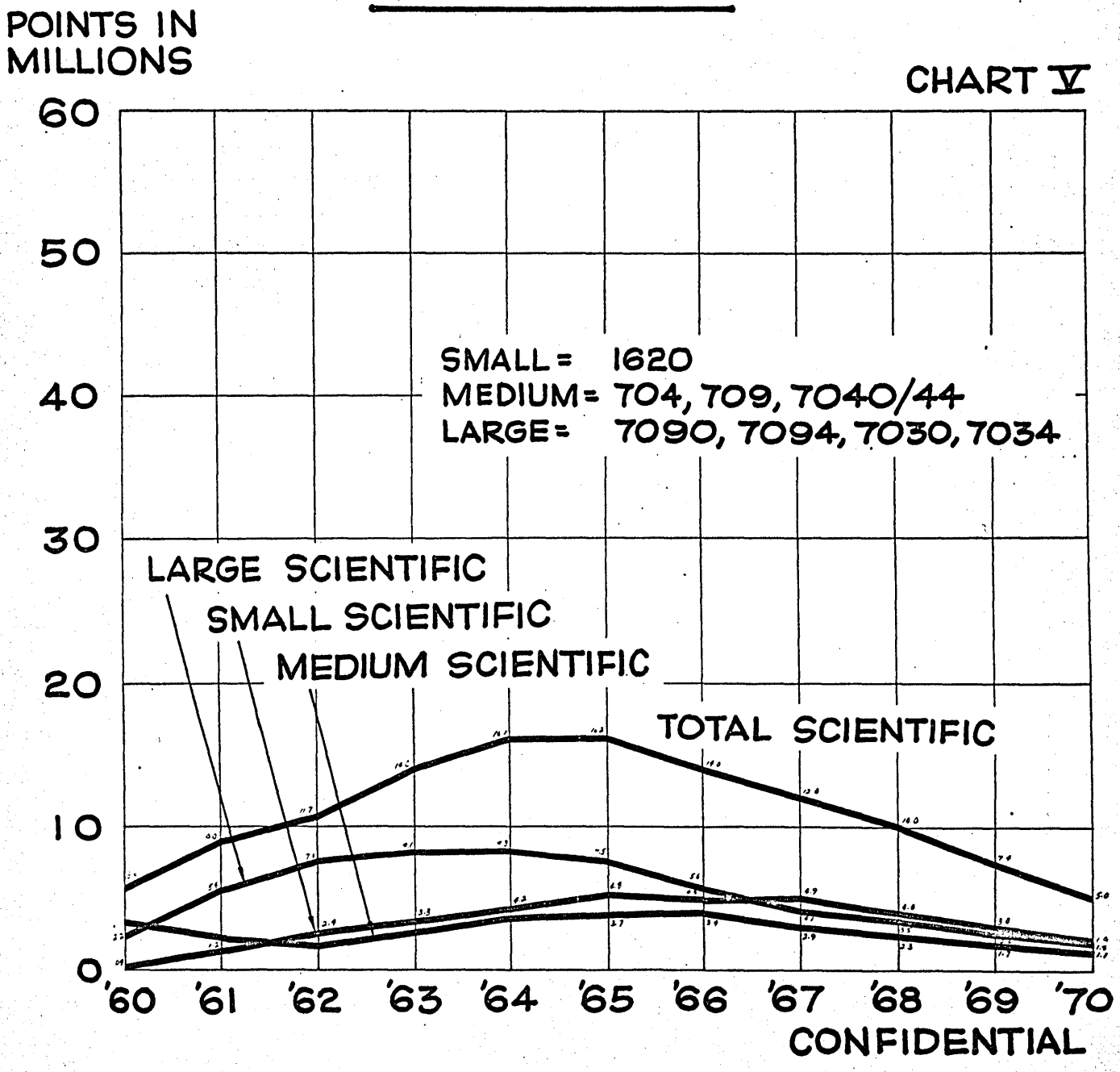
YEAR END



COMMERCIAL SYSTEMS
PROCESSOR POINTS INSTALLED
YEAR END



SCIENTIFIC SYSTEMS
PROCESSOR POINTS INSTALLED
YEAR END

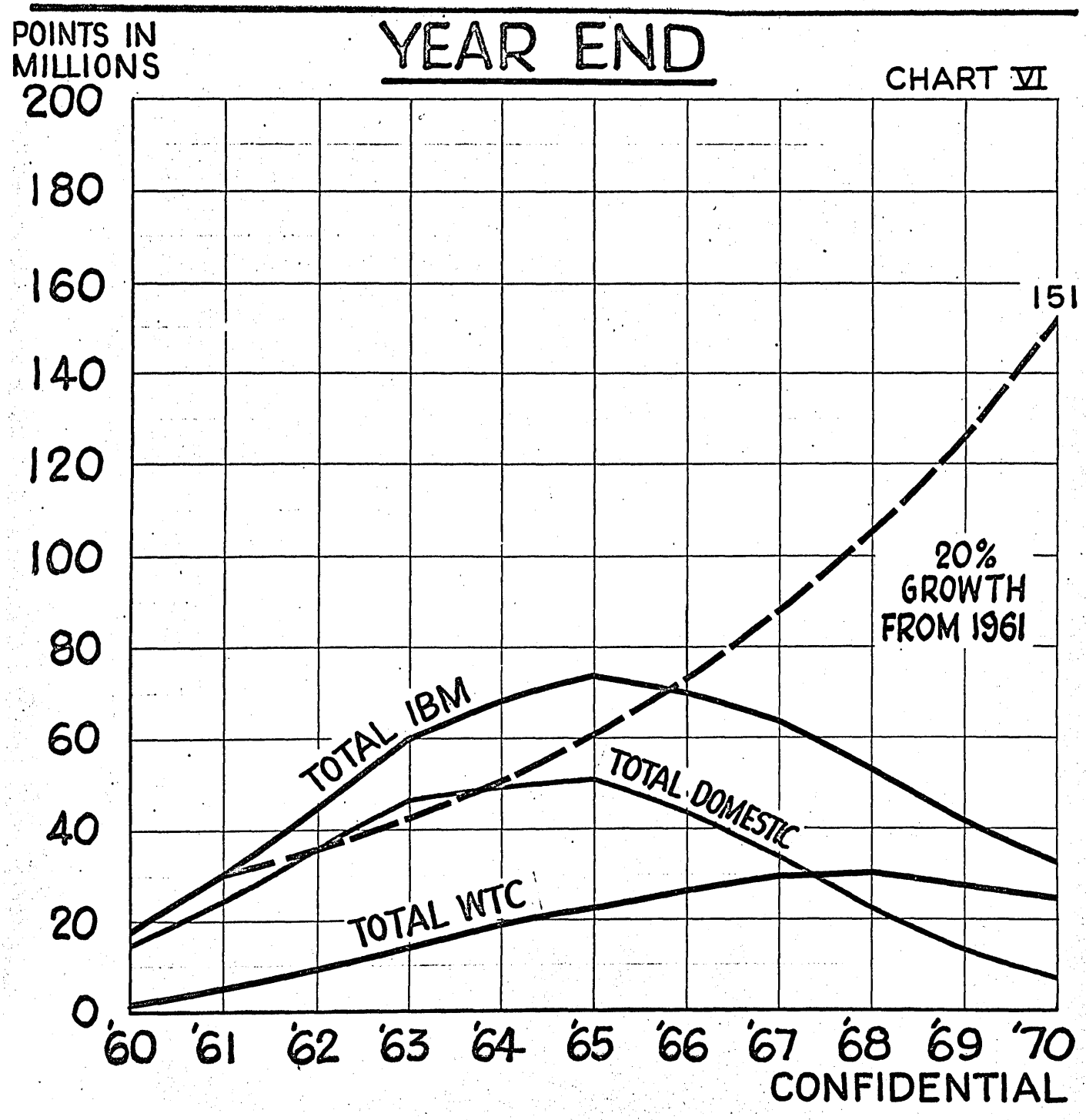


TOTAL IBM FIRM PRODUCT BASE

PROCESSOR POINTS INSTALLED

YEAR END

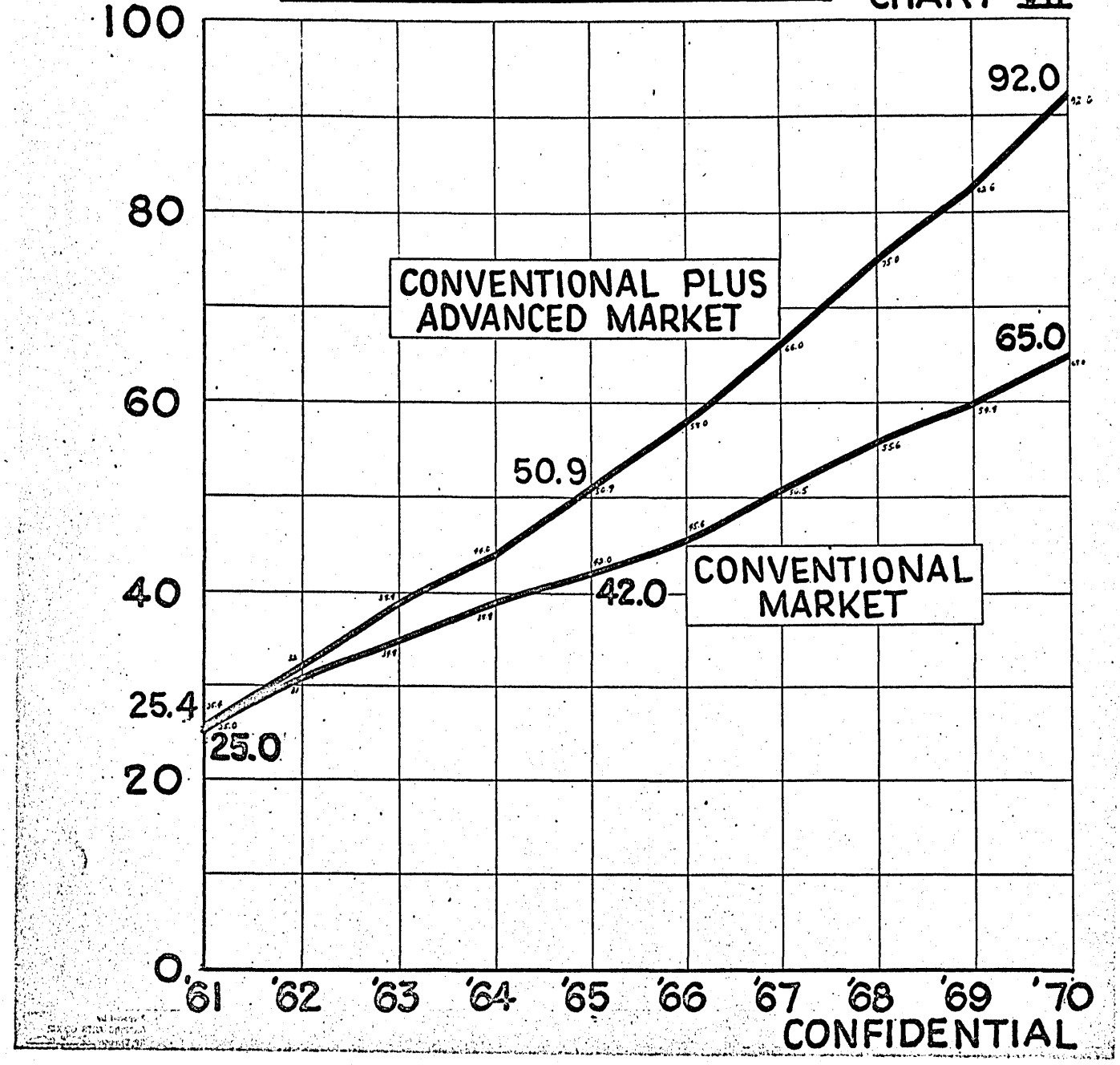
CHART VI



CONFIDENTIAL

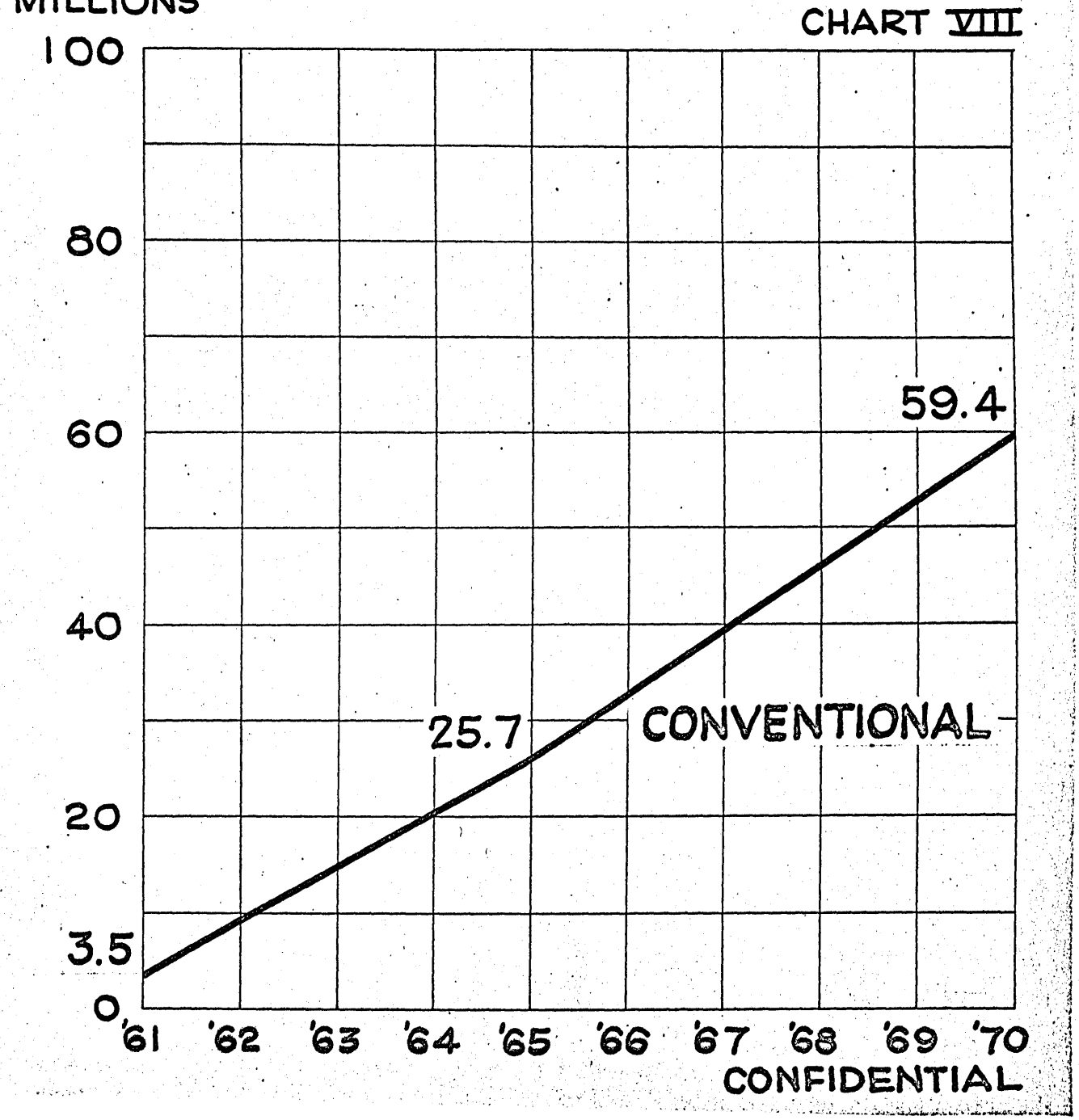
GP-DS FORECAST
PROCESSOR POINTS INSTALLED
YEAR END
DOMESTIC ONLY

CHART VII



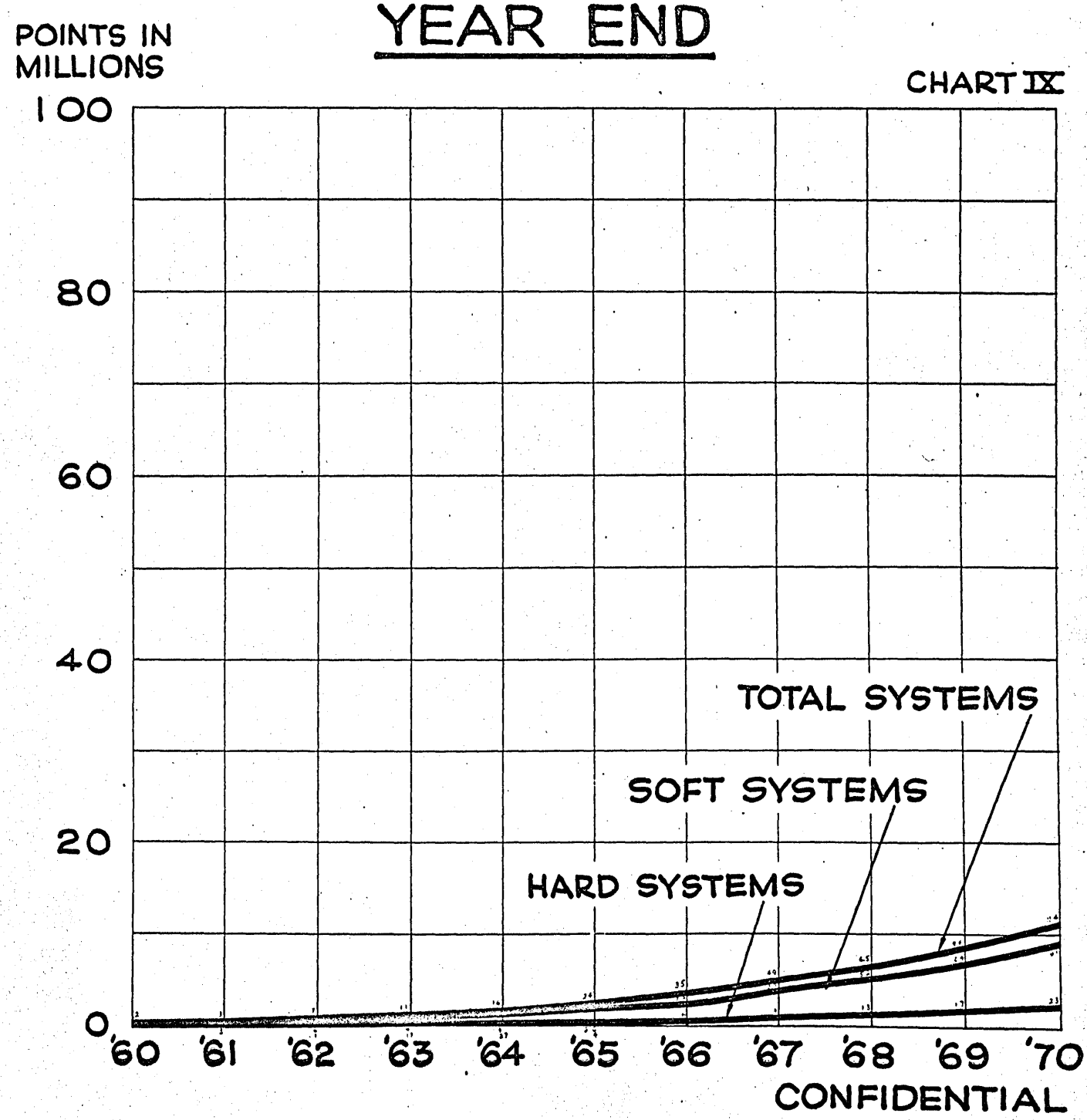
CONFIDENTIAL

WTC FORECAST
PROCESSOR POINTS INSTALLED
YEAR END



FSD SPECIAL SYSTEM FORECAST
PROCESSOR POINTS INSTALLED
YEAR END

CHART IX

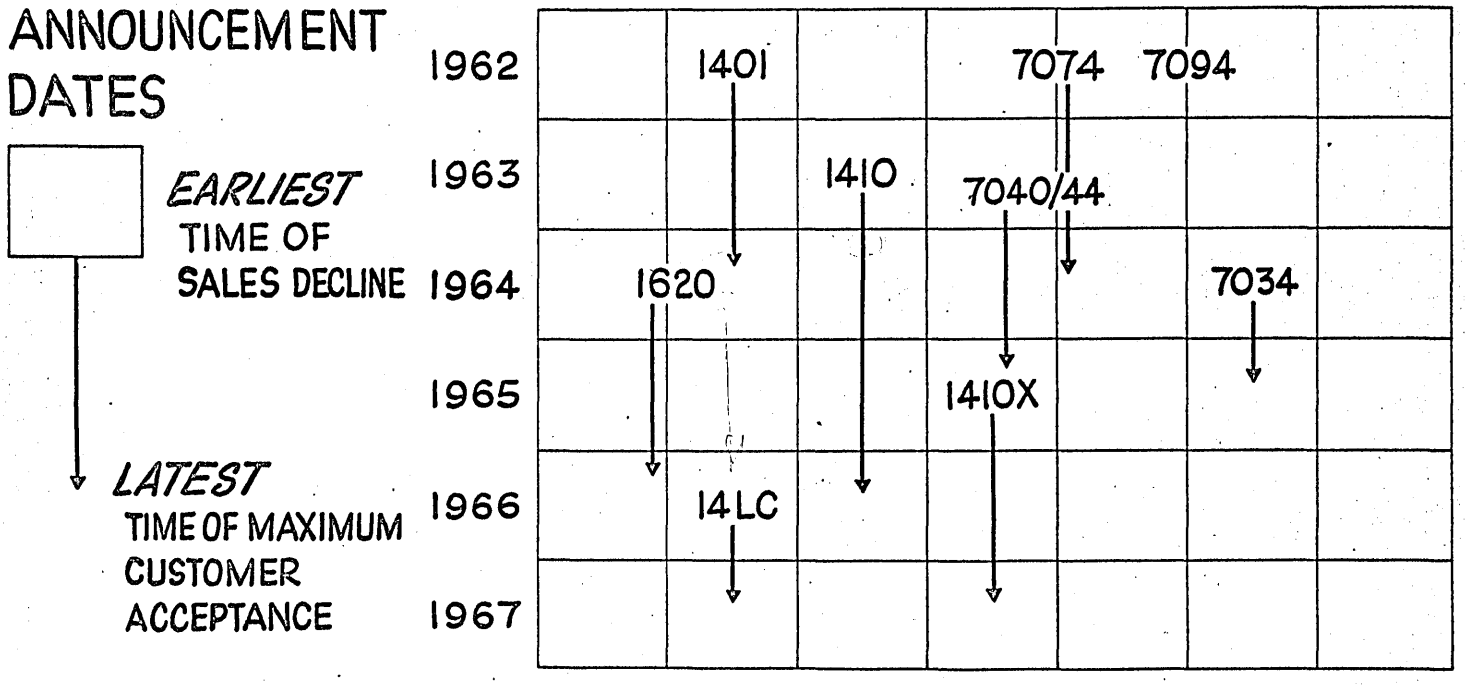


CONFIDENTIAL

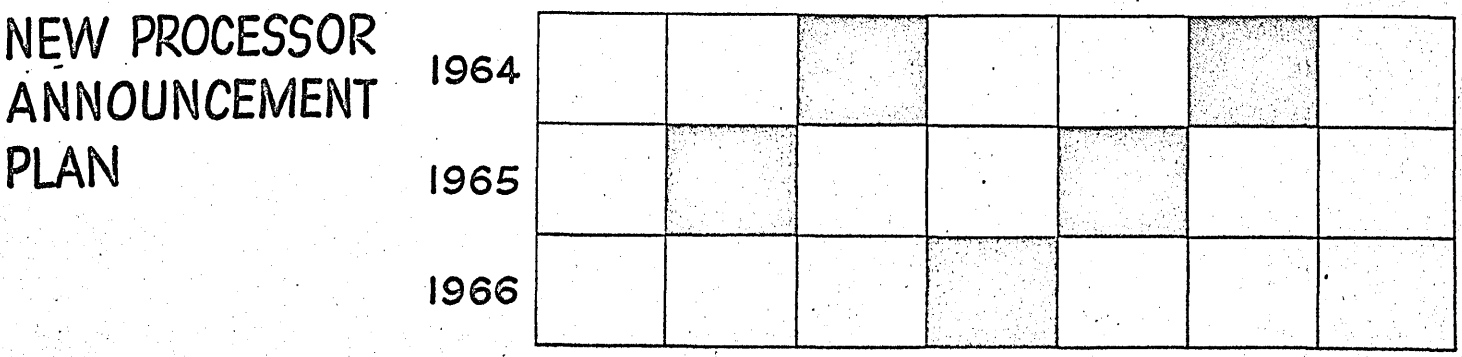
INTRODUCTION TIMING

CHART X

PROCESSOR LINE	VERY SMALL	1	2	3	4	5	VERY LARGE
2 ADDRESS ADD TIME 5 DIGITS μ SEC.		200 μS	75	25	5	1.0	



SUCCESSOR ANN'C'T OVERDUE							
			7070	7080 7090		7030	
ANN'C'T PLANNED 1962		14LC 2Q		1410X 3Q		7034 4Q	



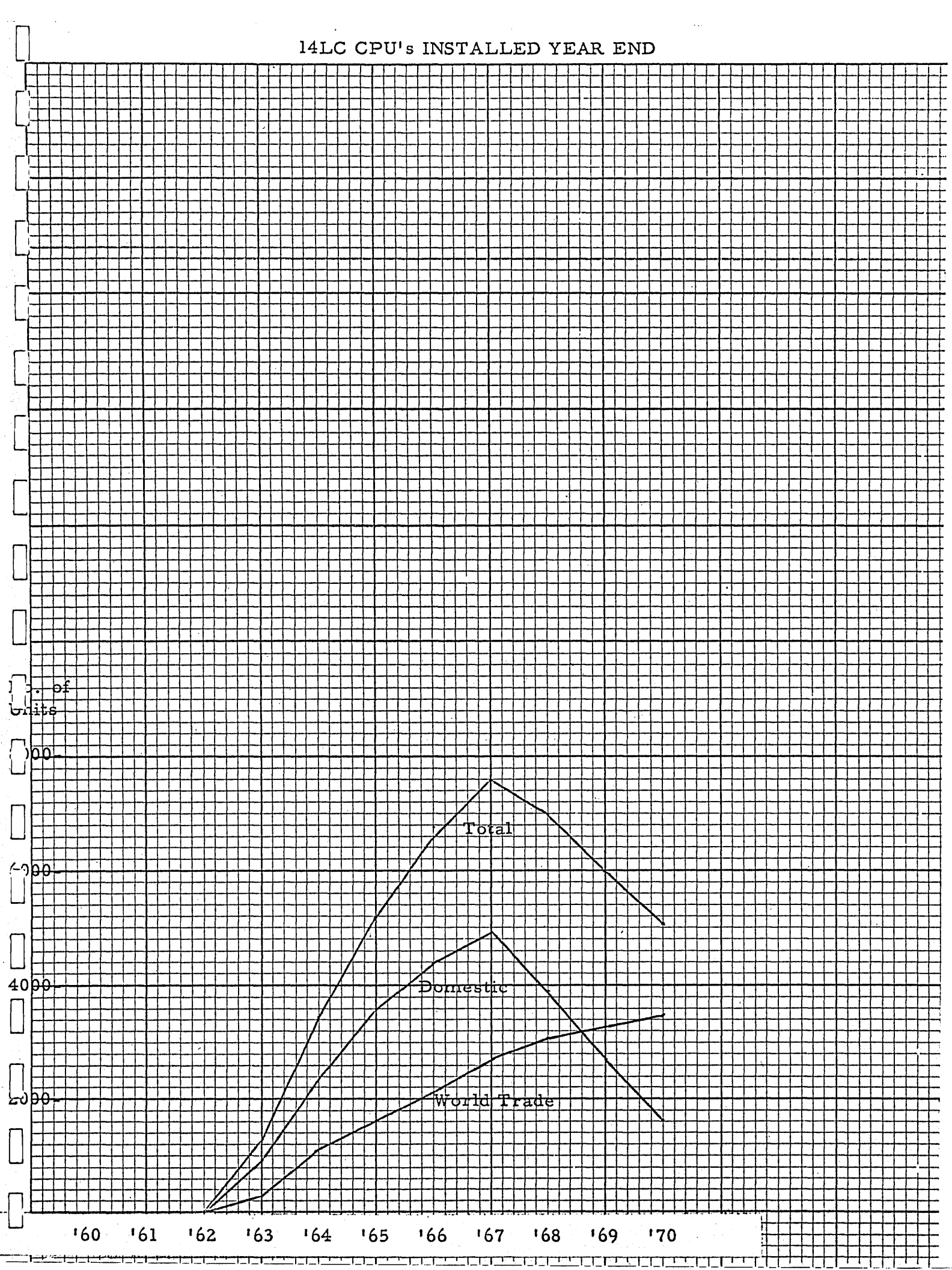
VIII. APPENDIX

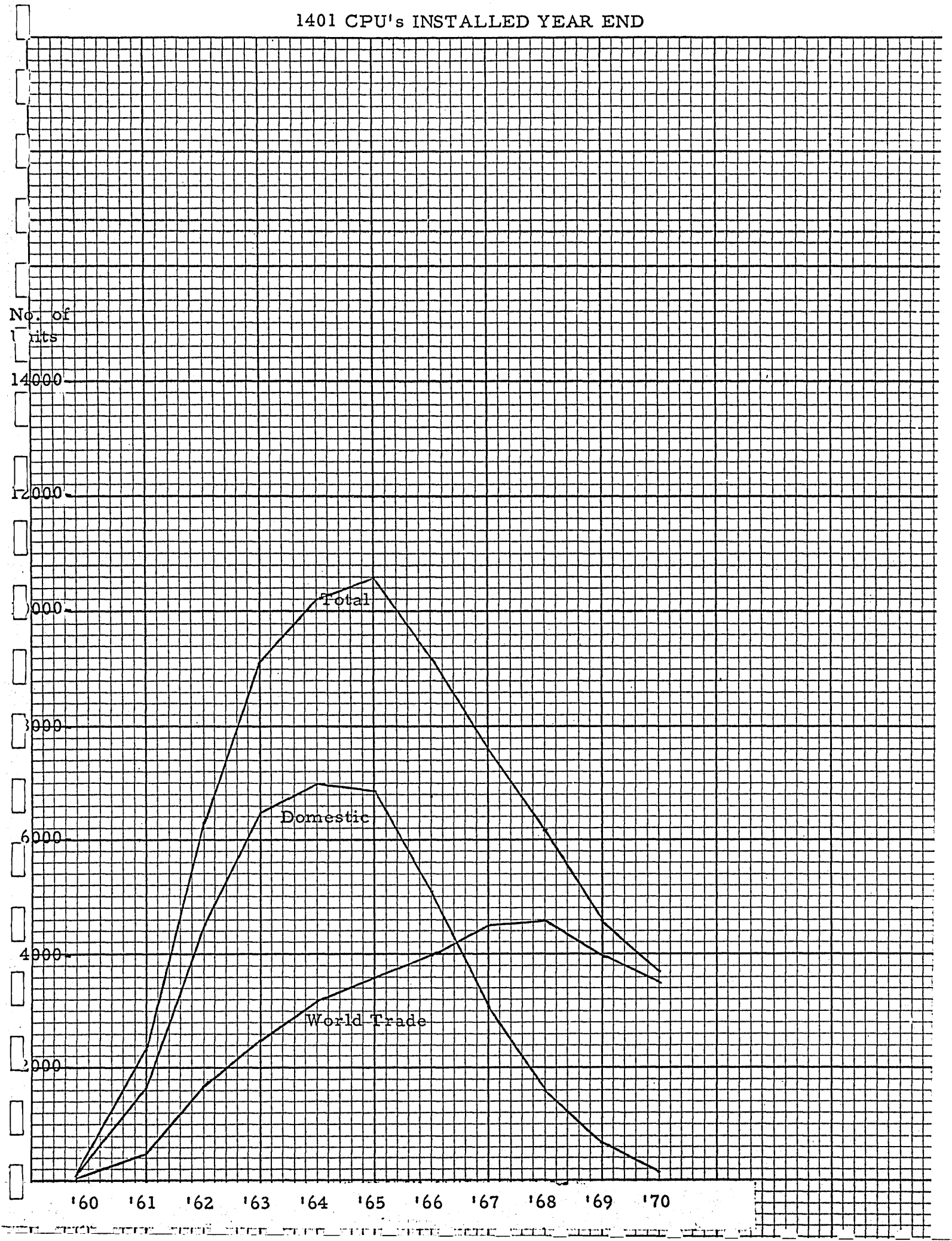
A. Product Survival Charts

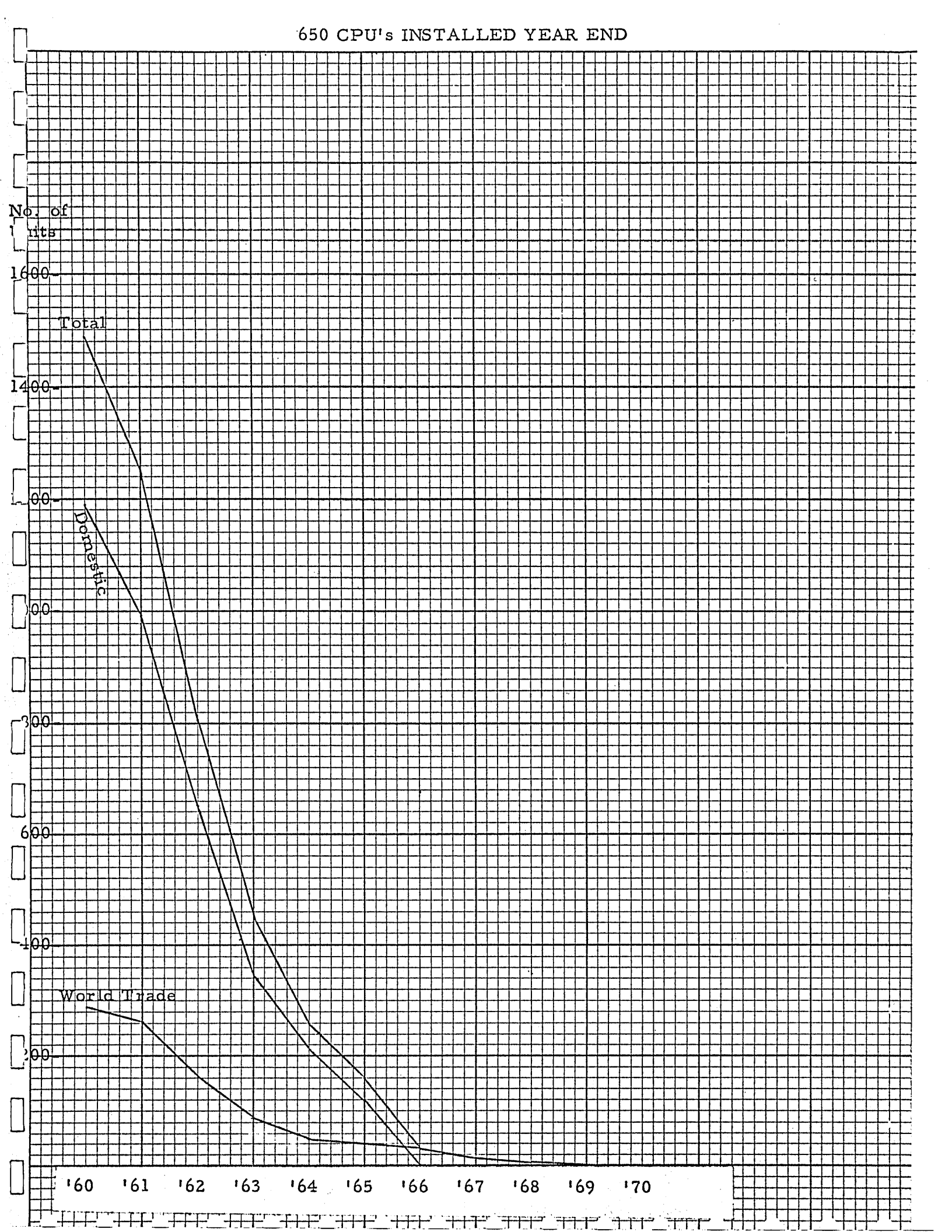
The following product survival charts cover the firm base products. The numbers of these "firm base" processors installed have been multiplied by the forecasted average processor rental points to establish a year-end points installed estimate.

These installed point figures show the net of both lease and purchase points expressed in terms of single shift monthly rental dollars. The average processor rental points used are as follows:

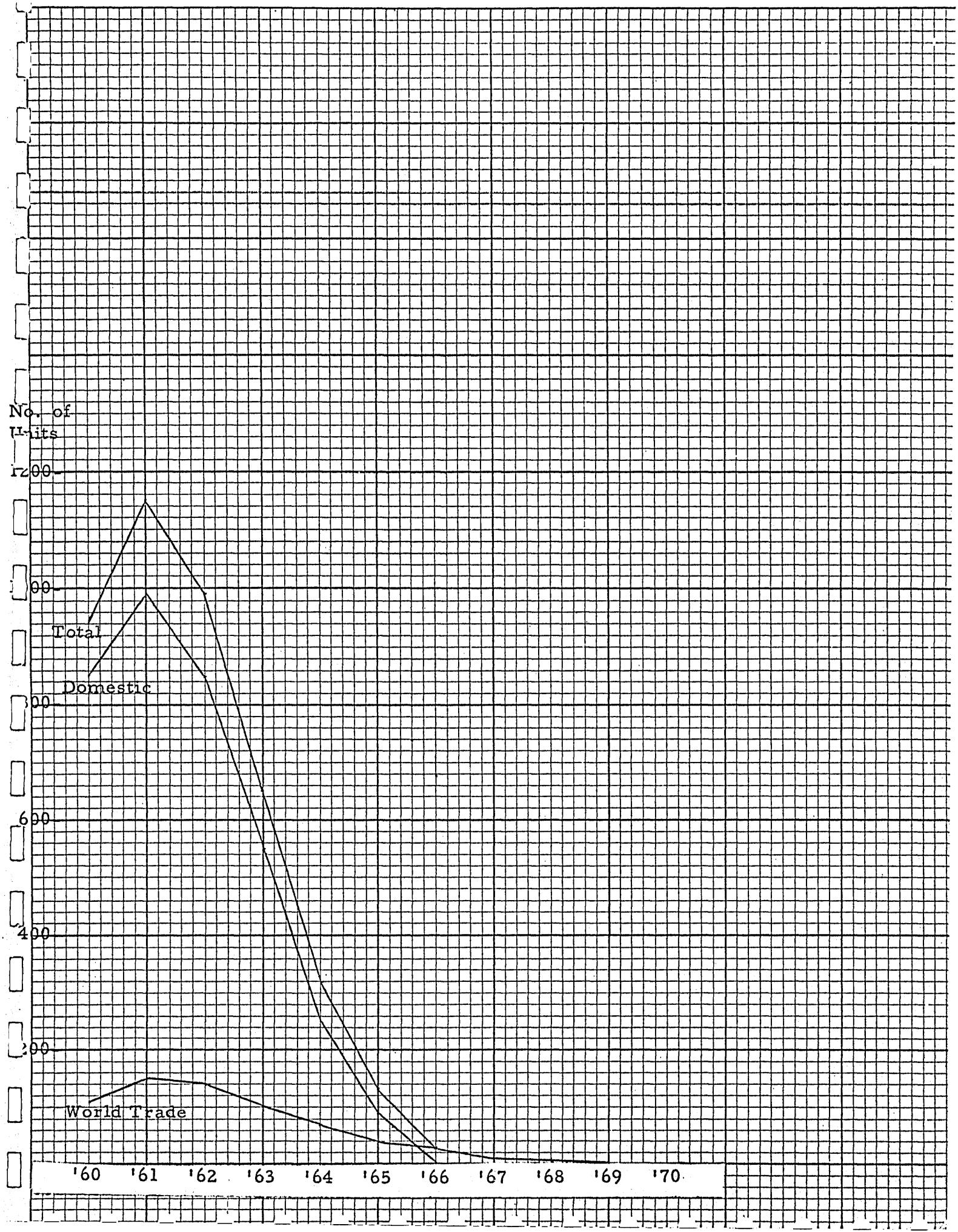
	Processor	Average Rental Points
GPD:	14LC	1,225
	1401	2,875
	650	4,200
	305	1,800
	1620	1,675
DSD:	1410	4,700
	1410X	14,100
	7070	10,100
	7072/74	16,600
	704	28,700
	709	33,000
	7040/44	11,300
	7090/94	45,800
	705	17,200
	705 III	20,200
	7080	28,900
	7030	95,800
	7034	115,000

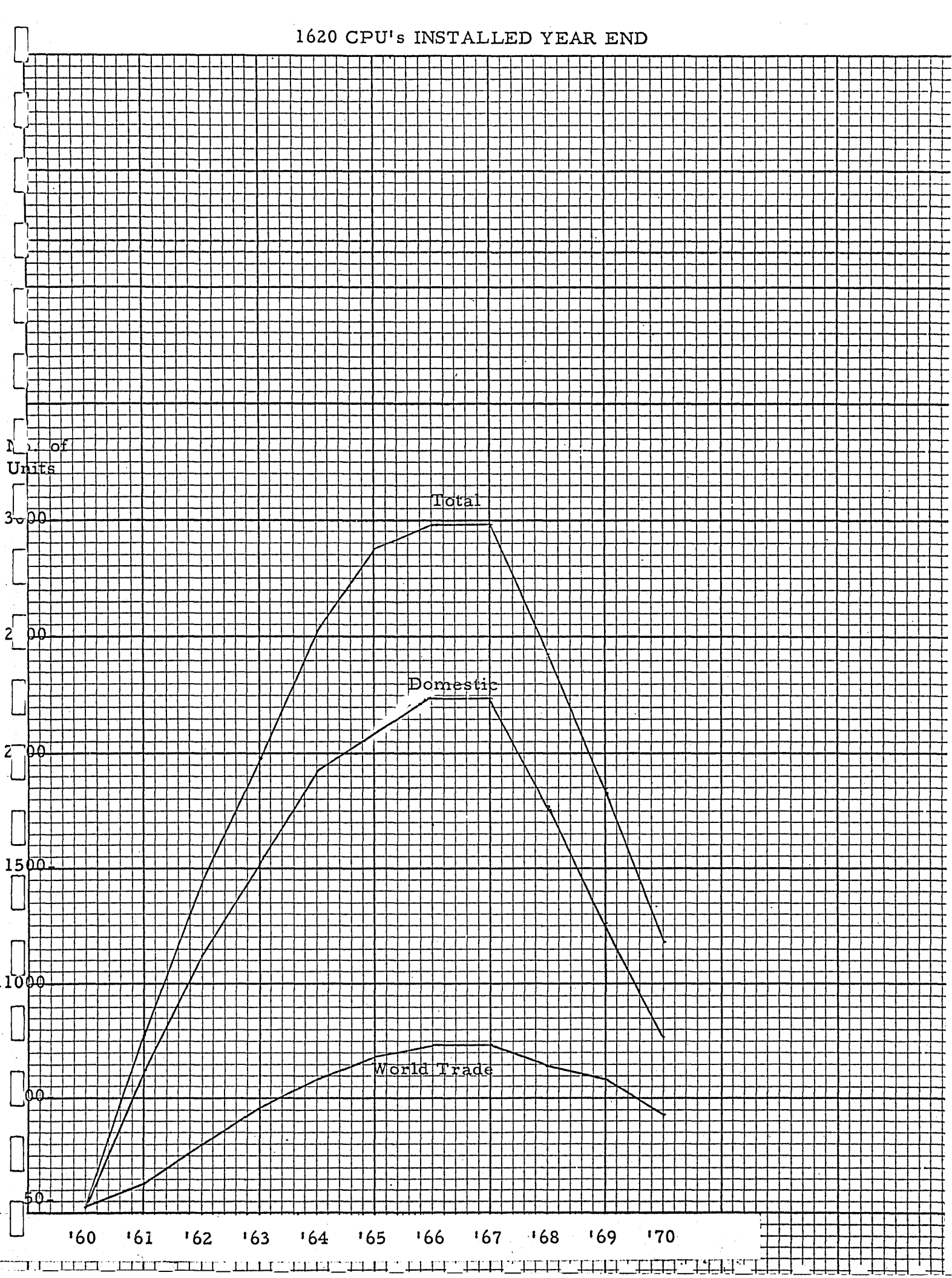

14LC CPU's INSTALLED YEAR END
. of
nits
00
000
4000
000
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

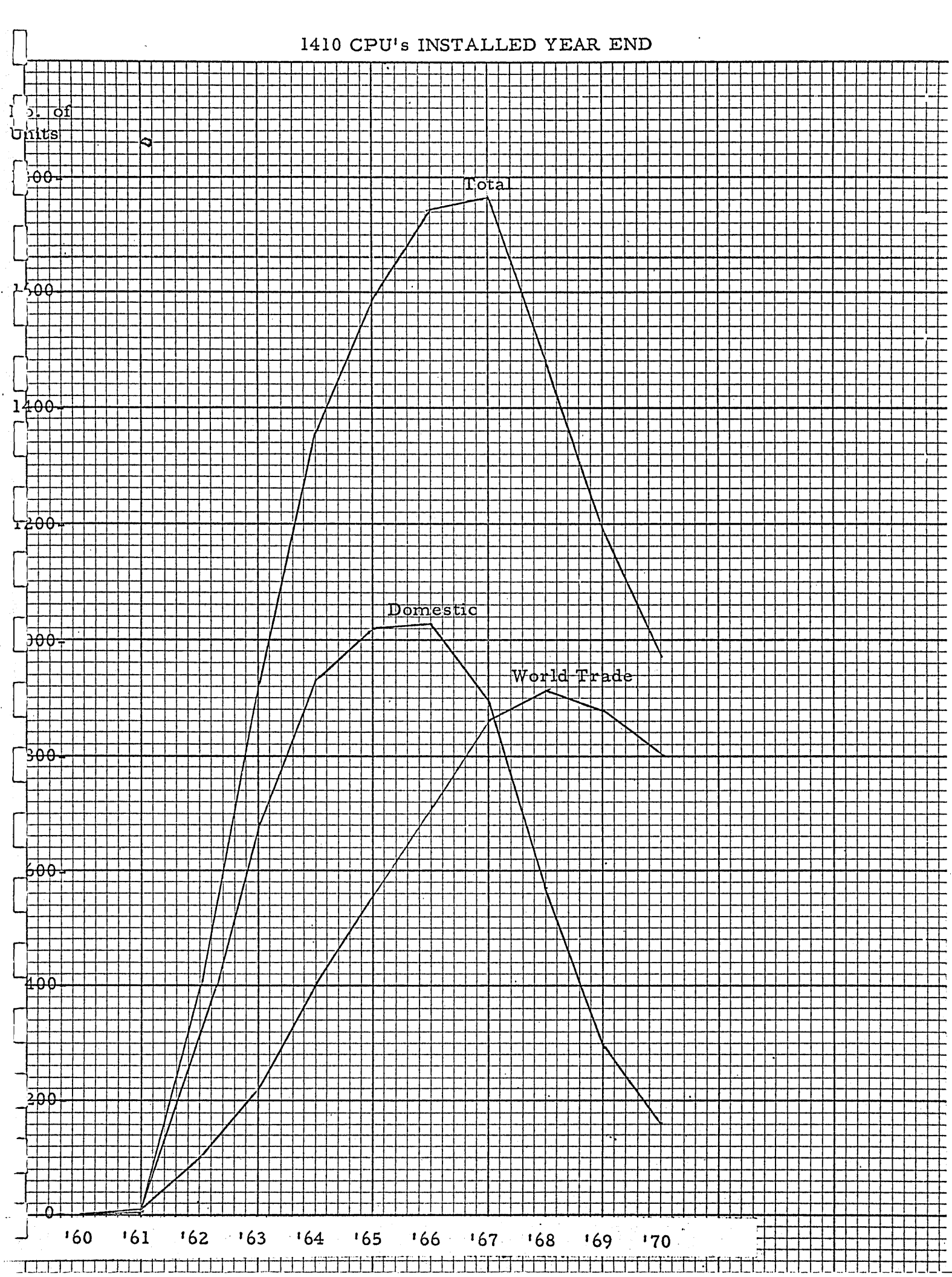

1401 CPU's INSTALLED YEAR END
No. of
Units
14000
12000
Total
Domestic
6000
4000
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

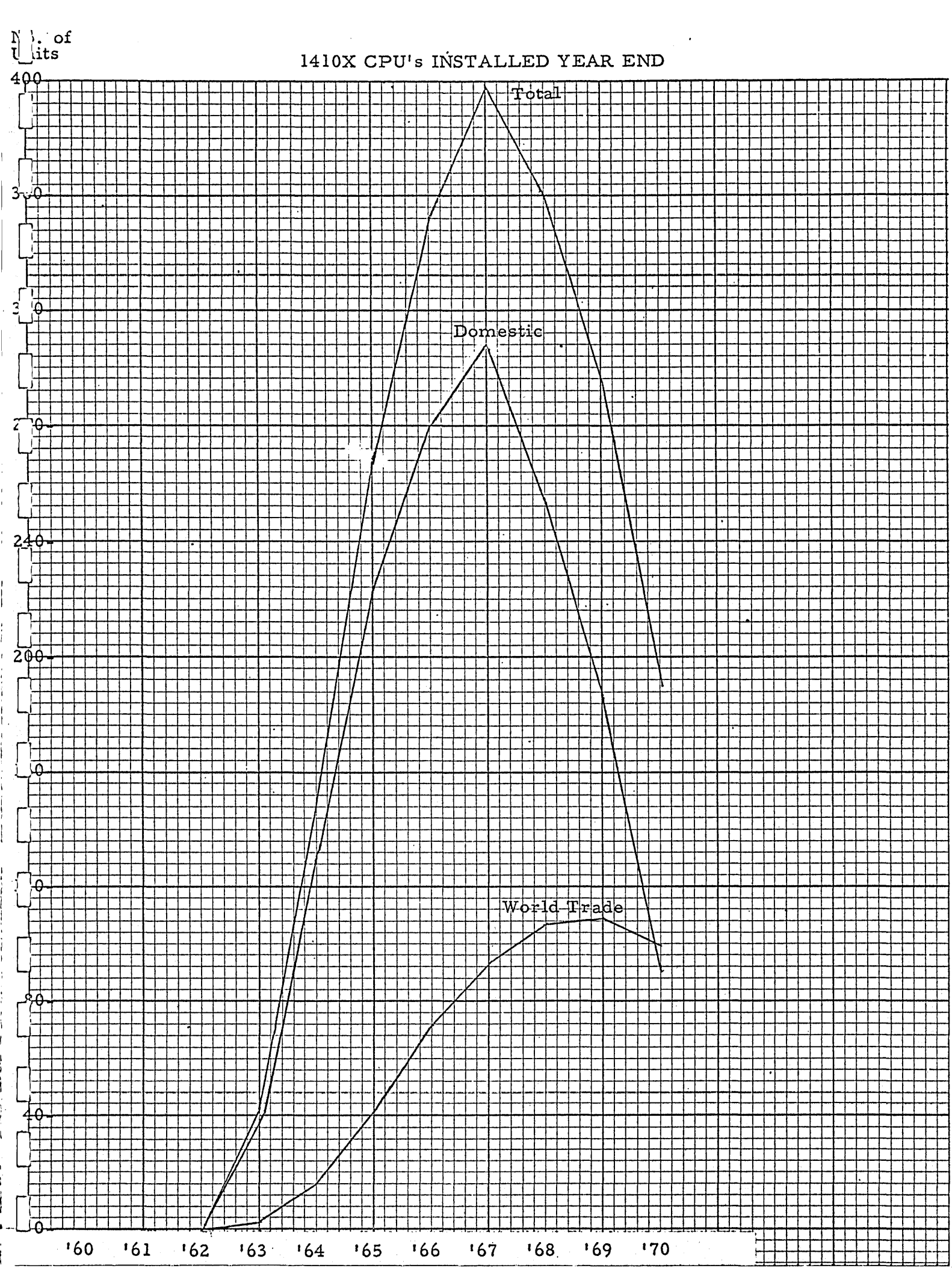

650 CPU's INSTALLED YEAR END
No. of
nits
1600
Total
1400
00
Domestic
00
300
600
400
World Trade
200
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

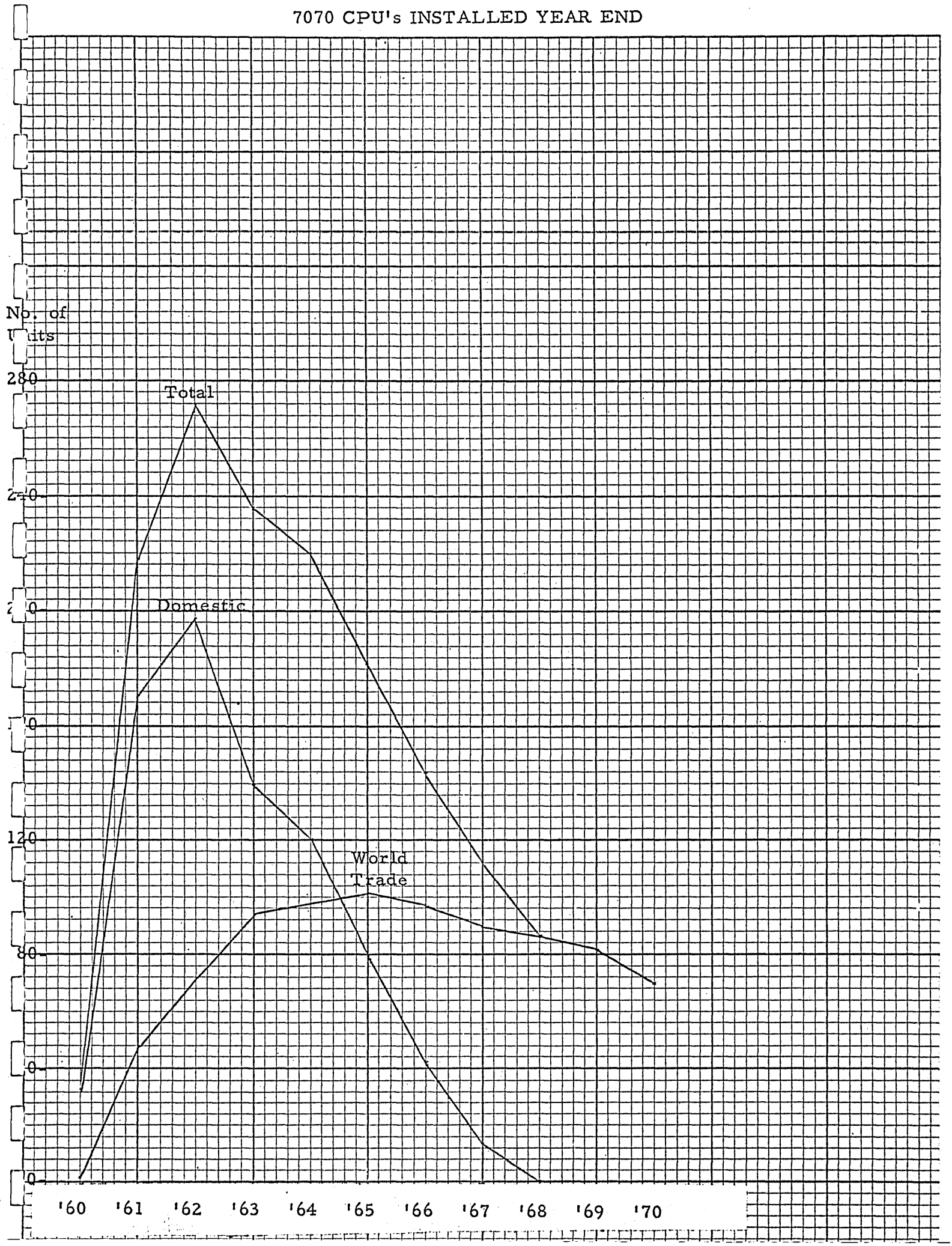
305 CPU's INSTALLED YEAR END

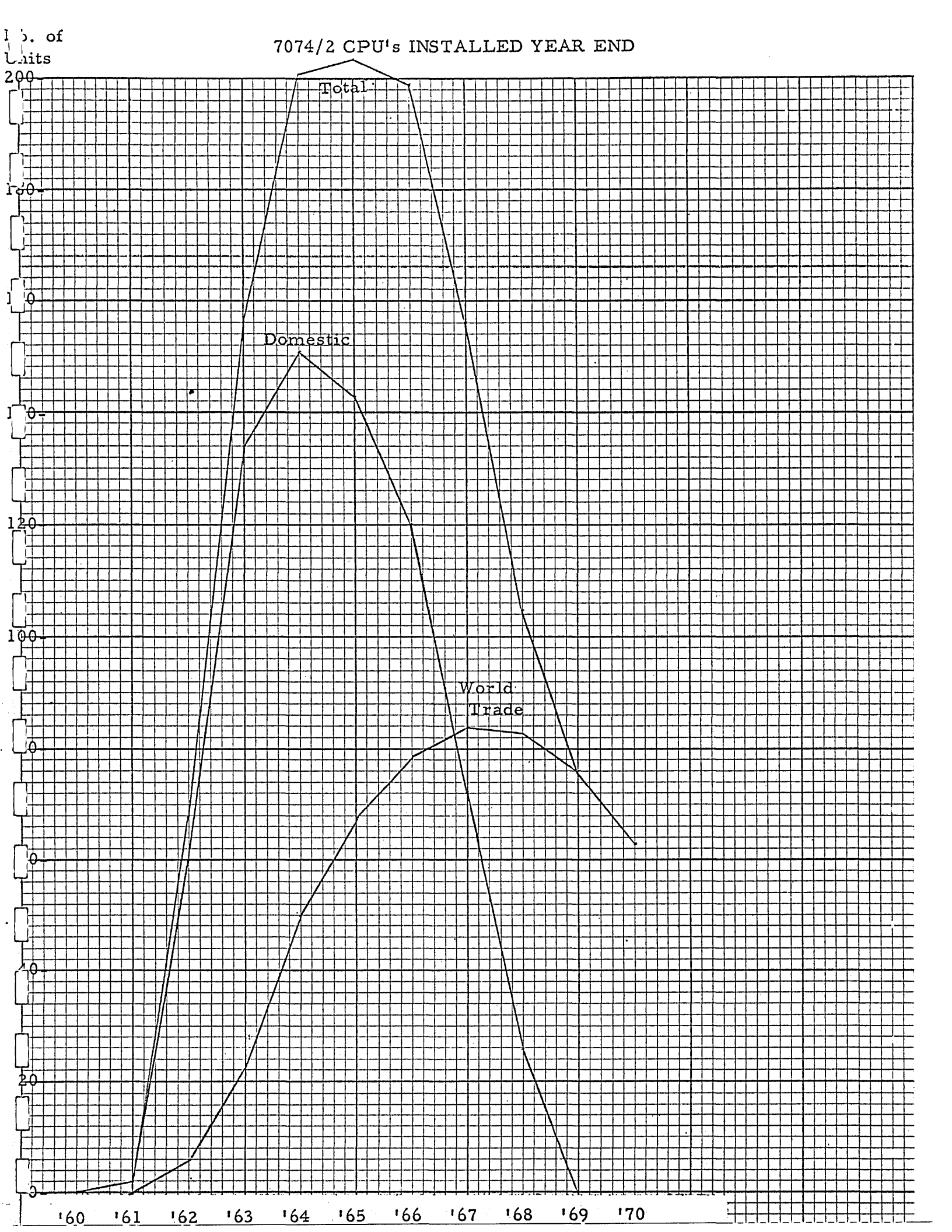


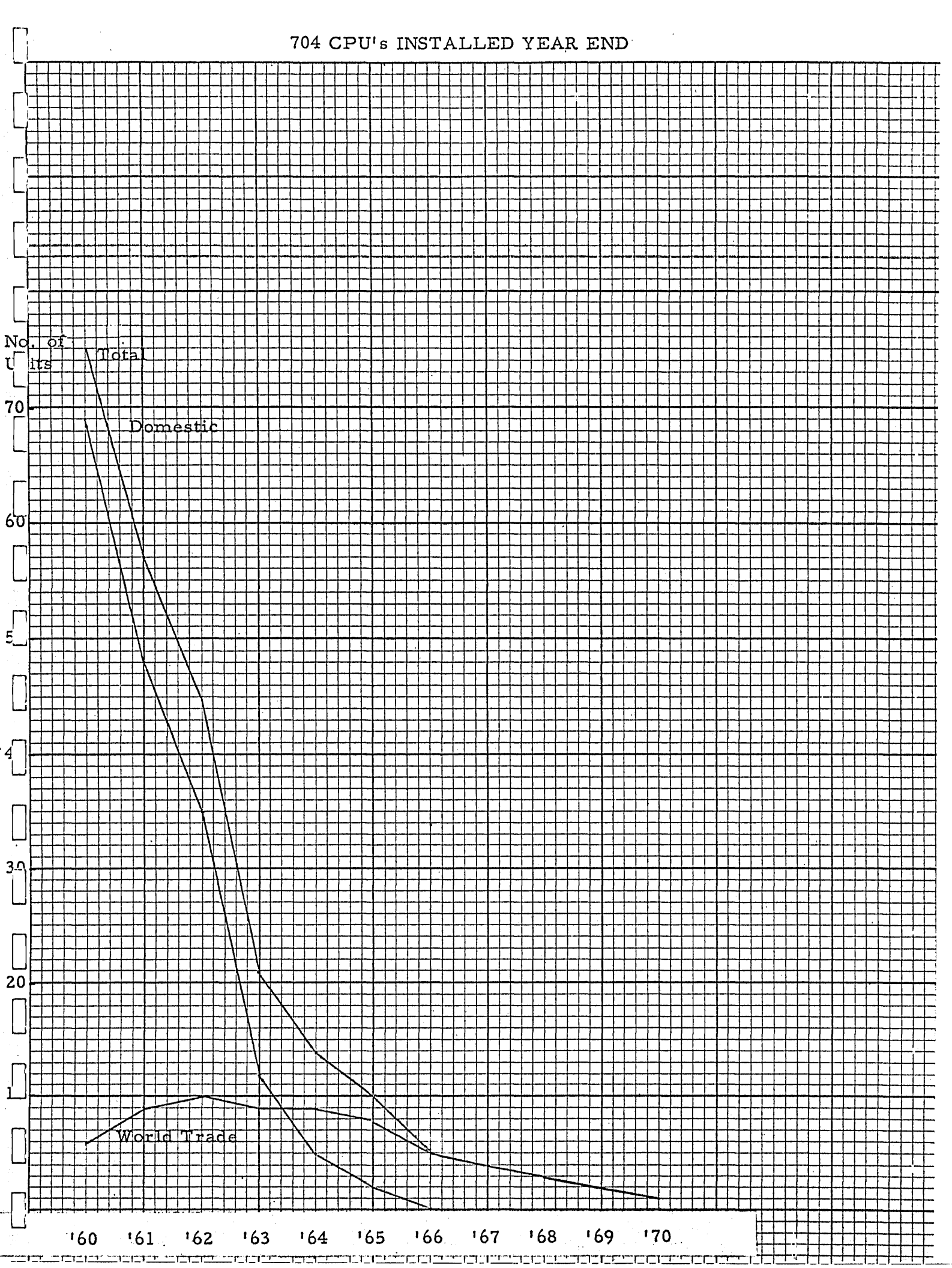

1620 CPU's INSTALLED YEAR END
No. of Units
Total
Domestic
World Trade
3000
2000
2000
1500
1000
00
50
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

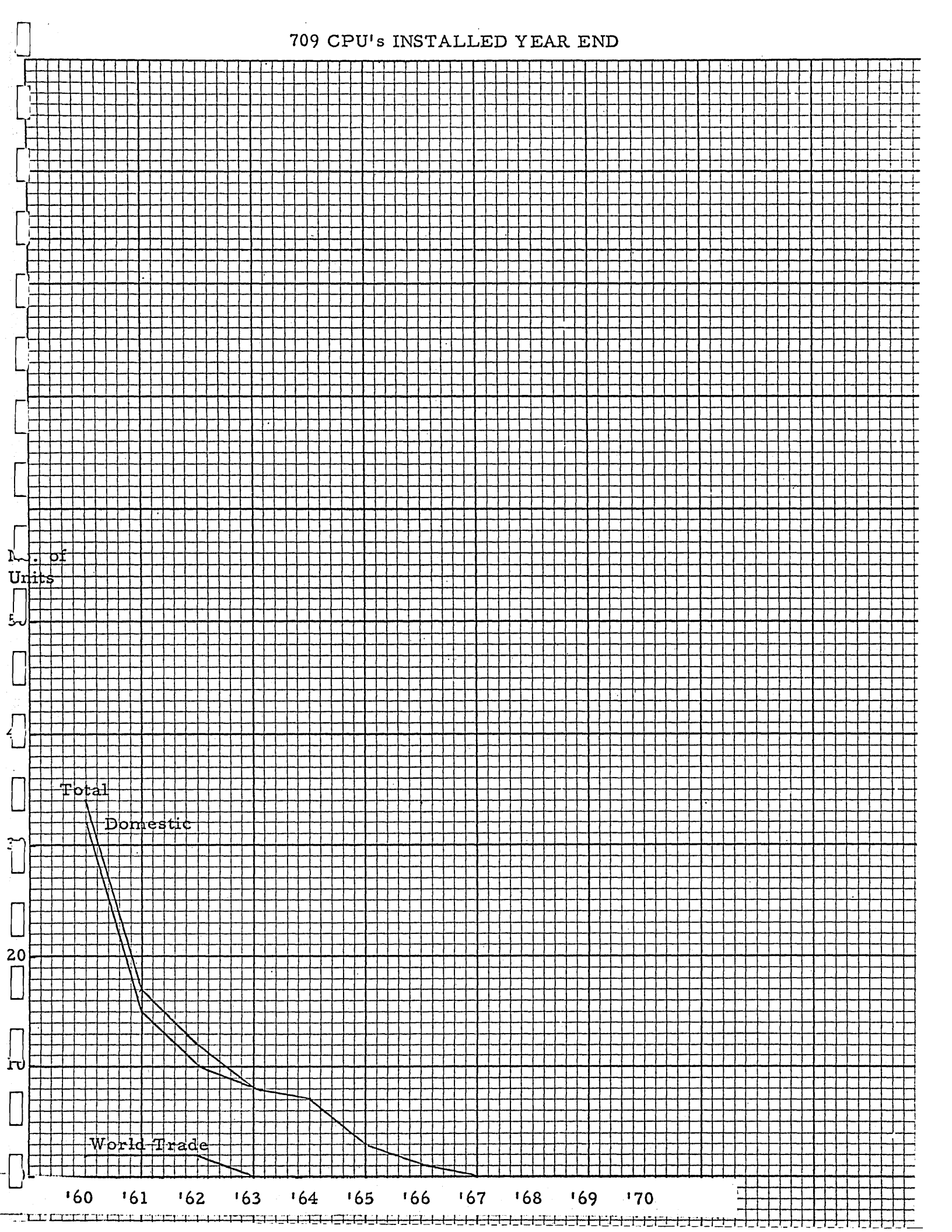

1410 CPU's INSTALLED YEAR END
No. of Units
Total
Domestic
World Trade
1400
1200
600
400
0
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

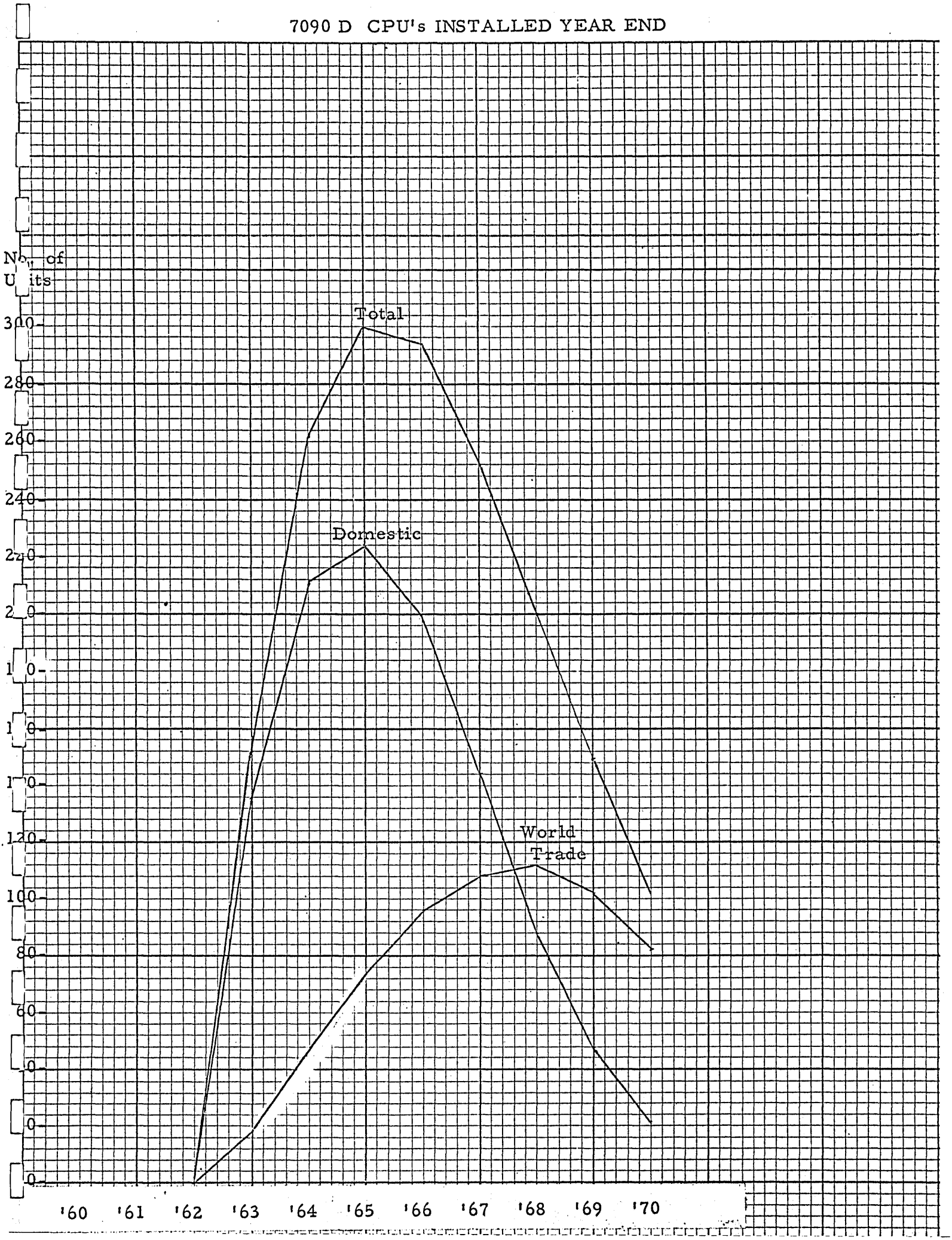

No. of Units
1410X CPU's INSTALLED YEAR END
400
300
200
100
0
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70


7070 CPU's INSTALLED YEAR END
No. of
Units
280
240
200
160
120
80
40
0
Total
Domestic
World
Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

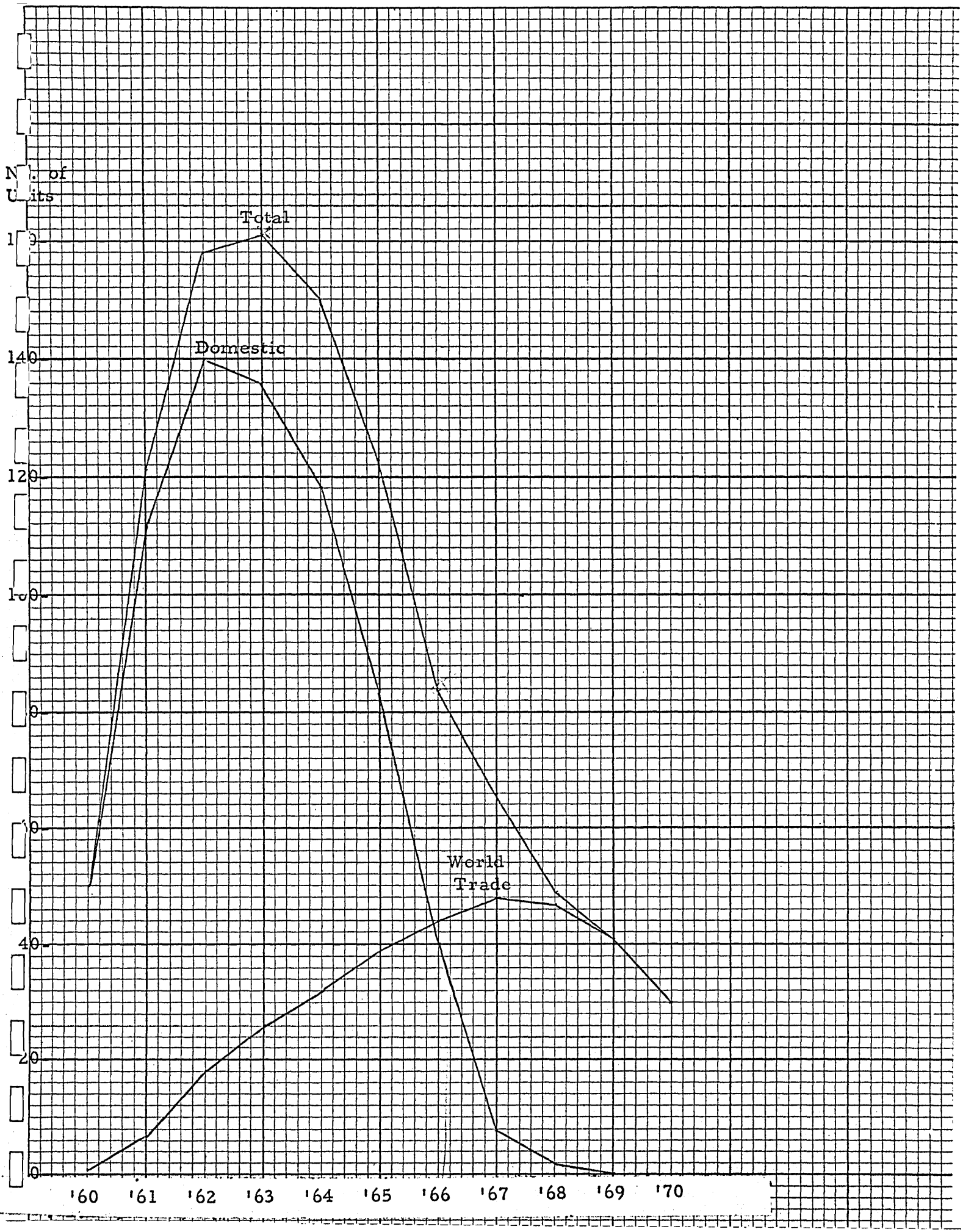

No. of Units
7074/2 CPU's INSTALLED YEAR END
200
100
100
120
100
0
0
0
20
0
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

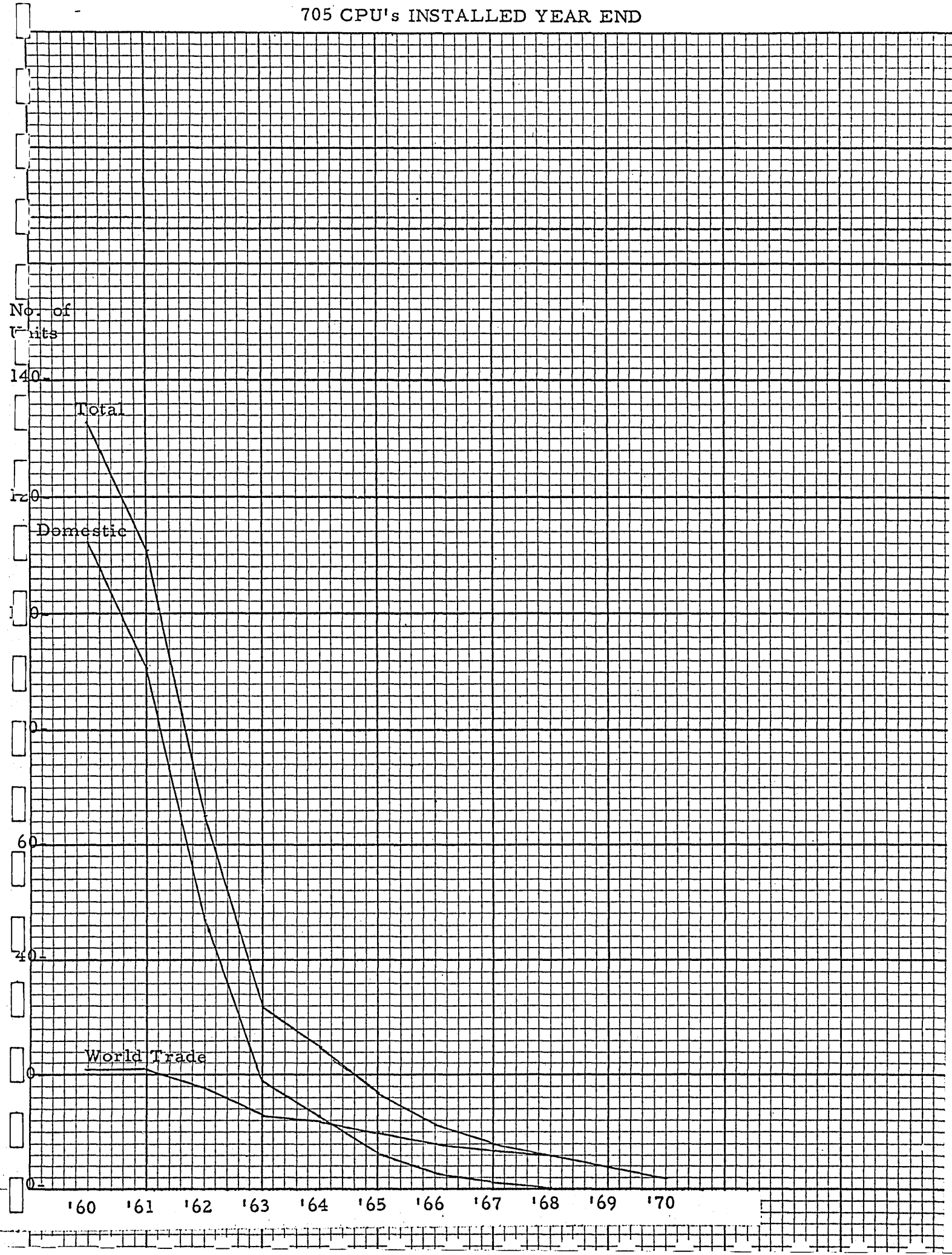

704 CPU's INSTALLED YEAR END
No. of Units
Total
Domestic
World Trade
70
60
5
4
30
20
1
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

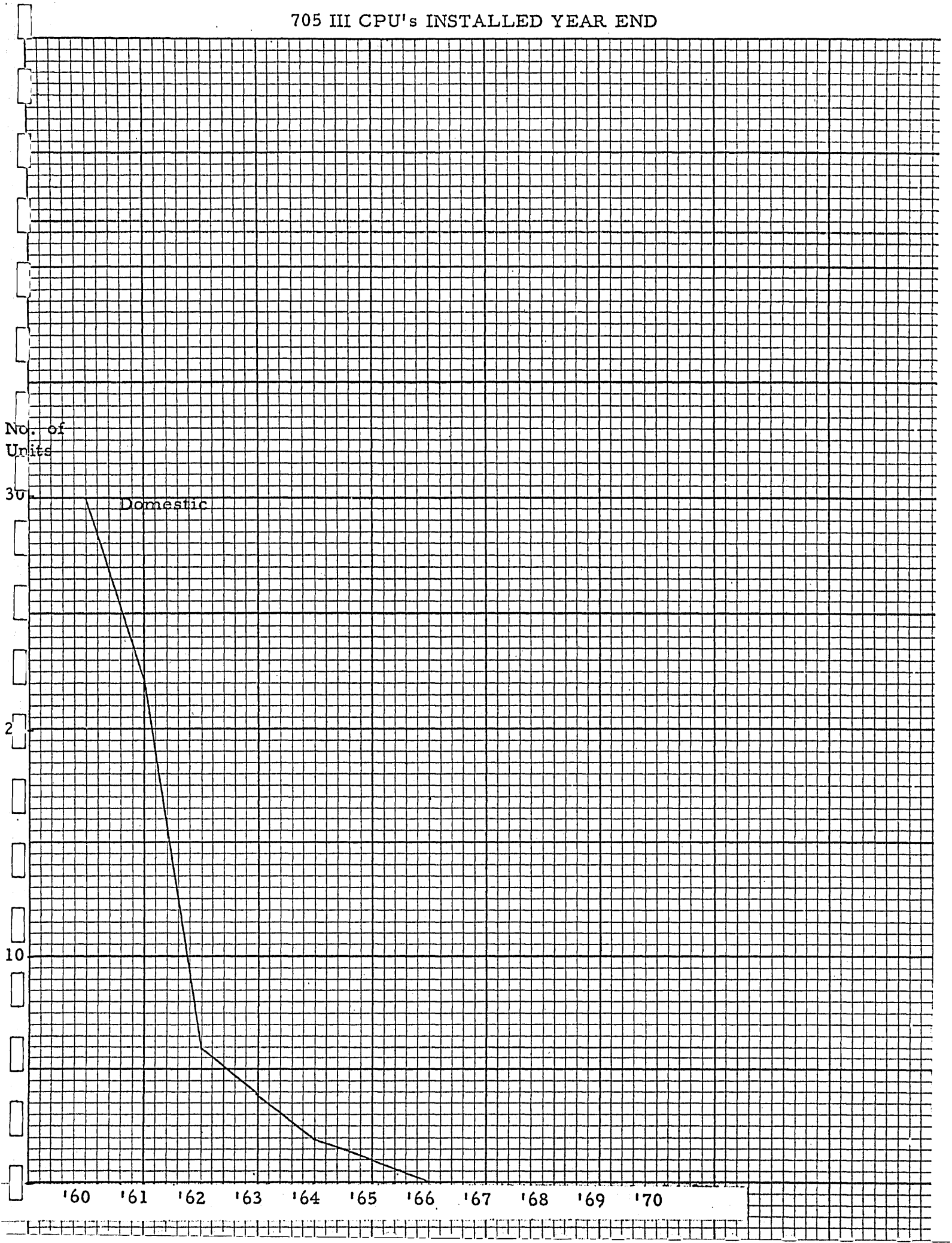

709 CPU's INSTALLED YEAR END
No. of Units
5
4
20
10
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

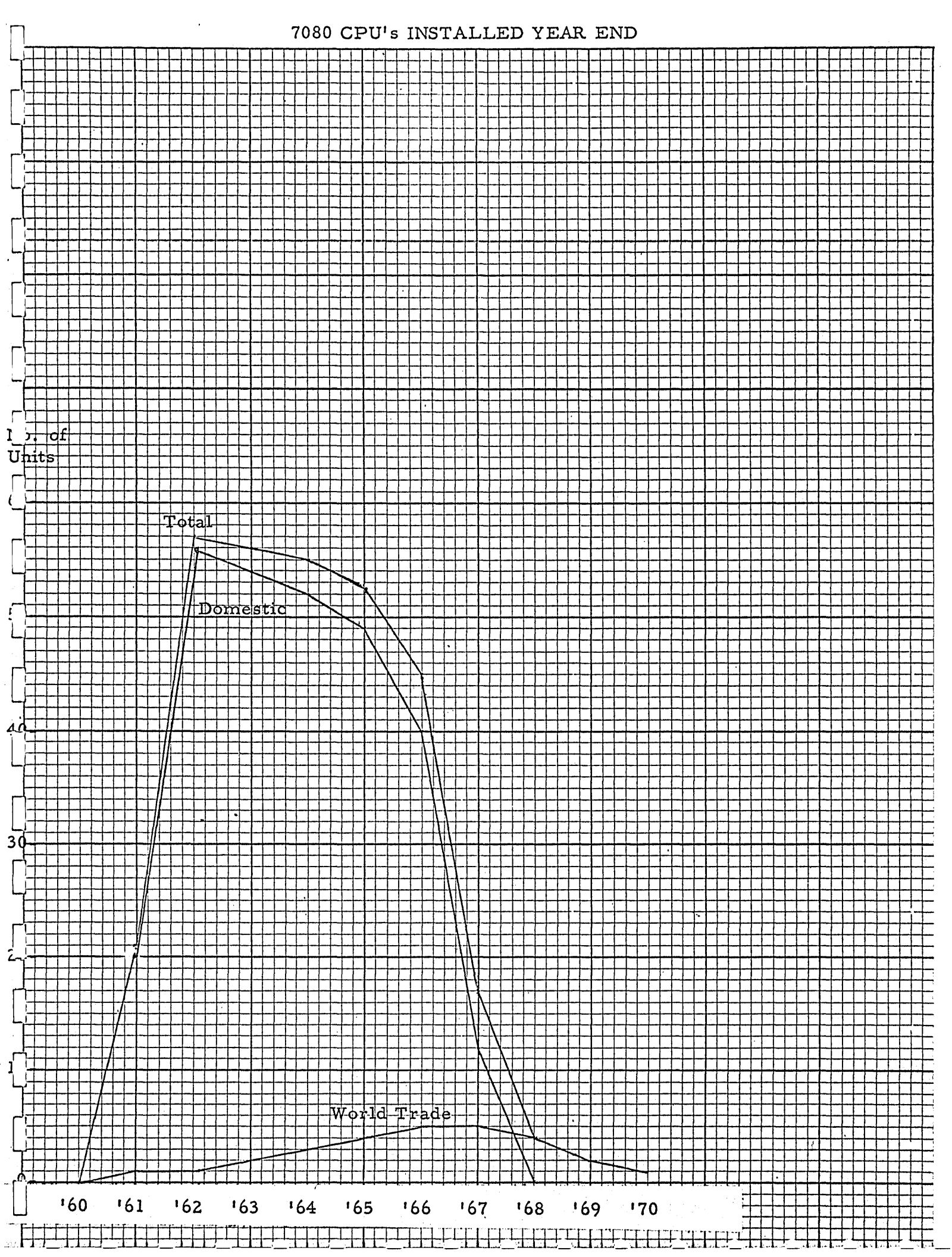

7090 D CPU's INSTALLED YEAR END
No. of Units
Total
Domestic
World Trade
300
280
260
240
220
200
180
160
140
120
100
80
60
40
20
0
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

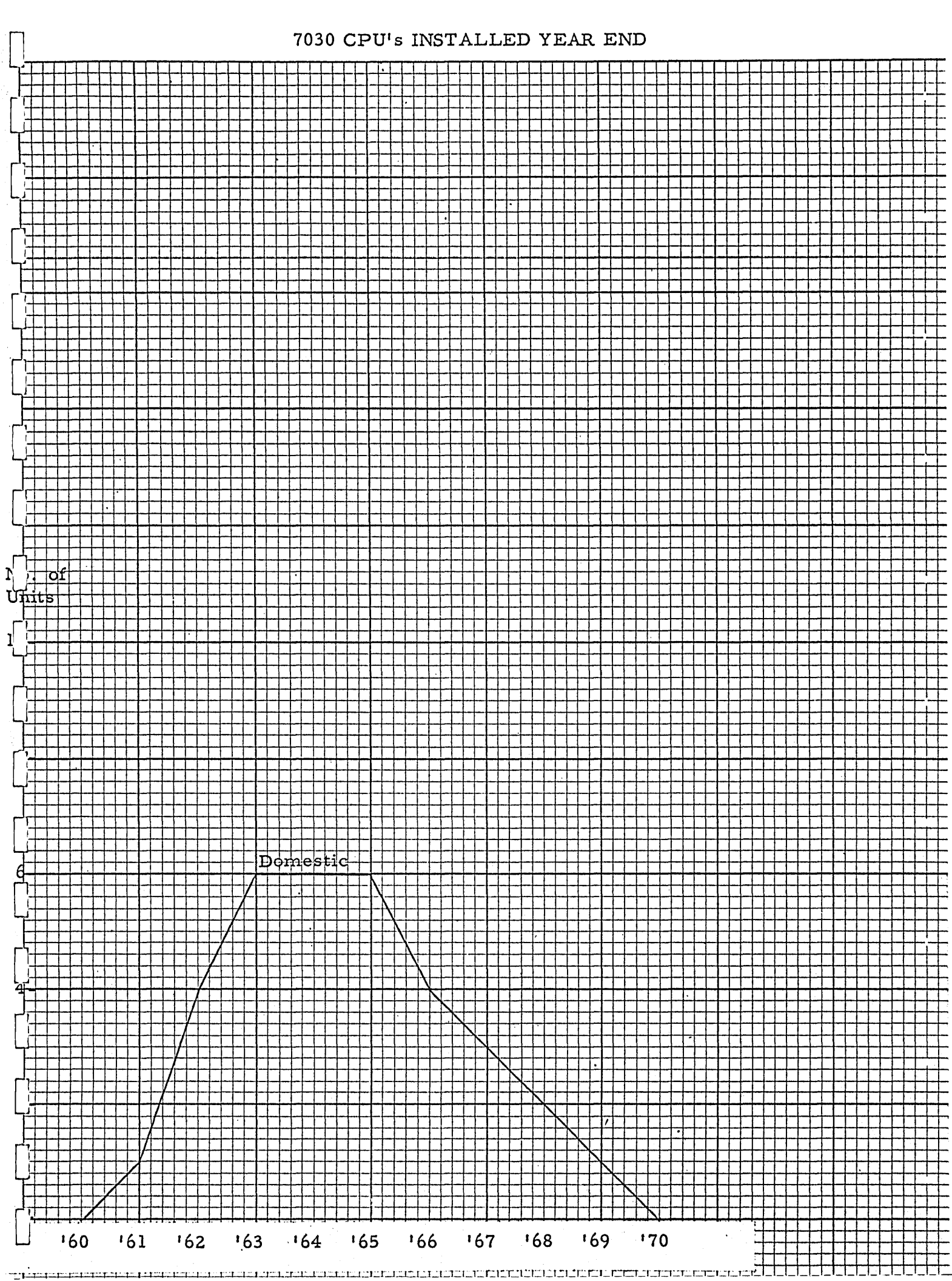
7090 & I CPU's INSTALLED YEAR END

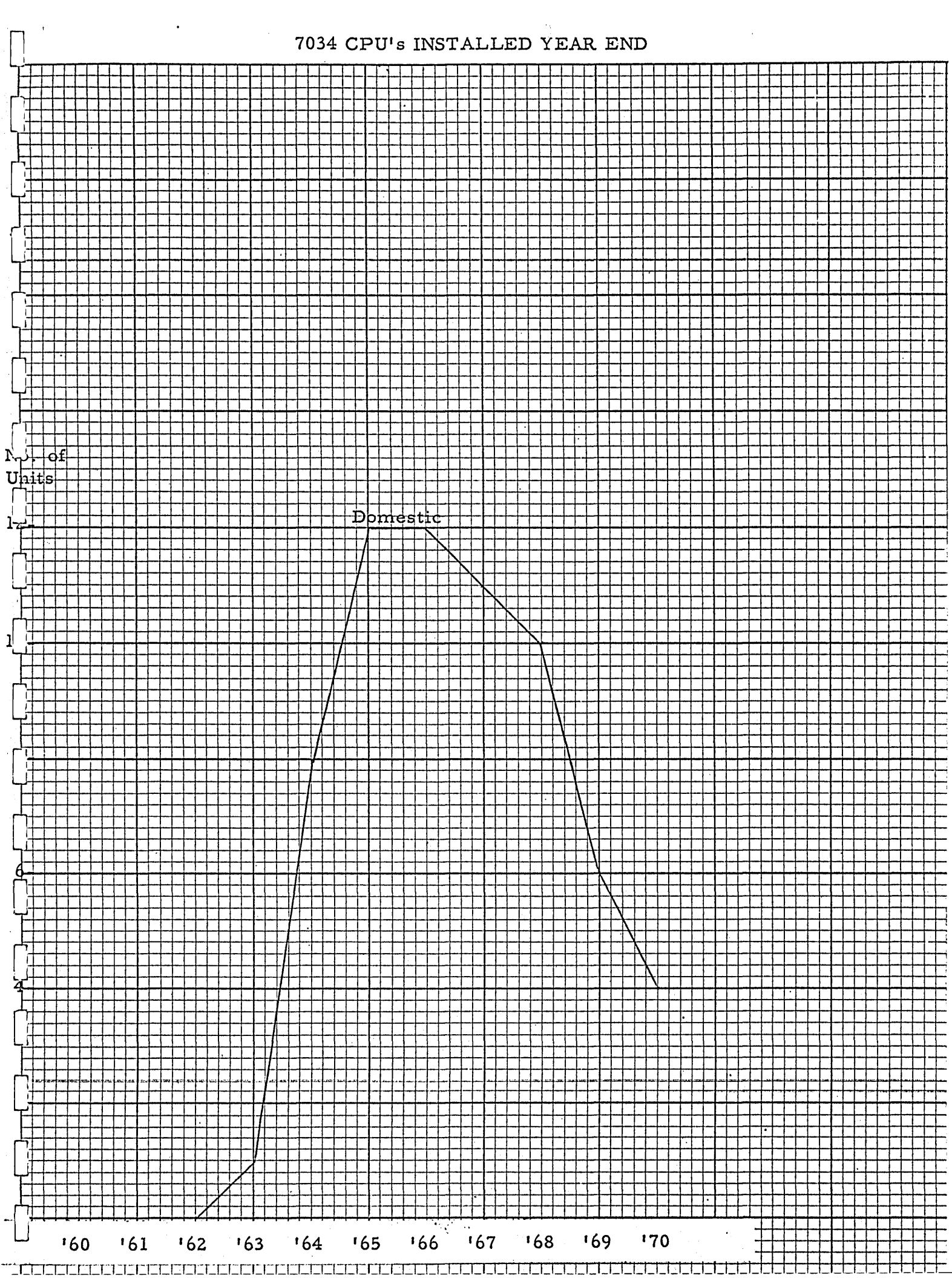



705 CPU's INSTALLED YEAR END
No. of
Units
140
120
100
80
60
40
20
0
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70


705 III CPU's INSTALLED YEAR END
No. of Units
30
2
10
Domestic
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70


7080 CPU's INSTALLED YEAR END
No. of Units
Total
Domestic
World Trade
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70


7030 CPU's INSTALLED YEAR END
No. of Units
Domestic
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70


7034 CPU's INSTALLED YEAR END
No. of Units
Domestic
'60
'61
'62
'63
'64
'65
'66
'67
'68
'69
'70

B. Relationship DSD, WTC, CPC

WTC is to develop machine #2 as part of the DSD product scope. The following relationship between WTC, The Corporate Processor Control, and DSD will apply:

A. Logical Structure

1. The Corporate Processor Control (CPC) is to be responsible for establishing and maintaining the basic logical specifications in a formal manual.

2. WTC is to concur with this manual and changes thereto.

3. British Labs Systems Support Group is to participate in defining the logical specifications and to work under the technical direction of CPC until the manual is completed. Thereafter, formal review review meetings, at alternate locations, will be scheduled under the chairmanship of CPC to consolidate and review changes and additions to the manual.

4. Resident liaison is to be established by CPC and WTC after completion of the manual.

B. Programming Systems

1. CPC is to be responsible for establishing the basic architectural ground rules to be formalized in manual form for the external and functional specifications.

2. WTC is to participate in establishing the external and functional specifications under the CPC technical direction. Thereafter, formal review meetings will be under the chairmanship of CPC.

3. WTC is to concur with the external and functional specifications.

4. WTC is to be responsible for the programming development of a part of the total new product line software product. Assuming that WTC will be in a position to start earliest on program checkout using actual hardware, the initial card oriented program package must be part of the WTC programming development assignment.

C. Engineering

1. WTC is to maintain engineering control up to 12 months after first delivery.

2. A WTC/CPC engineering standards working committee is to be established under the chairmanship of CPC and is to meet regularly at alternate locations. A formal engineering standards manual will be prepared.

3. WTC is to be responsible for the implementation of the system within the terms of the logical specifications manual and engineering standards manual.

D. Program Management

1. WTC is to be responsible for establishing a program schedule in PERT form and CPC to approve. CPC to coordinate and maintain a single PERT net for the complete product line.

2. Until a new Corporate Product Control Procedure is established, the WTC Product Procedure shall govern.

3. Program Phase change is to be with CPC approval.

4. Separate WTC and DSD Cost Estimates to be compiled at each phase with joint approval.

E. Product Test

1. Product Test A & B (hardware) and Alpha and Beta (software) is to be carried out and reported jointly by WTC and DSD.

2. Test procedures and specifications for A & B test (hardware) and Alpha and Beta (for the software assigned to WTC) to be written by WTC with DSD approval.

3. Product Test "C" to be made independently.

F. Marketing Requirements (Product Planning)

1. DSD is to be responsible for consolidating the system configuration, performance and feature requirements of the world market for a specific system.

2. Product objectives and specifications will be written by WTC as a basis for joint approval of the program by WTC and CPC.

3. WTC will be responsible for scheduling market forecasts and writing forecast assumptions which will have WTC/CPC approval before dissemination.

4. WTC and DSD will forecast their respective market areas.

G. Manufacturing

1. A single release format for the corporation will be of paramount importance in simplifying the release process. The new Design Automation Procedure, supporting documentation, and programs should be adopted as a corporate standard and maintained as such by the Components Division.

2. WTC is to be responsible for the release to DSD with support from DSD Manufacturing particularly with Product Engineering.

C. FSD - Correspondence

Following is correspondence relating to a hardened FSD Processor line for the Military market.

PERSONAL AND CONFIDENTIAL

December 27, 1961

Memorandum to: Mr. D. V. Newton

Reference: Your letter of December 12, 1961

You have asked for my opinion on each of four alternatives for developing a hardened SPREAD series as well as posing two supplemental questions. In answering all of these points, the question of degree is most important. For example, if FSD were to build one machine in line with the concepts in Alternatives 2 through 4, there might not be any significant problem if the peculiar design costs or FSD hardware requirements were reasonably costly; whereas, production of 100 units of the same character in all likelihood would be a problem.

Alternative No. 1 is, of course, acceptable. As an extension of Alternative No. 1, there would be no problem where FSD entered into a contract calling for the modification of a standard commercial machine procured under normal GSA terms and conditions.

Alternatives 2 through 4 have varying degrees of risk attached to them, depending upon such variables as quantity, degree and cost of modification including engineering and hardware. For this reason, I would be opposed to any of these three alternatives in implementing SPREAD in FSD.

You asked whether FSD could bid "one of a kind" systems which are compatible with the standard line. If such an FSD machine would not impact the product line, I would agree to their bidding same. Each case would have to be viewed separately because of the variables involved.

Finally, it is possible for FSD to produce and utilize similar sub-assemblies in their unique systems developments. Again, it is a matter of degree, particularly with regard to a similarity between the FSD and the commercial sub-assemblies. The greater the degree of difference, obviously the less risk and the greater the justification for a separate components line.

In the final analysis, just about all FSD proposals, other than those calling for the use of a standard commercial unit, must be carefully reviewed to insure that the FSD proposal does not impact the commercial line.

H. A. Faw

HAF:RWOK:cb

cc: Mr. K. N. Davis

PERSONAL & CONFIDENTIAL

December 12, 1961

Memorandum to: Mr. K. N. Davis
Mr. H. A. Faw

The Spread task group is considering IBM's future processor line and its relation to the various IBM divisions. We solicit your joint opinion on issues regarding FSD participation.

To date, the cost/price relationship between standard commercial units and FSD special militarized units has been resolvable, since the products have been divergent from basic components through sub-assemblies and systems organization. We understand that if we could technically achieve a single systems line to satisfy both the federal and commercial markets, no fundamental problem exists. We understand FSD will not be permitted their own proprietary line, however, they may bid unique military systems under certain rules of pricing and conflict with the commercial line. The Spread task group desires to explore the gray area in between the above boundaries.

The key to the questions lies in the depth of common use that planned commercial technologies will provide. One can conceive at least a common substrate containing active and passive elements assembled into a basic circuit design(s). It is conceivable that even greater common use is possible including larger sub-assemblies and/or identical logic organization as well as common tools for design mechanization.

The following alternatives exist for developing a hardened Spread series:

1. Identical organization--identical basic components with external appendages identifiable for separate pricing purposes.

2. Identical organization--identical basic components--internal additions to the basic sub-assemblies not identifiable for separate pricing purposes.

3. As in (1) with complete re-layout of logic and a milspec package.

4. Identical organization--different basic components (for example, Spread series implemented in Fieldata components, etc.).

We would appreciate your ruling on each of the above cases to establish whether or not the commercial line can be modified to provide compatible militarized system(s) for FSD.

In addition, assuming that FSD products are not derivable from the above alternatives, can FSD bid "one of a kind" systems which are compatible with the standard line?

There is a corollary question regarding FSD usage of commercial components. Is it possible for FSD to produce and utilize similar sub-assemblies (e.g., cards, substrates, etc.) in their unique systems developments assuming that a proprietary line is not permissible? For your information, attached is a Components Division estimate of SLT under varying production plans.

D. V. Newton
Sub-Group Chairman
Project Spread

DVN:bb

Attachment

COPY COPY

COMPONENTS DIVISION
Dept. 672 - Bldg. 906
Telephone GL 4-0030
November 30, 1961

MEMO TO: Mr. W. Graff

SUBJECT: Mr. J. W. Haanstra's Letter of November 16, 1961
Solid Logic Technology Estimates

Please find listed below quantities and costs requested in the subject letter as interpreted by you on November 28th.

	1964	1965	1966	1967
Case A				
# of lines	1	1	1	1
Quantity (Millions)	2.11	3.07	3.14	3.14
Costs	$6.82	$2.29	$1.61	$1.46
Case B				
# of lines	2	2	2	2
Quantity (Millions)	2.82	6.14	6.28	6.28
Costs	$5.51	$1.65	$1.25	$1.15
Case C				
# of lines	1	3	6	8
Quantity (Millions)	2.11	9.21	18.84	25.12
Costs	$7.15	$1.61	$1.08	$ .95
Case D				
# of lines	2	5	8	10
Quantity (Millions)	2.82	15.35	25.12	31.40
Costs	$6.20	$1.33	$1.01	$..91

s/ J. B. Hildebrand

JBH:jmc

cc: Mr. E. Bloch
Mr. G. A. McCauliff
Mr. R. M. James

MISSION

OVERALL
PLAN
FOR
FUTURE
PROCESSORS

SUMMARY

- SINGLE COMPATIBLE FAMILY
- RANGE OF ARCHITECTURAL AND ENGINEERING RULES
- PROGRAMMING PLAN
- REVENUE AND PROFIT GROWTH
- WORLD WIDE MARKET
- FSD HARDENED FAMILY
- IMPLEMENTATION PROGRAM

PROCESSOR CONCLUSIONS

1. ONE LINE OF FIVE PROCESSORS CAN SERVE FOR:
   - *ALL KINDS OF APPLICATIONS*
   - *BELOW THE 14LC THROUGH BEYOND THE 7034*

very small	1	2	3	4	5	very large
	200μs	75	25	5	1	
	1401	1410	1410X 7074			
	1620		7080	7094		
					7034	

2. EACH PROCESSOR IS GIVEN WIDER COVERAGE BY A VARIETY OF:
   MEMORY SIZES
   I/O CHANNELS
   I/O DEVICES

3. OVER THIS RANGE WE CAN BUILD PROCESSORS THAT ARE:
   ECONOMICALLY COMPETITIVE
   COMPATIBLE WITH EACH OTHER

PROCESSOR CHARACTERISTICS

- COMPATIBILITY
- FORMATS
- OPERATIONS
- INPUT - OUTPUT CONTROL
- RELIABILITY AND SERVICEABILITY
- ENGINEERING GROUND RULES

SOFTWARE PLANNING CONCEPTS

- EMPHASIZE NEW APPLICATION PROGRAMS FOR NEW MARKET AREAS
- THROUGH COMPATIBILITY, ALLOW CUSTOMERS TO GROW WITH MINIMUM DISRUPTION
- UNIFIED SOURCE LANGUAGE
- PROVIDE SOFTWARE PRODUCTS MORE EFFICIENTLY

SOFTWARE CONCLUSIONS

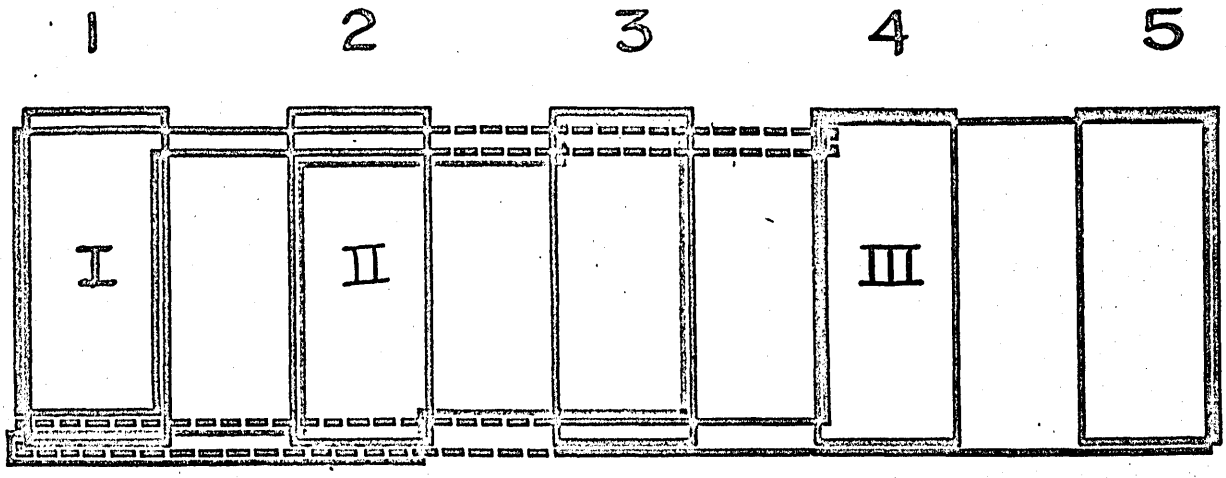
1. ONLY THREE PROGRAMMING SYSTEMS ARE REQUIRED

2. A SINGLE I/O CONTROL SYSTEM STRUCTURE WILL MEET REQUIREMENTS

3. CONTROL PROGRAMS REQUIRED ARE:
   - *CONSOLE COMMUNICATION*
   - *STACKED JOB MONITOR*
   - *BASIC SKELETAL REAL TIME CONTROL*
   - *SUPERMONITOR CONTROL*
   - *MULTIPROCESSING MONITOR (S)*

4. THE NUMBER OF INDUSTRY APPLICATION PROGRAMS REQUIRED WILL BE SIGNIFICANTLY REDUCED

SPREAD
PROCESSOR TYPES



CONFIGURATION CLASS

I CARD I/O · APPROXIMATELY 4,000 CHARACTERS OF STORAGE

II CARD I/O OR TWO TAPES, PLUS FIVE TAPES OR DISK FILE · 16,000 CHARACTERS OF STORAGE

III TWO TAPES AND; FIVE TAPES OR DISK FILE 128,000 CHARACTERS OF STORAGE

MARKETING

A COMPATIBLE FAMILY IS A MAJOR ADVANCE. IT OFFERS:

Sales Team

- *INCREASES PRODUCTIVITY*
- *PROVIDES NEW MARKETING TOOLS*
- *CONCENTRATES SUPPORT*

Customer

- *PROTECTS INVESTMENTS*
- *IMPROVES INDUSTRY PACKAGES*
- *MINIMIZES GROWTH DECISIONS*

POTENTIAL PROBLEMS

1. ANNOUNCEMENT MAY AFFECT ALL CUSTOMERS

   Solution:

   BETTER PRE-TESTING

2. ALLOWS COMPETITION TO BETTER ANTICIPATE OUR PROCESSORS

   Solution:

   SUPPORT AND SELL FULL SYSTEM

3. PRESSURES IBM TO PERPETUATE COMPATIBILITY INDEFINITELY

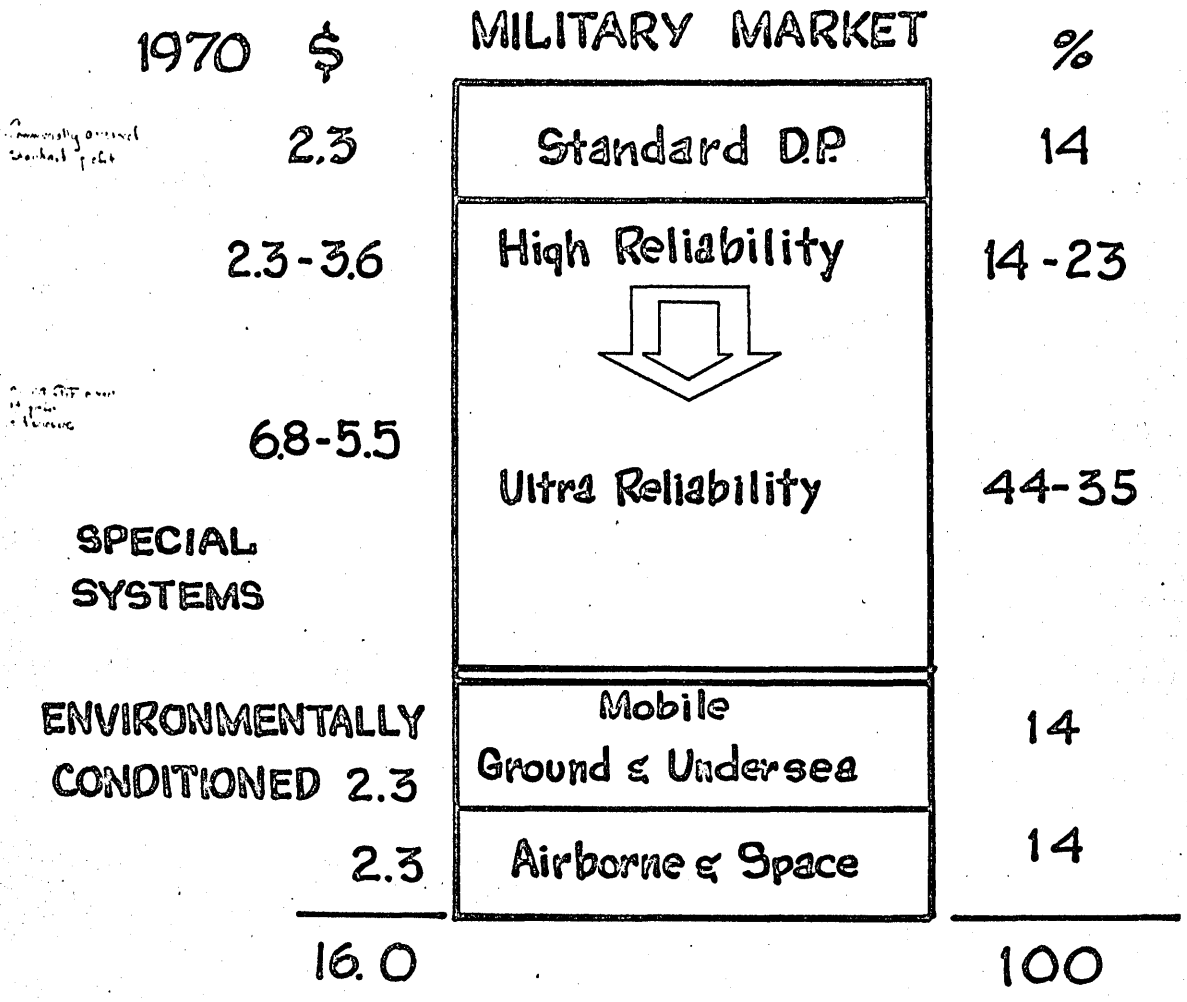
   Solution:

   COMMIT COMPATIBILITY ONLY TO ANNOUNCED FAMILY

RESULTS TO IBM

- SELL MORE MACHINES
- ESTABLISH BASE FOR VOLUME SELLING

FSD RELATION TO SPREAD



OBJECTIVE: Increase standard D.P. product share of military market by capitalizing on:

SLT RELIABILITY

MULTIPROCESSOR TECHNIQUES

IMPLEMENTATION

I INTERDIVISIONAL CONTROL

— A COMPATIBLE PROCESSOR FAMILY DICTATES:

- CENTRALIZED CONTROL IN OUR DECENTRALIZED BUSINESS HARDWARE / SOFTWARE

— PROCESSOR DEVELOPMENTS IN:

- SAN JOSE', ENDICOTT, POUGHKEEPSIE, HURSLEY, STUTTGART
- DIFFERENT DESIGN GROUPS =

  NON-COMPATIBLE DESIGN UNLESS CONTROLLED

II TO ACHIEVE COMPATIBLE FAMILY

- CORPORATE PROCESSOR CONTROL (CPC)
  - ASSIGN AS CORPORATE RESPONSIBILITY IN DSD
  - TO CONTROL PROCESSOR ARCHITECTURE/ENGINEERING

  DESIGN DEVELOPMENT - WITHIN PRODUCT SCOPE
  - GPD PROCESSOR #1
  - DSD PROCESSOR #2 (WTC SUBCONTRACTOR)
  - DSD PROCESSOR #3, 4, 5
- DEVELOPING GROUP WILL, WITH CPC APPROVAL
  - WRITE PRODUCT OBJECTIVES AND SPECIFICATIONS
  - PREPARE MARKET FORECAST ASSUMPTIONS
  - DEVELOP IN CONFORMANCE WITH ARCHITECTURE/ENGINEERING GROUND RULES

IV. DSD - CORPORATE PROCESSOR CONTROL

- ESTABLISH FRAMEWORK BY 4/1/62
  - HARDWARE/SOFTWARE
    - LOGICAL ORGANIZATION
    - REFINE PERFORMANCES RANGES
  - IMPLEMENTATION STANDARDS
    - PRODUCT CONTROL PROCEDURE
    - PRODUCT STANDARDS
    - PROGRAMMING STANDARDS
- CONTINUED MANAGEMENT OF EFFORTS WITHIN FRAMEWORK ESTABLISHED

V TECHNICAL DEVELOPMENT ACTIONS REQUIRED

- **CORP. MEMORY GROUP**
  - NON MECHANICAL MAIN MEMORIES
    - 32 TO 500 KILOBIT
    - 1/10 TO 1/2 PRESENT COST
    - CYCLE TIME TO 50 μs
  - INTERNAL MEMORIES
    - 3 – 512 WORDS
    - CYCLE TIME 1/4 TO 1/10 MAIN MEMORY
  - ROM FOR CONTROL
    - 2-250 KILOBIT
    - CYCLE TIME 1/4 TO 1/10 MAIN MEMORY
- **CORP. FILE GROUP**
  - BINARY ADDRESSED VERSIONS OF ALL PLANNED RANDOM ACCESS FILES
- **CORP. TAPE GROUP**
  - TAPE DRIVES < $200 RENT 5,000 CPS OR GREATER
- **DSD TECHNICAL DEVELOPMENT**
  - CROSSPOINT SWITCH OR TIME MULTIPLEX SYSTEM FOR I/O SWITCHING AMONG CHANNELS

VI APPLIED PROGRAMMING ACTIONS REQUIRED

- COMPLETE PROGRAMMING COMPATIBILITY VITAL
  - MUST INITIATE ADVANCED PROGRAMMING EFFORT IN DSD FOR CONFIGURATION INDEPENDENT PROGRAMMING
- PLAN FOR PROCEDURE LANGUAGES
  - FORTRAN / COBOL

    FOR FIRST INTRODUCTION

    ASSIST TRANSITION
  - IMMEDIATELY START ON : UNIFIED LANGUAGE FOR
    - SCIENTIFIC
    - COMMERCIAL
    - INFORMATION HANDLING

VII GROUP STAFF WITH DSD/GPD/WTC

TO DEVELOP MACHINE ORGANIZATION INDEPENDENT TECHNIQUES TO MEASURE

- INTERNAL PROCESSOR PERFORMANCE
- THROUGHPUT - SCIENTIFIC/ DATA PROCESSING/MIXED
- PROGRAMMING SYSTEM EFFICIENCY

TO DEVELOP TECHNIQUES FOR:

- QUICK MEASURE
- ULTRA PRECISE MEASURE

VIII MARKETING

OBJECTIVE

- NEW MARKET GROWTH
- IMPACT CONTROL-FOR REVENUE AND PROFIT

HOW TO ACHIEVE

- NEW INDUSTRY APPLICATION
- EXISTING MARKET GAPS
- USE 1400's AS SUBSYSTEM

ACTIONS REQUIRED

- INTERDIVISIONAL INDUSTRY APPLICATION DEVELOPMENT PROGRAM
  DPD, WTC, FSD, ASDD TO APPOINT MANAGERS
- MANAGERS TO:
  - ESTABLISH GROUND RULES - BY 6/30/62
  - IDENTIFY INDUSTRIES
  - MARKET POTENTIAL
  - DIVISION TASKS - PRODUCE NEW APPLICATION PACKAGES:
    NEW CUSTOMERS
    EXTEND PROCESSOR USE
    SUPPORT ANNOUNCEMENT AND INSTALLATION
    COORDINATE WITH CPC

IX. INTRODUCTION PLANNING

- PROCESSORS #2 & #5 TO BE ANNOUNCED IN 1ST. AND 3rd QTR 1964
- NO ANNOUNCEMENT UNTIL PROCESSOR#1 REACHES "A" TEST ENTRY LEVEL
- L²C TO ADHERE TO SPREAD ARCHITECTURAL RULES
- 14 LC ANNOUNCE AS PLANNED
- 1410X CONTINUE DEVELOPMENT AS PLANNED
- 7034 NO ANNOUNCEMENT UNTIL ECONOMICS ARE CONFIRMED:
  - (a) 7034 AND CPU #5
  - (b) CPU #5 ONLY

X. SECURITY

WE MUST KEEP SECURE:

- DECISION TO DEVELOP COMPATIBLE LINE
- TIME TABLE FOR INTRODUCTION OF PROCESSORS
- DESIGNATION OF PROCESSORS
- GROUND RULES FOR COMPATIBILITY
- INSTRUCTION SET

— ALL DOCUMENTS CONTAINING THESE DATA ARE TO BE REGISTERED COMPANY CONFIDENTIAL

— DIVISIONAL AND SUBSIDIARY IMPLEMENTATION PLAN

- GROUP STAFF APPROVAL