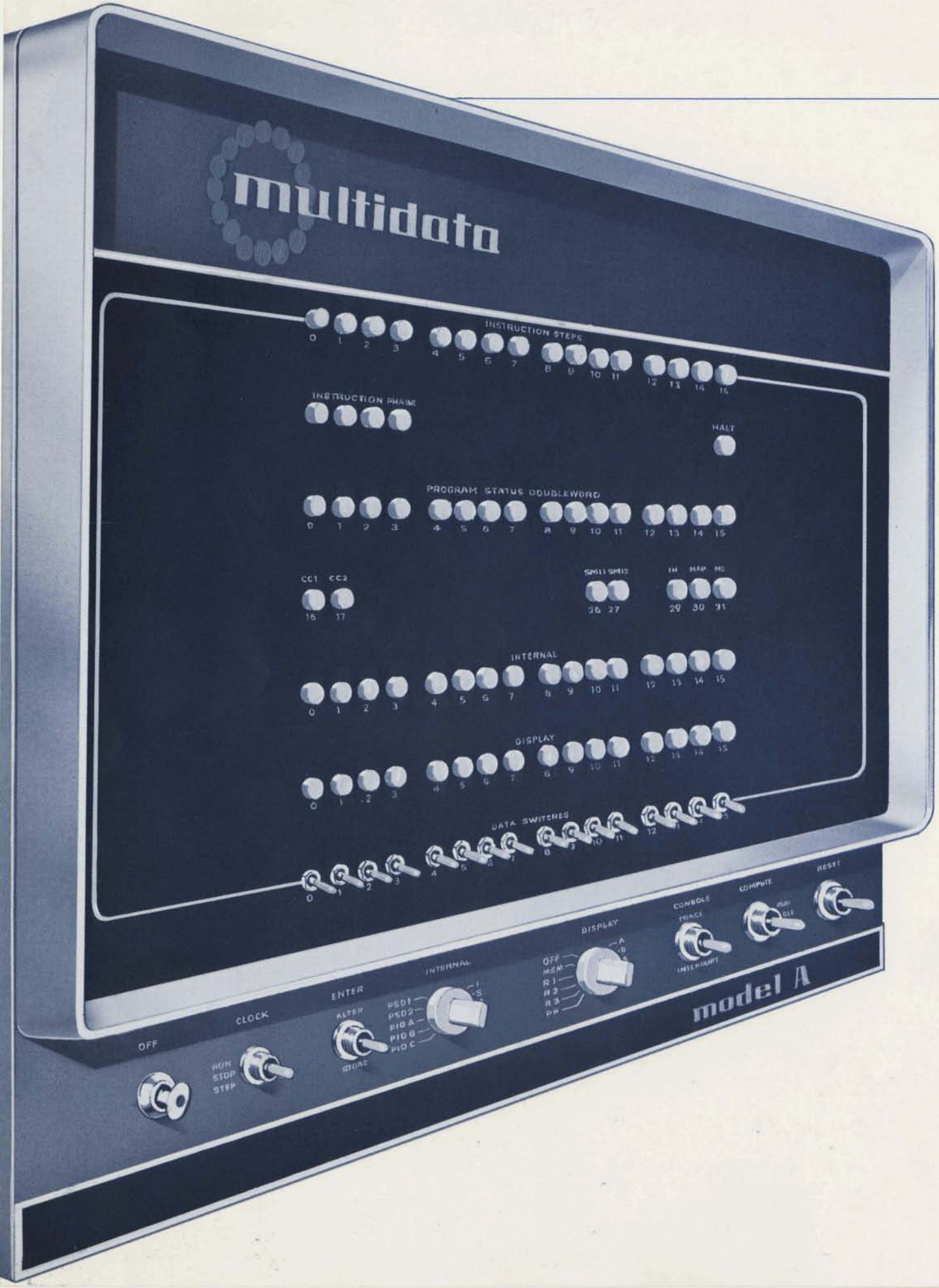

multidata


multidata
INSTRUCTION STEPS
INSTRUCTION PHASE
HALT
PROGRAM STATUS DOUBLEWORD
CC1 CC2
SMI1 SMI2
IH MAP MS
INTERNAL
DISPLAY
DATA SWITCHES
OFF
CLOCK
RUN
STOP
STEP
ENTER
ALTER
STORE
INTERNAL
PSD1
PSD2
PIO A
PIO B
PIO C
DISPLAY
OFF
MEM
R1
R2
R3
PP
CONSOLE
TRACE
INTERRUPT
COMPUTE
RUN
CLE
RESET
model A

INTRODUCING THE MODEL A

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$14,995

The Model A embodies large-scale system architecture to achieve a problem-solving capability unmatched by any other system-oriented computer in its price class.

Big-machine concepts include:

- large memory capacity . . . to handle programs approaching 65,536 words in length
- real-time rapid context switching . . . for faster response in a real-time, multiprogrammed environment
- automatic program fragmentation . . . for more efficient use of core memory
- privileged instructions and memory write protection . . . for system integrity
- device independent input/output . . . for flexible programming of peripheral devices
- multilevel interrupt system . . . for critical time response
- demand multiplexed input/output . . . for concurrent peripheral device operation
- command chaining . . . for single-instruction programming of a series of input/output operations
- data chaining . . . for scatter-read, gather-write operations

SYSTEM DESIGN

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Model A design criteria called for a system-oriented computer with the computing power and real-time system response to handle a wide variety of applications.

As shown in the block diagram, the basic configuration includes 4096 16-bit words of core memory in tandem with 32,768 words of disc memory, a memory access controller, a central processor, an input/output bus, and a teletypewriter with paper tape reader and punch.

The core-disc combination — a cost effective alternative to large core — provides the main prerequisite to computing power; large memory capacity. Using memory management ideas derived from the latest timesharing technology, the Model A has the versatility to cope with the following situations:

1 Real-time system requires 4096 words of core memory with a cycle time of less than one microsecond. Interrupt response must take less than five microseconds.

2 Real-time system requires 16,000 words of core memory for time-critical functions controlled by interrupts and 30,000 words of program storage for background analysis.

3 Real-time system requires special instructions for very fast computation of time-critical functions.

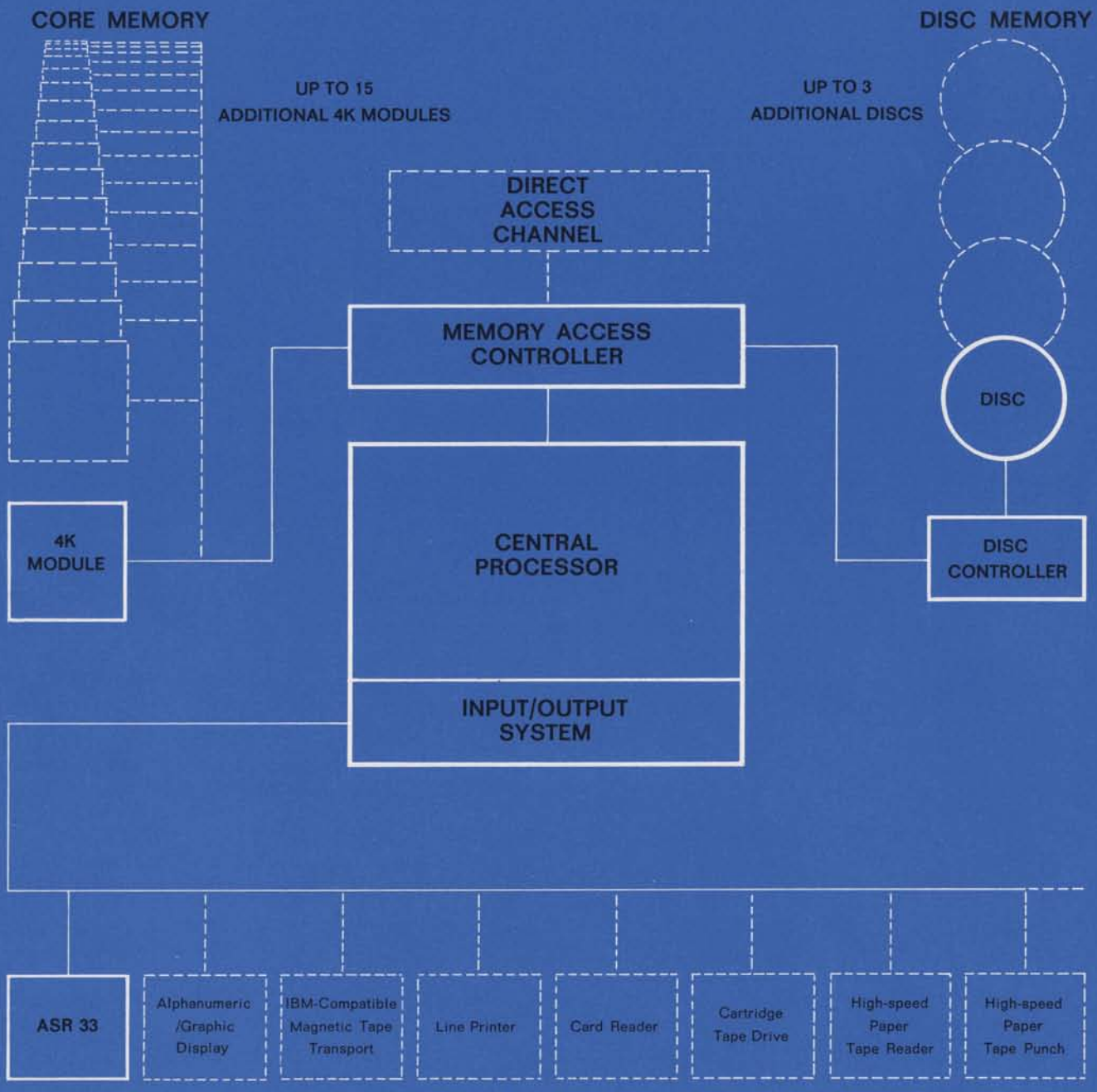
4 Analysis program requires program storage of 60,000 words. No real-time inputs, but problem turnaround time must be short.

MEMORY

A small computer is uniquely suited to using a core-disc memory efficiently: Its short address field forces the small computer to work in segments of core memory. Thus, it treats core as a series of little memories, most of which are idle much of the time. The Model A takes advantage of this limited use of core by making the disc load and unload unused segments of core in such a way that core has an effective capacity equal to the disc.

Memory Access Controller. The Memory Access Controller enables the central processor to execute programs approaching 32,768 (optionally 65,536) words in length from a 4096-word core. A larger core is necessary only if the time-critical portion of a program, which must be resident, will not fit into the basic module. The programmer may prepare programs for the Model A without regard to its core memory capacity. And program segmentation is not a problem — the Controller does it automatically.

The Controller divides core memory into 256-word pages and transfers program segments a page at a time from disc into core. Any program segment may go into any page, which means that contiguous program segments may be scattered in core. This allows core memory to be organized quickly and efficiently because contiguous pages need not be found for contiguous program segments. A memory map (a complement of 20-nanosecond registers in the Controller) keeps track of the page assigned to each program segment. Since the map


CORE MEMORY
UP TO 15
ADDITIONAL 4K MODULES
DISC MEMORY
UP TO 3
ADDITIONAL DISCS
DIRECT
ACCESS
CHANNEL
MEMORY ACCESS
CONTROLLER
DISC
4K
MODULE
CENTRAL
PROCESSOR
DISC
CONTROLLER
INPUT/OUTPUT
SYSTEM
ASR 33
Alphanumeric
/Graphic
Display
IBM-Compatible
Magnetic Tape
Transport
Line Printer
Card Reader
Cartridge
Tape Drive
High-speed
Paper
Tape Reader
High-speed
Paper
Tape Punch

associates program addresses with core memory addresses, it provides the dynamic relocation capability needed to handle program memory references. All of this activity is transparent to the user's program.

The map also provides memory protection capability; pages may be coded for no access, read only, or read and write. This protection extends to all core memory accesses because all such accesses are mapped, including those coming from the input/output system.

The Controller sets up priorities among the disc, the direct access channel, and the central processor; and it resolves simultaneous core memory access requests accordingly.

The (optional) memory parity feature causes the Controller to generate parity on each memory write operation and check parity on each memory read operation. A parity error detected during a read operation aborts the operation and forces the central processor to a trap location. This technique indicates that an error was about to occur; other computers usually interrupt, resulting in a nonrecoverable error.

Core Memory. Operating at an 880 nanosecond cycle time, each 16-bit, 4096-word memory module is independent and asynchronous. This allows overlapped accesses if a system contains two or more modules. The Model A accommodates up to 16 modules (65,536 words), and field installation is easy; each module requires the insertion of one printed circuit board assembly.

Disc Memory. The 32,768-word disc is field expandable to 65,536 or 131,072 words. Its fixed-head, head-per-track design minimizes access time, which averages 17 milliseconds. The heads ride on a cushion of air and do not contact the recording surface. This flying head feature increases reliability, particularly during startup and shutdown.

CENTRAL PROCESSOR

Adapting large-scale system concepts to its internal organization, the Central Processor is able to make full use of the large memory. The result is a balanced system — with far greater computing power than any other small computer.

Registers. The Model A makes programming easier by providing eight programmable registers. They are: Programmed Input/Output Register, Accumulator, Extended Accumulator, Index Register, Base Register, and three General Registers. Whether they occupy eight core memory locations or (optionally) eight integrated circuit registers, they may be addressed as memory locations. This enhances their usefulness because the load, store, arithmetic, and logical instructions may operate on them directly.

A pair of registers (the Program Status Double Word) monitors the program environment, keeping track of current location, condition codes, compare sequence mode, interrupt inhibit mode, map mode, and master/slave mode. Having this information immediately accessible at all times enables the Model A to transfer control quickly from one program to another.

Instruction Set. The five-bit operation field — twice the usual memory reference capability — hints at the scope of the instruction set. The 125-instruction complement includes the usual load, store, arithmetic, logical, shift, and branch instructions, as well as byte instructions, a memory incrementing instruction, and a three-way compare instruction. In addition, there are such useful instructions as Call, Branch on Conditions, and Branch and Link — normally found only in much larger computers. Each instruction requires only one word.

Special purpose instructions have been omitted because of their limited usefulness. Instead, six memory reference codes have been set aside for (optional) user-specified instructions. (These may be used for up to six memory reference instructions or for dozens of nonmemory reference instructions.) Among the more obvious choices are:

- Floating Point Arithmetic
- Fixed Point Multiply/Divide
- Compare within Limits
- Push Down/Pull Up List Pointers
- Bit Set/Test
- Load/Store Double Word
- Read and Increment/Decrement
- Increment on Mask
- Time-Slot Test

The richness of the instruction set by itself gives the Model A programming capability that leads to shorter, and consequently faster, programs. But a more striking facet of its superiority over other small computers stems from the way in which the Model A uses the instructions to full advantage. As mentioned, the instruction set operates on all eight programmable registers. Another example is the compare sequence mode, which enables the results of a series of compare instructions to be ORed and ANDed together. This provides the means for efficient data compression operations — often highly time-critical.

Addressing. Memory reference instructions may address the first 128 locations of core memory, up to 127

locations either forward or backward from the current location, or up to 127 locations forward from the contents of the Base Register. These instructions may apply either single-level indirect addressing or indexing (or both).

The Base Register, the Index Register, and the contents of any indirectly addressed location are each capable of addressing any location in the entire 65,536-word programmable range.

When an instruction calls for Base Register addressing and later for indexing, the Base Register performs what amounts to a pre-indexing and the Index Register then applies a post-indexing. This double indexing makes the Model A particularly effective in working with data tables because the Base Register points to the starting location of the table and the Index Register points to an element in the table that is not necessarily a full word. (A word instruction would access a word, a byte instruction would access a byte.)

Real-Time Clocks. Up to four (optional) Real-Time Clocks (two pairs) are available. Clock frequency may be set manually to either 60 Hz or 1 MHz — or it may be supplied from an external source. The program sets each clock to a count. Since each counter is an external register, it does not slow the program while counting down; it triggers an interrupt only when the count goes to zero.

Power Fail Safe. This option detects an imminent power failure and stores all volatile registers, including the Program Status Double Word, in nonvolatile core memory. It automatically configures the interrupts to their previous state, loads the registers, and starts the program again when power returns to normal. The restart occurs without operator intervention.

INPUT/OUTPUT SYSTEM

The Input/Output System incorporates large-scale system concepts while remaining flexible and uncomplicated.

Input/Output Bus. Using a demand multiplexed technique (asynchronous, unclocked data transfers), the Input/Output Bus handles concurrent device operation up to a composite data rate of 100,000 words/second. Command chaining and data chaining simplify the programming task.

A single instruction in the user's program initiates command chaining, which performs a series of operations on a peripheral device without further intervention from the user's program. The monitor obtains a series of four-word Input/Output Command Lists (IOCL) from the user's program, one for each operation to be performed. Each IOCL tells which operation to perform, the first core location to access, how many locations to access, and what to do upon terminating the operation. For example, one instruction in the user's program could read 16 magnetic tape records, rewind the tape, and reposition the tape 12 records from the load point.

Data chaining provides scatter-read, gather-write capability. Again, a single instruction, with appropriate IOCL's, can initiate a series of operations. A typical example of data chaining is the gathering of information from several areas of core memory, to be printed on a single line of the console teletypewriter.

Special interfaces to the Input/Output Bus are simple and straightforward. Multidata offers a general purpose interface card as a convenience to the interface designer. There is also a breadboard card with 150 integrated circuit sockets (ready for wirewrapping) for the user who wants to build an entire peripheral device controller on one board.

Direct Access Channel. Data rates approaching 1,000,000 words/second are possible through the (optional) Direct Access Channel. It interfaces directly to the Memory Access Controller and provides a Memory Address Register, a Data Register, and all necessary controls. It presents a simple interface to the user and guarantees system integrity.

Interrupts. The comprehensive, multilevel interrupt system controls all input/output operations. A program may arm/disarm, enable/disable, trigger, or sense individual interrupts of the (optional) 256 levels available.

Disarming turns an interrupt off. A program uses this capability to reassign a stimulus to a different priority level or to remove it altogether.

Disabling an armed interrupt prevents that interrupt from requesting service, but not from acknowledging a stimulus. Thus, a program can defer response to a stimulus without losing track of it.

Triggering is the means by which a program can initiate an interrupt stimulus of its own. These program-generated interrupts are useful in simulating external system elements during program checkout. They are also useful in putting portions of a program in the external stimulus queue.

Sensing checks the status of each interrupt level. This capability is essential to the power fail shutdown routine, which must record the interrupt configuration.

CONTROL PANEL

The fully developed Control Panel provides the register displays and controls needed for fast, thorough diagnostic testing of hardware and user programs.

The (optional) Portable Control Panel may be hand-carried along with test equipment to convenient test locations up to 25 feet away. This capability is especially useful in checking out a special front end system with the Model A.

The (optional) Console Interrupt is an added convenience. In the TRACE mode it interrupts automatically after every instruction for fast, efficient debugging of programs.

MAINTAINABILITY

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Small computers almost never receive resident on-site maintenance, and very often do not even get regular preventive maintenance. Therefore, reliability and remedial maintenance become important considerations to the cost-conscious small computer user. Multidata has taken pains to design in reliability and to set up realistic remedial maintenance resources.

RELIABILITY

Low maintenance costs start with high reliability. Quality components are a must. But it is also imperative that they be used carefully. Little things make a big difference when it comes to reliability. Little things like derating integrated circuits. Or preheating indicator lamps and operating them below rated voltages. Or running at least ten milliamperes of current through all the switches.

REMEDIAL MAINTENANCE

Multidata's realistic approach to remedial maintenance is evident in the documentation. The basic manual is not on the theory of operations; it is a Trouble-Shooter's Guide. This Guide tells how to use the diagnostic routines and gives detailed procedures for tracing a failure to the integrated circuit component level.

Another thoughtful design is the control panel. Its 76 indicator lights provide simultaneous display of several registers. Again, little things were not overlooked: The indicator lights are in sockets, not soldered, making them relampable from the front of the control panel.

The single-clock feature permits single-stepping through an instruction. For an output instruction to a special system device, this would show the effective address being calculated, the effective address and the data being sent to the device, and the status being sent back from the device. Detailed examinations like this resolve questions regarding hardware/software origin of errors.

SPARES

For the user who does his own maintenance, Multidata offers for sale a spare parts kit tailored to the needs of his configuration. Alternatively, Multidata will provide a complete spares inventory on the user's site for a nominal monthly stocking charge. As parts are used, Multidata will replenish the inventory at no additional charge. This puts the responsibility for reliable components on the manufacturer — where it should be — and is a further indication of Multidata's solid commitment to maintainable systems.

EMERGENCY SERVICE

For the user who needs attention before field maintenance personnel can arrive, Multidata offers emergency service from the home office. This service provides a control panel device which, when connected to a similar device at Multidata through telephone lines and acoustic couplers, enables home office personnel to monitor the control panel. It offers immediate expert assistance to even the most remote user.

PROGRAMMING SYSTEMS

The software takes full advantage of the Model A's advanced hardware. Model A software is based on a 32,768-word, not the usual 4096-word, memory — with a commensurate increase in usefulness. It is more flexible, comprehensive, and powerful.

MONITOR

The Monitor minimizes core memory requirements by maintaining system programs in core only while they are active.

Its core-resident Kernel operates in the master mode and optimizes core/disc page transfers through the Memory Access Controller. (The Kernel is transparent to the user's program.)

Its input/output handlers respond to Call instructions and perform input/output operations concurrently with the user's program.

Its Linking Loader relocates system routines into core memory to form a single program.

FORTRAN IV COMPILER

The multipass Fortran IV Compiler generates efficient object code without requiring successive source statement reloading.

ASSEMBLER

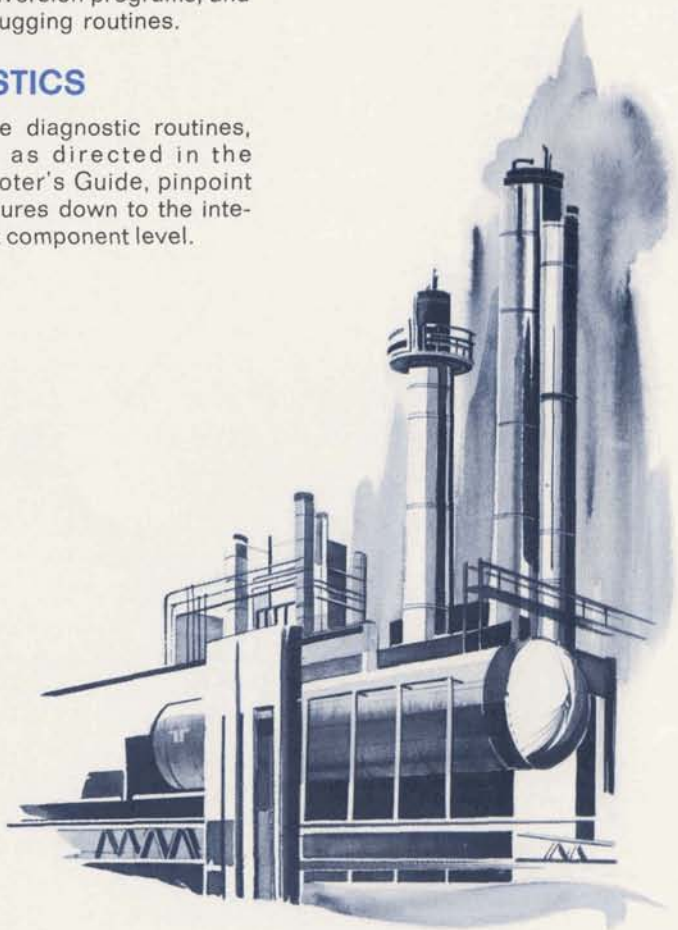
The two-pass Macro-Assembler provides a procedure-oriented capability. It can write an intermediate file in memory and eliminate the second reading of the source code.

UTILITY PROGRAMS

Model A software includes a subroutine library of arithmetic functions, a paper tape editor, device-to-device conversion programs, and program debugging routines.

DIAGNOSTICS

The hardware diagnostic routines, when used as directed in the Trouble-Shooter's Guide, pinpoint hardware failures down to the integrated circuit component level.



PERIPHERAL EQUIPMENT

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The Model A offers a broad range of field proven and cost effective peripheral devices.

TELETYPEWRITERS

One ASR33 comes with the basic configuration. The heavy-duty ASR35 is also available, as are the KSR33 and the KSR35. All of these units print at ten characters/second. The ASR units also read and punch paper tape at ten characters/second.

PAPER TAPE EQUIPMENT

A 300 bytes/second photoelectric paper tape reader offers higher performance paper tape handling than does the teletypewriter equipment. A 120 bytes/second paper tape punch is also available.

CARTRIDGE TAPE DRIVE

Four-track magnetic tape cartridges offer a convenient, economical medium for program and data storage. They are self-contained and reusable. The drive unit reads and writes 300 bytes/second. The tape holds more than 350,000 characters.

CARD READER

A pneumatic picker and a photoelectric read station assure gentle card handling in this 400 cards/minute card reader.

MAGNETIC TAPE TRANSPORT

This IBM-compatible, nine-track unit reads and writes 20,000 bytes/second at 800 bits/inch density.

LINE PRINTER

This quiet, non-impact unit is suitable for an office environment. It prints up to 136 columns at a rate of 100 to 360 lines/minute (depending on the number of columns printed). It has a 63-character set (ASCII characters).

ALPHANUMERIC/GRAPHIC CRT DISPLAY

This unit maintains over 800,000 points of flicker-free information on the display. Standard features include hardware vector and curve stroke generators, as well as a hardware character generator.

DISC MEMORY

The basic configuration disc may be expanded to a capacity of either 65,536 words or 131,072 words. Although not a peripheral device in the Model A, it merits listing here because any excess capacity beyond that taken by the program may be used for bulk storage.

APPLICATIONS

The Model A keeps pace with growing applications because of its large-scale system architecture. This means that system expansion comes later than usual and system replacement may not have to come at all — representing an important cost/performance advantage of the Model A over the typical stretched-to-the-limit small computer.

Its ability to handle a larger data base in memory makes the Model A an ideal choice for a deeper thrust into production testing, numerical control, biomedical systems, well logging, and computerized switching. Other areas include statistical analysis, information retrieval, vibration analysis, and management information systems.

SUMMARY

- Core Memory of 4096 Words, Expandable to 65,536 Words
- Disc Memory of 32,768 Words, Expandable to 131,072 Words
- Core Memory Cycle Time of 880 Nanoseconds
- Indirect Addressing
- Double Indexing
- Eight Programmable Registers
- Command Chaining
- Data Chaining
- Rapid Context Switching
- Up to 256 Nested Interrupts
- Latching Interrupts
- Double Precision Accumulator
- Only Single-Word Instructions
- Privileged Instructions
- Memory Write Protection
- Automatic Program Fragmentation
- Basic Complement of 125 Instructions
- Special Application-Oriented Instructions
- Multiple Real-Time Clocks
- Device Independent Input/Output
- Asynchronous Input/Output
- Demand Multiplexed Input/Output
- Broad Range of Peripheral Equipment
- ASR-33 in Basic Configuration

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