The Xerox 550 Computer

XEROX

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The Xerox 550 is a high-performance, real-time computer system. Its integrated hardware and software capabilities make it ideally suited for such applications as data acquisition, analysis, simulation, control, and communications.

The memory-centered architecture of the Xerox 550 computer system is responsive, flexible, and modular. Centralized system control is provided for up to 17 separate processors. Basic processors feature a microprogrammed arithmetic and logic unit. Input/output processors permit a wide range of peripherals and interfaces to operate simultaneously with computation. Use of main memory is efficiently managed by the Memory Map.

The Xerox 550 system emphasizes reliability and maintainability. Large-scale and large-board technology is used throughout. Maintainability is maximized by use of extensive error-detecting hardware and a hierarchical diagnostic system which includes microdiagnostics.

The Xerox 550 control software, the Control Program for Real Time (CP-R), takes advantage of the real-time hardware architecture to create a responsive and flexible multiprogramming, multitasking environment. Interactive, concurrent program development capabilities are also included.

In addition to a fully-integrated real-time computing capability, the Xerox 550 system includes the comprehensive customer support that has become synonymous with Xerox leadership in real-time computing.

Features

The Xerox 550 hardware architecture offers configuration flexibility and high throughput capabilities. The architecture features a multi-unit memory permitting high throughput and a multiple bus structure allowing independent processors to simultaneously access memory. The hardware architecture of the Xerox 550 system is designed to facilitate real-time responsiveness. The modularity of the architecture permits the 550 system to be optimized for each application.

The Xerox 550 Basic Processor, which includes the arithmetic and logic unit, is ideally suited for critical real-time applications. The 550 system offers computational speed and exceptional responsiveness. The instruction set, oriented for real-time requirements, is flexible and powerful, yet easy to use.

The Xerox 550 memory management capabilities optimize memory usage which makes the system very easy to use in a real-time environment. The Memory Map permits a powerful real-time multiprogramming capability, eliminating memory fragmentation problems without requiring base registers, program rebiasing, or memory repacking. Dynamic memory allocation is greatly facilitated. The 550 system also incorporates two stages of memory protection facilities.

The Xerox 550 system performs input/output transfers while the Basic Processor simultaneously satisfies real-time synchronization requirements and performs time-critical computations. Multiplexing Input/Output Processors directly interact with memory via independent memory busses. Each of these processors can support multiple peripherals. External interrupts and operator control commands are input, independently of other input/output transfers, through the centralized System Control Processor.

Many digital and analog interfacing requirements can be satisfied with the Xerox 550 system's extensive complement of systems interface units. The Xerox modular, "off-the-shelf" digital and analog capability permits satisfying most interface requirements without necessitating special hardware. Included with these interfaces are software handlers. The 550 system also features a comprehensive line of conventional peripherals, including fixed and moving head disk units, magnetic tape transports, and unit-record equipment.

The 550 control software, the Control Program for Real-Time (CP-R), optimizes the capabilities of the Xerox 550 hardware, creating a flexible environment for satisfying a wide range of real-time processing requirements. CP-R is a responsive and efficient virtual-memory, multiprogramming, multitasking control system. Included are hardware and software scheduling, task intercommunication, resource enqueing, task roll-in and roll-out, symbionts, and dynamic memory and file allocation. CP-R features interactive program development facilities permitting on-line editing, job-entry, and debugging. Processors include FORTRAN and the Assembly Program.

To maximize the availability of the Xerox 550 system, comprehensive reliability and maintainability capabilities are designed into both the hardware and software. Extensive availability features are included in the Xerox 550 hardware, the Diagnostic Programming System and CP-R. Operating within a hierarchical structure, this capability permits verification of each level of system operation before proceeding to test the next. The Xerox Remote Assist capability further enhances maintainability by permitting all diagnostic operations to be controlled remotely via a telephone connection.

When a special requirement is outside the Xerox 550 system's broad range of capabilities, Xerox will help. The Xerox Custom Systems organization will assist in defining these requirements, and in identifying and optimizing potential solutions. If requested, Xerox will also implement such solutions including hardware development, software development, software conversion, system integration, and documentation.


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Hardware

Architecture

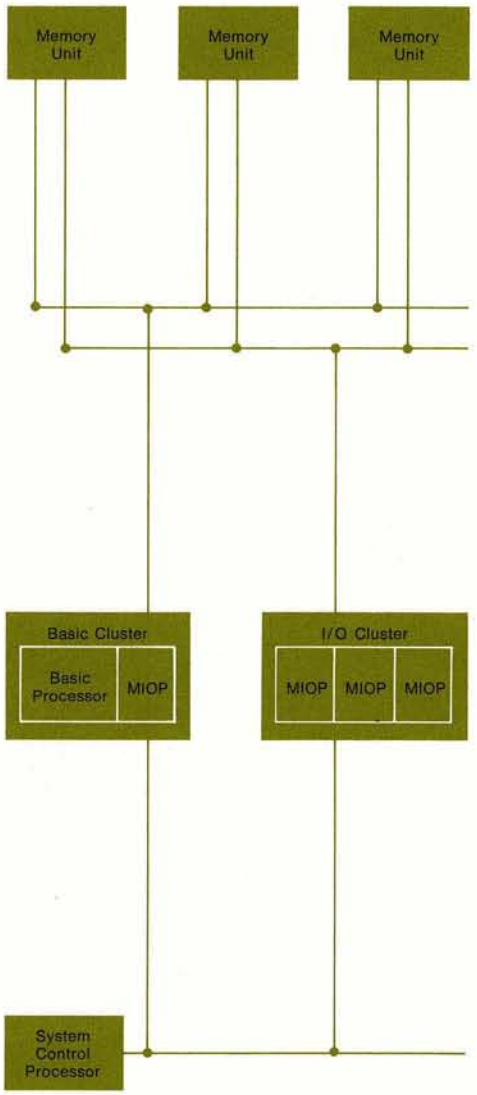
Architecture The architecture of the Xerox 550 system is both flexible and modular. Only the elements required for each application need be included in a 550 system. If these requirements subsequently change, so can the 550 configuration.

Main Memory Main Memory is divided into units, each of which may be accessed simultaneously. This overlap greatly increases total memory bandwidth. To automatically increase the occurrence of access overlap, unit addressing may be interleaved. The number of units and their size can be selected for the application.

Memory Bus Structure The parallel memory bus structure allows all clusters to independently access main memory. Each bus serves one cluster and has a port into each memory unit. Clusters may access different memory units simultaneously. Coincident accesses to a single unit are serviced by port priorities.

Cluster Configuration Clusters are groups of processors which are available in two standard configurations—the Basic Cluster and the I/O Cluster. The 550 Basic Cluster includes a Basic Processor and a Multiplexer Input/Output Processor (MIOP). Along with a System Control Processor, the Basic Cluster incorporates all the processor capability required for many applications. Each Input/Output Cluster permits adding up to three additional MIOPs. Processors within a cluster share the bandwidth of a single memory bus but access memory independently. Additional Basic and I/O Clusters may be configured as required by each application.

System Control Processor The System Control Processor (CP) is a centralized manager for interrupts, clocks, configuration and operator control. The optional Direct I/O Interface also is controlled by the CP. A separate processor bus provides a centralized responsive communication link between clusters and the CP. Intercommunication proceeds independently of memory operation.



System Specifications

Memory Word Size	32 bits plus 1 parity bit per 8-bit byte
Memory Cycle Time	645 nanoseconds per word (full-cycle)
Memory Size	16,384 to 262,144 words
Memory Unit Structure	1 to 8 memory units
Memory Unit Size	16,384 or 32,768 words
Interleaving	modulo 2 between memory units
Number of Busses	one per processor cluster
Number of Ports	up to 6 per memory unit
Bandwidth per I/O Processor	up to 1 million bytes/sec
Number of Processor Clusters	up to 6 per system
Types of Processor Clusters	Basic Cluster I/O Cluster
Types of Processors	Basic Processor Multiplexer I/O Processor (up to 3 per I/O Cluster) System Control Processor