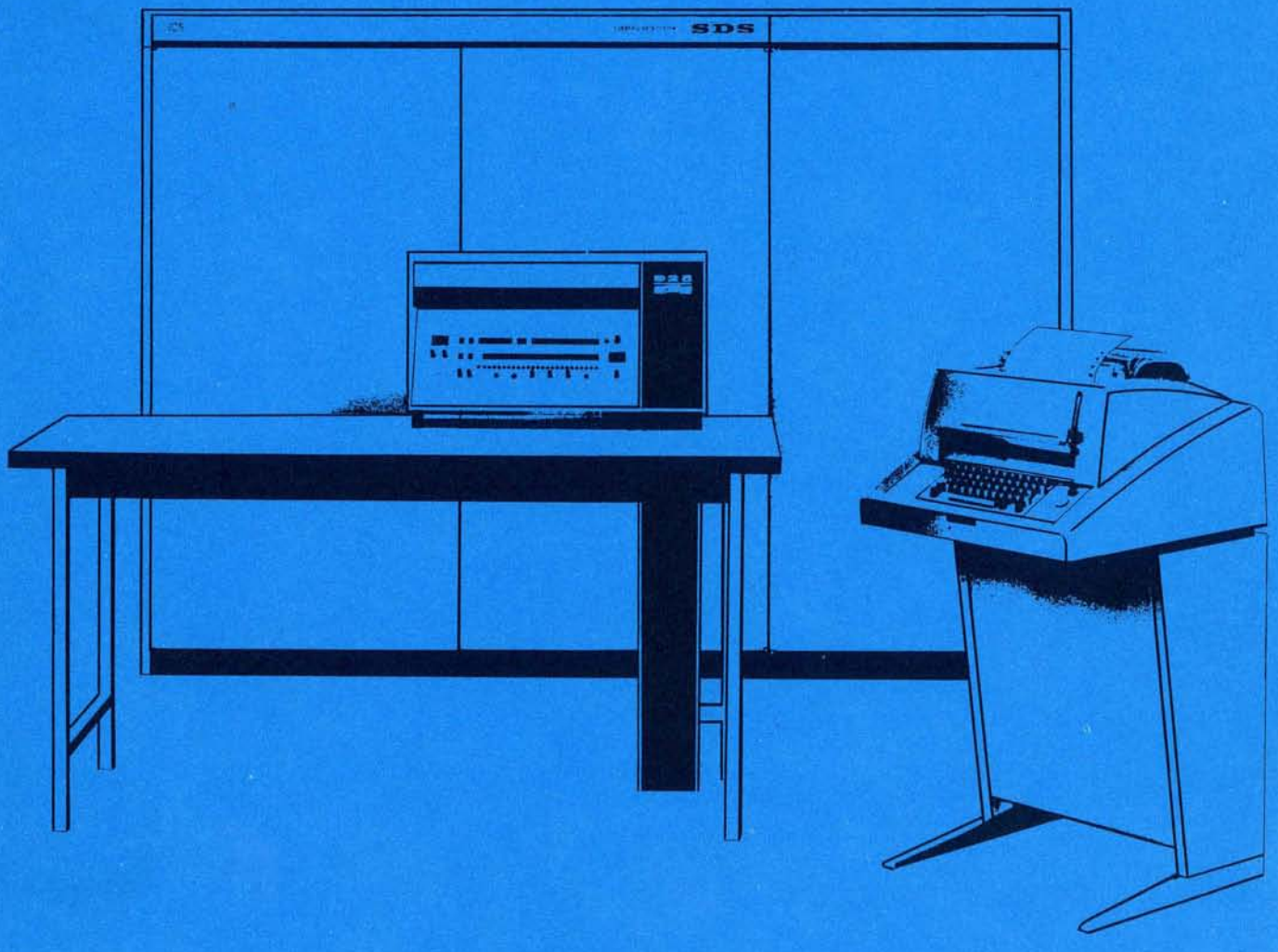
SDS 925 computer



SCIENTIFIC DATA SYSTEMS

GENERAL CHARACTERISTICS

The SDS 925 is a high-speed general purpose digital computer designed for scientific and engineering computation and for real-time systems integration. The basic price of the 925 is $81,000, including console, Model 35 Teletype Printer, Time Multiplexed Communication Channel, and 4096 words of memory.

The SDS 925 is fully compatible with SDS 900 Series computers. Because of this compatability, a complete set of field-proven software is available, and programs written for any 900 Series computer can be run on the 925 without modification. The entire line of field proven 900 Series peripherals—including SDS MAGPAK—can also be used without modification. And, like the SDS 900 Series computers, the 925 uses silicon semiconductors exclusively. Advanced SDS logical design techniques result in the use of from two to five times fewer components than conventionally designed equipment. This gives the 925 a significant reliability advantage over comparable computers.

THE SDS 925 HAS THE FOLLOWING CHARACTERISTICS:

- 24-bit word plus a parity bit
- 48-bit word for floating point arithmetic
- Hardware Index Register; indexing requires **no** additional time
- Basic memory of 4096 words, expandable to 16,384 words, **all directly addressable,** with:
  0.7 μsec access time
  1.75 μsec cycle time
- Extensive shift and register change instructions for data manipulation
- Execution times, including all access and indexing:

FIXED POINT

3.5 μsec	Add
54.25 μsec	Multiply

FLOATING POINT

(24-bit fraction, 9-bit exponent)		(39-bit fraction, 9-bit exponent)
95.5 μsec	Add	196.0 μsec
101.5 μsec	Multiply	371.0 μsec

- Automatic parity checking of all memory transfers and input/output operations
- Multiple-level indirect addressing, with indexing at any level
- Up to 4 Time Multiplexed Communication Channels, each capable of fully buffered operation at rates up to 286,000 characters per second
- Up to 4 optional Direct Access Communication Channels that operate on words or characters (6, 8, 12, or 24-bit) with a maximum transfer rate of 572,000 words per second. These Channels use a separate path to memory
- Optional Data Multiplexing System that uses the separate memory path. It can have a virtually unlimited number of independent input/output subchannels and is capable of transferring one word every 1.75 μsec
- Automatic subroutine execution with Programmed Operators
- Twenty-four-bit word parallel input/output standard, with optional block transmission at rates up to one word every 1.75 μsec. Completely independent from buffered input/output
- Up to 1024 levels of priority interrupt, each with a unique priority and address in memory. These can be individually armed and disarmed under program control
- Complete display of all programmable registers with extensive manual controls
- Four Sense Switches for console control during execution
- Up to 16,384 output control signals and input test signals
- Automatic program loading from cards, paper tape, magnetic tape, drums or discs
- FORTRAN II, REAL-TIME FORTRAN, ALGOL, SYMBOL and METASYMBOL symbolic assemblers, and MONARCH monitor routine as part of a comprehensive software package
- Low power requirements
- Memory Interlace feature that permits the input/output of large blocks of data without interrupting the main program

SDS 925 INSTRUCTIONS

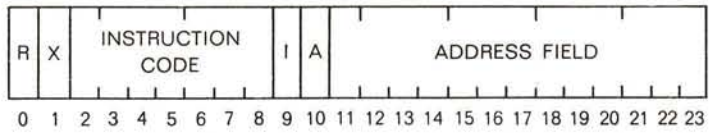
The SDS 925 has an instruction list with indexing and addressing capabilities that exceed most medium-scale computers. The 24-bit word length of the 925 holds more information per word—shorter programs, faster execution; greater precision—24-bit fixed point; 48-bit floating point; and ability to handle more data formats—3-bit octal, 4-bit decimal, 6-bit BCD.

The 925 instruction list includes: single and multiple precision arithmetic, including Memory Increment and Decrement; three logical operators (AND, OR, Exclusive OR); eight Branch instructions for decision making, including Skip if A greater than Memory and Skip if Memory Negative; a completely general shift and cycle capability of N places; register change instructions; and a complete set of input/output instructions.

The 925 provides direct addressing of up to 16,384 words of memory, as well as multiple-level indirect addressing with indexing at any level. Because a hardware index register is used, indexing adds **no** additional time to instruction execution. In indirect addressing, the computer interprets the contents of the effective address as if they constituted an instruction without an instruction code, and reinitiates address decoding. Since this is an iterative process, it can be carried to any number of levels. Each level of addressing adds one memory cycle to execution time. This multiple level capability is useful in list processing and when working with subscripted subscripts.

An SDS innovation, Programmed Operators, permits the automatic handling of up to 64 variable subroutines as if they were single, built-in instructions. These instructions are written exactly like machine instructions and can be modified by indexing and indirect addressing. This lets the programmer define his own set of 64 different instructions and provides program compatibility among all SDS 900 Series computers.

INSTRUCTION WORD FORMAT: The instruction word format for the SDS 925 is:



Bit Position	Function
0	Relative Address Bit—A "one" in this position causes the standard loading programs to add the assigned instruction location to the address field contents prior to actual storage. This bit position is not sensed by central processor decoding logic.
1	Index Register Bit—A "one" in this position causes the contents of positions 10-23 of the index register to be added to the address portion of the instruction prior to execution.
2-8	Instruction Code—The contents of these bit positions determine the operation to be performed. Bit position 2 is used with Programmed Operators and is considered part of the "tag" field (0-2).
9	Indirect Address Bit—A "one" in this position causes the computer to interpret the contents of positions 10-23 (possibly modified by indexing) as the address of the memory location where the effective address of the instruction may be found. A "zero" causes the contents of positions 10-23 (possibly modified by indexing) to be interpreted as the effective address of the instruction.
10-23	Address—The contents of these positions normally determine the memory address referenced by the instruction code.

SDS 925 INSTRUCTION LIST: Timing in the instruction list shown below is in memory cycles and includes all accessing. Indexing does not change execution time. Add one cycle for each level of indirect addressing.

INSTRUCTION		TIMING (1 CYCLE = 1.75 μSEC)
	LOAD-STORE	
LDA	LOAD A	2
STA	STORE A	3
LDB	LOAD B	2
STB	STORE B	3
LDX	LOAD INDEX	2
STX	STORE INDEX	3
	ARITHMETIC	
ADD	ADD M TO A	2
MIN	MEMORY INCREMENT	3
SUB	SUBTRACT M FROM A	2
MUS	MULTIPLY STEP	2
DIS	DIVIDE STEP	2
MDE	MEMORY DECREMENT	3
	BRANCH-SKIP	
BRU	BRANCH UNCONDITIONALLY	1
BRX	INCREMENT INDEX AND BRANCH	1, 2
BRM	MARK PLACE AND BRANCH	2
BRR	RETURN BRANCH	2
SKS	SKIP IF SIGNAL NOT SET	2, 3
SKG	SKIP IF A GREATER THAN M	2, 3
SKN	SKIP IF M NEGATIVE	2, 3
SKA	SKIP IF M AND A DO NOT COMPARE ONES	2, 3
SKS	SKIP IF A=M ON B MASK	2, 3
	LOGICAL	
ETR	EXTRACT (AND)	2
MRG	MERGE (OR)	2
EOR	EXCLUSIVE OR	2

INSTRUCTION		TIMING (1 CYCLE = 1.75 μSEC)
	REGISTER CHANGE	
CLR	CLEAR AB	1
XAB	EXCHANGE A AND B	1
BAC	COPY B INTO A, CLEAR B	1
ABC	COPY A INTO B, CLEAR A	1
	SHIFT	
RSH	RIGHT SHIFT AB	2+N
RCY	RIGHT CYCLE AB	2+N
LSH	LEFT SHIFT AB	2+N
LCY	LEFT CYCLE AB	2+N
NOD	NORMALIZE AND DECREMENT X	2+N
	CONTROL	
HLT	HALT	1
NOP	NO OPERATION	1
EXU	EXECUTE	1
EAX	COPY EFFECTIVE ADDRESS INTO INDEX REGISTER	2
	INPUT/OUTPUT	
MIW	M INTO W BUFFER WHEN READY	2+wait
WIM	W BUFFER INTO M WHEN READY	3+wait
MIY	M INTO Y BUFFER WHEN READY	2+wait
YIM	Y BUFFER INTO M WHEN READY	3+wait
EOM	ENERGIZE OUTPUT M	1
EOD	ENERGIZE OUTPUT TO DIRECT ACCESS CHANNEL	1
POT	PARALLEL OUTPUT	3+wait
PIN	PARALLEL INPUT	4+wait
BPO	BLOCK PARALLEL OUTPUT	3+N+wait
BPI	BLOCK PARALLEL INPUT	4+N+wait

SDS 925 INPUT/OUTPUT

The SDS 925 has unusually fast and flexible input/output capabilities that offer the user a wide choice of operating modes and permit easy integration into real-time systems. The complete line of proven SDS 900 Series peripheral equipment and all SDS systems components (multiplexers, A/D and D/A converters, etc.) are available for use with the 925.

TIME MULTIPLEXED COMMUNICATION CHANNELS: The SDS 925 includes as standard equipment a character-oriented, buffered Time Multiplexed Communication Channel (TMCC). This channel, called the W Channel, processes 6-bit plus parity characters under program control. Parity checking and generation and word assembly and disassembly are automatic. The programmer can specify a format of 1, 2, 3, or 4 characters per word. Input/Output is time-multiplexed with computation, so that computation continues except when information is actually transferred between the buffer and memory. The transfer of each word requires two memory cycles (3.5 μsec).

An optional Memory Interlace feature is available with the W channel that permits the input/output of large blocks of data, without interrupting the main program, at the maximum rate of 572,000 characters per second. Using interlace, the program specifies the address of the first word and the number of words to be transferred. The actual transfer is then controlled by the interlace; an interrupt to the main program does not occur until the last word has been processed.

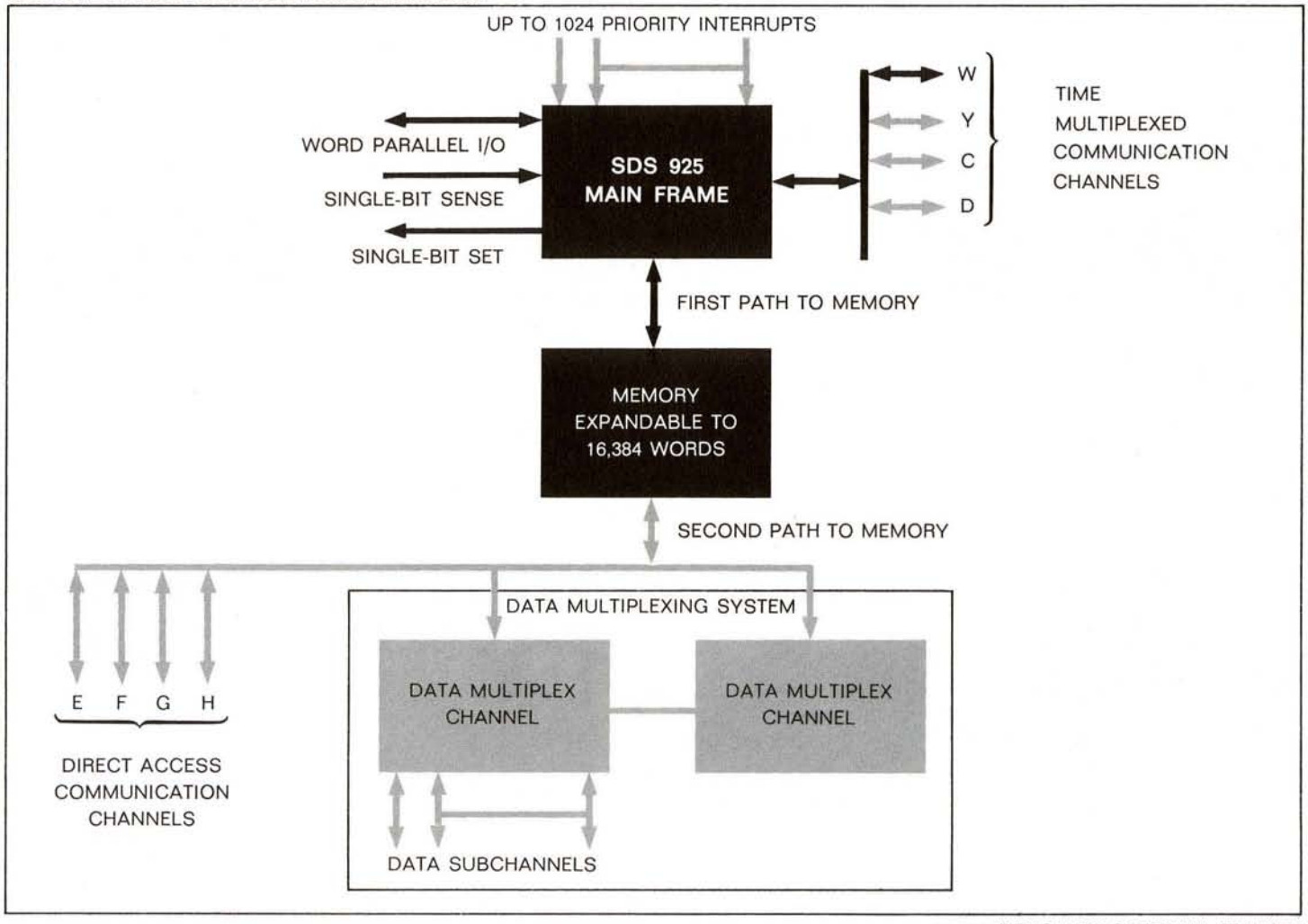
Three additional TMCC's (channels Y, C, and D) can be added to the 925. The Y Channel, like the W Channel, is available with or without the interlace feature; interlace is required with the C and D Channels.

All four TMCC's can be optionally extended to accept 6 and 12-bit characters, or 6, 12, and 24-bit characters. The external device specifies the character size. This option lets one channel handle several devices, with each device supplying data in the size most convenient for it.

WORD PARALLEL INPUT/OUTPUT: Parallel input/output of full 24-bit words under program control can take place simultaneously with input/output operations on the Time Multiplexed Communication Channels, or on the optional Direct Access Communication Channels or Data Multiplexing System. Standard instructions place the information from 24 input lines into a specified memory location, or vice-versa, without disturbing any operating registers. If the data consists of a block of words, an optional feature permits block transmission at rates up to 572,000 words per second.

SINGLE BIT CONTROL AND SENSE: Two instructions provide for single-bit ON/OFF control signals. The first, EOM, transmits a control signal and a 14-bit address to an external device or a function within the computer such as Interrupt Enable. The second, SKS, selects an external device or computer function

SDS 925 OVERALL COMPUTER CONFIGURATION



and skips in response to a false signal. Up to 16,384 control signals can be sent, and 16,384 input signals tested.

PRIORITY INTERRUPTS (OPTIONAL): Up to 1024 channels of priority interrupt are available with the SDS 925. Each of these channels has a unique priority and address in memory, and each can be selectively armed or disarmed under program control. The computer always processes the highest active interrupt, interrupting one of lower priority if necessary, and returns to the interrupted main program when all interrupts have been processed. This interrupt capability enables the computer to control or be controlled by its external environment and it permits time-independent programming in which various external stimuli are processed in order of their importance rather than the order in which they occur.

DIRECT ACCESS COMMUNICATION CHANNELS (OPTIONAL): Up to four Direct Access Communication Channels (DACC's) can be attached to the 925. These channels (E, F, G, and H) transmit information to and from the memory of the 925 over a separate path from that used by the computer proper and the standard I/O systems. This second path has priority over the first path and can transmit data in either direction at the rate of one word every 1.75 μsec. The DACC's operate on either words or characters, at the option of the programmer. All DACC's accept 6, 8, 12, and 24-bit characters, as specified by an external device. In all other respects, these channels are identical with the TMCC's.

Each DACC includes a Memory Interface Connection that accepts, from an external source, memory control addresses for information to be read into or from memory, thus permitting I/O operations to be controlled by an external system rather than the computer. This feature is also available as a separate option on any SDS 925.

DATA MULTIPLEXING SYSTEM (OPTIONAL): A Data Multiplexing System that uses the second path to memory is also available with the SDS 925. The structure of the Data Multiplexing System permits the connection of an unlimited number of Data Multiplex Channels, each of which can operate with an unlimited number of Data Subchannels. The system permits priorities to be assigned to each Data Multiplex Channel and to each Data Subchannel.

Either internal or external interlace can be used. If internal interlace is used, the interlace words (memory location and word count) are stored in memory and accessed each time a given subchannel transmits information. If external interlace is used, the identical information is held in an external register. With internal interlace, information can be transferred at a maximum rate of one word every 8.75 μsec—with external interlace the transfer rate is increased to one word every 1.75 μsec.

Two types of Data Subchannels are available. The first, the DSC-I, provides multiple I/O channels for standard SDS peripheral equipment. It contains a character assembly/disassembly register that operates on either one or two 6-bit characters or directly on 12-bit words. The second, the DSC-II accepts only 24-bit information and has no internal storage. It is provided to operate on high-speed data where the transmitting and receiving devices provide storage.

SDS 925 PERIPHERAL EQUIPMENT

The complete line of field-proven SDS 900 Series peripheral equipment is available for use with the SDS 925. Each unit is controlled by its own coupling electronics and requires no interfacing.

This equipment includes SDS MAGPAK, a low-cost magnetic tape system that consists of two independent tape drives, each of which controls a tape cartridge holding approximately 600 feet of mylar base tape. With two independent information tracks on each tape, a single MAGPAK provides a total of four data channels. Each of these channels has a capacity of approximately 1.5 million 6-bit characters. Transfer rate is in excess of 1000 characters/second. MAGPAK provides all of the operational functions of standard SDS high-performance IBM compatible tape units and uses the same instruction list. As a result, programs written for MAGPAK and those written for standard magnetic tape units are **identical.**

Other available equipment includes:

- Paper Tape I/O Equipment
- High and low speed Card Readers
- High and low speed Card Punches
- High, medium, low speed Line Printers
- High, medium, low speed Magnetic Tape Units
- Magnetic Drums
- Magnetic Disc Files
- Digital Plotters
- Display Scopes
- Data Communications Equipment

PAPER TAPE CART with 300 cps Reader, 60 cps Punch, and Spooler

CARD READER, 100 cards/min.

CARD READER, 800 cards/min.

LINE PRINTER, 600 lines/min., 132 characters/line, 64 printable characters.

SDS 925 SOFTWARE

The SDS 925 software package provides comprehensive, modular programming systems that take full advantage of the hardware capabilities of the computer. These capabilities include multiple-level indirect addressing with indexing at any level, one-cycle inter-register transfers, and automatic interpretation of subroutines. In addition to the programming systems described below, a large library of programs covering a variety of real-time applications and mathematical functions (such as matrix inversion) is available to the SDS 925 user. Through Programmed Operators, complete program compatability exists between the SDS 925 and all SDS 900 Series computers. The components of the standard SDS 925 software package include:

FORTRAN II: SDS FORTRAN II represents a major breakthrough in the field of automatic programming. Using recursive techniques, SDS FORTRAN II combines great speed, flexibility, and efficient object code, even in SDS 925 computer systems with only 4096 words of memory. Although it features multilevel n-dimensional subscripting, mixed mode expressions, and "backward" DO-loops, the compiler occupies only 2500 memory locations. It allows over 200 variables, labels, etc., and compiles more than 300 statements per minute. Where possible, complete syntactic generality is permitted, with the result that the SDS FORTRAN II language is a superset of most FORTRAN II languages, even large-scale ones.

REAL-TIME FORTRAN II: SDS REAL-TIME FORTRAN II is an expanded version of the proven SDS FORTRAN II that enables the SDS 925 to operate efficiently in real-time applications. In such an application, the 925 must react to and communicate with external devices within a time interval that is usually externally specified. To accomplish this, REAL-TIME FORTRAN II includes provisions for: generation of fast, efficient object code; special statements for convenient data manipulation; additional syntax for efficient handling of system input/output devices and formats.

SYMBOL: This two-pass assembly program provides for input of symbolic programs from typewriter, paper tape, cards, or magnetic tape. In addition to translating standard SDS 925 instruction mnemonics and symbolic expressions, SYMBOL recognizes a variety of generative and non-generative directives that aid the user in coding and debugging his programs. Compatible with other 900 Series software components, SYMBOL also includes the capability to assemble machine-language FORTRAN subroutines.

META-SYMBOL: This advanced symbolic processor brings compiler-level capability to the machine-language programmer. A superset of SYMBOL, the META-SYMBOL language includes general expressions, which may consist of one or more (list) items combined by arithmetic and/or Boolean operators. META-SYMBOL also has Function and Procedure capability, which permits the programmer to code in a high level, machine-independent language. Operationally, the assembler consists of an Encoder and a Translator. The Encoder compresses the input language to a fraction of its original size before it is processed by the Translator. The Translator allows source langauge modification with optional recovery of the resultant updated source code.

ALGOL: SDS ALGOL is a scientifically-oriented symbolic programming langauge that is available in two systems, one requiring only 4096 words of memory, and the other requiring 8192 words of memory and one magnetic tape unit. Both systems include a Compiler, a Loader/Executor, and a Library consisting of common input/output and mathematical function subroutines. Basic SDS ALGOL is comparable to SDS FORTRAN II with respect to speed (up to 250 statements per minute) and space requirements.

HELP: The HELP Utility Programming System aids the small-machine user in the checkout and operation of machine language programs. HELP is completely modular so that the programmer need load only applicable parts. The entire HELP system can be loaded in less than 1800 memory locations.

USERS GROUP: All SDS computer users are eligible to join the SDS Users' Group. This dynamic group provides a meeting ground for its many active members to review and exchange ideas, as well as a rapidly growing library of programs.

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